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Modular Multilevel Converter for Electric Motor Drive Applications

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Problem Description

Modular multilevel converters face challenges when operating at the low frequencies associated with electric motor drives. The aim of the master thesis is to present measures to mitigate the low frequency challenges, and to test some of the measures using simulations.

Preface

This report is the result of a master thesis on the topic of Modular Multilevel Converters. The master thesis is the final product of the Energy and Environmental Engineering masters programme at NTNU. The thesis was written during the last semester of the 2014-15 school year, and was continuation of the project thesis written during the first semester of the 2014-15 school year.

I would like to thank my supervisor Prof. Lars Norum for his guidance, especially when the scope of the thesis was developed. I would also like to thank Mr. Hamed Nademi who has been of great help when working with the simulation model.

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Bertil Lassesen Ekern

Abstract

In this master thesis the topic of Modular Multilevel Converters (MMC) has been studied. The working principle of the converter is presented with advantageous attributes such as a multilevel waveform, a modular realization and cost saving features. Vital control objectives are active and reactive power control, DC link voltage control, submodule capacitor voltage control and current control. A level-shifted pulse-width modulation (PWM) switching scheme was found to have relatively low total harmonic distortion (THD), thus used in the upcoming simulations. In order to ensure balancing of the converter capacitors, a voltage balancing algorithm was presented, sorting the capacitors based on their voltage level, and giving a state command accordingly. The thesis has examined the challenges of using MMC for electric motor drive applications. It has been found that the low frequency operation causes large voltage ripple in the capacitors, thus a large circulating current. Through a literature search, different measures where found in order to reduce the circulating current, including circulating current suppressing and manipulation. In addition an introduction of a common mode voltage was presented as a possible measure.

After developing the one-phase model of the project thesis into a three-phase model, the circulating current suppressing controllers (CCSC) were tested, first at $50Hz$, and then at $25Hz$. At $50Hz$, all three controllers worked as intended, reducing the circulating current by up to 72% and the voltage ripple was reduced from $\Delta v_c = 10V$ to $\Delta v_c = 6V$. At $25Hz$, all the controllers maintained their ability to reduce the circulating current. Nonetheless, it was concluded that further measures must be studied, as all controllers increased the capacitor voltage ripple at $f = 25Hz$.

Sammendrag

Denne masteroppgaven tar for seg temaet MMC, hvilket er en flernivå omformer. Oppgaven har presentert omformerens virkemåte, samt gunstige egenskaper som en flernivå bølgeform, en modulær oppbygning og kostnadsbesparende forhold. Aktiv- og reaktiv effektkontroll, DC-bro spenningskontroll, submodul kondensator spenningskontroll og strømkontroll har alle blitt beskrevet som viktige kontrolloppgaver. For å sikre korrekt veksling av omformerens brytere, ble en puls-bredde modulasjon basert på skifte av nivåer valgt. Denne teknikken sikrer at de harmoniske svingningene holder seg relativt lave, sammenlignet med andre puls-bredde modulasjonsteknikker. Velbalanserte submodulkondensatorer er viktig, og det ble derfor valgt en sorteringsalgoritme der spenningsverdiene ble sortert for deretter å gi et tilstandssignal til submodulen basert på plasseringen i den sorterte listen. Masteroppgaven har fokusert på MMC i tilknytning til anvendelser innenfor elektriske motordrifter. Det ble konkludert med at en MMC vil støte på problemer med de lave frekvensene påkrevd i motordrifter. Dette ettersom kondensator spenningsvariasjonen er omvendt proporsjonal med frekvensen på AC-siden av omformeren. Lave frekvenser vil dermed gi store spenningsvariasjoner i kondensatorene. De store spenningsvariasjonene skaper også grobunn for strømmer som sirkulerer innad i omformeren. Gjennom et litteraturstudie ble det funnet ulike tiltak for reduksjon av disse sirkulerende strømmene. Tiltakene innebar ulike former for fordelaktig forming av den sirkulerende strømmen, samt å dempe de sirkulerende strømmene så mye som mulig. I tillegg vil det å innføre et felles spenningsnivå blant fasene kalt common mode spenning kunne bidre til å øke omformerens evne til å takle lave frekvenser.

Etter å ha videreutviklet enfasemodellen fra prosjektoppgaven til å bli en trefasemodell, ble tre ulike tiltak testet for å minimere den sirkulerende strømmen i omformeren. Alle tre reduserte spenningsvariasjonen i kondensatorene fra $10V$ til $6V$, i tillegg til at den sirkulerende strømmen ble redusert med opp mot 72%. Under testing utført på halvparten av nominell frekvens viste det seg at kontrollerne opprettholdt sin evne til å redusere den sirkulerende strømmen. Det ble likevel konkludert med at ytterligere tiltak må bli sett nærmere på, ettersom alle tre kontrollerne økte spenningsvariasjonen i kondensatorene ved halvparten av nominell frekvens.

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Chapter 1

Introduction

1.1 Background

Modular Multilevel Converter (MMC) is a technology introduced in 2001 as a solution to some of the demands of a future power system. Decentralized power generation, combined with a deregulated international energy market, will increase the need for advanced power electronic systems [8]. The MMC technology offers several advantages compared to conventional voltage sourced converters (VSC), but it is also a more complex technology, demanding a more comprehensive control system. The attention for MMC is increasing and its first commercial application, the Trans Bay Cable in the US, was installed in 2012. The high-voltage direct current (HVDC) MMC had a rated power of 400MW and a 200kV DC-link [9]. Recently, the MMC has also gained interest for applications in the medium-voltage range, like medium-voltage high power motor drives [10]. However, for motor drives applications, measures are needed to ensure stability even during low-speed operations [11].

1.2 Objectives

The aim of this master thesis is to continue the work of the project thesis. Thus some parts of the project thesis are reproduced in this master thesis. The focus area of the report is MMC for electric motor drive applications. A literature search will therefore be conducted in order to enlighten challenges and possible solutions to the challenges. In addition, a simulation model will be developed in order to test the theory of the proposed solutions.

Chapter 2

Modular Multilevel Converter

2.1 Working Principle

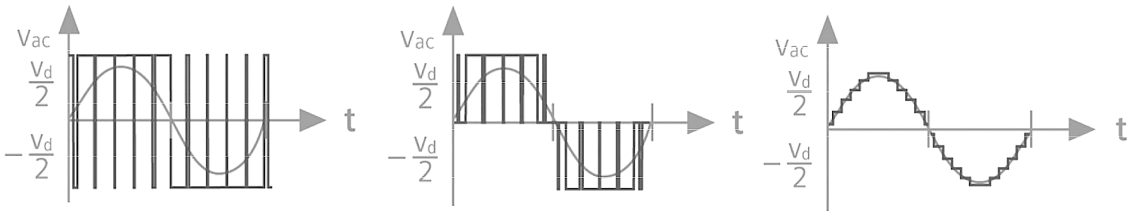
Voltage sourced converters can build up a three-phase AC voltage via a DC-voltage. It uses semiconductors such as IBGTs with turn-off capabilities in order to control the DC-voltage into a sinusoidal behavior [3]. The most common types are two or three level technologies, with two and three voltage levels respectively. The IGBT switching scheme ensures a sinusoidal average output, however as illustrated by figure 2.1a and 2.1b, the voltage steps are steep, thus creating an extensive filtering need [3]. The multilevel converter output in figure 2.1c shows how small increments builds a sinusoidal output without similar filtering needs.

MMC is a multilevel converter topology introduced by A. Lesnicar and R. Marquardt. [8] presents some of the advantageous features of an MMC:

Modular Realization A converter built up by modules can easily be scaled to different voltage- and power levels

Multilevel waveform The converter can be expanded to any number of voltage steps. A high number of voltage steps reduce the harmonic distortions.

High availability The use of well-known components together with the possibility for redundancy, minimizes the downtime.



(a) 2-level (b) 3-level (c) multilevel

Figure 2.1: VSC Output Voltages [3]

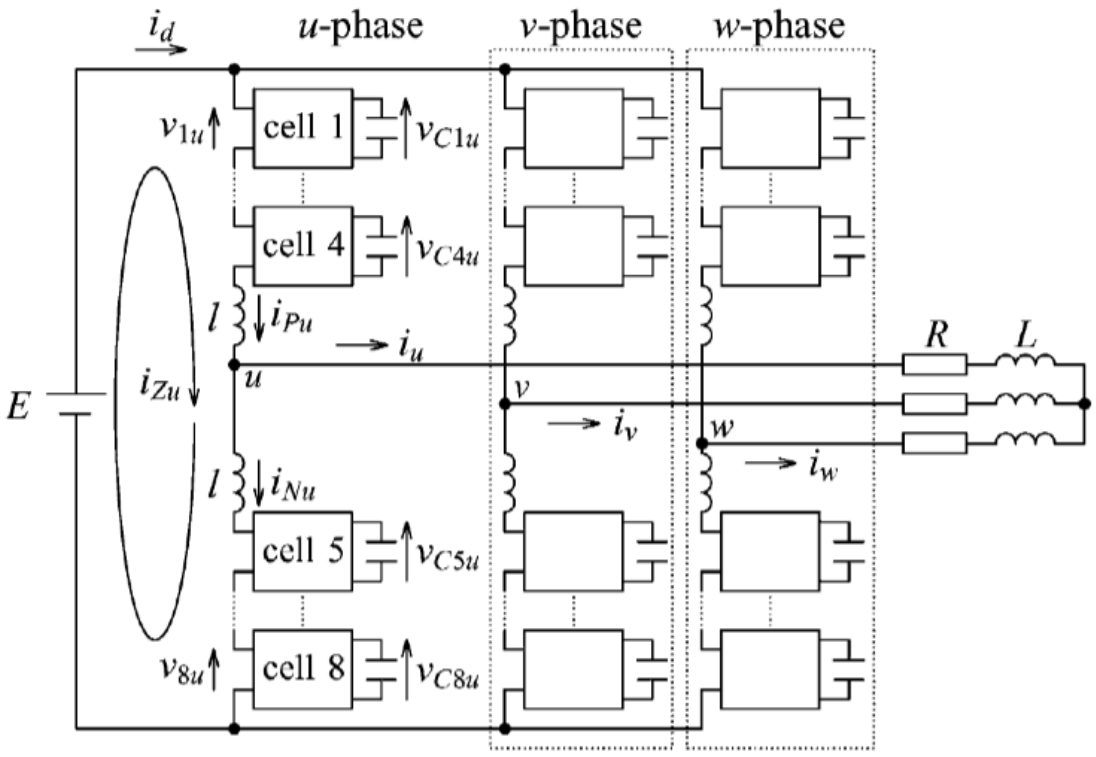


Figure 2.2: Structure of a three-phase double-star-configured Modular Multilevel Converter [4]

Failure management The converter can continue to operate, even though some of components experience failure.

Investment and life cycle cost A modular construction, combined with the use of standard components reduces the investment and life cycle cost.

A configuration of an MMC is illustrated in figure 2.2. The MMC consists of three legs, each representing one phase. Each leg consists of an upper and a lower stack of cells, called arms. A cell, also called submodule, can for ease be considered as a controllable DC voltage source. By switching the submodules on and off at the right time, the voltage can be built up stepwise, producing a sinusoidally shaped output. The number of steps can reach high numbers; the converter in the Trans Bay Cable project mentioned in chapter 1.1 had 216 submodules in each arm [9].

There are multiple ways of connecting the different phases of the MMC. The MMC-structure studied in this report, is the double-star configuration of figure 2.2. Motor drive applications favors MMC-configurations where both AC to DC and DC to AC conversion are supported, thus the double-star configuration is a suitable configuration [4]. There are multiple submodule technologies available. The most popular submodule technology is the half-bridge submodule with only two switches, resulting in fewer components and higher efficiency [5]. The discussions and derivations hereafter will be based on an MMC with half-bridge submodules.

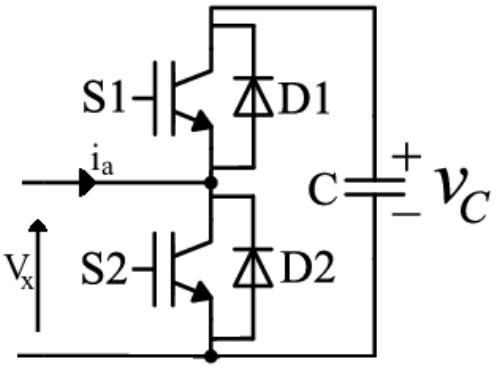


Figure 2.3: Halv-bridge submodule, [5]

The half-bridge submodule in figure 2.3 has several control states, dependent of the different switching states and the direction of the current through the submodule. Table 2.1 shows the different control states. When IGBT S1 is switched on and S2 is switched off, the voltage, v_c of the capacitor, C, is applied to the submodule terminals. A positive current, i_a, will charge the capacitor, while a negative i_a will discharge the capacitor. When S1 is turned off and S2 is turned on, the capacitor, C, is bypassed, making sure the terminal voltage, V_x is zero. In addition, it is possible to switch off both IGBTs. This will not happen under normal operation, but the submodules will be in this state at the moment when the MMC is connected to the system. This state will also be activated if a serious failure occurs [3]. Turning off both S1 and S2 will in the case of a positive current, i_a, charge the capacitor, C, while a negative i_a will bypass the capacitor. An additional switch is often implemented, bypassing and fully isolating the cell if needed for fault tolerant operation [12].

State	**S1**	**S2**	$\mathbf{i_a}$	$\mathbf{V_x}$	$\frac{\mathbf{dVc}}{\mathbf{dt}}$
1	on	off	>0	v_c	>0
2	on	off	<0	v_c	<0
3	off	on	>0	0	0
4	off	on	<0	0	0

Table 2.1: Submodule control states, [8]

2.2 Mathematical Model

From figure 2.2 and following Kirchhoff´s voltage law, the DC supply voltage, E, can be expressed by the following equation [4]:

$$E = \sum_{h=1}^{2n} v_{hj} + l\frac{d}{dt}(i_{Pj} + i_{Nj}) \tag{2.1}$$

Here v_{hj} means the output voltage of the h^{th} submodule in phase j, i_{Pj} means the positive

arm current, i.e. the upper arm current, while i_{Nj} denotes the negative arm current, i.e. the lower arm current. The summation is from 1 to 2n, where n is the number of submodules in each arm, hence all submodule voltages are added.

Based on the same principles, the relationship between the DC and AC side of the converter can be expressed as [1]:

$$\frac{E}{2} = \sum_{h=1}^{n} v_{hj} + l\frac{d}{dt} i_{Pj} + V_{load} \tag{2.2a}$$

$$\frac{E}{2} = \sum_{h=n+1}^{2n} v_{hj} + l\frac{d}{dt} i_{Nj} - V_{load} \tag{2.2b}$$

Equation 2.2a and 2.2b differs by the summation from 1 to n and (n+1) to 2n, representing the upper and lower arm, respectively. V_{load} represents the voltage drop over the load, which in figure 2.2 is illustrated by an RL load.

The phase-j current, i_j, is given by equation 2.3a and the upper and lower arm currents are given by equation 2.3b and 2.3c respectively [2]. I_{Zj} represents the circulating current in phase j.

$$i_j = i_{Pj} - i_{Nj} \tag{2.3a}$$

$$i_{Pj} = i_{Zj} + \frac{i_j}{2} \tag{2.3b}$$

$$i_{Nj} = i_{Zj} - \frac{i_j}{2} \tag{2.3c}$$

The voltage driving i_j, is the inner emf of the phase, e_j, and is given by equation 2.4 [2].

$$e_j = \frac{v_{Pj} - v_{Nj}}{2} \tag{2.4}$$

The voltage driving the circulating current, v_{Zj} is given by [7]:

$$v_{Zj} = \frac{E - (v_P + v_N)}{2} \tag{2.5}$$

From equation 2.3, the equation for circulating current, i_{Zj}, can be developed [5]:

$$i_{Zj} = \frac{i_{Pj} + i_{Nj}}{2} \tag{2.6}$$

Tu et al. [2] states that the source of the circulating current is the differences within each converter leg. The circulating current has a frequency twice the fundamental frequency and is in negative sequence form [2]. The circulating current causes a higher RMS-value of the arm currents, thus increasing the losses in the converter. It will also influence the distribution of both voltage and losses [13]. The second harmonic behavior of the circulating current can be

described by [2]:

$$i_{Zj_2} = I_{2f} sin(2\omega_0 t + \varphi_0) \tag{2.7}$$

Here I_{2f} is the amplitude of the double line-frequency circulating current, ω_0 is the fundamental frequency and φ_0 is the initial phase angle.

Based on equation 2.3 and 2.7 it can be stated that the arm current has three main frequency components: Zero frequency DC-current, fundamental frequency AC-current and two times the fundamental frequency circulating current [1].

The dynamics of the capacitor ripple is expressed by [5]:

$$\frac{dv_{CPj}}{dt} = \frac{i_{Pj}}{nC} x_{Pj} = \frac{1}{nC}\left(\frac{i_d}{3} + i_{Zu} + \frac{i_j}{2}\right) x_{Pj} \tag{2.8a}$$

$$\frac{dv_{CNj}}{dt} = \frac{i_{Nj}}{nC} x_{Nj} = \frac{1}{nC}\left(\frac{i_d}{3} + i_{Zj} - \frac{i_j}{2}\right) x_{Nj} \tag{2.8b}$$

where x_{Pj} and x_{Nj} are the number of submodules inserted in the upper and lower arm respectively.

2.3 Control Scheme

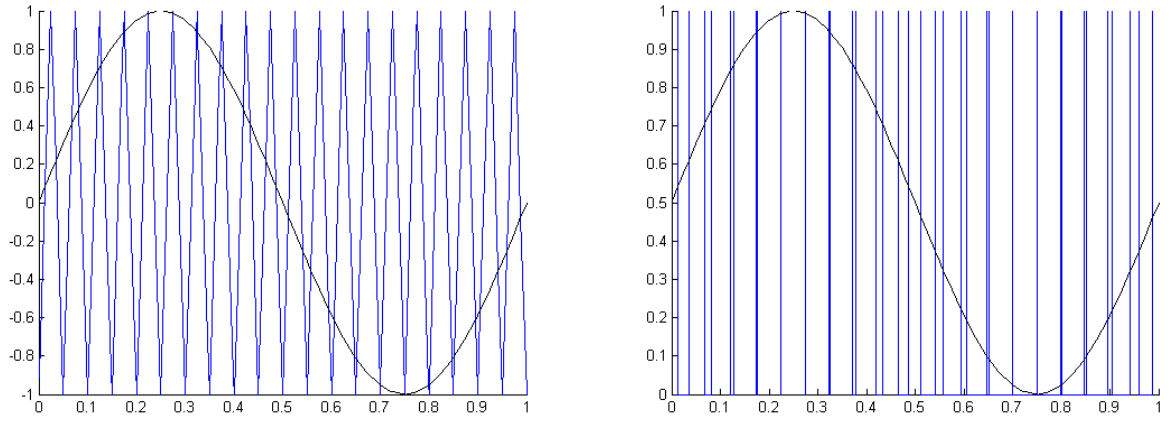
2.3.1 Control Objectives

Several different control loops are needed to ensure a desired operation of the MMC. Li et al. [14] lists four types of required control objectives:

- Control the active power in addition to either reactive power or AC voltage.
- Control of the DC link voltage
- Control of the SM capacitors, in terms of both average value and voltage balancing.
- Control of current, where elimination of both circulating currents and zero sequence current should be the desired outcome.

To control the active and reactive power, a dq control similar to conventional VSC dq control can be applied [14]. The dq control decomposes the active and reactive power, so that it can be controlled by the d-axis current and the q-axis current respectively [15]. Unlike in a conventional VSC, there is no DC-link capacitor in an MMC. Therefore, the DC link voltage is controlled by controlling the submodule voltages [14].

The arm current loop should make sure the upper and lower arm currents contribute equally to the output current. The zero-sequence current, I_0, can be eliminated by controlling the current in the positive and negative DC-link to be equal [14]. The average submodule capacitor voltage level can be controlled by controlling the stored energy. If the voltage level is too high,



(a) Triangular carrier

(b) Switching signals

Figure 2.4: Principle of PWM switching scheme

the control system should make sure more power is fed out of the converter than what is fed into the converter. The stored energy in the capacitors will therefore decrease, thus reducing the capacitor voltage [14]. In order to balance the individual capacitor voltage levels within an arm, Lesnicar and Marquardt [8] suggests to periodically measure the capacitor voltage levels. Based on these measurements the capacitors with the lowest voltages will be prioritized in terms of charging time in case of a positive arm current. When opposed to a negative arm current, the capacitors with the lowest voltages should be given less discharging time. The opposite applies for the submodules with high voltage [14].

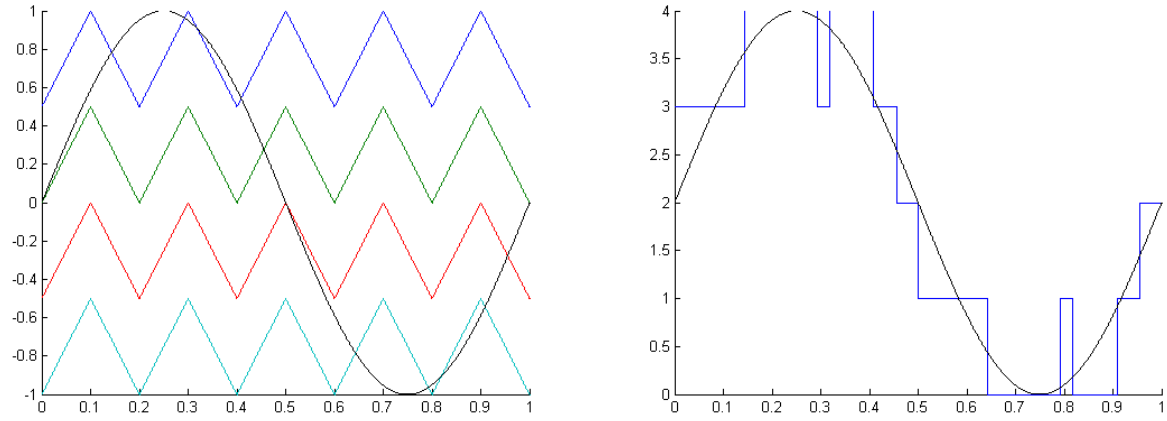
2.4 Pulse Width Modulation (PWM)

When choosing a switching scheme for a multilevel converter it is vital to consider the modular and scalable topology, favoring an easily expandable control scheme [8]. There are several types of pulse width modulation (PWM) switching schemes, with these properties. Figure 2.4a shows the principle behind a PWM switching scheme. Each time the triangular carrier crosses the sinusoidal reference signal the switch will change position, as is shown in figure 2.4b. This idea could be expanded to multiple triangular carriers, each linked to a switch.

2.4.1 Level-shifted PWM

A level-shifted PWM is shown in figure 2.5a, showing how the different switches are responsible for different parts of the sinusoidal curve. In this case, the switching scheme consists of four levels. At the top of the sinusoidal curve, all the switches will be in on-position, while at the bottom, all switches will be in off-position. The switching output is shown in figure 2.5b. A study by Rajan and Seyezhai [16] suggest that level-shifted PWM provides a better RMS load voltage

than comparable PWM switching schemes, as well as providing a low harmonic distortion. This is confirmed by Colmenares [17], explaining the difference by the relatively lower frequency needed in a level-shifted PWM.



(a) Triangular carriers, $f_{tri} = 5Hz$, $f_{sin} = 1Hz$ (b) Switching output

Figure 2.5: Level-shifted PWM switching scheme

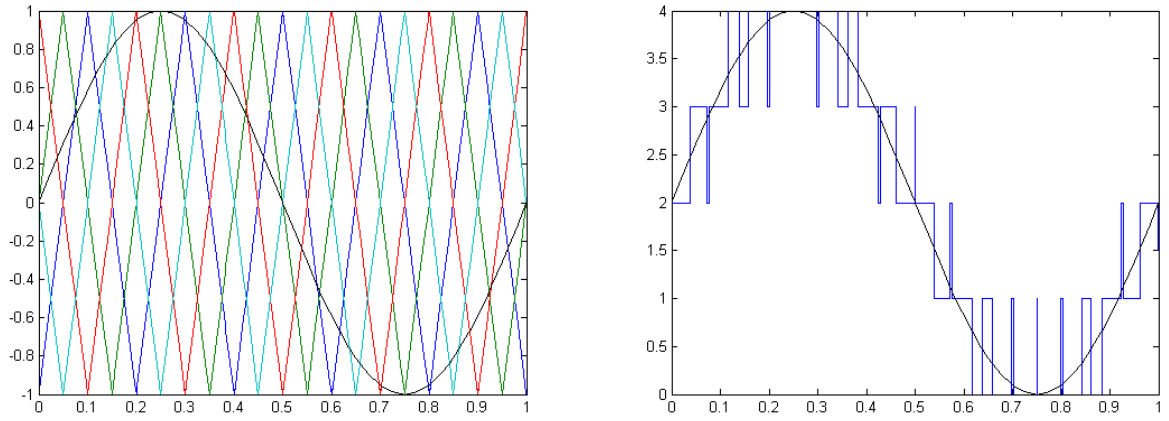
2.4.2 Phase-shifted PWM

A four carriers phase-shifted PWM is shown in figure 2.6a, where the phaseshift between the carriers is $\frac{360}{n}$. The output of the switches is seen in figure 2.6b. Unlike the level-shifted PWM, the switches can contribute in all parts of the reference signal, as all carriers can cross the reference signal at any point. Hence the phase-shifted PWM gives a better switching distribution compared to level-shifted PWM, improving the individual balancing performance [17].

2.5 Voltage Balancing

Voltage balancing of the submodule capacitors is one of the key issues of the MMC. [18] categorizes the voltage balancing methods into two: distributed methods and centralized methods. The distributed voltage balancing requires a control loop for each submodule, giving very complex system [19]. Hence the centralized voltage balancing method is studied in this thesis.

The centralized voltage balancing methods balance the capacitor voltages by choosing switching states based on the voltage level and the polarity of the current. The usual PWM method chosen for centralized voltage balancing is level-shifted PWM. Based on figure 2.5 in section 2.4, the switching states can be divided into three: switched on, switched off and PWM-switching, where PWM-switching means the state where the submodule is switched on and off rapidly [18]. After a sorting of the capacitor voltages, during a positive arm current, the



(a) Triangular carriers, $f_{tri} = 5Hz$, $f_{sin} = 1Hz$ (b) Switching output

Figure 2.6: Phase-Shifted PWM Switching Scheme

Required number of states
on: 3
off:1
pwm:1

Capacitor voltages
C1=4V
C2=6V
C3=1V
C4=3V
C5=2V

→

Sorted list
C3
C5
C4
C1
C2

→

Submodule states	
Positiv arm current	Negativ arm current
C3=on	C3=off
C5=on	C5=pwm
C4=on	C4=on
C1=pwm	C1=on
C2=off	C2=on

Figure 2.7: The principle behind the centralized capacitor voltage balancing algorithm

submodules with the lowest capacitor voltages will be switched on and the submodules with the highest voltage levels will be switched off. The submodules in between will be chosen for PWM switching. During a negative arm current, the opposite will happen. The principle behind the sorting algorithm is shown in figure 2.7

Chapter 3

Electric Motor Drives

3.1 Background

Of the total industrial electrical energy consumption, more than 65% is consumed by electric motors [20]. Traditionally, electric motors have been fixed speed motors. Given a fixed speed electric motor driving a pump, the motor will be rated to meet the maximum output of the pump. Under normal operation, the required power to the pump will be lower than the maximum power. However, as the fixed speed motor will have a constant speed, the solution is often to run the motor in an 'on-off' manner. The required power for the pump is proportional to the cube of the flow, thus a fixed-speed 'on-off' solution will require much more energy than a solution where the motor is driven at variable speed [21]. The AC motor speed can be controlled via a variable frequency drive (VFD), which is a type of variable speed drive (VSD). Figure 3.1 shows the circuit diagram of a VFD. The AC input power could for example be the national power grid or a diesel engine driven generator on a ship. The voltage is initially rectified via a rectifier. A DC bus connects the rectifier to an inverter. The output of the inverter is a controllable AC voltage, supplied to the motor. By controllable AC, it means that with proper control of the inverter, the VFD can provide an AC voltage of a desired frequency to the motor. [22] claims that full-torque operation in a variable-speed range is a common requirement for many motor drive applications, ranging from zero to base speed. High power applications sets strict requirements on the AC output power, as a distorted sinusoidal output can cause thermal problems and losses [22]. A simple two level inverter will create great filtering needs, while a higher level inverter can minimize or even eliminate the filtering needs. This is beneficial, as a filter can both be costly and bring losses to the system. Abu-Rub et al. [23] lists five factors affecting the waveforms of a medium-voltage drive:

1. The choice of converter technology
2. The application
3. The control algorithn

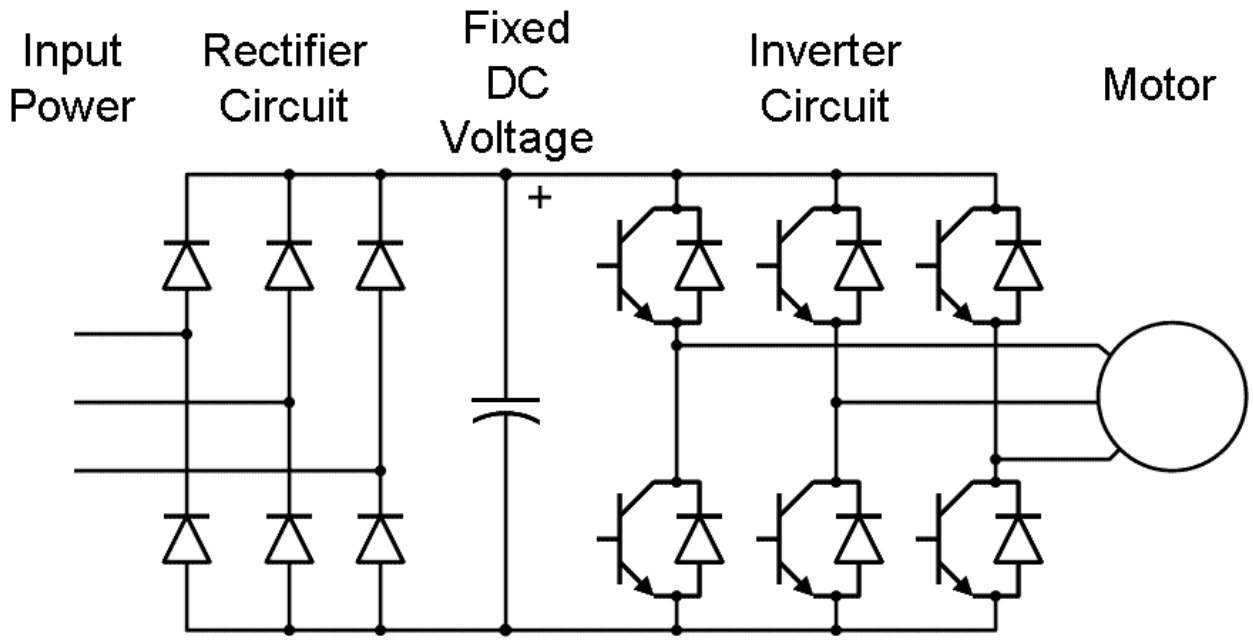


Figure 3.1: A circuit diagram of a three-phase variable frequency drive [6]

4. The choice of switching frequency
5. The size of the filter

3.2 Modular Multilevel Converter for Medium-Voltage Variable Speed Drives Applications

The MMC technology presented by Lesnicar and Marquardt [8] was originally intended for power generation and transmission applications. As discussed in chapter 3.1, high power electric motor drives have strict requirements when it comes to the output power, favoring technologies providing output with low harmonic distortion. In that respect, Antonopoulos et al. [22] states MMC as one of the most promising converter topologies. Hiller et al. [24] lists some other advantageous features of an MMC:

- Completely modular design
- Use of standard components
- Redundancy
- Scalability
- Flexible front end configuration

Hiller et al. [24] concludes that an MMC will give a compact and attractive solution, also for the medium voltage converter market.

An electric motor drive requirement mentioned in section 3.1 is that the drive should be able to operate at full torque for the whole speed range, including low speeds down to zero. As the submodule capacitor voltage variation is inversely proportional to the AC-side frequency, the low-frequency operation can lead to increased rating values of the converter, and it can also cause instability problems [11]. It is therefore by Debnath et al. [5] considered as the main challenge regarding MMC for electric motor drive applications.

Chapter 4

Circulating Current Suppression

The voltage balancing algorithm presented in section 2.5 ensures that the different submodule capacitors have an almost equal voltage level. However, the voltage levels will not be exactly the same, thus a voltage variation will occur. The voltage variation gives rise to a current circulating within the converter. The circulating current is in the negative sequence form, with a frequency of twice the fundamental frequency. It flows through the three phases of the converter without affecting the AC-side currents or voltages. However, it increases the rms-value of the arm currents, giving higher power losses in the converter. The circulating currents consist of a DC part corresponding to a third of the total DC current. Thus, the DC part of the circulating current provides the actual power transfer [2]. By increasing the size of the arm inductors, both the circulating current can be suppressed and the fault current rise rate can be limited [25]. However, as stated by Tu et al. [2], increasing the inductances is not a cost-effective solution, as there will be a large voltage drop over the inductances and the high-voltage inductors are costly. In addition, the circulating currents will not be completely removed using this method.

Hagiwara et al. [26] and Hiller et al. [24] have investigated MMC for motor drive applications down to half of nominal speed. Hiller et al. [24] concludes that the MMC technology can offer compact and attractive solutions for industrial motor drives applications. Hagiwara et al. [26] claims that the MMC is applicable for adjustable-speed motor drive of a fan/blower-like load, emphasizing the importance of further studies on low frequency behavior. Korn et al. [27] has reduced the capacitor voltage ripples by using a low frequency operating mode, where both a common-mode phase voltage and a circulating current are introduced. During the low frequency operating mode, the capacitor voltage ripples are made independent of the phase current frequency, thus the MMC is able to magnetize and start an induction machine from standstill. However, as extra circulating currents are floating in the converter, the available torque is lower than nominal [27]. Hagiwara et al. [28] suggests an injection of square wave common mode voltages and circulating currents as opposed to the sinusoidal wave injections of Korn et al. [27]. Hagiwara et al. [28] claims the square-wave method to be superior to the sinusoidal method as it drastically reduces the peak circulating current required. Compared to the injection of sinusoidal waves, which has a peak circulating current larger than the rated current, the square wave method can cut the peak circulating current by half. Reducing the peak

value of the circulating current reduces the converter loss and the inductor volume [28].

When using sinusoidal wave injections, the starting torque is very low. The square wave injection of Hagiwara et al. [28] raised the achievable starting torque to 40% of the rated value. However, it is by Antonopoulos et al. [7] claimed that by using a combination of common mode voltage and a sinusoidal circulating current, it is possible to exceed the perforance of the square wave circulating current. Antonopoulos et al. [7] divides the operation into three:

- Close to rated speed
- Intermediate speed range
- Low speed and standstill

Antonopoulos et al. [7] states that in a basic form, only the fundamental frequency output needs to be considered, while the circulating current, i_Z, needs to be dc in order to minimize resistive losses. The output current, i_j, inner emf, e_j, and circulating current, i_{Zj}, given by equation 2.3a, 2.4 and 2.6 in section 2.2 accordingly is therefore rewritten into [7]:

$$e_j = \hat{V}_j \cos(\omega_j) \tag{4.1a}$$

$$i_j = \hat{I}_j \cos(\omega_j t - \varphi) \tag{4.1b}$$

$$i_{Zj} = i_{Zj0} = \frac{\hat{V}_j \hat{I}_j \cos\varphi}{E + \sqrt{E^2 - 4R\hat{V}_j \hat{I}_j \cos\varphi}} \approx \frac{\hat{V}_j \hat{I}_j \cos\varphi}{2E} \tag{4.1c}$$

where ω_j is the stator angular frequency, ϕ is the power angle, E is the pole-to-pole dc bus voltage and R is the arm resistance.

With E being a constant quantity, the power delivered to the arm capacitors is given by [7]:

$$p_{Pj} = i_{Pj} v_{Pj} = \left(\frac{i_j}{2} + i_{c0}\right) \cdot \left(\frac{E}{2} - v_s - R i_{c0}\right) \tag{4.2a}$$

$$p_{Nj} = i_{Nj} v_{Nj} = \left(-\frac{i_j}{2} + i_{c0}\right) \cdot \left(\frac{E}{2} + v_s - R i_{c0}\right) \tag{4.2b}$$

The energy stored in the arms can be calculated by integrating the power delivered to the arm capacitors [7]:

$$W_{cP}^{\Sigma} = W_{cP0}^{\Sigma} - \frac{\hat{V}_j i_{c0} \sin\omega_j t}{\omega_j} + \frac{\left(\frac{E}{2} - R i_{c0}\right)\hat{I}_j \sin(\omega_j t - \varphi)}{2\omega_j} - \frac{\hat{V}_j \hat{I}_j \sin(2\omega_j t - \varphi)}{8\omega_j} \tag{4.3a}$$

$$W_{cN}^{\Sigma} = W_{cN0}^{\Sigma} + \frac{\hat{V}_j i_{c0} \sin\omega_j t}{\omega_j} - \underbrace{\frac{\left(\frac{E}{2} - R i_{c0}\right)\hat{I}_j \sin(\omega_j t - \varphi)}{2\omega_j}}_{\hat{I}_j/\omega_j - term} - \frac{\hat{V}_j \hat{I}_j \sin(2\omega_j t - \varphi)}{8\omega_j} \tag{4.3b}$$

Here, W_{cP0}^{Σ} and W_{cN0}^{Σ} are integration constants of the energy variation, which can be chosen arbitrarily. The constants can be used as a reference for the total arm average energy. The fact that they can be chosen freely, adds a degree of freedom [29].

The expression for the energy stored in the arms can be used to calculate the total capacitor voltage in the arms [7]:

$$v_{cP}^{\Sigma} = \sqrt{\frac{2nW_{cP}^{\Sigma}}{C}} \tag{4.4a}$$

$$v_{cN}^{\Sigma} = \sqrt{\frac{2nW_{cN}^{\Sigma}}{C}} \tag{4.4b}$$

, where n is the total number of submodules per arm.

The inserted arm voltages, v_{cP} and v_{cN}, are given by the following equation [7]:

$$v_{cP} = n_P v_{cP}^{\Sigma} \tag{4.5a}$$

$$v_{cN} = n_N v_{cN}^{\Sigma} \tag{4.5b}$$

, where n_P and n_N are the insertion indices. By studying the equivalent circuit in figure 2.2, the following expression for the inserted arm voltages also yields [29]:

$$v_{cP} = \frac{E}{2} - v_j - v_{Zj} \tag{4.6a}$$

$$v_{cN} = \frac{E}{2} + v_j - v_{Zj} \tag{4.6b}$$

The insertion indices, n_P and n_N, is the number of inserted submodules in each arm. It can found by using the total capacitor voltages, v_{cP}^{Σ} and v_{cN}^{Σ}, combined with the inserted arm voltages, v_{cP} and v_{cN} [7]:

$$n_u = \frac{\frac{v_d}{2} - v_j - v_{Zj}}{v_{cj}^{\Sigma}} \tag{4.7a}$$

$$n_l = \frac{\frac{v_d}{2} + v_j - v_{Zj}}{v_{cj}^{\Sigma}} \tag{4.7b}$$

4.1 Operation Close to Rated Speed

When the speed of a motor drive is reduced from its rated value, the voltage must be reduced almost proportionally. This is to keep the magnetization level, $\hat{V}_j/\omega_j$, constant [7]. The reduced voltage requirement allows a reduction of the average capacitor voltage, which can be controlled by adjusting the freely chosen integration constants, W_{cP0}^{Σ} and W_{cN0}^{Σ}, given by equation 4.3. By reducing the average capacitor voltage, the converter can allow bigger voltage ripples without

exceeding the capacitor voltage ratings [7].

4.2 Intermediate-Speed Range

A reduction of the average capacitor voltage level will only be a sufficient measure in an operating speed close to the rated speed. For lower speeds, the amplitude of the capacitor ripples will not be acceptable. An idea presented by Ilves et al. [13] is to benefit from the second harmonic behavior of the circulating current. The circulating current affects the ripple of the available voltage in the converter arms. By manipulating the circulating current, the ripple can be made such that it coincides with the peak of the requested voltage, thus improving the utilization of the submodule capacitor voltage. The fundamental frequency capacitor voltage ripple is caused by the $\hat{I}_j/\omega_j$-term of equation 4.3, as this is the dominant term. The idea presented by Ilves et al. [13] is therefore based on a compensation of the $\hat{I}_j/\omega_j$-term. The approach is not limited to the utilization of second order harmonics only, and an expanded approach by Antonopoulos et al. [7], suggests generating a voltage component at the output of the converter, which will not distort the stator voltages. The voltage component is created through a common mode voltage, v_{com}, explained by equation 4.8 [28]. Antonopoulos et al. [7] chooses v_{com} to be in the form given by equation 4.9.

$$v_{com} = \frac{v_u + v_v + v_w}{3} \tag{4.8}$$

$$v_{com} = \hat{V}_{com}\cos(\omega_{com}t + \varphi_{com}) \tag{4.9}$$

In addition, circulating currents should be generated, forming a positive and negative sequence relative to the common mode voltage, v_{com}. The positive and negative sequence circulating current components ,i_{Zp} and i_Zn, can be selected as [7]:

$$i_{Zp} = \hat{I}_{Zp}\cos[(\omega_{cm} + \omega_s)t + \varphi_{Zp}] \tag{4.10a}$$

$$i_{Zn} = \hat{I}_{Zn}\cos[(\omega_{cm} - \omega_s)t + \varphi_{Zn}] \tag{4.10b}$$

The frequency of i_{Zp} and i_{Zn} differs from the common mode voltage frequency by the stator frequency, which according to Antonopoulos et al. [7] will lead to both a fundamental frequency energy fluctuation in the arm capacitors and a fluctuation at the sum of the two frequencies. The fundamental frequency energy fluctuation should be placed so that it compensates fundamental frequency ripples of the capacitor. The fluctuation at the sum of the stator frequency and the common mode frequency will not give a small contribution, as the high frequency will cause a low capacitor reactance [7]. The effect of the positive and negative sequence currents, i_{Zp} and i_{Zn}, will be zero if they form a symmetrical system in the converter phases.

A part of the arm voltage is needed to drive the compensating currents:

$$v_Z = Ri_c + L\frac{di_c}{dt} \tag{4.11}$$

This gives an extended expression for the inserted arm voltages [7]:

$$v_P = \frac{E}{2} - v_j - v_{com} - v_{Zj} - R_a\tilde{i}_c \tag{4.12a}$$

$$v_N = \frac{E}{2} + v_j + v_{com} - v_{Zj} - R_a\tilde{i}_c \tag{4.12b}$$

, where R_a is a proportional gain active resistance controlling the circulating current and $\tilde{i}_c$ is the difference between the wanted circulating current and the measured. The $R_a\tilde{i}_c$-term will be zero under ideal conditions.

Finding the right contribution from i_{Zp}, i_{Zn} and v_{com} is not straight forward. In a scenario where the speed is decreasing from close to rated speed, it is not wise to apply full capacitor voltage compensation from the beginning, as the voltage driving the circulating currents, v_{Zj}, will be unnecessarily high, in addition to high losses. The compensation should then increase with the speed reduction. Another principle, is to generate the highest possible common mode voltage, reducing the need for compensating currents [7].

In order to select a reasonable common mode frequency, ω_{com}, there are several factors to take into consideration. A low ω_{com}, gives a low arm impedance, $\omega_{com}L$, thus reducing the voltage needed to drive the circulating current, v_{Zj}. This leaves space for a high common mode voltage. However, a low ω_{com} will cause a high capacitor energy ripple, due to the high capacitor reactance at a low $\omega_j + \omega_{com}$.

4.3 Low Speed and Standstill

In the case of standstill, i.e. zero frequency, equation 4.1 and 4.2, shows that v_j, i_j and the power delivered to the arm capacitors will be constant, giving a constant increase or decrease of sum capacitor voltage [7]. In Antonopoulos et al. [30] it is shown that by introducing a component in phase with and in the same frequency as the output voltage v_j, it is possible to control the balancing of the sum capacitor voltages.

With low speed, the phase voltage, v_j, and phase current i_j is almost constant and has a low amplitude. They can be approximated as [7]:

$$v_j = \hat{V}_{j0} \tag{4.13a}$$

$$i_j = \hat{I}_{j0} \tag{4.13b}$$

, where the amplitude of i_j depends on the torque demand.

A high frequency common mode voltage can be created, without affecting the stator voltages

[7]:

$$v_{com} = \hat{V}_{com}\cos(\omega_{com}t) \tag{4.14}$$

This gives a new expression for v_j:

$$v_j = \hat{V}_{j0} + \hat{V}_{com}\cos(\omega_{com}t) \tag{4.15}$$

Antonopoulos et al. [7] suggest the following circulating current injection in each phase, where the oscillating component does not affect the stator currents:

$$i_{Zj} = i_{Zj0} + \hat{I}_{Zj}\cos(\omega_{com}t) \tag{4.16}$$

As the circulating current creates losses, Antonopoulos et al. [7] recommends to minimize $\hat{I}_c$, by using all available voltage to generate the common mode voltage. By defining a fixed value for $\hat{V}_{com}$, the energy in the upper and lower arm can be controlled by varying $\hat{I}_{Zj}$. This gives the following voltage driving the circulating current [7]:

$$v_{Zj} = Ri_{Zj0} + R\hat{I}_{Zj}\cos(\omega_{com}t) - \omega_{com}L\hat{I}_{Zj}\sin(\omega_{com}t) \tag{4.17}$$

The power delivered to the arm capacitors are given by [7]:

$$p_{Pj} = i_{Pj}v_{Pj} = \left(\frac{\hat{I}_{j0}}{2} + i_{Zj0} + \hat{I}_{Zj}\cos(\omega_{com}t)\right)\cdot\left(\frac{E}{2} - \hat{V}_{j0} - \hat{V}_{com}\cos(\omega_{com}t) - v_{Zj}\right) \tag{4.18a}$$

$$p_{Nj} = i_{Nj}v_{Nj} = -\left(\frac{\hat{I}_{j0}}{2} + i_{Zj0} + \hat{I}_{Zj}\cos(\omega_{com}t)\right)\cdot\left(\frac{E}{2} + \hat{V}_{j0} + \hat{V}_{com}\cos(\omega_{com}t) - v_{Zj}\right) \tag{4.18b}$$

By carrying out the multiplication of equation 4.18 and removing the varying terms, you find the constant terms of equation 4.18:

$$p_{Pj0} = \left\{-\frac{\hat{V}_{j0}\hat{I}_{j0}}{2} + \frac{Ei_{Zj0}}{2} - Ri_{Zj0}^2 - \frac{R\hat{I}_{Zj}^2}{2}\right\} + \left\{\frac{E\hat{I}_{j0}}{4} - \hat{V}_{j0}i_{Zj0} - \frac{Ri_{c0}\hat{I}_{j0}}{2} - \frac{\hat{V}_{cm}\hat{I}_c}{2}\right\} \tag{4.19a}$$

$$p_{Nj0} = \left\{-\frac{\hat{V}_{j0}\hat{I}_{j0}}{2} + \frac{Ei_{Zj0}}{2} - Ri_{Zj0}^2 - \frac{R\hat{I}_{Zj}^2}{2}\right\} + \left\{-\frac{E\hat{I}_{j0}}{4} + \hat{V}_{j0}i_{Zj0} + \frac{Ri_{Zj0}\hat{I}_{j0}}{2} + \frac{\hat{V}_{com}\hat{I}_{Zj}}{2}\right\} \tag{4.19b}$$

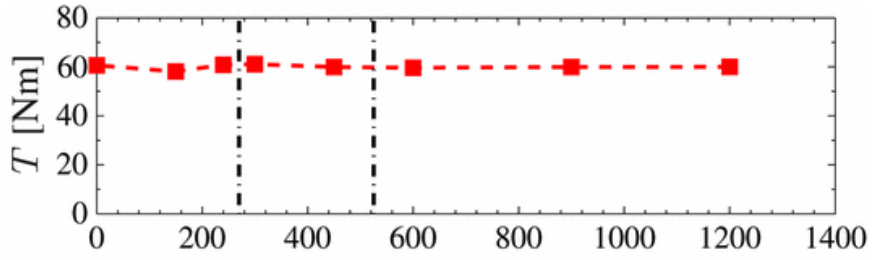
If the capacitors should remain balanced, the constant power delivered to the arms must be zero [7]:

$$\frac{\hat{V}_{j0}\hat{I}_{j0}}{2} - \frac{Ei_{Zj0}}{2} + Ri_{Zj0}^2 + \frac{R\hat{I}_{Zj}^2}{2} = 0 \tag{4.20a}$$

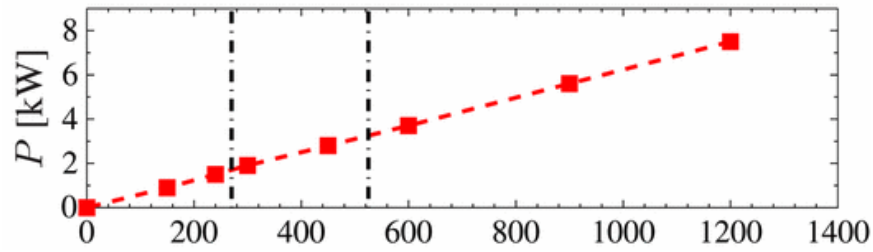
$$\frac{E\hat{I}_{j0}}{4} - \hat{V}_{j0}i_{Zj0} - \frac{Ri_{Zj0}\hat{I}_{j0}}{2} - \frac{\hat{V}_{com}\hat{I}_{Zj}}{2} = 0 \tag{4.20b}$$

In equation 4.20, both i_{Zj0} and $\hat{I}_{Zj}$ are unknown for a given $\hat{V}_{j0}$ and $\hat{I}_{j0}$ output. $\hat{I}_{Zj}$ can be obtained from equation 4.20b and substituted in to equation 4.20a, giving a second order equation for i_{c0}. The energy variation can then be found by integrating the oscillating terms of equation 4.18. In order to find the insertion indices, the same procedure as for speeds close to the rated speed can be followed. That means to find the total capacitor voltage in the arms [eq. 4.4], and insert it into equation 4.7 [7].

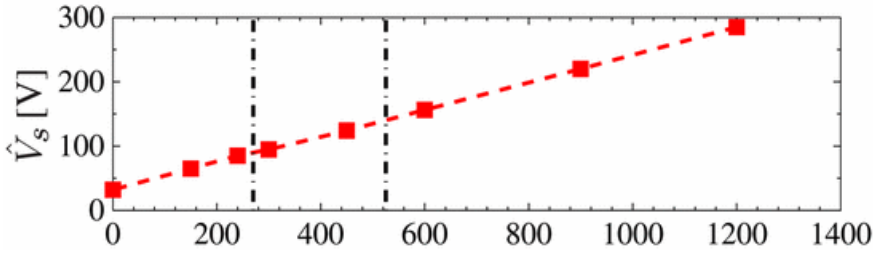
The experimental results of the study done by Antonopoulos et al. [7] are shown in figure 4.1. The dashed line separates the different operating regions from each other. Figure 4.1a shows that the converter is able to run a constant torque load during the whole frequency range. Figure 4.1d suggests that the critical point of operation is not at standstill, but rather at approximately 300rpm. [7] concludes that a cost-efficient converter design will be a function of the capacitor size, the dc-link voltage, and the output-voltage capability.



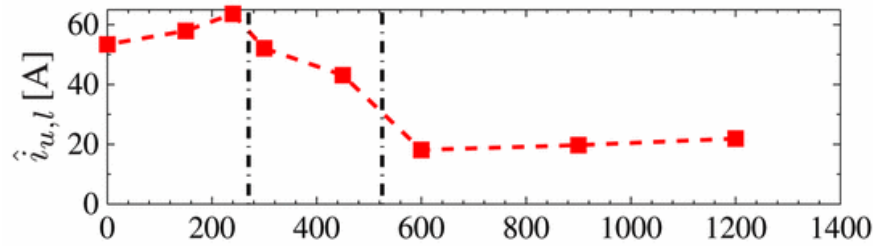
(a) Torque, T



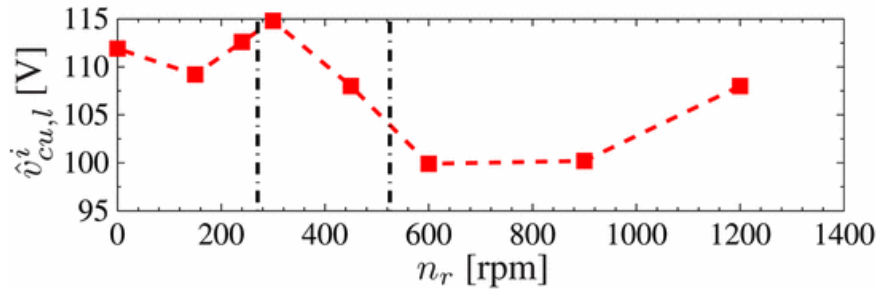
(b) Power, P



(c) Phase Voltage, $\hat{V}_s$



(d) Arm current, $\hat{i}_{u,l}$



(e) Individual Capacitor Voltage, $\hat{v}^i_{cu,l}$

Figure 4.1: Experimental results from [7]

Chapter 5

Current Suppressing Strategies

This thesis studies three different strategies for suppressing the circulating current:

- Strategy proposed by Nademi [1]
- Strategy based on arm voltage comparison
- Strategy proposed by Tu et al. [2]

5.1 Strategy proposed by Nademi [1]

The strategy proposed by Nademi [1] is based on the fact that the sum of the capacitor voltages in each arm should be equal to the DC supply voltage, E. The strategy uses the relationship between the two as a gain for the reference signal. Figure 5.1 illustrates the strategy.

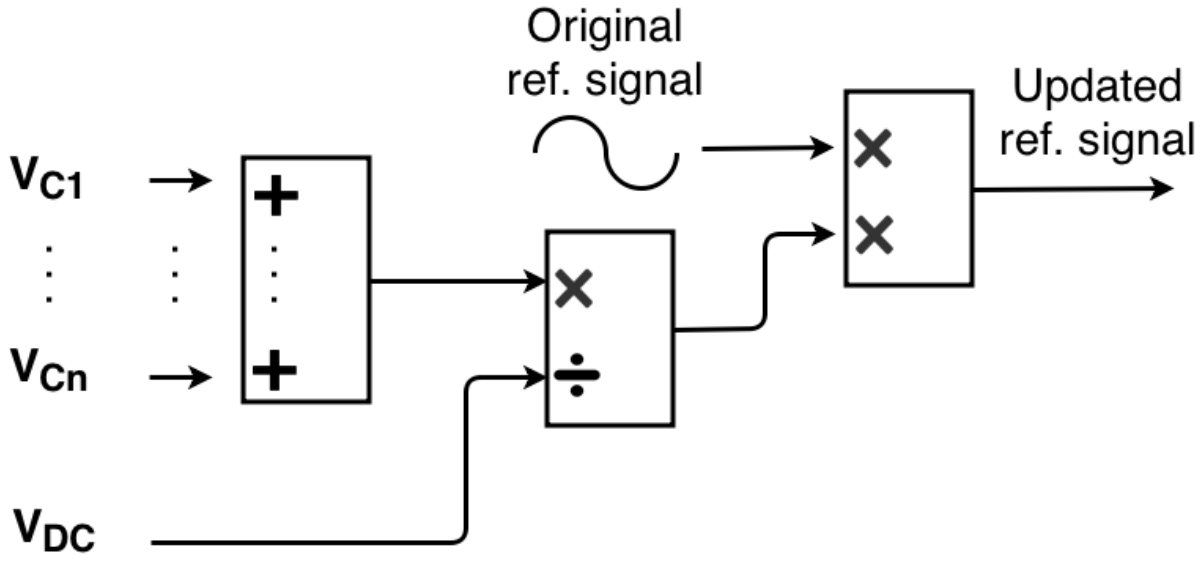


Figure 5.1: Illustration of the 2^{nd} harmonic minimization strategy proposed by Nademi [1]

5.2 Strategy based on arm voltage comparison

A strategy proposed by this thesis is to find the ratio between the actual arm voltage and the reference arm voltage. The ratio is then used as a modulation index for the reference signal. In this way, the arm voltages are forced to follow the reference arm voltage, thus suppressing the voltage differences within the converter.

5.3 Strategy proposed by Tu et al. [2]

Tu et al. [2] has proposed a circulating current suppressing controller, CCSC. The paper rewrites the circulating current, i_{Zj}, given by equation 2.6 into:

$$i_{\mathrm{Zu}} = \frac{I_{\mathrm{d}}}{3} + I_{2f}\sin(2\omega_0 t + \varphi_0) \tag{5.1a}$$

$$i_{\mathrm{Zv}} = \frac{I_{\mathrm{d}}}{3} + I_{2f}\sin\left[2\left(\omega_0 t - \frac{2\pi}{3}\right) + \varphi_0\right] = \frac{I_{\mathrm{dc}}}{3} + I_{2f}\sin\left(2\omega_0 t + \varphi_0 + \frac{2\pi}{3}\right) \tag{5.1b}$$

$$i_{\mathrm{Zw}} = \frac{I_{\mathrm{d}}}{3} + I_{2f}\sin\left[2\left(\omega_0 t + \frac{2\pi}{3}\right) + \varphi_0\right] = \frac{I_{\mathrm{dc}}}{3} + I_{2f}\sin\left(2\omega_0 t + \varphi_0 - \frac{2\pi}{3}\right) \tag{5.1c}$$

, where φ_0 is the initial phase angle.

According to Tu et al. [2], the inner dynamic performance of the MMC is characterized by:

$$v_{\mathrm{Zj}} = L_0\frac{di_{\mathrm{Zj}}}{dt} + R_0 i_{\mathrm{Zj}} = \frac{1}{2}\left[E - (v_{Pj} + v_{Nj})\right] \tag{5.2}$$

, which can be rewritten into:

$$\begin{bmatrix} v_{Zu} \\ v_{Zw} \\ v_{Zv} \end{bmatrix} = L_0\frac{d}{dt}\begin{bmatrix} i_{Zu} \\ i_{Zw} \\ i_{Zv} \end{bmatrix} + R_0\begin{bmatrix} i_{Zu} \\ i_{Zw} \\ i_{Zv} \end{bmatrix} \tag{5.3}$$

By using Park's transformation, equation 5.1 can be expressed by two DC components. The two components is in this case in the double fundamental frequency, negative-sequence rotational reference frame, and is given by [2]:

$$T_{acb/dq} = \frac{2}{3}\begin{bmatrix} cos\theta & cos\left(\theta - \frac{2\pi}{3}\right) & cos\left(\theta + \frac{2\pi}{3}\right) \\ -sin\theta & -sin\left(\theta - \frac{2\pi}{3}\right) & -sin\left(\theta + \frac{2\pi}{3}\right) \end{bmatrix} \tag{5.4}$$

, where $\theta = 2\omega_0 t$. By substituting equation 5.1 into 5.3 and multiplying the T-matrix given by equation 5.4 yields [2]:

$$\begin{bmatrix} v_{Zd} \\ v_{Zq} \end{bmatrix} = L_0\frac{d}{dt}\begin{bmatrix} i_{2fd} \\ i_{2fq} \end{bmatrix} + \begin{bmatrix} 0 & -2\omega_0 L_0 \\ 2\omega_0 L_0 & 0 \end{bmatrix} \cdot \begin{bmatrix} i_{2fd} \\ i_{2fq} \end{bmatrix} + R_0\begin{bmatrix} i_{2fd} \\ i_{2fq} \end{bmatrix} \tag{5.5}$$

Tu et al. [2] proposes the circulating current suppressing controller (CCSC) shown in figure 5.2. The inner difference current, i_{Zj} is transferred to the dq-frame currents, i_{2fd} and i_{2fq}, through the T-matrix given in equation 5.4. The dq-currents are then compared with a reference current, i_{2fd_ref} and i_{2fq_ref}, which both are set to zero, as the goal is to eliminate the circulating current. The dq inner unbalance reference signals, v_{Zd_ref} and v_{Zq_ref} are found through a PI controller and a cross-coupling. After an inverse transformation, the CCSC returns the reference inner unbalance voltage, v_{Zj_ref}. The arm voltage references are then found from the following equations:

$$v_{Pj\_ref} = \frac{E}{2} - e_j - v_{\mathrm{Zj}} \tag{5.6a}$$

$$v_{Nj\_ref} = \frac{E}{2} + e_j - v_{\mathrm{Zj}} \tag{5.6b}$$

This gives a control structure as shown in figure 5.3.

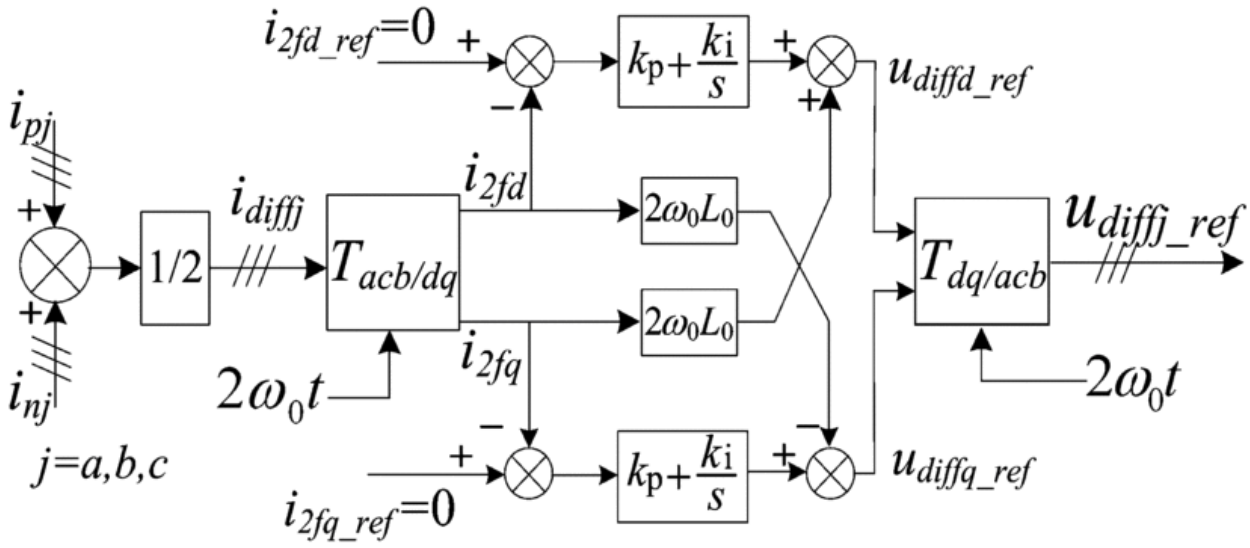


Figure 5.2: Circulating Current Suppressing Controller by [2]. The circulating current, i_{Zj}, is here labeled i_{diffj}

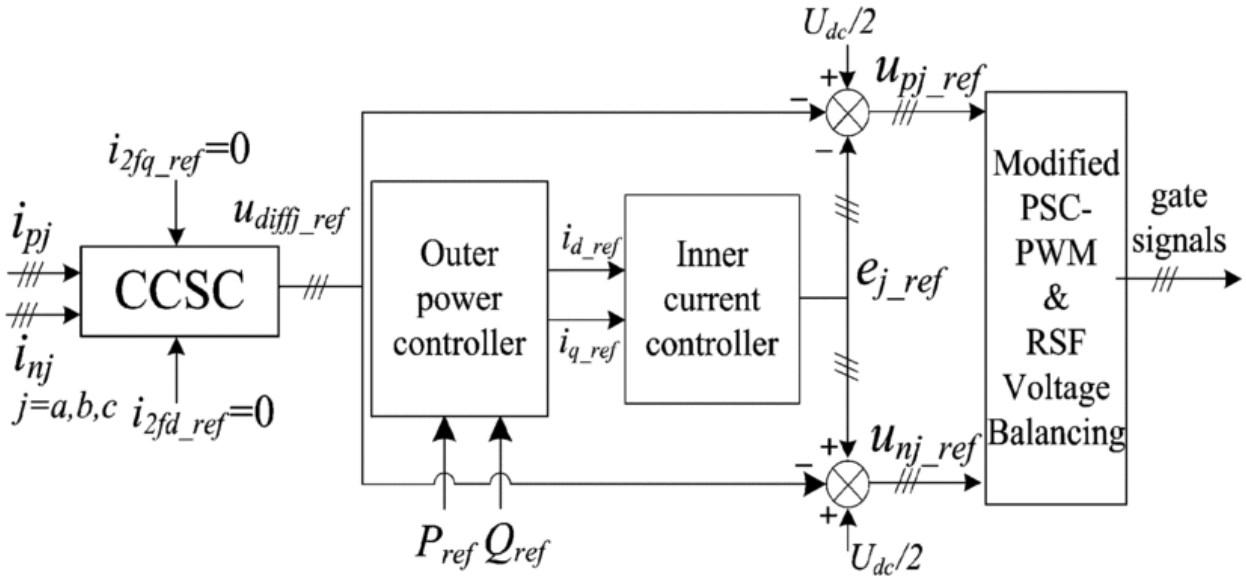


Figure 5.3: Control Structure of the MMC, including the CCSC [2]

Chapter 6

The simulation model

The simulations in this thesis are conducted using Matlab Simulink. The simulation model developed during the project thesis was a one-phase model. In this master thesis, the one-phase model has been further developed into a three-phase model. The model was developed using the theory of chapter 2. The developed model consists of eight half-bridge submodules in each arm and a level-shifted PWM switching scheme was implemented to ensure proper switching of the IGBTs. Table 6.1 lists the simulation parameters used for the simulation. The work of Mosgren [31] was used as a basis for the selection of converter parameters.

Vdc/2	300V
SM Capacitor	4.7mF
Load L	21.8mH
Load R	9.12omh
Arm Inductance	1.2mH
Arm Resistance	0.04ohm
Carrier Frequency	2000Hz
Nominal Frequency	50Hz
Modulation Index	1

Table 6.1: Simulation Parameters

This thesis presents three different scenarios that was implemented an simulated in Simulink.

1. No CCSC implemented
2. CCSC based on arm voltage comparison
3. CCSC proposed by Nademi [1]
4. CCSC proposed by Tu et al. [2]

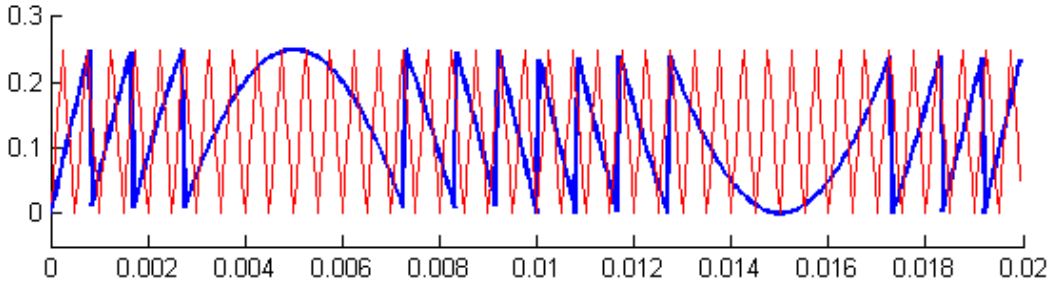


Figure 6.1: Reference signal brought inside one carrier

6.1 No CCSC implemented

The basis for all simulations in this thesis is the three-phase model shown in figure A.1 in appendix A. The upper arm of the converter model is shown in figure A.2 and the submodule is shown in figure A.3. The sorting algorithm is based on the centralized voltage balancing principles presented in section 2.5. Figure A.4 shows how the algorithm was implemented. The algorithm can be divided into three steps:

1. First the capacitors are sorted based on their voltage level. The capacitors position in the sorted list is used in the second step. The function providing this functionality is found in appendix B.

2. Second, the desired state of each submodule is found. From the reference signal, a desired number of contributing submodules are found. If the arm current is positive the submodules with the lowest capacitor voltage are chosen to contribute, and the opposite in the case of a negative arm current. The submodule in-between the on-state submodules and the off-state submodules is allocated for the PWM-state. The function providing this functionality is found in appendix B.

3. Third, based on the allocated state in the second step, each submodule is given the corresponding signal: on=1, off=0 and PWM=PWM.

The PWM-switching scheme chosen in this model, is a modified level-shifted concept proposed by Nademi [1]. To avoid synchronization problems, it is recommended to use only one triangular carrier of magnitude 2/n, where n is the number of submodules in each arm. The proposed method modifies the reference signal so that it is brought within the carrier. Each time the reference signal exceeds the values of the triangular carrier, the reference signal is shifted up or down. The modified reference signal can be seen in figure 6.1.

6.2 CCSC Proposed by Nademi [1]

In order to test the 2^{nd} harmonic minimization strategy discussed in section 5.1, the algorithm shown in figure A.5 in appendix A was implemented into the Simulink model. The capacitor

voltages of each arm are summed, and the ratio between the arm voltage and the DC supply voltage is used as a gain for the reference signal.

6.3 CCSC Based on Arm Voltage Comparison

A proposed algorithm for 2^{nd} harmonic suppression is shown in figure A.6 in appendix A. The algorithm is based on a comparison between the actual arm voltage and the arm voltage reference. The relationship between the two is used as a modulation index. As the arm voltage reference oscillates between 0 and the value of E, a constant is added to avoid division by zero. The constant is added to both the arm voltage and the arm voltage reference, and is by testing found to work best at $const \approx 0.3E$. The ratio between the actual arm voltage and the reference will be changed by adding a constant to the equation. However it will only change the amplitude of the modulation index and not have an impact on wether or not the modulation index is greater or smaller than 1. Thus the change of ratio is considered as an insignificant effect.

6.4 CCSC proposed by Tu et al. [2]

The CCSC proposed by Tu et al. [2] was presented in section 5.3. The implementation of the controller in the three-phase Matlab Simulink model are shown in figure A.7 in appendix A. The controller starts by calculating the circulating current, which is transformed into the dq-domain. The error between the actual circulating and the wanted circulating current, $i_{Zref} = 0$ is then processed through a PI-controller, giving an expression for the reference circulating voltage. The reference circulating voltage is then subtracted from the reference phase voltage, as given by equation 5.6.

Chapter 7

Results

The results of the simulations conducted on the Simulink model presented in chapter 6 are presented in this chapter.

7.1 No CCSC implemented

As a basis for comparison, a simulation without any CCSC implemented was conducted. The result shows a 9-level phase voltage in figure C.1 in appendix C, illustrating the distinctive multilevel waveform of an MMC. Figure C.2 shows the phase current, which is close to sinusoidal. Table 7.1 displays the THD content of the phase and arm voltages and currents. The THD content that stands out from the others is the arm current THD of 203%. The submodule capacitor voltages of figure 7.1 spans from 69V to 79V.

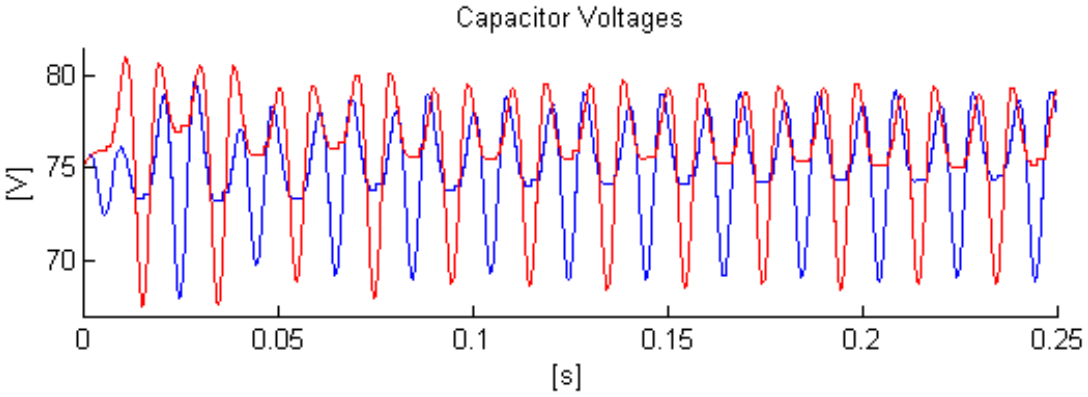


Figure 7.1: U-Phase Upper and Lower Capacitor Voltages When No CCSCs are Implemented

7.2 CCSC proposed by Nademi [1]

Figure 7.2 shows how the capacitor voltages decreases when turning on the CCSC proposed by Nademi [1] at $t = 0.25s$. Δv_c drops almost instantaneous from $10V$ to $6V$. The proper

THD		
	Phase	Arm
Voltage	15.7%	17.4%
Current	2.77%	203%

Table 7.1: Current and Voltage THD When No CCSCs are Implemented

functioning of the CCSC is verified by the 2^{nd} harmonic current drop from $25A$ to $16A$ [fig.7.3] and the THD content of the arm current of 151%, listed in table 7.2.

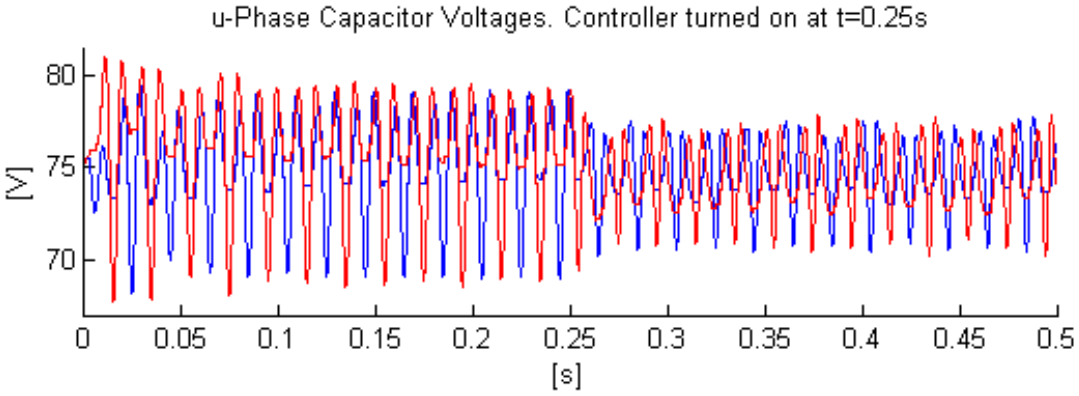


Figure 7.2: Submodule Capacitor Voltages Using the CCSC proposed by Nademi [1]

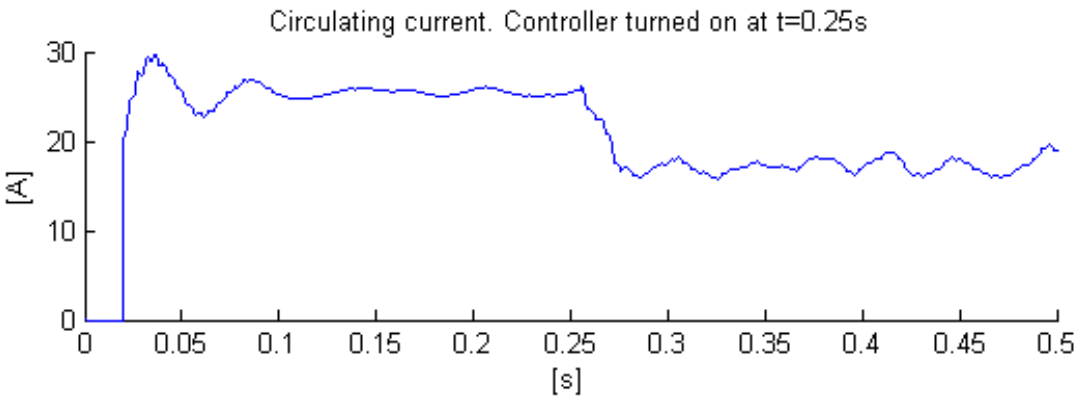


Figure 7.3: 2^{nd} Harmonic Arm Current Using the CCSC proposed by Nademi [1]

THD		
	Phase	Arm
Voltage	18.1%	16.0%
Current	3.26%	151%

Table 7.2: Current and Voltage THD Using the CCSC proposed by Nademi [1]

In order to test the controller on lower frequencies, simulations where conducted at half of nominal frequency as well. The result is found in figure C.3 and C.4, showing an increase of Δv_c and a reduction of 2^{nd} harmonic current accordingly.

7.3 CCSC Based on Arm Voltage Comparison

Figure 7.4 shows the decline in capacitor voltage ripple after turning on the controller based on the comparison between the actual arm voltage and the reference arm voltage. Δv_c drops from $10V$ to $6V$, and the 2^{nd} harmonic current drops from an amplitude of $25A$ to $15A$ [fig.7.5]. The 2^{nd} harmonic arm current reduction is also reflected in table 7.3, where the arm current THD are listed as 132%. The results of the simulations at half of nominal speed are found in figure C.5 and C.6, showing an increase of Δv_c and a reduction of 2^{nd} harmonic current accordingly.

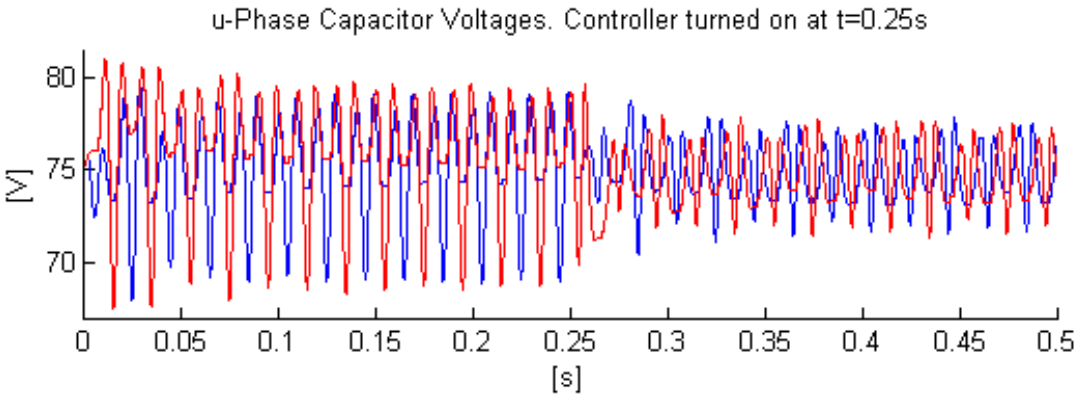


Figure 7.4: Submodule Capacitor Voltages Using the CCSC based on Arm Voltage Comparison

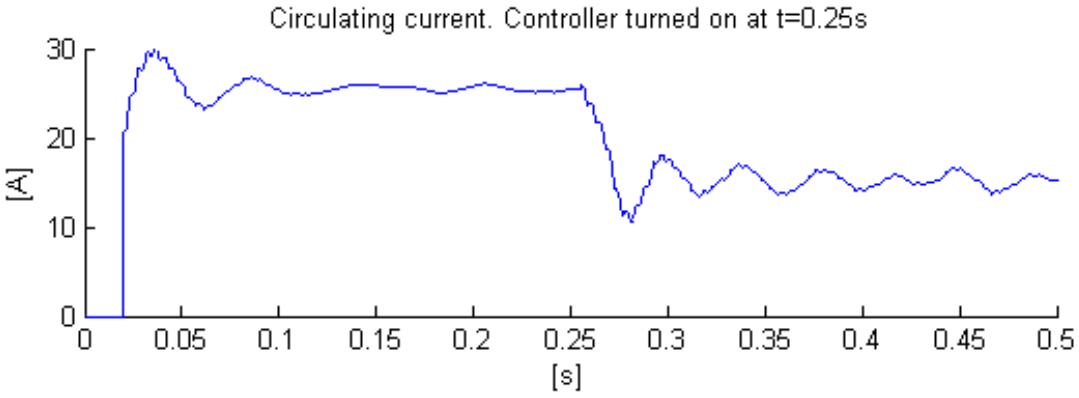


Figure 7.5: 2^{nd} Harmonic Arm Current Using the CCSC based on Arm Voltage Comparison

THD		
	Phase	Arm
Voltage	10.5%	17.9%
Current	2.50%	132%

Table 7.3: Current and Voltage THD Using the CCSC based on Arm Voltage Comparison

7.4 CCSC proposed by Tu et al. [2]

The effect of the CCSC proposed by Tu et al. [2] is illustrated in figure 7.6, indicating a reduction of Δv_c from $10V$ to $6V$. The reduction of 2^{nd} order harmonics in the arm current is significant, from $25A$ to $7A$ [fig.7.7]. Table 7.4 confirms the reduction of 2^{nd} order harmonics in the arm current, as the THD is measured to be 58%. Figure C.7 and C.8 in appendix C shows the output voltages and currents of the system when using the CCSC. In addition, the change of arm current when turning on the CCSC can be seen in figure C.9.

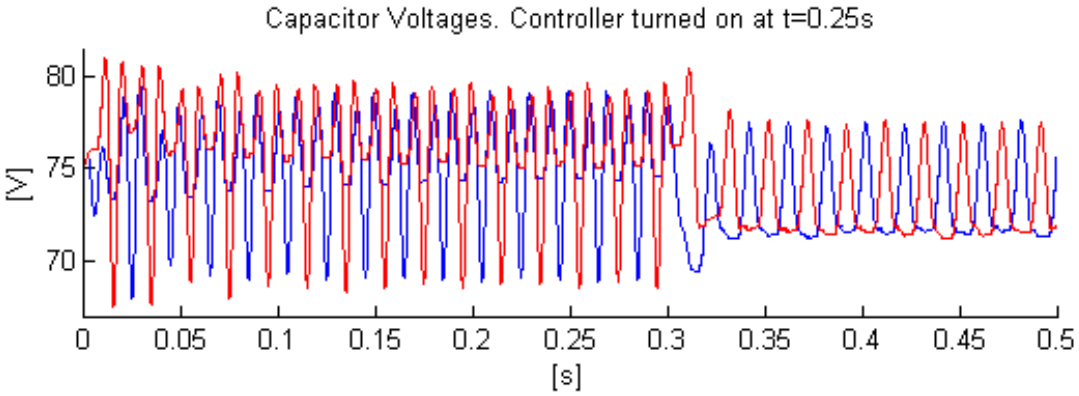


Figure 7.6: Submodule Capacitor Voltages Using the CCSC proposed by [2]

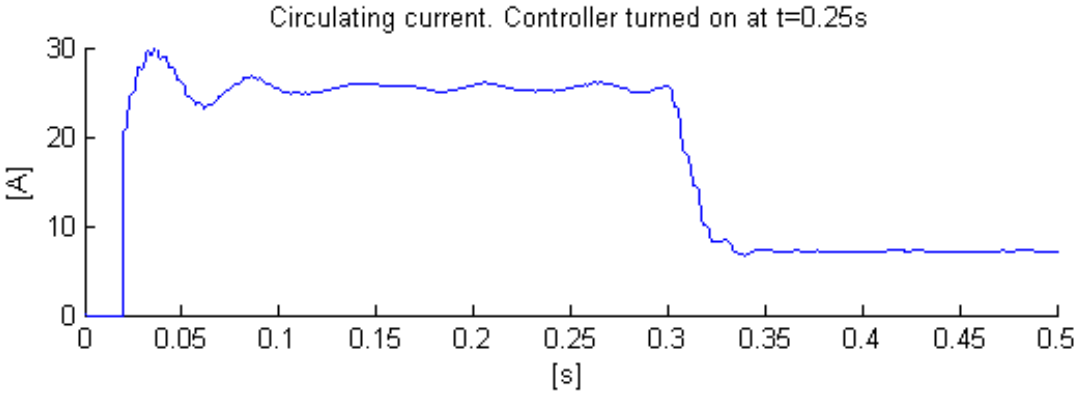


Figure 7.7: 2^{nd} Harmonic Arm Current Using the CCSC proposed by [2]

The low frequency performance of the controller was also tested, and the result is found in figure C.10 and C.11 in appendix C, showing an increase of Δv_c and a reduction of 2^{nd} harmonic

THD		
	Phase	Arm
Voltage	6.96%	14.3%
Current	0.82%	58.0%

Table 7.4: Current and Voltage THD Using the CCSC proposed by [2]

current accordingly.

Chapter 8

Discussion and Further Work

The result of this thesis shows that a three-phase MMC with a level-shifted PWM switching scheme will deliver a well balanced 9-level output [fig.C.1], with a sinusoidal output current [fig.C.2]. The balancing algorithm described in section 2.5 ensures well balanced capacitor voltages, thus a well balanced overall system. However, as illustrated by figure 7.1, the capacitor voltages spans from 69V to 79V which represents a large capacitor voltage ripple. As revealed by table 7.1, the THD of the arm current is large, indicating a high circulating current. In order to reduce the 2^{nd} harmonic of the arm current, a controller proposed by Nademi [1] was implemented. The result of figure 7.2 and 7.3 shows that the capacitor voltage ripple, Δv_c, drops from $10V$ to $6V$ and the 2^{nd} harmonic current drops from $25A$ to $16A$ when the controller is turned on. However, it is still a large proportion of 2^{nd} harmonics in the arm current, with an arm current THD of 151%. In order to mitigate a greater proportion of the 2^{nd} harmonics, another controller was proposed, using the arm voltages as a basis for a modulation index. The results shown in figure 7.4 and 7.5 shows a drop of capacitor voltage ripple and circulating current, comparable to what was achieved with the controller proposed by Nademi [1]. Table 7.3 indicates a slightly better performance however, with an arm current THD of 132%.

By implementing the CCSC proposed by Tu et al. [2], figure 7.6 shows a capacitor voltage ripple decrease, comparable to the result of the CCSC proposed by Nademi [1] and the CCSC based on arm voltage comparison. Figure 7.7 on the other hand, shows a drastically reduced circulating current, compared to the two other controllers. The controller proposed by Tu et al. [2] reduces the 2^{nd} harmonic content of the arm current from $25A$ to $7A$, which means a 72% reduction. The output voltages and currents [fig:C.7 and C.8] appears to be similar to the output without any controller. However, when comparing the THD content of the arm and phase voltages and currents, table 7.4 clearly indicates an improved performance of the converter when using the controller proposed by Tu et al. [2].

Figure C.9 showing the upper and lower arm currents of phase-u gives a good understanding of the importance of reducing the circulating currents in the converter. When the controller proposed by Tu et al. [2] is turned on, the 2^{nd} harmonic content is reduced, which can be seen in the overall arm current, which also reduces drastically. The result underlines the fact that the circulating current can occupy a large share of the available capacity of the converter.

When testing the controllers at half of nominal speed, the controllers proved weaknesses. All three controllers managed to reduce the circulating current, as illustrated by figure C.4, C.6 and C.11. Although the circulating current was reduced, all three controllers had a negative effect on the capacitor voltage ripples, as proved by figure C.3, C.5 and C.10, where all three controllers caused an increase of voltage capacitor ripple. The combination of a reduced circulating current, together with an increased voltage capacitor ripple suggests that for lower frequencies, the CCSCs studied in this thesis are not a sufficient measure to decrease the capacitor voltage ripples.

Further work on the topic covered by this thesis should include additional measures in combination with the CCSCs tested in this thesis. Additional measures are discussed in section 4 and includes a different type of circulating current shaping, in addition to the introduction of a high frequency common mode voltage. The aim of the further work should be to maintain the circulating current suppressing functionality, at the same time as the capacitor voltage ripples are reduced, also for lower frequencies.

Chapter 9

Conclusion

This thesis has looked into the topic of MMC, and especially the challenges regarding MMC for electric motor drive applications. Advantageous features such as a multilevel waveform, a modular realization and cost saving features have been presented. The structure of the MMC is given by figure 2.2, with the half-bridge submodule technology presented in figure 2.3. In order to ensure a desired operation of the MMC, control objectives such as active and reactive control, DC link voltage control, submodule capacitor voltage control and current control are all vital. The different PWM switching schemes have various properties, however level-shifted PWM was used in the Matlab Simulink simulations, with its low harmonic distortion combined with a better RMS load voltage than comparable switching schemes. Voltage balancing of the submodule capacitors are one of the key issues of the MMC, thus a centralized voltage balancing method has been presented in this thesis, where the capacitors are sorted based on voltage level, and given an operating state accordingly.

The objective of this thesis was to gain a better understanding of MMC for electric motor drive applications. The main challenge in that respect, is the low frequency operation associated with running the motor drive through the whole frequency range, as the submodule capacitor voltage ripples are inversely proportional to the AC-side frequency. Large voltage ripples will cause large variations within the converter, giving rise for an extensive circulating current. Measures for suppressing the circulating current was therefore reviewed through a literature search. The literatur focused on two measures: shaping/suppressing of the circulating current, and introduction of a common mode voltage. The thesis has focused on different circulating current suppressing controllers, and studied the effect of the suppression in combination with the voltage capacitor ripple.

Three CCSCs were tested in this thesis: a controller proposed by Nademi [1], a controller proposed by Tu et al. [2] and a controller proposed by this thesis. In order to simulate the effect of the controllers, the one-phase simulation model of the project thesis was developed into a three-phase model. The model proved stable and well balanced, as illustrated by figure C.1 and C.2 in appendix C. As shown in section 7, all three controllers had an equal effect on the capacitor voltage ripple, as Δv_c was reduced from $10V$ to $6V$ in all three cases. When it came to the circulating current, the controllers behaved differently. Without any controllers turned on,

the 2^{nd} harmonic content of the arm current had an amplitude of $25A$. The controller proposed by Nademi [1] managed to reduce it to 16A, the controller proposed by this thesis reduced it to $15A$, while the controller proposed by Tu et al. [2] reduced the 2^{nd} harmonic current amplitude to $7A$. The output voltages and currents are also improved using the Tu et al. [2]-controller, with a phase voltage THD reduced from 15.7% to 6.95% and the phase current THD reduced from 2.77% to 0.82%.

When testing the controllers at lower frequencies, they all showed weaknesses. Although all controllers managed to reduce the circulating current, they all increased the voltage ripple at the same time. Thus, the controllers tested in this thesis are not a sufficient measure alone with respect to electric motor drive applications for MMC. Further work needs to be done on this topic, and should include different types of circulating current suppressing or shaping, in combination with the introduction of a common mode voltage.

Appendix A

The Matlab Simulink Model

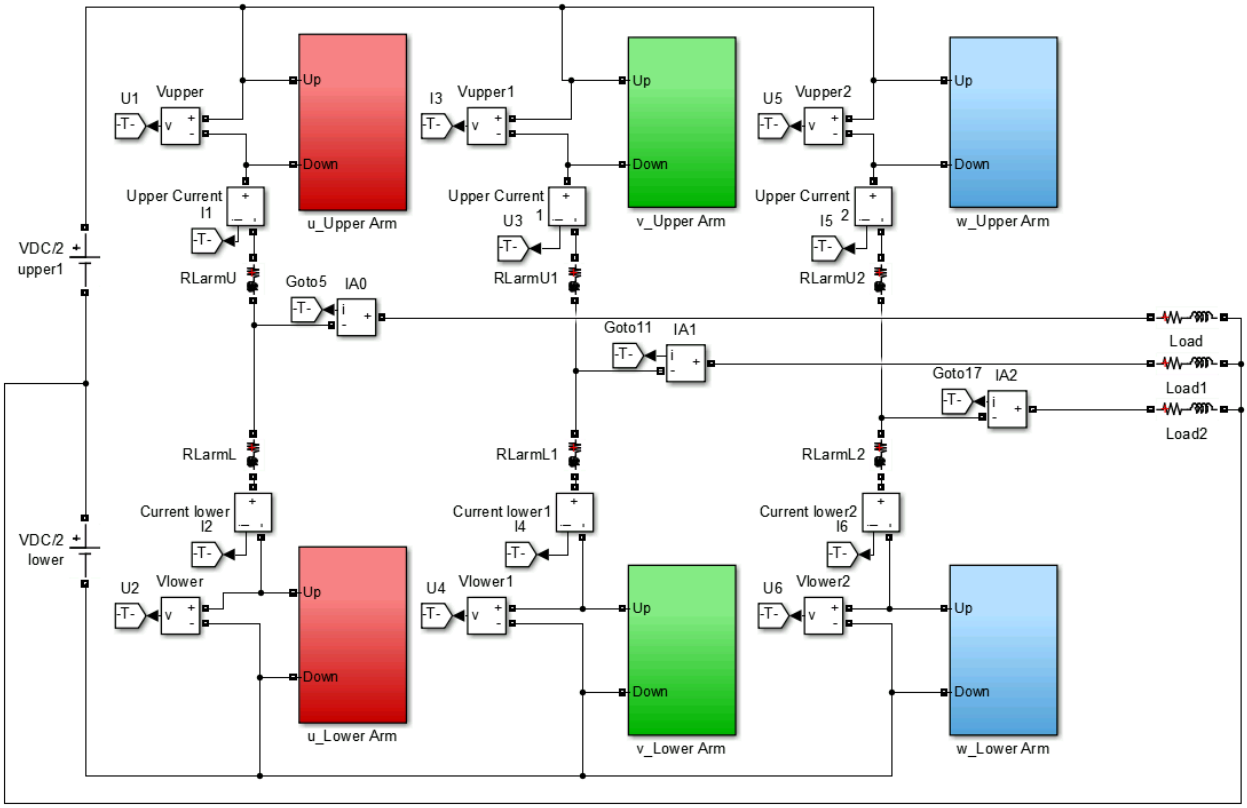


Figure A.1: Three Phase Simulink Simulation Model

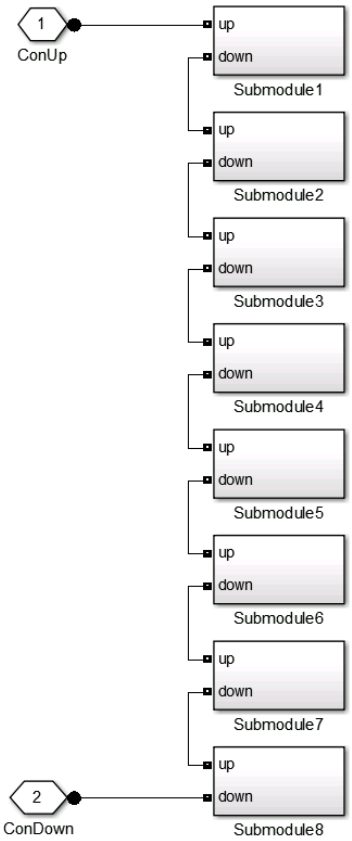


Figure A.2: Upper Arm of the Simulation Model

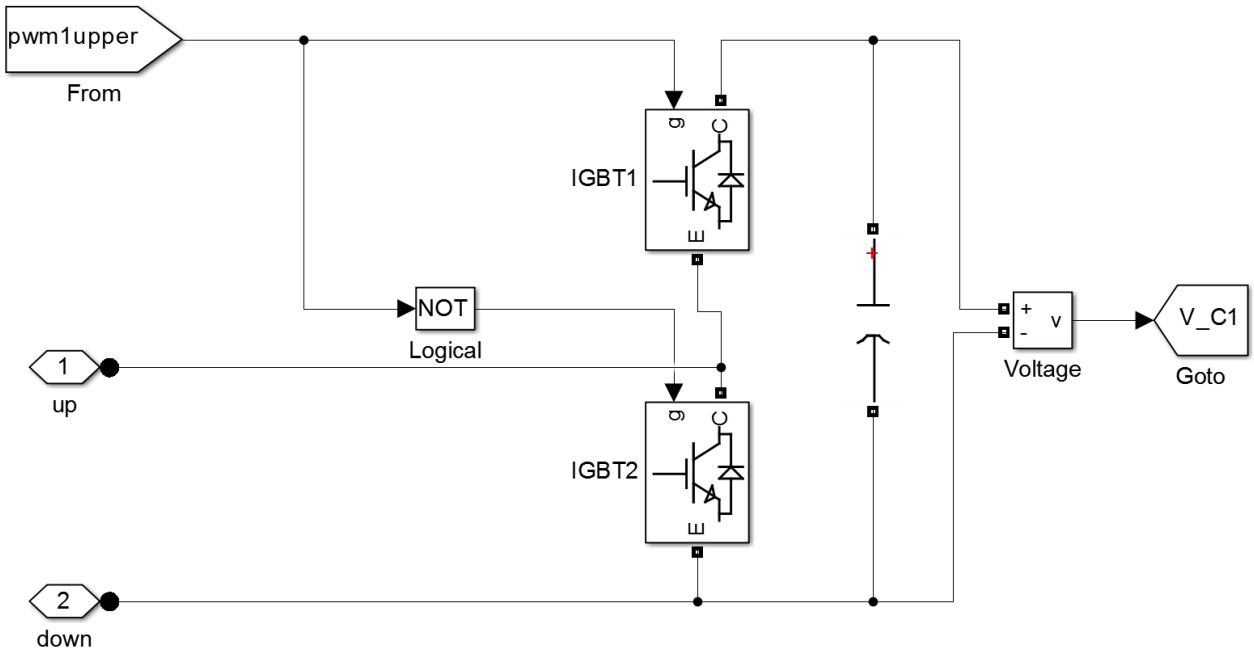


Figure A.3: The Simulation Model Submodule

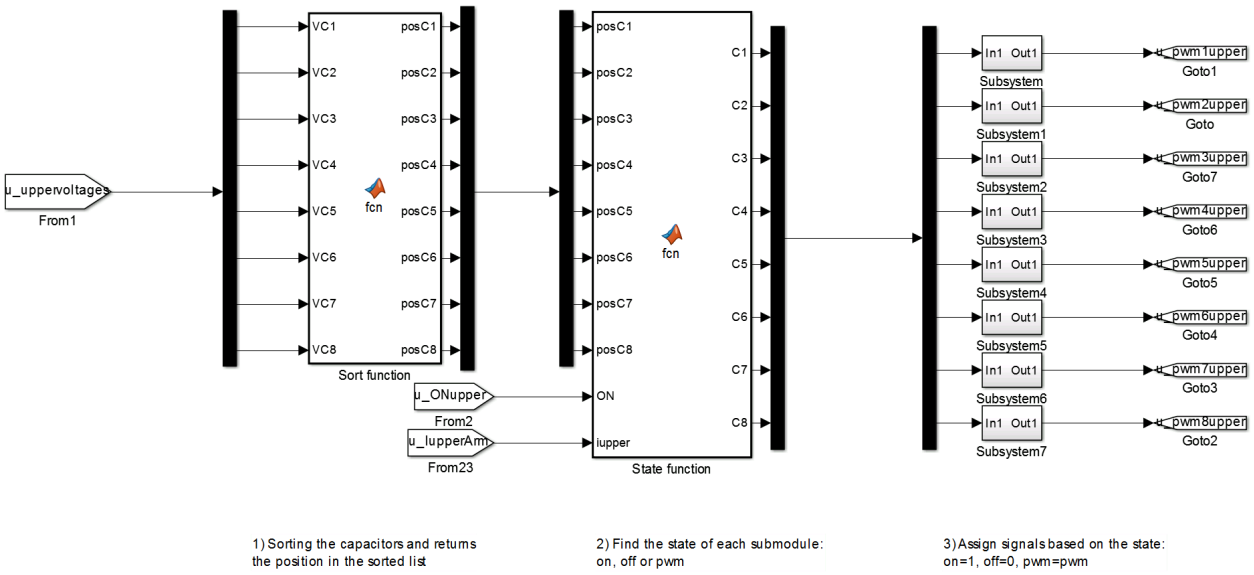


Figure A.4: Simulation Model Implementation of the Sorting Algorithm for the u-phase Upper Arm

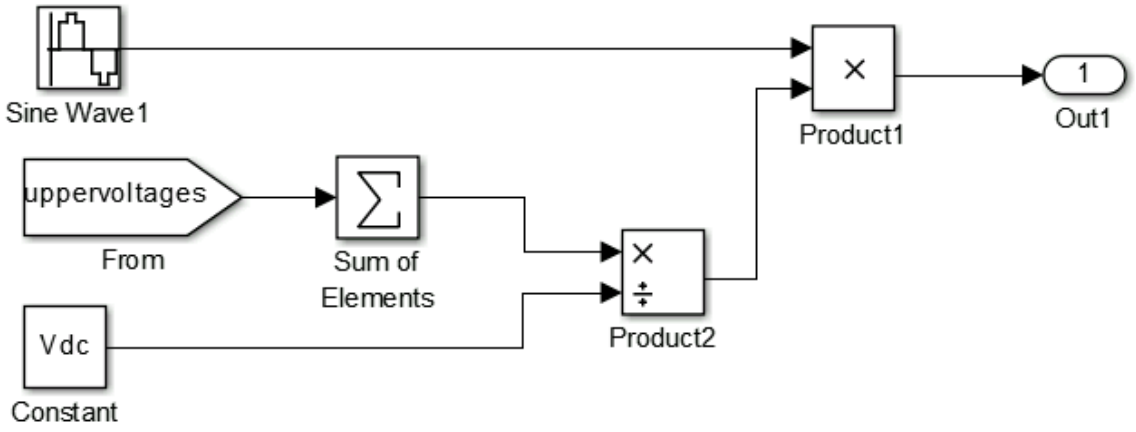


Figure A.5: Implementation of the 2^{nd} harmonic minimization strategy proposed by Nademi [1]

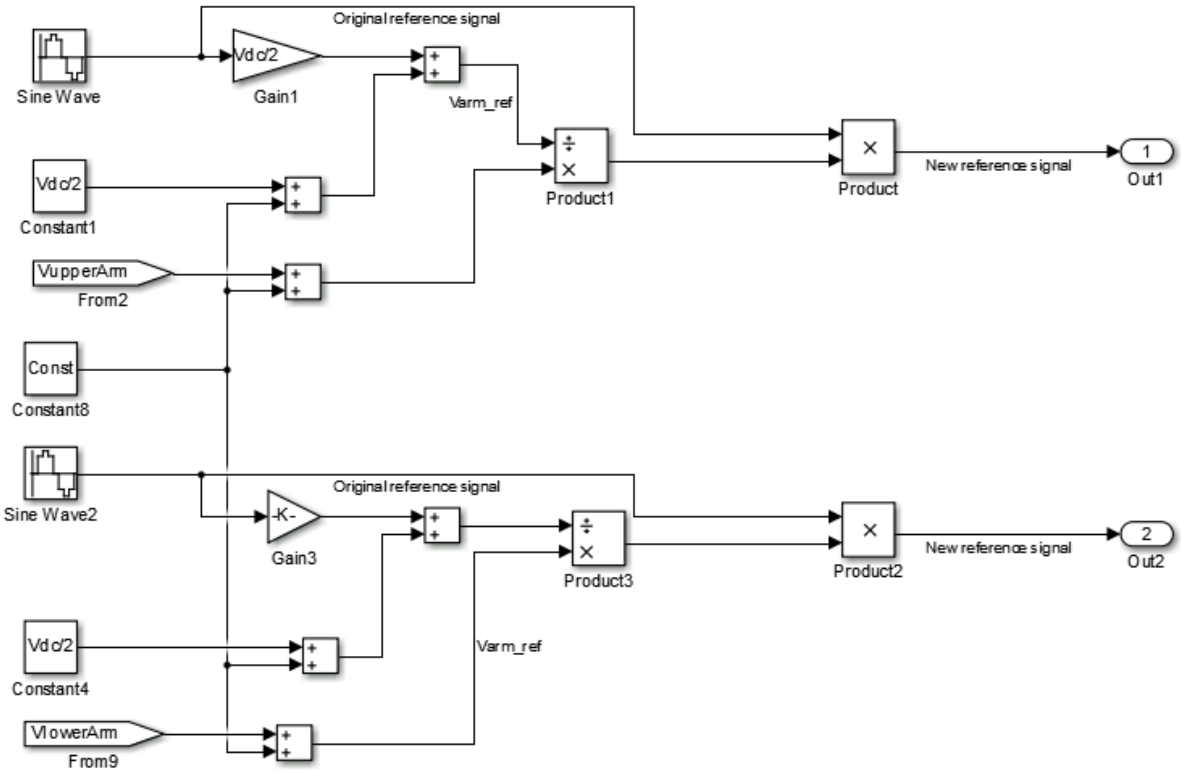


Figure A.6: Implented CCSC based on arm voltage relationship

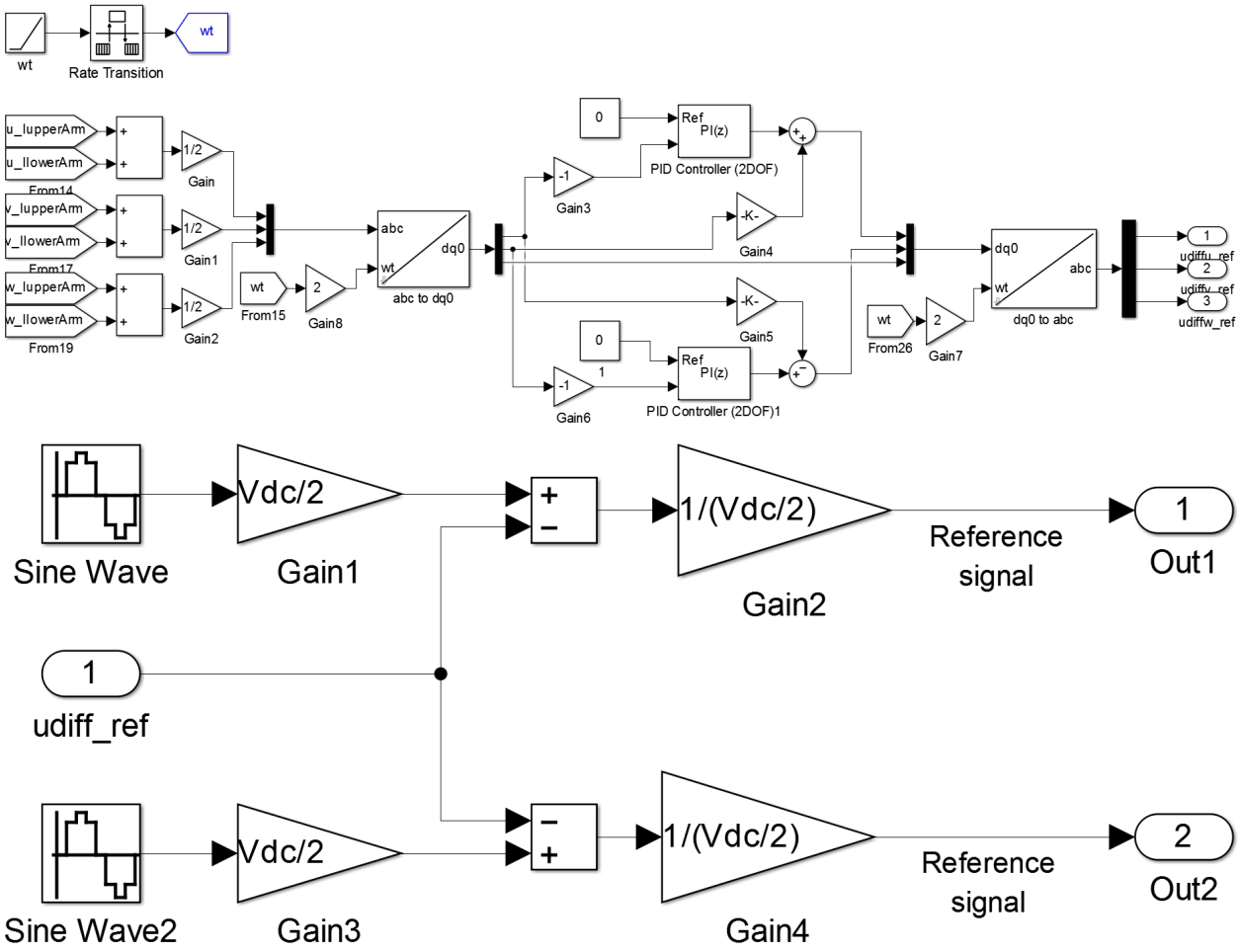


Figure A.7: Implementation of CCSC proposed by Tu et al. [2]

Appendix B

Matlab Simulink Functions

```
1      function [posC1,posC2,posC3,posC4,posC5,posC6,posC7,posC8] =
2      fcn(VC1,VC2,VC3,VC4,VC5,VC6,VC7,VC8)
3  %#codegen
4
5  %This function takes the capacitor voltages VC1-VC8 and sorts them by
6  %voltage level. It then returns the position of the capacitor in the sorted
7  %list. So if capacitor C5 has the 3rd lowest voltage, posC5 returns the
8  %number 3.
9
10 voltages=[VC1,VC2,VC3,VC4,VC5,VC6,VC7,VC8];
11 [b,I]=sort(voltages);
12
13 x=1;
14 posC1=x;posC2=x;posC3=x;posC4=x;posC5=x;posC6=x;posC7=x;posC8=x;
15
16 i=1;
17 while i<=8
18     if I(i)==1
19         posC1=i;
20     elseif I(i)==2
21         posC2=i;
22     elseif I(i)==3
23         posC3=i;
24     elseif I(i)==4
25         posC4=i;
26     elseif I(i)==5
27         posC5=i;
28     elseif I(i)==6
29         posC6=i;
30     elseif I(i)==7
31         posC7=i;
32     elseif I(i)==8
33         posC8=i;
```

```
    end
    i=i+1;
end
```

```
    function [C1,C2,C3,C4,C5,C6,C7,C8]  =
     fcn(posC1,posC2,posC3,posC4,posC5,posC6,posC7,posC8,ON,iupper)
%#codegen

%This function returns the state of the submodule. It returns 1 for
%on-state, 2 for PWM-state and 3 for off-state.

%Positive arm current:
%The function will return 1 for the capacitors lower on the sorted list
%than the required number of capacitors. For the capacitor with the same
%position on the sorted list as the required number of capacitors, the
%function will return 2. For the others, the function will return 3.

%So if the required number of capacitors is 5, the four capacitors with
%lowest values will be returned with 1, the 5th lowest value will be
%returned with 2, and the 6th-8th lowest values will be returned with 3.

%Negative arm current:
%The same procedure, buth the instead of prioritizing the submodules with
%the lowest capacitor level, it prioritizes the submodules with the
%highest capacitor voltage levels.

%% 1
if iupper>=0
    if posC1<ON
        C1=1;
    elseif posC1==ON
        C1=2;
    else
        C1=3;
    end
else
    if posC1>(9-ON)
        C1=1;
    elseif posC1==(9-ON)
        C1=2;
    else
        C1=3;
    end
end

%% 2
if iupper>=0
    if posC2<ON
```

```
45          C2=1;
46      elseif posC2==ON
47          C2=2;
48      else
49          C2=3;
50      end
51  else
52      if posC2>(9-ON)
53          C2=1;
54      elseif posC2==(9-ON)
55          C2=2;
56      else
57          C2=3;
58      end
59  end
60  %% 3
61  if iupper>=0
62      if posC3<ON
63          C3=1;
64      elseif posC3==ON
65          C3=2;
66      else
67          C3=3;
68      end
69  else
70      if posC3>(9-ON)
71          C3=1;
72      elseif posC3==(9-ON)
73          C3=2;
74      else
75          C3=3;
76      end
77  end
78
79  %% 4
80  if iupper>=0
81      if posC4<ON
82          C4=1;
83      elseif posC4==ON
84          C4=2;
85      else
86          C4=3;
87      end
88  else
89      if posC4>(9-ON)
90          C4=1;
91      elseif posC4==(9-ON)
92          C4=2;
93      else
```

```
94          C4=3;
95      end
96  end
97
98  %% 5
99  if iupper>=0
100     if posC5<ON
101         C5=1;
102     elseif posC5==ON
103         C5=2;
104     else
105         C5=3;
106     end
107 else
108     if posC5>(9-ON)
109         C5=1;
110     elseif posC5==(9-ON)
111         C5=2;
112     else
113         C5=3;
114     end
115 end
116
117 %% 6
118 if iupper>=0
119     if posC6<ON
120         C6=1;
121     elseif posC6==ON
122         C6=2;
123     else
124         C6=3;
125     end
126 else
127     if posC6>(9-ON)
128         C6=1;
129     elseif posC6==(9-ON)
130         C6=2;
131     else
132         C6=3;
133     end
134 end
135
136 %% 7
137 if iupper>=0
138     if posC7<ON
139         C7=1;
140     elseif posC7==ON
141         C7=2;
142     else
```

```
143         C7=3;
144     end
145 else
146     if posC7>(9-ON)
147         C7=1;
148     elseif posC7==(9-ON)
149         C7=2;
150     else
151         C7=3;
152     end
153 end
154
155 %% 8
156 if iupper>=0
157     if posC8<ON
158         C8=1;
159     elseif posC8==ON
160         C8=2;
161     else
162         C8=3;
163     end
164 else
165     if posC8>(9-ON)
166         C8=1;
167     elseif posC8==(9-ON)
168         C8=2;
169     else
170         C8=3;
171     end
172 end
```

Appendix C

Plots

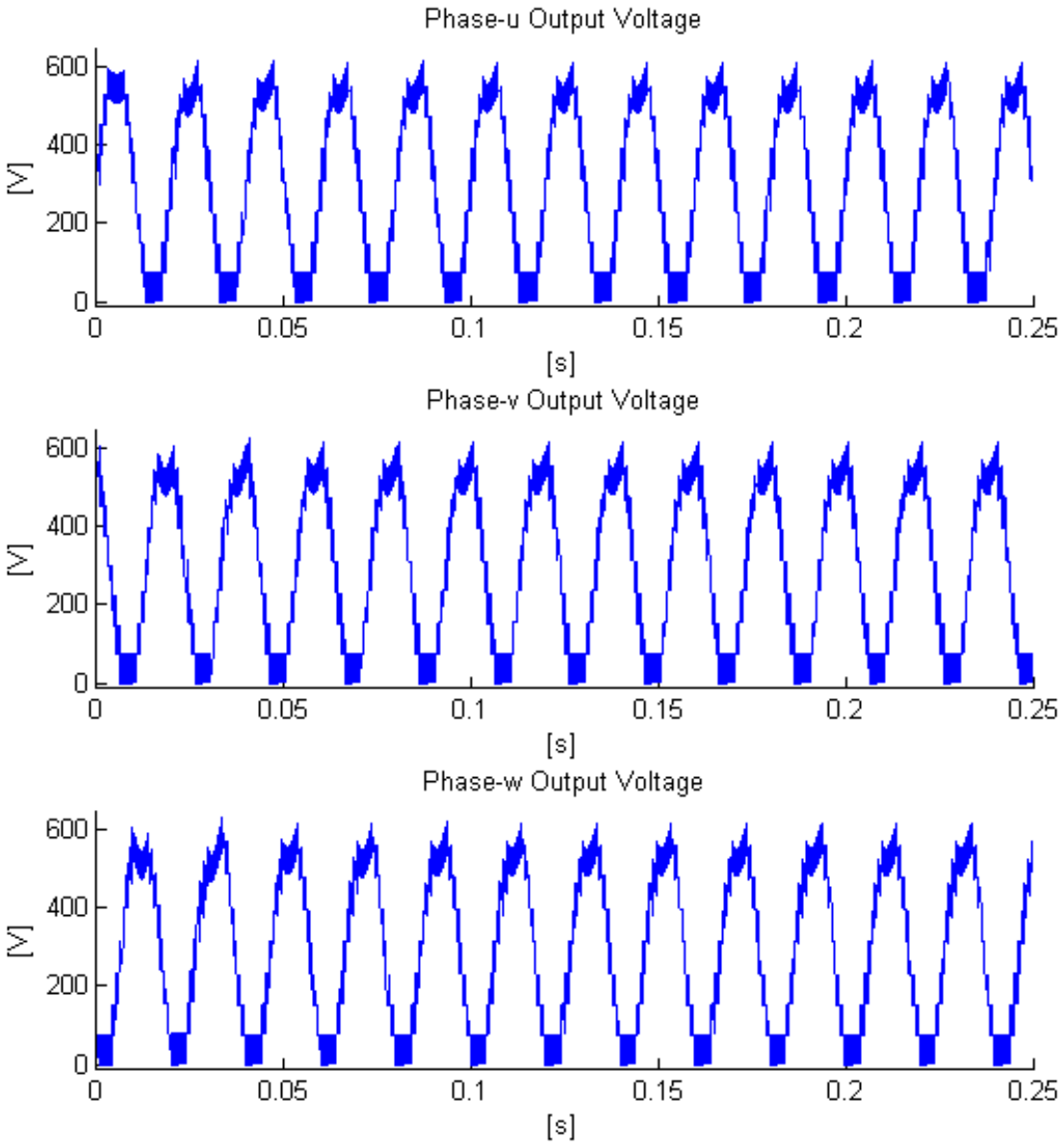


Figure C.1: Output Voltages When No CCSCs are Implemented

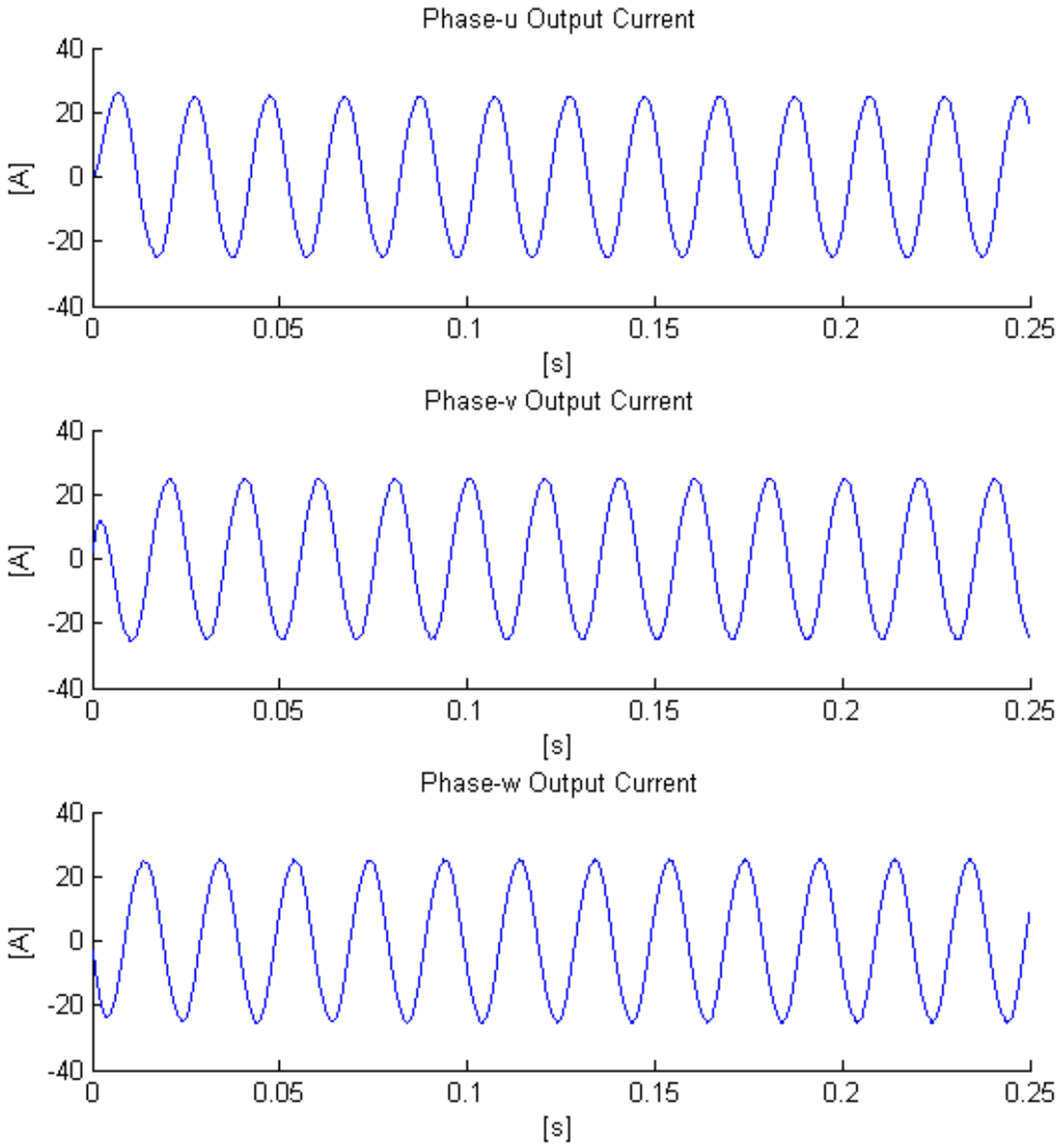


Figure C.2: Output Currents When No CCSCs are Implemented

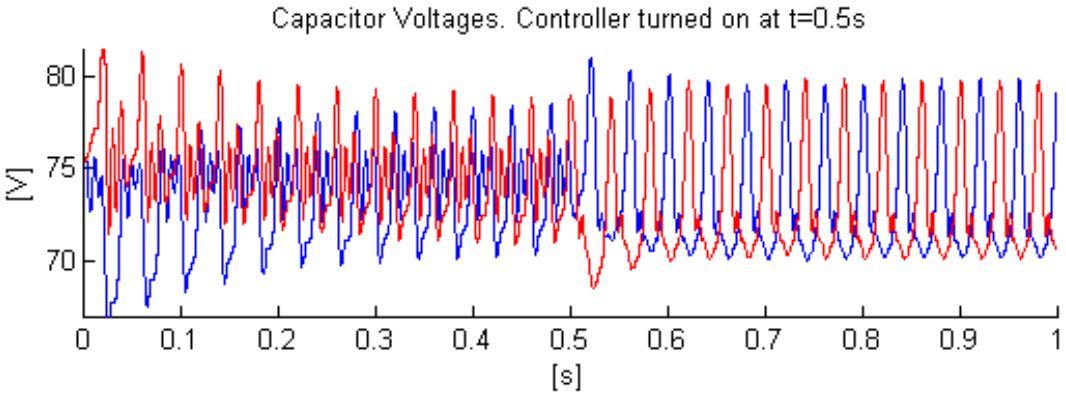


Figure C.3: Submodule Capacitor Voltages Using the CCSC proposed by Nademi [1], $f = 25Hz$

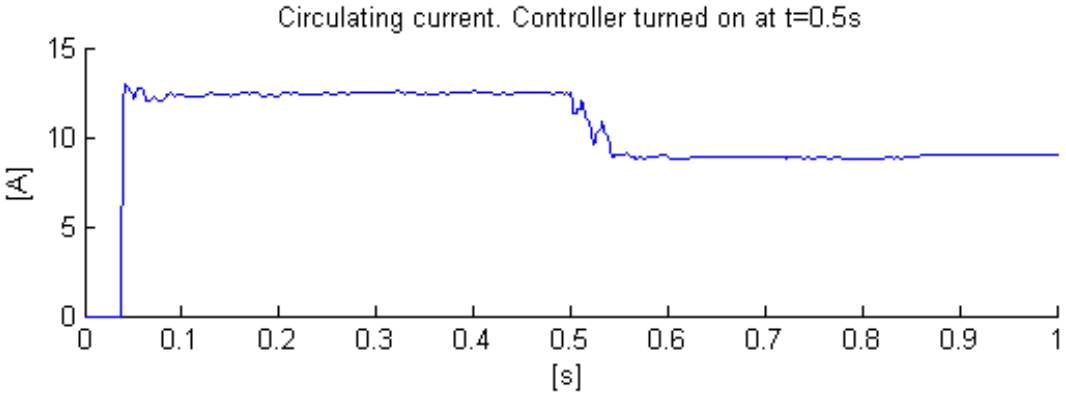


Figure C.4: 2^{nd} Harmonic Arm Current Using the CCSC proposed by Nademi [1], $f = 25Hz$

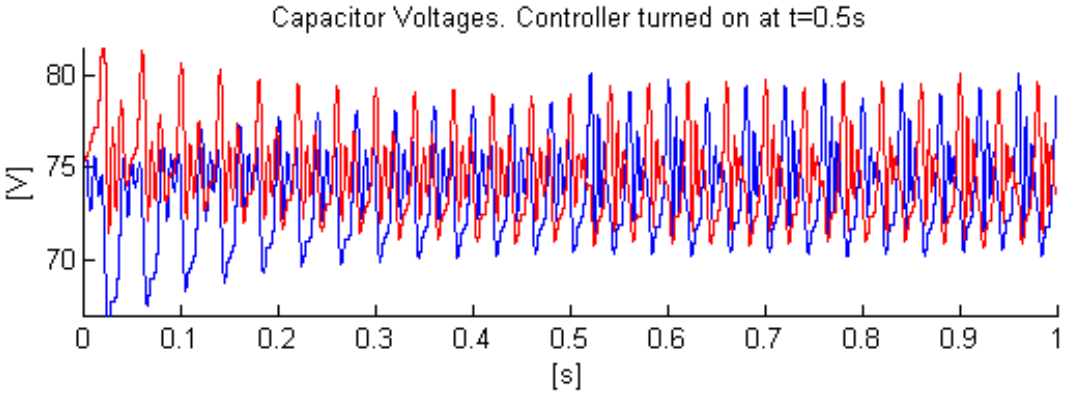


Figure C.5: Submodule Capacitor Voltages Using the CCSC based on Arm Voltage Comparison, $f = 25Hz$

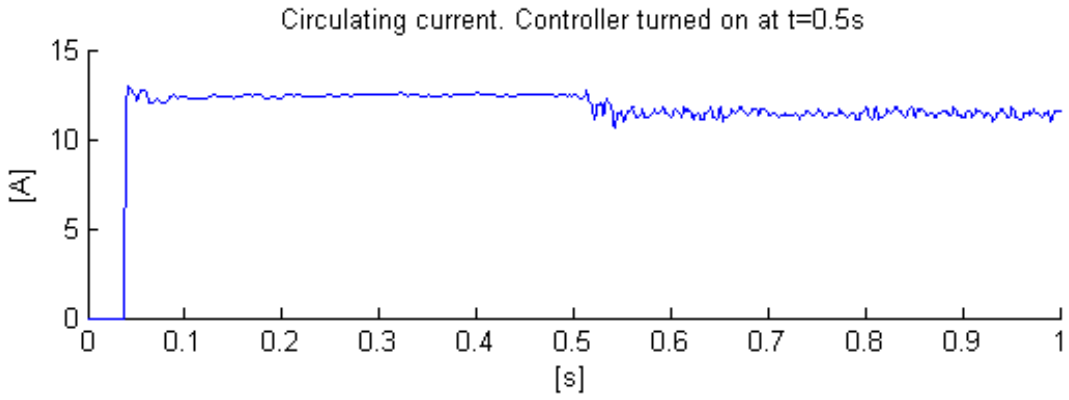


Figure C.6: 2^{nd} Harmonic Arm Current Using the CCSC based on Arm Voltage Comparison, $f = 25Hz$

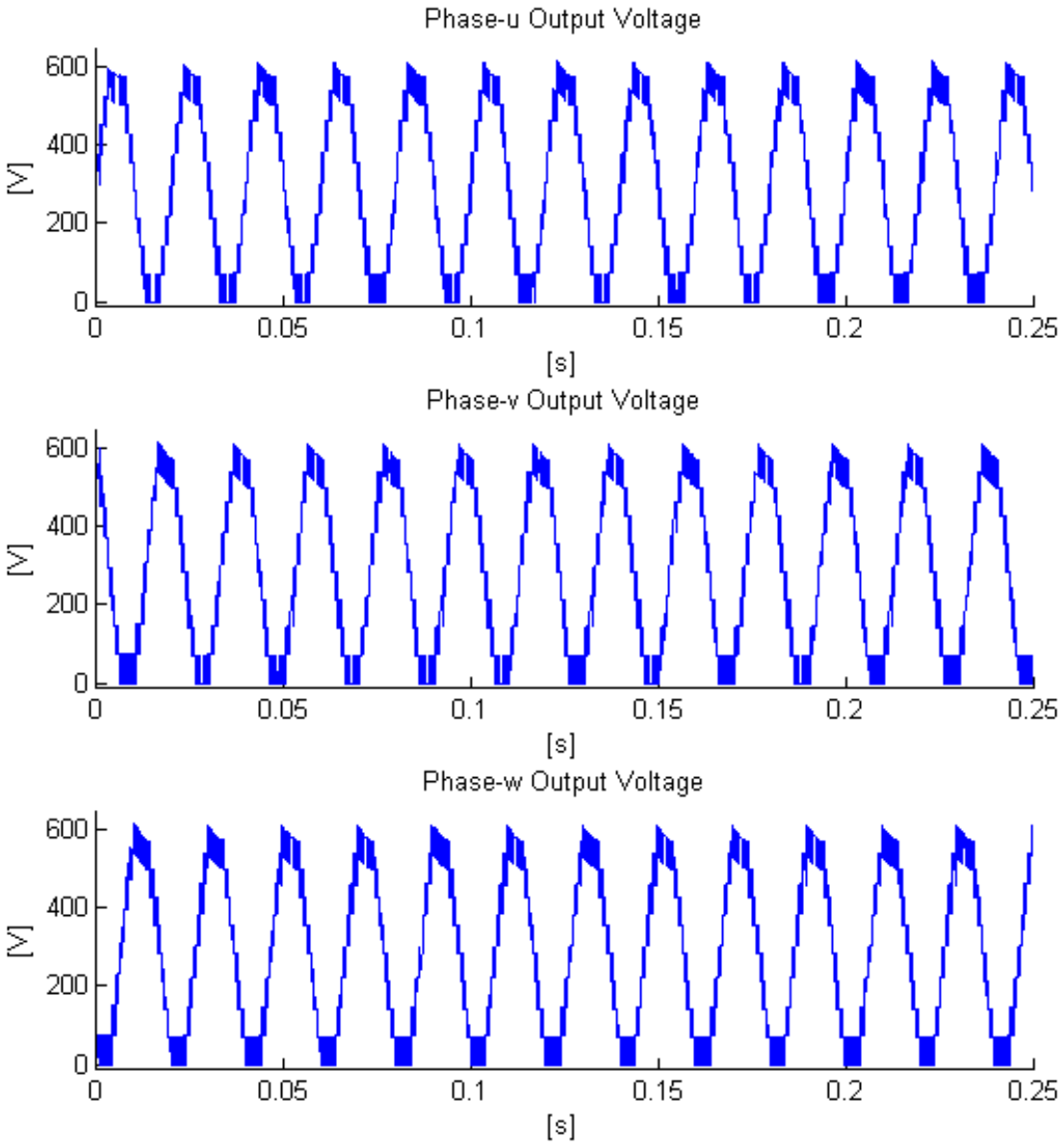


Figure C.7: Output Voltages Using the CCSC proposed by Tu et al. [2]

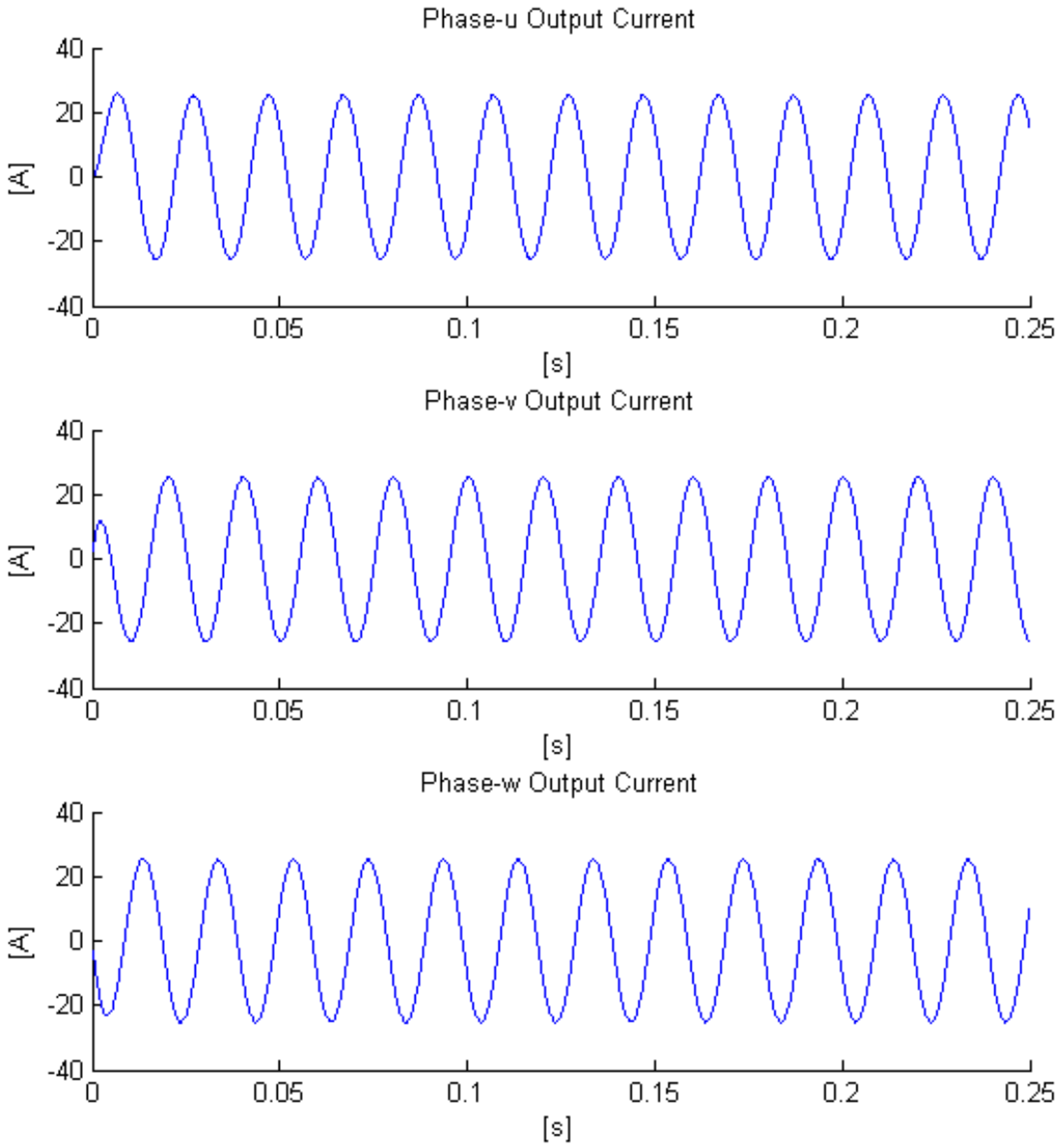


Figure C.8: Output Currents Using the CCSC proposed by Tu et al. [2]

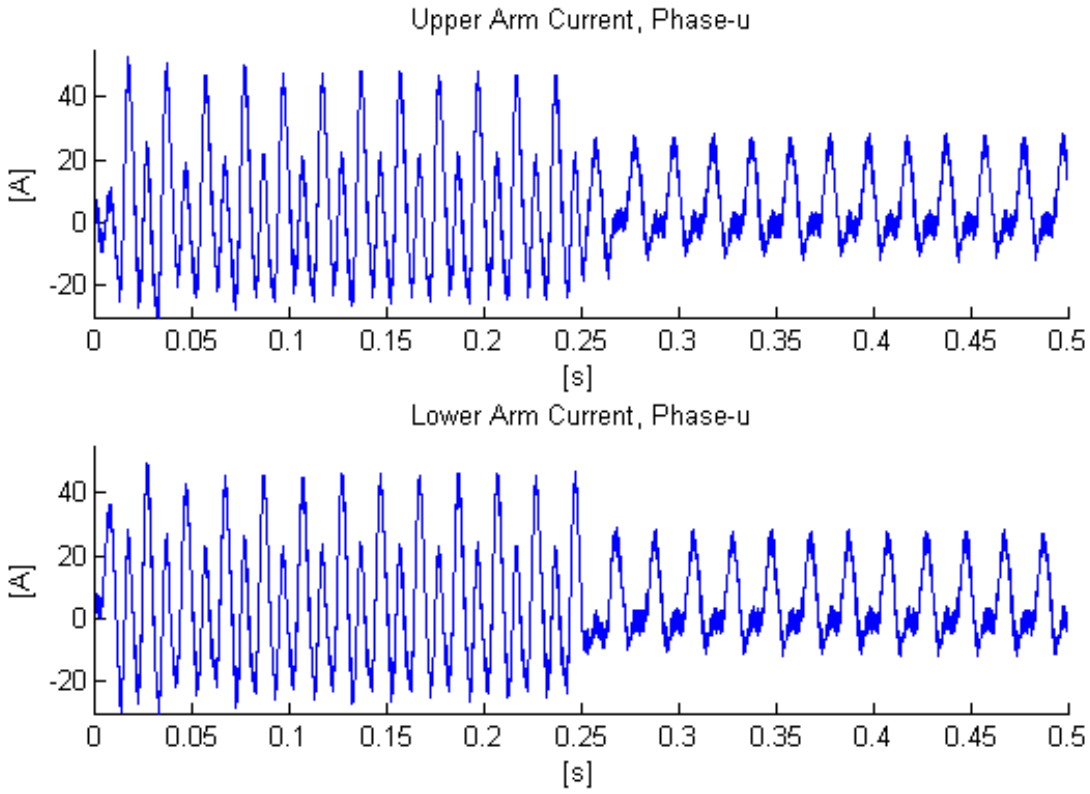


Figure C.9: Upper and Lower Phase-u Arm Currents Using the CCSC proposed by Tu et al. [2]

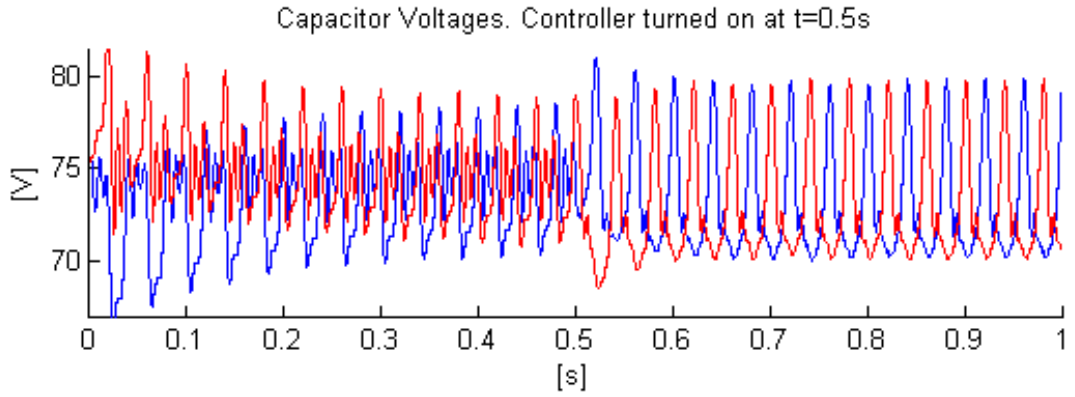


Figure C.10: Submodule Capacitor Voltages Using the CCSC Proposed by Tu et al. [2], $f = 25Hz$

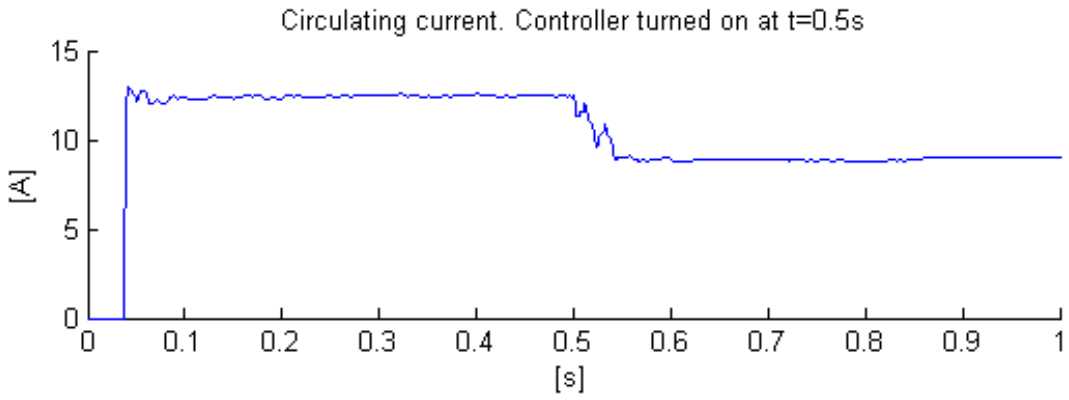


Figure C.11: 2^{nd} Harmonic Arm Current Using the CCSC Proposed by Tu et al. [2], $f = 25Hz$

Bibliography

[1] H. Nademi, "Advanced control of power converters: Modular multilevel converter," Ph.D. dissertation, Norwegian University of Science and Technology, NTNU, 2014.

[2] Q. Tu, Z. Xu, and L. Xu, "Reduced switching-frequency modulation and circulating current suppression for modular multilevel converters," *Power Delivery, IEEE Transactions on*, vol. 26, no. 3, pp. 2009–2017, July 2011.

[3] B. Gemmell, J. Dorn, D. Retzmann, and D. Soerangr, "Prospects of multilevel vsc technologies for power transmission," in *Transmission and Distribution Conference and Exposition, 2008. T #x00026;D. IEEE/PES*, April 2008, pp. 1–16.

[4] M. Hagiwara and H. Akagi, "Control and experiment of pulsewidth-modulated modular multilevel converters," *Power Electronics, IEEE Transactions on*, vol. 24, no. 7, pp. 1737–1746, July 2009.

[5] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard, and P. Barbosa, "Operation, control, and applications of the modular multilevel converter: A review," *Power Electronics, IEEE Transactions on*, vol. 30, no. 1, pp. 37–53, Jan 2015.

[6] C. J. Cowie. (2005) A circuit diagram of a three-phase variable frequency drive (vfd). [Online]. Available: http://commons.wikimedia.org/wiki/File:PWM_VFD_Diagram.png

[7] A. Antonopoulos, L. Angquist, S. Norrga, K. Ilves, L. Harnefors, and H.-P. Nee, "Modular multilevel converter ac motor drives with constant torque from zero to nominal speed," *Industry Applications, IEEE Transactions on*, vol. 50, no. 3, pp. 1982–1993, May 2014.

[8] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *Power Tech Conference Proceedings, 2003 IEEE Bologna*, vol. 3, June 2003, pp. 6 pp. Vol.3–.

[9] H. Liu, P. C. Loh, and F. Blaabjerg, "Generalized modular multilevel converter and modulation," in *Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE-ASIA), 2014 International*, May 2014, pp. 1634–1638.

[10] J. Kolb, F. Kammerer, and M. Braun, "Dimensioning and design of a modular multilevel converter for drive applications," in *Power Electronics and Motion Control Conference (EPE/PEMC), 2012 15th International*, Sept 2012, pp. LS1a–1.1–1–LS1a–1.1–8.

[11] S. Debnath, J. Qin, and M. Saeedifard, "Control and stability analysis of modular multilevel converter under low-frequency operation," *Industrial Electronics, IEEE Transactions on*, vol. PP, no. 99, pp. 1–1, 2015.

[12] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. Franquelo, B. Wu, J. Rodriguez, M. Perez, and J. Leon, "Recent advances and industrial applications of multilevel converters," *Industrial Electronics, IEEE Transactions on*, vol. 57, no. 8, pp. 2553–2580, Aug 2010.

[13] K. Ilves, A. Antonopoulos, L. Harnefors, S. Norrga, L. Angquist, and H.-P. Nee, "Capacitor voltage ripple shaping in modular multilevel converters allowing for operating region extension," in *IECON 2011 - 37th Annual Conference on IEEE Industrial Electronics Society*, Nov 2011, pp. 4403–4408.

[14] W. Li, L.-A. Gregoire, and J. Bélanger, "Control and performance of a modular multilevel converter system," in *CIGRÉ Canada, Conference on Power Systems, Halifax*, 2011.

[15] S. Li and T. Haskew, "Analysis of decoupled d-q vector control in dfig back-to-back pwm converter," in *Power Engineering Society General Meeting, 2007. IEEE*, June 2007, pp. 1–7.

[16] M. Rajan and R. Seyezhai, "Comparative study of multicarrier pwm techniques for a modular multilevel inverter," *International Journal of Engineering and Technology*, 2013.

[17] J. Colmenares, "Analysis, implementation and experimental evaluation of a phase shifted pwm control system for a modular multilevel converter," 2011.

[18] S. Fan, K. Zhang, J. Xiong, and Y. Xue, "An improved control system for modular multilevel converters with new modulation strategy and voltage balancing control," *Power Electronics, IEEE Transactions on*, vol. 30, no. 1, pp. 358–371, Jan 2015.

[19] K. Wang, Y. Li, Z. Zheng, and L. Xu, "Voltage balancing and fluctuation-suppression methods of floating capacitors in a new modular multilevel converter," *Industrial Electronics, IEEE Transactions on*, vol. 60, no. 5, pp. 1943–1954, May 2013.

[20] ABB, "Variable-speed drive abb technology guide," 2011.

[21] B. Mecrow and A. Jack, "Efficiency trends in electric machines and drives," *Energy Policy*, vol. 36, no. 12, pp. 4336–4341, 2008.

[22] A. Antonopoulos, L. Angquist, L. Harnefors, and H.-P. Nee, "Optimal selection of the average capacitor voltage for variable-speed drives with modular multilevel converters," *Power Electronics, IEEE Transactions on*, vol. 30, no. 1, pp. 227–234, Jan 2015.

[23] H. Abu-Rub, J. Holtz, J. Rodriguez, and G. Baoming, "Medium-voltage multilevel converters x2014;state of the art, challenges, and requirements in industrial applications," *Industrial Electronics, IEEE Transactions on*, vol. 57, no. 8, pp. 2581–2596, Aug 2010.

[24] M. Hiller, D. Krug, R. Sommer, and S. Rohner, "A new highly modular medium voltage converter topology for industrial drive applications," in *Power Electronics and Applications, 2009. EPE '09. 13th European Conference on*, Sept 2009, pp. 1–10.

[25] Q. Tu, Z. Xu, H. Huang, and J. Zhang, "Parameter design principle of the arm inductor in modular multilevel converter based hvdc," in *Power System Technology (POWERCON), 2010 International Conference on*, Oct 2010, pp. 1–6.

[26] M. Hagiwara, K. Nishimura, and H. Akagi, "A medium-voltage motor drive with a modular multilevel pwm inverter," *Power Electronics, IEEE Transactions on*, vol. 25, no. 7, pp. 1786–1799, July 2010.

[27] A. Korn, M. Winkelnkemper, and P. Steimer, "Low output frequency operation of the modular multi-level converter," in *Energy Conversion Congress and Exposition (ECCE), 2010 IEEE*, Sept 2010, pp. 3993–3997.

[28] M. Hagiwara, I. Hasegawa, and H. Akagi, "Startup and low-speed operation of an adjustable-speed motor driven by a modular multilevel cascade inverter (mmci)," in *Energy Conversion Congress and Exposition (ECCE), 2012 IEEE*, Sept 2012, pp. 718–725.

[29] L. Angquist, A. Antonopoulos, D. Siemaszko, K. Ilves, M. Vasiladiotis, and H.-P. Nee, "Open-loop control of modular multilevel converters using estimation of stored energy," *Industry Applications, IEEE Transactions on*, vol. 47, no. 6, pp. 2516–2524, Nov 2011.

[30] A. Antonopoulos, L. Angquist, and H.-P. Nee, "On dynamics and voltage control of the modular multilevel converter," in *Power Electronics and Applications, 2009. EPE '09. 13th European Conference on*, Sept 2009, pp. 1–10.

[31] I. R. Mosgren, "Fault taulerant modular multilevel converter," Master's thesis, Norwegian University of Science and Technology, NTNU, 2013.