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Power Cycle Testing of Press-Pack IGBT Chips

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Problem Description

Reliable power electronic components for high-power applications are desirable in an energy sector which is more and more dependent on power electronics. Press-pack housing of IGBTs is a packaging technology that enables design of converters with high power density, which is ideal for use in many renewable energy and smart grid applications.

Power cycle testing is an accelerated lifetime stress test ideal for testing the reliability of press-pack IGBTs. In a power cycle test, the test object is repeatedly temperature cycled from heat produced by the losses in the device. SINTEF Energy Research performed a power cycling test of high-power IGBT press-pack discs, it revealed that the devices had an unexpectedly short lifetime. The test also showed that the failure of the devices was caused by failure of only one or two chips in certain positions inside the disc.

To investigate if the short power cycling lifetime of the press-pack disks is caused by excessive stress on chips in certain positions, chips from an IGBT press-pack should be power cycled individually. Equipment for power cycle testing individual IGBT chips removed from a press-pack disk should therefore be developed. The power cycle tester must be able to create a stress level at least as high as SINTEF used when power cycling press-pack disks. The tester must also be able to precisely measure temperature and on-state voltage of IGBT chip during power cycling. In order to determine the lifetime of an IGBT chip, continuous power cycling for several days or weeks must be performed. Therefore the power cycle tester must be developed so that continuous unsupervised testing can be performed in a safe manner.

The goal is to determine if press-pack IGBT chips have a longer power cycling lifetime than press-pack IGBT discs.

Assignment given: Trondheim 13.01.2014
Supervisor: Tore Marvin Undeland

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Preface

This master thesis is the final achievement of my master studies at the Department of Electrical Engineering at NTNU. My involvement in the development of the single chip power cycle tester started in my summer job as a research trainee at SINTEF Energy Research in 2013. The development of the tester continued in my specialization project and was finalized as a part of this thesis. The development and utilization of the single chip power cycle tester, have therefore been an extensive work lasting for almost a year. The work have been both interesting and challenging. Much time have been spent in the laboratory to develop a tester that actually works, and is able to provide sufficient stress to the IGBT chips. For the laboratory work in the winter and spring of 2014, a large part of the time was dedicated to ensure safe operation. Run-in-testing to ensure that the results are reasonable and reliable have also been very time consuming.

First I would like to thank Atle Rygg Årdal, his support and dedicated involvement in my specialization project and master thesis have been truly invaluable. I would also like to thank Magnar Hernes for highly needed help and support.

Lukas Tinschert gave me crucial help in developing the single-chip tester and valuable feedback during the finalization of this report, both which I am truly grateful.

I feel honoured and are very grateful to have had Prof. Tore Undeland as my supervisor. His professional interest and personal dedication to all his master-students is exceptional.

Finally I would like to thank my fiancée for always being patient and supportive, not only during the work with my master thesis, but during my entire studies at NTNU.

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Abstract

In this thesis the power cycling capability of individual press-pack IGBT chips is investigated. Press-pack is a packaging technology used for power semiconductors. For press-packs, both thermal and electrical contact to the semiconductor chip is obtained by the application of force on the package. Press-pack IGBTs is claimed by the manufacturers to be especially suitable for high-power applications with large variations in power output. Power cycle testing is an accelerated lifetime stress test, ideal for assessing the lifetime of components in such applications. In power cycle testing, a component is thermally cycled by on-state-losses from a current repeatedly turned on and off.

SINTEF Energy Research have in cooperation with Technical University of Chemnitz developed a 2000 A power cycle tester. Power cycling of press-pack IGBT discs in this tester revealed an unexpectedly short power cycling lifetime. To obtain a sufficiently high current rating, press-pack IGBT discs consist of many paralleled IGBT chips. SINTEFs hypothesis is that changes in the internal pressure distribution, caused by deformation of the press-pack housing during power cycling, have caused a destructive stress level for IGBT chips in certain positions inside the press-pack.

To investigate this hypothesis, test equipment for power cycling individual IGBT chips removed from press-pack discs have been developed in this master thesis. Two IGBT chips have been continuously power cycled for a considerable number of cycles under tough conditions. The results supports the hypothesis that the early failure of press-pack discs is caused by excessive stress on chips in certain locations. Since the lifetime of the individual chips was found to be 10 - 50 times longer than that of press-pack discs tested under similar stress, this conclusion is justified.

Sammendrag

I denne masteroppgaven har press-pack IGBT brikker sin holdbarhet mot power-cycling blitt undersøkt. Press-pack er en innpakningsteknologi for effekthalvledere. I en press-pack blir både den termiske og elektriske kontakten til effekthalvlederbrikken etablert ved å påføre en ytre kraft på komponenten. I følge produsentene er press-pack IGBTer spesielt egnet for applikasjoner med høy effekt og store variasjoner. En power-cycling test er en akselerert levetidstest og ansees å være ideell for å vurdere levetiden til komponenter i slike applikasjoner. Under en power-cycling test blir en komponent termisk syklet av varmen fra ledetilstandstap generert av en strøm som kontinuerlig skrus av og på.

SINTEF Energi har i samarbeid med Technical University of Chemnitz utviklet en 2000 A power-cycling tester. Power-cycling av press-pack IGBT disker utført i denne testeren, avdekket at disse diskene hadde overraskende kort levetid. Press-pack IGBT disker består av mange parallell koplede IGBT brikker for å oppnå en tilstrekkelig høy merkestrøm. SINTEF sin hypotese er at endringer i den interne trykkfordelingen forårsaket av deformasjon av press-pack innpakningen under power-cycling, har ført til et kritisk høyt stressnivå for IGBT brikker i visse posisjoner inne i disken.

For å undersøke denne hypotesen, har det i arbeidet med denne masteroppgaven blitt utviklet testutstyr for power-cycle testing av individuelle IGBT brikker tatt fra en press-pack disk. To IGBT brikker har blitt kontinuerlig power-cyclet for et betydelig antall sykler under høyt stress. Resultatene støtter SINTEF sin hypotese om at den korte levetiden til press-pack diskene er forårsaket av at belastingen som blir påført enkelte brikker er for høy. Det faktum at levetiden til brikkene var 10 - 50 ganger lengre enn press-pack diskene, testet under lignende stress, rettferdiggjør en slik konklusjon.

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List of Acronyms

AI	Analog Input
cRIO	Compact Reconfigurable Input/Output
CTE	Coefficient of Thermal Expansion
DCB	Direct Copper Bonded
DUT	Device Under Test
ECC	Electrical Contact Conductance
FEM	Finite Element Method
FPGA	Field-Programmable Gate Array
GTO	Gate Turn-Off Thyristor
H3TRB	High Humidity High Temperature Reverse Bias Test
TGS	High Temperature Gate Stress Test
HTRB	High Temperature Reverse Bias Test
HTS	High Temperature Storage Test
HVDC	High Voltage Direct Current
I_C	Collector Current
I_{CES}	Collector Emitter Saturation Current
IEC	International Electrotechnical Commission
I_{GES}	Gate-Emitter Saturation Current
IGBT	Insulated Gate Bipolar Transistor
IV-characteristics	Current-Voltage Characteristics

LSL	Lower specification limit
LTS	Low Temperature Storage Test
MOSFET	Metal Oxide Field Effect Transistor
NI	National Instruments
OPE	Offshore Power Electronics
OPE Project	Power Electronics for Reliable and Energy Efficient Renewable Energy Systems Project
SCFM	Short Circuit Failure Mode
SCPCT	Single-Chip Power Cycle Tester
SVC	StaticVAR Compensation
TCC	Thermal Contact Conductance
TO	Test Object
T_{vj}	Virtual Junction Temperature
ΔT_{vj}	Virtual Junction Temperature Swing
$T_{vj,m}$	Medium Virtual Junction Temperature
$T_{vj,max}$	Maximum Virtual Junction Temperature
$T_{vj,min}$	Minimum Virtual Junction Temperature
TUC	Technical University of Chemnitz
PCT	Power Cycling Testing or Power Cycle Tester
R_{ge}	Gate-Emitter Resistance
R_{ce}	Collector-Emitter Resistance
R_{th}	Thermal Resistance
USL	Upper specification limit
V_{ce}	Collector-Emitter Voltage
$V_{ce,sat}$	Collector-Emitter Saturation Voltage (On-state voltage)
$V_{ce}(T) - method$	T_{vj} estimation method, using the temperature dependency of the collector-emitter voltage
$V_{GE(th)}$	Gate-Emitter Threshold Voltage

VI   Virtual Instrument

WD   Watch Dog

Chapter 1

Introduction

1.1 Background and Motivation

Intermittent power sources such as offshore wind power plays a critical role in reaching the EU2020 targets, and is an important step on the path to a sustainable future in a zero-carbon society [3]. The harsh offshore environment combined with long repair times due to inaccessibility, results in very strict requirements for reliability in offshore applications. Reliability testing is therefore of key importance for the success of the development of offshore wind power.

In large scale offshore wind power generation, it is expected that high voltage direct current (HVDC) will be used in the transmission of power to the onshore AC-grid [1]. AC- and DC- distribution systems will be used to connect individual wind turbines to the DC transmission lines. In this type of distribution systems power electronic converters will be an important component. All the power generated offshore, will flow through two or more power electronic converters before reaching the customers [1].

The Insulated Gate Bipolar Transistor (IGBT) have become the desired choice of semiconductor switch in high-power converters. Today, the module technology is the most common packaging method for high-power IGBTs. An emerging packaging technology for high-power IGBTs is the press-pack. In contrast to the soldered power modules, press-packs uses force to establish thermal and electrical contact, enabling double sided cooling. Press-pack manufacturers claim that their components are ideal for use in high-power applications, and applications with large variations in output power [4]. Energy conversion for renewable energy sources, is a typical application with a rapidly changing load profile.

Figure 1.1: Offshore wind turbine [1]

The difficulty of performing repair on offshore installations implies that any failure can lead to considerable downtime. It is therefore very important to conduct reliability testing of power electronic components used in offshore power production. Power cycling is an accelerated lifetime stress test, used to assess component lifetime in applications where large variations in the output power occur. It can therefore be used to assess the lifetime of press-pack IGBTs, in a stress similar to what offshore wind power conversion will generate. Power cycling can be particularity relevant for direct driven offshore wind turbines, the generator side converter can operate with a low frequency while have a high power output. That generates large thermal stress on the components in the converter.

This thesis will describe a power cycling test of press-pack IGBT chips, and how it is used to learn more about the power cycling lifetime of press-pack IGBTs.

1.2   Relation to Specialization Project

In 2013 the specialization project report "*Press-Pack Power Cycling - Power Cycle Tester for IGBT Press-Pack Chips*" was written [5] . Some of the material from that report have been used in this thesis. The following chapters are more or less directly taken from the specialization project report:

- Chapter 3.1 - Introduction

- Chapter 3.2 - Chip Related Tests

- Chapter 5.4 - Clamping Device for Individual Press-Pack Chips

In addition, some paragraphs in other sections originate from the specialization project, but the content is generally rewritten and restructured.

1.3   Outline of the Thesis

The following section explains the sequence of the contents.

A description of the IGBT, packaging concepts for IGBTs and how the junction temperature of an IGBT can be estimated using electrical measurements, is given in In *Chapter 2 - IGBT*. In *Chapter 3 - Accelerated Lifetime Stress Tests*, a description of different accelerated lifetime stress tests and power cycling in particular, is given.

The SINTEF 2000 A power cycle tester and results from power cycle testing of press-pack IGBT discs is presented in *Chapter 4 - SINTEF 2000 A Power Cycle Tester*.

The power cycle tester developed in this thesis is presented in *Chapter 5, Single-Chip Power Cycle Tester*. This chapter documents the tester and its limitations in detail. The chapter is partly written as documentation for further use of the single-chip tester.

In *Chapter 6 - Results* and *Chapter 7 - Discussion*, the results from the power cycle test of two individual IGBT chips is presented and discussed. The conclusion of the thesis is found in *Chapter 8 - Conclusion and Further Work*.

Chapter 2

IGBT

2.1 IGBT

The Insulated Gate Bipolar Transistor (IGBT) is a three-terminal power semi-conductor device. It is used as an electronic switch and allows a combination of high efficiency and fast switching. The IGBT is suitable for many applications in power electronics, like pulse width modulated three-phase variable speed drives, uninterruptible power supplies, switched-mode power supplies, high voltage direct current (HVDC) and other power circuits requiring high switch repetition rates.
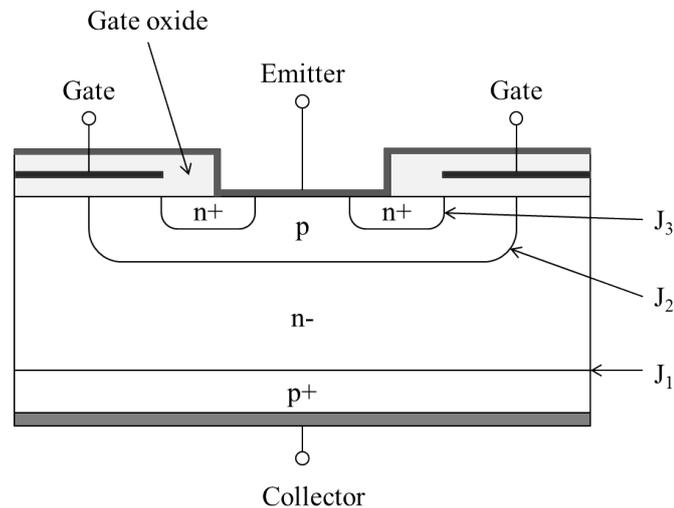
Figure 2.1: Layered schematics of an IGBT

Figure 2.1 illustrates a layered schematic of one cell in a typical IGBT design. It shows how the IGBT is a three terminal device, with connection points for gate, emitter and collector. The figure also shows how the gate on the IGBT is encapsulated in electrically insulating gate oxide.

An IGBT is turned off if the voltage between the gate and emitter is either negative or 0 V. If it is turned off, and the voltage at the emitter is more negative than at the collector, the device is in forward blocking mode. The pn-junction J_2 is then blocking, while the junctions J_1 and J_3 are conducting [6, p.40].

If a positive voltage is applied to the gate of the IGBT, it turns on and it transitions to forward conduction mode. It starts with the formation of a conducting channel in the p-region under the gate-oxide. The channel enables an electron current to flow from the emitter into the n^--base, leading to a reduction of the potential of the n^--base and opening of the J_1 pn-junction. Minority carriers (holes) are transported from the p^+-region to the n^--base. It leads to a concentration of holes in the n^--base, exceeding its doping level by several powers of magnitude. The high concentration of holes, cause electrons to move in great numbers from the emitter n^+-region to the n^--base to maintain charge neutrality. The inflow of charge carriers to the low doped, and therefore high impedance, n^--base increases its conductivity dramatically. This effect is called conductivity modulation, and greatly reduces the collector-emitter on-state voltage drop of the IGBT [6, p.40].

For high-voltage applications, an IGBT will due to the conductivity modulation have much lower conduction loss than a comparable MOSFET. The conductivity modulation enables the combination of high blocking voltage and low on-state resistivity. The switching of an IGBT is controlled by the voltage at the gate, that enables fast switching and simple drive circuits [6, p.40].

2.2   IGBT Packaging Technology

The active structure of an IGBT is placed on a silicon chip. As the semiconductor chip cannot be used in any converter application directly, packaging to enable practical use of the electrical properties of the chip is necessary. A power semiconductor component is therefore one or more semiconductor chips in a package. The package and connection technology, is just as important as the characteristics of the power semiconductor [6, p.66]

A high-power IGBT have a low on-state voltage, which reduces the conduction losses. The sum of conduction losses and switching losses can however, depending on the component and the application, be from a few hundred watts to several

kilowatts. The package must therefore be designed in a way that can transport the heat from these losses away from the chip, ensuring the temperature of the chip remains within the given limits. A power semiconductor package must have high reliability, meaning long lifetime in an application, and therefore a high durability under alternating load conditions [7, p.344]. Further the package must also provide high electrical conductivity to avoid undesirable electrical properties like parasitic resistance, parasitic capacitance and parasitic inductance [7, p.344].

For conventional power semiconductors like thyristors and GTOs, each semiconductor chip can be made much larger than what is possible for IGBTs. For an Infineon thyristor press-packs for HVDC applications, with a rated current of 5.6 kA and a blocking voltage of 8 kV, the semiconductor is one wafer with a diameter of approximately 150 mm [7, p.345]. The size of a modern IGBT chip from ABB with a blocking voltage of 4.5 kV and a rated current of 55 A, is 14.30x14.30 mm [8]. That means that the thyristor semiconductor wafer is approximately 85 times lager than the IGBT chip. Currently, IGBT components cannot be made with either blocking voltage or current rating in the range of the mentioned thyristor. The comparison of the size shows one very important point; to obtain a useful power rating, enabling use of IGBTs in high power applications, paralleling many IGBT chips is necessary. One reason for the limitation in IGBT chip size, is that the high cell density in modern IGBT chips would result in a yield problem due to single cell defects when the chip size increase [7, p.347].

Luckily, due to the positive temperature coefficient of its on-state resistance in the high current range, the IGBT is an ideal component for parallel connection. If one of the paralleled IGBTs conduct a higher current than the others, its temperature will increase leading to higher resistance. The increased resistance will in turn decrease the current, hence there is a thermal stabilization effect. The advantage of easy paralleling of IGBTs, together with the thermal disadvantages of large chip area does not produce a marked for production of larger IGBT chips [7, p.347].

IGBT components currently available, have switching power capability from 100 W to several MWs, and blocking voltage from 600 V to 6.5 kV [6, p.66]. Due to the large variety in both power and voltage rating, a large number of different IGBT components are produced. Different packaging technologies are used for different power levels and blocking voltages.

For low power and low bocking voltage, discrete packaging methods like the transistor outline (TO) package is most common. In a discrete package each component contains one circuit element that performs a single function. These packages are soldered to power circuit boards [7, p.345].

For IGBTs with high blocking voltage and high power ratings, power-modules and

press-packs are used. The next chapters will give a more detailed explanation of these packaging technologies.

In the description of IGBT packaging technologies in the next chapters, the focus will be on their power cycling capability. A more elaborate explanation of the power cycle testing will be given in chapter 3.4. To emphasize the focus of the next chapters a brief introduction to power cycling is given now. Power cycle testing is an accelerated lifetime stress test where the component is thermally cycled. Losses generated by conducting a load current through the IGBT is the heat-source for the thermal cycling. The stress level of a power cycle test is typically described by the maximum chip temperature during a cycle, and the difference between the minimum and maximum temperature, the temperature swing. Power cycle testing simulates in an accelerated manner, the stress a component experiences under cyclic load conditions.

2.3   IGBT Modules

Power semiconductor modules are in particular characterized by their electrically insulated architecture. The components in the electrical circuit of an IGBT module are electrically insulated from the heat sink the module is mounted on [7, p.346].

Unlike discrete packaging methods, where each component only serve one electrical function, a module component can due to its insulated architecture contain advanced electrical circuits. A large number of different circuit topologies are available. The lower the power and blocking voltage, the greater the integration of different topologies [6, p104]. For modules with high blocking voltage, 3.3 kV to 6.5 kV, single switch and half-bridge configurations are available. For modules with blocking voltage in the range of 600 V to 1.7 kV all manners of circuit topologies can be integrated. Some typical topologies is two and three level half-bridge, H-bridge and full-bridge with an optional brake chopper [6, p104].

2.3.1   Construction of IGBT Modules

Figure 2.2 shows an Infineon IGBT module, its appearance is typical for high power IGBT modules. The exterior of the module consist of a plastic frame with screw connections and a metallic backplate. The operating and storage temperature range of a modern IGBT module can be as large as -55 ℃ to 175 ℃. All the materials used in the construction of an IGBT module must work perfectly both alone, and with the other materials, for the whole temperature range [6, p.67].

Figure 2.2: Infineon 1.7 kV 1.6 kA IGBT module [9]

The plastic frame must be mechanically stable, and have high tensile strength within the whole temperature range. It must also be electrically insulating, and ensure a long creepage distance at its surface. All these properties must be maintained in highly polluted environments [6, p.68] Inside the plastic frame, a silicone gel is used to encapsulate the components. The silicone gel has very good electrical insulation properties [6, p.73]. The external contacts, both power connections and auxiliary connections, are in most cases for high-power IGBT modules screw contacts [6, p.84].
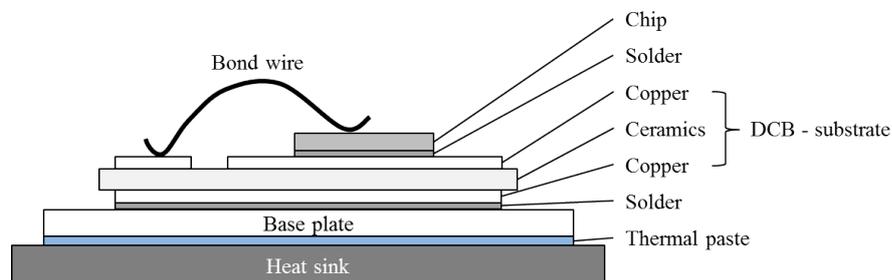
Figure 2.3: Cross section schematics af an IGBT Module IGBT

Most high-power IGBT modules have a copper baseplate to ensure good thermal connection to the cooling medium. The baseplate is usually curved, either convex or concave. This is to ensure optimal thermal contact with the cooling medium as the baseplate expands when the temperature increases [6, p.71]. As indicated in Fig. 2.3, a thin layer of thermal grease is applied between the baseplate and the heat sink. The thermal grease improves the thermal connection between the baseplate and the heat sink.

A direct copper bonded (DCB) - substrate is soldered onto the copper baseplate as Fig. 2.3 shows. The DCB-substrate, or just DCB as it is commonly called,

consist of a ceramic dielectric insulator with copper bonded to it. Through a high temperature melting and diffusion process, the copper is bonded to the substrate with great adhesive strength [6, p.69-70]. The DCB provides electrical insulation between the potential of the power component and the potential of the heat sink. It is also important that the DCB provides good thermal connection to the heat sink [6, p.70].

The upper copper layer of the DCB, consist of copper tracks. The metallic backside of the IGBT chip, the collector side, is soldered directly onto these copper tracks. To ensure good electrical and thermal connection, vacuum soldering is used. That avoids formation of air pockets in the solder between the chip and the DCB, which would increase the thermal resistance [6, p.75]. The copper tracks on the DCB is an important part of the circuit inside an IGBT module, and must be able to conducts the load current. All the properties of the DCB mentioned above, must be maintained while a high reliability towards power cycling induced stress is ensured [6, p.70].

As Fig. 2.3 shows, bond wires on the top of the chip provides electrical connection to the gate and emitter contact of the chip. Ultrasonic bonding with 40 - 100 kHz vibrations, is used when connecting the bond wires to the gate and emitter on the surface of the IGBT chip. The method ensures good connection and avoids excessive temperatures at the chip when the bond wires are connected [6, p.75]. Aluminium bond wires is most common, but recently manufacturers have started to use copper bond wires in high-power modules. The number of wires used, is determined by the rated current of the module. The silicone gel inside the module defines the maximum temperature of a bond wire. The resistivity of copper is lower than that of aluminium, copper bond wires will therefore allow a higher current before temperatures damaging for the silicone gel is reached.

2.3.2   Failure Mechanism in IGBT Modules

Bond wire lift-off is one of the main failure mechanisms in IGBT modules when power cycled [7, p.392]. The end of life failure for IGBT power modules is usually due to bond wire lift off. It happens when the interconnection between the bond wire and the emitter contact on the top of the chip is damaged. The degradation of the connection usually start with fractures, when the fractures grow it will eventually lead to disconnection of the bond wires. Improvements in the material of the bond wires and the connections method have increased the power cycling capability of bond wires [7, p.393].

In power cycling with large temperature swings, reconstruction of the chip met-

allization has been observed. The contact metallization on the chip is made of a vacuum-metallized aluminium layer, formed in a grain structure. When exposed to repeated temperature swings, the different coefficient of thermal expansion (CTE) for silicon and aluminium cause considerable stress to this layer. Silicone marginally expands with increasing temperature, with a coefficient of linear expansion of 2 - 4 ppm/K in the relevant temperature range. The aluminium in the metallization expands considerably more, with a coefficient of linear expansion of 25.5 ppm/K [7, p.400]. The metallization layer is therefore exposed to compressive stress during the heating phase of a power cycle. It has been found that this periodical compression during the heating phase, results in a plastic deformation of the grains in the metallization. The plastic deformation leads to the formation of larger grains, and the roughness of the surface increases. This has an observable effect, as the surface of the metallization gets a non-reflective appearance [7, p.401]. In the cooling phase of a power cycle, tensile stress leads to a cavitation effect at grain boundaries. That can lead to an increase in the electrical resistance of the of the surface metallization [7, p.401]. It is observed that the parts of the metallization that are covered by the bond wires, are less transformed, compared to regions that are not covered by another material. Other experiments have shown that any cover layer will restrict the movement of grains out of the contact layer [7, p.403]. Investigations of device failure under repetitive short circuit exposure, revealed that an increase in the contact resistance due to the reconstruction of the contact layer was the root cause for failure [7, p.403].

Solder fatigue is another fundamental failure mechanism in active power cycling of IGBT modules [7, p.403]. It is due to the formation of fractures in the solder between the chip and the copper tracks of the DCB. Fractures in the solder lead to an increase in the thermal resistance, accelerating the total failure of the component. The positive temperature coefficient of the forward voltage drop of an IGBT, gives an increased power loss if the temperature is increased. This positive feedback loop leads to an accelerated degradation of the power module [7, p.404]. The end of life failure is often the bond wire lift-off, however in several cases it has been found that the bond wire lift-off is a result of high chip temperature caused by fracture formation in the chip solder [7, p.404]. To transcend present limitations in the reliability of IGBT modules, problems related to solder fatigue must be solved [7, p.407].

The end of life failure mode of an IGBT module is open circuit [7, p.392]. In applications where a series connection of modules is used, that implies that the failure of one component leads to the failure the whole application.

2.4   Press-Pack IGBT

Press-pack, or "hockey puck", is the other packaging method for high power rated IGBTs. Instead of soldering the internal components together to obtain thermal and electrical contact, force is applied to a press-pack. Press-packs was introduced to provide a robust and reliable packaging method, for devices like diodes, thyristors and gate turn-off thyristors (GTO) in high power applications [10].
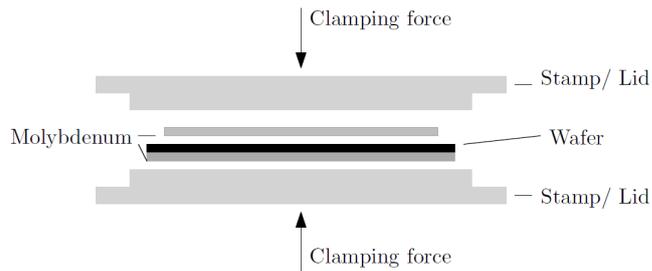
Figure 2.4: Press-pack for monolithic single-wafer devices [10, Fig 1]

Initially press-pack housing was only available for monolithic devices with a single silicon wafer containing the active structure of the power semiconductor [10]. A typical structure for a single wafer press-pack is shown in Fig. 2.4. It has a molybdenum plate and a metal lid on each side of the silicone wafer, providing thermal- and electrical- contact and ensuring homogeneous force distribution. The package is hermetically sealed with ceramic side walls [10]. Molybdenum has a CTE similar to that of silicone, that combined with its great hardness makes it ideal for placing between the metal lid and the chip. To ensure complete electrical and thermal contact, a defined pressure of typically 10 - 20 N/mm^2 must be applied to the package [7, p.347].

Some of the advantages with press-pack housing in high-power applications are [7, p.347]:

- Compact design
- Double sided cooling
- No wire bonds
- Few rigid interconnection between materials with different CTE

The last two factors, give the expectancy of high reliability for such devices. Some of the disadvantages with press-pack housing are [7, p.347]:

- No electric insulation
- Labour intensive assembly process

The many advantages of press-pack packaging have lead to the development of IGBTs with this type of housing. While press-packs for conventional power semiconductor devices consist of one large chip, an IGBT press-pack consist of many paralleled chips as shown in Fig. 2.5. The required paralleling, make the interior design of IGBT press-packs complex.
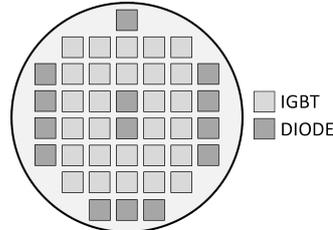
Figure 2.5: Possible chip layout in a press-pack IGBT

Since press-pack IGBTs easily can be series connected, the introduction of this packaging method has widened the field of applications for IGBTs. New applications include large HVDC, StaticVAR compensation systems, multi-level inverters and medium-voltage AC drives [11].

IGBT press-pack technology is here divided into two categories, conventional IGBT press-packs and individual press-pin IGBT press-packs. Both packaging technologies will be described, but as the IGBT chips tested in this thesis are from a conventional IGBT press-pack, that technology will be described in most detail.

2.4.1   Conventional Press-Pack IGBT

The conventional press-pack IGBT design, is based on the design of thyristor and GTO press-packs. The IGBT chip is placed between metal plates in a hermetically sealed capsule, electrical and thermal contact is established by the application of force.

Within this category of press-pack IGBTs, at least four different interior design concepts exist, as can be seen in Fig. 2.6. As for all high power IGBT components, parallel connection of several IGBT chips are used for all of the four design concepts [12]. The difference between the four concepts is mostly in the design of the pressure distribution system, as well as some differences in the design of the molybdenum spacer.
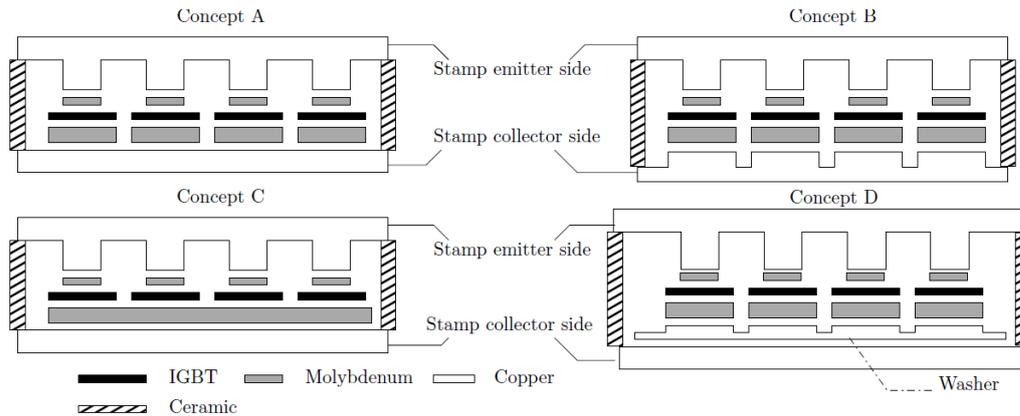
Figure 2.6: Different concepts for interior design of IGBT press-packs [12, Fig. 6.26]

Figure 2.7 shows a press-pack where the upper lid, the collector contact, is removed. All the connections to the chip are established through pressure contact alone [13].
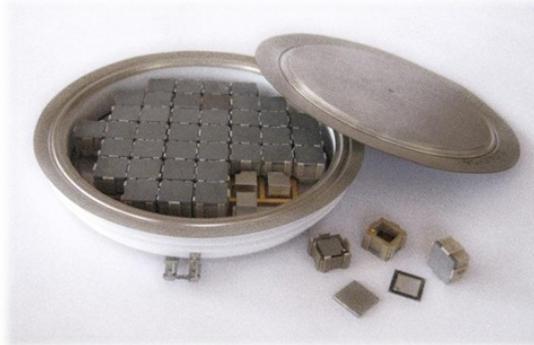
Figure 2.7: 1.6 kA 4.5 kV conventional press-pack IGBT [2]

In the type of press-pack shown in Fig. 2.7, the IGBT silicone die (chip) is mounted in a die-carrier. Figure 2.7 shows how the press-pack disc contains many parallel connected die-carriers. In Fig. 2.8 a disassembled die-carrier can be seen. Starting from the left, the parts show in Fig. 2.8 are: plastic die carrier, collector side molybdenum plate, IGBT die with emitter side up showing the gate corner pad, emitter side molybdenum plate, emitter side silver plate and the gate-pin.

The gate on the IGBT die is contacted through a corner pad, which can be seen in Fig 2.8. Individual sprung gate pins mounted in the die carrier, connects the gate to a distribution board inside the press-pack. The distribution board is connected
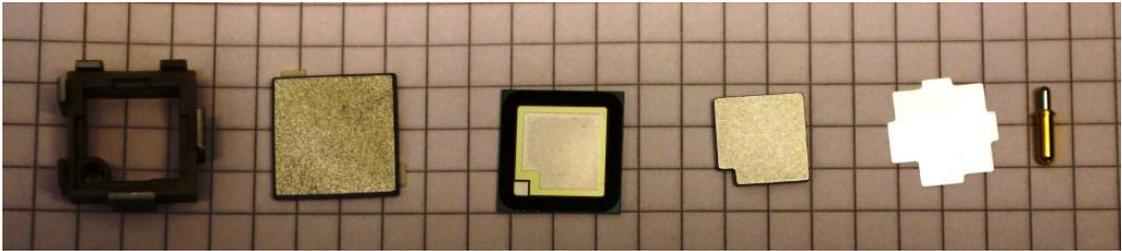
Figure 2.8: Disassembled die carrier

to the external gate terminal of the press-pack disc [13].

Molybdenum plates are positioned next to the chip on both sides. Their purpose are to homogenize the pressure distribution on a chip and avoid pressure peaks. The CTE of molybdenum and silicone is similar. In cyclic load situations, large variations in chip temperature will occur. If the material next to the silicone chip have a CTE very different from that of silicone, lateral movements in the intersection can cause damage to the chip surface [11].

The design with individual die carriers is, according to the manufacturer, a versatile design allowing rapid development in the package design [13]. The individual die carrier design also allow for any number of the IGBTs to be replaced with anti-parallel diodes. A IGBT-to-diode ratio of 2.5 give a symmetrical current rating for the component [13].

The manufacturer claims that their components have especially favourable power cycling performance, typically an order of magnitude better than modules [4]. Typical applications for this type of press-packs are therefore induction heating and mass transit, where there are repeated cyclic power demands [4]. The components are also explosion-rated, making them a good choice in critical applications such as mining, petro-chemical industry and transportation applications [4]. Other typical applications include HVDC, Active VAr controllers and medium voltage drives [4].

This type of IGBT press-pack, is claimed to be mechanically compatible with other press-pack devices based on thyristor technology. The IGBT press-packs are therefore suitable for upgrading existing systems without large changes to the mechanical design. The press-packs can be used to both retrofit existing systems, and to build new systems based on existing designs [13].

Pressure Distribution in Conventional Press-Packs

The electrical, thermal and mechanical behaviour of press-packs is very sensitive to variations in the applied clamping force. Knowledge on how the force applied to the lid of a press-pack, relates to the pressure distribution inside it is important. Especially since internal pressure distribution in a press-pack IGBT, like the one shown in Fig. 2.7, is more difficult to predict than that of traditional single wafer press-packs devices. The required paralleling of chips in high-power IGBT press-packs is a technological challenge. Identical and homogeneous force for each chip is necessary, leading to very tight tolerances in the production of every part of the package [7, p.348]. Another challenge is related to how the pressure distribution changes with increasing temperature.

Figure 2.9: Clamping device for press-pack IGBT

To obtain correct and even pressure, a clamping device, like the one shown in Fig. 2.9, is used. When heated, the test object and the clamp will expand, and the pressure on the chip will increase. The clamp have a spring to absorb this increase in pressure, but tests and simulations have shown an increase in pressure as the device is heated. More importantly, simulations have shown that when the clamping device is heated the pressure distribution changes [10].

Due to the complex internal geometry, it is complicated to calculate the pressure distribution. When heated, temperature gradients in the device and clamp makes this distribution even more complicated. Measuring the internal pressure distribution of a real device under testing would be very difficult, if not impossible. Finite Element Method (FEM) simulations is therefore necessary to predict this [10].

A FEM analysis of the pressure distribution in a press-pack IGBT was performed by T. Poller et. al. in 2013 [10]. It looked at the pressure distribution in a device after it was clamped, and after the clamped device was heated. The simulations assumes symmetry in the device and uses two symmetry axes. One of the findings was that the IGBT chips located at the border are subject to a steep lateral thermal gradient, and a non-uniform current distribution after the clamp is heated. The explanation is related to the status of the interconnection between the IGBT and the molybdenum after the heating. By comparing the pressure distribution in the press-pack when clamped in room temperature (Fig. 2.10a), and when it is clamped and heated (2.10b), it can be seen that the pressure in regions of the chips at the border of the disc, is zero [10].

(a) After clamping[10, Fig 9a]   (b) After heating[10, Fig 9b]
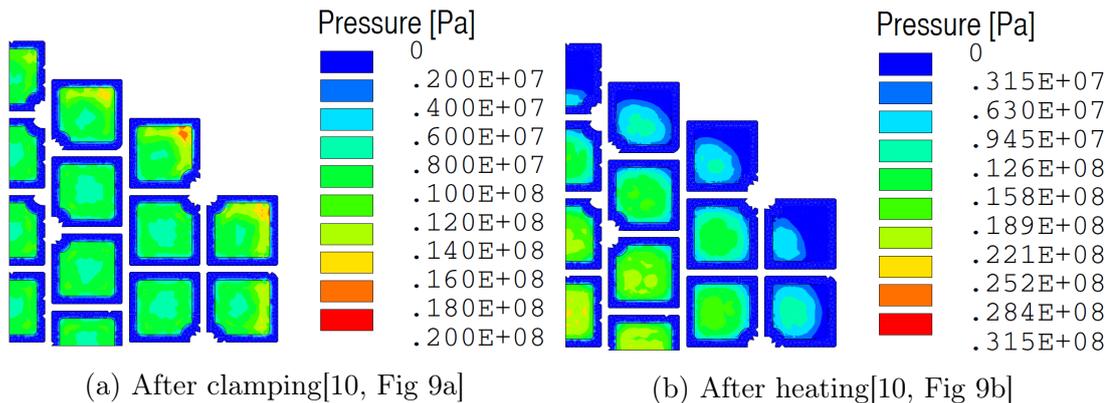
Figure 2.10: Pressure distribution in the press-pack

Zero pressure on the chip, means loss of mechanical contact between the silicone chip and the molybdenum plate. The partial loss of contact is a result of the deformation of the lid. The deformation is due to thermal gradients in the lid. The lid will expand in the lateral direction when heated, and areas with different lateral expansion leads to bending of the lid [10]. Figure 2.11b shows an exaggeration of how this deformation affects the contact between the molybdenum and the silicone chip. Complete or partial loss of contact will affect the current distribution in the chip and the press-pack. The regions of the press-pack remaining in good contact with the lid, must carry more current [10].

The study also looked at different clamp designs. A cylindrical clamp was com-

(a) [10, Fig 6b]

(b) [10, Fig 6c]
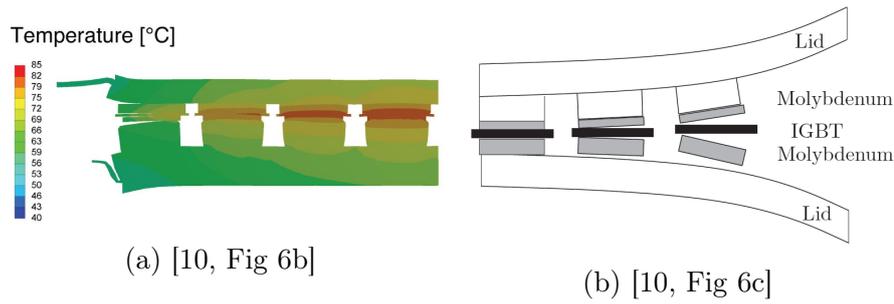
Figure 2.11: Deformation and temperature distribution in IGBT press-pack under power cycling conditions

pared with two different conical clamp designs. Some differences in how much the pressure distribution changed with the heating was observed, but for all the clamp designs partial loss of contact the chips occurred [10].

Thermal and Electrical Contact in Conventional Press-Packs

A press-pack consists of many materials stacked on top of each other, connected both thermally and electrically by applying a force on the device. All the materials, and the interfaces between them, represent both a thermal and an electrical resistance. If the thermal and electrical contact resistance of the material intersections is assumed constant, the result is a decoupling of thermal, mechanical and electrical behaviour of the press-pack [14]. Such a simplification will therefore lead to incorrect analysis of the component.

On a microscopic scale, the surface of the materials in a press-pack is not flat. The surface of the aluminium metallization on an IGBT chip for example contains rugosity. Therefore only parts of the surface between the silicone die and the molybdenum plate is in physical contact [14].

The pressure dependency of the thermal and electrical contact resistance was calculated by T.Poller et.al in 2013 [14]. The study performed measurements on a single IGBT press-pack chip, and used the result in a FEM simulation to find values for the thermal contact conductance (TCC) and the electrical contact conductance (ECC).

A simplified model of the how the silicone die is connected in an actual press-pack was used. The model analysed the thermal and electrical contact resistance of four different material intersections [14].

1. Emitter-side copper stamp and emitter-side molybdenum plate

2. Emitter-side molybdenum plate and the emitter-side of the IGBT chip (aluminium metallization)

3. Collector-side of the IGBT chip (aluminium metallization) and the collector-side molybdenum plate

4. Collector-side molybdenum plate and the collector-side copper stamp

The relation between ECC and TCC and the applied clamping force, for the copper-molybdenum interconnections, and the aluminium-molybdenum interconnections was found and is shown in Fig. 2.12 and Fig. 2.13 [14].
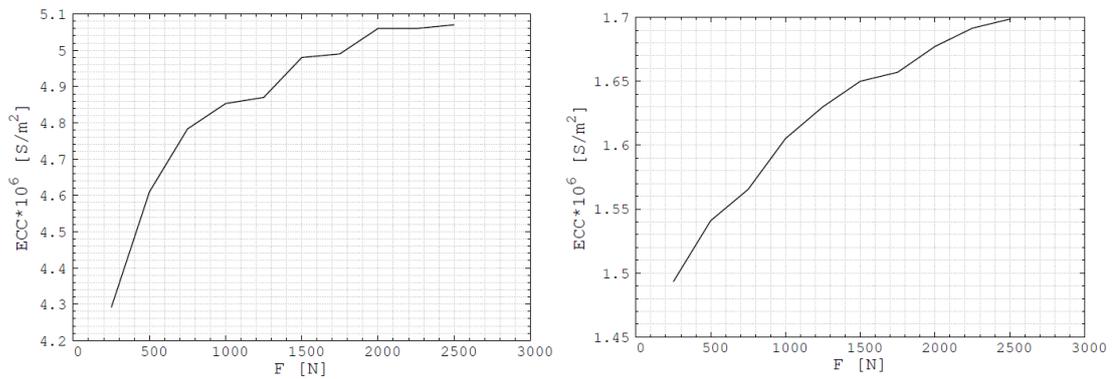
(a) ECC aluminium-molybdenum interface [14, Fig. 9a]

(b) ECC copper-molybdenum interface [14, Fig. 9b]

Figure 2.12: Relation between applied clamping force and the electrical contact conductance (ECC)

Figure 2.12 and Fig. 2.13 clearly show that both ECC and TCC are very dependant on the magnitude of the clamping force, for both the copper-molybdenum interface and the aluminium-molybdenum interface. The single-chip used for ECC and TCC calculation was removed from a 42 chip device [14]. The data sheet for a typical 42 chip press-pack disc specify a rated clamping force of 50 kN - 70 kN [15]. If it is assumed that the applied force is shared equally between the all 42 chips, the rated clamping force for a single-chip is 1.2 kN - 1.7 kN.

For the aluminium-molybdenum interface, ECC increases from 4.86 MS/m^2 to 4.98 MS/m^2 when the clamping force is increased from 1.2 kN to 1.7 kN. For the same material intersection and the same increase in clamping force, TCC increases from 2.32 MW/m^2K to 2.6 MW/m^2K. For ECC the increase was 2.4 %, while the increase in TCC was 10.7 %. These calculations is based on the values found in Fig.2.12 and Fig. 2.13, and is a rough calculation. Obtaining values from the a graph is inherently inaccurate, and the data in the graphs is calculated from a
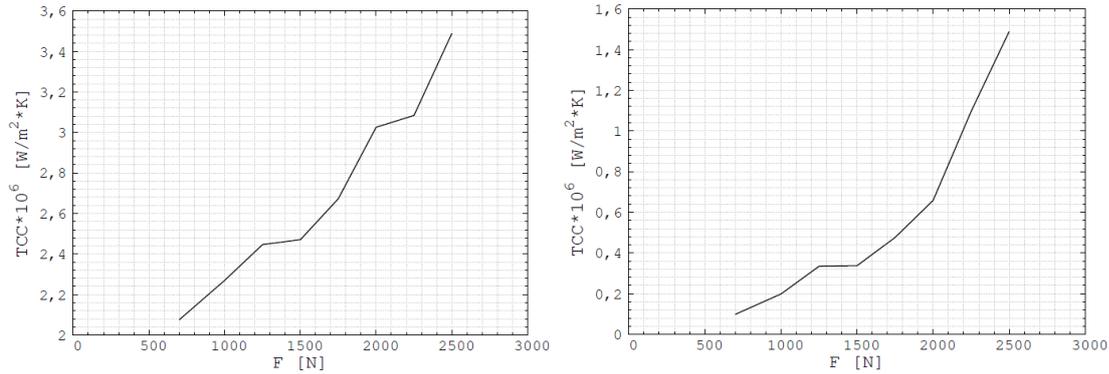
(a) TCC aluminium-molybdenum interface [14, Fig. 11a]

(b) TCC copper-molybdenum interface [14, Fig. 11b]

Figure 2.13: Relation between applied clamping force and the thermal contact conductance (TCC)

simplified model of the single chip. Assuming that the calculated increase in ECC and TCC is correct, an interesting fact about the contact resistances for the rated force range is demonstrated. The increase in TCC is larger than the increase in ECC, meaning TCC and thereby the thermal resistance is more pressure dependant than the electrical resistance, for this range in applied force.

What the difference in the increase of TCC and ECC implies, is that when the force is decreased, the ability to conduct the heat away from the silicone chip is decreasing faster than the ability to conduct current though the chip. Therefore temperature increase in the chip due to reduced pressure is not dominated by the increase in losses, but by the increase in thermal resistance.

The main fact is, changes in the applied force affects both the electrical and the thermal resistance of a pressure connected IGBT chips. These changes will in turn affect the temperature of the chip, and thereby the temperature of the whole component.

2.4.2 Individual Press-Pin Press-Pack IGBT

The ABB StakPak technology represents another packaging method for press-pack IGBTs. Individual press-pins ensures correct pressure for all of the parallel connected chips in the component.

Figure 2.14 shows an ABB StakPak press-pack IGBT with a submodule. As the figure shows, the press-pack can have a asymmetric design due to the internal

Figure 2.14: Asymmetric 4500V/1000A Press Pack IGBT along with a submodule comprising 12 IGBT chips [11, Fig. 1]

spring connections ensuring correct and homogeneous force distribution on all the chips [11].

The maximum blocking voltage of an IGBT is in the range 3.3 kV to 6.9 kV, so independent of the chosen technology, several IGBT components must be series connected to achieve a high voltage. In HVDC applications, DC-link voltages exceeding 100 kV is used; series connection of many IGBTs is therefore essential [11]. Since press-packs can be series connected by stacking them on top of each other, they are ideal for series connection. Individual press-pins press-packs are claimed to be especially suitable for stack assembly with many series connected components [11].
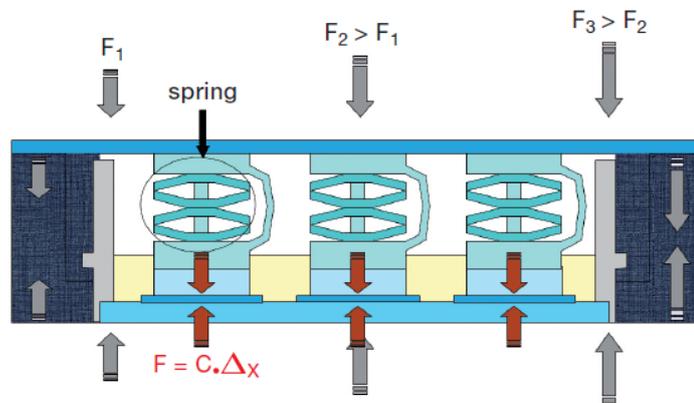
Figure 2.15: ABB StakPak schematics [16]

Figure 2.15 shows the schematics of the cross section of a press-pack with individual press-pins. Each of the press-pins is subjected to a force $F = c\Delta X$, where c is the spring constant and ΔX is the travel distance for the press-pin. As the figure shows, the spring system ensures equal force on each chip. Surplus force is

sustained by the rigid frame. The force distribution on the chips no longer depends on pressure homogeneity in the stack, but on the accuracy of the spring constant and travel distance, which can be accurately controlled [11].

2.4.3 Short Circuit Failure-Mode for Press-Pack IGBTs

Press-pack IGBTs can have short circuit failure-mode (SCFM). Compared to IGBT modules, which failure mode is open circuit, this gives the press-pack a great advantage in many applications. In HVDC applications SCFM, is a particularly favourable feature. By including redundant press-pack modules in the converter, failure of one component does not mean failure of the converter. If one components fails, the remaining components can share the voltage, while the stable short circuit in the failed component can carry the load current [11].

Especially in HVDC, failed press-packs must have sufficient lifetime, typically one year, in SCFM operation to avoid unscheduled interruptions in the electricity supply. Failed devices can then be removed and replaced during scheduled maintenance of the converter station. Since a large HVDC system can contain as many as 6000 IGBTs, it is clear that SCFM is important for the reliability of a HVDC system [11].

The ABB StakPak components can be delivered with SCFM capability [11]. The way SCFM is obtained in these components is by inclusion of a metal platelet in the contact system for each chip, as can be seen in Fig. 2.16. When a chip fails, for a short duration enough heat is dissipated to melt the metal platelet, and a stable alloy with silicon is created [11].
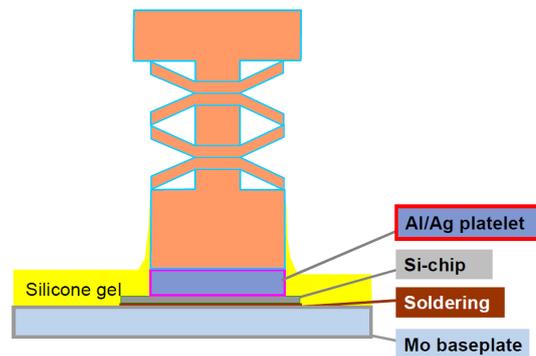
Figure 2.16: ABB StakPak with metal platelet for SCFM [11, Fig. 14]

Silver and aluminium form a low melting eutectic alloy with silicone, and are used for the platelet. Unfortunately, these metals have a large CTE compared

to silicon. That creates a trade-off between the SCFM capability and the power cycle lifetime of a component. Under power cycling, the comparatively high CTE of silver and aluminium, can cause a lateral relative movement of more than 10 µm at the chip-to-platelet-interface [11]. Cyclic lateral motion, combined with high current density and high temperature can damage the surface of the chip. This can eventually cause an electrical failure [11].

SCFM is only necessary in applications where series connection of many press-packs with redundant components is used. In industrial applications or traction applications a failure will cause an interruption anyway, and SCFM has no practical use. The silver and aluminium platelet should in such applications be replaced with a platelet in a material with a CTE closer to that of silicone, like molybdenum [11].

A manufacturer of conventional press-pack IGBTs claims on their website that their components have SCFM, and therefore are ideal for applications where series connection is required [4]. In an application note for their press-packs, the same manufacturer is on the other hand more careful with promising the SCFM capability of their components. They state that the failure mode for normal ceramic press-pack components is a short circuit, and that open circuit failure for these devices is highly unlikely. The application note further empathizes that there is no guarantee that their press-packs fail to a stable short circuit with a resistance comparable to that of a device in normal operation [17]. Based on information from the manufacturer, it can probably be said that the conventional press-pack components is likely to short circuit when they fail, but unless they are specifically designed to do so, it cannot be guaranteed that they will.

2.4.4   Failure Mechanisms in Press-Pack IGBTs

One of the failure mechanisms for IGBT modules is the reconstruction of the chip metallization. As described in chapter 2.3.2, the reconstruction of the metallization at the contact surface to other materials is limited. The whole surface of an IGBT die in a press-pack should be in contact with other materials, so the reconstruction of the metallization should be limited.

It have been observed that spreading of the chip metallization can occur after power cycling press-pack IGBT devices. The spreading was observed on the edge of the chip, and across the gate distribution track at the chip surface [18].

Figure 2.17a shows a pictures of a failed IGBT chip. Figure 2.17c shows the actual failure point, while Fig. 2.17b and 2.17d show a detail of the chip metallization [18]. Although the pictures of the failed chip show reconstruction and spreading of
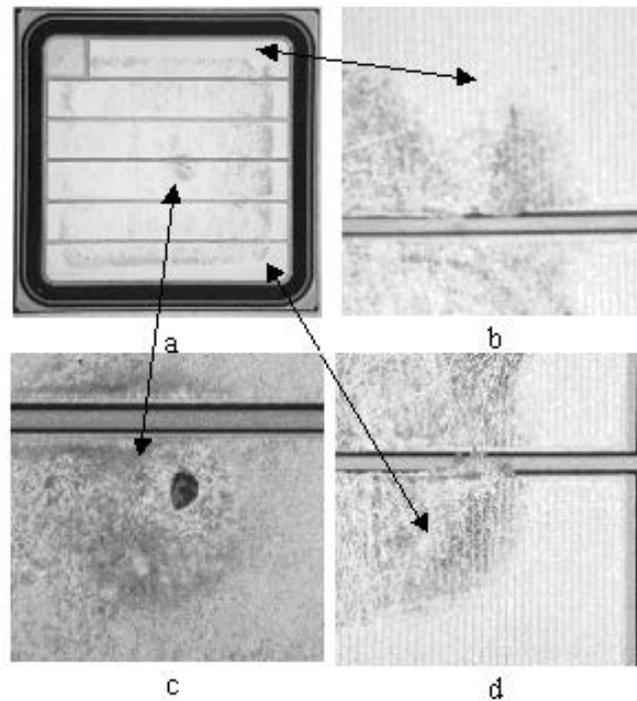
Figure 2.17: Failed IGBT chip with metallization spreading [18, Fig.11]

the chip metallization, is was not the cause of the chip failure. Other power cycled devices that had not failed showed similar, and in several cases more extensive, spreading of the metallization than what was found for the failed chip [18].

Although one study concluded that reconstruction of the chip metallization was not related to the failure of the device, it is mentioned here as a possible failure mechanism for press-pack IGBT devices. Changes to the physical structure of the chip is likely to have some effect on thermal and electrical properties of the device. The possibility that the reconstruction of the metallisation have a negative effect on a IGBT press-pack device, is therefore kept open.

In the power cycle testing of press-pack IGBT discs performed in the SINTEF 2000 A power cycle tester, it was found that for all the failed devices that was analysed, the failure was caused by chips in a specific location inside the device. It is therefore believed that changes in the pressure distribution due to bending of the lid is the cause of the device failures. The results and findings from this experiment is explained in more detail in chapter 4. Almost certainly other failure mechanisms for press-pack IGBT than the ones presented here exist.

2.5   IGBT Junction Temperature Estimation

Power cycle testing is a thermal cycling test, and two of the main parameters describing the stress level of a test, are maximum virtual junction temperature ($T_{vj,max}$) and the virtual junction temperature swing (ΔT_{vj}). A correct estimation of the virtual junction temperature is therefore particularly important for the work presented in this thesis.

The virtual junction temperature can be defined as a temperature representing the temperature of the junction(s) calculated on the basis of a simplified model of the thermal and electrical behaviour of the semiconductor device [19]. The term virtual junction temperature is taken from IEC standards and is used since the actual junction temperature in an IGBT cannot be measured. It is particularly applicable to multijunction semiconductors and is used to denote the temperature of the active semiconductor element when required in specifications and test methods [19].

Accurate estimation of $T_{vj,max}$ and ΔT_{vj} during power cycle testing is essential since these parameters are closely linked to the lifetime of a component. Obtaining an accurate measurement of the virtual junction temperature of a press-packed IGBT is however challenging. Two factors make it particularly challenging to obtain a good estimation of the temperature inside an IGBT chip when power cycled.

Firstly, very fast measurement of the chip temperature is necessary. In a power cycle test, a load current conducted through the IGBT test object is turned on and off in a cyclic manner. Immediately after the load current is turned off, the IGBT chip starts to cool down and very fast temperature transients occur. Therefore, to obtain a correct value of the $T_{vj\,max}$, temperature measurements less than a millisecond after load current turn-off is necessary. Placing a thermocouple sufficiently close to the chip is not possible without destroying the device. Even if the thermocouple could be placed close to the chip surface, the transient response of a thermocouple is > 100ms. They are therefore only useful for temperature measurements in equilibrium conditions [20]. Pyrometers and infrared-cameras are able to measure temperature change within the required time range, but they need free vision to the test object. For IGBT modules that can be performed with special preparation of the test object. For a press-packed IGBT, free vision to the semiconductor under testing is not possible, and pyrometers or infrared-cameras cannot be used [21].

Secondly, considerable lateral temperature gradients in the semiconductor chip is present. When power cycle testing a chip, it is heated by conduction losses and lateral temperature gradients evolves. The temperature in the centre of the chip is

considerably higher than the temperature at the edges [21]. The increasing power densities in modern power electronic systems lead to steeper temperature gradients in the chip. Temperature differences between the centre and the corners of a chip exceeding 40 ℃ is becoming normal [21].

2.5.1 $V_{ce}(T)$ - measurement

As explained above, measuring the transient behaviour of the temperature inside a press-packed IGBT with external sensors is not possible. Using the power chip itself as a sensor is a good solution the problem. It enables the virtual junction temperature to be measured without destroying the device. For the definition of a virtual junction temperature, the three-dimensional temperature map of the chip has to be transformed into a single value [21].

One way to perform this transformation is by electrical measurements, using a method called the $V_{ce}(T)$-method. The method takes advantage of the temperature dependence of the diffusion voltage of a pn-junction. For an IGBT the collector-emitter voltage (V_{ce}) is used. [21].

The current-voltage characteristics (IV-characteristics) of a modern IGBT has a positive temperature coefficient for nominal currents, meaning that an increase in temperature leads to an increase in V_{ce}. Fig. 2.18 shows that for nominal values of the forward current, the IV-characteristics has a positive temperature coefficient.

For a small forward current the temperature coefficient of the IV-characteristics is generally negative. When a small current is conducted through the IGBT chip, V_{ce} decays linearly with increasing temperature, at approximately -2 mV/K [21]. To utilize this linear voltage-temperature relationship, a very low magnitude sense current is conducted through the semiconductor chip. In Fig. 2.19 the linear V_{ce}-temperature relationship for an IGBT chip when a 25 mA sense current is conducted through it, can be seen. The sense current should be small, and for the test set-up described in this thesis, it is less than a thousandth of the nominal current. The power loss created in the chip by the sense current is therefore negligible, and the sense current can be continuously conducted through the chip without affecting test results [20].

The $V_{ce}(T)$-method can only be used to estimate T_{vj} when the load current is removed from the test object. In a power cycling test that means that this method is used to estimate the temperature of the chip during the cooling period.

To enable T_{vj} measurement using the $V_{ce}(T)$ -method, calibration of the test object is necessary. The calibration curve can be made by externally heating the device
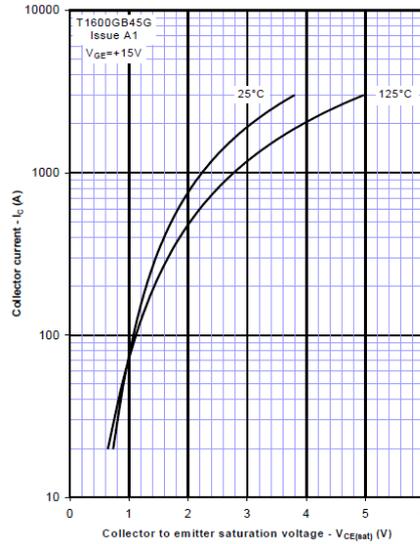
Figure 2.18: Positive temperature coefficient of an IGBT IV-characteristics for nominal forward currents [15, Fig. 1]
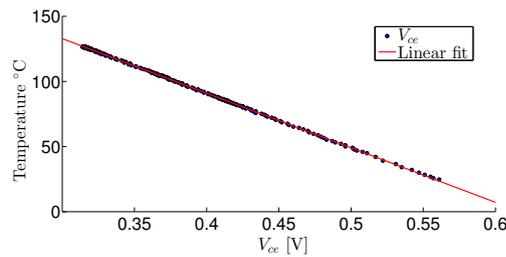
Figure 2.19: $V_{ce}(T)$-method calibration curve, $I_{sense} = 25\text{mA}$

while continuously measuring V_{ce} from the sense current. Fig. 2.19 shows a calibration curve from the single chip power cycle tester. Since the test object is externally heated during the calibration, the temperature distribution can be assumed homogeneous. It can then further be assumed that the sense current through the chip will be evenly distributed. If there is significant lateral temperature gradients present, the negative temperature coefficient of the IV-characteristics will lead to an uneven current distribution in the chip. The current density will be higher in the hot parts of the chip. Since all parts of the chip surface is electrically in parallel, V_{ce} will be the same for the whole chip. The sense current can be seen as a sum of partial currents laterally distributed in the chip. The measured V_{ce} is therefore the voltage drop created by all the partial currents in the chip. The $V_{ce}(T)$ -method is therefore a current weighted measurement of the mean temperature in the chip

[21].

When the semiconductor chip is heated by a load current under power cycle testing, considerable lateral temperature gradients are generated. While under calibration it is externally heated, leading to a homogeneous temperature distribution in the chip. The difference in temperature distribution between calibration and power cycling is a possible weakness of this method [20].

The temperature found using the $V_{ce}(T)$-method, is as explained above, a current weighted mean temperature of the junction. Regions of the chip will have temperatures higher than the mean temperature found using the $V_{ce}(T)$-method. A comparison of temperature measurements using the $V_{ce}(T)$-method and infrared-camera, performed by R.Schmidt et.al in 2009, showed this difference [21]. The experiment was performed on an IGBT module specially prepared for the experiment. A high emissivity lacquer for infrared measurement was applied to the surface of the chip. The current weighted $T_{vj\,max}$ found using the $V_{ce}(T)$-method was 108,5℃, while the area weighted $T_{vj\,max}$ found using the infrared-camera was 106,6℃. The maximum temperature close to the centre of the chip, measured with the infrared-camera, was 117,6℃ which is 12% higher than $T_{vj\,max}$ measured using the $V_{ce}(T)$-method [21].
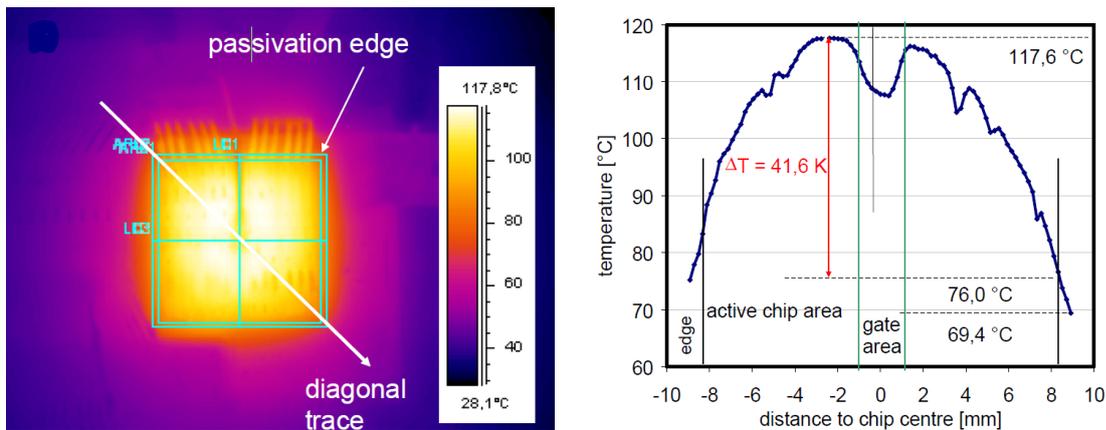
(a) Thermal image of a chip in thermal equilibrium [21, Fig. 4a]

(b) Temperature profile along the diagonal trace [21, Fig. 4b]

Figure 2.20: Lateral temperature distribution in an IGBT chip in thermal equilibrium, measured using infrared-camera

In Fig. 2.20 the thermal image and the lateral temperature distribution found using a infrared-camera can be seen [21]. It is important to be aware that regions of the chip can experience maximum temperatures at least 12 % higher than the $T_{vj\,max}$ estimated using the $V_{ce}(T)$-method [20]. The figures clearly demonstrates

why T_{vj} estimations close to the upper temperature limits of the an IGBT chip, using the $V_{ce}(T)$-method must be interpreted with care.

Since the $V_{ce}(T)$-method estimates the junction temperature based on electrical measurements, the temperature can be estimated shortly after load current turn-off. A time delay of typically 300 µs is however necessary, this time delay ensures that the electrical equilibrium within the pn-junction is reached by the recombination of excessive charge carriers [21]. The study performed by R.Schmidt et.at from 2009, also contains simulations of the lateral temperature distribution in an IGBT chip, and how it changes with the rapid temperature change after the removal of the load current. The simulation showed only a small decrease in temperature within the first 300 µs, the error in the temperature measured using the $V_{ce}(T)$-method, was found to be 1,8 K or 1,8 % [21].

The simulations in [21] also found that the lateral temperature gradients started to decrease after approximately 20 µs. Further it showed that approximately after 300 ms the lateral temperature profile was levelled. Meaning the whole chip can be assumed to have the current weighted average temperature found by the $V_{ce}(T)$-method after 300ms. The temperature development after 300 ms was found to be solely dependant on the time-constants in the copper baseplate and the heat sink [21]

The studies presented here were performed on IGBT modules. The results should however be applicable to press-pack IGBTs. The lateral temperature gradients observed in the chip in the IGBT module was a result of the conduction losses. The chip used in press-pack IGBTs will be similar, and given that the lateral temperature gradients is a result of thermal and electrical parameters in the silicon chip, the results should be transferable.

Chapter 3

Accelerated Lifetime Stress Tests

3.1   Introduction

The packaging and connection technology is an essential part of a power semiconductor component. The materials and the interconnections between them, must withstand high stress in tough conditions. High reliability and good quality of power semiconductor components is important, and lifetime testing is essential to ensure that. A large range of lifetime tests is available, and this section will give a short description of some of the most used lifetime tests.

The desired lifetime of a power electronic components can range from a few years up to 30 years, depending on the target application. Testing the reliability of the components under their nominal operating conditions will take as long time as its expected lifetime, and would obviously be very impractical. Manufacturers have therefore developed a set of accelerated test procedures. During an accelerated test, the components are exposed to higher stress than its operating condition. Based on the results from such tests, predictions about lifetime can be performed [7, p.381].

When evaluating test results, an exact definition of the failure criteria is important. IEC60747-1 defines failure this way: *A device, which after test does not meet the limits specified for one or more of the characteristics for its device category, is considered to be a failure* [22]. Other standards regulate how much different characteristics are allowed to change. One standard regulating this is IEC60747-9, which defines failure criteria and measurement methods for IGBT testing [23].

Table 3.1 show the acceptance-defining characteristics for endurance and reliability tests. IEC60747-9 further define measuring methods for these characteristics.

Characteristics	Criteria	Measurement conditions
I_{CES}	< USL	Specified V_{CE}
I_{GES}	< USL	Specified V_{GE}
$V_{GE(th)}$	>LSL, < USL	Specified V_{CE} and I_C
V_{CEsat}	< USL	Specified I_C
R_{Th}	< USL	Specified I_C

Table 3.1: Acceptance-defining characteristics
USL: Upper specification limit
LSL: Lower specification limit
[23, 7.2.3 Table-2]

Specification limits are found in the component data sheet. Failure criteria can also be given as an allowed change compared to specification limits, for certain parameters during the test. For critical parameters the allowed change is lower than for non-critical parameters [7].

Qualification and endurance tests for power electronic devices can be divided in three categories; chip-related tests, package stability tests and mechanical test of packaging. The mechanical tests of the packaging consist of a mechanical shock test and vibration test. Some of the other tests will be explained more in detail below.

3.2   Chip Related Tests

High Temperature Reverse Bias Test (HTRB)

The high temperature reverse bias test verifies the long-term stability of the leakage current of the chip. The chip is tested with a blocking voltage at or slightly below the rated blocking voltage of the device. During the test, ambient temperature is close to the operational limit of the device. The test can determine weakness in the field depletion structures at the device edges and in the passivation region. Due to the increased electrical field strength, in certain areas of the chip movable ions can accumulate and create surface charge. The source of the movable ions can be contamination from the fabrication process. Surface charge can affect the electric field and create additional leakage currents, and in worst case, produce inversion channels in low-doped areas creating short circuit paths across the pn-junction. The failure criteria for this test is the increase in leakage current when the device has cooled down after the test. HTRB is a highly accelerated test, and during 1000

h it generates stress similar to a lifetime of 20 years and more. In normal operation, the DC-link voltage is 50-60 % of the specified device blocking voltage, which is only reach during sudden voltage spikes. The maximum operational temperature is only occasionally reached [7, p.383].

High Temperature Gate Stress Test (HTGS)

The high temperature gate stress test, verifies the stability of the gate leakage current. Even though the gate voltage is only 20V the electric field across the gate oxide can become 2 MV/cm. This is due to the very thin layer of gate oxide in modern IGBTs and MOSFETs. The gate oxide layer must be free of defects and only a low density of surface charge is tolerable to keep the gate leakage current stable. The ambient temperature being the maximum operating temperature, accelerates the test [7, p.385].

3.3   Package Stability Tests

High Humidity High Temperature Bias Test (H3TRB)

The high humidity high temperature bias test is testing the influence of humidity on the long-term performance. Modules are not hermetically sealed like press-packs, and are the type of power components that is most affected by humidity. The humidity can diffuse through the silicone soft mold, and reach the chip surface. The test can detect weaknesses in the junction passivation, and humidity related weakness in the packaging [7, p.386].

High- and Low Temperature Storages Tests (HTS) and (LTS)

The high- and low temperature storages tests are used to verify the integrity of plastic materials, rubber materials, organic chip passivation materials, glues and silicone soft molds. These materials must keep their characteristics for the whole storage temperature range. Storage temperature is the non-operational temperature of the power electronic device installed an in application [7, p.387].

Thermal Shock Test (TST) and Thermal Cycling (TC)

Temperature swings are a major stress mechanism for power electronic devices. Thermal shock and thermal cycling tests investigates the components resilience towards this type of stress. A power electronic device consists of many materials with different thermal expansion coefficients. When the temperature changes this can cause fatigue at material intersections, possibly leading to device failure. Thermal stress tests are conducted by externally heating and cooling the devices. The difference between thermal shock and thermal cycling test are the rate of the temperature change. In thermal cycling, the rate-of-change in the ambient temperature is 10 - 40 ℃/min. In a thermal shock test the device is moved between two chambers with different temperatures, or if liquid cooled alternating between warm oil and liquid nitrogen. Common for all temperature cycling tests are that the test object must reach thermal equilibrium during each cycle. Changes in the electrical parameters are controlled by measuring before and after the test, and must comply with the failure criteria for the test. The lifetime of a component under temperature cycling, is depending on the combination of materials and the interconnection layers between the materials. Large modules are more prone to failure under thermal cycling than small packages [7, p.388].

3.4   Power Cycling Test

Power cycling test (PCT) is an accelerated lifetime stress test, where the power semiconductor component is actively heated by losses in the chip. It is one of the package stability tests, but due to its central part in this thesis, it is natural to describe it in a more detail than the other tests.

In a power cycling test, the power semiconductor is mounted on a heat sink as in a real application. A load current is conducted through it, and through on-state losses in the semiconductor chip, the device is heated. The load current is conducted through the test object until the desired maximum chip temperature is reached [7, p.390]. For the definition of the maximum temperature under a power cycling test, $T_{vj,max}$ is usually the defining parameter. The desired stress level of the test, is one of the factors determining the magnitude of $T_{vj,max}$. The on-time (t_{on}) is the length of the period when the load current is conducted through the test object. The duration of t_{on} depends on several factors: the magnitude of the load current, the cooling conditions and what the desired $T_{vj,max}$ is.

Once the desired maximum temperature is reached, the load current is removed and the test objects starts to cool down. It is cooled until the minimum temperature

is reached. Similarly as for the maximum temperature, the minimum temperature is usually defined by a virtual junction temperature, specifically $T_{vj,min}$. The off-time (t_{off}), is the time it takes from the load current is removed, and the cooling starts, to the minimum temperature is reached. The length of t_{off} is determined the cooling conditions.

The characteristic parameter describing the stress level of a power cycle test, is the temperature swing ΔT_{vj}. It is the difference between the maximum temperature at the end of the heating period, and the minimum temperature at the end of the cooling period.

$$\Delta T_{vj} = T_{vj,max} - T_{vj,min} \tag{3.1}$$
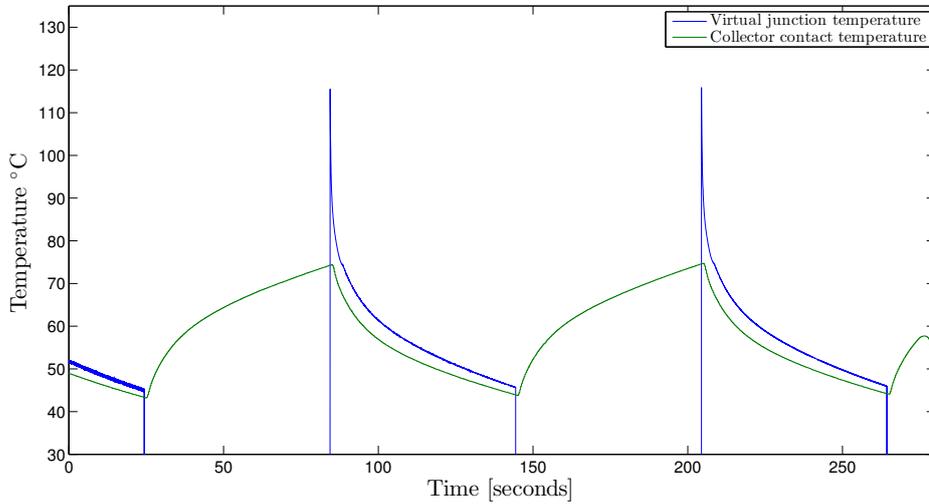
Figure 3.1: Temperature profile during a power cycle

Figure 3.1 shows the temperature profile of an IGBT test object under power cycling. The T_{vj} in the plot, is measured using the $V_{ce}(T)$-method described in chapter 2.5. The figure shows the fast thermal dynamics of T_{vj} in the beginning of the cooling period. Rapid temperature changes, creates considerable thermal gradients in the test object during each cycle. Different CTE for the various materials in a component creates mechanical stress at the material interfaces [7, p.391]. This thermal stress will in the long run lead to fatigue of materials and interconnections. This thermomechanical stress is an important failure mechanism in power cycling [7, p.391].

A relationship between ΔT_{vj}, $T_{vj,m}$ and lifetime, for a module power cycling test can be seen in Fig. 3.2 [24]. The medium virtual junction temperature $T_{vj,m}$, is

defined as $T_{vj,m} = T_{vj,min} + \dfrac{T_{vj,max} - T_{vj,min}}{2}$ [7, p.391]. As the figure shows, a small change in ΔT_{vj} can have a great effect on how many cycles a device can withstand. Analysis of failure mechanisms for the failed devices showed reconstruction of chip metallization and bond wires lift-off [24]. Both are typical module failures mechanisms, so direct comparison to press-pack behaviour can not be done. Although the failure mechanisms for press-packs and modules probably are different, the strong dependency on ΔT_{vj} clearly show the importance of exact virtual junction temperature measurement.
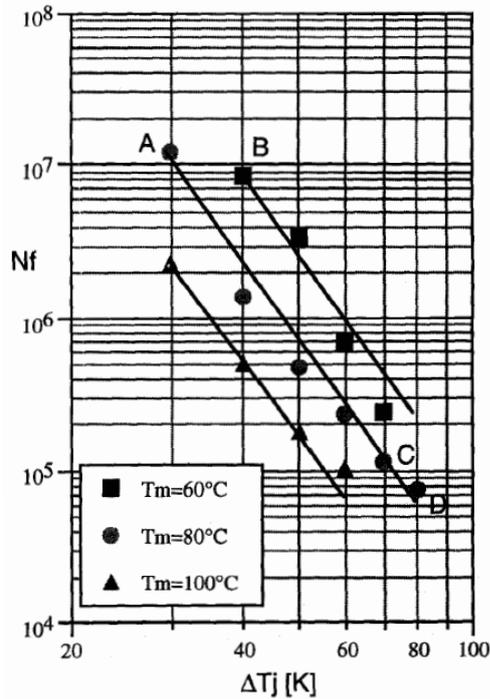
Figure 3.2: Number of power cycles to failure (N_f) as function of ΔT_{vj}, with $T_{vj\,m}$ as parameter [24, Fig 9]

Semiconductor switches like IGBTs or MOSTFETS, can be both actively and passively power cycled. In passive power cycling, the device is kept on during the whole test by continuously applying a positive gate-emitter voltage. The load current through the test object is switched on and off by auxiliary load current switches. In active power cycling, the load current is switched on and off by the test object itself. Compared to passive, active power cycling might generate more stress on the device, since the device electrically blocks the load current every cycle. Therefore large changes in the space charge distribution at the pn-junctions inside the silicone chip occur in every cycle. Possibly, that can lead to internal

electrical wear of the chip in addition to thermomechanical stress created by the large variations in temperature.

3.4.1 Load Conditions Simulated by Power Cycle Testing

Many applications for power semiconductors have large variations in the output power. A power cycling test creates a stress similar to what components are exposed to in such applications.

Low operating frequency for converters can lead to lifetime limiting power cycling. In converters for large direct-driven wind turbine generators, the operating frequencies can be as low as 6 - 13 Hz [25]. The generator-side converter is then continuously power cycling its semiconductor devices, possibly with a considerable ΔT_{vj} since the low frequency can be combined with high power. The SINTEF OPE project have performed a thermal simulation of a three level converter used in a wind energy conversion system. They found that for an operating frequency of 20 Hz the generator side converter had variations in T_{vj} of up to 20 ℃ [25]. Although a temperature swing of 20 ℃ might not be extreme, power cycling with a frequency of 20 Hz give 72000 cycles per hour.

In the doubly fed induction generator system, which is one of the most popular topologies in wind power, power cycling can also occur. The slip frequency of the machine can lead to very low frequency for the rotor-side converter, which combined with high power can cause severe power cycling stress [26].

Another example where low operating frequency might lead to power cycling is in electric vehicles and other traction applications. There the combination of low speed and high load often will occur. Since the mechanical frequency of the rotor in such situations is low, the electrical frequency in the stator of the induction motor and the converter, will then be low as well. An electrical vehicle moving at a low speed up a hill can cause this.

The load profile in an application is the other typical cause of power cycling of power semiconductor components. Energy conversion for renewable energy sources is a typical application that can have a rapidly changing load profile. In Fig. 3.3a a wind profile and the wind power profile for a 3-level voltage source converter is shown [27]. From a thermal simulation on the converter, T_{vj} for different valves was found. Figure 3.3b shows T_{vj} for the wind and power profile shown in Fig. 3.3a [27]. Several cycles with a ΔT_{vj} of more than 40 ℃ can be seen in a relatively short time. It can be assumed that for a longer time-scale, larger temperature swings will occur, as it will include start and stop of the wind turbine. In energy

conversion for solar power, it can also be assumed that rapid changes in the load will cause power cycling.
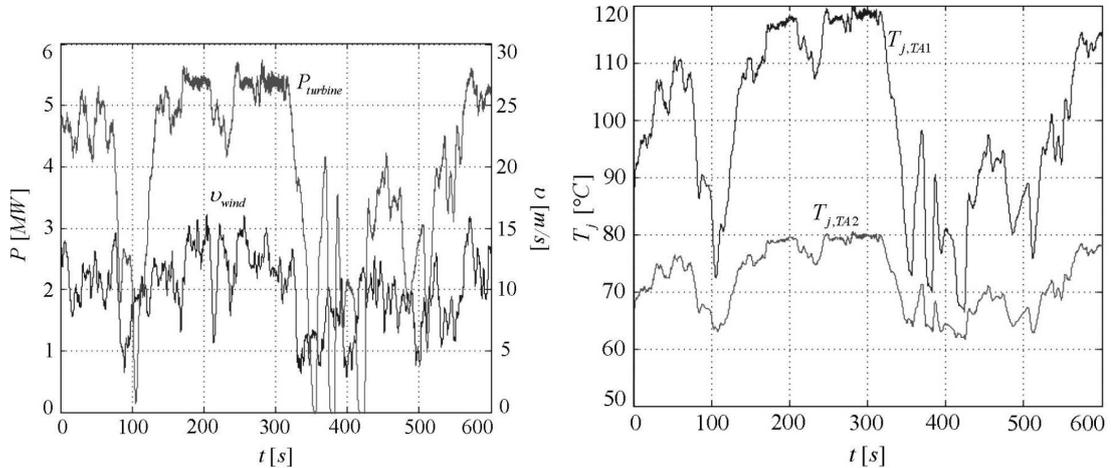
(a) Wind and power profiles of a 5.6 MW wind turbine at $v_{av} = 10$ m/s [27, Fig. 15]

(b) Junction temperatures for the wind profile with $v_{av} = 10$ m/s [27, Fig. 16]

Figure 3.3: Power cycling from wind profile

Start and stop of electrical vehicles in cold weather will create large temperature swings. As this can happen several times during the day, during its lifetime a converter it will experience many of these extreme power cycles.

Lastly, traction applications, like drives for buses, trams, trains, elevators and electric cars, is mentioned as an application where the load profile cause power cycling. In such applications the reliability is important and the components are expected to have a long lifetime. A typical reliability criteria for these applications is the capability to withstand up to 10 million power cycles [24]. For railway equipment, the required life expectancy is typically 30 years, corresponding to 5 million inter-station power cycles and 100 000 h working time [28].

Many more applications for power semiconductor components than those mentioned here have either a cyclic load profile, a low operating frequency or possibly a rapidly changing ambient temperature. In many cases a combination of all these factors probably occur. The purpose of describing all these applications, is to show that although a power cycling test is an accelerated lifetime test performed in a laboratory, the stress it exposes the components to is very realistic.

3.4.2 Failure Limits in Power Cycle Testing

A clear definition of device failure is important in reliability testing, and since the reliability of a device will be measured in how many power cycles it can endure, it is then essential to find out exactly when the failure limits are exceeded. Continuous measurement of critical parameters for a test object is therefore necessary.

Change in the collector emitter saturation voltage $V_{ce,sat}$ is one indication on device failure. The magnitude of I_{load} is kept constant under power cycle testing, therefore a change in resistance or temperature will lead to a change in $V_{ce,sat}$. In power cycle testing of IGBT modules, $V_{ce,sat}$ is a particularly important parameter to monitor. Bond wire lift-off leads to increased resistance and a step change in $V_{ce,sat}$ [7, p.392]. An increase in $V_{ce,sat}$ of 5 % to 20 %, depending on the supplier and the measurement accuracy, is a typical failure-limit for IGBT modules. Since the bond wires usually fail completely shortly after the first step change in $V_{ce,sat}$, the different failure limits have only negligible effect on the predicted lifetime [7, p.392].

Although press-packs do not have bond wires that can break, other failure mechanisms can lead to increased V_{ce}. Change in gate-emitter resistance (R_{ge}) is one example. Since an IGBT has an insulated gate, R_{ge} should be very high. Results from press-pack power cycle testing has shown a great reduction in R_{ge} in failed devices. A decrease in R_{ge} can lead to an increase in gate-emitter current(I_{ge}). If I_{ge} increase above what the gate driver is able to deliver, the result will be a reduction in the gate-emitter voltage V_{ge}. The IV-characteristics of an IGBT dictates that a decrease in V_{ge} will result in an increased V_{ce}.

As for IGBT modules, changes in the electrical resistance under the application of constant load current will lead to changes in V_{ce} for press-pack IGBTs as well. As described in the previous chapters, several factors can lead to changes in the electrical resistance. Some of these factors are: changes in clamping force distribution, reconstruction of the chip metallization and bending of the lid leading to partial disconnection. As several possible stress and failure mechanisms can lead to a changes in V_{ce}, it is evident that continuous measurement of V_{ce} is important.

For module testing, thermal resistance (R_{th}) is one of the parameters used to indicate failure. A typical failure limit for the thermal resistance is an increase of 20 % [7, p.392]. Fractures in the solder between the chip and the DCB will affect the thermal resistance. Whether changes in R_{th} can be used as an failure indicator for press-pack IGBT components or not, is not yet known. As described in chapter 2.4.1, heating of a press-pack can lead to bending of the lid, resulting in partial loss of contact. That should affect R_{th}, further testing will show if it is

sufficient to reveal failure of a component.

Little research on power cycle testing of press-pack components is performed, and therefore the existence of relevant literature is very limited. Failure limits given as a specific increase for certain parameters have not been found for IGBT press-packs.

Chapter 4

SINTEF 2000 A Power Cycle Tester

4.1 Objectives for Power Cycle Testing

The 2000 A power cycling tester was developed by Technical University of Chemnitz (TUC) and SINTEF Energy Research as a part of the project Power Electronics for Reliable and Energy Efficient Renewable Energy Systems (OPE project) [29].

The OPE project had initially three main objectives for the power cycle testing. Firstly, to gain experience with power cycle testing press-pack IGBTs. Secondly, to obtain statistical data to estimate the lifetime as function a of power cycling stress level. This data would be used as input for simulating converter reliability in offshore wind-power applications. Thirdly, to support the projects PhD works on stress modelling of press-pack IGBTs with experimental results [29].

Due to unexpected early failures of the press-pack IGBT discs, the focus was changed to investigating root causes for these early failures. It was important for the OPE project to clarify whether the root cause was related to the tested press-pack discs, or if the applied test procedure was unreasonable hard [29].

4.2 Power Cycling Equipment

When testing press-pack IGBTs in the SINTEF 2000 A tester, a power circuit represented by the simplified schematics in Fig. 4.1 was used. The figure shows how the test objects are placed in up to four bridge legs. Since each leg contains two IGBT test objects, there is no need for an external circuit to control the

current like the single chip tester described in the next chapter has. The bypass leg is used to bypassing the load current when failed test objects are removed from the rig, so that the remaining test objects can continue with same stress level. The reason why the current source is not stopped during these periods is that periodic start/stop would also have given potential lifetime limiting power cycling of the load current source [29].
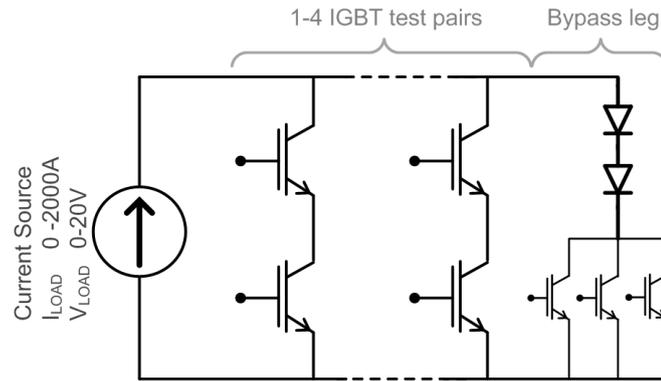
Figure 4.1: Simplifed power circuit for SINTEF 2000 A PCT [29, Fig.1]

The operation of the bridge legs is shown in Fig. 4.2. Fig. 4.2 (a) show the circuit during the heating period, where the entire load current is circulated through the bridge leg for a duration equal to the t_{on}. Fig. 4.2 (b) and Fig. 4.2 (c) show the circuit when T_{vj} of the upper and lower test object is estimated. One of the DUTs is turned off, which prevents any load current from circulating in the leg. The other DUT is conducting a small sense current. Figure 4.2 (d) shows the operating state where both DUTs are turned off, meaning that another bridge leg is using the sense current to estimate T_{vj}. The load current is then either conducted through a third bridge leg or the bypass leg [29].
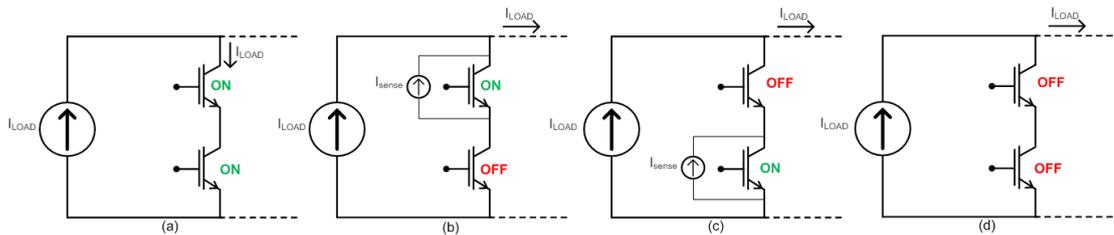
Figure 4.2: Operation states for one bridge leg [29, Fig.3]

Figure 4.3 shows the principle structure for one cycle, as seen from a test object. The load current is conducted through the device for a time t_{on}, and the losses produced by the current heats the device. The device is heated until the load

current is commutated to one of the other bridge legs. The duration of the cooling period t_{off} is the sum of the t_{on} for all the other load current paths. The figure also indicate when the different measurements are made.
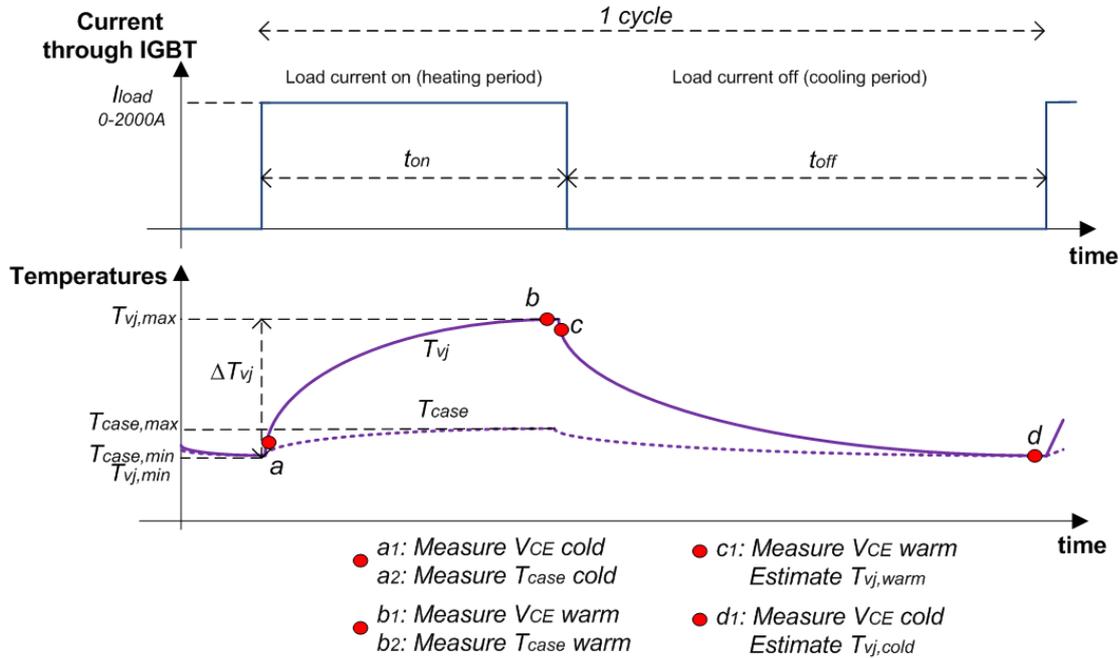
Figure 4.3: Principle schematics for one cycle for the SINTEF 2000 A PCT [29, Fig. 2]

4.3 Summary of Failures

The power cycle testing of press-pack IGBTs in the 2000 A PCT can be divided in test phase A and B.

In phase A, 8 high voltage press-packs discs were tested under very hard test conditions. The load current during the power cycling was 113 % of the rated current. For all the tested devices the ΔT_{vj} was above 100 ℃. When the testing was stopped after a low number of power cycles, 6 of the 8 devices had failed [29].

In phase B, only two test objects was power cycled. The test objects were the same type of IGBT press-pack discs that was tested in phase A. They were tested at a lower stress level than during phase A. ΔT_{vj} under the testing was 68 ℃ for one of the test objects and 82 ℃ for the other. The magnitude of the load current

was 84 % of the rated current, and $t_{on} = t_{off} = 60$ s. Both devices were brought to failure after a relatively low number of power cycles [29]. Exact numbers cannot be given here due to confidentiality.

Measurements made during and after the power cycle testing, indicates similar failure mechanisms for all the failed press-pack devices. The following observations were made:

- Sudden steps in collector-emitter voltage $V_{ce,sat}$

- Drop in gate-emitter resistance

- Increased gate leakage current

- Reduced blocking capability

Six of the eight failed devices were opened and examined. In four of them, one failed IGBT chips was assumed to have caused failure. In the fifth failed device, two failed chips was found. In the sixth examined DUT, it was found that the failure of the device was not due to failure of one or two chips. The final two devices have not been opened and examined yet [29].
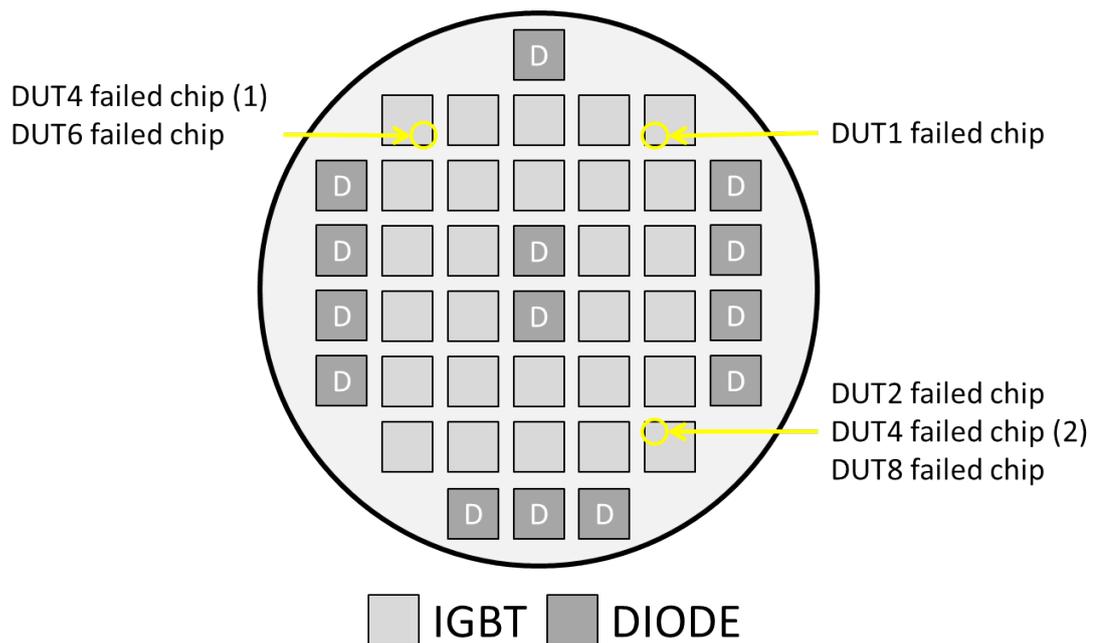
Figure 4.4: Location of failed chips, including the failure area at the specific chip [29, Fig. 3-2]

The tested press-pack IGBTs consist of 28 IGBT chips and 14 diode chips. The

IGBT chips form a 5x6 rectangle, with two diodes in the centre, as shown in Fig. 4.4. All of the six failed chips are located in one of the four corners of the IGBT rectangle [29].

The probability that all of the six failed chips are from a corner area is $\frac{4}{28}^6 =$ 0.0000085, it is therefore not assumed to be a random occurrence. Furthermore, the failure region within the chip always seems to be located at the corner facing the centre of the IGBT disc, see yellow circles in Fig. 4.4. SINTEF is very interested in finding an answer to why all the failed chips are located in the corner of the IGBT rectangle. Currently SINTEF is suggesting a that there could be some special issues related to the location of the chips. Results from FEM-analysis in TUC could possibly support this hypothesis. As described in chapter 2.4.1, FEM-simulations of the pressure distribution in a press-pack showed that the internal distribution of the applied force on a clamped press-pack changes when the clamp is heated [10]. The simulations showed that thermal expansion of the press-pack led to bending of the lid, which in turn led to loss of thermal and electrical contact at the corners of the device [10].

SINTEFs motivation for initiating the development of the single-chip power cycle tester is to investigate what effect the position of a chip has on its lifetime. In addition the single chip tester will hopefully give information on whether the package or the chip itself is the limiting factor in the power cycle lifetime of the press-pack IGBT discs.

Chapter 5

Single-Chip Power Cycle Tester

5.1 Introduction

This chapter will give a description of the single-chip power cycle tester (SCPCT). The motivation for the development of the single-chip tester was to compare the power cycle lifetime of individual chips removed from a press-pack disc, with the lifetime of press-packs tested in the SINTEF 2000 A power cycle tester. The final configuration of the SCPCT can be seen in Fig. 5.1.
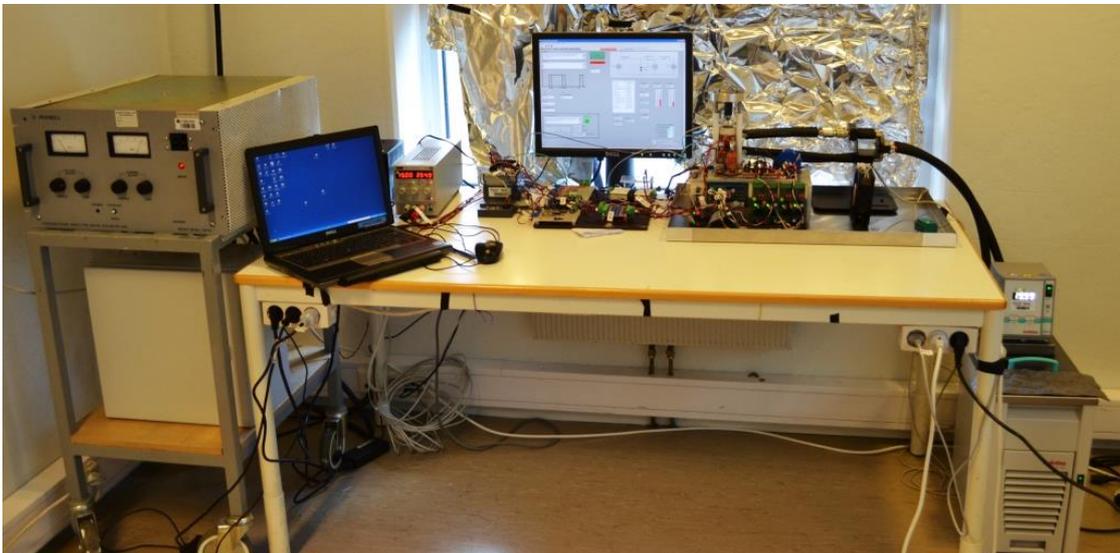
Figure 5.1: Overview of the single chip tester

5.2   Electrical Circuit for Passive Power Cycling

Power cycling is a thermal cycling test where the test object is actively heated by losses in the device. To generate a cyclic temperature in the the device, the load current generating the losses must be turned on and off repeatedly. In the single-chip power cycle tester, this is achieved by switching a constant load current between two current paths.

As described in chapter 3.4, a component can be both actively and passively power cycled. The single-chip power cycle tester is developed for passive power cycling, meaning the load current is not switched on and off by the test object itself. During a passive power cycle test, the IGBT test object is kept on by applying a constant positive voltage between its gate and emitter. The test object is therefore always in on-state, and all switching of the load current is performed by auxiliary switches as described below.
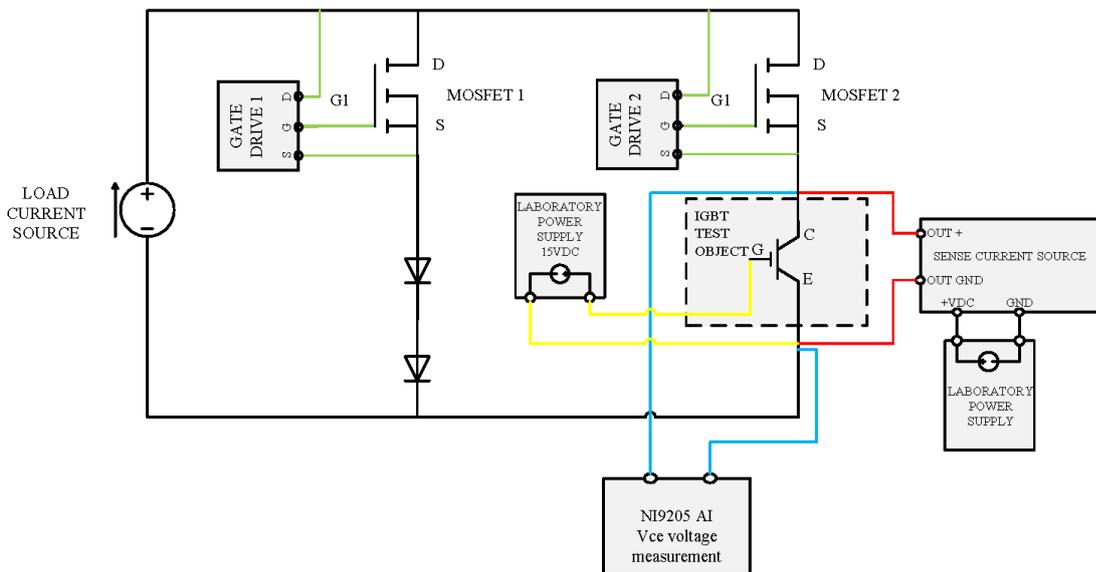
Figure 5.2: Simplified electrical circuit diagram of the SCPCT

Figure 5.2 shows a simplified electrical circuit diagram of the single-chip power cycle tester. The circuit diagram shows a load current source connected to a circuit with two alternative current paths. One is a bypass-path and consist of two diodes in series, the other is the test-object-path with a press-pack IGBT chip. Both paths has a MOSFET switch to control the load current.

It can be seen in the circuit diagram, that a sense current source is connected to the collector and emitter of the test object. The sense current source conducts a

small current (25 mA) through the test object, enabling estimation of T_{vj} using the $V_{ce}(T)$-method. Figure 5.3 shows the sense current source.
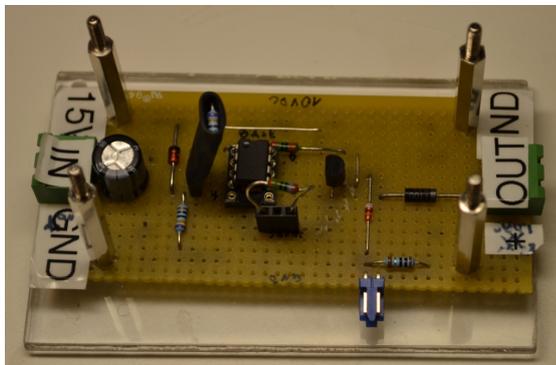
Figure 5.3: Sense current source

The load current switches, MOSFET 1 and MOSFET 2, depicted as a single MOSFET in the circuit diagram, is in the actual circuit made up of four parallel connected MOSFETs. That can be seen in Fig. 5.4. That decreases the current each MOSFET needs to conduct, and reduces the power cycling of them. MOS-FETs are ideal devices for paralleling, due to the positive temperature coefficient of their on-state resistance. If one of the paralleled MOSFETs conduct a higher current than the others, its temperature will increase leading to higher resistance. The increased resistance will in turn decrease the current, hence there is a thermal stabilization effect [30]. MOSFETs have very short switching time and no tail current, therefore fast switching between the two current paths, and voltage measurement immediately after turn-off is possible.

The bypass leg have in addition to MOSFET 1, two diodes in series. By using two diodes in series, the voltage drop of the bypass leg match the voltage drop of the IGBT test object. Regulation in the current source would cause current peaks when switching between the current paths, if the difference in the voltage drop of the two paths is large. Since the diodes are exposed to the same cyclic load current, they are power cycled as well. Ensuring sufficient cooling of the diodes was therefore a priority when developing the mechanical design of the heat sinks. Figure 5.4 shows that the diodes are placed on heat sinks to ensure good thermal conductivity. As it will be mentioned in later chapters, the power cycling lifetime of the diodes was found to be shorter than the length of a test.

Figure 5.5a and Fig. 5.5b show a simplification of the circuit diagram in Fig. 5.2. The figures describes the two states of the circuit during passive power cycling. In Fig. 5.5a the red line highlights the load current path during the heating phase, and in Fig. 5.5b it highlights the load current path during the cooling phase. The
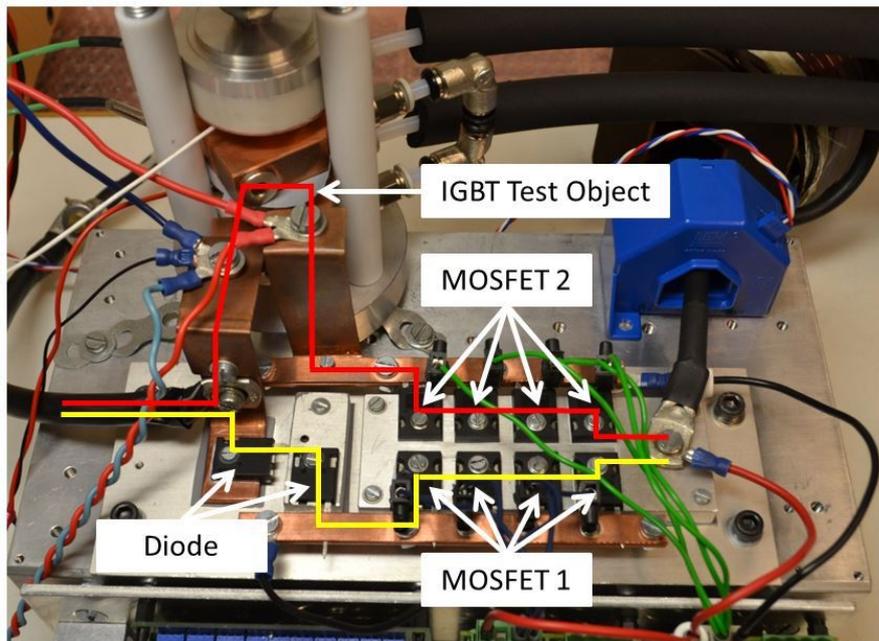
Figure 5.4: Electrical circuit of the single chip tester
The red line indicates the load current path during the heating phase.
The yellow line indicates the load current path during the cooling phase.

(a) t_{on} (b) t_{off}
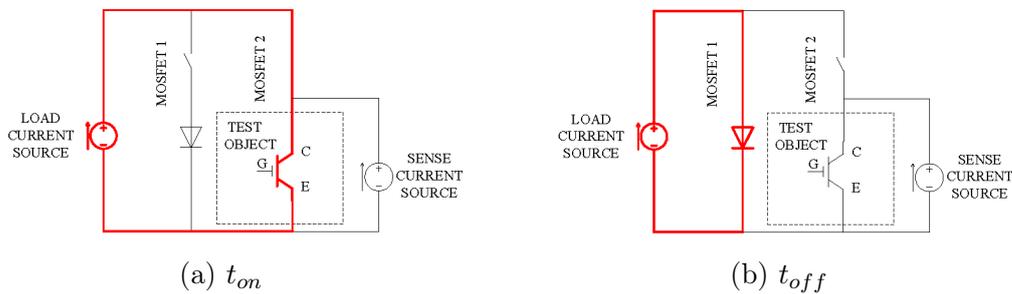
Figure 5.5: Simplified circuit diagram for the power circuit during passive power cycling. The red lines indicate the current path during the different time intervals

figures demonstrates how a chip is exposed to a cyclic load current, while the load current source provides a constant current. This is important to avoid lifetime limiting power cycling of the load current source.

An important goal in the mechanical design of the single chip tester, was to reduce the stray inductance in the electrical circuit to avoid overvoltage during switching. Two of the design choices made to the achieve a low inductive design can be seen in Fig. 5.4. One is that the test object is positioned very close to the MOSFET

switches, the other is that the electrical connection to the press-pack clamp is made with copper strips.

Overcurrents when switching can occur if the voltage seen by the load current source changes rapidly. This is partly prevented by including diodes in the bypass leg. In addition a short overlap time where both MOSFETs are on simultaneously is used. The overlap limits the overcurrents, and thereby also the over voltage when switching. An overlap of 30 µhave been used. In Fig. 5.6 an oscilloscope measurement of the current and voltage during switching illustrates to overlap.
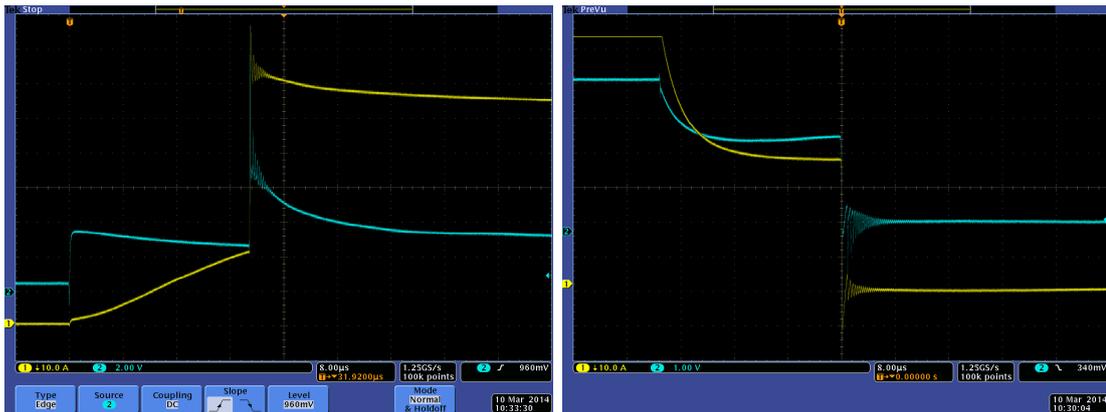
(a) V_{ce} (Blue) and I_{load} (Yellow) Current commutation from bypass leg to test object.

(b) V_{ce} (Blue) and I_{load} (Yellow) Current commutation test object to from bypass leg.

Figure 5.6: 30 µs overlap time during turn on and turn off

5.3   Electrical Circuit for Active Power Cycling

As described above, the single-chip power cycle tester is designed for passive power cycling. In the SINTEF 2000 A power cycle tester, the test objects were actively power cycled. Since the main purpose of the single-chip testing is to compare the power cycling lifetime of press-pack discs and individual chips, it is important to conduct an active power cycling test of a single chips as well.

By doing some simple modifications to the set-up, the single-chip tester can be used for active power cycling. As explained in chapter 3.4, in active power cycling the test object turns the load current on and off. To achieve this without major modifications, the gate-signal used to control MOSFET 2 in the passive test is connected to the IGBT chip, while a constant positive voltage is applied

to MOSFET 2 keeping it constantly on.The modifications is demonstrated in the simplified schematics in Fig. 5.7.

(a) t_{on} (b) t_{off}
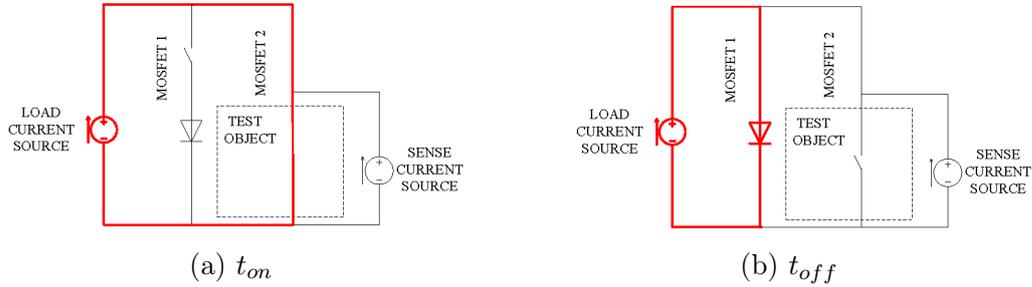
Figure 5.7: Simplified circuit diagram for the power circuit of during active power cycling. The red lines indicate the current path during the different time intervals

The main limitation in using this tester for active power cycling, is that the virtual junction temperature cannot be estimated using the $V_{ce}(T)$-method. As Fig. 5.7 indicates, the IGBT test object can electrically be represented as an open switch during the cooling phase. That prevents the conduction of the sense current through the chip, and consequently the estimation of the T_{vj}. A solution is to start the power cycling of a test object as a passive power cycle test to find a suitable operating point, then stop the test, change to active power cycling, and then complete the test without direct estimation of T_{vj}.

As for the passive power cycling test, an overlap is used when switching between the current paths to avoid an over voltage.

5.4   Clamping Device for Individual Press-Pack Chips

A press-pack device use force to ensure thermal and electrical contact. When testing individual IGBT chips removed from its press-pack housing a custom made clamp is required. The SINTEF workshop has developed a clamping device for individual chips, shown in Fig. 5.8. An explanation of the single-chip clamp is given below the figure.
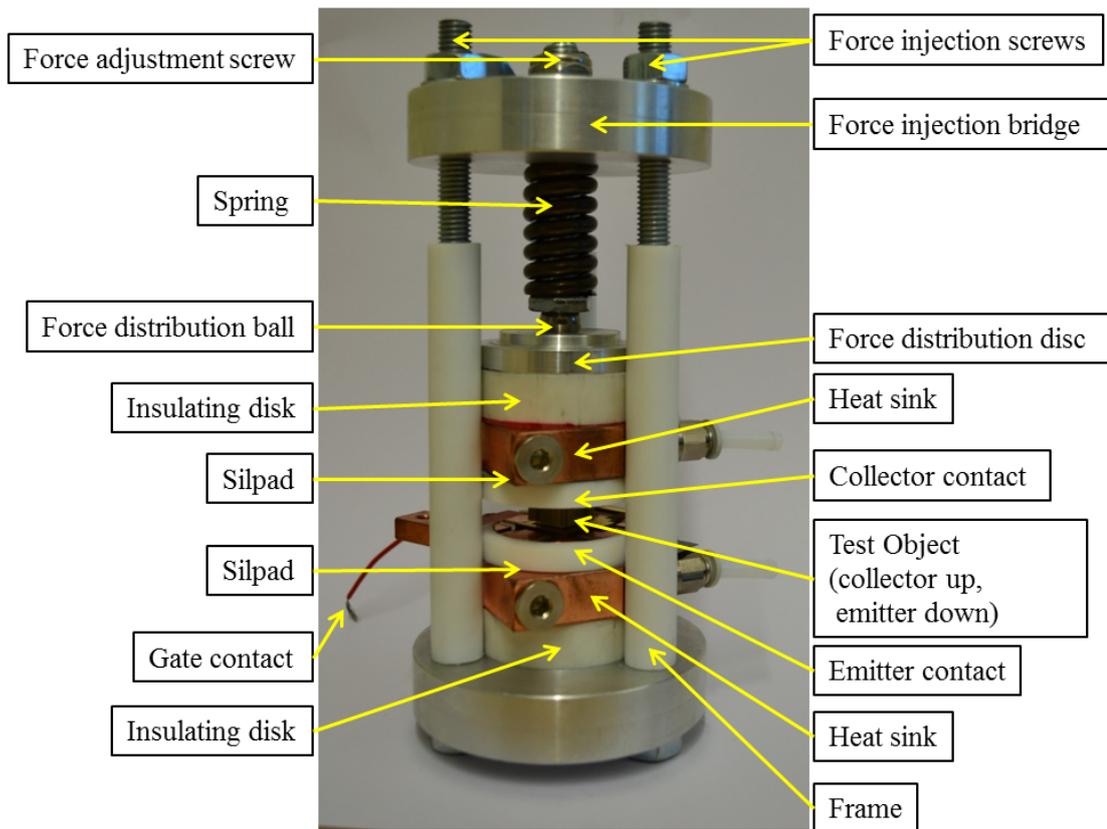
Figure 5.8: Single-chip press-pack clamp

Force Injection Screws   Three screw threads for applying even and controlled force on the clamp.

Spring   For absorbing expansion of the clamp when its heated, and thereby ensuring relatively constant pressure on the test object.

Force Distribution Ball   To obtain even lateral pressure on the chip by injecting the force as a point source.

Force Distribution Disc   Mounting point for the force distribution ball. Converts the point source pressure from the ball to a even pressure for the chip.

Insulating Discs   Ensures thermal and electrical insulation between collector/emitter and clamp.

Pressure Sensor   For measuring pressure with high sampling rate. The pressure sensor is not shown in Fig. 5.8, but can be seen in Fig. 5.9.

Figure 5.9: Pressure sensor with measure module

Heat sink   Copper heat sinks for circulation of liquid coolant.

Silpad   Ensures electrical insulation between collector/emitter and heat sink since silicone-oil is used as coolant.

Collector Contact   Positive load current terminal for the test object and contact point for collector side molybdenum disc. The copper contact is made by cutting out a section of the collector side lid from an IGBT press-pack housing, ensuring similar contact conditions as in a real press-pack. An insulating spacer is placed around the disc for alignment.

Test Object   The test object is a press-pack IGBT die-carrier, or just IGBT chip. Figure 5.10 shows a test object.

Figure 5.10: Press-pack IGBT chip

Emitter Contact   Negative load current terminal for the test object and contact point for emitter side molybdenum disc. It is cut out from the emitter side lid of an IGBT press-pack housing. Its geometry is different from the collector contact, but the surface properties are the same.

Figure 5.11 show how the emitter contact have a copper stem for supporting the single chip shown in Fig. 5.10. This makes it different from the collector contact. The longer distance between chip and heat sink on the emitter side affect the thermal resistance and hence the temperature distribution, this will be explained more in detail later.   An insulating spacer around the copper disc is used for alignment.
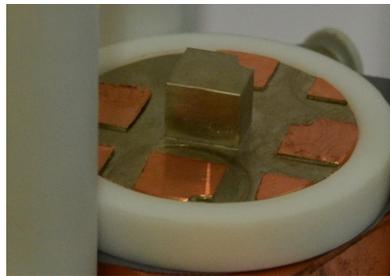
Figure 5.11: Emitter side contact in clamp

Thermocouples   In both the collector and the emitter contact discs, thermocouples are placed in a hole drilled into the contact disc. The thermocouple is not shown in Fig. 5.8.

Gate contact   The press-pack IGBT die carrier shown in Fig. 5.10 has as explained in chapter 2.4.1, a sprung gate-pin. The gate pin connects to a distribution board, cut out from the distribution board of a press-pack disc.

5.5   Control Software - NI labVIEW

Control of the single-chip tester is performed using National Instruments (NI) labVIEW. LabVIEW is short for Laboratory Virtual Instrument Engineering Workbench, and is a graphical software tool for control and measurement applications. LabVIEW is used to generate control signals for the two load current MOSFET switches and to gather and store measurements.

The basic structure of the labVIEW code was developed by M.Sc Lukas Tinschert, while he worked as a research internship for SINTEF Energy Research. The program have been developed further to meet the requirements for high precision switching, high sample-rate measurement of collector emitter voltage and safe operation of the single chip tester.

A code or program in labVIEW is called virtual instrument(VI). The VI for controlling the tester from a PC, serves as a control panel for the tester. A labVIEW VI consist of a front panel for easy control, Fig. 5.12, and a block diagram where the structure of the program is developed, Fig. 5.13.
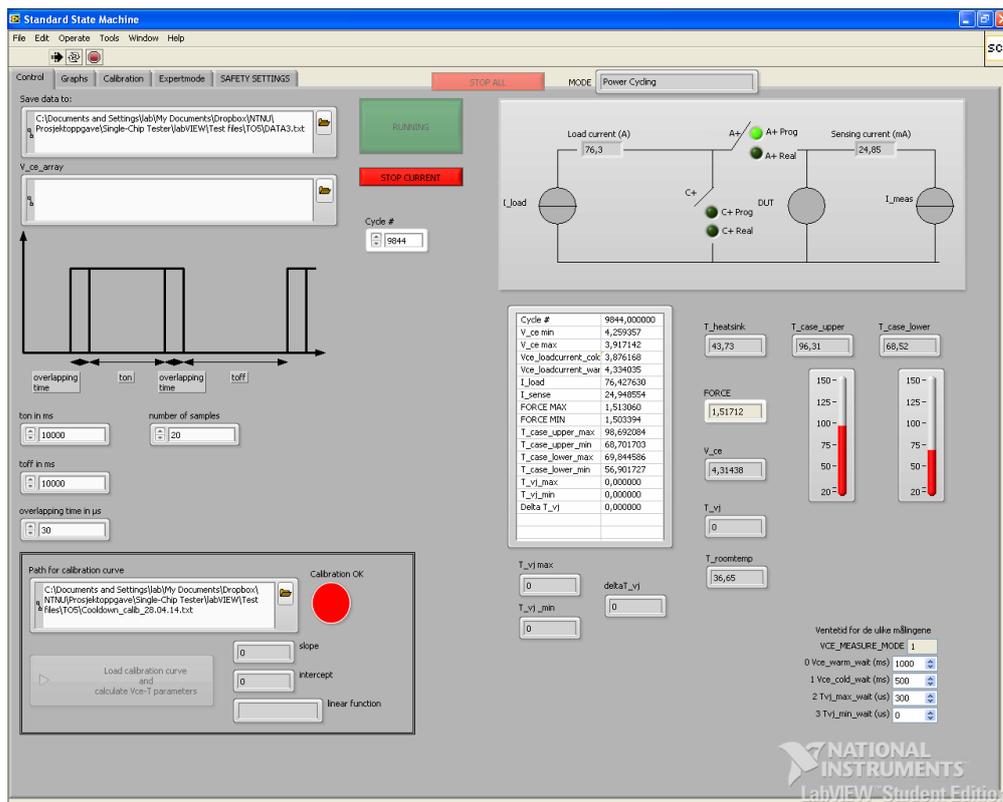
Figure 5.12: Control panel in top-level VI front panel

The control panel shown in Fig. 5.12 contain control input for the test parameters t_{on} , t_{off} and $t_{overlap}$ and measurement parameters like the number of high sample measurements and delay time for high sample measurements. All the measured parameters can also be monitored here.
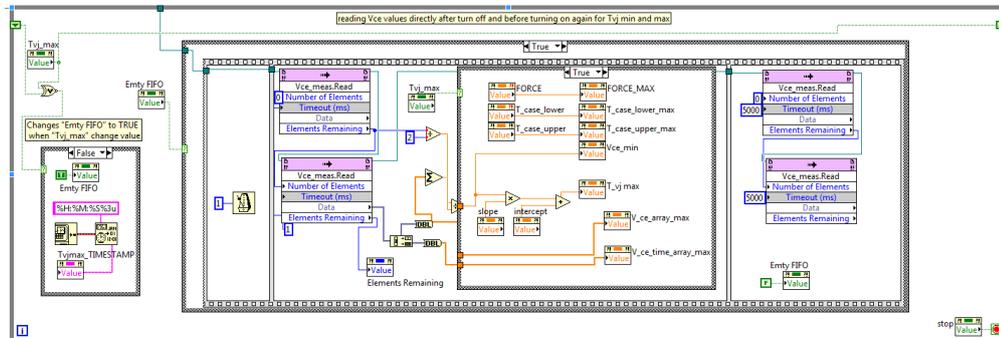
Figure 5.13: Part of labVIEW block diagram

The block diagram shown in Fig. 5.13, is a small part of the block diagram in the top-level VI. As the figure shows, the block diagram contains the graphical source code of the LabVIEW program. For the single-chip tester, the control program is built as a state-machine with different states for start, stop, power cycling and calibration. The graphical code contains many states and sub VIs, making a good representation of the code in a report challenging.

To enable remote monitoring of the single-chip tester TeamViewer have been used. In addition, the laptop in the lab is set to saving data directly to a Dropbox-folder, which also enables remote monitoring of all the measured parameters.

5.6   Control and Measurement Hardware - NI cRIO FPGA

The control software described in the previous section creates digital signals for control of the load current switches, and processes and store all measurements. For gathering the measurements and sending control signals, a NI compact reconfigurable Input/Output (cRIO) Field-Programmable Gate Array (FPGAs) module is used. It enables fast measurement and control of the single chip tester. The NI cRIO FPGA module with input and output modules connected to it can be seen in Fig. 5.14.

In addition to the top-level VI described in the previous section, a VI is made for
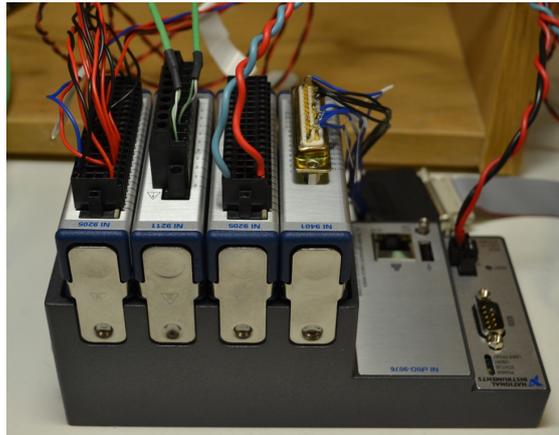
Figure 5.14: cRIO FPGA module with measurement modules

control of the cRIO FPGA module as well. While the top-level VI run on a PC, the FPGA VI is compiled to a code executable on the cRIO FPGA module. The cRIO have a 400 MHz processor enabling loop times in the FPGA code as low as 2.5 ns. High speed calculations and data analysis can therefore be performed in the cRIO device. The acquired measurements are transferred to the host PC using a FIFO buffer.

A NI 9474 Digital Output Module mounted in the NI cRIO chassis is used for sending load current switch control signals to the SINTEF Driver Interface Board v4.0. The SINTEF Driver Interface Board v4.0. connects to the EFI SMD ver. 2 gate drivers, used to control the two MOSFETs load current switches.

The DC converter in the Driver Interface Board power supply generates some of electrical noise. This noise is conducted to the test object, where it has a negative effect on the accuracy of the collector-emitter voltage measurement. To reduce this noise, ferrite cores are placed around the wires between the interface board and the gate driver cards.

Since V_{ce} require high-sample rate measurements, one Analog Input (AI) module is dedicated to only measure V_{ce}. A second NI 9205 AI module are used for force-, voltage- and current-measurement.

The load current is measured using a LEM LA-205-S current transducer. The LEM-shunt and its position can be seen in Fig. 5.4. The output of the LEM-shunt is a current, the AI module therefore measure the voltage drop over a 10 Ω resistor. The sense current is measured by the AI module as the voltage drop over a fixed resistors. The power supply and calibrated measurement adaptor for the pressure sensor produces a voltage signal that is read by the AI module.

Since the ground potential for all the inputs on the AI module is different, a common ground is made. This is done by connecting all the inputs of the AI module to the modules ground potential through a 100 kΩ resistor.

Thermocouple measurement of the collector and emitter contact temperature is performed using pre-calibrated thermocouples. The thermocouple measurements are read by a NI 9211 thermocouple input module.

5.7   Safety Measures Enabling Continuous Testing

Even though the single-chip power cycle tester is designed to perform an accelerated stress test, a test can last for several weeks. Safety features enabling continuous unsupervised testing is therefore an essential part of the test rig. If measurements indicate that the test object, or some of the other components, are about to fail the test must be shut down in a safe manner. Since the tester runs continuously during nights and weekends, it can take a long time from a failure occur until it will be detected by personnel supervising the tester. Therefore the tester must be put in a safe mode when it shuts down.

Before continuous testing was commenced, a risk assessment was performed. The continuous load current of $\approx$ 75 A is a possible fire hazard, and it is considered the major risk factor. The voltage during testing is very low, with a magnitude of less than 5V, there is no risk of electrical shock. The complete risk assessment can be found in appendix A.
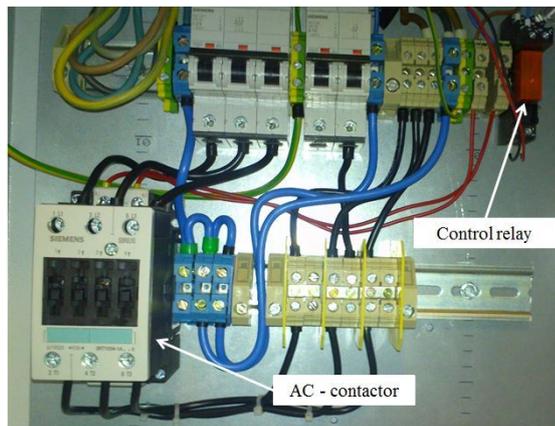
Figure 5.15: AC-contactor, circuit breakers and contactor control relay

To ensure that the single chip tester operates in a fail-to-safe mode, the power to the load current source and the oil cooler is supplied through an AC-contactor.

The contactor is normally off, and it can only be turned on if the tester is running and no failure is detected. The contactor is turned on by a AC-relay controlled by 5V DC signal provided from a custom made analog circuit. The contactor with the required circuit breakers and the 5V contactor-control relay can be seen in Fig. 5.15. The contactor ensures that the power circuit of the single-chip tester is de-energized if a fault is registered. This is an important measure to limit the fire hazard from the load current. Another benefit of using the AC contactor for shut down, is related to the power circuit of the single chip tester being high inductive. If the 75 A load current is switched off using the MOSFETs, a large overvoltage would occur.

Control computer labVIEW program
Software control parameters:
- Vce,sat warm and cold
- Load current
- Tvj
- MOSFET and diode heat sink temperature

If any of these parameters have a value outside the predefined limit, stop is indicated by stopping the software WD signal.

cRIO labVIEW program
Check that a continuous software WD signal is received from the computer labVIEW program. Stop is indicated by stopping the hardware WD signal.

SINTEF Hardware WatchDog Card
Controls that a continuous hardware WD signal is received from cRIO module. If not, 5 V output signal which will trig the safe shutdown card is removed.

Liquid sensor
5V signal to safe shutdown card is removed if leakage is detected

Safe shutdown card
Analog circuit controlling contactor relay. If fault on input is registered, relay on-signal is turned off. Inputs are latching, and must be manually reset.

Smoke detector
If smoke is detected, AC-contactor control relay is disconnected.

Emergency stop button
AC-contactor control relay disconnected if button is pushed.

AC –Contactor
Load current source and oil cooler is de-energized if contactor is disconnected

Figure 5.16: Safe shutdown flowchart

The chart in Fig. 5.16 illustrates how shutdown is initiated by different triggers.

The safe shutdown system is designed so that in the case of any fault, the first action is to de-energize the power circuit.

The safety code-sequence in the labVIEW control-software monitors these parameters: I_{load} , $T_{vj,max}$, $V_{ce,satwarm}$, $V_{ce,satcold}$ and the temperature of the MOSFET and diode heat sink. If any of them are outside the limits specified by the operator, a stop signal is sent to the labVIEW program running on the NI cRIO-module. The stop signal is sent by triggering the software watch dog (WD). The software watch dog is a part of the labVIEW program on the cRIO-module, that is controlling that the labVIEW program on the computer is working. The program on the computer is sending a repeating on/off signal with a certain frequency to the cRIO-module. The program in the cRIO-module is continuously checking that sign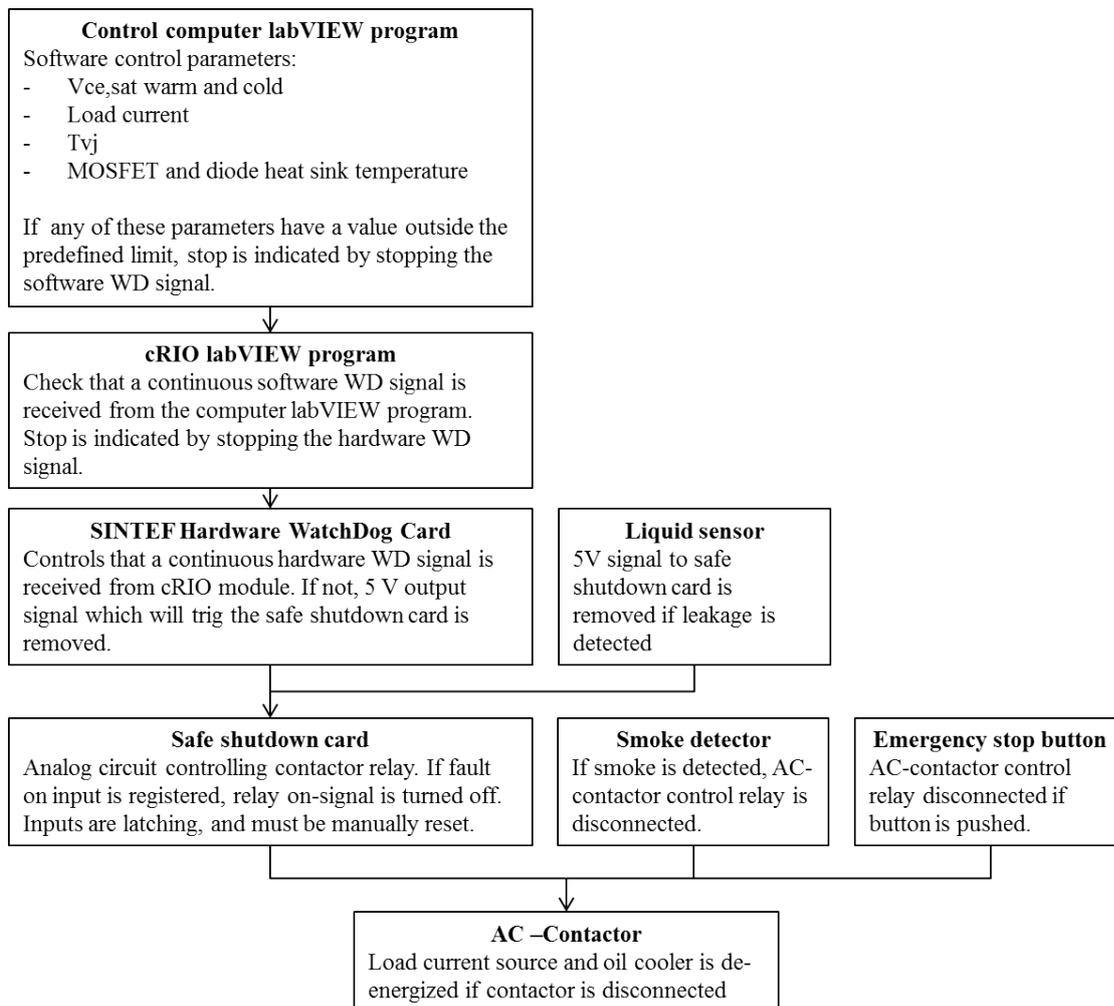al coming from the computer is a repeating on/off signal. If the program in the computer freezes, or is shut off, the signal is no longer repeating. The labVIEW program in the cRIO module will then stop the test. The cRIO labVIEW program stop the test by triggering the hardware watch dog.

Figure 5.17: SINTEF hardware watch dog card

The hardware watch dog system with the SINTEF hardware watch dog card, operates on the same principle as the software watch dog described above. The cRIO labVIEW program sends a digital on/off signal (5 V/0 V) to the WD card. The WD card contains an analog circuit with timers. If the digital on/off input signal is not updated within 500 ms, the voltage on the output of the WD card is decreased from 5 V to 0 V, which in turn trig the safe shutdown-card to disconnect the AC-contactor. The hardware WD ensures that if the cRIO module freezes, the test is shut down in a safe manner. Figure 5.17 show the SINTEF hardware WD card.

The software and hardware watchdog systems is a crucial part of the single chip tester. If either the computer of the cRIO module freezes, the WDs make sure the test is stopped. This is essential, since it is the labVIEW program in the

computer that monitors that all the parameters are within the specified range. The WDs also ensure that the power circuit is de-energised before the switching of the MOSFETs is stopped.

The safe shutdown-card can be seen in Fig. 5.18. It is a custom-made analog circuit using CMOS logic, and a signal MOSFET to control the contactor-control relay. The circuit diagram can be seen in appendix B. The circuit is trigged if the voltage on the input is 0 V. A latching CMOS logic is used; meaning even if a temporary fault is registered, the output will stay off until the circuit is manually reset. It is possible to manually turn on the AC-contactor using a latch at the output.
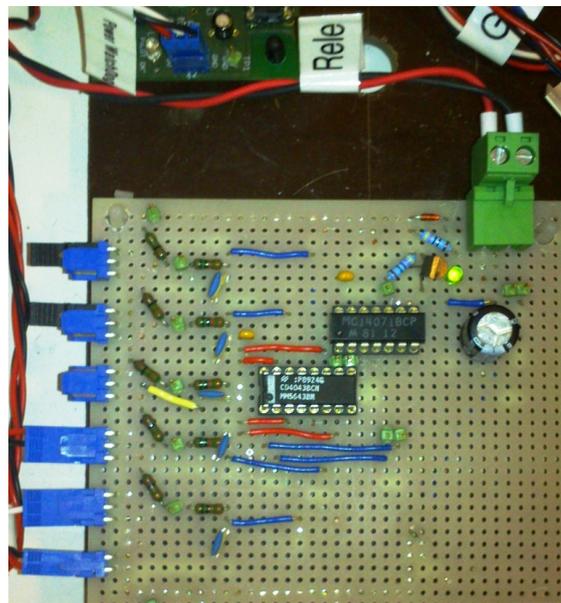
Figure 5.18: Safe shutdown card

5.8   Electrical Characterization of Test Objects

Before starting and immediately after a power cycle test, electrical characterization measurements are conducted. For the electrical characterization measurements, the clamping device is disconnected and removed from the single-chip tester and brought to the SINTEF 2000 A PCT, where there are specialized measurement equipment. In Fig. 5.19 the single-chip clamp can be seen in front of some the equipment used for the characterisation measurements. The characterization measurements are performed on the chip, when positioned in the clamping device.

Figure 5.19: Single chip clamp and characterisation equipment

In the documentation of SINTEF 2000A PCT the characterization measurements are numbered as pre-testing procedure A1.1, A1.2, A1.3, etc. This nomenclature will be used when describing the characterisation of the single-chip test objects as well. It makes comparison to SINTEF 2000 A PCT characterization measurements easy.

Saturation Voltage Characterisation, A1.1

The saturation voltage $V_{ce,sat}$, or forward voltage-drop, is measured for different load current magnitudes. The IGBT is kept on by applying 15 V to gate.

Equipment:

- Schuster DM659 - Forward voltage measuring device
- Mascot Type 719 - Voltage source. Used to generate $Vge = 15$ V

Electrical circuit:
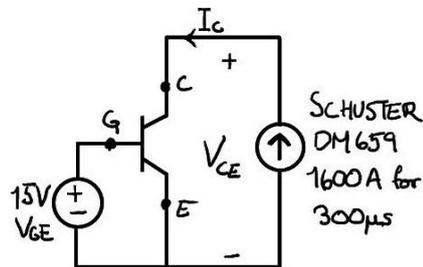
Figure 5.20: Electrical circuit for saturation voltage characterisation [29, Fig. A1.1]

Blocking Voltage Characterisation, A1.2

Gate-emitter is shorted, and the collector leakage current ($I_{C(block)}$) is measured when a collector-emitter voltage is applied. In the A1.2 characterisation of the test objects in the SINTEF 2000 A PCT, the rated blocking voltage was applied to the press-pack disc. For the single-chips, the rated blocking voltage cannot be applied since they are in air, and not an electrically insulating gas as they are inside a press-pack. To avoid destruction of the test objects due to flash-over, $I_{C(block)}$ is only measured for a blocking voltage of $\approx$ 200 V.

Equipment:

- fug HCP 140-35000 - High voltage adjustable DC-source
- Keithley 6485 - Picoampere current meter.

Electrical circuit:
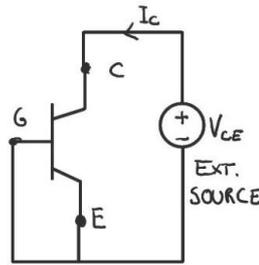
Figure 5.21: Electrical circuit for blocking voltage characterisation [29, Fig. A1.2]

Gate Leakage Current Characterisation, A1.3

With the collector-emitter shorted, the gate leakage current (I_{GES}) is measured when applying a gate voltage of 20 V.

Equipment:

- Mascot Type 719 - Voltage source. Used to generate $V_{ge} = 20$ V

- Fluke 179 - Multimeter. Used to accurately measure and adjust V_{ge}

- Keithley 6485 - Picoampere current meter.

Electrical circuit:
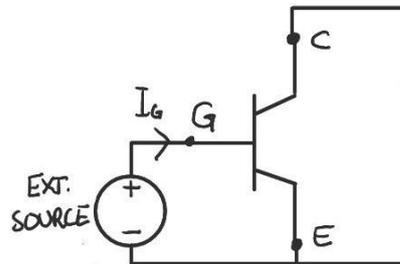
Figure 5.22: Electrical circuit for gate leakage characterisation [29, Fig. A1.3]

Gate Threshold Voltage Characterisation, A1.4

With gate-collector shorted, the collector current I_C is measured while the gate-emitter voltage (V_{ge}) is increased. For the characterisation of the 28 chip IGBT press-pack discs, V_{ge} was increased until I_C=10 mA. If evenly distributed that

means 357 µA per chip. To obtain good accuracy when measuring with the picoamperemeter, it was found that $I_C = 200$ µA was practical limit. The A1.4 characterisation parameter is therefore the value of V_{ge} that gives an $I_C = 200$ µA.

Equipment:

- Mascot Type 719 - Voltage source. Used to generate V_{ge}.

- Fluke 179 - Multimeter. Used to accurately measure and adjust V_{ge}

- Keithley 6485 - Picoampere current meter.

Electrical circuit:
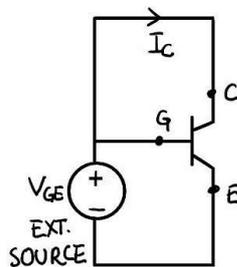
Figure 5.23: Electrical circuit for gate threshold voltage characterization [29, Fig. A1.4]

Gate-Emitter and Collector-Emitter Resistance, A.1.5

The electrical resistance R_{ge}, R_{eg}, R_{ce} and R_{ec} are measured with a multimeter. R_{ce} and R_{ec} is measured with both gate-emitter shorted, and with V_{ge}=15 V.

Equipment:

- Fluke 179 - Multimeter. Used to measure electrical resistance.

Electrical circuit:
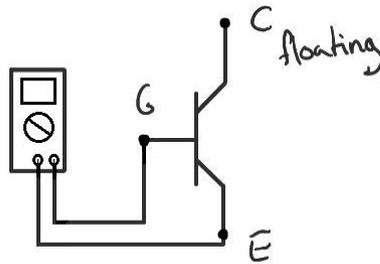
Figure 5.24: Electrical circuit for gate emitter resistance measurement [29, Fig. A1.5]

5.9   Virtual Junction Temperature Estimation

5.9.1   Collector-Emitter Voltage Measurement

The virtual junction temperature (T_{vj}) is estimated using the $V_{ce}(T)$-method, as described in chapter 2.5. Due to fast thermal transients, temperature estimation shortly after the load current is removed is necessary to obtain a correct value of $T_{vj,max}$. High sample-rate measurement of V_{ce} is performed to ensure that.

V_{ce} is measured with a NI 9205 AI module connected to the NI cRIO chassis. Maximum sampling rate for the module is 250 kS/s. For the V_{ce} measurement, a sampling rate of 62.5 kS/s is used, meaning one measurement every 16 µs. This high sample-rate measurement of V_{ce} is performed at the beginning and the end of both the heating and the cooling period, indicated in Fig. 6.2. The V_{ce} measurement at the beginning and the end of the cooling phase is used to calculate the maximum and minimum virtual junction temperature. For all of the measuring points shown in Fig. 6.2, 20 V_{ce} measurements 16 µs apart is made. These values are averaged into one V_{ce} value which is saved to a file. The V_{ce} from the cooling phase is then converted to T_{vj} using calibration data.

5.9.2   Estimation of the Maximum Virtual Junction Temperature

The $V_{ce}(T)$ calibration data, is a series of measurements of the voltage drop created by the sense current at different temperatures. T_{vj} is estimated by converting the V_{ce} during the cooling period to a temperature using calibration data. It is therefore important for the accuracy of the estimation, that the measured V_{ce} is the voltage drop from the sense current alone. It has been found that for the first

300 µs the measured V_{ce} is not a result of the sense-current voltage-drop alone.

(a) Time resolution = 1 ms   (b) Time resolution = 100 µs
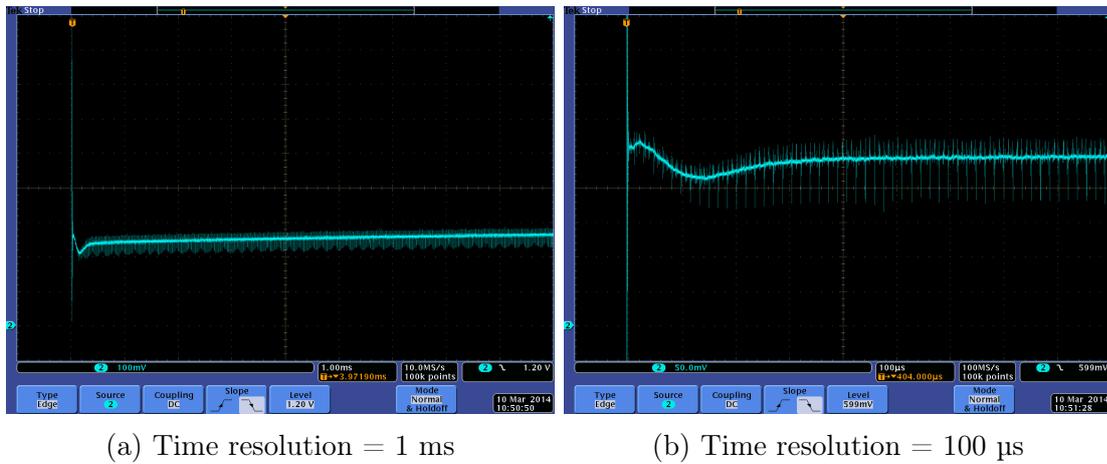
Figure 5.25: V_{ce} at the start of the cooling period

Fig. 5.25a and Fig. 5.25b both show an oscilloscope measurement of V_{ce} after the load current through the test object is removed. Figure 5.25a shows V_{ce} for the first 9 ms of the cooling period. It can be seen that after an initial dip in V_{ce}, there is a gradual increase. Since V_{ce} has a negative temperature coefficient, an increase in V_{ce} means a decrease in T_{vj}. The increase in V_{ce} seen in Fig. 5.25a is therefore the cooling of the test object leading to a decrease in T_{vj}. In Fig. 5.25b the first 900 µs of the cooling phase is shown, showing the inital oscillation in V_{ce} more clearly.

(a) V_{ce} measured with NI 9205 AI module   (b) T_{vj} calculated from V_{ce} measurement
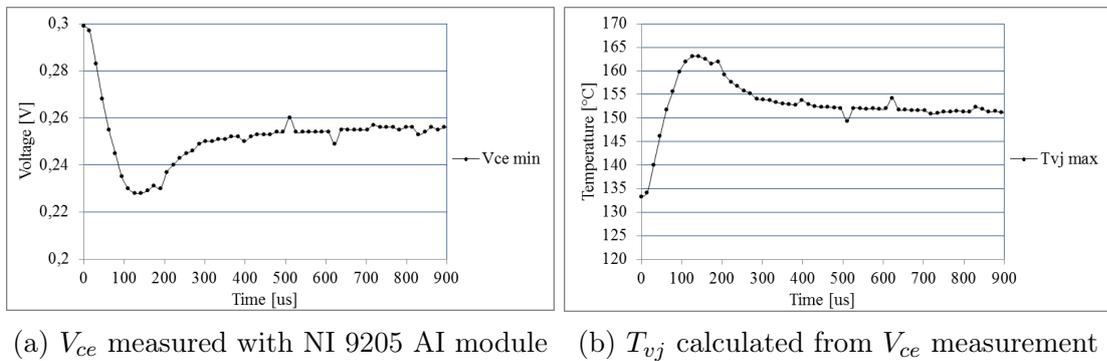
Figure 5.26: V_{ce} and T_{vj} at the start of the cooling period. The dots indicate the measurements

Figure 5.26a shows V_{ce} measured using the NI 9205 AI module and the labVIEW control-program. It can be seen that the high sample-rate measurement of V_{ce} is well within the range of the first transients in V_{ce}. In Fig. 5.26b, the V_{ce}

measurement in Fig. 5.26a is converted to T_{vj}. The figure shows how the dip in V_{ce} corresponds to a peak in T_{vj}. It can be seen that after the oscillation the first 300 µs, T_{vj} is relatively stable within the time scale of the figure.

As described above, $T_{vj,max}$ and $T_{vj,min}$ is made by averaging 20 V_{ce} measurements, converted to T_{vj}. The labVIEW program it is set to make the first of the 20 V_{ce} measurements 300 µs after the removal of the load current, the delay of 300 µs was chosen based on voltage measurements with oscilloscope and the labVIEW program. Since the time between each measurement is 16 µs, it implies that T_{vj} is estimated from V_{ce} measurements from t = 300 µs to t = 620 µ.

To be certain that the V_{ce} used for $T_{vj,max}$ estimation is only the voltage drop of the sense current, a delay of more that 300 µs should have been chosen. The next section will elaborate more on that.

5.9.3   Initial Oscillations in the Collector Emitter Voltage

The oscillation in V_{ce} observed in the first 300 µs of the cooling period, is as explained above not assumed to be a result of the voltage drop created by the sense-current source alone. The V_{ce} behaviour seen in Fig. 5.25b, is interpreted as a DC signal (the sense current voltage drop), with a ripple component on top of it. Investigations on what the cause of this ripple component is, have been performed.

Figure 5.27: Circuit diagram of the single chip tester with load current measurement points highlighted

Incorrect measurements is always a possibility that must be considered. Since the labVIEW measurements (Fig. 5.26a) and the oscilloscope measurements (Fig. 5.25b) show the same V_{ce} behaviour, the measurements are considered correct.

It was first assumed that the regulation in the sense current source was cause of the oscillation. As the circuit diagram in Fig. 5.27 shows, the voltage at the output of the sense current source is the collector-emitter voltage of the test object. When the load current is removed, V_{ce} will almost have a step change from the $V_{ce,sat\ warm}$ of ≈ 4.3 V, to the sense current voltage drop of ≈ 0.3 V. It was considered possible that regulation in the sense current source generated an oscillation in the sense current, which consequently would cause oscillation in V_{ce}. Figure. 5.28a shows the sense current and V_{ce} at the beginning of the cooling period. As the figure shows, there is no oscillations in the sense current, and it is therefore not the cause of the oscillation in V_{ce}.
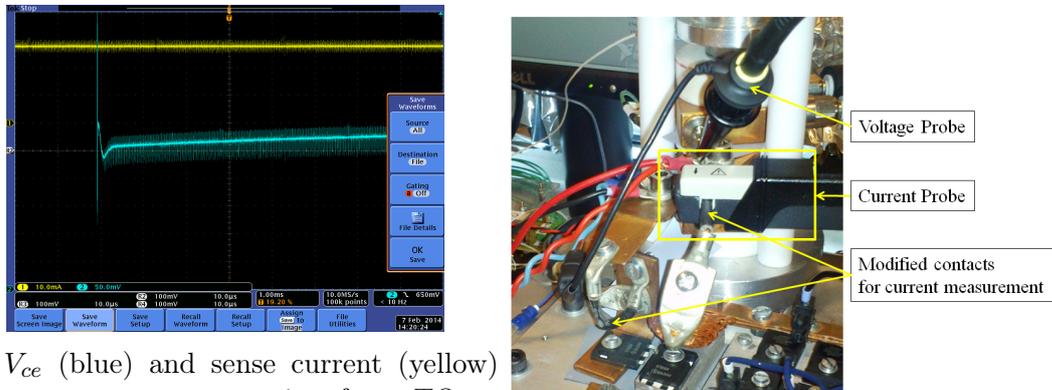
(a) V_{ce} (blue) and sense current (yellow) during current commutation from TO to bypass leg

(b) Position of current probe

Figure 5.28: Measured current and current probe

To further investigate possible causes of the oscillations in V_{ce}, the current at both the collector and emitter side of the test object was measured. Figure 5.27 shows the location in the circuit, where the load current was measured. In Fig. 5.28b the current- and voltage-probe and the modified contacts for current measurements can be seen.

Figure 5.29 shows an oscilloscope measurement of V_{ce} and I_{load} at the start of the cooling phase. The load current was 30 A, which was the maximum for the current probe. Figure 5.29a and 5.29c show the current measured on the collector side, Fig. 5.29b and 5.29d show the current measured on the emitter side. It can be seen that in the first 300 µs after the switching, the current is negative, meaning that it flows in the opposite direction of the load current. If Fig. 5.29d and 5.29c

is compared it can also be seen that the negative current is much larger on the emitter side.
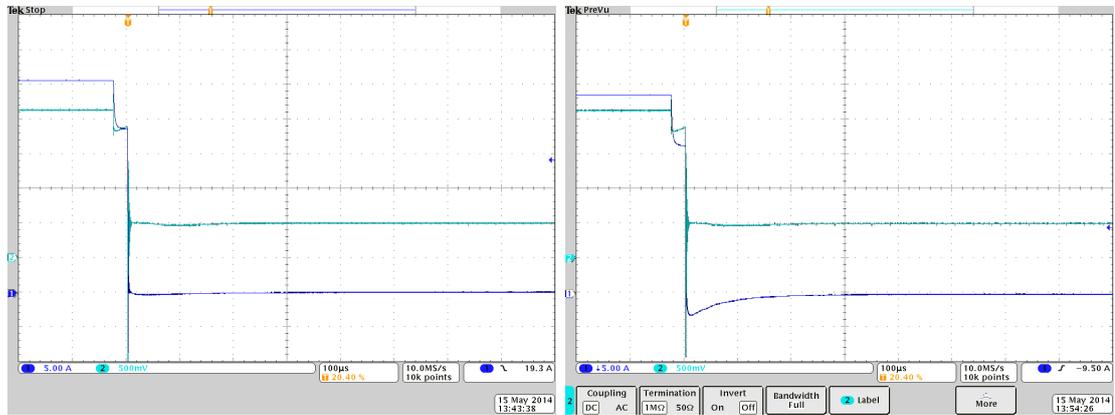
(a) I_{load} measured at the collector side

(b) I_{load} measured at the emitter side
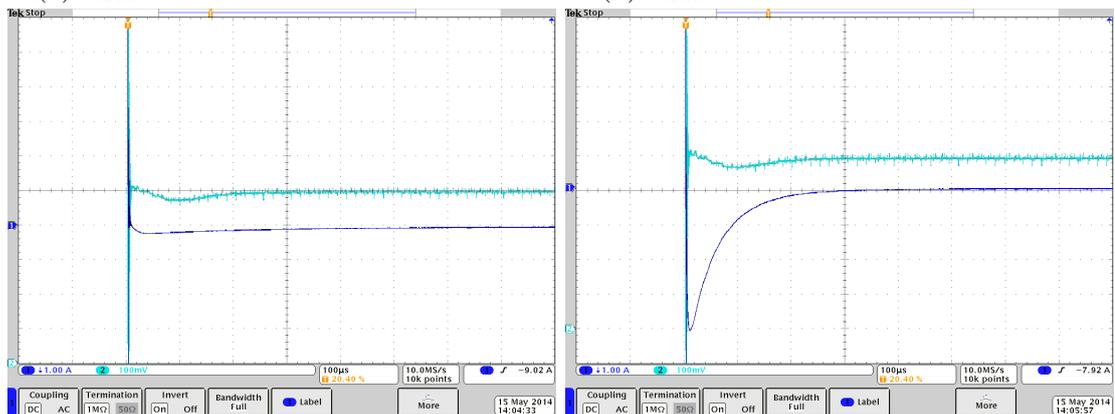
(c) I_{load} measured at the collector side

(d) I_{load} measured at the emitter side

Figure 5.29: V_{ce} (green) and I_{load} (blue) at the start of the cooling phase, $I_{load} = 30\ A$
(a) and (b) show V_{ce} and I_{load} before and after switching
(c) and (d) is zoomed in on the current and voltage behaviour seen in (a) and (b)

In another attempt to find the source of the negative current, and more importantly the implications it has on test results, the current during commutation was measured with a current probe with a higher current limit. This probe is lager than the one shown in Fig. 5.28b, and current measurement was only possible on the collector side. In Fig. 5.30 measurements of V_{ce} and I_{load} is shown for different load current magnitudes.
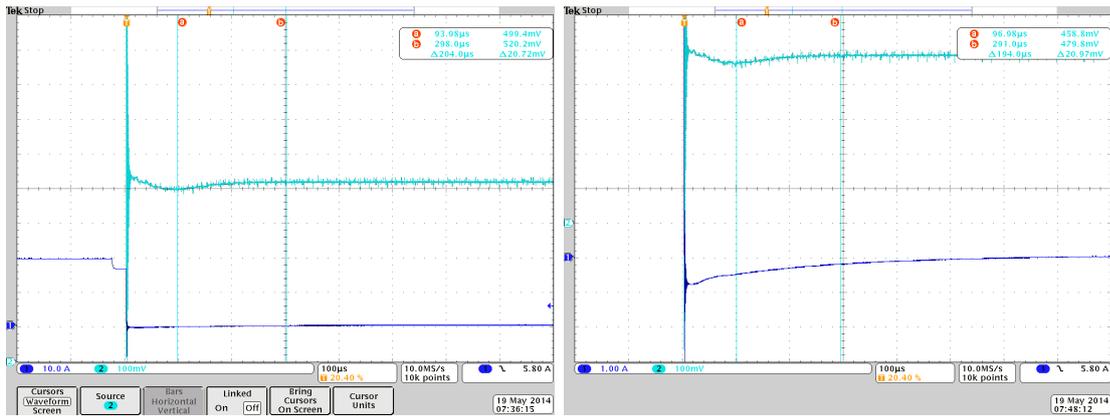
(a) $I_{load} = 20$ A, Overview

(b) $I_{load} = 20$ A, Detail
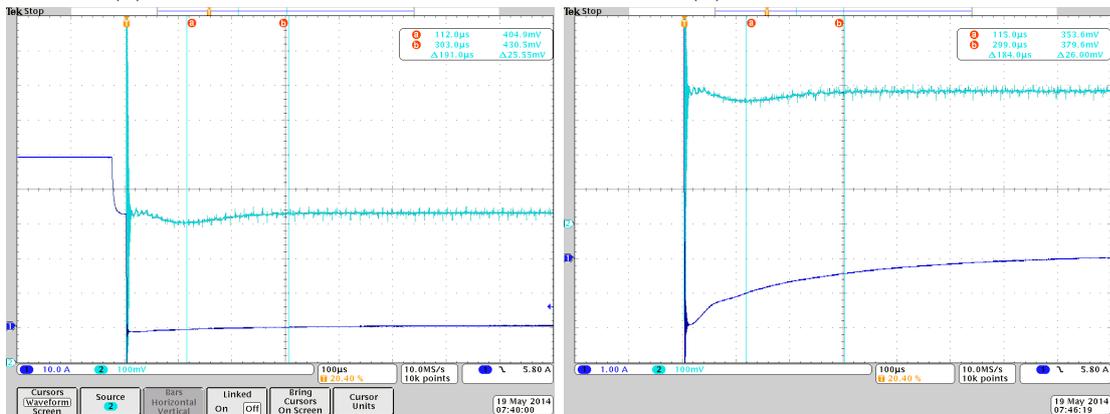
(c) $I_{load} = 50$ A, Overview

(d) $I_{load} = 50$ A, Detail
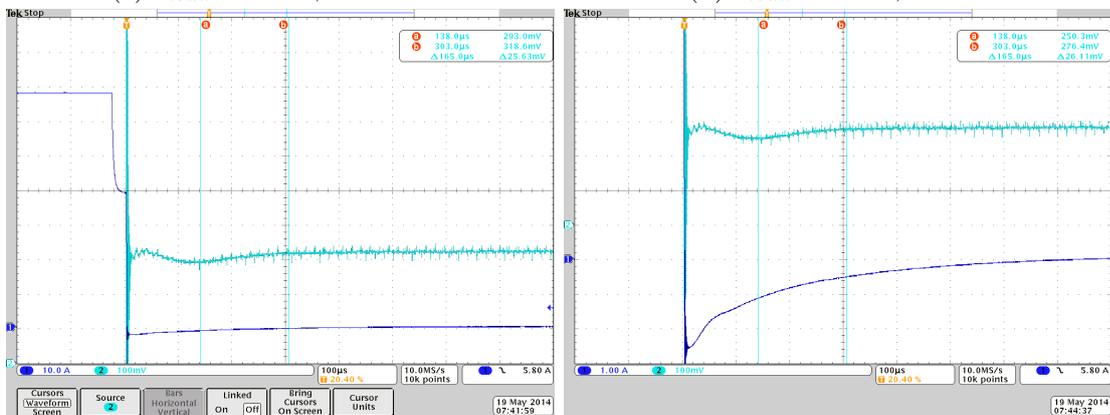
(e) $I_{load} = 70$ A, Overview

(f) $I_{load} = 70$ A, Detail

Figure 5.30: V_{ce} (blue). I_{load} (green) measured at the collector side.
Measured during current commutation from TO bypass leg.

Figure 5.30a, 5.30c and 5.30e show an overview of the load current as it is commu-

tated from the TO to the bypass leg. the overlap time can be seen as a small step between full and no load current. Figure 5.30b, 5.30d and 5.30f show the current measured with a higher resolution, and the magnitude of the negative current for the different values of I_{load} can be compared. The figures shows that the magnitude of the undercurrent, increases with increasing load current. It can also be seen that as the load current is increased the magnitude of the oscillation in V_{ce}, only has a small increase. The minimum point in the oscillation in V_{ce}, seems to occur later when the current is increased.

In Fig. 5.30f it can be seen that with a load current of 70 A, the undercurrent last for over 700 µs. To find out if the negative current affects the estimation of $T_{vj,max}$, V_{ce} was measured when applying a sense-currents in the range 100 mA to 1,3 A. The temperature of the test object was ≈ 20 ℃ when the measurements was performed. Figure 5.31 show V_{ce} at 20 ℃ and 160 ℃(Extrapolated), for different sense current values.
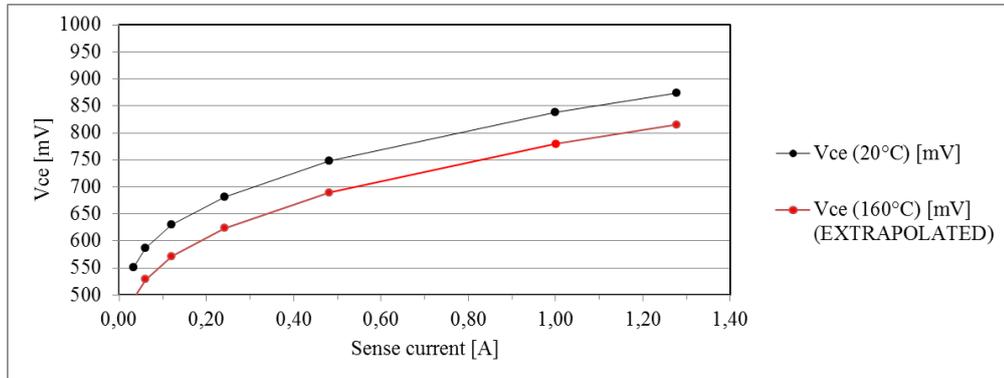
Figure 5.31: I_{sense} and V_{ce}

The V_{ce}-I_{sense} characteristics in Fig. 5.31 show that a negative current of ≈ -2.5 A through the test object, should give a negative voltage drop of in excess of 800 mV. In Fig. 5.30f it can be seen that while the current measured on the collector side was ≈ -2.5 A, the oscillation in V_{ce} have a magnitude of 26 mV.

If the oscillation in V_{ce} is caused by conduction losses from the negative current, a much larger oscillations in V_{ce} should have been observed. It is therefore assumed that although a negative current on the collector side have been observed up to 700 µs after the commutation, it does not have any direct effect on the V_{ce}. The $T_{vj,max}$ estimated from V_{ce} measurements from 300 µs to 620 µs after the switching is therefore most likely a very good estimation of the maximum junction temperature of the chip. The measurement delay of 300 µs was chosen before the cause of the oscillations in V_{ce} was properly investigated. This is unfortunate, since although it

is not believed the $T_{vj,max}$ estimation is affected, a longer delay would would have completely removed this possible inaccuracy.

None of the findings described above explains neither the cause of the negative current nor the oscillations in V_{ce}. It is suggested that the negative current is related to the discharge of space-charges in the IGBT chip. Since the test objects is a high-voltage IGBT chips, a large amount of space charges can accumulate in it. No further explanation on how the discharge might create the negative current will be given here.

Why a much lager current was measured on the emitter side compared to the collector side, is not known either. According to normal circuit theory, currents must flow in closed loops; the magnitude of the current should therefore be independent on where it is measured.

5.10 Distribution of Clamping Force and Thermal Resistance

In the run-in-testing, it was found that when changing test objects, $T_{vj,max}$, $T_{vj,min}$ and consequently also ΔT_{vj} changed. It was first believed that the differences was caused by individual differences between the chips. Therefore three different test objects were power cycled with identical test parameters, $I_{load} = 55\ A$, $t_{on} = 10\ s$, $t_{off} = 10\ s$ and $F \approx 1.4\ kN$. Large variations in T_{vj} was observed, as can be seen in Fig. 5.32.
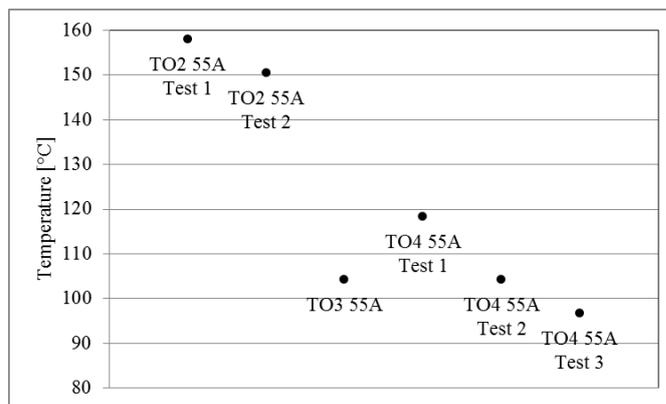

Figure 5.32: $T_{vj,max}$ for different TOs. $t_{on}=t_{on}=10$ s and I_{load} 55 A

It was suspected that the large differences in $T_{vj,max}$, was a result of variations it the thermal resistance (R_{th}). A rough estimation of R_{th}, using equation 5.1

and data from power cycling with $I_{load} = 55$ A, $t_{on} = 10$ s, $t_{off} = 10$ s and $F \approx 1.4$ kN was performed. The R_{th} found should not be interpreted as an absolute value describing the actual thermal resistance, but as relative value used to compare R_{th} of the different test objects. Since the distribution of the heat flow is unknown, an average heat sink temperature is used in the calculations.

$$R_{th} = \frac{T_a - T_b}{P_{loss}} = \frac{T_{vj,max} - \frac{T_{heatsink\ upper} + T_{heatsink\ lower}}{2}}{I_{load} \times V_{ce,sat\ warm}} \tag{5.1}$$
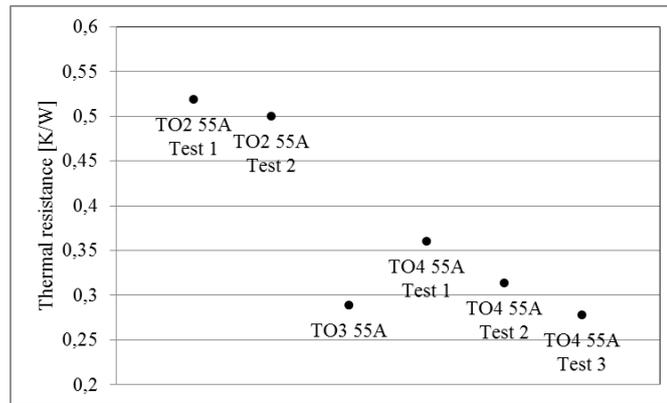
Figure 5.33: R_{th} for different TOs. $t_{on}{=}t_{on}{=}10$ s and I_{load} 55 A

Figure 5.33 shows the calculated R_{th} for the different test objects. It is emphasised that it is a rough estimation, but the large variation in R_{th} indicates that there is an actual difference.

Figure 5.33 might indicate that individual differences between the chips is one of the major factors explaining the changes in R_{th}. Variations in the lateral distribution of the applied clamping force is however believed to be the main reason for the observed differences in R_{th}. When changing test object, the clamping device must be disassembled. After a new test object is placed in the clamp, it is reassembled and pressure is applied by tightening the force injection screws. Although the clamp is made to ensure the same distribution of force every time it is assembled, the large variation in R_{th} for different tests, suggested that the clamping process is not sufficiently precise to ensure that. Minor differences in the position of any parts of the clamp, can possibly lead to changes in the force distribution, which in turn will affect both electrical and thermal resistance.

Further investigations to find the cause of the variations in R_{th} was performed. The distribution of clamping force on the collector side of the chip was analysed

using pressure sensitive FUJI-paper. Figure 5.34 shows how the FUJI paper is placed on the collector contact of the chip.

Figure 5.34: FUJI-paper measurement

In Fig. 5.35 the force distribution on four different test objects can be seen. For each of the test objects three measurements were performed. For all the FUJI-paper measurements shown in Fig. 5.35, the electrical collector-contact to the clamp, highlighted by the yellow rectangle in Fig. 5.38a, was disconnected. Although three FUJI-paper measurements was taken of each test object, the results should be interpreted with care. It seems like each of the test objects have an individual "fingerprint", but the differences are small and its easy to see patterns that do not exist. The conclusion drawn from the measurements presented in Fig. 5.35, is that the distribution of force is similar for all of the four test objects. The force seems to be fairly homogeneously distributed over chip surface.
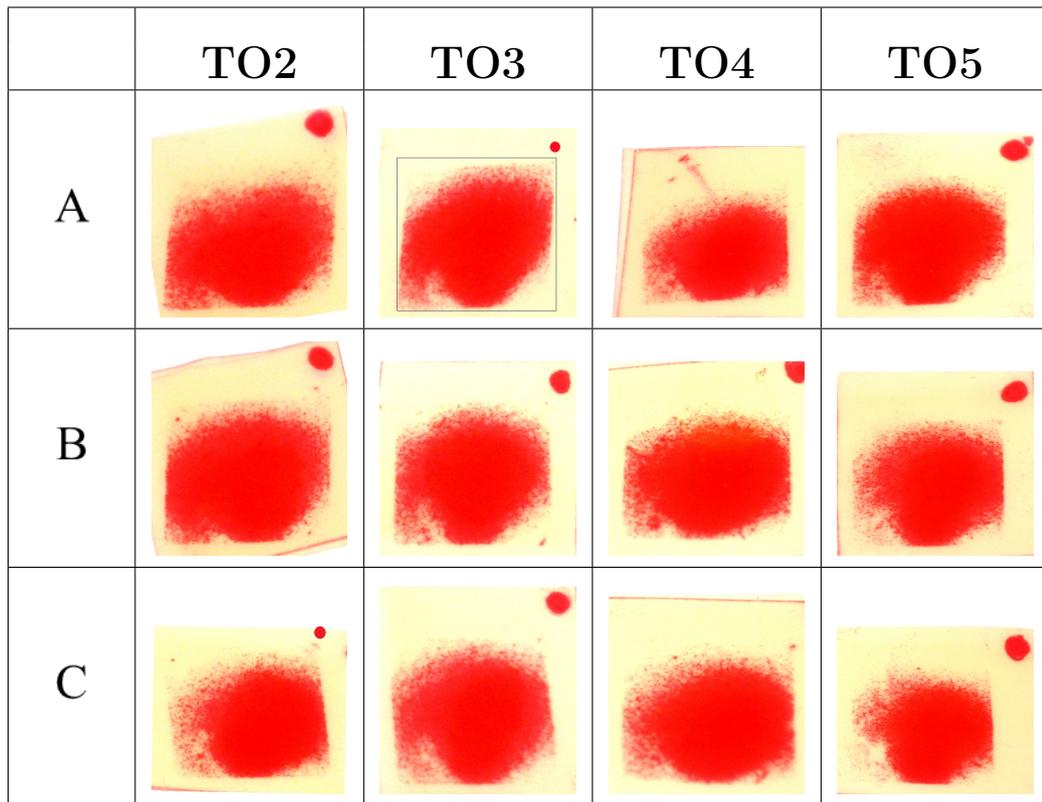
Figure 5.35: Measurement of the force distribution

Although the measurements in Fig. 5.35 indicates that there are no major differences in the distribution of the clamping force for the different test objects, it was still believed that the large variation in R_{th} was related to differences in the lateral force distribution. For a more correct calculation of R_{th}, it should be based on measurements of a test object in thermal equilibrium. Therefore t_{on} was increased to 65.5 s and t_{off} decreased to 500 ms. Figure 5.36 shows the emitter and collector contact temperature for a power cycle with $t_{on} = 65.5$ s and $t_{off} = 0.5$ s. It can be seen from the figure that the temperature stabilises, meaning the test object is in a thermal steady state.

R_{th} for four supposedly identical tests of TO4, was calculated using equation 5.1. The clamp was opened between each test. In Fig. 5.37 the thermal resistance measurements can be seen. The difference in R_{th} values compared with Fig. 5.33, is because only the temperature of the upper heat sink was used. The largest value is 30.5 % higher than the smallest. This is considered a large variation for supposedly identical tests of the same test object.

A FUJI paper measurement of the force distribution with the collector contact
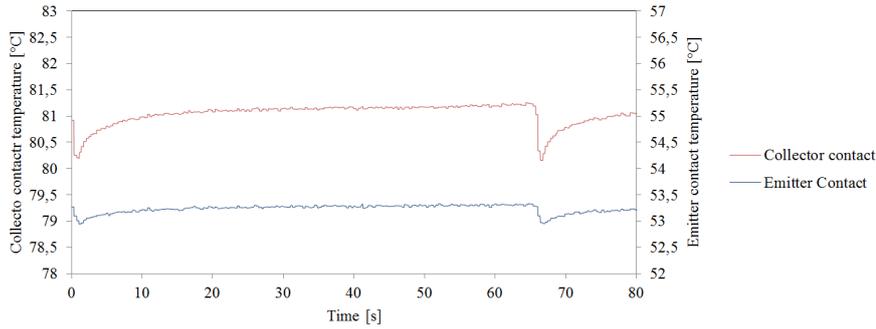
Figure 5.36: Collector and emitter contact temperature under thermal resistance test
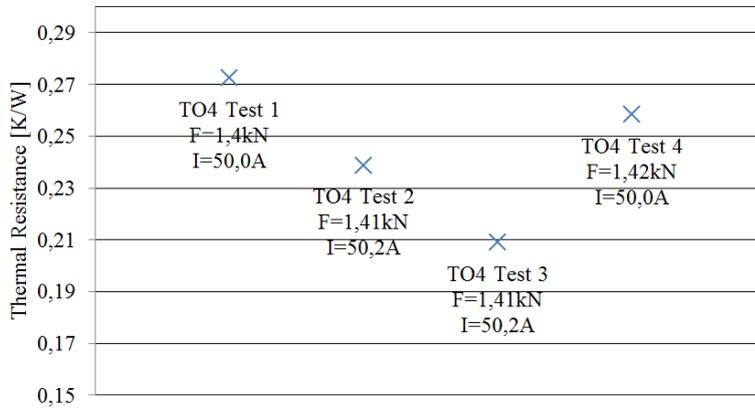
Figure 5.37: R_{th} for four different test on TO4

connected was performed. It showed that the when the contact was connected, the force distribution was severely altered as can be seen in Fig. 5.39a. Several tests was performed, and large variations in the force distribution was observed. Based on this finding it is believed that the large variation in R_{th}, was mainly caused by the collector contact creating a different force distribution every time the clamp was reassembled.

To remove this source of error, a new collector contact was created. Instead of a rigid contact which easily can create a force on the collector contact in the clamp, a flexible contact, shown in Fig. 5.38b, was installed. The distribution of the clamping force with the improved contact can be seen in Fig. 5.39b.

Unfortunately no test of R_{th}, like the one described above, was not performed after the improved collector contact was installed. Such a test would clearly have showed whether the new contact had the desired effect or not. It is believed that the

improvement had this effect. Only minor differences in T_{vj} when testing different chips with the same conditions, have been seen after the contact was replaced. The lack of measurements prevents this to be demonstrated in a scientific way.
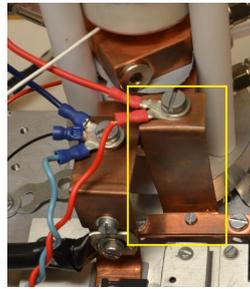
(a) Initial collector contact
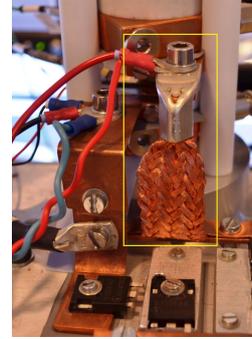
(b) Improved collector contact

Figure 5.38: Connection between clamping device and single chip tester

(a) Force distribution with initial collector contact
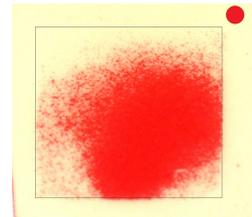
(b) Force distribution with improved collector contact

Figure 5.39: FUJI-paper measurement of the force distribution on the collector side of TO4

5.11   Operating Point and Stress Level

The motivation for power cycling individual chips is to compare their power cycling lifetime with that of press-pack discs. Therefore the stress level is adjusted to be at least as though as when SINTEF power cycled press-pack discs in the 2000 A PCT.

The controllable parameters used to adjust the operating point is, the magnitude of the load current, t_{on}, t_{off} and the temperature of the cooling oil. The goal was to achieve a high ΔT_{vj}, with as short cycle time as possible without $T_{vj,max}$ getting to high.

According to the press-pack disc data-sheet, the maximum operating temperature is 125 ℃. That limit is set for a whole disc, and probably contains considerable safety margins. To achieve tough test conditions, a $T_{vj,max}$ well above 125 ℃ is used. How high $T_{vj,max}$ can be without destroying the device, is however hard to tell. One manufacturer have in an unofficial statement to SINTEF mentioned that the chip should not be damaged by the temperature, as long as it is below 180 ℃. The T_{vj} is estimated using the $V_{ce}(T)$-method, and as explained in chapter 2.5 due to steep lateral temperature gradients, regions of the chip can have considerable higher temperature than the estimated $T_{vj,max}$. Therefore the $T_{vj,max}$ should be considerably lower than 180 ℃. In [21] it is described that for a test where T_{vj} was found to be 108.5 ℃ using the $V_{ce}(T)$-method, a maximum lateral chip temperature of 117.6℃ was found. That means that the maximum chip temperature was 8.4 % higher than the T_{vj} estimation. Based on that, it is considered that a $T_{vj,max}$ up to $\approx$ 160 ℃ can be used without directly destroying the chip.

The ΔT_{vj} used in phase A of the SINTEF 2000 A PCT was above 100 ℃, as described chapter 4.3. It is therefore desirable to use a ΔT_{vj} of at least 100 ℃.

To enable a high number of power cycles during a test, the duration of each cycle should be as short as possible. The custom-made clamping device provide good cooling of the chip, so in order to obtain a large ΔT_{vj} within a short time, a high current must be used. Many different combinations of t_{on}, t_{off} and load current magnitude was therefore tested. It was found that $t_{on} = t_{off} = 10$ s and a load current of 75 A, gave a ΔT_{vj} of almost 100 ℃ with $T_{vj,max}$ between 155 ℃ and 160 ℃.

The applied clamping force to the IGBT press-pack disc should, according to the data-sheet, be between 50 kN and 70 kN. The disc consist of 28 IGBT chips and 14 anti-parallel diodes. It is assumed that the applied force is intended to be distributed equally to all the chips in a device. A force equivalent to 60 kN for the press-pack device was chosen, for each chip that translates to 60 kN / 42 = 1.43 kN.

The test object is cooled through oil cooled heat sinks. The temperature of the cooling oil affects the efficiency of the cooling. For practical reasons the oil temperature is set to 20 ℃. The cooling unit in the oil circulator have a limited cooling capability, therefore cooling the oil is a slow process. When a oil-temperature close to the room-temperature is used, less time is needed to reach stable conditions which is beneficial when starting a test.

To summarize, the value of the controllable parameters is shown in the table below.

I_{load} [A]	t_{on} [s]	t_{off} [s]	$T_{coolingoil}$ [°C]	F [kN]
≈ 75	10	10	20	1.43

5.12   Suggested Improvements to the Single-Chip Tester

5.12.1   Measurement of the Diode and MOSFET Voltage

By including measurements of the forward voltage drop of the diodes and the MOSFETs, the state of the diodes can be monitored to indicate when they might start to fail. This allows for the components to be replaced before they fail. Such an addition would require some changes to the labVIEW control program.

5.12.2   Logging of Current Measurement

Most of the parameters are measured at a specific time during a cycle, as shown in Fig. 6.2. They are stored as a variable in the program until they one time each cycle is saved to a file. The program is set to save data to the file each time a new value of $V_{ce,min}$ is measured. As indicated by point a in Fig. 6.2, that is shortly after the current is commutated to the bypass leg. The magnitude of the load current is measured at the instant all the other data for a cycle is saved to the file.

The behaviour of the load current for one cycle can be seen in Fig. 5.40. The heating phase is from 3 s to 13 s, and the cooling phase from 13 s to 23 s. If the resolution of the x-axis is taken into account, it can be seen that it is very stable. An undercurrent-spike can be seen when the load current is commutated from the bypass leg to the test object (time = 3 s), and an overcurrent-spike when commutated from the test object to the bypass leg (time = 13 s). This is caused by regulation in the current source due to small differences in the voltage drop of the two current paths. The duration of the oscillation is a few hundred milliseconds.

Since the current is measured shortly after the switching, it is not the magnitude of the load current for the majority of a cycle that is measured. When the diodes are healthy it has no implication on the results, due to the low magnitude of the oscillations as Fig. 5.40 shows. If one of the diodes fails into short circuit, which happened several times during the continuous testing, the voltage difference between the current paths increase. That results in a large increase in the over- and under-current spikes. It was found that neither the magnitude or the duration
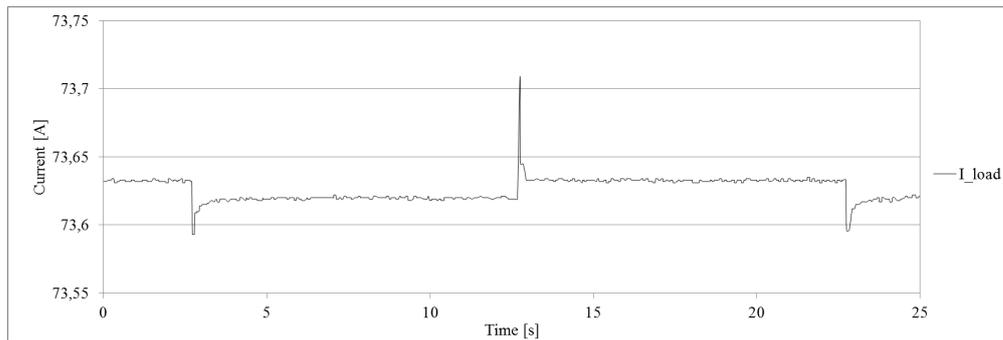
Figure 5.40: Load current for one cycle, TO6

of the oscillation was constant. The implication is that if a diode fails, the log file will give the impression that the load current have been unstable as Fig. 5.41 shows, while it in reality have been stable.

This problem can be solved very easily by changing the when the code store the value of the load current to the file. It was not identified as a weakness of the program until one of the diodes failed. It was not fixed, since it was considered best that the whole test was conducted without changing the control program. In addition to, or maybe instead of, changing the when load current is measured, an average value of the load current during the heating phase could be added.
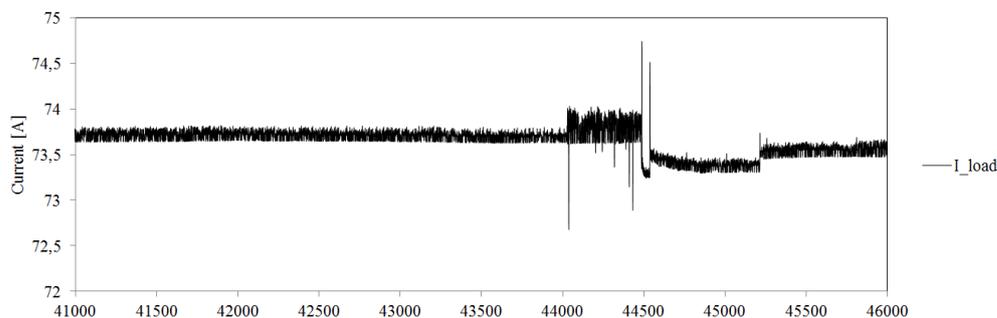
Figure 5.41: I_{load} during diode failure

5.12.3 Diode Heat Sink

To improve the quality of the test results from future testing, the design of the heat sinks for the diodes in the bypass leg should be improved. A possible solution could be to design a liquid cooled heat sink. When the tester was developed, a load current magnitude of approximately 57 A, which is the rated current for a chip,

was assumed. In the run-in-testing, it was found that to achieve a sufficiently high stress level within a reasonably short time, a significantly higher higher current must be used. This puts a lot of stress on the other component in the power circuit. In the continuous testing, it was found that the power cycling of the bypass diodes reduced their lifetime well below the duration of a test. In the next chapter, where the results from the power cycling is presented, this will be clearly seen. For the MOSFETs the stress on each component is reduced by parallel connecting four MOSFETs for each of the load current switches. A parallel connection of diodes might be difficult since they unlike the MOSFETs have a negative temperature coefficient of the forward voltage drop. Diodes with a higher current rating is another possibility, but improving the diode heat sinks is the suggested option.

5.12.4   Emitter Electrical Contact

In the re-design of the diode heat sink it is also suggested that the emitter connection to the clamping device is changed to a flexible contact, like the on showed for the collector contact in Fig. 5.38b.

Chapter 6

Results

6.1 Description of Test Objects

The test objects are IGBT chips, or more precisely IGBT die-carriers, removed from press-pack IGBT discs power cycled in the SINTEF 2000 A power cycle tester. The press-pack discs were power cycled until failure. It is believed that the device failure was due to failure in only some of the paralleled IGBT chips. The rest of the paralleled IGBT chips in the press-pack disc are considered healthy.

The press-pack discs tested in the SINTEF 2000 A power cycle tester, where identified as different devices under test (DUTs). To avoid confusion, an IGBT chip tested in the single-chip power cycle tester, is called a test object (TO).

Figure 6.1 shows the internal layout of a press-pack disc. Indicated in the figure is the test object number of the die-carriers used for single-chip testing. SINTEFs hypothesis is that bending of the lids cause extra stress to the chips in the outer corner of the IGBT rectangle. All the test objects are therefore chips positioned close to the centre of the IGBT disc. It is believed that these chips received less stress during the power cycling in the 2000 A tester.

All the test objects are either from DUT1 or DUT8, which both were power cycled in phase A of the testing with the 2000 A tester. The test conditions in phase A, was described in chapter 4.3. The load current was 113 % of rated current, and ΔT_{vj} was above 100 ℃.

TO1 to TO4 are chips from DUT1 tested in the 2000 A tester, the position of the chips can be seen in Fig. 6.1. After the test in the 2000 A tester was stopped, all the chips were removed from the press-pack disc and placed in an antistatic bag.

This was probably not an ideal storage of the chips, as damages to the gate-pin system and gate metallization possibly could occur.

TO5 to TO8 are chips from DUT8, and the position of the chips can be seen in Fig. 6.1. After the test in the 2000 A tester, these chips were stored in the press-pack disc. The gate and emitter was kept short circuited to avoid accumulation charges in the device. By storing them in the press-pack disc, damages to the gate-pin system and gate metallization is also avoided.
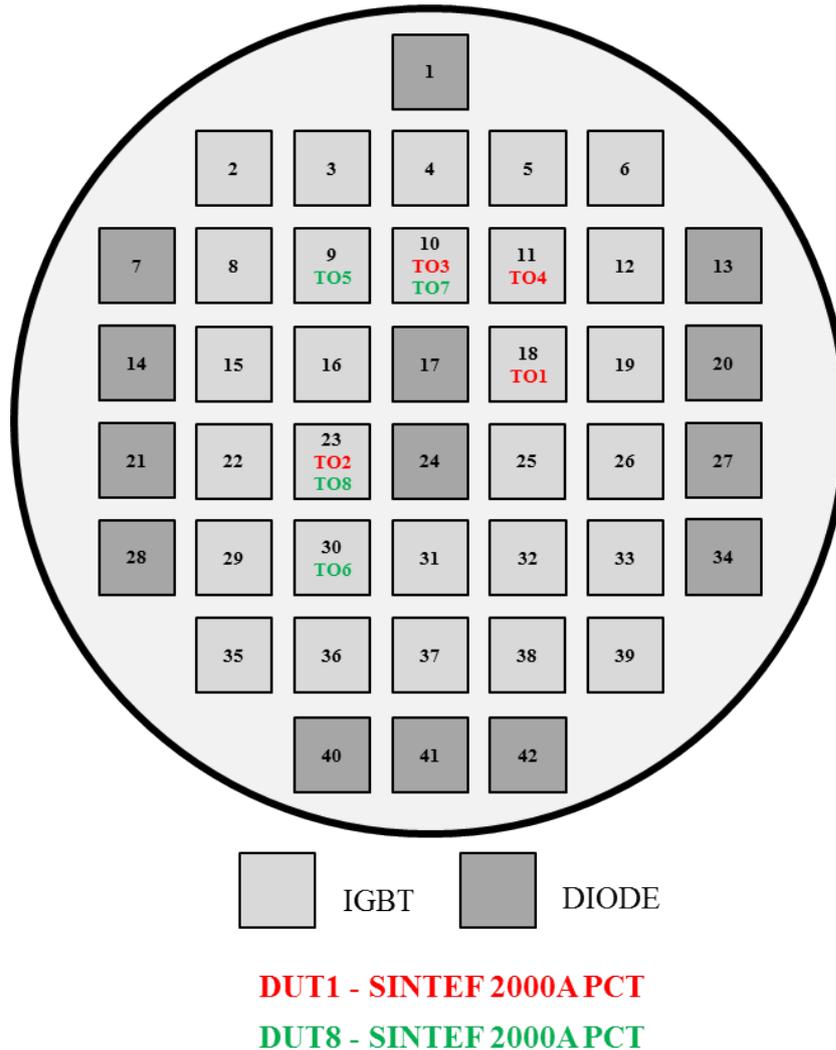
Figure 6.1: Test objects
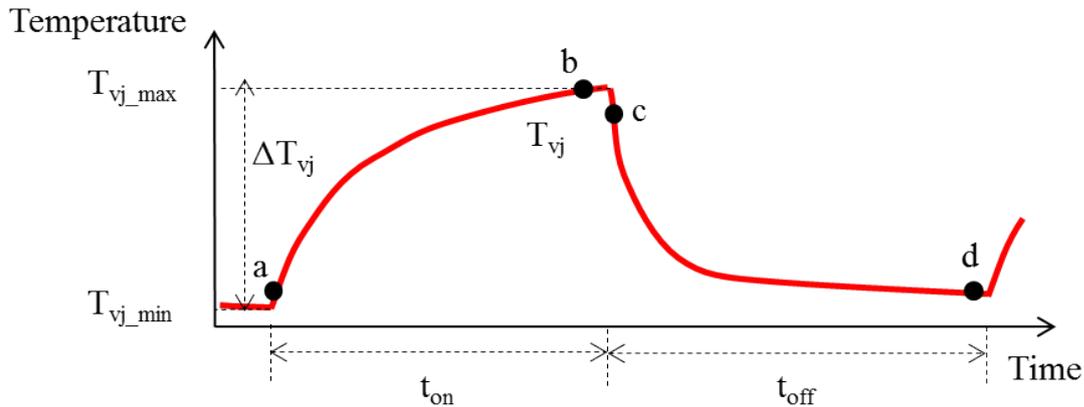
Figure 6.2: Point of measurement for the different parameters

Figure 6.2 illustrate the principle thermal behaviour of a test object during one cycle. The named dots indicate when measurements are performed. The list below describes which measurements that are performed at the different points.

Measurements performed at point <u>a</u>

- Cold-state collector-emitter saturation voltage, $V_{ce,sat\ cold}$

Measurements performed at point <u>b</u>

- Warm-state collector-emitter saturation voltage, $V_{ce,sat\ warm}$

Measurements performed at point <u>c</u>

- Cooling-phase minimum collector-emitter voltage, $V_{ce,min}$
  Used to estimate $T_{vj,max}$ in passive power cycling mode

- Maximum bypass leg voltage, $V_{bypass,max}$
  Voltage drop of the series connection of MOSFET 1 and the two bypass diodes, measured during active power cycling

- Load current magnitude, I_{load}

- Maximum clamping force

- Maximum collector and emitter contact temperature, measured with thermocouples inside the contacts

Measurements performed at point <u>d</u>

- Cooling-phase maximum collector-emitter voltage, $V_{ce,max}$
  Used to estimate $T_{vj,min}$ in passive power cycling

- Minimum bypass leg voltage, $V_{bypass,min}$
  Voltage drop of the series connection of MOSFET 1 and the two bypass diodes, measured during active power cycling

- Minimum clamping force

- Minimum collector and emitter contact temperature, measured with thermocouples inside the contacts

6.2   TO1

TO1 was used for the first attempt on continuous testing, it was only tested during daytime. In the start of one test, the oil cooler was not initially turned on, that resulted in a $T_{vj,max}$ of 250 ℃, the test object was considered destroyed, and the test was stopped. The test served as a run-in test, and valuable experience in using the single-chip tester was gained.

6.3   TO2 - TO4

It was found that when testing TO2 with the same t_{on}, t_{off}, and I_{load} as for TO1, the $T_{vj,max}$, $T_{vj,min}$ and ΔT_{vj} was significantly different. TO2-TO4 was therefore used to investigate how the distribution of the clamping force affects the thermal resistance between a chip and the heat sinks. The results of this testing was discussed in chapter 5.10.

6.4   TO5

The test object was characterized together with TO6. Between the characterization and the intended start of power cycle testing it was stored in a sealed antistatic bag. After installing the test object in the clamp and applying the clamping force, a resistance measurement was performed. It was discovered that the gate-emitter resistance of the test object was 0.2 Ω, which implies that the gate-emitter was short circuited. When this was discovered, the test object was discarded.

6.5   TO6

The first test object power cycled for a sufficiently amount of cycles to say anything about its power cycle durability, was TO6. The test started 19.03.2014 and ran continuously, apart from a few temporary stops, until 11.04.2014. It had then completed 88900 cycles. Given that the chip was still healthy, 88900 cycles is sufficient to conclude that the lifetime of a chips is considerably longer than that of a press-pack discs, and the testing was therefore stopped.

The power cycle test of TO6 was a passive power cycle test, meaning the IGBT test object is turned on for the entire test, while MOSFETs switches are used to control which current paths the load current flows through. Passive power cycling was described in chapter 5.2.

6.5.1   Characterization Measurements of TO6

Table 6.1 shows the characterization measurement performed on TO6 before and after the power cycle testing. Resistance measurement was not performed before the testing started. The resistance values for the post-testing characterization of TO6 are similar to pre-testing values for other test objects, therefore the resistance characterization does not indicate failure.

The electrical circuit used for the different characterization measurements was described in chapter 5.8.

None of the parameters changed significantly, between the pre- and post-testing characterization.

TO6 - Chip30 from SINTEF 2000A PCT DUT8						
		Char A1.1	Char A1.2	Char A1.3	Char A1.4	Char A1.4
Date	#Cycles	Vce, sat	Ic, block	Ige, leakage	Vge(th)	Vge(th)
		Ic=75A	Vce = 151 V	Vge = 20 V	Ice = 200 uA	Ice = 10 mA
17.03.2014	0	2.952	ca 40 nA	immeasurable	5.542	6.215
22.04.2014	88907	3.018	15 nA	immeasurable	5.658	6.345

TO6 - Chip30 from SINTEF 2000A PCT DUT8							
		Char A1.5					
Date	#Cycles	Rge	Reg	Rce	Rec	Rce	Rec
				Vge = s.c	Vge = s.c	Vge = 14.98	Vge = 14.98
17.03.2014	0	-	-	-	-	-	-
22.04.2014	88907	Inf	Inf	Inf	235.6 kΩ	15.4 kΩ	Inf

Table 6.1: Characterization measurements of TO6

6.5.2   Log of Events from the Power Cycling of TO6

Figure 6.3 shows $V_{ce,sat\ warm}$ for the entire test of TO6. The figure is used to describe the test development.
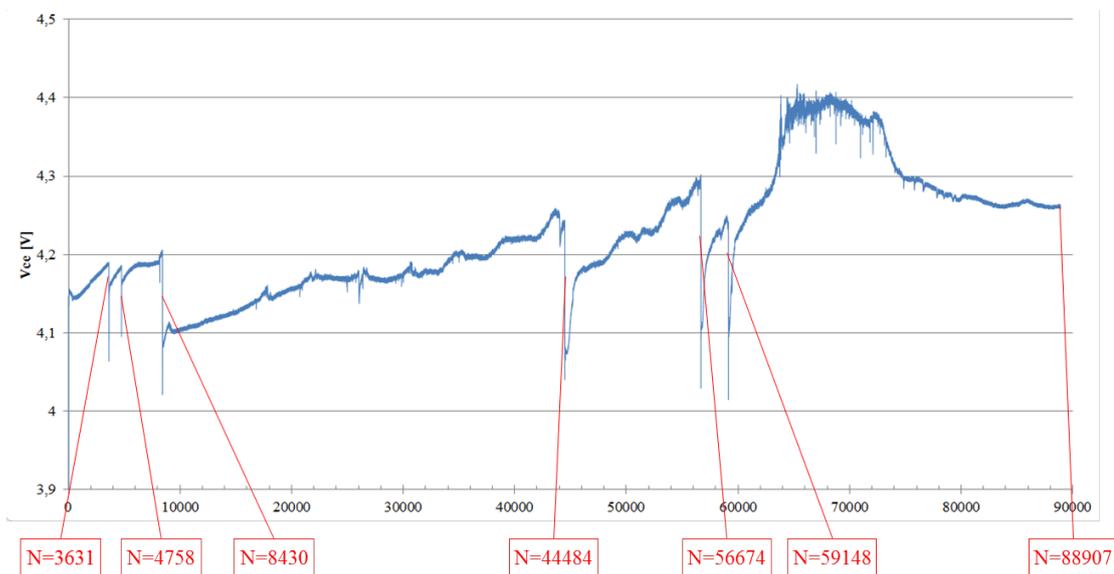
Figure 6.3: $V_{ce,sat\ warm}$ with cycle numbers for stops in testing, TO6

N=3631 Stop in power cycling due to $T_{vj,max}$ above 160 ℃. Initially that was one of the safety criteria for stopping the test. The limit for $T_{vj,max}$ was increased to 170 ℃, and the test was continued.

N=4758 The load current was detected to be below the specified minimum value, and the control software triggered stop of the test. The cause of the drop in load current was not found, and the testing was resumed.

N= 8430 The room temperature increased the first two days of testing, leading to an increase in $T_{vj,max}$ above what was desired. The increase in room

temperature can be seen in Fig. 6.11a, and the increase in $T_{vj,max}$ can be seen in Fig. 6.10b. The increase in the room temperature was mainly due to large losses in the load current source. To limit $T_{vj,max}$ the load current was reduced to 73.5 A.

N=30000 It was observed that the sense current had decreased slightly, it was therefore increased to the level it had when the testing started. This can be seen in Fig. 6.12b.

N=34000 Large daily variations in the room temperature was observed. In the afternoon on sunny days, the room temperature increased with about 5 ℃, as can be seen in Fig. 6.4. The window was therefore covered with aluminium foil to limit the temperature increase in the afternoons. Figure 6.4 clearly shows that the daily swing in room temperature decreases significantly after $N \approx 34000$, when the window was covered with aluminium foil. The figure also shows that the daily swing in $T_{vj,max}$ was reduced.
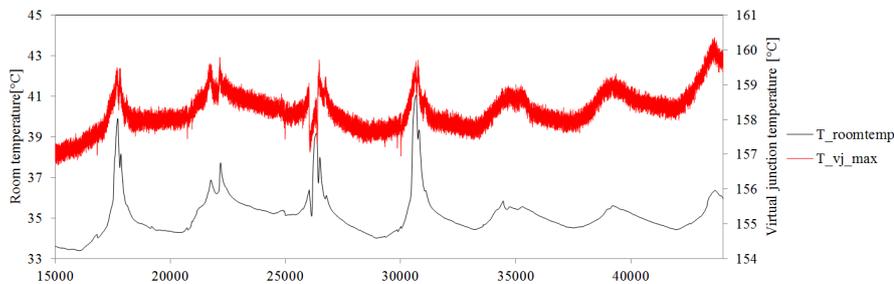
Figure 6.4: Reduction in the daily temperature swing after covering the window with aluminium foil

N=44484 The test was stopped by the labVIEW control program due to the load current being below the specified safety limit. When the power circuit was analysed, it was found that one of the diodes in the bypass leg had broken down, and was short circuited. The short circuit of one of the diodes led to larger difference in the voltage drop of the bypass leg and IGBT test object. The increased difference in the voltage drop of the two current paths, led to an oscillation in the load current during switching between the paths. As Fig. 6.5 shows, for ≈ 500 cycles before the test was stopped the load current appearers to be unstable. As described in chapter 5.12.2, the load current was in reality stable, but since the current was measured shortly after switching from the test object path to the bypass path it appears to be unstable. Most likely, one of this oscillation had an amplitude large enough to trip the current detection in the labVIEW program which consequently

stopped the test.
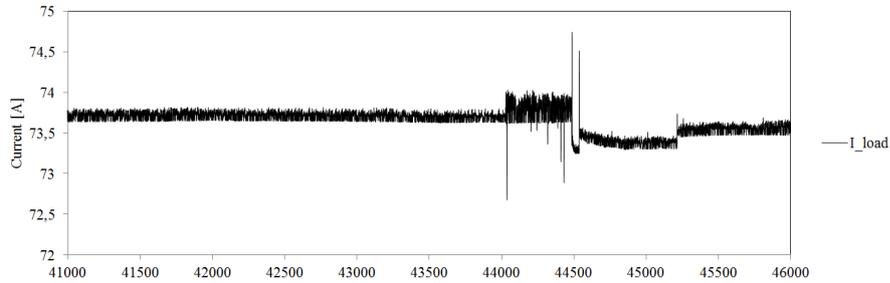
Figure 6.5: I_{load} during diode failure 1

N=56674 The maximum limit for $V_{ce,sat\ warm}$ was initially set to 4.3 V. This limit was reached, and the labVIEW program stopped the test. The limit was changed to 4.5 V, which means a 10 % increase in $V_{ce,sat\ warm}$. The testing was then continued.

N=59148 The second diode in the bypass leg failed, and the test was stopped by the labVIEW program detecting a load current below the specified limit. In Fig 6.6 a ripple in the load current similar to what was observed when the first diode failed can be seen. In Fig.6.7 the backplate of the failed diode next to its heat sink can be seen. The backplate have dark areas indicating that very high temperatures have been present. Both diodes was replaced, and a different thermal paste for better electrical connection was applied.
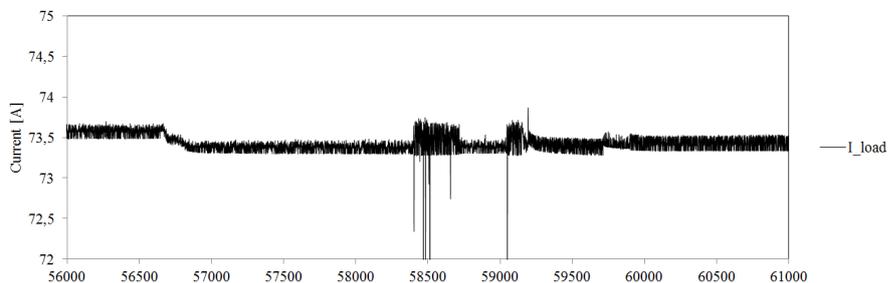
Figure 6.6: I_{load} during diode failure 2

Figure 6.7: Destroyed diode and heat sink

N=88907 The power cycle test was permanently stopped. Figure 6.3 shows that the behaviour of $V_{ce,sat\ warm}$ between $N \approx 63000$ and $N \approx 73000$ was different from how it was earlier in the test. The test was stopped so that investigation of the chip could be performed. After $N \approx 73000$ it can be seen that $V_{ce,sat\ warm}$ at first decreases, then stabilizes. This behaviour suggested that something had changed. It was decided to stop test before the chip was completely broken. Since it was a passive power cycling test, it was not possible to say anything about the chip characteristics during the test. It was therefore not known whether its electrical properties as an IGBT was still intact.

6.5.3   Measurements from the Power Cycling of TO6

Figure 6.8 to 6.14 show the development of some of the measured parameters during the power cycling of TO6. The graphs show one measurement for each cycle.
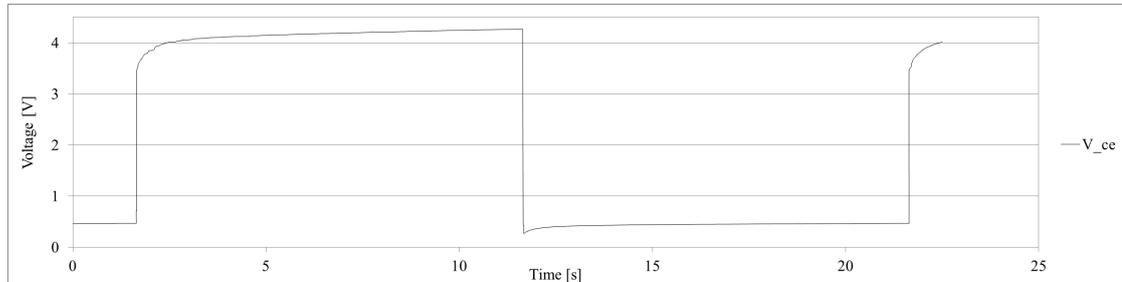
(a) V_{ce} one cycle, TO6
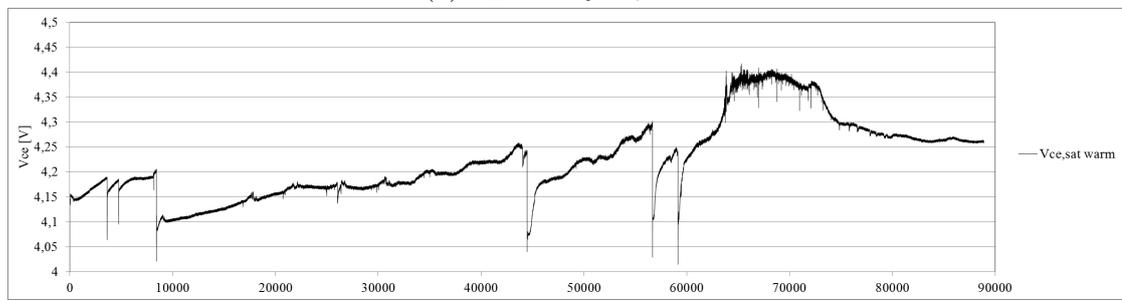
(b) $V_{ce,sat\ warm}$, TO6
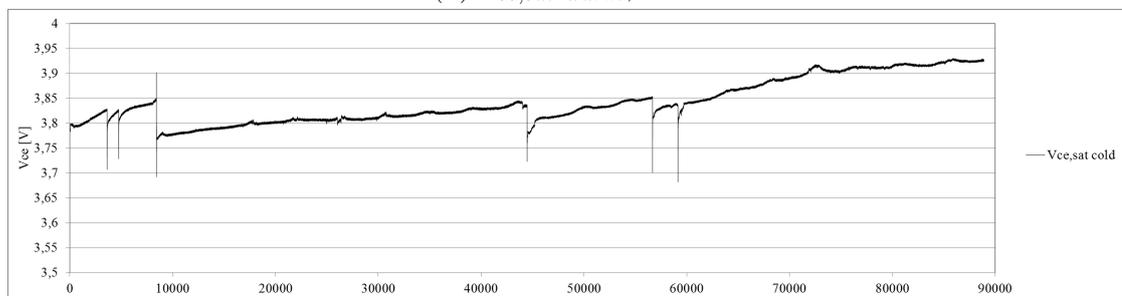
(c) $V_{ce,sat\ cold}$, TO6

Figure 6.8: Maximum and minimum collector-emitter saturation voltage, TO6

Figure 6.8a shows V_{ce} for an entire cycle. The large difference between the voltage drop of the load current and the sense current can clearly be seen. The opposite temperature coefficients of the two voltage drops can be seen as an increase in voltage for both the heating and cooling phase. Figure 6.8b and 6.8c show the development of $V_{ce,sat\ warm}$ and $V_{ce,sat\ cold}$ during the power cycling of TO6. These parameters are measured at the beginning and the end of each heating phase, as

indicated by point a and b in Fig. 6.2. The figures show that the behaviour of $V_{ce,sat\ warm}$ and $V_{ce,sat\ cold}$ are very similar, apart from the development between $N \approx 63000$ and $N \approx 73000$.
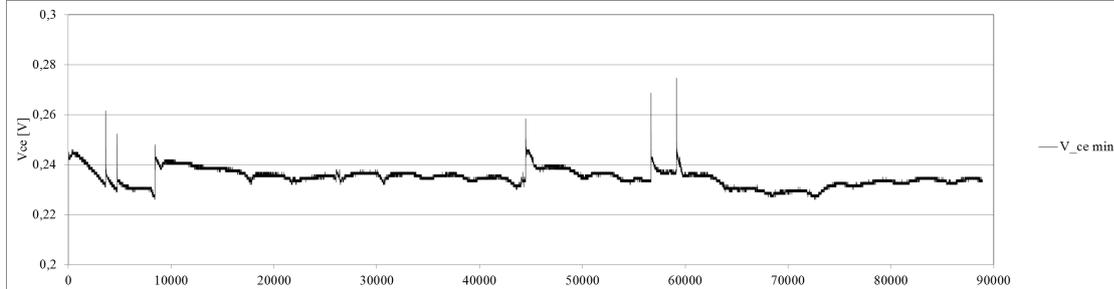
(a) $V_{ce,min}$, TO6
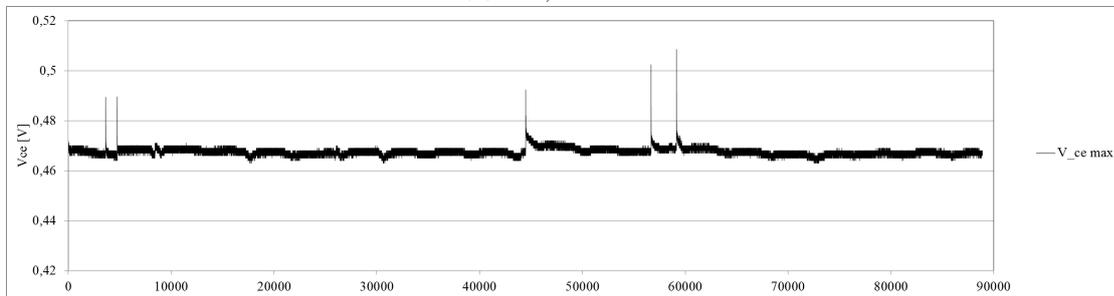
(b) $V_{ce,max}$, TO6

Figure 6.9: Maximum and minimum cooling-phase collector-emitter voltage, TO6

Figure 6.9a and Fig. 6.9b show $V_{ce,min}$ and $V_{ce,max}$, these parameters are measured at the beginning and the end of each cooling phase, as indicated by point c and d in Fig. 6.2. They are the voltage drop created by the sense current, $V_{ce,min}$ is used to estimate $T_{vj,max}$ and $V_{ce,max}$ to estimate $T_{vj,min}$. As this voltage drop has a negative temperature coefficient, in contrast to $V_{ce,sat}$ which has a positive, it can be seen that $V_{ce,min}$ and $V_{ce,max}$ decreases when test is restarted after a stop.
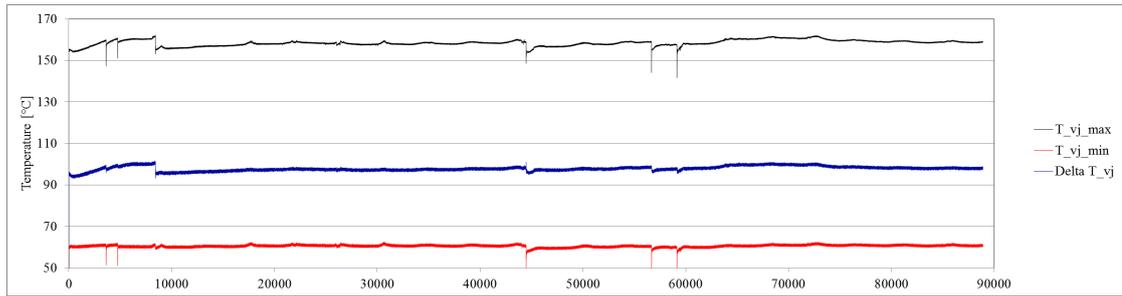
(a) $T_{vj,max}$, $T_{vj,min}$ and ΔT_{vj}, TO6
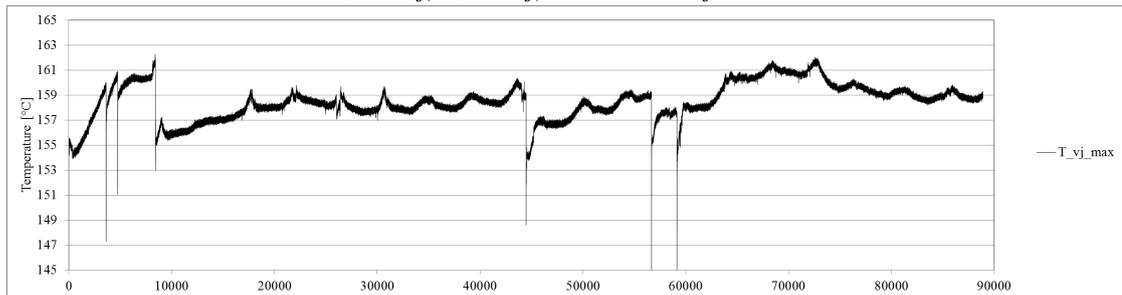
(b) $T_{vj,max}$, TO6

Figure 6.10: Virtual junction temperature, TO6

$T_{vj,max}$, $T_{vj,min}$ and ΔT_{vj}, estimated from the V_{ce} in Fig. 6.9a and Fig. 6.9b, can be seen in Fig 6.10a. Figure 6.10b shows $T_{vj,max}$ with a different resolution on the Y-axis. The figures show that T_{vj}, and consequently also the thermal stress level, was relatively stable for the whole test. A large increase in $T_{vj,max}$ for the first ≈ 4000 cycles was caused by the increase in room temperature, which can be seen in Fig. 6.11a.
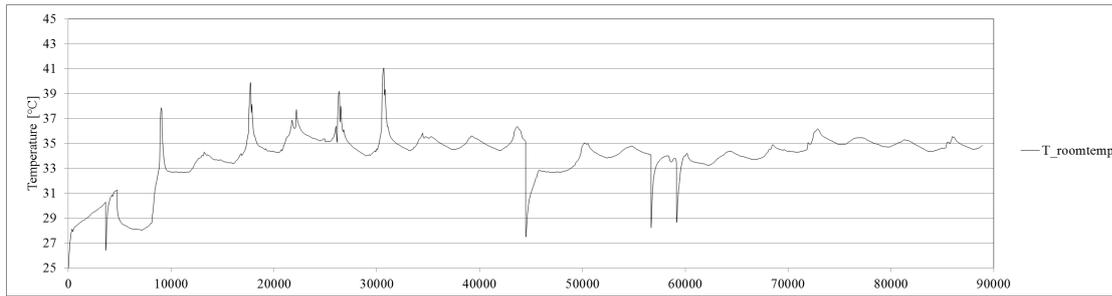
(a) Room temperature, TO6
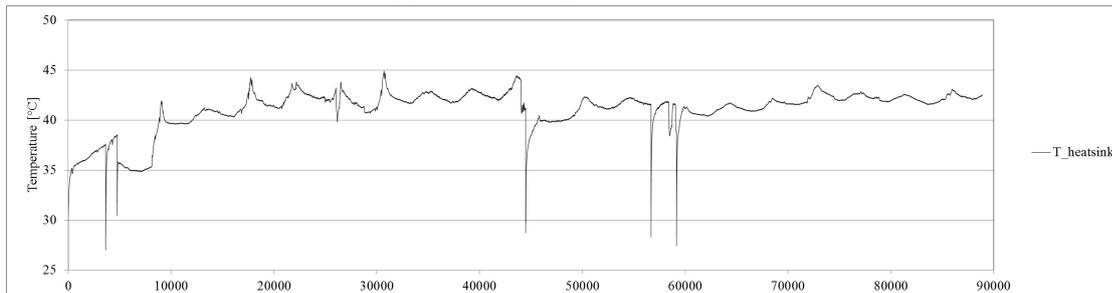
(b) MOSFET and diode heat sink temperature, TO6

Figure 6.11: Temperature measurements, TO6

Figure 6.11a shows the room temperature, and Fig. 6.11b shows the temperature of the MOSFET and diode heat sink. In both figures a steep increase in the temperature can be seen for the first few thousand cycles, followed by a gradual increase until $N \approx 20000$. At $N \approx 5000$ a decrease in both temperatures can be seen. The reason is that the door to the adjacent the room was kept open. It was kept open until $N \approx 8500$ when a very steep increase in temperature can be seen. Firstly this illustrate that the heat production from the single chip tester is large, with the load current source as the main contributor. Secondly it illustrates the large thermal time constant of the room. Both figures also show how the daily variations in temperature is reduced after N$\approx$ 34000, when aluminium foil on the window was installed. Significant drops in temperature can be seen in both figures during the temporary stops. In Fig. 6.11b it can be seen that the heat sink temperature drop when on of the diodes is short circuited, and the voltage drop, and thereby the power loss, in the bypass leg is reduced.
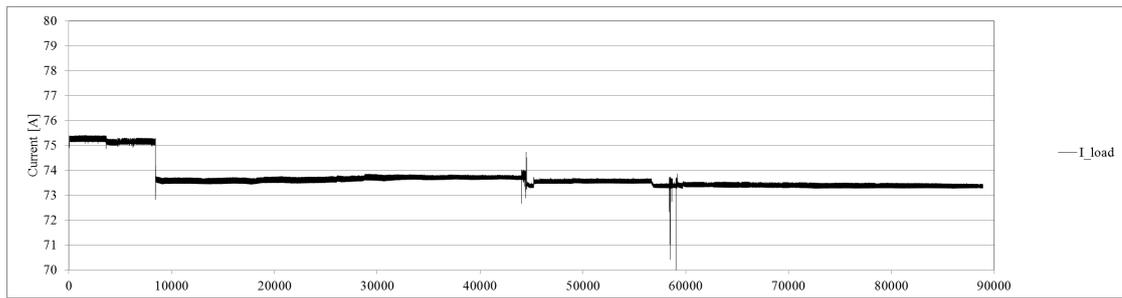
(a) Load current, TO6
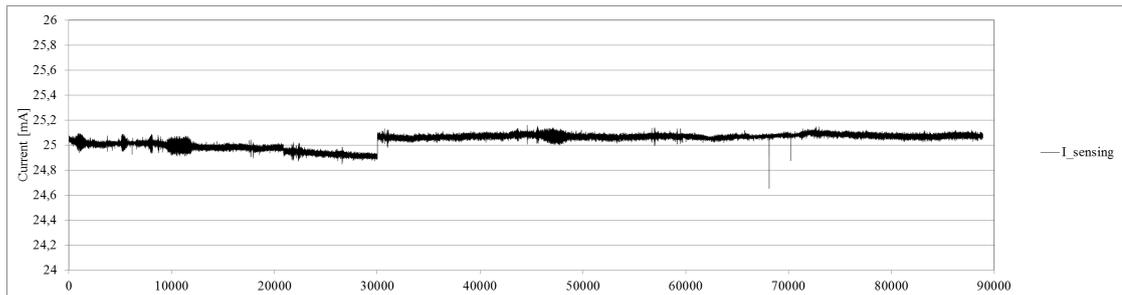
(b) Sensing current, TO6

Figure 6.12: Current measurements, TO6

Figure 6.12a shows the measured load current for the entire test of TO6. It can be seen how the load current was reduced from 75 A to 73.5 A to avoid $T_{vj,max}$ to get to high after 8430 cycles. The figure also clearly show when the diodes failed.

In Fig. 6.12b the sense current can be seen. Apart from a minor adjustment at N$\approx$ 30000, the sense current was very stable throughout the test, with variations of less than 0.1 mA. The sensitivity of the T_{vj} measurement towards changes in I_{sense} have been checked, and this adjustment did not affect the results.
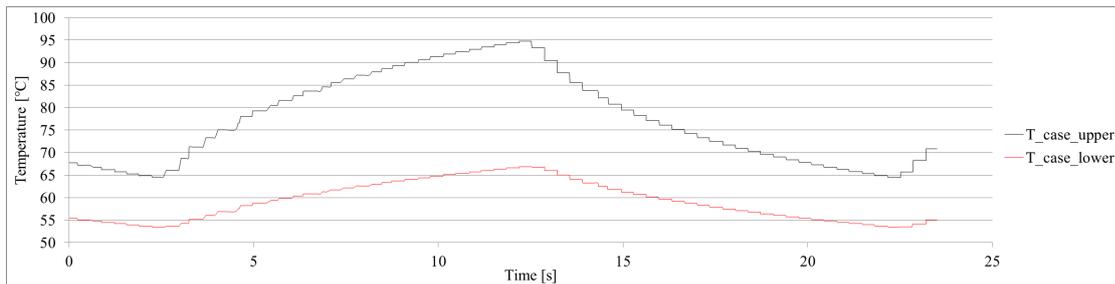
(a) Emitter and collector thermocouple measurement of one cycle, TO6
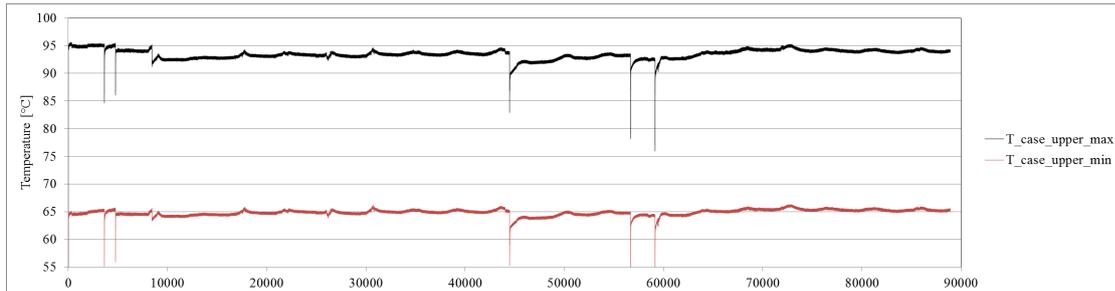
(b) Collector contact thermocouple measurement, TO6
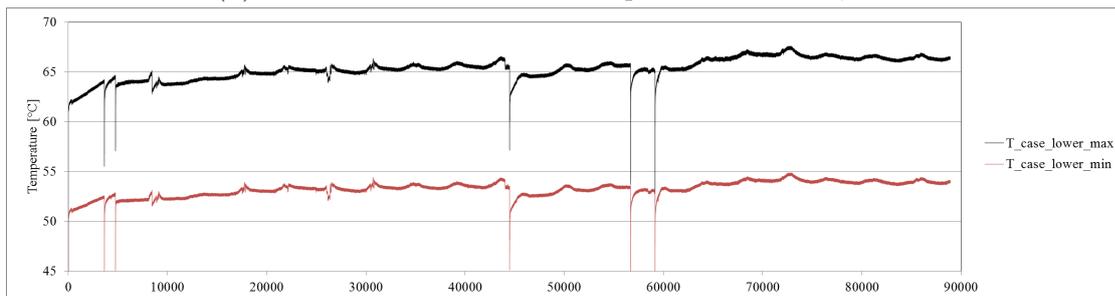
(c) Emitter contact thermocouple measurement, TO6

Figure 6.13: IGBT heat sink temperature, TO6

Figure 6.13a shows the temperature of the collector and the emitter contact measured by thermocouples inside the contacts. The figures show how the temperature in the collector contact is much higher than in the emitter contact. That implies that the thermal resistance between the junction of the chip, where the majority of the heat is produced, and the liquid cooled heat sink is lower on the collector side of the chip. This is mainly due to the design of the die-carrier and the emitter stamp in the clamp. Figure 6.13b and 6.13c show the maximum and minimum temperatures, the daily variations in room temperature is visible in both figures. The maximum temperature is measured at point c, and the minimum at point d in Fig. 6.2 on page 83.
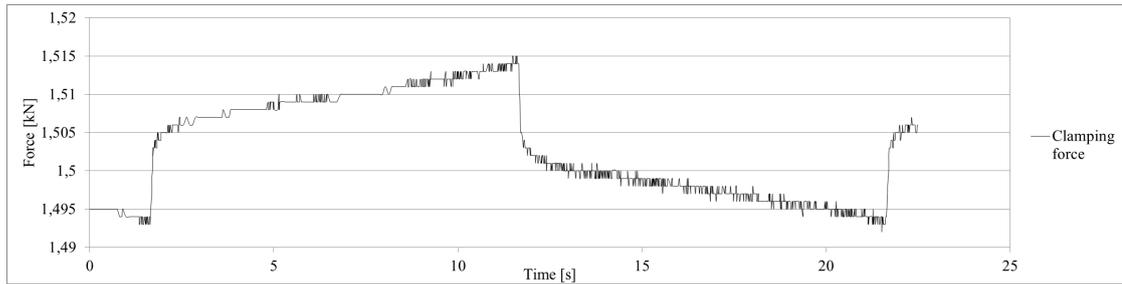
(a) Clamping force for one cycle, TO6
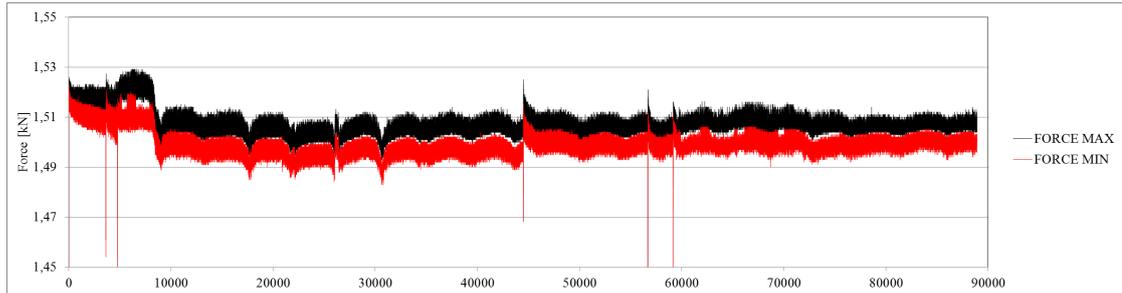
(b) Maximum and minimum clamping force, TO6

Figure 6.14: Clamping force measurements, TO6

The maximum and minimum clamping force measured with the pressure sensor
can be seen in Fig. 6.14b. The maximum force is measured at the same time as
$V_{ce,min}$, indicated by c in Fig. 6.2. The minimum force is measured at the same
time as $V_{ce,max}$ indicated by point d. The changes in clamping force for one cycle
can be seen in Fig. 6.14a, the variations is due to thermal expansion.

Microscopy Analysis of TO6

After the power cycling of test object 6 was completed, it was removed from the
clamp and sent to Chemnitz University of Technology for optical investigation.
The die-carrier was disassembled, and a microscopy analysis was conducted by
Lukas Tinschert. The report from the optical investigation is in appendix C.

6.6   TO8

To see if the long lifetime of TO6 was related to it being passively power cycled, TO8 was actively power cycled. Active power cycling, and the changes made to the electrical circuit, is described in chapter 5.3. Instead of keeping the IGBT test object constantly on, like in a passive test, the IGBT is used to switch the load current on and off.

The test started 29.04.2014 with passive power cycling for a few hundred cycles to enable use of the $V_{ce}(T)$-method to measure T_{vj}. Using the same load current as for the test of TO6, gave for TO8 a lower $T_{vj,max}$ and ΔT_{vj}. The reason is probably minor differences in R_{th} due to inaccuracies in the clamping process. Since the purpose of the test, was to see if passive power cycling had prolonged the lifetime of TO6; it was important that the stress level during the testing of TO8 was at least as high as during the testing of TO6. To achieve that, the load current was increased to 76.5 A. The cycle length was the same with $t_{on}=t_{off}=$ 10 s. After 300 cycles the run-in testing was completed. With $I_{load} =$76.597 A the virtual junction temperatures was measured to: $T_{vj,max} =$ 153.083 ℃, $T_{vj,max} =$ 63.456 ℃, ΔT_{vj} = 89.627 ℃. From previous testing, it was known that the temperatures would increase with increasing room temperature, so it was assumed that this operating point would give a sufficient stress level.

After completing 52450 cycles, the power cycling was stopped 10.05.2014. Before the test started it was decided that if the test object survived more than 50000 cycles, it could be concluded that the long power cycling lifetime of TO6 was not just because it had been passively power cycled.

6.6.1   Characterization Measurements of TO8

TO8 - Chip 23 from SINTEF 2000A PCT DUT8					
		Char A1.1	Char A1.2	Char A1.3	Char A1.4
Date	#Cycles	Vce, sat	Ic, block	Ige, leakage	Vge(th)
		Ic=70A	Vce = 156 V /144V	Vge = 20 V	Ice = 200 uA
28.04.2014	0	2.85 V	56 nA (Vce = 156 V)	immeasurable	5.58 V
19.05.2014	88907	2.878 V	58 nA (Vce = 144V)	immeasurable	5.73V

As can be seen from table 6.2, no significant changes was observed in any of the characterization parameters between the pre- and post-testing characterization. The electrical circuit used for the different characterization measurements was described in chapter 5.8.

TO8 - Chip 23 from SINTEF 2000A PCT DUT8							
		Char A1.5					
Date	#Cycles	Rge	Reg	Rce	Rec	Rce	Rec
				Vge = S.C.	Vge = S.C.	Vge = 14.02	Vge = 14.02
28.04.2014	0	Inf	Inf	Inf	204 kΩ	12.8 kΩ	41.3 kΩ
19.05.2014	88907	Inf	inf	32.3 kΩ	235.6 kΩ	14.26 kΩ	Inf

Table 6.2: Characterization measurements of TO8

The increase in R_{ce} measured when gate-emitter is short circuited, is not believed to be related to wear of the chip. Measurement error is a very possible explanation for that increase.

6.6.2   Log of Events from the Power Cycling of TO8

Figure 6.15 shows the warm-state collector-emitter saturation voltage ($V_{ce,sat\ warm}$) for the entire test of TO8. The figure is used to describe the test development.

As all the red lines in Fig. 6.15 indicates, the tester was temporarily stopped several times. Ideally a power cycle test should not be stopped until either failure, or completion of the desired number of cycles.
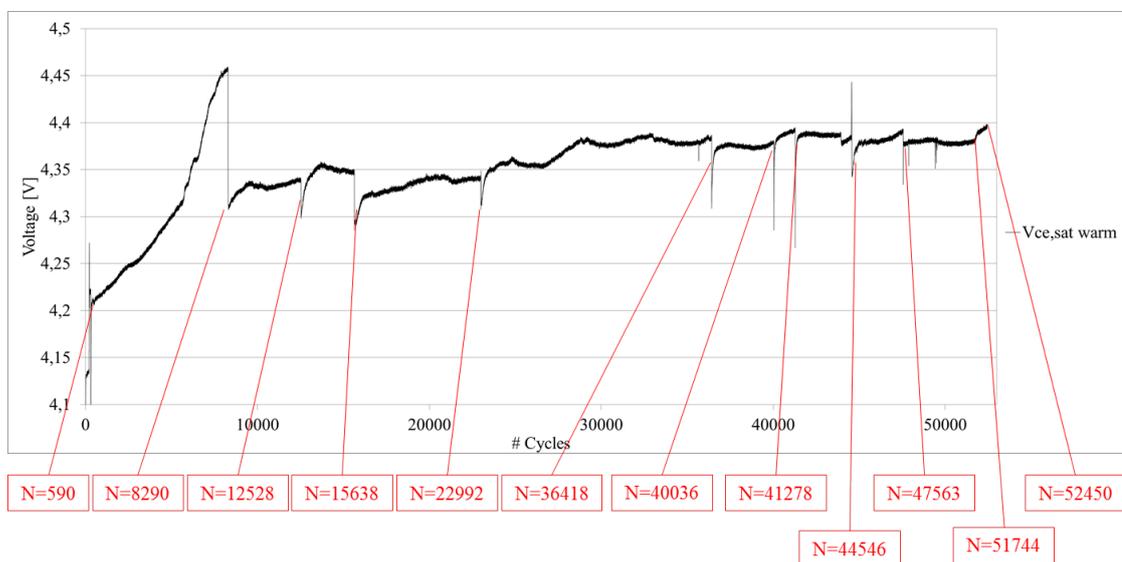
Figure 6.15: $V_{ce,sat\ warm}$ with cycle numbers for stops in testing, TO8

N=1, 29.04.2014 Power cycling of TO8 started. Started as a passive power cycle

test to enable measurement of $T_{vj,max}$.

N=300, 29.04.14 Passive power cycling stopped, and the test was restarted as an active power cycle test. With a load current of 76.6 A, the virtual junction temperatures measured before stopping (N=298) were: $T_{vj,max} = 153.083\,\text{°C}$, $T_{vj,max} = 63.456\,\text{°C}$, $\Delta T_{vj} = 89.627\,\text{°C}$.

N=5500, 30.04.14 Load current started to increase by itself. The load current adjustment is quite sensitive, and it is believed that the increase was caused by an error in the load current source. Figure 6.19 shows the increase in load current.

N=8290, 01.05.2014 When it was detected that the load current had increased, it was decreased from 78 A to 76.5 A.

N=12528, 02.05.2014 The labVIEW control program stopped unintentionally when screenshots for documentation was taken. Although the testing was restarted within a few minutes, the tester cooled down sufficiently to show a decrease in the $V_{ce,sat\ warm}$.

N=15638, 03.05.2014 Power cycling was stopped, it is not known what triggered it. It is suspected that a power outage in the building might have occurred since the laptop, which have virtually no battery, had rebooted shortly after the testing had stopped.

N=22992, 05.05.2014 Graphs showed that the voltage in the bypass leg was no longer stable, as can be seen in Fig. 6.18a and 6.18b. It was believed that it indicated that one or both of the diodes started to fail. The test was stopped at N=22992, both diodes was replaced, and the power cycling was resumed. Figure 6.18b and 6.18a show that the voltage was more stable after the diodes was replaced.

N=33000, 07.05.2014 Figure 6.18a and 6.18b show that the voltage in the bypass leg has a sudden drop at N=33000. This was because one of the bypass diodes failed and was short circuited. In Fig. 6.20b it can be seen that the temperature of the MOSFET and diode heat sink also decreases when one of the diodes is short circuited.

N=36418, 08.05.2014 The test was stopped to replace the failed diodes. Resistance measurements of the diode on the aluminium heat sink showed it was completly short circuited. The diode was replaced with a new one. The four MOSFETs in MOSFET 1 shown in Fig. 5.4 on page 47, was also replaced. Ideally all eight MOSFETs should have been replaced, but only 7 new MOSFETs were available.

N=40036, 09.05.2014 To measure T_{vj} and thereby ensuring a that the stress level was sufficiently high, the testing was stopped to change from passive to active power cycling.

N=41278, 09.05.2014 To change back to active power cycling, the test was stopped. Before stopping, with I_{load} =76.6 A the virtual junction temperatures were: $T_{vj,max} = 163.815$ ℃, $T_{vj,min} = 65.066$ ℃ and $\Delta T_{vj} = 98.749$ ℃. A resistance of $\approx 200\ \Omega$ was measured between one of the diode heat sinks and the air cooled common heat sink for the MOSFETs and diodes. The resistance should be immeasurable on a multimeter, and the silpad under the heat sink was replaced. It was considered possible that the unstable bypass leg voltage could be related to reduced resistance. The voltage was just as unstable after replacing the silpad.

N=43934, 10.05.2014 Figure 6.18a and 6.18b show sudden decrease in the voltage of the bypass leg at N=43934, indicating a short circuited bypass diode. A corresponding drop in the temperature of the MOSFET and diode heat sink can be seen in Fig. 6.20b.

N=44546, 10.05.2014 The voltage drop indicating short circuit of one of the diodes was detected, and the test was stopped to replace it. More MOSFETs and diodes had been ordered, and arrived 12.05.2014. Since the cause of the instability of the bypass leg voltage had not been found, all the semiconductor components in the bypass leg was removed and replaced, as Fig. 6.16a and 6.16b show. The replacement components were not the same type as the old ones, and a slightly lower voltage in the bypass leg was observed. In Fig. 6.18a and 6.18b it can be seen that the voltage in the bypass leg was stable after the all semiconductor components was replaced. That rules out the possibility that the cause of the unstable bypass voltage was failure of the IGBT test object.

(a) Bypass components removed   (b) New bypass components installed

Figure 6.16: Replacing bypass components

N=47563, 13.05.2014 The load current was manually decreased from 76.7 A to 76.5 A.

N=51744, 14.05.2014 To measure T_{vj} before completing the test of TO8, the power cycling was stopped and switched to passive power cycling.

N=52450, 14.05.2014 The power cycle test of TO8 was permanently stopped. Before stopping, with I_{load} =76.6 A the virtual junction temperatures were: $T_{vj,max} = 164.201$℃, $T_{vj,min} = 64.816$ ℃and $\Delta T_{vj} = 99.385$ ℃.

6.6.3   Measurements from the Power Cycling of TO8

Figure 6.17 to 6.23 show how some of the measured parameters changes during the power cycling of TO8.
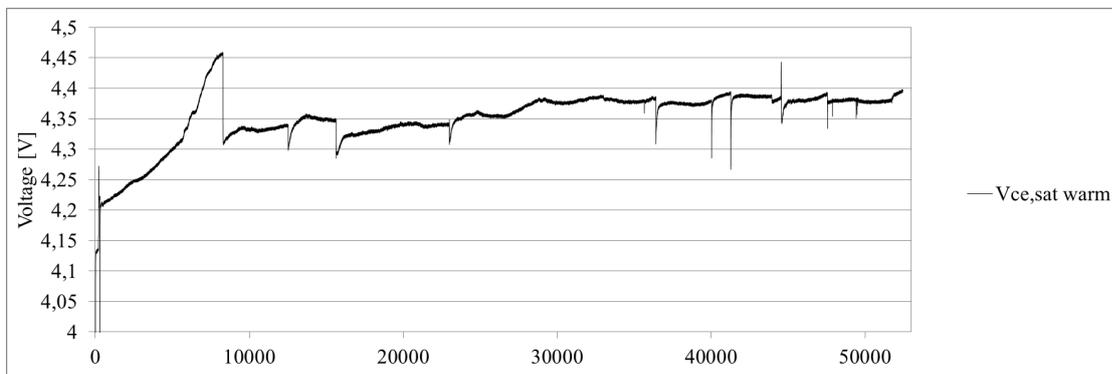
(a) $V_{ce,sat\ warm}$, TO8
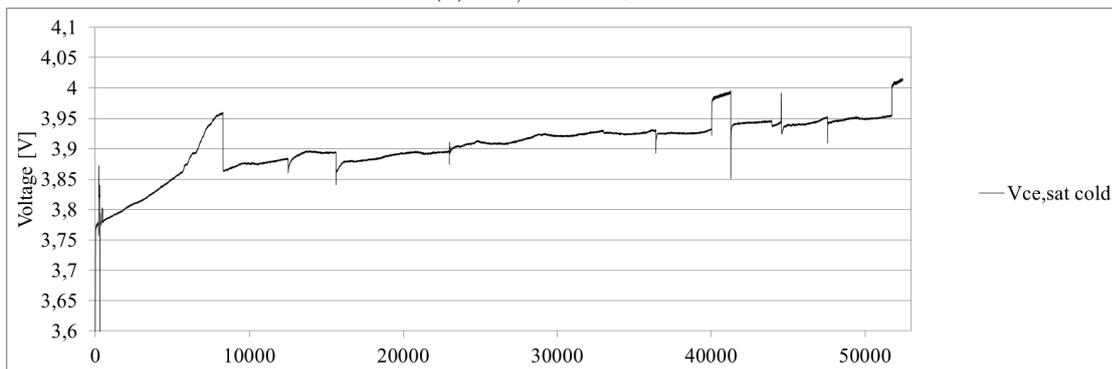
(b) $V_{ce,sat\ cold}$, TO8

Figure 6.17: Maximum and minimum collector-emitter saturation voltage, TO8

Figure 6.17a and Fig. 6.17b show the development of $V_{ce,sat\ warm}$ and $V_{ce,sat\ cold}$

during the power cycling of TO8. These parameters are measured at the beginning and the end of each heating phase, as indicated by point a and b in Fig. 6.2. An increase in both $V_{ce,sat\ warm}$ and $V_{ce,sat\ cold}$ can be seen during the increase in current between N=5500 and N=8290. Figure 6.17b shows an increase in $V_{ce,sat\ cold}$ between N=40036 and N=41278 and between N=51744 and N=52450, when TO8 was passively power cycled. It is not known why the passive power cycling led to a higher $V_{ce,sat\ cold}$.
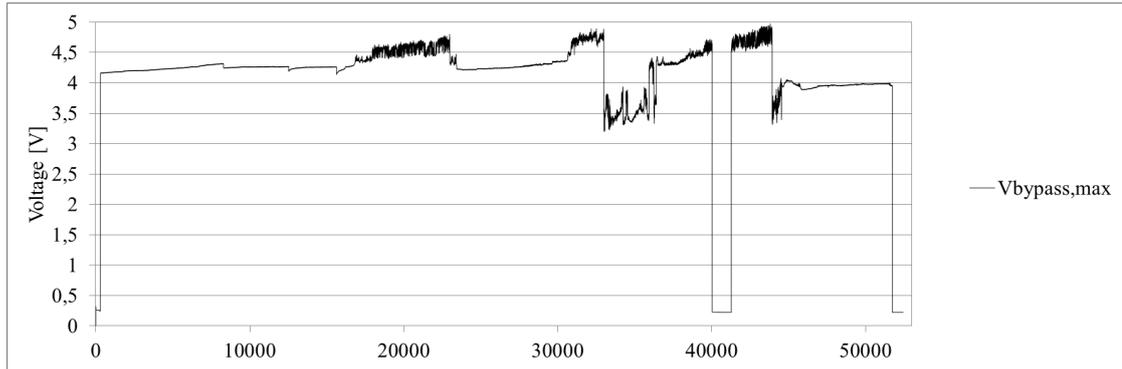
(a) $V_{bypass,max}$, TO8
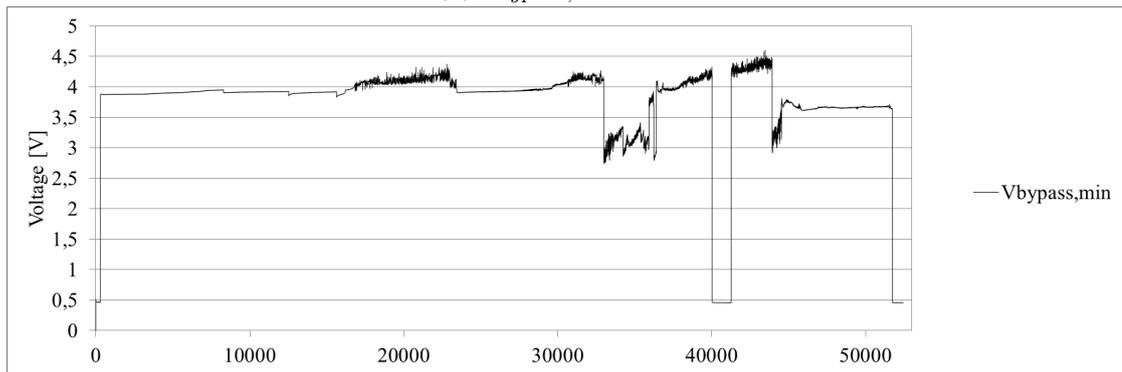
(b) $V_{bypass,min}$, TO8

Figure 6.18: Maximum and minimum bypass leg voltage, TO8

In figure 6.18a and Fig. 6.18b the maximum and minimum voltage of the bypass leg, $V_{bypass,max}$ and $V_{bypass,min}$, can be seen. Measurement of V_{bypass} is only possible in active power cycling mode, since it is performed with the voltage probes at the collector and emitter of the test object. The simplified electrical circuit diagram for active power cycling is shown in Fig. 5.7. It shows that when MOSFET 2 is turned on and the test object is turned off, V_{ce} is the voltage of the series connection of MOSFET 2, MOSFET 1 and the two diodes. Since no current flows through MOSFET 2, there is no voltage drop over it. The measured V_{ce} is therefore

the voltage drop of the series connection of MOSFET 1 and the diodes. The large variations in voltage in Fig. 6.18a and Fig. 6.18b, indicates that the semiconductor components in the bypass leg have been exposed to a very high stress level. As explained in the log of events for TO8, the MOSFETs and the diodes was replaced several times. TO8 was passively power cycled from N=0 to N=300, N=40036 to N=41278 and N=51744 to N=52450. The voltage seen in Fig. 6.18a and Fig. 6.18b for these periods is therefore the voltage drop of the sense current, used for T_{vj} estiamtion.
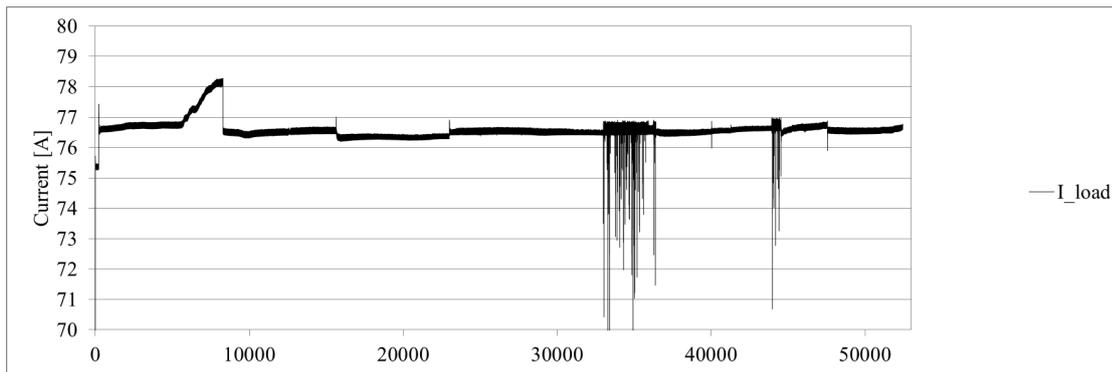
Figure 6.19: Load current, TO8

The load current can be seen in Fig. 6.19. Between N=5500 and N=8290 the increase described in the log of events can be seen. The figure also show how the load current appears to be unstable when one of the diodes is short circuited (N=33000 to N=36418 and N=43934 to N=44546). As for the power cycling of TO6 this is due to the unfortunate choice of measuring point, a further explanation was given in chapter 5.12.2.
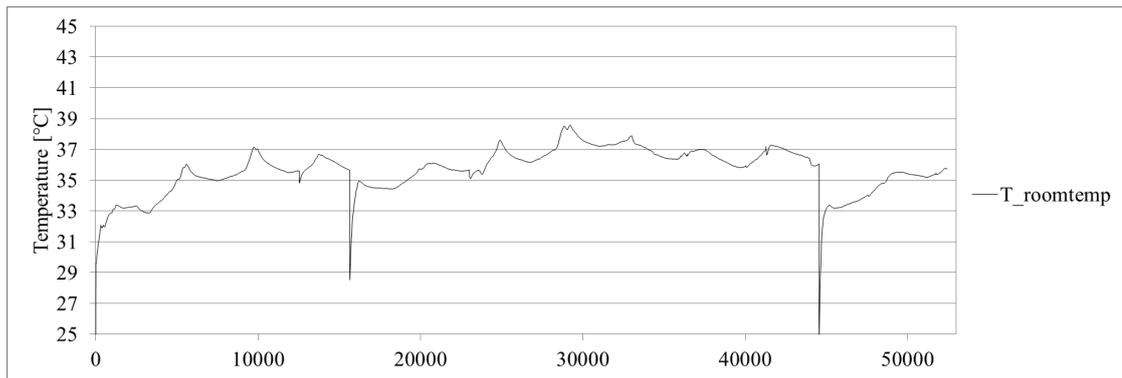
(a) Room temperature, TO8
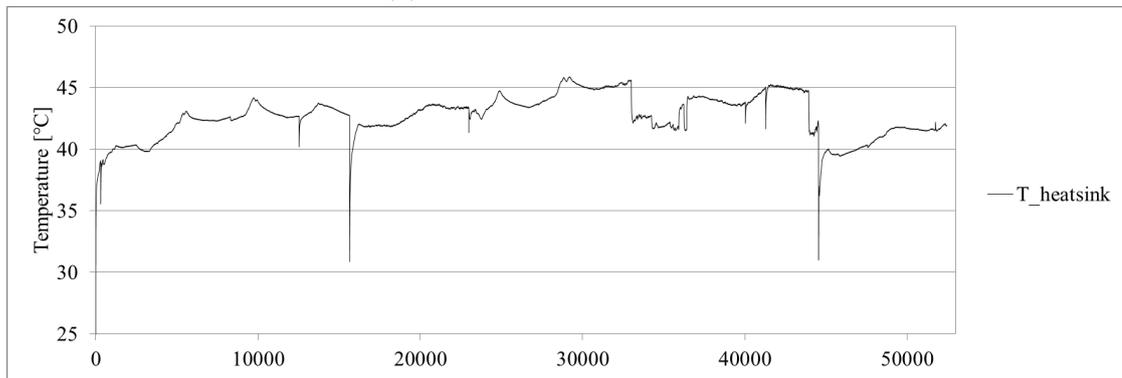
(b) MOSFET and diode heat sink temperature, TO8

Figure 6.20: Temperature measurements, TO8

Figure 6.20a and Fig. 6.20b shows the development of the room temperature and the diode and MOSFET heat sink temperature for the power cycle test of TO8.
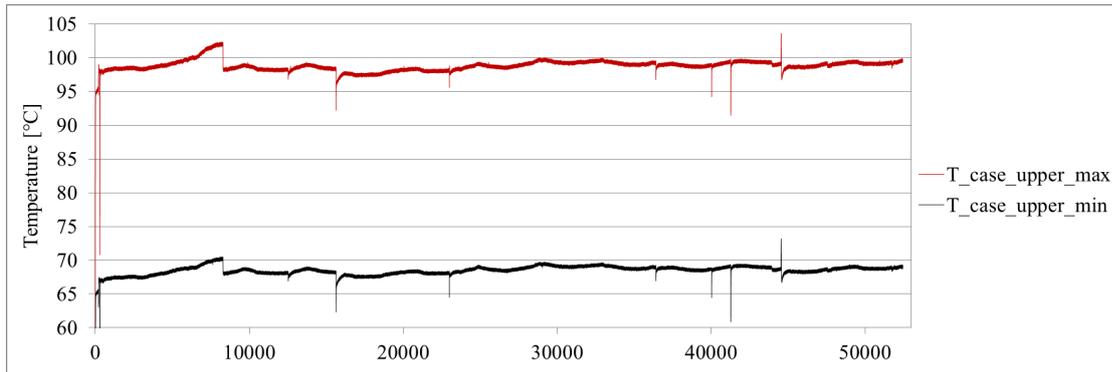
(a) Collector contact thermocouple measurement, TO8
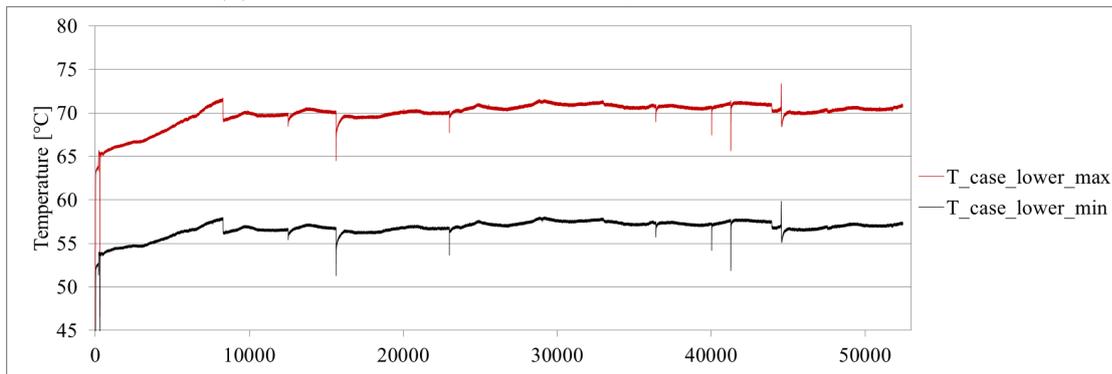
(b) Emitter contact thermocouple measurement, TO8

Figure 6.21: IGBT heat sink temperatures, TO8

The maximum and minimum temperatures of the of the collector and emitter contacts, can be seen in Fig. 6.21b and Fig. 6.21b. As for the testing of TO6, it can be seen that the temperatures is much higher in the collector contact.
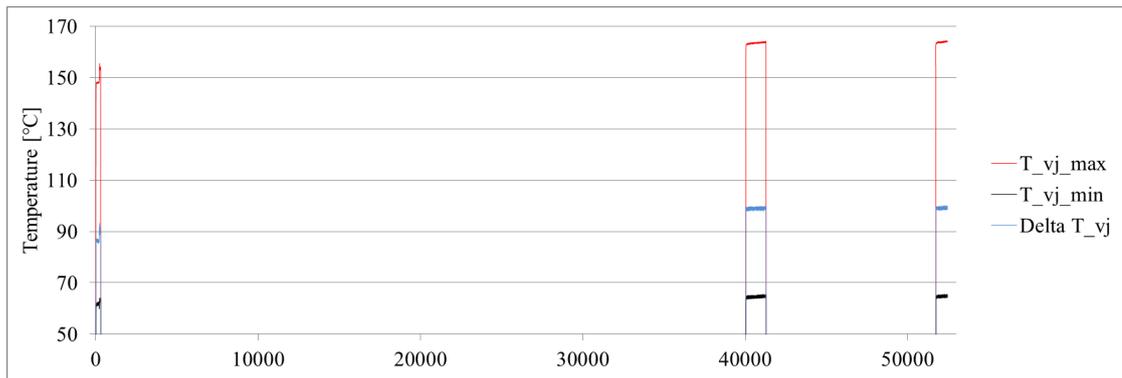
Figure 6.22: Virtual junction temperature, TO8

Figure 6.22 shows T_{vj} measurements during the power cycling of TO8. Since T_{vj} cannot be measured during active power cycling, it is only in the periods with passive power cycling a T_{vj} measurement could be performed.
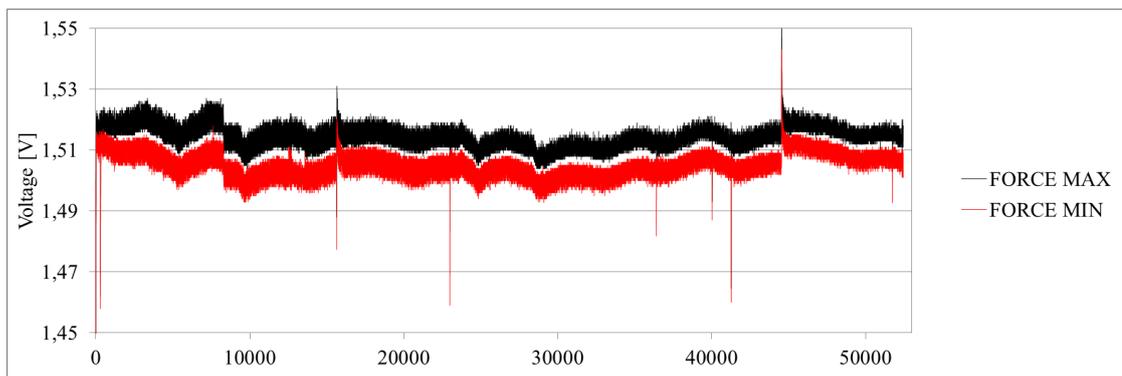
Figure 6.23: Maximum and minimum clamping force, TO8

The maximum and minimum clamping force measured with the pressure sensor during the power cycling of TO8, can be seen in Fig. 6.23.

Chapter 7

Discussion

7.1 Power Cycling Procedure

In several ways, both of the performed power cycling tests could be considered as a run-in-test of the single chip power cycle tester. Firstly, there were several temporary stops during both tests. Ideally the test should have run continuously from start to stop. A continuous test would have produced results with less noise, making them easier to interpret. More importantly, in a continuous test the stress level could be described more accurately, strengthening any conclusions made regarding power cycling lifetime of the test objects. Secondly, large variations in the room-temperature made it challenging to find a stable operating-point. A large temperature increase with a long time constant, lead to considerable change in the test conditions for the first few thousand cycles.

As described in chapter 5.10, measurements with pressure sensitive FUJI-paper revealed that the electrical contacts to the clamp affects the pressure distribution on the collector side of the chip. This was found to have a large effect on the thermal resistance. This corresponds well with the description of the pressure dependency of the thermal contact conductance, given on page 19 in chapter 2.4.1. There it is described how the thermal contact conductance is more dependant on the magnitude of the clamping force, than the electrical contact conductance. Improvements were made to the contacts, but it is likely that changes in the pressure distribution occurring each time the clamp is reassembled is still affecting the results. It is mentioned here to highlight a weakness of the single chip tester. The pressure distribution sensitivity of chips tested in the single chip tester, does however indicate how changes in the pressure distribution inside a press-pack will create unequal conditions for the different chips.

As described in the previous chapter, and discussed in the next sections; an increase in $V_{ce,sat}$ was observed for both of the tested chips. A possible explanation for parts of this increase is oxidation of the chip surface. The chips were tested in air, in contrast to a press-pack where oxidation is prevented by the presence of an inert gas. The high temperature during testing is accelerating the oxidation process. The microscopy analysis of TO6 indicated that considerable oxidation of the chip surface had occurred. An oxidation layer will increase the resistance of a chip, and under constant current that implies an increase in the voltage. The gradual increase in $V_{ce,sat}$ for both tests, corresponds well to this theory. Even if the increase in $V_{ce,sat}$ is not related to oxidation, it is considered important to emphasize that the chips are tested in an environment different from what they are designed for.

Another factor relating to the stress level of the chips during the power cycle testing, is the uncertainty of the $V_{ce}(T)$-method used for estimating T_{vj}. This was discussed in chapter 2.5.1, and is related to the fact that the $V_{ce}(T)$-method estimates a current-weighted average temperature of the chip, while due to considerable lateral temperature gradients the actual maximum temperature of regions of the chip surface might be higher. In addition, due to the very steep temperature decrease when the cooling starts, the estimated $T_{vj,max}$ is lower than the actual maximum temperature of the chips during a cycle. Based on these two limitations in $V_{ce}(T)$-method, it is suggested that the thermal stress level given by $T_{vj,max}$ and ΔT_{vj} can be regarded as a minimum value.

Since testing stopped before either of the chips failed, their power cycling lifetime cannot be determined. Statistical analysis is required to perform lifetime predictions. Considerably more experimental data than the results from two run-in-tests is required to do so.

7.2   Power Cycling Test of TO6

As seen in table 6.1, no significant changes were observed in any of the parameters between the pre- and post-testing electrical characterization. Therefore based on those measurements TO6 was still fully functional as an IGBT after completing 88900 power cycles with a $\Delta T_{vj} \approx 100$ ℃.

Failure-limits for $V_{ce,sat}$ during power cycle testing was described in chapter 3.4.2. It was mentioned that for module testing, a device is considered failed if, depending of the manufacturer, an increase in $V_{ce,sat}$ of 5 % to 20 % is observed. Since the current was reduced at N=8340, the initial value of $V_{ce,sat\ warm}$ is considered to be 4.1 V, which was the $V_{ce,sat\ warm}$ value shortly after the current adjustment.

Initially a failure-limit of 5 % increase in $V_{ce,sat\ warm}$ was used, that limit was exceeded after 56674 cycles. No failure criteria for increase in $V_{ce,sat}$ for power cycling of press-pack IGBTs have been found in IEC standards. In collaboration with SINTEF, it was therefore decided that a more appropriate limit is 10 % increase in $V_{ce,sat\ warm}$. That was partly because some of the increase in $V_{ce,sat\ warm}$ could be explained by the increase in room temperature. The 10 % increase-limit of 4.5 V was not exceeded for the remainder of the test.

Between $N \approx 63000$ and $N \approx 73000$, $V_{ce,sat\ warm}$ was unstable as was seen in Fig. 6.8b on page 90. The reason for this instability is not known. One possibility is that it is related to a contact resistance between the collector and emitter voltage-measurement-points that was not properly established before $N \approx 73000$. This hypothesis cannot by proved, but several factors indicates that it is a possibility. Firstly, it can be seen in Fig. 6.8b that after 73000 cycles, $V_{ce,sat\ warm}$ decreases before it is stabilized. Secondly, in the power cycle test of TO8, which was performed after the test of TO6, $V_{ce,sat\ warm}$ was considerably more stable. Further, the instability between $N \approx 63000$ and $N \approx 73000$ can only be seen in $V_{ce,sat\ warm}$, while the behaviour of $V_{ce,sat\ cold}$ is similar to what is seen for the rest of the test. Finally, throughout the test, all temperature changes, both thermocouple (Fig. 6.13b and 6.13c) and T_{vj} (Fig. 6.10) measurements, corresponds to changes in both $V_{ce,sat\ warm}$ and $V_{ce,sat\ cold}$. The change in $V_{ce,sat\ warm}$ between $N \approx 63000$ and $N \approx 73000$ is however not reflected in neither of the temperature measurements. Based on these factors it is suggested that the increase and instability in $V_{ce,sat\ warm}$ seen between $N \approx 63000$ and $N \approx 73000$, is not due to changes in IGBT chip.

In the SINTEF 2000 A tester, a permanent step in both $V_{ce,sat\ warm}$ and $V_{ce,sat\ cold}$ was observed when the DUTs failed. It is therefore assumed that even if the observed change in $V_{ce,sat\ warm}$ for TO6 is due to changes in the test object, it is not the same type of failure that was observed in the DUTs in the 2000 A tester.

After the testing of TO6, an optical analysis was performed by Lukas Tinschert at Chemnitz University of Technology (TUC). The report from this analysis can be seen in appendix C. When discussing the results from the optical analysis of TO6, it is emphasized that the chip was first power cycled inside a press-pack disc in the SINTEF 2000 A PCT before it was removed from the device and power cycled in the single chip tester. It can therefore not be determined whether it was the testing in the single-chip tester, or in the 2000 A tester which caused the observed wear on the chip.

According to the team at TUC who analysed the pictures of TO6, the pictures show that the chip has been exposed to considerable mechanical wear and visually

appears to be destroyed. When microscopy pictures of TO6 is compared to those of other chips that were power cycled in the 2000 A tester, the wear seen on TO6 is considerably worse. Wear close to guard rings and chip passivation was seen in the pictures. A gentle blocking test of a few hundred volts, did however indicate that the forward blocking capability of the chip is intact.

The electrical characterization measurements and the optical analysis, gave diverging conclusions. One suggests that the chip survived the test without signs of damage, while the other revealed that the chip had been exposed significant mechanical wear. That means that any strong conclusions on the power cycling lifetime of the TO6 should not be made.

7.3   Power Cycling Test of TO8

As for TO6, no significant changes were observed between pre- and post-testing characterization of TO8, suggesting that the device passed the test.

The load current was gradually increased to from 76.5 A to 78 A between $N \approx 5000$ and N = 8290 (Fig. 6.19), due to problems with the current source. A large increase in both $V_{ce,sat\ warm}$ and $V_{ce,sat\ cold}$ were observed in that period. Ideally the test should have been terminated, and a new test with a new test object started. Due to limited time available, the current was reduced and the testing resumed. The test object received an increased stress during this period. The purpose of the test was to expose TO8 to at least as high stress as during the test of TO6, and see if it survived for at least 50000 cycles. Therefore it can be justified that the test was continued, although it was not according to proper power cycle testing procedure.

The power cycling test of TO8 is considered successful. It showed that although a test object was actively power cycled, it was based on the electrical characterization measurements unaffected by the test.

Chapter 8

Conclusion and Further Work

8.1 Conclusion

The work in this thesis has been supported by SINTEF Energy Research through the project Power Electronics for Reliable and Energy Efficient Renewable Energy Systems. Results from power cycle testing of high-power press-pack IGBTs in the SINTEF 2000 A power cycle tester (PCT) conducted in that project, showed that the press-pack discs had an unexpectedly short power cycling lifetime. Post testing examination of the failed press-pack discs revealed that it was caused by the failure of only one or two of the 28 paralleled IGBT chips. Further, it was found that all the failed chips had similar relative position inside the press-pack. The failures are believed to be related to changes in the internal pressure distribution, caused by deformation of the press-pack housing when it is heated. This failure hypothesis is supported by FEM simulations performed at the Chemnitz University of Technology.

To further investigate this hypothesis, this master thesis has developed a test equipment for power cycling individual IGBT chips removed from press-pack discs. After an initial run-in-phase, two chips were power cycled for a considerable number of cycles under tough conditions, with $T_{vj,max} \approx 160$ ℃ and $\Delta T_{vj} \approx 100$ ℃. One chip was passively power cycled for 88900 cycles, while another chip was actively power cycled for 52450 cycles. Based on comparison of electrical characterization measurements before and after the tests, both tested chips are considered to have survived the power cycling. A gradual increase in $V_{ce,sat\ warm}$ was observed for both chips. Based on the size of the increase, it is suggested that considerable wear of the chips can be assumed; but since the change is gradual and not stepwise as it was in the 2000 A PCT, the chips are not considered failed because of the increase

in $V_{ce,sat\ warm}$. A microscopy analysis of one of the tested chips showed that it had been exposed to considerable mechanical stress, and judged by the pictures the chip appeared to be destroyed. A limitation in the optical analysis is the fact that the tested chips were removed from a press-pack that was power cycled in the SINTEF 2000 A tester. It is therefore not known when the observed wear on the chip was inflicted. As neither of the chips were tested until failure, the power cycling lifetime of the press-pack chips cannot be determined. Even if they were tested until failure, two tests give insufficient data to perform any statistical analysis, which is necessary if the lifetime of a component is to be determined.

The results from power cycling individual press-pack chips supports the hypothesis that the early failure of press-pack discs is caused by excessive stress on chips in certain locations. The fact that the lifetime of the individual chips was found to be 10 - 50 times longer than that of press-pack discs tested under similar stress, justifies this conclusion even though several factors abates the quality of the results from the single chip tester.

8.2   Further Work

To further investigate the validity of the SINTEFs failure hypothesis, power cycle testing of more press-pack IGBT chips is necessary. More testing is also necessary to provide data for a statistical analysis of power cycling lifetime.

The FEM simulations on the changes in pressure distribution when a clamped press-pack is heated showed that the clamping force on the chips in the outer corners is greatly reduced. It is the same chips that failed in the testing in the 2000 A tester. Testing of chips with reduced clamping force should therefore be performed to investigate what effect it has on the power cycling lifetime of a chip.

Testing of new chips should be performed. The test objects used in this thesis are removed from press-packs that were tested in the SINTEF 2000 A tester. By testing new chips, the results from a microscopy analysis can be used to investigate what type of mechanical, wear power cycling in the single-chip tester inflicts on a chip.

By including a test of the switching characteristics to the pre- and post-testing electrical characterization, it is possible that more information on how chips are affected by power cycle testing could be obtained.

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Appendix A

Safety Assessment

NTNU		utarbeidet av HMS-avd.	Nummer HMSRV2603	Dato 4.3.2010
HMS/KS		godkjent av Rektor	side 1 av 4	Erstatter 9.2.2010

Risikovurdering

Dato: 27.02.2014

Enhet: Institutt for elkraftteknikk
Linjeleder: Professor Erling Ilstad
Deltakere ved risikovurderingen (m/ funksjon):
Øyvind Bjerke Frank, Student
Atle Rygg Årdal, veileder SINTEF

Generelt:
Testen skal kjøres døgnkontinuerlig uten tilsyn over en lengre periode.

ID nr	Aktivitet og rom/sted	Mulig uønsket hendelse/belastning	Vurdering av sannsyn-lighet (1-5)	Vurdering av konsekvens:				Risiko-verdi	Kommentarer/status Forslag til tiltak
				Menneske (A-E)	Ytre miljø (A-E)	Øk/ materiell (A-E)	Om-dømme (A-E)		
	IGBT Power Cycling ELBYGGET / F167	Uforutsette hendelser som fører til feil på utstyr	4	A	A	B	A	A4	Innføre en oppstartsperiode der forsøk kun foregår på dagtid med kontinuerlig tilsyn.
	IGBT Power Cycling ELBYGGET / F167	Feil forårsaket av labVIEW kontrollprogram	4	A	A	B	A	A4	Software watchdog er implementert, for å kontrollere om PC eller labVIEW fungerer. Hardware watchdog er implementert for å kontrollere at FPGA enhet fungerer.
	IGBT Power Cycling ELBYGGET / F167	Berøring av spenningsførende deler	5	A	-	-	A	A5	Maks kontinuerlig spenning er kun 30V DC. Overspenninger kan oppstå.
	IGBT Power Cycling ELBYGGET / F167	Væskekjøler stopper å fungere	3	A	A	A	A	A3	Temperaturen vil øke, programmet vil skru av strømkilden og deretter avsluttes
	IGBT Power Cycling ELBYGGET / F167	Lekkasje i kjølekrets	3	A	A	A	A	A3	Oppsamlingskar vil samle opp oljen, væskesensor vil detektere lekkasje og strømmen vil kobles fra.

NTNU		Risikovurdering		utarbeidet av	HMS-avd.	Nummer	HMSRV2603	Dato	4.3.2010
HMS/KS				godkjent av	Rektor	side	2 av 4	Erstatter	9.2.2010

							Tiltak
IGBT Power Cycling ELBYGGET / F167	Lekkasje av olje under kalibrering. Oljen er på det varmeste 140°C.	3	C	-	B	C3	Holde avstand fra utstyr. Trykk inn UT-knapp om noe oppstår slik at væskekjøleren kobles fra. Væsketrykk er lavt. Alltid to personer tilstede når oljen er over 100°C.
IGBT Power Cycling ELBYGGET / F167	Feil som fører til varmeutvikling	4	A	-	A	A4	Kontrollprogram skal koble ut strømkilden hvis den målte temperaturen blir for høy. Hvis røykutvikling oppstår, vil en røykvarsler plassert over lab oppsettet utløses og strømkilden kobles ut.

Sannsynlighet
1. Svært liten
2. Liten
3. Middels
4. Stor
5. Svært stor

Konsekvens
A. Svært liten
B. Liten
C. Moderat
D. Alvorlig
E. Svært alvorlig

Risikoverdi (beregnes hver for seg):
Menneske = Sannsynlighet x Konsekvens Menneske
Ytre miljø = Sannsynlighet x Konsekvens Ytre miljø
Økonomi/materiell = Sannsynlighet x Konsekvens Øk/matriell
Omdømme = Sannsynlighet x Konsekvens Omdømme

NTNU			utarbeidet av	HMS-avd.	Nummer	HMSRV2603	Dato	4.3.2010
HMS/KS		Risikovurdering	godkjent av	Rektor	side	3 av 4	Erstatter	9.2.2010

Sannsynlighet vurderes etter følgende kriterier:

Svært liten 1	Liten 2	Middels 3	Stor 4	Svært stor 5
1 gang pr 50 år eller sjeldnere	1 gang pr 10 år eller sjeldnere	1 gang pr år eller sjeldnere	1 gang pr måned eller oftere	Skjer ukentlig

Konsekvens vurderes etter følgende kriterier:

Gradering	Menneske	Ytre miljø Vann, jord og luft	Øk/materiell	Omdømme
E Svært Alvorlig	Død	Svært langvarig og ikke reversibel skade	Drifts- eller aktivitetsstans >1 år.	Troverdighet og respekt betydelig og varig svekket
D Alvorlig	Alvorlig personskade. Mulig uførhet.	Langvarig skade. Lang restitusjonstid	Driftsstans > ½ år Aktivitetsstans i opp til 1 år	Troverdighet og respekt betydelig svekket
C Moderat	Alvorlig personskade.	Mindre skade og lang restitusjonstid	Drifts- eller aktivitetsstans < 1 mnd	Troverdighet og respekt svekket
B Liten	Skade som krever medisinsk behandling	Mindre skade og kort restitusjonstid	Drifts- eller aktivitetsstans < 1uke	Negativ påvirkning på troverdighet og respekt
A Svært liten	Skade som krever førstehjelp	Ubetydelig skade og kort restitusjonstid	Drifts- eller aktivitetsstans < 1dag	Liten påvirkning på troverdighet og respekt

Risikoverdi = Sannsynlighet x Konsekvens
Beregn risikoverdi for Menneske. Enheten vurderer selv om de i tillegg vil beregne risikoverdi for Ytre miljø, Økonomi/materiell og Omdømme. I så fall beregnes disse hver for seg.

Til kolonnen "Kommentarer/status, forslag til forebyggende og korrigerende tiltak":
Tiltak kan påvirke både sannsynlighet og konsekvens. Prioriter tiltak som kan forhindre at hendelsen inntreffer, dvs. sannsynlighetsreduserende tiltak foran skjerpet beredskap, dvs. konsekvensreduserende tiltak.

NTNU			utarbeidet av	Nummer	Dato
HMS/KS		Risikovurdering	HMS-avd.	HMSRV2603	4.3.2010
			godkjent av	side	Erstatter
			Rektor	4 av 4	9.2.2010

MATRISE FOR RISIKOVURDERINGER ved NTNU

KONSEKVENS						
Svært alvorlig	E1	E2	E3	E4	E5	
Alvorlig	D1	D2	D3	D4	D5	
Moderat	C1	C2	C3	C4	C5	
Liten	B1	B2	B3	B4	B5	
Svært liten	A1	A2	A3	A4	A5	
	Svært liten	Liten	Middels	Stor	Svært stor	
			SANNSYNLIGHET			

Prinsipp over akseptkriterium. Forklaring av fargene som er brukt i risikomatrisen.

Farge	Beskrivelse
Rød	Uakseptabel risiko. Tiltak skal gjennomføres for å redusere risikoen.
Gul	Vurderingsområde. Tiltak skal vurderes.
Grønn	Akseptabel risiko. Tiltak kan vurderes ut fra andre hensyn.

Appendix B

Circuit Diagram of the Safe Shutdown Card

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13.01.2014 09:23:06 f=1.02 C:\Users\oyvindb\Documents\eagle\HÆLVETE\Skjema sikkerhetskort.sch (Sheet: 1/1)
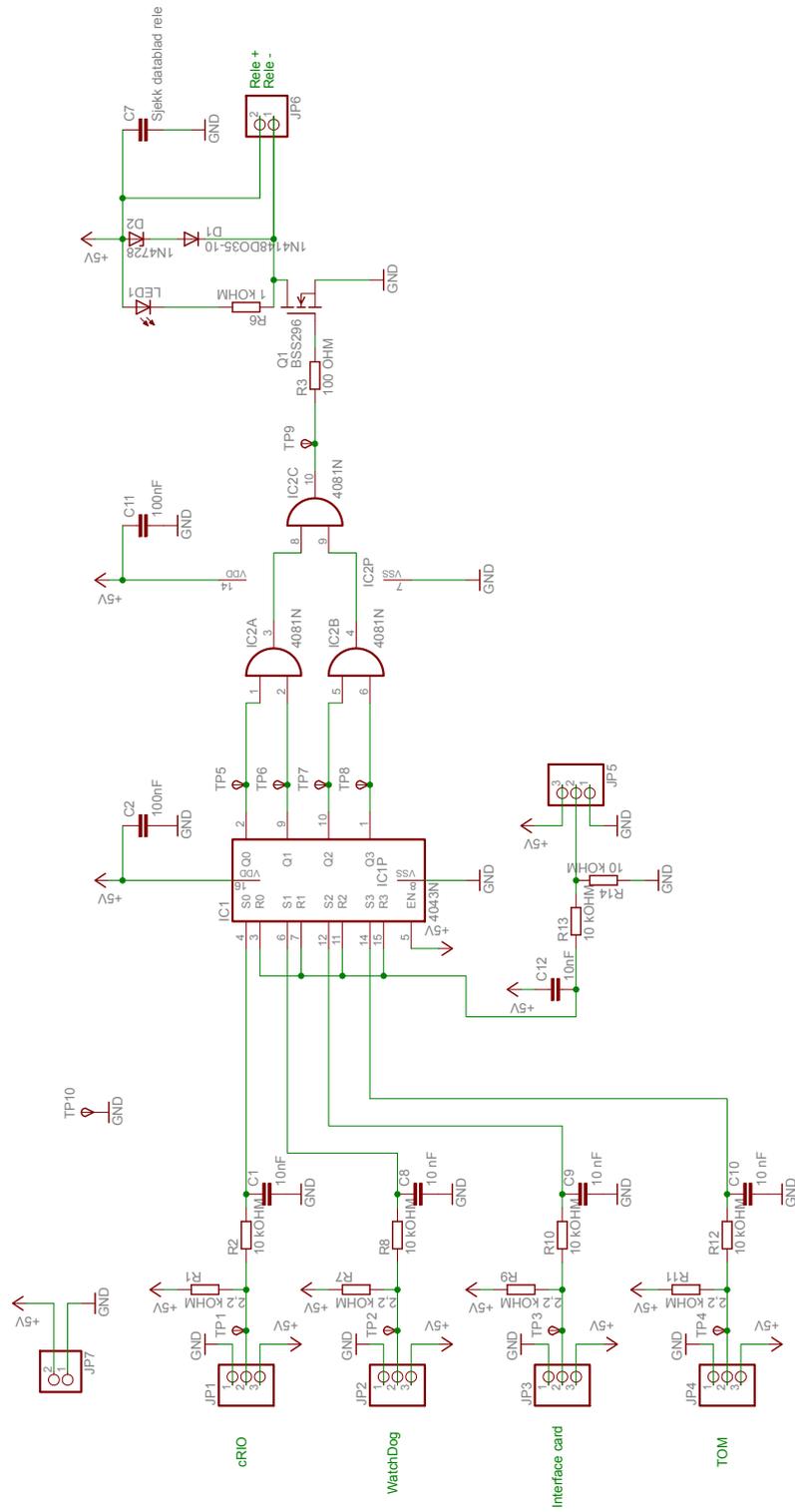
Appendix C

Microscopy Analysis TO6

After the power cycling of test object 6 was completed it was removed from the clamp, and sent to Chemnitz University of Technology for optical investigation. The die carrier was disassembled, and a microscopy analysis was conducted by Lukas Tinschert. The report is form the optical investigation is found in this appendix.

TECHNISCHE UNIVERSITÄT
CHEMNITZ

Fakultät für Elektrotechnik und Informationstechnik
Professur Leistungselektronik und elektromagnetische Verträglichkeit

TU Chemnitz • D-09107 Chemnitz

Date   2014-05-09
Failure Analysis Report No: 2/2014

Failure Analysis Report

1. Order

1.1 Costumer   SINTEF Energy AS
1.2 Manufacturer
1.3 Part ID No
1.4 Quantity   1
1.5 Part Codes
1.6 Label
1.8 Mode of failure

2. Appearance check result

The cassette 30 from DUT8 (part code: 321400-13-GB45G) was tested by SINTEF, characterized electrical and sent to Chemnitz University of Technology for further optical investigation.

Fig. 1: Cassette before disassembly

The molybdenum on the collector side and the IGBT were lopsided inside the cassette as it can be seen in Fig. 1. The gap between chip and cassette on the left side is much wider than on the right side.
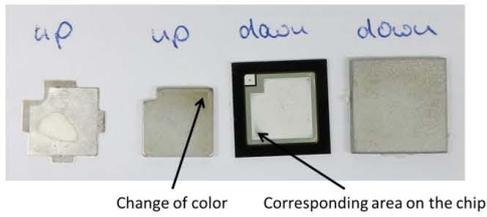
Fig. 2: Disassembled cassette
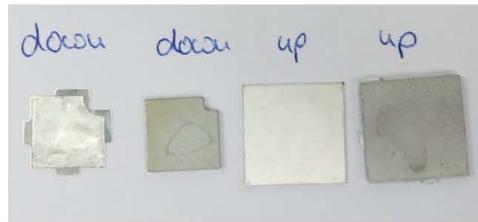
Fig. 3: Other side of disassembled parts

Fig. 4: Detail of mark between silver and molybdenum

Inside the cassette no ablation has been found. However an area with changed color on the molybdenum towards the IGBT was discovered (marked in Fig. 2) as well as a corresponding mark on the silver and the molybdenum (Fig. 4).

3. Microscopy

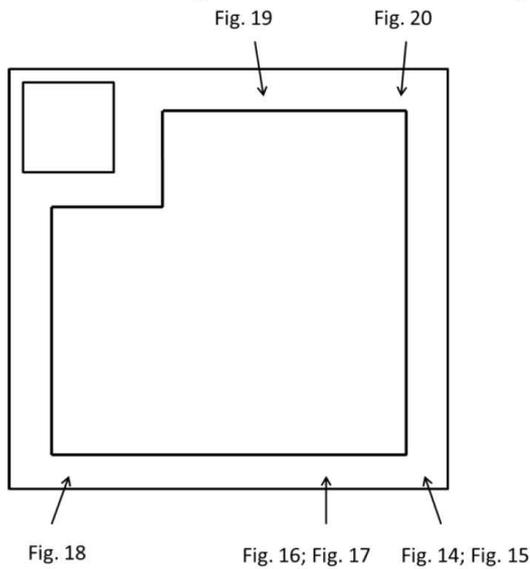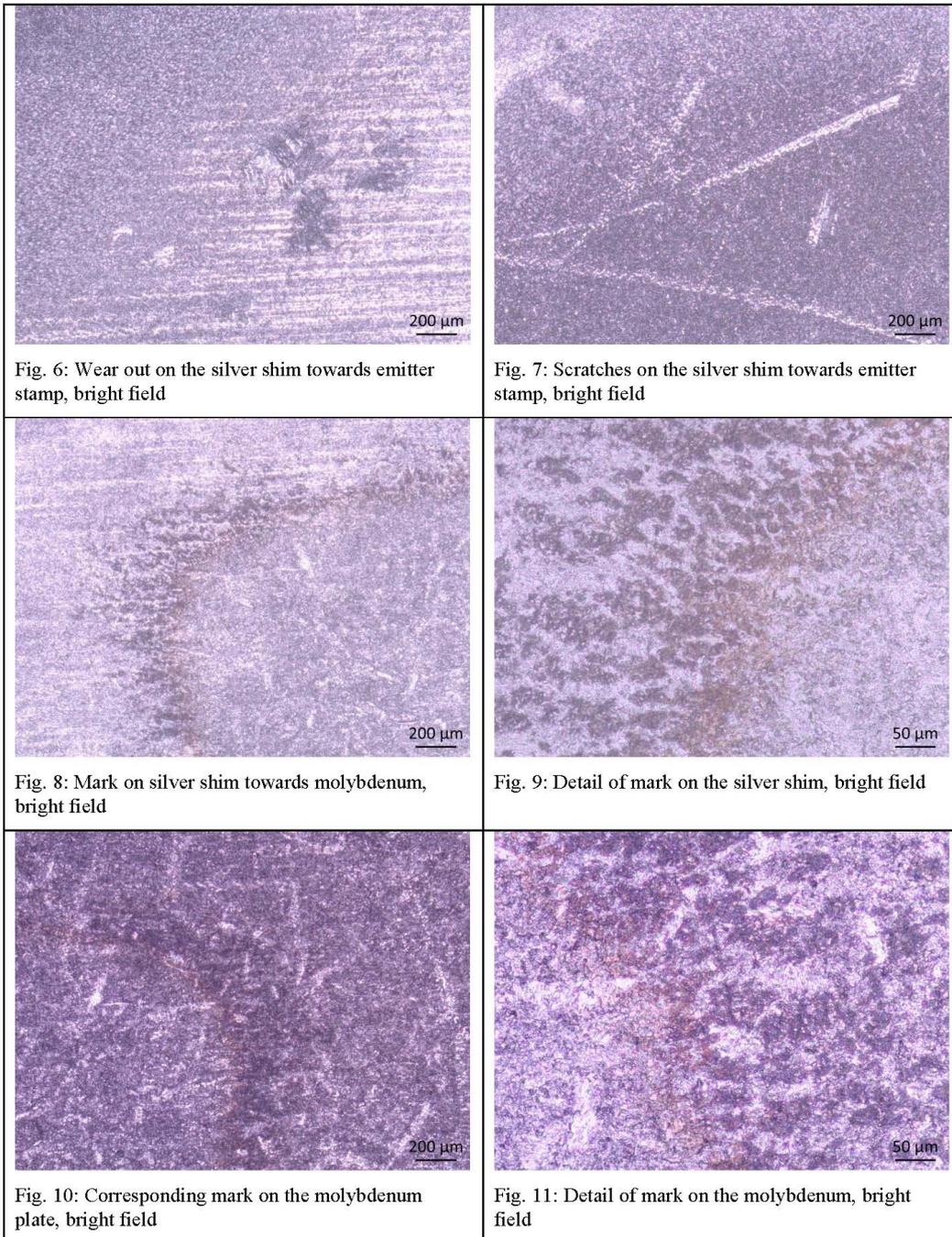For the microscopy a Zeiss AxioCam microscope was used.

Fig. 5: Location of the taken pictures

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To SINTEF Energy AS
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Fig. 6: Wear out on the silver shim towards emitter stamp, bright field

Fig. 7: Scratches on the silver shim towards emitter stamp, bright field

Fig. 8: Mark on silver shim towards molybdenum, bright field

Fig. 9: Detail of mark on the silver shim, bright field

Fig. 10: Corresponding mark on the molybdenum plate, bright field

Fig. 11: Detail of mark on the molybdenum, bright field

On the surface of the silver shim towards the emitter lid an area with signs of heavier wear out was determined (Fig. 5). These signs are only local as it can be seen in Fig. 5. Furthermore some scratches were observed in this area as well (Fig. 6).
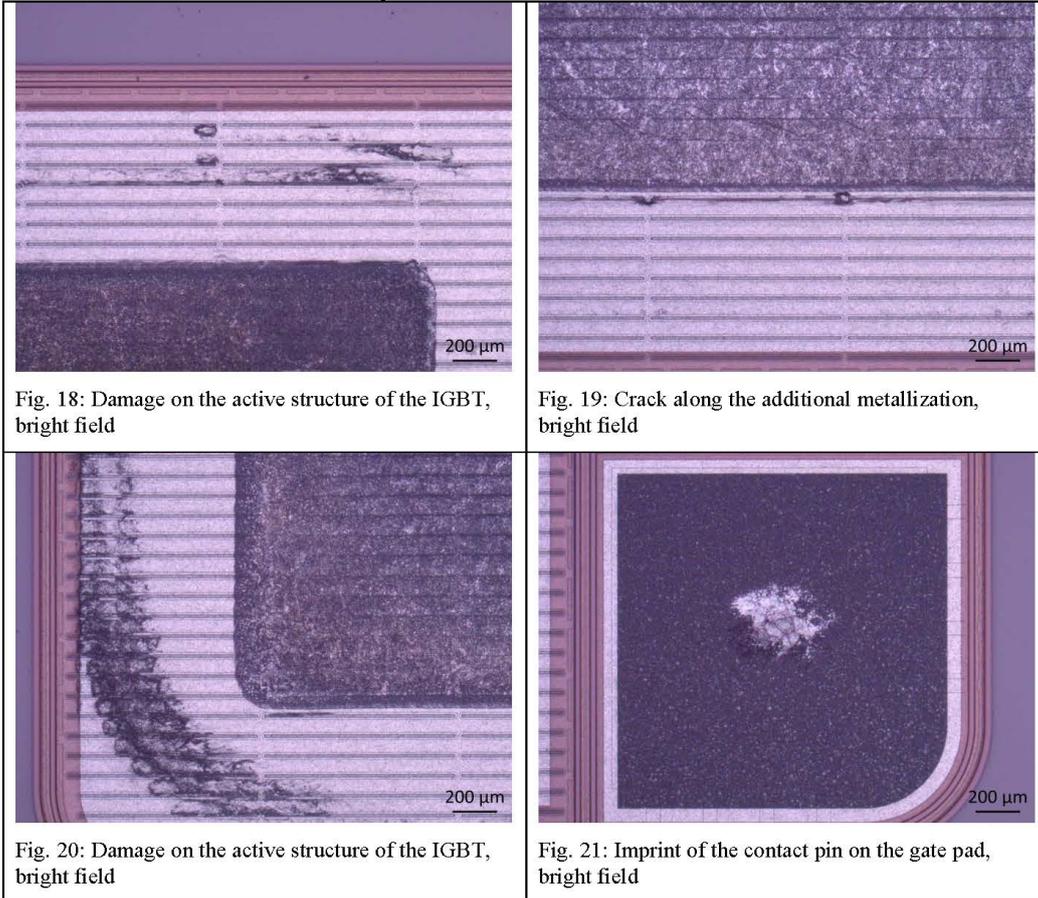
On the surfaces of the silver shim and the molybdenum plate towards each other, corresponding marks were observed (Fig. 4). Details of this mark are shown in Fig. 7 to Fig. 10.

Fig. 12: Area with changed color on the molybdenum towards the IGBT, bright field

Fig. 13: Additional metallization on the IGBT corresponding to the change of color on the molybdenum, bright field

Fig. 14: Damage on the active structure of the IGBT, bright field

Fig. 15: Detail of the damage, bright field

Fig. 16: Crack in the active structure, bright field

Fig. 17: Detail of the crack, bright field

At one corner of the molybdenum a change of color was observed (Fig. 2 and Fig. 11). The corresponding area on the IGBT showed heavy wear out of the additional metallization (Fig. 12).

Heavy damage of the active structure was determined at 3 out of 4 corners (Fig. 13, Fig. 14, Fig. 17, Fig. 19). Due to this damage the active structure was deformed severe. This kind of damage has been observed in previous investigations. Furthermore on one side of the IGBT

very thin cracks (Fig. 15) were determined which are assumed to be deeper than the cracks discovered so far. As shown in Fig. 16 these cracks cause a mismatch in the active structure.

Fig. 18: Damage on the active structure of the IGBT, bright field

Fig. 19: Crack along the additional metallization, bright field

Fig. 20: Damage on the active structure of the IGBT, bright field

Fig. 21: Imprint of the contact pin on the gate pad, bright field

Furthermore a long crack parallel to the additional metallization was found (Fig. 18). The damage on the gate pad is the same as for the other investigated chips (Fig. 20).

The change of color on the molybdenum and the marks on the silver/ molybdenum could be caused by a chemical reaction/ oxidation since the test was run in air and not in an inert atmosphere.

Analysis conducted by Lukas Tinschert.