NTNU – Trondheim
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Science and Technology

Single-Phase Bidirectional Power Factor Correction Boost Converter

Performance Evaluation of Totem-Pole PFC
Converter Using Wide Band Gap Devices:
GaN-HEMT and SiC

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Master of Science in Electric Power Engineering
Submission date: Januar 2015
Supervisor: Ole-Morten Midtgård, ELKRAFT
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By

Kalkidan Amare Gobena

A thesis submitted to

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Problem Description

Nowadays, telecom and data center industries are looking for a reliable and high performance power converter. The converter should provide high efficiency and high power density at reasonable cost. These issues can be addressed by a careful design and implementation of a converter topology that employs semiconductor devices with wide band gap material property and comprises few numbers of components. Wide band gap (WBG) devices are characterized by low on-state resistance and high thermal conductivity which in turn result in high efficiency and power density. Moreover, the design technique of the gate driver circuit also plays an important role to meet the specifications required by the industries.

The second main objective of this thesis is to utilize the stored energy in the batteries which serves as a backup source for several DC loads in data center and telecom sectors. Therefore, the proposed converter should allow bidirectional power flow between electricity mains and the backup batteries. The assignment is given for two students; single-phase AC-DC converter with PFC boost stage which is presented in this paper and DC-DC converter stage done by another fellow student.

Hence, in this master's thesis the student should:

- Assess different bidirectional PFC boost rectifier topologies and propose a topology which can give better performance: very close to unity power factor, low total harmonic distortion, high efficiency and high power density.
- Analyze and evaluate the performance of the converter topology by employing different semiconductor devices, basically Si, SiC and GaN HEMT.
- Simulate and study the performance of converter topology using LT Spice IV software.
- Produce a prototype for the converter and perform laboratory experiment at NTNU lab.
- Compare the results from computer simulation and laboratory experiment.

Assignment given: 18 August 2014, Trondheim

Supervisor: Ole-Morten Metgård, Elkraft

Co-supervisor: Tore M. Undeland, Elkraft and Erik Myhre, Eltek AS

Preface

First and foremost, I would like to thank Almighty God for his showers of blessings throughout my life and strengthen me to complete the master thesis successfully.

I would like to express my deepest gratitude to Professor Ole-Morten Midtgård, my supervisor. I have got his helpful guidance all the way in the thesis work and recommended me some good practices in the profession. He encouraged me to write a paper for EPE 2015 conference.

I would like to extend my sincerest thanks and appreciation to Professor Tore M. Undeland for his full support, expert guidance and encouragement on my thesis work. His valuable support was not only on the thesis work but also through other academic and professional advices. He was always there when I desperately need his technical and psychological help. He was my supervisor in the specialization project in fall 2013 and co-supervisor in my thesis work.

My sincere thanks also go to Erik Myhre, Dr. Ibrahim Abuishmais and Odd Roar Schmidt for proposing the thesis idea and giving technical support. Aksel Hanssen deserves great thank you for his support regarding practical matters in producing my prototype.

I would also like to thank my parents; my elder sister, Dad and Mom. They were always supporting and encouraging me to face every challenge in life. Their prayer really helps me to be who I am today.

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Kalkidan Amare Gobena
Trondheim, Norway
13 January, 2015

Abstract

Several DC loads in data center and telecom industry are fed by power electronic rectifiers. The same rectifiers are used to charge a number of batteries which serve as a backup power source in case of power outage or failure of rectifiers. However, the stored energy in the backup batteries is not utilized efficiently due to reliable source of power from the mains. Therefore, the industry is demanding a highly efficient PFC converter with bidirectional power flow.

Significant improvement has been observed in the performance of power converters since the existence of wide band gap (WBG) devices in the power electronics industry. WBG devices provide high breakdown voltage and high thermal conductivity which enable to produce a more efficient and higher power density converter.

In this master thesis, a novel bidirectional PFC converter with totem–pole topology is presented for energy storage application. The totem–pole topology employs two fast WBG switches and another two slow but very low on-resistance Si MOSFET switches. Since the current is not flowing through the body diode of power MOSFETs the reverse recovery dissipation of the active switches are significantly reduced. The proposed topology provides high PF with minimum input current harmonics, high efficiency and high power density.

A literature review on wide band gap devices such as SiC and GaN has been done. The dual benefits of low on-resistance and reverse recovery charge from GaN enhance the performance of the totem–pole topology, especially in terms of efficiency. Whereas, high thermal conductivity property of SiC enable to down size the heat sink and hence increase power density.

A brief study is made on the functionality of the proposed converter for smart grid application together with battery capacities in telecom network. The research indicates that there is a huge potential of stored energy in the telecom site. Therefore, bidirectional PFC boost converter will be a power solution for efficient and cost effective use of electricity storage that also can feed power back to the grid.

The proposed topology has been studied using computer simulation and tested in laboratory experiment. Based on the specification, a prototype is produced by employing SiC MOSFETs.

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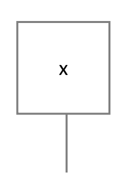
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Acronyms and Symbols

A	Ampere
AC	Alternating Current
ACMC	Average Current Mode Control
CCM	Continuous Conduction Mode
CM	Common mode
CSPI	Cooling System Performance Index
DCM	Discontinuous Conduction Mode
DC	Direct Current
DAB	Dual Active Boost
2-DEG	two dimensional electron gases
EMI	Electromagnetic Interference
GaN	Gallium Nitride
HEMT	High Electron Mobility Transistor
IC	Integrated Circuit
IEC	International Electromechanical Commission
IEEE	Institute of Electrical and Electronics Engineers
IGBT	Insulated-Gate Bipolar Transistor
JFET	Junction Field Effect Transistor
LTE	Long Term Evolution
LTSpice	Linear Technology Spice
MPP	Magnetics Molypermalloy Powder
MOSFET	Metallic Oxide Semiconductor Field Effect Transistor
Ni-Cad	Nickel cadmium
ORNL	Oak Ridge National Laboratory
PF	Power Factor

PFC	Power Factor Correction
PWM	Pulse Width Modulation
Qrr	Reverse Recovery Charge
R&D	Research and Development
RoHS	Restriction of Hazardous Substances
Si	Silicon
SiC	Silicon Carbide
SPICE	Simulated Program with Integrated circuit Emphasis
SBD	Schottky Barrier Diode
SMPS	Switch Mode Power Supply
Std.	Standard
TCM	Triangular Current Mode
THD	Total Harmonic Distortion
TI	Texas Instrument
t_{rr}	Reverse recovery time
UPS	Uninterruptable Power Supplies
V	Voltage
W	Watt
WDG	Wide Band Gap
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

1 Introduction

This master thesis is a continuation of my specialization project in fall 2013. Some part of the thesis work was carried out in specialization project phase and hence they are included in the thesis report with some alteration.

Chapter one discusses about background of AC-DC power converter with PFC boost stage. The need for a bidirectional PFC boost converter for telecom application is also the focus of this chapter. State-of-the art of wide band gap devices and PFC are also covered together with relevant literature reviews. Scope and limitation of the thesis work and the structure of the report are discussed at the end of the chapter.

1.1 Background

Different electrical loads require different amount of electric power for their operation. However, most of the time the electric power supplied from utility companies is AC power. This implies that there should be some kind of power processing unit which can fill the gap between the demand of electric power required by the different DC loads and the fixed AC power. Solid state devices can be used to process and control electrical energy such as rectifiers, inverters and DC-DC converters [1]. The AC-DC converters, commonly known as rectifiers, can be realized using diodes or controlled solid state switches such as Power MOSFETs.

The input current drawn from the AC mains contain harmonics. Power electronic equipment, welding machines, transformers, motors and generators are major cause for the degradation of power quality in the mains. Current harmonics result in damage to sensitive electronic equipment, excessive overheating of capacitors and interference with neighboring electronic equipment. The input current drawn should be shaped in accordance with the input voltage waveform so that current harmonics will be reduced in the mains [2].

The quality of power in AC lines can be measured, quantitatively, by power factor (PF) and total harmonic distortion (THD). Power factor can be defined as the ratio of the amount of useful power being consumed by an electrical system to apparent power in the circuit. The current harmonics can be reduced by incorporating power factor correction (PFC) circuit in the rectifiers [3].

1.2 Motivation

The demand on solid state AC-DC power converters increases from time to time. They are employed in several application areas such as uninterruptable power supplies (UPSs), back up energy storage systems, hybrid electric vehicle chargers, power supply for telecom loads and adjustable speed drives (ASDs) [3]. However, the power converters draw pulsating input current from the utility grids which results in poor power factor. Meanwhile, the converters pollute the AC mains by injecting significant amount of harmonic current from the switching devices due to high switching frequency [4]. Improving the poor power quality becomes a great challenge for power supplying companies (utilities) as well as power converter manufacturers.

The quality of input current drawn by low power electronic devices depends on the amount of current harmonics at the mains. In order to meet harmonic regulation and standards, such as IEC 61000-3-2 and IEEE Std 519, active PFC circuit is added as a front end stage [5].

The purpose of IEEE 519 is to recommend limits on harmonic distortion according to two distinct criteria, namely:

- There is a limitation on the amount of harmonic current that a consumer can inject into a utility network.
- A limitation is placed on the level of harmonic voltage that a utility can supply to a consumer [58].

The PFC circuit can reduce a significant amount of current harmonics. Low electromagnetic interference (EMI) can be achieved by employing boost type PFC converter as compared to other types of active PFC converters in continuous conduction mode (CCM) [5]. Moreover, most of the bridgeless topologies implemented so far are boost type configuration (also referred as dual-boost PFC rectifiers) because of its low cost and its high performance in terms of efficiency, power factor and simplicity [6].

Most of the PFC converters available today are unidirectional, from the AC mains to the DC load. Power electronics rectifiers are the primary source of electric power for DC telecom loads and batteries are used as a backup power supply during failure of the rectifiers or power outage. However, most of the rectifiers employed on this sector are unidirectional and the energy stored in the batteries is not utilized properly. Hence, this master thesis project targets to design and implement a converter which allows a bidirectional power flow between AC mains and the batteries so that the reserve energy in the batteries can be efficiently utilized.

An imminent to produce high PF rectifiers with reduced harmonic content in the input current, minimized EMI level, high efficiency, high power density, and lower cost and of course bidirectional power flow. In this paper, to meet this motivation, several single phase AC-DC boost converter topologies dedicated to PFC are studied and the best topology is selected and implemented using SiC and GaN.

Recently, many researchers and semiconductor manufacturers are attracted towards WBG materials and devices in order to use their benefits as switches in power converter application. Diodes and transistors made from SiC show a promising result in enhancing the power density and efficiency. Moreover, the newly invented GaN HEMT will be the future semiconductor material to produce the most efficient power converter.

1.3 State - of - the art

In this paper, state-of-the art for bidirectional PFC boost converter is discussed by looking the PFC converter stage and the impact of wide band gap materials on the efficiency of switch mode converter.

1.3.1 Power Factor Correction (PFC) Converter

These days, there is a dramatic increase in electrical loads and hence harmonic pollution of AC grid needs a lot of attentions. AC-DC converter with power factor correction is realized in order to address this issue. In passive PFC, large capacitor bank or LC tuned filter may be required to suppress the low frequency ripple which in turn results in large volume and weight of the converter [6].

According to [7] and [8], passive PFC converters provide a lot of advantages over active PFC converters based on ease of construction, reliability, reduced noise and surge, and also it avoids the high frequency EMI. However, their application is limited to low power, mostly below 200W, due to the bulky size of the filters, lack of voltage regulation, very sensitive to line frequency. Moreover, the fundamental component of current harmonics results in a phase shift that leads to a reduction in power factor. As suggested on [5], active boost AC-DC converter dedicated to PFC circuit can alleviate most of the problems related to passive PFC by replacing large resistors, inductors and capacitors by controlled solid state switches.

The conventional single stage AC–DC boost converter consists of a bridge diode, boost inductor and transistor switch. Even though this converter is very simple in construction, it provides low efficiency characteristics due to high switching loss in the diode bridge rectifier and high snubber loss [5], [9].

Since the two stage AC-DC converter incorporate PFC stage and DC–DC stage, the cost and size of the converter are somehow higher than single stage converter. However, the DC-DC converter stage is easy to design because the input voltage is fixed link capacitor voltage and hence the size and efficiency of DC-DC stage is improved. Moreover, size of input filters decreases due to the effect of PFC stage. High power density and high efficiency can be achieved by using two stage AC-DC boost converter with PFC topology [10], [11].

In this paper, only the bidirectional PFC - boost conversion stage will be covered. The DC-DC conversion stage is covered by a fellow student. Figure 1.1 show two-stage AC-DC converter structure.

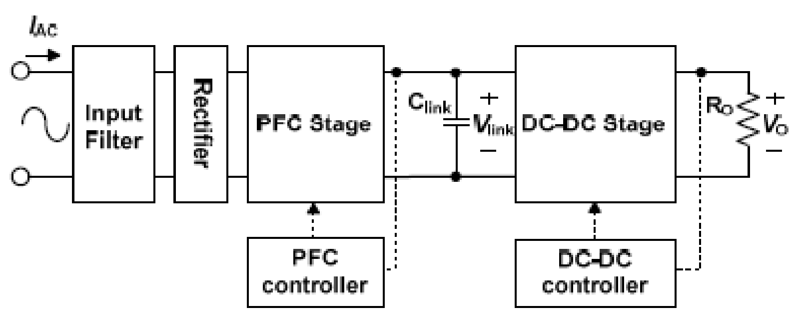


Figure 1.1: Two-stage AC-DC converter structures [12]

The selection of a suitable converter topology for a specific application is based on several criteria such as power density, efficiency, cost, complexity, and robustness. Within this context, a lot of work has been done in the last few years in order to improve the characteristics of conventional converters used for PFC purpose, such as the reverse recovery problem of boost diode as well as an increase in the output voltage of the converter [5], [12], [13] and [14].

In another research, the performance of the PFC converter has been evaluated by using two different switching schemes; hard switched dual boost PFC rectifier and a soft switched triangular current mode PFC. According to [15], a maximum efficiency of 99.2 % at a power density of 1.1kW/dm^3 has been achieved using the dual boost rectifier. For higher power density, the efficiency might be compromised and in dual boost rectifier the efficiency can be improved by 0.5 % with the expense of a decrease in power density by 1kW/dm^3. In order to avoid the limitation imposed by the switching losses, a new topology called Triangular Current Mode (TCM) resonant-transition PFC rectifier with zero voltage switching (ZVS) is proposed. Based on the research, this approach provides a power density of 5kW/dm^3 at efficiency of 98.3%.

In this paper, a novel bidirectional AC-DC converter using MOSFETs for all active switches is proposed for energy storage system applications. According to [16], the reverse recovery dissipation of the power switch is greatly reduced due to absence of freewheeling current flowing through the body diode of power MOSFET. The advent of high electron mobility transistors such as gallium nitride will be a key enabler for efficient bidirectional PFC boost converters.

1.3.2 Wide band gap materials (WBG)

Before the advent of wide band gap (WBG) materials, silicon was dominant semiconductor material used for switch application. WBG materials, such as silicon carbide and gallium nitride, enable the development of smaller semiconductor device that demonstrate significantly higher performance while demanding less power than more commonly used silicon semiconductor devices [17]. With the properties suitable for conducting electricity in extreme environments, they are ideal devices for applications that are subjected to high voltages and temperatures application found in electric vehicles and telecom converters which are located in harsh environment conditions.

Despite the benefits, commercial viability of wide band gap materials and devices is limited with pricing 3 to 5 times higher than silicon semiconductor devices. WBG materials contribute about 40% of the total cost device cost depending on the availability, quality and performance. Device design, fabrication and packaging are also key factors to higher cost.

According to [17], a world leader in materials research, Oak Ridge National Laboratory (ORNL), is applying vast expertise in a single crystal growth, epitaxial film decomposition and buffer development to improve the quality of WBG semiconductors by reducing internal defects and stresses.

GaN HEMTs and SiC MOSFTEs play a very important role in producing a high quality PFC converter. The devices are supposed to produce high efficiency and power density converter with almost unity power factor.

1.4 Scope and Limitation of the thesis

The scope of the project work encompasses:

- Reviewing of bidirectional converter topologies dedicated to PFC
- Over view of bidirectional PFC- boost converter for smart grid functionality
- Evaluate and analyze different bidirectional PFC boost topologies
- Design and implement the proposed topology
- Study the performance of silicon (Si), silicon carbide (SiC) and gallium nitride (GaN) in order to meet the desired requirement for the proposed converter.
- Design frequency control and voltage control
- Simulation based study on the proposed converter
- Establish experimental set up and discuss on the results
- Compare the results from simulation and laboratory
- Testing the new topology and providing a prototype

In any given research, there are always some limitations. In view of the foregoing, I hereby list some of the limitations of this thesis:

- It was unable to find GaN HEMT model in LTspice software so that Si MOSFETs with characteristics somehow similar to WBG devices are used instead.
- It was difficult to get freestanding substrate for GaN switching devices for the laboratory work.

1.5 Structure of the report

The first chapter presents the background of the PFC boost converter. Moreover, the motivation of the master thesis and state-of-the art of PFC boost converter together with wide band gap devices are also the main discussion points. Chapter 2 deals about the properties of wide band gap materials and also selection of WBG devices for the specific type of power converter. The third chapter mainly focuses on topology study. Active power factor correction converter, synchronous rectification and bidirectional PFC with totem-pole topology are briefly discussed. Smart grid functionality and battery management system are also point of discussion in this chapter. Design and implementation phase of the proposed converter is seen on chapter 4. Different gate drive control circuits are discussed including digital control techniques. Chapter 5 presents the simulation task on the novel bidirectional PFC-boost topology. List of components and equipment together with experimental set up are dealt on chapter 6. The main findings of the study, both from simulation task and lab experiment, are briefly discussed in chapter 7. The last chapter, chapter 8, gives conclusion of the thesis project and proposes future works to be done in the topic.

2. Comparison and Selection of Switching Devices

The main focus of this chapter is to study the property of semiconductor materials, specifically wide band gap (WBG), in order to get better performance from a power converters.

2.1 Wide band gap materials

Most power converters and wireless communication systems require switching devices having high breakdown voltage, high thermal conductivity and operate at high frequency [18]. Silicon based semiconductor technology doesn't fulfill all the above requirements due to its narrow band width. Currently, the focus of many researches is towards wide band gap devices (WDG) such as Silicon Carbide, Gallium Nitride and Diamond to address the shortcomings associated with Si based switching devices. Among those devices, diamond provides extremely large band gap and also has unique thermal characteristics but the research is at very early stage and needs more detailed study in the future. SiC and GaN show the best trade-off between theoretical characteristics, real commercial availability and maturity of their technological process [19]. SiC possess high thermal conductivity and wide band gap which makes the device a good choice for power electronics application. However, GaN offers a direct band gap and high frequency performance; because of which it finds great applications in optoelectronics and RF (radio frequency) devices [18].

In nowadays, silicon carbide (SiC) power switching device has got a lot of attention in power electronics industry which require high power and high temperature. The concentration of intrinsic charge carrier (n_i) in SiC is lower than conventional silicon based switching devices at specified temperature and this characteristic makes it better choice for high temperature application even in harsh environment. SiC MOSFETs can handle more than 700^{o}c of junction temperature. Whereas; Si-based switching device can only work at a maximum temperature of 175^{o}c at specified intrinsic charge carries [20].

2.2 Properties of WBG Semiconductor materials

Selecting the suitable semiconductor material used for power switches is not an easy task. It is very important to look and examine the property of the material in the design of a power converter. The main critical properties in the selection of switching device are band gap, electric breakdown field and thermal conductivity.

In addition to these, drift region width, on-resistance, saturation drift velocity and coefficient of thermal expansion also play significant role in determining the right choice of switching device for specific type of converter.

2.2.1 Band gap

In semiconductor physics, the band gap refers to the minimal energy state in the conduction band and the maximal energy state in the valance band. Wide band gap device requires more energy for the intrinsic charge carriers to cross the gap this results in lower leakage current in the blocking mode. The junction temperature of the WBG device is very high so that it can be used for high temperature application. Moreover, it provides reduced heat sink size and which in turn leads to a significant decrease in weight and cost of the converter. Figure 2.1 show the intrinsic charge carrier concentration versus junction temperature graph for Si and SiC with 4H hexagonal close packing of polytypes.

$$ni^2 = C.exp\frac{q.Eg}{KT} \qquad \text{[Eq 2.1]}$$

Where, ni =Intrinsic concentration (cm^{-3}), C=Constant (exact value depends on material and temperature [per unit volume]), q= Electron charge (C), Eg= Band gap (eV), K= Boltzmann's constant (J/K) and T=Temperature (K).

From the relationship given in equation [2.1], the concentration of intrinsic charge carriers is directly proportional to the band gap and inversely proportional to the junction temperature of the device.

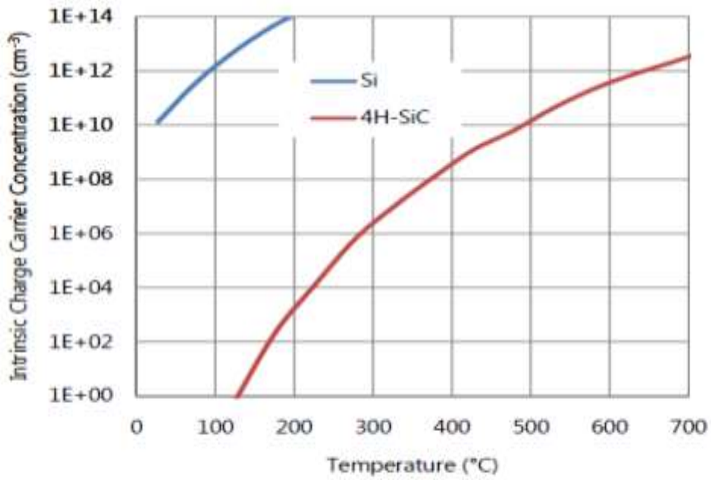


Figure 2.1: Intrinsic charge carriers' vs Temperature graph for Si and SiC [21]

As it is shown in Figure 2.1, for a large temperature range, intrinsic charge carrier concentration of 4H-SiC stays below 10^{15} cm^{-3}, where the intrinsic conduction of the semiconductor starts and it behaves as a bulk resistor and will not act as a semiconductor anymore. The intrinsic charge carrier concentration (n_i) of 4H-SiC at 700˚C is equal to that of Si at 100˚C. SiC does not approach this critical intrinsic carrier concentration until temperature exceeds 1000°C. From this, we can see that SiC power semiconductor devices can operate at much higher temperature than Si made power semiconductors device [21].

2.2.2 Electric breakdown field

High electric breakdown field enables the drift layer structure to be thinner and shorter which results in low specific on-state resistance, $R_{on\text{-}sp}$. The key figure of merit for power switching devices is the specific on-resistance and this parameter explains directly how much resistive loss a device generates in the forward conduction mode [21]. On-resistance of SiC polytypes (3H, 6H & 4H) and GaN devices is approximately 10 times less than Si based devices and hence WBG device provide much higher efficiency [18].

As an example, SiC can handle a higher electric field, approximately 10 times, than the Si before breakdown occurs. High electric field property of SiC enables to fabricate a semiconductor device very much thinner than its Si counterpart, approximately 0.1 times thinner. In addition to this, more highly doped drift layer and lower on-resistance can be achieved which is 10 times doping concentration and 10 times lower resistance than Si on the same blockage voltage [21].

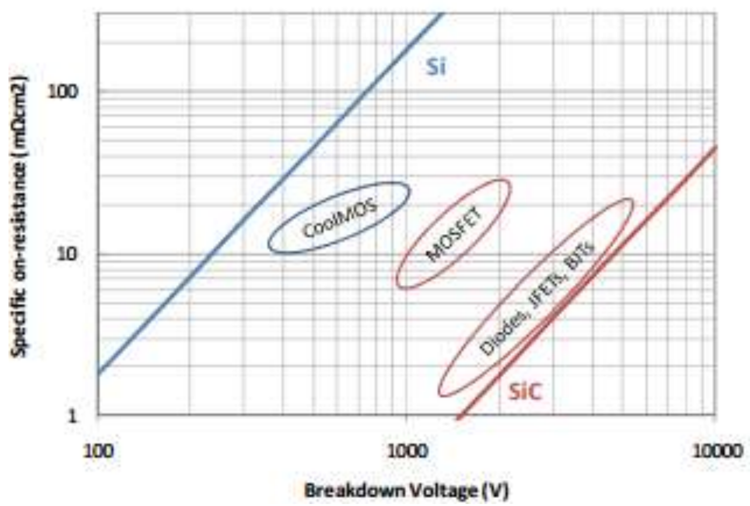


Figure 2.2: Comparison of unipolar limit of specific on-resistance versus blocking voltage for some device types in Si and SiC [22].

The mathematically relationship between specific on resistance and electric breakdown field for unipolar device is given as:

$$R_{on,sp} = \frac{4{V_B}^2}{\varepsilon \mu_n V {E_C}^3} \qquad \text{[Eq 2-2]}$$

Where, V_B= Breakdown voltage (V), E_c=Critical electrical field (V/cm), ε = permittivity (F/cm^2), μ_n=Electron mobility (cm^2/V/s).

2.2.3 Higher saturation electron drift velocity

Saturation velocity is the maximum velocity a charge carrier in a semiconductor, generally an electron, attains in the presence of very high electric fields [23]. Charge carriers normally move at an average drift speed proportional to the electric field strength they experience temporally. The proportionality constant is known as mobility of the carrier, which is property of the material. A charge carrier cannot move any faster once its saturation velocity has reached [24].

Saturation velocity is a very important parameter in the design of a semiconductor device, especially field effect transistor. Typical values of saturation velocity might vary greatly for different semiconductor materials, for example Si has saturation velocity about 1×10^{7} cm/s whereas; WBG devices such as GaAs and 6H-SiC have near to 1.2×10^{7} cm/s and 2×10^{7} cm/s respectively. Typical electric field strength at which carrier velocity saturate is usually on the order of 10-100 kV/cm.

High saturated drift velocity directly proportional to high switching frequency capabilities and therefore the power devices based on WBG can be switched at higher frequencies. This results in an extremely reduced in conduction and switching losses (much superior performance) thereby increasing efficiency [21].

2.2.4 High thermal conductivity

Thermal conductivity can be defined as the rate of heat transfer between two materials. WBG devices have high thermal conductivity and hence they transmit heat faster than Si based semiconductor devices. Higher thermal conductivities ease heat sinking requirements for WBG devices.

2.2.5 Coefficient of thermal expansion (CTE)

CTE measures the fractional change in size per unit change in temperature at a constant pressure. Semiconductor materials that have a closer CTE match to available electrically insulating ceramics (or the packing) can more easily be adapted for high power and wider temperature excursion applications. The table below summarizes some of the property of major power semiconductor materials.

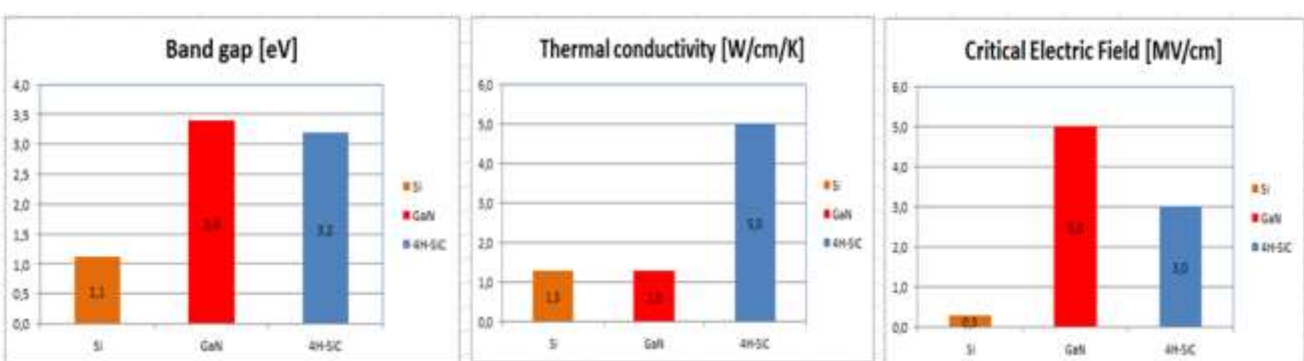


Figure 2.3: Comparison of three major physical properties of semiconductor devices using graph

Table 2.1 Physical properties of various semiconductors for power devices [26].

Property	Si	GaAs	3H-SiC	6H-SiC	4H-SiC	GaN	Diamond
Band gap, Eg (eV @300K)	1.12	1.4	2.3	2.9	3.2	3.39	5.6
Critical Electric field, Ec ($x10^5$ V/cm)	3.0	4.0	20	25	30	50	560
Thermal conductivity, λ (W/cm/K @300K)	1.3	0.54	5.0	5.0	5.0	1.3	20
Saturation electron drift velocity, Vsat ($x10^7$ cm/s)	1.012	2.0	2.5	2.0	2.0	2.0	3.0
Electron mobility, µn ($x10^3$ cm^2/V/s)	1.45	8.5	1.0	0.415	0.95	1.0	2.2
Hole mobility, µp ($x10^3$ cm^2/V/s)	0.45	0.4	0.045	0.09	0.115	0.035	1.8
Dielectric constant, εr	11.7	12.9	9.6	9.7	10	8.9	5.7

2.3 Comparison of wide band gap (WBG) devices

Recently, most power electronics manufacturers are more attracted in fabrication of WBG devices to exploit their high power and high temperature advantages. WBG devices, especially SiC and GaN, provide the best trade-off between material properties and commercial maturity [26]. These devices can be used for wide range of power application as shown in the figure below. However, this paper only focuses on low power converter application, in few ranges of kilowatts; specifically power supply/PFC range as depicted in Figure 2.4.

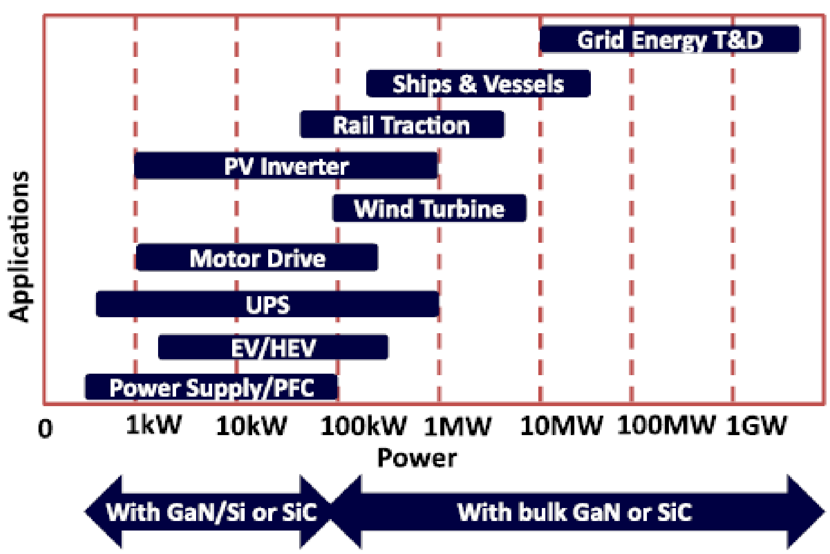


Figure 2.4: Entire ranges of power applications that can be addressed with SiC and GaN [28]

Figure 2.5 illustrate the summary of Silicon, Silicon carbide and Gallium nitride devices with respect to the properties of semiconductor materials. GaN can be used for high voltage and high switching frequency operations. Whereas, high temperature application needs a semiconductor material like SiC. Therefore, it is a trade-off to choose either of the WBG devices for desired application.

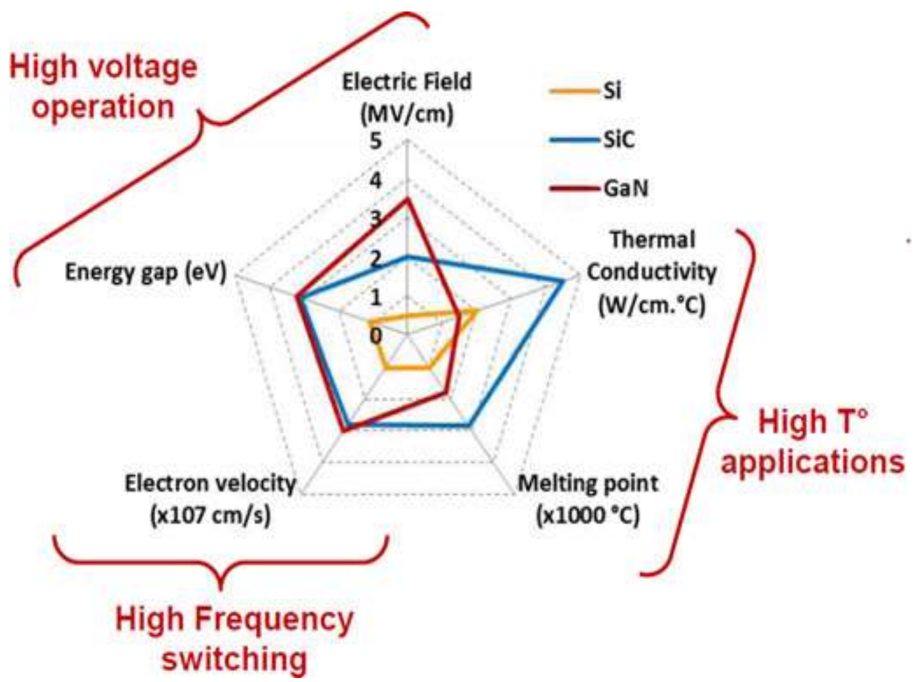


Figure 2.5: Summary of Si, SiC, and GaN relevant material properties [19]

2.3.1 Silicon Carbide (SiC)

Silicon carbide device technology has matured greatly over the past decades and gone from research to commercial production. The semiconductor technology greatly depends on the substrate and the epitaxial material. By definition, substrate or wafer is the crystalline material whereas epitaxy is the overlay deposition on the substrate [27]. In the last decade, a great improvement has been observed on the material quality and epitaxial processes of SiC and currently it is able to manufacture 100 mm wafers without any degradation. The material quality of 4H-SiC wafers and epitaxial is at such a high quality that many companies are offering commercial SiC wafers and epitaxial on 4H-SiC with wafer diameter 100 mm [22].

2.3.1.1 SiC Diodes

The market share of SiC by CREE and Infineon is substantially increased since 2009 [22]. SiC diodes are mainly used in power factor correction circuits (PFC), power supplies and recently photovoltaic (PV) inverters. The main advantage of the schottky barrier diodes (SBD) is the absence of reverse recovery current during switching; hence it is possible to increase the switching frequency considerably. Moreover, it can provide a significant decrease in volume, weight and cost for the system. For higher voltage (>3kV) either pn-diode structures or merged SBD/pn designs are considered because of the superior reverse blocking and surge current capability.

Table 2.2 Summary of the latest progress on SiC power rectifiers [21]

SiC Power rectifiers	State-of-the art device	Availability	Features
PiN diode	CREE 10kV, 20A 2" wafer	Commercially available (CREE and Infinion basically)	High voltage operation with low on-state resistance and low leakage current but requires reverse recovery charge during switching.
Schottky Barrier Diodes (SBD)	CREE1.2kV, 50A die size 5.6 mmx5.6 mm	Commercially available (CREE and Infinion basically)	Free from reverse recovery current, extremely high switching speed but lower blocking voltage and higher leakage current.
Junction Barrier Diode	CREE 10kV, 20A 3" wafer Chip size 10.6 mmx14.9 mm	Commercially available (CREE and Infinion basically)	Schottky like on-state and switching characteristics and PiN like off-state characteristics.

The major SiC power device products are still rectifiers based on Schottky barrier diodes (SBD) or junction barrier diodes (JBD). Nevertheless, many companies are manufacturing active power switching devices based on MOSFETs, JFETs and BJTs.

2. 3.1.2 SiC MOSFETs

One of the greatest achievements in the area of Silicon carbide power semiconductor device technology was the development of high voltage power MOSFETs. One of the challenges to use SiC MOSFET in power application is stability of the oxide layer. Recently, vertical power MOSFTE becomes quite popular for power switching application. It operates in normally-off (enhancement mode) and doesn't require complex gate drive circuit. However, this device has a short coming in terms of reliability due to sensitivity of gate dielectric and also relatively poor channel mobility under the gate dielectrics. The low mobility gives the MOSFETs a relatively high $R_{on,sp}$ for medium breakdown voltage (<2kV). Commercially available 1200V MOSFETs are recently released by CREE and a recent publication shows impressive performance [22].

Conventional silicon based MOSFETs are basically characterized by their high speed switching capabilities and high current carrying capacity at low blocking voltages. As the device blocking voltage increases, the on-state resistance goes higher and the current carrying capacity decreases in order to limit the on-state power dissipation. This tradeoff comes from the fact that a high blocking voltage requires a thicker drift region (epilayer). Since there is no conductivity modulation in majority carrier devices, the on-state resistance increases significantly [21].

2.3.1.3 SiC JFETs

A SiC JFET is typically a normally-on (depletion mode) device and conducts even though there is no gate voltage applied rather a gate voltage should be applied in order to stop conduction. A normally-on device is not recommended to use in power electronics application since it requires additional protection circuitry to prevent a DC bus short if the gate signals fail. The normally-on features demands a special gate drive design which results in complex design. However, this device looks very promising regarding reliability issues. This is because the device doesn't rely on the quality of gate control dielectrics unlike MOSFET device instead it strongly depend on the pn junction operation. Moreover, JFET exhibits a small capacitance and can thus be operated at high switching speed.

2.3.2 Gallium Nitride - High Electron Mobility Transistor (GaN-HEMT)

Currently, GaN-based semiconductor device are already in the market in photonics area. However, due to lack of high quality freestanding GaN substrates in the market it was unable to use the material for power application in the past few years. A well-defined global epitaxial relationship between the epitaxial GaN film and the substrate is the determining factor in order to grow high-quality, single-crystalline GaN film for power application. It was started by introducing foreign substrates such as Si, Sapphire and SiC to develop the epilayers of GaN. From the studies, substrate with Si provides GaN epilayer with lower cost compared to other substrates.

GaN actually has a higher theoretical critical field for breakdown, and would thus seem to be better than SiC. However, the GaN devices have so far shown much lower breakdown voltages than expected, possibly from the lack of free-standing GaN substrates. High injection devices are also not possible in the direct band gap of GaN [22].

GaN power devices become dominant in the power electronics industry due to their unique and most interesting property known as a 2-dimensional electron gas (2DEG) [19]. 2DEG is a gas of electrons free to move in two dimensions, but tightly confined in the third. This tight confinement leads to quantized energy levels for motion in that direction. Among the three WBG devices, GaN is the only heterostructure material which means it has unequal band gap due to a layer formed by dissimilar crystalline semiconductors. In AlGaN/GaN heterostructures, a large conduction band discontinuity between GaN and AlGaN is formed and the presence of polarization fields allows large 2DEG concentration with high electron mobility values (1200–2000 cm^2/Vs). Therefore, high breakdown voltage property of GaN-HEMT is realized by optimizing field plate technique and also by low on-state resistance.

A negative bias should be applied to the gate of GaN-HEMT in order to remove the 2DEG because they are intrinsically normally-on devices. Figure 2.6 show the cross section of normally-on GaN HEMT device. Recently, GaN-HEMT devices are getting much attention for high power application due to very low specific on-resistance and high break down properties. Moreover, they can provide high current handling capacity.

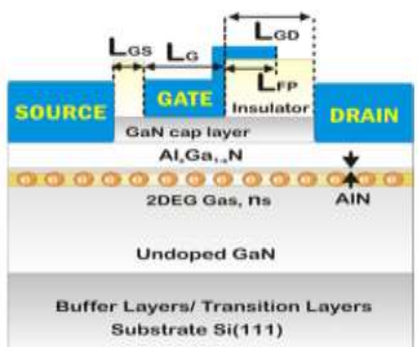


Figure 2.6: Cross section of a normally-on GaN HEMT [19]

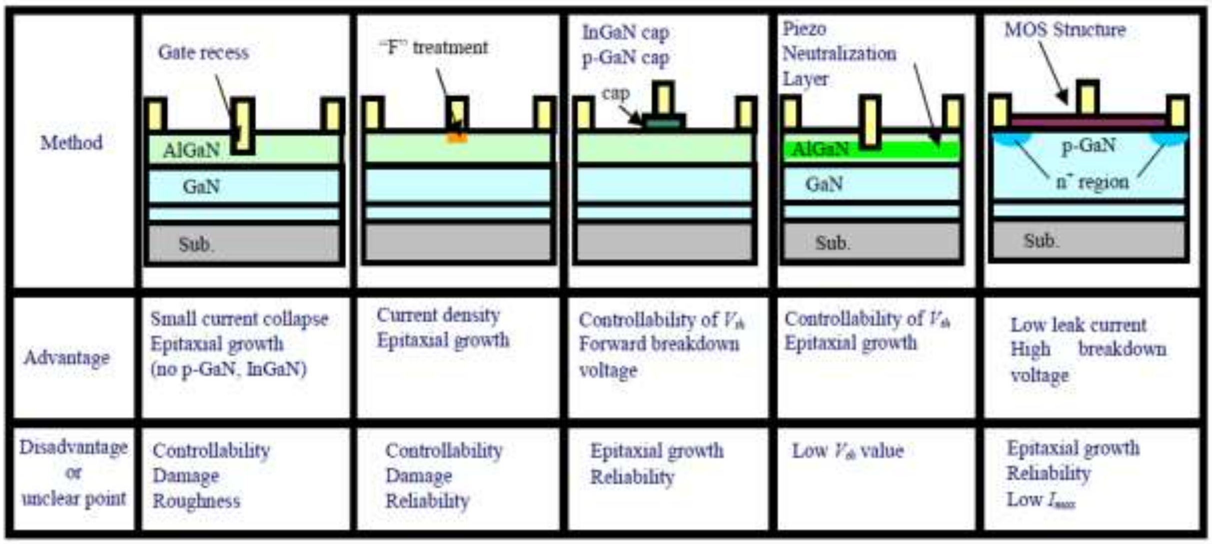
High speed and low switching loss characteristics of GaN devices make them very attractive for switching power supplies in ultrahigh bandwidth, in megahertz range [19]. Significant changes have been seen since the evolvement of the first GaN based HEMT switch both in terms of output power capability and voltage capability. Recently, it is able to manufacture a GaN-HEMT switch with 40W/mm output power capability and 10kV Voltage capability [18]. These remarkable performances of GaN-HEMT are achieved by suppressing the drain current collapse and also by increasing the gate-to-drain breakdown voltage through a control of the bulk and surface trap densities.

AlGaN/GaN HEMTs are generally promising candidates as switching transistors in power electronics area of application this is due to their high breakdown strength and current density in transistor channel gives a low on-state resistance, R_{on} [23] & [24]. However, their inherent normally-on behaviour would exclude them from most power electronics applications. Several approaches have been studied in the past few years to get the best out of the GaN-HEMT to apply for power switching device. Surface-charge-controlled n-GaN-cap structure, the recessed gate and field-modulating plate structure, and the passivation of surface states via silicon nitride or other dielectric layer can be mentioned as major research points [19].

2.3.2.1. Enhancement-mode (E-mode) GaN HEMT

The inherent problems associated with normally-on GaN HEMTs limit their application in power converter. Normally-off (or E-mode) GaN HEMTs are preferred for safety reason and fast switching speed [22]. Recent attempts to convert GaN HEMTs into normally-off devices using gate recess or fluorine plasma treatment showed limited applicability for power electronics due to their low threshold voltages $V_{th} < +1V$ and their voltage swings of approximately 2V. However, a Schottky-type metal on the AlGaN barrier acts as gate for normally-on HEMTs, a P-type doped semiconductor as gate is able to deplete the transistor channel when unbiased, thus yielding a normally-off device [23].

Table 2.3 Different approaches to realize enhancement mode GaN HEMT device [25]



Method	Gate recess AlGaN GaN Sub.	"F" treatment	InGaN cap p-GaN cap cap	Piezo Neutralization Layer AlGaN GaN Sub.	MOS Structure p-GaN n^+ region Sub.
Advantage	Small current collapse Epitaxial growth (no p-GaN, InGaN)	Current density Epitaxial growth	Controllability of V_{th} Forward breakdown voltage	Controllability of V_{th} Epitaxial growth	Low leak current High breakdown voltage
Disadvantage or unclear point	Controllability Damage Roughness	Controllability Damage Reliability	Epitaxial growth Reliability	Low V_{th} value	Epitaxial growth Reliability Low I_{max}

According to [25], it has been already able to develop n-GaN cap structure, called a surface-charge controlled structure for power amplifier application. Using n-GaN cap layer instead of AlGaN layer is able to prevent instability of frequency dispersion related surface. One good example is, n-GaN cap structure suppresses current collapse which is a key issue for the GaN based devices. Current collapse is the phenomena that on-resistance changes when transistor turns on. From the hypothesis, it has demonstrated that in off state high electric field will occur at the drain side edge of gate when high voltage is applied between source and drain. In this case, electrons are trapped on the surface of this area. These trapped electrons cannot be released easily even if gate voltage becomes turned-on, which results in the increase of on-resistance.

The paper, [25], also assessed the performance of n-GaN over the conventional AlGaN cap layer structure through experiment. From the result, embedding the top surface by n-GaN cap layer provides suppression in the current collapse by reducing the concentration of electric field at the gate edge and smooths the surface.

3. Single-Phase Bidirectional PFC - Boost Converter Topology Study

In this chapter, the characteristics and performance of different PFC - boost converters topologies are assessed in detail. Overview of smart grid functionality in bidirectional converter is also the main discussion point.

3.1 Active Power Factor Converter

Active power factor converters use power electronics active switches to change the current waveform drawn by the load in order to improve the power factor. Single phase PFC boost converter employs an input capacitor filter in order to limit the amount of switching noise propagation in to AC mains [29]. Based on this research, high power factor and low harmonic distortion can be achieved by operating the converter in CCM with average current mode control (ACMC).

PCF circuits can be broadly classified as passive and active. The basic building blocks of passive PFC are bridge diode and passive elements, such as resistor, inductor and capacitor. Whereas; active PFC uses active switch devices in conjunction with inductors [8]. Government agencies give a big attention towards active PFC circuit in order to improve grid supply capacities [3], [8]. Figure 3.1 show traditional PFC with line rectifying bridge.

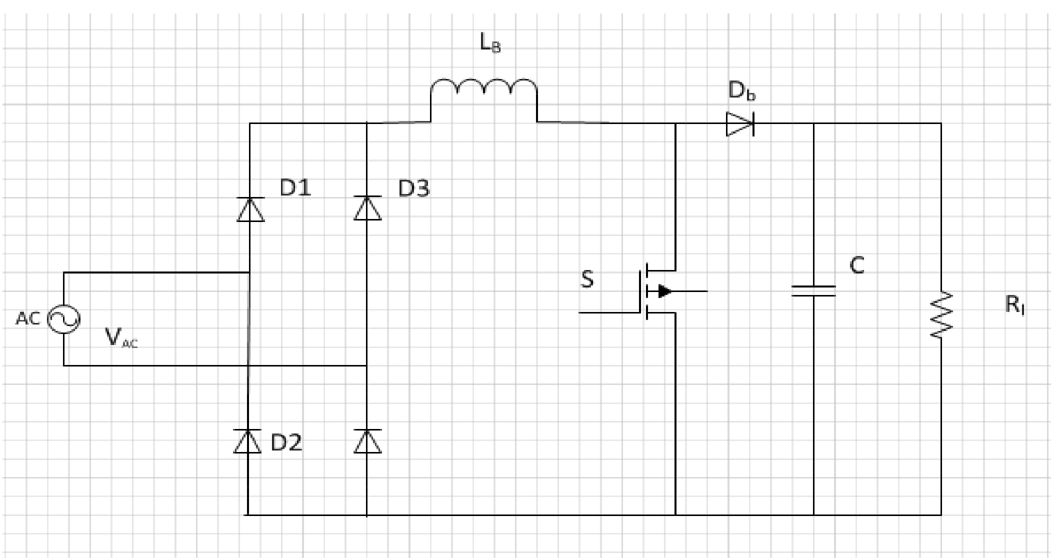


Figure 3.1: Traditional PFC with line rectifying bridge

According to [3], traditional PFC boost circuit is built from bridge diode, boost inductor, a slow diode and AC active switch. Based on continuity of the input inductor current, active PFC can be further divided into discontinuous conduction mode (DCM) and continuous conduction mode (CCM). Active PFC circuits operating in DCM are simpler than their CCM counterparts and hence their cost is much cheaper. However, low efficiency due to high current stresses and a need for large input EMI filter limit the DCM PFC circuit for low power applications only [30], [31]. For medium and high power CCM PFC is preferable.

Active PFC boost converters operating in CCM can be designed and implemented by using either single stage or two stages approach [32].The two stage converter comprises front-end PFC stage and DC–DC converter stage. According to [31] and [32], the two stage approach incurs additional PFC power stage and its control circuitry. However, it is the most widely used and cost efficient approach in high power application because of two major factors:

- ✓ PFC controller can provide a unity input power factor by sensing the input voltage waveform and shaping the input current to be in phase with the line voltage [31], [32].
- ✓ Since the voltage at the DC link is fixed, the efficiency of the DC-DC converter stage can be improved [32].

Active PFC boost converter operating in CCM produces an output voltage higher than the input voltage as shown in the figure 3.2 below. Since the converter can operate for the whole cycle of AC main, crossover distortion will not be a question for the input current. Moreover, the boost inductor is connected in series with the input that results in a continuous input current flow in the converter and even the switch cannot stop the input current to flow. Therefore, the input current contains fewer harmonic that leads to a reduced filter size and lower EMI.

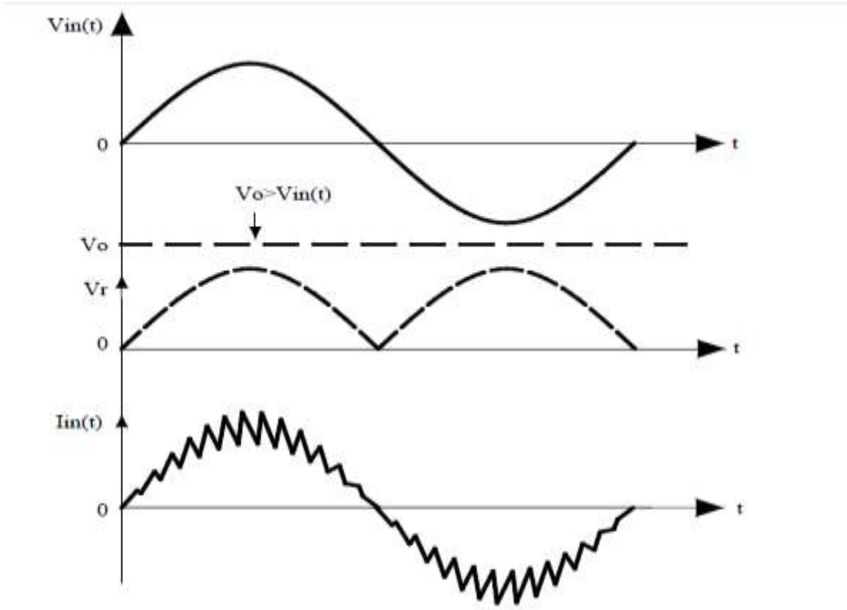


Figure 3.2: Current and voltage waveforms of a CCM boost PFC converter [30]

3.1.1 Review of two stage approaches

Two stage approach has two independent power stages. CCM boost PFC converter is usually employed as the front - end PFC power stage due to its high power factor, low total harmonic distortion (THD) and high efficiency characteristic [31],[32]. It consists of boost inductor, boost switch and rectifier. The rectifier can be either diode bridge for unidirectional converter or MOSFET switches if bidirectional power flow is required. The PFC controller is used to improve the input power factor. Based on [31], this can be achieved by detecting the waveform of line voltage and forcing the input current to follow the line voltage until there is no phase shift between the rectified current and voltage waveforms as shown below in Figure 3.4 (a).

The second power stage in the two stage approach is the DC-DC converter and its controller. The DC-DC output stage is the isolated output stage that is implemented with at least one switch, which is controlled by an independent controller to tightly regulate the output voltage [31]. In any PFC circuit, there should be an energy storage capacitor to store unbalanced energy. In single stage approach, the energy storage capacitor voltage varies with the load and line voltage because the controller is used to regulate the output voltage not the dc link voltage. However, in two stage approach, the PFC controller controls the dc link voltage and DC-DC controller control the DC output voltage. General structure of a two stage PFC boost converter is shown in the figure 3.3 below.

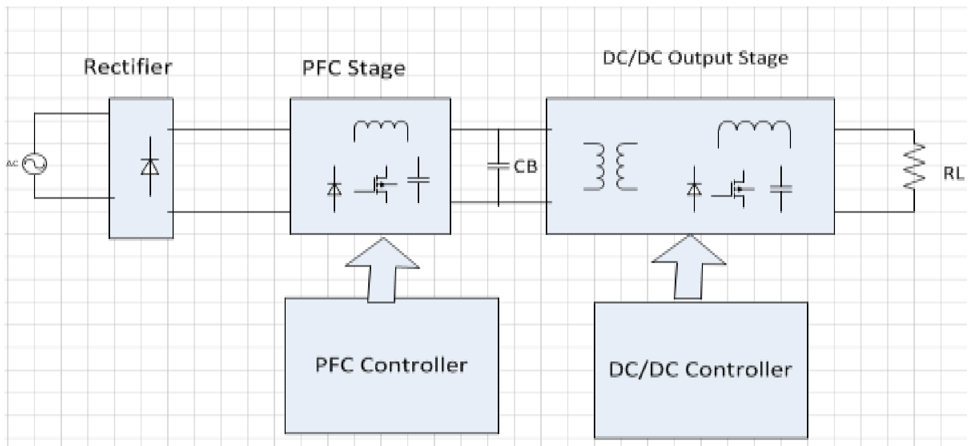


Figure 3.3: Conceptual structure of two-stage PFC converter

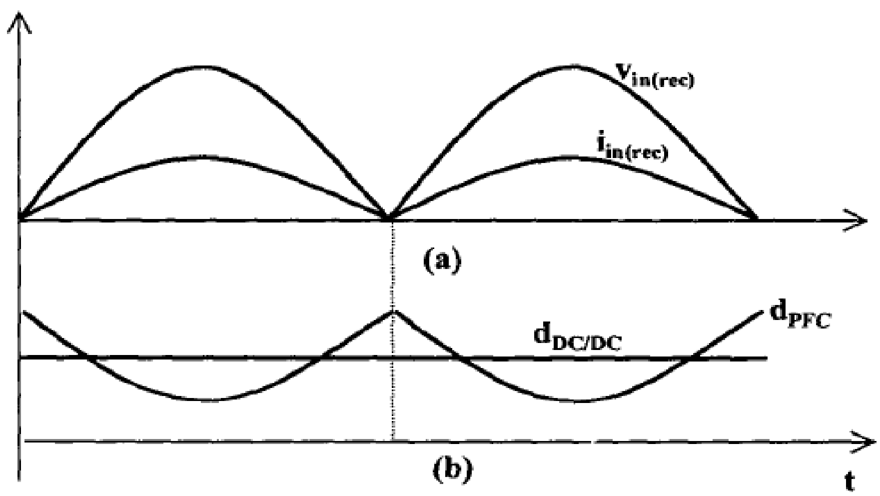


Figure 3.4: Ideal waveforms of the two-stage PFC converter

a) Rectified input voltage and current

b) Duty cycle of PFC and DC-DC switches [33]

Figure 3.4 (a) show the PFC controller can shape the input current waveform in accordance with the input voltage waveform to enhance the power factor of the converter and to reduce the input current harmonics. On the other hand, Figure 3.4 (b) show that the duty cycle of the front- end

PFC stage varies with time. Whereas, the duty cycle of DC-DC converter stage is almost constant in time because the input and the output voltage of the converter are fixed [32].

3.2 Synchronous Rectification (SR)

A synchronous rectification in high performance converter design is an essential block for low voltage and high current applications since significant efficiency and power density improvements can be achieved by replacing schottky diodes with low on-resistance MOSFETs [33]. Even though using SR in switching DC-DC converter provides a lot of advantages, there are also a lot of challenges to implement it correctly especially in boost converter design.

According to [33], most manufacturers were attracted to work on the buck controller. However, the existence of automotive start-stop, together with the widespread of battery-operated devices and telecom systems creates an opportunity for the development of boost based converters with higher efficiency, higher power density and novel protection features which were not available in the previous products. The problem is addressed by using a new generation boost controller ICs which can drive SR MOSFETs.

3.2.1 Diode Vs MOSFET

Typical boost converter diagram with diode is show in the figure below. The TI (Texas Instrument) authors show that the power dissipated in the diode D1 is considerably high and given by as:

$$P_{Diode} = V_D * I_{Out} * (1 - \mathrm{D}) \qquad \text{Eq [3.1]}$$

Where D is the duty cycle of the boost MOSFET

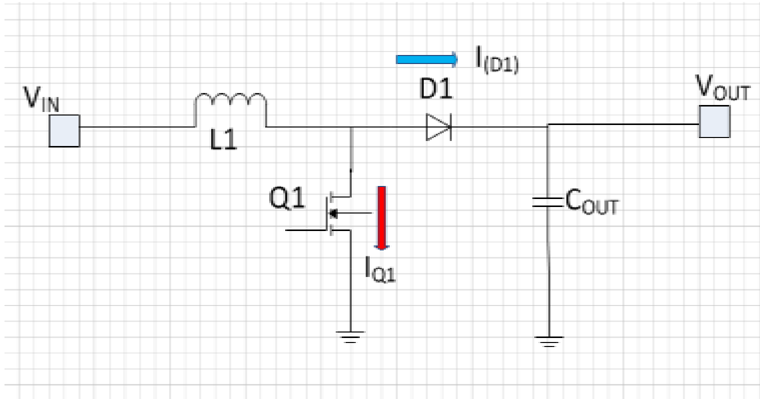


Figure 3.5: A boost converter with diode rectification

Bell and Lee's stated on their article, [34], that if the magnitude of the input and output voltages are very close, the duty cycle of the boost MOSFET is small. In the meantime, the corresponding (1-D) duty cycle of the diode is large. Since the diode carry large portion of the conducting time, the power loss associated with it becomes very high. The power dissipated in the diode can be approximated as:

$$P_{Diode} = V_D * I_{In} * (1 - \mathrm{D}) \qquad \text{Eq [3.2]}$$

However, the loss can be significantly minimized by employing MOSFET in place of diode and the Equation 3.2 can be written as:

$$P_{MOSFET} = R_{DS(ON)} * {I^2}_{In} * (1 - \mathrm{D}) \qquad \text{Eq [3.3]}$$

As it is clearly noticed from the two Equations given above, the power dissipation on diode is determined by the forward voltage drop V_D and the input current I_{In}. However, the power dissipation on SR MOSFET is dependent on on-state resistance of the transistor $R_{DS(ON)}$ and the input current I_{In}.

TI designers have built a MOSFET boost converter using new synchronous boost controller IC LM5122. The controller provides integrated gate drivers that directly control the low side boost MOSFET and the floating high side synchronous MOSFET. Moreover, the internal adaptive dead-time circuit avoids shoot-through between the two MOSFETs while optimizing efficiency.

3.3 Bidirectional PFC boost Converter topology

Most of the literatures regarding PFC boost converter are unidirectional [35] - [41]. However, allowing power flow in both directions has got a lot of attention these days. Bidirectional dual active boost (DAB) converter is proposed in [42]. High density bidirectional rectifier for 380V DC distribution system was tested with SiC-JFET switches in the laboratory and showed better performance than the conventional PFC rectifier [45].

According to [42], the single stage converter doesn't require front end PFC circuit and suitable for low power applications. However, the efficiency is less than two stage approach and also its application is limited to low power. Recently, more effort is exerted in order to increase the efficiency of the PFC converter at low line input for universal application using two stage approach [43]. The main objective of this paper is to study single phase bidirectional power converter for smart grid functionality. Specifically this sub chapter deals about the first stage of the two stage approach, front-end PFC boost converter, which allows bidirectional power flow between the AC mains and the DC link.

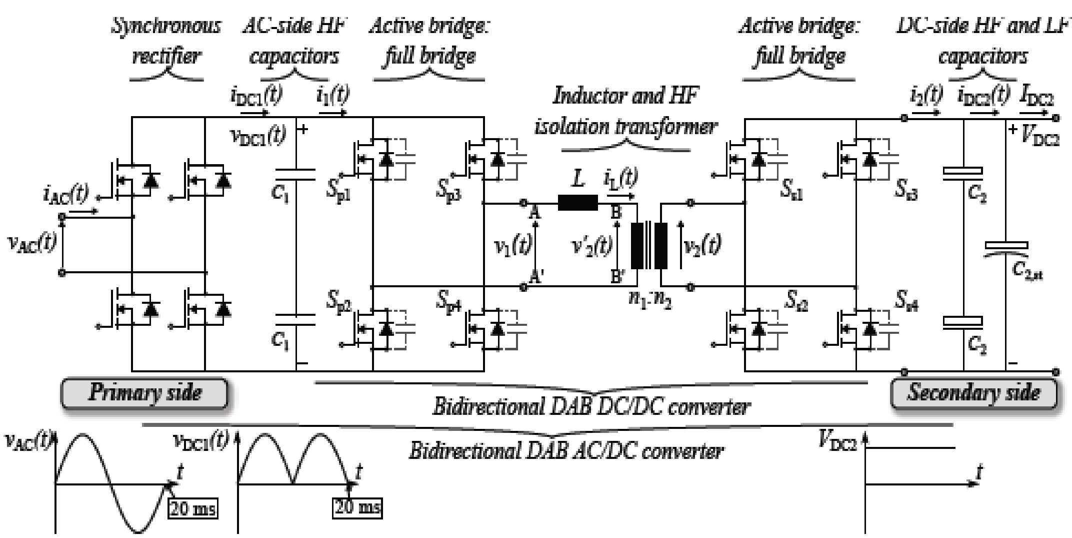


Figure 3.6: Circuit schematics of the bidirectional, isolated AC-DC converter topology [42]

The bidirectional power flow in PFC boost converter stage is controlled by the PFC controller. The control system monitors the DC link voltage and stabilizes the voltage by changing the source current. When the power flows from the grid to the DC side, which is in rectifier mode, the control system maintains the source current waveform and also be in phase with the grid line voltage. When the converter works in inverter mode, power flow from the DC link side to the grid, the source current is 180 degree out of phase from the line voltage. Therefore, the input power factor becomes approximately unity [44].

Since the current does not flow through the body diode of power MOSFET then the power dissipation due to reverse recovery of the active switch is greatly reduced. An interleaved totem-pole boost bridgeless rectifier is proposed with reduced reverse recovery for improved PFC [43], [46]. According to [43], the totem-pole boost bridgeless PFC rectifier eliminates common mode (CM) interference problem because the output is clamped to the input by slow diodes during each half cycle. Moreover, it has low conduction losses and hence high efficiency and low revers recovery process. In addition, totem pole topology has a potential capacity for bidirectional power conversion. However, the conduction of MOSFET intrinsic diode makes it not suitable for continuous current mode (CCM) operation. To suppress the reverse recovery of the diode, many methods have been proposed.

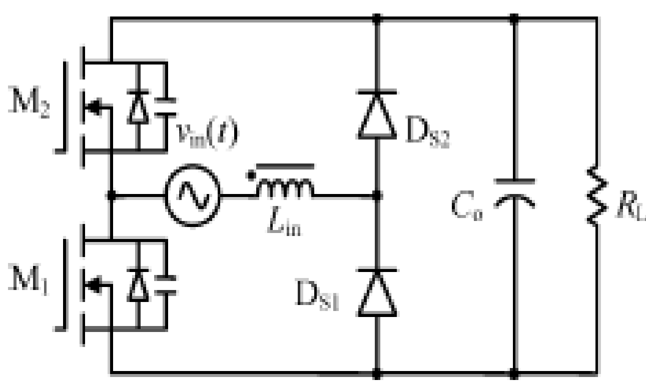


Figure 3.7: Totem-pole boost bridgeless PFC rectifier [43]

The totem- pole topology, shown in Figure 3.7, demands very low reverse recovery charge (Qrr) for the MOSFET body diodes which is not possible with high voltage silicon (Si) MOSFETs [43], [44]. The advent of gallium nitride (GaN) high electron mobility transistor (HEMT), in 1993, alleviates the problems associated with body diodes in SiC MOSFET [46]. In the future, the need for energy saving in electric conversion will be satisfied by currently emerging GaN HEMTs. The new 600V-class low Qrr transistors make this highly promising circuit a practical reality.

3.3.1 GaN totem - pole PFC topology

Transphorm Inc. introduced the first qualified 600V GaN HEMTs with low cost Si substrate [46], [47]. These days, the power electronics market is filled with these low on - resistance device, typically 15 milliohm, and low reverse recovery charge Qrr of 54 nC which is 20 times lower than state-of-the art Si counterpart as shown in Figure 3.8. Moreover, high power density and capacity for higher frequency operation make GaN very promising device in the power electronics industry.

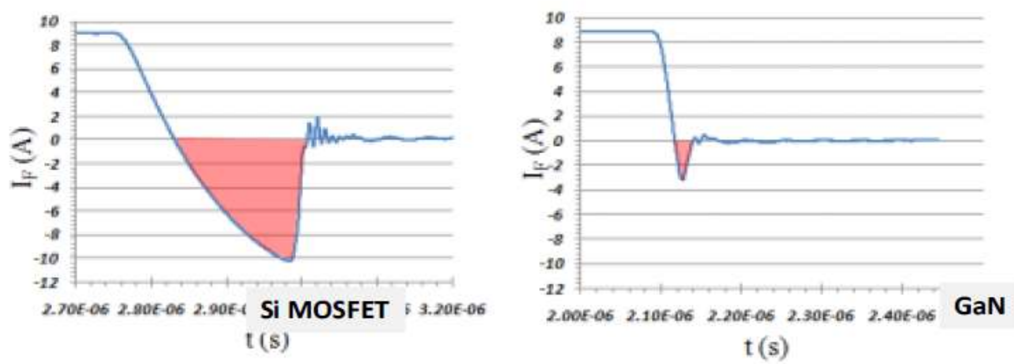


Figure 3.8: Reverse recovery charge test result for Si MOSFET and GaN HEMT with similar on-resistance,showing a 20x reduction of Qrr for GaN [48]

The totem - pole topology, shown in figure 3.9 (a), consists of a pair of GaN HEMT switches (Q_1 and Q_2) and another pair of MOSFET switches (S_1 and S_2). The GaN HEMT switches operate at very high pulse width modulation (PWM) frequency whereas the MOSFETs are operating at very low frequency, typically 50 Hz or 60 HZ. The switches, S_1 and S_2, serve as synchrounous rectifier by replacing the power diodes in bridgeless totem pole topology so that better efficiency can be achived. This is because the MOSFET switches provide constant and very low on resistance ($R_{DS(on)}$) when conducting as compared to power diodes [48].

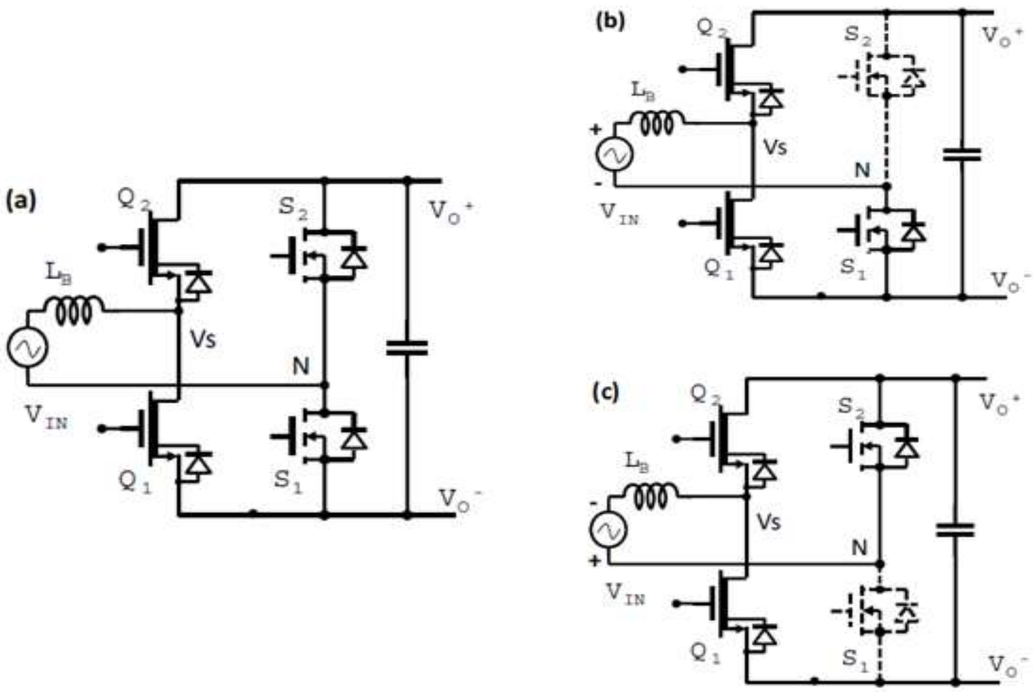


Figure 3.9: GaN totem-pole (a) Simplified schematics and illustration (b) positive AC cycle (c) negative AC cycle [48]

The operation priniple of totem - pole PFC for two half cycles is illustarted in Figure 3.9 (b) and (c). In the positive half cycle, the current flows through S_1 which connects the AC line to the output ground whereas S_2 is kept in the off position. In the GaN HEMT switch pairs, Q_1 is the active boost switch while Q_2 freewheels the inductor current and discharges inductor energy to the output side. In the negative ac cycle, Q_2 serves as active switch and Q_1 freewheels the inductor current. In the meantime, S_1 is in the off state and S_2 forces the ac neutral line tied to the positive terminal of the dc output.

In either AC polarity, one of the GaN HEMT transistor acts as a master switch and the other as a slave switch. The master switch allows the current to charge the boost inductor whereas the slave switch releases the stored energy in the inductor to the DC output [48]. The role of the two GaN transistors interchange in every half cycle so that each transistor has got a chance to be a master in one cycle and a slave on the other half. When both MOSFET switches are either fully or partially turned on, it provides a path for current to shoot through from V_{in} to ground. To avoid this situation, a dead-time is added in between two switching events during which both transistors are momentarily off.

During dead-time, the body diode of the slave transistor has to function as a free-wheeling diode for the inductor current to flow, therefore CCM operation can be achieved from the converter.

3.4 Overview of smart grid functionality on bidirectional converters

It is very important to study the meaning and behavior of smart grid since the modern PFC converters can be connected and work in synchronized manner with smart grid. What is smart grid? According to U.S. Department of Energy's modern green initiative, a smart grid is defined as a system that integrates advanced sensing technology, control methods and integrated communication into the current electricity grid system [49]. At the transmission level, the grid is intelligent and efficient. At the distribution and customer level, there are opportunities for automation, advanced data collection, and intelligent appliance control that provide opportunities for energy efficiency and better integration of distributed generation including renewables to reduce carbon emission.

Smart grid encompasses the distribution network with an interface to the transmission system. This includes distributed energy resources, grid interfaces, distribution circuits, customer loads and internet protocol (IP) addressable load control architecture that represent the decision support system of the smart grid. The distributed generation sources can be made by interconnecting solar cells, wind turbines, fuel cells and storage technologies.

Bidirectional power converter will be a key enabler for cost effective use of electricity storage that also can feed power back to the grid.

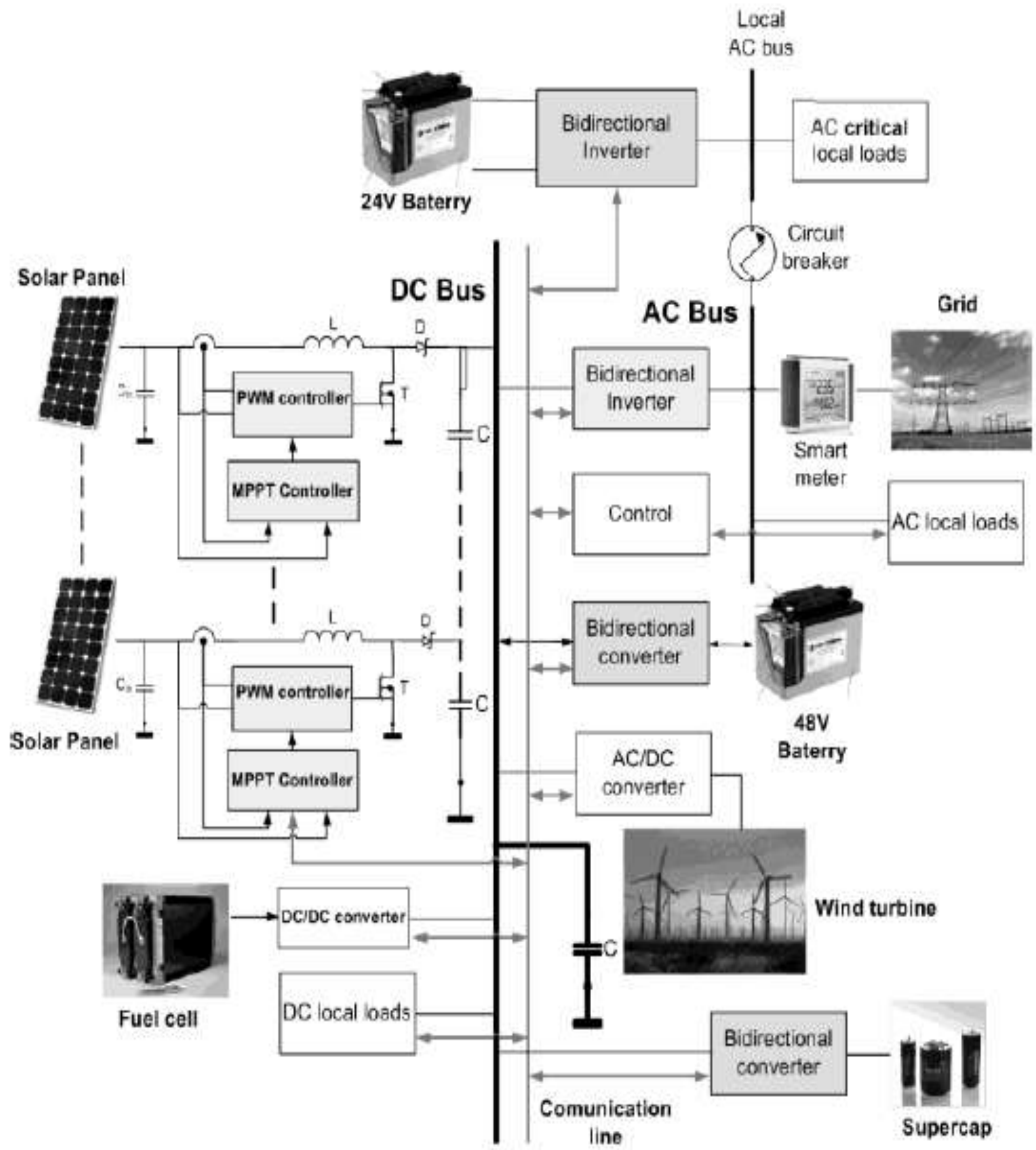


Figure 3.10: Typical smart grid [50]

A smart grid is a digital network that controls both distributed energy resources and interconnected load in order to operate the grid efficiently as shown in Figure 3.10. It can improve power distribution efficiency based on the design of the grid and customer usage power to flow in both directions.

The control system together with the bidirectional converter and the storage configuration will allow bidirectional power flow. The energy demand and the available energy determine the action of the smart grid which is either a current source or a current sink.

3.5 Battery capacity in telecom networks

Today, Information and communication technology (ICT) becomes the main tool for wide range of application and hence large amount of network traffic in telecommunication buildings and data centers has been seen. Energy saving in these buildings and data centers will contribute in saving our global environment problems. Therefore, having high efficient and space saving power supplies has become more indispensable. A 48-V DC power supply is now widely used for switching facilities, servers, and routers in telecommunications buildings [51].

In wireless data transmission infrastructures, the demand for batteries increases from time to time. Moreover, most European countries are attracted to the new wireless technology known as 4th generation-long term evolution (4G–LTE) network [52]. The new network provides users higher bandwidth for data communication, better internet service, good voice quality through mobile phones. The advancement in the network technology and the increase in power demand lift the battery market to new height. Nickel cadmium (Ni-Cad), lead acid and lithium-ion batteries can be used for telecom application.

According to [52], the rising popularity of hybrid base transceiver stations (BTS) promote the use of batteries as a renewable power source by most telecom network providers in order to reduce the cost of fuel in conventional diesel generators. The increase in the number of remotely located BTS and relevance of off-grid boosts the adoption of batteries for energy storage applications.

Figure 3.11: Rectifier and battery system for telecom application [From Eltek AS]

Telecom sites are installed in location where the application conditions can be quite different; they range from indoor to outdoor, from average low temperature to average high temperatures from a reliable grid with good continuous power to unreliable grid with extended outages every day to off grid. Whatever the location or application, all these sites are subject to a common focus by operators; that is to minimize the operating cost, to decrease the energy consumption, to reduce carbon emission, to increase reliability, to be more compact, to be lighter and to be easier to install, to get access for maintenance.

4. Control Circuit Design

In this chapter overview of the drive circuits is presented, PWM technique and soft switching technique are described and also drive circuitry of the proposed topology is discussed.

4.1 Overview of gate driver circuits

Bipolar transistors are current driven semiconductor switches whereas; powers MOSFETs with insulated gate are voltage driven. A basic knowledge of the principles of driving the gates of these devices is very crucial for the designer so that the switching speed of the device can be varied according to the requirements of the application. Totem - pole converter employees GaN HEMT or SiC as fast switch and Si MOSFETs as slow switch with very low on-resistance for synchronized rectification.

Average current mode control (ACMC) for single phase AC–DC boost converters with PFC is presented in [53]. According to [53], ACMC improves the performance of current control loop by significantly reducing the bandwidth requirement for a given line frequency in both unidirectional and bidirectional boost PFC converters. Moreover, ACMC has a capability of reactive power control in bidirectional converters. It supplies a prescribed amount of reactive power, either leading or lagging, independently of the DC load power which the converter to be used as a static reactive power compensator in power system.

The features of ACMC allow to employ a relatively low switching frequency and slow switching power devices such as insulated-gate bipolar transistors (IGBTs) in boost PFC converters. However, this master thesis considers a converter topology with high switching speed such as GaN HEMTs and SiC MOSFETs and hence this controller is not discussed here anymore and not employed.

4.2 Pulse Width Modulation (PWM)

In the PWM switching technique, the switch control signal is generated by comparing the control reference signal and the saw tooth or triangular signal at constant switching frequency. Duty cycle is defined as the ratio of the on-time duration to the total period of the signal and can be expressed by:

$$D = \frac{t_{on}}{T_s} = \frac{V_{Control}}{V_{tri}} \qquad \text{[Eq. 4.1]}$$

Where: t_{on} – On time, T_s– Switching period, $V_{Control}$ – Magnitude

V_{tri} – Amplitude of triangular signal or saw tooth signal

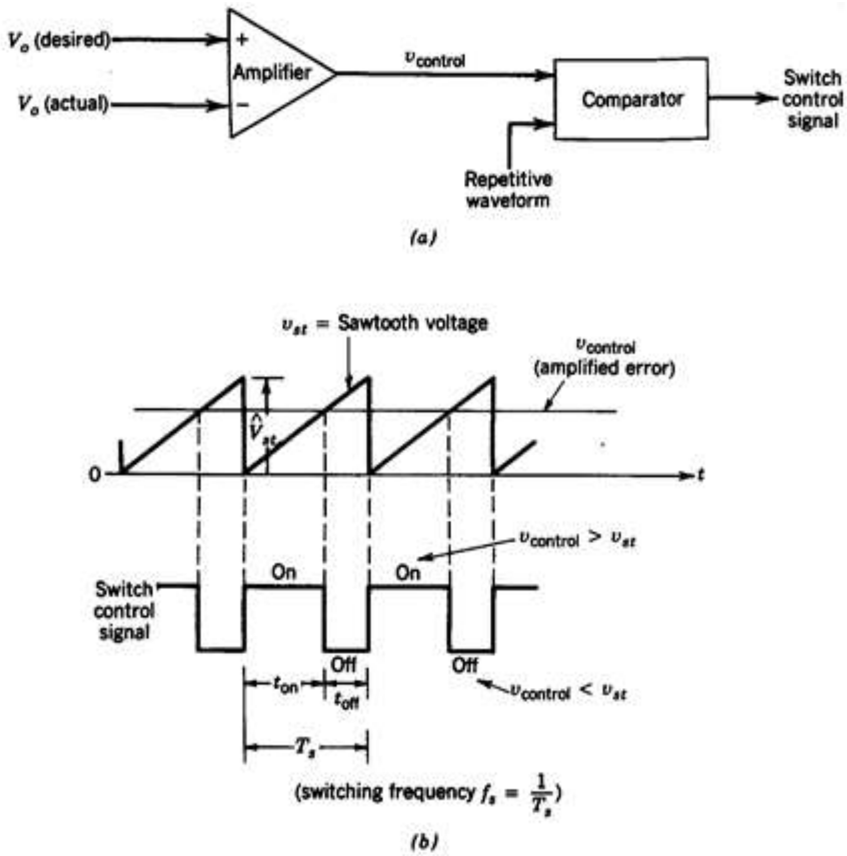


Figure 4.1: PWM generator (a) block diagram (b) PWM signal [1]

PWM control scheme is compared with one–cycle control technique [54]. According to the paper, the control reference signal in PWM is linearly modulated into the duty ratio signal and in a direction that reduce the error. However, one–cycle control technique is a nonlinear control method, which takes advantage of the pulsed nonlinear nature of the switching converters.

One inherent characteristic in totem–pole bridgeless PFC topology is the operation mode transition at AC voltage zero–crossing. For instance, when the circuit operation mode changes from the positive half cycle to the negative half cycle at the zero crossing, the duty ratio of switch Q_1 changes abruptly from 100 % to 0 % and the duty ratio of switch Q_2 changes from 0 %

to 100 %. Due to slow reverse recovery of body diode of the MOSFET, the voltage at V cannot jump from zero to V_{DC} instantly a current spike will be induced referring to figure 3.3. To alleviate this problem, a soft start at every zero crossing should be introduced to make a smooth reverse duty ratio. The current spike problem can be solved by employing large inductance in order to run the proposed totem-pole bridgeless PFC topology in CCM. The soft start time can be done for few switching cycles so that the situation can be handled in a perfect way.

4.3 MOSFET gate drive circuit design considerations

Since the gate of the MOSFET is electrically isolated from the source by silicon dioxide layer, current will not flow through the gate when a dc voltage is applied. Therefore, driving the gate of the MOSFET is similar to driving a very high impedance capacitive network [55]. The terminal capacitances are used to model power MOSFET as depicted in figure 3.2. The switching speed of the MOSFET is largely dependent on impedance of the capacitances and output impedance of gate drive circuit.

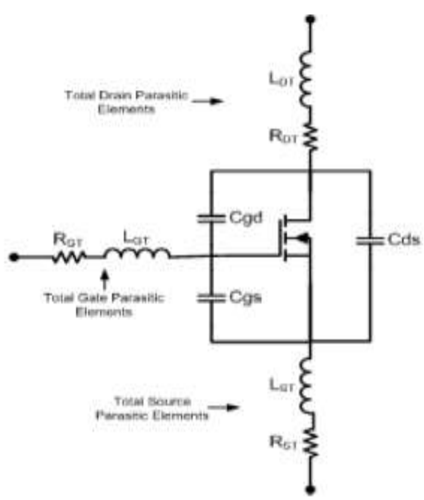


Figure 4.2: MOSFET parasitic elements [55]

According to [55], the most commonly occurred problems related to gate drive circuits breakdown of the gate oxide due to large voltage spikes, oscillation, ringing or false turn on and these problems can be minimized by proper design of electrical gate drive circuit.

The design consideration for MOSFET gate drive is expressed on the following capacitances; input, output, and reverse common source capacitances (C_{iss}; C_{oss}, and C_{rss}, respectively). The relationship between these capacitances is given as:

$C_{iss} = C_{gs} + C_{gd}$, when C_{ds} is shorted [Eq. 4.2]

$C_{oss} = C_{ds} + C_{gd}$, when C_{gs} is shorted [Eq. 4.3]

$C_{rss} = C_{gs}$ [Eq. 4.4]

The switching speed of the device depends largely on Crss and also the total output impedance of the gate driver circuit as seen from the MOSFET's gate. Therefore, during design phase it important to put the gate drive circuit very close to the MOSFET in order to minimize the parasitic elements caused by wire inside the chip.

Another problem that might occur during the operation of the converter is shoot- through. Shoot – through is defined as a condition if both MOSFETs switches are either fully or partially on then shorting the input voltage to the ground will happen [55]. Based on this paper, shoot-through can be reduced by inserting dead time between the switching signals supplied to the gate of the MOSFETs.

At the instant the high side of the MOSFET is turned on another type of shoot - through will occur. A high dv/dt will induce on the drain of the low side of the MOSFET that couple charges through C_{gd} which results in the low side of the MOSFET starts to turn on.

4.3.1 Bipolar totem-pole driver

One of the most commonly used and cost effective gate drive circuit for driving MOSFETs is a bipolar, non-inverting totem-pole drive as depicted Figure 4.3.

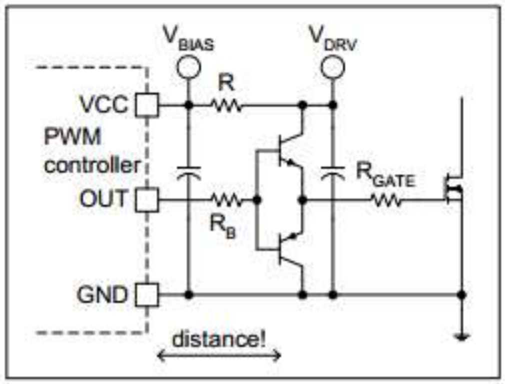


Figure 4.3: Bipolar totem-pole MOSFET gate driver [55]

Bipolar totem-pole driver can handle the current spikes and power losses and hence it makes it suitable for PWM controller. Of course, it should be placed right next to the power MOSFET it is driving so that the high current transients of driving the gate localized in a very small loop area and hence reducing the value of parasitic inductances.

4.4 Gate drive control of totem-pole PFC

The control of totem – pole PFC with MOSFET for synchronized line rectification is shown in Figure 3.4 with two more driving PWM signals for the MOSFET during each half cycle. The voltage and current loop control are the same as conventional boost PFC converter. The feedback signals from the converter are the V_{DC}, V_{AC-P}, V_{AC-N} and I_L. The polarity and rms value of input voltage can be determined from V_{AC-P} and V_{AC-N}. The output of the outer voltage loop multiplied by the magnitude of the input voltage, $|V_{AC}|$, gives sinusoidal current reference. The current loop provides the duty ratio for the boost circuit. The polarity of the input voltage is used to determine how the PWM signal is distributed between switches Q_1 and Q_2. Soft start is used, for a short period of time after the zero – crossing, in order to make smooth reverse duty ratio.

As it is depicted in Figure 4.4, the PWM distribution block generate a gate drive signal for the fast switches Q_1 and Q_2 for demonstration purpose only. It can be considered that the distribution block also produce gate drive signal for slow switches S_1 and S_2 during each half cycle.

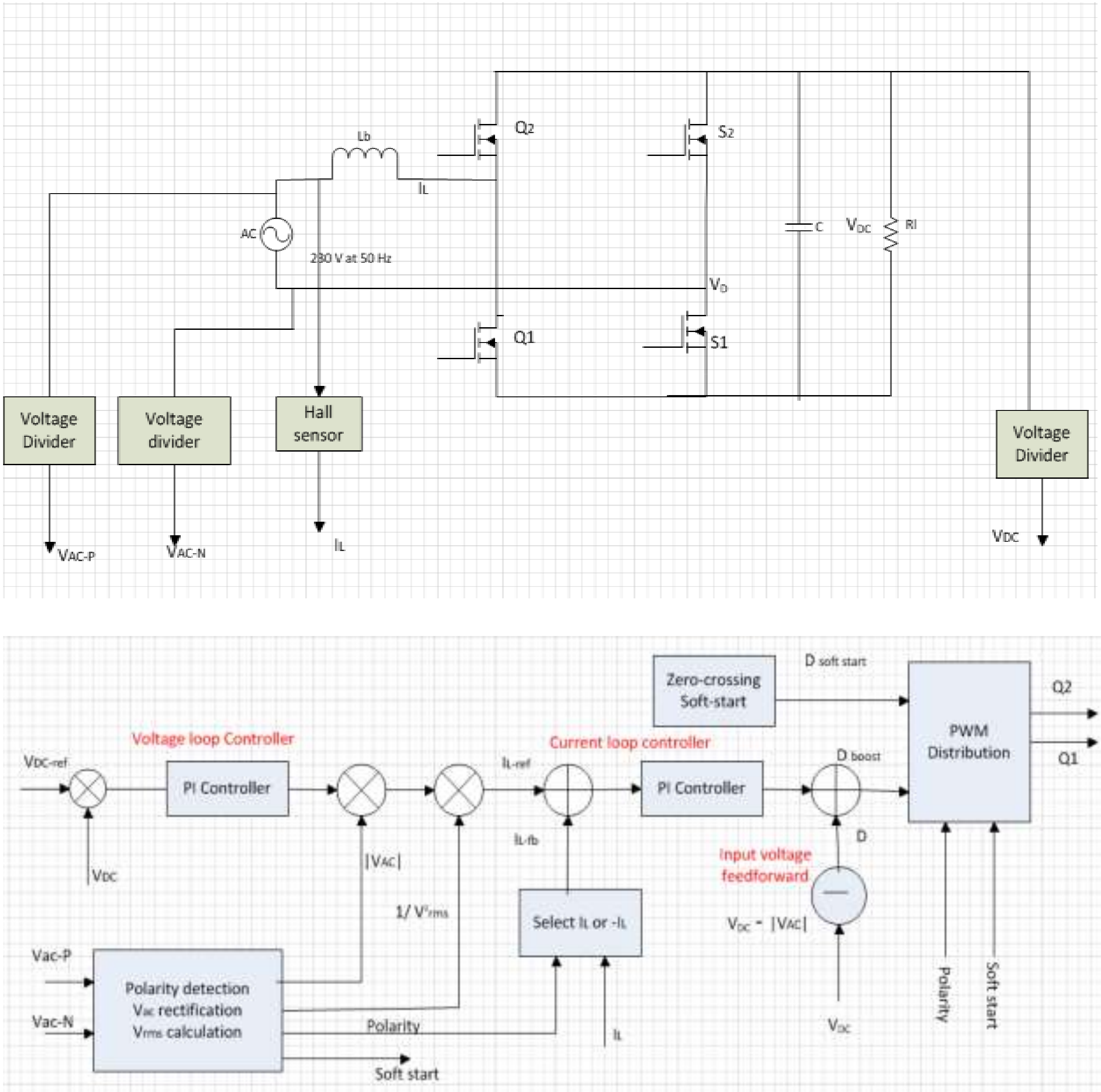


Figure 4.4: Totem-pole topology with control circuit block diagram

4.5 Switching Technique

The efficiency of static power converter can be maximized by using switch mode technique. Switching frequency can be varied from 50 Hz in Silicon Controlled Rectifier (SCR) to 1MHz in MOSFET case. The switching or dynamic behavior of power semiconductor devices thus attract attention, especially for the faster ones, for a number of reasons such as optimum drives, power dissipation, EMI/RFI issues and switching aid network.

At present day, power converters operate at very high switching frequency mainly to reduce weight and size of the filter component. For a converter with high power rating, above 1KW, soft switching is widely used to reduce the losses associated with switches. It still needs soft-switching in high-frequency operation due to considerable package and layout parasitic inductors and capacitors.

4.4.1 Concept of Soft Switching

The operation of power electronics switches in zero voltage switching (ZVS) or zero current switching (ZCS) mode is called soft switching. Switching transitions occurs under favorable conditions such as device voltage is zero or device current is zero.

In ZVS, during turn ON, switching voltage brought to zero before the gate voltage is applied. It is ideally zero-loss transition. During turn OFF transition, low-loss and the parallel capacitor serve as loss-less snubber. ZVS is mostly preferred for very high frequency applications using MOSFETs. However, due to tail current at turn-off ZCS is best suited for converters with IGBTs. During turn off in ZCS mode, the switch current brought to zero before gate voltage is removed.

Figure 4.5: ZVS scheme

In general, soft switching provides lower losses, lower EMI and it allows high frequency operation. The tables given below show the comparison between soft switching and hard switching.

Table 4.1 Comparisons of hard and soft switching

Switching	Hard switching	Soft switching
Switching loss	severe	Almost zero
Overall efficiency	Normal	Possibly higher
Heat sinking requirement	Normal	Possibly lower
Hardware count	Normal	More
Overall power density	Normal	Possibly higher
EMI problem	Severe	Low
dv/dt	Severe	Low
Modulation Scheme	Versatile	Limited
Maturity	Mature	Developing
Cost	Normal	Higher

From the table 4.1, it is clearly seen that soft switching provides better performance for the converter with a bit higher cost. Soft switching can be applied for the proposed totem-pole topology so that higher efficiency and high power density is obtained. However, it is in the developing phase and is not implemented in this prototype.

4.4.2 Dead-time circuit

Dead time circuit provides a means of limiting the output switch duty cycle to a value less than 100%. Without any dead-time, the inductor does not have sufficient time to reset and hence it might probably result excessive saturation transistor currents. Dead-time refers to the time that exists between the outputs of a PWM that is designed for push-pull operation. It is very important to add dead-time in the control circuitry in the PWM controller this is because if two transistors are ON at the same time, large shoot-through currents will flow. Therefore, dead-time helps the transistors not to conduct at the same time and considered as measure of assurance for the transistors.

One important issue in totem-pole PFC boost converter is the operation mode transitions at AC voltage zero crossing. For instance, during the transition period from positive half cycle to negative half cycle, the duty ratio of switch S_2 drops sharply from100% to 0%. In the meantime, the duty ratio of another slow MOSFET switch, S_1, abruptly changes from 0% to 100%. Due to slow reverse recovery of the body diode of MOSFET, the voltage V_D cannot jump from ground to V_{DC} instantly and this result in a current spike. This problem can be alleviated by adding a dead-time in the control circuit at every zero-crossing so that smooth reverse duty ratio can be achieved. Moreover, the proposed totem-pole PFC boost topology is designed to operate in CCM, large boost inductance is used and it will solve the current spike issue at zero-crossing. Dead time can be introduced in the gate control circuitry by using digital electronics as shown in the Figure 4.6.

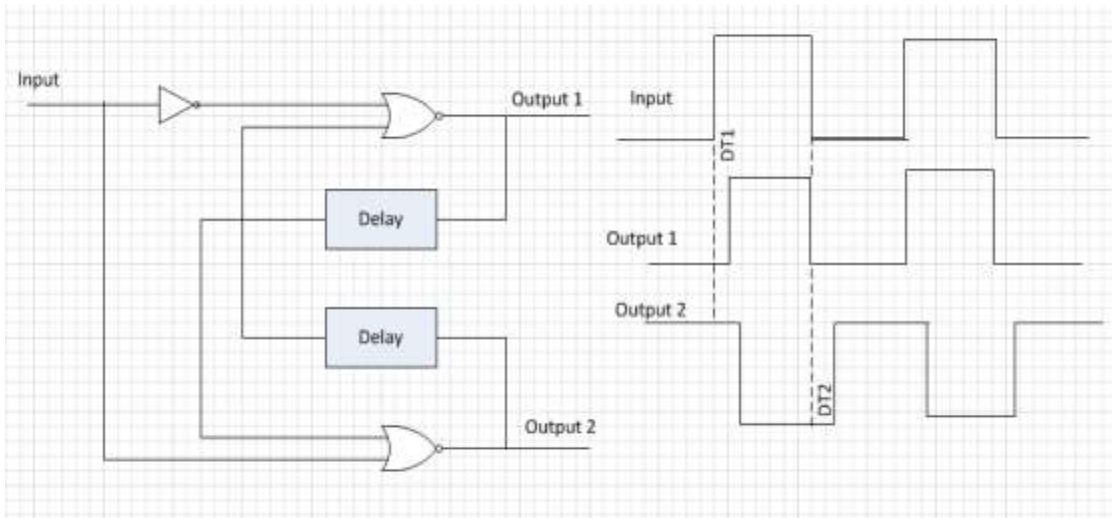


Figure 4.6: Dead-time generation circuit

4.4.3 Soft- start

During start-up, the power switching transistors go through a high stress. In order to minimize the stress on the transistors, the start-up surge that occurs as the output filter capacitor charges must be reduced. The availability of the dead-time circuit makes input implementation of a soft-start circuit relatively simpler [56]. For instance in Figure 4.7, at the start, capacitor C_s forces the input of the dead-time circuit to follow the 5V reference regulator that disables both outputs, i.e., 100% dead-time. As the capacitor charges through R_s, the output pulse slowly increases until the control loop takes command. If additional control is to be introduced at the input, a blocking diode should be used to isolate the soft-start circuit. The use of a blocking diode for soft-start protection is recommended. This is not only to prevent large current surges during power-up but also protects against any false signals that might be created by the control circuit as power applied. Soft-start for few switching cycle is enough to tackle the problem.

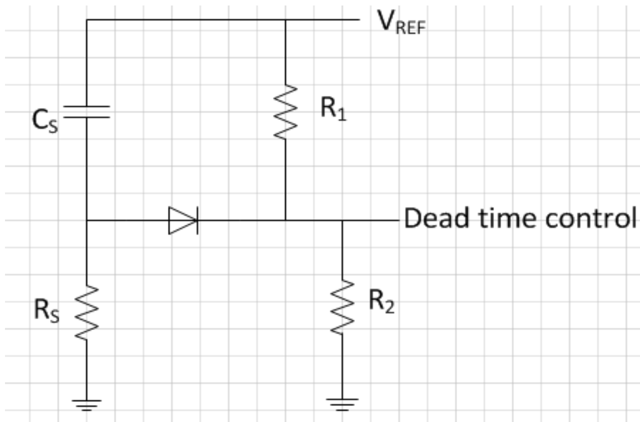


Figure 4.7: Soft-start circuit

The soft-start circuit allows the pulse width at the output to increase slowly, as shown in Figure 4.8 below, by applying a negative slope waveform to the dead-time control input (pin 4) [56]. Initially, capacitor C2 forces the dead-time control input to follow the 5V regulator which disables the output (100% dead time). As the capacitor charges through R6, the output pulse width signal increases slowly until the control loop takes command. After start-up, the voltage at pin 4 is 0.5V at 1:10 resistor ratio between R6&R7 [56].

In general, the soft-start time is in the range of 25 to 100 clock cycles. For example, If 50 clock cycles at 50 kHz switching frequency, which is typical for totem-pole topology, switching rate is selected, the soft-start time is:

$$t = \frac{1}{f} = \frac{1}{50\ \text{kHz}} = 20\ \mu\text{s per clock cycle} \qquad \text{[Eq 4.5]}$$

The value of the capacitor then is determined by:

$$C2 = \frac{\text{soft-start time}}{R6} = \frac{20\ \mu\text{s} * 50\ \text{cycles}}{1\ \text{k}\Omega} = 1\ \mu\text{F} \qquad \text{[Eq 4.6]}$$

This helps to eliminate any false signals that might be created by the control circuit during start-up.

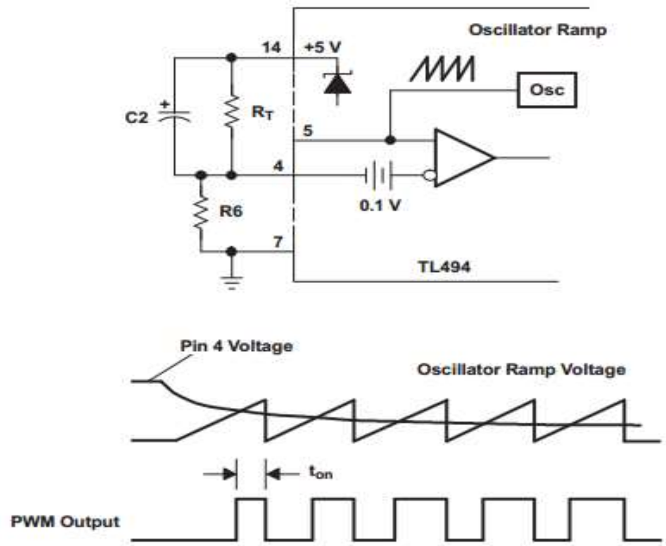


Figure 4.8: Soft-start circuits with TL 494 –PWM control circuit [56]

The Figure below, Figure 4.9, show that the timing diagram for the driving signal of MOSFET switches S_1 and S_2. During soft–start, at the beginning of the positive half cycle some fraction of millisecond is added before turning the switch S_2 ON. On the other hand, S_1 will turn-on after the soft–start at the beginning of negative half cycle. During the soft–start, when both MOSFETs are turn off, they behave like diodes and the soft–start is exactly the same as diode version of bridgeless totem – pole PFC converter.

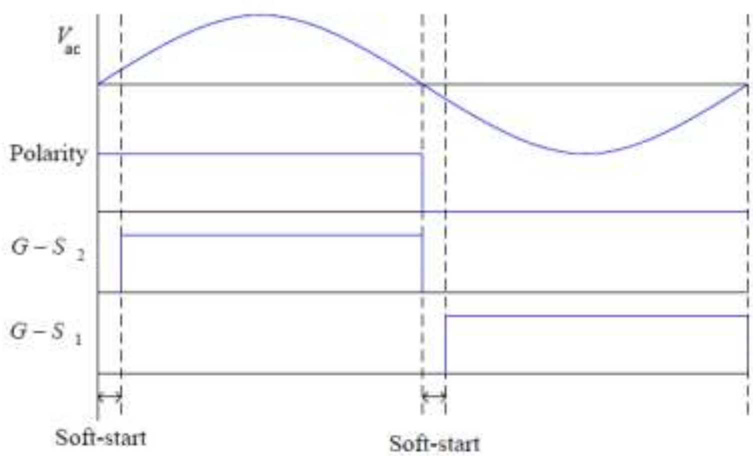


Figure 4.9: Timing of gate signals for two active MOSFET switches (S1 and S2)

5. Simulation-Based Study

Chapter 5 deals about simulation based study on totem-pole topology using GaN-HEMT, wide band gap devices. Moreover, it show some important parameters for the selection of components which can be used in the converter topology. The control strategy is also covered in this chapter.

5.1 Simulation set up

5.1.1 Selection of suitable simulation software

Different software can be used to simulate the proposed topology; Simulink or any spice software. In this thesis, it is decided to use LTspice IV and this is because is R&D power electronics specialists at Eltek AS recommended the software to work with. Therefore, LTspice IV is used as a simulation tool to simulate the totem – pole boost PFC converter topology using WBG devices, specifically GaN HEMT. LTspice is application software with good interface and user friendly. The software is developed by a semiconductor device manufacturing company known as linear technology (LTC). Since the simulation of switching regulators is made extremely fast compared to normal SPICE simulators, it allows the users to view the waveforms for most switching regulators in just a few milliseconds.

5.1.2 Component selection

Selection of components is the first and critical task before going to simulation work. Material property comparison for Si, SiC and GaN is illustrated in table 2.1 from chapter 2. These properties greatly influence on the performance of the devices and hence the application of these devices in different power converter is based on those properties.

As clearly seen from the table, GaN has very high electron mobility as compared to Si and SiC and it can ultimately be used when high frequency is desired from the converter. However, SiC is superior material property in terms of conducting heat efficiently due to its high heat conductivity and wide band gap nature.

This master thesis deals about low and medium power application, in the range of 1 kW to 4 kW, for telecom and data center application and then GaN HEMT is used for the simulation purpose and SiC is tested in the laboratory experiment. The proposed topology is supposed to provide power factor very close to one. The totem–pole PFC boost converter uses two different types of switching transistors are required; GaN HEMT transistors used as active boost switches and Si MOSFET switches serve as synchronous rectification. However, gallium nitride is very recent technology for power electronics application so that it is unable to find its model on LTspice IV software. MOSFET with some similar characteristics' to GaN HEMT are employed instead to perform the simulation. The components used in simulation and their part numbers are listed below:

- ✓ Two IXTH88N30P Si MOSFET models (S_1 and S_2).
- ✓ Two SPA11N60c3 MOSFETs to replace the action of GaN HEMT FET models (Q_1 and Q_2).
- ✓ 768775312WE-PD2 boost inductor (L_b).
- ✓ EEFUD0D331R dc link capacitor.
- ✓ A resistor as a load.
- ✓ Two LTC6702 comparators.
- ✓ Voltage source 230 V at 50 Hz.
- ✓ Control reference signal generator.
- ✓ Triangular wave signal generator.
- ✓ Logic Inverter.
- ✓ Universal opamp.

5.2 Converter Design

In the converter design phase, calculating and determining the values of the components are very important task and this can be done by considering the specification given for design and implement the converter. A totem-pole PFC boost converter with an input voltage of 230V AC at 50Hz line frequency and the output voltage of 400V DC with output power of 2kW. The boost inductor should operate in the CCM and its value is dependent on switching period, output voltage, duty cycle and output current of the converter.

$$L_b = \frac{T_s V_0}{2I_0} D(1 - D)^2 \qquad \text{[Eq. 5.1]}$$

The DC link capacitor is used to maintain the output voltage more or less constant across the load and it value can be determined by equation 5.2.

Parameters such as duty cycle, resistance of the load, output ripple, output voltage and switching period determine the value of the DC link capacitor.

$$C = \frac{T_S V_0 D}{R \triangle V_0} \qquad \text{[Eq. 5.2]}$$

The load current can be easily found by dividing the output power to the output voltage of the converter as shown below:

$$I_0 = \frac{P_0}{V_0} \qquad \text{[Eq. 5.3]}$$

The load resistor (R_l) also can be determined from the output power and output voltage value which is given as;

$$R_l = \frac{Vo^2}{P_0} \qquad \text{[Eq. 5.4]}$$

Calculating the component values and some important parameters will help to get good result from the simulation software and hence the analysis will be simpler to explain.

The topology is designed and implemented by taking the parameters in to consideration. In addition to these, the characteristics of the MOSFET switches and gate drive circuit are also the main focus in the design phase and the simulation circuit is found in appendix.

5.3 A novel bidirectional AC–DC converter with PFC boost

The LTspice IV model for the novel topology for bidirectional AC–DC converter is illustrated in Figure 5.1. The input is 230V AC at 50 Hz frequency and the output is 400V DC at 2kW output power and also the switches are arranged to enable bidirectional power flow with the help of drive control circuitry. PWM1 and PWM2 controls the switching time for Q1 and Q2 which are operating at 50 kHz whereas PWM3 and PWM4 controls the slow switches S1 and S2 at 50 Hz frequency. The two fast switches, Q1 and Q2, are n-channel MOSFETs manufactured by Infineon with V_{ds} = 650V, R_{ds}(on) = 0.34 Ω, Q_{gate} = 4.5e0.008. The simulation model for the topology is shown in Figure 5.1.

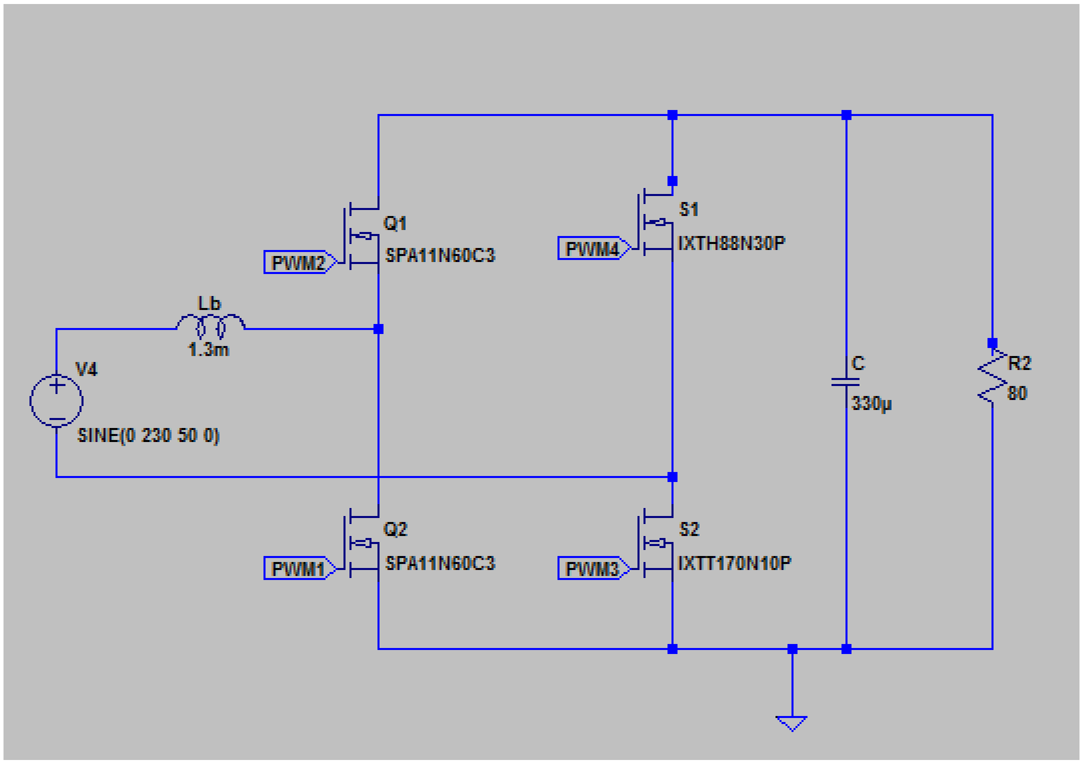


Figure 5.1: LTSpice IV model for totem-pole PFC boost converter topology

Note : The power supply symbol for voltage sources in LTspice is all DC but as it is shown in Figure 5.1 SINE (0 230 50 0) is to mean an AC voltage of 230V at 50 Hz frequency with DC offset and time delay both zero.

5.4 Gate drive circuit in LTspice IV

Power losses in a MOSFET can be either from conduction loss or switching loss. Conduction loss is occurred during the conduction or ON state of the MOSFET and dependent on R_{DS}(ON). On the other hand, switching loss can be experienced when the MOSFET is turn on or turn off and dependent on MOSFET switching speed which means how fast is the gate capacitances charged or discharged.

During selection of components, it is a smart idea to select a MOSFET with small R_{DS}(ON) and operate at optimum high switching speed so that a significant amount of reduction in power loss can be achieved. Figure 4.2 show the PWM waveform produced by comparing a reference control signal and a triangular wave. The switching frequency is given as:

$$f_{sw} = \frac{1}{T_{sw}} \qquad \text{[Eq. 5.5]}$$

Where T_{sw} - switching period = (2.64ms – 2.62ms) = 0.02ms and f_{sw} = 50 kHz

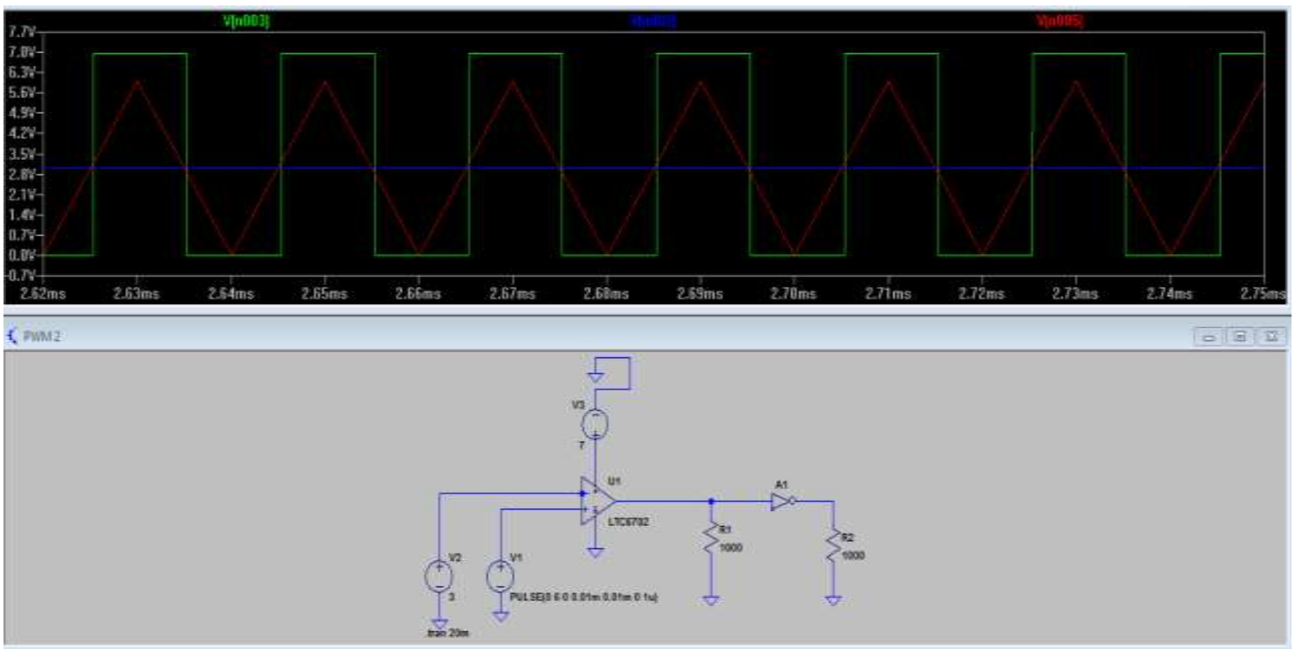


Figure 5.2: PWM generator with its output wave form on LTSpice IV

The complete gate driver circuit for the totem-pole PFC boost topology is shown in the Figure 5.3 and the generated gate driver signal is depicted in Figure 5.4. The gate driver circuit is designed to generate two different PWM signals one for fast switches at 50 kHz and the other for the slow switches at 50 Hz frequency.

The circuit compares control reference signal and triangular wave in order to generate the gate driver signal. The duty cycle of the gate driver signal depends on magnitude of $V_{control}$ and V_{tri} as it is given in the Equation 5.1.

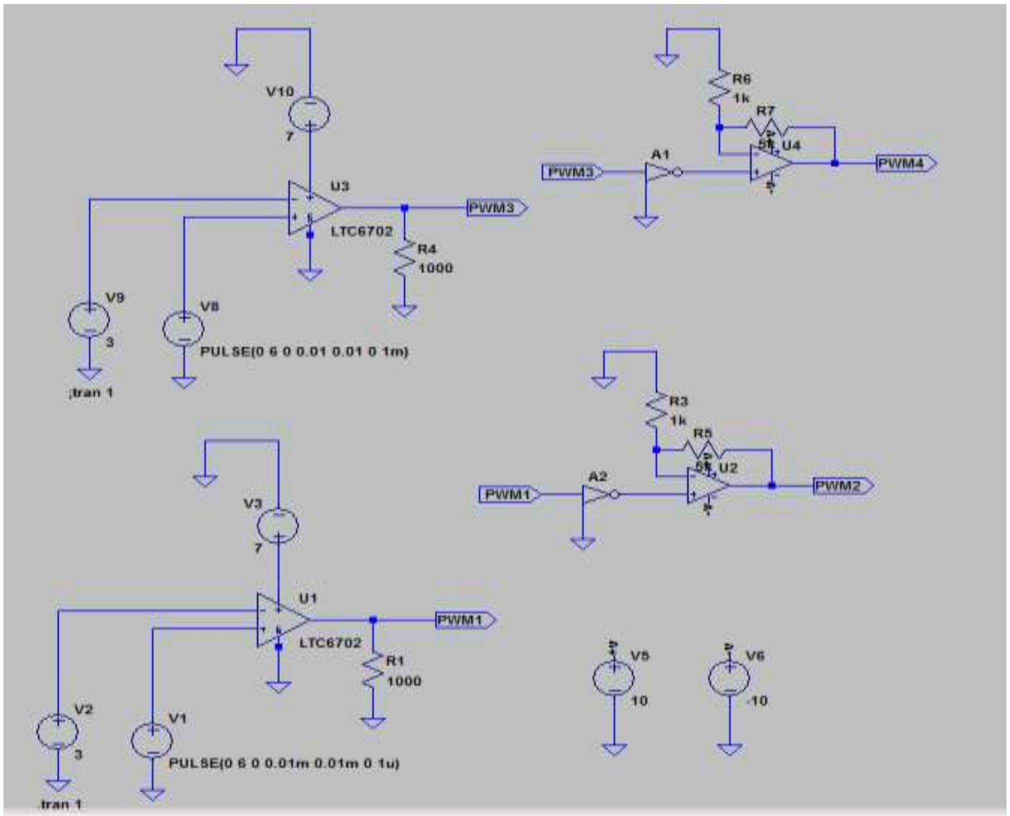


Figure 5.3: Gate driver circuit

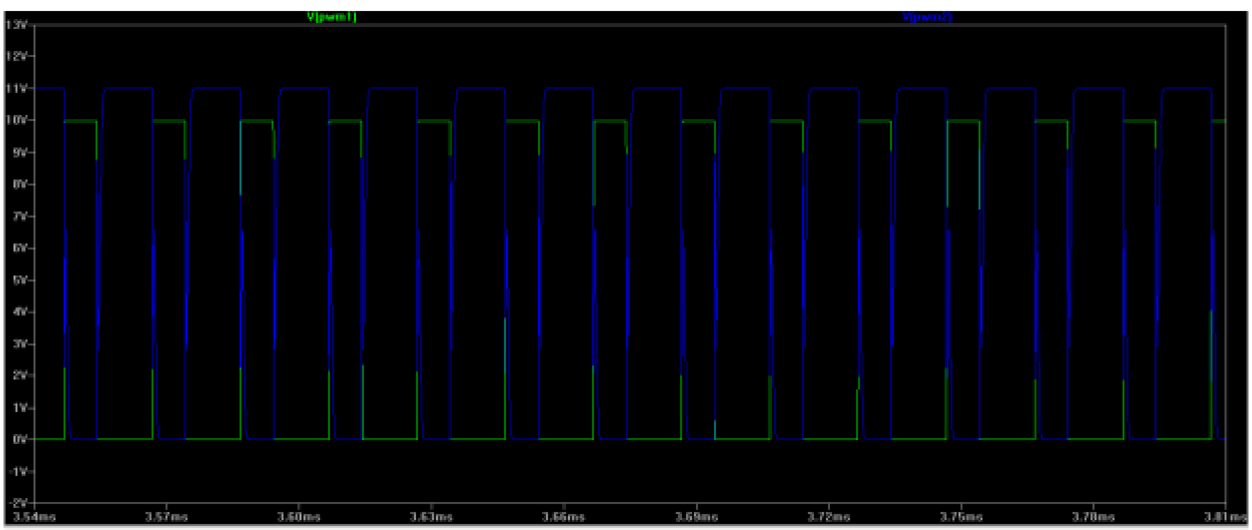


Figure 5.4: Gate driver signals for Q1 (PWM1 - green) and Q2 (PWM2 - blue)

5.5. Simulation results

The AC input voltage and the DC output voltage waveforms are shown in Figure 5.5 below. Properly designed filter and gate driver signals produce a good output waveform.

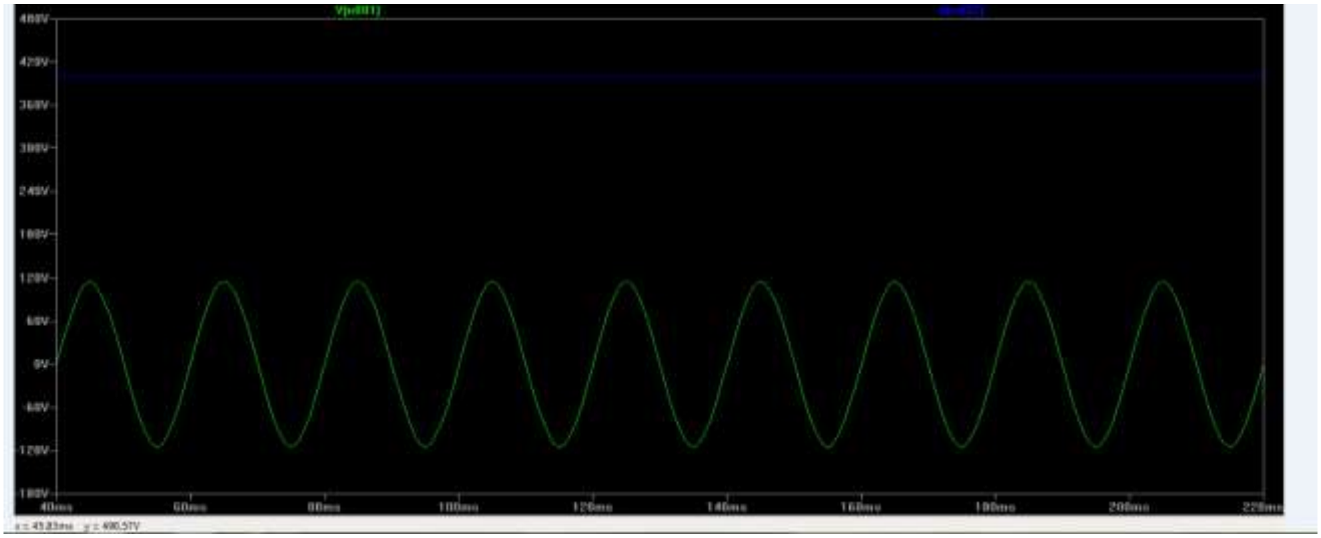


Figure 5.5: Waveform of 230V AC input (green) and 400V DC output (blue)

During the soft–start, when both MOSFETs are turn off, they behave like diodes and the soft-start is exactly the same as diode version of bridgeless totem – pole PFC converter. When the MOSFET takes over the load current from the free-wheeling diode of the opposite MOSFET during switch-on, the reverse recovery effect occurs when this diode blocks. Effect of dead time can be seen from the plot given below, Figure 5.6.

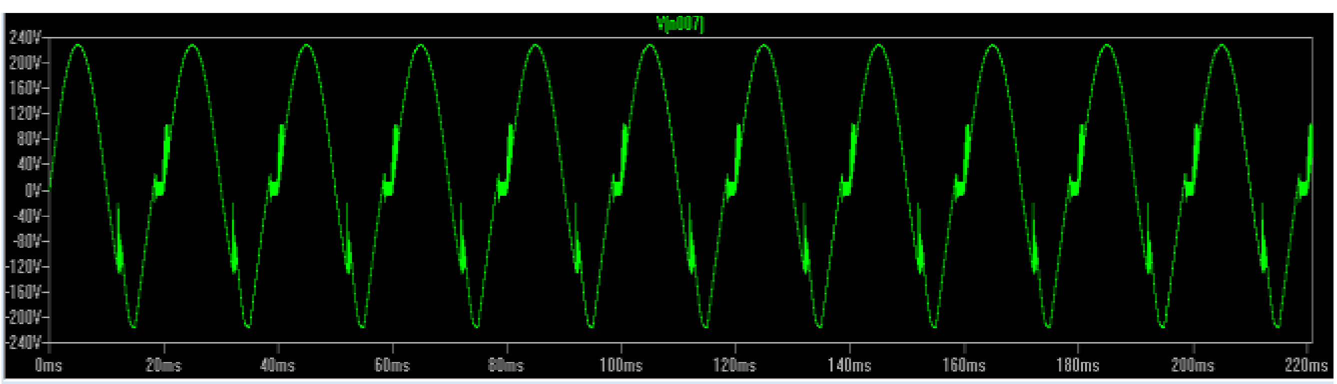


Figure 5.6: Effect of soft-start

The Figure below show the relationship between input current and input voltage waveforms. The PFC controller provides very close to unity input power factor by sensing the input voltage waveform and shaping the input current to be in phase with the line voltage.

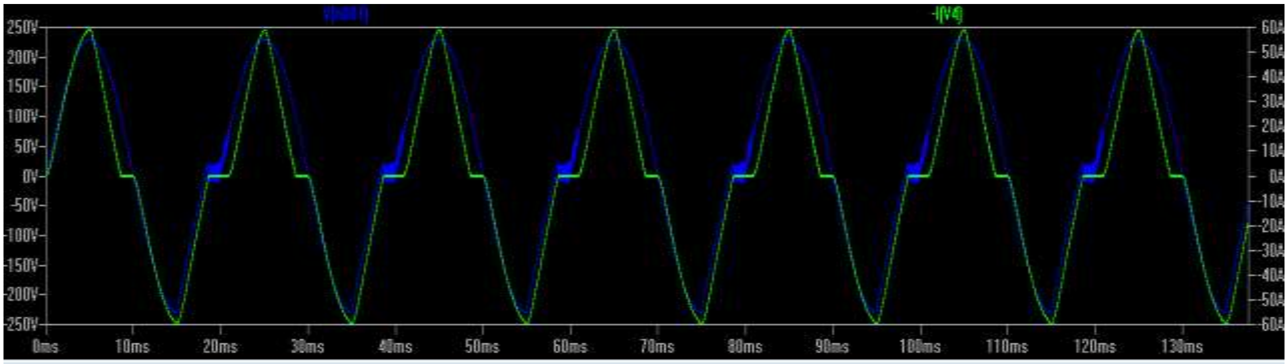


Figure 5.7: Wave form for input current (green) and input voltage (blue)

6. Laboratory Experiment Setup and Measurements'

In the previous chapter, the totem-pole PFC boost converter topology was realized based on GaN HEMTs using LTSpice software. In this chapter, laboratory experiment has been performed on the topology using SiC MOSFET switches. The following points are the focus of the chapter: component selection based on the specification of the topology, lab experiment setup, testing the prototype and make some important measurements.

6.1 Component selection

The selection of components for totem-pole PFC boost converter is made based on the specification in order to produce a prototype which can provide high efficiency and power density. In order to meet the specification, two major tasks are performed in this thesis. The first one is selection of low-loss switching devices and the other one is employing digital controller which incorporate dead time in the switching technique. WBG devices are supposed to provide the intended result from the converter. Material technology for GaN HEMT is not matured enough to be used in power electronics application this is due to the absence of freestanding substrate for GaN epitaxy and hence the technology is still in development phase. Therefore, this laboratory experiment is based on SiC MOSFET devices.

Table 7.1 Specification of the prototype single phase totem-pole PFC boost converter

AC voltage	230V, 50 Hz
DC voltage	400V
Power factor	Greater than 0.99
Output power	1 kW
Switching frequency	50 kHz
Power efficiency	Greater than 98%
Current harmonics	Within 3%, THD: within 5%

6.2 Power loss in Power MOSFETs

Efficiency of the power converter greatly depends on the losses in the switching devices. There are two kinds of losses related to semiconductor switches; conduction loss or on-state loss and switching loss. In low frequency applications, such as an automotive electronics, the on-state power loss is dominant so that an arbitrary large die area can be chosen in order to reduce on-resistance of the power MOSFET. However, high frequency application like switch mode power supply (SMPS) the switching loss has also significant impact on the efficiency of the converter. Therefore, it is very important to choose an optimal chip area to achieve minimum total power dissipation within the power MOSFET device [52].

At high frequency, significant amount of switching power losses comes from the charging and discharging of the large input capacitance in the power MOSFET devices. During each period of the operating cycle, the input capacitance (C_{in}) of the power MOSFET structure must be charged to the gate supply voltage (V_{GS}) when turning on the device and then discharged to zero volts when turning off the device. The energy loss during the turn-on and off event is given by

$$E_{on} = \frac{1}{2} C_{in} {V_{GS}}^2 \qquad \text{[Eq 6.1]}$$

The total power loss can be calculated by adding the two losses.

$$P_T = P_{ON} + P_{SW} = D\, R_{ON} {I_{ON}}^2 + C_{in} {V_{GS}}^2 f \qquad \text{[Eq 6.2]}$$

Where D is duty cycle, R_{ON} is the on-resistance of the power MOSFET structure, I_{ON} is the on-state current, and f is the operating frequency.

The on-resistance can be defined by,

$$R_{DS}\text{ (on)} = R_{Source} + R_{ch} + R_A + R_J + R_D + R_{sub} + R_{wcml} \qquad \text{[Eq 6.3]}$$

Where,

R_{Source} = Source diffusion resistance

R_{ch} = Channel resistance

R_A = Accumulation resistance

R_J = "JFET" component-resistance of the region between the two-body regions

R_D = Drift region resistance

R_{sub} = Substrate resistance

R_{wcml} = Sum of Bond Wire resistance, the Contact resistance between the source and drain metallization and lead frame contributions.

For power MOSFETs, a minimum total power loss occurs at optimal active area of the MOSFET structure. The minimum total power dissipated in the power MOSFET devices is given by;

$$P_T(min) = 2\, I_{ON} V_{GS} \sqrt{D f R_{ON,sp} C_{IN,SP}} \qquad \text{[Eq 6.4]}$$

As we can see from the above equation, the minimum total power dissipation in the power MOSFET device doubles when the switching frequency is quadrupled. Consequently, the ability to migrate to higher operating frequencies in power converter circuits is dependent on making enhancements to the power MOSFET technology. At higher operating frequency, large portion of the total power loss for power MOSFET comes from the switching losses associated with the drain current and voltage transitions.

The body diode of power MOSFET exhibits very slow reverse recovery with large reverse recovery current as shown in the Figure below.

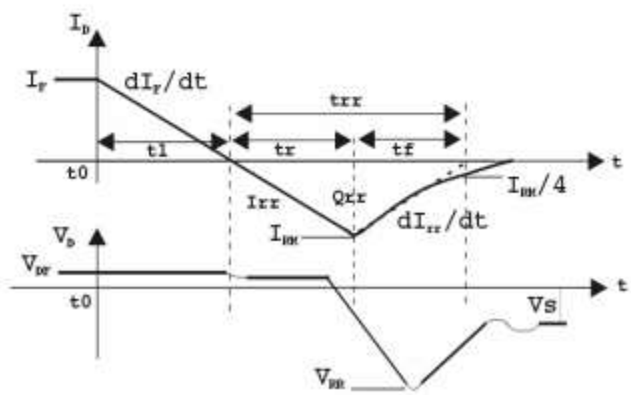


Figure 6.1: Typical reverse recovery waveform for body diode in power MOSFET [57]

The reverse recovery time can be given as: $t_{rr}= t_r + t_f$. This time is also referred as the storage time because it is the time required to clear away all excess charge, Q_{rr}.

6.3 SiC based Laboratory setup

6.3.1 Totem-pole topology using «C2M0160120D» SiC MOSFET

In the totem pole PFC boost topology, a pair of SiC MOSFETs is used as fast switches and another pair of slow but very low on-resistances Si MOSFETs for synchronous rectification are employed. Moreover, the proposed topology employs one input boost inductor and one output electrolytic capacitor. During testing the converter, a load is connected at the DC output side and measurements are taken. In addition, two schottky diodes are employed in order to bypass inrush current during start up.

Table 7.2 Component of the prototype

2 * IXFH50N20	N-Channel Enhancement Mode MOSFET
2 * C2M0160120D	SiC MOSFET from CREE
2 * IDW10G65C5	SiC Schottky diode
1.3 mH	Inductor with MPP core
470 µF	Electrolytic Capacitor

- **Characteristics of «C2M0160120D» SiC MOSFET (CREE)**

The data sheet of the component show that the device is N-channel enhancement mode MOSFET with the following features;

- ✓ High speed switching with low capacitance
- ✓ High blocking voltage with low $R_{DS\ (on)}$
- ✓ Easy to parallel and simple to drive
- ✓ Halogen free, RoHS compliant

Figure 6.2: Commercial available 1200V «C2M0160120D» SiC MOSFET from CREE

The device has superior performance over ordinary Si MOSFETs and it provides;

- ✓ Higher system efficiency
- ✓ Reduced cooling requirements
- ✓ Increased system switching frequency

The proposed topology is benefited from the unique characteristics of SiC MOSFET in terms of reduced heat sink size which in turn results in high power density PFC converter. Moreover, higher system efficiency also can be achieved by operating the device at high switching frequency.

6.3.2 *«CRD-001»* SiC isolated gate driver

CREE manufactures CRD-001 isolated gate driver for SiC MOSFET switches. The driver consists of two DC-DC converters (X2 and X3), an opto-isolator (U1) and gate driver integrated circuit (U2). The schematic diagram of the isolated gate driver is shown in the Figure below.

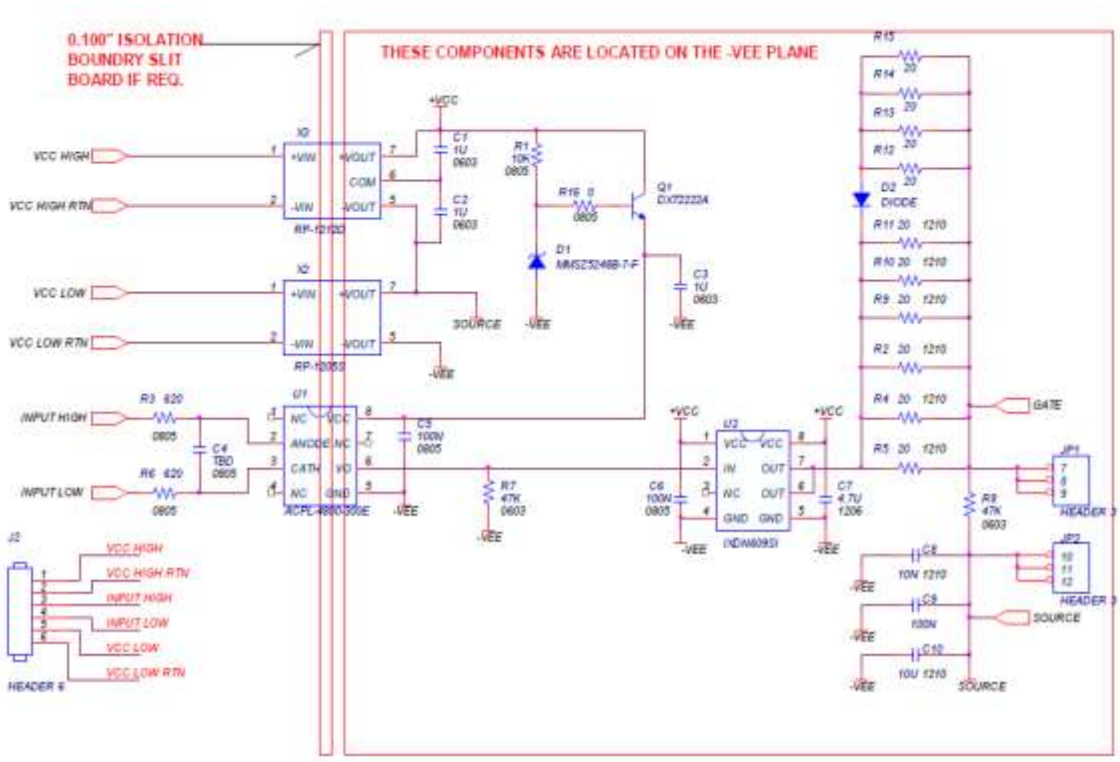


Figure 6.3: schematic diagram of CRD-001 SiC Isolated gate driver [CREE]

An isolated gate driver is suitable for testing and evaluating SiC MOSFETs in a variety of application. The top and bottom view of the gate driver is shown in Figure 6.4.

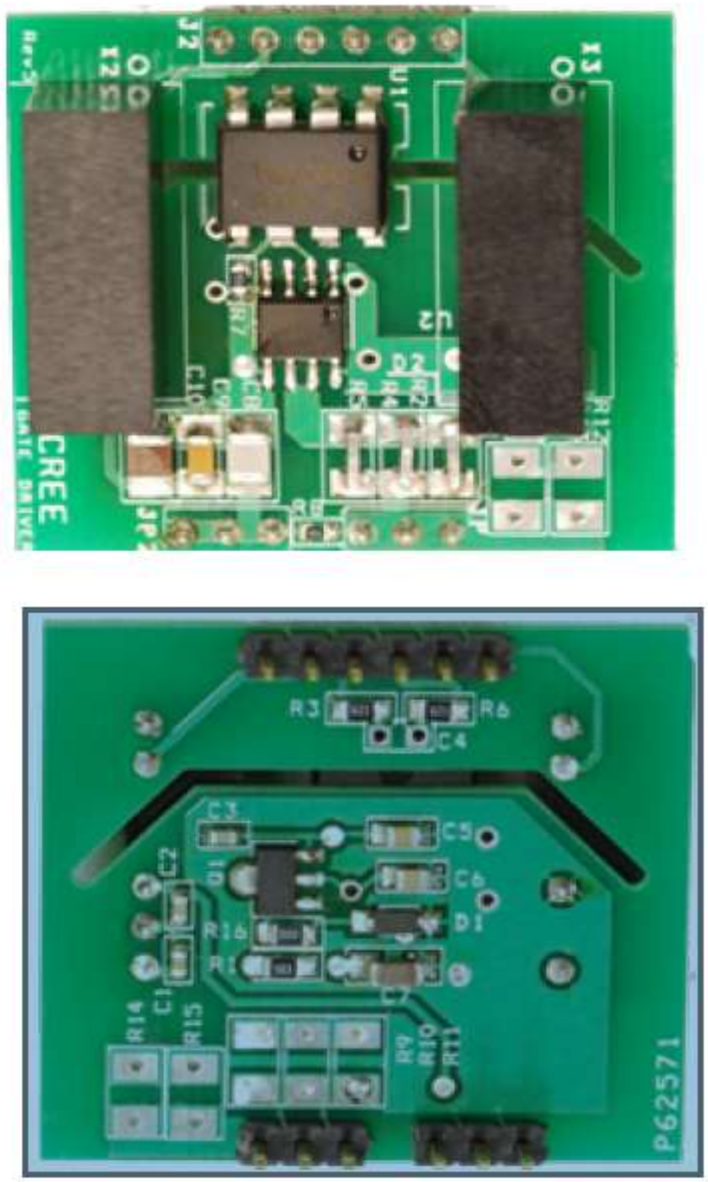


Figure 6.4: CRD-001 SiC MOSFET gate driver from CREE, Top view (upper) and Bottom view (lower)

The interconnection of the input and the output pins of the driver are shown below. The PWM signal at 50 kHz used to drive the gate of SiC switches Q1&Q2. The signal generator is connected to pin 3&4 of the driver to synthesize the required PWM signal.

To minimize stray inductance, capacitors C8-C10 are located very close to the source output pin and the gate driver to provide very tight coupling between the source output terminal and the –VEE node.

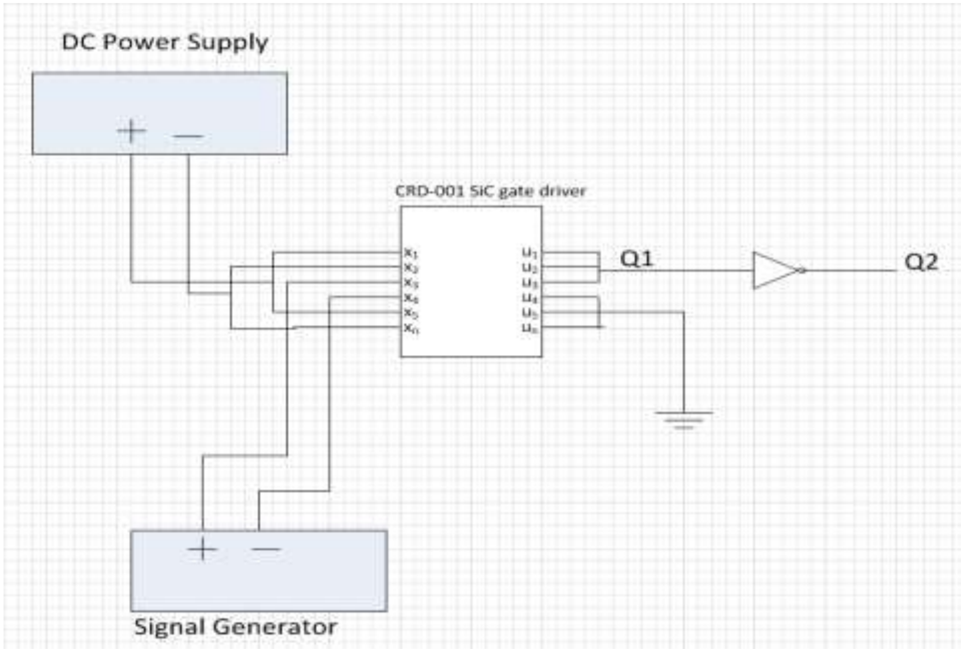


Figure 6.5: CRD-001driver pin interconnection and PWM signals for Q1&Q2

On the other hand, switches S1&S2 operate at 50Hz low frequency. Dead time should be added in the control circuit in order to make sure that the two switches are not switched ON or OFF at the same time. The circuit diagram of digital dead-time control is depicted in Figure 4.6, in chapter 4.

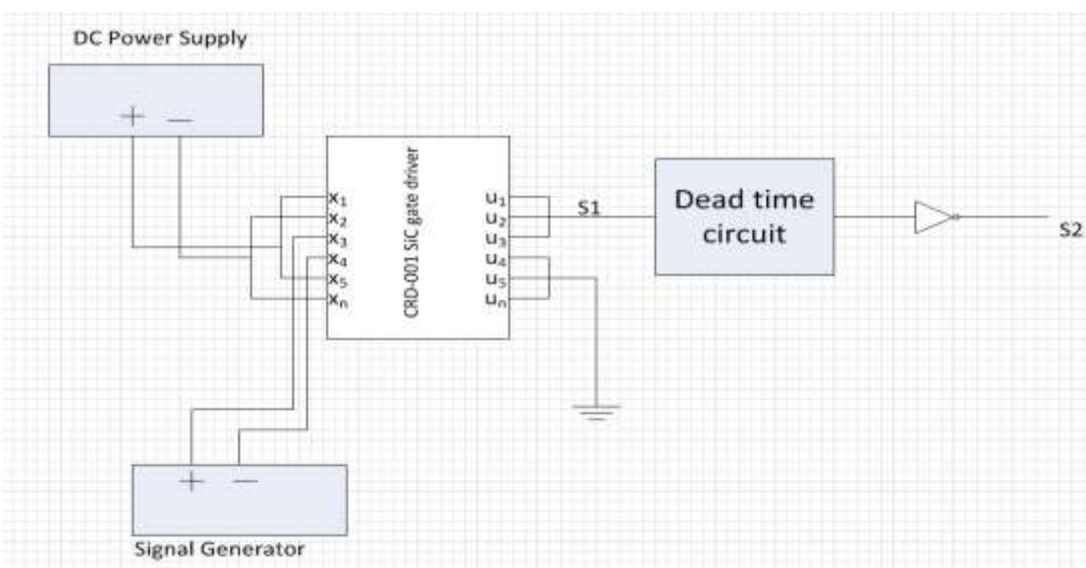


Figure 6.6: PWM signals for S1 and S2

During start-up, it might take some time to pre-charge bulk capacitor which can cause inrush current. Two additional SiC schottky diodes, D1 and D2, are added in front of the inductor, so that inrush current will flow through these diodes instead of SiC MOSFETs. Diodes D1 and D2 together with the body diode of S1 and S2 will form a bridge diode to charge up the capacitor and then Q1 and Q2 will actively switched to ramp up the DC bus voltage is established.

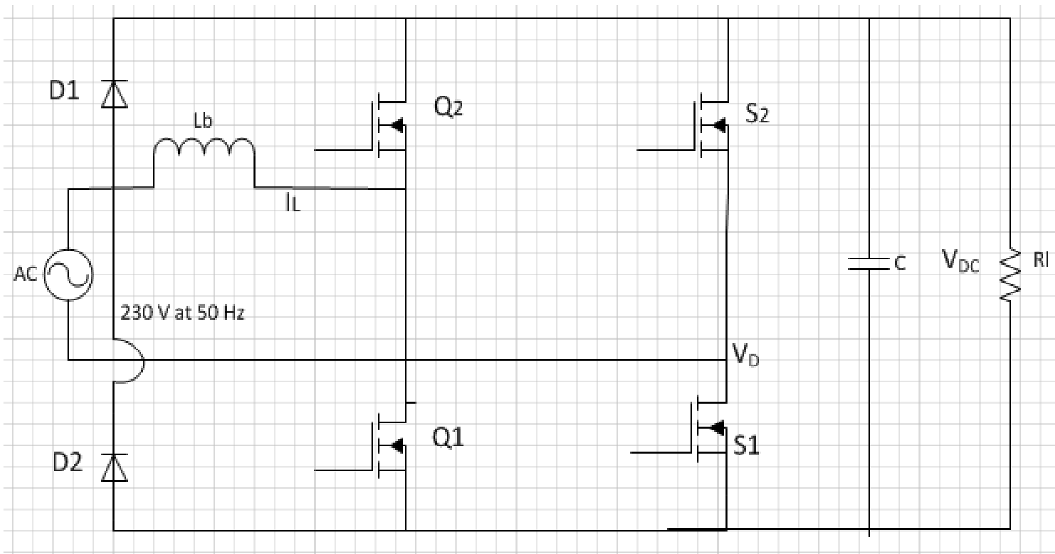


Figure 6.7: Diodes used to bypass inrush current during start-up

6.4 Prototype testing and measurements

The final part of the thesis work is producing a prototype based on the specification. CadSoft EAGEL PCB Design software is used to draw the board layout and the card is manufactured at NTNU workshop.

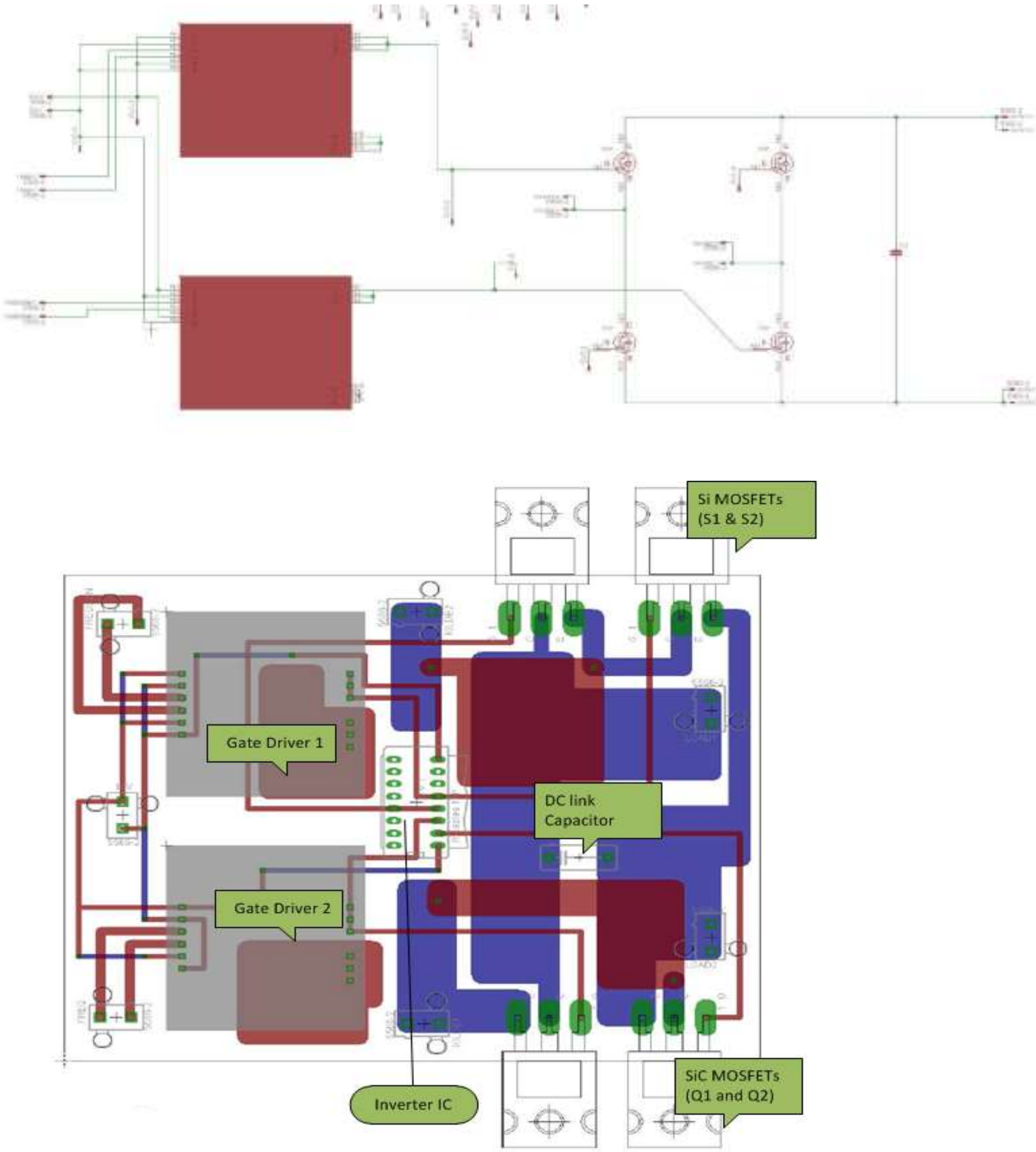


Figure 6.8: PCB schematic diagram and board layout of the prototype

The boost inductor is not indicated in the PCB layout. However, it is included in the actual prototype manufactured. Figure 6.9 show the picture of the actual prototype.

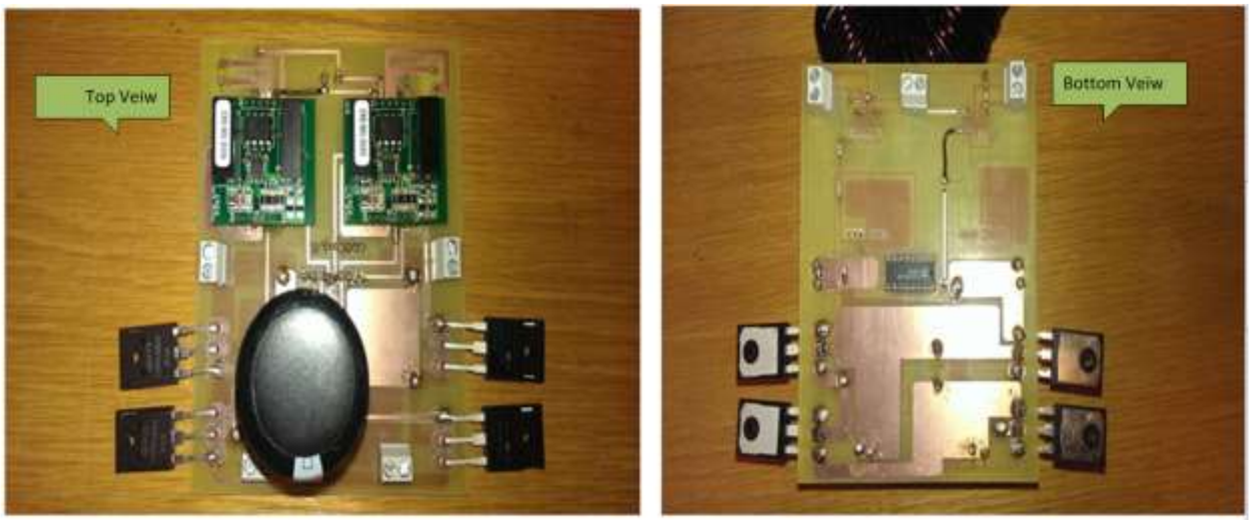


Figure 6.9: Top and Bottom view of the totem-pole PFC boost converter prototype

6.4.1 Heat sink design

Since power MOSFET has a limitation on the junction temperature (T_J), it should be operated below the maximum junction temperature (T_{JM}) which is specified on the data sheet to ensure reliability. The heat produced from the silicon and silicon carbide chip is typically dissipated by means of heat sink in to the ambient surroundings. The thermal system for a Power MOSFET with heat sink can be represented as a network thermal resistance and thermal capacitance as shown in Figure 6.10.

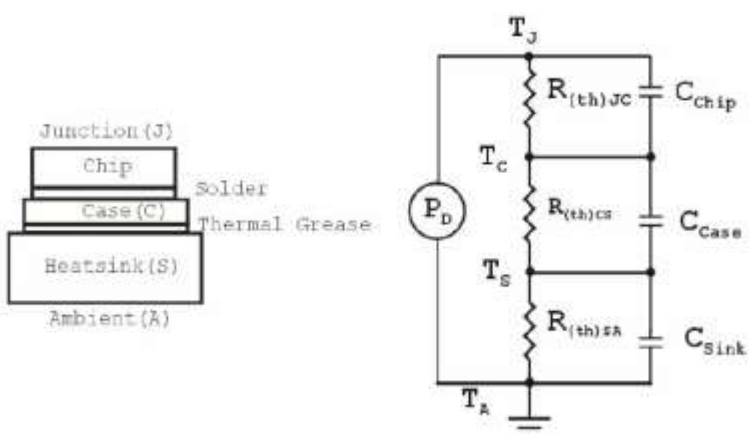


Figure 6.10: Power MOSFET chip thermal model with simplified heat sink system [57]

Heat flow and junction to ambient thermal resistance (R_{thJA}) are the determining factors for the rise in the junction temperature (T_J) above the ambient surrounding (T_A). The steady-state junction temperature can be defined by:

$$T_J = P_D\, R_{(th)JA} + T_A \leq T_{JM} \qquad \text{Eq. [6.5]}$$

Where; P_D = Maximum power dissipated in the junction.

$R_{(th)JA}$ is made up of two separate thermal resistances, $R_{(th)JC}$ and $R_{(th)CA}$. The value of $R_{(th)JC}$ is under the control of the manufacturer and typically low. On the other hand; $R_{(th)CA}$ can be further split in to $R_{(th)CS}$ and $R_{(th)SA}$ and hence the total thermal resistance between the junction and ambient is;

$$R_{(th)JA} = R_{(th)JC} + R_{(th)CS} + R_{(th)SA} \qquad \text{Eq. [6.6]}$$

Where;

$R_{(th)JA}$ – Thermal resistance between the junction and the ambient.

$R_{(th)JC}$ – Thermal resistance inside the device package, between the junction and its outside case.

$R_{(th)CA}$ – Thermal resistance between the case and the ambient.

$R_{(th)CS}$ – Thermal resistance of the interface compound used or thermal material.

$R_{(th)SA}$ – Thermal resistance of the heat sink (surface to ambient).

To calculate the thermal resistance required between the semiconductor junction and the ambient air the following expression can be applied:

$$R_{(th)JA} = \frac{(T_J - T_A)}{P_D} \qquad \text{Eq. [6.7]}$$

Where; T_J= Maximum Junction temperature, ^oC; T_A= Maximum ambient temperature, ^oC and

P_D = Maximum power dissipated in the junction.

It is a good idea to use a high thermal conductive material between the semiconductor device and the heat sink so that better mechanical contact at the interface and minimum total thermal resistance can be obtained.

Therefore, after determining the required resistance for the entire assembly and the resistance of the semiconductor and thermal material, then the thermal resistance of the heat sink can be calculated as;

$$R_{(th)SA} = R_{(th)JA} - R_{(th)JC} + R_{(th)CS} \qquad \text{Eq. [6.8]}$$

In order to get high power density from the prototype it is important to employ a heat sink with its size as small as possible. This is discussed briefly in chapter 7.

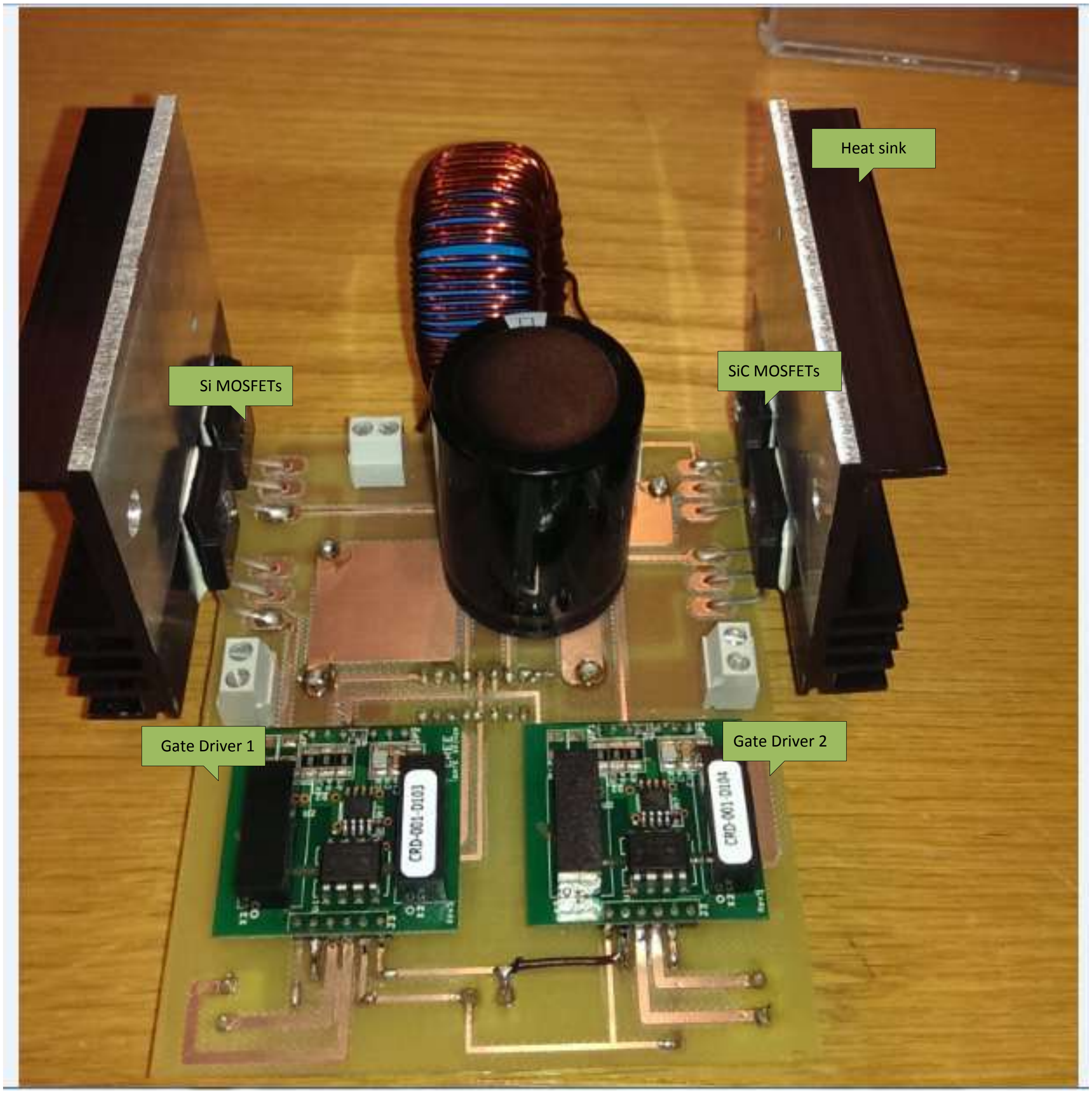


Figure 6.10: Prototype for the totem-pole PFC boost with heat sink

The picture for the whole interconnection of the prototype including the DC load is shown in the Appendix B, FigureB-2.

The totem-pole prototype with SiC MOSFETs is tested and some measurements are taken for the report. The waveforms of the input AC voltage and input AC current are almost in phase which means the converter provides better power factor correction, very close to unity.

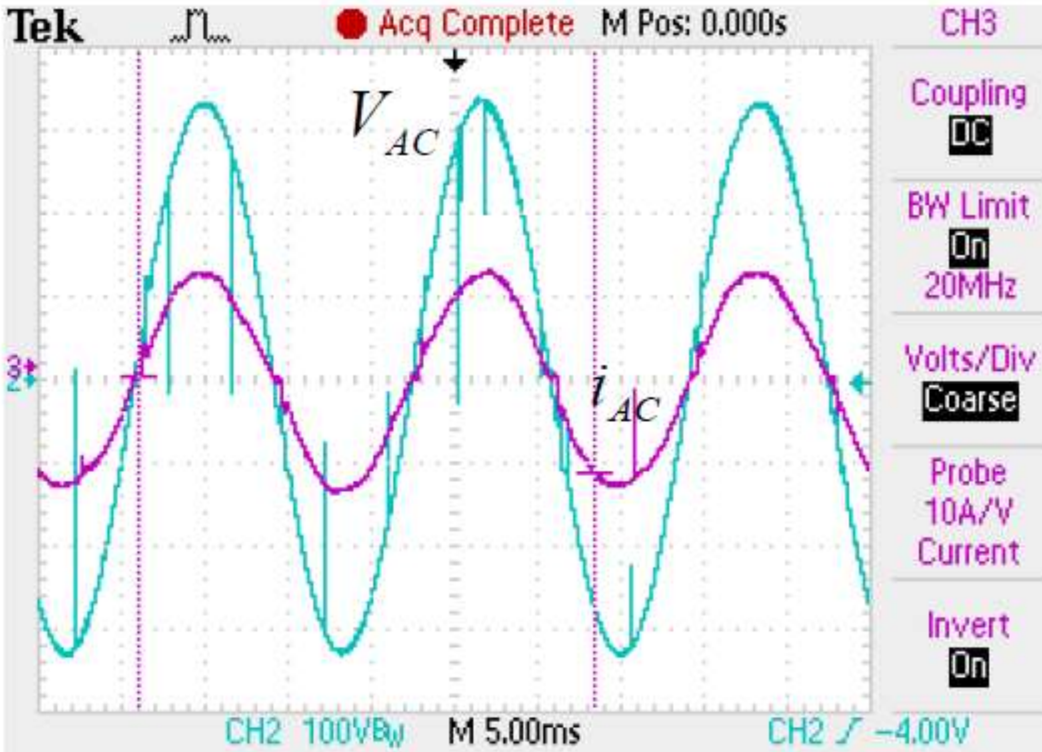


Figure 6.11: Waveform of SiC based totem-pole bridgeless PFC at full load 1kW. CH2: Input AC voltage(100V/division); CH3: input AC current (5A/division)

Figure 6.12 show four major waveforms: The PWM gate signal for one of low speed Si-MOSFET switches, S2. The switching frequency is 50 Hz from the gate driver. The second one is the current flow in the boost inductor. The size of the inductor is big enough to make the flow of current continuous. The one in green color show the polarity of the input voltage. The polarity of the input voltage is used to determine how the PWM signal is distributed between switches Q_1 and Q_2. The last one, with pink color, is the waveform for Voltage V_D.

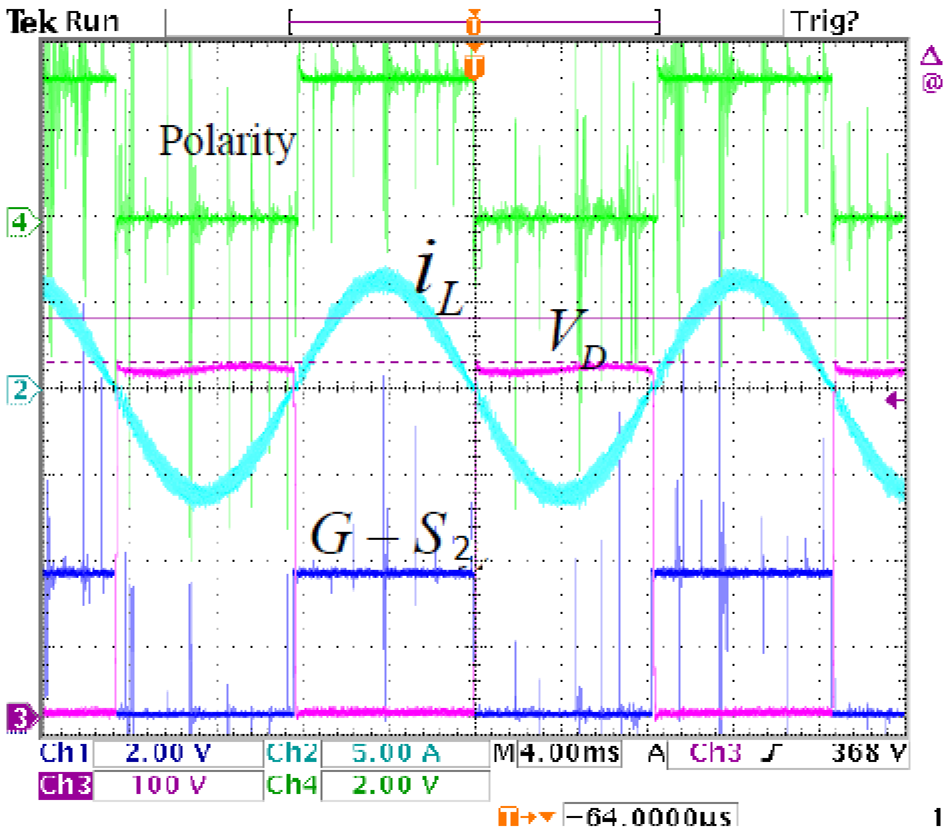


Figure 6.12: (a) CH1: PWM Gate signal for S2; CH2: IL waveform (5A/division); CH3: VD waveform (100V/division); CH4: AC input polarity signal

Soft-start concept is applied in the gate drive controller and gate signal for Si MOSFET switch S2 shown in the Figure below. In part (a), Soft-start gradually increases the voltage V_D from 0V to 400V. Whereas; part (b) show the gradual decease of voltage V_D from 400V to 0V. Zero-cross transition between two half cycles is depicted in the Figure 6.13. Switch S2 is turned on after the soft-start.

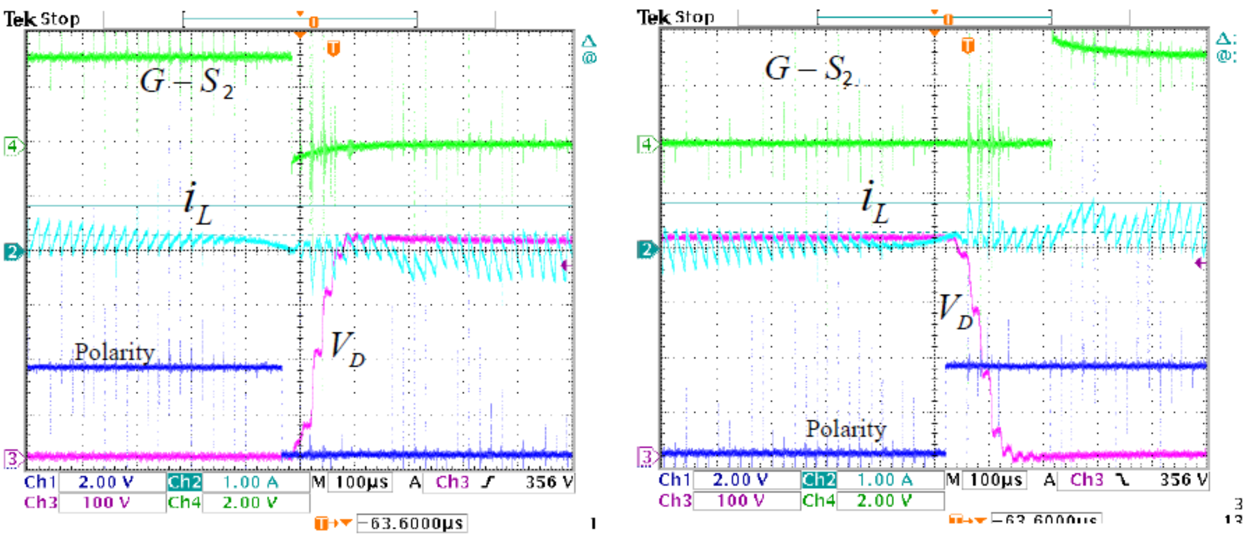


Figure 6.13: Zero-crossing transitional waveform (a) from positive to negative half cycle (b) from negative to positive half cycle CH1: AC input polarity; CH2: I_L waveform; CH3: V_D waveform; CH4: PWM gate for S2

7. Result and Discussion

This chapter focuses on analyzing the main findings from both computer simulation task and laboratory experiment of the totem-pole PFC boost converter using WBG devices. GaN semiconductor switch is used in the simulation part whereas; SiC is implemented and tested in the lab experiment.

7.1 Simulation based

The main objective of this thesis is to design and implement a novel bidirectional totem-pole PFC boost converter using WBG materials and devices. GaN-HEMTs and SiC are the two promising WBG devices for power converter applications and the focus of this paper in simulation and lab experiment respectively. The simulation results from GaN-HEMTs show that the converter can provide the desired output if the good substrate is used for the GaN epitaxy and proper design of the gate drive control circuit is employed.

Considering that the specialization project work is part of the master thesis and most of the simulation tasks are done in the specialization project phase. The findings were concentrated on design and implementation of the right topology on the software simulation; employing the WBG device in the topology, design the gate driver circuit, and then evaluate power factor correction and efficiency of the converter.

Theoretically, the topology provides high efficiency, approximately 98 %, for 2 kW PFC boost rectifier. However, the simulation result show the efficiency is a bit lower than what is expected from the theoretical value and this is due to lack of proper models for some components on LTspice IV simulation software such as GaN-HEMT switching device and also soft switching method is not employed in the gate driver circuit.

The efficiency of single phase totem–pole PFC boost topology is shown in the figure 7.1. From the graph, the highest efficiency is obtained when 400W output power is required from the converter and as the power output increases the efficiency decreases. On the other hand, the power loss is directly proportional to the power output.

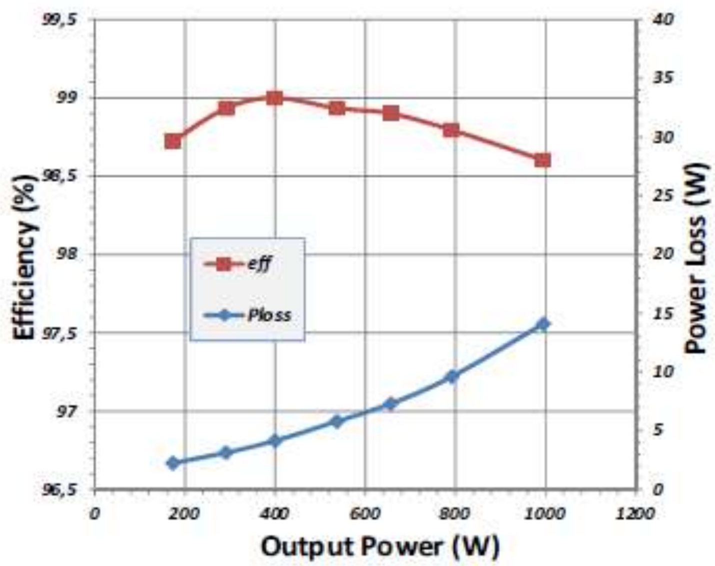


Figure 7.1: Measured efficiency for GaN totem – pole topology

The choice of the switching component significantly affects the overall performance of the totem–pole converter. Fast switching device, Q_1 and Q_2, can be made from silicon (Si), Silicon carbide (SiC) or gallium nitride (GaN) materials and the comparison of the materials is illustrated in the table 7.1.

Table 7.1 Comparison of components for high speed switching devices (Q1 and Q2)

Device	Dissipation on Body diode	Breakdown voltage (V)	Usage	Reliability	Driving requirement capacitances	High frequency suitability	Driving voltage
Si	High	500 - 900	Not used	OK	High	Not good	-
SiC	Medium	900	L–L,400V	-	Medium	Good	Need 20V
GaN	Low	650	L–N,230V	OK	Low	Excellent	Need negative voltage

From the property of the devices, GaN HEMT can provide the highest efficiency, compared to Si and SiC, when it is used as fast switching device in totem–pole topology. This is due to low on-resistance and low recovery charge of the device. Since the library of LTSpice doesn't contain the model for newly invented GaN-HEMT, n- channel MOSFETs are used instead by adjusting to properties of GaN devices.

The gate driver circuit is designed to generate four different signals each to drive the four gates of the switches. Q_1 and Q_2 are considered to operate at very high frequency and when one of the switches is ON the other should go OFF. On the other hand, the two slow switches serve as synchronous rectifiers and operate at 50 Hz switching frequency. Similar to the fast switches, S_1 and S_2 should turn ON and OFF in different time slots and not at the same time.

The biasing voltage of the comparator greatly affects the magnitude of the PWM signal and hence the signal level that drives the gate of the MOSFET. Even though the inverter and opamp combination in the gate drive circuit doesn't give satisfactory output signal, the generated PWM signal can drive the gate of the MOSFETs. From the first simulation, the output voltage waveform was not good enough to use as a gate drive signal. However, some changes have been made on the gate drive circuitry to get a better output voltage waveform which is illustrated in Figure 5.5 in chapter 5. Figure 7.2 show the voltage output waveform does not reach its stability during start-up which means it takes some time to get 400 V constant output voltage.

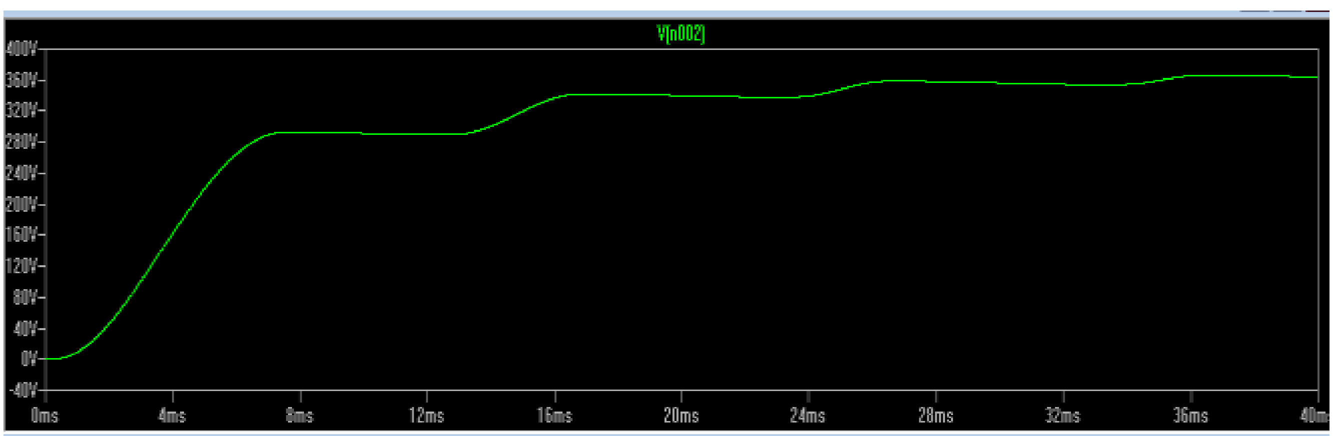


Figure 7.2: Output voltage waveform during start-up

The polarity determines how the PWM signal is distributed to drive Q_1 & Q_2. A soft-start sequence with a duty ratio ramps is employed for a short-period at each AC zero crossing for better stability. During buck operation, the power flows from the DC link side to the AC side and the output waveform should be pure AC at 50 Hz before it is fed back to the grid.

7.2 Experiment based

Since producing a compact and high efficiency power converter saves a lot of space in the rack and energy cost, the demand towards wide band gap semiconductor devices increase for power converter application in modern data center and telecom power systems. In this section, the experimental results are discussed based on SiC totem-pole PFC boost converter.

7.2.1 Effect of parasitic elements

Parasitic elements always exist and it is almost impossible to avoid them in electrical circuits. All conductors possess resistance and inductance and hence there will also be capacitance which is undesirable. A lot of effort has been put to minimize parasitic elements in electrical circuits but it is almost impossible to completely eliminate them.

Stability and voltage conversion ratio of the boost converter are greatly influenced by parasitic elements [1]. They are mainly caused by the losses associated with the inductor, capacitor, switches and diodes used in the converter. Even though it is difficult to eliminate parasitic elements from electrical circuits, it is possible to decrease their effect by placing the gate drive circuit much close to the power switch and this can improve the performance of the converter by reducing the parasitic inductances associated with long wire.

7.2.2 Discussion on measurements

1 kW prototype has been built in order to evaluate the performance of the proposed converter using SiC semiconductor device. The laboratory experiment setup is shown in Figure B-1 and Figure B-2, in the Appendix. Moreover, the waveforms of the test result are depicted in the last section of Chapter 6.

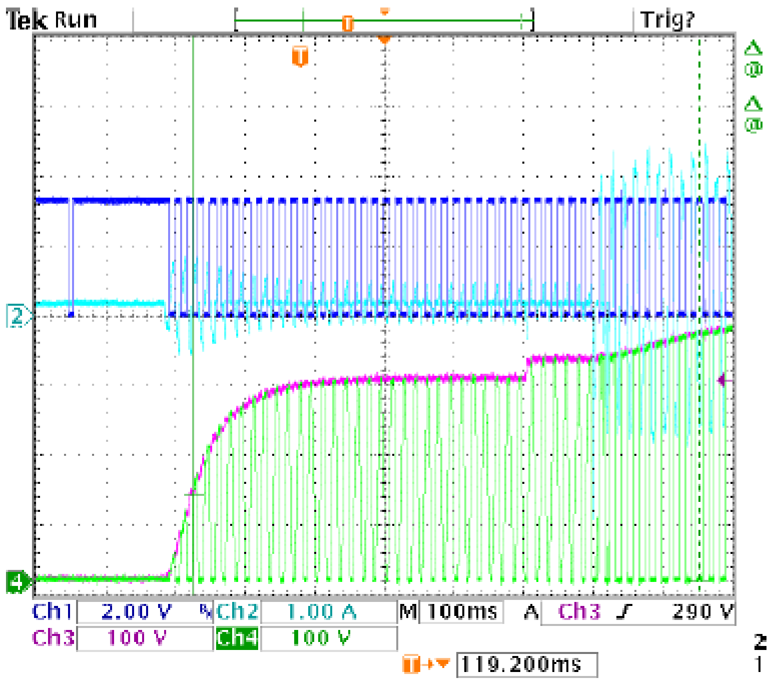


Figure 7.3: Start-up of the totem-pole PFC prototype (CH1: AC Polarity, CH2: Inductor current, CH3: Output voltage (VO), CH4: VD)

As it is shown in Figure 7.3 CH3 with pink color, laboratory result of the output voltage at start-up of the totem-pole topology using SiC MOSFET switches has similar waveform with the simulation result (in Figure 7.2) using GaN devices. In both cases, the DC output voltage will rises gradually from 0V to 400V. Meanwhile, the inductor current will stay at 1A during start-up period.

7.2.2.1 Efficiency

The main idea of soft switching is to prevent or minimize the overlap between the voltage and current so that the switching loss is minimal. SiC based totem-pole converter provides higher efficiency by introducing soft-switching technique even though implementing ZVS incurs complexity of the gate driver circuit and additional cost. On the other hand, GaN-HEMT based totem-pole topology can also give higher efficiency with hard switching technique when good free-standing substrate is able to manufacture for GaN epitaxy for power system application. This has been shown from LTSpiece simulation result.

Due to its high thermal conductivity property of SiC MOSFETs, the size of the heat sink can be reduced so that much weight and space can be saved. This reduced size of the heat sink comes with the expense of a slight decrease in the efficiency of totem-pole converter.

7.2.2.2 Power Factor

The purpose of the power factor correction circuit is to minimize the input current waveform distortion and make it in phase with the voltage. Figure 6.11 show the waveform of input voltage and input current of 1 kW SiC totem-pole prototype at full load. The test result show the proposed converter can provide very close to unity power factor (greater than 0.99) and very low harmonic distortion. The power factor can be calculated as:

$$\mathrm{PF} = \frac{P}{S} = \frac{\frac{1}{T}\int_0^T V_i\,(t)\;\; i_t(t)\mathrm{dt}}{V_{i(eff)}\, I_{i(eff)}} \qquad \text{Eq [7.1]}$$

High power factor has the following benefits:

- Reduce the distortion of voltage waveform.
- Reactive power becomes negligible, all the power is active.
- The rms value of the current is smaller.
- Increase in number of loads that can be fed from the same source.

7.2.2.3 Power Density

The volumetric power density is the relation between the converter power transfer and its volume.

$$\mathrm{VPD} = \frac{\mathrm{P_{out}}}{\mathrm{Volume}} \qquad \text{Eq [7.2]}$$

Where:

VDP -Volumetric power density

P_{out} - Output power

Volume - Converter volume

As it is given in Equation [7.2], output power and volume of the converter are important parameters in order to determine the power density of the converter. The power output of the converter is known during the design phase of the topology. Whereas; volume of the converter includes both the volume of the heat sink and the components' size in the topology and it requires calculating the volume of the heat sink. However, it is very challenging to calculate the heat sink size analytically since heat sinks comes in a wide variety of shapes, which makes it difficult to tie their thermal resistance to their volume or weight. Therefore, the size of the heat sink is somehow estimated using a concept called cooling system performance index (CSPI). It is given as follows:

$$\mathrm{Vol}_{\mathrm{heat}} = \frac{1}{\mathrm{R}_{\mathrm{th(SA)}} * \mathrm{CSPI}} \qquad \text{Eq [7.3]}$$

Where:

$\mathrm{Vol}_{\mathrm{heat}}$ – Volume of the heat sink

$R_{th(SA)}$ - the surface-to-ambient thermal resistance

CSPI – is determined from datasheet

Higher CSPI means higher power density for the converter. Since SiC semiconductor has high CSPI, it provides higher power density for the totem-pole PFC boost converter.

7.2.2.4 Cost Analysis

Cost of the converter is an important objective function in many of the designs. In fact, high-production costs may be a barrier for using some technologies, which are desirable for certain applications.

It is very important to optimize the performance converter with its cost. Type of semiconductor devices used and number of components incorporated in the converter greatly affect the cost of the converter. The number of components, in totem-pole PFC boost converter, is very few as compared to other type of PFC converter topologies.

The cost of wide band gap materials and devices is 3 to 5 times higher than silicon semiconductor devices. WBG materials contribute about 40 % of the total device depending on availability, quality and performance. Moreover, device design, fabrication and packaging are also key factors to higher costs.

GaN on SiC wafers cost about 20% more than their SiC on SiC counterparts. GaN on silicon wafers promise to be substantially lower cost than either the SiC on SiC or GaN on SiC wafers leading to a great deal of current interest in this combination.

8. Conclusion and Further Work

In this chapter, conclusion of the master thesis is presented and future work on the topic is also proposed.

8.1 Conclusion

Improving the quality of input current to the mains is important in order to meet some forcing standards, such as IEC 61000-3-2 and IEEE 519. Poor quality of input current significantly affects the power factor of the input power and the problem is alleviated by employing PFC circuit as a front- end in a single phase or three phase AC–DC converter. Active PFC technique which operates in CCM is used to achieve better power factor from the converter. Boost type is preferred to reduce EMI as compared to other types of active PFC.

In this master thesis work, two major tasks has been done in addition to literature study on PFC topologies and design of gate drive circuit. Performance of totem-pole topology was evaluated using GaN semiconductor devices on computer simulation software and laboratory experiment is carried out by employing SiC devices.

PFC boost converter can be implemented either by using single stage approach or two stage approach. In spite of its complexity and additional controller in two stage approach, PFC controller in single phase AC–DC bidirectional converter provides better power factor and the DC-DC controller gives higher efficiency than single stage approach. EMI from this novel topology is another problem considered in the thesis work and its major source is switching noise from the MOSFETs. Therefore, some alteration should be made of the conventional topology in order to reduce EMI from its source and that might be much less costly than adding LC filter later to minimize the interference level. During the design phase of the converter topology, it should be considered to optimize the performance of the converter with lower cost.

Even though most of the literatures regarding PFC converter focus on unidirectional power flow, some researches have been made on bidirectional PFC boost converter and this thesis is done based on totem–pole bidirectional topology. The main focus of this paper is realization of ultra-compact and ultra-efficient converter modules employing latest power semiconductor technology, GaN and SiC.

The advent of GaN HEMT is supposed to move the performance of the converter one step forward. Even though GaN HEMTs are already used in opto-electronics application, the device is not matured to employ in power electronics area due to cost and free standing substrate. And hence its performance for PFC totem-pole converter is limited in computer simulation stage. In this thesis, LTSpice IV simulation software from Linear Technology (LT) is used to evaluate and analyze the performance of GaN in totem-pole topology.

Two key issues are considered in order to produce a high density PWM converter. The first one is the use of ultra-low loss semiconductor power devices, such as SiC, to downsize the heat sink. The other one is regarding switching frequency of the converter. The gate driver operates at high frequency in order to minimize the passive components' volume.

The gate drive controller produces a signal that is sufficient to drive the gate of the MOSFETs. Nevertheless, the waveform of the generated signal after pass through the amplifier is not as perfect as before it is being amplified. To avoid the problem, an operational amplifier with non-inverting input is used and better result is achieved. In the laboratory work, the inverter is replaced by an IC in the prototype.

Moreover, a scientific study is performed to improve the efficiency of the totem–pole bidirectional topology and from the result it can be deduce that synchronous rectification using active semiconductor switches like MOSFET provide high efficiency as compared to employing power diodes due to reduced reverse recovery dissipation in the power MOSFET. A 1 kW PFC boost rectifier prototype is tested to analyze the study.

The volume of the heat sink for SiC based totem-pole topology is very small and this is the result of high temperature difference between the ambient temperature and the junction temperature of the SiC, that is high CSPI. Therefore, high power density PFC converter can be obtained from SiC semiconductor.

The converter also has the following features:

- Low conduction loss due to synchronous rectification.
- Low switching loss due to low reverse recovery charge of SiC MOSFET
- ZVS over the complete mains period.
- Minimum heat sink size due to high thermal conductivity nature of SiC MOSFET.
- Low CM noise.

- Bidirectional operation.

From both simulation and laboratory experiment results, this conclusion has been given:

- GaN HEMTs are best to use if the efficiency of the converter is the critical issue.
- SiC, on the other hand, can be a first choice when high power density is required.

8.2 Further Work

In this thesis work, a lot of tasks have been done such as Literature review on different types of PFC converters topologies, study of semiconductor material properties, design of the gate driver circuit, design and implementation of the proposed topology. Moreover, both simulation and laboratory based tasks have been performed on the totem-pole PFC boost converter using GaN-HEMTs and SiC. However, the thesis has some limitation which can be done in the future. The following topics may be of immediate interest.

- ✓ Testing the prototype with a high quality free standing substrate GaN devices in order to operate the converter at high switching frequency.
- ✓ The gate driver circuit needs some alteration so that it enables to control both voltage and frequency at the same time.
- ✓ Study the impact of running frequency and voltage controllers simultaneously on the performance DC link capacitor and battery status.

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Appendix

Appendix A: LTspice IV Simulation circuit and waveforms

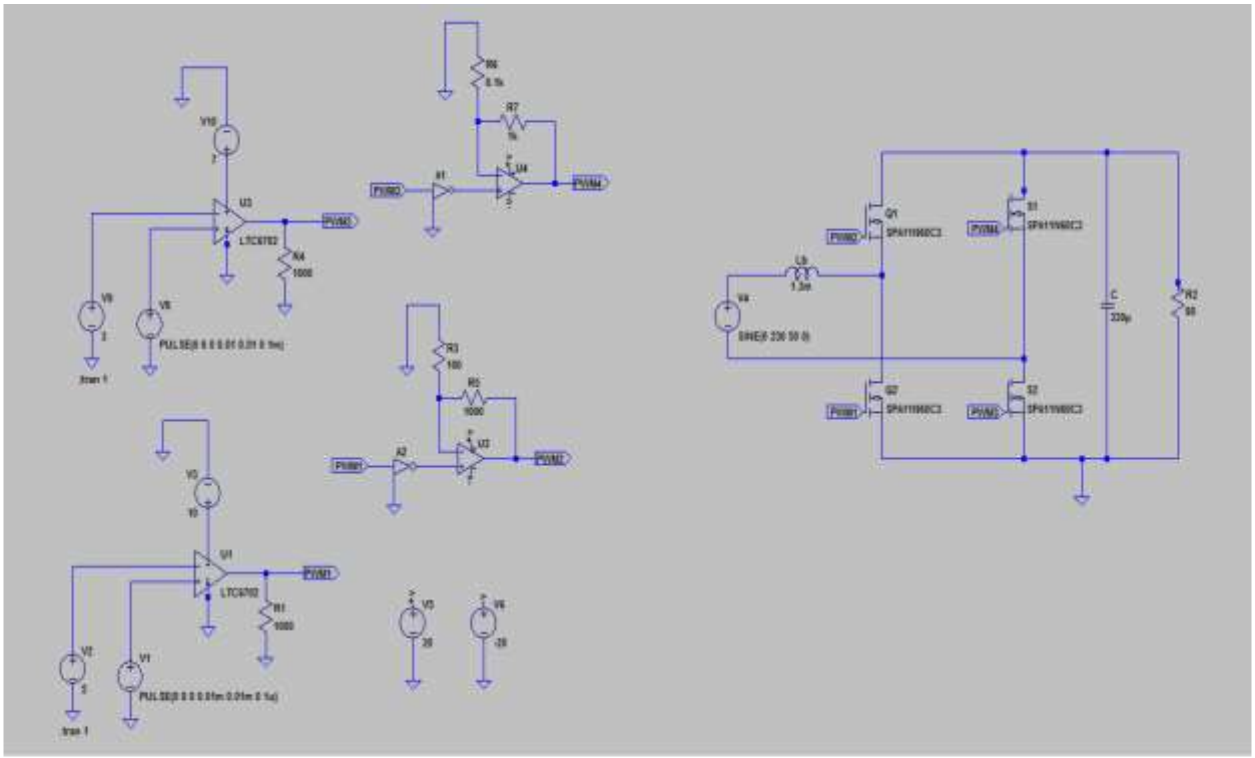


Figure A-1 Over all converter schematic

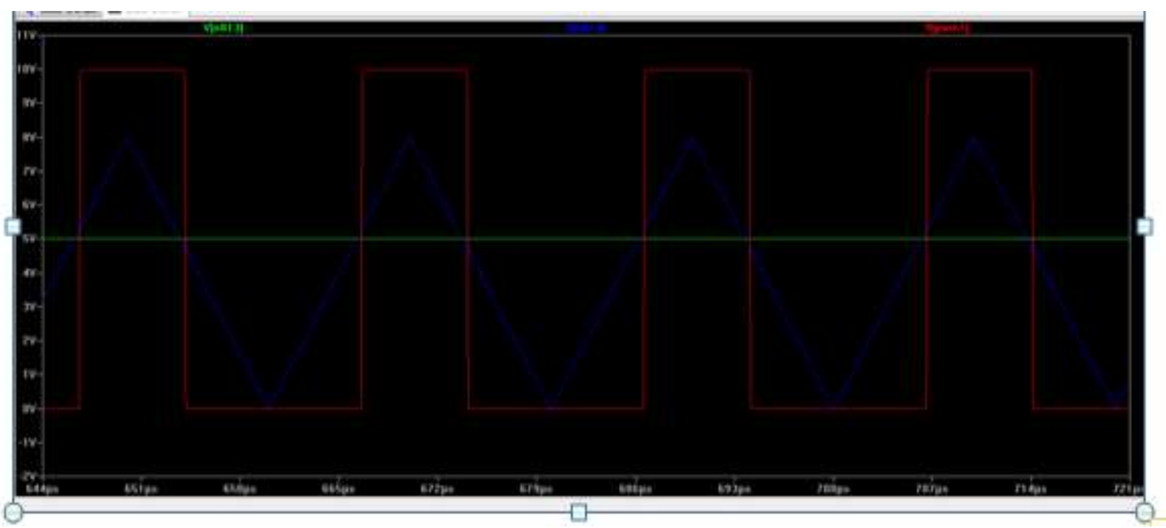


Figure A-2 PWM waveform

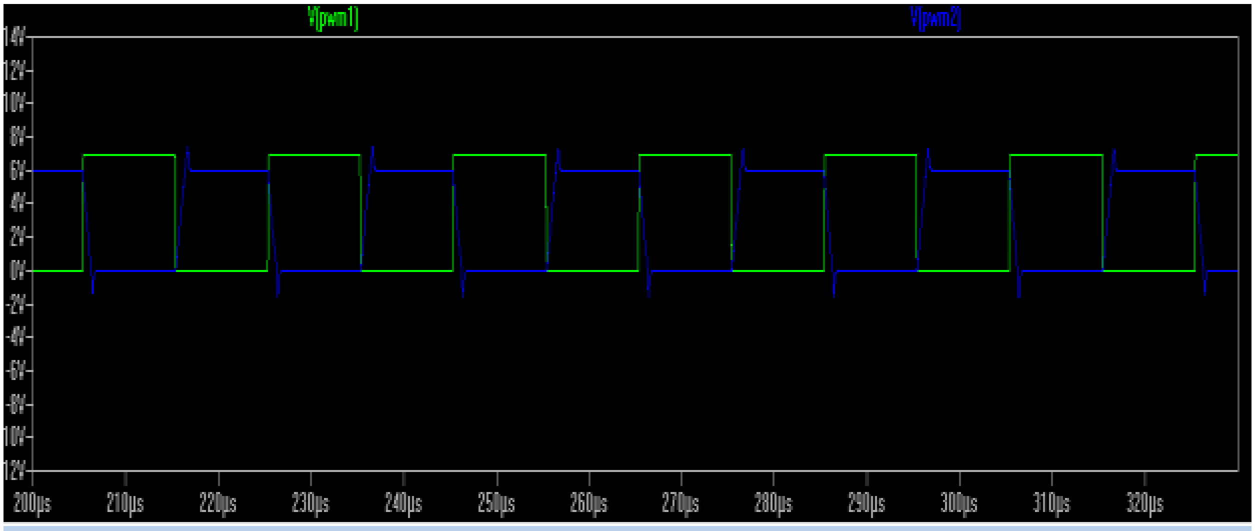


Figure A-3 Gate drive waveform for Q_1 and Q_2

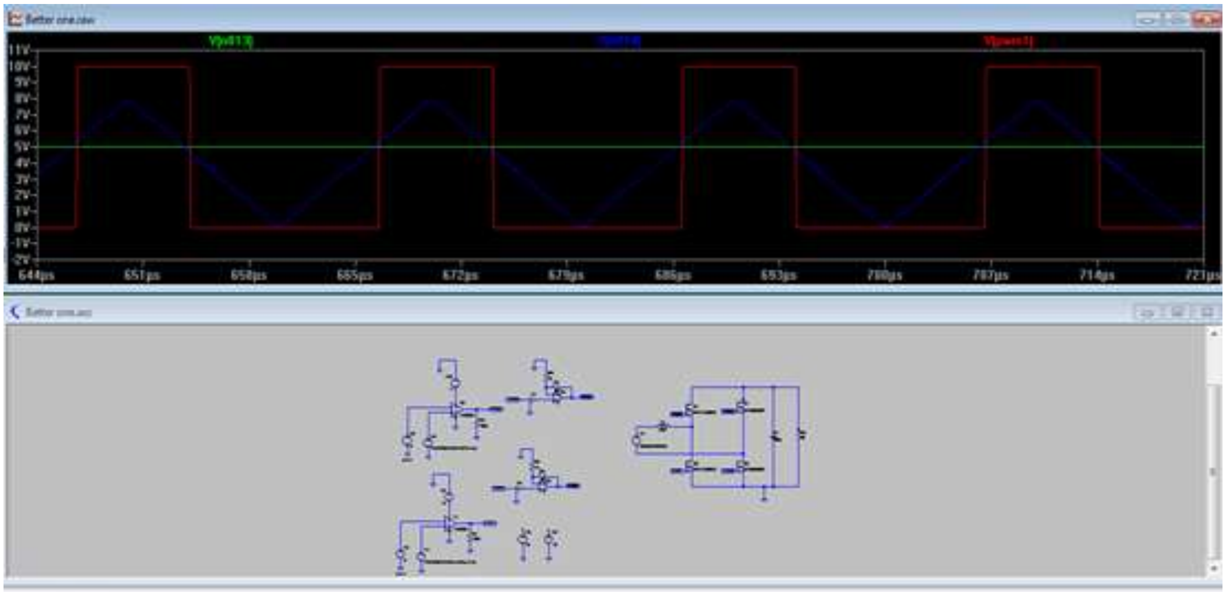


Figure A-4 Gate drive circuit and its output PWM waveform

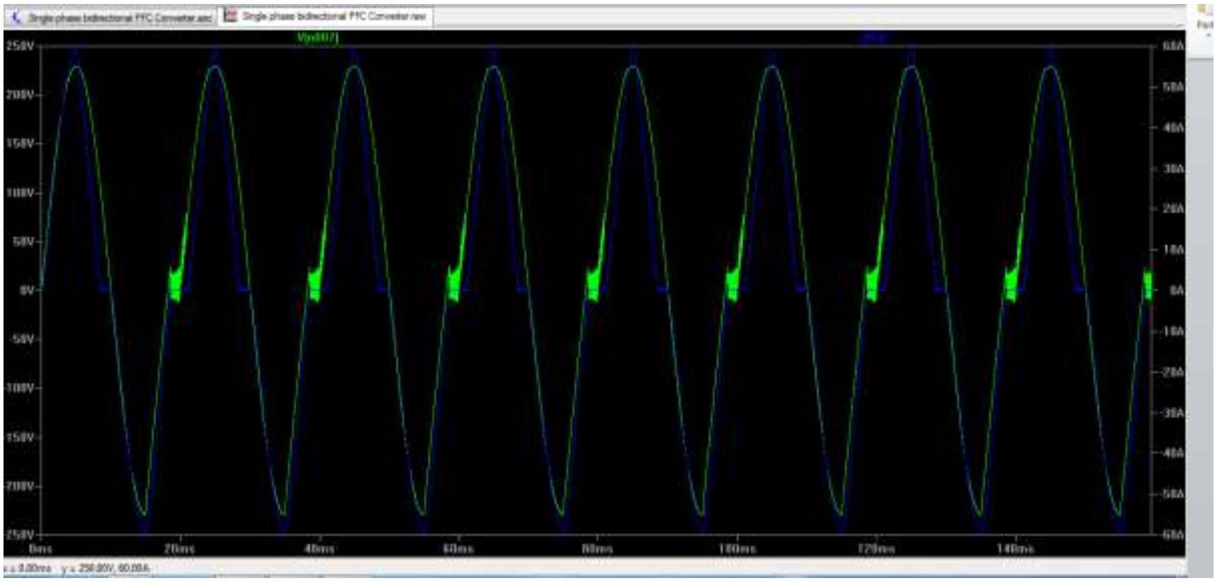


Figure A-6 Sample waveform for input current and voltage

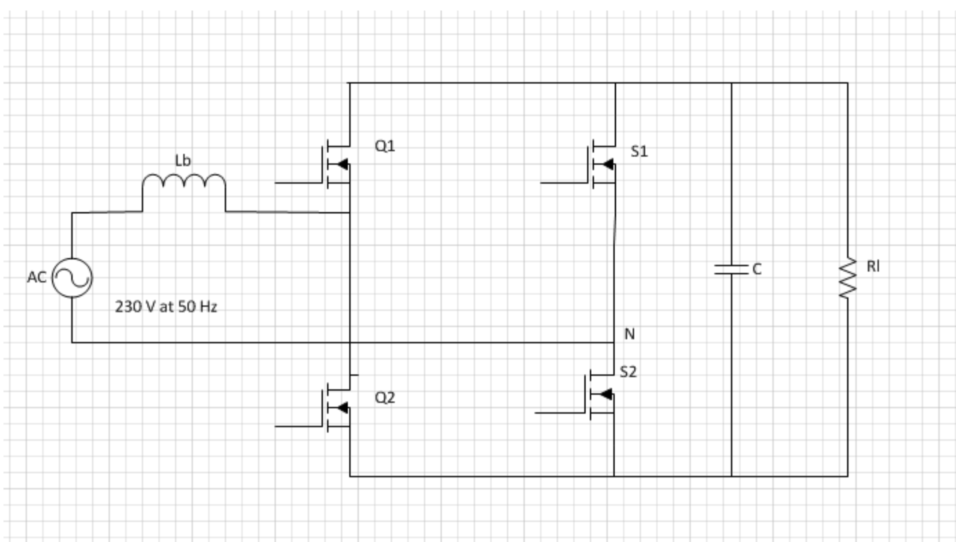


Figure A-7 Totem-pole PFC converter topology

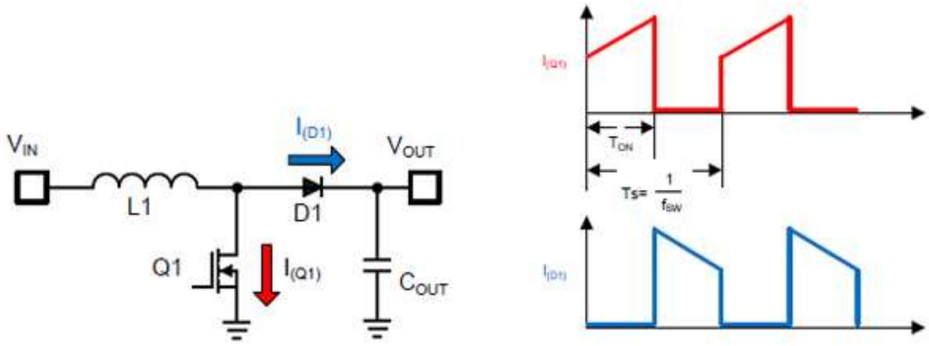


Figure A-8 Boost converter Circuit and current flow in D1 and Q1

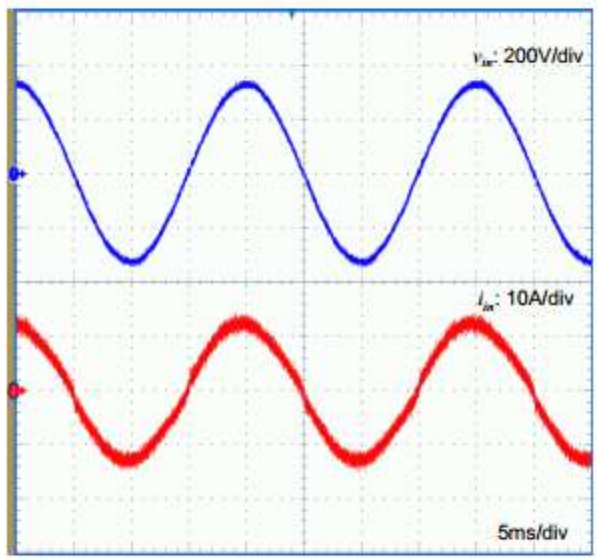


Figure A-9: Input voltage and input current waveforms at output power of 2kW

Appendix B: Laboratory set up

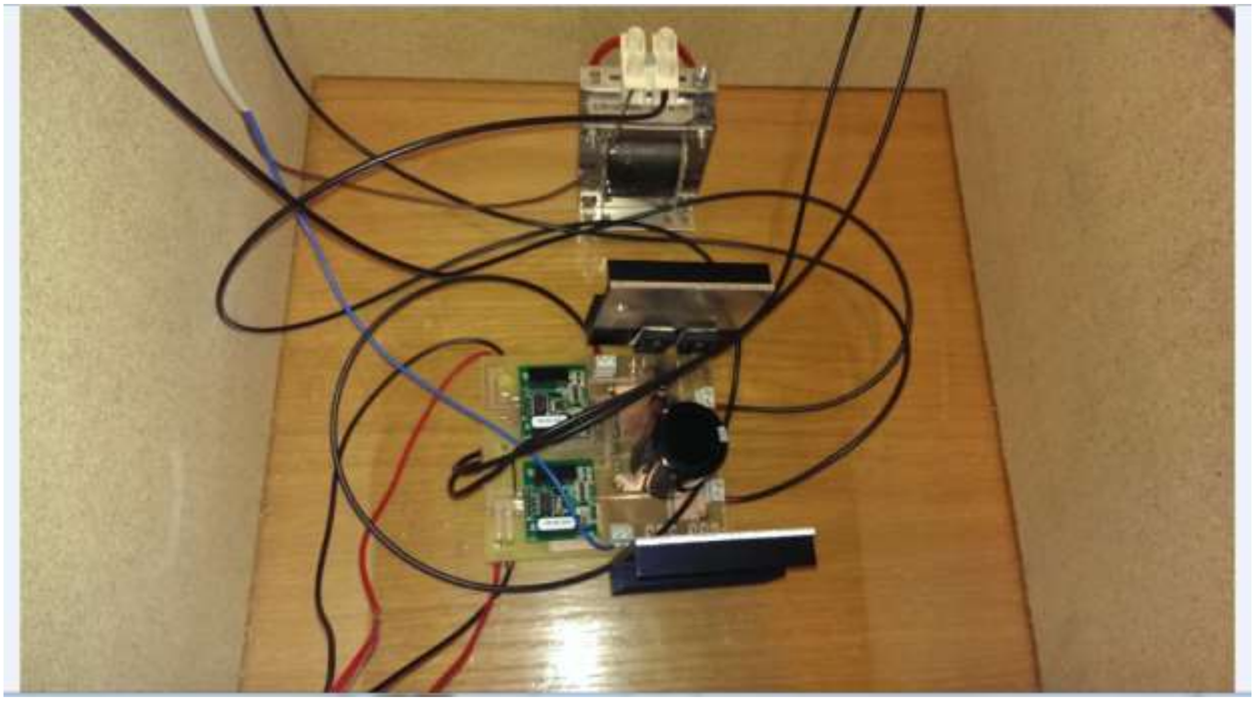


Figure B-1: Connection of the prototype

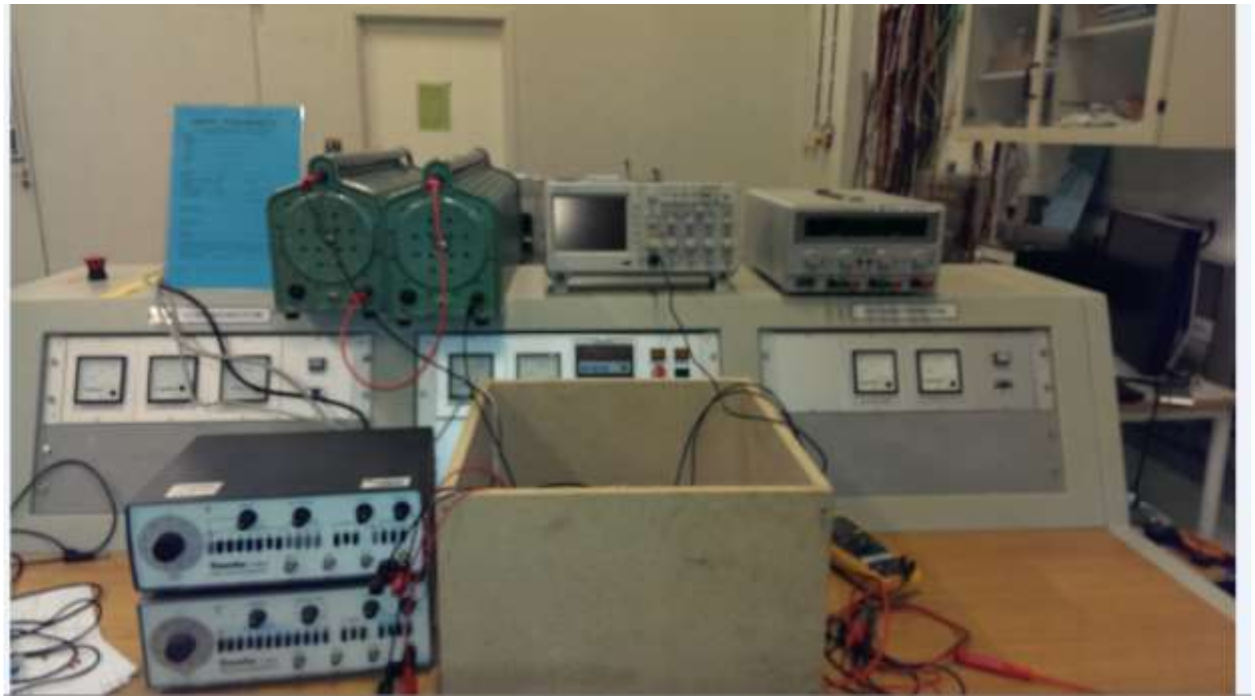


Figure B-2: Complet labratory setup

Appendix C: Additional Pictures and Graphs

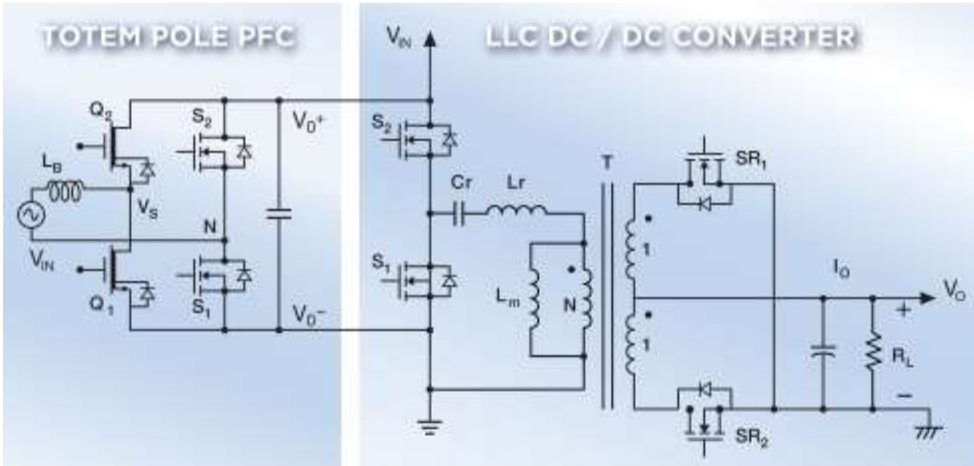


Figure C-1: Simplified circuit diagram for high-efficiency PFC off-line power supply

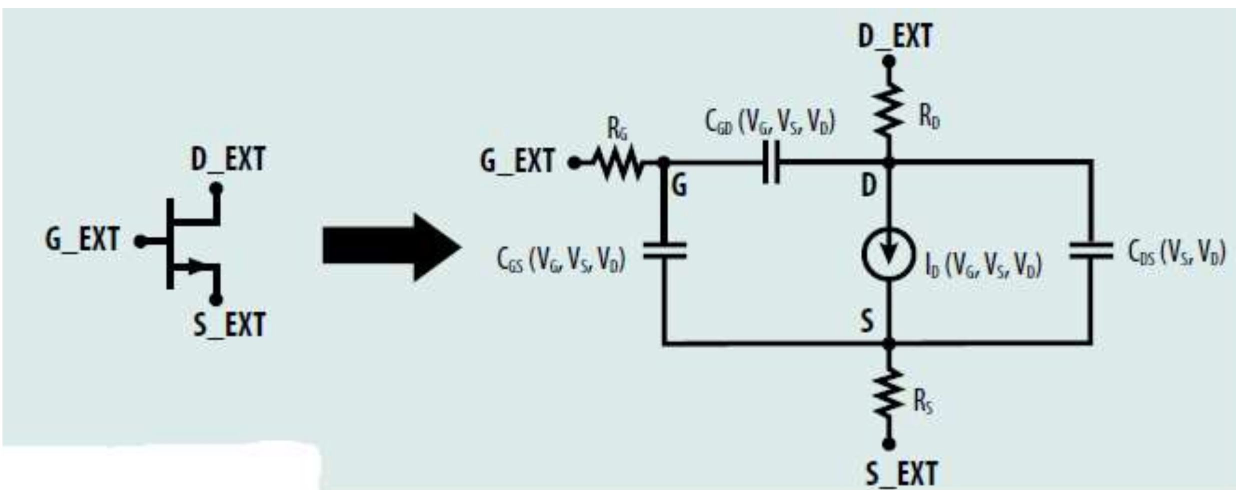
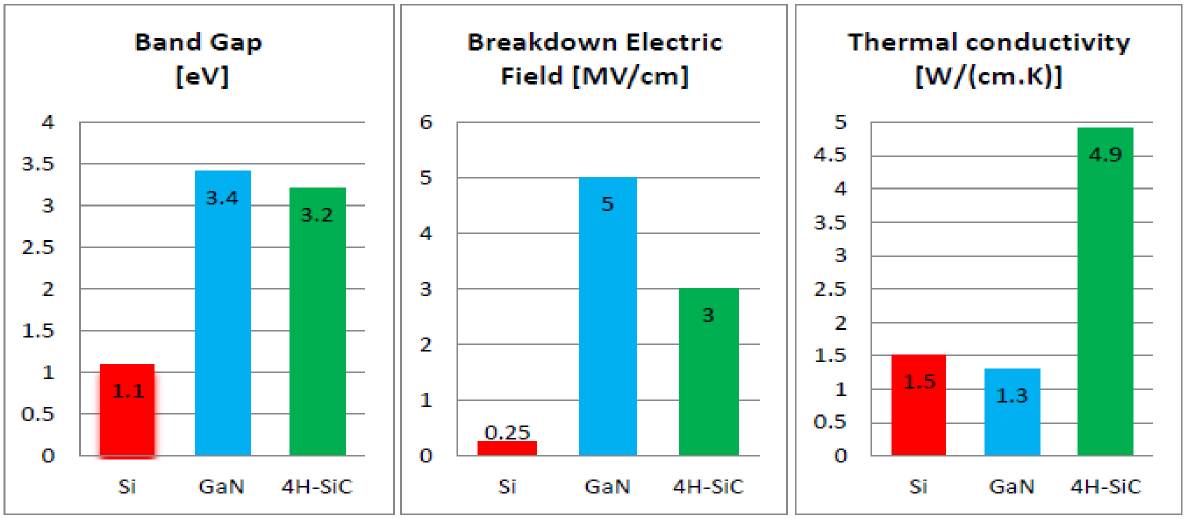


Figure C-2: GaN Model



Larger band gaps means	Higher critical field results in	Increased thermal conductivity allows
Decrement in Intrinsic carriers	Increment in Blocking voltage	
Increment in Operating temperature	Decrement in On-resistance	Increment in heat dissipation
	Increment in Switching Speed	Increment in power density

Figure C-3 Bar diagram showing the comparison of semiconductor properties