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Thesis for the degree of
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1 Abstract

When connecting distributed power generation systems to the utility grid, a power converter is normally placed between the main grid and the local micro-grid, at the point of common coupling. In order to synchronize the converter to the utility grid voltages, a synchronizing circuit is needed. A common way of doing this, is to use a phase-locked loop (PLL). This circuit estimates a voltage reference angle which is fed to the control system of the power converter. One of the simplest PLL designs is based on the grid voltage zero crossings. The drawback of this method is that no information about the grid voltage conditions is available in the interval between the zero crossing. The design has been implemented and successfully tested on a Field Programmable Gate Array (FPGA) circuit connected to a power converter.

A more advanced way of designing a PLL is by using voltage vector control. The method is more complex and time consuming. On the other hand, information about the grid voltage condition is always available. The design fails to run properly if the grid voltages are unbalanced or distorted. In order to improve the performance, a multi-variable filter tuned at nominal grid frequency may be added. This solution has been implemented on an FPGA circuit and successfully tested.

The multi-variable filter will cause an angle displacement if the grid frequency deviates from its nominal value. The author proposes a method called Adaptive Signal Cancellation (ASC), in order to make the PLL frequency independent. The method is based on a method called Delayed Signal Cancellation (DSC) where the grid voltages are inputted and symmetric voltage components are outputted. Instead of delaying signals, the ASC is phase shifting signals, obtaining approximately the same performance. In addition to providing the control circuit with an estimated voltage reference angle, the circuit also outputs signals determining grid voltage conditions: voltage level, symmetry and frequency. These signals can be used in an overhead control structure taking care of power management and protection.

2 Preface and Acknowledgement

This thesis is submitted in partial fulfillment of the requirements for the degree of Doktor Ingeniør at Norwegian University of Science and Technology. The work has been carried out at Narvik University College.

I am grateful to my supervisor Associate Professor Dr. Waldemar Sulkowski at Narvik University College for supporting and inspiring me through my entire work. He has also provided me abundantly with needed background information. I also want to give a deep-felt thank to Professor Dr. Lars Norum at Norwegian University of Science and Technology for important feedback and for adding perspective to my work. I want to thank my colleagues at Narvik University College for their interest, support and constructive discussions. Indeed they form an inspiring working environment.

I have had access to a lot of laboratory resources, owing to Johnny Tokle and Zoran Dokic at Narvik University College and Valdimir Klubicka at Norwegian University of Science and Technology.

Finally, I want to thank Todd Nolen for his kind contribution, proof-reading this thesis.

Contents

3 Nomenclature

α	phase-shift operator
$v_{\alpha,del}$	delayed stationary reference active voltage component
$v_{\beta,del}$	delayed stationary reference reactive voltage component
τ_{filter}	multivariable filter response time
β	asymmetry factor phase B
$\Delta\theta$	deviation between real and estimated reference angle
Δf_{filter}	multivariable filter bandwidth
Δv_d	active voltage component deviation
Δv_q	reactive voltage component deviation
Δx	numeric increment
γ	asymmetry factor phase C
ω_c	centre (nominal) angular velocity
ω_n	undamped resonance frequency
τ_i	untegrator time constant
ε	control phase angle
φ	phase angle
$\widehat{\omega}$	estimated angular velocity
$\widehat{\theta}''$	estimated reference angle phase C
$\widehat{\theta}'$	estimated reference angle phase B
$\widehat{v}_\alpha$	estimated stationary reference frame active voltage component
$\widehat{v}_\beta$	estimated stationary reference frame reactive voltage component
ζ	damping coefficient
e	error signal
f_1	fundamental frequency
f_{sw}	switching frequency
f_s	sampling frequency
$H_{LF}(s)$	loop filter transfer function
$H_{NCO}(s)$	transfer function of the numerically controlled oscillator
$H_{PFD}(s)$	transfer function of the phase frequency detector
$H_{PLL}(s)$	transfer function of the phase-locked loop
i_a	current phase A
i_b	current phase B
i_c	current phase C
${i_d}^*$	active current component reference value
${i_q}^*$	reactive current component reference value
I_m	current amplitude
k_i	integrator gain
k_p	proportional gain
M_3	relative injection of third harmonic voltage
S_a	switching state phase A
S_b	switching state phase B
S_c	switching state phase C

V	amplitude of fundamental phase voltage component
v_{ab}	line voltage between phase A and B
v_{bc}	line voltage between phase B and C
v_{ca}	line voltage between phase C and A
$v_a{}^*$	PWM reference voltage phase A
$v_b{}^*$	PWM reference voltage phase B
$v_c{}^*$	PWM reference voltage phase C
V_{dc}	voltage at DC bus
$v_d{}^*$	active voltage component reference value
$v_q{}^*$	reactive voltage component reference value
v_{conv}	mean value of converter
v_{grid}	phase voltage of strong grid
x_{k+1}	a posteriori integer value
x_k	a priori integer value
θ	voltage reference value
$\widehat{\omega}_{\mathrm{lim}}$	lower stability limit for estimated frequency
$\widehat{\theta}$	estimated reference angle phase A
$\widehat{v}_{\alpha,1}$	estimated positive sequence reference active voltage component
$\widehat{v}_{\beta,1}$	estimated positive sequence reference reactive voltage component
$\widehat{v}_{\alpha,del}$	estimated delayed stationary reference active voltage component
$\widehat{v}_{\beta,del}$	estimated delayed stationary reference reactive voltage component
$\widehat{V}_{\alpha}$	estimated amplitude of stationary reference active voltage component
$\widehat{V}_{\beta}$	estimated amplitude of stationary reference reactive voltage component
v_{α}	stationary reference active voltage component
v_{β}	stationary reference reactive voltage component
v_a	phase voltage in phase A
v_b	phase voltage in phase B
v_c	phase voltage in phase C
ALC	adaptive linear combiner
ASC	adaptive signal cancellation
CHP	combined heat and power
CSI	current source inverter
DG	distributed generation
DPC	direct power control
DPGS	distributed power generation system
EPS	area electric power system
FFT	Fast Fourier Transform
FIR	finite impulse response
FPGA	field-programmable gate array
IGBT	insulated gate bipolar transistor
LF	loop filter
ll	line-to-line fault

llg	line-to-line-to ground fault
slg	single-line-to-ground fault
MPP	maximum power point
NCO	numerically controlled oscillator
NDZ	non-detection zone
PCC	point of common coupling
PFD	phase frequency detector
PLL	phase-locked loop
PWM	pulse width modulation
THD	total harmonic distortion
UPF	unity power factor
UPS	uninterruptible power supply
VFOC	virtual flux oriented control
VOC	voltage oriented control
VSI	voltage source inverter
Subscript $_{\alpha}$	active component in stationary reference frame
Subscript $_{\beta}$	reactive component in stationary reference frame
Subscript $_{d}$	direct axis component in synchronous reference frame
Subscript $_{q}$	quadrature axis component in synchronous reference frame
Subscript $_{0}$	zero-sequence component
Subscript $_{1}$	positive-sequence component
Subscript $_{2}$	negative-sequence component

4 Introduction

Due to climate challenges, such as global warming and increased CO_2-emissions, there might be a need for a considerable growth in power production based on new renewable energy sources, like wind power, bio fuel, photovoltaic etc. One concept is to generate electricity close to the customer, so-called distributed energy generation. Generating energy close to the load reduces the need of long distance power lines. Making a reliable connection between renewable energy sources and the utility grid, may however be a challenge.

New renewable energy sources are often intermittent, e. g. solar panels, wind turbines etc. These energy systems could be combined or connected to a local energy storage system, in order to obtain a continuous power flow between the mains grid and the local network. The latter is termed a micro-grid. The connection between these two energy systems is called point of common coupling. A power converter located at this point will yield a better control of the power flow between the mains and the micro-grid.

In order to control a converter at point of common coupling, the conditions of the grid need to be supervised. First of all, the converter should be synchronized to the grid voltages. Moreover, grid voltage disturbances should be detected, in order to disconnect the circuit breaker at point of common coupling , if neccesary. Finally, it is important to disconnect the circuit breaker if the main grid is to be de-energized. If distributed systems feed energy into a disconnected part of the grid, an unintended island occurs.

A synchronizing circuit should provide control signals to the power converter, based on grid voltage measurements. It would be beneficial if the circuit also detects grid voltage disturbances like voltage sags and swells, asymmetry, voltage harmonics and frequency deviation. The signals could be utilized in a multi-function protection system for the micro-grid. The synchronizing and detection circuit should also yield proper control signals to the converter during such disturbances.

A common solution for a synchronizing circuit is a phase-locked loop. In Chapter 9 a circuit based on a Field Programmable Gate Array is utilized. The chapter describes the author's diploma work and subsequent work with this technology. Another solution is described in Chapter 11, where the design is realized using a more complex design with a lot of calculations. The method is well known, and is usually run on a computer, using floating point calculations. The author has tested the method on a Field Programmable Gate Array with fixed point calculations and has obtained good results.

An alternative method, called Adaptive Signal Cancellation, is proposed in Chapter 12. Like the above mentioned approaches, the method utilizes a phase-locked loop. The major advantages of the proposed method is that the circuit is very robust to grid voltage asymmetry and frequency deviations. The design is built and tested with satisfactory results.

In the author's opinion the development of the Adaptive Signal Cancellation method is his original achievement.

5 New Renewable Energy Sources

This chapter focuses on the need for new reneable energy sources, due to climate challenges. Different kinds of renewable energy sources are considered, their operating mode and stage of development.

5.1 Climate challenges

The situation today with increasing emission of carbon dioxide into the atmosphere, calls for immediate measures to avoid an extensive rise in the average temperature of the atmosphere. The consequences are unpredictable, with a meltdown of the polar ice caps as a quite possible scenario. In order to avoid such climate impacts, it is necessary to search for alternatives to energy sources based on fossil fuels; i.e., oil; coal and natural gas. According to [1], the future global energy demand will continue to rise at an accelerating rate, which can be seen from Fig. 5.1. The figure shows that energy production based on fossil fuels will decrease, while energy demand will continue to rise. This calls for renewable alternatives. [2] states that since 1971, each one percent increase in the gross world product has yielded a 0.64 percent increase in energy consumption. The International Energy Agency has created a scenario called "New Game", where the emission goals of the Kyoto protocol are to be fulfilled [1]. The results of this scenario are presented in Fig. 5.2. In this figure, nuclear power will play a significant role, while oil and gas production will be reduced to a minimum by 2020.

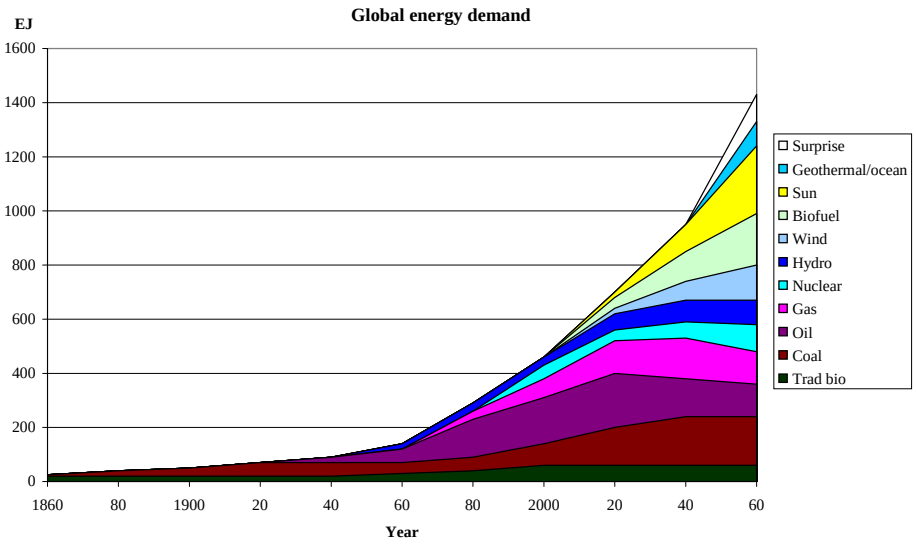

Figure 5.1: Past and future energy demand.

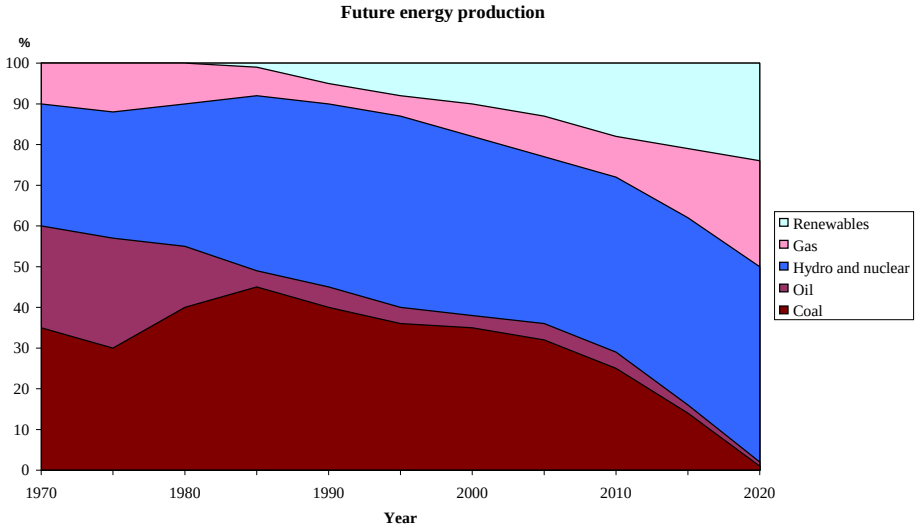

Figure 5.2: Energy production over the last decades and predicted future energy production.

One must expect that developing countries will increase their energy consumption quite significantly in decades to come. [3] has made a study of the international energy outlook in 2007, and Fig. 5.3 predicts that the developing countries will catch up with the industrialized world in a few years to come.

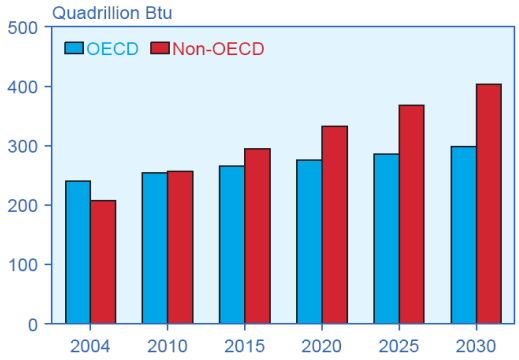

Figure 5.3: Present and future energy consumption by region.

5.2 New renewable energy sources

New renewable energy sources incorporate solar energy, bioenergy, wind energy, ocean energy, geothermal energy, hydro energy, blue energy and energy from heat pumps. Solar energy can be either thermal or electric, generated by various kinds of sunlight collector or photovoltaic (PV) panel, respectively. Bioenergy is generated by burning biofuel, thereby generating heat and/or electricity. This latter system generates combined heat and power (CHP). Wind energy is generated by means of a wind turbine connected to a generator. There are different kinds of new renewable ocean energy sources; ocean waves, thermal ocean energy, tidal water and ocean currents. Geothermal energy is used for heating and/or electrical generation. Small scale hydro energy is also considered as a new renewable energy source, even though large scale hydro power has been utilized for decades. Blue energy is the energy retrieved from the difference in the salt concentration between seawater and river water with the use of ion specific membranes. Heat pumps transmit heat from the surroundings into buildings, thereby indirectly utilizing the solar energy [4].

New renewable energy sources can be arranged into two categories; heat sources and sources of electric power, as shown in Fig. 5.4. Only the electric power sources are considered here. Some of them have a continuous power flow while others are intermittent. Some are fully developed while others are still in early stages of development. Table 5.1 classifies the different new renewable electric power sources, depending on operating modes, stages of development and CHP capability. As can be seen from the table, some sources are at initial stages, while others are fully developed. One also notices that energy sources; like wind turbines, PV panels, tidal water turbines and ocean wave generators are running in an intermittent operating mode. They need to be connected to the utility grid or an energy storage device in order to supply a load with a continuous power flow.

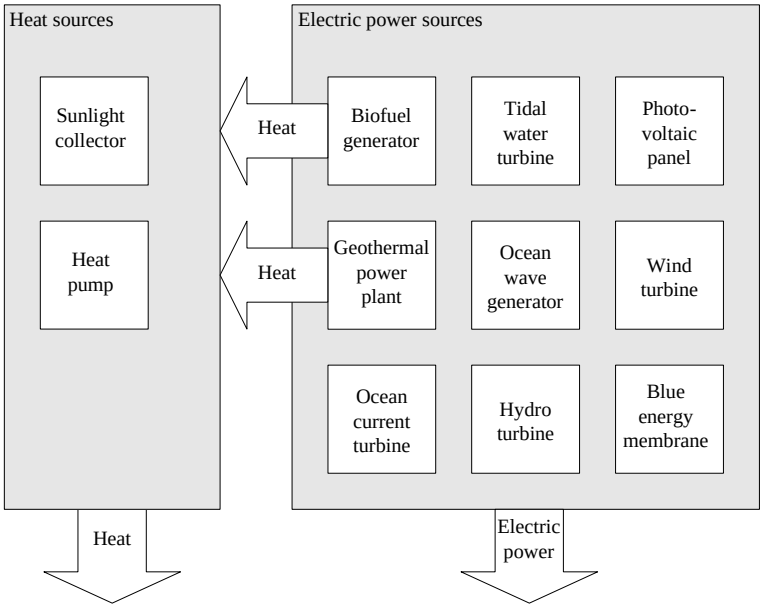

Figure 5.4: New renewable energy sources.

Table 5.1: Properties of new renewable electric power sources

Energy source	Operating mode	Stage of development	Combined heat and power
Biofuel generator	Continuous	Working prototypes	Yes
Tidal water turbine	Intermittent	Working prototypes	No
Photovoltaic panels	Intermittent	Fully developed	No
Geothermal power plant	Continuous	Fully developed	Yes
Ocean wave generator	Intermittent	Early stage of research	No
Wind turbine	Intermittent	Fully developed	No
Ocean current turbine	Continuous	Early stage of research	No
Hydro turbine	Continuous	Fully developed	No
Blue energy membrane	Continuous	Prototype testing	No

The sizes of the energy sources are quite different. PV panels will normally generate just a few kilowatts, while a geothermal power plant may generate hundreds of megawatts. Wind turbines and hydro turbines span a wide range of sizes, even though a single wind turbine has a rated power of a few megawatts, a large wind farm may yield hundreds of megawatts. There is an extensive research on biofuel generators and tidal water turbines, but these systems are still not manufactured in large numbers, so it is too early to predict what the typical sizings will be. Blue energy and energy from ocean waves and currents are still immature technologies.

6 Distributed Energy Sources

Distributed power generation is made by utilizing a variety of small energy sources close to the customer. According to [5], Distributed Generation (DG) is defined as small, modular, decentralized, grid-connected or off-grid energy systems located in or near the place where energy is used.

6.1 Classical versus distributed generation

In a classical power generation system, huge power plants are located far away from the customer. These plants generate vast amounts of electric power which is transferred to the customers through long high voltage transmission lines. This is illustrated in Fig. 6.1.

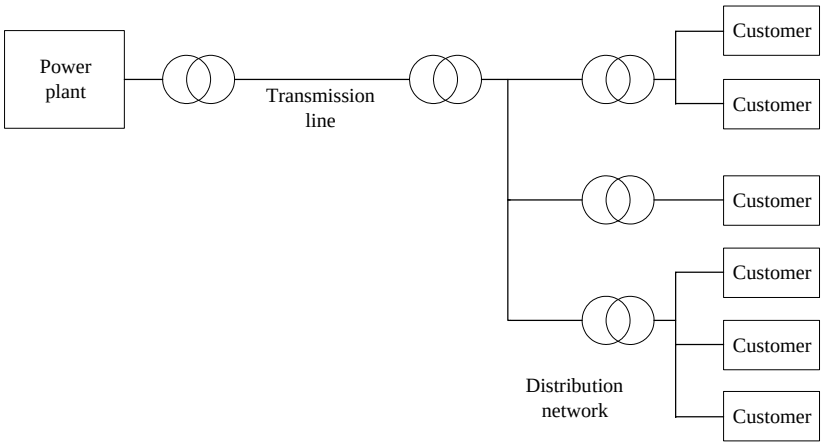

Figure 6.1: Block diagram of a classical power generation system.

In a distributed power generation system, part of the energy demand is covered by small-scale power generation close to the customer. The system is shown in Fig. 6.2. A classical system has good stability. The solution has been used and optimized for decades. The major drawback of this long distance power transmission is significant power losses through the very long transmission and distribution lines.

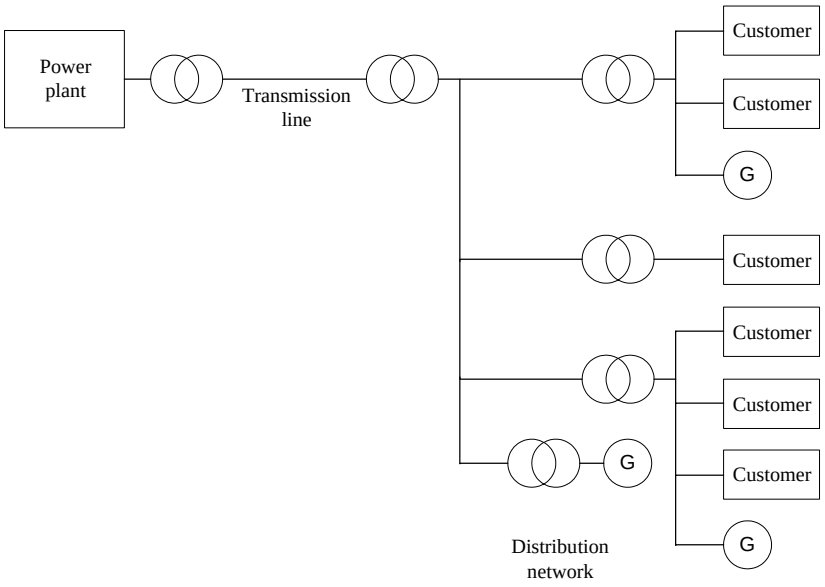

Figure 6.2: Block diagram of a distributed power generation system.

By generating considerable parts of the power close to the customers, the losses are significantly reduced. In addition, heat losses may be used in a CHP system. A customer with a distributed power generation system (DPGS), has the opportunity both to buy and to sell electricity, depending on the ratio between production and consumption. In such a system, the customer also has a backup source if voltage disturbances should occur at the grid. Moreover, DG based on new renewable energy sources is environmentally friendly.

The major challenges of DG power penetration into the grid is system stability, unintended islanding and personnel safety. Many of the DG sources are intermittent, and if the DG power flow is fluctuating, stability can be put at risk. If a part of the distribution network (an island) is disconnected from the rest of the grid, all DG sources should be disconnected, in order to de-energize the network. If DG sources continue to energize the island, arcs might be sustained, and both grid voltage and frequency may exceed tolerance limits. Automatic reclosure of circuit breakers between the energized island and the rest of the grid may significantly strain the equipment, since the phase sequence of the island most likely will drift away from the strong grid. There will be a hazard of electric shock for personnel maintaining the isolated network if it is unintentionally energized.

6.2 Point of Common Coupling

A DPGS will usually contain one or more power sources in combination with local load, tied together on a so-called micro-grid. This micro-grid is connected to the main grid (area electric power system - EPS) by a connection named *Point of Common Coupling* (PCC). Fig. 6.3 shows an example on a wind turbine, a PV panel and a prioritized load connected to a micro-grid. The rest of the load is unprioritized and is connected to the PCC by a

transformer. If a fault is detected on the area EPS; the circuit breaker opens and the micro-grid operates in stand alone mode, thereby supplying the critical load, while the rest of the load is subjected to the fault conditions. As soon as the voltage conditions on the area EPS is restored and the micro-grid is synchronized to the area EPS, the circuit breaker is reclosed, and the DPGS returns to normal operation.

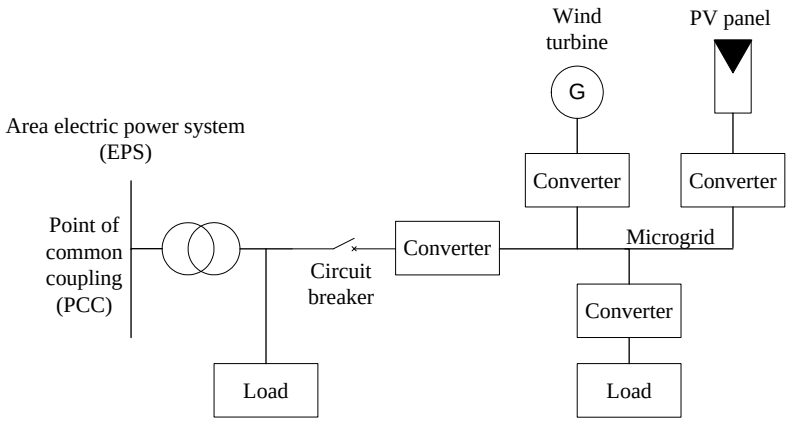

Figure 6.3: Microgrid with point of common coupling to the area electric power system.

Sometimes the local network might have several connections to the area EPS, and then it can be difficult to define an explicit PCC. Such a problem is beyond the parameters of this thesis, so it will need to be researched separately.

6.3 Structure and size

There are several ways to configure a DPGS. The microgrid might use DC, single phase or three-phase AC, and some of the converters might be omitted. If, for instance, the microgrid is a three-phase grid, the converter between the circuit breaker and the micro-grid and the converter between the load and the micro-grid may be left out. By keeping the converter between the micro-grid and the PCC, it is possible to inject or consume reactive power at the PCC, thereby using the DPGS for phase compensation. In addition, the area EPS and the micro-grid may run at different frequencies. Depending on the energy sources, possible storage devices, different power sources and different operation strategies of the DPGS, the system could be configured in different ways. The grid connection through the PCC is common to all possible configurations.

The power production of a DPGS is typically in the range from a few kilowatts to fifty megawatts.

7 Challenges in Connection with Distributed Generation

When connecting DPGS to the utility grid, there is a need for synchronizing the energy systems and monitoring the main grid. There should also be systems for power management and disconnection of the DPGS.

7.1 Synchronizing

Fig. 7.1 shows a grid-connected voltage source inverter (VSI). In order to keep a proper voltage across the filter inductances L, the VSI voltages must be synchronized to the grid voltages. In addition, line currents and DC voltage need to be measured in order to keep these parameters at acceptable levels. In Fig. 7.2 voltage and current measurements are supplied to a synchronization and control circuit, with the switching signals S1 - S3 switching the transistors on and off. The AC voltages are measured on the front end of the circuit breaker. If the circuit breaker is opened and the VSI is out of operation, the synchronization circuit is still operating. When it is time to reconnect the inverter to the grid, information about the grid voltage is always present. If the voltage measurements were to be done inside the circuit breaker, no information about the grid voltages would be available.

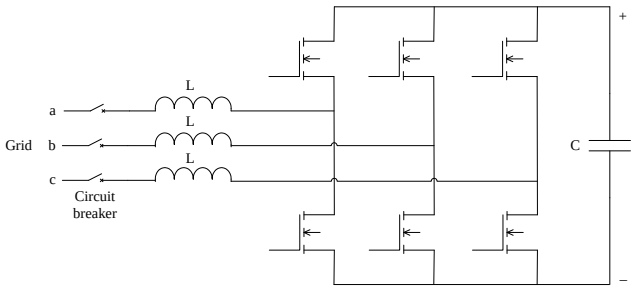

Figure 7.1: Grid connected voltage source inverter.

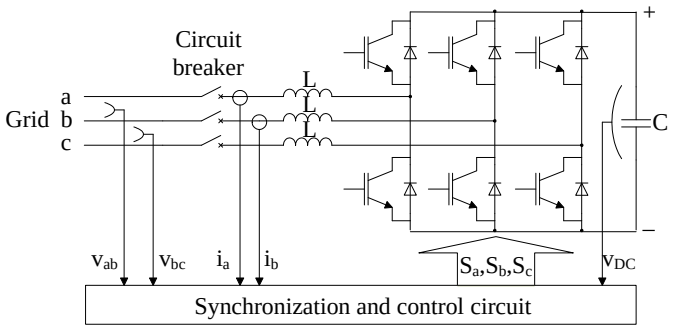

Figure 7.2: Grid connected voltage source inverter with synchronization and control.

7.2 Grid monitoring

The AC voltage measurements also give the possibility to monitor the grid voltages. Various types of voltage disturbances can be detected through these measurements. Typical voltage disturbances are:

- Voltage swell or sag
- Asymmetry
- Voltage harmonics
- Frequency variations
- Transient overvoltages
- Phase disconnection

All these disturbances can cause malfunction on motor drives and electronic equipment. If the grid frequency or grid voltage deviates significantly from nominal value, the line currents of an induction motor will increase. If the grid voltages sag or are unbalanced, the torque will drop significantly. Voltage harmonics will increase the resistance losses in the machine. Some voltage disturbances will influence the performance of electronic power supplies. Under- or overvoltage can easily cause computer tripping [6]. Some voltage disturbances will give rise to flicker in lighting systems. Overvoltages may permanently damage equipment. Extending a synchronization circuit with an additional function of analyzing voltage quality would be beneficial for monitoring the voltage quality on the grid.

7.3 Connection and disconnection

According to [7], DPGS should cease to energize the area EPS within 2.0 s if the grid voltage falls below 88% of its nominal value and within 160 ms if the voltage falls below 50%. This American standard also states that the DPGS should be disconnected within 1.0 s if the grid voltage rises above 110% and within 160 ms if it rises above 120%. According to [8], the supply voltage should be within the range of $\pm 10\%$ for low and medium voltage supplies. This European standard also states that grid voltage asymmetry should not exceed 2%, but in some cases 3%. DPGS with a rated power less than 30 kW should be disconnected in 160 ms if the frequency goes beyond 60.5 Hz or 59.3 Hz with a nominal frequency of 60.0 Hz [7]. In [9], the nominal frequency is 50.0 Hz, and the frequency should never go beyond 47.0 Hz or 52.0 Hz. In 99.5% of the time it should remain between 49.5 Hz and 50.5 Hz. The same standard states that transient overvoltages in a system with a nominal voltage of 230 V, should usually not exceed 6,0 kV peak value. It also states that total harmonic distortion (THD) should be less than 8%. If the above mentioned limits are exceeded, the DPGS should be disconnected within the defined time limits. If there are no time limits or the fault is a borderline case, it will be a trade-off between protection of the equipment (disconnection) or stability issues (continuos operation). The disturbance may be temporary, and disconnecting considerable amounts of DG can reduce grid voltage stability.

Another kind of disturbance can be annoying, but not necessarily damaging, namely flicker due to voltage changes. According to [10], the steady state voltage change shall not exceed 3%, and the maximum voltage change shall not exceed 4%. [11] shows that the flicker impact both depends on the magnitude of the voltage change and the slope of the change. When connecting DPGS with intermittent power flow to the grid, possible voltage fluctuations and flicker in the neighborhood should be considered.

7.4 Power management

Fig. 7.3 shows an example on a power management control system in a DPGS. The power management control monitors and adjusts the power flow in all the converters and the status of the circuit breaker, based on current and voltage information from the different parts of the micro-grid and the main grid. If the voltage on the DC bus drops, the power management control increases the local production, draws energy from the battery or reduces the surplus power flow to the grid. If a severe voltage disturbance occurs, the power management control disconnects the circuit breaker and runs the micro-grid in stand-alone operation. The power management control must also track the maximum power point (MPP) of the solar panel, keep a constant power flow to the critical load and maintain a full charge on the battery. There are many different strategies for power management. A solution for managing reactive power generation in a wind farm is suggested in [12]. Power management for parallel adjustable speed power-electronic generation systems is presented in [13]. Power management of a system with PV panels in combination with uninterruptible power supplies (UPS) is described in [14].

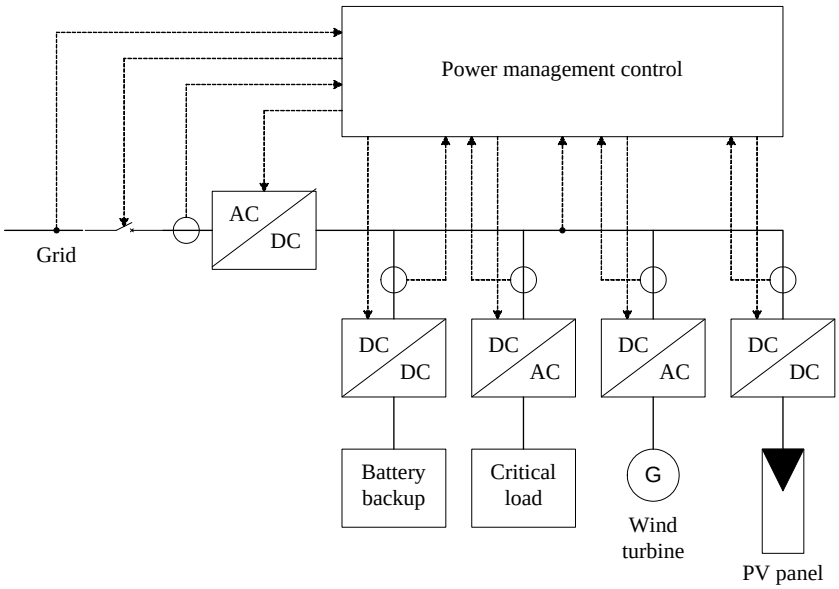

Figure 7.3: Distributed power system with power management control.

8 Grid Connection, Islanding and Stand-Alone Operation

This chapter focuses on ride-through capability, island detection and stand-alone operation. Different DPGS configurations are compared to different uniterruptible power systems.

8.1 Ride-through capability

Ride-through capability is the ability of equipment to withstand momentary interruptions or sags, and some typical time limits are given in [15]. A motor or a generator will lose its torque if the grid voltage drops or disappears. The machine may spin out of control or come to a halt before the grid voltages recover. The filter capacitor of power supplies will discharge completely if the interruption lasts for some tens of milliseconds. Other sensitive equipment may also malfunction due to voltage sags or interruptions. If considerable parts of the grid load or the generation trip, the disturbance may have an impact on system stability. Ride-through capability of wind turbines are described in [16-18], for critical loads on [19,20], and for motor drives on [21,22].

8.2 Island detection

As mentioned earlier, it is necessary to detect an island, in order to disconnect the DPGS at PCC. The only way to monitor the state of the grid is to analyze the voltages and currents at PCC. The traditional way to detect an island is by means of passive techniques; using sensed or calculated parameters such as voltage magnitude, phase shift or frequency deviation to detect an islanding condition. Usually these techniques have so-called non-detection zones (NDZ), which are windows of operating conditions that allow for operation during an islanding event [23]. If grid frequency at PCC is used as a detection parameter, usually it will deviate significantly from its nominal value during an island event. If the active power demand is much higher than the generation on the island, the frequency will drop beyond the limits of safe operation, and an island is detected. If the demand is much less than the generation, the frequency will rise, and an island is detected. If, on the other hand, active power generation and consumption balances approximately, then the frequency may remain inside the interval of safe operation, and the island is not detected.

Active techniques reduce or eliminate the NDZ by using control loops to continuously perturb the output [23]. One technique manipulates the output frequency to try to increase the grid frequency. As long as the strong grid is in normal operation, these perturbations will not affect the grid frequency, but during an islanding, the frequency of the island will most likely go beyond the upper frequency limit [24-27]. A related method is to measure the ratio between frequency and output power at PCC [28]. Another method is to have a positive feedback voltage loop which is stabilized by the strong grid during normal operation, but forces the output voltage to go beyond safety limits during an islanding [23]. A mix of active and passive island detection is described in [29]. Common to all the active techniques is that they perturb the output voltage at PCC in one way or another, thereby influencing the grid voltages and/or frequency.

8.3 Stand-alone operation

During stand-alone operation the DPGS should have uninterruptible power system (UPS) capability, meaning that the power flow to critical loads should be continuos, even if the DPGS is disconnected from the grid. In addition, voltage quality should be sufficient. The most common UPS configurations are described in [30]. Fig. 8.1a shows an off-line UPS. During normal operation the static bypass switch is closed and the power is transferred directly from the grid to the load. The rectifier keeps the battery fully charged. If a grid fault occurs, the static bypass switch opens, and the battery supplies the load through the inverter.

Fig. 8.1b shows an off-line-interactive UPS with a single converter. The inductor filters out some current harmonics. During normal operation the power is bypassed through the static switch, through the filter and to the load. The converter operates as a rectifier and charges the battery. During a grid fault, the static bypass switch is open and the converter operates as an inverter, supplying the load by means of the battery.

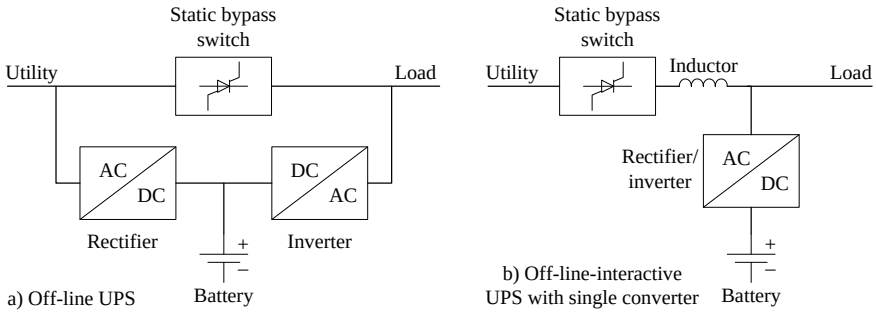

Figure 8.1: Block diagrams of UPS systems: a) Off-line UPS, b) Off-line interactive UPS with single inverter.

Another version of the off-line-interactive UPS is shown in Fig. 8.2. This configuration has two converters and an additional series transformer.

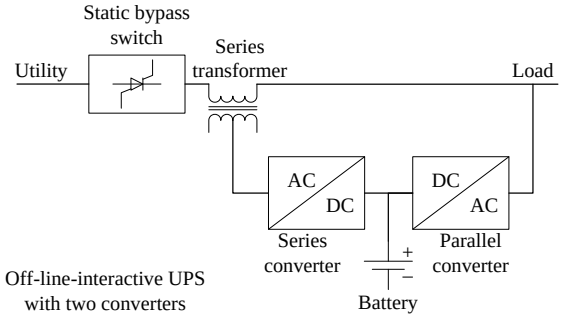

Figure 8.2: Block diagram of off-line-interactive UPS with two converters.

During normal operation the power is bypassed through the static switch, over the transformer and to the load. The parallel converter runs as an active rectifier with an active filter capability and charges the battery. The series converter and series transformer are used for load voltage conditioning. During a grid fault, the static bypass switch is open, and the load is supplied through the parallel converter from the battery.

An on-line UPS is shown in Fig. 8.3. The cascaded converters are continuosly operating. The power flows through both converters and to the load. The rectifier keeps the battery fully charged. During a grid fault the power flow through the rectifier is reduced or lost. The battery will then supply the load through the inverter. The static bypass switch is normally open, but will be closed if one of the converters fails. The power will then be transferred directly from the grid to the load.

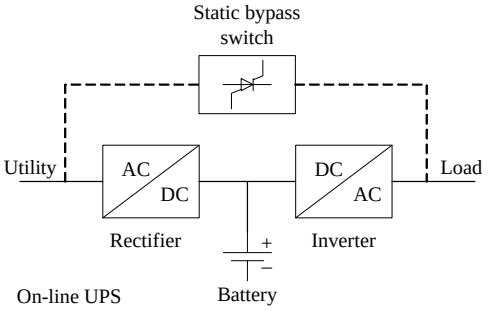

Figure 8.3: Block diagram of on-line UPS.

A DPGS is more complicated than a UPS and can be configured in many different ways, based on available distributed energy resources (DER). If one focuses on the critical load, however, the DPGS can be configured in a similar fashion to the above described UPS topologies. Fig. 8.4 shows a simple solution where the load normally is connected directly to the grid. The DER and energy storage devices are grouped together in a single block. This solution do not have power conditioning properties while the system is grid connected. Whenever the circuit breaker opens, the load is supplied by the local DER resources, and the energy storage system will yield proper power shaving.

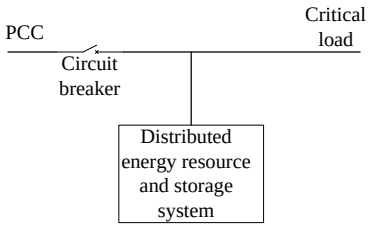

Figure 8.4: DPGS with directly connected load.

Fig. 8.5 shows a solution where the inverter between the DC bus and the critical load secures good voltage and power quality to the load. Even if the DC bus voltage is fluctuating due to intermittent power generation, the inverter will keep the power flow and output voltage at proper levels. If the inverter should fails, the critical load is severed from any possible power source. In Fig. 8.6, an additional bypass switch makes it possible to connect the critical load directly to the grid if the DPGS is down.

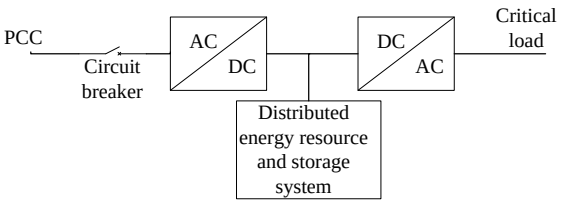

Figure 8.5: DPGS with load power flow control.

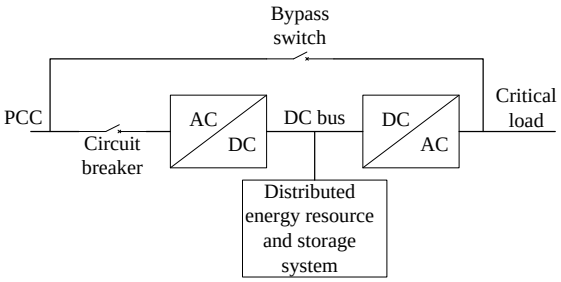

Figure 8.6: DPGS with load power flow control and bypass connection.

Common to any inverter running in stand-alone operation is the need of output voltage filtering. L-filters are not enough to filter pulsewidth-modulated voltages to passive loads. LC- or LCL-filters must be used, in order to make the output voltages as sinusoidal as possible [31].

9 Phase-Locked Loops

Different ways of generating a synchronizing reference signal are considered. The fundamental principle of phase-locked loops is explained. PLL designs based on zero voltage detection are described, in single-phase and three-phase versions, respectively.

9.1 Synchronizing circuits

Three-phase voltage reference

A voltage reference angle is needed synchronize the converter to the grid voltages. Fig. 9.1 shows balanced phase voltages in a three-phase wye-connected system. The reference frame $\alpha\beta$ is stationary. The reference angle θ lays between the positive real axis α and the phase voltage v_a.

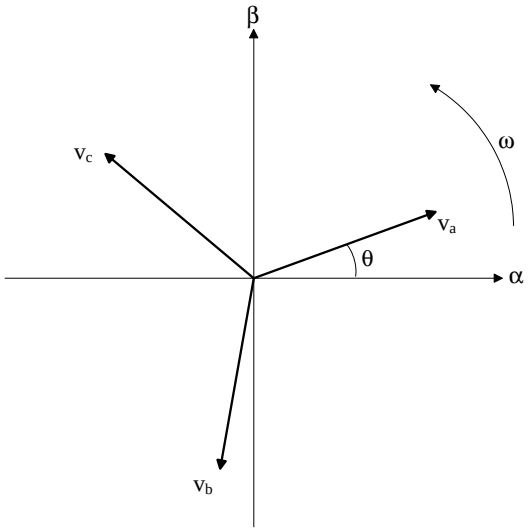

Figure 9.1: Balanced three-phase voltages with stationary reference frame.

For balanced three-phase voltages, the voltages can be defined as equation (9.1):

$$\begin{aligned} v_a &= V\cos(\theta) \\ v_b &= V\cos\left(\theta - \tfrac{2\pi}{3}\right) \\ v_c &= V\cos\left(\theta - \tfrac{4\pi}{3}\right) \end{aligned} \tag{9.1}$$

where V is the amplitude value of the phase voltages.

The voltages in (9.1) can be represented by a single voltage space vector in a stationary reference frame. This is done by means of the Clark transform, expressed in equation (9.2):

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{9.2}$$

Inverse tangent

The simplest way of calculating the reference angle is by means of an inverse tangent calculation equation (9.3):

$$\widehat{\theta} = \arctan\left(\frac{v_\beta}{v_\alpha}\right) \tag{9.3}$$

The method is fast and simple, but not robust. Transient voltage disturbances will immediately affect the estimated reference angle $\widehat{\theta}$, since neither equation (9.1) nor equation (9.2) have inherent filtering properties.

Phase-locked loop

Another way of estimating the reference angle is to use a phase-locked loop (PLL). This circuit compares the estimated reference angle $\widehat{\theta}$ with the real reference angle θ. A control loop minimizes the angle displacement between these signals. The circuit is described in detail later in this chapter. The PLL has inherent lowpass properties, thereby filtering out transient voltage disturbances.

Observer

An observer is a very powerful way to determine the grid voltage condition, not only the voltage sequence, but also voltage harmonics. This solution is complex and requires considerable computational capability. An observer of this type is described and utilized in [32].

9.2 Fundamental principle of a PLL

Fig. 9.2 shows the basic principle of a general PLL. The design is described in [33]. The reference angle θ and the estimated angle $\widehat{\theta}$ are compared in the phase detector. If the estimated reference signal lags the real one, the error signal e is positive and the error signal is negative if the estimated signal leads the real one. If the reference signals are in phase, the error signal is zero.

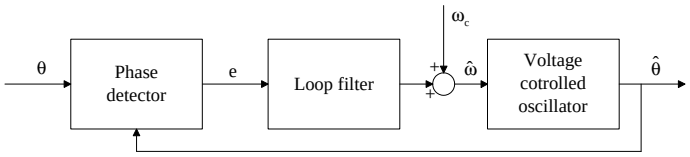

Figure 9.2: Block diagram of phase-locked loop.

The loop filter filters out transient disturbances on the error signal e. The loop filter can be a lowpass filter, a P controller or a PI controller. The latter is the most convenient alternative, since the error signal e will be minimized. The output of the loop filter is added to the centre angular velocity ω_c, determined by the nominal grid frequency. If the nominal grid frequency is $50\,\mathrm{Hz}$, the centre angular frequency should be $100\pi\ \mathrm{rad/s}$. The sum of the centre angular velocity ω_c and the output of the loop filter represents the estimated angular grid velocity $\widehat{\omega}$.

The estimated reference angle $\widehat{\theta}$ are calculated simply by means of an integration , as shown in equation (9.4):

$$\widehat{\theta}\left(t\right) = \int \widehat{\omega}\left(t\right) dt \tag{9.4}$$

In the frequency domain equation (9.4) can be expressed as equation (9.5):

$$\widehat{\theta}\left(s\right) = \frac{1}{s}\widehat{\omega}\left(s\right) \tag{9.5}$$

The diagram in Fig. 9.2 is based on analog signals, but the signals of course can be digitized, using a discrete control loop, which is the most common solution today.

9.3 Zero crossing detection

There are two common PLL designs employed in power electronics. The simplest one is based on zero crossing detection of the grid voltages or similar signals to be synchronized [34,35]. Fig. 9.3 shows the applied comparator circuits, and Fig. 9.4 depicts the different signals.

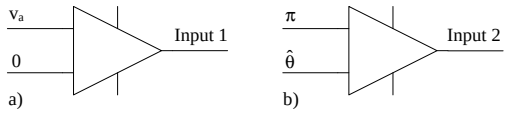

Figure 9.3: Phase pulse generators: a) zero crossing detection, b) estimated zero crossing.

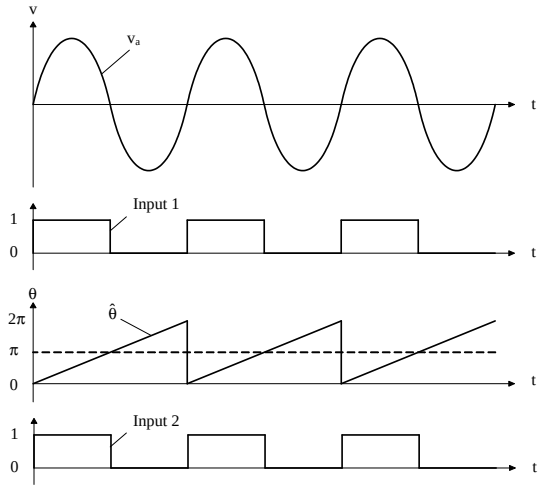

Figure 9.4: From the top: Phase voltage v_a, phase detection signal *input 1*, estimated reference angle $\widehat{\theta}$, phase detection signal *input 2*.

I Fig. 9.3a the phase voltage v_a is inputted, and the sign of this voltage determines the level of the square signal *Input 1*. This is evident from Fig. 9.4 and from equation (9.6). The other pulse train, *Input 2*, is generated by means of the comparator shown in Fig. 9.3b. As long as the estimated reference angle $\widehat{\theta}$ is less than π, the pulse signal is high. This can be seen from Fig. 9.4 and from equation (9.7).

$$Input\ 1 = \begin{cases} 1 \text{ for } v_a > 0 \\ 0 \text{ for } v_a \leq 0 \end{cases} \tag{9.6}$$

$$Input\ 2 = \begin{cases} 1 \text{ for } \widehat{\theta} < \pi \\ 0 \text{ for } \widehat{\theta} \geq \pi \end{cases} \tag{9.7}$$

The circuit in Fig. 9.5 is described in [36]. Fig. 9.6 shows a case where the estimated reference angle $\widehat{\theta}$ is lagging. At time t_1 a rising edge at *input 1* sets the upper flip-flop in Fig. 9.5, and the Up-signal goes high. At time t_2, the lower flip-flop also is set, and the AND-gate goes high, thereby clearing both flip-flops, and the Up-signal is turned off. Nothing happens at t_3 and t_4, since falling edges do not affect the flip-flops. On Fig. 9.7 the estimated reference angle $\widehat{\theta}$ is leading. At time t_1 the lower flip-flop is set and outputs a Down-signal. At time t_2 both flip-flops are set for a brief moment, until the AND-gate clears them both, and the Down-signal is put off. The duration of the output signals Up and Down is proportional to the angle displacement between the real and the estimated reference angle.

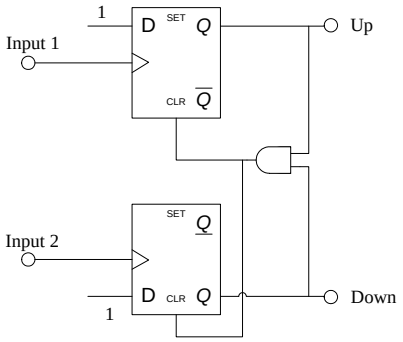

Figure 9.5: Block diagram of phase frequency detector.

The circuit on Fig. 9.5 is not just a phase detector, but also a frequency detector. The angle displacement is defined as equation (9.8). If the frequency of the estimated reference is too low, the angle $\widehat{\theta}$ will be lagging, with a changing positive angle displacement, and a changing positive error signal is outputted, i.e. the Up signal. If the frequency is too high, the angle $\widehat{\theta}$ will be leading and $\Delta\theta$ will be negative, with a changing Down signal as a result. Fig. 9.8 expresses the relationship between the angle displacement and the output value of the PFD circuit.

$$\Delta\theta = \theta - \widehat{\theta} \tag{9.8}$$

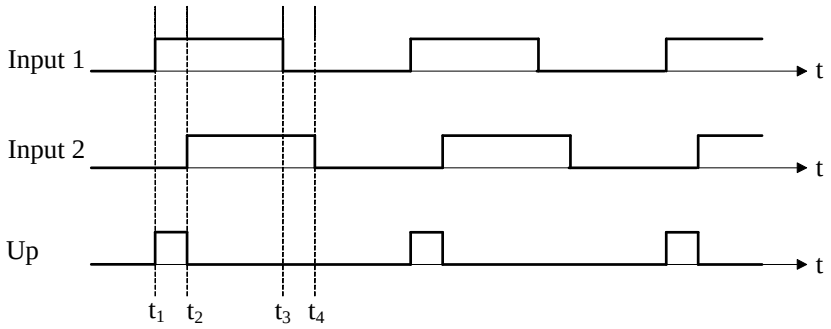

Figure 9.6: Signals of PFD when the estimated reference angle is lagging.

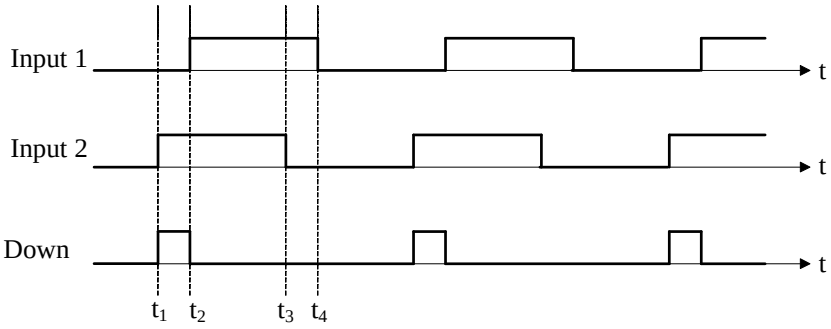

Figure 9.7: Signals of PFD when the estimated reference angle is leading.

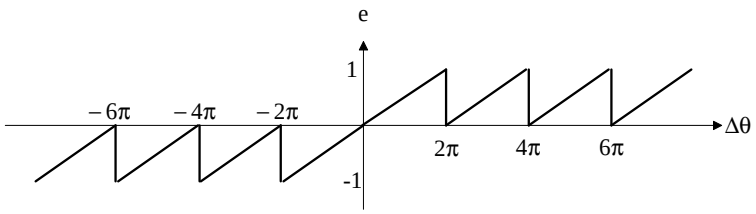

Figure 9.8: Output characteristic of the PFD circuit.

If the phase voltage v_a is distorted, there may be more than one zero crossing due to voltage harmonics or voltage transients, as can be seen from Fig. 9.9a. The pulse train generated by the PLL will not have multiple rising edges, since the estimated reference angle $\widehat{\theta}$ is always rising, provided the estimated angle velocity $\widehat{\omega} > 0$. The reference angle ramp will have a bulky shape, as Fig. 9.9b shows, but the slope is always positive.

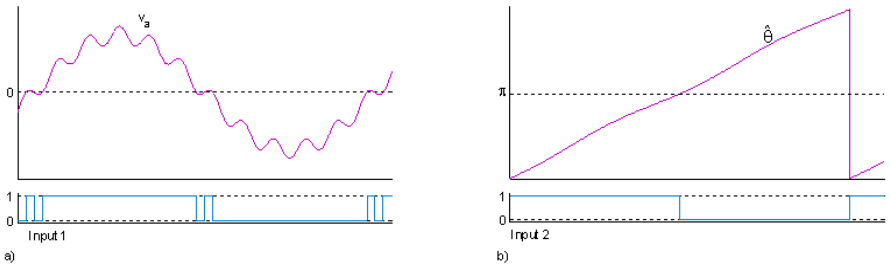

Figure 9.9: Pulse generation during distorted signal conditions.

Fig. 9.10 shows a case where the Input 1 signal is distorted and leading. At times t_1 and t_2 the circuit behaves as expected, giving a short Up pulse. A t_3 an unexpected rising edge of Input 1 causes a prolonged Up pulse, sustained until t_4. The output signal is not proportional to the angle displacement between the input signals. Fig. 9.11 shows an even more disorderly case, where the distorted Input 1 signal is lagging. At t_1 a Down pulse is initiated and ended at t_2, as expected. At t_3 a rising edge of Input 1 generates an Up signal, lasting until t_4. At t_4 a new Down pulse should have started. Instead a new Up pulse starts at t_5. The signals are not proportional to the angle displacement, and the Up signal dominates, whereas the Down signal should be the only present output signal in this case.

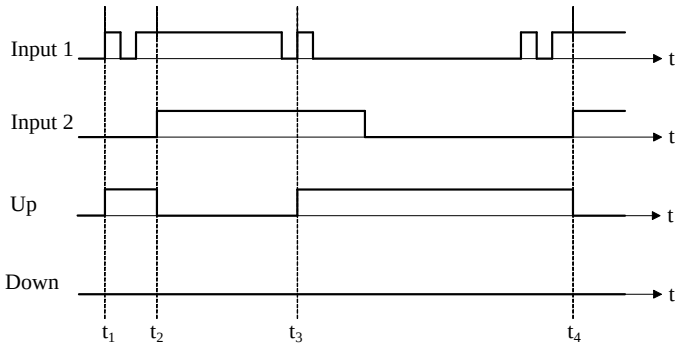

Figure 9.10: Distorted zero detection signal with lagging estimated reference angle.

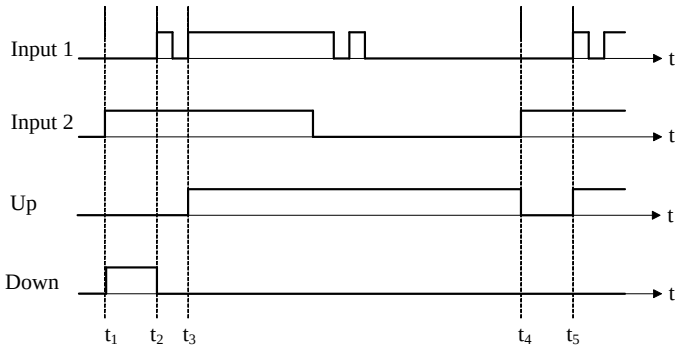

Figure 9.11: Distorted zero detection signal with leading estimated reference angle.

Another disadvantage with the zero crossing detection method is that no information about the grid is available between the zero crossings. The PFD only detects the rising edges of the input signals, and it takes $20\,\mathrm{ms}$ between each information update as long as the grid frequency is $50\,\mathrm{Hz}$.

Using a PI controller as a loop filter (LF) is beneficial, in order to minimize the static error. The error signal derived from the Up and Down signals is expressed in equation (9.9):

$$e = \begin{cases} 1 \text{ if Up is } 1 \\ -1 \text{ if Down is } 1 \\ 0 \text{ if Up and Down are } 0 \end{cases} \tag{9.9}$$

The transfer function of the PI controller is given in equation (9.10). The integrator is realized by means of an up/down counter. The integration time constant is dependent on the clock frequency and the resolution of the counter. A block diagram of the integrator is shown in Fig. 9.12.

$$H_{LF}(s) = k_p + \frac{k_i}{\tau_i s} \tag{9.10}$$

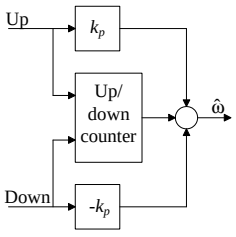

Figure 9.12: Simplified block diagram of the loop filter.

The estimated angular velocity $\widehat{\omega}$ is put into a numerically controlled oscillator (NCO) which acts as an accumulator, according to equation (9.11). The circuit is depicted in Fig. 9.13.

$$\begin{aligned} x_{k+1} &= x_k + \Delta x \\ \Delta x &= k_1 \widehat{\omega} \\ \widehat{\theta} &= k_2 x \end{aligned} \tag{9.11}$$

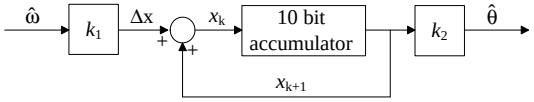

Figure 9.13: Block diagram of numerically controlled oscillator.

The constant k_1 scales down the angular velocity $\widehat{\omega}$ to a proper increment Δx. It depends both on the resolution of the accumulator and the sampling frequency f_s of the calculation in equation (9.11). The constant k_2 scales down the accumulator integer value to an angular representation. Equation (9.12) expresses k_1 and k_2 for an accumulator with 10 bit resolution.

$$\begin{aligned} k_1 &= \frac{1024}{f_s} \\ k_2 &= \frac{2\pi}{1024} \end{aligned} \tag{9.12}$$

9.4 Three-phase design

In a three-phase system with zero crossing detection on each phase voltage, six edges are available during a whole period, reducing the information update time to $3.33\,\mathrm{ms}$. As long as the three-phase voltages are balanced, zero crossing detection of all three line voltages will give the same result. This approach is used in [37]. In Fig. 9.4 the estimated reference angle is 90° ahead of the phase voltage v_a. The pulse train of the line voltage v_{bc} is in phase with phase voltage v_a, as can be seen from Fig. 9.14. By generating zero crossing pulse trains for each line voltage, plus inverted pulse trains, all the signals on the lower part of Fig. 9.14 are generated.

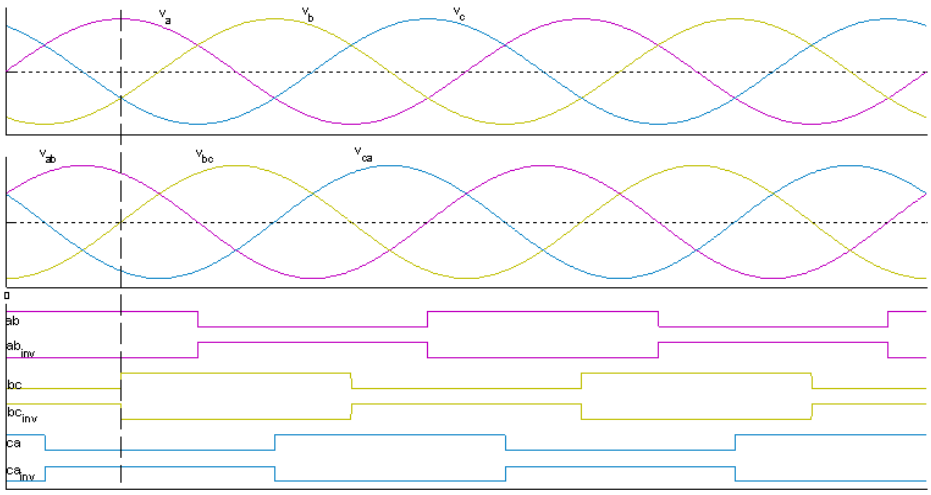

Figure 9.14: From the top: phase voltages, line voltages and zero crossing signals.

In addition to the estimated reference angle $\widehat{\theta}$, two other angles are generated, as expressed in equation (9.13):

$$\begin{aligned} \widehat{\theta}' &= \widehat{\theta} - \tfrac{2\pi}{3} \\ \widehat{\theta}'' &= \widehat{\theta} - \tfrac{4\pi}{3} \end{aligned} \tag{9.13}$$

Pulse signals for these angles are generated using equation (9.7). Both the inverted and non-inverted signals are matched with the pulse signals on Fig. 9.14, using six PFD circuits. These signals are joined together as shown on Fig. 9.15.

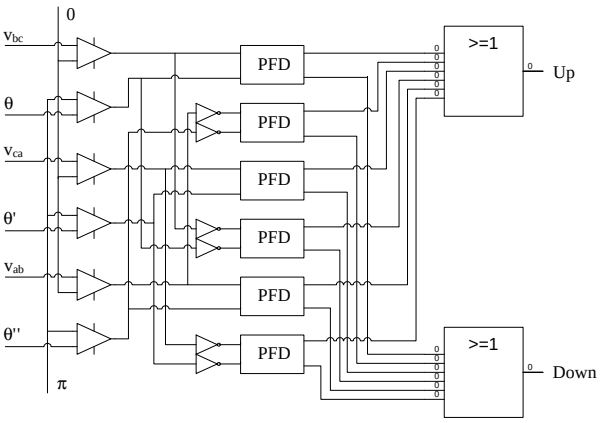

Figure 9.15: Three-phase PFD circuit.

The complete three-phase PLL is shown in Figure 9.16.

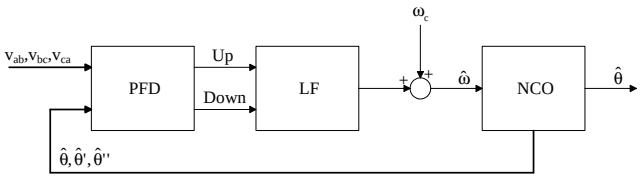

Figure 9.16: Block diagram of three-phase PLL.

9.5 Stability analysis

Figure 9.8 shows that the mean value of the output signals from the PFD is piecewise linear, but according to equation (9.9), the instantaneous value of these signals is non-linear. Choosing a low-pass filter as an LF instead of the PI controller would allow a more smooth estimated angular velocity ω, but would reduce the response of the PLL. Such a solution would also bring about a static error of the control loop.

Linearizing the PLL around $\Delta\theta = 0$ would be an acceptable approximation, since the state variable $\widehat{\theta}$ will be further filtered by the inherent integral in the NCO. The PFD can then be modelled as equation (9.14):

$$H_{PFD}(s) = \frac{1}{2\pi} \tag{9.14}$$

The transfer function of the open loop is given in equation (9.15):

$$H_{PLL,open}(s) = H_{PFD}(s) H_{LF}(s) H_{NCO}(s) = \frac{1}{2\pi}\left(k_p + \frac{k_i}{\tau_i s}\right)\frac{1}{s} = \frac{k_p \tau_i s + k_i}{2\pi\tau_i s^2} \tag{9.15}$$

Closing the loop yields the following transfer function equation (9.16):

$$H_{PLL}(s) = \frac{H_{PLL,open}(s)}{1 + H_{PLL,open}(s)} = \frac{\frac{k_p}{2\pi}s + \frac{k_i}{2\pi\tau_i}}{s^2 + \frac{k_p}{2\pi}s + \frac{k_i}{2\pi\tau_i}} = \frac{2\zeta\omega_n s + {\omega_n}^2}{s^2 + 2\zeta\omega_n s + {\omega_n}^2} \tag{9.16}$$

where $\omega_n = \sqrt{\frac{k_i}{2\pi\tau_i}}$ and $\zeta = \sqrt{\frac{{k_p}^2\tau_i}{8\pi k_i}}$.

10 Pulse Width Modulated Converters

Voltage and current source inverters are described. Different modulation strategies are considered. Some vector control theory is presented. An experimental setup is described and tested for different disturbances.

10.1 Converter topology

The two main classes of active converters are the voltage source inverter (VSI) and the current source inverter (CSI) depicted on Fig. 10.1a and b, respectively. In this thesis, the VSI converter is further investigated and utilized. The circuit uses pulse width modulation (PWM) to generate AC output voltages, and the power flow can go in both directions, meaning that the circuit can operate both as a rectifier and an inverter. Usually insulated gate bipolar transistors (IGBT) are used for this circuit.

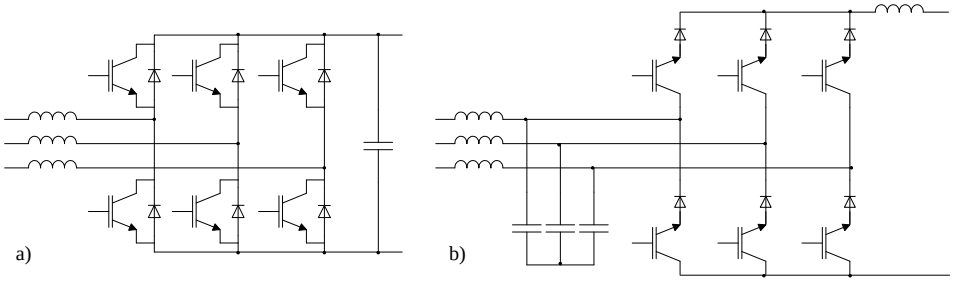

Figure 10.1: Active converter topologies: a) voltage source inverter; b) current source inverter.

The active PWM converter has eight switching states which is described in [38]. These are shown in Table 10.1. S_a, S_b and S_c are the switching states of phase a, b and c, respectively.

Table 10.1: Switching states of PWM converter

Voltage vector	S_a	S_b	S_c	v_a	v_b	v_c
0	0	0	0	$-\frac{1}{2}V_{dc}$	$-\frac{1}{2}V_{dc}$	$-\frac{1}{2}V_{dc}$
1	1	0	0	$\frac{1}{2}V_{dc}$	$-\frac{1}{2}V_{dc}$	$-\frac{1}{2}V_{dc}$
2	1	1	0	$\frac{1}{2}V_{dc}$	$\frac{1}{2}V_{dc}$	$-\frac{1}{2}V_{dc}$
3	0	1	0	$-\frac{1}{2}V_{dc}$	$\frac{1}{2}V_{dc}$	$-\frac{1}{2}V_{dc}$
4	0	1	1	$-\frac{1}{2}V_{dc}$	$\frac{1}{2}V_{dc}$	$\frac{1}{2}V_{dc}$
5	0	0	1	$-\frac{1}{2}V_{dc}$	$-\frac{1}{2}V_{dc}$	$\frac{1}{2}V_{dc}$
6	1	0	1	$\frac{1}{2}V_{dc}$	$-\frac{1}{2}V_{dc}$	$\frac{1}{2}V_{dc}$
7	1	1	1	$\frac{1}{2}V_{dc}$	$\frac{1}{2}V_{dc}$	$\frac{1}{2}V_{dc}$

If the switching state is 1, the phase is connected to the plus pole of the DC voltage. If the switching state is 0, the phase is connected to the minus pole. The resulting instantaneous phase voltages are named v_a, v_b and v_c. Voltage vector 0 connects all phases to

the minus pole, thereby giving no power transfer through the converter. Voltage vector 7 connects all phases to the plus pole, giving no power transfer. The line voltages of the converter will also be zero, using the above mentioned vectors. Consequently these vectors are called zero vectors. During these switching stages (zero vectors), the line inductances shown in Fig. 10.1 avoid short-circuiting the three-phase voltage source.

Fig. 10.2 shows the relationship between the phase voltages of the grid and the operating area of the different voltage vectors. The areas are fuzzy, because they depend both on the power flow and voltage level, and zero vectors will also be used to keep the converter output voltage at a proper level.

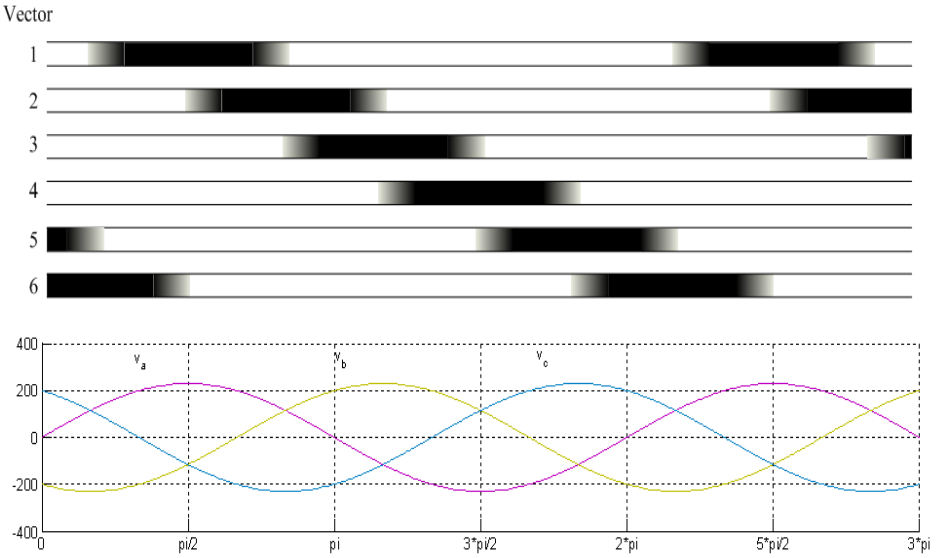

Figure 10.2: Relationship between grid phase voltages and voltage vectors.

Fig. 10.3 shows a grid connected PWM rectifier with a DC load. R and L represent line resistance and inductance, respectively. Fig. 10.4 is a single phase representation of the circuit. v_{grid} is the phase voltage on the strong grid, and v_{conv} is the mean value of the converter phase voltage. The voltage drops over the line resistance and line inductance are expressed as $i \cdot R$ and $i \cdot j\omega L$, respectively. Phasor diagram of the circuit is shown in Fig. 10.5 for operation at unity power factor (UPF). Fig. 10.5a shows *rectifier mode*, and Fig.10.5b shows *inverter mode*. The angle ε is named control phase angle and represents the angle between grid voltage and converter voltage.

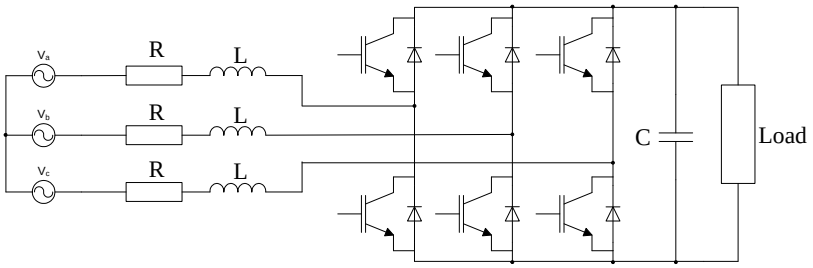

Figure 10.3: Grid connected three-phase PWM rectifier.

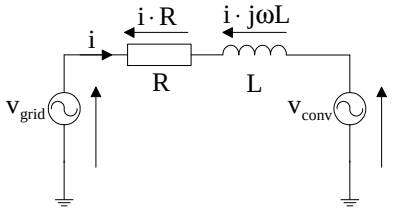

Figure 10.4: Single phase representation of grid connected rectifier.

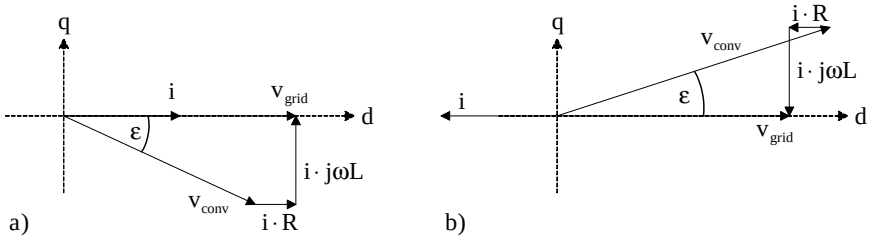

Figure 10.5: Phasor diagram for the PWM rectifier at unity power factor: a) *rectifier mode*, b) *inverter mode.*

According to [39], the mathematical description of the grid connected PWM inverter in a synchronous reference frame is expressed in equation (10.1) and equation (10.2):

$$\begin{aligned} v_{grid,d} &= Ri_d + L\frac{di_d}{dt} - \omega L i_q + v_{conv,d} \\ v_{grid,q} &= Ri_q + L\frac{di_q}{dt} + \omega L i_d + v_{conv,q} \end{aligned} \tag{10.1}$$

$$C\frac{dv_{dc}}{dt} = (i_d S_d + i_q S_q) - i_{dc} \tag{10.2}$$

The switching states S_d and S_q are defined in equation (10.3):

$$\begin{aligned} S_d &= S_\alpha \cos\omega t + S_\beta \sin\omega t \\ S_q &= S_\beta \cos\omega t - S_\alpha \sin\omega t \\ S_\alpha &= \frac{1}{\sqrt{6}}(2S_a - S_b - S_c) \\ S_\beta &= \frac{1}{\sqrt{2}}(S_b - S_c) \end{aligned} \tag{10.3}$$

10.2 Modulation strategies

The PWM can be performed in two ways, either as carrier based PWM (CB-PWM) or space vector modulation (SVM). These methods give the same result, but in different ways. Several modulation strategies can be carried out on any of the above mentioned method [40]. The simplest strategy is sinusoidal PWM, which is shown on Fig. 10.6.

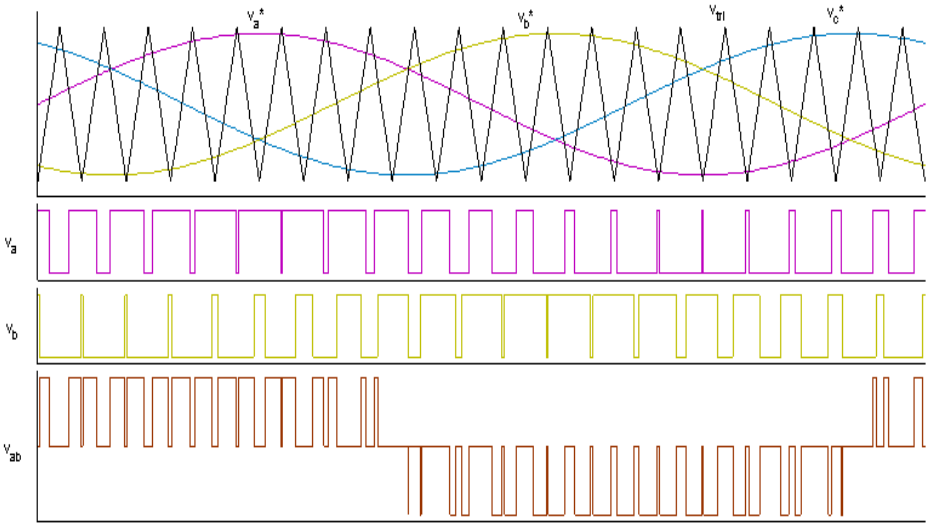

Figure 10.6: Waveforms of sinusoidal CB-PWM.

Another common modulation strategy is sinusoidal PWM with 3rd harmonic injection [41]. It is expressed by equation (10.4) and depicted in Fig. 10.7.

$$\begin{aligned} {v_a}^* &= V\left(\sin(\omega t) + M_3 \sin(3\omega t)\right) \\ {v_b}^* &= V\left(\sin\left(\omega t - \tfrac{2\pi}{3}\right) + M_3 \sin(3\omega t)\right) \\ {v_c}^* &= V\left(\sin\left(\omega t - \tfrac{4\pi}{3}\right) + M_3 \sin(3\omega t)\right) \end{aligned} \tag{10.4}$$

V is the amplitude of the fundamental voltage component, and M_3 is the relative injection of third harmonic voltage. According to [42], the highest sinusoidal voltage output is obtained when $M_3 = \frac{1}{6}$.

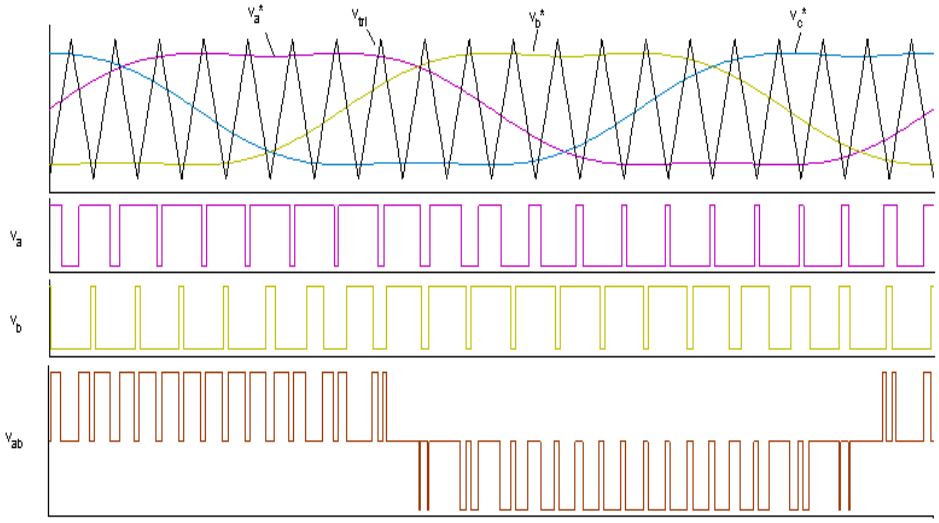

Figure 10.7: Waveforms of sinusoidal CB-PWM with third harmonic injection.

10.3 Vector control theory

Balanced three-phase voltages or currents can be modelled by a space vector. The phase voltages or currents are shifted 120° and then added to each other. The resulting space vector is doing one revolution per grid period. For voltages this is purely a theoretical model, while the current space vector has a physical representation in the induction machine. Each phase winding is shifted 120° and the magnetizing current components are generating an air gap field concurrent to the current vector of these components.

Balanced three-phase currents can be expressed as equation (10.5):

$$\begin{aligned} i_a &= I_m \sin(\omega t - \varphi) \\ i_b &= I_m \sin\left(\omega t - \tfrac{2\pi}{3} - \varphi\right) \\ i_c &= I_m \sin\left(\omega t - \tfrac{4\pi}{3} - \varphi\right) \end{aligned} \tag{10.5}$$

where I_m is the current amplitude and φ is the phase angle between voltages and currents.

If φ is chosen to be zero, and ωt has an instantaneous value $\omega t = 0$, then $i_a = I_m$, $i_b = -0.5I_m$ and $i_c = -0.5I_m$. The resulting space vector is shown in Fig. 10.8. This is obtained by the Clark Transform equation (9.2).

So far in this thesis, the grid voltages and currents have been observed in a stationary reference frame, either three-phase (abc) or stationary two-axis representation ($\alpha\beta$). In both cases, the signals are AC signals and the constantly changing values makes it more difficult to design proper control loops. By choosing a synchronous reference frame synchronized to the voltage space vector, the voltages and currents appear as DC signals, which are easier to control.

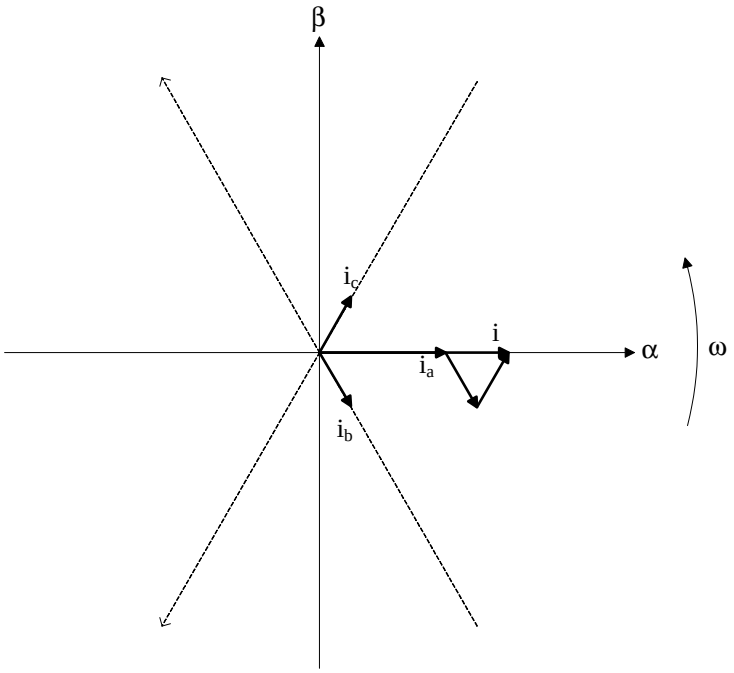

Figure 10.8: Current space vector in stationary reference frame.

Fig. 10.9 shows the relationship between the stationary and the synchronous reference frame. The projection of the space current vector at the stationary reference frame consists of the components i_α (real axis) and i_β (imaginary axis). The projection at the synchronous reference frame consists of the active current component i_d and the reactive current component i_q. The conversion from stationary to synchronous reference frame is obtained by means of the Park transform, expressed in equation (10.6):

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \tag{10.6}$$

In Fig. 10.9 the voltage vector is chosen as the synchronous reference, and the respective current control is named voltage oriented control (VOC). Another control strategy is named virtual flux oriented control (VFOC) [44]. The idea is to regard the grid as a virtual electric machine and to estimate a virtual flux, based on the grid voltages. Another control strategy is to calculate active and reactive power flow and to use a direct power control (DPC) [43].

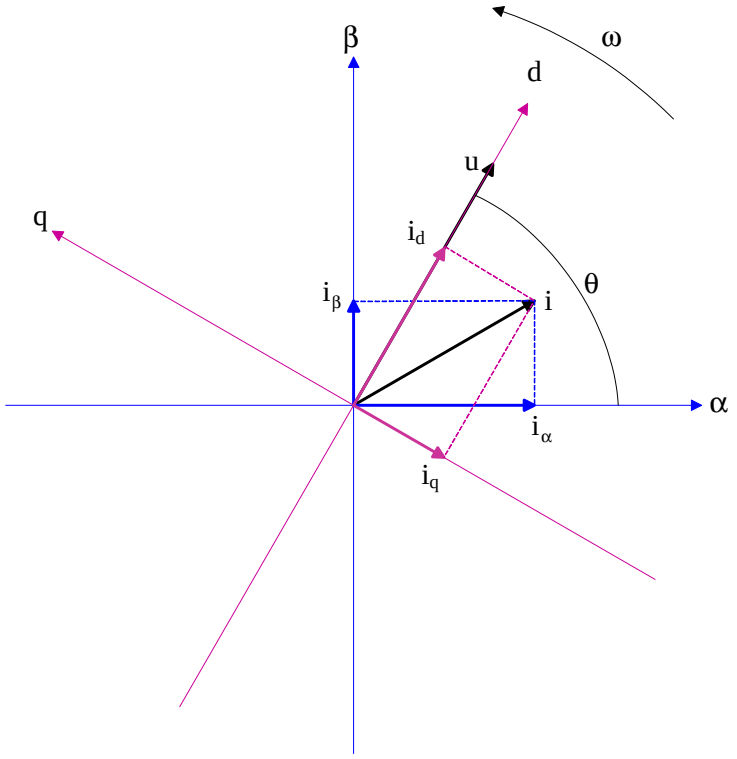

Figure 10.9: Relationship between stationary and synchronous reference frames.

10.4 Voltage oriented control

Fig. 10.10 shows a block diagram of an active rectifier with VOC current control. The grid connection is a three-wire connection with an isolated neutral point. Then equation (10.7) applies for the grid voltages and currents and it is sufficient to measure two line voltages and two line currents.

$$\begin{aligned} v_{ab} + v_{bc} + v_{ca} &= 0 \\ i_a + i_b + i_c &= 0 \end{aligned} \tag{10.7}$$

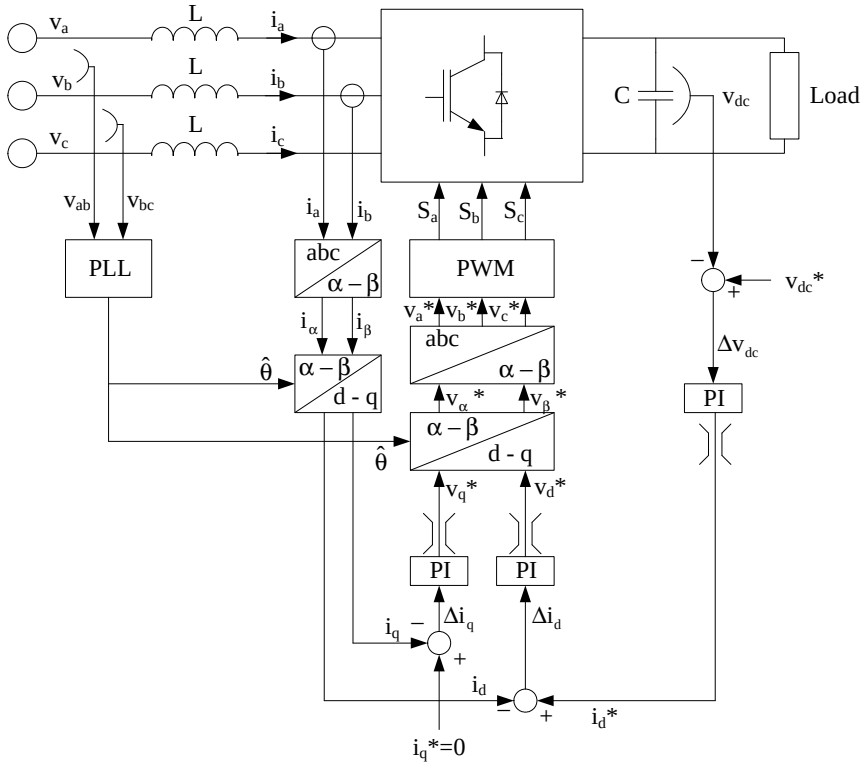

Figure 10.10: Voltage oriented control with unity power factor.

The line voltages are fed into the PLL which outputs the voltage reference angle θ. The line currents are transformed to stationary reference signals $i_{\alpha\beta}$ in equation (9.2) and to synchronous reference signals i_{dq} in equation (10.6). The active current reference value $i_d{}^*$ is the output value of the dc voltage controller. If the dc voltage v_{dc} is dropping, more active power is to be supplied to the converter, and the reference value $i_d{}^*$ will rise. The reactive current reference value $i_q{}^*$ is zero, in order to keep $\cos\varphi = 1.0$. The current controllers output the reference voltages $v_d{}^*$ and $v_q{}^*$. These are transformed to stationary reference frame and to three-phase properties and inputted to the PWM. The switching signals S_a, S_b and S_c controls the IGBT transistors. All controllers are PI-controllers, in order to minimize the static errors of the line currents and the dc voltage.

There is a coupling between the d and q axis currents, and it is easily observed in equation (10.8):

$$\begin{aligned} v_{grid,d} &= Ri_d + L\frac{di_d}{dt} - \omega L i_q + v_{conv,d} \\ v_{grid,q} &= Ri_q + L\frac{di_q}{dt} + \omega L i_d + v_{conv,q} \end{aligned} \tag{10.8}$$

The PLL will keep the voltage $v_{grid,q} = 0$. Since the line reactance will be much bigger than the resistance, the following assumption can be done: $R \approx 0$. At UPF the current component $i_q = 0$. Assuming that this is true, equation (10.8) can be simplified:

$$\begin{aligned} v_{grid,d} &= L\frac{di_d}{dt} + v_{conv,d} \\ 0 &= \omega L i_d + v_{conv,q} \end{aligned} \tag{10.9}$$

According to [45], a decoupling structure should be added to the current control loops, as shown in equation (10.10) and Fig. 10.11.

$$\begin{aligned} {v_d}^* &= \omega L i_q + v_{grid,d} + \Delta v_d \\ {v_q}^* &= -\omega L i_d + \Delta v_q \end{aligned} \tag{10.10}$$

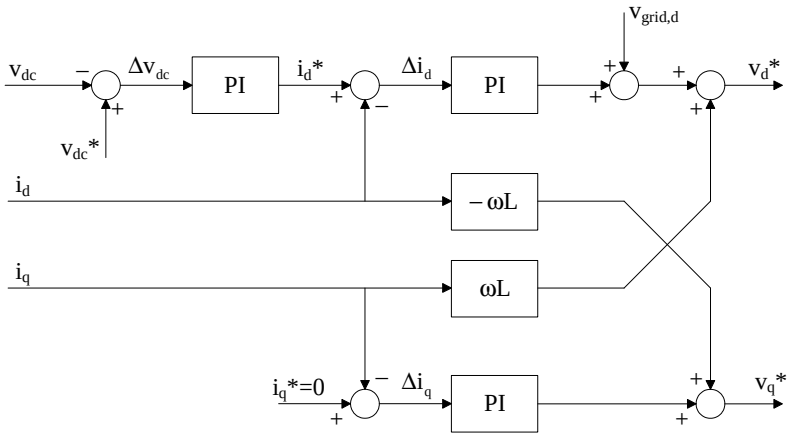

Figure 10.11: Decoupled current control of a PWM rectifier.

10.5 Experimental setup

A field-programmable gate array (FPGA) is a device built up of I/O blocks, logic blocks and programmable interconnects. A simplified FPGA structure is described in Fig. 10.12. Due to its hardware structure, the FPGA is a very fast and robust circuit. One of the major disadvantages, however, is that any floating point calculation is prohibited.

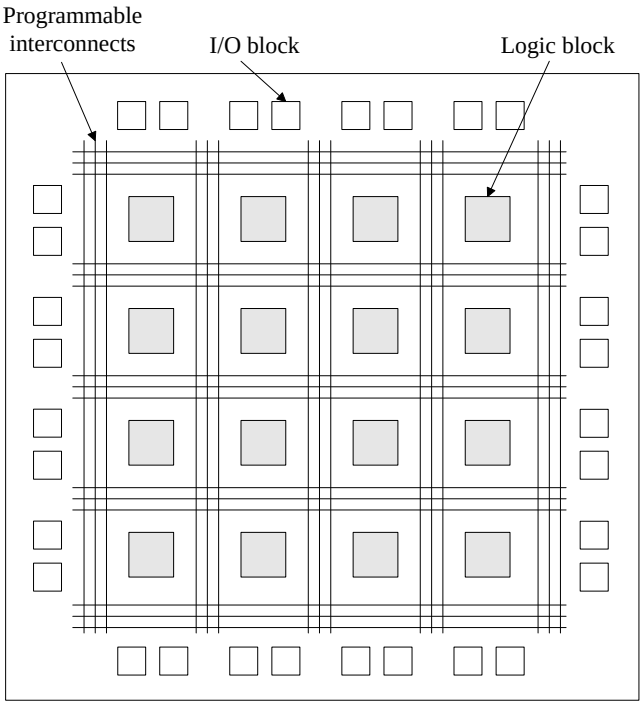

Figure 10.12: Simplified block diagram of field-programmable gate array.

The PLL design described in Chapter 9.4 is implemented using a Xilinx 4003 FPGA circuit with a clock frequency of $8.0\,\mathrm{MHz}$. The work is described in [37]. In this work, a low-pass filter is chosen as LF, to make the circuit less sensitive to the non-linear behavior of the PFD. The circuit is connected to a strong grid, and as long as the center frequency ω_c of the NCO is chosen to be 100π, which is in accordance with a grid frequency of $50\,\mathrm{Hz}$, the static error will be negligible. The transfer functions of the PFD and the LF are given in equations (10.11) and (10.12), respectively.

$$H_{PFD}(s) = k_{PFD} \tag{10.11}$$

$$H_{LF}(s) = \frac{1}{\tau_{LF} s + 1} \tag{10.12}$$

The constants were chosen to be $k_{PFD} = 97.66$ and $\tau_{LF} = 6.7\,\mathrm{ms}$. The transfer function of the open loop is given in (10.13), and closing the PLL gives the transfer function

expressed by equation (10.14). A Bode diagram of the PLL is shown in Fig. 10.13. The bandwidth of the PLL is about 20 Hz, and it shows good stability. A slower LF would reduce the noise sensitivity of the PLL, but the non-linearities mentioned in Chapter 9.3 could make the loop unstable outside the region of normal operation, especially during startup.

$$H_o(s) = H_{PFD}(s) H_{LF}(s) H_{NCO}(s) = k_{PFD} \frac{1}{\tau_{LF} s + 1} \frac{1}{s} = \frac{k_{PFD}}{\tau_{LF} s^2 + s} \quad (10.13)$$

$$H_{PLL}(s) = \frac{k_{PFD}}{\tau_{LF} s^2 + s + k_{PFD}} \quad (10.14)$$

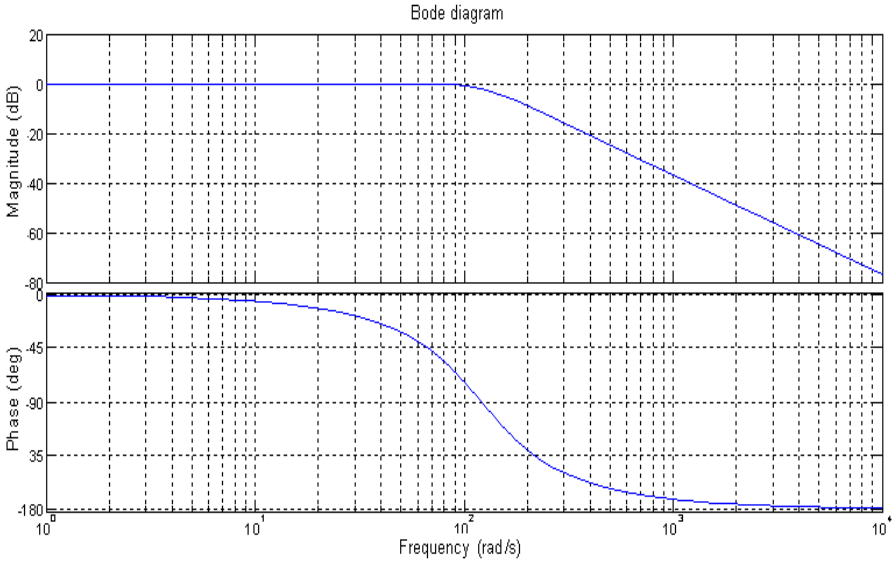

Figure 10.13: Bode diagram of PLL.

The setup described in [37] is shown in Fig. 10.14. The line voltages are fed into a zero voltage detection circuit. The PLL uses these zero crossing signals, as described in Chapter 9.4. The VOC circuit and the PWM are realized in dSpace using MatLab/Simulink software. The full-bridge converter uses IGBT transistors with a switching frequency $f_{sw} = 6.25\,\mathrm{kHz}$. The inductors have an inductance $L = 10\,\mathrm{mH}$ and a resistance $R_L = 35\,\mathrm{m\Omega}$. The capacitor has a value of $C = 2000\,\mu\mathrm{F}$. The reactive current reference $i_q{}^* = 0$ in order to obtain UPF. The DC load is a pure resistive load.

Before testing the whole circuit on Fig. 10.14, some voltage disturbance tests were done on the PLL to test its robustness. The line voltages of this circuit are measured. In order to measure the phase voltages, the circuit on Fig. 10.15 was used. The wye-connected resistances R constitute a balanced load with a virtual neutral point n'. The measured phase voltage v_a is compared to the reference angle $\widehat{\theta}$ outputted from the PLL. The reference angle should be zero when v_a reaches its positive peak value.

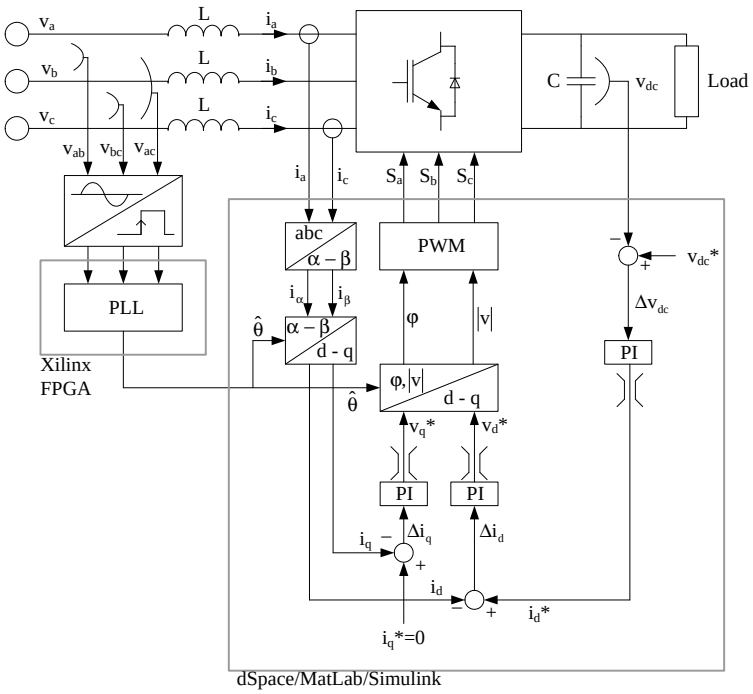

Figure 10.14: PWM rectifier with synchronizing circuit and VOC current control.

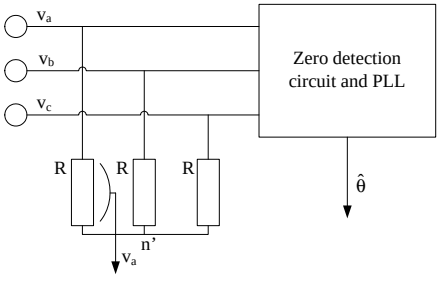

Figure 10.15: Phase voltage measurement using a virtual neutral point.

Voltage sags

The PLL was tested for different grid voltages in order to verify that it will operate even during voltage sags. Fig. 10.16a shows the performance at nominal grid voltage and the plot shows that the reference angle is locked to the phase voltage v_a. It is still locked on Fig. 10.16b, where the voltage has dropped to 75% of its nominal value. On Fig. 10.16a the voltage is just 15% of the nominal voltage. The reference angle is no longer synchronized, and in this case the converter should immediately be disconnected from the grid because of the severe voltage disturbance.

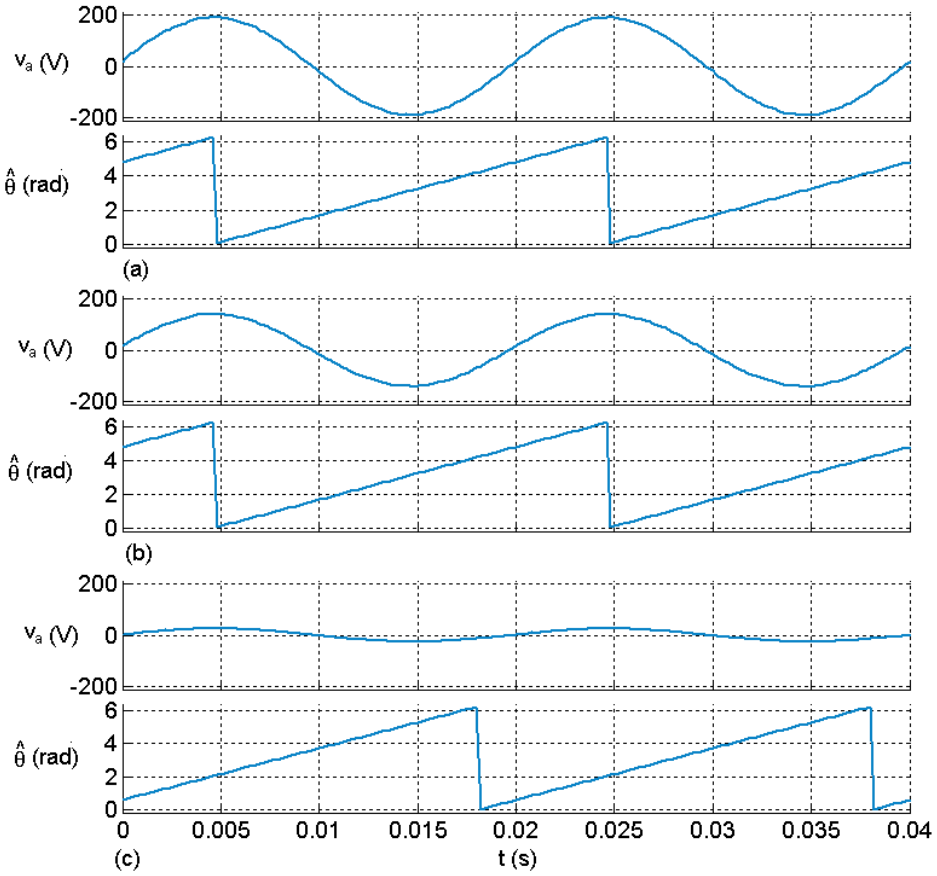

Figure 10.16: Comparison of phase voltage and reference angle: a) nominal voltage, b) 70% of nominal voltage, c) 15% of nominal voltage.

Frequency deviation

The PLL was also tested for frequency deviations from the nominal grid frequency of $50\,\mathrm{Hz}$. Fig. 10.17a shows the behavior of the PLL at a frequency of $49\,\mathrm{Hz}$, and 10.17b at $53\,\mathrm{Hz}$. A synchronous machine was used to generate the voltage. The slightly distorted sine waves could explain why the angle θ diverts slightly from the phase voltage v_R. It has been observed that the PLL locks properly for both $49\,\mathrm{Hz}$ and $53\,\mathrm{Hz}$, which are both beyond the limits of normal operation.

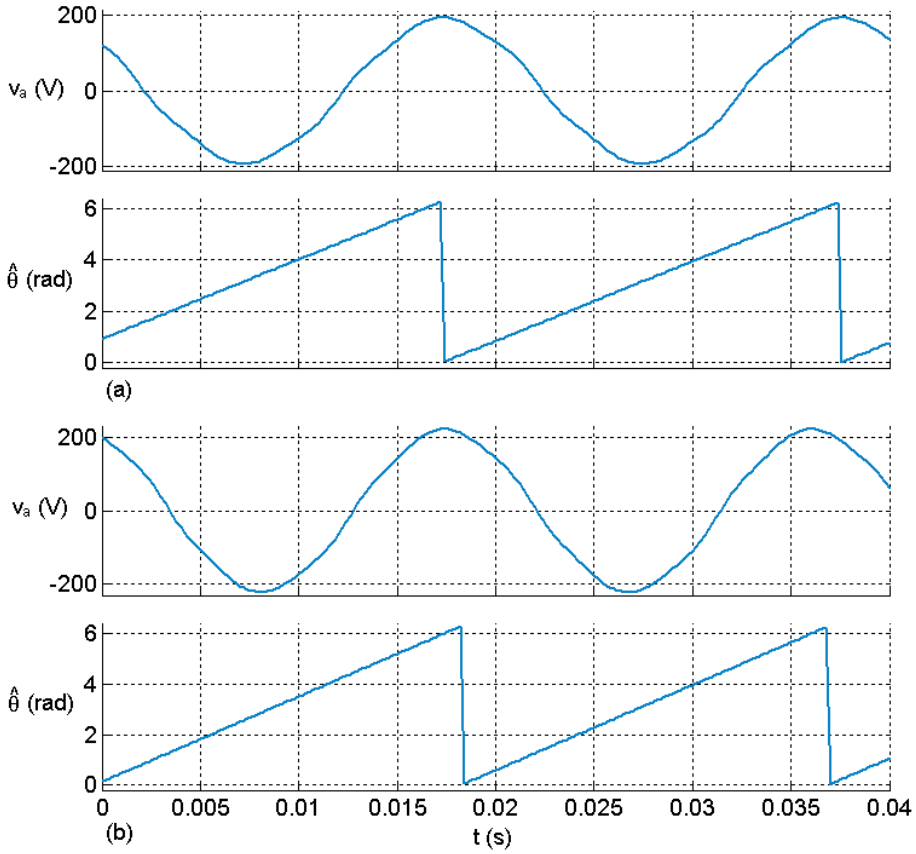

Figure 10.17: Comparison of phase voltage and reference angle for different frequencies: a) $49\,\mathrm{Hz}$, b) $53\,\mathrm{Hz}$.

DC reference step change

The DC voltage is controlled independently, as shown in Fig. 10.14. A step change of the DC voltage reference will increase the line currents. To examine the dynamic behavior of the system, a DC voltage reference step change was introduced. The result is shown in Fig. 10.18. The DC voltage has some overshot before it settles. The input currents increase during a transient period before they take a new stationary value. This increase matches well with the shape of the active current component i_d. The power factor deviates significantly from $\cos\varphi = 1.0$ during the voltage change, which can be seen by the temporary increase in the reactive current component i_q. The decoupling structure described in Fig. 10.11 would have reduced this unintentional reactive power flow.

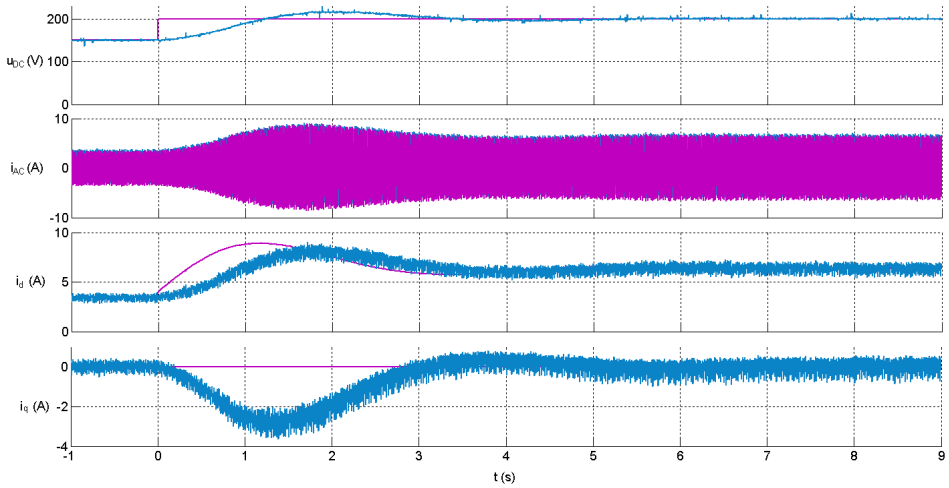

Figure 10.18: DC voltage reference step change. From the top: DC voltage, AC currents, active current component i_d, and reactive current component i_q.

Stepwise load change

Another sudden change that perturbs the system is a load step acting as a dynamic disturbance. In Fig. 10.19 the results of this step is shown. The load increase results in a significant voltage drop. Afterwards, the voltage smoothly returns to its reference value. The AC increases considerably and displays an irregular pattern during the transient period. The active current component i_d is almost proportional to the DC voltage, because the active AC current component coincides with the DC current. During the voltage drop a significant reactive current component i_q appears, but it vanishes as the DC voltage is fully restored.

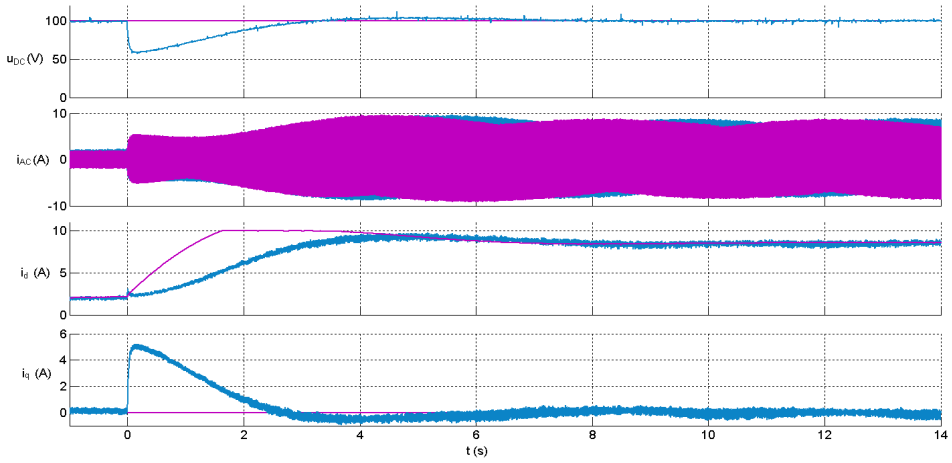

Figure 10.19: Stepwise load increase. From the top: DC voltage, AC currents, active current component i_d, and reactive current component i_q.

Current harmonics content

An oscilloscope with a Fast Fourier Transform (FFT) function was used to generate a frequency spectrum for the line currents. The result is shown in Fig. 10.20.

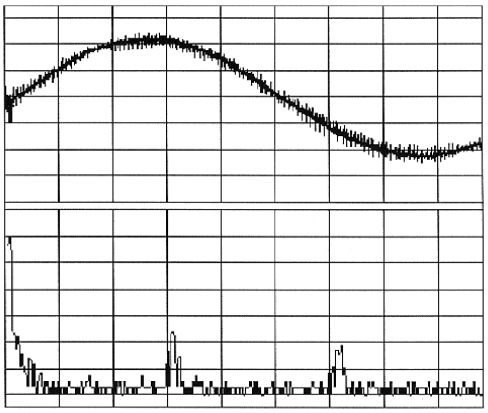

Figure 10.20: Spectrum analysis based on FFT of the input line current.

Each bin along the x-axis represents a frequency interval $\Delta f = 2\,\mathrm{kHz}$, and each bin along the y-axis represents an amplitude ratio of $11.8dB$. The spectrum displays significant peaks for the fundamental frequency $f_1 = 50\,\mathrm{Hz}$ and for the switching frequency $f_{sw} = 6.25\,\mathrm{kHz}$. Fig. 10.20 shows an amplitude ratio of approximately $42dB$ between the fundamental current component i_1 and the current switching ripple corresponding to the 125th harmonic i_{125}. A ratio of $42dB$ implies that the switching ripple is 0.8% of the fundamental current. According to [46] the 125th harmonic current should be $\leq 0.6\%$ of the fundamental current for equipment with $i_{AC} > 16\,\mathrm{A}$. For equipment with $i_{AC} \leq 16\,\mathrm{A}$, the content of the 125th harmonic is not defined. As earlier mentioned, the inductances $L = 10\,\mathrm{mH}$, which give quite a strong boost of the rectifier, so the inductances should not be increased. Increasing the switching frequency is a better way to reduce the switching ripple, as long as the dynamic switching losses are kept within acceptable limits.

Fig. 10.18 and 10.19 reveal that there are some overshoots present. By fine-tuning the controllers and including a de-coupling circuit, these overshoots may be reduced, possibly at the expense of the response time.

Robustness

Line current transients occasionally occurred, sometimes causing protective relay tripping. These disturbances are described in [47]. Fig. 10.21 shows an occurrence of PLL malfunction, probably caused by multiple zero crossings as described in Chapter 9.4. The pronounced peak of the reactive current i_q is a direct result of the disturbance on the voltage reference angle θ. An improved design of the PLL is needed in order to obtain an improved robustness of the system.

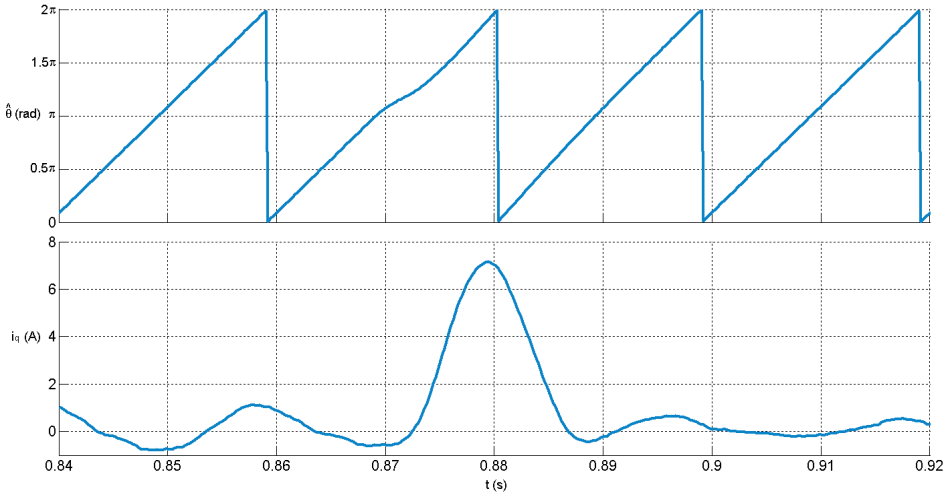

Figure 10.21: Comparison of reactive current component i_q (upper plot) and voltage reference angle $\widehat{\theta}$ (lower plot) during PLL malfunction.

Experiments show that apart from the above mentioned PLL malfunction, the rectifier satisfies the requirements and performs well, with UPF and quite low content of current harmonics.

11 Robust PLL

An alternative PLL design based on voltage vector control in synchronous reference frame is presented. The design is modelled and analyzed. A robust solution based on a multivariable filter is then presented. Finally the design is built and partly tested.

11.1 Synchronous reference frame

In Chapter 9.4 a PLL using zero voltage detection was described. Another approach is to use a PLL based on voltage vector control in a synchronous reference frame, as described in [48]. The major advantage is that information about the grid voltages is available at any time. The voltage vector control design requires more space and computation power, however, thus the design is more complex than for the zero voltage detection PLL. Fig. 11.1 shows the design of the PLL. The lower left block represents the Clark transform (9.2), converting the phase voltages to a stationary reference. The multiplications expressed by equation (11.1) perform the quadrature (q-part) of the Park transform in equation (10.6):

$$v_q = -v_\alpha \cdot \sin\widehat{\theta} + v_\beta \cdot \cos\widehat{\theta} \tag{11.1}$$

The control loop consisting of the LF and the NCO keeps the synchronous voltage component v_q close to zero. By using a PI controller as LF, the static error e will be minimized, and thus $v_q = 0$.

If $v_q > 0$, then $e < 0$, and $\widehat{\omega}$ will decrease. When $v_q < 0$, then $e > 0$, and $\widehat{\omega}$ will increase. As a consequence, the positive half cycle of the signal e will have a longer duration than the negative. Gradually $\widehat{\omega}$ will increase until the PLL synchronizes with the grid. Two working points are possible for $v_q = 0$: either $\widehat{\theta} = \theta$ or $\widehat{\theta} = \theta + \pi$, where θ is the angle between the real stationary axis α and the grid voltage vector v_a, whereas $\widehat{\theta}$ is the angle between the α axis and the estimated voltage reference. This is illustrated on Fig. 11.2. On Fig. 11.2a the estimated reference angle is in phase with voltage v_a. If, however, $v_q \neq 0$, the reference angle would drift until it is in an opposite phase with the voltage v_a. This is shown on Fig. 11.2b. Thus there will be a stable equilibrium point at $\widehat{\theta} = \theta + \pi$.

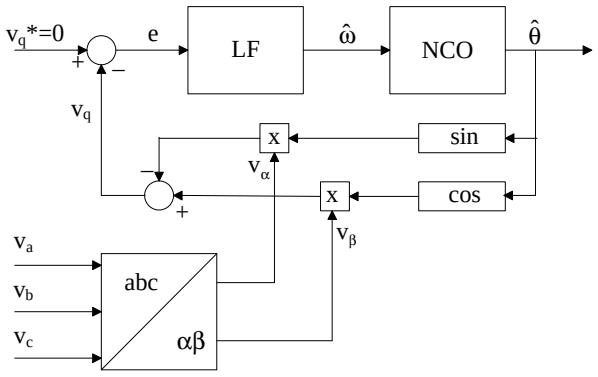

Figure 11.1: PLL with voltage vector control.

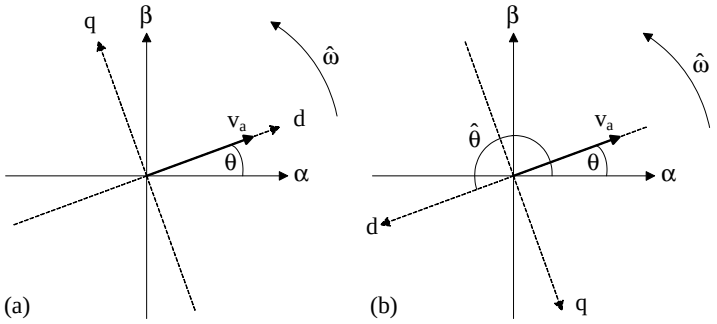

Figure 11.2: Reference angle in synchronous reference frame: a) in phase with voltage v_a, b) in opposite phase.

The reference angle should be in phase with v_a, not in an opposite phase. One solution is to add π to the estimated angle. Another solution is to change the sign of the q-axis signal as in equation (11.2):

$$v_q = v_\alpha \sin\widehat{\theta} - v_\beta \cos\widehat{\theta} \tag{11.2}$$

The solution is shown on Fig. 11.3. If $v_q > 0$, then $e > 0$, and $\widehat{\omega}$ will increase. When $v_q < 0$, then $e < 0$, and $\widehat{\omega}$ will decrease. The PLL reaches a stable equilibrium point at $\widehat{\theta} = \theta$, which is in phase with voltage v_a.

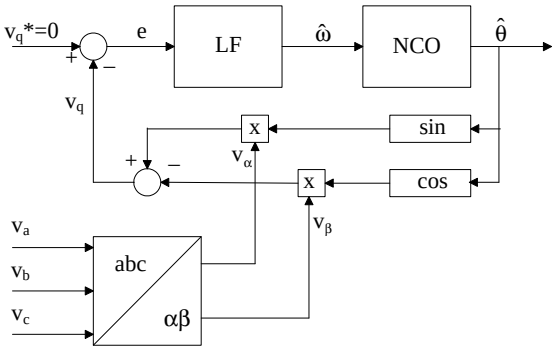

Figure 11.3: PLL with voltage vector control and opposite sign of the q-axis.

The solutions on Fig. 11.1 and 11.3 require quite a long time for the PLL to lock. By adding a center frequency $\omega_c = 100\pi$ to the output of the PI controller, $\widehat{\omega}$ will be initially set at its nominal value. The solution is shown on Fig. 11.4.

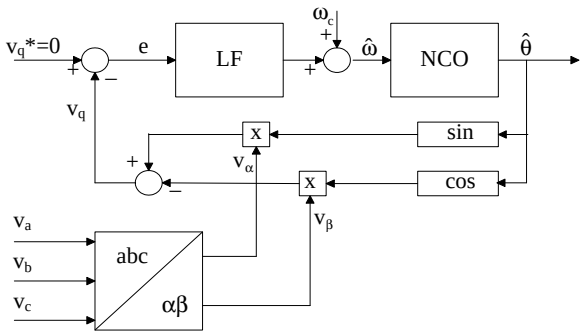

Figure 11.4: PLL with voltage vector control and centre frequency ω_c.

Fig. 11.5 is a comparison between the PLL on Fig. 11.3 (without center frequency) and 11.4 (with centre frequency). It is obvious from the figure that the PLL settles much faster when the center frequency is added to the LF output, as long as the grid frequency is close to its nominal value.

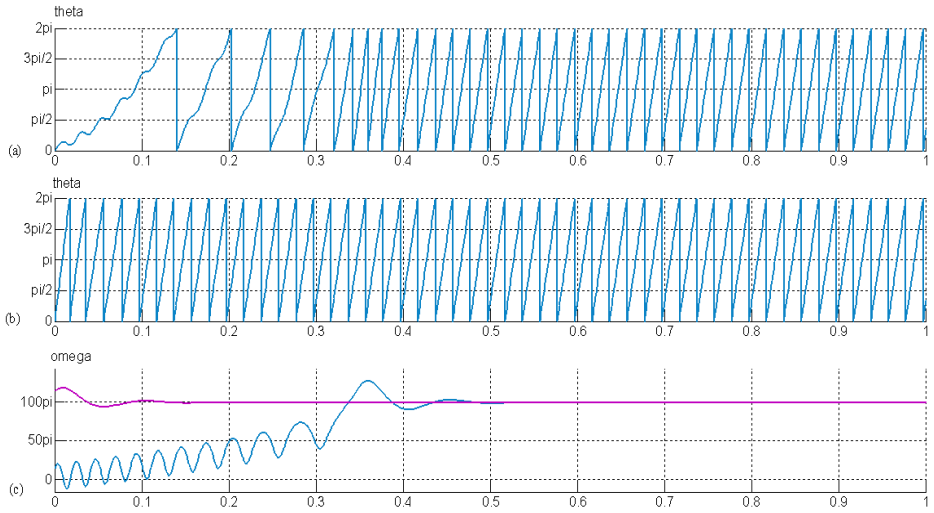

Figure 11.5: Initializing PLL with and without center frequency ω_c. a) Reference angle without ω_c, b) reference angle with ω_c, c) estimated angle velocity omega with ω_c (red) and without (blue).

11.2 Voltage disturbances

Two common voltage disturbances affecting PLL with voltage vector control are voltage harmonics and voltage asymmetry. An analysis of the PLL performance is given in [49], and the current subsection is mainly based on this work.

Voltage harmonics

The distorted grid voltages in this specific case are defined by equation (11.3):

$$\begin{array}{l} v_a = V_m \sin(\omega t) + \frac{V_m}{5}\sin(5\omega t) + \frac{V_m}{7}\sin(7\omega t) \\ v_b = V_m \sin\left(\omega t - \frac{2\pi}{3}\right) + \frac{V_m}{5}\sin\left(5\left(\omega t - \frac{2\pi}{3}\right)\right) + \frac{V_m}{7}\sin\left(7\left(\omega t - \frac{2\pi}{3}\right)\right) \\ v_c = V_m \sin\left(\omega t - \frac{4\pi}{3}\right) + \frac{V_m}{5}\sin\left(5\left(\omega t - \frac{4\pi}{3}\right)\right) + \frac{V_m}{7}\sin\left(7\left(\omega t - \frac{4\pi}{3}\right)\right) \end{array} \tag{11.3}$$

where V_m is the amplitude value of the fundamental voltage component.

The voltage vector in a stationary reference frame is expressed by equation (11.4):

$$\begin{array}{l} v_\alpha = V_m \sin(\omega t) + \frac{V_m}{5}\sin(5\omega t) + \frac{V_m}{7}\sin(7\omega t) \\ v_\beta = -V_m \cos(\omega t) + \frac{V_m}{5}\cos(5\omega t) - \frac{V_m}{7}\cos(7\omega t) \end{array} \tag{11.4}$$

In the synchronous reference frame the direct component will be expressed by equation (11.5):

$$v_d = V_m \sin\left(\theta - \widehat{\theta}\right) + \frac{V_m}{5}\sin\left(5\theta + \widehat{\theta}\right) + \frac{V_m}{7}\sin\left(7\theta - \widehat{\theta}\right) \tag{11.5}$$

where $\theta = \omega t$. For $\theta - \widehat{\theta} \approx 0$, equation (11.5) can be simplified to equation (11.6):

$$v_d \approx V_m\left(\theta - \widehat{\theta}\right) + \frac{12V_m}{35}\sin(6\theta) \tag{11.6}$$

It can be seen from equation (11.6) that an unwanted 6^{th} harmonic component will appear on the active voltage component v_d due to the grid voltage harmonics defined in equation (11.3). Fig. 11.6 illustrates this particular case, and the 6^{th} harmonic component is apparent on the estimated reference angle $\widehat{\theta}$, as can be seen from the upper plot. The grid voltages are heavily distorted, as shown in the lower part of the figure.

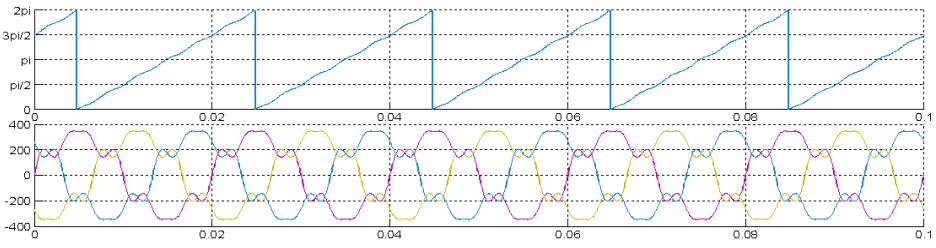

Figure 11.6: PLL performance with voltage harmonics. Upper part: Estimated angle $\widehat{\theta}$. Lower part: Voltage v_a (red), v_b (green), v_c (blue).

Voltage asymmetry
The unbalanced grid voltages are defined by equation (11.7):

$$\begin{aligned} v_a &= V_m \sin(\omega t) \\ v_b &= V_m (1+\beta) \sin\left(\omega t - \tfrac{2\pi}{3}\right) \\ v_c &= V_m (1+\gamma) \sin\left(\omega t - \tfrac{4\pi}{3}\right) \end{aligned} \tag{11.7}$$

where β and γ are constants to create voltage asymmetry.

The stationary reference frame voltage components are defined by equation (11.8):

$$\begin{aligned} v_\alpha &= V_m \sin(\omega t) + \tfrac{V_m}{6}(\beta+\gamma)\sin(\omega t) + \tfrac{\sqrt{3}V_m}{6}(\beta-\gamma)\cos(\omega t) \\ v_\beta &= -V_m \cos(\omega t) + \tfrac{\sqrt{3}V_m}{6}(\gamma-\beta)\sin(\omega t) - \tfrac{V_m}{2}(\beta+\gamma)\cos(\omega t) \end{aligned} \tag{11.8}$$

In a synchronous reference frame this corresponds to equation (11.9):

$$\begin{aligned} v_d = &-V_m \sin\left(\theta - \widehat{\theta}\right) + \tfrac{V_m}{2}(\beta-\gamma)\cos\left(\theta + \widehat{\theta}\right) \\ &+ \tfrac{V_m}{6}(\beta+\gamma)\left[\sin(\theta)\cos\left(\widehat{\theta}\right) - 3\cos(\theta)\sin\left(\widehat{\theta}\right)\right] \end{aligned} \tag{11.9}$$

For $\theta - \widehat{\theta} \approx 0$ the following approximation can be made: $\cos\left(\theta + \widehat{\theta}\right) \approx \cos(2\theta)$, revealing that the voltage v_d contains a 2^{nd} harmonic component. Fig. 11.7 illustrates this particular case, and the 2^{nd} harmonic component is apparent on the estimated reference angle $\widehat{\theta}$, as can be seen from the upper plot. The grid voltages are unbalanced, as shown in the lower part of the figure.

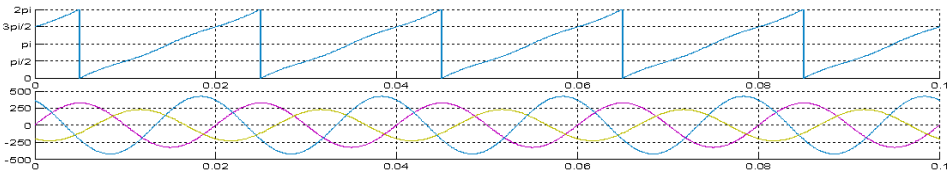

Figure 11.7: PLL performance with voltage asymmetry. Upper part: Estimated angle $\widehat{\theta}$. Lower part: Voltage v_a (red), v_b (green), v_c (blue).

11.3 Robust solutions

There are several different approaches in order to avoid the problems previously discussed. Common to all solutions is some kind of filtering in addition to the inherent filter properties of the PLL. A repetitive controller acting as a Finite Impulse Response (FIR) filter is suggested in [50]. A complex method based on an Adaptive Linear Combiner (ALC) is described in [51]. [49] proposes a multi-variable band-pass filter. Yet another method suggested by the author will be discussed in Chapter 12.5. The multi-variable filter proposed by [49] will be thoroughly described in this section. A practical utilization based on the solution will be presented in Subsection 11.4.

Fig. 11.8 shows a modified design of the PLL with a band-pass filter following the Clark Transform. The filter is tuned at a centre frequency, typical $50\,\mathrm{Hz}$. Voltage harmonics will thereby be attenuated.

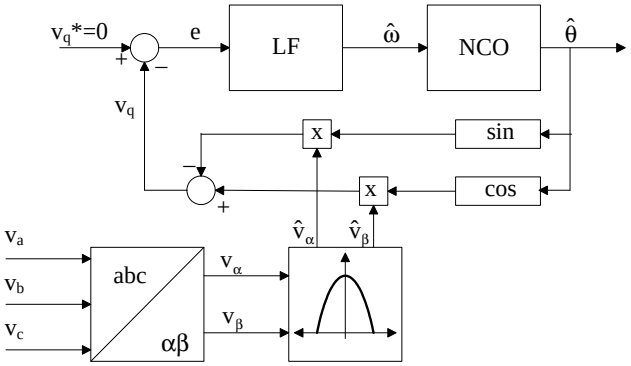

Figure 11.8: PLL with multi-variable band-pass filter.

The function of the filter is described in equation (11.10):

$$\begin{aligned} \widehat{v}_\alpha(s) &= \tfrac{k}{s}\left[v_\alpha(s) - \widehat{v}_\alpha(s)\right] - \tfrac{\omega_c}{s}\widehat{v}_\beta(s) \\ \widehat{v}_\beta(s) &= \tfrac{k}{s}\left[v_\beta(s) - \widehat{v}_\beta(s)\right] + \tfrac{\omega_c}{s}\widehat{v}_\alpha(s) \end{aligned} \tag{11.10}$$

where k is a filter constant and ω_c is the angular velocity of the centre frequency. Fig. 11.9 shows the block diagram of the filter.

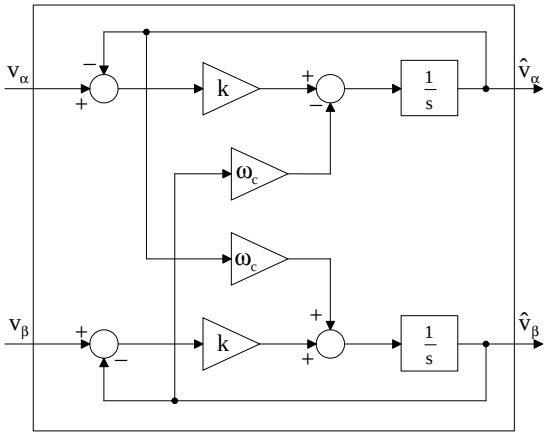

Figure 11.9: Block diagram of the multi-variable filter.

For balanced voltages with no voltage harmonics the output values are expressed by equation (11.11) for a nominal grid frequency:

$$\begin{aligned} \widehat{v}_\alpha &= V_m \cos(\omega_c t) \\ \widehat{v}_\beta &= V_m \sin(\omega_c t) \end{aligned} \tag{11.11}$$

By choosing $k = 0$, equation (11.10) would be reduced to equation (11.12):

$$\begin{array}{l} \widehat{v}_{\alpha}(s) = -\frac{\omega_c}{s}\widehat{v}_{\beta}(s) \\ \widehat{v}_{\beta}(s) = \frac{\omega_c}{s}\widehat{v}_{\alpha}(s) \end{array} \tag{11.12}$$

The two cross-coupled loops on Fig. 11.9 would thereby sustain fundamental balanced output voltages. If the initial value of the integrators are zero, no signals will be outputted. If the integrators have initial values, the filter will act as a multi-variable oscillator tuned at ω_c, completely insensitive to the input signals. For a low value of k, the filter will slowly build up the fundamental frequency and effectively reject harmonics and negative sequence components. For high values of k the filter will have a faster response, but be more sensitive to unbalanced and distorted voltages. Table 11.1 shows the band width and response time for different values of k.

Table 11.1: Band width and response time for different values of k

k	Δf_{filter} [Hz]	τ_{filter} [s]
1	± 0.16	1.0
3	± 0.48	0.33
10	± 1.6	0.10
30	± 4.8	0.033
100	± 16	0.010

11.4 Grid connected photovoltaic (PV) inverter with robust PLL

A PV system consisting of 16 strings of solar panels is situated at The Norwegian University for Science and Technology, Trondheim. Fig. 11.10 shows the overall structure of this PV system.

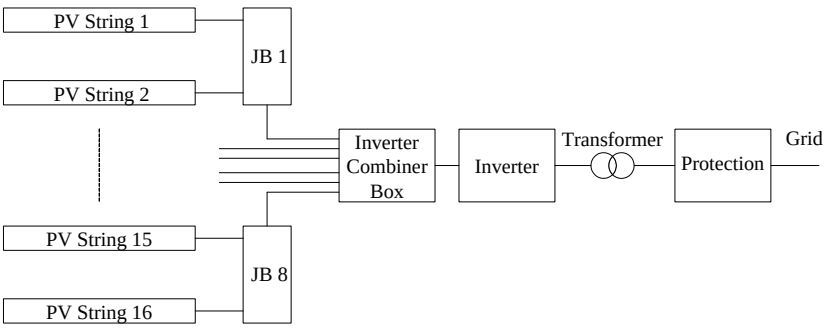

Figure 11.10: PV system at Norwegian University for Science and Technology, system block diagram.

The work described in this subsection, aims at connecting one single PV string to the grid by means of a step-up dc/dc converter and a grid connected three phase inverter, as depicted in Fig. 11.11.

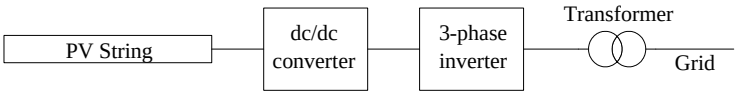

Figure 11.11: Block diagram of inverter system with one single PV string connected to the grid.

Table 11.2 presents some of the electrical data for the PV string. The dc/dc converter will both cover maximum power point tracking and keep the dc voltage of the inverter at a constant level. In the scope of this subsection, the inverter is directly connected to the PV string, leaving maximum power point tracking and protection systems for future work. The PV system of The Norwegian University for Science and Technology is thoroughly described in [52].

Table 11.2: Electrical data for the PV string at Norwegian University for Science and Technology

Nominal array voltage	210 V DC
Maximum array voltage	300 V DC
Maximum array current	5 A

PLL design

The PLL is described in Subsection 11.3. The PLL operates even at heavily distorted voltages and will continue to generate a rotating reference angle during a severe voltage sag and by blocking input noise at voltage interruption the PLL will continue to run even under such conditions. That may be useful for stand-alone operation. When the grid voltage is restored, the PLL will effectively synchronize and the system may be reconnected to the grid.

The angular frequency of the multi-variable band-pass filter is $\omega_c = 100\pi$, and the filter constant k was chosen to be $k = 20$, thereby achieving a suitable band-width for the filter. If the band-width is too narrow, the filter will also suppress the control signals v_α and v_β if the grid frequency deviates significantly from 50 Hz. If the band-width is too wide unwanted voltage harmonics will pass through the filter. It can also be difficult to tune the LF, making a trade-off between response and reliability. In this case the LF is a PI controller, and the transfer function of this controller is given in equation (11.13).

$$H_{LF}(s) = k_p \frac{1 + \tau_i s}{\tau_i s} \tag{11.13}$$

where $k_p = 2.23$k and $\tau_i = 9.0\,\mathrm{ms}$. This gives a good trade-off between stability and dynamic performance.

The transfer function of the NCO is simply an integration and is given in equation (11.14):

$$H_{NCO}(s) = \frac{1}{s} \tag{11.14}$$

Voltage Oriented Control

The structure of the voltage oriented current controller system is shown in Fig. 11.12. The DC voltage is measured and compared to a reference voltage. The output of the voltage PI controller in the left of Fig. 11.12 makes a reference for the current component i_d, i.e. the active component of the line currents. The reference of the reactive current component i_q is set to zero, thereby seeking for UPF.

The outputs of the current controllers are converted to a polar representation, outputting a voltage reference amplitude and angle correction, the latter added to the reference angle $\widehat{\theta}$.These signals control the pulse width modulator (PWM).

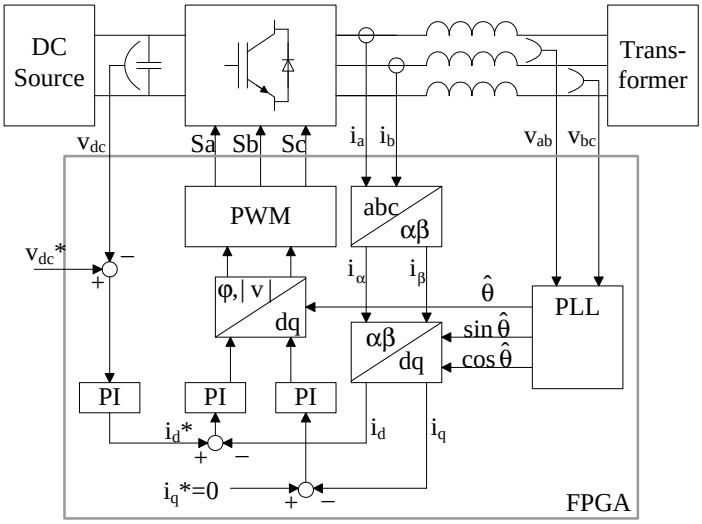

Figure 11.12: Inverter with Voltage Oriented Control system.

At the time this subsection was written, the different parts of the design were successfully tested, but energizing the inverter, tuning the controllers and closing the feedback loop still needed to be done, in order to experimentally verify the overall design.

The inductors between the inverter and the grid have an inductance of about $10\,\mathrm{mH}$. The inverter switches are insulated gate bipolar (IGBT) transistors.

The design of Fig. 11.12 may be expanded, thereby decoupling the active and reactive current components, as suggested in [45].

Simulation results

The PLL with a multi-variable filter was simulated in Simulink and the results are presented in Fig. 11.13 - 11.15. In each figure the uppermost plot shows the grid voltages, the middle shows the angle $\widehat{\theta}$, and the last plot shows $\sin\widehat{\theta}$ and $\cos\widehat{\theta}$. In Fig. 11.13 there is a considerable grid voltage asymmetry; in Fig. 11.14 there is a sudden voltage drop; in Fig. 11.15 there are voltage harmonics present. As can be seen from these simulations, confirming the results obtained in [49], the PLL is very robust and not much influenced by these disturbances.

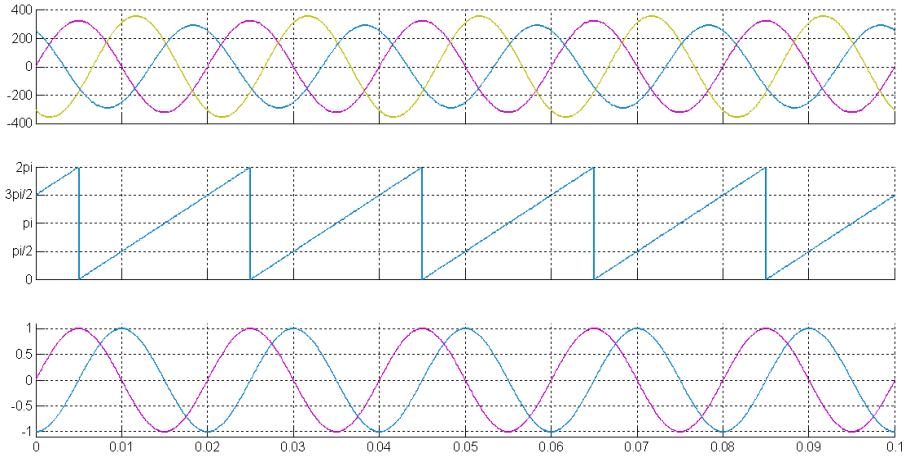

Figure 11.13: Simulation of robust PLL with asymmetrical grid voltages. From the top: Grid voltages; reference angle $\widehat{\theta}$; $\sin\widehat{\theta}$ and $\cos\widehat{\theta}$.

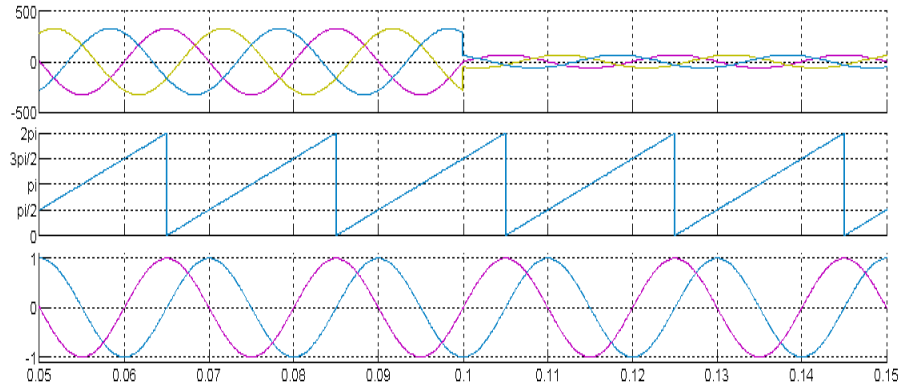

Figure 11.14: Simulation of robust PLL with voltage drop. From the top: Grid voltages; reference angle $\widehat{\theta}$; $\sin\widehat{\theta}$ and $\cos\widehat{\theta}$.

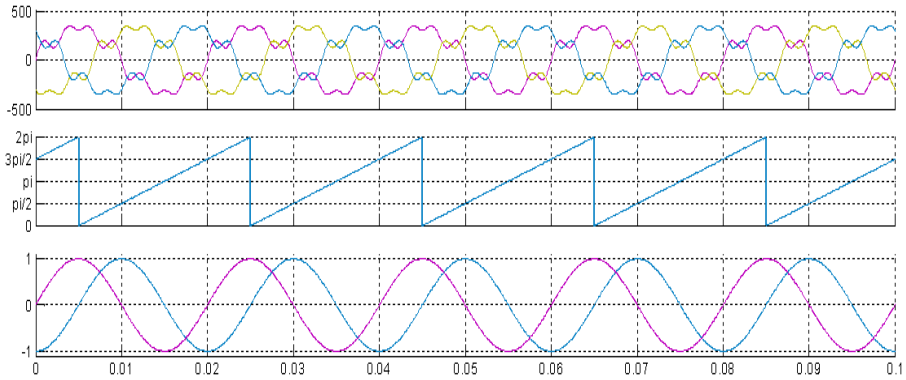

Figure 11.15: Simulation of robust PLL with grid voltage harmonics. From the top: Grid voltages; reference angle $\widehat{\theta}$; $\sin\widehat{\theta}$ and $\cos\widehat{\theta}$.

FPGA implementation

The design is implemented on a Xilinx FPGA of type Virtex2, mounted on a National Instruments PXI-7831R device with 8 analog inputs, 8 analog outputs and 16 digital input/output signals.

The voltage and current measurements are supplied through analog inputs, and the switching signals for the inverter are allocated at the digital outputs. The resolution of the ADCs is 16 bits. They are of successive approximation type with a conversion time of $4\,\mu$s, which gives a sampling rate of $200\,$kHz. The clock frequency of the FPGA is $40\,$MHz.

The PXI-7831R device is running on a NI PXI computer with LabView 7.1 software. All FPGA programming is done in LabView, even though almost all of the design is put in the FPGA. Only a monitoring and control interface is located with LabView as the execution target.

Floating point calculations are not possible on the FPGA. Multiplying a signal with a constant gain can be done as shown in equation (11.15).

$$k \approx \frac{N}{2^M} \tag{11.15}$$

where k is the gain to be reached, and M and N are integers. In equation (11.15) the signal is multiplied by N, and then shifted M bits to the right. The order of the operations can be reversed, but then the signal resolution is decreased. In integer arithmetic a trade-off between resolution and overflow problems needs to be done. Besides, high resolution leads to space/time-consuming multipliers. Also in summations and subtractions one must be aware of overflow problems.

Sine and cosine calculations are made through 1-dimentional look-up tables. Each table has 1024 addresses with a resolution of 16 bits.

One of the major benefits of the FPGA circuits is the ability to have several processes running in parallel. The data caption, the Clark and Park Transforms, the PLL, the PWM and the VOC are all running in parallel, sharing signals. There is no need for interrupting

a main program sequence to carry out more critical tasks, since all functions are running constantly.

The proportional part of the controller is made according to equation (11.15). Adding a shift register gives an integrator, as described in [53], and expressed in equation (11.16).

$$F_i(z) = \frac{1}{z-1} \tag{11.16}$$

The input (or output) signal must be scaled to obtain a correct time scale, depending on the sample interval z.

The most challenging part of the FPGA design is to implement the rectangular to polar transform in the middle of Figure 11.12 in a simple and accurate way. This transform is expressed in equation (11.17)

$$\begin{aligned} |v| &= \sqrt{({v_d}^*)^2 + ({v_q}^*)^2} \\ \varphi &= \arctan\left(\frac{{v_q}^*}{{v_d}^*}\right) \end{aligned} \tag{11.17}$$

where ${v_d}^*$ and ${v_q}^*$ is the active and reactive reference voltages, respectively, $|v^*|$ is the absolute value of the reference voltage, and φ is the reference angle correction given by the VOC system. Both the $\arctan$ and square root calculation are difficult to perform in integer arithmetic.

One solution is to approximate the output variables as shown in equation (11.18)

$$\begin{aligned} |v^*| &\approx {v_d}^* \\ \varphi &\approx k \cdot {v_q}^* \end{aligned} \tag{11.18}$$

where k is some constant. These approximations are only valid if $v_d >> v_q$ and v_d is close to its nominal value.

Experimental results

Fig. 11.16 shows a test result for the PLL under normal voltage conditions, showing two line voltages plus the reference angle. The signals look a little bit sloppy, because the data captions of these plots are quite slow, due to the asynchronous data transfer between the FPGA and the PC. However, the Figure 11.16 shows that the reference angle is locked to the grid voltages. In Fig. 11.17, phase c is disconnected, but still the PLL synchronizes to the grid.

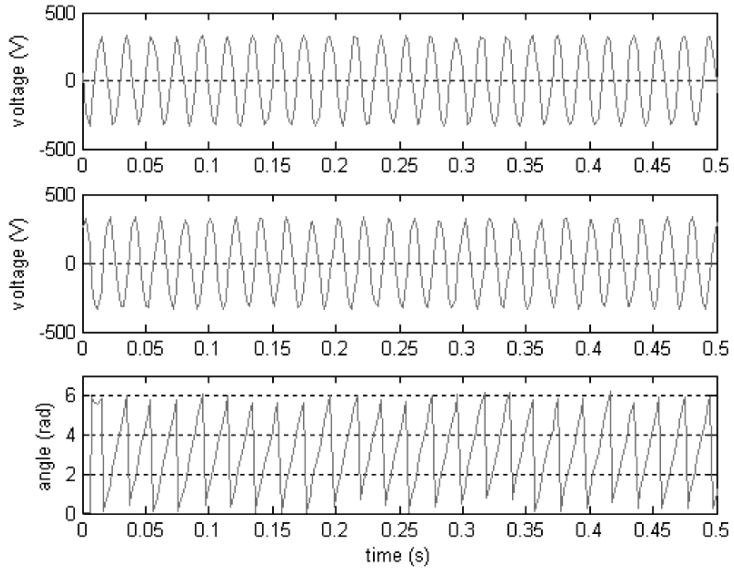

Figure 11.16: Robust PLL during normal voltage conditions. From the top: line voltages v_{ab}, v_{bc} and the reference angle $\widehat{\theta}$.

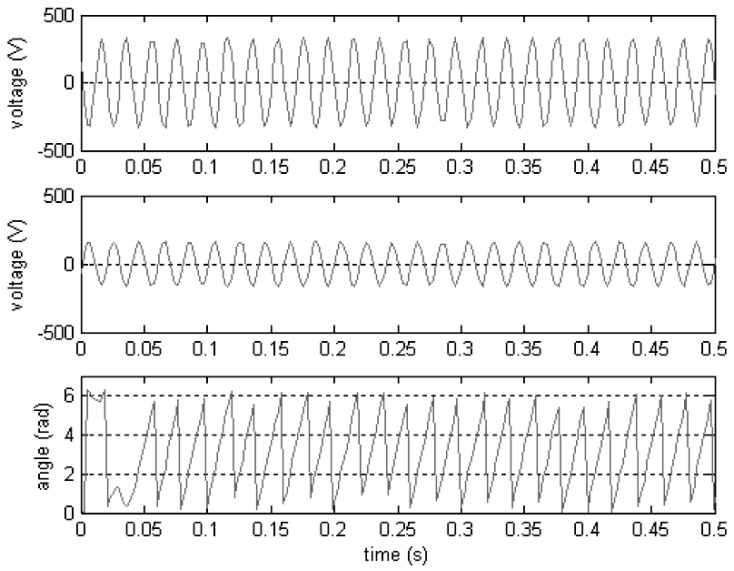

Figure 11.17: Robust PLL with phase c disconnected. From the top: line voltages v_{ab}, v_{bc} and the reference angle $\widehat{\theta}$.

The synchronous reference currents i_d and i_q were tested, using the test arrangement on Figure 11.18, with a partly inductive load on Figure 11.18a and a pure resistive load on Figure 11.18b.

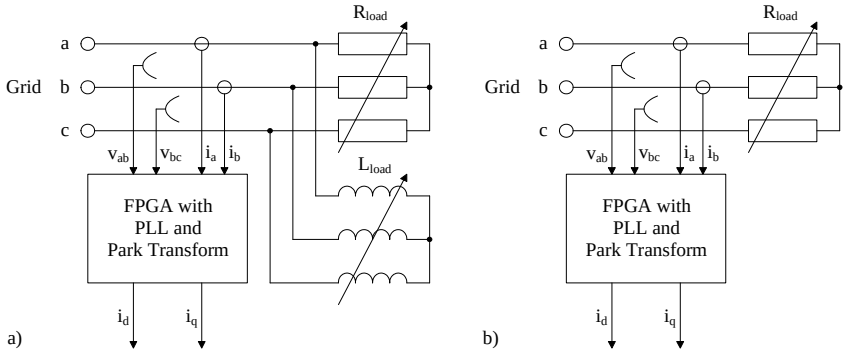

Figure 11.18: Test arrangement for measuring synchronous reference currents i_d and i_q.

The measurement results are shown on Fig. 11.19 and Fig. 11.20, respectively. The figures show the line voltage v_{ab}, the line current i_a, and the transformed currents i_d and i_q.

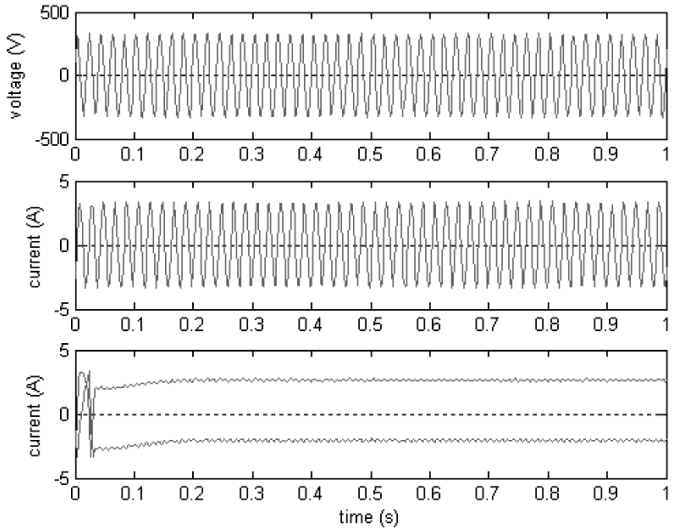

Figure 11.19: Park Transform of line currents with partly inductive load. From the top: Line voltage v_{ab}; line current i_a; transformed currents i_d (positive) and i_q (negative).

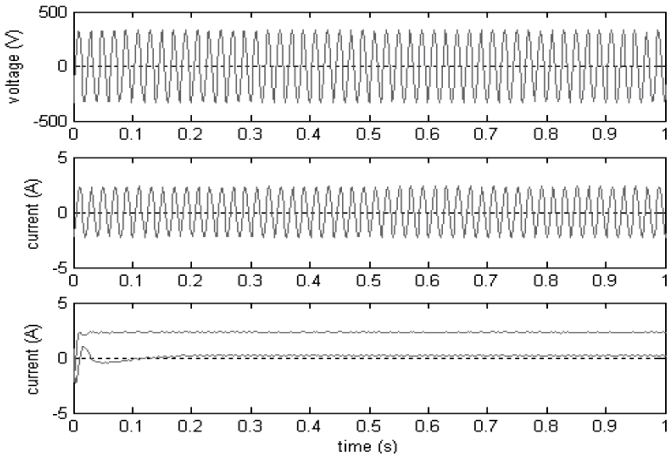

Figure 11.20: Park Transform of line currents with resistive load. From the top: Line voltage v_{ab}; line current i_a; transformed currents i_d (positive) and i_q (close to zero).

The plots show that the Park Transform is working properly and so is the PLL. Otherwise, significant ripple should occur on the transformed currents. The ripple on these currents is probably caused by asymmetrical load or lack of symmetry in the current measurements. It can be seen from the figures that it takes about $0.2\,\mathrm{s}$ before the PLL has fully stabilized. One should also notice that the reactive current component has a negative value when the load is partly inductive. The reason is the synchronous reference frame, where the active current component is in phase with the voltage reference and a leading current component (capacitive load) will be interpreted as positive.

In the tests of the PWM, a voltage source was connected to the dc bus of the inverter, as shown on Fig. 11.21, and the inverter ac voltages were measured for different values of the reference voltages $v_d{}^*$ and $v_q{}^*$.

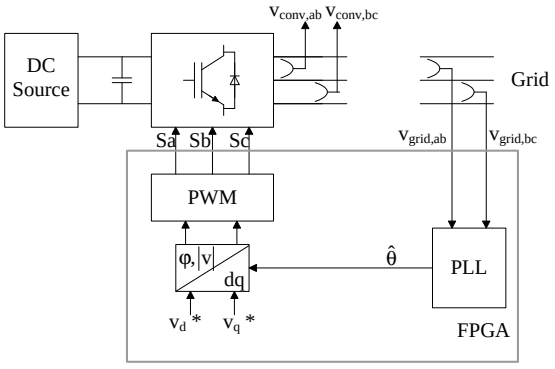

Figure 11.21: Arrangement for testing the PWM and the inverter.

Fig. 11.22 - 11.24 show the line voltage $v_{grid,ab}$ and the inverter voltage $v_{conv,ab}$ for different values of ${v_q}^*$. It can be seen that the inverter voltage is phase shifted to the line voltage when ${v_q}^*$ is changed, as expected.

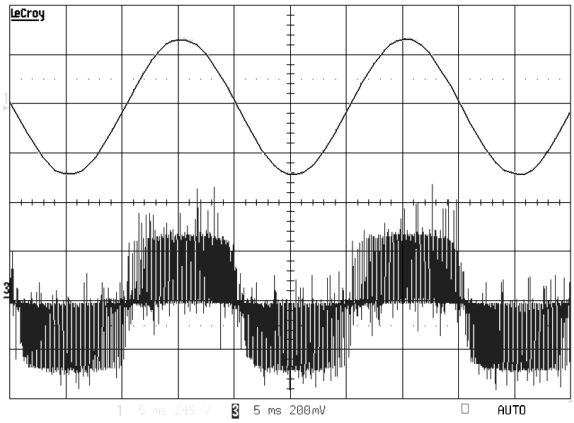

Figure 11.22: PWM test with ${v_d}^*$ positive and ${v_q}^* = 0$. From the top: $v_{grid,ab}$, $v_{conv,ab}$.

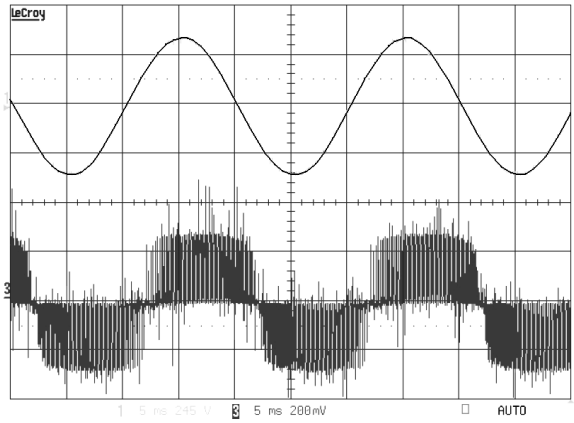

Figure 11.23: PWM test with ${v_d}^*$ positive and ${v_q}^*$ negative. From the top: $v_{grid,ab}$, $v_{conv,ab}$.

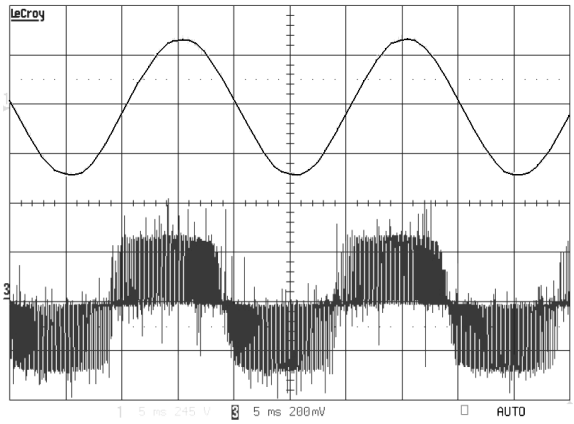

Figure 11.24: PWM test with both v_d * and v_q * positive. From the top: $v_{grid,ab}$, $v_{conv,ab}$.

Further work

Further tests need to be done in order to verify the performance of the overall design. Both the PI controllers and the rectangular to polar transform must be thoroughly tested. For the former, lack of precision of small integer values may cause problems such as dead-band or hysteresis, and for the latter, start-up conditions may be critical. It remains to be seen whether any of these components of the design must be moved to the high level part (LabView) of the design, or re-designed in the FPGA.

A successful solution for the FPGA design described in this article should be extended with a dc/dc converter between the PV string and the inverter and procedures for maximum power point tracking should be implemented. Monitoring and protection schemes are also needed, to meet the requirements of [54,55], concerning islanding conditions and de-energizing of the grid.

12 Adaptive Signal Cancellation

Frequency deviations due to grid disturbances are considered. Symmetrical components are described. The Delayed Signal Cancellation method for detecting the symmetrical components is then described. An alternative method is proposed: Adaptive Signal Cancellation. The method is analyzed and experimentally tested.

12.1 Frequency deviation

Traditional devices for grid voltage synchronization and voltage disturbance detection often assume the grid frequency to be constant. If, however, parts of the distribution grid are weak, such devices may display a poor performance during frequency variations. The simplest circuits are also sensitive to voltage disturbances such as transients, harmonics and asymmetry.

A traditional phase-locked loop [33,37] is a common solution for generating a voltage synchronizing signal for the power converter. It has inherent low-pass properties, thereby filtering out short voltage disturbances. It is, however, sensitive to voltage asymmetry and harmonics and needs some additional filtering. In [49] a multi-variable filter is proposed. This filter effectively removes both voltage harmonics and the 2^{nd} harmonic disturbance caused by voltage asymmetry. If the grid frequency is fluctuating, this filter design would both attenuate and phase shift the signals as soon as the frequency deviates from its nominal value.

A frequency change can be disastrous for specific kinds of equipment and should be carefully monitored. In [56], an adaptive and robust method is applied for fast frequency estimation. The method uses fast Fourier transform (FFT) and thereby requires a time consuming algorithm to produce a frequency estimate.

Study Case: Nygårdsfjellet wind farm

In the vicinity of Narvik a small wind farm is located. It contains three wind turbines. Four hydro power generators are connected to the same distribution network and the complete power generation system is connected to a strong grid through a single underwater cable. The map on Fig. 12.1 shows where the different generators are located. The generators G1 - G3 are placed at Nygård hydro power plant. G4 is located at Sirkelvann mini plant, while G5 - G7 are situated at Nygårdsfjellet wind farm. Some data for these generators is given in Table 12.1. Some parameters for the transformers and distribution lines are given in Table 12.11 and Table 12.3, respectively.

Table 12.1: Some rated values for different generators

Generator	Nominal power [MW]	Nominal voltage [kV]
G1, G2	8.0	4.2
G3	9.0	4.2
G4	0.7	6.9
G5-G7 (wind farm)	2.3	0.75

Figure 12.1: Power plants and distribution lines in the Narvik area (Map source: www.hvor.no, copyright Keyteq AS).

Table 12.2: Some rated values for the transformers

Transformer	Nominal power [MV A]	Nominal voltage [kV]
T1, T2	10	35/4.2
T3	10	33.3/4.2
T4	1.1	22/6.9
T5	7.0	32.4/23

Table 12.3: Parameters for distribution lines

Length [km]	Max. current [A]	Resistance [Ω]	Inductance [mH]	Mutual capacitance [μF]
Underwater cable Frydenlund - Nygård				
7.55	400	1.18	4.01	4.54
Overhead line Nygård - sirkelvann				
6.76	454	1.95	8.4	0.61
Overhead line Sirkelvann - Nygårdsfjell				
5.02	454	1.29	5.79	0.1

Fig. 12.2 shows a simplified version of the above mentioned distribution network. The generator closest to the wind farm is also the smallest one. It has the weakest grid connection and is most like to experience rotor oscillations caused by intermittent power flow from the wind farm.

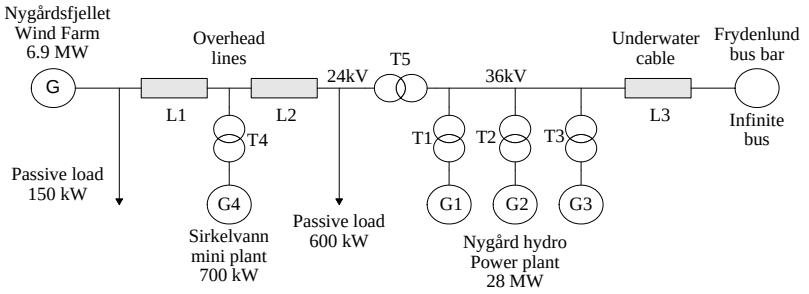

Figure 12.2: Simplified distribution network in the Narvik area.

Based on the network described in Fig. 12.2, a simulation was performed, using the simulation tool ATPDraw. It was assumed that generator G1 - G3 were disconnected while G4 and the wind farm were running normally. At time $t = 5.0\,\mathrm{s}$ the wind farm was suddenly disconnected, and the simulation investigated how large the rotor oscillation of G4 would be and to what degree this would influence the frequency of the nearby passive load of $150\,\mathrm{kW}$. Fig. 12.3 shows the simulation results. The upper plot displays the grid frequency, and the lower one shows the load angle of G4.

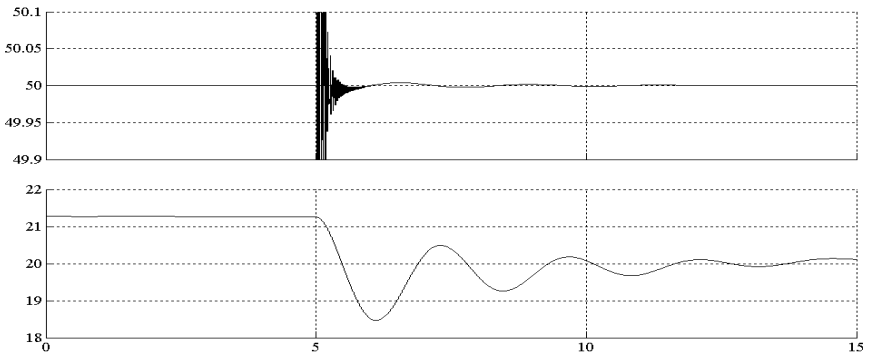

Figure 12.3: Frequency deviation and rotor oscillation at Sirkelvann mini plant. Upper plot: Grid frequency. Lower plot: Load angle.

Even if the simulation is not verified by experimental results, it concludes that interaction between wind power and hydro power normally would not cause significant frequency deviation, even if the grid connection is weak. A sustained island, however, is a different issue. With no connection to the strong grid, the frequency may drift, until the island eventually is de-energized.

12.2 Symmetrical components

Any three-phase voltages or currents may be decomposed in symmetrical components: i.e.; a positive-sequence set; a negative-sequence set and a zero-sequence set. For balanced voltages or currents with no ground faults, only the positive-sequence set is present. For unbalanced voltages or currents, a certain combination of the three symmetrical components will represent the unbalanced system. Symmetrical components are described in [57].

Positive-sequence set

Positive-sequence currents are defined in equation (12.1) and voltages in equation (12.2)

$$\begin{aligned} i_{a1} &= i_1 \\ i_{b1} &= a^2 i_{a1} = i_1 \angle 240^\circ \\ i_{c1} &= a i_{a1} = i_1 \angle 120^\circ \end{aligned} \tag{12.1}$$

$$\begin{aligned} v_{a1} &= v_1 \\ v_{b1} &= a^2 v_{a1} = v_1 \angle 240^\circ \\ v_{c1} &= a^2 v_{a1} = v_1 \angle 120^\circ \end{aligned} \tag{12.2}$$

where $a = -\frac{1}{2} + j\frac{\sqrt{3}}{2}$ and the subscript 1 designates a positive-sequence set. For a negative-sequence set subscript 2 is used, and for a zero-sequence set subscript 0 is used. The positive-sequence voltages of equation (12.2) are visualized on Fig. 12.4, where the system is rotating counter-clockwise at the system frequency.

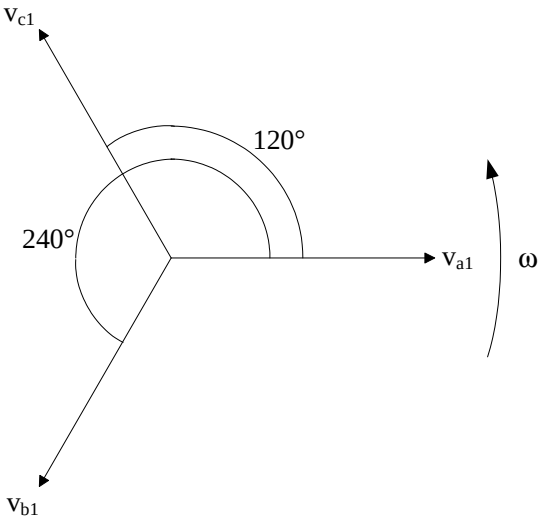

Figure 12.4: Positive-sequence voltage phasors.

Negative-sequence set

For the rest of the subsection only symmetrical voltage components will be discussed, although the same principles apply for currents. The negative-sequence voltage set is defined in equation (12.3) and depicted on Fig. 12.5:

$$\begin{aligned} v_{a2} &= v_2 \\ v_{b2} &= a v_{a2} = v_2 \angle 120^\circ \\ v_{c2} &= a^2 v_{a2} = v_2 \angle 240^\circ \end{aligned} \tag{12.3}$$

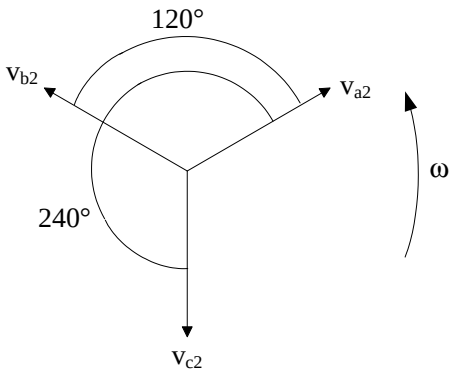

Figure 12.5: Negative-sequence voltage phasors.

Zero-sequence set

For the zero-sequence set the phasors are equal and overlapping, as can be seen from equation (12.4) and Fig. 12.6:

$$v_{a0} = v_{b0} = v_{c0} = v_0 \tag{12.4}$$

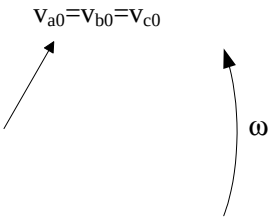

Figure 12.6: Zero-sequence voltage phasors.

General equations

Unbalanced voltages can be determined by combining equations (12.2 - 12.4), as expressed in equation (12.5):

$$\begin{aligned} v_a &= v_1 + v_2 + v_0 \\ v_b &= a^2 v_1 + a v_2 + v_0 \\ v_c &= a v_1 + a^2 v_2 + v_0 \end{aligned} \tag{12.5}$$

This is illustrated on Fig. 12.7, where the symmetrical components of Fig. 12.4 - 12.6 are put together, resembling unbalanced three-phase voltages. Positive-sequence voltage phasors are drawn with red lines, negative-sequence voltages with green lines, zero-sequence voltages with blue lines and the resulting unbalanced phase voltages with thick black lines.

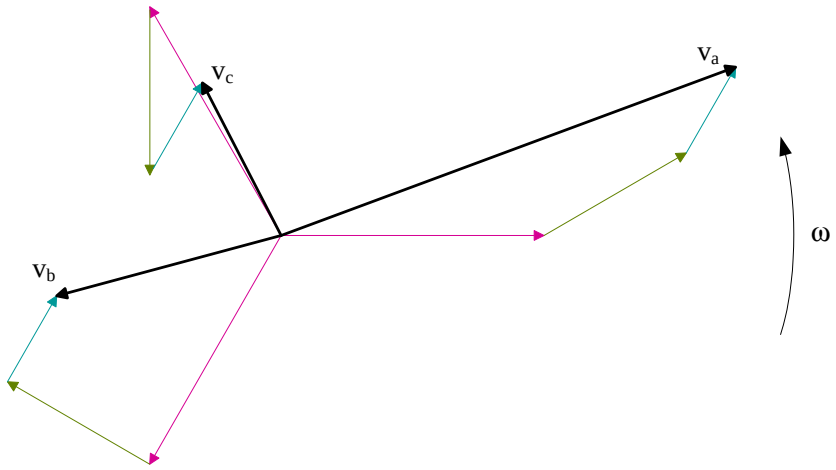

Figure 12.7: Unbalanced voltage phasors.

The symmetrical reference phasors V_1, V_2 and V_0 are determined by adding and phase shifting the unbalanced voltages, as expressed in equation (12.6):

$$\begin{aligned} v_0 &= \tfrac{1}{3}\left(v_a + v_b + v_c\right) \\ v_1 &= \tfrac{1}{3}\left(v_a + a v_b + a^2 v_c\right) \\ v_2 &= \tfrac{1}{3}\left(v_a + a^2 v_b + a v_c\right) \end{aligned} \tag{12.6}$$

12.3 Two-axis representation

The positive-sequence reference phasor v_1 can be written as equation (12.7)

$$v_1 = \frac{1}{3}\left(v_a - \frac{1}{2}v_b - \frac{1}{2}v_c + j\left(\frac{\sqrt{3}}{2}v_b - \frac{\sqrt{3}}{2}v_c\right)\right) \tag{12.7}$$

which is proportional to the Clarke Transform, defined in equation (9.2), where the real part is represented by $\frac{1}{2}v_\alpha$ and the imaginary by $\frac{1}{2}v_\beta$.

The positive-sequence reference phasor v_1 can be written as equation (12.8)

$$v_2 = \frac{1}{3}\left(v_a - \frac{1}{2}v_b - \frac{1}{2}v_c + j\left(-\frac{\sqrt{3}}{2}v_b + \frac{\sqrt{3}}{2}v_c\right)\right) \tag{12.8}$$

where the real part is represented by $\frac{1}{2}v_\alpha$ and the imaginary by $-\frac{1}{2}v_\beta$.

12.4 Delayed Signal Cancellation

One way of monitoring the voltage condition for protection purposes is to calculate the symmetric components of the three-phase voltages. A fast and simple way of doing this is described in [58,59], based on Delayed Signal Cancellation (DSC). In this method, signals have a fixed delay, determined by the grid frequency. If the frequency drifts from its nominal value, the performance of the method is deteriorated. In [58] the authors analyze the impact of frequency deviations. In [59,60] the authors take advantage of the fact that a sinusoidal signal is 90° phase shifted when differentiated.

The DSC method delays the input signal, as given in equations (12.9) and (12.10)

$$\begin{aligned} v_{\alpha 1}(t) &= \tfrac{1}{2}\left[v_\alpha(t) - v_\beta\left(t - \tfrac{T_g}{4}\right)\right] \\ v_{\beta 1}(t) &= \tfrac{1}{2}\left[v_\beta(t) + v_\alpha\left(t - \tfrac{T_g}{4}\right)\right] \end{aligned} \tag{12.9}$$

$$\begin{aligned} v_{\alpha 2}(t) &= \tfrac{1}{2}\left[v_\alpha(t) + v_\beta\left(t - \tfrac{T_g}{4}\right)\right] \\ v_{\beta 2}(t) &= \tfrac{1}{2}\left[v_\beta(t) - v_\alpha\left(t - \tfrac{T_g}{4}\right)\right] \end{aligned} \tag{12.10}$$

where T_g is the period of the grid voltages, subscript 1 designates a positive-sequence and subscript 2 designates a negative-sequence set. A block diagram of the DSC circuit is shown on Fig. 12.8. For convenience, the terms $v_\alpha\left(t - \frac{T_g}{4}\right)$ and $v_\beta\left(t - \frac{T_g}{4}\right)$ will be referred to as $v_{\alpha,del}$ and $v_{\beta,del}$, respectively.

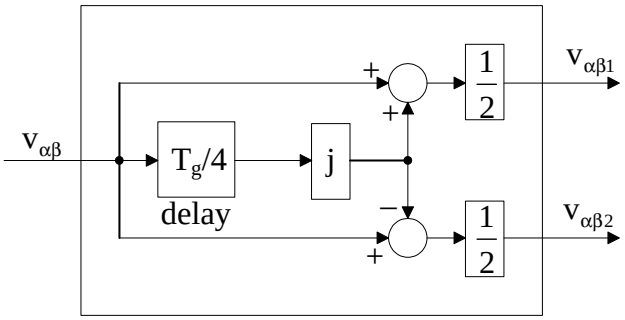

Figure 12.8: Block diagram of Delayed Signal Cancellation.

Fig. 12.9 and 12.10 illustrate what takes place in the calculations of equations (12.9) and (12.10). The upper plot shows the input signals v_α (red) and v_β (blue). The next plot shows the delayed signals $v_{\alpha,del}$ (blue) and $v_{\beta,del}$ (red). The third plot shows the positive-sequence signals $v_{\alpha,1}$ (red) and $v_{\beta,1}$ (blue). The last plot shows the negative-sequence signals $v_{\alpha,2}$ (red) and $v_{\beta,2}$ (blue). Fig. 12.9 displays balanced conditions, where the positive-sequence signals equal the input signals and the negative-sequence signals are zero. On Fig. 12.10 there is some unbalance present, and the amplitude of positive-sequence signals is reduced. Negative-sequence signals are present, revealing that some voltage unbalance is present. Thus, these signals are convenient for detecting various voltage disturbances.

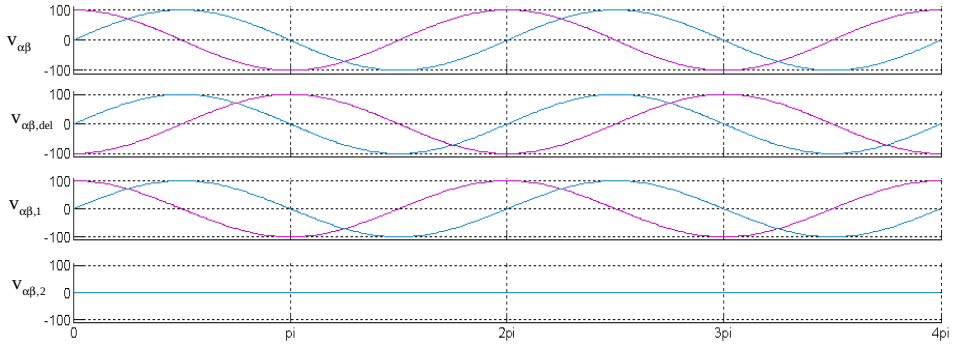

Figure 12.9: DSC with balanced voltages. From the top: Input signals; delayed signals; positive-sequence signals and negative-sequence signals.

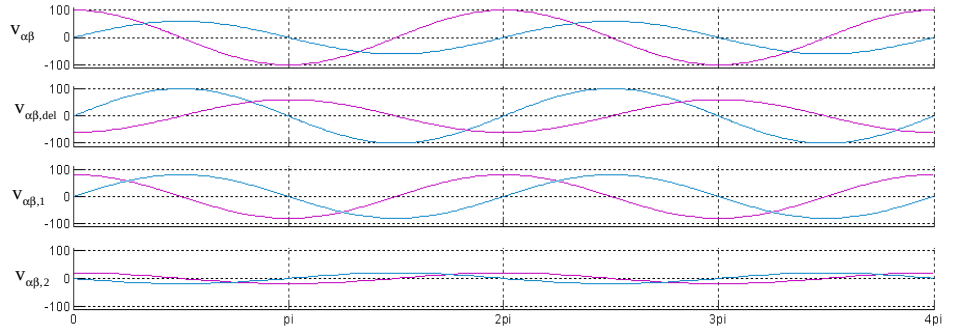

Figure 12.10: DSC with unbalanced voltages. From the top: Input signals; delayed signals; positive-sequence signals and negative-sequence signals.

Alternative methods

The DSC method is based on delaying the input signals, i.e. a phase shift of $90°$. Some alternative solutions are suggested, based on the fact that $\sin(\omega t)$ and $\cos(\omega t)$ are $90°$ phase shifted. In [59] a differentiation is performed on the input signals, thereby phase shifting them $90°$. Equation (12.11) explains how this might be obtained.

$$\begin{aligned} v_{\alpha,del}(\omega t) &= -\frac{1}{\omega_c}\frac{d}{dt}(v_\alpha(\omega t)) \\ v_{\beta,del}(\omega t) &= -\frac{1}{\omega_c}\frac{d}{dt}(v_\beta(\omega t)) \end{aligned} \tag{12.11}$$

The scaling factor of $\frac{1}{\omega_c}$ is used in order to align the amplitude of the differentiations to the input signals. Thus, the method assumes that the system frequency is constant. A benefit of this method is that it is fast and simple and does not require a lot of calculations. A major drawback, however, is that the differentiation of the input signals would augment voltage harmonic components, rather than filtering them out.

12.5 Adaptive Signal Cancellation

As long as the grid frequency is constant, the multi-variable band-pass filter proposed in [49] will filter the input signals properly. If the frequency deviates significantly, however, the filter tuned at the centre frequency ω_c would both attenuate and phase shift the filtered signals. An alternative method is suggested in [61], based on DSC. This Adaptive Signal Cancellation (ASC) method has very good frequency tracking properties, and the design is robust. The circuit outputs the positive-sequence signals to the PLL. In addition, negative-sequence signals can be used for monitoring the grid voltage conditions. The design is realized in an FPGA, thereby obtaining very fast calculations and a compact design.

System Description
Overall system

Fig. 12.11 shows the complete system. The input voltages v_a, v_b and v_c are converted into v_α and v_β through the Clark Transform abc/$\alpha\beta$. The signal delay estimator calculates the signals $\widehat{v}_{\alpha,del}$ and $\widehat{v}_{\beta,del}$.

The phase sequence detector performs a DSC operation and a calculation of the amplitudes of the symmetric voltage components $|\widehat{v}_1|$ and $|\widehat{v}_2|$. The estimated positive sequence signals $\widehat{v}_{a,1}$ and $\widehat{v}_{\beta,1}$are put into the PLL, which returns estimated angular frequency $\widehat{\omega}$ and phase angle $\widehat{\theta}$, plus $\sin\widehat{\theta}$ and $\cos\widehat{\theta}$.

If the signals v_α and v_β from the Clark Transform were to be connected directly to the PLL, the phase sequence detector would continue to estimate the symmetric voltage components, but the filtering properties of the ASC system would not be utilized.

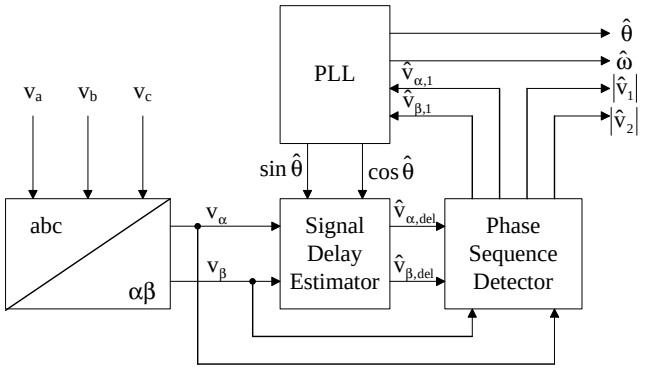

Figure 12.11: Block diagram of the entire system.

The PLL is described in Chapter 11.1.

Signal Delay Estimator

Fig. 12.12 shows the block diagram of the signal delay estimator. An important condition for this circuit to function, is that the estimated reference angle $\widehat{\theta}$ is synchronized to the voltage signals v_α and v_β. The two control loops in the top and the bottom of the figure amplifies the sine and cosine signals of $\widehat{\theta}$, until they have equal amplitude to the input signals. The transfer function of the closed loop is expressed by equation (12.12), and it acts as a first order low-pass filter.

$$H(s) = \frac{\frac{1}{\tau_{i,ASC}s}}{1 + \frac{1}{\tau_{i,ASC}s}} = \frac{1}{1 + \tau_{i,ASC}s} \tag{12.12}$$

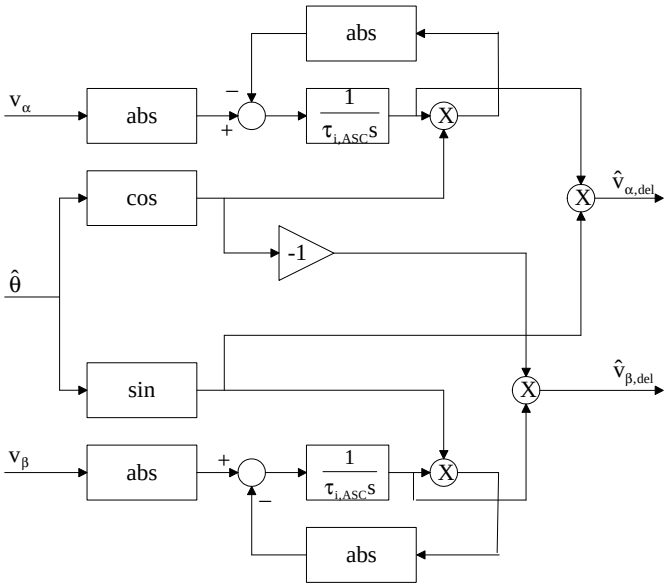

Figure 12.12: Block diagram of signal delay estimator.

If the input signals have constant amplitudes, the integrators will eventually output the amplitudes of these signals. The feedback for the upper and lower control loop contains estimated variables $\widehat{v}_\alpha$ and $\widehat{v}_\beta$, as expressed in equation (12.13),

$$\begin{aligned} \widehat{v}_\alpha &= \widehat{V}_\alpha \cos\widehat{\theta} \\ \widehat{v}_\beta &= \widehat{V}_\beta \sin\widehat{\theta} \end{aligned} \tag{12.13}$$

where $\widehat{V}_\alpha$ is the estimated amplitude of v_α and $\widehat{V}_\beta$ is the estimated amplitude of v_β. The real amplitudes of v_α and v_β will be denoted V_α and V_β, respectively. Then the output signals are expressed in equation (12.14).

$$\begin{aligned} \widehat{v}_{\alpha,del} &= \widehat{V}_\alpha \sin\widehat{\theta} \\ \widehat{v}_{\beta,del} &= -\widehat{V}_\beta \cos\widehat{\theta} \end{aligned} \tag{12.14}$$

As long as the PLL is synchronized and the feedback loops on Fig. 12.12 output the amplitudes V_α and V_β, the output signals will be phase shifted $90°$ degrees to the input signals for any utility voltage frequency. However, during step voltage changes the estimator will need some time to follow the input signal, due to the low-pass characteristic described in equation (12.12).

Fig. 12.13 displays different signals for the voltage component v_α. The upper plot shows v_α, which is sinusoidal. The estimated signal $\widehat{v}_\alpha$ takes some time to settle, as it is proportional to the estimated amplitude $\widehat{V}_\alpha$. These signals are shown on the second and the third plot. The two next plots show the absolute values of v_α and $\widehat{v}_\alpha$. The last plot shows the error signal e inputted to the integrator. e is expressed as $e = |v_\alpha| - |\widehat{v}_\alpha|$. The response time depends on the integral time $\tau_{i,ASC}$, which in this case was chosen to be $\tau_{i,ASC} = 20\,\mathrm{ms}$. Similar signals would be generated for v_α. The result on Fig. 12.13 is based on the assumption that the estimated reference angle $\widehat{\theta}$ is equal to the real angle θ (no angle displacement error in the PLL).

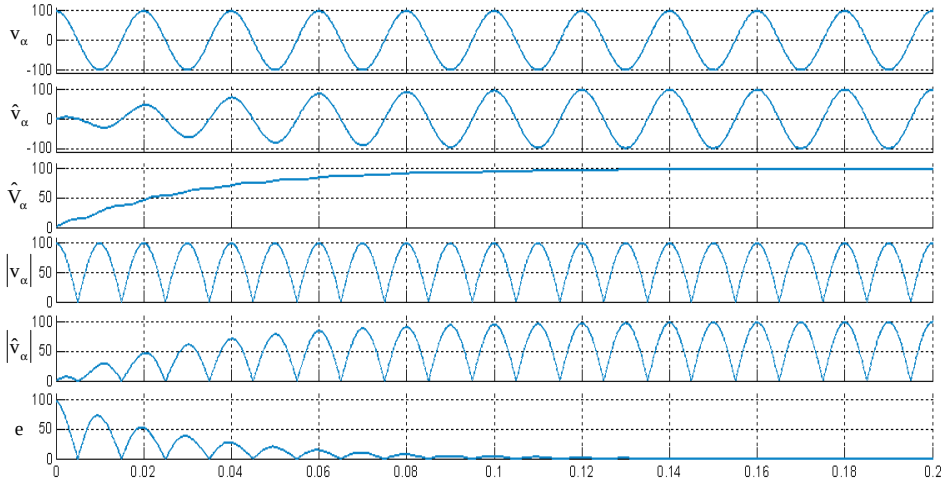

Figure 12.13: Signals inside the Signal Delay Estimator. From the top: v_α, $\widehat{v}_\alpha$, $\widehat{V}_\alpha$, $|v_\alpha|$, $|\widehat{v}_\alpha|$ and e.

The absolute value calculations are necessary in order to generate a "DC component", even if the v_α and $\widehat{v}_\alpha$ signals should be out of phase or even in opposite phase. In such cases the mean value of the estimated amplitude $\widehat{V}_\alpha$ will be zero, as can be seen from Fig. 12.14. The absolute value calculations act as rectifiers, making sure that just the signal amplitudes are compared, and not the polarity as well.

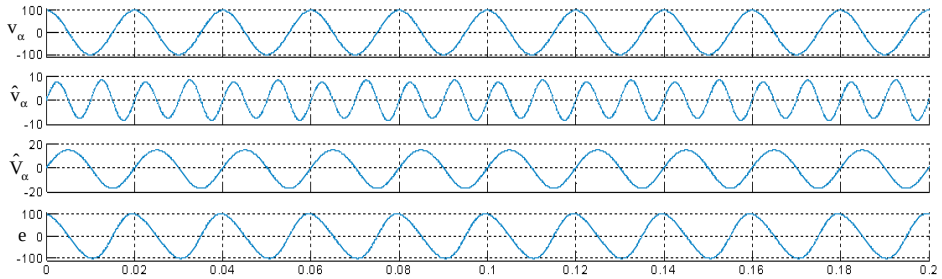

Figure 12.14: Signals inside the Signal Delay Estimator with the absolute value calculations removed. From the top: v_α, $\widehat{v}_\alpha$, $\widehat{V}_\alpha$ and e.

Even if the PLL is not locked to the grid frequencies, the Signal Delay Estimator will still approximate the signal amplitude, as can be seen from Fig. 12.15, even though there is some 2^{nd} harmonic ripple present. This ripple causes the slightly distorted shape of the estimated signal $\widehat{v}_\alpha$. The figure illustrates the worst case where the PLL is leading by $90°$. The same applies for the PLL lagging $90°$. Should the signals be in opposite phase, then the "rectified" signals will be in phase, and the circuit would perform as on Fig. 12.13 and give a smooth amplitude estimate after some initial disturbances.

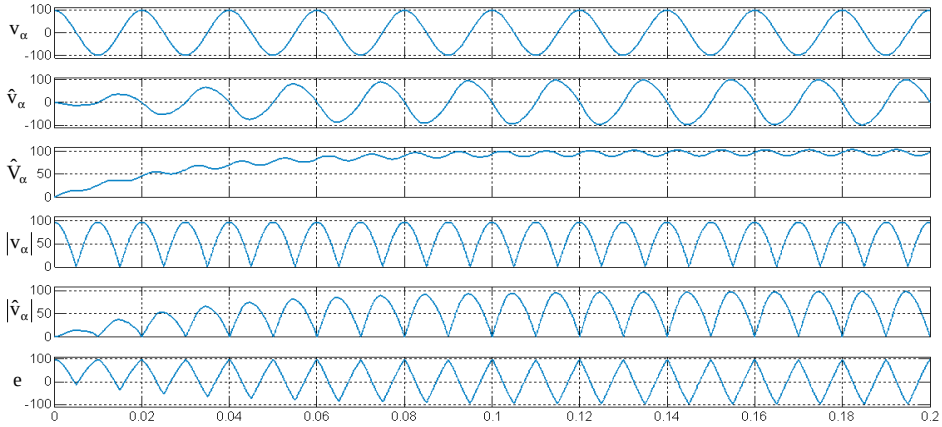

Figure 12.15: Signals inside the Signal Delay Estimator with the PLL leading by $90°$ in relation to the grid voltages. From the top: v_α, $\widehat{v}_\alpha$, $\widehat{V}_\alpha$, $|v_\alpha|$, $|\widehat{v}_\alpha|$ and e.

Another way of calculating the voltage amplitude is to determine the maximum value inside some time interval. For sinusoidal voltages that would work fine, but if voltage harmonics are present, this method would fail, as the peak voltage is then different from the amplitude of the fundamental component. This is evident on Fig. 12.16, where 10% 5^{th} harmonic voltage is present, and the filter time constant $\tau_{i,ASC}$ remains at $20\,\text{ms}$. The low-pass filtering properties of the Signal Delay Estimator makes the estimated voltage $\widehat{v}_\alpha$

almost sinusoidal, even though the input voltage v_α is distorted.

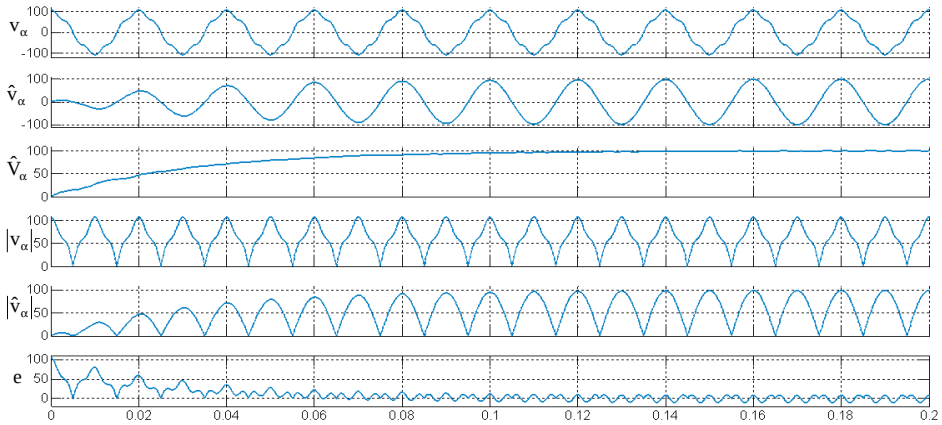

Figure 12.16: Signals inside the Signal Delay Estimator with 10% 5^{th} harmonics and $\tau_{i,ASC} = 20\,\text{ms}$. From the top: v_α, $\widehat{v}_\alpha$, $\widehat{V}_\alpha$, $|v_\alpha|$, $|\widehat{v}_\alpha|$ and e.

The choice of the time constant $\tau_{i,ASC}$ is a trade-off between good filtering and fast response to step voltage changes. On Fig. 12.17 there is still 10% 5^{th} harmonic voltage present, but time constant is reduced to $\tau_{i,ASC} = 5\,\text{ms}$. There is a little bit more ripple on the estimated amplitude V_α, but the estimated voltage $\widehat{v}_\alpha$ is not very much affected. One assumes that the estimated reference angle $\widehat{\theta}$ is without disturbance and thus the slight variation of the amplitude will play a minor role.

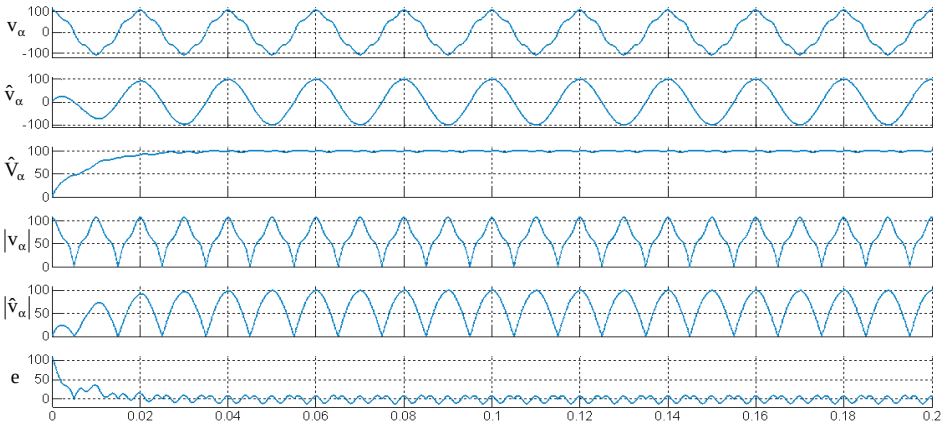

Figure 12.17: Signals inside the Signal Delay Estimator with 10% 5^{th} harmonics and $\tau_{i,ASC} = 5\,\text{ms}$. From the top: v_α, $\widehat{v}_\alpha$, $\widehat{V}_\alpha$, $|v_\alpha|$, $|\widehat{v}_\alpha|$ and e.

Fig. 12.18 shows the effect of a 20% voltage drop at $t = 0.1\,\mathrm{s}$. The amplitude takes about two periods to settle, which is quite a longer delay than the fourth of a period required using the DSC method. Still, for most equipment the response of the ASC circuit would be fast enough.

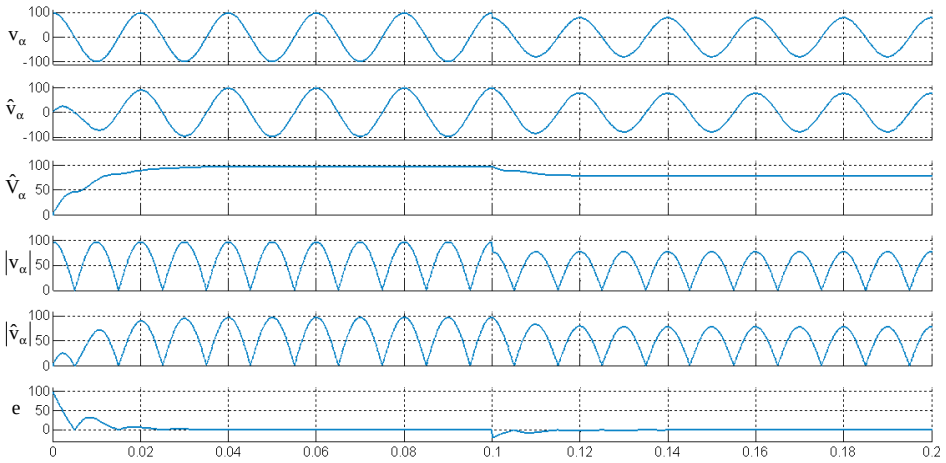

Figure 12.18: Signals inside the Signal Delay Estimator with $\tau_{i,ASC} = 5\,\mathrm{ms}$ and a 20% voltage drop at $t = 0.1\,\mathrm{s}$. From the top: v_α, $\widehat{v}_\alpha$, $\widehat{V}_\alpha$, $|v_\alpha|$, $|\widehat{v}_\alpha|$ and e.

Phase Sequence Detector

This part of the design utilizes a traditional DSC method and is shown in Fig. 12.19. The mathematical description is given in equations (12.15) and (12.16).

$$\begin{aligned} \widehat{v}_{\alpha,1} &= \tfrac{1}{2}\left(v_\alpha - \widehat{v}_{\beta,del}\right) \\ \widehat{v}_{\beta,1} &= \tfrac{1}{2}\left(v_\beta + \widehat{v}_{\alpha,del}\right) \end{aligned} \tag{12.15}$$

$$\begin{aligned} \widehat{v}_{\alpha,2} &= \tfrac{1}{2}\left(v_\alpha + \widehat{v}_{\beta,del}\right) \\ \widehat{v}_{\beta,2} &= \tfrac{1}{2}\left(v_\beta - \widehat{v}_{\alpha,del}\right) \end{aligned} \tag{12.16}$$

An additional circuit estimates the amplitudes of the output signals from the circuit shown in Fig. 12.19. The amplitudes are determined by using Park transforms with different synchronous references for the positive and the negative sequence system.

Fig. 12.20 shows the performance of the Phase Sequence Detector. The input voltages v_α and v_β are plotted on the top. The next plot shows the estimated delayed signals $\widehat{v}_{\alpha,del}$ and $\widehat{v}_{\beta,del}$. The two last plots shows the estimated positive-sequence voltages $\widehat{v}_{\alpha,1}$ and $\widehat{v}_{\beta,1}$ and the negative-sequence voltages $\widehat{v}_{\alpha,2}$ and $\widehat{v}_{\beta,2}$. Properties with subscript α is drawn with red lines and properties with subscript β with blue lines. The time constant is chosen to be $\tau_{i,ASC} = 5\,\mathrm{ms}$.

The input voltages are balanced. After an initial transient period the positive-sequence signals equal the input signals and the negative-sequence signals are cancelled out.

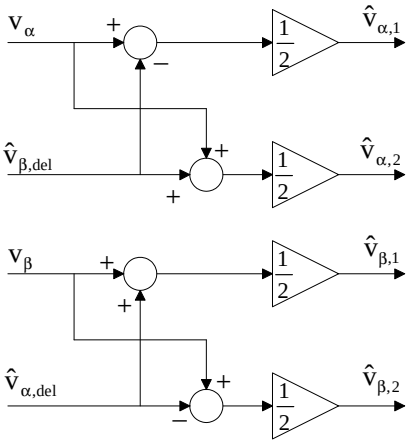

Figure 12.19: Block diagram of Phase Sequence Detector.

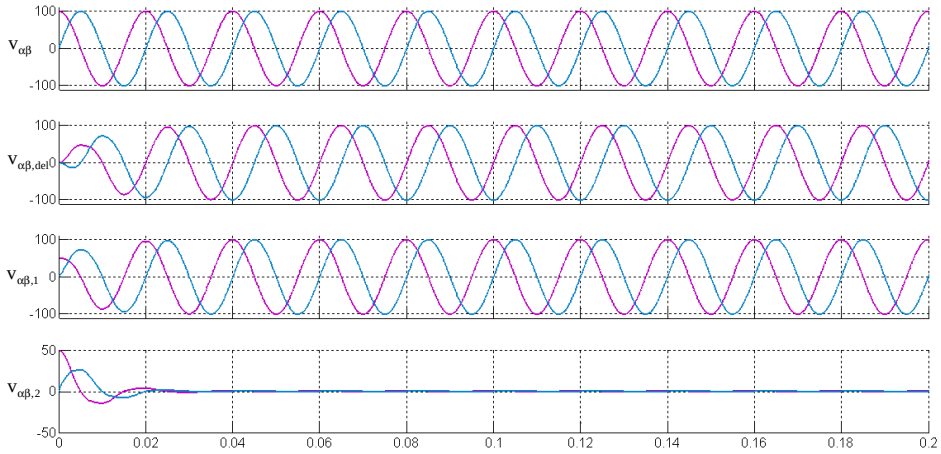

Figure 12.20: Input signals and estimated signals with $\tau_{i,ASC} = 5\,\mathrm{ms}$. From the top: $v_{\alpha\beta}$, $\widehat{v}_{\alpha\beta,del}$, $\widehat{v}_{\alpha\beta,1}$ and $\widehat{v}_{\alpha\beta,2}$.

If the PLL is lagging or leading, the estimated signals became phase shifted and saturated, as can be seen on Fig. 12.15. This will influence the output of the Phase Sequence Detector too, but the impact is less, since the calculations of equations (12.15) and (12.16) act as an averaging of the input signals and the estimated delays. This will both reduce the waveform distortion and the angle displacement. Fig. 12.21 and 12.22 illustrate the impact of the PLL leading and lagging $90°$, respectively. Since the original signals v_α and v_β and the estimated delayed signals $\widehat{v}_{\alpha,del}$ and $\widehat{v}_{\beta,del}$ are not $90°$ phase shifted, the negative sequence signals will not be cancelled out. Actually, for a PLL lagging $90°$, the negative-sequence signals exceed the positive-sequence signals.

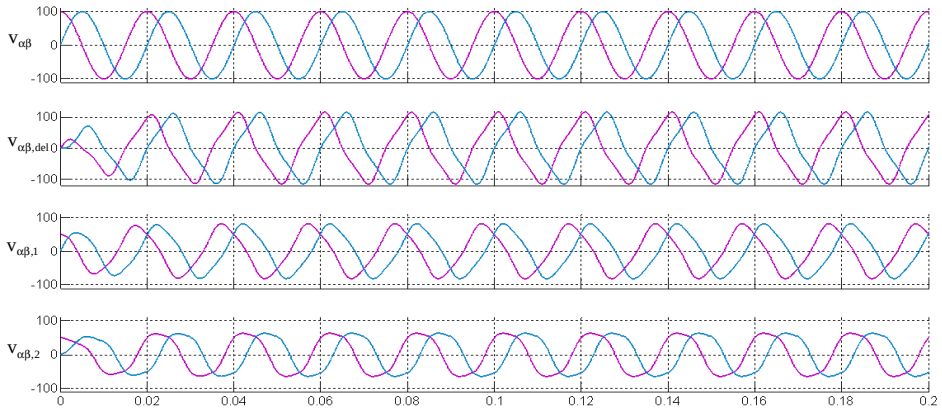

Figure 12.21: Input signals and estimated signals with $\tau_{i,ASC} = 5\,\mathrm{ms}$ and the PLL leading $90°$. From the top: $v_{\alpha\beta}$, $\widehat{v}_{\alpha\beta,del}$, $\widehat{v}_{\alpha\beta,1}$ and $\widehat{v}_{\alpha\beta,2}$.

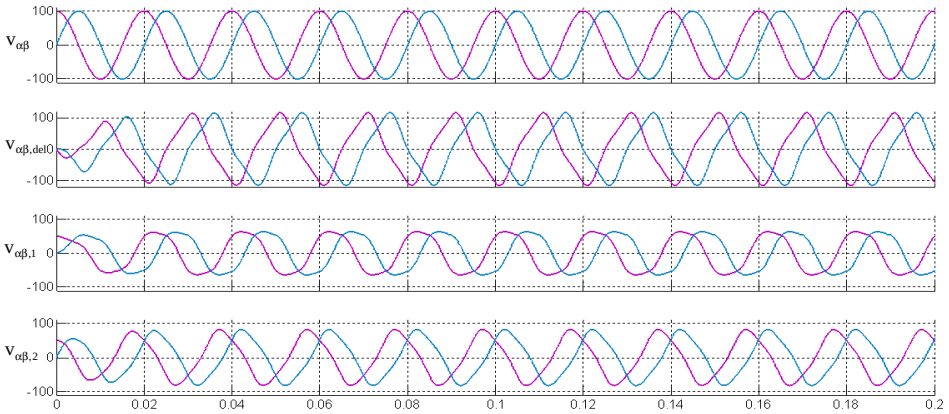

Figure 12.22: Input signals and estimated signals with $\tau_{i,ASC} = 5\,\mathrm{ms}$ and the PLL lagging $90°$. From the top: $v_{\alpha\beta}$, $\widehat{v}_{\alpha\beta,del}$, $\widehat{v}_{\alpha\beta,1}$ and $\widehat{v}_{\alpha\beta,2}$.

Fig. 12.23 shows a case where the signals v_α and v_β contain 10% 5^{th} harmonic. The averaging properties of the Phase Sequence Detector reduces the harmonic content of the positive-sequence signals. The negative-sequence signals simply contain the 5^{th} harmonic. Finally, a 20% voltage drop was applied at $t = 0.1\,\text{s}$. This is shown on Fig. 12.24. The positive-sequence signals follow the input voltages after some settling time; during this transient period the negative-sequence signals deviate from zero.

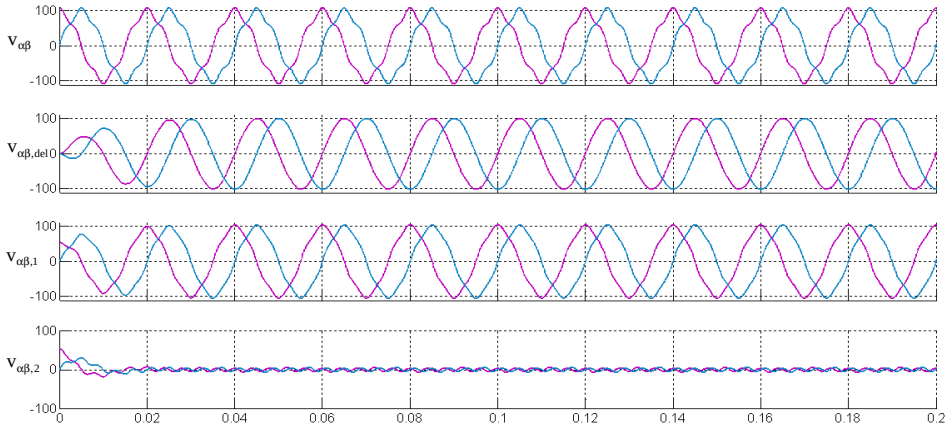

Figure 12.23: Input signals and estimated signals with $\tau_{i,ASC} = 5\,\text{ms}$ and 10% 5^{th} harmonic voltages. From the top: $v_{\alpha\beta}$, $\widehat{v}_{\alpha\beta,del}$, $\widehat{v}_{\alpha\beta,1}$ and $\widehat{v}_{\alpha\beta,2}$.

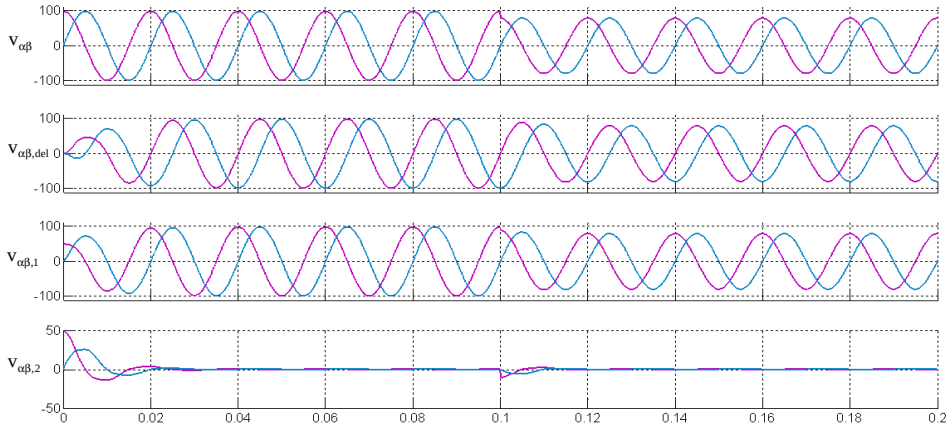

Figure 12.24: Input signals and estimated signals with $\tau_{i,ASC} = 5\,\text{ms}$ and 20% voltage drop at $t = 0.1\,\text{s}$. From the top: $v_{\alpha\beta}$, $\widehat{v}_{\alpha\beta,del}$, $\widehat{v}_{\alpha\beta,1}$ and $\widehat{v}_{\alpha\beta,2}$.

Realization in FPGA

The system described in fig. 1 was realized on an FPGA of type Xilinx Virtex 2. The clock frequency is 40 MHz, and the sampling frequency of the AD converters is 200kS/s. The FPGA board is placed in a LabView computer and is programmed by compiling LabView code to VHDL code. In [48], a solution is described where additional current and voltage controllers are included in the FPGA design.

By using an FPGA, one obtains very fast calculations and a structure with many parallel functions. The design is robust. FPGA cannot perform floating point calculations, and the multiplications need logic space. Sine and cosine calculations are solved by using look-up tables. Data is transferred between parallel functions by using FIFO registers.

The transfer function for the Signal Delay Estimator is given in equation (12.12). However, this is based on linear conditions in the feed-back loops, while Fig. 12.13 - 12.19 reveal that the error signal e is non-linear. Normally the error signal would decrease exponentially for a first order control loop. The envelope (dashed line) on Fig. 12.25 represents a typical continuous error signal, while the solid line resembles the error signal of the Signal Delay Estimator.

The relationship between the peak value and the average value of a rectified sinusoidal signal x is

$$x_{average} = \frac{2}{\pi}\widehat{x} \tag{12.17}$$

where $x_{average}$ is the average value of the signal and $\widehat{x}$ is the peak value. This also applies for a decaying signal where

$$x_{average}\left(t\right) = X_{average} \cdot e^{-\frac{t}{T}} = \frac{2}{\pi} \cdot \widehat{X} \cdot e^{-\frac{t}{T}} \tag{12.18}$$

where $X_{average}$ and $\widehat{X}$ are the initial values of the average and peak signal, respectively. The ratio between the average value of the continuous line and the envelope is $\frac{2}{\pi}$, then.

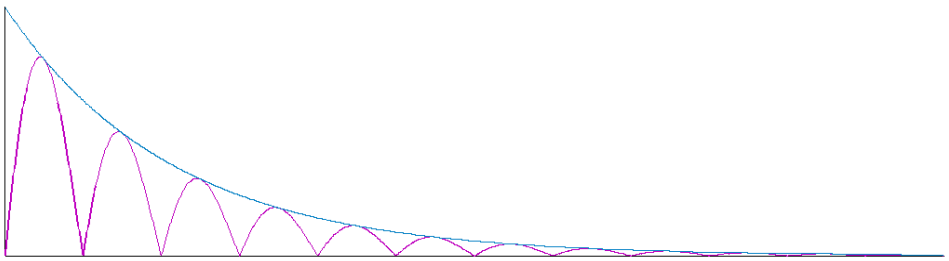

Figure 12.25: Non-linear error signal e (red line) with an exponentially decaying envelope (blue line).

Since the average value of the error signal is reduced, the control loop takes correspondingly longer time to settle. The relationship between the time constant $\tau_{i,ASC}$ and the effective time constant $\tau_{i,ASC}{}'$ is given in equation (12.19):

$$\tau_{i,ASC}{}' = \frac{\pi}{2}\tau_{i,ASC} \tag{12.19}$$

Modelling the ASC algorithm in frequency domain

Substituting equationc (12.13) and (12.14) into equations (12.15) and (12.16) yields equations (12.20) and (12.21):

$$\begin{aligned} \widehat{v}_{\alpha,1} &= \tfrac{1}{2}\left(V_\alpha \cos\theta + \widehat{V}_\beta \cos\widehat{\theta}\right) \\ \widehat{v}_{\beta,1} &= \tfrac{1}{2}\left(V_\beta \sin\theta + \widehat{V}_\alpha \sin\widehat{\theta}\right) \end{aligned} \tag{12.20}$$

$$\begin{aligned} \widehat{v}_{\alpha,2} &= \tfrac{1}{2}\left(V_\alpha \cos\theta - \widehat{V}_\beta \cos\widehat{\theta}\right) \\ \widehat{v}_{\beta,2} &= \tfrac{1}{2}\left(V_\beta \sin\theta - \widehat{V}_\alpha \sin\widehat{\theta}\right) \end{aligned} \tag{12.21}$$

According to equation (11.2), the synchronous reference reactive voltage component will be equation (12.22):

$$\begin{aligned} v_q &= v_{\alpha,1}\sin\widehat{\theta} - v_{\beta,1}\cos\widehat{\theta} \\ &= \tfrac{1}{2}\left(V_\alpha \sin\widehat{\theta}\cos\theta + \widehat{V}_\beta \sin\widehat{\theta}\cos\widehat{\theta}\right) - \tfrac{1}{2}\left(V_\beta \sin\theta\cos\widehat{\theta} + \widehat{V}_\alpha \sin\widehat{\theta}\cos\widehat{\theta}\right) \end{aligned} \tag{12.22}$$

As can be seen from Fig. 11.3, this voltage component equals the error signal e, which can be written as equation (12.23):

$$e = -v_q = -\frac{1}{2}\left[V_\alpha \sin\widehat{\theta}\cos\theta - V_\beta \sin\theta\cos\widehat{\theta} + \frac{1}{2}\left(\widehat{V}_\beta - \widehat{V}_\alpha\right)\sin 2\widehat{\theta}\right] \tag{12.23}$$

The estimated voltage amplitudes $\widehat{V}_\alpha$ and $\widehat{V}_\beta$ will need some response time according to equation (12.19). Thus, the dynamic expression of these variables will be equation (12.24):

$$\begin{aligned} \widehat{V}_\alpha &= \tfrac{1}{\tau'_{i,ASC}s+1} V_\alpha \\ \widehat{V}_\beta &= \tfrac{1}{\tau'_{i,ASC}s+1} V_\beta \end{aligned} \tag{12.24}$$

Substituting equation (12.24) into equation (12.23) gives equation (12.25):

$$\begin{aligned} e = -v_q &= -\tfrac{1}{2}\left[V_\alpha \sin\widehat{\theta}\cos\theta - V_\beta \sin\theta\cos\widehat{\theta} + \tfrac{1}{2}\left(V_\beta - V_\alpha\right)\tfrac{1}{\tau'_{i,ASC}s+1}\sin 2\widehat{\theta}\right] \\ &= -\tfrac{1}{2}\left[V_\alpha \sin\widehat{\theta}\cos\theta - V_\beta \sin\theta\cos\widehat{\theta} + \tfrac{1}{2}\left(V_\beta - V_\alpha\right)\tfrac{1}{\tau'_{i,ASC}s+1}\sin 2\widehat{\theta}\right] \end{aligned} \tag{12.25}$$

This expression can be simplified, as shown in equation (12.26). The calculations are presented in Appendix A.

$$e = \frac{1}{4}\left[\begin{array}{c} (V_\alpha + V_\beta)\sin(\theta - \widehat{\theta}) \\ +\left(V_\beta - V_\alpha\right)\left(\sin(\theta + \widehat{\theta}) - \tfrac{1}{\tau'_{i,ASC}s+1}\sin 2\widehat{\theta}\right) \end{array}\right] \tag{12.26}$$

A block diagram of the complete PLL, including the non-linear elements of equation (12.26), are shown on Fig. 12.26. There are three non-linear branches on the left side of the figure. The upper one is the common one. It has negative feedback and can easily be linearized around an equilibrium point for $\widehat{\theta} \approx \theta$. The middle branch has a positive feedback, and the lower one is not at all affected by the reference signal.

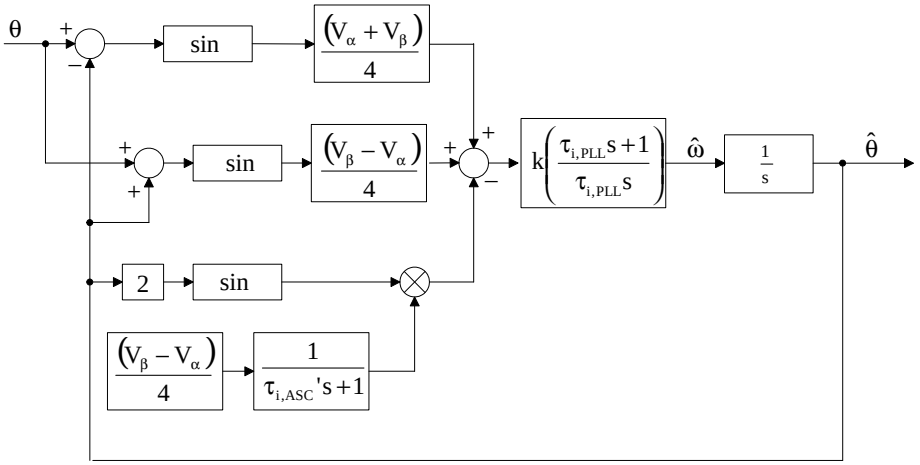

Figure 12.26: Block diagram of PLL with an ASC circuit.

If the grid voltages are symmetrical, then $V_\alpha = V_\beta = V$, and equation (12.26) will be simplified to equation (12.27):

$$e = \frac{V}{2} \sin\left(\theta - \widehat{\theta}\right) \tag{12.27}$$

If the voltages are unbalanced, meaning that $V_\alpha \neq V_\beta$, equation (12.26) still will be simplified to equation (12.27), assumed that the PLL locks properly. For $\widehat{\theta} \approx \theta$, the expression $\sin\left(\theta + \widehat{\theta}\right)$ can be written as $\sin 2\widehat{\theta}$, and then the last part of equation (12.26) cancels out after some initial transient period.

By rearranging Figure 12.26, the block diagram appears as depicted on Fig. 12.27, separated into a linear System 1 and a non-linear System 2. A Maclaurin expansion of 5^{th} order is made on the first part of equation (12.26), as expressed in equation (12.28):

$$\begin{aligned} &\tfrac{(V_\alpha+V_\beta)}{4} \sin\left(\theta - \widehat{\theta}\right) \approx \tfrac{(V_\alpha+V_\beta)}{4} \left(\theta - \widehat{\theta}\right) \\ &+\tfrac{(V_\alpha+V_\beta)}{4} \left(-\tfrac{\left(\theta-\widehat{\theta}\right)^3}{3!} + \tfrac{\left(\theta-\widehat{\theta}\right)^5}{5!} - \tfrac{\left(\theta-\widehat{\theta}\right)^7}{7!} + \tfrac{\left(\theta-\widehat{\theta}\right)^9}{9!}\right) \end{aligned} \tag{12.28}$$

The linear element $\frac{(V_\alpha+V_\beta)}{4} \left(\theta - \widehat{\theta}\right)$ is included in System 1, while the rest of the Maclaurin expansion is put into System 2. Thus, all non-linear elements are collected in one common block.

As earlier mentioned, for balanced voltages and a locked PLL, System 2 cancels out, but in order to investigate stability limits during voltage asymmetry and other disturbances, a more thorough analysis is needed. One criterion for stability is the Small Gain Theorem [62].

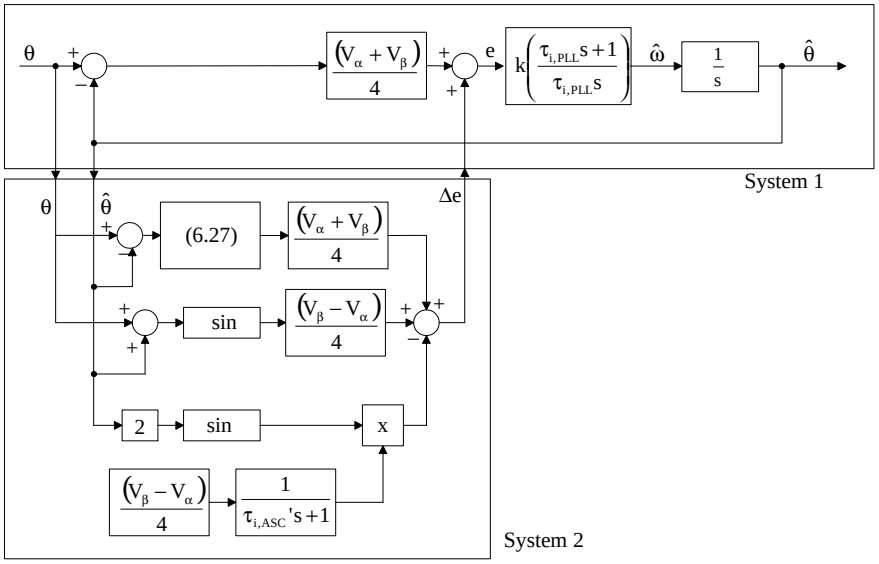

Figure 12.27: Block diagram of the PLL arranged into a linear system (System 1) and a non-linear system (System 2).

Theorem 1 *Consider two stable systems S_1 and S_2 in a feedback loop according to Fig. 12.28. The closed loop system, thus defined with r_1, r_2 as inputs and e_1, e_2, y_1 y_2 as outputs is input-output stable if the product of the gains is less than* 1*:*

$$\|S_2\| \cdot \|S_1\| < 1 \tag{12.29}$$

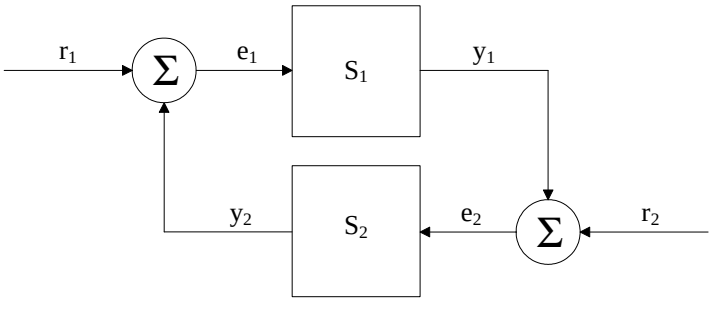

Figure 12.28: A closed loop system.

Table 12.4: Comparison between exact calulation and Maclaurin expansion

$\theta - \widehat{\theta}$	$\sin\left(\theta - \widehat{\theta}\right)$	Maclaurin expansion
$-\pi$	0	-0.0069
$-\frac{\pi}{2}$	-1	-1.0
0	0	0
$\frac{\pi}{2}$	1	1.0
π	0	0.0069

It is evident that the maximum gain of System 1 is as stated in equation (12.30)

$$\|S_1\| = k \tag{12.30}$$

For the non-linear system, System 2, determining the system gain is more laborious. Three branches contribute to this gain.

The Maclaurin expansion in equation (12.28) is quite accurate for input signals in the range from $-\pi$ to π. Table 12.4 compares exact values and approximated values using the Maclaurin expansion. The small signal will be confined to $\pm\pi$ in the further analysis, since this will cover a complete revolution of the reference angle.

The part of the expansion contained in System 2 can be defined as equation (12.31):

$$\begin{aligned}\Delta e_1 &= \tfrac{(V_\alpha+V_\beta)}{4}\left(-\tfrac{\left(\theta-\widehat{\theta}\right)^3}{3!}+\tfrac{\left(\theta-\widehat{\theta}\right)^5}{5!}-\tfrac{\left(\theta-\widehat{\theta}\right)^7}{7!}+\tfrac{\left(\theta-\widehat{\theta}\right)^9}{9!}\right)\\ &= \tfrac{(V_\alpha+V_\beta)}{4}\left(\sin\left(\theta-\widehat{\theta}\right)-\left(\theta-\widehat{\theta}\right)\right)\end{aligned} \tag{12.31}$$

This element will reach its maximum for $\theta - \widehat{\theta} = -\pi$. Then $\Delta e_1 = \frac{(V_\alpha+V_\beta)}{4}\pi$. Similarly, $\Delta e_1 = -\frac{(V_\alpha+V_\beta)}{4}\pi$ for $\theta - \widehat{\theta} = \pi$. To obtain maximum gain from this branch of System 2, it is thus assumed that $\widehat{\theta} = \theta - \pi$.

The second and the third branch of the system both contain trigonometric elements. These two branches can be combined in a signal called Δe_2, given in equation (12.32):

$$\Delta e_2 = \frac{(V_\beta - V_\alpha)}{4}\left[\sin\left(\theta+\widehat{\theta}\right)-\sin\left(2\widehat{\theta}\right)\right] \tag{12.32}$$

The second branch contains the expression $\sin\left(\theta+\widehat{\theta}\right)$, which in this particular case will be $\sin(2\theta-\pi)$. The gain of the third branch has a dynamic element, which will increase exponentially from zero to 1. One therefore assumes that this particular dynamic element has reached its final value, and the third element can be written as $\frac{V_\beta-V_\alpha}{4}\sin\left(2\widehat{\theta}\right)$. For $\widehat{\theta} = \theta - \pi$ it can be expressed as $\frac{V_\beta-V_\alpha}{4}\sin(2\theta-2\pi)$. For maximum gain Δe_2 will become equation (12.33):

$$\begin{aligned}\Delta e_{2,\max} &= \tfrac{(V_\beta-V_\alpha)}{4}\left[\sin(2\theta-\pi)-\sin(2\theta-2\pi)\right]\\ &= -\tfrac{(V_\alpha-V_\beta)}{2}\sin 2\theta\end{aligned} \tag{12.33}$$

By differentiating this expression, the reference angle giving maximum gain can be determined, as shown in equation (12.34):

$$\frac{d\Delta e_{2,\max}}{dt} = -\frac{(V_\beta - V_\alpha)}{2}\cos 2\theta = 0 \tag{12.34}$$

The angle $\theta = \frac{\pi}{4}$ will thus give a maximum gain of Δe_2. Substituting the angle into equation (12.33) yields equation (12.35):

$$\Delta e_{2,\max} = -\frac{(V_\beta - V_\alpha)}{4}\left[\sin\left(\frac{\pi}{2} - \pi\right) - \sin\left(\frac{\pi}{2} - 2\pi\right)\right] = \frac{(V_\beta - V_\alpha)}{2} \tag{12.35}$$

This gain will also depend on the voltage asymmetry $V_\beta - V_\alpha$ with a maximum for $V_\alpha = 0$. The amplitude of the phase voltages will have a nominal value of $\sqrt{\frac{2}{3}}$ of the rms line voltage of the grid. According to [7] the grid voltage should never exceed 120% of nominal voltage. With a nominal line voltage of $230\,\mathrm{V}$, the voltage amplitude is chosen to be $V_\beta = 225$. The total gain of System 2 will then be expressed by equation (12.36)

$$\|S_2\| = (V_\alpha + V_\beta)\,\frac{\pi}{4} + (V_\beta - V_\alpha)\,\frac{1}{2} \tag{12.36}$$

For $V_\alpha = 0$ this will be simplified to:

$$\|S_2\| = V_\beta\left(\frac{\pi}{4} + \frac{1}{2}\right) \tag{12.37}$$

Applied on the Small Signal Theorem this leads to equation (12.38):

$$k \cdot V_\beta\left(\frac{\pi}{4} + \frac{1}{2}\right) < 1 \tag{12.38}$$

implying that for $k < 0.00346$ the system is stable. However, this is a conservative criterion, meaning that the system could still be stable even if the Small Signal Theorem is not fulfilled.

As described in Chapter 11.1, the linear part of the PLL will increase $\widehat{\omega}$, since the average value of the error signal e will be positive. The reason is that the positive half cycle of the error signal will have a longer duration than the negative. This component of the error signal will be denoted as e_1. Fig. 12.26 shows also two other components of the error signal: $e_2 = \frac{V_\beta - V_\alpha}{4}\sin\left(\theta + \widehat{\theta}\right)$ and $e_3 = \frac{V_\beta - V_\alpha}{4\left(\tau'_{i,ASC}s+1\right)}\sin\left(2\widehat{\theta}\right)$.

The signal component e_2 will give a slight negative contribution to the PLL. During the negative half cycle of e_2 the estimated angle velocity $\widehat{\omega}$ will be more or less reduced; as can be seen from Fig. 12.29, depending on the parameters of the PI controller. This will reduce the slope of the estimated reference angle $\widehat{\theta}$. During the positive half cycle the situation is opposite, thus the negative half cycle will be slightly longer than the positive. The signal component e_2 will bring the estimated angle velocity $\widehat{\omega}$ from some initial value down to zero. The impact is not very significant, since e_2 also is dependent of θ, which normally will have an average value of zero.

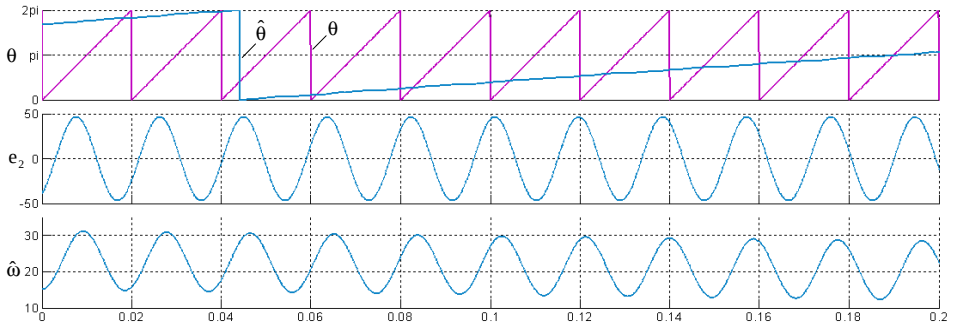

Figure 12.29: Error signal component e_2 during startup. From the top: Reference angle θ (red line) and estimated angle $\widehat{\theta}$ (blue line), error signal component e_2 and estimated angular velocity $\widehat{\omega}$.

The signal component e_3 will also reduce the estimated angle velocity $\widehat{\omega}$, as can be seen from Fig. 12.30. Since e_2 is independent of θ, it will give a considerably larger contribution to the frequency reduction than e_2.

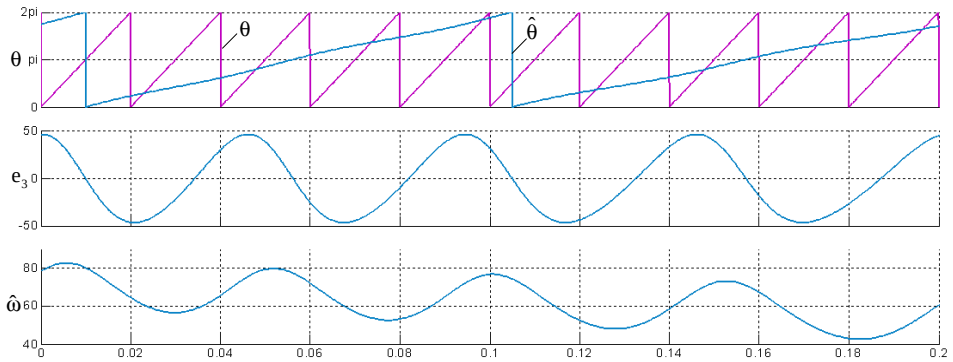

Figure 12.30: Error signal component e_3 during startup. From the top: Reference angle θ (red line) and estimated angle $\widehat{\theta}$ (blue line), error signal component e_3 and estimated angular velocity $\widehat{\omega}$.

In other words, the signal component e_1 tries to increase the estimated frequency following some path $\widehat{\omega}_1$, while the components e_2 and e_3 try to decrease the frequency along the paths $\widehat{\omega}_2$ and $\widehat{\omega}_3$, respectively. This is shown on Fig. 12.31.

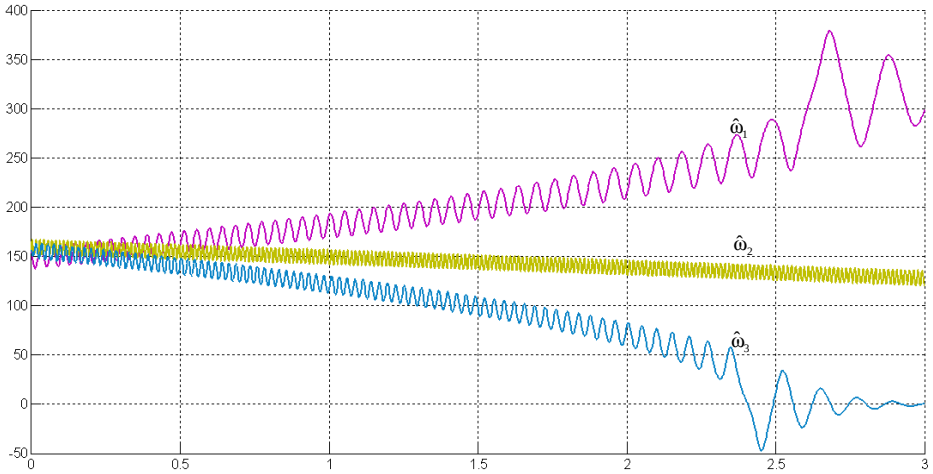

Figure 12.31: Frequency change for different error signal components.

Fig. 12.31 also reveals that $\widehat{\omega}_1$ dominates for higher frequencies, while $\widehat{\omega}_2$ and $\widehat{\omega}_3$ dominate for lower frequencies. Thus there exists some lower boundary frequency $\widehat{\omega}_{\mathrm{lim}}$ for the initial value of the estimated frequency $\widehat{\omega}$. If the initial value goes beyond this limit, the PLL will slow down until $\widehat{\omega}$ becomes zero. If, however, the initial value is above this limit, the PLL will speed up until it locks at grid frequency. The boundary frequency $\widehat{\omega}_{\mathrm{lim}}$ is dependent on the voltage components V_α and V_β; the controller parameters k and $\tau_{i,PLL}$, plus the time constant $\tau_{i,ASC}$. Due to its complexity, it is not possible to reach an analytical solution for this limit. However, empirical data are collected in Tables 12.5 - 12.8, showing the relationship between the boundary frequency $\widehat{\omega}_{\mathrm{lim}}$ and the above mentioned parameters.

Table 12.5 shows that the PLL will always lock if the voltages are symmetrical. If however, there is some asymmetry at start-up time, the estimated frequency $\widehat{\omega}$ needs to have an initial value depending on the degree of asymmetry.

Table 12.5: Boundary frequency $\widehat{\omega}_{\mathrm{lim}}$ for different asymmetic voltages

V_α [V]	V_β [V]	$\widehat{\omega}_{\mathrm{lim}}$ [rad/s]
186	186	0
93	186	37
186	93	49
0	186	198
186	0	193

Table 12.6 reveals that an increasing value of the controller gain k provides a higher initial value of $\widehat{\omega}$. The reason is that the faster response of the controller makes $\widehat{\omega}$ vary over a wider range and then the average value of e_2 and e_3 will fluctuate more from zero.

Table 12.6: Boundary frequency $\widehat{\omega}_{\mathrm{lim}}$ for different values of proportional gain

V_α [V]	V_β [V]	k	$\widehat{\omega}_{\mathrm{lim}}$ [rad/s]
186	93	0.075	42
186	93	0.15	49
186	93	0.3	63
186	0	0.075	189
186	0	0.15	193
186	0	0.3	204

Changing the time constant of the controller has a similar effect, as can be seen from Table 12.7, for the same reason: a fast response allows $\widehat{\omega}$ to vary over a wider range; a short time constant requires a higher initial value of $\widehat{\omega}$.

Table 12.7: Boundary frequency $\widehat{\omega}_{\mathrm{lim}}$ for different values of PLL time constant

V_α [V]	V_β [V]	$\tau_{i,PLL}$	$\widehat{\omega}_{\mathrm{lim}}$ [rad/s]
186	93	0.002	72
186	93	0.005	49
186	93	0.015	39
186	0	0.002	211
186	0	0.005	193
186	0	0.015	186

According to Fig. 12.27, the time constant $\tau_{i,ASC}$ of the Signal Delay Estimator should not influence the frequency range vsignificantly. Table 12.8 confirms this assumption, but there is still some relationship between the time constant and the boundary frequency $\widehat{\omega}_{\mathrm{lim}}$. The explanation is that a slow response of the Signal Delay Estimator reduces the impact of e_3, thereby allowing the PLL to lock for slightly lower initial frequencies.

Table 12.8: Boundary frequency $\widehat{\omega}_{\mathrm{lim}}$ for different values of ASC time constant

V_α [V]	V_β [V]	$\tau_{i,ASC}$	$\widehat{\omega}_{\mathrm{lim}}$ [rad/s]
186	93	0.001	51
186	93	0.005	49
186	93	0.025	41
186	0	0.001	194
186	0	0.005	193
186	0	0.025	191

Tables 12.5 - 12.8 are made in order to determine the performance limits for the circuit. During normal operation, however, there will not be an option to connect the DPGS to the grid, since a pronounced asymmetry is a severe fault situation. Moreover, the initial value of $\widehat{\omega}$ should be $\widehat{\omega}_c = 100\pi$, which is far above $\widehat{\omega}_{\lim}$ in any case. In other words, by adding $\widehat{\omega}_c$ to the output of the controller, the PLL will always lock. As long as the PLL remains locked and keeps on tracking the real reference angle θ, equation (12.26) will be simplified to equation (12.27):

$$e = \frac{1}{4}\left(V_\alpha + V_\beta\right)\sin\left(\theta - \widehat{\theta}\right) \tag{12.39}$$

By linearizing the transfer function for the PLL around $\theta - \widehat{\theta} = 0$, the following transfer function for the closed loop is obtained:

$$H_{PLL}\left(s\right) = \frac{k\frac{V_\alpha+V_\beta}{4}\frac{\tau_{i,PLL}s+1}{\tau_{i,PLL}s}\frac{1}{s}}{1+k\frac{V_\alpha+V_\beta}{4}\frac{\tau_{i,PLL}s+1}{\tau_{i,PLL}s}\frac{1}{s}} = \frac{k\frac{(V_\alpha+V_\beta)}{4}s + k\frac{(V_\alpha+V_\beta)}{4\tau_{i,PLL}}}{s^2 + k\frac{(V_\alpha+V_\beta)}{4}s + k\frac{(V_\alpha+V_\beta)}{4\tau_{i,PLL}}} \tag{12.40}$$

For symmetrical conditions $V_\alpha = V_\beta = V_m$. Then equation (12.40) can be further simplified:

$$H_{PLL}\left(s\right) = \frac{\frac{V_m k}{2}s + \frac{V_m k}{2\tau_{i,PLL}}}{s^2 + \frac{V_m k}{2}s + \frac{V_m k}{2\tau_{i,PLL}}} = \frac{2\zeta\omega_n s + {\omega_n}^2}{s^2 + 2\zeta\omega_n s + {\omega_n}^2} \tag{12.41}$$

where $\omega_n = \sqrt{\frac{V_m \cdot k}{2\tau_{i,PLL}}}$ and $\zeta = \sqrt{\frac{\tau_{i,PLL}V_m k}{8}}$.

Equation (12.42) expresses the command to tracking error transfer function of the PLL:

$$N_{PLL}\left(s\right) = \frac{1}{1+\frac{V_m k(\tau_{i,PLL}s+1)}{2\tau_{i,PLL}s^2}} = \frac{s^2}{s^2 + \frac{V_m k}{2}s + \frac{V_m k}{2\tau_{i,PLL}}} \tag{12.42}$$

System Stability

Table 12.9 shows the chosen parameter values for the controllers. These values give an angular frequency $\omega_n = 13.3\,\mathrm{rad/\,s}$ and a damping $\zeta = 0.067$.

Table 12.9: Control parameters

V_m	230
k	0.0154
$\tau_{i,PLL}$	0.01
$\tau_{i,ASC}$	0.005

The cutoff frequency for the PLL is chosen to be about 2.1 Hz, which should give sufficient response for common frequency variations on the grid. The tuning of the PLL is a trade-off between proper filtering and sufficient damping. The ASC circuit is tuned to give a fast response. Fig. 12.32 shows the Bode diagram of the PLL, using the parameter values shown in Table 12.9. Typical frequency grid deviations caused by rotor oscillations will be quite slow. It can be seen from Fig. 12.32 that rotor oscillations with a frequency of $1.0\,\mathrm{Hz}$ will be dampened by -45dB, equivalent to 0.56%.

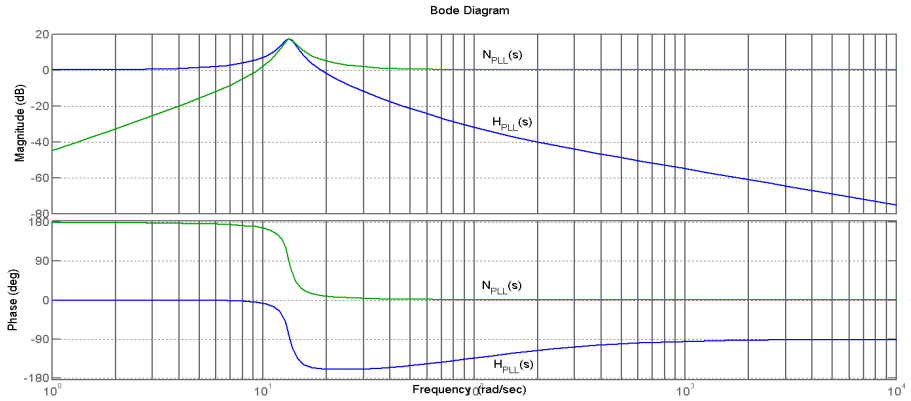

Figure 12.32: Bode diagram of the PLL.

Simulation Results

A major voltage drop could be critical to the equipment. A voltage drop exceeding 50% of nominal voltage should be cleared in 160ms, according to [7]. The same applies to a voltage swell exceeding 120% of nominal voltage.

Some typical faults causing asymmetry are described in [63]. One of them is a single-line-to-ground fault (slg), where the phase voltage of one phase drops as a result of a ground fault. A line-to-line fault (ll) causes the phase voltage angles to move closer to each other, and the voltage drops in the power lines create a voltage drop in the affected phases. A line-to-line-to-ground fault (llg) causes a voltage drop in the affected phases. These arcing faults are shown in Fig. 12.33.

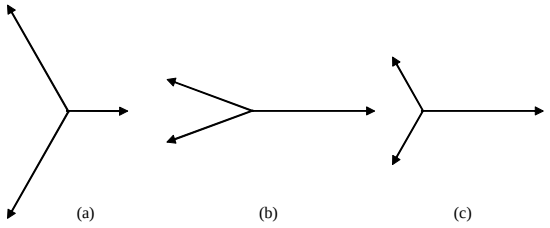

Figure 12.33: Asymmetry caused by arcing faults: (a) single-line-to-ground fault; (b) line-to-line fault; (c) line-to-line-to-ground fault.

Generators with a weak connection to the utility grid may show considerable rotor oscillation as a response to a disturbance, with a fluctuating frequency as a result. This can be the case in distribution networks with a combination of wind power and hydro power. A sudden gust of wind can cause rotor oscillation in hydro power generators close to the wind farm. Voltage harmonics may also reduce the performance of distribution generation equipment. The total harmonic distortion (THD) should be less than 8%, according to [64]. Simulations were done in Matlab/Simulink.

Voltage Sag and Swell

Fig. 12.34 shows simulation results of the above mentioned voltage disturbances. The low-pass characteristic of the signal delay estimator is the source of the apparent negative sequence signals immediately after the step changes. In Fig. 12.34a and b it takes just $5\,\mathrm{ms}$ for the positive sequence signal to cross the thresholds of 80% and 110% of nominal voltage, respectively.

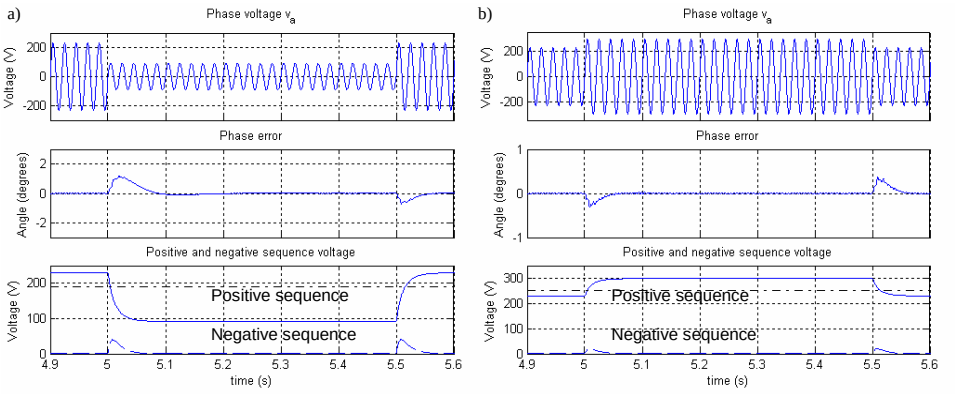

Figure 12.34: Grid voltage step changes: (a) Voltage sag to 40% of nominal value; (b) Voltage swell to 130% of nominal value. The dash-dot line indicates 110% of nominal voltage.

Voltage Asymmetry

In this case, the phase voltages of phase b and c are reduced to 75% of nominal voltage and the voltages are phase shifted 30° towards each other. The fault occurs at $5.0\,\mathrm{s}$ and lasts for $0.5\,\mathrm{s}$.

Fig. 12.35 shows the performance of the circuit during these conditions. The phase voltage plot reveals that the voltage is suddenly phase shifted and decreased. The positive and negative sequence signals behave as expected.

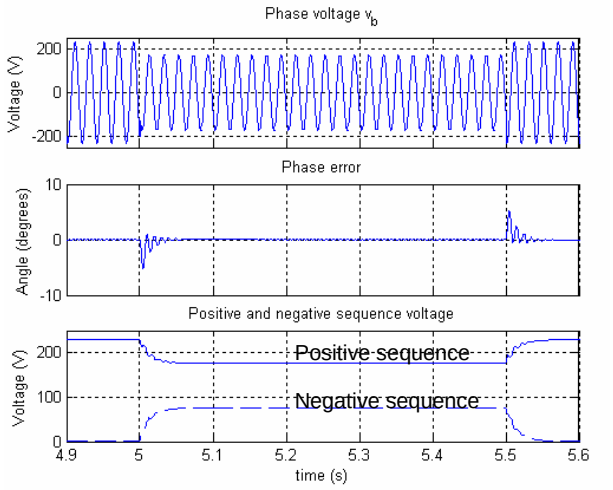

Figure 12.35: Line-to-line fault. From the top: Phase voltage v_b; phase error; positive (solid) and negative (dashed) sequence voltage.

Frequency Variation

The time variant angular frequency is defined in equation (12.43):

$$\omega\left(t\right) = 100\pi + 5e^{-0.2t}\sin\left(2t\right) \tag{12.43}$$

where $\omega\left(t\right)$ is the time variant angular frequency of the grid.

A comparison is made between the suggested design and the PLL proposed in [49]. Symmetrical voltages with nominal values are supplied for $10\,\mathrm{s}$, and the frequency changes as expressed in equation (12.43). Performance of estimated angle frequency and voltage reference angle are to be analyzed.

Fig. 12.36 shows the performance of the two different solutions. Since the multi variable filter is tuned at $50\,\mathrm{Hz}$, frequency deviations will cause significant phase displacement to occur. During normal operation ($49.9 - 50.1\,\mathrm{Hz}$) this will not be a big problem, but Fig. 12.36 reveals that any deviation from $50.0\,\mathrm{Hz}$ will cause some phase displacement. The solution proposed in this paper, on the other hand, is very nearly unaffected, since the filtering properties of the PLL is frequency independent.

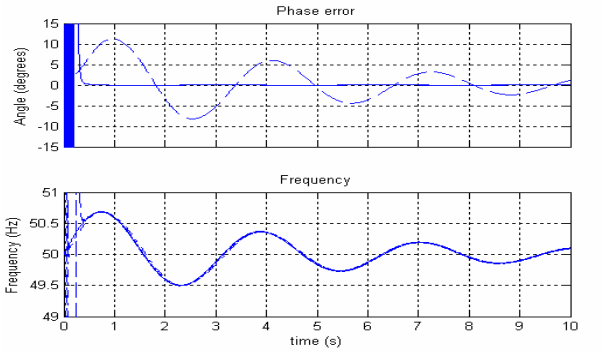

Figure 12.36: Frequency variation. From the top: Phase error: PLL with ASC (solid), PLL with multi variable filter (dashed); Frequency: Grid frequency (solid), estimated frequency from PLL with DSC (dashed) and estimated frequency from PLL with multi variable filter (dashed-dotted).

Voltage Harmonics

In this case, the simulation starts with pure sinusoidal symmetrical voltages, and harmonics are introduced at $5.0\,\mathrm{s}$ and remain for the rest of the simulation. The distorted voltages contain 10% 5^{th} harmonics and 5% 7^{th} harmonics, and this is done in order to go beyond the limits described in [8]. Fig. 12.37 shows that the PLL is influenced by the voltage distortions, and the cyclic deviation is less than one degree, with a period of $10\,\mathrm{ms}$. Total THD for $\sin\widehat{\theta}$ and $\cos\widehat{\theta}$ is 0.8% and 0.68%, respectively, during the period of distortion. The negative sequence signal has a mean value of about $12\,\mathrm{V}$ with a $100\,\mathrm{Hz}$ ripple. The positive sequence signal increases a bit, and also has, for this signal, a $100\,\mathrm{Hz}$ ripple. A circuit for identifying the harmonic content is not included, but it is feasible, provided the harmonics are present in the unfiltered positive and negative sequence signals.

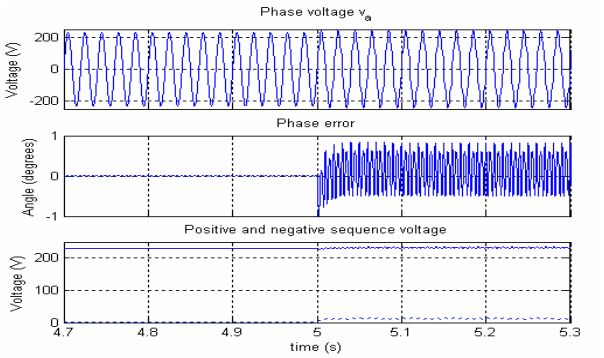

Figure 12.37: Voltage harmonics. From the top: Phase voltage v_a; phase error; positive (solid) and negative (dashed) sequence voltage.

Experimental Setup

Fig. 12.38 shows the block diagram of the experimental setup,and Fig. 12.39 is a picture of the laboratory setup. A voltage reference generator creates reference voltages with user-defined disturbances. These reference values are reproduced by a DC/AC converter with output filter, with the switching frequency at 10 kHz. The filter is an LC-filter with a cutoff-frequency of 1 kHz. The step up transformer is needed to bring the output voltage closer to the nominal voltage of the PLL with the ADC circuit. The transformer is Yy0 connected.

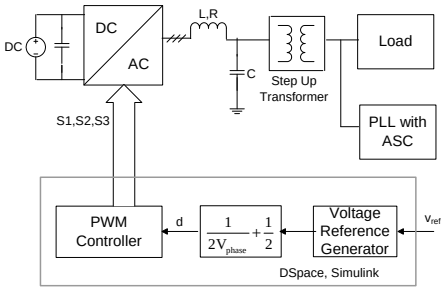

Figure 12.38: Block diagram of the experimental setup.

Figure 12.39: Photo of the experimental setup. To the left is the computer with the reference generator and the PWM. The LC-filter is placed on the table close to the computer, and the DC source is partly hidden by an oscilloscope. The step up transformer is placed on the left part of the table, and the load resistance is placed on the floor below the table. The rack contains measurement equipment and a power converter, and a computer with the FPGA board included is placed on the top of the rack.

Voltage Sag and Swell

Fig. 12.40a and b shows experimental results for voltage sag and swell, respectively. The plots display the positive and the negative sequence signals from the ASC circuit. The response is quite fast and two small peaks in the negative sequence signals occur immediately after the step changes, as expected.

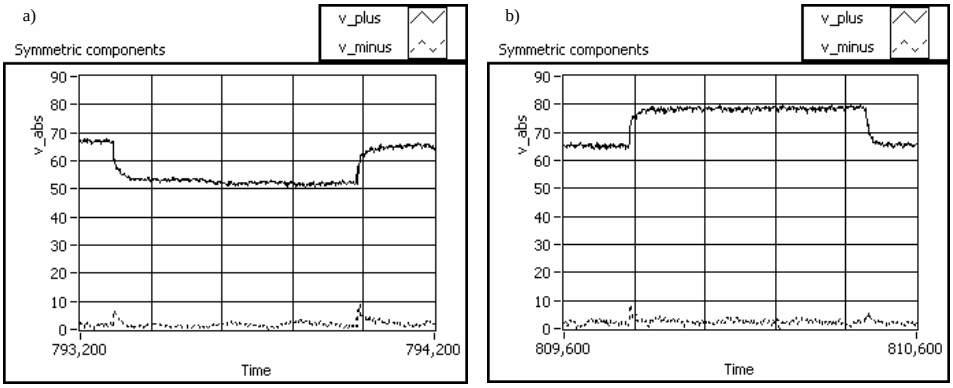

Figure 12.40: (a) Voltage sag to 80% of nominal value. (b) Voltage swell to 120% of nominal value. Solid line: positive sequence component. Dashed line: negative sequence component.

Voltage Asymmetry and frequency variation

Fig. 12.41 shows the plot of a line-to-line fault. During the fault, the voltages of phase b and c are reduced by 35% and shifted $30°$. This severe asymmetry can be readily detected by the signal changes in Figure 12.41.

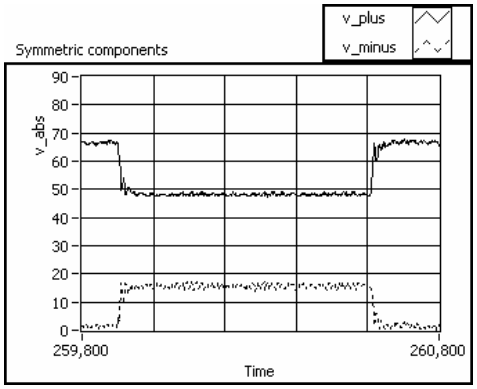

Figure 12.41: Line-to-line fault. 35% sag in phase b and c and a 30 degreees phase shift. Solid line: positive sequence component. Dashed line: negative sequence component.

Fig. 12.42 shows a frequency variation with a maximum overshoot of 3 Hz. The estimated frequency tracks the real frequency during the entire frequency disturbance. Some noise peaks appear on the signal, but the effect on the PLL would be negligible, according to equation (11.14). For control and protection purposes this noise can be filtered out, if necessary.

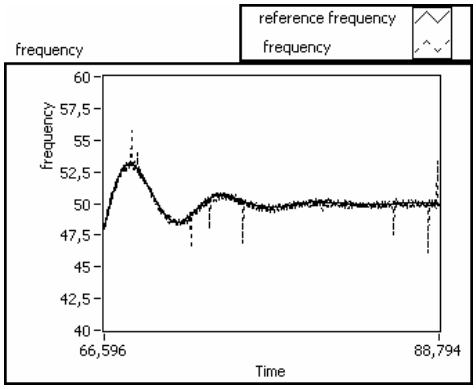

Figure 12.42: Frequency variation. Solid line: reference frequency. Dashed line: estimated frequency.

Finally, phase a was disconnected, and Fig. 12.43 a and b show the performance of the PLL without the ASC circuit and with the ASC circuit, respectively. The filtering properties of the ASC improve the performance significantly, as can be seen from the plots.

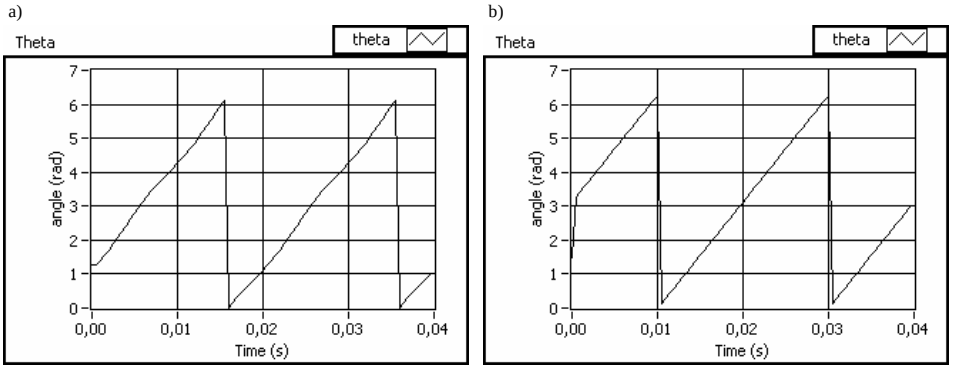

Figure 12.43: a) Reference angle $\widehat{\theta}$ without ASC. b) Reference angle $\widehat{\theta}$ with ASC.

Conclusion

The proposed solution for improving the performance of a synchronizing circuit takes advantage of DSC for calculating the symmetrical components of the three-phase voltages, by using an adaptive method called ASC. The proposed solution is frequency independent and provides signals for protection purposes by estimating instantaneous frequency and voltage values. Simulations and experimental results validate the performance and robustness of the design. The proposed design is significantly better than classical solutions for DPGS with weak grid connection.

13 Application in a power system

This chapter focuses on applying an adaptive synchronizing circuit in a power system. Four subjects need to be considered: Synchronization, fault detection, connection/disconnection, and power management.

Synchronizing

As described in Chapter 7.1, there is a need for synchronizing during normal operation. In addition, as mentioned in Chapter 8.1, the system should have sufficient ride-through capability, which means that during momentary faults, the synchronization circuit should be operational. Even during stand-alone operation, which may be caused by some severe and permanent fault, there is a need for synchronizing. Otherwise it would be impossible to perform a safe reconnection to the grid after the grid restoration. The PLL with ASC described in Chapter 12.5 can handle both short-lived and permanent voltage disturbances. Initially it is sensitive to voltage disturbances, but as soon as the PLL locks, it is very robust.

Fault detection

In order to decide whether to open or close the circuit breaker at PCC, information about the grid voltage conditions must be provided. The PLL with ASC gives information about voltage sags and swells, voltage asymmetry and frequency deviations. Information about voltage harmonics is inherent in the control signals, but must be further refined in order to be fully utilized. In a DPGS some island detection system should also be applied, as described in Chapter 8.2.

Connection and disconnection

An overhead protection circuit should be added to the synchronization and fault detecting circuit for the purpose of connecting and disconnecting DPGS at PCC according to present standards and grid codes. A circuit breaker must be placed at PCC, in order to disconnect the DPGS, if necessary. This circuit breaker must be fast enough to protect equipment from damage and to de-energize the EPS within fixed time limits.

Power management

This overhead circuit should also have functionality for power flow management through PCC and also between the internal components of the DPGS. Different power flow strategies could be evaluated; constant active power flow, reactive power injection, frequency and/or voltage control by means of droop characteristics etc.

14 Concluding Remarks and Suggestions for Further Work

In a DPGS, the voltage conditions at PCC need to be supervised in order to determine when or if to open or close the circuit breaker between the main grid and the DPGS. It would be wise to place a power converter at PCC, thereby enabling a proper control of the power flow between the DPGS and the grid. A synchronizing circuit is needed, in order to synchronize the converter to the grid. It would be beneficial if this circuit also could generate additional control signals for circuit breaker operation at PCC.

This thesis presents alternative designs for synchronizing a power converter to the grid voltages. The synchronizing circuit is based on a PLL. The simplest designs behave well during normal voltage conditions, but will not run properly if certain voltage disturbances occurs. More complex PLL designs with time consuming calculations are to be utilized in order to filter out the disturbances. One way of implementing the design is to create program code running on a fast processor. Another approach is to use an FPGA with multiple structures, thereby obtaining a very fast and reliable system. The FPGA cannot handle floating point calculations. The work described in this thesis is based on different FPGA designs.

The simplest one is a classical PLL in combination with a zero voltage detection circuit. The main benefit of the design is its simplicity, and the main disadvantage is that no grid voltage information is available between the zero crossings. Another PLL design is based on a grid voltage vector calculations and transforms. The design is more complex and contains time consuming calculations. On the other hand, the gird voltages are continuously supervised.

The above mentioned design operates well as long as the grid voltages are balanced and sinusoidal. If, however, voltage harmonics or asymmetry occur, the circuit will not perform well. An additional multi-variable filter was applied on the FPGA design, in order to filter out the disturbances. Experimental tests gave successful results.

The above mentioned multi-variable filter is tuned at a center frequency corresponding to the nominal grid frequency. Normally, the grid frequency will remain practically constant, but, if for some reason, a frequency deviation should take place, the tuned filter will naturally cause a considerable angle displacement of the output signal. An alternative filter design is proposed by the author. The method is based on the DSC method, but instead of delaying the input signals the fourth of a grid voltage period, phase shifted signals are generated, using adaptive measures. This ASC method filters out voltage disturbances, and it runs well even during frequency deviations.

The main purpose of the synchronizing circuit is to provide the current control system of the power converter with an estimated voltage reference angle. In addition, the ASC outputs estimated grid frequency, as well as the magnitudes of the symmetric voltage components. These signals can be used in an overhead structure, both providing power management and protection. If the signals from the ASC exceed certain limits, the circuit breaker at PCC would disconnect the DPGS from the grid.

The ASC should be tested together with a power system, in order to verify that the circuit is robust and shows good performance when also integrated into the entire system. During these test procedures, different kinds of voltage disturbances should be generated.

In a complete DPGS, an overhead protection and power management system is to be built. Some kind of island detection strategy ought to be implemented in the system.

A micro grid with a common internal bus and some energy sources, connected to the

grid at PCC, should be implemented and tested. If the DPGS is expected to run separately during grid disconnection, the inverters should be equipped with proper output filters.

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A Trigonometric calculations

In equation (12.25) the error signal e is defined as

$$e = -\frac{1}{2}\left[V_\alpha \sin\widehat{\theta}\cos\theta - V_\beta \sin\theta\cos\widehat{\theta} + \frac{1}{2}\left(V_\beta - V_\alpha\right)\frac{1}{\tau'_{i,ASC}s+1}\sin 2\widehat{\theta}\right] \tag{A.1}$$

According to [**?**], $\sin\alpha\cos\beta$ can be written as

$$\sin\alpha\cos\beta = \frac{1}{2}\left[\sin\left(\alpha+\beta\right) + \sin\left(\alpha-\beta\right)\right] \tag{A.2}$$

and $\cos\alpha\sin\beta$ can be written as

$$\cos\alpha\sin\beta = \frac{1}{2}\left[\sin\left(\alpha+\beta\right) - \sin\left(\alpha-\beta\right)\right] \tag{A.3}$$

Applying this on equation (A.1), the two first links inside the bracket can be written as

$$\begin{aligned} V_\alpha\cos\theta\sin\widehat{\theta} &= \tfrac{V_\alpha}{2}\left[\sin\left(\theta+\widehat{\theta}\right) - \sin\left(\theta-\widehat{\theta}\right)\right] \\ V_\beta\sin\theta\cos\widehat{\theta} &= \tfrac{V_\beta}{2}\left[\sin\left(\theta+\widehat{\theta}\right) + \sin\left(\theta-\widehat{\theta}\right)\right] \end{aligned} \tag{A.4}$$

Substituting v(A.4) into equation (A.1) yields

$$\begin{aligned} e &= \tfrac{1}{4}\left[\begin{array}{c} -V_\alpha\sin\left(\theta+\widehat{\theta}\right) + V_\alpha\sin\left(\theta-\widehat{\theta}\right) + V_\beta\sin\left(\theta+\widehat{\theta}\right) + V_\beta\sin\left(\theta-\widehat{\theta}\right) \\ +\left(V_\alpha - V_\beta\right)\frac{1}{\tau'_{i,ASC}s+1}\sin 2\widehat{\theta} \end{array}\right] \\ &= \tfrac{1}{4}\left[\begin{array}{c} \left(V_\alpha+V_\beta\right)\sin\left(\theta-\widehat{\theta}\right) + \left(V_\beta - V_\alpha\right)\sin\left(\theta+\widehat{\theta}\right) \\ +\left(V_\alpha - V_\beta\right)\frac{1}{\tau'_{i,ASC}s+1}\sin 2\widehat{\theta} \end{array}\right] \end{aligned} \tag{A.5}$$

which can be further simplified:

$$e = \frac{1}{4}\left[\left(V_\alpha+V_\beta\right)\sin\left(\theta-\widehat{\theta}\right) + \left(V_\beta - V_\alpha\right)\left(\sin\left(\theta+\widehat{\theta}\right) - \frac{1}{\tau'_{i,ASC}s+1}\sin 2\widehat{\theta}\right)\right] \tag{A.6}$$