Article

An Efficient Non-Inverting Buck-Boost Converter with Improved Step Up/Down Ability

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Abstract: In this article, a new non-inverting buck-boost converter with superior characteristics in both bucking and boosting is presented. The proposed converter has some distinct features, such as high step-up/-down ability and low voltage/current stress on its switching devices. The voltage gain of the proposed converter is double the reported value for the traditional buck-boost converter. Although it has three switches, the three switches operate simultaneously, hence no dead-time is required. Two out of the three switches are under voltage stress equal to half of the output voltage. The overall efficiency of the system is promising because of the ability to select devices with low voltage drops. Converter analysis and steady-state performance in both continuous conduction mode (CCM) and discontinuous conduction mode (DCM) are presented in detail. A 1 kW hardware prototype of the converter was implemented in the laboratory; with a step-up ratio of 3.5 and 1 kW power, the measured efficiency is above 95.4%, and with step-up ratio 8, it is around 91.5%.

1. Introduction

Traditional buck-boost converters, CUK and SEPIC, are able to buck or boost input voltage; however, their bucking or boosting abilities are limited, and they have high stress on their switching devices, hence their efficiency and applications are limited [1–6]. In order to improve step-up/-down abilities, a group of power converters have been developed in the literature [7–17]. The topology proposed in [7] is a modification of the traditional buck-boost converter with improved voltage gain, but it has an inverted output and two of the switching devices are under high voltage stress. A high gain with continuous input current buck-boost converter has been proposed in [7,8], but the converter is inverted and includes many storage devices. In [9], a novel buck-boost converter is proposed with lower component stresses and less storage devices, However, the converter has limited voltage gain; high ripple; and the converter switches operate in a complementary manner, which increases dead-time and switching protection issues.

The quadratic voltage gain buck-boost converters developed in [10–12] provide good performance in step-up mode, but their step-down ability is very limited.

In [13,14], semi-quadratic buck-boost converters are proposed. Despite their improved performance in both bucking and boosting modes, there is no common ground and the input current is discontinuous. A quasi-Y source-based buck-boost dc–dc converter is introduced in [15,16]. This converter achieved a very high voltage gain using two inductors. Nevertheless, the severe slope of the voltage gain ratio makes controlling the converter very difficult.

In order to achieve higher voltage and gain and sustain higher efficiency at a wide range of input voltage change, this paper presents a new high-gain non-inverting buck-boost converter. The structure proposed has different merits, such as non-inverting, high voltage gain, reduced components' stresses, and the ability to sustain better efficiency at wide voltage and load ranges.

The rest of the paper is organized as follows: Section 2 discusses the principle of operation and analysis of the proposed converter; Section 3 presents the experimental results of the converter; and finally, Section 4 presents the conclusions.

2. Proposed Buck-Boost Dc–Dc Converter

The configuration of the proposed buck-boost dc–dc converter is illustrated in Figure 1 [17]. The structure is implemented using three power switches (S_1, S_2, S_3), two diodes (D_1, D_o), two inductors (L_1, L_2), and an output capacitor (C_o). The three switches are triggered on and off simultaneously, and the diodes operate as freewheeling diodes. The two inductors charge in parallel and discharge in series.
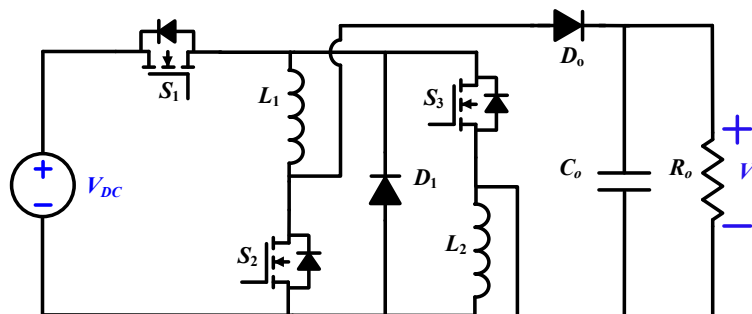

Figure 1. Proposed buck-boost dc–dc converter.

The converter is able to operate in continuous conduction mode (CCM) and discontinuous conduction mode (DCM). Both modes of operation will be considered in the following sections.

2.1. Continuous Conduction Mode

In order to simplify the analysis of the CCM mode, two assumptions are considered in the forthcoming analysis:

✓ Capacitor voltage ripple is very small compared with the voltage itself, thus it could be neglected.

✓ Inductor current ripple is negligible because of its very small value.

✓ All semiconductor devices are ideal.

The converter power switches are triggered ON and OFF simultaneously, hence the converter will have two operating modes; see Figure 2a,b. Typical waveforms of the converter in CCM are shown in Figure 3.

Mode I [0-DT_S]: In this time period, switches (S_1, S_2, S_3) are turned ON, while diodes (D_1, D_o) are turned OFF. This mode is illustrated in Figure 2a. As can be seen from the figure, the two inductors charge in parallel from the source. Applying Kirchhoff voltage law (KVL) and Kirchhoff current law (KCL) to Figure 2a, the following equations are deduced:

$$v_{L1} = v_{L2} = V_{dc} \tag{1}$$

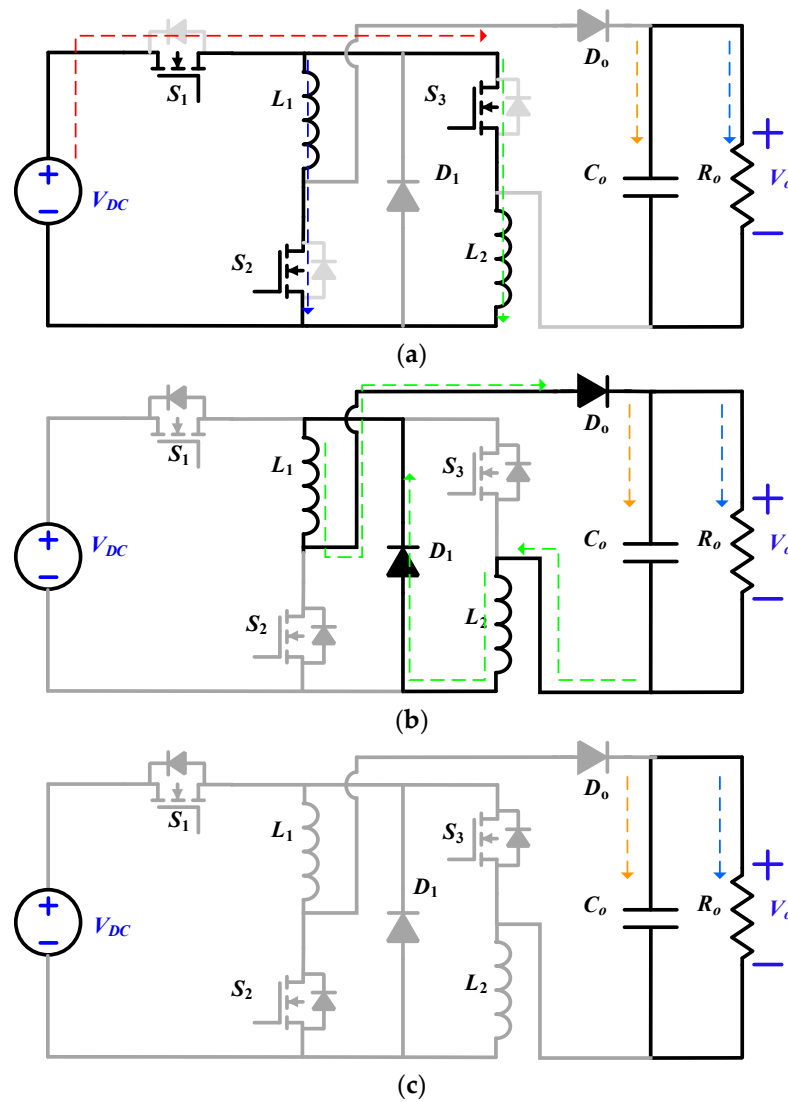$$i_c = -\frac{V_o}{R} \tag{2}$$

$$i_d = 0 \tag{3}$$

Figure 2. Operation modes of the proposed converter: (**a**) operation mode #1, (**b**) operation mode #2, and (**c**) operation mode #3.

Mode II $[DT_S\text{-}T_S]$: In this time period, switches (S_1, S_2, S_3) are turned OFF and, consequently, diodes (D_1, D_o) are turned ON to provide a freewheeling path for the current. This mode is illustrated in Figure 2b. As can be investigated from the figure, the two inductors discharge their energies to the load in series. Applying Kirchhoff voltage law (KVL) and Kirchhoff current law (KCL) to Figure 2b, the following equations are deduced:

$$v_L = v_{L1} = v_{L2} \tag{4}$$

$$2v_L = -V_o \tag{5}$$

$$i_C = I_L - \frac{V_o}{R} \tag{6}$$

$$i_d = I_L \tag{7}$$

The steady-state voltage gain of the proposed converter could be deduced from the analysis of the two modes of operation by applying voltage second balance, and the voltage gain of the proposed converter is as follows:

$$\frac{V_o}{V_{dc}} = M = \frac{2D}{(1-D)} \tag{8}$$

where v_{L1}, v_{L2}, V_{dc}, V_o, I_L, i_C, i_d, M, and D are inductor L_1 voltage, inductor L_2 voltage, input voltage, output voltage, inductor current, capacitor current, diode current, voltage gain, and duty cycle, respectively.
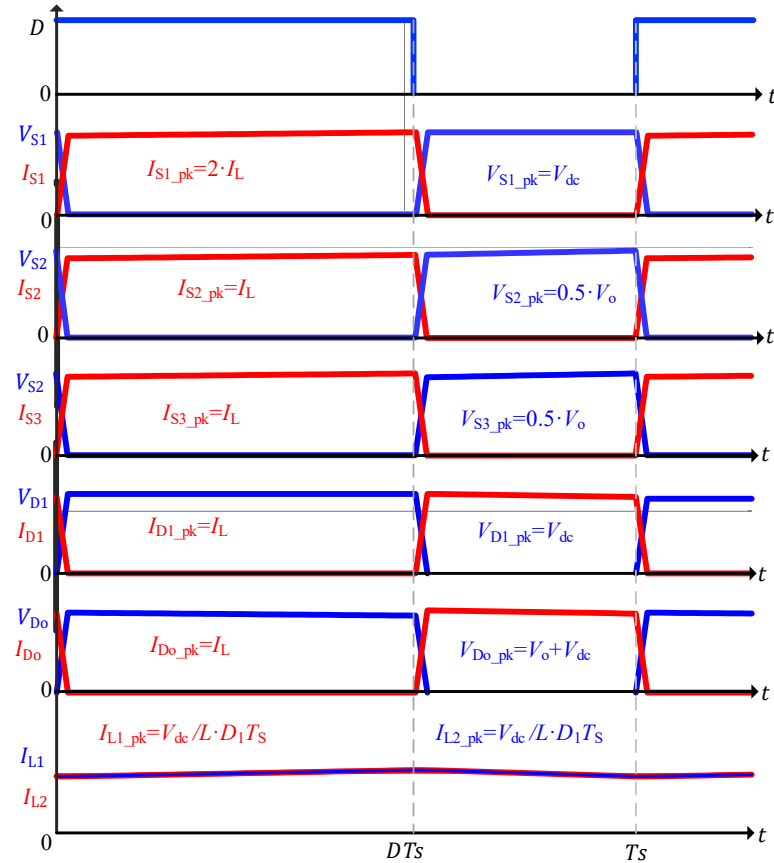

Figure 3. Typical converter waveforms in CCM.

2.2. Discontinuous Conduction Mode

The discontinuous conduction mode typically occurs with large inductor current ripple in a converter operating at light load and containing current unidirectional switches. However, some converters are purposely designed to operate in DCM. The proposed converter will have three modes of operation while operating in DCM; see Figure 2a–c. The typical converter waveform while operating in DCM is illustrated in Figure 4.

Mode I and Mode II, which were discussed in the previous section, are similar to CCM analysis.

Mode III: In this interval, both the power switches and diodes are turned off. The inductors' currents are zero, as illustrated in Figure 2c.

$$v_L = 0 \tag{9}$$

$$i_C = \frac{V_o}{R} \tag{10}$$

$$i_d = 0 \tag{11}$$

Applying inductor volt-second balance in Equations (1), (5), and (9), the relation between input and output voltage is obtained:

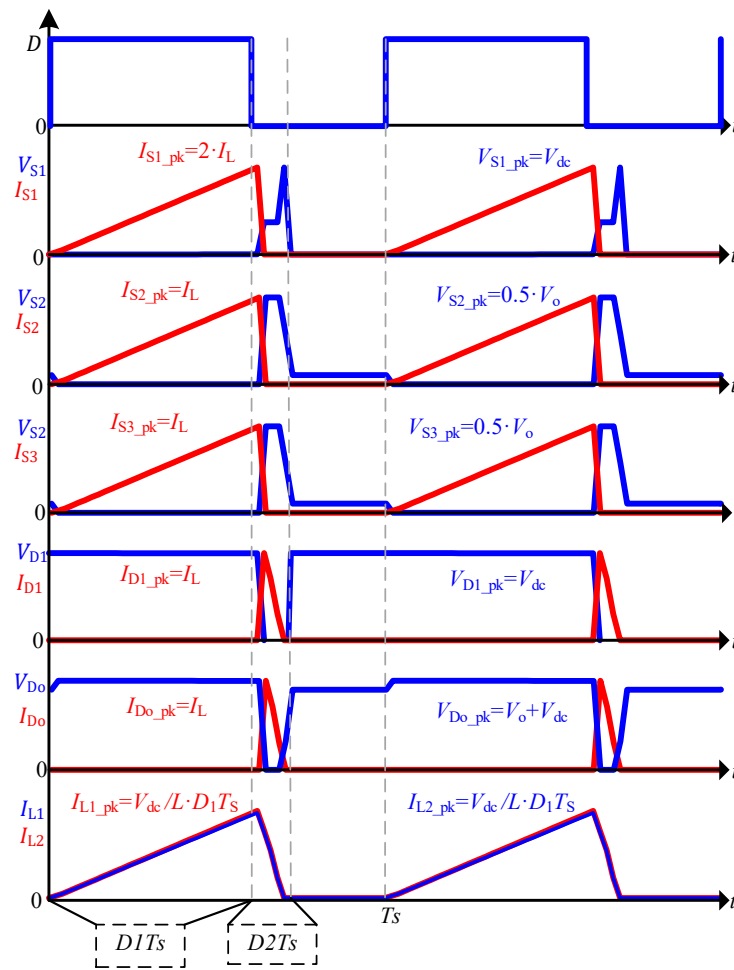$$D_1 * v_{dc} = D_2 * v_o \tag{12}$$

Figure 4. Typical converter waveforms in DCM.

The duty cycle D_2 is an unknown, so a second equation is needed to eliminate D_2. Capacitor charge-balance is used to obtain the second equation. The average of the diode current is equal to the output current:

$$\langle i_d \rangle = \frac{V_o}{R} \tag{13}$$

A sketch of the inductor and diode currents in DCM is illustrated in Figure 5a,b. The dc component of the diode current is given by

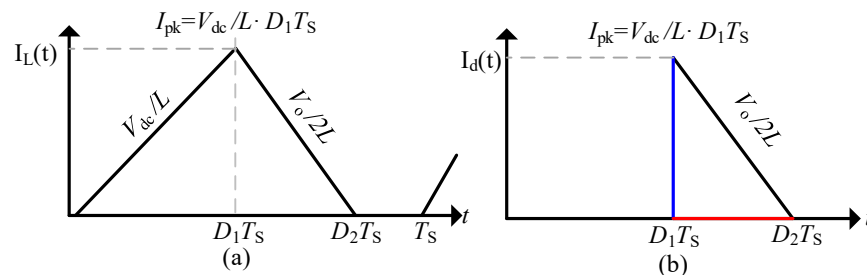$$\langle i_d \rangle = \frac{1}{T_S} \int_0^{T_S} i_d(t)\,dt \tag{14}$$

Figure 5. DCM operation (**a**) inductor current and (**b**) diode current.

The peak diode current could be obtained from the graph as

$$i_{pk} = \frac{V_o}{2L} * D_1 * T_S \tag{15}$$

Solving Equations (13)–(15), the second required equation is obtained as

$$\langle i_d \rangle = \frac{1}{2} * D_2 * T_S * \frac{V_o}{2L} * D_1 = \frac{V_o}{R} \tag{16}$$

Let

$$k = \frac{2L}{RT_S} \tag{17}$$

Then

$$D_2 = 2 * k / D_1 \tag{18}$$

Finally, the converter voltage gain in DCM operation is given as

$$\frac{V_o}{V_{dc}} = M = \frac{D_1^2}{(2 * K)} \tag{19}$$

where D_1, D_2, T_S, and R_0 are periods when the switches are conducting, periods when the diode is conducting, switching time, and load resistance, respectively.

The boundary for CCM and DC operation can be obtained by relating inductor current and inductor ripple

$$I_L > \Delta i_L \text{ For CCM} \tag{20}$$

$$I_L < \Delta i_L \text{ For DCM} \tag{21}$$

Substituting CCM solutions for I_L and Δi_L in (20)

$$\frac{V_{dc}}{R} * \left(\frac{2D}{1-D}\right)^2 > \frac{V_{dc}}{2L} * D T_S \tag{22}$$

Equation (22) could be rearranged to

$$\frac{2L}{RT_S} = K > D * \left(\frac{2D}{1-D}\right)^2 \tag{23}$$

Hence

$$K_{cri} = D * \left(\frac{2D}{1-D}\right)^2 \tag{24}$$

where K_{cri} is the critical boundary between CCM and DCM.

According to the above analysis, the converter can operate on CCM or DCM based on the operating conditions; in order to avoid such conditions, accurate design of the converter must be considered. Figure 6 represents the boundary condition between CCM and DCM at different duty cycles and different power while the output voltage is fixed at 350 V.

2.3. Switches' and Diodes' Voltage Stresses

Voltage and current stress are important parameters in designing and selecting circuit parameters, and the proposed converter switching elements' stress is discussed below.

Switches S_1, S_2, and S_3 are triggered in a simultaneous manner, but their ratings are different. The voltage stress of switch S_1 is equal to
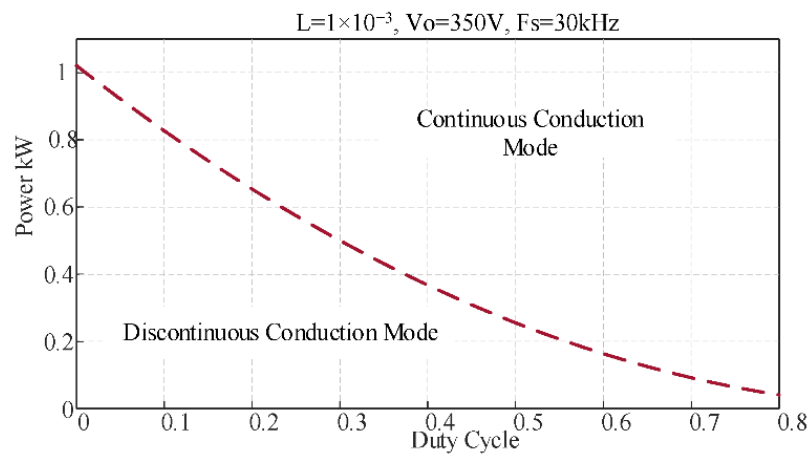
$$V_{dsS1} = V_{dc} \tag{25}$$

Figure 6. CCM and DC boundary.

The current stress of switch S_1 is given by

$$I_{S1} = 2 * I_L \tag{26}$$

Switches S_2 and S_3 face similar voltage and current stress, as follows:

$$V_{dsS2} = V_{dsS3} = \frac{V_o}{2} \tag{27}$$

$$I_{S2} = I_{S3} = I_L \tag{28}$$

Diodes D_1 and D_o work as freewheeling diodes and are activated in complementary manners to the switches. The voltage and current stress of both diodes are given by

$$V_{d1} = V_{dc} \tag{29}$$

$$I_{d1} = I_L \tag{30}$$

$$V_{do} = V_{dc} + V_o \tag{31}$$

$$I_{S2} = I_L \tag{32}$$

A depiction of the devices' normalized voltage stresses with different voltage gain is illustrated in Figure 7. In Figure 7, the voltage stress is normalized to the input voltage.
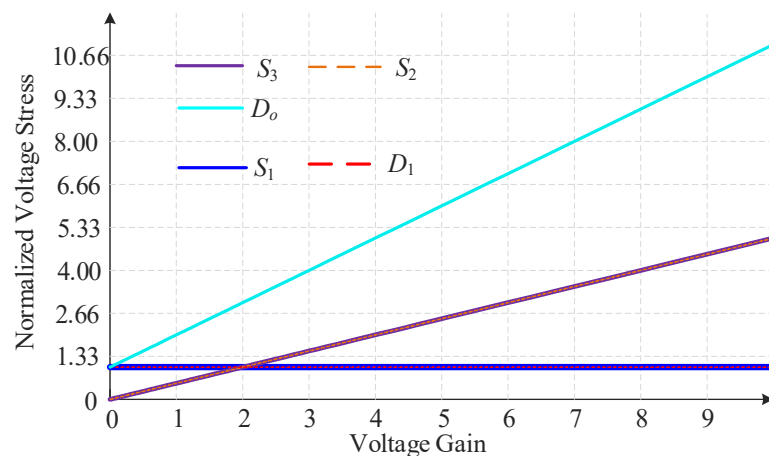

Figure 7. Circuit component voltage stress normalized to input voltage vs. converter voltage gain.

2.4. Components' Design

The design of the circuit parameters, inductors, and capacitor is obtained from the steady-state analysis performed in the previous sections. Utilizing inductor volt-second balance and capacitor charge, the designs of parameters are as follows:

2.4.1. Inductors' Design

Inductors' selection is based on the required ripple of its current. The inductor current ripple in CCM is drawn in Figure 8a and is given by

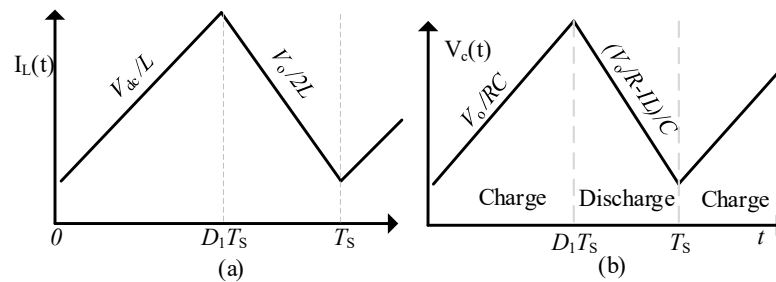$$\Delta i_L = \Delta i_L^{on} = \Delta i_L^{off} = \frac{V_{dc} D T_S}{L} = \frac{V_o(1-D)T_S}{2L} \tag{33}$$

Figure 8. CCM operation (**a**) inductor current and (**b**) output capacitor voltage.

This equation is valid in both CCM and DCM. By defining the required amount of ripple, the inductor value could be defined as follows:

$$L = \frac{(V_o * (1-D)) * T_S}{(2 * \Delta i_L)} \tag{34}$$

Based on Equation (29), there is a dependency between inductance L and duty cycle D. In order to avoid any misoperation of the converter, we design the inductance based on the extreme condition that the current ripple at the extreme scenario does not exceed the required ripple and when duty cycle below the ripple will be below the required level.

Let us assume the required ripple Δi_L is 10%, then we can calculate L at the duty cycle around 0.82. Then, when the duty cycle is lower than 0.85, the ripple will be less than 10%.

2.4.2. Capacitors' Design

The output capacitor value is selected based on the amount of voltage ripple acceptable in the output voltage. The output capacitor voltage waveform is illustrated in Figure 8b and the ripple equation is as follows:

$$\Delta v = \Delta v_c^{on} = \Delta v_o^{off} = \frac{(V_o - IL)(1-D)T_S}{RC} = \frac{V_o D T_S}{RC} \tag{35}$$

This equation is valid in both CCM and DCM. By defining the required amount of ripple, the capacitor value could be defined as follows:

$$C_o = \frac{(V_o * D * T_S)}{(\Delta v * R)} \tag{36}$$

where Δi_L, Δi_L^{on}, Δi_L^{off}, L, Δv, Δv_c^{on}, Δv_o^{off}, and C are inductor current ripple, inductor ripple while the inductor is charging, inductor ripple while the inductor is discharging, inductor value, capacitor ripple, capacitor ripple while the capacitor is charging, capacitor ripple while the capacitor is discharging, and capacitor value, respectively.

Based on Equation (30), there is a dependency between capacitance C and duty cycle D. In order to avoid any misoperation of the converter, we design the capacitance based on

the extreme condition that the voltage ripple at the extreme scenario does not exceed the required ripple and when duty cycle below the ripple will be below the required level

Let us assume the required ripple Δv is 10%, then we can calculate C at the duty cycle around 0.82. Then, when the duty cycle is lower than 0.85, the ripple will be less than 10%.

2.4.3. Comparative Study

Converter performance mainly depends on the input voltage, input power, and step-up ratio. The converter voltage gain is affected by the loading profile and supply voltage. In Figure 9a, the input voltage is fixed at 150 V, while different loading profiles are applied; at light load, the converter conversion ability is higher than at heavy loading. The second case study is illustrated in Figure 9b, where load profile is fixed with different supply voltages; as the supply voltage increases, the step-up/-down ability increases.
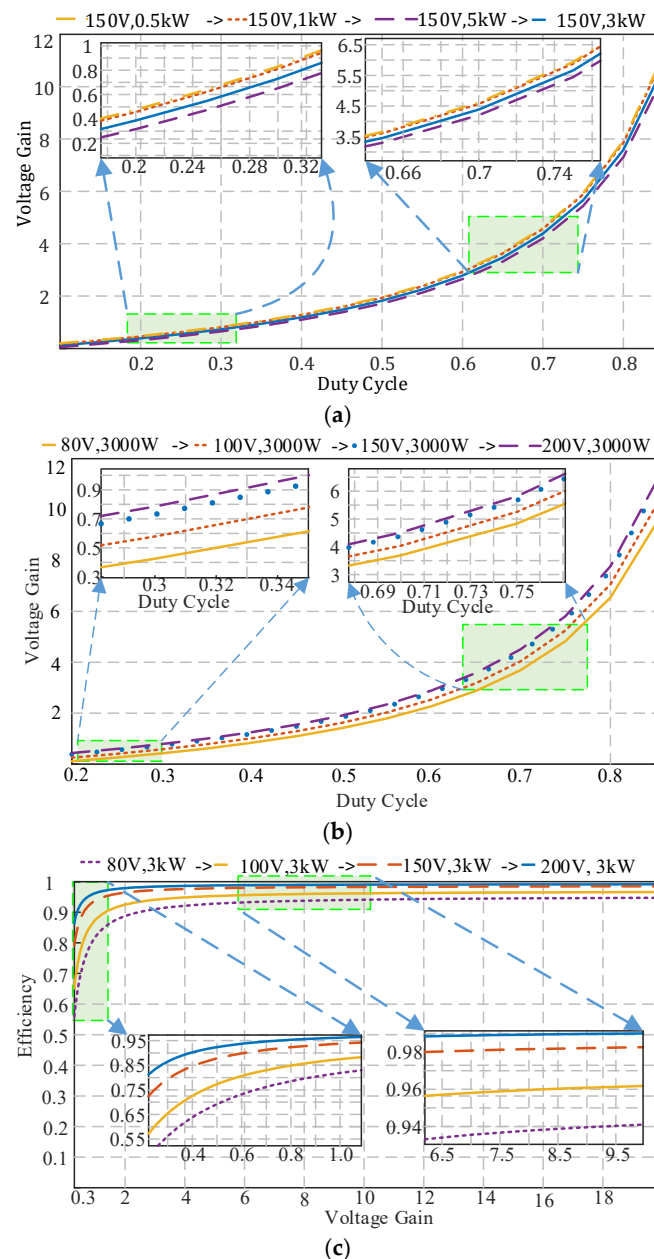

Figure 9. Different cases of study for the proposed converter: (**a**) Voltage gain at different duty cycle and different loading. (**b**) Voltage gain with fixed loading and different input voltages. (**c**) Converter efficiency at different input voltages.

However, in both case studies, the differences in the voltage gain do not have a very high ratio.

Converter efficiency depends on many factors such as the load profile, source voltage, and voltage gain. In the scenario illustrated in Figure 9c, the load profile is fixed while both voltage gain and source voltage are variable. In buck mode, as the source voltage increases and the bucking ratio is lowered, the converter demonstrates the highest efficiency, while with lower input voltage and a higher bucking ratio, the converter efficiency is low. During boosting mode, as source voltage increases, efficiency increases too.

Another case study is considered in Figure 10a, where input voltage is set to 150 V, while load profile is variable and efficiency is measured at different voltage gains. With heavy loading, the converter demonstrates lower efficiency than with a medium or moderate loading profile. A comparison between the proposed converter and different converters reported in the literature is illustrated in Table 1. In the voltage gain comparison illustrated in Figure 10b, both the proposed converter and switched inductor buck-boost converter have similar step-up/-down ability, but the proposed converter has higher efficiency; see Figure 10c.

**Table 1.** Voltage gain and component stress comparison.

| Converter Topology	Gain $M = V_o/V_{in}$	Components' Count				Switches' and Diodes' Voltage Stress	Switches' and Diodes' Current Stress
		Switch	Diode	L	C		
Buck-Boost [18]	$(D/(1-D))$	1	1	1	1	$S:V_o$ $D:(V_o+V_{in})$	I_L I_L
Non-Inverting [19]	$(D/(1-D))$	2	2	1	1	$S_1:V_{in}$ $S_2:V_o$ $D_1:V_{in}$ $D_o:V_o$	I_L I_L I_L I_L
Cuk [5]	$(D/(1-D))$	1	2	2	1	$S_1:V_{in}/(1-D)$ $D_1:V_{in}$ $D_o:V_o$	I_L I_L I_L
SEPIC [19]	$(D/(1-D))$	1	1	2	2	$S_1:V_o+V_{in}$ $D_1:V_o+V_{in}$	$2I_L$ I_L
SIBBC [20]	$2D/(1-D)$	1	4	2	1	$S_1:V_o+V_{in}$ $D_1:V_{in}$ $D_2:V_o/2$ $D_3:V_o/2$ $D_o:V_o+V_{in}$	$2I_L$ I_L I_L I_L I_L
Lakshmi [21]	$(1+D1)/(1-D_1-D_2)$	3	2	2	1	$S_1:(V_o+V_{in})/2$ $S_2:(V_o+V_{in})/2$ $S_3:V_o$ $D_1:V_o$ $D_o:V_o+V_{in}$	I_L I_L I_L I_L I_L
[22]	$2D/(1-D)^2$	2	3	2	3	$S_1:1/(1-D)*V_{in}$ $S_2:V_{in}*(1+D)/(1-D)^2$ $D_1:V_{in}/(1-D)$ $D_2:V_{in}/(1-D)$ $D_o:V_o+V_{in}/(1-D)$	I_L I_L I_L I_L I_L
[23]	$D^2/(1-D)^2$	2	2	2	2	$S_1:1/(1-D)*V_{in}$ $S_2:V_{in}*D/(1-D)^2$ $D_1:V_{in}/(1-D)$ $D_2:V_{in}*D/(1-D)^2$	$2I_L$ I_L I_L I_L

Table 1. *Cont.*

Converter Topology	Gain $M = V_o/Vin$	Components' Count				Switches' and Diodes' Voltage Stress	Switches' and Diodes' Current Stress
		Switch	Diode	L	C		
Proposed	$2D/(1-D)$	3	2	2	1	$S_1:V_{in}$ $S_2:V_o/2$ $S_3:V_o/2$ $D_1:V_{in}$ $D_o:V_o+V_{in}$	$2I_L$ I_L I_L I_L I_L
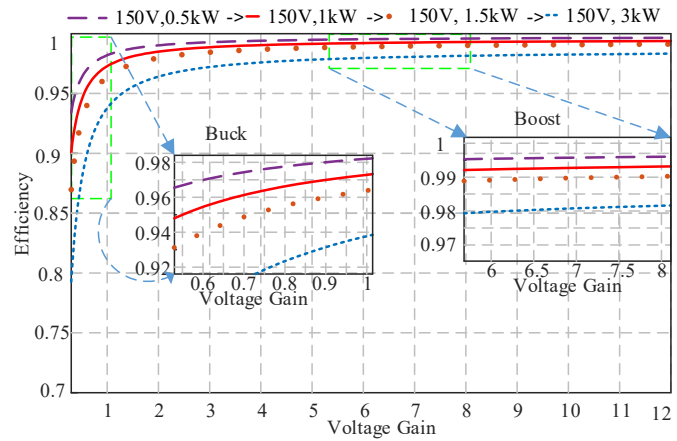
(a)
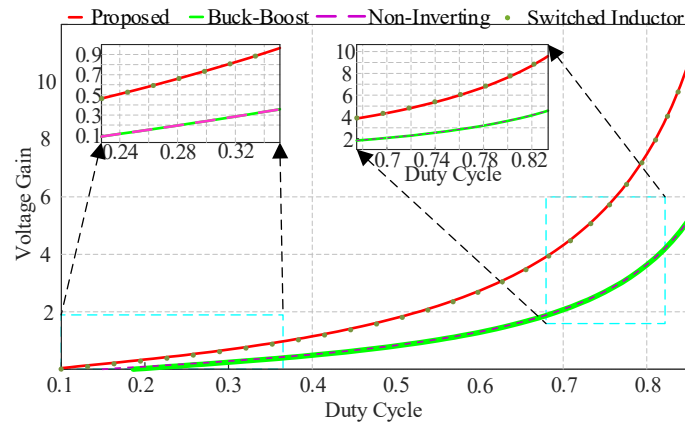
(b)
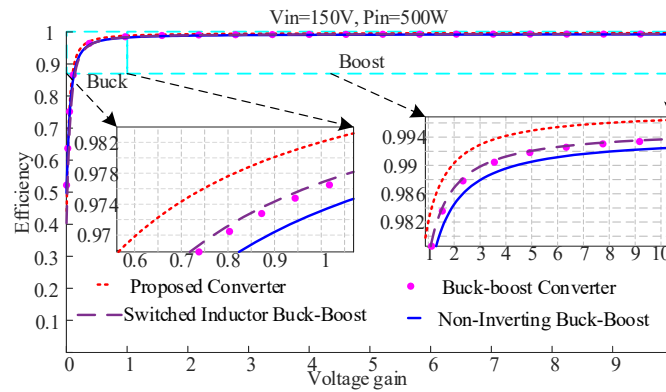
(c)

Figure 10. (**a**) Converter efficiency at fixed input voltage and different loading, (**b**) voltage gain comparison among the proposed and other buck-boost converters, and (**c**) efficiency comparison among the proposed and other buck-boost converters.

3. Experimental Verification

This section provides the experimental results of the developed system, and the parameters used to build the prototype are illustrated in Table 2. A photo of the proposed system is shown in Figure 11.

Table 2. Hardware prototype specifications.

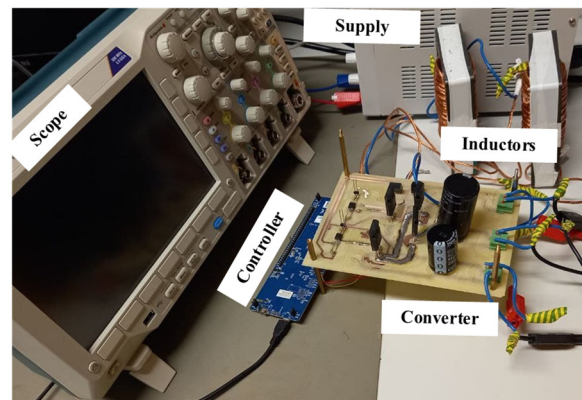| Parameter	Value
Input voltage range [*V*]	33–150
P [*W*]	700 W
F_s Switching Frequency	30 kHz
Switches S_1, S_2, S_3	IMZ120R030M1HXKSA1
Diodes D_1, D_o	DPG10I300PA
Inductors $L_1 = L_2$	1 mH
Capacitor C_o	320 μF

Figure 11. Experimental set-up schematic.

A case study where the duty cycle is set to 0.6 with 30 V input voltage is illustrated in Figure 12. Three switches are operating in synchronous manner, hence the gate source pulses for the three switches are the same as illustrated in Figure 12a. Diodes D_1 and D_o are operating as freewheeling diodes. The cathode–anode voltages of the two diodes are illustrated in Figure 12b. The input current is the sum of the two inductors' currents when the switches are on and zero when the switches are off, and the input capacitor smoothens the input current. The drain source voltages of the three switches are illustrated in Figure 12c. Switches S2 and S3 face the same voltage stress and carry the same current.

Figure 12d illustrates switch S_1 current, which is equal to the sum of the two inductors' currents. Switch S_2 current is illustrated in Figure 12e, which is equal to the inductor current. The output diode current is illustrated in Figure 12f, where spikes are noted in the switches and diode currents because of a problem in the used probe; however, it does not exist in real current as there are no spikes in the measured voltages.

A boosting case study is considered in Figure 13, where the input voltage is 25 V and the output voltage generated is around 38 V, and a bucking case study is illustrated in Figure 14, where the input voltage is 23 V, output voltage is 9.25 V, duty cycle is 0.2244, and voltage gain is 0.4.
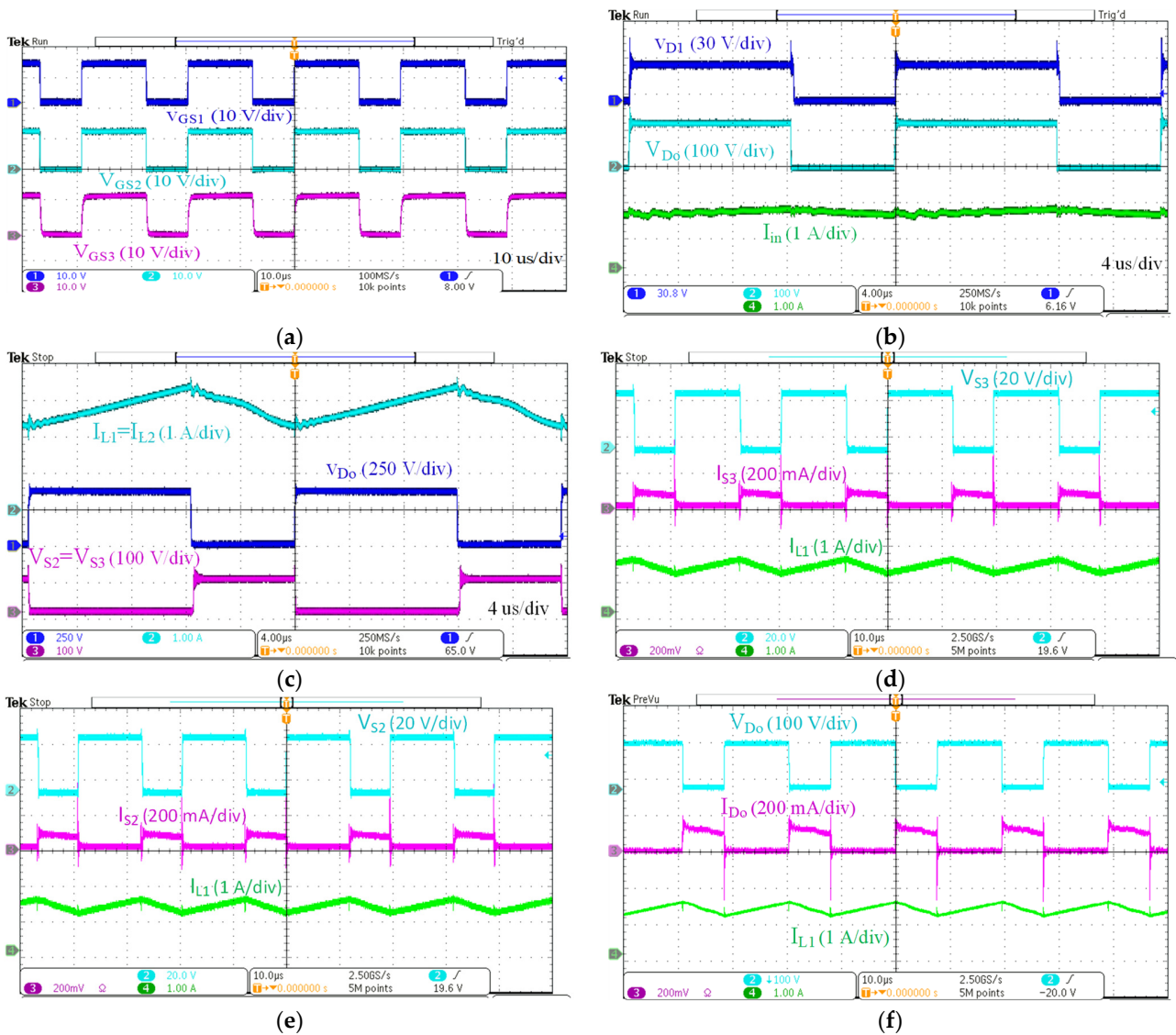
Figure 12. Experimental results of converter at duty cycle of 0.6 and input voltage of 30 V: (**a**) gate source pulses; (**b**) Ch1 diode D_1 voltage, diode D_o voltage, and input current; (**c**) Ch1 output diode D_o voltage, Ch3 switches' S_2 and S_3 voltage, and Ch2 inductor L_1 current; (**d**) Ch1 switch S_3 voltage; Ch2 switch S_3 currents; (**e**) Ch2 switch S_2 voltage, Ch3 switch S_2 current, and inductor current; and (**f**) Ch2 diode D_o voltage and diode D_o current.
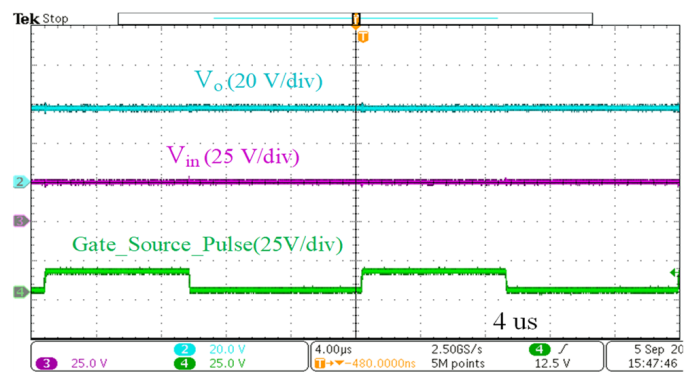

Figure 13. Boosting case study, where the input voltage is 25 V, output voltage is 38 V, duty cycle is 0.428, and voltage gain is 1.52.
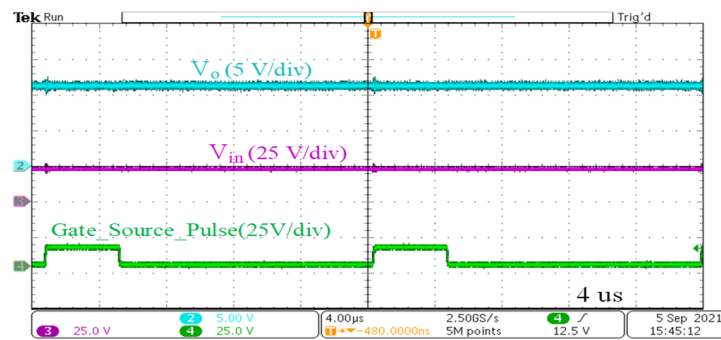
Figure 14. Bucking case study, where the input voltage is 23 V, output voltage is 9.25 V, duty cycle is 0.2244, and voltage gain is 0.4.

The converter voltage gain was measured experimentally, and the theoretical and measured voltage gains of the converter with varying duty cycles are illustrated in Figure 15. For comparison purposes, three prototypes were built in the laboratory for the traditional buck-boost, non-inverting buck-boost, and proposed converter. The three prototypes were built using the same parameters as in Table 2. In the first case study, which is illustrated in Figure 16, the input voltage is set to 100 V and the step ratio is fixed at 3.7. For such a step-up ratio, the proposed converter requires a duty cycle of 0.68, while the conventional and non-inverting buck-boost converters both require a duty cycle of 0.8.
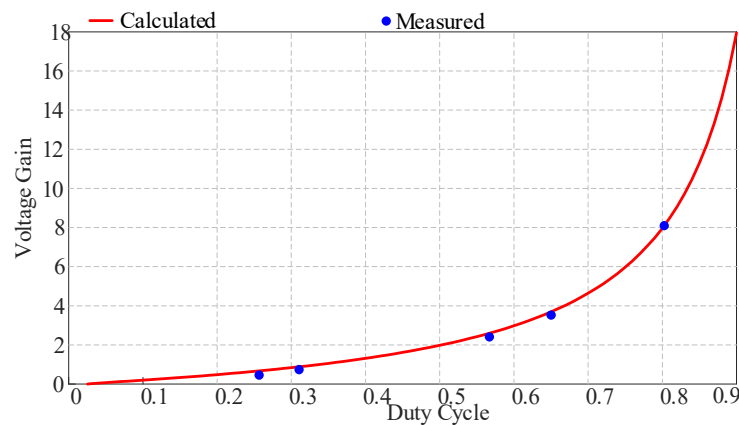

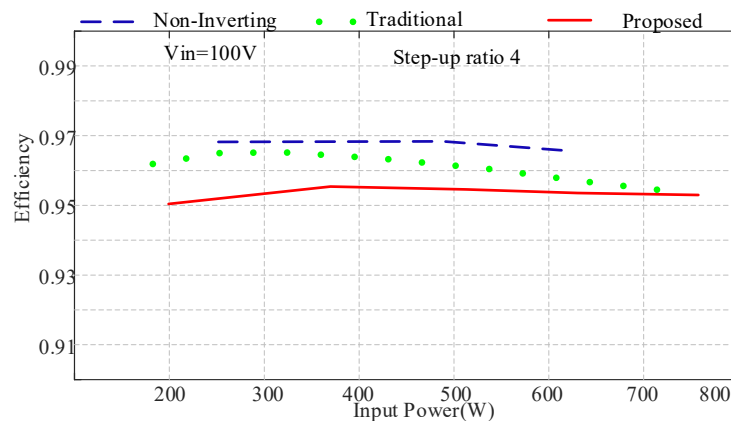**Figure 15.** Calculated and measured converter voltage gain vs. duty cycle.

Figure 16. Measured efficiency comparison between the proposed converter, non-inverting buck-boost, and traditional buck-boost converter at a step-up ratio of 3.7.

In this case study, the non-inverting converter demonstrates the highest efficiency, while at high power, both the proposed and conventional converter have the same efficiency. In the second case study, which is illustrated in Figure 17, the input voltage is fixed at 30 V and the step-up ratio is 8. The efficiency of the proposed converter and the non-inverting converter is comparable, but with the increase in power (over 300 W), the proposed converter demonstrates the highest efficiency.
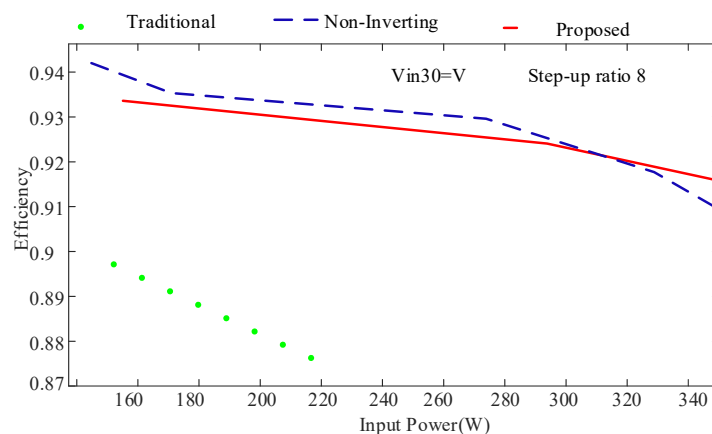

Figure 17. Measured efficiency comparison between the proposed, non-inverting, and traditional buck-boost converter at a step-up ratio of 8.

The last case study demonstrates step-down comparison. In Figure 18, the input voltage is fixed at 150 V and the step-down ratio is 3. The non-inverting converter demonstrates the lowest efficiency. The proposed converter and the conventional converter demonstrate comparable efficiency at low power, but with the increase in input power, the proposed converter demonstrates the highest efficiency.
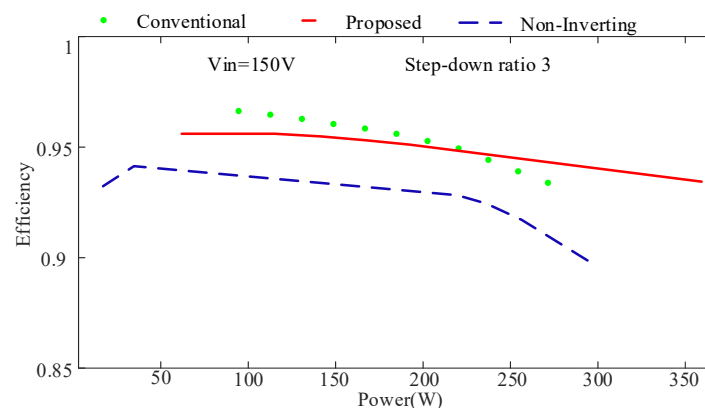

Figure 18. Measured efficiency comparison between the proposed, non-inverting buck-boost, and traditional buck-boost converter at a step-down ratio of 3.

4. Conclusions

In this paper, a new non-inverting high-gain buck-boost structure is developed with improved step-up/-down ability. The performance of the converter in both CCM and DCM is studied and analyzed. The design of the converter elements is investigated and described. The operating conditions and voltage/current stress of each device are studied. Based on the performed analysis, the proposed converter devices are under low voltage and current stress compared with other buck-boost converters. A 700 W prototype was built for the converter to investigate its performance experimentally. The efficiency of the proposed converter is measured at different voltage gains and compared with the traditional buck-boost converter.

The theoretical and measured voltage gain matched. While working in step-up, the converter demonstrated better performance at high power. The peak measured efficiency of the converter at a step-up ratio of 3.7 was 95.4%.

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