A Carrier-Based Discontinuous PWM for Single and Parallel Three-Level T-type Converters with Neutral-Point Potential Balancing

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***Abstract*—The three level converters have an inherent problem of the neutral point (NP) voltage unbalance due to the split dc-link capacitors. This NP voltage unbalance degrades the output voltage/current waveform quality. A carrier based discontinuous pulse width modulation (CB-DPWM) with NP voltage balancing strategy- that involves the injection of calculated zero-sequence voltages to the original modulation signal - is implemented for the three level T-type converter in this paper. The zero-sequence voltages are determined from the space vector synthesis of the converter output voltages. This method allows the determination of the zero-sequence voltages with few judgment conditions. Unlike the space vector based discontinuous pulse width modulation (SVB-DPWM), the CB-DPWM is easier to realize in practical applications. Moreover, the proposed CB-DPWM can also be directly used in parallel systems, which can suppress NP voltage ripples and circulating currents simultaneously by a coordinated strategy. The efficacy of the proposed method in balancing the neutral point voltage in single and parallel systems is demonstrated by simulations and experiments.**

Keywords—Carrier-based discontinuous PWM, circulating currents, neutral-point voltage balance, three-level T-type converter, zero-sequence voltage

I. INTRODUCTION

Due to their improved technical features, three-level T-type converters are widely used in various applications: photovoltaic generation system [1], wind turbine system [2], ac motor drives etc. Compared with the traditional two-level converter topology, the three-level T-type converter shows great improvements in terms of lower harmonic distortion, higher efficiency and power capability [3]-[5]. However, this topology suffers from the unwanted effect of dc-link capacitor voltage unbalancing due to the flow of non-zero average neutral current caused mainly by non-ideal components and the nature of the controlling modulation technique [6]. The neutral-point voltage variation problem may cause higher distortion of output waveforms and requires the oversizing of the dc-link capacitors and switching devices to withstand this additional voltage stress [7]-[8].

In order to realize the proper operation of the three-level converters and overcome the neutral-point (NP) voltage unbalanced problem, many modulation strategies such as carrier based PWM (CB-PWM) and space-vector-based PWM (SVB-PWM) methods which have been widely used in industry applications [9]-[12]. For example, a space-vector current control is investigated in [9] to use circular hysteresis areas and to perform the balancing of the dc bus voltages. A theoretical optimum algorithm employing interpolation method to calculate the appropriate zero-sequence voltage of CB-PWM was introduced in [10]. Most of these methods can solve the problem of NP voltage variation, but at the same time there will be high switching losses, which is not conductive to medium/high-voltage applications.

For the purpose of reducing switching losses, many discontinuous PWM (DPWM) schemes have been studied for different applications, and some of them have coped with NP voltage variation problem in three-level converters [13-16]. In [13], the generalized DPWM scheme for two-level converters was discussed. The author showed, that for the two-level converters, all available DPWM schemes can be obtained by the choice of a parameter. For three-level converters, the NP voltage balancing in space vector-based DPWM (SVB-DPWM) is performed without affecting converter efficiency in [14]. However, the SVB-DPWM methods are difficult to implement in practical applications, especially in cases under performance optimized situations because they are based on space vector and requires sector judgment, switching time calculation and pulse pattern generation. Actually, the SVB-DPWM is functionally equivalent to sine-triangle CB-DPWM, which is easier to be achieved in practical applications. Although [15], and [16] adopt CB-DPWM, the procedures to calculate zero sequence voltage are divided into many situations and only results for unity power factor load condition are shown in [15]. Besides, there are too many judgment conditions to obtain injected zero-sequence voltage in [16].

Seeking to address the challenges indicated above, this paper proposes a CB-DPWM for three-level T-type converters. Using the functional equivalence of the SVB-PWM and the CB-PWM, the generalized zero sequence voltages are determined. Then the CB-DPWM can be obtained by the choice of a parameter. The scheme provides few generalized expressions for the zero-sequence voltages which are easier to implement and they give sufficiently good voltage balancing due to their analytical forms. Only the difference in the capacitor dc voltages is required for the neutral-point control implementation.

With the increased penetration of renewable energy in the grid, the parallel operation of converters is a well-known method to achieve higher power level. Therefore, it is also very important to extend the proposed method to parallel systems. However, zero-sequence circulating currents (ZSCCs) will be generated due to the differences of the parallel system in modulation signals and parameters in practical applications [17]-[18]. It is worth noting that NP potential is also affected by the ZSCCs, which leads to many methods that control neutral

current to suppress the NP voltage variation cannot be used in parallel systems, such as [10], [16] and [19]. Fortunately, the proposed CB-DPWM is based on judging the difference in the capacitor dc voltages to control the NP voltage balance, so it is not affected by the circulating currents of parallel systems. In this case, a coordinated strategy based on proposed CB-DPWM is also presented to tackle the problems of NP voltage unbalance and ZSCCs in parallel systems.

The ideas in this paper has been presented at the 2019 Energy Conversion Congress and Expo (ECCE) [20], [21]. In its current version, a detailed derivation of the modulation scheme has been laid out including a new section that discusses factors calculation of proposed methods. In addition, The proposed method is extended to parallel systems and a detailed analysis of the results is carried out. This paper is organized as: following the introduction, the operation principle of three-level T-type converter is introduced in Section II. Then the injected zero-sequence voltages of proposed CB-DPWM are calculated, and simulation results are shown in Section III. Based on the proposed CB-DPWM, a coordinated strategy is introduced to suppress the NP variations and ZSCCs of parallel systems in Section IV. The experimental results from a laboratory prototype are shown in Section V. Conclusions are finally presented in Sections VI by highlighting the advantages of the proposed CB-DPWM scheme.

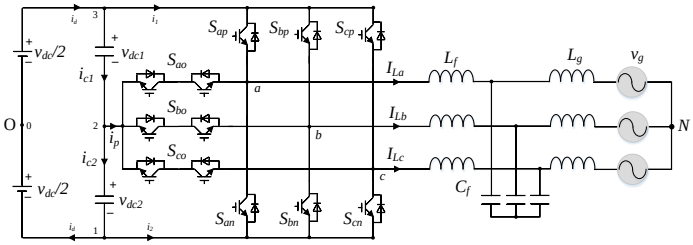


Fig. 1. Topology of a three-level T-type converter.

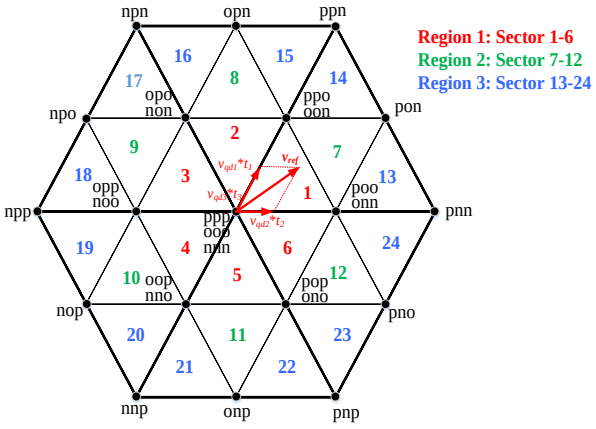


Fig. 2. Three-level space-vector diagram.

II. Operation Principle

A typical power stage of the three-level T-type converter is presented in Fig.1. The switching functions of the top devices are defined as $S_{ip}(i = a, b, c)$, that of the middle two devices as S_{io} and for the bottom devices they are S_{in}. Suppose that $C_{dc1} = C_{dc2} = C$ and v_{dc} denotes the dc voltage. Currents i_{La}, i_{Lb}, i_{Lc} denote the three phase output currents, respectively. The output phase voltage (v_{iN}) are given by (1).

$$v_{iN} = S_{ip} * v_{30} + S_{io} * v_{20} + S_{in} * v_{10} - v_{NO} \tag{1}$$

In order to satisfy the requirement of KCL, in orther words for the sum of currents at nodes a, b annd c to be zero, the equation (2) should be satisfied:

$$(S_{ip} + S_{io} + S_{in}) = 1 \tag{2}$$

Substituting (2) into (1) yields the following equation:

$$v_{iN} + v_{NO} = S_{ip} * \frac{v_{dc}}{2} - S_{in} * \frac{v_{dc}}{2} + (1 - S_{ip} - S_{in}) v_{20} \tag{3}$$

where $v_{20} = (v_{dc2} - v_{dc1})/2$, which is also the NP potential voltage. v_{NO} is the voltage between the neutral of the star connected load and the neutral-point of the input dc source, which is referred to as the zero-sequence voltage v_z. From equation (3), it is worth noting that appropriate zero-sequence voltage has the direct relationship with the NP potential voltage.

Given that the middle switch S_{io} has been expressed as a function of the top and bottom switches (S_{ip}, S_{in}) for each leg, there are six independent switching devices and hence 64 switching states for the converter of Fig. 1. There is however, a further constrain on the converter of Fig. 1. In order to avoid dc voltage short circuit, in other words to satisfy the requirement of KVL, any state in which both S_{ip}, S_{in} are turned on simultaneously is not valid. In a three-phase three-level T-type converter, there are therefore 27 feasible switching states comprising of 24 active and 3 null states. The feasible states are shown in the stationary reference frame in Fig. 2 with 24 sectors. Moreover, the sectors can be divided into three regions according to the composition of different types of vectors in that sector. In Fig. 2, (p) stands for the ON state of the top switching devices in a leg of the converter, (o) means the middle devices of the converter leg are ON while (n) means the bottom devices of the converter legs are ON. For instance (pno) means the top switching device on the phase-a leg, the bottom switching device on the phase-b leg and the middle switching device on the phase-c leg are all turned ON.

In general, the three-phase voltages, expressed in the stationary reference frame, situated in an appropriate sector (taking sector 1 as example shown in Figure 3), are approximated by the time-average over a sampling period of the three nearest voltage vectors of the triangle sector. If the three nearest vectors v_{qd1}, v_{qd2} and v_{qd3} are called into play for times t_1, t_2 and t_3 respectively, then the reference voltage $v^*_{\alpha\beta}$ can be written as:

$$v^*_{\alpha\beta} = v_\alpha + jv_\beta = v_{qd1}t_1 + v_{qd2}t_2 + v_{qd3}t_3 \tag{4}$$

and the devices have to switch according to the following constraint:

$$t_1 + t_2 + t_3 = 1 \tag{5}$$

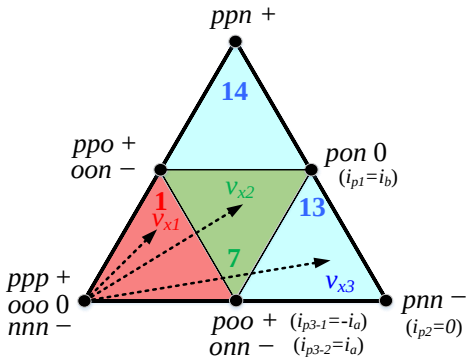


Fig. 3. Sectors 1, 7 and 13 of the space vector diagram.

Substituting formula (5) into (4) separating the real and imaginary terms:

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \begin{bmatrix} v_{q1} - v_{q3} \\ v_{d1} - v_{d3} \end{bmatrix} t_1 + \begin{bmatrix} v_{q2} - v_{q3} \\ v_{d2} - v_{d3} \end{bmatrix} t_2 \tag{6}$$

By solving the above matrix for t_1 and t_2:

$$\begin{cases} t_1 = \dfrac{v_{q2}v_\beta - v_{q2}v_{d3} - v_{q3}v_\beta + v_{d2}v_{q3} - v_\alpha v_{d2} + v_\alpha v_{d3}}{v_{d1}v_{q2} - v_{d1}v_{q3} - v_{d3}v_{q2} - v_{d2}v_{q1} + v_{d2}v_{q3} + v_{d3}v_{q1}} \\ t_2 = \dfrac{v_{d1}v_\alpha - v_{d1}v_{q3} - v_{d3}v_\alpha + v_{d3}v_{q1} - v_\beta v_{q1} + v_\beta v_{q3}}{v_{d1}v_{q2} - v_{d1}v_{q3} - v_{d3}v_{q2} - v_{d2}v_{q1} + v_{d2}v_{q3} + v_{d3}v_{q1}} \end{cases} \tag{7}$$

From Fig.2, it can be seen that each sector includes one or two pair of small vectors (vertices of the inner hexagon), and one pair of small vectors can be divided into a positive and a negative vector. Positive and negative vectors will cause opposite zero-sequence voltages. The influences of positive zero-sequence voltage and negative zero-sequence voltage on the NP are complementary according to equation (3). Therefore, the NP voltage can be controlled by selecting proper small vectors in a pair.

III. Proposed CB-DPWM

In a three-level converter, it is very common that NP voltage can be controlled by proper small vectors based on SVB-PWM. However, this method requires a lot of tedious judgment and calculation, which greatly increases the workload. As mentioned before, the SVB-PWM is functionally equivalent to sine–triangle CB-PWM, which directly injects the calculated zero-sequence voltage into modulation wave and is easier to be achieved in practical applications. Therefore, the generalized zero-sequence voltage of CB-PWM required to control the NP voltage is calculated according to SVB-PWM. Then implement CB-DPWM modulation to reduce switching losses.

A) Injected Zero-Sequence Voltage Calculation

In this section, the method of calculating the injected zero-sequence voltage is laid out. A detailed step by step analysis of the injected zero-sequence voltage in sectors 1, 7 and 13 is provided to show how the calculation is done for every other sector. The calculated generalized zero-sequence voltage for all the other sectors of Fig. 2 is then provided.

For a reference voltage located in sector 1 of region 1 shown in Fig. 3, vectors (ppp), (ppo), (poo) and (ooo) are considered as the positive zero sequence (+) group while vectors (ooo), (oon), (onn) and (nnn) are the negative zero sequence (-) group. The time average of the positive or negative zero sequence components of the nearest vectors in a sector corresponding to the reference αβ0 voltage are calculated using (8).

$$\begin{cases} v_z^+ = v_{o1}^+ t_1 + v_{o2}^+ t_2 + v_{o3-1}^+ \alpha t_3 + v_{o3-2}^+ (1-\alpha) t_3 & \textit{positive} \\ v_z^- = v_{o1}^- t_1 + v_{o2}^- t_2 + v_{o3-1}^- \alpha t_3 + v_{o3-2}^- (1-\alpha) t_3 & \textit{negative} \end{cases} \tag{8}$$

where $v_{01}^+, v_{02}^+, v_{03-1}^+, v_{03-2}^+$ are the zero-sequence voltage of corresponding positive vectors (ppo), (poo), (ooo), (ppp) respectively, and $v_{01}^-, v_{02}^-, v_{03-1}^-, v_{03-2}^-$, are the zero-sequence voltage of negative vectors (oon), (onn), (ooo), (nnn) respectively. The quantity α is used to divide the time interval t_3 between the positive (ppp) and zero vector (ooo) or the negative vector (nnn) and the zero vector (ooo). The times t_1 and t_2 can be obtained for this sector according equation (7) and is given as (9):

$$\begin{cases} t_1 = \dfrac{2\sqrt{3}v_\beta}{v_{dc}} \\ t_2 = \dfrac{3v_a - \sqrt{3}v_\beta}{v_{dc}} \end{cases} \tag{9}$$

Now the output voltage of the converter in Fig. 2 are given from the inverse transformation in (10):

$$\begin{bmatrix} v_{ao} \\ v_{bo} \\ v_{co} \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1 \\ -\dfrac{1}{2} & -\dfrac{\sqrt{3}}{2} & 1 \\ -\dfrac{1}{2} & \dfrac{\sqrt{3}}{2} & 1 \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \\ v_z \end{bmatrix} \tag{10}$$

Moreover, the zero-sequence voltage of each vector in sector 1 are given as:

$$\begin{aligned} &v_{o1}^+ = \frac{v_{dc}}{3};\ v_{o2}^+ = \frac{v_{dc}}{6};\ v_{o3-1}^+ = \frac{v_{dc}}{2};\ v_{o3-2}^+ = 0 && \textit{positive} \\ &v_{o1}^- = -\frac{v_{dc}}{6};\ v_{o2}^- = -\frac{v_{dc}}{3};\ v_{o3-1}^- = -\frac{v_{dc}}{2};\ v_{o3-2}^- = 0 && \textit{negative} \end{aligned} \tag{11}$$

Therefore, the injected zero-sequence voltage of sector 1 can be expressed as:

$$\begin{cases} v_z^+ = 0.5\alpha v_{dc} - \alpha v_{ao} + (\alpha - 1) v_{bo} \\ v_z^- = -0.5\alpha v_{dc} - (\alpha - 1) v_{ao} + \alpha v_{bo} \end{cases} \tag{12}$$

In sector 1, the maximum and minimum phase voltage can be obtained as (13) according to (10):

TABLE I. GENERALIZED ZERO SEQUENCE VOLTAGE FOR ALL SECTORS

Sectors	Generalized Zero sequence voltage expression (v_z)	
1-6	$Positive\ 0.5\alpha v_{dc} - \alpha v_{max} + (\alpha - 1)v_{min}$	
	$Negative - 0.5\ \alpha v_{dc} + (\alpha - 1)v_{max} - \alpha v_{min}$	
7-12	$Positive\ 0.5\alpha v_{dc} + 2(\alpha - 1)v_{min} + (\alpha - 2)v_{max}$	$Positive\ 0.5\alpha v_{dc} + (1 - 2\alpha)v_{max} + (1 - \alpha)v_{min}$
	$Negative\ 0.5(\alpha - 1)v_{dc} + (2\alpha - 1)v_{min} + \alpha v_{max}$	$Negative\ 0.5(\alpha - 1)v_{dc} - 2\alpha v_{max} - (\alpha + 1)v_{min}$
13-24	$Positive\ or\ Negative\ 0.5(2\alpha - 1)v_{dc} - \alpha v_{max} - (1 - \alpha)v_{min}$	

$$\begin{cases} v_\alpha \in (0, \dfrac{v_{dc}}{3}) \\ v_\beta \in (0, \dfrac{2\sqrt{3}v_{dc}}{3}) \end{cases} \Rightarrow \begin{cases} v_{\max} = v_{ao} \\ v_{\min} = v_{bo} \end{cases} \tag{13}$$

Therefore, the injected zero-sequence voltage of sector 1 can be expressed as:

$$\begin{cases} v_z^+ = 0.5\alpha v_{dc} - \alpha v_{\max} + (\alpha - 1)v_{\min} \\ v_z^- = -0.5\alpha v_{dc} - (\alpha - 1)v_{\max} + \alpha v_{\min} \end{cases} \tag{14}$$

The other sectors in region 1 can be calculated by the similar steps, whose results are the same as equation (14). Then take sector 7 as an example of region 2, there are two cases of the zero-sequence voltage in the sector 7 shown in Fig. 3 due to the combination of different vectors, which can be expressed as:

$$\begin{cases} v_z^+ = v_{o1}^+\alpha t_1 + v_{o1}^-(1-\alpha)t_1 + v_{o2}t_2 + v_{o3}^+t_3 \\ v_z^- = v_{o1}^+\alpha t_1 + v_{o1}^-(1-\alpha)t_1 + v_{o2}t_2 + v_{o3}^-t_3 \end{cases} \quad or \quad \begin{cases} v_z^+ = v_{o1}^+t_1 + v_{o2}t_2 + v_{o3}^+\alpha t_3 + v_{o3}^-(1-\alpha)t_3 \\ v_z^- = v_{o1}^-t_1 + v_{o2}t_2 + v_{o3}^+\alpha t_3 + v_{o3}^-(1-\alpha)t_3 \end{cases} \tag{15}$$

Similarly, the zero sequence voltage in the sectors of region 3 for instance sector 13 shown in Fig. 3 is given in (16):

$$v_z = v_{o1}t_1 + v_{o2}t_2 + v_{o3}^+\alpha t_3 + v_{o3}^-(1-\alpha)t_3 \tag{16}$$

Different from the voltage configuration in regions 1 and 2, sectors in region 3 have only one injected zero-sequence voltage expression because they only have a pair of small vectors. In this case, the partition quantity α should be chosen as 1 to obtain v_z^+ and 0 to obtain v_z^-. Following the same procedure, the generalized zero-sequence voltage for all other sectors are calculated and shown in Table I.

B) Factor α Calculation for CB-PWM and CB-DPWM

As mentioned before, the influence of positive and negative zero-sequence voltage on the NP are complementary. When the upper dc capacitor voltage is higher, the zero-sequence voltage calculated by positive zero-sequence voltage should be selected to charge the lower capacitor. Otherwise, the negative zero-sequence voltage are selected. However, when the modulation index is higher than 0.58, the working area of the system will include region 3, which has only one generalized zero-sequence voltage as shown in Table I. Therefore, its positive and negative properties cannot be fully guaranteed. In this case, an exact factor α of region 3 can be calculated to control the neutral current i_p equal to 0, so that the dc-link capacitor voltages does not change in region 3. At the same time, the positive and negative zero-sequence voltages are injected to adjust the capacitor voltage difference in region 1 and 2. Therefore, the system can achieve NP voltage balance in each region by using CB-PWM based on Table I.

An exact α of region 3 is calculated to control the neutral current for NP potential balancing. For the dc link as shown in Fig. 1, the equation (17) should be satisfied:

$$i_p = i_{c1} - i_{c2} = C_{dc}\frac{d(v_{dc1} - v_{dc2})}{dt} = -2C_{dc}\frac{dv_{20}}{dt} \tag{17}$$

Equation (17) can be transformed as:

$$v_{20} = -\frac{1}{2C_{dc}}\int_0^t i_p dt + V_0 \tag{18}$$

where $i_p = (i_{La}S_{ao} + i_{Lb}S_{bo} + i_{Lc}S_{co})$ and V_0 is the initial value of v_{20}. Therefore, v_{20} will be constant if the average of i_p is controlled to be zero in each sampling period. In region 3, taking sector 13 shown in Fig. 3 as example, the average i_p can be expressed for region 3 as:

$$i_p = t_1 i_{p1} + t_2 i_{p2} + \alpha t_3 i_{p3\text{-}1} + (1-\alpha)t_3 i_{p3\text{-}2} \tag{19}$$

where i_{pi} (i =*1*, *2*, and *3*) are the neutral currents of the corresponding vectors. α is used to divide the time interval t_3. i_{pi} can be simply represented by three phase output currents i_{La}, i_{Lb} and i_{Lc} according to the switching states shown in Fig. 3.

To achieve the $i_p = 0$, equation (20) can be obtained:

$$\alpha = \frac{t_1 * i_{p1} + t_2 * i_{p2} + t_3 * i_{p3\text{-}2}}{t_3 * (i_{p3\text{-}2} - i_{p3\text{-}1})} \tag{20}$$

Thus, the corresponding α of each sector can also be calculated and shown in Table II. Then substitute α into Table I, the injected zero sequence voltage in region 3 can be determined as:

$$v_z = \frac{t_1 * i_{p1} + t_2 * i_{p2} + t_3 * i_{p3\text{-}2}}{t_3 * (i_{p3\text{-}2} - i_{p3\text{-}1})} * (v_{dc} - v_{\max} + v_{\min}) - 0.5v_{dc} - v_{\min} \tag{21}$$

In the proposed CB-PWM method, each sector in region 3 has its own injected zero-sequence voltage. Similar to the previous SVM and CB-PWM methods, the judgment calls and computational intensiveness for this method is also obviously large.

In order to avoid the above problems, the injected zero-sequence voltage of region 3 can be re-planned. It can be seen from equation (16) that when α is 1, the injected zero-sequence voltage is the maximum value, which thus can be regarded as a positive zero-sequence voltage. In contrast, when α is 0, the

TABLE II. FACTOR α OF REGION 3 TO ACHIEVE CB-PWM

Sectors 13, 19	$\alpha=\frac{1}{2}[1-\frac{t_2 i_c}{t_3 i_a}]$	Sectors 16, 22	$\alpha=\frac{1}{2}[1-\frac{t_1 i_a}{t_3 i_c}]$
Sectors 14, 20	$\alpha=\frac{1}{2}[1-\frac{t_1 i_c}{t_3 i_b}]$	Sectors 17, 23	$\alpha=\frac{1}{2}[1-\frac{t_2 i_b}{t_3 i_c}]$
Sectors 15, 21	$\alpha=\frac{1}{2}[1-\frac{t_2 i_a}{t_3 i_c}]$	Sectors 18, 24	$\alpha=\frac{1}{2}[1-\frac{t_1 i_b}{t_3 i_a}]$

injected voltage is the minimum value, and it can therefore be regarded as a negative zero-sequence voltage. Moreover, another advantage of selecting 1 and 0 for α is to realize CB-DPWM, thereby reducing switching losses. Similarly, the α of region 1 and 2 should be chosen 1 or 0 to achieve CB-DPWM. Generally, the factor α should be chosen 0 rather than 1 in region 1 to prevent switching state changing rapidly due to the large magnitude of v_z, while a should be chosen as 1 for v_z^+ and 0 for v_z^- in region 2 and 3. However, it is very interesting that when the factor α of region 1 is selected as 1, the positive and negative zero-sequence voltages of all regions are the same, as shown in equation (22):

$$\begin{cases} v_z^+ = 0.5v_{dc} - v_{\max} \\ v_z^- = -0.5v_{dc} + v_{\min} \end{cases} \tag{22}$$

Therefore, the zero-sequence voltage shown in (22) can be injected into the original modulation signals to reduce the NP ripple, which is easier realized in practical applications compared with the CB-PWM method of this paper and other CB-DPWM methods of previous literatures.

C) *Control Scheme and Simulation Results*

The control schemes of the T-type converters with NP potential balancing based on the zero-sequence voltage injection is presented as Fig. 4. The PI controller block, PLL, stationary transformation, synchronous frame transformation and all inverse transformation have been put together in the controller block to emphasize the method of zero sequence voltage injection in Fig. 4. Note that the voltage/current control block takes as input the grid line current measurement, the grid voltage measurement and the dc link capacitor measurement. Within this block the measured grid voltages are used to obtain the grid frequency using a PLL, a synchronous reference frame PI current controller [22] is implemented. The synchronous reference frame variables are obtained from a reference frame transformation within the controller block using the synchronous reference frame angle obtained from the PLL output also implemented within the block. The *qd* modulation are calculated and inverse transformation applied to obtain the *abc* modulation signals. In the proposed CB-DPWM method, the injected zero sequence voltages are then determined based on the calculations in Table I (or equation (22)) and the relative magnitudes of the capacitor voltages. Compared with the CB-DPWM, CB-PWM requires more conditional judgments, calculation and three-phase output current values. The phase disposition modulation scheme [23] has been used as shown in the drive signal generating block in Fig. 4.

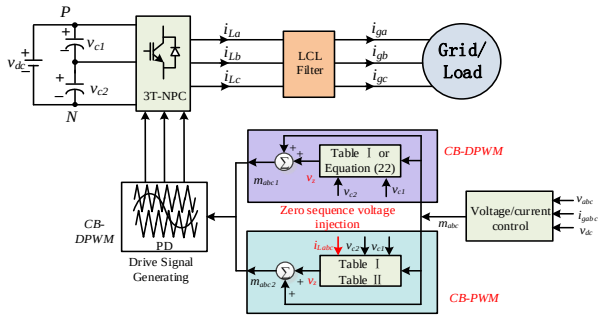


Fig. 4. Control scheme of the proposed modulation strategy.

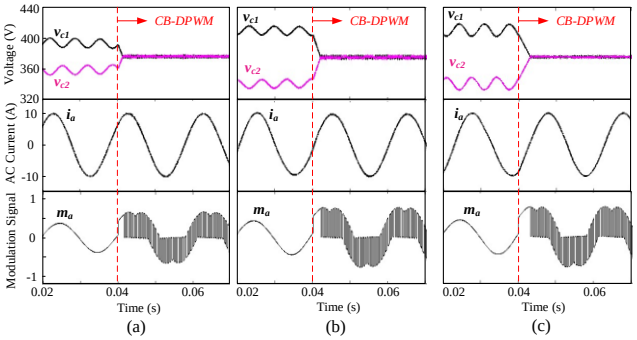


Fig. 5. Simulation results of the CB-DPWM at low modulation index, m = 0.42. (a) φ = 45 (lagging). (b) φ=0 (unity). (c) φ=-45 (leading)

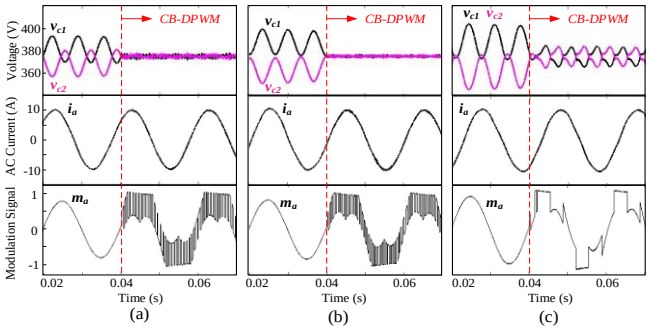


Fig. 6. Simulation results of the CB-DPWM at high modulation index, m = 0.83. (a)φ = 45(lagging). (b) φ = 0 (unity). (c) φ=-45 (leading)

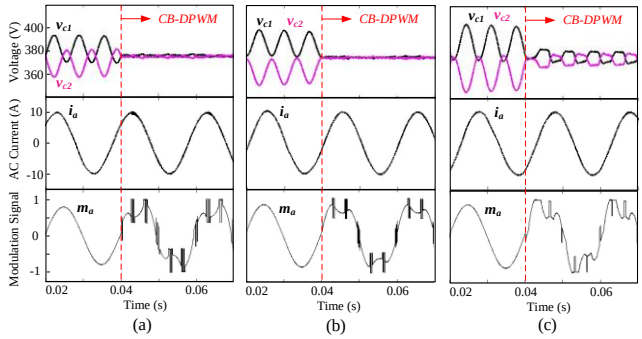


Fig. 7. Simulation results of the CB-PWM at high modulation index, m = 0.83. (a) φ=45 (lagging). (b) φ=0 (unity). (c) φ=-45 (leading)

To verify the effectiveness of the proposed modulation strategy, a MATLAB/SIMULINK model is built. The switching frequency is 10 kHz and sampling frequency is 10 kHz in the simulation. The dc-link voltage is 750 V and dc-link

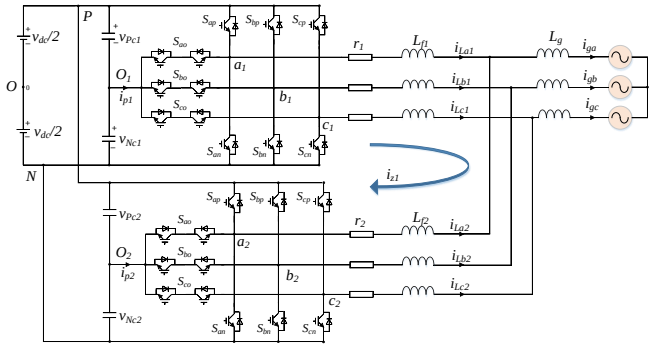


Fig. 8. Structure of the parallel three-level T-type converter system.

capacitances are 220 μF each. The AC grid voltages are 220 V and the fundamental frequency is 50 HZ. The parameters of LCL filter are 7.3 mH, 3.3 μF and 0.7 mH. It is worth noting that a 1Ω resistor is connected in series with the capacitor of the filter to increase damping. The simulation results are shown in Fig.5, Fig. 6 and Fig. 7. In these figures, φ is the angle between the ac currents and ac voltages, which is the power factor angle. On each figure from top to bottom are the voltages of the two capacitors, output current and modulation signal of phase A.

Fig. 5 shows the simulation results for low modulation index ($m = 0.42$), the proposed CB-DPWM method is applied at $t = 0.04sec$. It can be seen that NP voltage ripple can be eliminated quickly and modulation signal are clamped to 0 around 1/3 cycle period in region 1 when the proposed modulation strategy is used. Moreover, the method is effective at low modulation index for lagging power factor shown in Fig. 5(a), unity power factor shown in Fig. 5(b) and leading power factor shown in Fig.5 (c). In all the cases, the dc link capacitor voltages are equalized when the modulation strategy is applied therefore the neutral point voltage which is proportional to the difference of the dc link capacitor voltages is zero. It can be seen from Fig. 5 that the maximum voltage difference of two dc-link capacitors has changed from 48 V, 85 V and 90 V to 3 V, 3 V and 2 V in the three cases respectively when the proposed control strategy is implemented. In regions 2 and 3 (high modulation index), the modulation strategy is also effective as shown in Fig. 6 and Fig. 7. While Fig. 6 shows the results for CB-DPWM, Fig. 7 shows the results for the same load conditions but using CB-PWM. In Fig. 6, the maximum capacitor voltage difference in the three cases changed from 41 V, 52 V and 60 V to 5 V, 2 V and 15 V respectively while implementing the proposed control strategy. Similarly, the voltage difference in Fig. 7 also changes from 41 V, 52 V and 60 V to 4 V, 3 V and 11 V in the three cases respectively. Therefore, it can be found that the NP voltage ripple is only reduced rather than eliminated completely in Fig. 6(c) and 7(c) for the leading power factor case. The reason is that the proposed methods are also based on conventional SVM, which cannot fully achieve the NP balancing at high modulation indexes and low power factors [24], [25]. This drawback is inherent for conventional SVM or CB-PWM. From the perspective of the proposed methods, the injected positive zero-sequence voltage and negative zero-sequence voltage of the region 3 as shown in (16) cannot be guaranteed to be greater than 0 and less than 0 in these cases, respectively. Compared with the CB-DPWM, the CB-PWM has higher switching losses

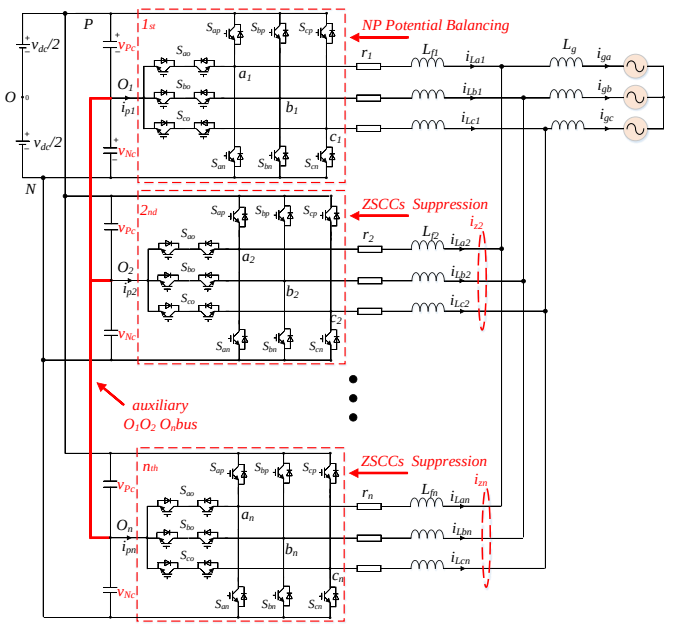


Fig. 9. *N* Parallel three-level T-type converters.

and complex calculation but smoother capacitor voltages shown in Fig .7(c). Compared to the SPWM without the zero-voltage injection, both methods in this paper will have less switching losses since as can be seen in the modulation signals of Fig. 6 and Fig. 7, there is a significant clamping of the modulation signal at both the positive and negative rails.

IV. Discussion on Parallel Converters

Parallel operation of three-level converters is a very common way to increase the power level and provide multi-level output waveforms. In this section, the proposed methods will be discussed for parallel converter systems. However, ZSCCs will be generated due to the injected zero-sequence voltages and parameters differences of the parallel system in practical applications. Moreover, ZSCCs and NP voltage unbalance will affect each other. In this case, many methods that use neutral current i_p to deal with NP voltage variation of a single three-level converter are not applicable in parallel systems, including the CB-PWM method shown in this paper. Different from CB-PWM, a coordinated strategy based on proposed CB-DPWM can be used in parallel systems to tackle the problems of NP voltage unbalance and ZSCCs simultaneously.

The parallel two three-level T-type converter system using separate inductors is shown in Fig. 8, which shares the same NP. In fact, it is also common to use intercell transformer to connect parallel converters due to isolation, filtering and very good dynamic behavior [26], [27]. However, the intercell transformer technique requires a high number of cells to avoid additional output inductor and has a complex faulty cell management due to high coupling. Therefore, the case of the parallel T-type converters connected by separate inductors are shown in this paper for the convenience of discussion. Assume all the active switches to be ideal. Then, according to the Kirchhoff's laws, the following equations can be obtained:

$$\begin{cases} L_{f1}\dfrac{di_{La1}}{dt}+r_1 i_{La1}-V_{a1O1}-L_{f2}\dfrac{di_{La2}}{dt}-r_2 i_{La2}+V_{a2O2}+V_{O2O1}=0 \\ L_{f1}\dfrac{di_{Lb1}}{dt}+r_1 i_{Lb1}-V_{b1O1}-L_{f2}\dfrac{di_{Lb2}}{dt}-r_2 i_{Lb2}+V_{b2O2}+V_{O2O1}=0 \\ L_{f1}\dfrac{di_{Lc1}}{dt}+r_1 i_{Lc1}-V_{c1O1}-L_{f2}\dfrac{di_{Lc2}}{dt}-r_2 i_{Lc2}+V_{c2O2}+V_{O2O1}=0 \end{cases} \quad (23)$$

where V_{k1O1} and V_{k2O2} are the phase-k output voltage of the first and second converter between phase output and dc-link potential point O respectively; i_{Lk1} and i_{Lk2} are the phase-k output currents of the first and second converter respectively; $k\in\{a, b, c\}$; V_{O2O1} is the voltage between the dc-link potential point of the second converter O_2 and that of the first converter O_1.

The ZSCCs of the first converter can be defined as:

$$i_{z1}=\frac{1}{3}(i_{La1}+i_{Lb1}+i_{Lc1}) \quad (24)$$

So by adding the above equations in (23), and using (24), the equation (25) can be obtained:

$$i_z(s)=\frac{\frac{1}{3}\sum_{i=a,b,c}(V_{i1O1}-V_{i2O2})+V_{O1O2}}{(L_{f1}+L_{f2})s+(r_1+r_2)} \quad (25)$$

It is noting that only low-frequency ZSCCs is discussed in this paper.

In this case, the NP potential of parallel systems has been controlled by injecting the zero-sequence voltage of converter-1 as shown in Table I, while the ZSCCs could be suppressed by the distribution factor α_2 of small vectors of converter 2. As mentioned before, the expression of the ZSCCs is shown in equation (25). To achieve i_z=0, a direct solution is presented as equation (26):

$$\sum_{i=a,b,c}(V_{i1O1}-V_{i2O2})=0 \quad and \quad V_{O1O2}=0 \quad (26)$$

To achieve V_{O1O2}=0, the neutral points O_1 and O_2 of parallel converters can be linked as shown in Fig.9. However, auxiliary O_1O_2 bus cause different i_p, which is difficult to be calculated accurately at this time. Therefore, the method of controlling NP voltage ripple by calculating i_p in a single converter is not suitable for parallel systems, including the proposed CB-PWM method. It is worth noting that proposed CB-DPWM method is not included, which adjusts the NP voltage ripple according to the capacitor voltage differences.

Moreover, it can be seen from equation (26) that the distribution factor of small vectors of converters are only used to control the output voltage of the parallel converters to be the same to suppress the circulating currents. Although the ZSCCs can be separated into the high-frequency components and low-frequency components, only low-frequency ZSCCs is affected by the distribution factor. Therefore, while the high-frequency components are neglected, the output voltage of converters can be expressed as (27):

$$\sum_{i=a,b,c}V_{ijOj}=v_{aj}+v_{bj}+v_{cj}+3v_{zj} \quad (j=1,2) \quad (27)$$

where v_{ij} are the phase i original modulation voltage of the j converter and v_{zj} are the injected zero-sequence voltage of the j converter. Then, the v_{z2} can be obtained:

$$v_{z2}=v_{z1}+\frac{1}{3}(\sum_{i=a,b,c}v_{i1}-\sum_{i=a,b,c}v_{i2}) \quad (28)$$

where v_{z1} is the injected zero-sequence voltage of the first converter to deal with NP voltage ripple problem. It is worth noting that the distribution factor α_2 can also be calculated and conducive to further analysis in the future work. Because region 3 has only one controllable degree of freedom, taking sector 13 shown in Fig. 3 as example, the injected zero-sequence voltage of converter-2 v_{z2} are shown in (29):

$$v_{z2}=t_{a2}v_{oa2}+t_{b2}v_{ob2}+\alpha_2 t_{c2}v_{oc2}^{+}+(1-\alpha_2)t_{c2}v_{oc2}^{-} \quad (29)$$

where t_{a2}, t_{b2} and t_{c2} can be calculated by the equation (5); v_{oa2}, v_{ob2}, v_{oc2}^{+} and v_{oc2}^{-} are the zero-sequence voltage of corresponding vectors PON, PNN, POO, ONN respectively. The distribution factor α_2 is used to divide the time interval t_c between the positive vector POO and negative vector ONN.

The distribution factor α_2 of converter-2 in region 3 can be obtained by combining (28) and (29):

$$\alpha_2=\frac{v_{z1}+(\sum_{i=a,b,c}v_{i1}-\sum_{i=a,b,c}v_{i2})/3-(v_{oa2}+v_{ob2})-v_{oc2}^{-}*t_{c2}}{v_{oc2}^{+}*t_{c2}-v_{oc2}^{-}*t_{c2}} \quad (30)$$

The proposed method can be easily extended to n parallel three-level T-type converters. In n converter parallel system, n-1 ZSCCs exist. Therefore, the converter-1 controls the common NP potential with the extra NP bus, and n-1 converters are in charge of ZSCCs suppression. Generally speaking, the sum of modulation signals of each converter is almost the same. Therefore, the zero-sequence voltage of all converters should be equal for suppressing ZSCCs [28], which are shown as:

$$v_{z1}=v_{z2}=v_{z3}=\bullet\bullet\bullet=v_{zn} \quad (31)$$

Similarly, the distribution factor a_j of jth converter in region 3 can be calculated, which are shown in (32):

$$\alpha_j=\frac{v_{z1}-(v_{oaj}+v_{obj})-v_{ocj}^{-}*t_{cj}}{v_{ocj}^{+}*t_{cj}-v_{ocj}^{-}*t_{cj}} \quad (32)$$

Similarly, in order to verify the proposed control strategy of the parallel system, a MATLAB/SIMULINK model was established. The parameters are the same as the previous simulation parameters of a single converter. The grid inductance value L_g is 2.5 mH. The simulation results are shown in Fig. 10. Each figure from top to bottom are the voltages of two capacitors, circulating currents, grid currents and phase A modulation signal of the converter-1. i_{1ref} and i_{2ref} represent the output current reference of the converter-1 and converter-2 respectively. To begin with, Fig.10(a) shows the steady-state simulation results with conventional method. It is obvious that there are large NP voltage ripple and circulating current, which also causes low-

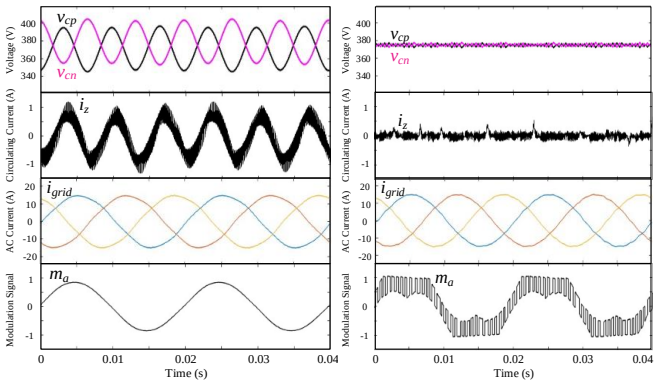


Fig. 10. The steady-state simulation results with i_{1ref}=10A, and i_{2ref}=5A. (a) for the conventional method; (b) for the proposed method.

frequency harmonics of grid currents. In comparison, Fig.10(b) shows the steady-state simulation results with the proposed method. As expected, the upper dc capacitor voltage v_{cp} is almost equal to the lower dc capacitor voltage v_{np}, while the low-frequency components of circulating currents are eliminated. Moreover, the modulation signal usually clamp to 1 or -1. Although the every clamping time is not long, it is far greater than the switching period.

V. Experimental Results

For experimentally validating the findings, a low power-rate laboratory prototype is built as shown in Fig. 11, whose system specifications are listed in Table III. It is worth noting that the parameters of the converter in the experiment are not the same as those of the simulation, because converters in the experiments are existing products and parameters are fixed. In order to highlight the effectiveness of the control strategy, smaller DC capacitance and higher voltage levels are given in the simulation. In the experiments, the AC side was emulated by a programmable source Chroma 61511. The DC side is obtained from the power grid through the diode rectifier. A T-type NPC inverter with the model of 10-F112M3A025SH from Vincotech [29] is used for the switching processor. The digital signal controller dSPACE 1005 is used to implement the digital control.

A) Experimental Results for Single Converter

Fig. 12 shows the experimental results with a converter operating in low modulation index comparable to the case of the simulation results shown in Fig. 5. In order to verify the effectiveness of the proposed method, the initial voltages on the dc-link capacitors are unbalanced. However, since the dc-link capacitance is too large, the capacitor voltages in the experiments does not have the same large AC voltage ripple as that of the simulation. When the proposed CB-DPWM method was activated, the two capacitor voltages of dc link are balanced rapidly. In a similar way Fig. 13 presents the experimental results of different power factors with high modulation index. It can be seen that the capacitor voltages were controlled to be balanced within 20ms. Moreover, it is worth noting that the grid currents under SPWM have obvious low-order harmonics due to unbalanced capacitor voltages, which are basically eliminated under the proposed CB-DPWM.

TABLE III. Parameters Used for the Experimental Test

Symbol	Description	Value
f_c	Carrier frequency	10 kHz
f_s	Sampling frequency	10 kHz
f_o	Fundamental frequency	50 Hz
v_{dc}	DC-link voltage	375 V
i_g	Peak grid current	4 A
C_{dc}	DC-link Capacitance	1340 μF
L_f	AC filter inductances	7.3 mH
C_f	AC filter capacitances	3.3 μF
L_g	AC grid inductances	0.7 mH
V_{ac}	AC grid voltage	220 V
IGBTs	Intelligent Power Module	10-F112M3A025SH

As for the dynamic responses, Fig. 14 shows the waveforms under the CB-DPWM, when the magnitude of the grid currents changed from 2A to 4A. It is evident that the capacitor voltages remain balanced and the grid currents also perform well. In Fig. 15, the experimental results of CB-PWM with unity power factor is shown, where the balanced time of capacitor voltages is slightly slower than that of CB-DPWM.

The modulation signals of the converter cannot be measured directly by the oscilloscope, which are thus shown in the layout. For completeness Fig. 16 is included to shows the modulation signals of the SPWM, CB-DPWM at low modulation index, CB-DPWM at high modulation index and CB-PWM at high modulation index, respectively. It is clear from Fig. 16 that the switching off-time of CB-DPWM is longer than that of CB-PWM. This is because the injected zero-sequence voltage in CB-PWM only achieves i_p=0 for most of the time, rather than adjusting the capacitor voltages at all times. Therefore, the capacitor voltage balance under the CB-DPWM method is also faster as shown in Fig. 13 and Fig. 15.

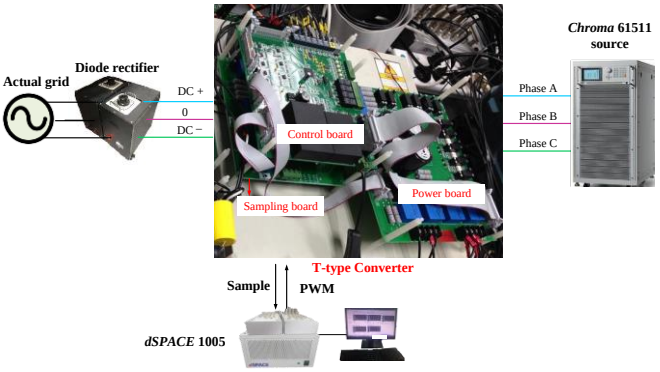


Fig. 11. Experimental setup in the lab to validate the proposed topologies.

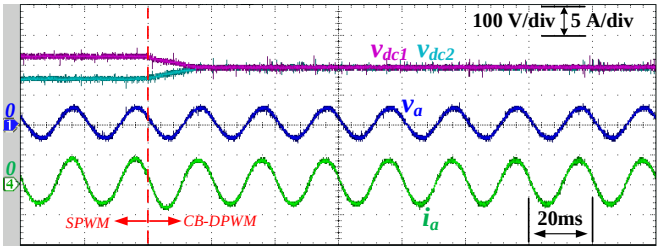
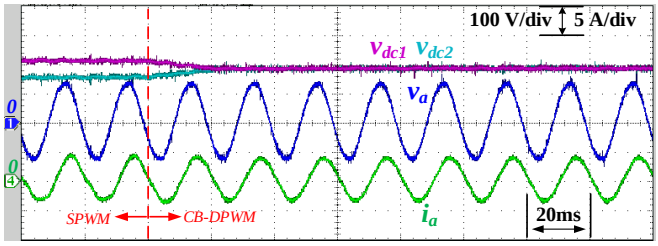
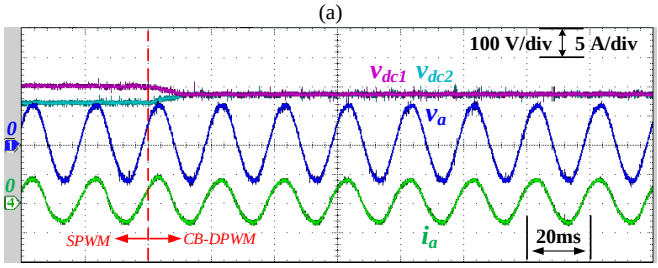


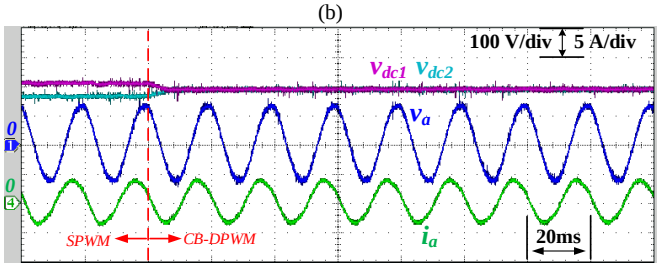
Fig. 12. Experimental results of the CB-DPWM: m = 0.35, φ=0 (unity).



(a)



(b)



(c)

Fig.13. Experimental results of the CB-DPWM at high modulation index, *m* = 0.83. (a) φ = 45(lagging). (b) φ = 0 (unity). (c) φ=-45 (leading)

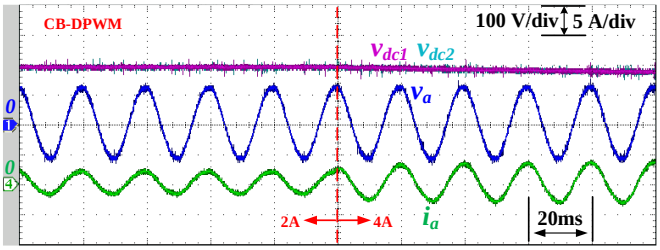


Fig. 14. Experimental results of grid-current responses when implementing CB-DPWM.

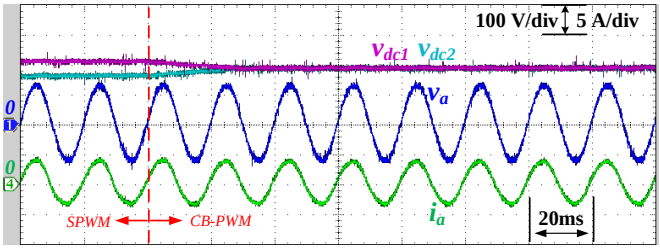
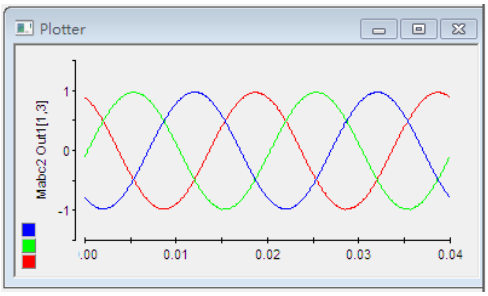
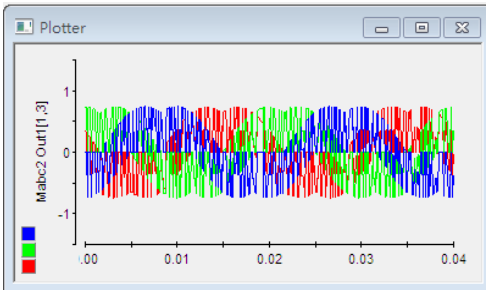


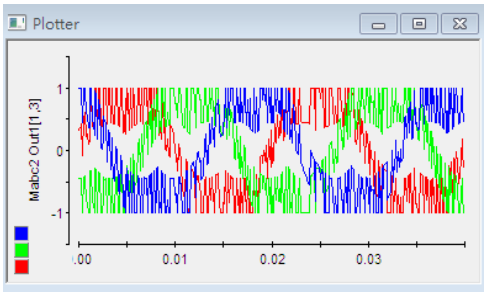
Fig. 15. Experimental results of the CB-PWM: m = 0.83, φ=0 (unity).



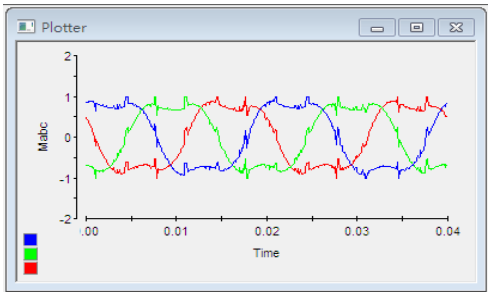
(a)



(b)



(c)



(d)

Fig. 16. Experimental results of the modulation signals under (a) the SPWM, (b) the low modulation index of the CB-DPWM, (c) the high modulation index of the CB-DPWM, (d) the high modulation index of the CB-PWM.

B) Experimental Results for Parallel Converters

To prove the effectiveness of the proposed strategy in parallel T-type converters, the corresponding experimental results are given. The equations of the carrier-based generalized discontinuous modulation signals given in Table I and in (28) have been programmed in a dSPACE 1005 for the neutral point voltage balancing and circulating currents suppression of parallel two three-phase three-level T-type converters. Similarly, to verify the effectiveness of the proposed methods, the parallel resistances of dc-link capacitors are different, so the initial voltages on the dc-link capacitors are unbalanced. In this

case, Fig. 17 shows the steady-state experimental results under the SPWM. It can be seen that the parallel system has unbalanced dc-link capacitor voltages and circulating currents. Under the same conditions, Fig. 18 shows the steady-state experimental results under the proposed CB-DPWM. Similar to the simulation, the dc-link capacitor voltages are balanced and low-order circulating currents are eliminated. As for the dynamic performances, Fig. 19 presents the experimental results under the CB-DPWM, when the magnitude of the output grid currents changed from 2A to 5A. During this period, the parallel system still performs well. To show the differences between the SPWM and the proposed CB-DPWM clearly, the phase A modulation signals of the converter-1 are given in Fig. 20. Compared with the modulation signals of the SPWM, the modulation signals of the proposed CB-DPWM usually clamp to 1 or -1, so the switches does not work to reduce the switching losses during these periods. The viability and performance of the proposed method has been verified by the above simulation results and experimental results. The viability and performance of the proposed method has been verified by the above simulation and experimental results.

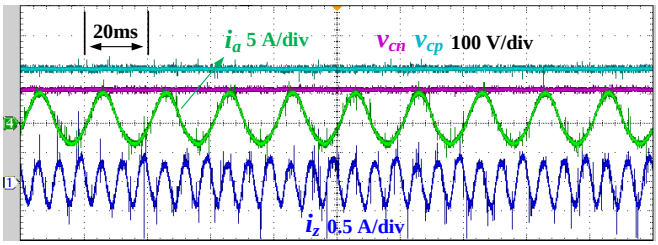


Fig. 17. The steady-state experimental results under the SPWM.

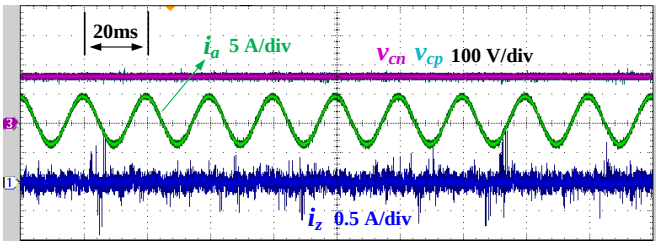


Fig.18. The steady-state experimental results under the proposed CB-DPWM.

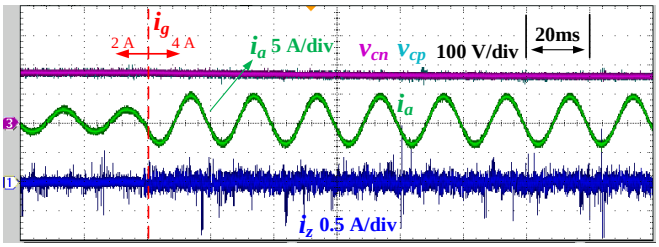


Fig.19. The dynamic experimental results under the proposed CB-DPWM.

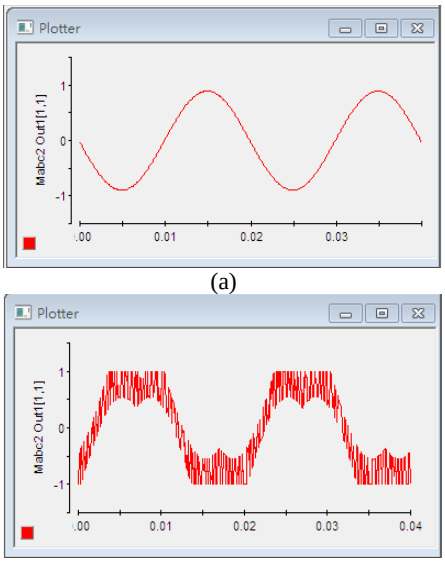


Fig. 20. Experimental results of the phase A modulation signals in parallel system. (a) under the SPWM; (b) under the proposed CB-DPWM.

VI. Conclusion

This paper shows the generalization of the injected zero-sequence voltage expressions for the modulation signals in three-level T-type converters for controlling NP voltage. The zero sequence voltages are determined from the space vector synthesis of the converter output voltages using only a few judgment conditions. The balancing of NP voltage is achieved for full power factors in low modulation indexes and wide range of power factors in high modulation index. Using the CB-DPWM method discussed in the paper, the switching losses for the T-type converter are reduced as the modulation signal is clamped to zero, positive or negative rails for a significant portion of the period. Another advantage of the proposed method is that it is really simple and can therefore be implemented quickly in practical applications compared with the SVM and even previous CB-DPWM. Moreover, the proposed CB-DPWM can also be extended to parallel systems, which can suppress NP voltage ripples and circulating currents simultaneously by a coordinated strategy. MATLAB-based simulations and experiments on a small-scale prototype demonstrate the feasibility of the proposed methods.

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