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Ultra-low-power Analog-to-Digital Conversion

A sub-nano-Watt 10-bit 1ksample/s asynchronous SAR ADC in 22nm FDSOI

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Abstract

An Ultra-Low-Power fully differential asynchronous Successive-Approximation (SAR) Analog-To-Digital Converter (ADC) is implemented in a conventionally available $22nm$ Fully-Depleted-Silicon-On-Insulator (FDSOI) technology. With the demand for long-lifetime devices powered by small batteries increasing, components specialized for low power consumption have become ever more popular. An ADC with low power consumption at the cost of lower sampling frequency could be used for various sensing systems, for example, home automation.

The presented ADC has a sampling rate of $1000samples/s$ and a resolution of 9.1 Effective Number Of Bit (ENOB). With a V_{dd} of $0.4V$, the ADC uses $< 500nW$ average per conversion partly post-layout. The comparator used is a strongarm latch. The Digital-To-Analog (DAC) is a Capacitive DAC (CDAC) with a unit capacitance of $1.15fF$. The inputs are compared through switching between three voltage references at $0.4V$, $0.2V$, and $0V$. Pre-charging the DAC to $0.2V$ volts limits the voltage change to $\frac{V_{ref}}{2}$ compared to V_{ref} in a conventional SAR ADC.

Sammendrag

En ultra-lav-effekt fulstendig differensiell asynkron suksessiv-approksimations-register (SAR) analog-til-digital-ommformer(ADC) er foreslått i en konvensjonelt tilgjengelig $22nm$ fullstendig-utarmet-silisium-på-isolator-teknologi. Etterspørselen etter enheter med lang levetid drevet av små batterier øker. Med det blir komponenter spesialisert på lavt strømforbruk stadig mer populære. En ADC med lavt strømforbruk på bekostning av lavere samplingsfrekvens kan brukes til en rekke ulike sensorsystemer, for eksempel i hjemmeautomasjon.

ADC-en som pressenteres har en samplingshastighet på $1000sample/s$ og en oppløsning på $9,1$ Effektivt antall bit(ENOB). Med en V_{dd} på $0,4V$ bruker ADC-en $< 500nW$ i gjennomsnitt per konvertering simulert delvis post-layout. Komparatoren som brukes er en dynamisk vippe. digital-til-analog-ommformeren(DAC) er en kondensatorarray-DAC med en enhetskapasitans på $1,15fF$. Inngangene sammenlignes ved å bytte mellom tre spenningsreferanser på $0,4V$, $0,2V$ og $0V$. Forhåndslading av DAC-en til $0,2V$ volt begrenser spenningsendringen til $\frac{V_{ref}}{2}$ sammenlignet med V_{ref} i en konvensjonell SAR ADC.

Acknowledgements

This thesis concludes my master's education at NTNUI. Therefore, I would like this opportunity to share my gratitude to a group of amazing people:

First of all, a great thanks to my parents. You always support me, whether with words or driving fourteen hours to pick up a TV, which is truly remarkable. Furthermore, thanks to Dr. Paul L. Bergstrom at MTU for introducing me to the magnificent world of VLSI. Trond Ytterdal and Olivia Mirea at NTNU for all knowledge shared through the last two years. Finally, thanks to NTNUI Lacrosse for keeping me sane with great friendship and exercise.

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List of Acronyms

ADC - Analog-To-Digital Converter

BOX - Burried Oxide layer

CDAC - Capacitive-Digital-To-Analog Converter

CMOS - Complimentary-Metal-Oxide-Semiconductor

DAC - Digital-To-Analog Converter

DFF - Data Flip-flop

DRC - Design Rule Check

ENOB - Effective Number Of Bit

FDSOI - Fully-Depleted-Silicon-On-Insulator

FFT - Fast Fourier transform

LSB - Least Significant Bit

LVS - Layout Versus Schematic

MSB - Most Significant Bit

NMOS - Negative-Channel Metal-Oxide-Semiconductor

PMOS - Positive-Channel Metal-Oxide-Semiconductor

RC - Resistor-Capacitor

RMS - Root mean square

SAR - Successive-Approximation- Register

SNDR - Signal-To-Noise-and-Distortion ratio

SQNR - Signal-To-Quantization noise ratio

WPE - Well-Proximity-Effect

1 Introduction

The race to down-scale Complimentary-Metal-Oxide-Semiconductor (CMOS) technologies is traditionally motivated by the need for larger units of computational power on a small physical area. However, restrictions such as power dissipated as heat draw a line for what is physically possible on a silicon chip. Therefore, designers and technology developers have to think in new and different ways. Modern technology nodes provide continuously better options for developing energy-efficient circuits. As a result, both analog and digital designers are testing the limits of how energy-efficient their designs can be. Low-frequency clocks are one way to minimize energy consumption. For many applications where computational power is non-critical, sacrificing clock speed for lower energy consumption is a consideration.

A concrete example is remote sensing circuits in home automation systems. Such circuits could be implemented to monitor temperature, light, or humidity. After that, the measurement could be sent to a mother circuit elsewhere in the house. The sensing system could be implemented with an intrinsic battery, making it entirely remote for easy installation. Maximizing the lifetime of the battery would be crucial for this circuit. A key component in any sensor system is the Analog-To-Digital Converter (ADC), which converts the analog sensor information into the digital domain for further processing. The sensing system just described is mare one example of the usefulness of an ultra-low-power ADC.

In order to compare performance between ADCs with different specifications, designers use a Figure of Merit (FOM). A widely used FOM for low-power ADCs is the quantity of power consumed per conversion-step. The FOM is calculated as:

$$\frac{Power[J]}{2^{EffectiveNumberofBit} Samplingfrequency[Hz]} \tag{1}$$

Several ADC topologies are proposed and implemented in the literature. However, when energy efficiency is prioritized together with the FOM: Successive-Approximation-Register (SAR), ADCs perform well [2][3]. SAR ADCs consist of a comparator, an n-bit register, a Capacitive Digital-To-Analog Converter (CDAC) (two if the ADC is fully differential), and a minimal amount of digital circuitry to control the SAR algorithm. Much of the SAR ADC's functionality is controlled by the size of the capacitors in the DAC. Therefore, the SAR ADC can be modified to have high accuracy, high speed, or low power consumption, sacrificing one for the others. Different techniques are used

to improve the standard SAR ADC, such as adding a $\Sigma\Delta$-filter or multi-step ADCs. However, these techniques add complexity compared to the conventional SAR ADC.

1.1 Design specifications

A SAR ADC is to be designed and verified digitally. The ADC should be comparable to state-of-the-art ADCs concerning power consumption. Furthermore, the ADC should have a resolution of at least > 9 Effective-number-of-bit to justify using a 10-bit output. To perform at low power, the ADC will operate with a sampling rate of 1k-Samples per second. Additionally, the ADC shall produce an internal clock signal for internal operations, thus minimizing the dependency on external signals. The ADC will be designed using a commercially available 22nm Fully-Depleted-Silicon-on-Insulator (FDSOI) technology node. The technology's thin oxide devices do not allow for larger voltages than $800mV$; other than that, the power supply is a parameter to be optimized. Finally, the on-chip area should be minimized whenever the area does not affect the device's performance. The specifications are listed in table 1.

Table 1: Design specifications.

Resolution	> 9 ENOB
Sampling frequency	$1kS/s$
Power consumption	Minimize
Area	Minimize
Power supply	Optimize

1.2 Contribution

This thesis is a continuation of the specialization project [4] in which an in-depth analysis of State-of-the-art ADCs is performed. Additionally, a comparator, DAC, DAC switching scheme, and an internal clock driven by the comparator outputs were implemented on schematics. The digital logic was implemented as an ideal Verilog code, and the simulations were performed with a mix between the Spectre and the internal digital simulator in Cadence Virtuoso.

This thesis contributes to the implementation of schematic digital circuitry and improvements

to the comparator and DAC by increasing their accuracy and lowering the power consumption. Moreover, the DAC switches are improved by decreased distortion in the DAC and implementing a bootstrapped input switch with increased resistive linearity. An area estimation for the ADC will be presented, together with implementing a custom non-ideal unit capacitor. Finally, simulations are performed with post-layout parasitic for the comparator.

1.3 Thesis structure

The outline of this thesis is as follows:

2. **Background Theory -** Relevant theory to describe concepts and decisions.
3. **High-level design and design choices -** Reasoning behind the chosen topologies and techniques used for the implementation.
4. **implementation -** The implementation of the SAR ADC is described.
5. **Results -** Results are presented with a description of their test bench.
6. **Discussion -** A retrospective discussion of design choices, implementation, and results.
7. **Conclusion and future work -** A conclusion is presented together with proposed future work.

2 Background theory

This section will cover essential background theory to explain the methodology and discuss results and design choices. Some of the theory is already mentioned in [4] but is repeated for convenience.

2.1 Fully Depleted Silicon On Insulator

Traditionally, Complimentary-Metal-Oxide-Semiconductor (CMOS) technology nodes are scaled-down by decreasing the minimum length of the gate. However, as the gates get smaller, non-idealities and physical limits force the developers to think new. One alternative to the conventional bulk process transistor is the Fully-Depleted-Silicon-on-Insulator (FDSOI) transistor structure. Essentially the FDSOI process differs from the bulk process with its Buried-Oxide layer (BOX). The BOX is grown on top of the substrate, fully isolating the channel as shown in figure 1. As a result, the transistors are less affected by threshold variability due to random dopant fluctuation in the substrate. Furthermore, the isolated channel leads to less leakage current in the transistors' "off"-state, allowing high-performance transistors without the high leakage in small bulk CMOS technology nodes. Another advantage of the FDSOI compared to, for example, finFET is that it is a linear technology. Therefore, traditional design tools used for bulk technologies are still available[5].

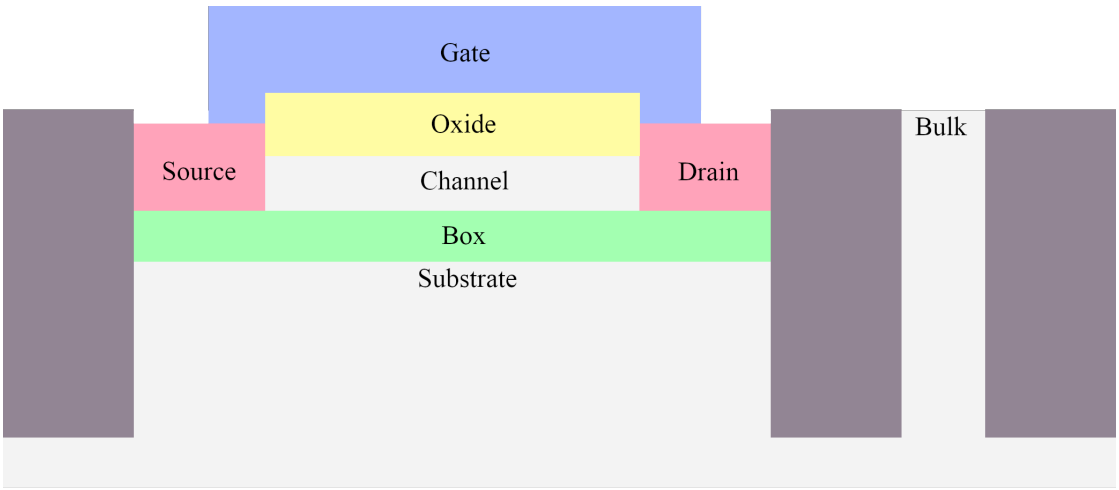


Figure 1: Cross section of an FDSOI structure.

2.2 Data conversion

While the digital platforms for problem-solving are continuously improved, the world around it remains analog. Therefore, a crucial part of all digital solutions is the conversion between the two domains. Whether it is a digital-to-analog- or analog-to-digital conversion, some terminology used in, for example, [6][7] is needed to describe the process effectively.

Firstly, the smallest conversion step available in a n-bit conversion module is referred to as a Least Significant bit (LSB). One LSB is calculated:

$$1LSB = \frac{1}{2^n}[unitless] \tag{2}$$

A physical converter needs an analog value to represent the LSB. One option is to use a voltage V_{LSB}. V_{LSB} is defined as the smallest voltage step available in the conversion and is calculated by dividing the dynamic range by 2 to the power of n.

$$V_{LSB} = \frac{V_{max} - V_{min}}{2^n}[V] \tag{3}$$

Figure 2 show an analog and quantized signals. The quantized signal is converted to the digital domain by an Analog-To-Digital Converter (ADC), then converted back into the analog domain by a Digital-to-Analog Converter(DAC). It is visible that the quantized signal is moving along the grid lines, even though the analog signal moves between the lines. The reason for this is in the very nature of the two domains. The analog domain is what surrounds us in the real world.

An analog signal can have any value at any time. Therefore, it is continuous in time and amplitude. Digital signals are discrete in both time and amplitude. For this reason, the digital signal has only information about the analog signal limited to every T_S second. Additionally, the digital signal will have an error in the amplitude due to V_{LSB}; this is called Quantization error (V_Q). The Root Mean Square value of V_Q can be found:

$$V_{Q(rms)} = \frac{V_{LSB}}{\sqrt{12}} \tag{4}$$

Furthermore, the best theoretical Signal-to-Quantization noise ratio(SQNR) can be found:

$$SQNR = 6.02N + 1.76 \tag{5}$$

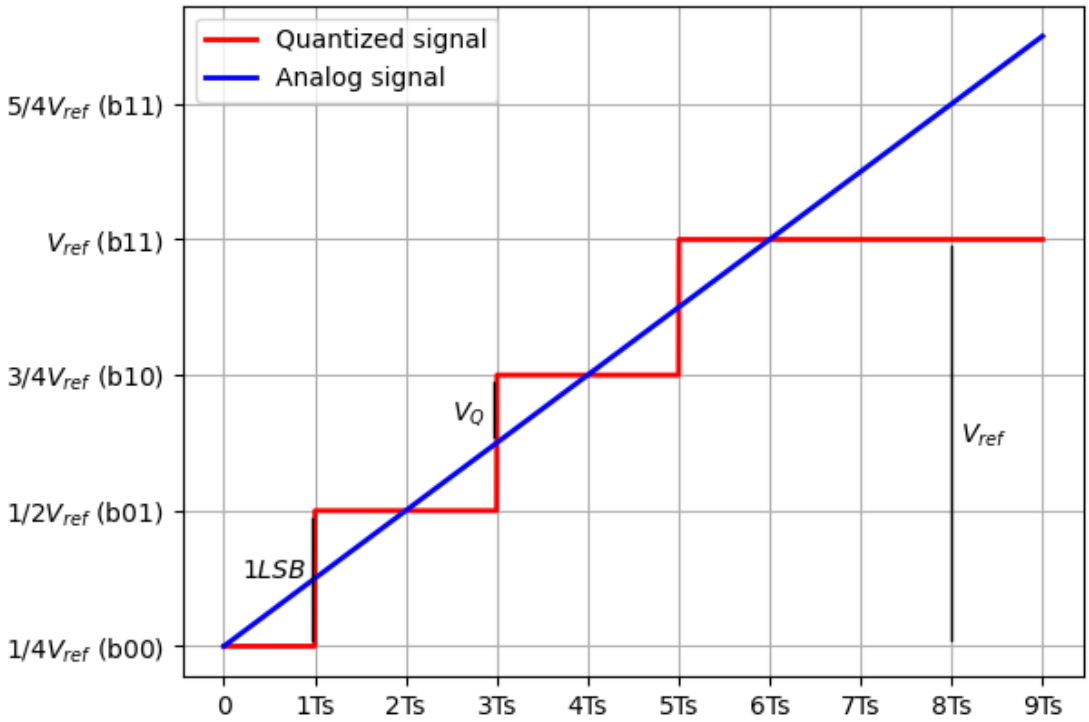


Figure 2: Analog and Quantized signal.

However, the real world has non-idealizes represented by ND for noise and distortion. A more including measure is Signal-to-Noise-and-Distortion (SNDR) ratio written as:

$$SNDR = SQNR - ND[dB] \tag{6}$$

Having defined SNDR, one can derive an equation for the Effective Number of Bit (ENOB). ENOB is a common measure for dynamic range in conversions. For ADCs, ENOB is found by inputting a single-tone sinusoid. After that, the output signal spectrum is inspected to find SNDR. Finally, the ENOB can be found using the equation:

$$ENOB = \frac{SNDR - 1.76}{6.02}[bit] \tag{7}$$

2.3 Successive Approximation

A popular ADC topology for reaching either quick conversion time or high accuracy is the Successive-Approximation Register (SAR) ADC[6]. The idea of a SAR ADC is to perform a binary search[8] by comparing the input voltage V_I to a known reference voltage.

Figure 3 shows a simplified top-level version of the single-ended SAR ADC. The Single-ended SAR ADC consists of a DAC, a comparator, and a SAR-and-control block.

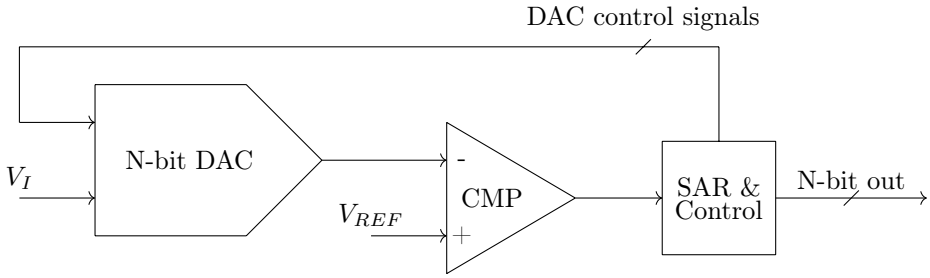


Figure 3: Single ended SAR ADC topology.

The DAC in figure 3 has two jobs. First, the input voltage V_I is sampled directly on the DAC. In order to do so, a Capacitive DAC (CDAC) can be used. Furthermore, the DAC adds the voltage V_{DAC} on top of V_I. In other words, the output of the DAC is:

$$DAC_{out} = V_I + V_{DAC} \tag{8}$$

As V_{DAC} is configurable within the DAC range, and V_{REF} is known, V_I can be found through a binary search by repeating the comparison:

$$V_I + V_{DAC} > V_{REF} \tag{9}$$

If the comparator deems the equation true, it gives a logical one. Otherwise, the comparator gives a logical zero. The result of every comparison is stored in the SAR and fed back through the control block.

Figure 4 shows a fully differential SAR ADC topology. The basic building blocks are the same as the single-ended, except for an extra DAC on the positive input of the comparator.

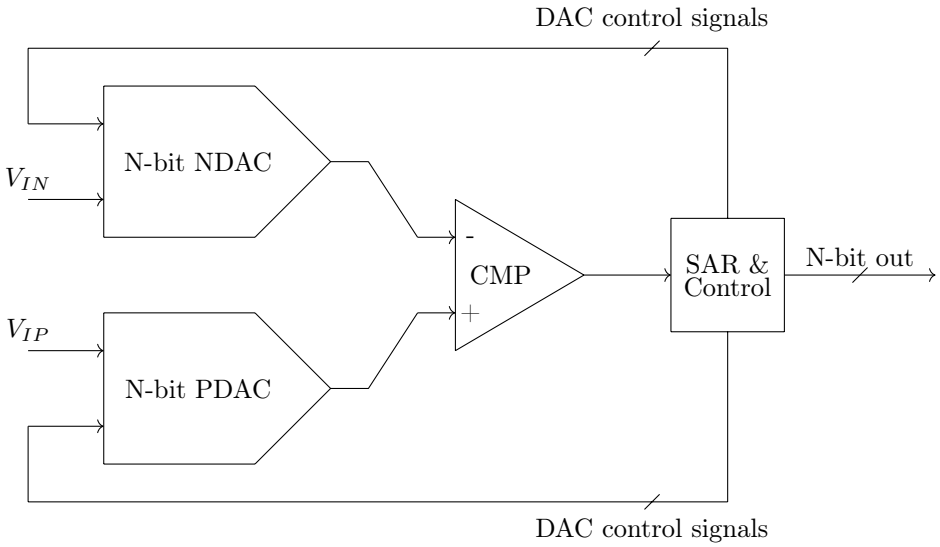


Figure 4: Fully differential SAR ADC topology.

The fully differential SAR ADC functionality is similar to the single-ended one. The SAR and Control block keeps track of the comparisons in a binary search. However, the differential SAR ADC does not compare V_I directly to V_{REF}. Instead, the two signals V_{IP} and V_{IN} are found, then summed. The following system of equations can be solved for V_{IP} and V_{IN}:

$$\begin{cases} V_{IP} = -V_{IN} \\ V_{IP} + V_{PDAC} > V_{IN} + V_{NDAC} \end{cases} \tag{10}$$

Also, in the fully differential SAR ADC V_{PDAC} and V_{NDAC} are controlled by the SAR and control block. Thus, the input signals are found by performing a binary search.

2.4 Charge redistribution

In order to perform a binary search using the DAC, V_{DAC} needs to be controlled. V_{DAC} is controlled by applying reference voltages on the outside of the capacitors in the DAC. Figure 5 displays three capacitors, C_1, C_2 and C_3 modeling a simplified DAC used to derive a general formula for ΔV_{out}. C_1 represent all capacitance connected to reference V_{ref1}, C_3 represent all capacitance connected to V_{ref2}, while C_2 represent all capacitance that are switched to the other reference.

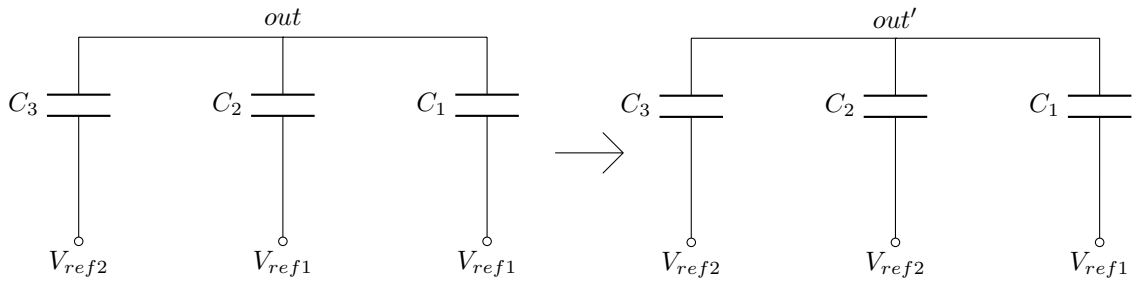


Figure 5: Example of charge redistribution.

The fundamental assumption for calculating the new voltage $V_{out'}$ is that no charge leaves *out*. Thus Q_{out} is the same as $Q_{out'}$. Therefore, the initial step is to derive an expression for the charge in each case, then bind them together by the conservation of charge:

$$\begin{aligned} Q_{out} &= Q_{out'} \\ Q_{out} &= C_3(V_{out} - V_{ref2}) + (C_2 + C_1)(V_{out} - V_{ref1}) \\ (C_3 + C_2)(V_{out'} - V_{ref2}) + C_1(V_{out'} - V_{ref1}) &= Q_{out'} \\ (C_3 + C_2)(V_{out'} - V_{ref2}) + C_1(V_{out'} - V_{ref1}) &= C_3(V_{out} - V_{ref2}) + (C_2 + C_1)(V_{out} - V_{ref1}) \end{aligned} \tag{11}$$

Denoting C_2 as $C_{switched}$ and the total capacitance as C_{tot} a solution for $V_{out'}$ can be found to be:

$$V_{out'} = V_{out} + \frac{C_{switched}}{C_{tot}}(V_{ref2} - V_{ref1}) \tag{12}$$

Thus, a general solution for ΔV_{out} is:

$$\Delta V_{out} = \frac{C_{switched}}{C_{tot}}(V_{ref2} - V_{ref1}) \tag{13}$$

2.5 Noise

The main contributors to noise in Meta-Oxide-Semiconductor-Field-Effect-Transistors (MOSFET) are thermal- and flicker noise[6].

Thermal noise occurs as a random motion of charge carriers in all resistive materials. Therefore, it is modeled as a root mean square (RMS) current source parallel to the resistor. The current source is present at all frequencies with an amplitude of kT. Boltzmann's constant is presented as k, and T is temperature Kelvin.

Flicker noise occurs as charge carriers get trapped and released, for example, in a MOSFET channel. For MOSFETs, flicker noise is modeled as an RMS voltage source on the gate. Flicker noise is most present at low frequencies, decreasing at a linear rate with higher frequencies.

2.6 Bootstrapping

An issue with using pass transistors or transmission gates[7] as analog switches is that the on-resistance depends on the gate-source voltage. In analog circuits, the source voltage is not always static. One solution is bootstrapping, a technique where the gate is moved together with the source instead of keeping a static source voltage. Ideally, this will decrease non-linearity in the analog switch[9].

Figure 6 shows a conceptual bootstrapped switch while in the "off"-state. The gate of the switch Negative-Channel Metal-Oxide-Semiconductor (NMOS), M_1 is connected to ground, keeping it shut. Meanwhile, the capacitor C_1 is charged to the desired gate-source voltage. For the main switch to turn on, Sw_1, Sw_2, and Sw_3 are flipped. The negative side of C_1 is connected to the input voltage and the positive side of C_1 to the gate of M_1. Therefore, the gate-source voltage will always be close to $V_{dd} - V_{ground}$.

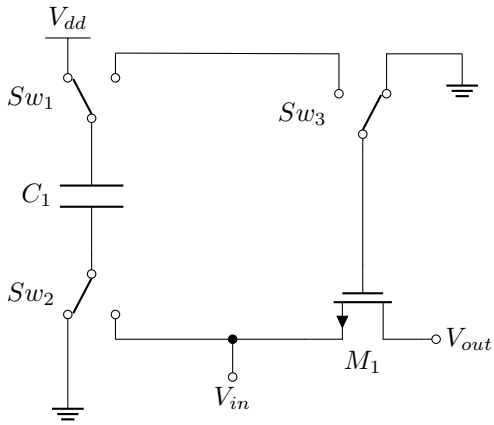


Figure 6: Conceptual bootstraped switch.

2.7 Static- and dynamic power consumption

In static CMOS circuits such as digital circuitry, power dissipation can be arranged into two groups: static and dynamic power[7]:

$$P_{total} = P_{static} + P_{dynamic} \tag{14}$$

The static power consumption comes from the finite "off"-resistance through a transistor. Therefore, static power consumption is highly affected by the technology node. Dynamic power dissipation has two main contributors: Charging and discharging capacitance and rail-to-rail connection in transition between states. Unless additional load capacitance is added, the first originates from the transistors' intrinsic capacitance, which depends on the technology node. The latter is more sensitive to poor design choices. Therefore, assuming a good topology has little rail-to-rail connection through open transistors, P_{static} and charging intrinsic capacitance are the main contributors. A way to get a feel for the power dissipation in digital circuits is by counting transistors and branches of current.

3 High-level design and design choices

This section presents choices made on a high level. These are choices made prior to the implementation. The design choices are made by logical thinking, studying previous work, or simulating single parts. As the main goal for this thesis is reaching ultra-low-power consumption, this is also the main concern through this section.

3.1 Comparator

The strongarm latch[10] is a popular comparator topology for Successive-Approximation-Register (SAR) Analog-To-Digital Converters (ADC) due to its low static power consumption, clean rail output and simple design [11][12][13][14]. A strongarm latch with Negative-Channel Metal-Oxide-Semiconductor (NMOS) input stage is described in [15]. In short, the strongarm latch is made up of a latch with a pair of common source transistors disconnecting it from one of the rails. These common source transistors function as input transistors. The input transistors are connected to the rail through a tail transistor clocked by a reset signal. Finally, a reset switch is added to all those nodes in the latch not already connected to the rail. Its functionality can be divided into three phases:

- The comparator is idle, waiting for the reset signal to switch.
- The reset signal switching initiates the amplification phase. The two common source transistors will race to flip their side of the latch to the opposite rail.
- The last phase is where the comparator makes its decision. One of the outputs will switch rail while the other is forced back to where it was.

When asynchronous functionality is desired in an ADC using the strongarm latch, it is common practice to utilize these phases. Adding a logic port to the output of the comparator to signal whether the comparator is in the second or third phase. Adding a delay to this signal before feeding it back to reset the strongarm latch generates a self-driven clock with the strongarm latch in its core.

3.2 Standard components

In order to simplify the layout, some standard components are chosen and reused. Most transistors are implemented with a length of $28\mu m$ as this is the shortest length available for all transistors.

Digital circuitry is implemented with the highest threshold devices; the unit transistor is $200nm$ wide. Furthermore, a unit capacitor is created and multiplied in parallel to create a larger capacitance. The unit capacitor is created in the fourth metal layer to minimize parasitic capacitance to the substrate. The capacitor is drawn using two non-connected metal strips in a fork-like pattern. The fork pattern maximizes the adjacent area between two metal strips as shown in figure 7[16]. The unit capacitor is $1.327\mu m$ wide and $0.854\mu m$ long and has a capacitance of $1.15fF$. One disadvantage of implementing a custom capacitor is that it lacks a corner and mismatch model. The only capacitance simulated is the capacitance between the metal strips and the parasitic capacitance to the substrate.

Figure 7: Unit capacitor

3.3 Timing circuitry

Correct timing is essential for all the SAR ADC components to work appropriately together. Therefore, delay circuitry will be added to the system. One way to create a short delay is by adding inverters or conventional buffers consisting of an even number of cascade inverters. However, when creating a delay of several microseconds, the amount of inverters needed becomes inconvenient. Another way to implement a longer delay is by adding a current-starved buffer[17] as shown in figure 8.

Instead of using long strings of inverters, one single current starved buffer can create long delays. R_{starve} can be implemented with one or more transistors. Therefore, one advantage of the current starved buffer is the area saved by avoiding several inverters. However, the technology has little static power consumption through branches with at least one closed transistor. Thus, the power consumption should be lower through the two branches of the current starved buffer than through the long string of conventional buffers.

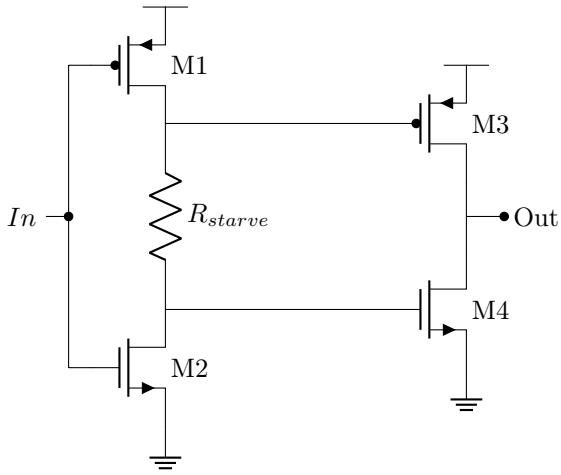


Figure 8: Current starved buffer delay circuitry.

3.4 Digital building blocks

Conventional complimentary NANDs, NORs, and inverters are used for the digital circuitry[7]. However, two possible Data Flip-Flops (DFF) are considered. Figure 9 shows a conventional DFF, built by logical gates. This DFF is made up of four NAND gates and an inverter. The conventional DFF consists of 18 transistors spread over five branches of current.

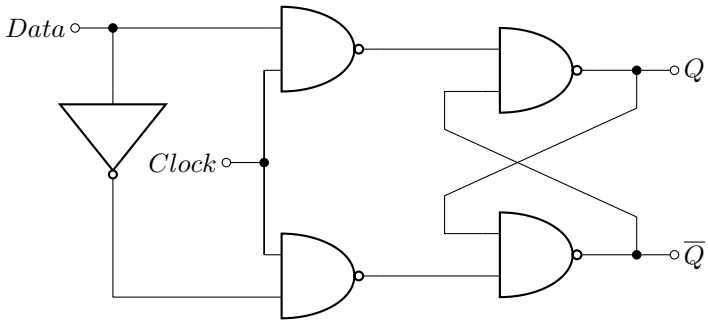


Figure 9: Conventional DFF.

A second DFF topology is the tri-state-inverter-based DFF displayed in figure 10 [18]. This DFF comprises two clocked tri-state inverters, also described in [7], separated by a normal inverter. Finally, an additional inverter makes an inverted clock signal. The tri-state-inverter-based DFF consists of 12 transistors spread over four branches of current. Furthermore, the DFF can be

modified to have an asynchronous set or reset with an extra transistor on Q and $\overline{Q}$.

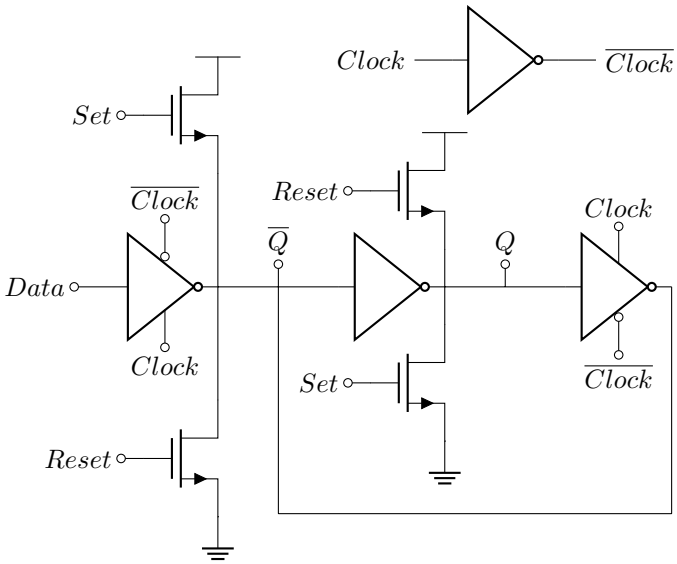


Figure 10: Tri-state inverter based DFF.

In order to choose a unit DFF, the two alternatives are tested over all corners pre-layout. Power consumption is the sole concern as the DFFs will not be challenged on speed. The simulations suggest the inverter-based DFF use between 60% and 70% power compared to the conventional DFF, depending on the corner. See appendix for the test bench and raw results.

3.5 Digital-to-Analog Converter

An essential part of the SAR ADC is the Digital-To-Analog Converter (DAC). First of all, if the DAC is not accurate enough, it will directly affect the accuracy of the ADC. Furthermore, the DAC is bound to be one of the major power consumers. Therefore, great care should be taken when choosing the DAC for a specific ADC. Regarding SAR ADCs, binary scaled Capacitive DAC (CDAC) is the most popular. The input can be sampled directly onto the capacitors in the DAC, and the binary scaled capacitors can be switched to different references as shown in 2.3 to perform a binary search.

Much of the power dissipated through the DAC is through charge redistribution. Designers are therefore creative in finding ways to minimize the capacitance needed, lower the reference voltage, or both. The conventional SAR ADC is fully differential and is presented in [6]. The total

capacitance in the DAC is $2^n C_{unit}$ to create an n-bit DAC. C_{unit} is the smallest capacitance in the DAC. [13] presents a monotonic switching scheme that requires $2^{n-1}C_{unit}$, potentially removing half of the total capacitance in the DAC. Removing half of the capacitance is enabled by sampling the input inside the DAC, making the first comparison before switching any capacitors. The energy dissipation is further reduced by switching capacitors in only one of the DACs for every output bit found. Contrary to the conventional SAR switching scheme, a switched capacitor is never switched twice. The major downside to monotonic switching schemes is that the input common-mode for the comparator is changing. However, the monotonic switching scheme, and variations of it is popular[13][14][11][12].

Another way to reduce the power dissipated in the DAC is by reducing the charge moved. 2.4 shows that the voltage change across the capacitors in the DAC is linearly related to the difference between the switched references. [1] takes advantage of this by introducing a third reference V_{cm}. Instead of switching the capacitors from rail to rail, the capacitors are charged to the middle. The upper rail is connected to increase the DAC voltage, while the lower reference is used to lower the DAC voltage. In either case, the voltage change over the capacitors is half that of the monotonic and conventional switching scheme. Like the monotonic switching scheme, the switching scheme uses $2^{n-1}C_{unit}$ while having the advantage of a stable common-mode voltage. On the other hand, an additional implemented reference with more digital circuitry is needed for the ADC to work. Finally, to charge the inside of the DAC to V_{cm} with any input voltage on the outside, the analog switch needs the ability to drive both large positive and negative currents. Additionally, the switch must have a high "off"-resistance for the DAC not to leak. A final consideration is a mix between monotonic and V_{cm} switching as presented in [19].

As the goal is to minimize the power consumption, this is also the main consideration in choosing a switching scheme. [13] estimates that the conventional switching scheme consumes $1365.5C_{unit}Vref$ and the monotonic switching scheme consumes $255.5C_{unit}V_{ref}$ for a $10bit$ ADC. [1] estimates that the V_{cm} switching scheme uses $63.75C_{unit}V_{ref}$ for a $10bit$ ADC. However, the V_{cm} switching scheme proposed in [1] uses only a single DAC. A fully differential V_{cm} topology as shown in figure 11 has a estimated power consumption of $127.5C_{unit}V_{ref}$

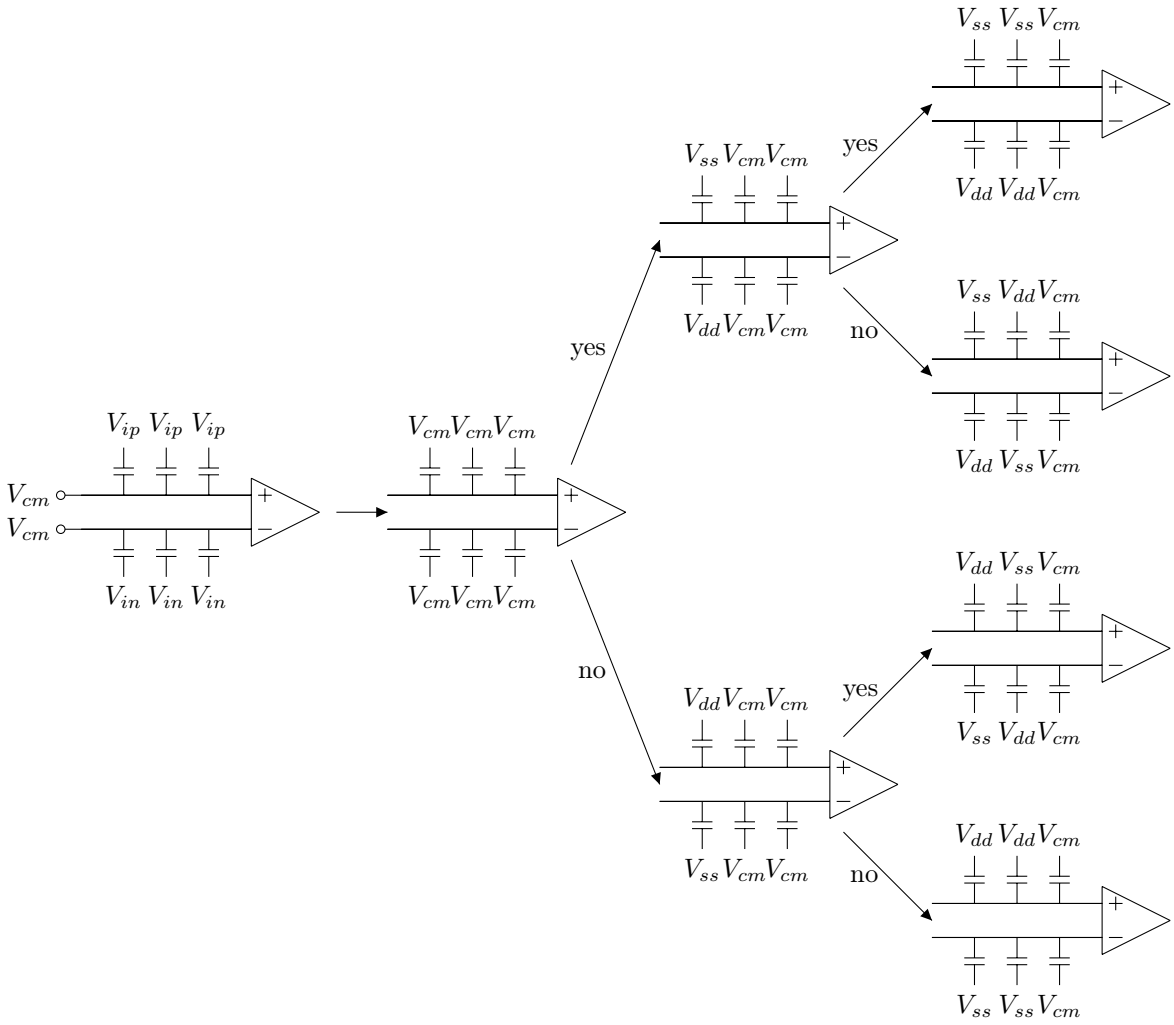


Figure 11: CDAC switching scheme based on [1]

3.6 ADC flow table

Table 3 is a pseudo code of the SAR ADC in the shape of a table. The first column describes different events in the two clocks, and column two describes reactions in the digital circuitry and comparator at the different clock events. Finally, the third column combines figure 11 with columns one and two. The pseudo-code describes only the first cycle of the internal clock as the successive cycles are assumed self-explanatory.

Table 3: Flow table.

Events	**Reactions: Digital & Comparator**	**Reactions: DACs**
Clk_{sample} low	Idle.	Idle.
Clk_{sample} rising	(Optional: read output register)	Open sample switch and inside V_{cm} switch.
Clk_{sample} high	-	Charge DACs to $V_{cm} - V_i$
Clk_{sample} falling edge	Set iteration counter, Initiate internal clock.	Close inside V_{cm} switch, Close V_i switch, Connect outside of DAC to V_{cm}.
$Clk_{internal}$ low	Comparator compares DAC outputs (decision is latched)	-
$Clk_{internal}$ rising	Counter MSB goes low, Comparator is reset.	Outside of DACs switched from V_{cm} to V_{ref1} or V_{ref2} depending on first comparison
$Clk_{internal}$ high	-	DACs are being charged to new voltage.
$Clk_{internal}$ falling	Write latched comparator result to MSB in output register.	-
Internal clock is low	Comparator compares new DAC outputs (decision is latched)	-
Repeat until counter LSB goes low marking last cycle.		

4 Implementation

This section describes the Successive-Approximation-Register (SAR) Analog-To-Digital Converter (ADC) as it is implemented. First a top level implementation is described, before each building block is described in detail. For exact widths and lengths of all transistors see appendix.

4.1 Top level Design

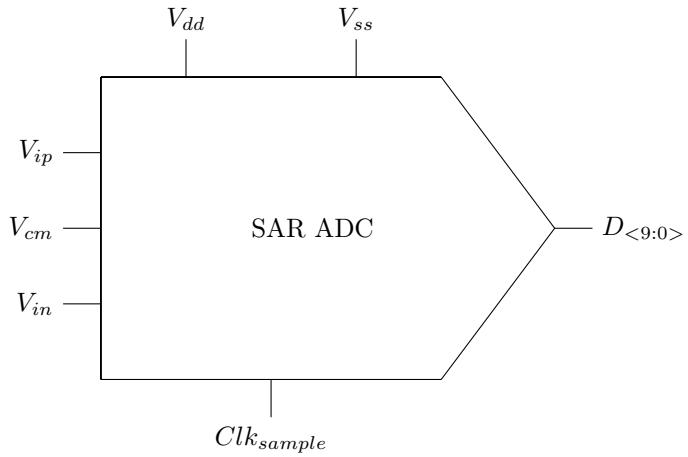


Figure 12: ADC top level symbol.

Table 5: ADC top level symbol pin description.

V_{ip}	Input - Positive input signal $0 - 400mV$.
V_{cm}	Input - Reference voltage at $200mV$.
V_{in}	Input - Negative input signal $0 - 400mV$ ($V_{in} = V_{dd} - V_{ip}$).
V_{dd}	Power supply - $400mV$.
V_{ss}	Ground.
Clk_{sample}	Input - Active high, frequency $1kHz$, pulse width = $\frac{0.1}{1k}$.
$D_{<9:0>}$	Output - $10bit$ register containing quantized measurement.

Figure 12 together with table 5 shows a symbol with the SAR ADC's in- and output pins. These are the signals any user of the ADC would have to take into consideration. Furthermore, figure 13 shows the top level topology of the SAR ADC. External signal connections are marked with a "o" termination.

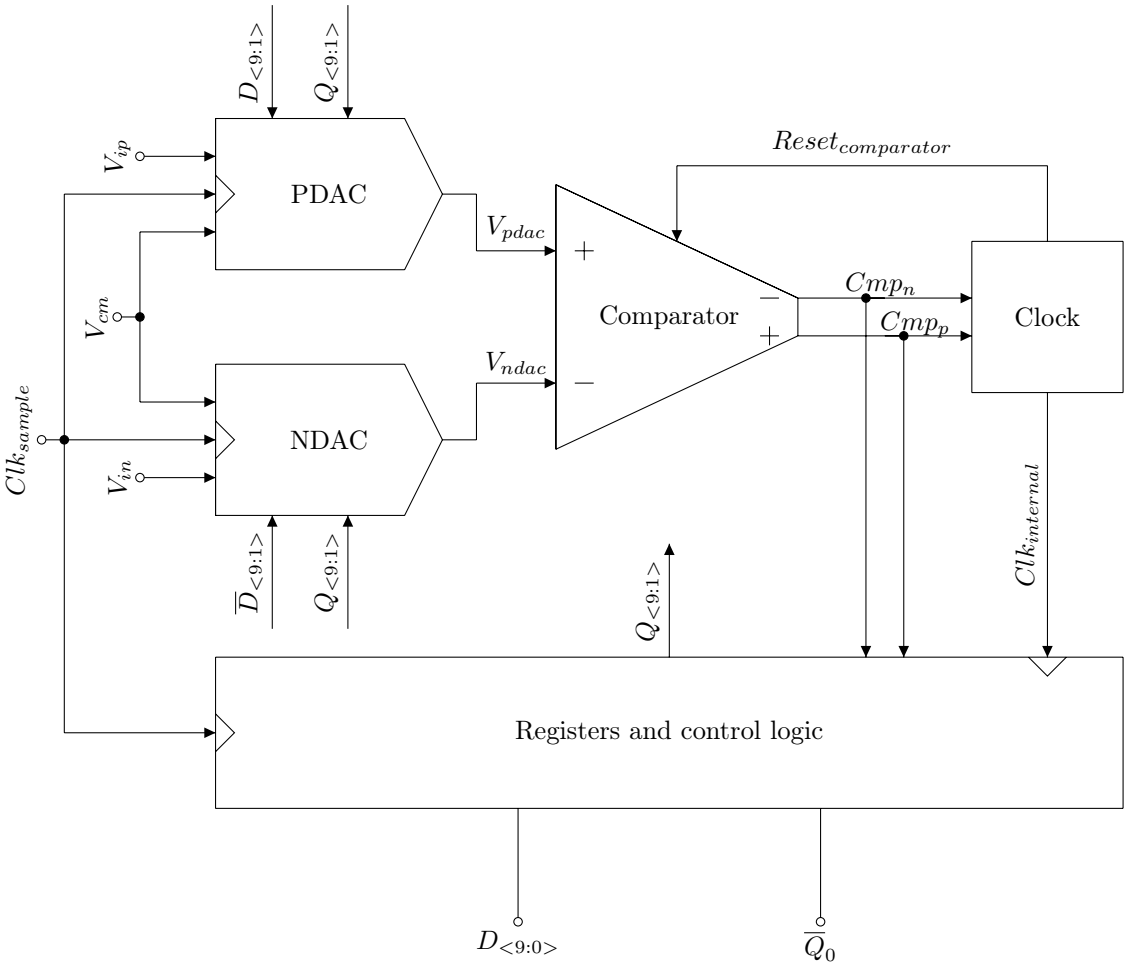


Figure 13: SAR ADC top level design.

The internal top-level design consists of five blocks. First, the comparator has two roles: to compare the two signals V_{pdac} and V_{pdac}, and to initiate the clock signal. The second block is the internal clock. As the ADC has asynchronous functionality, the internal clock is the core of internal timing. Its job is to clock the digital block and reset the comparator. The third block is the registers

and control logic. This block has two purposes: Store the result of every comparison made by the comparator and feed the comparison together with an iteration count back into the Digital-To-Analog Converters (DAC). Finally, the two DACs make up the fourth and fifth blocks. The DACs have two purposes: The signals V_{ip} and V_{in} are sampled directly onto the DACs. Secondly, the DACs add a digitally controlled voltage on top of the input signals to perform the binary search as described in 2.3.

4.2 Comparator

The implemented comparator is a strongarm latch as described in 3.1. The implemented topology is the same as [15] but with Positive-Channel Metal-Oxide-Semiconductor (PMOS) input stage as shown in figure 14.

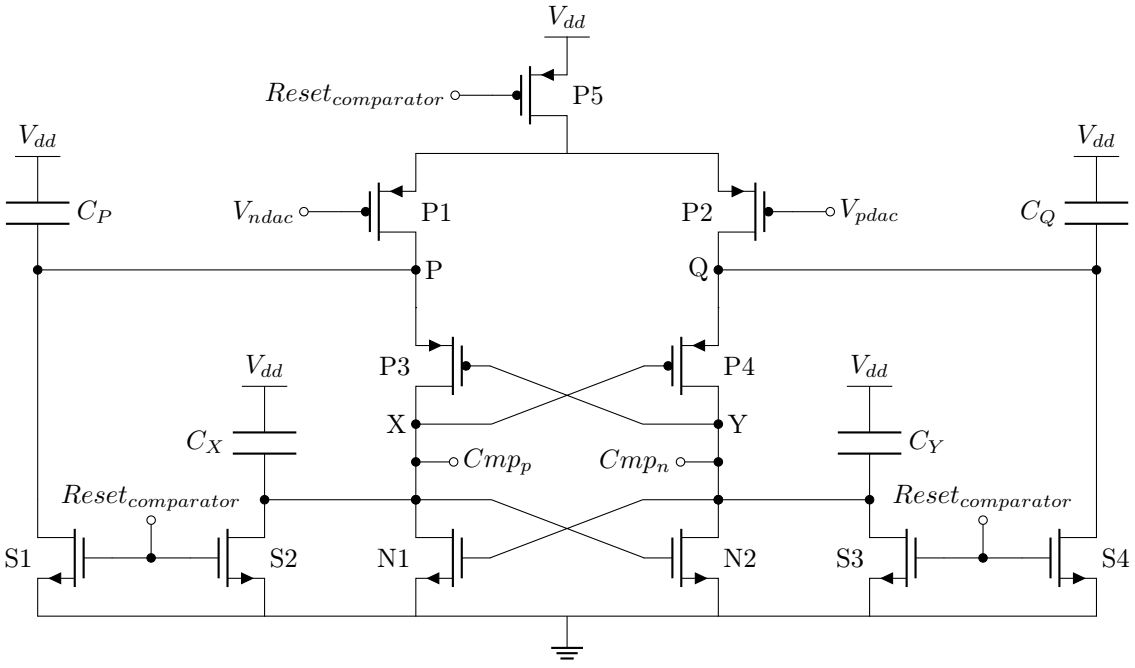


Figure 14: Strong arm latch with PMOS input stage.

The dynamic nature of the strongarm latch is a two-sided coin. On one side, the low static power consumption helps minimize the power consumption. Conversely, the need for clocking makes operation point analysis hard. The design process used in this thesis is mainly inspired by the design equations presented in [15]. The current drives the speed of the comparator passed through

P_5. Meanwhile, it is slowed down by the capacitance on P and Q and the threshold of the latch. The input-referred noise is driven by the gate-source voltage of P_1 and P_2. Meanwhile, it is lowered by their threshold and the capacitance in nodes P and Q. As the operation of the comparator is relatively slow, most effort is put into lowering the input-referred noise.

Initially, the comparator was implemented using very high threshold input devices and a slightly lower threshold for the rest of the devices. Furthermore, the capacitance of X, Y, P, and Q were made as large as possible within the sampling frequency. Meanwhile, $P5$ is implemented with a high threshold. The width of $P5$ was optimized for the performance of the entire ADC [4]. A second version using similar latch transistors but changing the flavor of the input transistor to the same as the latches gives the same accuracy with less load capacitance. By simulation, C_X and C_Y are chosen to be half the size of C_P and C_Q, which are 46 unit capacitors. The reset switches $S_1 - S_4$ are implemented with the highest threshold devices. Finally, buffers are added to drive the outputs. The exact sizes can be found in the appendix.

The layout of the comparator is shown in figure 15. The total width of the comparator is $5.612\mu m$, and the length is $5.601\mu m$. The figure shows P_4 and P_3 at the bottom, marked in gray. P_3 transistors are marked with a yellow color over the gray to show the transistors are placed in every second pattern. The same pattern is shown for N_2 and N_1 marked by pink. The transistors are placed in the following pattern from top to bottom: Negative-Channel Metal-Oxide-Semiconductor (NMOS), V_{ss}, substrate bulk connection, NMOS, PMOS, V_{dd} N-Well bulk connection, PMOS, and then repeat. As a result, as many transistors as possible can share bulk contacts, especially for PMOSes, where transistors can share the same well. Furthermore, P_5 is split into two locations to fill the space around the V_{dd} bulk connection to the N-Well around P_4 and P_3. The input PMOSes P_1 and P_2 are placed to the right in the figure. They are laid out in a common centroid pattern[20] to minimize the mismatch effect. Finally, the input transistors are placed in their N-Well with a guard ring around the well. Doing so ensures that P_1 and P_2 see the same in all directions and minimizes the Well-Proximity-Effect(WPE). Great care is also taken not to add metal strips above any transistors to avoid injuring them after they are produced. The Comparator layout has passed both Design Rule Check (DRC) and Layout Versus Schematic (LVS).

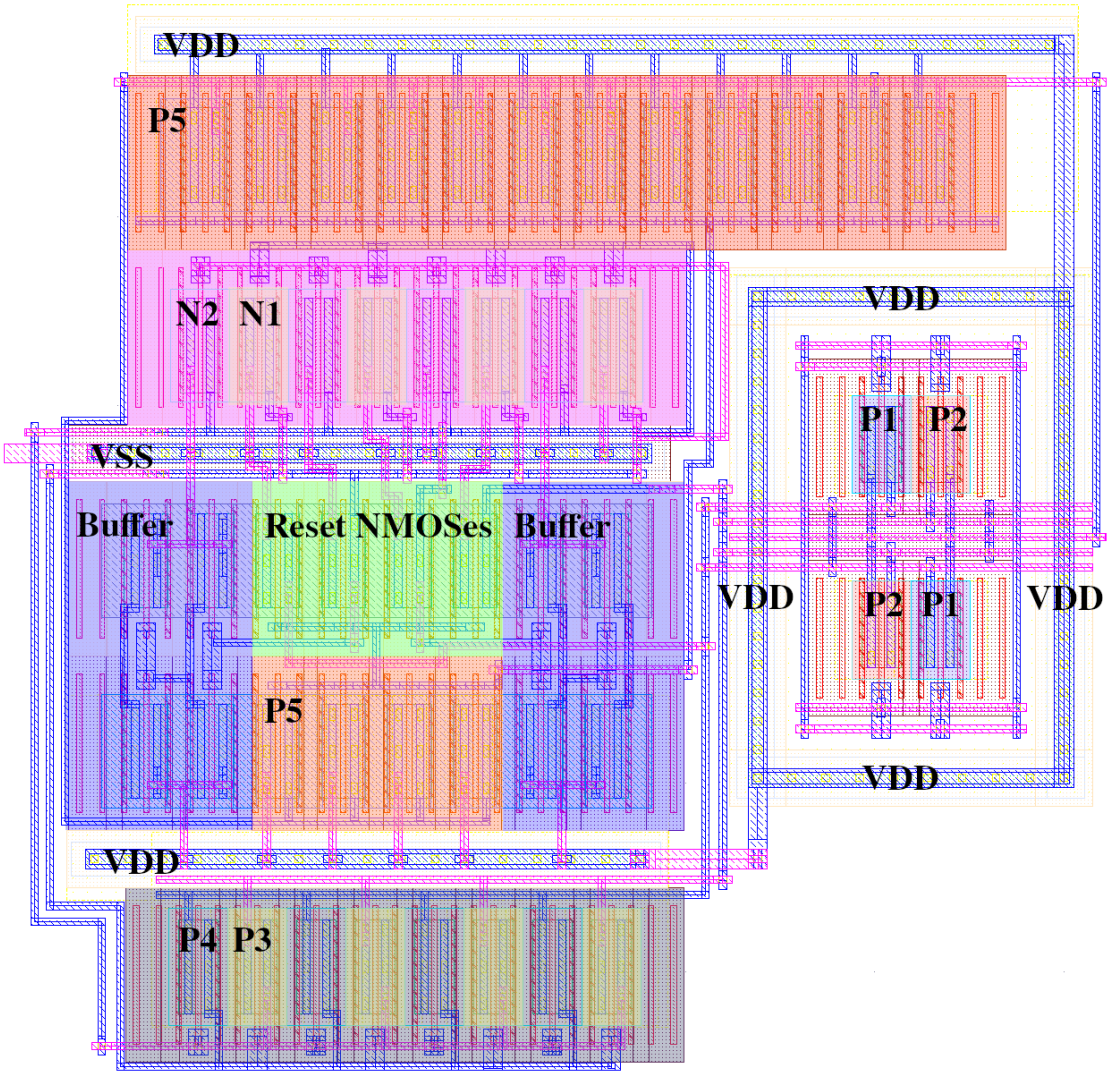


Figure 15: Strongarm latch layout.

4.3 Clock circuitry

The clock circuitry is shown in figure 16. It consists of three NOR gates, an inverter, and a delay block. I_2 is added to enable the clock circuitry. When the external sample clock has a falling edge, the counter will be reset, making $\overline{Q}_0$ go low. The circuit will wait for one delay before the comparator reset goes low. The comparator will eventually make a decision putting Cmp_n and

Cmp_p to opposite rail and Cmp_{ready} goes low. As both $Reset_{comparator}$ and Cmp_{ready} is low, $Clk_{internal}$ will go high. A logical low on the output of I_2 will be delayed before the comparator will be reset, and $Clk_{internal}$ goes low. The pattern repeats until the counter reaches the end, and $\overline{Q}_0$ disables the clock circuitry.

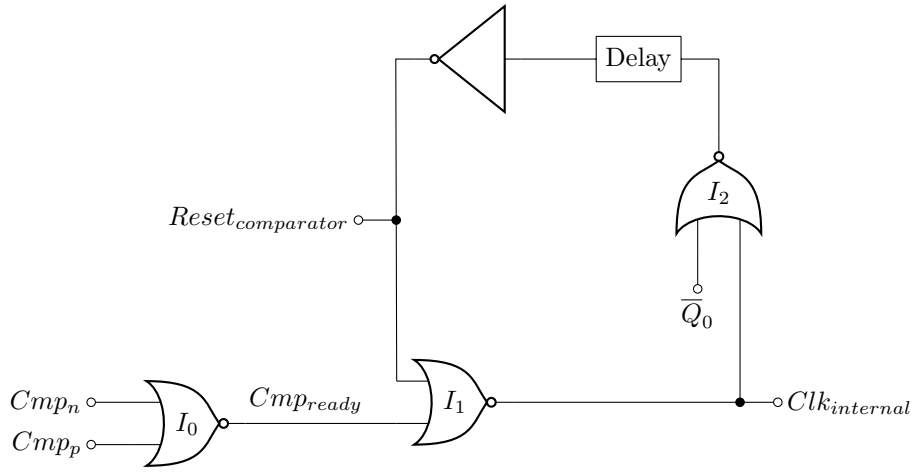


Figure 16: Clock circuit schematics.

The NOR gates and inverter are built using unit-size transistors, while the delay is tuned to about $15\mu s$. The clock circuit is not laid out; however, an area estimation can be made. The gates are $1.51\mu m$ wide, and three NORs plus one inverter would be $1.317\mu m$ long, assuming they share active. Not all transistors can share active, so the length is rounded up to $1.5\mu m$. The delay is $1.3\mu m$ wide and $1.3\mu m$ long.

Additionally, bulk contacts would need to be created, which would be $0.3\mu m$ wide. The same pattern for P- and NMOS as in the comparator would be used. The PMOSes would be placed towards each other with a shared N-Well bulk contact. The NMOSes with their bulk contacts would be placed outside the PMOSes. In total, there would be three bulk contacts. An estimated area can therefore be made to be:

$$\begin{aligned} Width &= 1.51\mu m + 1.3\mu m + 3 * 0.3\mu m = 3.71\mu m \\ Length &= 1.5\mu m \end{aligned} \tag{15}$$

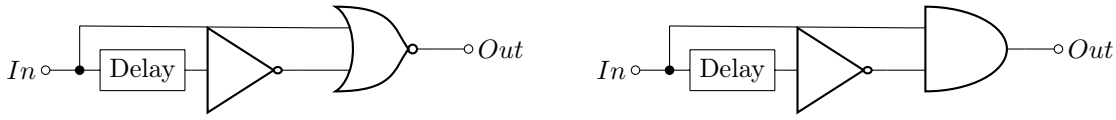
4.4 Digital Circuitry

The digital circuitry consists of two 10*bit* registers and the logic to give them proper functionality. The first register is a ripple counter, which keeps track of the iteration index. The other register stores the result of each comparison after the comparator has made a decision.

4.5 Edge detectors

Figure 17 shows support circuitry to create rising and falling edge signals. 17b is a falling edge detector. The NOR will give a high output when the inputs are low. However, the inverter tries to prevent this in all cases except when the inverter input is precharged to V_{dd} and the input goes low. In this case, the delay would keep the inverter input charged to V_{dd}. Thus, letting both NOR inputs low and create a high output for the duration of the delay. 17b is a rising edge detector; the principle is the same as for the falling edge detector. However, the rising edge detector uses an AND gate instead of the NOR. Therefore, the input of the inverter needs to be precharged to the ground while the input goes high.

Finally, a note on notation through this section: a signal noted as an over-lined edge is an edge signal inverted. For example, $\overline{Clk}_{sample-rising}$ is equivalent to the rising edge of Clk_{sample} ran through an inverter, not to be confused with the rising edge of $\overline{Clk}_{sample}$.



(a) Falling. (b) Rising.

Figure 17: Edge detectors.

4.6 Iteration counter

Figure 18 displays a compressed schematic representation of the iteration counter. A falling edge on Clk_{sample} initiates the iteration counter. $Q_{<9:0>}$ will be set to a logical high activating the clock circuitry. Every time $\overline{Clk}_{internal}$ has a falling edge, one of the NOR gates will generate a clock signal for their Data Flip-Flop (DFF). In addition to the falling edge of $\overline{Clk}_{internal}$, the NOR has two more inputs: First, the input is connected to Q_{n+1}; this makes sure that the DFF will not go low before the one to its left. The last input is connected to the negative output of the same

DFF to avoid oscillations. Except for the Most Significant Bit (MSB) DFF, all DFFs have a delay added to their input. Thus, no two DFFs will flip on the same rising edge $\overline{Clk}_{internal}$. The MSB DFF has the input connected to ground, starting the ripple effect. It is logically possible to use a two-input NOR for the MSB. However, it is implemented with a three-input NOR to ensure that Clk_9 is the same as the other DFF clocks. The leftover input of the NOR is connected to ground.

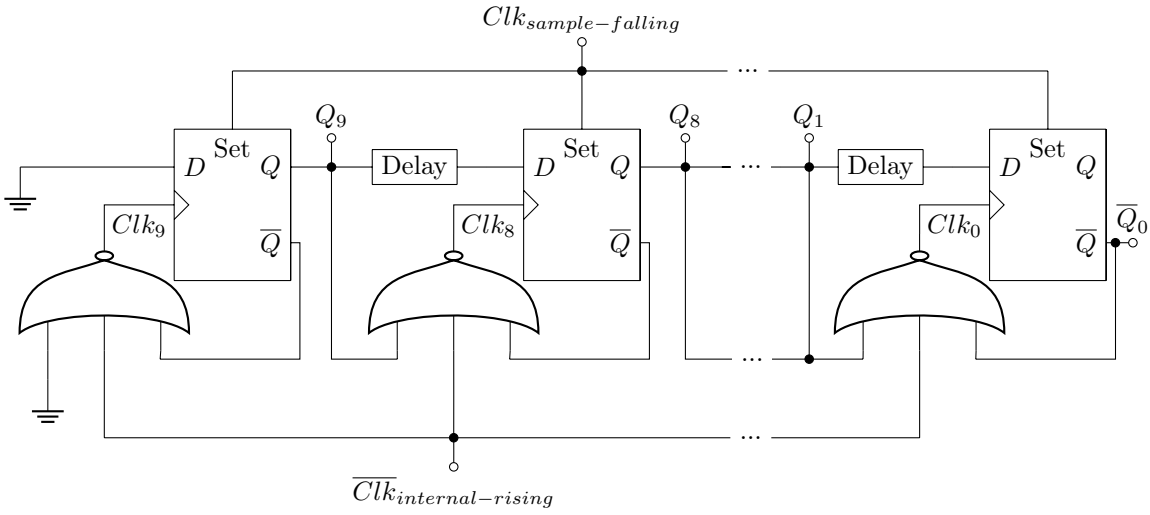


Figure 18: Iteration counter.

The NOR gates are implemented as conventional three input complimentary NOR gates as described in [7]. The transistors in the NORs are flavored with the highest possible threshold voltage, using minimal length and $300nm$ width. The delay is generated with all unit-sized transistors to minimize area. The DFFs used are the tri-state inverter-based DFF described in 3.4 with the set transistors added. The reset transistors are neglected as no reset is needed. The transistors are implemented with the highest threshold flavor, shortest length, and $300nm$ width.

Figure 19 show parts of the iteration counter layout. DFF_6 to DFF_0 are neglected as the pattern for the displayed DFFs repeat. Digital circuitry is not as affected by mismatch as some analog transistors. Therefore, as many digital transistors as possible share active to minimize area. Furthermore, no matching techniques are used on any transistors.

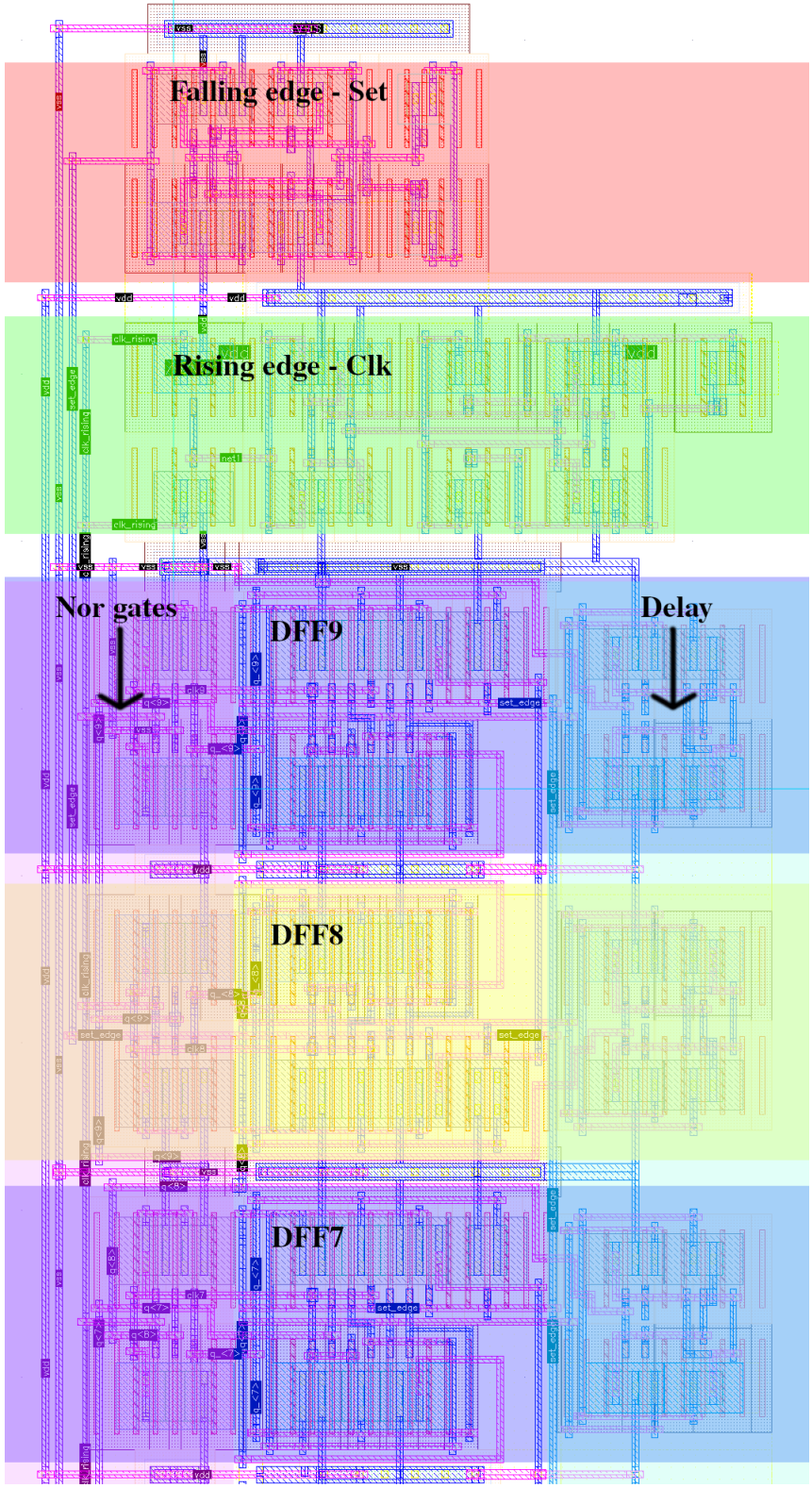


Figure 19: Iteration counter layout.

At the top of the layout marked with red is the falling edge detector connected to Clk_{sample}. This is the edge detector used to generate the falling edge set signal. Excluding the bulk contact, the falling edge detector is $1.31\mu m$ wide and $2.168\mu m$ long. Marked in green is the rising edge detector generating $\overline{Clk}_{internal-rising}$. It is $1.31\mu m$ wide and $3.856\mu m$ long. At the bottom, marked with blue and yellow, are the DFFs. DFF_9 and DFF_7 are marked in blue. Likewise, DFF_8 is marked in yellow. The different colors indicate that DFF_9 and DFF_7 are laid out with the NMOSes on top, while DFF_8 is laid out with the PMOSes. As explained in 4.2 this is to save space on bulk contacts. The same goes for the delay blocks in cyan and green and the NOR gates in purple and orange. One DFF with the delay and NOR gate is $1.51\mu m$ wide and $4.092\mu m$ long. Including routing, the entire iteration counter has passed DRC but has an unknown missing connection to V_{ss}. Thus it can not pass the LVS check and is valid only for area estimation. The total width of the iteration counter is $21.667\mu m$, and the length is $4.382\mu m$.

4.7 Output register

Figure 20 shows a compressed schematic representation of the output register. The registers are being written the same way as the iteration counter. However, the register is never set nor reset. Furthermore, the data is written on a falling edge, as Cmp_{ready} produces the low clock, which indicates that the comparator has made a decision. The other NOR gate inputs come from Q_n and $\overline{Q}_{n-1}$, ensuring that only the correct DFF is being written. The input of the DFFs is the positive output of a conventional SR latch as described in [7].

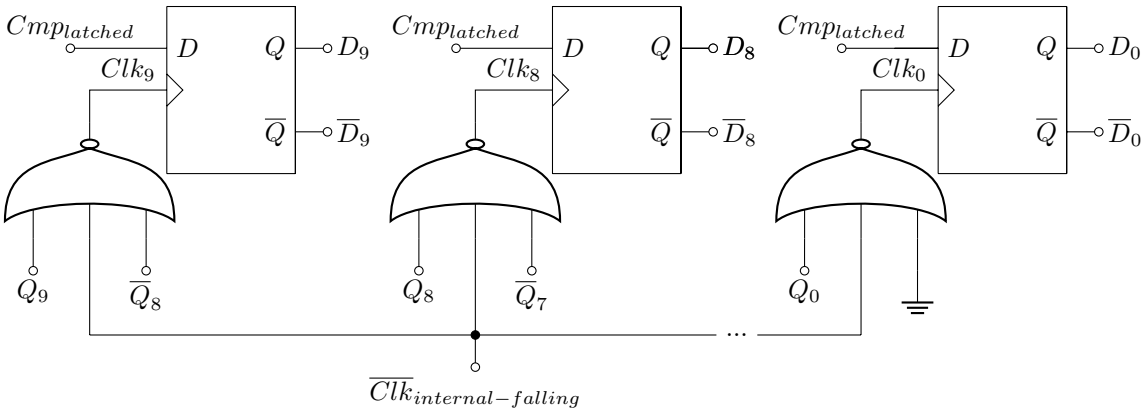


Figure 20: Output register.

The latch is fed by the comparator's outputs, ensuring the output is kept ready for the entire internal clock period, even after the comparator is reset.

No layout is made for the output register in its entirety. However, the DFFs are about the same size as those used in the iteration counter. Therefore, the iteration counter can be used as a template to measure an estimated size for the output register. There are no delay blocks in the output register. Furthermore, only one falling edge detector is used. Thus, one can assume the output register is $20.357\mu m$ wide and $3.067\mu m$ long.

4.8 Capacitive Digital-to-Analog Converter

The DAC will be presented in two parts: first, the switches used to implement the switching scheme, then the capacitor array.

4.8.1 DAC switches

Figure 21 shows the switches used to implement the DAC switching scheme. While Clk_{sample} is high, the transmission gate made up by P_1 and N_1 is closed, and the input is sampled through the bootstrapped switch shown in figure 22. The bootstrapping technique explained in 2.6 increases the linearity of the switch resistance as the input is not a fixed DC voltage. When Clk_{sample} goes low, the bootstrapped switch is shut close, and the $P_1 - N_1$ transmission gate is opened.

The V_{cm} transmission gate is opened slightly later by Φ driven low and $\overline{\phi}$ driven high, reducing the effect of charge injection. Finally, the iteration counter signal goes low, and the tri-state inverter opens. More or less, simultaneously with the tri-state inverter opening, the V_{cm} transmission gate is shut close. The inverting nature of the tri-state inverter is used to precharge the tri-state inverter to V_{dd} or V_{ss} depending on D_n from the output register. The digital gates are implemented using digital unit transistors, while the N_1, N_2, P_1, P_2 and the tri-state inverter are implemented with highest threshold flavor with $1.3\mu m$ width.

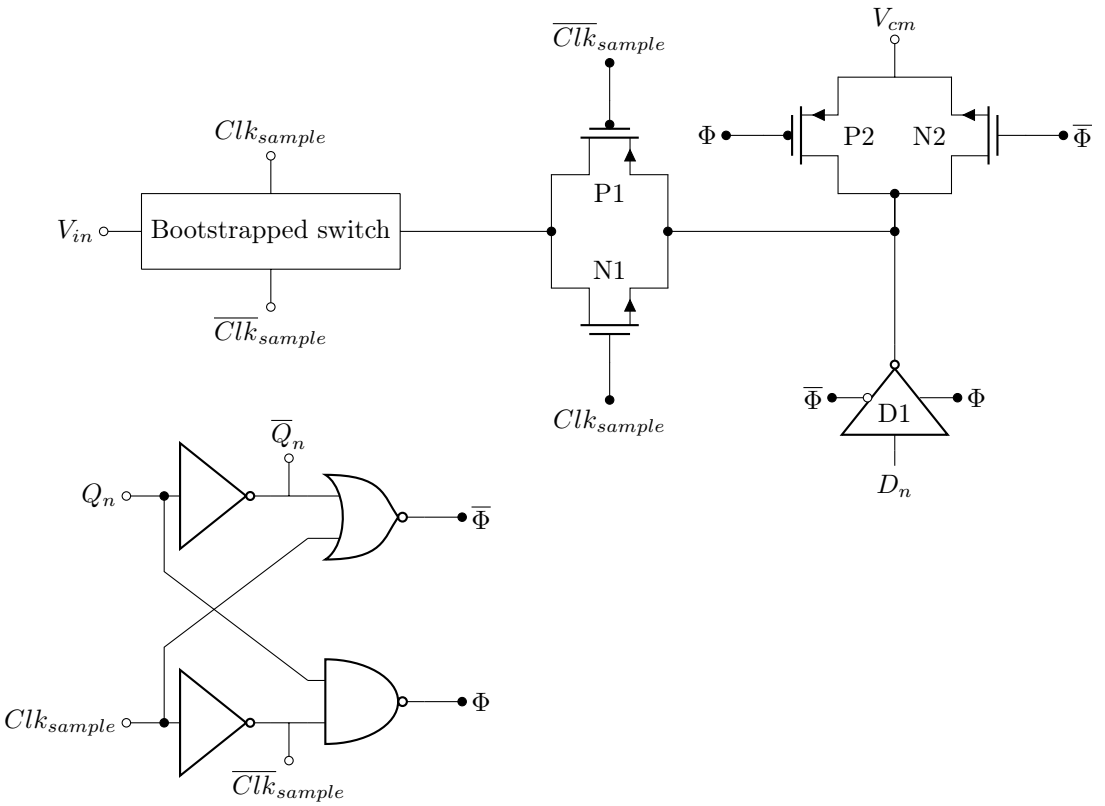


Figure 21: The Implemented DAC switches.

Figure 22 shows the implemented bootstrap switch. The bootstrap switch is implemented as [21] except for the dummy transistor on the output. All transistors are implemented with digital unit size except for the bootstrapped switch Mn_s, which is $2\mu m$ wide.

No layout is made for the switching circuitry. Therefore, an area estimation is made by placing all transistors in a layout view and adding space in width for bulk connections. The estimated layout of the digital switches is measured to be $4.3\mu m$ wide and $5\mu m$ long with some overhead. The bootstrap switches are measured to be $4.25\mu m$ wide and $4.2\mu m$ long.

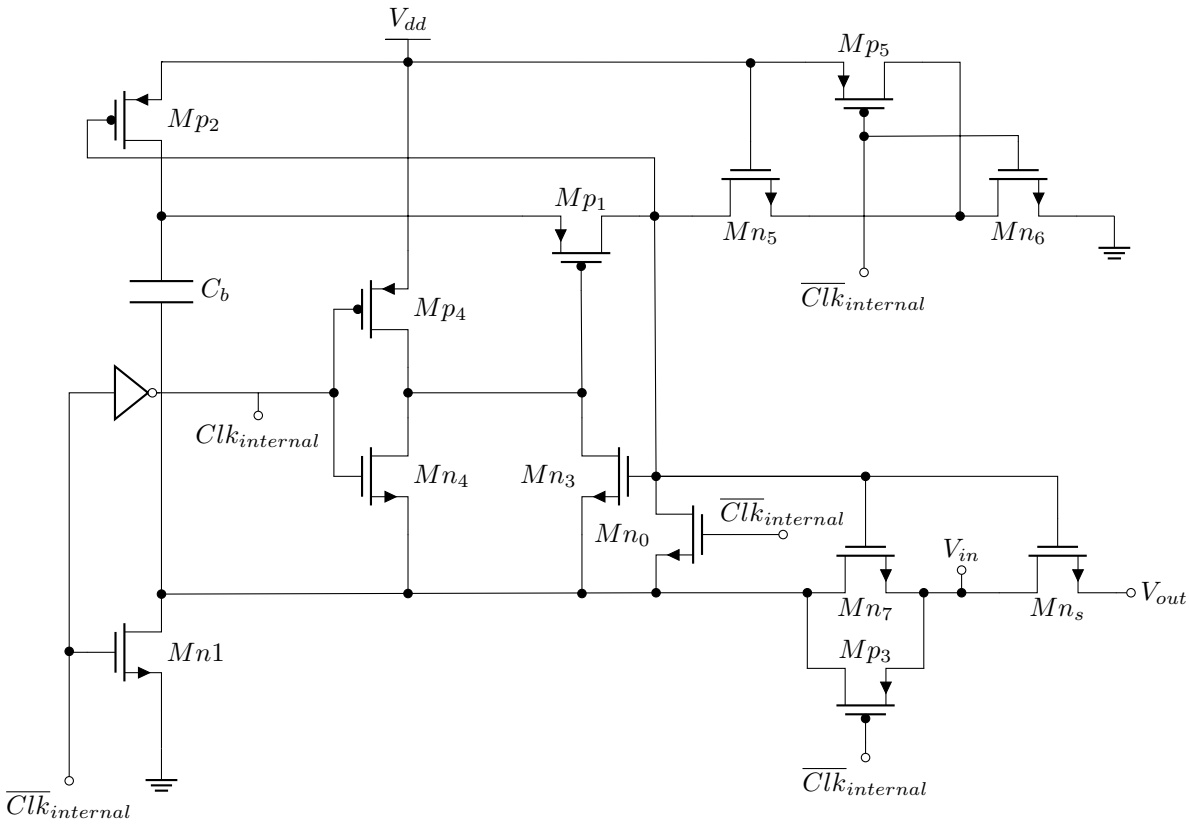


Figure 22: The implemented bootstrapped switch.

4.8.2 Capacitor array

Figure 23 shows the implemented Capacitive DAC (CDAC) schematic. C in the figure is the unit capacitor described in 3.2. Furthermore, the capacitance is multiplied by two-exponents starting at C, $2C$, $4C$, $8C$, and so on. Larger capacitors are made by adding unit capacitors in parallel. The sampling switch M_1 is an NMOS clocked synchronously to $Clk_{sampling}$ but with an amplitude of $2V_{dd}$. This signal could be taken from elsewhere on the chip or implemented with a charge pump[22]. Vs_1 is connected to a switch built much like an inverter. However, the PMOS source is connected to V_{cm}, and the NMOS source is connected to V_{in}. $V_{c<0:8>}$ are connected to the DAC switches described in 4.8.1.

No layout is implemented for the DAC. Therefore, an estimation for the area will be presented: One unit capacitor is $1.327\mu m$ wide and $0.854\mu m$ long. Thirty-two capacitors are stacked in the length direction and sixteen in the width direction. Thus the capacitor array is $42.464\mu m$ long and $13.664\mu m$ wide.

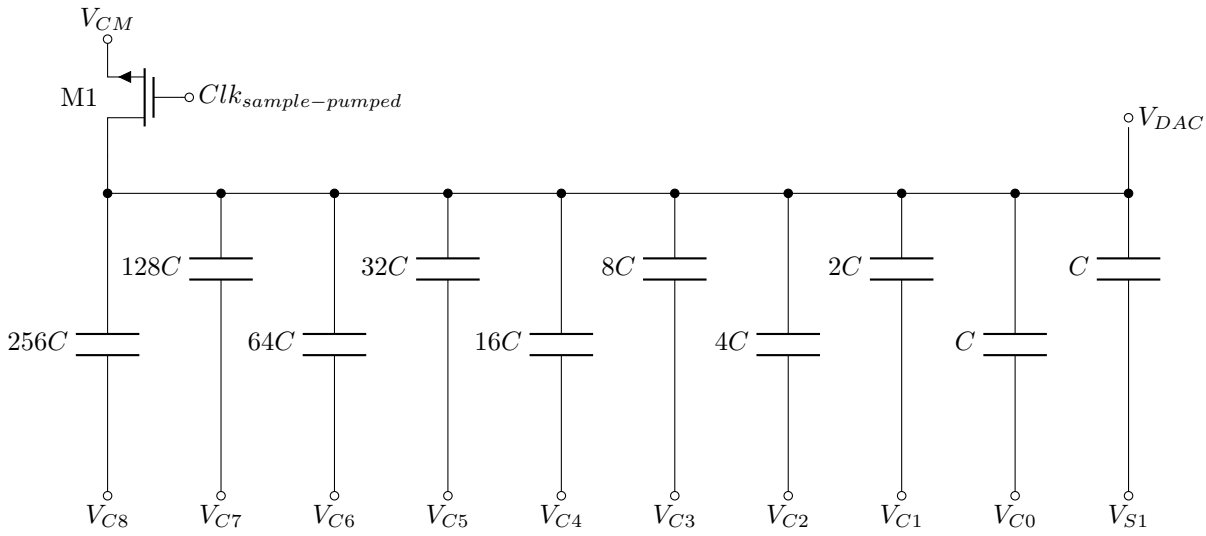


Figure 23: The Implemented CDAC.

5 Results

This section presents the final results of simulations and layout plans for the implemented Successive-Approximation-Register (SAR) Analog-To-Digital Converter (ADC).

5.1 Validation details

To validate the ADC, a sinusoid signal with an amplitude of V_{dd} is applied to both V_{in} and V_{ip}. The input signals are in opposite phase so that $V_{in} = V_{dd} - V_{ip}$ at all time. This way, the common-mode between the inputs will always be $\frac{V_{dd}}{2}$. Clk_{sample} is generated by a pulse source with an amplitude of V_{dd} and a pulse width of $100\mu s$. Finally, the three reference voltages: ground, V_{cm} and V_{dd} are generated using ideal DC voltage sources at respectively $0V$, $0.2V$, and $0.4V$. The output of the data register is then applied to an ideal Digital-To-Analog Converter (DAC) written in Verilog-A, which outputs a quantized version of the input signal. The Cadence Virtuoso spectrum tool evaluates the quantized signal in the frequency domain. The exact test bench setup can be found in the appendix.

The ADC is sampled according to coherent sampling [23]. Two different input signals will be used: For corner simulations, the ADC will perform 128 samples over three periods of an input signal at $23.4375Hz$ with a sampling rate of $1kHz$ per Fast Fourier Transform (FFT). A brief frequency sweep is performed in the nominal corner. The sweep is performed with 2048 samples, sampled at $1kHz$ with two input frequencies: $2.4414Hz$ is used to test performance at low frequencies, while $498.5352Hz$ is used to test the ADC performance at the Nyquist rate. Finally, the simulations are performed with a noise bandwidth of $2.5MHz$. The noise bandwidth is chosen by gradual increment until minimal changes are seen in the result. At $2.5MHz$, changing the noise seed has the same effect as increasing the noise bandwidth. For the final simulations, noise seed three is used.

5.2 Simulations

The ADC is being simulated using post-layout models. However, only the unit capacitor and comparator have an extracted layout to simulate. Furthermore, the unit capacitor is created using metal strips; thus, it does not have a model card. In other words, the ADC is simulated mainly pre-layout, except for the comparator.

5.2.1 Corner simulations

Table 7 shows the accuracy and power consumption of the ADC after corner simulations. The power consumption is further broken down into components below the Figure-Of-Merit (FOM).

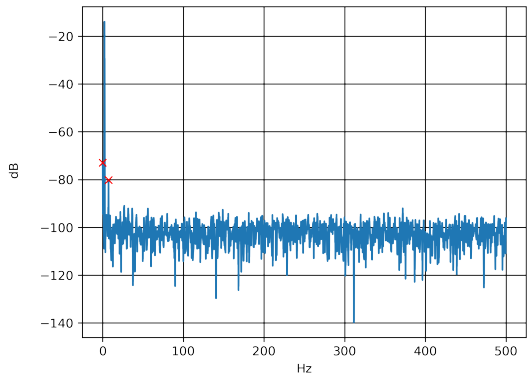
Table 7: Power and accuracy results from the corner simulations.

	tt	**ff**	**sf**
f_{in}	$23.4375Hz$	$23.4375Hz$	$23.4375Hz$
ENOB	9.1	9.1	7.4
Total power	$493.1pW$	$1.3nW$	$530.7pW$
FOM $\left[\frac{fJ}{conversion-step}\right]$	0.9	2.3	3.15
Comparator power	$233.8pW$	$234.5pW$	$264.5pW$
CDACs power	$158.7pW$	$718.5pW$	$173.1pW$
Counter power	$42.4pW$	$179.3pW$	$38.4pW$
SAR power	$23.2pW$	$107.8pW$	$21.2pW$
Clock circuit power	$35.0pW$	$69.4pW$	$33.2pW$

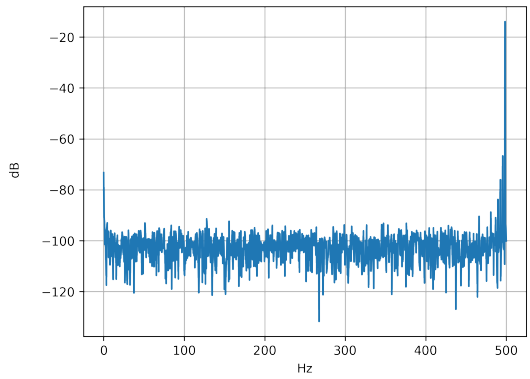
5.2.2 Frequency sweep

Figure 25a shows the spectrum of an FFT produced by the ADC with an input frequency of $2.4414Hz$. The DC component and third harmonic are the second and third largest. Therefore, they are marked on the figure. Figure 25b shows the spectrum of and FFT produced by the ADC with an input frequency of $498.5352Hz$. The accuracy and power consumption results are shown in table 10.

Figure 24: Spectres produced by the ADC through the frequency sweep.



(a) Spectrum from FFT of ADC with input signal $2.4414Hz$.



(b) Spectrum from FFT of ADC at Nyquist rate.

f_{in}	$2.4414Hz$	$498.5Hz$
ENOB	9.0	8.1
Total power	$480.4pW$	$544.0pW$
Comparator power	$233.6pW$	$229.0pW$
CDACs power	$147.0pW$	$209.5pW$
Counter power	$21.3pW$	$42.4pW$
SAR power	$22.5pW$	$25.2pW$
Clock circuit power	$56.0pW$	$37.9pW$

Table 10: Power and accracy results from the frequency sweep.

5.2.3 Static power consumption

Table 11 shows the static power consumption of the ADC simulated in the nominal corner. For the simulations, V_{in} and V_{ip} are left floating, and the clock is turned off while the power supply is still connected. The static power consumption is simulated with and without the V_{cm} connected.

Table 11: Static power consumption.

Total power	$68.4pW$
Comparator power	$1.0pW$
NDAC power	$28.2pW$
PDAC power	$15.9pW$
Counter power	$11.6pW$
Output register power	$5.9pW$
Clock circuit power	$5.8pW$

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5.3 Estimated total area

Figure 26 is a rough top-level floor plan for the finished layout. The relative sizes of the blocks in the plan are according to the area measurements and calculations presented through 4.

Circuitry belonging to the DAC is marked with red, digital registers are marked with blue, the comparator with green, and the clock in pink. The total width of the layout is estimated to 28.8μm, and the length is estimated to 92μm

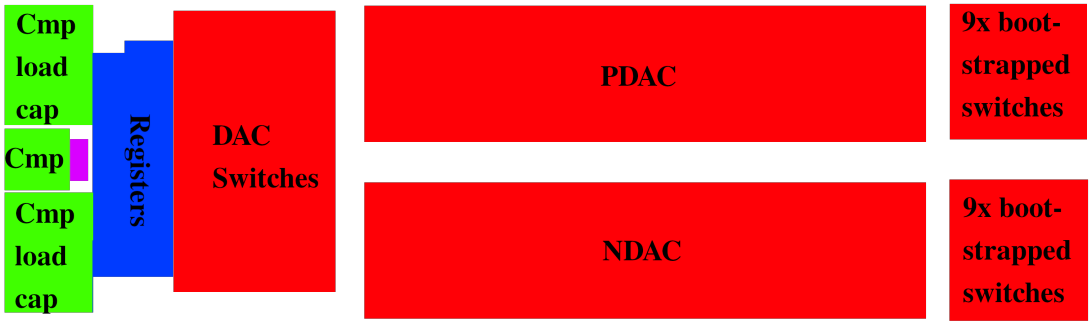

Figure 26: Layout floor plan.

6 Discussion

This section summarizes the previous sections by first discussing the results presented in 5. Some hypotheses for improvements are presented and tested through separate test benches in the appendix.

6.1 Accuracy

The implemented Analog-To-Digital Converter (ADC) shows good accuracy results when simulated in the nominal corner. It reaches 9.1 Effective Number of bit (ENOB) with an input frequency of $23.4375Hz$ and 9.0 with an input frequency of $2.4414Hz$. This is just above the specified goal. Thus, it indicates that the design could be implemented with more work. The spectrum shown in Figure 25a shows that the ADC has a slight DC offset and peak at the third harmonic. The ADC works up to the Nyquist rate. However, the ENOB is degraded to 8.1. Also figure 25b show a slight DC offset.

The design falls apart when introducing slow Positive-Channel Metal-Oxide-Semiconductor (PMOS) corners and mismatch simulations. It is clear from transient simulations that the clock pulses are unstable outside of the nominal corners. In the slow-slow corner, the clock can only produce one pulse between the sampling clock pulses. One solution could be to slow down the sample clock to slack the restrictions on the internal clock. However, the clock must be slowed down to one-tenth of the specifications for the clock to complete in all corners. Furthermore, brief experimentation with lowering the external clock frequency revealed issues producing the rising edge setting the iteration counter in slow PMOS corners.

A common factor for the clock and generating the set edge is the delay block presented in 3.3. Therefore, one hypothesis is that the delay block is strongly affected by variations in threshold voltage. Charging the gates of the output transistors to their threshold can be seen as a Resistor-Capacitor(RC) response. As the resistive element of the RC response is a transistor, the first threshold dependency could be present in the input. Furthermore, the delay created in the clock circuit is on the order of μs. This makes the settling time of the RC response long. For this reason, slight variations in the threshold voltage of the output transistors make significant variations in the total delay created by the circuit.

6.2 Power usage

The results in the nominal and sf corners show promise. Total power consumption of under $493.1pW$ is among the best of the ADCs referenced in this thesis, only beat by [12] pre-layout. However, the only post-layout parasitic extracted in this thesis is those of the comparator. [12] and [11] report that extracting parasitic for the digital logic significantly influences the power consumption. Therefore, additional power consumption should be expected in a complete post-layout simulation.

Also, the ff corner shows a significant increase in power consumption. Especially the digital components and the Digital-To-Analog Converters (DAC) have an increased power consumption. This could indicate that the digital building blocks are weak to either leakage or increased dynamic power consumption in the ff corner. However, the ff corner is as little likely in a real chip as the tt corner and is expected to increase the power consumption. Therefore, the power consumption is not of high priority for future work.

The static power consumption present when the clock is disabled as shown in table 11 is $68.4pW$. As expected, the comparator has a low static power consumption of only $1pW$, which is promising. The NDAC has close to double the static power consumption of the PDAC. The only difference between the PDAC and NDAC is that the bit from the output register is inverted in the NDAC. This indicates that the switches could be improved concerning static power consumption. The counter has a static power consumption of $11.6pW$, and the output register has $5.9pW$. This is is no surprise as they are made the same, except for extra delay and logic in the counter.

6.3 Comparator

The strongarm latch is a safe choice of a comparator. It is well represented among published Successive-Approximation-Register (SAR) ADCs [13][1] to mention some. As the most obvious component of the SAR ADC, it was also the first one to be implemented preceding the period documented by this thesis.

The comparator implemented works as expected as far as the simulated results through this thesis go. As it is the only component simulated post-layout, it is also the most realistically simulated one. However, the design could still be improved. With a more thorough characterization of the transistors used to make the comparator, the design equations presented in [15] could be used to control the delay and noise. Some iterative optimizations are still needed in such an approach, but in this way, the experience of other designers is better utilized. The design approach used for

this project is iteration-heavy, using the design equations only to know how different parameters affect the circuit. Ideally, one could design a comparator with the desired input refereed noise and settling time according to a grander plan than to improve the ENOB slightly per iteration.

The simulations were not much affected by the extracted comparator layout parasitic, which indicates a good layout. The input transistors are well protected by the guard ring, its N-well, and common centroid placement. The design could be made smaller by using shared active regions. On the other hand, shared active regions could generate more process variations and are avoided even on the latch, tail, and reset transistors. As shown in figure 15, the latch transistors are placed every second to minimize mismatch. However, assuming a mismatch in doping has a stable gradient in a horizontal direction, this placement would not decrease the sum of the mismatch. [20] proposes horizontal common centroid techniques that could be used to minimize the effect of a mismatch gradient by mirroring the layout in the middle.

As the comparator is a part of the clock circuitry, it can not be ruled out the significant variations in the internal clock frequency without further testing.

6.4 Digital circuitry

The digital circuitry works to the expectations. In [11] The digital circuitry uses more power than the DAC. In the implemented design, the digital circuitry consumes the least energy except for simulations in the ff corner. Much credit for low digital power could probably be given to the technology node. Fully-Depleted-Silicon-On-Insulator (FDSOI) technology allows for very low leakage devices. Therefore, almost all power consumption is dynamic from logic changing its state. The low frequency of operation enables low power consumption even further by enabling the use of high threshold devices even with a power supply of $400mV$.

6.5 Digital-to-Analog Converter

The DAC is where this thesis differs the most from previous work done with ultra-low-power SAR ADCs at NTNU. This is the decision of using the V_{cm} based switching scheme described in 4.8.1 instead of a monotonic switching scheme. A direct comparison between the two schemes can be made by comparing the results presented in [12]. The DACs presented is reported to use $88.8pW$ with a C_{unit} of $1fF$. The implemented DACs in this thesis use $158.7pW$ with a C_{unit} of $1.15fF$. Normalizing the results concerning C_{unit} gives a power consumption of 88.8 and 138.0 for the

monotonic and V_{cm} based switching scheme, respectively.

At first glance, the monotonic switching scheme seems to have a lower power consumption. However, the comparison also includes the power consumption of the DAC switches. Another regard is that the DACs are not implemented with the option to operate solely on a $0.4V$ clock signal. During the sampling time, V_{cm} is connected to the inside of the capacitor array using a $2 * V_{dd}$ clock. In order for the DACs to operate on one clock alone, a charge pump would need to be implemented. This would lead to an even higher power consumption in the V_{cm} based switching scheme.

On the other hand, a bootstrap switch is implemented outside all the capacitors in the DACs. These could be implemented with shared logic, saving space and possibly power. Nevertheless, not even mentioning the logic presented in 4.8.1, the implemented V_{cm} switching circuit is complex. Even more so, taken into consideration that [12] reports using a single bootstrap switch inside the DACs, and a single inverter on the outside of each capacitor.

As the V_{cm} based switching scheme is complex, some additional power is expected to be consumed in the switches. Therefore, figuring out how much of the consumed energy is dissipated through charge redistribution is interesting. If most of the power is dissipated through the switches, it could be possible to optimize the DACs further. For example, the bootstrap switches. There are, in total, eighteen bootstrap switches. Even though all the switches are needed, one larger capacitor could be used to bootstrap all the switches, lowering the power consumption and the area.

Finally, another high precision voltage reference is required is a noteworthy downside. [24] is an implementation of a reference generator specifically for the ADC in this thesis. Even though the additional reference could lower the power consumption in the ADC, the additional reference brings higher power consumption and more complexity to the design of the required reference generator.

6.6 Clock circuit

The implemented clock circuit is simple but effective in the nominal corner. The principle is that the comparator gets to take its time to settle. After that, the extra delay makes sure that the output register has time to save the comparison, and the DACs have time to settle to their new output. However, the significant variations in the clock frequency are one of the presented design's most apparent bottlenecks. Therefore, improving the mismatch tolerance for the clock circuitry is

the highest priority on the list of future work.

6.7 Hypothesis validation

The hypothesis that the delay blocks are the reason why the design does not work in all corners is verified through further testing. A test bench mimicking the clock circuit in the ADC is available in the appendix. The first test bench is identical to the clock circuit. However, an ideal delay of $15\mu s$ implemented with Verilog-A replaces the settling time of the comparator. In this test, the clock circuit's time to create ten clock pulses is measured over corners and through mismatch simulation. The hypothesis that the delay changes drastically over corners is confirmed as the measured time in ff, sf, nominal fs, and ss respectively is $57.45\mu s$, $307.5\mu s$, $648.6\mu s$, $1.399ms$ and $5.136ms$. This indicates a direct connection between the ADC's failed corners and the delay block.

Both [12] and [11] reported an increase in power consumption due to the digital layout. Therefore, the Data Flip-Flops (DFF) are tested before and after the layout. The same test bench is used as the one used to compare the conventional DFF to the tri-state inverter-based DFF in 3.4. The pre- and post-layout simulations give more or less identical results, giving more credit to the reported power consumption. However, the digital circuitry consists of, in total, twenty DFFs. Additionally, there are logic gates and edge detectors. Therefore, nothing can be said with certainty without completing the layout of the entire registers.

The delay blocks are proven to destroy the results over corner simulations and mismatch simulations. The ADC is therefore simulated with mismatch without delay. These simulations show that even if the clock circuit were functioning, the ADC would still not work up to specification with a mismatch. The results are available in the appendix.

6.8 Comparison to state-of-the-art

Table 13 shows the comparison between key results in the presented ADC, the ADC used for comparison to the monotonic switching scheme, and the ADC with the lowest power consummation in [2]. [25] is reported as part of a signal chain. Therefore the area used in table 13 is a rough estimate based on the reported total area and layout. In a nominal corner, the presented SAR ADC is comparable to the state-of-the-art. However, compared to the nominal corner simulations presented in [12] the ADC results are not as good. Much work is left to verify the ADC as a state-of-the-art ADC. Even more so, taking into consideration, the modern technology node used.

However, [12] reported a significant increase in power consumption post-layout. The DFF used in this project showed no increase in post-layout power consumption. On the other side, no tests are done on the logic gates. The logic gates could increase the power consumption in the digital circuitry for the presented design.

The estimated area usage is promising in comparison to the other ADCs. However, the layout is expected to change as the ADC is altered to handle mismatch. Furthermore, the technology node helps with the area as well.

Table 13: Comparison to state-of-the-art.

	This work	[12]	[25]
Technology node	$22nm$	$28nm$	$180nm$
Area used	$0.0026mm^2$	$0.01mm^2$	$0.1875mm^2$
simulated in	Nominal	Nominal(pre-layout)	Measured
ENOB	9.141	9.4	7.7
Total power consumption	$493.1pW$	$350.4pW$	$2.7nW$
FOM[fJ/conversion-step]	0.9	0.5	13.0

7 Conclusion and future work

An asynchronous ultra-low-power Successive-Approximation-Register (SAR) Analog-To-Digital Converter (ADC) is designed and implemented in a commercially available $22nm$ Fully-Depleted-Silicon-On-Insulator (FDSOI) technology. The ADC is created using a fully differential V_{cm} based switching scheme to minimize power consumption. The ADC is verified with a post-layout implementation of a strongarm latch, custom-made unit capacitor, and schematic Digital-To-Analog Converter (DAC) and Digital circuitry. The ADC reaches an Effective Number of Bit (ENOB) of 9.141 in the nominal corner. The power consumption is $493.1pW$, and the sampling frequency is $1kHz$ leading to a figure-of-merit of $0.9fJ/conversion-step$. Finally, the complete layout has an estimated area of $0.0026mm^2$. These results are comparable to state-of-the-art ADCs. However, much work is left concerning layout and mismatch verification.

7.1 Future Work

The first item on the list is to improve the design over corner simulations. First of all, the clock circuitry has to be improved. The delay block is the apparent bottleneck in the current design; however, mismatch simulations excluding the delay block also show other issues. Possible solutions are to use buffers instead of the current delay block; however, large buffers would be needed. Another solution is to obliterate the delay block. [14] uses circuitry to detect that the DACs have settled, which removes the need for delay.

The delay block does not owe all the blame for inaccuracies appearing in mismatch and corner simulations. Although it is the most critical and apparent cause of the error, removing mismatch variations in the delay block does not fix the simulations. Further characterization of the DAC and Comparator over corners is therefore needed.

When the design show improvements, it is essential to do mismatch simulations. Although corners reveal worst-case scenarios, they are no more likely scenarios than the nominal corner. Therefore, mismatch simulations should be used frequently to continue this project. One option is to always simulate with a mismatch, then change the seed or iteration once in a while.

Once the problems with mismatches and corners are solved on a schematic level, it is crucial to finish a layout. Extracting layout parasitics will introduce other mismatch effects. Some iterations with layout improvement are, therefore, to be expected. Extracting the layout is also expected to

increase the power consumption, especially in digital circuitry. Some testing is done post-layout with the Data Flip-flops (DFF), but the digital logic is expected to consume more power post-layout. One solution to this event could be implementing less power-hungry logic gates than the conventional, complementary logic. The significant advantage of complimentary gates is their equal ability to drive high and low output. However, the frequencies involved in the presented design are relatively low, which opens the possibility of using less power-hungry gate logic.

More testing should be done regarding the capacitors used in the circuit. The methods described in [26] are tested with failure. However, the attempt is performed with several glitches and inaccuracies not present in the presented design. Revisiting [26] is therefore an interesting next step. Once the cap sizes are changed, the switches need to be optimized to the new capacitance. Measuring the resistance through the switches in a separate test bench and then calculating the Resistor-Capacitor (RC) response could be more effective than intuition and iterative testing.

Finally, once a satisfying design is acquired, more testing than presented for this thesis should be performed. First, a design tested without post-layout mismatch will not work in reality, and the ADC should be tested over multiple input frequencies to look for resonance. Finally, Differential-Non-Linearity and Integrated-Non-Linearity should be extracted as described in [6]. However, these are extensive final results that require a large set of measurements of the ADC's output states.

References

[1] D. Verma, K. Shehzad, D. Khan, S. J. Kim, Y. G. Pu, S.-S. Yoo, K. C. Hwang, Y. Yang, and K.-Y. Lee, "A design of low-power 10-bit 1-ms/s asynchronous sar adc for dsrc application," *Electronics*, vol. 9, no. 7, 2020. [Online]. Available: https://www.mdpi.com/2079-9292/9/7/1100

[2] B. . Murmann, "Adc performance survey 1997-2021," accessed: 2022-01-10. [Online]. Available: http://web.stanford.edu/~murmann/adcsurvey.html

[3] X. Tang, J. Liu, Y. Shen, S. Li, L. Shen, A. Sanyal, K. Ragab, and N. Sun, "Low-power sar adc design: Overview and survey of state-of-the-art techniques," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 69, no. 6, pp. 2249–2262, 2022.

[4] S. F. Morken, "Parts to create a ultra low power analog-to-digital converter for ultrasound temperature measurements." 2022.

[5] C. Mazuré, R. Ferrant, B.-Y. Nguyen, W. Schwarzenbach, and C. Moulin, "Fdsoi: From substrate to devices and circuit applications," in *2010 Proceedings of ESSCIRC*, 2010, pp. 45–51.

[6] T. C. Carusone, D. Johns, and K. Martin, *Analog Integrated Circuit Design*, 2nd ed. Wiley, 2012.

[7] D. M. H. Neil Weste, *Integrated Circuit Design: International Version: A Circuits and Systems Perspective*, 4th ed. Pearson, 2010.

[8] R. Chinnaiyan and A. Kumar, "Construction of estimated level based balanced binary search tree," in *2017 International conference of Electronics, Communication and Aerospace Technology (ICECA)*, vol. 1, 2017, pp. 344–348.

[9] J. Steensgaard, "Bootstrapped low-voltage analog switches," in *1999 IEEE International Symposium on Circuits and Systems (ISCAS)*, vol. 2, 1999, pp. 29–32 vol.2.

[10] T. Kobayashi, K. Nogami, T. Shirotori, Y. Fujimoto, and O. Watanabe, "A current-mode latch sense amplifier and a static power saving input buffer for low-power architecture," in *1992 Symposium on VLSI Circuits Digest of Technical Papers*, 1992, pp. 28–29.

[11] S. Josephsen, "An ultra-low power sar-adc in 65 nm cmos technology," *NTNU Open*, 2013. [Online]. Available: http://hdl.handle.net/11250/2433737

[12] T. H. Nornes, "Ultra-low power sar-adc in 28nm cmos technology," *NTNU Open*, 2015. [Online]. Available: http://hdl.handle.net/11250/2371499

[13] C.-C. Liu, S.-J. Chang, G.-Y. Huang, and Y.-Z. Lin, "A 10-bit 50-ms/s sar adc with a monotonic capacitor switching procedure," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 4, pp. 731–740, 2010.

[14] H. Fon, "Sar adc in 22 nm fdsoi," *NTNU Open*, 2018. [Online]. Available: http://hdl.handle.net/11250/2564174

[15] B. Razavi, "The strongarm latch [a circuit for all seasons]," *IEEE Solid-State Circuits Magazine*, vol. 7, no. 2, pp. 12–17, 2015. [Online]. Available: https://ieeexplore.ieee.org/document/7130773

[16] P. Harpe, C. Zhou, X. Wang, G. Dolmans, and H. de Groot, "A 12fj/conversion-step 8bit 10ms/s asynchronous sar adc for low energy radios," in *2010 Proceedings of ESSCIRC*, 2010, pp. 214–217.

[17] J. Puhan, D. Raič, T. Tuma, and Árpád Bűrmen, "Break-before-make cmos inverter for power-efficient delay implementation," *The Scientific World Journal*, vol. 2014, p. 11, 2014.

[18] M. G. Kunwar Singh, Satish Chandra Tiwari, "A modified implementation of tristate inverter based static master-slave flip-flop with improved power-delay-area product, article id: 453675," in *The Scientific World Journal*, vol. 2014, 2014.

[19] X. Zhou, X. Gui, M. Gusev, N. Ackovska, Y. Zhang, and L. Geng, "A 12-bit 20-ks/s 640-nw sar adc with a vcdl-based open-loop time-domain comparator," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 69, no. 2, pp. 359–363, 2022.

[20] R. J. Baker, *Resistors, Capacitors, MOSFETs*. John Wiley & Sons, Ltd, 2010, ch. 5, pp. 105–130. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/9780470891179.ch5

[21] H. Chen, L. He, H. Deng, Y. Yin, and F. Lin, "A high-performance bootstrap switch for low voltage switched-capacitor circuits," in *2014 IEEE International Symposium on Radio-Frequency Integration Technology*, 2014, pp. 1–3.

[22] G. Palumbo and D. Pappalardo, "Charge pump circuits: An overview on design strategies and topologies," *IEEE Circuits and Systems Magazine*, vol. 10, no. 1, pp. 31–45, 2010.

[23] *A Tutorial in Coherent and Windowed Sampling with A/D Converters*, renesas, 2 1997, rev. 0.00.

[24] I. Hannisdal, "Reference generator for a sub-nw 9-bit 1ksample/s asynchronous sar-adc in 22nm utbb fdsoi." 2022.

[25] S. Jeong, Y. Chen, T. Jang, J. Tsai, D. Blaauw, H.-S. Kim, and D. Sylvester, "21.6 a 12nw always-on acoustic sensing and object recognition microsystem using frequency-domain feature extraction and svm classification," in *2017 IEEE International Solid-State Circuits Conference (ISSCC)*, 2017, pp. 362–363.

[26] T. Sundstrom, B. Murmann, and C. Svensson, "Power dissipation bounds for high-speed nyquist analog-to-digital converters," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 56, no. 3, pp. 509–518, 2009.

8 Appendix

Appendix is available on:

https://drive.google.com/drive/folders/1cPAECgF-7dcYwfzHHtYorNRWENJ_lHWu?usp=sharing