Control of DC-capacitor Peak Voltage in Reduced Capacitance Single-Phase STATCOM

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***Abstract*—This paper discusses the design and control of a single-phase STATCOM with reduced dc capacitance. It is first demonstrated how operation with reduced dc capacitance and large dc voltage oscillations can be possible without increasing the maximum dc voltage, as long as only operation for reactive power injection is required. Then, a method for dc peak voltage control is proposed, based on adaptive filters for dynamically detecting the average value and the amplitude of the dc voltage oscillations. It is demonstrated by simulations and experiments that the presented control strategy can be effectively utilized to regulate the peak voltage in the dc capacitor under various operating conditions.**

I. Introduction

A high dc-side capacitance is usually required for single-phase converters to limit the dc voltage oscillations caused by the double frequency instantaneous power inflow to the capacitor. The high capacitance results in large dimensional size of the capacitor, since a film capacitor is usually used in such converters. To address this problem, it has been proposed to reduce the capacitance in single-phase STATCOM by accepting a larger amplitude of the double frequency dc voltage oscillations [1]. By applying this approach, the capacitor size of the single-phase STATCOM can be reduced, and a considerable size reduction can be expected. The same concept can be applied to transformer-less STATCOMs using modular multilevel converter (MMC) topologies [2], [3], [4], where significant improvement its power density can also be achieved.

The basic concept of capacitance reduction has been demonstrated in [1]; however, the previous analysis was mainly dedicated to the validation of the system design and verification of the general operational characteristics. Thus, for simulations and experiments, the single-phase converter was controlled by a voltage control loop without any explicit current control or current limitation. Furthermore, to achieve high power density, the grid-side filter inductor should also be kept small. This requires a relatively high switching frequency and fast closed loop current control to prevent over-currents during grid-side disturbances. Thus, a conventional control structure with an inner loop current controller for the the ac-side filter current and an outer loop controller for the dc voltage is more suitable for practical applications.

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Contrary to conventional converter designs and control system configurations for single-phase grid-connected converters, a small dc-capacitance might make it more important to control the maximum and/or minimum dc-side voltage than the average capacitor voltage. To address this issue, a strategy is proposed in this paper for combined closed loop current and dc voltage control of a single-phase STATCOM, designed for regulating the peak value of the dc voltage while operating with large voltage oscillations at twice the line frequency. The proposed control method is based on the use of adaptive filters for detecting the average and oscillating components of the dc voltage, which are used as feedback for controlling the peak capacitor voltage. The operation of the proposed control method is demonstrated by time-domain simulations and laboratory experiments.

II. Principle of Capacitance Reduction

Fig. 1 shows the circuit configuration of a two-level voltage source converter (VSC) -based single-phase STATCOM. Fig. 2(a) shows the operation principles with a conventional design of the capacitor. For STATCOM operation with negligible losses, the instantaneous power flowing into the bridge can be derived as:

$$p = v_{\mathrm{conv}(1)} i = V_{\mathrm{conv}} I \sin 2\omega_g t, \tag{1}$$

where $v_{\mathrm{conv}(1)}$ and i are the fundamental frequency components of the converter output voltage and current, while V_{conv} and I are their rms values, respectively. The power, p, is oscillating at twice the line frequency, as shown in the figure. The oscillating instantaneous power flow results in capacitor voltage oscillations, and the dc capacitor voltage v_{c} can be

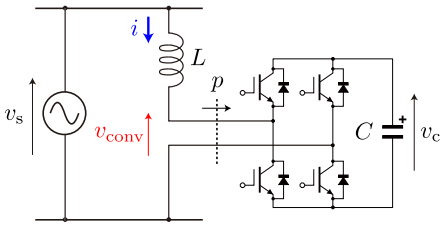


Fig. 1. Circuit configuration of a single-phase STATCOM. Definitions of symbols are also shown.

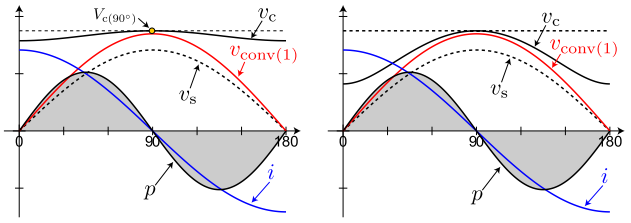


Fig. 2. Schematic half-cycle waveforms of the STATCOM with (a) Conventional design and (b) Reduced capacitance.

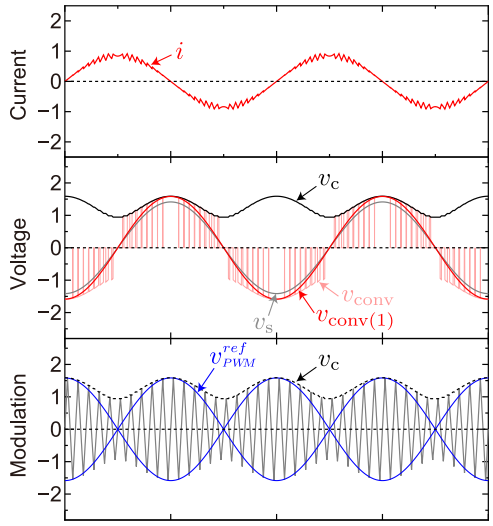


Fig. 3. Schematic view of the modulation technique for strongly swinging capacitor voltage.

expressed as

$$v_c = \sqrt{{V_{c(90°)}}^2 - X_c V_{conv} I^* (1 + \cos 2\omega_g t)}, \qquad (2)$$

where X_c is the reactance of the dc capacitor at the line frequency, defined as $1/\omega C$, and $V_{c(90°)}$ is v_c at the current zero-crossing. Usually the voltage ripple of the capacitor is maintained within a certain range; for instance 5%, by selecting a high capacitance to ensure low X_c. For controlled operation of the VSC, v_c must be always higher than $v_{conv(1)}$ during the full grid frequency cycle; usually, simply selecting $V_{c(90°)} > \sqrt{2} V_{conv}$ satisfies this requirement.

In [1], it has been proposed that the capacitance can be reduced by accepting larger double frequency oscillations in the capacitor voltage, as shown in Fig. 2(b). This depends on

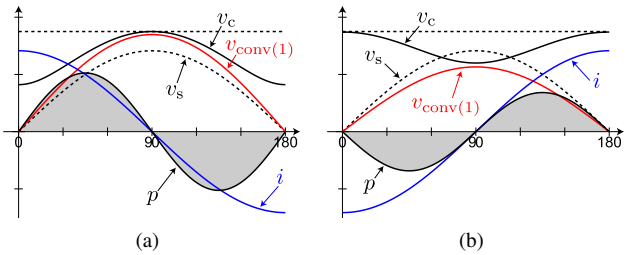


Fig. 4. Schematic half-cycle waveforms of the STATCOM with a reduced capacitance to achieve the same current within the same peak voltage both in (a)Capacitive operation, (b)Inductive operation.

a modulation technique that takes into account the significant capacitor voltage oscillations while ensuring a good offset voltage control. Fig. 3 shows a schematic view of the modulation technique for operation in capacitive range with a reduced capacitance. In this figure, v_{conv} is the converter output voltage and $v_{conv(1)}$ is its fundamental components while v^{ref}_{PWM} is the voltage given to the carrier based PWM. The modulation must be based on the actual capacitor voltage since the ripple voltage is high. Thus, the carrier waveform has an envelope corresponding to v_c to ensure that the desired output voltage can be generated with the highly oscillating capacitor voltage.

The capacitance reduction by accepting large capacitor voltage oscillations can be achieved mainly when operated for reactive power generation, i.e. in the capacitive compensation mode as shown in Fig. 4 (a). In this particular condition, v_c has its peak at the same time as $v_{conv(1)}$; therefore, the capacitance reduction does not require that the peak capacitor voltage must be increased. In inductive operation, the operating range will be limited by the allowable peak voltage. However, due to the voltage drop across the filter inductor, a relatively lower $v_{conv(1)}$ is needed for inductive operation when increasing the current. Thus, some inductive operating range can also be achieved within the same voltage as required for the rated capacitive operation, as shown in Fig. 4 (b). However, this effect is determined by the filter inductor, and will be limited in case of operation with high switching frequency and low filter inductance.

III. Proposed Control Method

From the above discussion, it is clear that under certain conditions the peak value of the dc voltage could be maintained at a constant and limited level while the current amplitude varies; however, the common approach for control of single-phase STATCOMs is to regulate the average value of the dc voltage. This is not the most suitable approach in case of highly fluctuating capacitor voltage since the peak will increase when the current amplitude is increased. To ensure good dynamic response for the control and safe operation of the STATCOM, it is also important to have a fast estimation of peak value of the dc voltage. In this paper, it is proposed to utilize a frequency-adaptive filter based on a Second Order Generalized Integrator (SOGI) [5] to estimate the dynamic peak value of the dc voltage. This peak voltage estimate will be used as a feedback signal for effectively controlling the single-phase STATCOM.

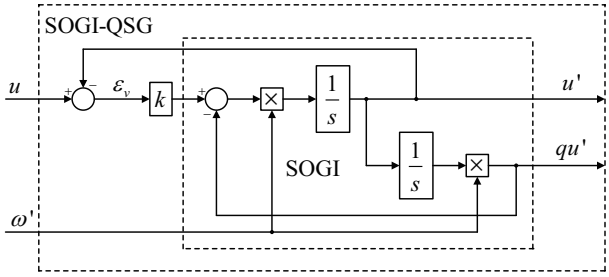


Fig. 5. Second Order Generalized Integrator (SOGI) configured as Quadrature Signal Generator (SOGI-QSG).

A. Peak voltage detection by adaptive filters

The continuous time block diagram of a SOGI configured as a Quadrature Signal Generator (QSG) is shown in Fig. 5. In this configuration, the SOGI-QSG has two output signals, providing band-pass characteristics for the in-phase signal u' and second-order low-pass characteristics for the in-quadrature output signal qu'. It is also clearly seen from the figure that qu' is the integral of the band-pass filtered signal u'. The transfer functions from the input signal to the two output signals are given on generic form for a signal u by (3) and (4), respectively:

$$h_{\mathrm{SOGI},\alpha} = \frac{u'(s)}{u(s)} = \frac{k\cdot\omega'\cdot s}{s^2+k\cdot\omega'\cdot s+\omega'^2} \quad (3)$$

$$h_{\mathrm{SOGI},\beta} = \frac{qu'(s)}{u(s)} = \frac{k\cdot\omega'^2}{s^2+k\cdot\omega'\cdot s+\omega'^2} \quad (4)$$

It should be noted that the SOGI-QSG will be frequency-adaptive as long as the actual or estimated center frequency ω' is available as a dynamic input signal.

As seen from equation (2), the dc voltage is a square-root function of the reactive power controlled by the STATCOM. Thus, the square of the dc voltage is used for signal processing, since this value is proportional to the energy stored in the dc capacitor, and will contain a pure double frequency sinusoidal oscillation.

The applied SOGI-QSG can be easily configured as a notch-filter for eliminating the double frequency oscillation and by that estimating the dynamic average value of the input signal. The corresponding transfer function for identifying the dynamic average value of the square of the dc voltage is given by:

$$\begin{aligned}\overline{v}_{\mathrm{C}}^2(s) &= v_{\mathrm{C}}^2(s) - h_{\mathrm{SOGI},\alpha}(s)v_{\mathrm{C}}^2(s)\\ &= v_{\mathrm{C}}^2(s) - \frac{k\cdot(2\omega_{\mathrm{g}}')\cdot s}{s^2+k\cdot(2\omega_{\mathrm{g}}')\cdot s+(2\omega_{\mathrm{g}}')^2}v_{\mathrm{C}}^2(s)\\ &= \left(\frac{s^2+(2\omega_{\mathrm{g}}')^2}{s^2+k\cdot(2\omega_{\mathrm{g}}')\cdot s+(2\omega_{\mathrm{g}}')^2}\right)v_{\mathrm{C}}^2(s) \quad (5)\end{aligned}$$

It is also possible to configure the same filter structure for detecting the amplitude of the double frequency oscillating component of the squared dc voltage signal. This depends on representation of the oscillations as a virtual two-phase system. where the amplitude can be calculated directly from the two orthogonal sinusoidal signals. The oscillating component of the input signal is already available as the in-phase output signal $\widetilde{v}_{\mathrm{C},\alpha}^2$ from the SOGI-QSG. However, the in-quadrature output signal $v_{\mathrm{C},\beta}^2$ from the SOGI-QSG will contain a dc-component in addition to a 90° phase shifted version of the double frequency oscillation. Detecting the amplitude of this oscillation requires that the pure oscillating component $\widetilde{v}_{\mathrm{C},\beta}^2$ of the in-quadrature output signal from the SOGI-QSG is isolated from the dc-component. The steady-state dc-component of this output signal is given by:

$$\begin{aligned}\overline{v_{\mathrm{C},\beta}^2} &= \lim_{s\to 0}\overline{v_{\mathrm{C}}^2}\cdot h_{\mathrm{SOGI},\beta}(s)\\ &= \lim_{s\to 0}\overline{v_{\mathrm{C}}^2}\frac{k\cdot(2\omega_{\mathrm{g}})^2}{s^2+k\cdot(2\omega_{\mathrm{g}})\cdot s+(2\omega_{\mathrm{g}})^2}\\ &= k\cdot\overline{v_{\mathrm{C}}^2} \quad (6)\end{aligned}$$

Thus, the oscillating component of $v_{\mathrm{C},\beta}^2$ can be estimated by subtraction of the dynamic average value of v_{C}^2 scaled by k:

$$\widetilde{v}_{\mathrm{C},\beta}^2 = v_{\mathrm{C},\beta}^2 - k\cdot\overline{v_{\mathrm{C}}^2} \quad (7)$$

From the two orthogonal double frequency signals, the amplitude $\widehat{v}_{\mathrm{C},2\omega}^2$ of the oscillations can be estimated as:

$$\widehat{v}_{\mathrm{C},2\omega}^2 = \sqrt{\left(\widetilde{v}_{\mathrm{C},\alpha}^2\right)^2+\left(\widetilde{v}_{\mathrm{C},\beta}^2\right)^2} \quad (8)$$

By adding the estimate of the average value, $\overline{v}_{\mathrm{C}}^2$, and the amplitude of the double frequency energy oscillations, $\widehat{v}_{\mathrm{C},2\omega}^2$, a dynamic estimate for the square of the dc-voltage peak value can be obtained:

$$\widehat{v}_{\mathrm{C}}^2 = \overline{v_{\mathrm{C}}^2} + \widehat{v}_{\mathrm{C},2\omega}^2 \quad (9)$$

This signal can be used as feedback for control of the dc-side of the single-phase STATCOM.

From the above considerations, the proposed adaptive filter structure for estimating the dynamic peak value of the squared dc voltage signal can be illustrated by a block diagram as shown in Fig. 6.

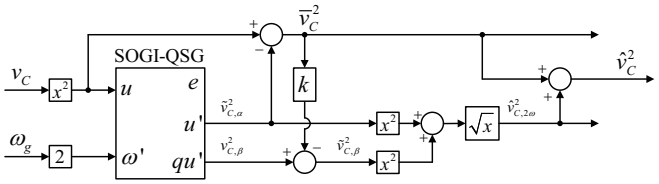


Fig. 6. Block diagram of the voltage measurement processing part. The peak capacitor voltage $\hat{v}_c$ is estimated.

B. Control system overview for reduced capacitance single-phase STATCOM

With the presented strategy for estimating the dynamic peak value of the squared dc-voltage, a conventional cascaded control structure can be designed, as shown in Fig. 7. This figure shows how the proposed method for dynamic peak value estimation is used in the feedback from the measured dc voltage, while a simple PI controller is used to regulated the peak value of the dc voltage to the reference value. The output of this PI-controller is the amplitude of the active

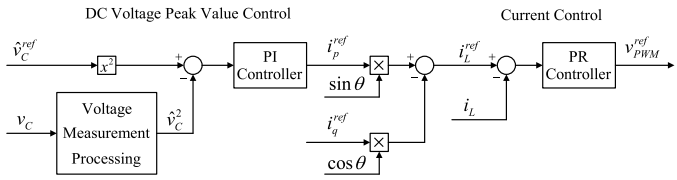


Fig. 7. Overview of the proposed control including dc peak voltage control and current control.

current component required to maintain the dc voltage at the reference value. Thus, this current amplitude reference is multiplied with a sinusoidal signal in phase with the grid voltage as provided by the grid synchronization mechanism, which in this case is assumed to be a conventional PLL. The reference for the reactive current amplitude is multiplied with a 90° phase shifted signal, and the two in-quadrature reference signals are added to generate the stationary frame sinusoidal current reference for the single-phase STATCOM.

Since the current reference resulting from the combined operation of the dc-voltage control and the reactive power control results in a single stationary frame sinusoidal current reference, a resonant controller is used for the inner control loop [6]. As shown in Fig. 7, the output from the resonant controller is the voltage reference, which is used for the PWM operation and the generation of the gate signals for the single-phase STATCOM. The carrier based PWM with considering the high voltage ripple as shown in Fig.3 can be applied to ensure a good linearity for the current control.

C. Active power feed-forward control for dynamic characteristics improvement

As shown in Fig. 4, the capacitor voltage reaches its peak value at zero current in the capacitive operation; therefore, if the current set-point is updated at the zero current phase, the capacitor peak voltage can be maintained smoothly. On the other hand, the capacitor voltage will be at its minimum at the current zero crossing during inductive operation. Therefore, the minimum voltage could be maintained smoothly in the inductive operation, if the control objective would be to regulate the minimum capacitor voltage to a constant value. However, the peak voltage should be maintained at the same level in all operating range for practical reasons.

The proposed voltage estimation technique with feedback control of the peak voltage can regulate the peak to its reference value also in the inductive operation, but after a transient response of several cycles; however, during this transient, some over-voltage or under-voltage can be observed. If the set-point change is slowly applied, the peak voltage can be almost constant; however, for the case of step or quick set-point change is needed, an active power feed-forward control can be applied to avoid the over-voltage.

Fig. 8 shows the concept. In Fig. 8(a), the solid lines show actual variables when the current was increased in step, and the dotted lines show variables in the case without the change. The instantaneous power p is increased after the current is increased, as a result, integration of p does not become zero and the capacitor voltage does not be same with the original value. The difference in energy shown as the gray area in the

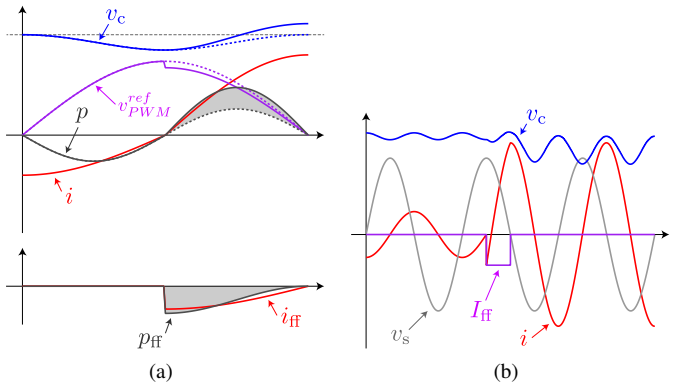


Fig. 8. Schematic view of the active power feed-forward control for transient characteristics improvement in inductive operation. (a)Feed-forward current calculated method. (b)Resulting waveforms with feed-forward.

top figure can be calculated by the original and new current set-point. The idea is to subtract the same energy by i_p, which is the current in phase with the grid voltage. The bottom figure shows the current $i_{\rm ff}$ to be added to i_p, and the resulting power $p_{\rm ff}$ transferred by the current.

Fig. 8(b) shows the schematic view of the proposed feed-forward method. $I_{\rm ff}$, which is the rms value of $i_{\rm ff}$, is subtracted from i_p^{ref} for a quarter of a period (i.e. $1/2\pi$ rad.) With some assumptions to make the calculation easy, $I_{\rm ff}$ can be calculated as

$$I_{\rm ff} = \frac{2}{\pi} I_{\rm diff}, \tag{10}$$

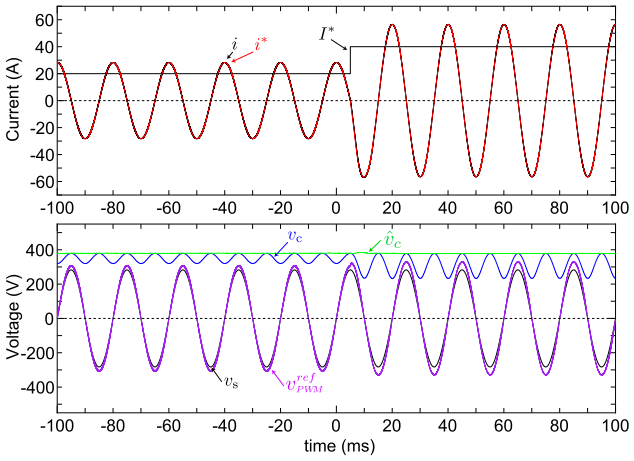
where $I_{\rm diff}$ is the step change in the current set-point in rms.

IV. Simulation Results

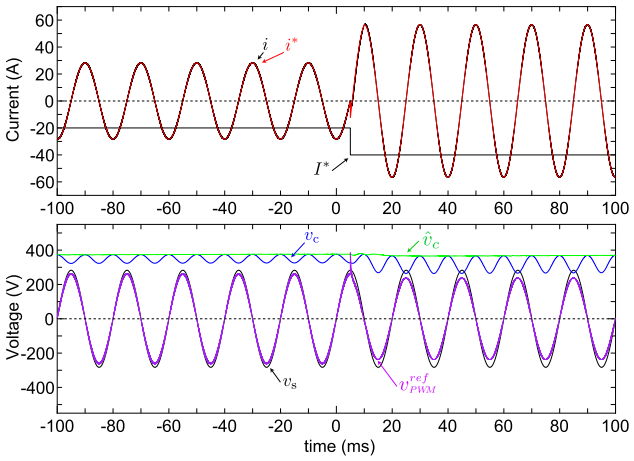
Simulations were performed based on a single-phase STATCOM module with the parameters listed in Table I. The controls proposed in the previous section, including the capacitor peak voltage estimation using a SOGI-QSG and a PR current controller using a SOGI were implemented as continuous models in the simulation. The active power feed-forward control for inductive operation was also implemented.

Fig. 9 shows resulting waveforms with a step-change in the reactive current set-point. The estimation result from the proposed voltage measurement processing part, $\hat{v}_c$, is also shown. It can be seen from the figure that $\hat{v}_c$ provides an accurate estimation of the peak value of the capacitor voltage, which has good dynamic performance in response to the step-change in reactive current reference. The active power control using this value maintained the peak capacitor voltage as expected. In the inductive operation, a current phase jump was observed since the active power was subtracted in step for 5 ms, corresponding to $1/2\pi$ radians, just after the set-point was changed.

The results in Fig. 9 (a) clearly demonstrate how the proposed operation allows for capacitive operation with large oscillations in the dc capacitor voltage while maintaining a regulated peak value. When imposing a step in the reactive current reference, it is shown how the peak value of the dc voltage is smoothly regulated to a constant value, while the



(a)



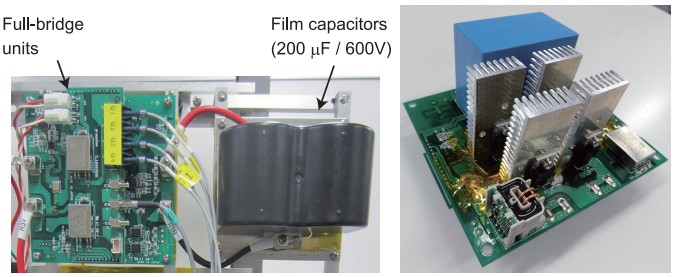
(b)

Fig. 9. Simulation results with the proposed current control and peak voltage control of the capacitor. The current set-point was changed in step from 20 A to 40 A (a)in capacitive operation, (b)in inductive operation.

TABLE I. PARAMETERS FOR THE SIMULATION.

Source voltage	V_s	200 V (in rms)
Line frequency	f_s	50Hz
Grid connecting inductor	L	2.536 mH
Capacitor	C	663 μF
Peak capacitor voltage	$\hat{v}_c^{ref}$	360 V
Maximum current	$I_{\max}$	60 A
Switching frequency	f_{sw}	10 kHz

STATCOM is also allowed to operate with a minimum dc voltage reaching values lower than the peak phase voltage without having any negative consequences on the operation of the system. Fig. 9 (b) shows the operation in inductive operation, where the peak value of the dc voltage is also smoothly regulated to the reference voltage due to the feed-forward control. The figure also shows how the dc capacitor voltage in this case can be allowed to reach slightly lower values than the grid-side voltage v_s without entering over-modulation, due to the the voltage drop over the filter inductor.



(a) (b)

Fig. 10. An overview of a unit single-phase STATCOM for the experiments. (a)Front side. (b)Back side of the circuit board.

TABLE II. PARAMETERS OF THE EXPERIMENTAL SETUP.

Source voltage	V_s	66.7 V (in rms)
Line frequency	f_s	50Hz
Rated current	I_{rated}	10 A
Rated capacity	S_{rated}	0.667 kVA
Grid connecting inductor	L	1.11 mH (0.052 p.u)
Capacitor	C	300 μF (1.591 p.u)
Peak capacitor voltage	$\hat{v}_c^{ref}$	150 V
Switching frequency	f_{sw}	10 kHz

V. EXPERIMENTAL VERIFICATION

To verify the proposed control concept, small scale experiments with a laboratory prototype of a single-phase STATCOM were conducted.

A. Experimental setup

An overview of the full-bridge converter and its capacitor is shown in Fig. 10, and its parameters are listed in Table II. This prototype was designed as a part of small scale model of a MMC based STATCOM; however, the experiments shown in this paper focus on the control of a single-phase two-level STATCOM module.

In the full-bridge converter, SiC-MOSFETs were used to ensure low losses at high switching frequency, to avoid considering voltage ripple generated by the switching, which can be increased by the capacitance reduction. The total capacitance of the dc-capacitor is 300 μF, which consists of an 100 μF capacitor on the circuit board and a 200 μF external capacitor which can be seen in Fig. 10. The peak voltage set-point of 150 V was given, that ensures the same current rating of 10 A in both capacitive and inductive operations with the same capacitor peak voltage. As an ac voltage source, a linear mode ac power supply was used to ensure ideal condition without any significant background harmonic distortion in the grid voltage.

A DSP based controller with a FPGA was used. Control calculations were performed on the DSP, and modulation and A/D conversion were performed on the FPGA. The carrier based modulation and unipolar switching, which uses 180 degree phase-shifted carriers for two legs of the full-bridge converter, were implemented on the FPGA. A/D conversion was invoked at both edges of the carrier, and an average of last two values was used as the capacitor voltage for the control, to avoid influences from the switching ripples.

The switching frequency was 10 kHz; therefore, the control cycle was 50 μs. SOGI and SOGI-QSG were implemented on

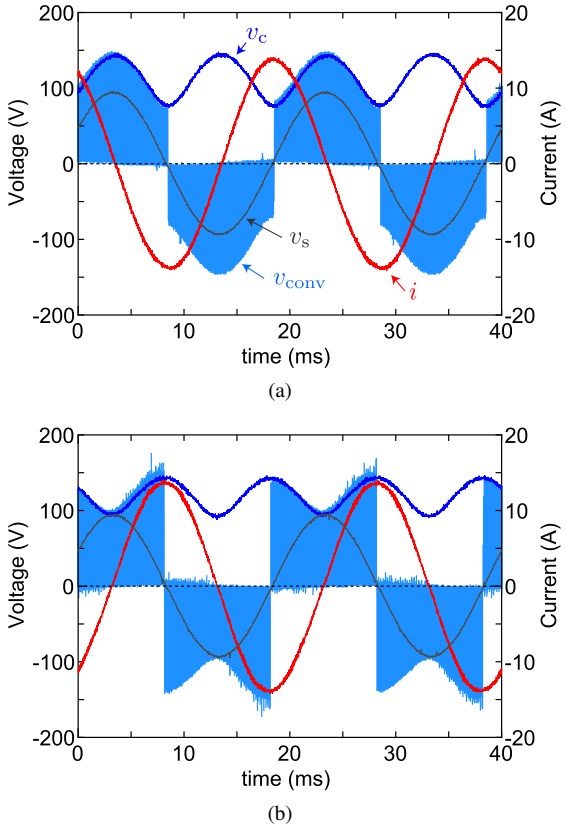


Fig. 11. Measured waveforms of steady-state operation with (a) Capacitive 10 A, (b) Inductive 10 A.

the DSP with this discrete control step, and a discrete-time implementation based on [7] was applied.

The experiments shown in this paper were based on single-phase unit; however, two line-to-line voltages of a three-phase voltage source were detected and used for grid synchronization since the setup was a part of a three-phase system. From the voltages, the grid voltage phase was estimated by using a dq0-type PLL; however, this paper does not focus on the PLL performance and assumes only ideal grid situation without considering the particular implementation of single-phase PLLs. The dc-capacitor voltage and ac current were also measured by sensors.

B. Steady-state operation

Fig. 11 shows measured waveforms of steady-state operation. Rated current operations in both capacitive and inductive ranges were confirmed. A strong voltage ripple which reaches around 50% of the peak voltage was observed in the capacitive rated operation. There were no oscillation or poorly damped responses in the capacitor voltage, and stable cyclic waveforms were observed. The current waveforms were almost pure sinusoidal wave and their THD (total harmonic distortion) were around 1.5%, with appropriate tuning of the PR current controller.

C. Step-change response

To evaluate the control performance of the proposed control method, step-changes were applied and waveforms were

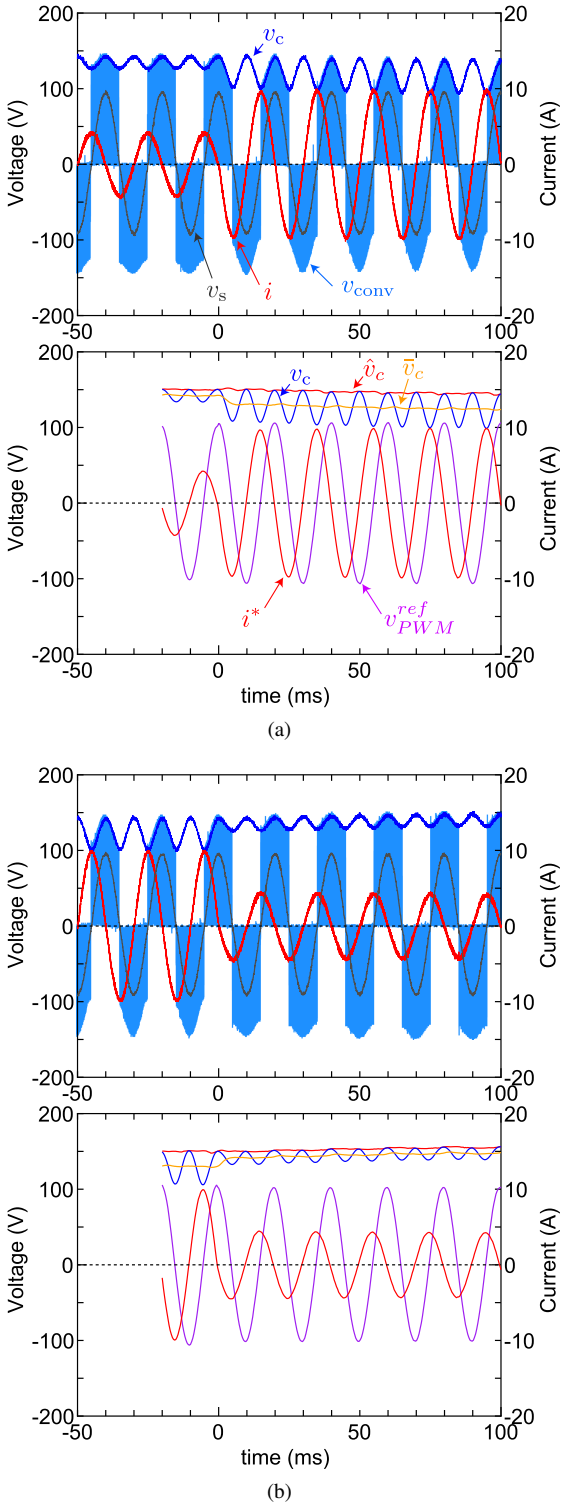


Fig. 12. Measured waveforms (top) and control variables (bottom) when step change is applied in capacitive operation. (a)3 A to 7 A. (b)7 A to 3 A.

measured. Variables in the DSP controller were also measured. Both of the oscilloscope waveforms and control variables in the DSP were sampled with a common trigger. In the experiments, step changes were applied only at the current zero crossing, as discussed in section III-C.

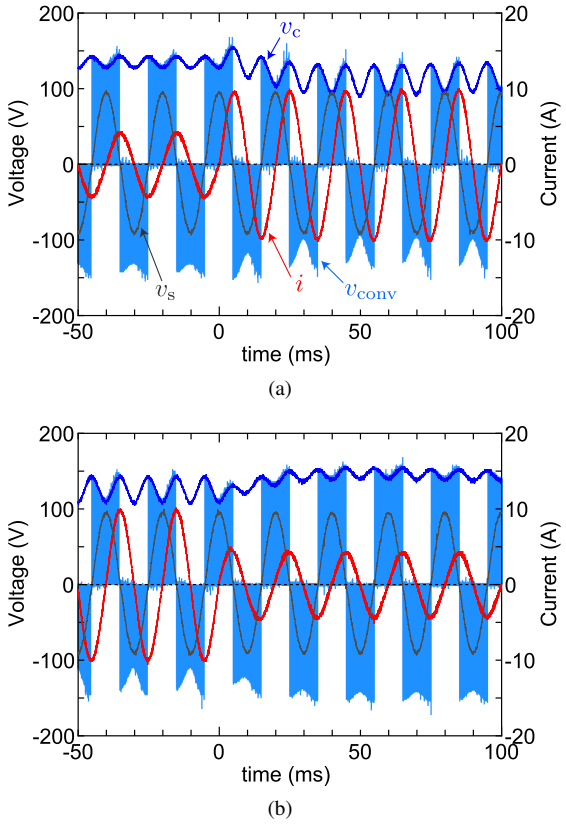


Fig. 13. Measured waveforms when step change is applied in inductive operation without feed-forward control for transient. (a)3 A to 7 A. (b)7 A to 3 A.

Fig. 12 shows the results when the step changes were applied within the capacitive operating range. The capacitor peak voltage estimation $\hat{v}_c$ was almost constant while the transient, and changes in other waveforms were also smooth. After the current was increased, the peak capacitor voltage showed a small transient decrease; however, it became the same voltage as original after a few tens of cycles. Similarly, the peak capacitor voltage increased slightly after the current was decreased. These responses seem to be caused by increased or decreased losses in the circuit, and a delay of the capacitor voltage feedback control were observed.

Fig. 13 shows the results within the inductive operating range without the proposed active power feed-forward control. In contrast to the capacitive operation, the first peak voltage after the step change increased significantly above the set-point value when the current amplitude was increased. Similarly, the peak voltage noticeably decreased when the current amplitude was decreased. Then dc voltage controller was compensating for this initial response, but could only return to the set-point value for the peak voltage after several cycles.

Fig. 14 shows the results with the proposed feed-forward control method in inductive operation. The significant increase or decrease in the first peak of the dc voltage as observed without hte feed-forward control were effectively avoided. However, a slight voltage decrease could be observed after the current set-point was increased, and a slight voltage increase resulted from the decrease of the current set-point, and this

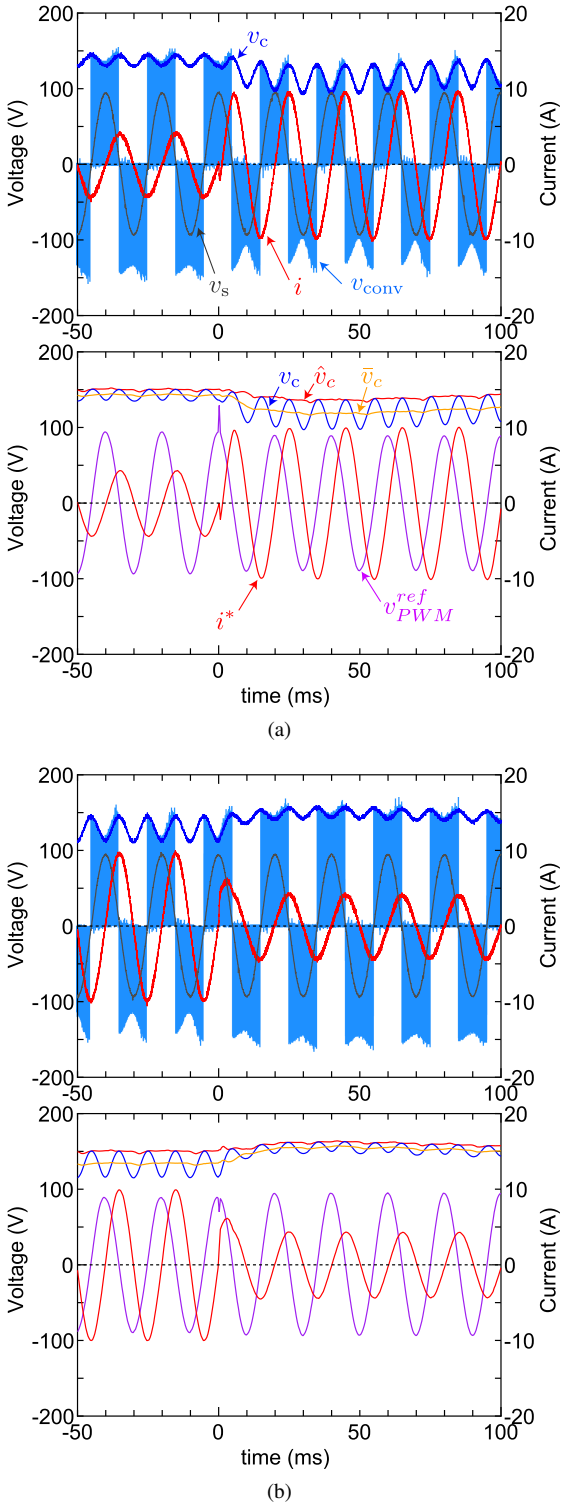


Fig. 14. Measured waveforms when step change is applied in inductive operation with the feed-forward control for transient. (a)3 A to 7 A. (b)7 A to 3 A.

smoother transient response lasted for several cycles until steady-state operation at the dc voltage peak value set-point was reached. These transients were similar to the long term response without the feed-forward control as seen in Fig. 13, but the maximum initial over- or under-voltage was effectively

avoided. Further tuning of the controller gains could also improve the slower transient response, both with and without the feed-forward control.

VI. Conclusion

This paper proposed a control method for dc peak voltage regulation in a single-phase STATCOM with reduced capacitance. The proposed control method has been verified by simulations and laboratory experiments. Steady-state operations in both capacitive and inductive operation were confirmed. The reduced capacitance causes some challenges, since it increases the requirements for the dc voltage control loop. This paper only discusses the step-change applied at the current zero-cross. In the capacitive operation, that situation does not require any exchange of the active power, which is the average of the instantaneous power in a half cycle, for keeping the peak voltage at a constant. Thus a smooth transient without any significant over- or under-shoot in the dc voltage is obtained. On the other hand, in the inductive operation, some active power must be exchanged to keep the peak voltage at its set-point value. An active power feed-forward control was proposed in this paper for improving the response to step-changes or fase variations in the reactive current. The concept can be extended to more general situations. If the step-change can be applied at any phase, this active power exchange is needed also for the capacitive operation.

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