Rene A. Barrera-Cardenas

Meta-parametrised meta-modelling approach for optimal design of power electronics conversion systems

Application to offshore wind energy conversion systems

Thesis for the degree of Philosophiae Doctor

Trondheim, June 2015

Norwegian University of Science and Technology
Faculty of Information Technology,
Mathematics and Electrical Engineering
Department of Electric Power Engineering

NTNU – Trondheim
Norwegian University of
Science and Technology

NTNU
Norwegian University of Science and Technology

Thesis for the degree of Philosophiae Doctor

Faculty of Information Technology, Mathematics and Electrical Engineering
Department of Electric Power Engineering

978-82-326-0872-0 (print)
978-82-326-0873-7 (digital)
1503-8181

Doctoral theses at NTNU, 2015:108

Printed by NTNU Grafisk senter

Acknowledgements

This thesis describes the work undertaken as part of my Ph.D., which was conducted at the Department of Electric Power Engineering, at the Norwegian University of Science and Technology (NTNU) over a four year period (between 2011 and 2015). This work was financially supported by the Research Council of Norway, and the project was defined as part of Work-Package 4 in the Norwegian Research Centre for Offshore Wind Technology (NOWITECH).

I would first like to thank my supervisor Professor Marta Molinas for giving me the opportunity to explore this interesting topic and for her faith in my ability to complete successfully the Ph.D. study program. Her support, advice and guidance have been important for both my development and motivation. I could not have had a better supervisor.

I would like to thank my beloved wife, Myshelle, for her tender support, motivation and patience over these past years. Her positive attitude towards any situation that life presents has taught me that I am able to overcome any obstacle that stands in my way.

I am also grateful to all my colleagues at the Department of Electric Power Engineering with whom I had the opportunity to discuss academic matters and spend memorable times during various social events.

My deepest gratitude goes to my mother and my grandparents. Without their support and sacrifices, I would not be where I am today.

Finally, I would also like to thanks to my best friend, German, and also Juan Jose for encouraging me to apply to this Ph.D. project in this beautiful country called Norway.

I would like to dedicate my work to

my beloved wife Myshelle

Abstract

In an offshore environment, the efficiency (η), the power density (ρ) and the power-to-mass ratio (γ) are of paramount importance in the design of wind energy conversion systems (WECS). Indeed, the optimisation of these performance indices can reduce investment costs, especially if most of the electrical conversion components are located in the nacelle or tower of the wind turbine. This thesis describes a simple procedure to calculate the η, the ρ and the γ of power converters via the calculation of power losses, volume and mass of the main components of the WECS: the power electronics valves, the magnetic components and the capacitors.

In the proposed method, the system is first characterised, then a set of figures of merits are evaluated for a set of design parameters. Finally, a multi-objective optimisation is performed and the Pareto concept is used to present the set of solutions (for different sets of parameters) and the best trade-off for the performance indicators is identified. The approach does not identify a unique solution; instead, several solutions are obtained and other criteria can be used to choose the final solution, thus giving freedom in the design process and flexibility in the final decisions of conceptual design.

The proposed method is applied to different offshore WECS topologies to illustrate the evaluation procedure. First, a well known topology used in AC-Grid connected wind turbines, the two level voltage source converter, is considered. Then, the meta-parametrised approach and the fundamental component models described in this thesis are used to compare six different WECS based on a medium frequency transformer for a 10 MW WECS interfacing a permanent magnet synchronous generator suitable for offshore DC-grids. A modular approach in the power converter is considered and the impact of the number of modules and variation in nominal transformer frequency on performance indicators is studied.

The proposed approach can be applied to identify key components/parameters to optimise a standard solution, to quantify the impact of a new component technology on state-of-the-art solutions for a given application, or to determine, at least in part, the best solutions for new applications regarding state-of-the-art converter topologies, modulation strategies, component technologies and system parameters.

Contents

List of Tables

List of Figures

List of Abbreviations

2L-VSC Two-Level Voltage Source Converter

3L-NPC Three-Level Neutral Point Clamped

B2B Back-to-Back

B2B1p Back-to-Back converter with single-phase square waveform

B2B3p Back-to-Back converter with sinusoidal output waveform

B2B3pSq Back-to-Back with Three-Phase Squared waveform

CSO Current Source Operation

CSR Current Source Rectifier

DMC Direct Matrix Converter

FB Full-Bridge

FBD Full-Bridge Diode Rectifier

IEGT Injection Enhanced Gate Transistor

IGBT Insulated Gate Bipolar Transistor

IGCT Integrated Gate Commutated Thyristor

IMC Indirect Matrix Converter

ISV Indirect Space Vector

MC Matrix Converter

MFT Medium Frequency Transformer

NOWITECH Norwegian Research Centre for Offshore Wind Technology

PMSG Permanent Magnet Synchronous Generator

PWM Pulse Width Modulation

RMC Reduced Matrix Converter

RMS Root Mean Square

SAB Single Active Bridge

SFTM Symmetrical Flat-Top Modulation

SPWM Sinusoidal Pulse Width Modulation

SST Solid State Transformer

SVM Space Vector Modulation

SVPWM Space Vector Pulse Width Modulation

VSC Voltage Source Converter

VSI Voltage Source Inverter

VSR Voltage Source Rectifier

WECS Wind Energy Conversion System

WT Wind Turbine

Part I

Background

Chapter 1

Introduction

Wind energy conversion systems (WECS) are being developed to meet demands for higher efficiency (η, 'eta') and power density (ρ, 'rho') [3, 4, 5, 6, 1]. These requirements can be satisfied through the use or development of new converter topologies, modulation strategies, new semiconductor technologies and new materials in the magnetic or capacitive elements of the system. The improvement in performance decreases over time following the establishment of the new concept or technology. After the basic concept has been adopted, a significant gain in performance can only be achieved by allocating the optimal values of design variables during the design process. Indeed, by analysing the influence of the component parameters on the performance of the system, the development of components may be adjusted to ensure optimal performance [7, 2].

One of the most important technological challenges related to the optimisation of offshore WECS is the demand for higher η and ρ because the maximisation of these two performance indices are two conflicting objectives. A high ρ implies a compact solution. Here, the operational frequency of the converter plays an important role because an increase in the switching frequency allows the volume of passive elements to be reduced and enables the use of a Medium Frequency Transformer (MFT) in the intermediate stages of the converter. However, an increase in the operation frequency of the converter implies higher switching frequencies in the power electronic components, which will generate higher switching losses and therefore deteriorate the η of the system.

To define an optimal solution, first a complete model of the converter circuit must established, including thermal and magnetic component models. This model may be based on analytical equations, numerical simulations or a combination of both.

Analytical models enable fast calculation but are more complicated and/or more time consuming to develop. In addition, they cannot be easily adjusted to different topologies or modulation schemes. Simulations are fairly flexible but may require substantial computational effort, to the point of becoming a non-viable option. To reduce the burden of the computation, meta-modelling can be considered. Basically, meta-modelling generates a simpler model that captures only the relationships between the relevant input and output variables [8].

Based on a converter circuit model, multiple objectives (e.g. η and ρ) can be optimised. This optimisation process makes good use of all degrees of freedom of a design and can determine the sensitivity of the system's performance based on the η of the power semiconductors or properties of the magnetic core materials. Furthermore, different topologies can be easily compared and inherent performance limits can be identified [9, 10, 11].

This project presents a meta-parametrised meta-modelling method for the design and evaluation of power electronics converters, which is applied to optimise the η, ρ and power-to-mass ratio (γ, 'gamma') of the WECS in offshore Wind Turbines (WTs). The use of the proposed meta-parametrised meta-modelling approach reduces the dimensionality of the problem such that several converter solutions can be compared in the earliest stages of conceptual design. First, analytical and semi-empirical approaches for the design of the main functional elements of a WECS are described and arranged in a linear design process. A set of figures of merits are then evaluated for a set of parameters and design variables and a multi-objective optimisation is performed. The Pareto concept is used to present the set of solutions (for different sets of parameters) with the best trade-off for the performance indicators considered. Therefore, this approach does not produce a unique solution; instead, a set of solutions are obtained and other criteria can be used to choose the final solution, thus giving freedom in the design process and flexibility in the final decisions of conceptual design.

1.1 Objectives

The main objective of this thesis was to develop a design methodology and evaluation approach to optimise the ρ and η of a given WECS in offshore WTs. This main objective can be broken down into several smaller objectives:

- To propose a model to evaluate the power losses, volume and mass of the main components of a WECS. The considered elements of the system are: Insulated Gate Bipolar Transistor (IGBT) based power electronic switches, DC and AC bank capacitors, filter Inductors and MFT.

- To detail a multi-domain design process of a WECS for a given topology and modulation scheme.
- To adapt an optimisation methodology to the multi-domain design process to determine the Pareto-Front of η and ρ for a given technology of WECS suitable for offshore WTs.
- To compare different converter topologies to establish which one is most suitable for offshore WECS.
- To identify the main parameters to be taken into account when designing offshore wind converters to improve the component oriented standard approach for onshore turbine modelling and to optimise the operation performance and stringent requirements such as size/weight and η for offshore installations.

1.2 Scope

This project is focused on the modelling and design of high power electronics systems and their application to WECS that interface WT generators in offshore wind applications. The research in this thesis was developed in light of the need for a method to evaluate power electronics converters at the earliest stage of conversion system design. The engineering design process behind of production and marketing of commercial converter solutions is complex and involves multiple stages and a lot of feedback; thus, it is impossible to cover all these stages in just one Ph.D. thesis.

To delimit the scope of this thesis, let's consider the basic engineering design process flowchart presented in Figure 1.1. When a market need is expressed, the process to develop a feasible solution goes from conceptual design (research and exploration) to the detailed design (prototyping and testing). First, background research (stage 2 in Figure 1.1) is done to identify past work, including existing solutions to similar problems (e.g. power converter solutions implemented in onshore wind applications are the most relevant solutions for offshore wind applications). Then, in a third step, the minimum requirements for the solutions are established, and the design criteria and constraints for the solution are decided upon.

When the basic operating conditions and main guidelines for the design have been defined, possible solutions should be explored. In this stage, designers should try as many possible solutions as they can, and compare the results of each one. Some performance indices are taken into account during this comparison and the best solutions are then chosen. The selected solutions are analysed in more detail and

are then compared again to choose the best solution regarding the performance indices considered in the application.

Following the identification of the best possible solution, the development phase can begin (stage 6 in Figure 1.1), in which the system is analysed in detail based on complex models of the converter. Here, the manufacturing specifications are identified and evaluated for each component of the system. A prototype of the solution is then constructed, analysed and tested to determine whether the solution meets the requirements of the application. If the solution satisfies the requirements, then it progresses to the production and marketing stage, which ends with the solution being made available to the final customer. If the solution does not meet the application requirements, then based on results and data, the solution is redesigned or the search of the solution is refined to find other alternatives. Steps 6 to 11 in Figure 1.1 are recursive, implying an iterative process, which is time consuming.

From conceptual design to preliminary design, the modelling of the different possible solutions is intensified progressively. In the earliest stages of conceptual design, the main objective is to explore various solutions while focusing on the diversification and not the intensification of the solution; therefore, the use of meta-models at the conceptual design stage appears to be a smart choice. The focus of this thesis is to provide an approach for the design and evaluation of power electronics system at the earliest phase of stage 4 in Figure 1.1, which implies the use of a simpler model that captures only the relationships between the relevant input and output variables, thus avoiding the complex and time-consuming design algorithms for the power electronics components. The comparative analysis is based on three performance indices, the power losses, volume and mass of the converter, or similarly the η, the ρ and the γ, which are defined in section 2.3.

1.3 Main contributions

The main contribution of this Ph.D thesis is the development of a systematic method to search for the optimal parameters and design variables in the conceptual design of energy conversion systems comprising power electronic and magnetic components. In this thesis, a system model reduction (meta-modelling) is performed by meta-parametrising the stage of conversion. This new knowledge enables the search for an optimal design solution for multi-domain systems at an early stage of the design process. By using this approach, a multi-domain design method has been developed for an offshore WECS composed of several stages of conversion with several domains (technologies) for AC and DC types of offshore collection grid.

The conceptual design approach calculates the η, the ρ and the γ of offshore WECS

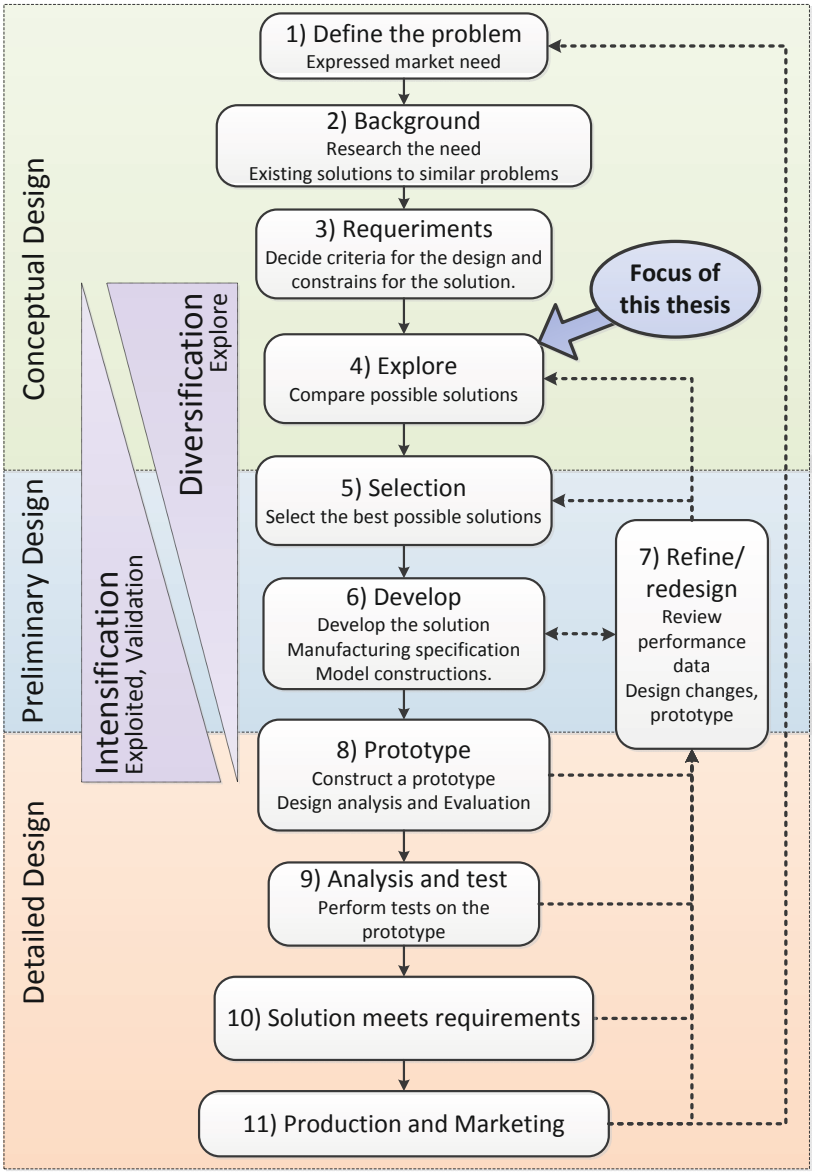


Figure 1.1: Basic flowchart of engineering design process

by calculating the power losses, volume and mass of the main components of the WECS. The performance indices are obtained for a set of design parameters and constraints. Furthermore, this thesis proposes the use of the Pareto-Front as a method to compare WECS by identifying their figures of merit.

In addition, the specific contributions of this thesis are:

- **Comparative analysis of a WECS:** The meta-parametrised approach and the fundamental component models presented in this thesis, which are used to evaluate the power losses, volume and mass of six different WECS based on MFT, are also applied to perform a comparative study for a 10 *MW* WECS with a permanent magnet synchronous generator (PMSG) suitable for offshore DC-grids. A modular approach in the power converter is considered and it is shown how the number of modules and variation in transformer frequency affects the performance indicators.

- **Meta-Parametrised Meta-Modelling Approach:** This thesis describes a simple procedure to calculate the η, the ρ and the γ of high power converters for offshore WTs via the calculation of power losses, volume and mass of the main components of the WECS: the power electronics valves, the magnetic components (AC and DC filter inductors), the capacitors (DC-link capacitors and AC filter capacitors) and the MFT. A base topology known as the two level voltage source converter (2L-VSC) is considered to illustrate the evaluation procedure. The nominal η, the ρ and the γ are obtained for a set of design parameters and constraints. Furthermore, the $\eta - \rho$ Pareto-Front and the $\rho - \gamma$ Pareto-Front are considered to compare different design parameters. Additionally, this thesis proposes the use of Pareto-Front as a method to compare wind energy converters at the earliest stage of design.

- **Switch valves:** Power switch valves based on IGBT semiconductors have been considered; however, the models can be easily extended to include other types of semiconductor. Given that the models used include parameters to quantify how the connection of devices in parallel affects semiconductor losses, low rating devices connected in parallel can be considered to reach the required current rating. Furthermore, the main parameters of the system are identified and the characterization of a semiconductor technology is proposed. These hybrid models enable the identification of the most relevant semiconductor parameters in a given application and assign them as an input/requirement for the development of future or new types of semiconductor devices.

- **Passive components:** Models to evaluate the power losses, volume and

mass of inductors and capacitors used in power electronics converters are presented. These models are based on a meta-parametric approach of the component technology, which enables iterative algorithms normally involved in the design of these components to be avoided. The inductor models developed in these thesis have never been proposed before, and new lines of research can be explored based on this idea.

- **Medium frequency transformer**: Although a reduced model to evaluate the volume and mass of the MFT has not been presented, a reduced but accurate design algorithm has been developed and validated against state-of-the-art transformer designs reported in the literature.

1.4 List of publications

Journal papers

- R. Barrera-Cardenas and M. Molinas, "Comparative study of wind turbine power converters based on medium frequency AC-link for offshore DC-Grids," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. PP, pp. 265–273, September, 2014. Reference [12]

- R. Barrera-Cardenas and M. Molinas, "Multi-objective design of a modular power converter based on medium frequency AC-link for offshore DC wind park," Energy Procedia, vol. 35, pp. 265–273, January, 2013. Reference [13]

- R. Barrera-Cardenas and M. Molinas, "Optimal LQG controller for variable speed wind turbine based on genetic algorithms," Energy Procedia, vol. 20, pp. 207–216, January, 2012. Reference [14]

- R. Barrera-Cardenas and M. Molinas, "A simple procedure to evaluate the efficiency and power density of power conversion topologies for offshore wind turbines," Energy Procedia, vol. 24, pp. 202–211, January, 2012. Reference [15]

Book chapters

- R. Barrera-Cardenas and M. Molinas; "Chapter 29: Modelling of Power Electronic components for evaluation of efficiency, power density and power-to-mass ratio of offshore wind power converters", in the book "Offshore wind farms: Technologies, design and operation"; Elsevier, Woodhead Publishing (in press).

Full papers in conferences

- R. Barrera-Cardenas and M. Molinas, "A comparison of WECS based on medium frequency AC-link for offshore DC wind park," in POWERTECH, 2013 IEEE Grenoble, pp. 1–7, France, June, 2013. Reference [16]

- R. Barrera-cardenas and M. Molinas, "Wind energy conversion systems for DC-series based HVDC transmission", in XV ERIAC - CIGRE, Brazil, May, 2013. Reference [17]

- R. Barrera-Cardenas and M. Molinas, "Comparison of wind energy conversion systems based on high frequency AC-Link: three-phase vs. single-phase," in Power Electronics and Motion Control Conference (EPE/PEMC), 2012, pp. LS2c.4–1 –LS2c.4–8, Serbia, September, 2012. Reference [18]

- R. Barrera-Cardenas and M. Molinas, "Optimized design of wind energy conversion systems with single-phase AC-link," in 2012 IEEE 13th Workshop on Control and Modelling for Power Electronics (COMPEL), pp. 1 –8, Japan, June, 2012. Reference [19]

- R. Barrera-Cardenas and M. Molinas, "Comparative study of the converter efficiency and power density in offshore wind energy conversion system with single-phase transformer," in 2012 International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM), pp. 1085 –1090, Italy, June, 2012. Reference [20]

- R. Barrera-Cardenas, N. Holtsmark, and M. Molinas, "Comparative study of the efficiency and power density of offshore WECS with three-phase AC-link," in 2012 3rd IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG), pp. 717 –724, Denmark, June, 2012. Reference [21]

Poster/Oral presentations

- R. Barrera-Cardenas and M. Molinas, "Optimal Design of a Modular Power Converter Based on Medium Frequency AC-Link for Offshore Wind Turbines", poster presentation in EERA DeepWind'2015-12th Deep Sea Offshore Wind R&D conference, Trondheim, Norway 2015.

- R. Barrera-Cardenas and M. Molinas, "Analysis and design of an AC/DC converter for offshore wind turbines", oral presentation in EERA DeepWind'2014-11th Deep Sea Offshore Wind R&D conference, Trondheim, Norway 2014.

- R. Barrera-Cardenas and M. Molinas, "Multi-objective Optimization of a Modular Power Converter Based on Medium Frequency AC-Link for Offshore DC Wind Park", oral presentation in EERA DeepWind'2013-10th Deep Sea Offshore Wind R&D conference, Trondheim, Norway 2013.

- R. Barrera-Cardenas and M. Molinas, "Optimized Design of a Modular Power Converter Based on Medium Frequency AC-Link for Offshore DC Wind Park", poster presentation in NOWITECH day 2013, Trondheim, Norway 2013.

- R. Barrera-Cardenas and M. Molinas, "Modular Power Converter Based on Medium Frequency AC-Link for Offshore DC Wind Park", oral presentation in Wind Energy Research at NOWITECH and Fraunhofer IWES Ph.D. Seminar, Bremerhaven, Germany 2013.

- R. Barrera-Cardenas and M. Molinas, "Comparative Study of the Efficiency and Power Density of Offshore Wind Energy Conversion System based on High Frequency AC-Link", poster presentation in NWIN'2012-2nd Nordic Wind Integration Research Network seminar, Helsinki, Finland 2012.

- R. Barrera-Cardenas and M. Molinas, "Optimal LQG controller for variable speed wind turbine based on genetic algorithms", oral presentation in Technoport 2012, Trondheim, Norway 2012.

- R. Barrera-Cardenas and M. Molinas, "Optimization of the Design process of a Wind Energy Conversion System with Single-Phase AC-Link.", poster presentation in NOWITECH day 2012, Trondheim, Norway 2012.

- R. Barrera-Cardenas and M. Molinas, "Incidence of the Switching Frequency on Efficiency and Power Density of Power Conversion Topologies for Offshore Wind Turbines", poster presentation in 9th Deep Sea Offshore Wind R&D conference, Trondheim, Norway 2012.

- R. Barrera-Cardenas and M. Molinas, "Performance Space of Wind Energy Conversion Systems by Regression Curve Losses", poster presentation in NOWITECH day 2011, Trondheim, Norway 2011.

- R. Barrera-Cardenas and M. Molinas, "Smart control wind turbine for MPPT based on LQG methodology", poster presentation in NTNU India Week, Trondheim, Norway 2011.

1.5 Outline of the thesis

The thesis is divided into three parts designed to address the stated problems. The first part Background covers the introduction to the thesis with a short overview and the main objectives, scope and contributions. In particular, this section contains an introduction to the meta-parametrised meta-modelling approach, in which the mathematical abstraction of the analysis of power electronics systems, the Pareto-Front concept and the definition of considered performance indices are also presented.

The second part Modelling of power electronic converter components describes the modelling and parametrisation process performed to evaluate the power losses, volume and mass of the main components of the power electronics converter: the switch valves, the passive elements and the MFT.

The third and last part Application to offshore wind power converters and Conclusion concerns the application of the proposed method and the comparison of the different converter topologies and modulation strategies, along with the conclusions of the accomplished work.

Each part is further divided into several chapters. This structure is outlined in Figure 1.2 on the facing page.

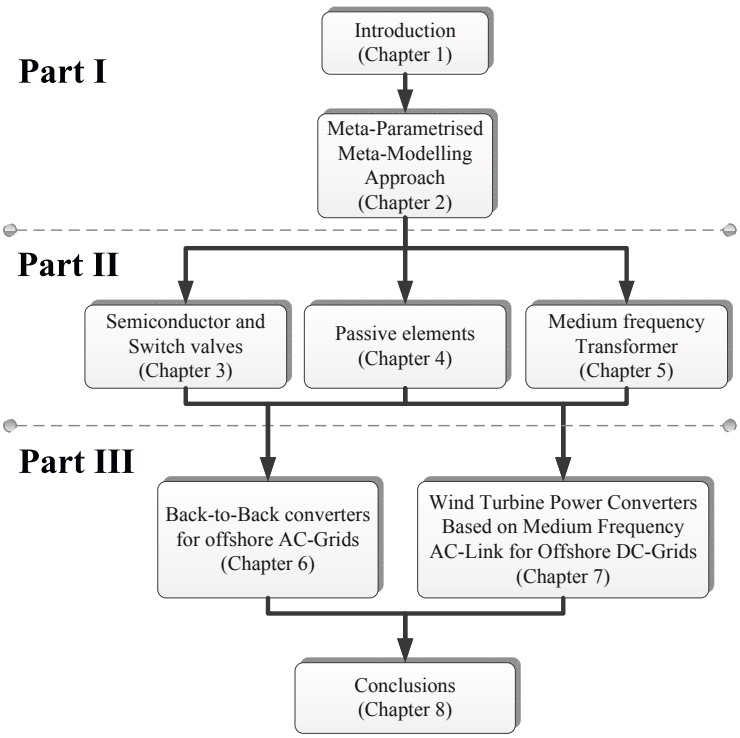


Figure 1.2: The structure of the thesis

Chapter 2

Meta-parametrised meta-modelling approach

2.1 Definition of the problem

This project is focused on the modelling and design of power electronics conversion systems to interface WT generators in offshore wind applications. Generally, in the design of power electronics systems, the choice of components values and operating parameters depends mainly on experiments conducted by development engineers and on earlier product designs. This design process can be supported (and eventually replaced) by mathematical procedures to exploit fully the potential of a given technology. The methodology of this Ph.D. project is based on mathematical modelling and the Pareto-Frontier as explained below.

The mathematical abstraction of power electronics systems presented in [2] is considered to describe this problem. Given the system specifications and operating requirements

$$\vec{r} = \{r_1, r_2, ..., r_l\} \tag{2.1}$$

e.g. input/output voltage, output power, maximum allowed current ripple, minimum power factor at nominal condition, overload factor, over-voltage factor and inter alia, the goal in the design of power electronics systems is to assign values to the free design parameters

$$\vec{x} = \{x_1, x_2, ..., x_n\} \tag{2.2}$$

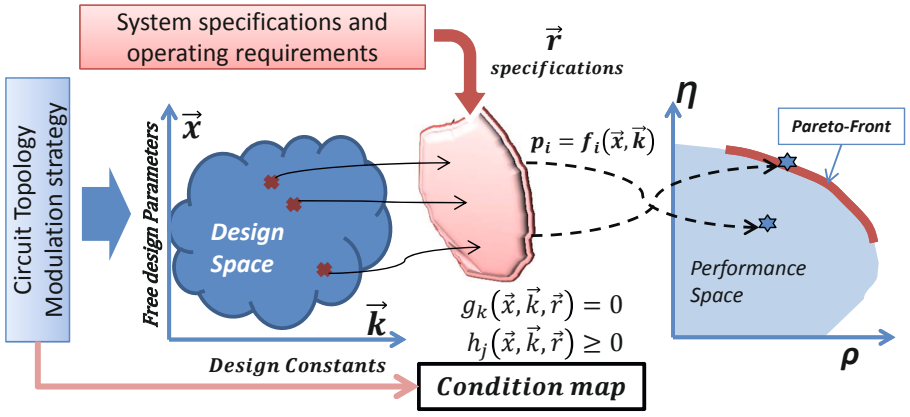


Figure 2.1: The mathematical abstraction of the design of power electronics systems [2].

e.g. circuit component values, operating parameters, turn ratio of the transformer, switching frequency and inter alia, while taking into account design constants

$$\vec{k} = \{k_1,\ k_2,\ ...,\ k_m\} \tag{2.3}$$

e.g. the saturation flux density of magnetic material, maximum temperature increase of magnetic materials and semiconductor devices, maximum blocking voltage of available semiconductor technology and inter alia.

Each possible design solution is then defined by the multi-dimensional design space $\left(\vec{x},\ \vec{k}\right)$, and the performance of each design may be evaluated by calculating performance indices

$$p_i = f_i\left(\vec{x},\ \vec{k}\right) \tag{2.4}$$

e.g. η , ρ, active mass, total cost and inter alia, in which the system specification and converter behaviour are included as side conditions

$$g_k\left(\vec{x},\ \vec{k},\ \vec{r}\right) = 0 \tag{2.5}$$

$$h_j\left(\vec{x},\ \vec{k},\ \vec{r}\right) \geq 0 \tag{2.6}$$

Figure 2.1 shows the design of a power electronics system as a mathematical problem, in which a multi-dimensional design space is mapped into a performance space, defined by the performance indices (η, ρ). It can be noted that for a given set of performance indices, the optimal design can be found by searching many possible designs for the solution that maximizes the performance space.

2.2 Multi-objective optimization and Pareto-Front

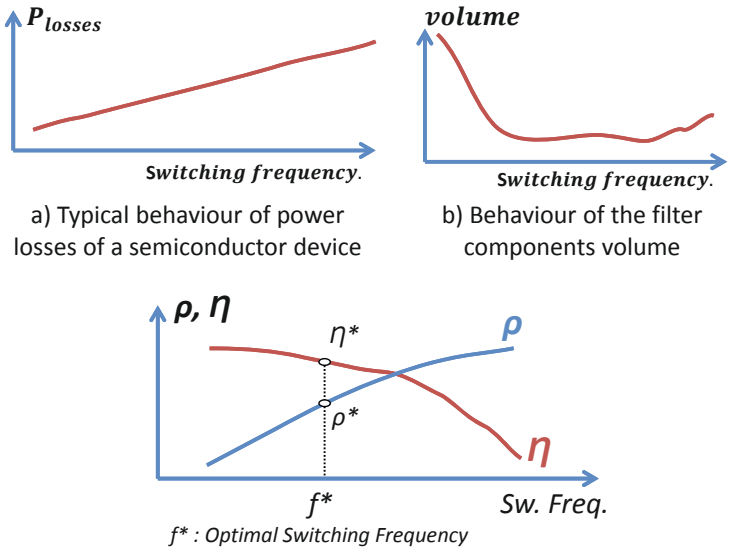
In this context, multi-objective optimization is important because one solution rarely provides the best result for every performance indicator [2]. For example, Figure 2.2a and 2.2b show the typical behaviour of a semiconductor device regarding power losses and the size of the filter passive components that is required to fulfil harmonic limitation as a function of the switching frequency of the converter.

Typically, major losses originate from semiconductor devices and the main volume from the passive components; therefore, the η and ρ (for illustration purpose only) of this power converter can be roughly estimated based on Figure 2.2a and 2.2b, as shown in Figure 2.2c. It is clear from Figure 2.2c that high η and high ρ in power electronics converters are two conflicting objectives. To handle effectively multi-objective solutions, the concepts of Pareto optimality and Pareto-Front were considered. In this context, Pareto optimality can be defined as a state of allocation of performance indices of the possible designs obtained by mapping a set from the design space, in which it is impossible to improve one performance indicator without making at least another worse off [22].

Following the initial allocation of performance indices, a change in the subspace of design to produce a different allocation that makes at least one performance index better off without making any other performance indices worse off is called a Pareto improvement. When no further Pareto improvements can be done, the final allocation is called the Pareto-Front or Pareto-Frontier [23]. By restricting their attention to the set of performance indices in the design space within the Pareto-Front, a designer can make a trade-off within this set, rather than considering the full design space. Figure 2.3 shows a graphical definition of the concept explained above.

2.3 The considered performance indices

In an offshore environment, the WECS must be designed to take into account not only efficiency and reliability, but also size and weight, because expensive platforms are required to support each new component. Therefore, the performance indices η, ρ and γ are of paramount importance to reduce investment costs, especially if most of the electrical conversion components are going to be located in



a) Typical behaviour of power losses of a semiconductor device

b) Behaviour of the filter components volume

c) Rough estimation of efficiency and power density of a basic power converter

Figure 2.2: Example of power electronics converter typical trade-off between η and ρ when optimal design is searched by the selection of the switching frequency.

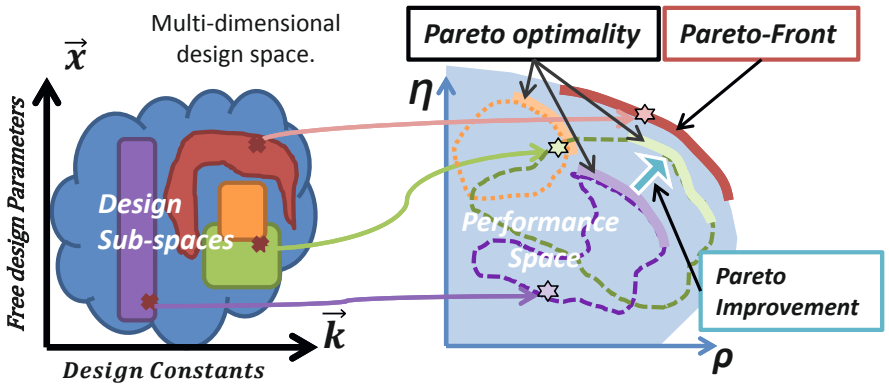


Figure 2.3: Graphical definition of Pareto-optimality, Pareto improvement and Pareto-Front

the nacelle or tower of the WT.

The efficiency (η, 'eta') of an electrical system is the ratio of power output and power input (P_{in}), defined by equation (2.7). The power output can be expressed as the difference between power input and the total losses of the WECS, which is expressed by adding the individual losses $P_{loss,(i)}$ of each element of the WECS (e.g. power semiconductors and passive elements like inductors and capacitors).

$$\eta = \frac{P_{in} - \sum P_{loss,(i)}}{P_{in}} \times 100 \tag{2.7}$$

By contrast, the power density (ρ, 'rho') defined by equation (2.8), characterises the degree of compactness of a WECS. Since the power output can be expressed as a function of the power losses, the ρ is calculated by evaluating the total converter volume and power losses of the system. The total converter volume (Vol_{Total}) is obtained by adding the individual volumes $Vol_{(i)}$ of the components and the use of the Vol_{Total} by active parts is characterized by the volume utilisation factor C_{PV}, the value of which typically ranges between 0.5 and 0.7. [2]

$$\rho = \frac{P_{out}}{Vol_{Total}} = \frac{P_{in} - \sum P_{loss,(i)}}{\frac{1}{C_{PV}} \sum Vol_{(i)}} \tag{2.8}$$

The WECS should be located in the nacelle, tower or pillar of the WT, so the weight of the converter is also relevant for the comparison of different solutions. The power-to-mass ratio (γ, 'gamma') defined by equation (2.9), indicates the heaviness of the WECS. Like the total converter volume, the total converter active mass W_{Total} is calculated by adding the individual masses $W_{(i)}$ of the components.

$$\gamma = \frac{P_{out}}{W_{Total}} = \frac{P_{in} - \sum P_{loss,(i)}}{\sum W_{(i)}} \tag{2.9}$$

One of the most important technological challenges related to the optimisation of offshore WECS is the demand for high η and ρ; however, maximisation of these performances indices are two conflicting objectives. A high ρ implies a compact solution. The operational frequency of the converter can play an important role here because an increase of switching frequency enables the volume of passive elements to be reduced. However, higher frequencies in the power electronic semiconductors will generate higher switching losses and therefore deteriorate the η of the system.

Additionally, these performance indices are influenced by several parameters such as the rated power, the switching frequency, the voltage level, the converter topology, the modulation technique, the technology of each of the elements in the converter (semiconductors, inductors, capacitors), and inter alia. A comprehensive process of optimisation is necessary to find the most suitable solutions. Volume, mass and power-loss models are necessary to evaluate the component scaling depending on parameter variation.

To find the values of the free design parameters that produce the best design regarding the given design objective (e.g. maximum η, maximum ρ, minimum mass), an automatic optimisation procedure must be performed [2]. The optimisation procedure in this study is based on the complete model of the converter circuit including multi-domain component models. This model could be based on analytical equations, numerical simulations or a combination of both. Furthermore, a method must be defined to calculate the performance indices of the design objective based on design variables.

2.4 Main power electronic components

In this Ph.D. project, the above explained systematic methodology based on components and sub-system modelling has been applied to evaluate the ρ, γ and η of the entire WECS. The system is characterised using a hybrid approach based on empirical modelling, analytical equations, numerical simulation or a combination of them depending on the availability of information and complexity of the power electronics topologies and modulation schemes. First, the circuit electrical waveforms of the main components are obtained as a function of the circuit parameters. This information and a set of design guidelines are then combined with empirical modelling based on the properties of physical components and/or data-sheet information provided by manufacturers to evaluate the power losses, volume and mass of the system.

This process was carried out for key components in state-of-the-art and future high power converters. Three main groups of components were identified: power converter units with power semiconductor devices, passive components (inductors and capacitors) and MFT. Power semiconductor valves based on IGBT devices have been considered, and detailed models have been described to include parameters quantifying the effects of devices connected in parallel to reach the current rating. State-of-the-art IGBT power modules have also been characterised. The inductive and capacitive components were modelled based on commercial elements (data-sheet information) and analytical formulations, which enables different technologies and materials to be considered while maintaining accuracy in the evaluation of the performance indices. A simplified design process of MFT to estimate

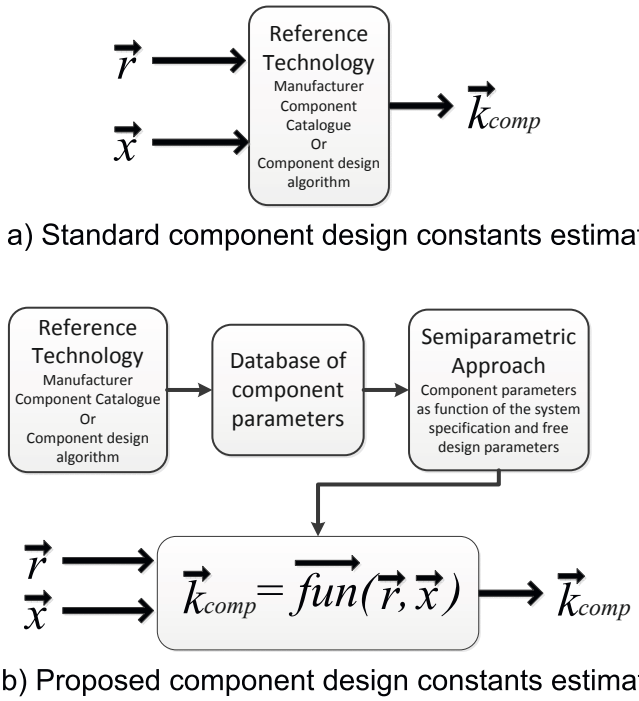


Figure 2.4: Component design constants estimation

the performance indices has been developed, which takes into account the main constraints and leaves a degree of freedom in the key design parameters.

2.5 Proposed component meta-modelling structure

To estimate accurately the volume/mass of power electronics components, a complex design algorithm normally has to be run, which is time-consuming. Moreover, power losses are component dependent, which means that some components are more convenient for some topologies than others. The selection of components depends on the specifications, operating requirements ($\vec{r}$) and the free design parameters ($\vec{x}$) of a given system. This selection determines some of the design constants ($\vec{k}$), and therefore equation (2.3) can be expressed as follows:

$$\vec{k} = \left[\vec{k}_{Comp}, \vec{k}_{NonComp}\right] \tag{2.10}$$

where $\vec{k}_{Comp}$ are the design constants which are component dependent and $\vec{k}_{NonComp}$ are the design constants which are component independent. The component mod-

elling structure proposed here provides a simple way to evaluate the component design constants $\vec{k}_{Comp}$, without running a complex algorithm or basing the selection of the component on the availability in the manufacturer's catalogue.

Figure (2.4) shows the standard (Figure (2.4)a) and the proposed (Figure (2.4)b) method for estimating the parameters of the components. The proposed estimation is based on a parametric approach, which analyses a component database and uses an empirical model based on physical properties to express the component parameters or $\vec{k}_{Comp}$ as a function of $\vec{r}$ and $\vec{x}$. The database can be created from a reference technology described in a manufacturer's catalogue or from the parametric sweep of a component design algorithm. With these approaches, it is possible to parametrise a component technology and therefore compare different technologies and their impact on converter topologies (e.g. different semiconductor types, generations and/or manufacturers, magnetic core materials, inductor shapes and inter alia).

Part II

Modelling of power electronic converter components

Chapter 3

Semiconductor and Switch Valves

Switch valves in power electronic converters are arrays of power semiconductor devices (connected in parallel or in series) with a cooling system. Ideally, arrays of low rating devices connected in parallel or in series are very efficient because of the high η of low rating semiconductors. However, combinations of series and parallel connections in semiconductors are rare in real-world applications; instead, high rating devices are connected in parallel at the low-voltage side of the converter, whereas at the high-voltage side, semiconductor devices are connected in series to reach the required blocking voltage.

This chapter presents the models used to evaluate the power losses of a semiconductor device and discusses how the connection of semiconductors in parallel or in series influences these losses. In addition, this chapter discusses models to evaluate the volume/mass of the valve and the cooling system based on the power losses of the semiconductor module and its average thermal model. Finally, the parameters of the semiconductor are summarised for each model and examples of the parameters for the most common power devices used in wind energy applications are given.

3.1 Semiconductor power losses

The power semiconductors used in power converters are operated mostly as switches, and take on two possible static states, conducting or blocking, and two possible transition states, “turn-on action” and “turn-off action”. Each of these states generates one energy dissipation component, which heats the semiconductor and adds to the total power dissipation of the switch. Figure 3.1 shows the simplified device switching waveforms (voltage and current) and the power losses associated with

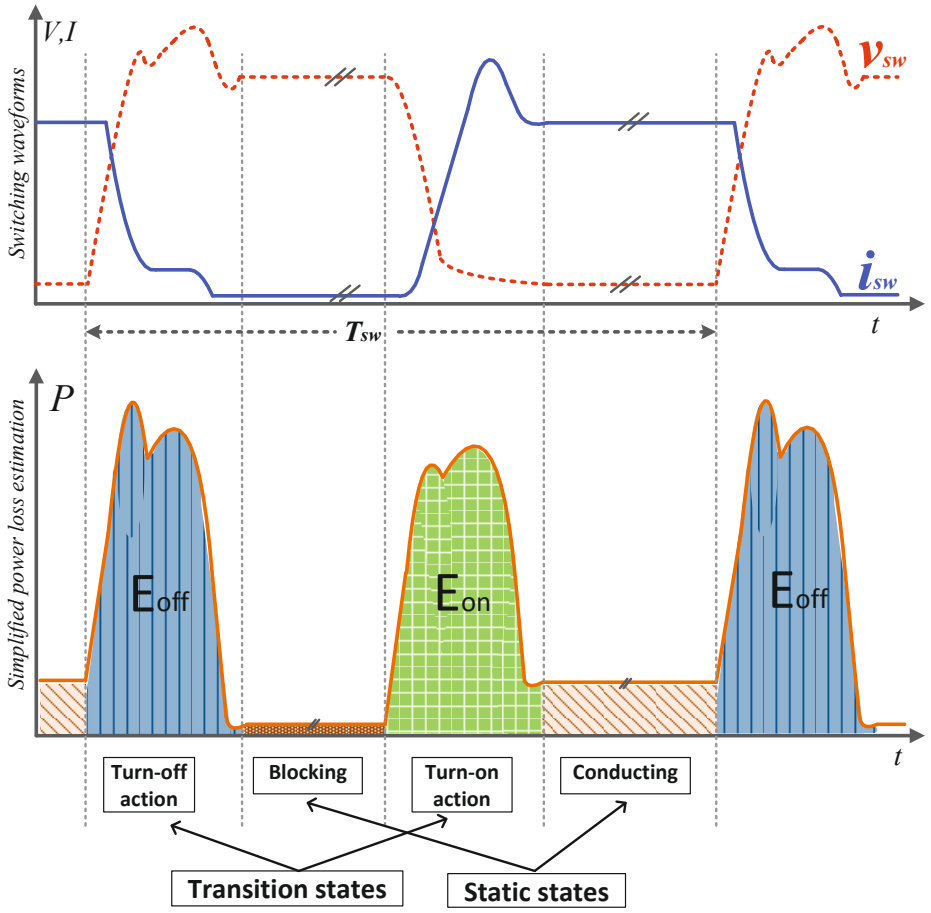


Figure 3.1: Possible states of a semiconductor power switch showing the simplified device switching waveforms and an estimation of power loss.

each possible operation state of the power switch.

3.1.1 Conduction losses

Static losses are determined by the non-linear voltage-current characteristic of the semiconductor device. A typical voltage-current characteristic of a power semiconductor device is shown in Figure 3.2. The two static states or regions can be noted from Figure 3.2. The blocking state ($v_{sw} < 0$) has much smaller currents than the nominal current of the device, whereas the conducting state ($v_{sw} > 0$) is characterised by small voltages (compared with the nominal blocking voltage) for currents smaller than maximum current of the device.

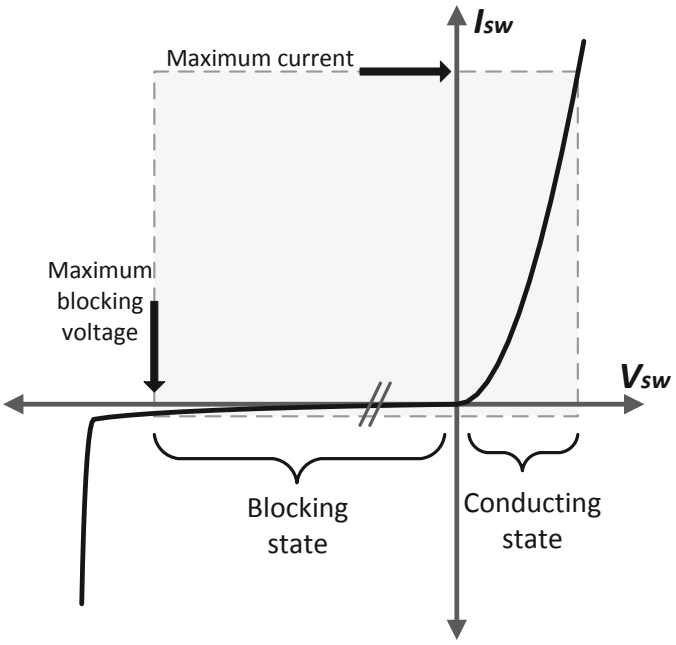


Figure 3.2: Typical voltage-current characteristics of a semiconductor device

The instantaneous power losses of the semiconductor at static state can be calculated as the product of the device voltage (v_{sw}) and the device current (i_{sw}). When the switch is in blocking state, the device has a very small current (thousands or a million times smaller than the nominal current) for any voltage lower than the nominal blocking voltage of the semiconductor device. In this case, blocking losses only make up a small share of the total power dissipation and may thus be neglected in power devices [24]. In fact, the voltage-current characteristic in the blocking region is usually not reported by manufacturers of power semiconductor.

The voltage-current characteristic of the power device in conduction state is usually approximated by a linear relationship [25] and the forward on-state voltage of the power semiconductor device can be expressed as a function of the instantaneous device current:

$$v_{sw} = V_{sw0} + R_C \cdot i_{sw} \tag{3.1}$$

The parameters V_{sw0} (threshold voltage) and R_C (on-state resistance) can be calculated using the data sheet for each device. As an example, the characteristic describing the relationship between the voltage and current for both the IGBT and

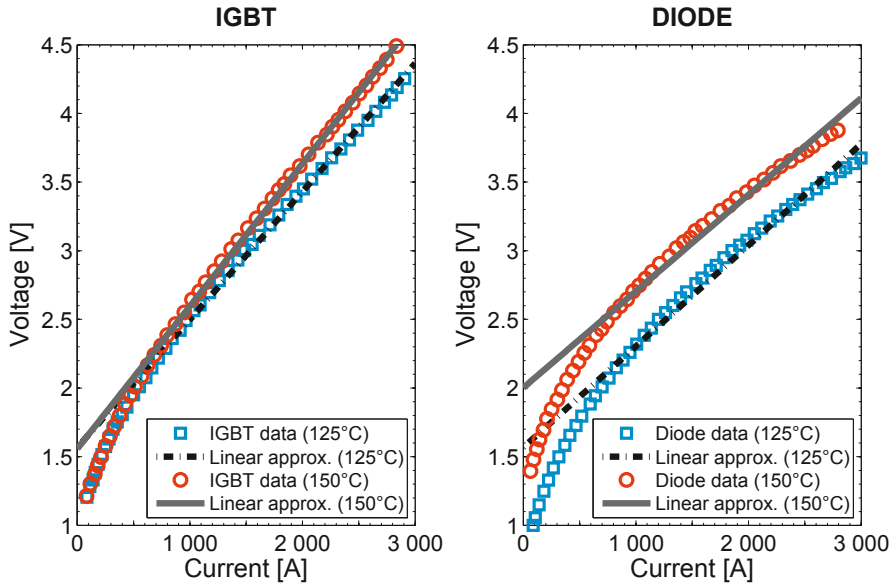


Figure 3.3: Current-voltage conduction characteristics of the power module Infineon FZ1500R33HE3 for two junction temperatures (125 *ºC* and 150 *ºC*).

diode as given in the data sheet of the power module Infineon FZ1500R33HE3 [26] are shown in Figure 3.3. The voltage-current characteristic depends on the junction temperature (T_j) as shown in Figure 3.3, in which two different junction temperatures are considered for each device. A linear approximation is also included for each curve.

To describe the temperature dependency of the curve, the parameters V_{sw0} and R_C can be made temperature-dependent. The order of the approximation depends on the availability of curve data at different operating temperatures. Normally, the data sheet includes data for two or three operating temperatures, so a linear approximation can be made:

$$V_{sw0}(T_j) = V_{sw00} \cdot (1 + \alpha_{Vsw0} \cdot (T_j - T_{j0})) \tag{3.2}$$

$$R_C(T_j) = R_{C0} \cdot (1 + \alpha_{Rc} \cdot (T_j - T_{j0})) \tag{3.3}$$

where α_{Vsw0} and α_{Rc} are the temperature coefficient of threshold voltage and on-state resistance, respectively, T_{j0} is a fixed reference junction temperature, V_{sw00} and R_{C0} are the threshold voltage and on-state resistance at temperature T_{j0}.

When the voltage-current characteristic has been defined, the conduction losses (P_{cond}) can be calculated as the product of the voltage across the device (v_{sw}) and the current that the device is conducting (i_{sw}). The average dissipated power resulting from conduction in each device in one period of time (T) is calculated as:

$$P_{cond} = \frac{1}{T}\int_0^T (v_{sw} \cdot i_{sw})\, dt = \frac{1}{T}\int_0^T (V_{sw0}(T_j) + R_C(T_j) \cdot i_{sw}) \cdot i_{sw} \cdot dt \quad (3.4)$$

Assuming a constant operating junction temperature during the period T, the equation can be simplified as follows:

$$P_{cond} = \frac{V_{sw0}(T_{j,AVG})}{T}\int_0^T i_{sw} \cdot dt + \frac{R_C(T_{j,AVG})}{T}\int_0^T i_{sw}^2 \cdot dt \quad (3.5)$$

$$P_{cond} = V_{sw0}(T_{j,AVG}) \cdot I_{sw,AVG} + R_C(T_{j,AVG}) \cdot I_{sw,RMS}^2 \quad (3.6)$$

where $T_{j,AVG}$ is the average junction temperature, $I_{sw,AVG}$ is the average current, and $I_{sw,RMS}$ is the R.M.S current the device is conducting in a given period. The values of $I_{sw,AVG}$ and $I_{sw,RMS}$ can be calculated based on the input/output current of the converter and mainly depend on the converter topology, modulation strategy and input/output power factor (examples of calculations are presented in part III for different converter topologies and modulation strategies).

3.1.2 Switching losses

By contrast, the transition losses, also called switching losses (P_{sw}), are calculated based on the energy dissipated during commutation, $E_{sw,on}$ and $E_{sw,off}$ for turn on and turn off, respectively. This commutation energy loss mainly depends on the voltage in the switch device at moment before it is turned on (v_{swb}) or after it is turned off (v_{swa}), the current through the switch device at moment after it is turned on (i_{swa}) or before it is turned off (i_{swb}), and the junction temperature of the device (T_j). According to the data commonly reported in the data sheets of the devices, the following model is proposed to calculate the commutation energy loss:

$$E_{sw,on} = E_{sw0,on} \cdot (1 + \alpha_{Eon} \cdot (T_j - T_{j0})) \quad (3.7)$$

$$E_{sw0,on} = v_{swb} \cdot \left(K_{Eon0} + K_{Eon1} \cdot i_{swa} + K_{Eon2} \cdot i_{swa}^2\right) \quad (3.8)$$

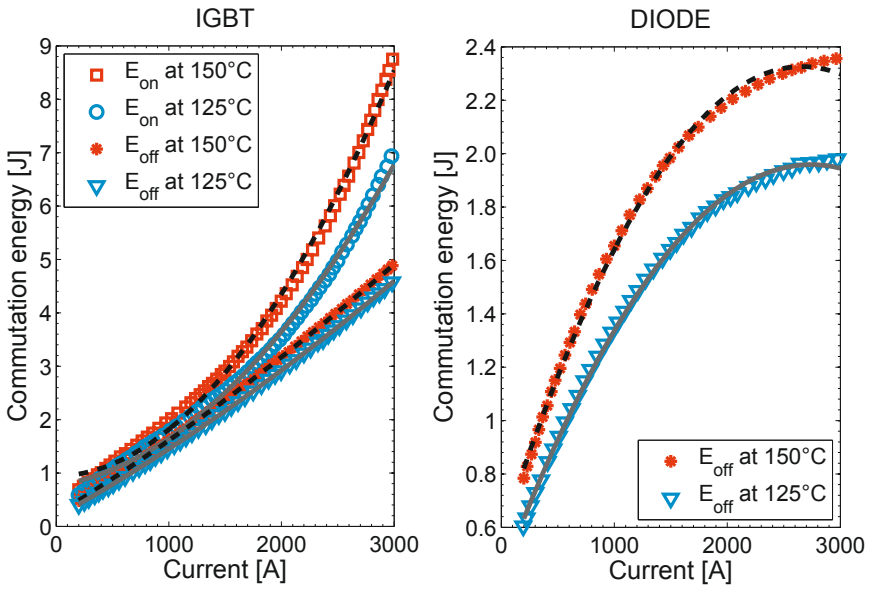


Figure 3.4: Example of the relationship between current and commutation energy loss for the turn-on and turn-off action of the IGBT and diode of the power module Infineon FZ1500R33HE3, as given in the data sheet.

$$E_{sw,off} = E_{sw0,off} \cdot (1 + \alpha_{Eoff} \cdot (T_j - T_{j0})) \tag{3.9}$$

$$E_{sw0,off} = v_{swa} \cdot \left(K_{Eoff0} + K_{Eoff1} \cdot i_{swb} + K_{Eoff2} \cdot i_{swb}^2\right) \tag{3.10}$$

where $\alpha_{Eon/off}$ is called the temperature coefficient of commutation energy loss at turn on/off, T_{j0} is a fixed reference junction temperature, $E_{sw0,on/off}$ is the commutation energy loss at turn on/off and temperature T_{j0}, and $K_{E(on/off)0}$, $K_{E(on/off)1}$, $K_{E(on/off)2}$ are the polynomial regression coefficients used to describe how the current depends on the commutation energy loss at turn on/off. All these parameters can be calculated using the data sheet of the device.

As an example, the characteristic describing the relationship between commutation energy loss and the current of the IGBT and diode as given in the data sheet of the power module Infineon FZ1500R33HE3 [26] are shown in Figure 3.4. The solid lines in Figure 3.4 show the 2nd order polynomial fitting curve as given in equations (3.8) and (3.10). The commutation energy at turn on is not plotted for the diode (right side of Figure 3.4). Manufacturers usually do not report this

characteristic because the switching losses when the power diodes are turned on are very small and therefore neglected.

When the model of commutation energy has been defined, the average switching loss over a complete fundamental period (T) may be determined by summing all the commutations of the device during an interval of time and dividing by that interval. The average switching loss for turn on and turn off can be expressed as:

$$P_{sw,on} = \frac{1}{T} \cdot \sum_{j=1}^{N} E_{sw,on} \tag{3.11}$$

$$P_{sw,off} = \frac{1}{T} \cdot \sum_{j=1}^{N} E_{sw,off} \tag{3.12}$$

where N is the number of switching actions in a fundamental period T, and can be expressed as a function of the switching frequency (f_{sw}) or the switching period (T_{sw}),

$$N = \frac{T}{T_{sw}} = T \cdot f_{sw} \tag{3.13}$$

When the switching frequency is equal to the fundamental period, only one switching action occurs in a fundamental period and equations (3.11) and (3.12) can be expressed as:

$$P_{sw,on} = f_{sw} \cdot E_{sw,on} \tag{3.14}$$

$$P_{sw,off} = f_{sw} \cdot E_{sw,off} \tag{3.15}$$

For applications that have a much lower switching period than fundamental period, the following approximation is possible based on Riemann integral:

$$\int_0^T E_{sw} \cdot dt \approx \frac{T}{N} \cdot \sum_{j=1}^{N} E_{sw} \tag{3.16}$$

and the switching losses for turn on ($P_{sw,on}$) can be expressed as follows:

$$P_{sw,on} = \frac{1}{T} \cdot \frac{N}{T} \cdot \int_0^T E_{sw,on} \cdot dt \tag{3.17}$$

The operating junction temperature ($T_{j,AVG}$) can be assumed to be constant during the period (T), and the voltage in the switch device at the moment before it is turned on (v_{swb}) can be approximated to the blocking voltage of the application (V_{bk}). Thus, the equation can be simplified by putting (3.7), (3.8) and (3.13) in (3.17):

$$E_{sw0,on} = V_{bk} \cdot \left(K_{Eon0} + K_{Eon1} \cdot I_{swa,AVG} + K_{Eon2} \cdot I^2_{swa,RMS}\right) \tag{3.18}$$

$$P_{sw,on} = f_{sw} \cdot E_{sw0,on} \cdot (1 + \alpha_{Eon} \cdot (T_{j,AVG} - T_{j0})) \tag{3.19}$$

where $I_{(swa,AVG)}$ is the average value, and $I_{(swa,RMS)}$ is the Root Mean Square (RMS) value of the current through the switch device at the moment after it is turned on.

A similar procedure can be applied to derive an expression for $P_{(sw,off)}$

$$E_{sw0,off} = V_{bk} \cdot \left(K_{Eoff0} + K_{Eoff1} \cdot I_{swb,AVG} + K_{Eoff2} \cdot I^2_{swb,RMS}\right) \tag{3.20}$$

$$P_{sw,off} = f_{sw} \cdot E_{sw0,off} \cdot (1 + \alpha_{Eoff} \cdot (T_{j,AVG} - T_{j0})) \tag{3.21}$$

where $I_{(swb,AVG)}$ is the average value, and $I_{(swb,RMS)}$ is the RMS value of the current through the switch device at moment before it is turned off . The values of $I_{(swa,AVG)}$, $I_{(swa,RMS)}$, $I_{(swb,AVG)}$ and $I_{(swb,RMS)}$ can be calculated based on the input/output current of the converter and they mainly depend on the converter topology, modulation strategy and input/output power factor. Examples of calculations are presented in part III for different converter topologies and modulation strategies.

3.2 Parallel connection of power modules

Offshore wind converters are required to manage high power ratings. If a low/medium voltage feeds the converter, then a high current should be managed by the power

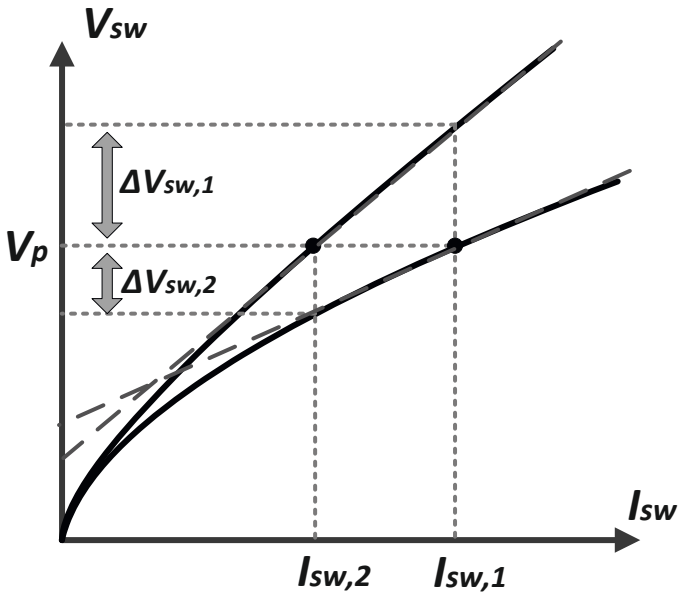


Figure 3.5: Example of current imbalance given by the differences in the voltage-current characteristics of two modules connected in parallel

switches. In this case, the parallel connection of semiconductor modules is considered to be the best option to fulfil the current requirements. The number of modules connected in parallel (n_p) has no limit [27]. However, parallel connection has some disadvantages, like current imbalance in the modules at static state and transition state, which arise mainly because the modules connected do not have identical properties.

The difference in the voltage-current characteristic of the modules is a major factor contributing to current imbalances. The static voltage deviation (ΔV_{sw}) of two modules with the same production reference is given by small variations in the properties of the modules resulting from the fabrication process or by junction temperature differences between modules. Figure 3.5 shows how a difference in the static characteristic of two semiconductors connected in parallel can cause current imbalance. The average current in the parallel connection ($I_{p,AVG}$) can be derived using equation 3.1 to model the voltage-current characteristic of each module. For the sake of simplicity, the threshold voltage is assumed to be equal for the modules ($V_{sw0,1} = V_{sw0,2}$). Thus, $I_{p,AVG}$ can be expressed by:

$$I_{p,AVG} = \frac{i_{sw,1}}{2} \cdot \left(\frac{R_{C,1} + R_{C,2}}{R_{C,2}} \right) \tag{3.22}$$

where $R_{c,1}$ and $R_{c,2}$ are the on-state resistance of each module. When $R_{c,1} < R_{c,2}$, module one has a higher current than module two ($i_{sw,1} > i_{sw,2}$) because of the voltage deviation of the modules (ΔV_{sw}). The maximum voltage deviation ($\Delta V_{sw,max}$) at maximum current ($I_{sw,max}$) can be calculated from the data given in the data sheet of the semiconductor module. Assuming that the deviation between the modules is maximal, and using the same assumptions of equation 3.22, the voltage deviation can be expressed by:

$$\Delta V_{sw,max} = (R_{C,2} - R_{C,1}) \cdot I_{sw,max} \tag{3.23}$$

The current imbalance rate (δ_{CI}), which represents the ratio of shared current in the parallel connection, is defined by:

$$\delta_{CI} = \left(\frac{i_{sw,1}}{I_{p,AVG}} - 1 \right) \tag{3.24}$$

Using equations 3.22 and 3.23, the current imbalance rate can be expressed as a function of the voltage deviation as follows:

$$\delta_{CI} = \left(\frac{R_{C,1} - R_{C,2}}{R_{C,1} + R_{C,2}} \right) = \frac{\Delta V_{sw}}{(R_{C,1} + R_{C,2}) \cdot I_{sw,max}} \tag{3.25}$$

Figure 3.6 shows examples of the representative relationship between deviation voltage and current imbalance rate. Three IGBT power modules from the manufacturer Infineon, FZ750R65KE3 (6500Vx750A), FZ2400R17HP4 (1700Vx2400A), and FZ1500R33HE3 (3300Vx1500A), are presented in Figure 3.6. As an example, if two FZ1500R33HE3 semiconductor modules are connected in parallel and a voltage deviation between the modules of 1 V is expected at maximum current, then the current imbalance rate is 15%. In other words, this means that the current through one of the switches is 15% higher than the average current of the parallel connection. Therefore, it is necessary to decrease the total current (de-rating) that the parallel connection may carry (sum of individual current ratings) to ensure that the maximum current of any semiconductor in the parallel connection is never exceeded.

The manufacturers of high power semiconductor devices recommend that the peak current of a switch should not exceed 80% of the maximum current of the semi-

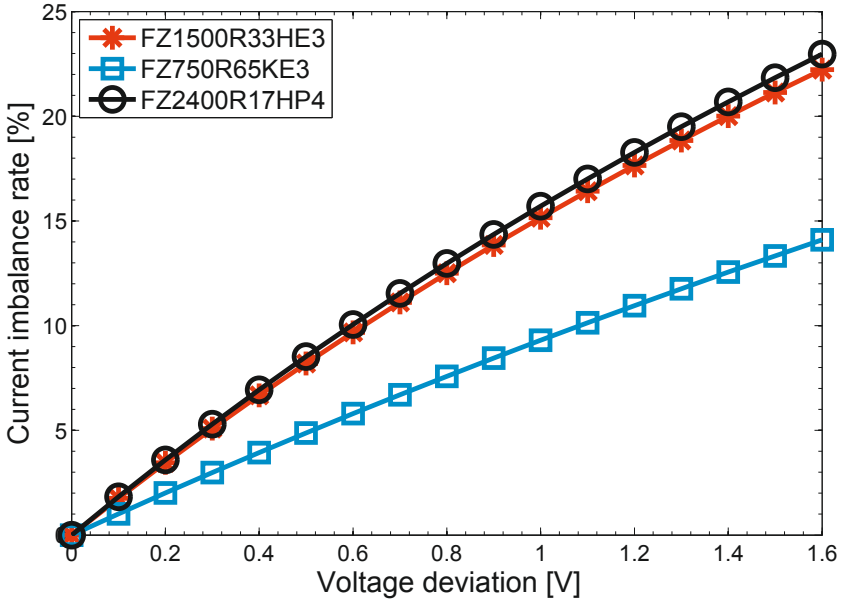


Figure 3.6: Example of current imbalance ratio as a function of the voltage deviation for three different IGBT modules from the manufacturer Infineon

conductor [27]. In line with this recommendation and taking into account the current imbalance rate, when n_p modules are connected in parallel, the following expression must be satisfied:

$$I_{psw} \leq 1.6 \cdot I_n \cdot n_p \cdot k_{cdp} \tag{3.26}$$

$$k_{cdp} = \frac{1}{n_p} \cdot \left[1 + (n_p - 1) \cdot \frac{(1 - \delta_{CI})}{(1 + \delta_{CI})}\right] \tag{3.27}$$

where I_{psw} is the peak current of the parallel connection, n_p is the number of semiconductor modules connected in parallel, I_n is the nominal current of one semiconductor (normally half of the maximum current), δ_{CI} is the current imbalance rate, and k_{cdp} is the de-rating factor. The de-rating factor (k_{cdp}) is the decrease of the maximum total current that can be applied under the worst case conditions in which $n_p - 1$ modules are identical and the current imbalance is concentrated into the module with the smallest on-state resistance [27].

An example of the de-rating factor as a function of the number of modules connected in parallel for different voltage deviations is shown in Figure 3.7. Infineon

FZ1500R33HE3 IGBT power modules are considered in Figure 3.7. As the number of modules connected in parallel increases, the de-rating factor decreases. Furthermore, an increase in the voltage deviation results in a decrease in the de-rating factor, because the current imbalance rate increases. For example, if six Infineon FZ1500R33HE3 IGBT modules ($I_n = 1500\,A$) are connected in parallel ($n_p = 6$) and a maximum voltage deviation of 1.2 V is expected ($\triangle V_{sw,max} = 1.2\,V$), then the expected current imbalance rate in the parallel connection is 18% (as can be noted from Figure 3.6) and a de-rating of 25% is needed ($k_{cdp} = 75\%$). In this case, the peak current of the parallel connection (I_{psw}) should not exceed 10.8 *kA* (following equation 3.26).

In addition, the current imbalance in the parallel connection should be taken into account during the calculation of power losses because different currents in the modules will generate different losses. Power losses in the parallel connection can then be calculated by determining the power losses in a module with an equivalent current and multiplying these losses by the number of modules connected in parallel. The equivalent current ($I_{sw,eq}$) for the calculation of semiconductor power losses can be estimated from equation 3.28, where $I_{sw,Total}$ is the total current of the array of IGBT modules connected in parallel.

$$I_{sw,eq} = \frac{\left(1 + \frac{\delta_{CI}}{2}\right)}{n_p} \cdot I_{sw,Total} \tag{3.28}$$

3.3 Series connection of power modules

When the required blocking voltage in the application is higher than the maximum blocking voltage of the available semiconductor modules, the connection of the devices in series can be considered. However, series and parallel connections are not usually combined in power semiconductors in real-world applications; instead, high rating devices are connected in parallel at the low-voltage side of the converter, and at the high-voltage side, the semiconductor devices are connected in series to reach the required blocking voltage.

If the semiconductor devices are connected in series, then all the devices carry the same current at conduction state, but there may be some differences in the forward voltage of each device because of the non-identical voltage-current characteristics of the modules. Furthermore, voltage imbalance between modules connected in series may exist at blocking state for the same reason. Manufacturers normally do not include the voltage-current characteristics at blocking state; thus, it is probably not worthwhile to introduce the calculation for voltage imbalance. However, the considered power loss models are proportional to the forward voltage and blocking

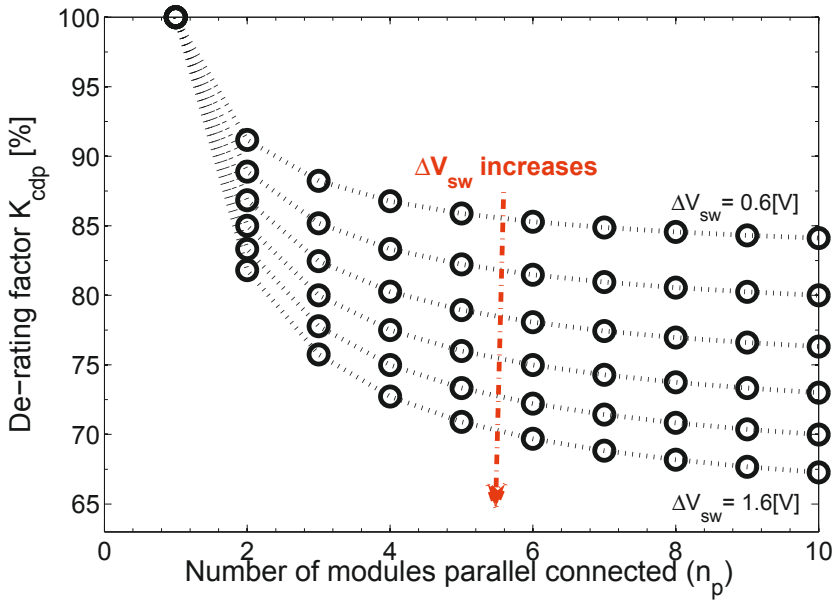


Figure 3.7: Example of the de-rating factor k_{cdp} as a function of the number of parallel-connected Infineon FZ1500R33HE3 power modules for different voltage deviations.

voltage; therefore, voltage imbalance can be neglected in the calculation of power losses and the average blocking voltage (total voltage divided by number of devices connected in series n_s) can be used during the calculation.

To estimate the number of devices connected in series that are required for a specific application, and considering the application notes from the manufacturers of semiconductors [28, 27], the following requirement must be satisfied (without considering voltage imbalance for non-identical devices connected in series):

$$\frac{V_{P,max}}{k_{vp} \cdot V_{block}} \leq n_s \; and \; \frac{V_{DC,max}}{k_{vdc} \cdot V_{block}} \leq n_s \tag{3.29}$$

where $V_{P,max}$ is the maximum voltage amplitude to be blocked for the series connection array, k_{vp} is a safety factor for peak voltage (normally between 0.75 and 0.85), $V_{DC,max}$ is the maximum DC voltage of the array, k_{vdc} is a safety factor for DC voltage (normally between 0.6 and 0.7), and V_{block} is the rated blocking voltage of a single device. The safety factors k_{vp} and k_{vdc} are used to ensure that the rated blocking voltage is not exceeded by repetitive overshoot voltage spikes that occur at the moment the device is turned off. These factors also guarantee that the device is switched on its Safe Operating Area [29].

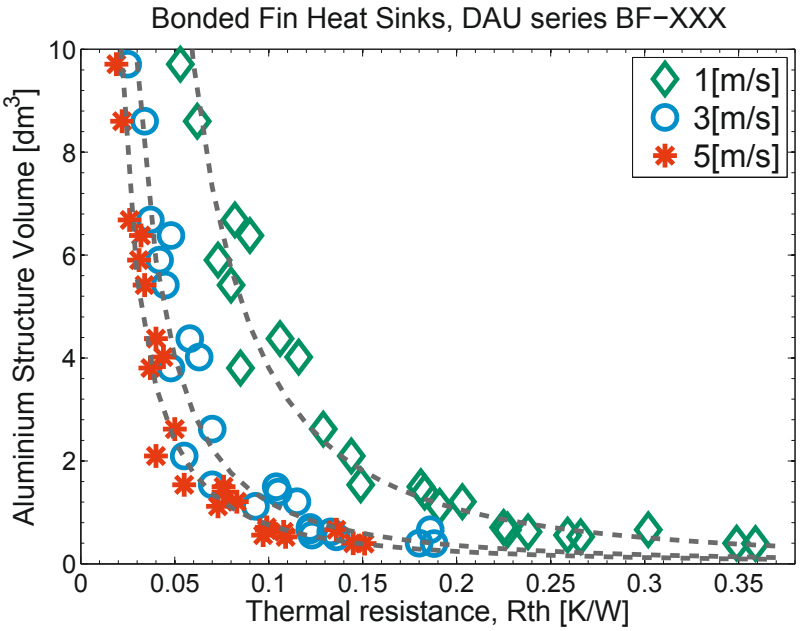


Figure 3.8: Example of the relationship between aluminium structure volume and the thermal resistance of the heat sink. The dashed lines show the fitting curve as given in equation (3.32)

The minimum number of series-connected devices required to fulfil the aforementioned conditions can be calculated as follows:

$$n_{s,min} = max\left\{\frac{V_{P,max}}{k_{vp}\cdot V_{block}}; \frac{V_{DC,max}}{k_{vdc}\cdot V_{block}}\right\} \tag{3.30}$$

3.4 Volume and mass of a switch valve

At each state of operation, semiconductor devices dissipate energy which heats the semiconductor and adds to the total power dissipation of the switch. Therefore, the maximum junction temperature (e.g. $T_{j,max} = 125$ ºC or $T_{j,max} = 150$ ºC in the newest high power modules) given by the manufacturer has to be obeyed at all times during the operation of the converter and the use of an appropriate cooling system becomes vital to avoid the destruction of the power switch.

A thermal model of the semiconductor device can be used to calculate the required thermal resistance of the cooling system for the worse operating condition, and then size and weight of the power switch with the cooling system can be estimated.

Two main types of cooling system are used in high power applications: forced air cooling and liquid cooling. However, only forced the air cooling system is presented in this chapter.

The volume of a power switch valve (Vol_{valve}) is given by the number of power devices connected in parallel (n_p) or in series (n_s), the semiconductor module itself and by the module heat sink:

$$Vol_{valve} = n_p \cdot n_s \cdot (Vol_{mod} + Vol_{HS}) \tag{3.31}$$

The volume of the semiconductor module (Vol_{mod}) can be found in the data sheet of the power module. The heat sink volume (Vol_{HS}) is given by the volume of the aluminium/copper structure (Vol_{HSal}) and the fan volume is (Vol_{fan}). The volume of the aluminium/copper structure (Vol_{HSal}) is inversely proportional to the thermal resistance of the heat sink for a given fan velocity [30], and the fan volume is proportional to the volume of the aluminium/copper structure. The forced air heat sink is designed according to a fixed fan velocity, and using the definition of thermal resistance ($R_{th}\,(K/W) = \triangle T/P_{loss}$), the following model can be proposed:

$$Vol_{HSal} = K_{HS0} \cdot \left(\frac{1}{R_{thHS}}\right)^{K_{HS1}} = K_{HS0} \cdot \left(\frac{P_{loss,mod}}{\Delta T_{HS,max}}\right)^{K_{HS1}} \tag{3.32}$$

$$Vol_{fan} = K_{fan0} \cdot (Vol_{HSal} - K_{fan2})^{K_{fan1}} \tag{3.33}$$

Where R_{thHS} is the required thermal resistance of the heat sink, $\triangle T_{HS,max}$ is the maximum allowable heat sink to ambient temperature difference, $P_{loss,mod}$ is the total power loss of the power module, and the parameters K_{HS0}, K_{HS1}, K_{fan0}, K_{fan1} and K_{fan2} are proportionality regression coefficients, the value of which can be found by examining data from commercially available heat sinks and fans.

Figure 3.8 shows an example of the relationship between Vol_{HSal} and thermal resistance for the bonded fin heat sink series BF-XX from the manufacturer DAU. Data for three different fan velocities are presented in Figure 3.8. The dashed lines show the fitting curve as given by equation 3.32. The thermal resistance of a given aluminium structure depends on fan velocity; therefore, the parameters K_{HS0} and K_{HS1} also depend on fan velocity. This is shown in Figure 3.9, which presents variation in thermal resistance with fan velocity for four heat sink structures from

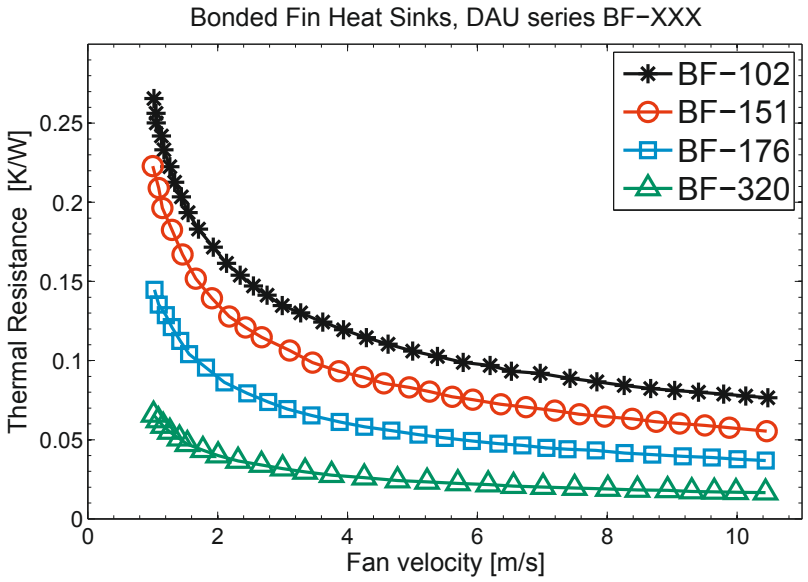


Figure 3.9: Example of the relationship between the thermal resistance of the heat sink and fan velocity.

Table 3.1: Calculated regression coefficients for the proposed volume model of the heat sink aluminium structure at different fan velocities. The bonded fin heat sink BF-XX series is from the manufacturer DAU.

Fan Velocity *m/s*	$K_{HS0}\, dm^3$	K_{HS1}
1	56.19e-3	1.8311
3	21.72e-3	1.7415
5	16e78e-3	1.6539
10	9e322e-3	1.4321

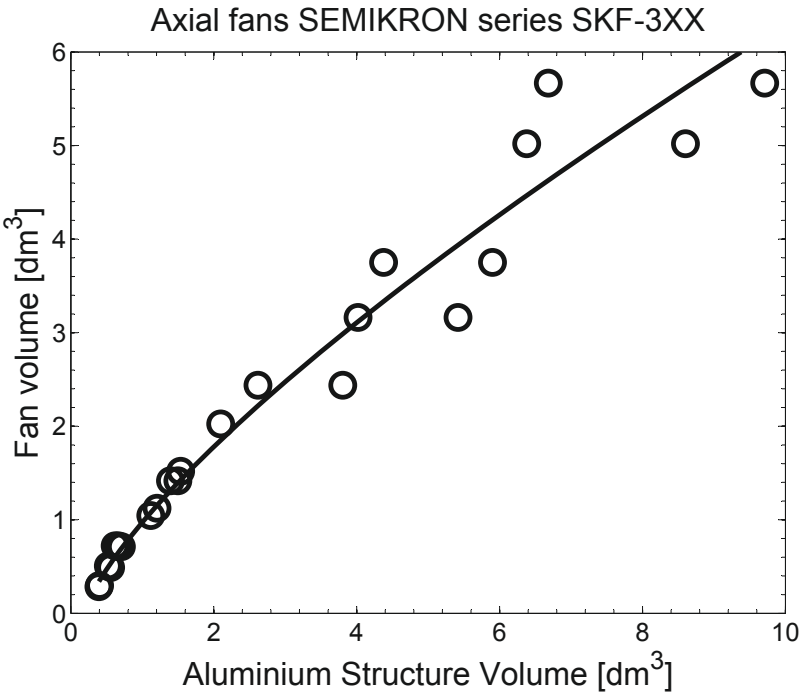


Figure 3.10: Example of the relationship between fan volume and aluminium structure volume for the axial fan SKF-3XX series manufactured by SEMIKRON and the bonded fin heat sink BF-XX series manufatured by DAU.. The solid line shows the fitting curve as given in equation (3.33)

the DAU BF-XX series. Table 3.1 shows the calculated values of parameters K_{HS0} and K_{HS1} for different fan velocities.

An example of the correlation between fan volume and aluminium structure volume is presented in Figure 3.10, in which the axial fan SKF-3XX series manufactured by SEMIKRON and the bonded fin heat sink BF-XX series manufactured by DAU are considered. The solid line in Figure 3.10 shows the fitting curve, which was plotted according to the model proposed by equation 3.33. The calculated regression coefficients for the example presented in Figure 3.10 are $K_{fan0} = 0.1992$, $K_{fan1} = 0.7467$ and $K_{fan2} = 0.1966\, dm^3$.

The maximum allowable heat sink to ambient temperature difference, $\triangle T_{HS,max}$, is calculated according to the average thermal analysis of the power module. For example, if a power module composed of an IGBT and an anti-parallel diode is considered, the average thermal model presented in Figure 3.11 can be used to calculate $\triangle T_{HS,max}$ as follows:

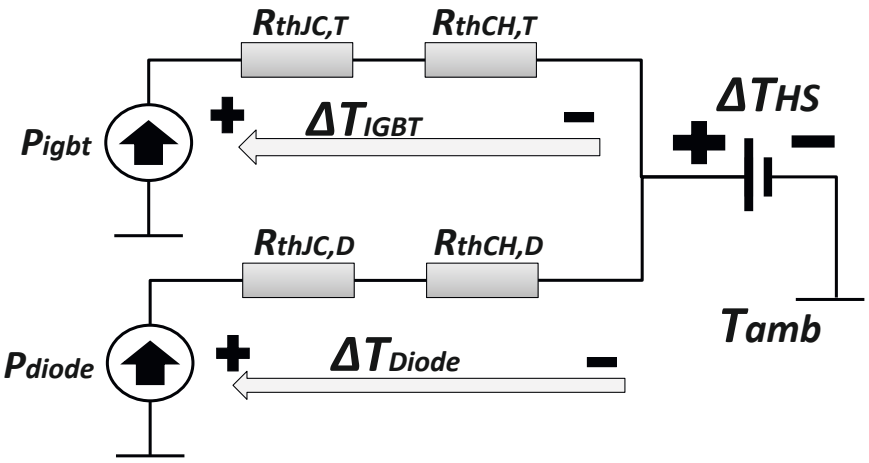


Figure 3.11: Average thermal model of an IGBT power module

$$\Delta T_{HS,max} + T_{amb} = K_{SFT} \cdot T_{j,max} - \triangle T_{mod,max} \tag{3.34}$$

$$\triangle T_{mod,max} = max \left\{ R_{th,igbt} \cdot \frac{P_{igbt}}{N_{isxm}}; R_{th,diode} \cdot \frac{P_{diode}}{N_{isxm}} \right\} \tag{3.35}$$

$$P_{igbt} = P_{cond,igbt} + P_{sw,on,igbt} + P_{sw,off,igbt} \tag{3.36}$$

$$P_{diode} = P_{cond,diode} + P_{sw,off,diode} \tag{3.37}$$

where K_{SFT} is the safety factor of thermal design, T_{amb} is the ambient temperature, N_{isxm} is the number of internal IGBTs/Diodes per module, and $R_{th,igbt}$ and $R_{th,diode}$ are the junction-to-heat sink thermal resistance per IGBT and diode, respectively. These latter values can be calculated by adding the junction-to-case and the case-to-heat sink thermal resistances (R_{thJC} and R_{thCH} in Figure 3.11) of IGBT and diode, which are given in the data sheet of the power device. For modules connected in parallel, the highest current of the modules should be considered when calculating P_{igbt} and P_{diode} (also taking into account the current imbalance rate, as described in equation 3.28).

To guarantee realistic heat sink designs, a constraint related to the minimum thermal resistance ($R_{thHS,min}$) should be taken into account. This constraint can be defined

as the maximum ratio between the volume of the heat sink structure and that of the module ($\delta_{HS,max} = Vol_{HSal}/Vol_{mod}$) beyond which equation 3.32 is no longer valid (normally, $\delta_{HS,max} \leq 6$). Thus, the temperature increase of a heat sink with minimum thermal resistance should be lower or equal to the maximum allowable heat sink to ambient temperature difference (from equation 3.34). This establishes the maximum power that the module can dissipate in the heat sink mounting without overheating itself, and can be expressed as follows:

$$R_{thHS,min} \cdot (P_{igbt} + P_{diode}) \leq \Delta T_{HS,max} \tag{3.38}$$

$$R_{thHS,min} = \left(\frac{K_{HS0}}{\delta_{HS,max} \cdot Vol_{mod}} \right)^{\frac{1}{KHS1}} \tag{3.39}$$

Given that conduction losses and switching losses depend on the junction temperature, iteration may be needed to solve equation 3.34. Alternatively, equations 3.6, 3.7 and 3.9 can be set to be temperature-independent for the highest acceptable junction temperature and the cooling system can be designed to keep the junction temperature below the highest assumed temperature. This assumption even provides an inbuilt thermal safety margin [31] and is considered in the examples presented in this thesis.

Finally, the mass of the valve can be expressed by the density and volume of each element (power semiconductor module, heat sink and fan):

$$Mass_{valve} = n_p \cdot n_s \cdot (\rho_{mod} \cdot Vol_{mod} + \rho_{HSal} \cdot Vol_{HSal} + \rho_{fan} \cdot Vol_{fan}) \tag{3.40}$$

The density values (ρ_{mod}, ρ_{HSal} and ρ_{fan}) can be calculated from the reference data sheet for each element. For example, the power module Infineon FZ1500R33HE3 has a density value $\rho_{mod} = 1187.2\,Kg/m^3$, and for the heat sink and fan considered in Figure 3.9 and Figure 3.10, the calculated density values are $\rho_{al} = 1366\,Kg/m^3$ and $\rho_{fan} = 769.23\,Kg/m^3$, respectively.

3.5 Semiconductor parameters

The η and ρ of the converter are highly influenced by the type of semiconductor device selected for the high power switch valve. Semiconductor devices that are commonly used in high power converters include the Insulated Gate Bipolar Transistor (IGBT), the Integrated Gate Commutated Thyristor (IGCT) and the Injec-

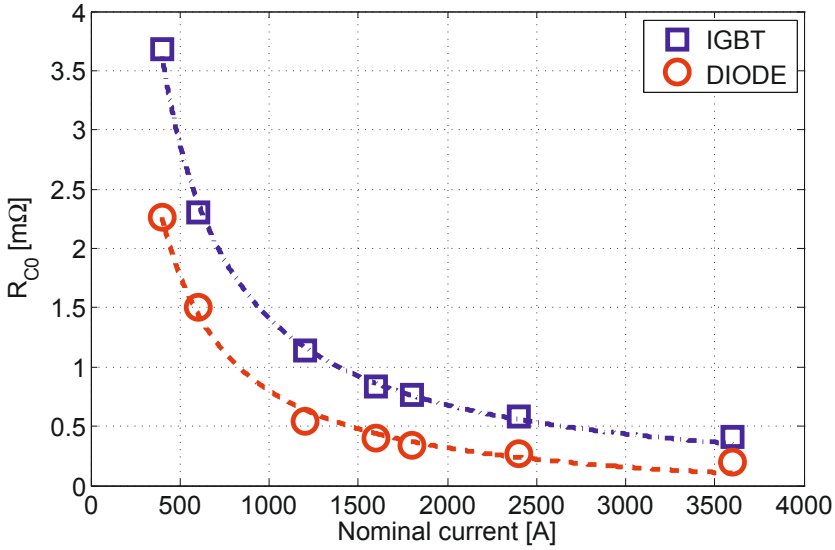


Figure 3.12: Dependence of on-state resistance R_{C0} on the nominal current for Infineon IGBT modules IGBT4 technology

tion Enhanced Gate Transistor (IEGT) [32]. The analysis of each type of semiconductor device is beyond the scope of this thesis, therefore, only switch valves based on IGBT devices are considered in the applied examples presented in this thesis. However, the models presented in this section can be adapted to any of the three devices (IGBT, IGCT or IEGT).

Table 3.2 summarises the semiconductor parameters needed to evaluate the switch valve models presented in this chapter. This table also includes the values of these parameters for three IGBT modules with different ratings: 1.7*kV*/3600*A* (Infineon FZ3600R17KE3), 3.3*kV*/1500*A* (Infineon FZ1500R33HE3) and 6.5*kV*/750*A* (Infineon FZ750R65KE3). These three modules are taken into account in chapter 6 for the evaluation of the power losses, volume and mass of a B2B converter based on two level voltage source topology.

In addition, 1.7 *kV* IGBT devices were selected to implement the power switches in the comparative study of chapter 7 because the generator output voltage considered is 690 *V* and these components are widely available on the market [33]. The parameters of the Infineon IGBT module IGBT4 technology FZXXR17HP4 were used in the comparative study presented in chapter 7 of this research. Given

Table 3.2: Semiconductor Parameters; IGBT modules manufatured by Infineon for three different voltage ratings are considered.

General Info.	Ratings	(1700Vx3600A)		(3300Vx1500A)		(6500Vx750A)	
	Reference	FZ3600R17KE3		FZ1500R33HE3		FZ750R65KE3	
	$Vol_{mod}\,[dm^3]$	1.0108		1.0108		1.2768	
	Mass $[Kg]$	1.5		1.2		1.4	
		IGBT	DIODE	IGBT	DIODE	IGBT	DIODE
Cond. losses model	V_{sw00}	0.964	0.959	1.436	1.359	1.891	1.413
	$\alpha_{Vsw0}[\frac{1}{C}]$	-0.89e-3	-1.36e-3	-0.237e-3	-3.19e-3	0.583e-3	-1.82e-3
	$R_{C0}[m\Omega]$	0.401	0.249	1.130	0.804	2.326	1.862
	$\alpha_{Rc}[\frac{1}{C}]$	3.47e-3	2.54e-3	3.26e-3	0.62e-3	3.18e-3	1.34e-3
	$T_{j0}[C]$*	125		150		125	
Switching ON losses model	$K_{Eon0}[\frac{mJ}{V}]$	0.158	—	0.4895	—	0.2346	—
	$K_{Eon1}[\frac{mJ}{VA}]$	6.36e-5	—	3.873e-5	—	1.3062e-3	—
	$K_{Eon2}[\frac{mJ}{VA^2}]$	3.44e-8	—	4.626e-7	—	1.1187e-6	—
	$\alpha_{Eon}[\frac{1}{C}]$	3.10e-3	—	2.7586e-3	—	3.5385e-3	—
Switching OFF losses model	$K_{Eoff0}[\frac{mJ}{V}]$	0.037	0.328	0.116	0.314	0.021	0.185
	$K_{Eoff1}[\frac{mJ}{VA}]$	4.04e-4	3.34e-4	7.31e-4	7.28e-4	1.55e-3	1.12e-3
	$K_{Eoff2}[\frac{mJ}{VA^2}]$	7.73e-9	-2.68e-8	4.53e-8	-1.35e-7	1.45e-8	-3.26e-7
	$\alpha_{Eoff}[\frac{1}{C}]$	3.28e-3	4.25e-3	2.44e-3	5.33e-3	1.429e-3	5.33e-3
Parallel Connect.	$\triangle V_{sw}[V]$	0.45	0.40	0.55	0.75	0.4	0.5
	$\delta_{CI}[\%]$	18.48	28.72	19.36	26.16	12.95	21.81
Static thermal model	$R_{thJC}[\frac{K}{kW}]$	6.3	14	7.35	13	8.7	18.5
	$R_{thCH}[\frac{K}{kW}]$	8.7	19.5	10	11	8.8	14
	N_{isxm}	3		3		3	
	$T_{j,max}[C]$	125		150		125	
Switch. times** at $T_{j,max}$	$t_{on,max}[\mu s]$	1.05	—	1.15	—	1.2	—
	$t_{off,max}[\mu s]$	2.1	0.88	3.85	1.73	8.1	2.67
	$f_{sw,max}[kHz]$	$4.96 \rightarrow 4$		$2.97 \rightarrow 2$		$1.67 \rightarrow 1.5$	

*Reference temperature for all the temperature coefficients.

** Maximum switching frequency is calculated as the conduction time per switching period is higher than 98%

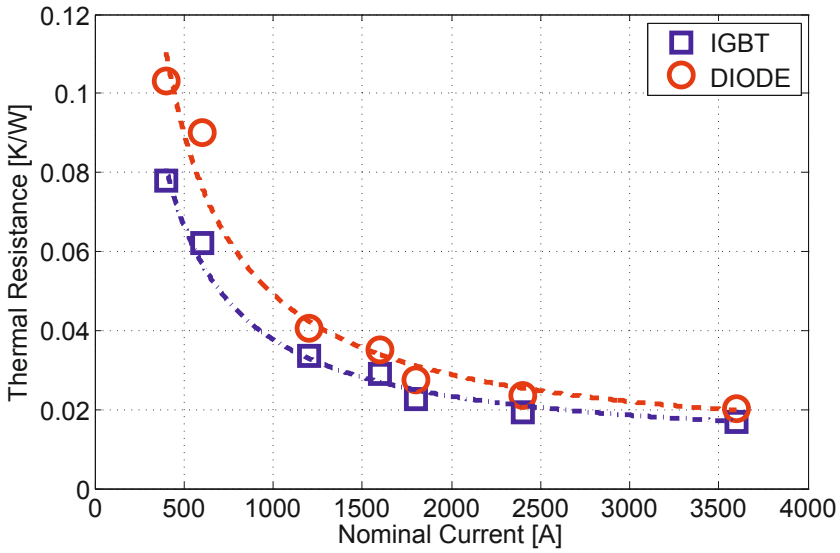


Figure 3.13: Dependence of the thermal resistance R_{th} on the nominal current for Infineon IGBT modules IGBT4 technology

that these parameters depend on the power rating of the IGBT module and that the use of a high power semiconductor module in low power applications is not cost-effective, the semiconductor power rating may be used as a design parameter to determine the best semiconductor for each modular design. Therefore, the semiconductor parameters are modeled as a function of the power rating.

From the analysis of the parameters for Infineon 1.7 kV IGBTs, it can be seen that the thermal resistance $R_{th,igbt/diode}$ and the on-state resistance $R_{C0,igbt/diode}$ are inversely proportional to the nominal current of the semiconductor as shown in Figure 3.12 and Figure 3.13. The other parameters can be considered constant for this type of technology. The following model can then be proposed:

$$R_{C0} = \frac{K_{cond21}}{I_n} + K_{cond20},$$

$$R_{th} = \frac{K_{Rth1}}{I_n} + K_{Rth0}$$

Table 3.3: Parameter of the Semiconductor modules used in chapter 7

Parameter	IGBT Module 1.7 kV		Power Diode	Bridge Diode
	IGBT	DIODE	Mod. 3.3 kV	Mod. 1.6 kV
V_{sw00}	1.0828	0.9804	1.4383	0.75
K_{cond21}	1.4679	0.9702	1.1208	0.4186
K_{cond20}	-5.38e-5	-1.664e-4	0	-1.4e-3
K_E·1e-7	(on) 3.1	(rr) 4.08	(rr) 7.22	—
	(off) 4.7			
T_{jmax}	150 *ºC*	150 *ºC*	150 *ºC*	150 *ºC*
K_{Rth1}	28.8635	40.842	11	12.053 per mod.
K_{Rth0}	0.009	0.0084	0.0082	0.0267 per mod.

where I_n is the nominal current of the IGBT module and the main parameters are given in Table 3.3.

A maximum nominal current of 3600 *A* for the IGBT module is considered to be the limit for the selected technology. The minimum number of modules connected in parallel $n_{p,min}$ is calculated according to 3.26.

By contrast, the full bridge diode rectifier, considered in chapter 7, is implemented with power diodes for 3.3 *kV* applications. The parameters of the Infineon power diode modules from the IGBT3 DDXXS33HE3 series have been considered. The same analysis was performed for these devices and the parameters are shown in Table 3.3.

Chapter 4

Passive Elements

4.1 Filter inductors

4.1.1 Main constraints for the design of the inductor

The starting point for the design of an inductor is the stored energy relation (equation 4.1), defined by the inductance L, the inductor peak current ($\hat{I}_L$), the RMS current (I_L), the RMS current density (J_L), the peak flux density (B_L), the winding conductor fill factor (k_{wc}), the winding window area (A_w) and the core area (A_{core}) [34].

$$L \cdot \hat{I_L} \cdot I_L = k_{wc} \cdot J_L \cdot B_L \cdot A_w \cdot A_{core} \tag{4.1}$$

The product ($A_w \cdot A_{core}$) appears in equation 4.1. It indicates the core size and is called area product. For a given core material, the peak flux density is limited by the saturation flux density (B_{sat}) of the core material. This resembles the situation for the winding conductor, which physically limits the maximum current density (J_{max}) of the inductor winding. Moreover, if a conductor type and core type are fixed for the inductor design, the winding conductor fill factor becomes approximately a design constant.

When the total size of the inductor is reduced by targeting some given electrical parameters like inductance and current, the design of the inductor should enable the peak flux density and current density to be pushed as close as possible to the physical limits and thermal constraints, because the product $J_L \cdot B_L$ is inversely proportional to the winding area and the core area. The minimum area product for a given set of constraints can then be written as follows:

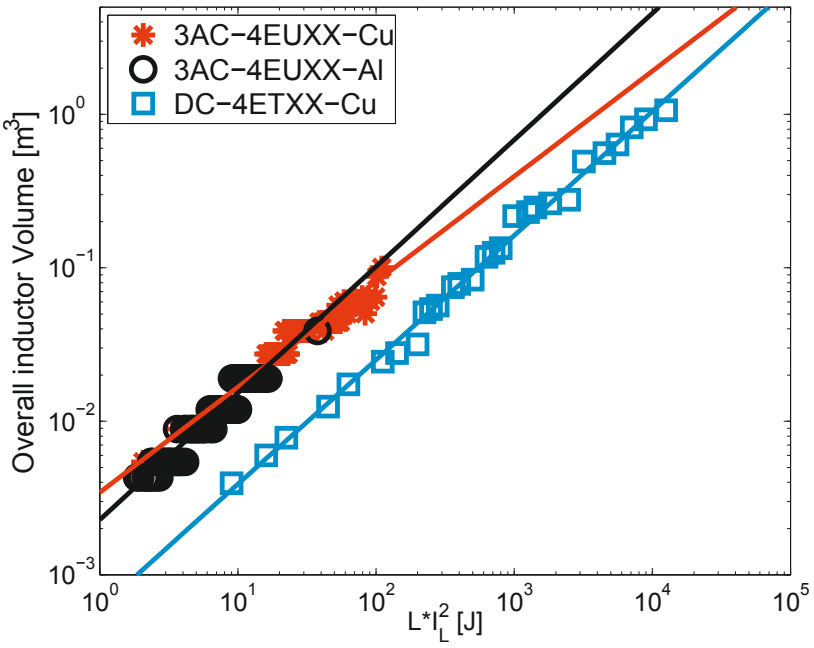


Figure 4.1: Example of inductor Volume and product ($L \cdot I_L^2$) relationship for three different inductor technologies manufactured by Siemens. The three-phase reactor series 4EUXX with a Cu or Al winding conductor, and the DC iron core smoothing reactor series 4ETXX with a Cu winding are considered.

$$A_w \cdot A_{core} \propto \frac{L \cdot \hat{I_L} \cdot I_L}{J_{max} \cdot B_{sat}} \propto E_L \propto L \cdot I_L^2 \tag{4.2}$$

4.1.2 Size modelling

Geometrically, the area product is also related to the volume of the inductor by [34]:

$$A_w \cdot A_{core} \propto Vol_L^{3/4} \tag{4.3}$$

Combining equations 4.2 and 4.3, the inductor volume can be expressed as:

$$Vol_L \propto \left(L \cdot I_L^2\right)^{3/4} \tag{4.4}$$

Then, if the same inductor design technology is maintained (core material, con-

ductor type, core geometry) for different inductance values and current requirements, the overall inductor volume and inductor total mass can be predicted by:

$$Vol_L = K_{VL0} \cdot \left(L \cdot I_L^2\right)^{K_{VL1}} \tag{4.5}$$

$$Mass_L = K_{\rho L0} \cdot (Vol_L)^{K_{\rho L1}} \tag{4.6}$$

where K_{VL0}, K_{VL1}, $K_{\rho L0}$, and $K_{\rho L1}$ are proportionality regression coefficients found by taking data from reference inductor technology. Figure 4.1 presents the relationship between the inductor volume and the product $L \cdot I_L^2$ for three different inductor technologies manufactured by Siemens: the three-phase reactor series 4EUXX (with a Cu or Al winding conductor), and the DC iron core smoothing reactor series 4ETXX (with a Cu winding conductor). The lines in Figure 4.1 show the calculated model based on equation 4.5 for each family of considered inductors. Figure 4.2 displays the total mass against the overall volume for the same families of inductors considered in Figure 4.1. The calculated models based on equation 4.6 are also included in Figure 4.2. The calculated parameters of the size and mass models for the inductors considered in Figure 4.1 and Figure 4.2 are presented in Table 4.1.

4.1.3 Winding losses

The inductor power losses (P_L) are divided into winding and core losses. To estimate winding and core losses in the inductor, the concept of loss power density in the winding and core is used [33]. The winding power loss density (p_{wL}) can be expressed by

$$p_{wL} = \frac{dP_{wL}}{dVol_{wL}} = \rho_{wc} \cdot k_{wc} \cdot F_r \cdot J_L^2 \tag{4.7}$$

where ρ_{wc} is the resistivity of the winding conductor material, and F_r is a factor that relates DC resistance to AC resistance which accounts for all the high frequency effects and eddy current losses in winding (skin and proximity effects). For conductor diameters lower than the skin depth diameter and for a high number of strands ($N_s > 25$), the factor F_r can be approximated by [35, 36]:

$$F_r = 1 + \left(\frac{p_{layer} \cdot \pi \cdot \mu_0 \cdot K_{layer} \cdot f_{eff}}{12 \cdot \rho_{wc}}\right)^2 \cdot N_s \cdot d_s^4 \tag{4.8}$$

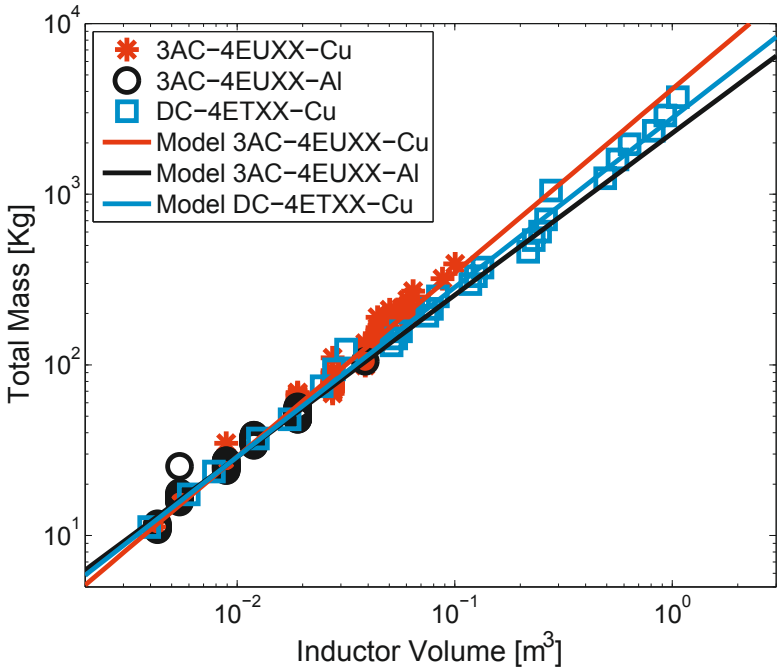


Figure 4.2: Total Mass of the inductor against its overall volume. Three inductor technologies from the manufacturer Siemens are plotted: The three-phase reactor series 4EUXX with a Cu or Al winding conductor, and the DC iron core smoothing reactor series 4ETXX with a Cu winding conductor.

Table 4.1: Parameters of the Inductor model; Inductor technologies from the manufacturers Siemens and CWS are considered: The three-phase reactor series 4EUXX with a Cu or Al winding conductor, the AC nano-crystalline inductor TPC series from CWS, and the DC iron core smoothing reactor series 4ETXX with a Cu winding conductor.

Parameter	3-AC Inductors		DC-Inductors	AC-Inductor
Reference	series 4EUXX		series 4ETXX	series TPC
Manufacturer	Siemens			CWS
Conductor	Copper	Aluminium	Copper	Copper
Core material	Power Iron	Power Iron	Power Iron	Nano-crystalline
K_{VL0}	3.4353e-3	2.2818e-3	0.60434e-3	4.96e-4
K_{VL1}	0.6865	0.82494	0.80946	0.5192
$K_{\rho L0}$	4129.2244	2276.9539	2797.6215	805.3
$K_{\rho L1}$	1.0768	0.94879	0.99314	0.87
$K_{\rho w0}$	9412.0118	6005.6682	10874.8628	1.26e5
$K_{\rho w1}$	0.85361	0.75117	0.82048	1.072
f_{Lref}	50	50	50	500
$K_{\rho C0}$	8242.2998	8805.6895	493.0059	1.401e4
$K_{\rho C1}$	0.99926	0.97691	1.0349	0.831
α_L	1.1	1.1	1.1	1.53
β_L	2.0	2.0	2.0	1.52
δ_{iLref}	—	—	0.3	—

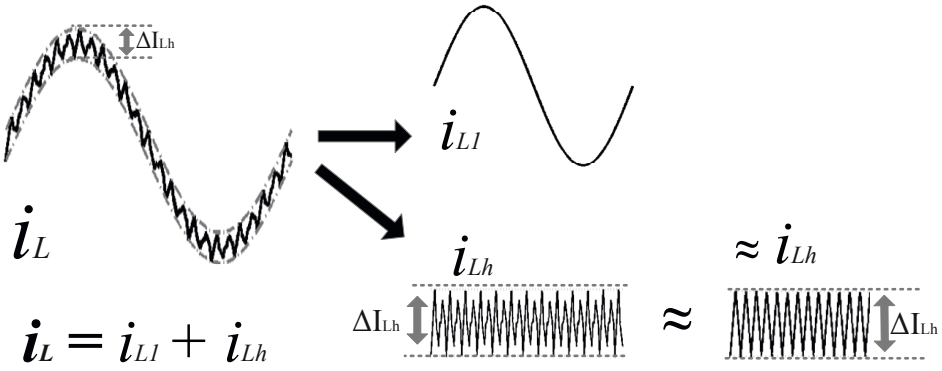


Figure 4.3: Typical inductor current waveform in power converter applications and its decomposition into the two main components: the fundamental component and the harmonic component.

where p_{layer} is the number of winding layers, K_{layer} is the layer utilization factor, and d_s is the diameter of the conductor. f_{eff} is an effective frequency for a non-sinusoidal current waveform (that takes into account harmonic effects in losses) [35], and can be estimated using equation 4.9, where I_j is the RMS amplitude of the Fourier component at frequency w_j.

$$2 \cdot \pi \cdot f_{eff} = \sqrt{\frac{\sum_{j=0...\infty} I_j^2 \cdot w_j^2}{\sum_{j=0...\infty} I_j^2}} = \frac{rms\left\{\frac{d}{dt} I(t)\right\}}{I_{RMS}} \tag{4.9}$$

All the parameters (except f_{eff}) in equation 4.8 are design parameters and they are defined when the winding conductor is designed; therefore, for a given inductor, equation 4.8 can be expressed as:

$$F_r = 1 + k_{Fr} \cdot f_{eff}^2 \tag{4.10}$$

where k_{Fr} is constant for a given inductor. When the optimal strand diameter is chosen for a given number of strands, the factor F_r can be minimized, and its minimum value is $F_r = 4/3$ [37]. However, the winding design is normally limited by many factors and realistic values of F_r can range from 1.5 to 2 [35].

Given that the main use of the inductors in power converters is to limit the peak-to-peak ripple current ($\triangle I_{Lh}$) by filtering the current, the inductor current is expected to have harmonic components, which cannot be neglected during the calculation

of winding losses. Figure 4.3 shows the typical inductor current waveform in power converter applications and its decomposition into the two main components: a fundamental component (i_{L1}) and a ripple component (i_{Lh}). To simplify the calculations, the ripple current is approximated to a triangular waveform with a maximum amplitude equal to the maximum current ripple.

Thus, the inductor winding losses (P_{wL}) can be calculated with the winding volume (Vol_{wL}) and inductor current components by equation 4.7:

$$P_{wL} = (p_{wL1} + p_{wLh}) \cdot Vol_{wL} = \left(1 + \frac{p_{wLh}}{p_{wL1}}\right) \cdot p_{wL1} \cdot Vol_{wL} \tag{4.11}$$

where p_{wL1} and p_{wLh} are the winding power loss density given by the fundamental and ripple component of the current, respectively. The ratio p_{wLh}/p_{wL1} is equal to:

$$\frac{p_{wLh}}{p_{wL1}} = \frac{F_r\left(f_{Lh}\right) \cdot J_{Lh}^2}{F_r\left(f_{L1}\right) \cdot J_{L1}^2} \tag{4.12}$$

where f_{L1} is the fundamental frequency, f_{Lh} is the effective frequency of current ripple component, and J_{L1} and J_{Lh} are the RMS current density of the fundamental and ripple components of the inductor current, respectively. If the ripple current is approximated to be a triangular waveform with the same frequency as the switching frequency (f_{sw}) of the converter and a maximum amplitude equal to the maximum current ripple ($\triangle I_{Lh}/2$) (see Figure 4.3), the effective frequency of current ripple component can be calculated using equation 4.9:

$$f_{Lh} = \frac{rms\left\{\frac{d}{dt} i_{Lh}(t)\right\}}{2 \cdot \pi \cdot I_{Lh}} = \frac{2 \cdot \triangle I_{Lh} \cdot f_{sw}}{2 \cdot \pi \cdot \triangle I_{Lh}/(2\sqrt{3})} = \frac{2\sqrt{3}}{\pi} \cdot f_{sw} \tag{4.13}$$

If the winding design is suitable, then $F_r = 3/2$ at fundamental frequency and the constant k_{Fr} can be calculated from equation 4.10. Furthermore, the ratio of current densities in equation 4.12 is proportional to the ratio of ripple current to fundamental current; therefore, equation 4.12 can be simplified to (using equations 4.10 and 4.13):

$$\frac{p_{wLh}}{p_{wL1}} = \frac{\left(1 + k_{Fr} \cdot f_{Lh}^2\right)}{\left(1 + k_{Fr} \cdot f_{L1}^2\right)} \cdot \frac{I_{Lh}^2}{I_{L1}^2} = \left(\frac{2}{3} + \frac{4}{\pi^2} \cdot \left(\frac{f_{sw}}{f_{L1}}\right)^2\right) \cdot \left(\frac{\delta_{iL}^2}{6}\right) \tag{4.14}$$

$$\delta_{iL} = \frac{\triangle I_{Lh}}{\sqrt{2} \cdot I_{L1}} \tag{4.15}$$

where δ_{iL} is the ratio of peak-to-peak current ripple to maximum fundamental current. Then equation 4.11 is reduced to:

$$P_{wL} = \left[1 + \left(\frac{2}{3} + \frac{4}{\pi^2} \cdot \left(\frac{f_{sw}}{f_{L1}}\right)^2\right) \cdot \left(\frac{\delta_{iL}^2}{6}\right)\right] \cdot p_{wL1} \cdot Vol_{wL} \tag{4.16}$$

To express equation 4.16 as a function of the parameters of reference inductor technology, as was done for the overall inductor volume and mass (using equations 4.5 and 4.6, respectively), first, the winding volume (Vol_{wL}) can be assumed to depend on overall volume (Vol_L), and the winding losses can be expressed by:

$$P_{wL} = p_{wL} \cdot Vol_{wL} = K_{\rho w0} \cdot (Vol_L)^{K_{\rho w1}} \tag{4.17}$$

where $K_{\rho w0}$, and $K_{\rho w1}$ are proportionality regression coefficients found by taking data from reference inductor technology. The winding volume in equation 4.16 can then be replaced, using equation 4.17, as follows:

$$P_{wL} = \left[1 + \left(\frac{2}{3} + \frac{4}{\pi^2} \cdot \left(\frac{f_{sw}}{f_{L1}}\right)^2\right) \cdot \left(\frac{\delta_{iL}^2}{6}\right)\right] \cdot \frac{p_{wL1}}{p_{wL*}} \cdot K_{\rho w0} \cdot (Vol_L)^{K_{\rho w1}} \tag{4.18}$$

where p_{wL*} is the reference power loss density for reference inductor technology. Assuming that p_{wL*} is given for a reference frequency (f_{Lref}), and that the winding design has been optimized for that particular reference frequency ($F_r = 3/2$ at reference frequency), the ratio (ρ_{wL1}/ρ_{wL*}) can be simplified as follows (assuming constant nominal current density):

$$\frac{p_{wL1}}{p_{wL*}} = \frac{\left(1 + k_{Fr} \cdot f_{L1}^2\right)}{\left(1 + k_{Fr*} \cdot f_{Lref}^2\right)} \cdot \frac{J_{L1}^2}{J_{Lref}^2} = \frac{2}{3} + \frac{1}{3}\left(\frac{f_{L1}}{f_{Lref}}\right)^2 \tag{4.19}$$

Finally, the winding losses can be expressed as a function of the electrical and reference inductor technology parameters, as follows:

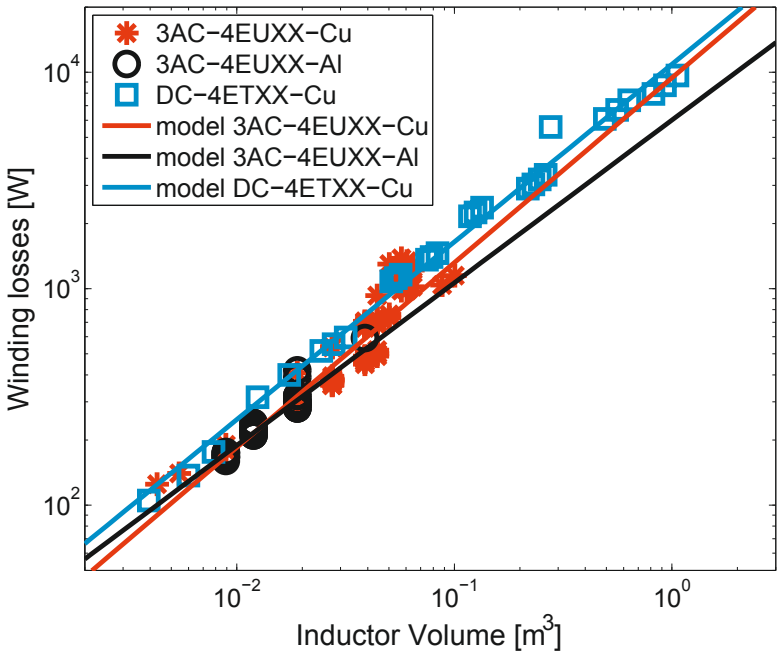


Figure 4.4: Example of relationship between inductor winding losses and overall volume for three different inductor technologies from the manufacturer Siemens. The three-phase reactor series 4EUXX with a Cu or Al winding conductor, and the DC iron core smoothing reactor series 4ETXX with a Cu winding conductor are considered

$$P_{wL} = \left[1 + \left(\frac{2}{3} + \frac{4}{\pi^2}\left(\frac{f_{sw}}{f_{L1}}\right)^2\right)\left(\frac{\delta_{iL}^2}{6}\right)\right] \cdot \left[\frac{2f_{Lref}^2 + f_{L1}^2}{3f_{Lref}^2}\right] \cdot K_{\rho w0} \cdot (Vol_L)^{K_{\rho w1}} \tag{4.20}$$

Figure 4.4 presents the relationship between the inductor winding losses and total volume (expressed by equation 4.20) for three different inductor technologies from the manufacturer Siemens: the three-phase reactor series 4EUXX (with a Cu or Al winding conductor), and the DC iron core smoothing reactor series 4ETXX (with a Cu winding conductor). The lines in Figure 4.4 show the calculated model based on equation 4.20 for each family of inductor. The parameters calculated for the inductors considered in Figure 4.4 are presented in Table 4.1.

It should be noted that equation 4.20 is valid for an inductor current with a fundamental component that differs from the DC component ($f_{L1} > 0$). When the DC current is the main component of the inductor current, the above procedure

can be modified to determine the winding losses. In this case, assuming that the winding design is optimized for low frequencies with an effective frequency of $f_{L0} < 50\,Hz$, and noting that equation 4.19 becomes equal to one for the DC inductors, the following expression can be derived:

$$P_{wL} = \left[1 + \left(1 + \frac{6}{\pi^2} \cdot \left(\frac{f_{sw}}{f_{L0}}\right)^2\right) \cdot \left(\frac{\delta_{iL}^2}{12}\right)\right] \cdot K_{\rho w0} \cdot (Vol_L)^{K_{\rho w1}} \tag{4.21}$$

4.1.4 Core losses

The core power loss density (p_{cL}) can be approximated using the empirical Steinmetz equation:

$$p_{cL} = \frac{dP_{coreL}}{dVol_{cL}} = K_{core} \cdot f_{eff}^{\alpha_L} \cdot B_L^{\beta_L} \tag{4.22}$$

where K_{core}, α_L and β_L are the usual Steinmetz coefficients, which are related to the material of the core , B_L is the peak flux density, and f_{eff} is the effective frequency as defined in equation 4.9. Given that the superposition principle can be not applied in this case, an effective frequency should be calculated that accounts for all the components of the flux density, which is related to the peak flux density of the inductor.

The inductor current has two main components, the fundamental component (I_{L1}) and the ripple component (I_{Lh}) (as shown in Figure 4.3), and the flux density is proportional to the inductor current for flux densities lower than saturation flux (which is the case under normal operation); therefore, the flux density in the inductor core can be approximated by two main components, the fundamental flux density and the ripple flux density, which are proportional to the fundamental and ripple current, respectively. The peak flux density can thus be expressed by:

$$B_L = B_{L1} + \frac{\triangle B_{Lh}}{2} = \left(1 + \frac{\triangle B_{Lh}}{2 \cdot B_{L1}}\right) \cdot B_{L1} \tag{4.23}$$

where B_{L1} is the fundamental peak flux density ($B_{L1} \propto \sqrt{2} \cdot I_{L1}$) and $\triangle B_{Lh}$ is the peak to peak ripple flux density ($\triangle B_{Lh} \propto \triangle I_{Lh}$). The ratio $^{\triangle B_{Lh}}/_{B_{L1}}$ can be simplified as follows (using equation 4.15):

$$\frac{\triangle B_{Lh}}{B_{L1}} = \frac{\triangle I_{Lh}}{\sqrt{2} \cdot I_{L1}} = \delta_{iL} \tag{4.24}$$

Equation 4.23 can then be expressed as:

$$B_L = \left(1 + \frac{\delta_{iL}}{2}\right) \cdot B_{L1} \tag{4.25}$$

By contrast, the effective frequency can be calculated using equation 4.9, as follows:

$$f_{eff} = \sqrt{\frac{I_{L1}^2 \cdot f_{L1}^2 + I_{Lh}^2 \cdot f_{Lh}^2}{I_{L1}^2 + I_{Lh}^2}} \tag{4.26}$$

The ripple component can be expressed as a function of the fundamental component using equation 4.15, as follows:

$$I_{Lh} = \frac{\triangle I_{Lh}}{2 \cdot \sqrt{3}} = \frac{\sqrt{6} \cdot \delta_{iL} \cdot I_{L1}}{6} \tag{4.27}$$

Equation 4.26 can then be simplified using equations 4.13, 4.15 and 4.27, as follows:

$$f_{eff} = \sqrt{\frac{I_{L1}^2 \cdot \left(f_{L1}^2 + \frac{\delta_{iL}^2 \cdot f_{sw}^2}{6}\right)}{I_{L1}^2 \cdot \left(1 + \frac{\delta_{iL}^2}{6}\right)}} = f_{L1} \cdot \left(\frac{6 + \left(\frac{\delta_{iL} f_{sw}}{f_{L1}}\right)^2}{6 + \delta_{iL}^2}\right)^{\frac{1}{2}} \tag{4.28}$$

The inductor core losses (P_{coreL}) can be calculated with the core volume (Vol_{coreL}) and the core power loss density (p_{cL}). Using equations 4.22, 4.25 and .4.28, the following expressions are obtained:

$$P_{coreL} = p_{cL} \cdot Vol_{coreL} = K_{core} \cdot f_{eff}^{\alpha_L} \cdot B_L^{\beta_L} \cdot Vol_{coreL}$$

$$P_{coreL} = K_{core} \cdot \left(\frac{6 + \left(\frac{\delta_{iL} f_{sw}}{f_{L1}}\right)^2}{6 + \delta_{iL}^2}\right)^{\frac{\alpha_L}{2}} f_{L1}^{\alpha_L} \cdot \left(1 + \frac{\delta_{iL}}{2}\right)^{\beta_L} B_{L1}^{\beta_L} \cdot Vol_{coreL}$$

$$p_{cL1} = K_{core} \cdot f_{L1}^{\alpha_L} \cdot B_{L1}^{\beta_L} \tag{4.29}$$

$$P_{coreL} = \left(\frac{6 + \left(\frac{\delta_{iL} f_{sw}}{f_{L1}} \right)^2}{6 + \delta_{iL}^2} \right)^{\frac{\alpha_L}{2}} \cdot \left(1 + \frac{\delta_{iL}}{2} \right)^{\beta_L} \cdot p_{cL1} \cdot Vol_{coreL} \tag{4.30}$$

To express equation 4.30 as a function of the parameters of a reference inductor technology, as was done for winding losses, the core volume (Vol_{coreL}) can be assumed to depend on the overall volume (Vol_L). The core losses can thus be expressed by:

$$P_{coreL} = p_{cL} \cdot Vol_{coreL} = K_{\rho c0} \cdot (Vol_L)^{K_{\rho c1}} \tag{4.31}$$

where $K_{\rho c0}$, and $K_{\rho c1}$ are proportionality regression coefficients found by taking data from reference inductor technology. Core volume in equation 4.30 can then be replaced, using equation 4.31, as follows:

$$P_{coreL} = \left(\frac{6 + \left(\frac{\delta_{iL} f_{sw}}{f_{L1}} \right)^2}{6 + \delta_{iL}^2} \right)^{\frac{\alpha_L}{2}} \cdot \left(1 + \frac{\delta_{iL}}{2} \right)^{\beta_L} \cdot p_{cL1} \cdot \frac{K_{\rho c0} \cdot (Vol_L)^{K_{\rho c1}}}{p_{cL*}} \tag{4.32}$$

where p_{cL*} is the reference power loss density for reference inductor technology. Assuming that p_{cL*} is given for a reference frequency (f_{Lref}) and a reference flux density (B_{Lref}), and that the inductor has been designed to minimize losses according to the optimum flux density method presented in [38], the reference frequency and flux density are related as follows:

$$f_{Lref}^{\alpha_L+2} \cdot B_{Lref}^{\beta_L+2} = K_{Lopt*} \tag{4.33}$$

where K_{Lopt*} is a constant given by the inductor design parameters. Reference inductor technology is then used to design an inductor for a f_{L1} higher than f_{Lref}. The fundamental flux density should be varied according to equation 4.33, such that:

$$\left(\frac{f_{Lref}}{f_{L1}} \right)^{\alpha_L+2} = \left(\frac{B_{L1}}{B_{Lref}} \right)^{\beta_L+2} \tag{4.34}$$

then the ratio p_{cL1}/p_{cL*} can be simplified as follows:

$$\frac{p_{cL1}}{p_{cL*}} = \left(\frac{f_{L1}}{f_{Lref}}\right)^{\alpha_L} \cdot \left(\frac{B_{L1}}{B_{Lref}}\right)^{\beta_L} = \left(\frac{f_{L1}}{f_{Lref}}\right)^{2\cdot(\alpha_L-\beta_L)} \tag{4.35}$$

However, if f_{L1} is lower than f_{Lref}, the fundamental flux density is assumed to be constant (because of magnetic saturation). The ratio p_{cL1}/p_{cL*} can then be simplified as follows:

$$\frac{p_{cL1}}{p_{cL*}} = \left(\frac{f_{L1}}{f_{Lref}}\right)^{\alpha_L} \tag{4.36}$$

If the DC current is the main component of the inductor current, the above procedure can be modified to calculate the core losses. In this case, it should be noted that the DC component does not produce core losses; therefore, the reference data is given for the ratio of peak-to-peak current ripple to maximum DC current (δ_{iLref}) and a reference ripple frequency (f_{Lref}). The following expression can then be derived:

$$P_{coreL} = \left(\frac{2\sqrt{3}f_{sw}}{\pi \cdot f_{Lref}}\right)^{\alpha_L} \cdot \left(\frac{\delta_{iL}}{\delta_{iLref}}\right)^{\beta_L} \cdot K_{\rho c0} \cdot (Vol_L)^{K_{\rho c1}} \tag{4.37}$$

Figure 4.5 shows the relationship between the inductor core losses and total volume for three different inductor technologies from the manufacturer Siemens: the three-phase reactor series 4EUXX (with a Cu or Al winding conductor), and the DC iron core smoothing reactor series 4ETXX (with a Cu winding conductor). The lines in Figure 4.5 show the calculated model based on equation 4.31 for each family of considered inductors. The parameters calculated for the inductors considered in Figure 4.5 are presented in Table 4.1.

4.2 Filter capacitors

4.2.1 Size modelling

Almost all conventional capacitors used in high power wind converter applications, are constructed based on the structure of plate capacitors. In a plate capacitor, the capacitance (C) increases with the area of the plates (A_{PC}) and with the permittivity (ε) of the dielectric material, and decreases with the distance between the plates (d_{PC}). This relationship is expressed by equation 4.38.

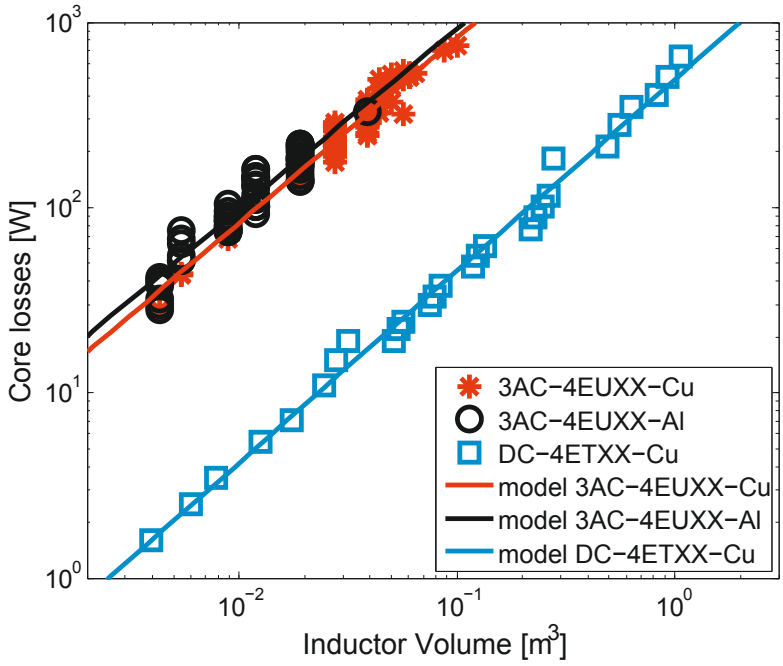


Figure 4.5: Example of inductor core losses and overall volume relationship for three different inductor technologies from the manufacturer Siemens. The three-phase reactor series 4EUXX with a Cu or Al winding conductor, and the DC iron core smoothing reactor series 4ETXX with a Cu winding conductor are considered.

$$C = \frac{\varepsilon \cdot A_{PC}}{d_{PC}} \tag{4.38}$$

The voltage applied between plates is limited by the distance between them and the properties of the dielectric material (the breakdown electric strength, E_{Bd}). When an increase in the rated voltage (V_{CN}) of the capacitor is desired, the distance between the plates must be increased to avoid dielectric breakdown. This relationship is expressed by equation 4.39, which assumes a uniform voltage distribution in the dielectric material.

$$V_{CN} \propto d_{PC} \cdot E_{Bd} \tag{4.39}$$

The volume of a plate capacitor (Vol_{PC}) is proportional to the area of the plates and the distance between them. Taking into account equations 4.38 and 4.39, it can be shown that the volume of a plate capacitor is proportional to its capacitance and the square of its rated voltage, as follows:

$$Vol_{PC} \propto A_{PC} \cdot d_{PC} = \left(\frac{C \cdot d_{PC}}{\varepsilon}\right) \cdot d_{PC} \propto \frac{C}{\varepsilon} \cdot \left(\frac{V_{CN}}{E_{Bd}}\right)^2 \tag{4.40}$$

If the same capacitor technology is maintained (dielectric material, fabrication process, and geometry) for different capacitance values and rated voltage requirements, the overall capacitor volume and capacitor total mass can be predicted by:

$$Vol_C = K_{VC0} \cdot C^{K_{VC1}} \cdot V_{CN}^{K_{VC2}} \tag{4.41}$$

$$Mass_C = K_{\rho C0} \cdot (Vol_C)^{K_{\rho C1}} \tag{4.42}$$

where K_{VC0}, K_{VC1}, K_{VC2}, $K_{\rho C0}$, and $K_{\rho C1}$ are proportionality regression coefficients found by taking data from reference capacitor technology. Figure 4.6 shows the relationship between the volume of the capacitor and its capacitance for different voltage ratings and different capacitor technologies: Figure 4.6a. shows the DC link capacitor series MKP-B256xx from the manufacturer TDK, Figure 4.6b. shows the DC link capacitor series LNK-M3xx1 from the manufacturer ICAR, Figure 4.6c. shows the AC filter capacitor series MKP B3236x from TDK, and Figure 4.6d. shows the AC filter capacitor series MKV-E1x from ICAR. The lines in Figure 4.6 plot the calculated model based on equation 4.41 for each family of considered capacitors.

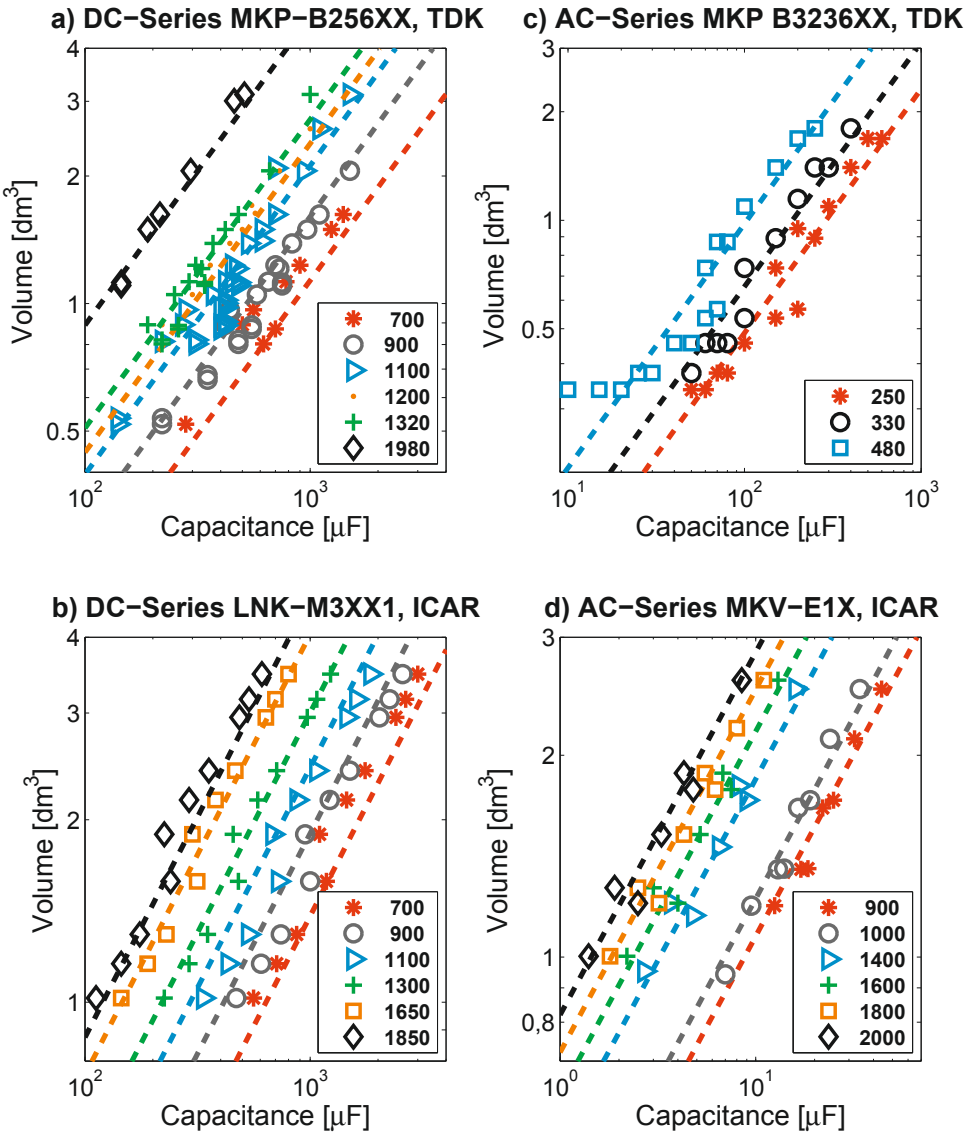


Figure 4.6: Film capacitor volume vs. capacitance for different voltage ratings and capacitor technologies: a) the DC link capacitor series MKP-B256xx manufactured by TDK; b) the DC link capacitor series LNK-M3xx1 manufactured by ICAR; c) the AC filter capacitor series MKP B3236 from TDK; d) the AC filter capacitor series MKV-E1x from ICAR. The dashed lines show the fitting curves as given in equation 4.41

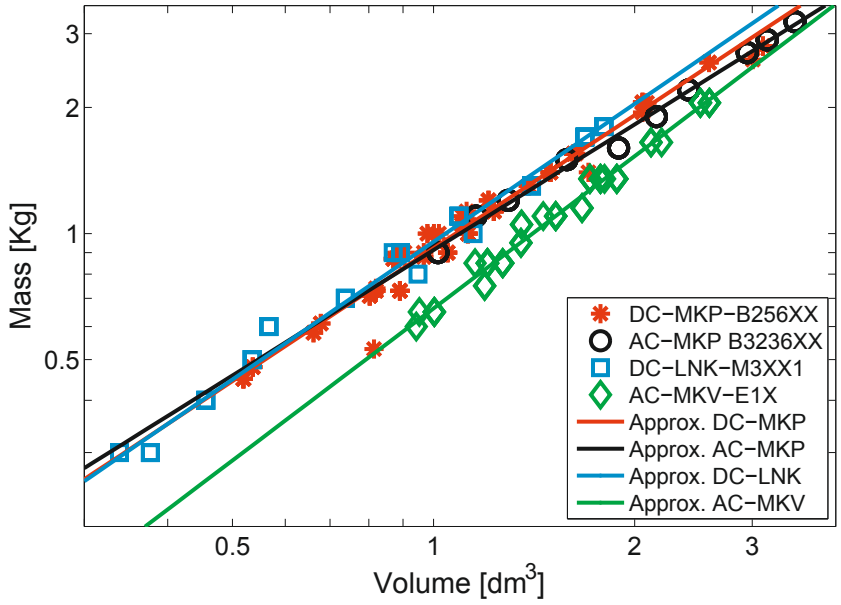


Figure 4.7: Film capacitor mass vs. overall volume for the capacitor technologies considered in Figure 4.6. The solid lines show the fitting curves as given in equation 4.42

By contrast, Figure 4.7 displays the total mass against the overall volume for the same families of capacitors considered in Figure 4.6. The calculated models based on equation 4.42 are also included in Figure 4.7. The calculated parameters of the size and mass models for the capacitors considered in Figure 4.6 and Figure 4.7 are presented in Table 4.2.

4.2.2 Capacitor dielectric Losses

The capacitor losses (P_C) are modelled by adding the dielectric losses ($P_{\varepsilon C}$) and the resistive losses ($P_{\Omega C}$). The dielectric losses can be calculated by [39]

$$P_{\varepsilon C} = \pi \cdot f_c \cdot C \cdot \tan(\delta_0) \cdot V_{Cac}^2 \tag{4.43}$$

where V_{Cac} is the maximum amplitude of the alternating voltage applied to capacitor with effective frequency f_c, and $\tan(\delta_0)$ is the dissipation factor of the dielectric. Normally, the dielectric dissipation factor depends on the dielectric material of the capacitor and can be considered to be constant for all capacitors in their normal working frequency range. For example, the typical value of the dissipation factor for polypropylene is 2e-4, which is the dielectric of the capacitors considered in Figure 4.6 and Figure 4.7.

Table 4.2: Parameters of various models of capacitor: DC and AC capacitor technologies from the manufacturers TDK and ICAR are considered.

Parameter	DC Capacitors		AC capacitors	
Manufacturer	TDK	ICAR	TDK	ICAR
Reference	MKP-B256xx	LNK-M3xx1	MKP B3236x	MKV-E1x
K_{VC0}	2.0734e-5	5.9622e-5	67.303e-5	13.406e-5
K_{VC1}	0.7290	0.7271	0.6770	0.5410
K_{VC2}	1.3796	1.2473	1.0706	1.2216
$K_{\rho C0}$	1.3428e3	0.8821e3	1.8079e3	2.7496e3
$K_{\rho C1}$	1.0543	0.9950	1.0923	1.2060
$\tan(\delta_0)$	2e-4	2e-4	2e-4	2e-4
$K_{\Omega C0}$	4.069e-3	2.3056e-5	1.5711e-3	4.9369e-6
$K_{\Omega C1}$	-0.3211	-0.0430	-0.3970	0.0783
$K_{\Omega C2}$	-0.4661	0.4986	-0.4539	1.0316

For DC capacitors, the voltage V_{Cac} is the peak value of the superimposed ripple voltage. When the ripple voltage is approximated to be a triangular waveform with the same frequency as the switching frequency (f_{sw}) of the converter and a peak-to-peak amplitude equal to the maximum voltage ripple, the following approximation can be made based on equation 4.9:

$$P_{\varepsilon C} = \frac{\sqrt{3}}{2} \cdot f_{sw} \cdot C \cdot \tan(\delta_0) \cdot \delta_{Vdc}^2 \cdot V_{DC}^2 \tag{4.44}$$

where δ_{Vdc} is the ratio of peak-to-peak voltage ripple to DC voltage (V_{DC}) of the converter.

For AC capacitors, the voltage V_{Cac} is the peak value of the fundamental component plus the peak voltage ripple, and the effective frequency can be approximated to the fundamental frequency. Dielectric losses can then be expressed as:

$$P_{\varepsilon C} = \pi \cdot f_{c1} \cdot C \cdot \tan(\delta_0) \cdot \left(1 + \frac{\delta_{Vac}}{2}\right)^2 \cdot V_{acp}^2 \tag{4.45}$$

where δ_{Vac} is the ratio of peak-to-peak voltage ripple to the peak fundamental voltage (V_{acp}) with fundamental frequency f_{c1}.

4.2.3 Capacitor resistive Losses

Resistive losses ($P_{\Omega C}$) occur in the electrodes, in the contacting and in the inner wiring. These losses can be calculated as follows [39]:

$$P_{\Omega C} = R_{sC} \cdot I_C^2 \tag{4.46}$$

where I_C is the RMS value of the capacitor current, and R_{sC} is the series resistance at maximum hot-spot temperature, which is the sum of all resistances occurring inside the capacitor. The series resistance R_{sC} is typically estimated from average film metallisation parameters [39] and its value can be found in the data sheet of the reference capacitor technology. Due to thinness of metallised layer, high frequency effects such as the skin effect are negligible [25, 40].

A model based on the capacitance value and the capacitor rating voltage can be used to predict the value of series resistance, as follows:

$$R_{sC} = K_{\Omega C0} \cdot C^{K_{\Omega C1}} \cdot V_{CN}^{K_{\Omega C2}} \tag{4.47}$$

where $K_{\Omega C0}$, $K_{\Omega C1}$, and $K_{\Omega C2}$ are proportionality regression coefficients found by taking data from reference capacitor technology. The value of series resistance given in the data-sheets is given for a capacitor temperature of 20^oC, but a conversion factor of 1.25 can be used to estimate the resistance at nominal temperature (typically, 85^oC for film capacitors) [39, 41].

Figure 4.8 shows the relationship between the series resistance per energy storage and the capacitance for different voltage ratings and different capacitor technologies: Figure 4.8a. shows the DC link capacitor series MKP-B256xx from the manufacturer TDK, Figure 4.8b. shows the DC link capacitor series LNK-M3xx1 from the manufacturer ICAR, Figure 4.8c. shows the AC filter capacitor series MKP B3236x from TDK, and Figure 4.8d. shows the AC filter capacitors series MKV-E1x from ICAR. The lines in Figure 4.8 plot the calculated model based on equation 4.47 for each family of considered capacitors. The series resistance in Figure 4.8 refers to the resistance at nominal temperature ($85\ ^oC$).

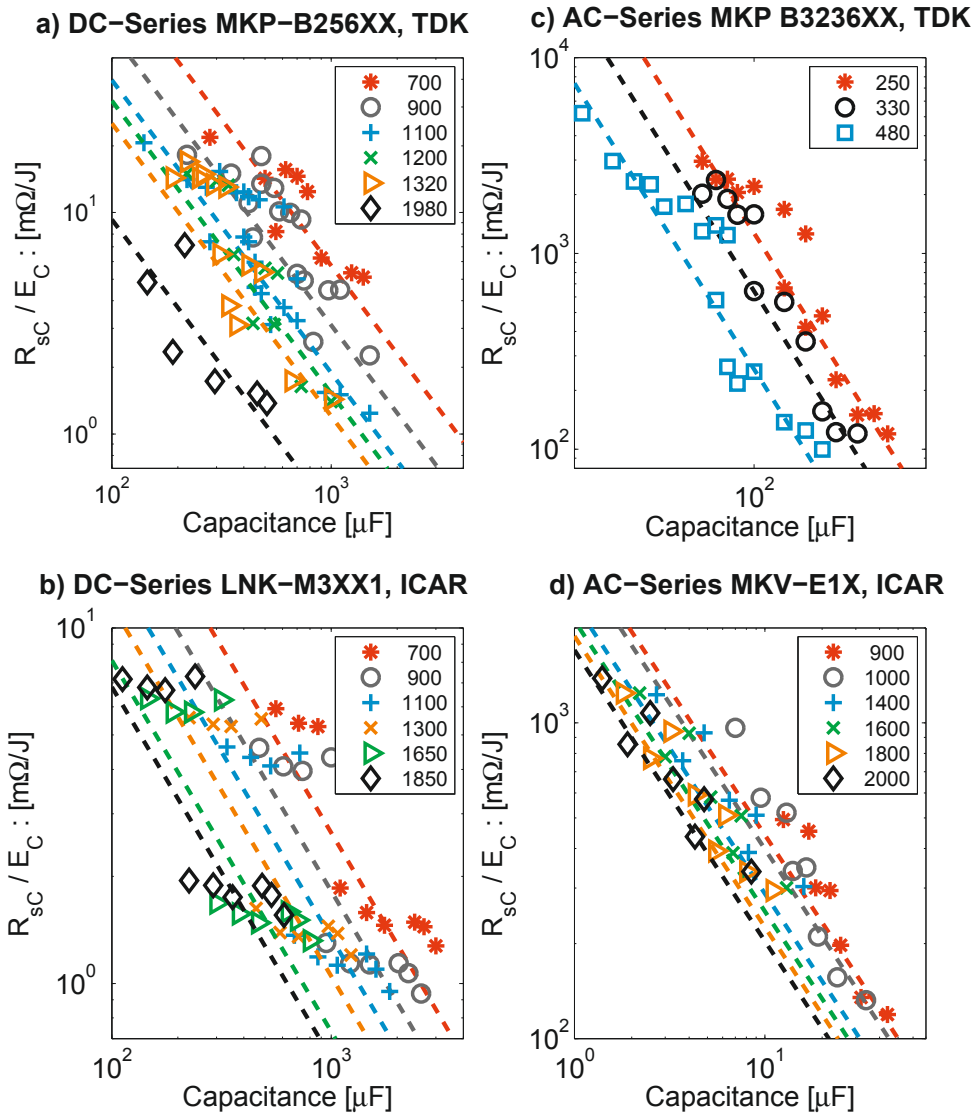


Figure 4.8: Film capacitor series resistance per energy storage vs. capacitance for different voltage ratings and capacitor technologies: a) the DC link capacitors series MKP-B256xx from the manufacturer TDK; b) the DC link capacitor series LNK-M3xx1 from the manufacturer ICAR; c) the AC filter capacitor series MKP B3236 from TDK; d) the AC filter capacitor series MKV-E1x from ICAR. The dashed lines show the fitting curves as given in equation 4.47.

Chapter 5

Medium Frequency Transformer

5.1 Power Losses

The power losses in the MFT consist mainly of core and copper losses. The cooper losses are the sum of the ohmic losses of all windings:

$$P_{W,Tr} = \sum_{i=1}^{nw} (F_{sk(i)} \cdot F_{pe(i)}) \cdot \frac{\rho_{cu} \cdot N_{(i)} \cdot MLT_{(i)}}{A_{w(i)}} \cdot I_{Tr(i)}^2$$

where *nw* is the number of windings, I_{Tr} is the RMS current value in each winding, ρ_{cu} is the resistivity of the conductor, ***MLT*** is the mean length of a turn in the winding, A_w is the wire conduction area, N is the number of turns in each winding, F_{sk} is the skin-effect factor and F_{pe} is the proximity-effect factor. In MFTs, eddy current losses in windings, i.e. the losses due to skin and proximity effects, cannot be ignored. The approximate model for estimating the proximity-effect factor for a litz wire conductor, presented in [36], is used in this paper:

$$F_{pe} = \frac{R'_{ac}}{R_{dc}} = 1 + \frac{5 \cdot p_{layer}^2 \cdot N_s - 1}{45} \cdot \Delta^4, \tag{5.1}$$

$$\Delta = \frac{d_s}{2\delta} \cdot \sqrt{\pi \cdot K_{layer}}; \quad \delta = \sqrt{\frac{\rho_{cu}}{\pi \cdot \mu_0 \cdot f_{Tr}}},$$

$$K_{layer} = \sqrt{\pi N_s} \frac{d_s}{2D_L}; \quad D_L = k_{pf} \cdot d_s \cdot \sqrt{N_s}$$

where f_{Tr} is the working frequency, δ is the skin depth, p_{layer} is the number of layers of winding, N_s is the number of strands of the litz wire conductor, d_s is the diameter of a strand, D_L is the diameter of the litz wire conductor, Δ is the ratio of the thickness of a equivalent rectangular conductor to the skin depth , and k_{pf} is the packing factor ($k_{pf} = 1.28$ for $N_s > 25$). The approximate model for estimating the skin-effect factor presented in [38] is used in this paper:

$$F_{sk} = \begin{cases} 1 + \frac{\Delta^4}{48+0.8\cdot\Delta^4} & \Delta < 1.7 \\ 0.25 + 0.5\Delta + \frac{3}{32\Delta} & \Delta \geq 1.7 \end{cases}$$

In a litz wire conductor, the proximity-effect factor is more important than the skin-effect factor[36]. The strand diameter d_s of litz wire conductor and the number of strands N_s are selected by taking into account the expression derived in [42, 38] which estimates the optimal Δ and thus minimises (5.1):

$$\Delta^4 = \frac{15}{5 \cdot p_{layer}^2 \cdot N_s - 1} \tag{5.2}$$

Additionally, to ensure that the winding does not overheat, the simplest practical assumption is that a certain current density (J_{max}) should not be exceeded. Based on the maximum current (I_{TrMax}) that the transformer will carry, the following equation can be written:

$$\frac{I_{TrMax}}{N_s} = K_{sfw} \cdot J_{max} \cdot \frac{\pi}{4} \cdot d_s^2 \tag{5.3}$$

where K_{sfw} is a safety factor of the maximum current of the conductor, which is set at 0.8. Then, (5.2) and (5.3) can be solved for N_s and d_s to optimize the winding.

By contrast, the core losses depend on the magnetic material, core volume (V_c), working frequency (f_{Tr}), flux density amplitude (B_m) and waveform factor (K_{wf}). The modified Steinmetz equation is often used to evaluate the core losses and it can be expressed simply as a function of the waveform factor of the voltage [1]:

$$P_{C,Tr} = \rho_c \cdot V_c \cdot p_{c0} \cdot \left(\frac{f_{Tr}}{f_0}\right)^{\alpha_C} \cdot \left(\frac{B_m}{B_0}\right)^{\beta_C} \cdot \left(\frac{K_{wf}}{K_{wf0}}\right)^{2(\alpha_C - 1)}$$

where the coefficients α_C and β_C are determined by the characteristics of the material, p_{c0}, f_0, B_0 and K_{wf0} are reference core losses which can be established

from the manufacturer's data sheet. The waveform factor (K_{wf}) of a waveform is defined as the ratio between its RMS-value and its average value of the impressed voltage over the time period between zero and maximal flux density [1].

5.2 Induced Voltage and Power equation

The equation for voltage in a transformer winding is given by [38]

$$V_P = K_{wf} \cdot k_f \cdot N_p \cdot f \cdot B_m \cdot A_{core} \tag{5.4}$$

where K_{wf} is the waveform factor introduced to take into account the ratio of the RMS value of the applied voltage waveform, k_f is the core stacking factor (typically 0.95 for laminated cores), A_{core} is the cross-sectional area of the magnetic core, B_m is the flux density amplitude and $N_p$is the number of turns on the primary winding. The number of turns on the secondary winding is given by:

$$N_S = (V_S/V_P) \cdot N_P \tag{5.5}$$

To ensure the optimum design of the transformer, the winding power loss on the primary side is equal to that on the secondary side [34, 43]. This criterion implies that each winding carry the same current density (J). The sum of VA products for each winding of a transformer is expressed as [38, 37]:

$$\sum VA = K_{wf} \cdot k_f \cdot \frac{k_b}{K_{cu}} \cdot f \cdot B_m \cdot J \cdot A_{core} \cdot b_w \cdot h_w \tag{5.6}$$

where k_b is the ratio of bare conductor area to the window area (typically 0.5 [44]), and the other variables are as defined above.

5.3 Thermal Constraint

The temperature of the transformer should be estimated during the optimisation process to verify that temperature specifications are not exceeded. In a transformer with natural air cooling, as considered in this thesis, the largest heat-transfer mechanism is convection [43]. Newton's equation of convection is therefore used to determine the temperature rise (ΔT_{Tr})of the magnetic component [38, 42]:

$$P_{C,Tr} + P_{W,Tr} = h_{Tr} \cdot A_t \cdot \Delta T_{Tr} = \frac{1.42 \cdot A_t}{H_{Tr}^{0.25}} \cdot \Delta T_{Tr}^{1.25}$$

where A_t is the external surface area of the core and windings, and h_{Tr} is the

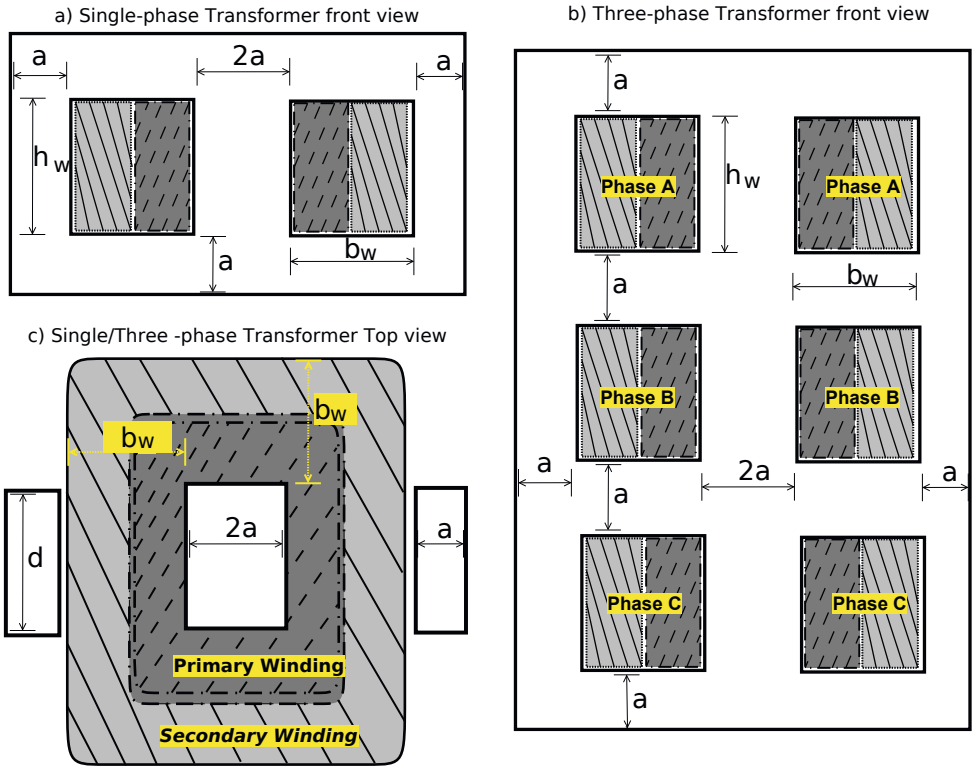


Figure 5.1: Shell-type transformer Structure. a) Front view of single-phase transformer. b) Front view three-phase transformer. c) Top view for both transformers.

convection heat transfer coefficient ($h_{Tr} = 1.42 \cdot (^{\Delta T_{Tr}}/_{H_{Tr}})^{0.25}$ [38]), and H_{Tr} is the height of the transformer.

5.4 Evaluation of Volume and Mass

The design process is developed for dry shell-type transformers. Figure 5.1 shows the front and top section of the single-phase and three-phase transformers. The relevant core dimensions (a, b_w, h_w, d) are indicated on the diagram. Table 5.1 shows the geometric characteristics defined using these relevant core dimensions. The overall volume and active mass of the transformer can be calculated by:

$$Vol_{Tr} = (d + 2b_w)\,(4a + 2b_w)\,((n_\phi + 1) \cdot a + n_\phi \cdot h_w)$$

$$Mass_{Tr} = \rho_c \cdot Vol_c + n_\phi \cdot \rho_{cu} \left(Vol_{cu(1)} + Vol_{cu(2)}\right)$$

Table 5.1: Geometric characteristic of the transformer design process

Single-phase	A_{core}	$2a \cdot d$
	MLT - Low Vol.	$4a + 2d + \pi \cdot D_{L1} \cdot p_{layer1}$
	MLT - High Vol.	$4a + 2d + \pi(b_w - D_{L2} \cdot p_{layer2})$
	Window area	$b_w \cdot h_w$
	Vol_c	$d\,(4a + 2b_w)\,(2a + h_w) - 2\,(b_w h_w d)$
	Winding volume	$(4a + 2d + \pi b_w)\,(b_w \cdot h_w)$
Three-phase	A_{core}	$2a \cdot d$
	MLT - Low Vol.	$4a + 2d + \pi \cdot D_{L1} \cdot p_{layer1}$
	MLT - High Vol.	$4a + 2d + \pi(b_w - D_{L2} \cdot p_{layer2})$
	Window area	$3 \cdot b_w \cdot h_w$
	Vol_c	$d\,(4a + 2b_w)\,(4a + 3h_w) - 6\,(b_w h_w d)$
	Winding volume	$3\,(4a + 2d + \pi b_w)\,(b_w \cdot h_w)$

$$Vol_{cu(i)} = N_{s(i)} \cdot \pi/4 \cdot d^2_{s(i)} \cdot N_{(i)} \cdot MLT_{(i)}$$

where ρ_c is the density of the core material, ρ_{cu} is the density of the conductor material, N is the number of turns (subscript *i=1* means low voltage, *i=2* means high voltage), n_ϕ is the number of phases (*1 or 3*), and the other variables are defined as before.

The optimization criterion to minimise losses and the optimum flux density expression presented in [38] have been taken into account to estimate transformer volume, mass and power losses. The flowchart of the minimum transformer volume is shown in Fig. 5.2. Optimum flux density depends on design requirements and constraints. The main constraints considered in this thesis are: the maximum allowed temperature rise ($\triangle T_{Tr}$), the saturation flux density B_{sat}, the copper fill constraint (which ensures that the transformer windings fit into the transformer window) and the minimum allowed efficiency η_{min}.

An optimisation algorithm was developed to estimate the core dimensions (a, b_w, h_w, d) and the number of layers of each winding (p_{layer1}, p_{layer2}), which minimises the objective function (OF_{Tr}) defined by (5.7) for a given set of input variables (nominal power, input voltage, voltage ratio, maximum input current, waveform factor, and frequency).

$$OF_{Tr} = \frac{P_{Tr}}{P_{Tr,min}} + \frac{Vol_{Tr}}{Vol_{Tr,min}} + \frac{Mass_{Tr}}{Mass_{Tr,min}}, \tag{5.7}$$

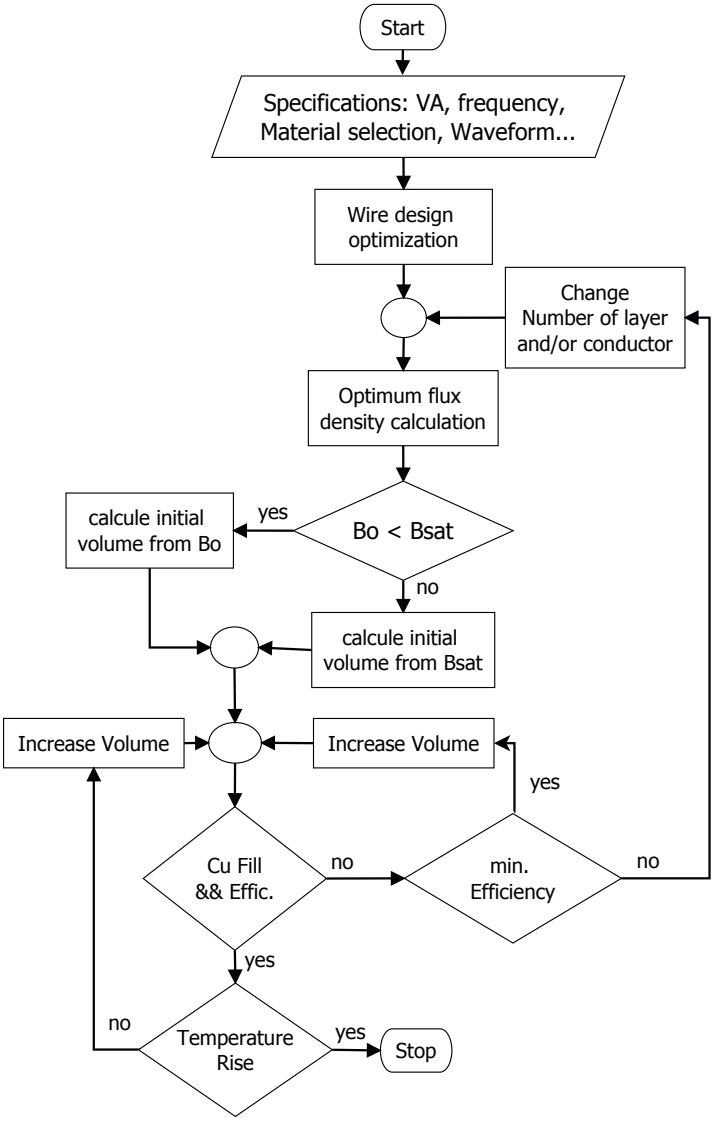


Figure 5.2: Basic flowchart to minimise transformer volume

Table 5.2: Transformer specifications of design example [1]

Rated Power	3 MW		Rated Frequency	500 Hz
Rated Low voltage	3 kV		Peak flux density	1 T
Rated High voltage	33 kV		Max. current density	4 A/mm^2

$$P_{Tr} = P_{W,Tr} + P_{C,Tr}.$$

Figure 5.3 and Figure 5.4 show the results of the optimization algorithm for a 3MW-500Hz single-phase shell-type transformer with specifications listed in Table 5.2. To examine how the Pareto-Front of the proposed methodology compares with a commericially available transformer design, Figure 5.3 and Figure 5.4 include a reference design, which refers to transformer design results presented in [1] for the same transformer specifications and similar constraints. Furthermore, Figure 5.3 and Figure 5.4 show a selected design, i.e. the design that minimises the objective function (5.7). Unlike the proposed model, the transformer design presented in [1] takes into account the use of cooling ducts for the thermal design, enabling a more compact solution.

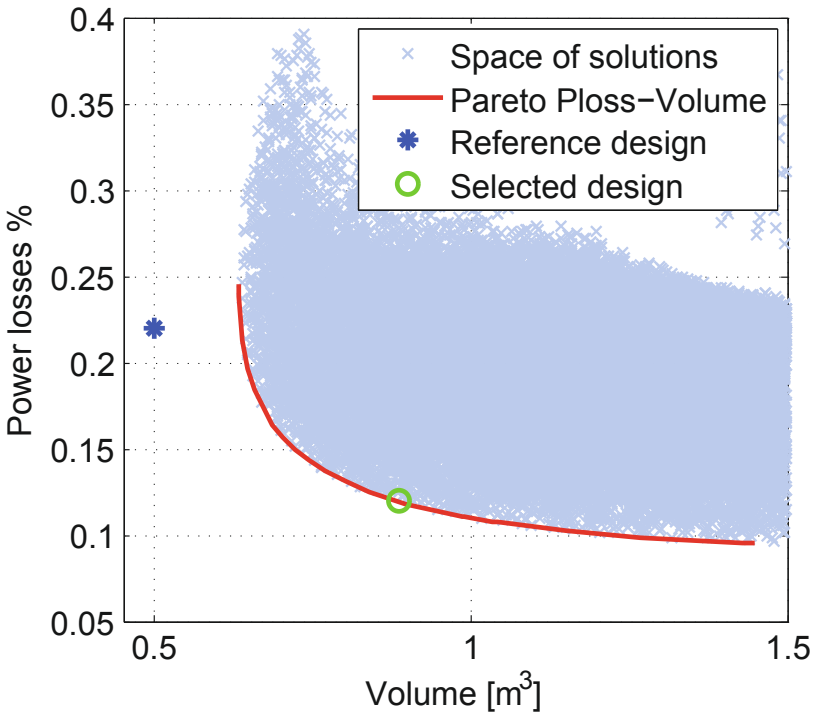


Figure 5.3: MFT performance space Power Losses vs. Volume. Results for a design example of a $3MW$-$500Hz$ single-phase shell-type transformer.

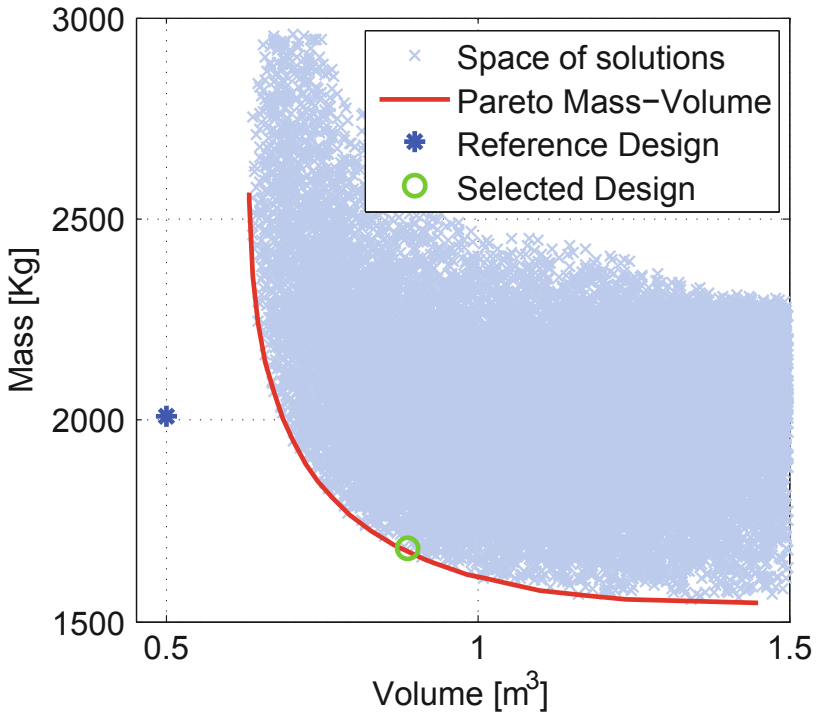


Figure 5.4: MFT performance space Volume vs. Mass. Results for a design example of a $3MW$-$500Hz$ single-phase shell-type transformer.

Part III

Application to offshore wind power converters and Conclusion

Chapter 6

Back-to-Back Converters for Offshore AC-Grids

Full scale power converters have become the conversion system of choice in WTs for several reasons, primarily because they allow turbines to operate in a wide speed range which increases the energy harvest, and they enable the use of efficient PMSGs. As the wind energy penetration increases, the grid code becomes increasingly strict and can only be fulfilled with a full scale power converter.

Therefore, full-scale power converters are used increasingly in offshore wind power. Two main topologies in commercial full-scale converters for offshore AC grid parks have been described in the literature, the Two-Level Voltage Source Converter (2L-VSC) and the Three-Level Neutral Point Clamped (3L-NPC) [45, 33].

The evaluation of η, ρ and γ of a Back-to-Back converter based on the 2L-VSC has been chosen as an applied example of the models introduced in this thesis. Figure 6.1 shows the basic schematic of the 2L-VSC with unidirectional switches implemented by IGBTs with anti-parallel diodes. All the aspects needed to design a 2L-VSC with IGBTs and to evaluate its η, ρ and γ are presented herein.

6.1 Modulation strategies

The goal of the modulation strategy is to synthesise a desired output voltage by controlling the switch states of the converter. The aim of this section is to characterise the modulation strategy to evaluate the power losses of the switches, but the reader can refer to [34] for an introduction to Pulse Width Modulation (PWM) methods or to [46] for details about the most relevant modulation techniques based on Space Vector Modulation (SVM).

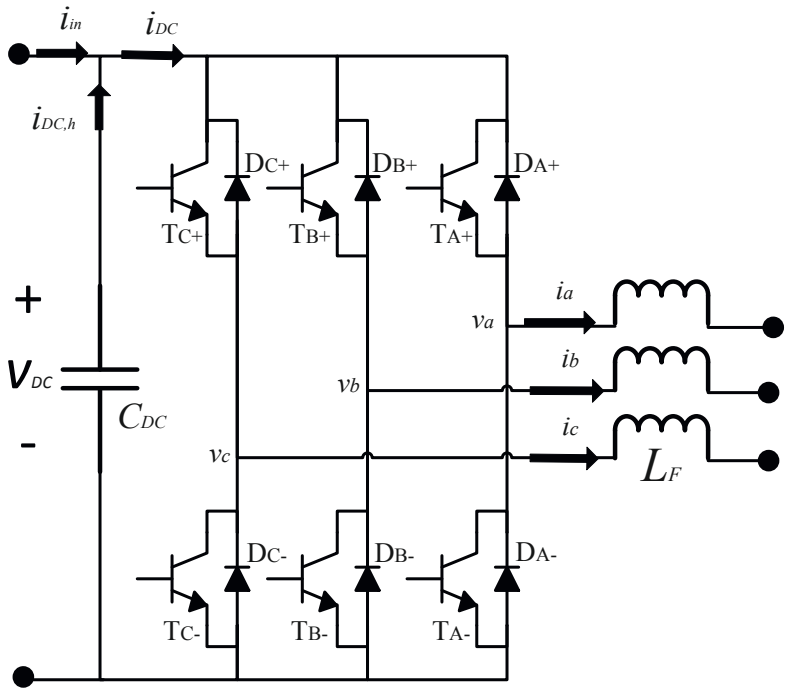


Figure 6.1: Two level voltage source converter (2L-VSC) with IGBTs

The modulation strategy strongly affects the η of the converter; therefore, at least two modulation strategies should be compared when the converter is designed. In this chapter, three modulation strategies are considered: Sinusoidal PWM (SPWM), Space Vector PWM (SVPWM) (also called suboptimal modulation) and a discontinuous modulation scheme known as Symmetrical Flat-Top Modulation (SFTM). Details of SPWM modulation can be found in [47, 34]. Details about SVPWM and SFTM modulation methods can be found in [46, 47].

To characterise a given modulation strategy, two main variables have to be evaluated: the modulation index and the relative turn-on time of the converter bridge legs. Different definitions of the modulation index exist in the literature [46]; thus, to compare the three modulation methods considered, it is convenient to define the modulation index as follows:

$$M_S = \frac{\|v_A^*\|}{V_{A,om}} \tag{6.1}$$

where v_{A*} is the desired inverter phase peak voltage, and $V_{A,om}$ is the maximum amplitude of the phase voltage reference at which the modulation approach enters the over-modulation range. Thus, the modulation index becomes unity at the over-modulation boundary. The value of $V_{A,om}$ depends on the modulation method, and for the modulation methods considered:

$$V_{A,om} = \begin{cases} \frac{V_{DC}}{2} & for\, SPWM \\ \frac{V_{DC}}{\sqrt{3}} & for\, SVPWM\, and\, SFTM \end{cases} \tag{6.2}$$

From the definition in equation 6.1, the desired RMS inverter reference line-to-line voltage (V_{LL}) is related to the modulation index as follows:

$$V_{LL} = \sqrt{3} \cdot M_S \cdot K_{mod} \cdot V_{DC} \tag{6.3}$$

$$K_{mod} = \begin{cases} \frac{\sqrt{2}}{4} & for\, SPWM \\ \frac{1}{\sqrt{6}} & for\, SVPWM\, and\, SFTM \end{cases} \tag{6.4}$$

However, the phase modulation function should be defined for each modulation method to calculate the relative turn-on time of the converter bridge legs. Considering a purely sinusoidal three phase voltage, it can be defined by the output phase voltage (v_{a*}):

$$v_{a*}(wt) = \sqrt{\frac{2}{3}} \cdot V_{LL} \cdot \sin(wt) \tag{6.5}$$

The phase modulation function (m_a) is defined by equations 6.6, 6.7 and 6.8 for SPWM [47], SVPWM [46] and SFTM [46] modulations, respectively. Once the phase modulation function has been obtained, the relative turn-on time of the converter bridge leg a (α_a) can be calculated according to equation 6.9 [47]. Figure 6.2 shows the relative turn-on time of the converter bridge leg a (α_a) for the modulation methods considered.

$$m_{a,SPWM}(wt) = M_S \cdot \sin(wt) \tag{6.6}$$

$$m_{a,SVPWM}(wt) = \frac{2}{\sqrt{3}} \cdot M_S \cdot \sin(wt) + v_{0,SVPWM} \tag{6.7}$$

$$v_{0,SVPWM} = \begin{cases} \frac{1}{2} \cdot \frac{v_{a*}}{V_{A,OM}} & if\ \|v_{c*}\| > \|v_{a*}\| < \|v_{b*}\| \\ \frac{1}{2} \cdot \frac{v_{b*}}{V_{A,OM}} & if\ \|v_{a*}\| > \|v_{b*}\| < \|v_{c*}\| \\ \frac{1}{2} \cdot \frac{v_{c*}}{V_{A,OM}} & if\ \|v_{b*}\| > \|v_{c*}\| < \|v_{a*}\| \end{cases}$$

$$m_{a,SFTM}(wt) = \frac{2}{\sqrt{3}} \cdot M_S \cdot \sin(wt) + v_{0,SFTM} \tag{6.8}$$

$$v_{0,SFTM} = \begin{cases} \frac{\|v_{a*}\|}{v_{a*}} - \frac{v_{a*}}{V_{A,OM}} & if\ \|v_{c*}\| < \|v_{a*}\| > \|v_{b*}\| \\ \frac{\|v_{b*}\|}{v_{b*}} - \frac{v_{b*}}{V_{A,OM}} & if\ \|v_{a*}\| < \|v_{b*}\| > \|v_{c*}\| \\ \frac{\|v_{c*}\|}{v_{c*}} - \frac{v_{c*}}{V_{A,OM}} & if\ \|v_{b*}\| < \|v_{c*}\| > \|v_{a*}\| \end{cases}$$

$$\alpha_a(wt) = \frac{1}{2} \cdot (1 + m_a(wt)) \tag{6.9}$$

6.2 Evaluation of the semiconductor device currents

To calculate the power losses of each device (IGBT and Diode), it is necessary to calculate the average and RMS values of the current that each device conducts in a particular period (needed to evaluate equation 3.6) and those of the current through the device at moment it is turned on or off (needed to evaluate equations 3.18 and 3.20). Unfortunately, there is no simple relationship between the RMS output current (I_a) and the current in the diode (I_d) and IGBT (I_t). The current

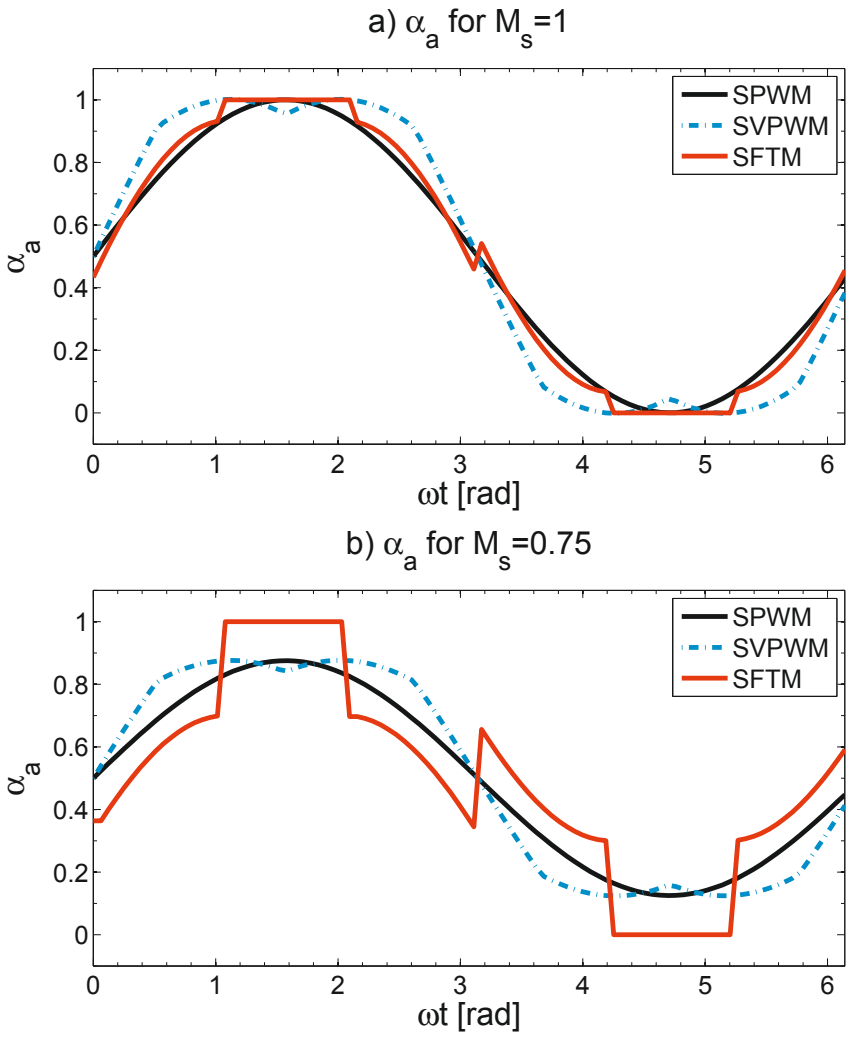


Figure 6.2: The relative turn-on time of the voltage source inverter bridge leg a (α_a) for three different modulation methods: SPWM (Sinusoidal PWM), SVPWM (Space-vector PWM), and SFTM (Symmetrical Flat-Top Modulation).

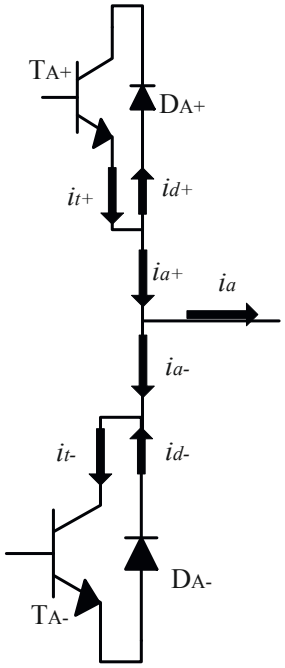


Figure 6.3: Bridge leg current definitions for the 2L-VSC

distribution between diode (*DA*+) and IGBT (*TA*-) is a function of the relative turn-on time of the converter bridge leg (α_a), the modulation index (M_s) and the displacement angle (ϕ) between the inverter phase voltage and current [46].

To establish a relationship between the output current and the currents of the diode and IGBT, Figure 6.3 defines the current of the elements in a bridge leg of the 2L-VSC. From Figure 6.3, the relationship between the current of the diode and that of the IGBT at any time is given by:

$$i_a = \begin{cases} i_{t+} + i_{d-} & if\, i_a > 0 \\ i_{t-} + i_{d+} & if\, i_a \leq 0 \end{cases} \tag{6.10}$$

The currents i_{t+} and i_{d-} (or i_{t-} and i_{d+}) are orthogonal; therefore, when the upper IGBT (TA+) is conducting, the lower Diode (*DA*-) is not (and vice versa). The average current through the IGBT and diode respectively can be evaluated by:

$$I_{t,AVG} = \frac{1}{2\pi}\int_{\phi}^{\pi+\phi} (\alpha_a(\theta) \cdot i_a(\theta)) \cdot d\theta \tag{6.11}$$

$$I_{d,AVG} = \frac{1}{2\pi}\int_{\phi}^{\pi+\phi} ((1-\alpha_a(\theta)) \cdot i_a(\theta)) \cdot d\theta \tag{6.12}$$

where ϕ is the displacement angle between the inverter phase voltage (v_a) and current (i_a), and α_a is the relative turn-on time of the converter bridge leg a for the modulation methods considered (defined by equation 6.9). Assuming a purely sinusoidal phase current with RMS value (I_a), [47] evaluated the equations 6.11 and 6.12 for SPWM modulation, and [46] evaluated them for SVPWM and SFTM modulations. Comparison of the results from [46] and [47] reveals that the average current through the IGBT and diode is independent of the chosen PWM modulation method and is given by [46]:

$$I_{t,AVG} = \left(\frac{\sqrt{2}}{2\pi} + \frac{K_{mod}}{2} \cdot M_S \cdot \cos(\phi)\right) \cdot I_a \tag{6.13}$$

$$I_{d,AVG} = \left(\frac{\sqrt{2}}{2\pi} - \frac{K_{mod}}{2} \cdot M_S \cdot \cos(\phi)\right) \cdot I_a \tag{6.14}$$

Similarly, the RMS current through the IGBT and diode can be evaluated by:

$$I_{t,RMS} = \sqrt{\frac{1}{2\pi}\int_{\phi}^{\pi+\phi} (\alpha_a(\theta) \cdot i_a^2(\theta)) \cdot d\theta} \tag{6.15}$$

$$I_{d,RMS} = \sqrt{\frac{1}{2\pi}\int_{\phi}^{\pi+\phi} ((1-\alpha_a(\theta)) \cdot i_a^2(\theta)) \cdot d\theta} \tag{6.16}$$

In contrast with the average current expression, the expression for the RMS current is dependent on the selected modulation technique. Equations 6.17, 6.18 and 6.19 show the closed-form expression for the ratio of IGBT RMS current to RMS phase current of the inverter, which are reported in [47] for SPWM and in [46] for SVPWM and SFTM.

SPWM modulation

$$\left(\frac{I_{t,RMS}}{I_a}\right)^2 = \frac{3\pi + 8 \cdot M_S \cdot \cos(\phi)}{12\pi} \tag{6.17}$$

SVPWM modulation

$$\left(\frac{I_{t,RMS}}{I_a}\right)^2 = \begin{cases} \frac{-M_s+3\pi-4M_S\cos^2(\phi)+8\sqrt{3}M_S\cos(\phi)}{12\pi} & \|\phi\| < \frac{\pi}{6} \\ \frac{3\pi+2M_S\cdot\left(2+\frac{\sqrt{3}}{2}\sin\|2\phi\|-\cos^2(\phi)\right)}{12\pi}\ldots & \frac{\pi}{6} < \|\phi\| < \frac{\pi}{2} \\ \ldots + \frac{2M_S\cdot\left(-2\sin\|\phi\|+2\sqrt{3}\cos(\phi)\right)}{12\pi} & \end{cases} \tag{6.18}$$

SFTM modulation

$$\left(\frac{I_{t,RMS}}{I_a}\right)^2 = \begin{cases} \frac{(6-8M_S)\sqrt{3}\cos^2(\phi)+\sqrt{3}M_S(4+8\cos(\phi))}{12\pi}\ldots & \|\phi\| < \frac{\pi}{3} \\ \ldots\frac{-8M_S\sin\|\phi\|+(4M_S-3)\sin\|2\phi\|-3\sqrt{3}+2\pi+6\|\phi\|}{12\pi} & \\ \frac{3\pi-3\|\phi\|+(4M_s-3)\sin\|2\phi\|}{6\pi} & \frac{\pi}{3} < \|\phi\| < \frac{\pi}{2} \end{cases} \tag{6.19}$$

The ratio of Diode RMS current to RMS phase current of the inverter can be calculated by

$$\left(\frac{I_{d,RMS}}{I_a}\right)^2 = \frac{1}{2} - \left(\frac{I_{t,RMS}}{I_a}\right)^2 \tag{6.20}$$

Expressions 6.13, 6.14 and 6.17-6.20 are valid if the active power flows out of the inverter, as defined from Figure 6.3, which shows the inverter operation mode. In the case of rectifier operation (the power flows in the opposite direction), the expressions for the diode and IGBT must be exchanged.

However, to evaluate the switching losses, it is necessary to calculate the average and RMS values of current through the IGBT device at the moment afterit is turned on ($I_{ta,AVG}$ and $I_{ta,RMS}$) and the average and RMS values of current through the IGBT and Diode devices at moment before they are turned off ($I_{tb,AVG}$, $I_{tb,RMS}$, $I_{db,AVG}$ and $I_{db,RMS}$).

Given that the current through the upper IGBT commutates to the lower diode, the turn on switching current of the upper IGBT is approximately equal to the turn off switching current of the lower diode ($i_{ta+} \approx i_{db-}$). Furthermore, for

switching frequencies much higher than the fundamental frequency, the current along a switching period can be assumed to be constant, and therefore the turn on switching current can be approximated to the turn off switching current ($i_{ta+} \approx i_{db+}$). Therefore, the average and RMS values of switching currents through the all devices (IGBT and diode) are approximately equal:

$$I_{swa,AVG} = I_{ta,AVG} = I_{tb,AVG} = I_{db,AVG} \tag{6.21}$$

$$I_{swa,RMS} = I_{ta,RMS} = I_{tb,RMS} = I_{db,RMS} \tag{6.22}$$

The average and RMS values of the switching current can be calculated as follows:

$$I_{swa,AVG} = \frac{1}{2\pi} \int_{\phi}^{\pi+\phi} \left(\alpha_{swa}\left(\theta\right) \cdot i_a\left(\theta\right)\right) \cdot d\theta \tag{6.23}$$

$$I_{swa,RMS} = \sqrt{\frac{1}{2\pi} \int_{\phi}^{\pi+\phi} \left(\alpha_{swa}\left(\theta\right) \cdot i_a^2\left(\theta\right)\right) \cdot d\theta} \tag{6.24}$$

Where α_{swa} is the switching function of the converter, which is a function of the relative turn-on time of the converter bridge leg and is given by:

$$\alpha_{swa} = \begin{cases} 1 & 0 < \alpha_a < 1 \\ 0 & \alpha_a = 1 \, or \, \alpha_a = 0 \end{cases} \tag{6.25}$$

Equation 6.25 shows that the switching function is constant and equal to 1 for the SPWM and SVPWM modulation methods, but SFTM modulation has different values. Equations 6.26 to 6.29 show the closed-form expression for the average and RMS values of the equations evaluating the switching current 6.23 and 6.24 for the modulation methods considered.

SPWM and SVPWM modulation

$$I_{swa,AVG} = \frac{\sqrt{2}}{\pi} \cdot I_a \tag{6.26}$$

$$I_{swa,RMS} = \frac{1}{\sqrt{2}} \cdot I_a \tag{6.27}$$

SFTM modulation

$$I_{swa,AVG} = \begin{cases} \frac{\sqrt{2}(2-\cos(\phi))}{2\pi} I_a & \|\phi\| < \frac{\pi}{3} \\ \frac{\sqrt{6}\sin\|\phi\|}{2\pi} I_a & \frac{\pi}{3} < \|\phi\| < \frac{2\pi}{3} \\ \frac{\sqrt{2}(2-+\cos(\phi))}{2\pi} I_a & \frac{2\pi}{3} < \|\phi\| < \pi \end{cases} \tag{6.28}$$

$$I_{swa,RMS} = \sqrt{\frac{1}{3\pi} - \frac{\sqrt{3}}{4\pi} \cdot \cos(2\phi)} \cdot I_a \tag{6.29}$$

6.3 Main guidelines for the design of a 2L-VSC

To evaluate the η and ρ of a converter, the components first have to be selected. The selection of components depends on the requirements of the application like the limit of the current and voltage ripples or peak values of the current and voltage. In the case of a 2L-VSC, three main parts can be distinguished: the DC link, the AC filter and the switch valves. The main guidelines for the design of these parts are presented below.

6.3.1 DC-link design and semiconductor voltage rating requirements

The design of the DC-link in a 2L-VSC is based on the selection of a nominal DC voltage ($V_{DC,N}$) and the specification of the capacitance value (C_{DC}) in Figure 6.1. The nominal DC voltage is related to the nominal AC voltage by (from equation 6.3):

$$V_{DC,N} = \frac{V_{LL,N}}{\sqrt{3} \cdot K_{mod} \cdot M_{S,nom}} \tag{6.30}$$

where $V_{LL,N}$ is the nominal line-to-line RMS voltage and $M_{S,nom}$ is the modulation index at nominal operation. Assuming that the voltage $V_{LL,N}$ is given by the application, then the nominal modulation index $M_{S,nom}$ should be determined.

When designing the DC voltage, a safety margin for the operation of the 2L-VSC is taken into account to guarantee controllability under abnormal conditions. The boundary of over-modulation occurs when equals one, therefore $M_{S,nom}$ should be lower but close to one. For example, a value of 0.98 for $M_{S,nom}$ will leave a safety margin of approximately 2% for operation, i.e. the 2L-VSC can manage a 2% increase in voltage without entering the over-modulation range. Low values of $M_{S,nom}$ will require higher values of nominal DC voltage, which are mainly

limited by power semiconductor technology if the connection of devices in series is to be avoided.

In the 2L-VSC configuration, each valve will support the total DC voltage, and if the semiconductors are not connected in series, the minimum blocking voltage required by the semiconductor device can be calculated by (from equation 3.29)

$$V_{block,min} = \begin{cases} \frac{V_{DC,N} \cdot k_{ovf}}{k_{vdc}} & for\ \delta_{Vdc} \leq 2 \cdot \left(\frac{k_{vp}}{k_{vdc}} - 1 \right) \\ \frac{V_{DC,N} \cdot k_{ovf} \left(1 + \frac{\delta_{Vdc}}{2} \right)}{k_{vp}} & for\ \delta_{Vdc} > 2 \cdot \left(\frac{k_{vp}}{k_{vdc}} - 1 \right) \end{cases} \tag{6.31}$$

where δ_{Vdc} is the ratio of peak-to-peak voltage ripple to DC voltage, and k_{ovf} is the over voltage factor. For typical industrial networks, $k_{ovf} = 1.1$ for low voltage systems ($V_{DC,N} < 1\,kV$) and $k_{ovf} = 1.15$ for medium voltage systems [29]. The voltage device rating is selected as the next standard device voltage rating higher than $V_{block,min}$. Standard voltage ratings for commercial IGBT power modules (IGBTs with anti-parallel diodes) are 1.2 *kV*, 1.7 *kV*, 2.5 *kV*, 3.3 *kV*, 4.5 *kV* and 6.5 *kV*.

Figure 6.4 shows the selection of IGBT power modules as a function of the nominal modulation index and the nominal line-to-line voltage for a 2L-VSC, when the relative peak-to-peak DC-link ripple is lower than 20% and the safety factors are $k_{vp} = 0.8$ and $k_{vdc} = 0.65$. Figure 6.4a presents the selection map for SPWM and Figure 6.4b shows the selection map when SVPWM or SFTM is selected. For the sake of simplicity, only three standard voltage ratings are shown in Figure 6.4 (1.7 *kV*, 3.3 *kV* and 6.5 *kV*).

From Figure 6.4, it can be noted that for a given nominal voltage, the applicability of a given power module is limited if the nominal modulation index is decreased in the 2L-VSC. Furthermore, under these conditions, the use of the 2L-VSC in medium voltage systems is restricted by IGBT module technology, which limits the application nominal voltage to around 2.2 *kV* with SPWM and to around 2.5 *kV* with SVPWM or SFTM.

By contrast, the DC-link capacitance can be designed according to expression presented in [48], which is derived with the knowledge that, in one switching cycle, the input power drops to zero while the inverter keeps the maximum output power, or vice versa:

$$C_{DC} = \frac{P_N}{V_{DC,N}^2 \cdot \left(\delta_{Vdc} + 0.5 \cdot \delta_{Vdc}^2 \right) \cdot f_{sw}} \tag{6.32}$$

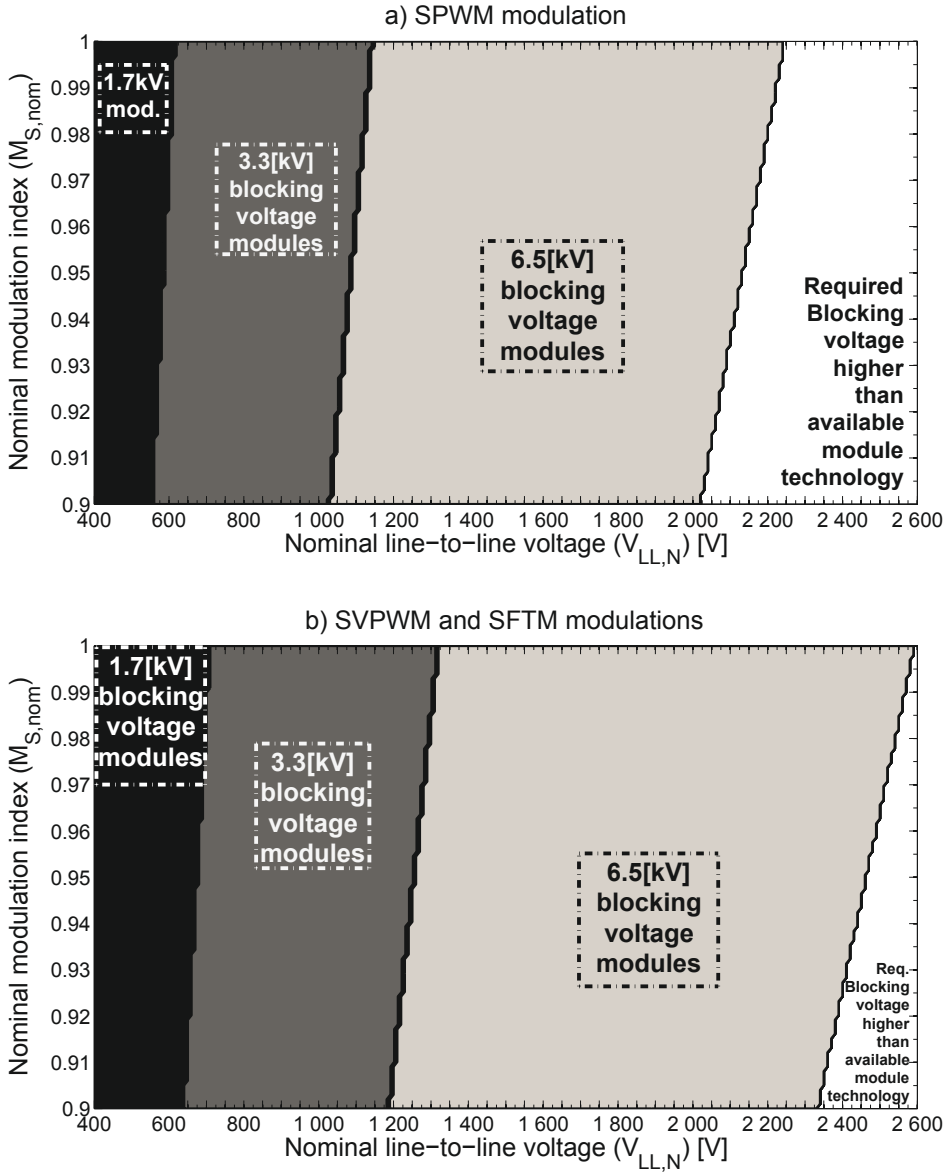


Figure 6.4: Selection of IGBT modules depending on required blocking voltage in a 2L-VSC. For illustration simplicity, only three standard voltage ratings are taken into account. a) SPWM modulation; b) SVPWM and SFTM modulation.

where P_N is the nominal power of the 2L-VSC and f_{sw} is the switching frequency of the converter. Since the nominal power and the line-to-line voltage (which defines the DC-link voltage) are given by the specifications of the application, the DC-link capacitance will be determined by the selected switching frequency and the relative peak-to-peak DC-link ripple, which are considered to be design variables. Normally, their values are limited by design constraints.

The maximum switching frequency is determined by the switch device technology. IGBT power modules can have switching frequencies of up to 4 *kHz* [29] (depending on the voltage rating). The maximum relative peak-to-peak DC-link ripple is given by specifications related to stability and controllability requirements of the system, and may be limited to 6%.

Once the nominal DC voltage ($V_{DC,N}$) and the capacitance value (C_{DC}) have been defined, the volume, mass and capacitor dielectric losses can be calculated using models presented in section 4.2. However, the capacitor RMS current should be evaluated to calculate the capacitor resistive losses (equation 4.46). From Figure 6.1, the capacitor current can be defined by the DC-link input current (i_{in}) and the input current of the Voltage Source Converter (VSC) (i_{vsc}). Given that the DC component of i_{vsc} is supplied by the DC-link input current (i.e., $I_{in,AVG} = I_{vsc,AVG}$), the capacitor current is defined solely by the AC components of i_{in} and i_{vsc} [49]:

$$i_C = i_{vsc,AC} - i_{in,AC} \tag{6.33}$$

It is difficult to derive the capacitor RMS current using equation 6.33; therefore, we can consider that the currents i_{in} and i_{vsc} do not contain common harmonics (which may be the case if the input current comes from a bridge diode rectifier or from a PWM rectifier operated at a different switching frequency). Then, the current stress on the DC-link capacitor can be approximated by [49]:

$$I^2_{C,RMS} = I^2_{vsc,AC,RMS} + I^2_{in,AC,RMS} \tag{6.34}$$

The analytical expression presented in [49], is used to evaluate how the VSC contributes to current stress of the DC-link capacitor. For any PWM modulation method, and assuming a purely sinusoidal phase current:

$$I_{vsc,AC,RMS}^2 = \frac{\sqrt{6} \cdot K_{mod} \cdot M_S}{\pi} \cdot \left[1 + \left(4 - \frac{3\sqrt{6}\pi \cdot K_{mod} \cdot M_S}{2} \right) \cdot \cos^2(\phi) \right] \cdot I_a^2 \tag{6.35}$$

The contribution of the DC-link input current to current stress of the DC-link capacitor is determined by the type of rectifier interfacing the 2L-VSC. In brief, it can be considered to be a system specification parameter for the design of the 2L-VSC. This value can be defined relative to the DC component of the DC-link:

$$I_{in,AC,RMS} = \delta_{Iin} \cdot I_{in,AVG} \tag{6.36}$$

where δ_{Iin} is the ratio of the RMS ripple component to the DC component of the DC-link input current. Given that $I_{in,AVG} = I_{vsc,AVG}$, and that the average input current of the VSC is calculated from the average current of the upper devices (*TA*+, *DA*+, *TB*+, *DB*+, *TC*+ and *DC*+, in Figure 6.1), the average DC-link current can be expressed by:

$$I_{in,AVG} = I_{vsc,AVG} = 3 \cdot (I_{t,AVG} - I_{d,AVG}) = 3 \cdot K_{mod} \cdot M_S \cdot \cos(\phi) \cdot I_a \tag{6.37}$$

Figure 6.5a shows how the DC-link capacitor current RMS value (normalized by the RMS phase current) depends on the scaled modulation index ($K_{mod} \cdot M_S$) for two displacement factor values ($cos(\phi) = 0.6$ and $cos(\phi) = 1$) and different values of the ratio δ_{Iin}. The three-dimensional representation of the dependency of DC-link capacitor current RMS value on the modulation index and displacement factor (for $\delta_{Iin} = 30\%$) is presented in Figure 6.5b.

6.3.2 AC filter inductor and current ripple

The input inductance (L_F) is sized according to [50], which presents a theoretical derivation based on the peak-to-peak current ripple ($\triangle I_{Lh}$) at the switching frequency (f_{sw}) for a given line-to-line voltage amplitude (V_{LL}) and a DC-link voltage (V_{DC}):

$$L_F = \left(\frac{V_{LL}}{\sqrt{3}} - \frac{V_{LL}^2}{2 \cdot V_{DC}} \right) \cdot \frac{1}{\triangle I_{Lh} \cdot f_{sw}} \tag{6.38}$$

Since the maximum peak-to-peak current ripple is normally specified by the ratio of peak-to-peak current ripple to maximum fundamental nominal current (δ_{iL}), the

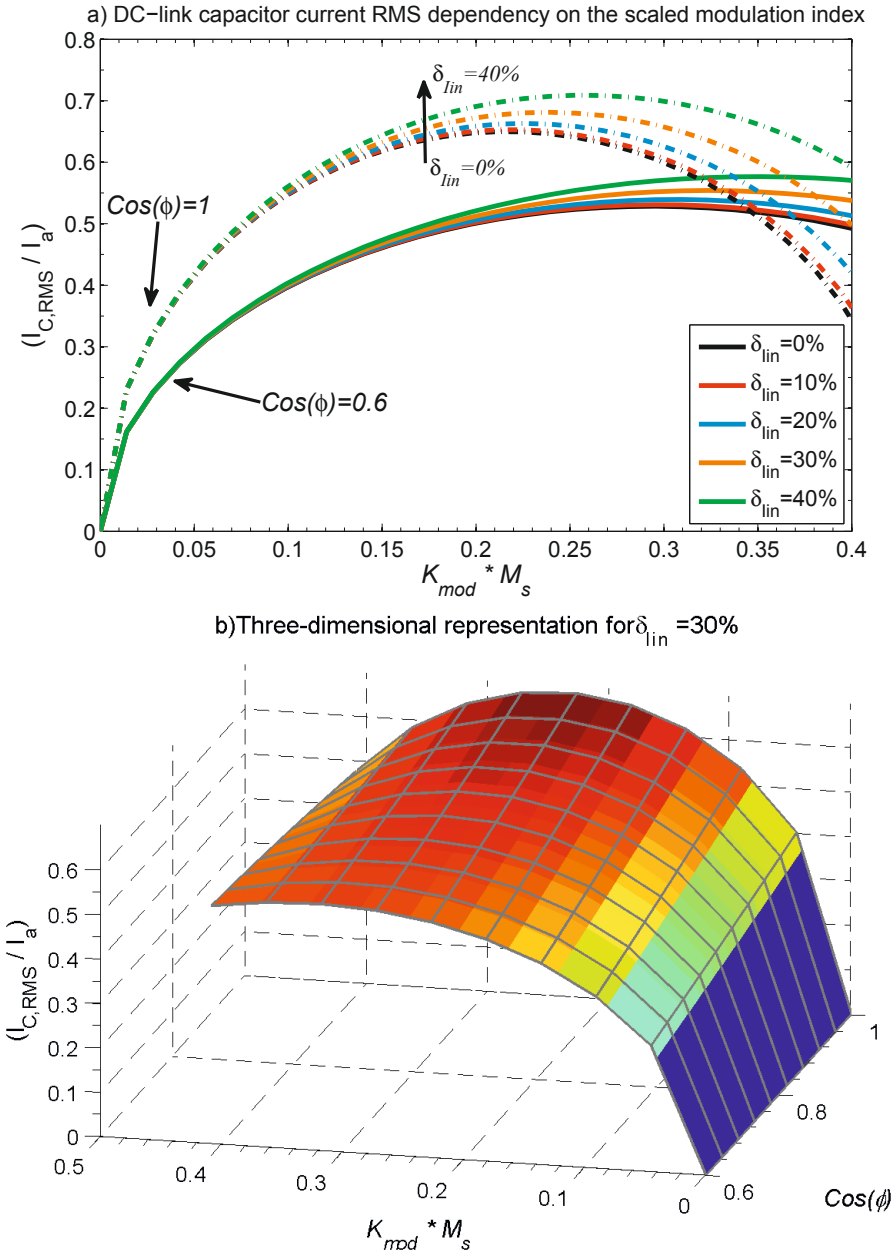


Figure 6.5: Dependency of the DC-link capacitor current RMS value on the scaled modulation index $(K_{mod} \cdot M_S)$ and the displacement factor $\cos(\varphi)$ of the fundamental phase voltage and the phase current in a 2L-VSC. a) Dependency on scaled modulation index for two displacement factor values (0.6 and 1) and five values of the ratio δ_{Iin}. b) Three-dimensional representation for $\delta_{Iin} = 30\%$

inductance value required to limit the current ripple can be calculated as follows (using equations 4.15 and 6.30):

$$L_F = \left(1 - \frac{3}{2} \cdot K_{mod} \cdot M_{S,nom}\right) \cdot \frac{V_{LL,N}^2 \cdot \cos(\phi)}{\sqrt{2} \cdot \delta_{iL} \cdot f_{sw} \cdot P_N} \tag{6.39}$$

Normally, the inductance value is limited by the maximum ratio of inductor voltage to line-to-line voltage at nominal power (δ_{VL}); therefore, using inductor RMS current at the fundamental frequency f_1, the maximum inductance value can be approximated by:

$$L_{F,max} = \frac{3 \cdot \delta_{VL} \cdot V_{LL,N}^2 \cdot \cos(\phi)}{\pi \cdot f_1 \cdot P_N \cdot \sqrt{6 + \delta_{iL}^2}} \tag{6.40}$$

Additionally, if the 2L-VSC interfaces a machine (motor or generator), the equivalent per phase inductance of the machine (L_M) acts as an additional filter. In this case, it is possible to reduce the value of the inductor filter L_F, and the AC filter is not necessary for some conditions (when $L_F < L_M$). If the converter interfaces a machine, the input inductance can be calculated by:

$$L_F = \left(1 - \frac{3}{2} \cdot K_{mod} \cdot M_{S,nom}\right) \cdot \frac{V_{LL,N}^2 \cdot \cos(\phi)}{\sqrt{2} \cdot \delta_{iL} \cdot f_{sw} \cdot P_N} - L_M \tag{6.41}$$

Finally, the nominal inductor RMS current (I_{LF}) should be calculated to evaluate the inductor volume, mass and power losses using models presented in section 4.1. Given the approximation of Figure 4.3, the inductor RMS current is calculated as follows:

$$I_{LF} = \sqrt{I_a^2 + I_{Lh}^2} = \sqrt{1 + \frac{\delta_{iL}^2}{6}} \cdot \frac{P_N}{\sqrt{3} \cdot V_{LL,N} \cdot \cos(\phi)} \tag{6.42}$$

6.3.3 Switch valve design and selection of semiconductor devices

To design the switch valve, first the required blocking voltage and the maximum peak current of the valve should be calculated. The semiconductor device used in the valve is then selected from a set of available devices, depending on the preferred type of connection (series, parallel or neither) and the maximum rating

of the available devices. Once the device has been selected, the semiconductor power losses can be calculated for the worst operating condition and therefore the size of the module cooling system can be estimated using models from chapter 3.

For the sake of simplicity, only the design of the switch valve for the 2L-VSC with a parallel connection of the IGBT modules is discussed in detail, but it should be noted that the design process can easily be adapted to devices connected in series (considering section 3.3). In addition, to simplify the selection of the devices, only the IGBT modules presented in Table 3.2 with ratings 1.7*kV*/3600*A*, 3.3*kV*/1500*A* or 6.5*kV*/750*A* are considered (which are also considered in Figure 6.4).

If the device is not connected in series, the expression derived for the minimum blocking voltage required by the semiconductor device can be used (equation 6.31 and Figure 6.4) and the nominal line-to-line voltage is limited to around 2.5 *kV* (with SVPWM) for the devices considered (maximum 6.5 *kV* blocking voltage), as discussed previously. The maximum peak current of the parallel connection (valve) is given by the phase current, its current ripple component and the overload factor (k_{olf}) (typically 30%; then $k_{olf} = 0.3$), and can be calculated by:

$$I_{psw} = \sqrt{2} \cdot I_a \cdot \left(1 + \frac{\delta_{iL}}{2}\right) \cdot (1 + k_{olf}) = \sqrt{\frac{2}{3}} \cdot \frac{P_N \cdot \left(1 + \frac{\delta_{iL}}{2}\right) \cdot (1 + k_{olf})}{V_{LL,N} \cdot \cos(\phi)} \tag{6.43}$$

Then, from equation 3.26, the minimum number of parallel connected devices needed to ensure that the current rating of the devices is not exceeded can be calculated by equation 6.44 (where the function $\lceil x \rceil$ means that the smallest integer is not less than x). Since the switch is implemented by the IGBT with anti-parallel diode modules, and the IGBT and diode have different current imbalance rates (for example modules in Table 3.2), then $n_{p,min}$ should be chosen as the maximum value according to the equation 6.44 for the parameters of the IGBT and diode.

$$n_{p,min} = \left\lceil \left(\frac{I_{psw}}{1.6 \cdot I_n} - 1 \right) \cdot \left(\frac{1 + \delta_{CI}}{1 - \delta_{CI}} \right) + 1 \right\rceil \tag{6.44}$$

Figure 6.6 shows the minimum number of parallel connected modules as a function of the line-to-line voltage and the nominal power of the 2L-VSC with SVPWM modulation for the three power modules in Table 3.2. A displacement factor of $cos(\varphi) = 0.85$ and a nominal modulation index of $M_{s,nom} = 0.98$ are considered in Figure 6.6.

Equation 6.44 gives the minimum value of n_p to ensure that the current rating of

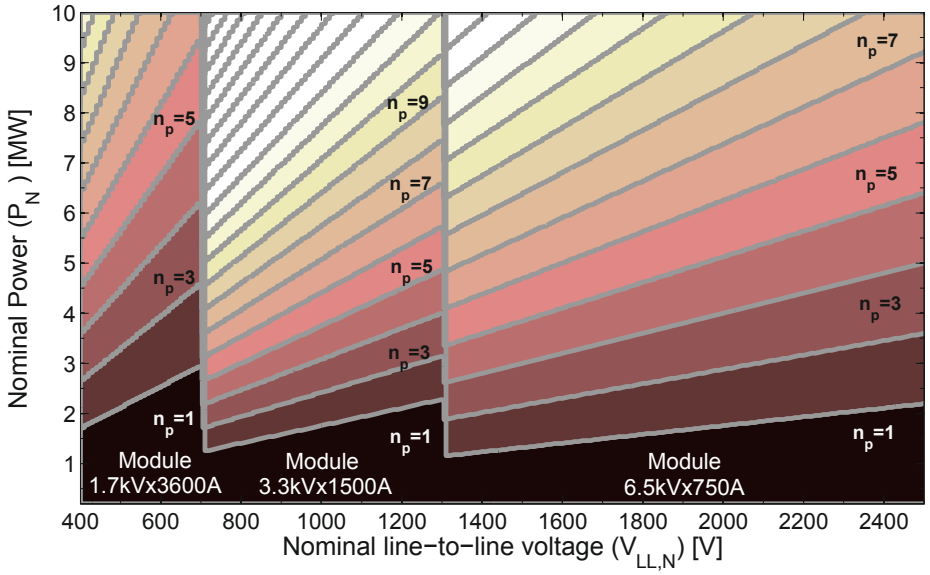


Figure 6.6: Minimum number of parallel connected devices as a function of the nominal power (P_N) and the nominal line-to-line voltage ($V_{LL,N}$) of the 2L-VSC with SVPWM modulation for three semiconductor power modules. A displacement factor $cos(\varphi)$ of 0.85 and a nominal modulation index of 0.98 are considered

the modules connected in parallel with maximum current imbalance (δ_{CI}) is not exceeded. However, if the converter is designed to operate with a relatively high switching frequency, it may be necessary to increase n_p such that the maximum power that the module can dissipate via the heat sink mounting without overheating itself is not surpassed (restriction from equation 3.38).

Figure 6.7 shows the maximum allowable heat sink temperature increases (calculated from equation 3.34) as a function of the switching frequency for a 2 *MW* 2L-VSC with SVPWM modulation and three designs with different nominal line-to-line voltage for each semiconductor power module from Table 3.2 (considering one module per switch from Figure 6.6). The converter operated as an inverter is shown in Figure 6.7a, and rectifier operation mode is presented in Figure 6.7b.

From Figure 6.7, it can be noted that when the minimum number of parallel devices from equation 6.44 is considered, there is a limit to the switching frequency ($f_{sw,limit}$) which the converter can operate without exceeding the maximum power that the module can dissipate in the heat sink mounting with minimum thermal resistance ($R_{thHS,min} = 10\,K/kW$ in Figure 6.7). Beyond the limit switching frequency, the heat sink thermal resistance required to stay within the maximum

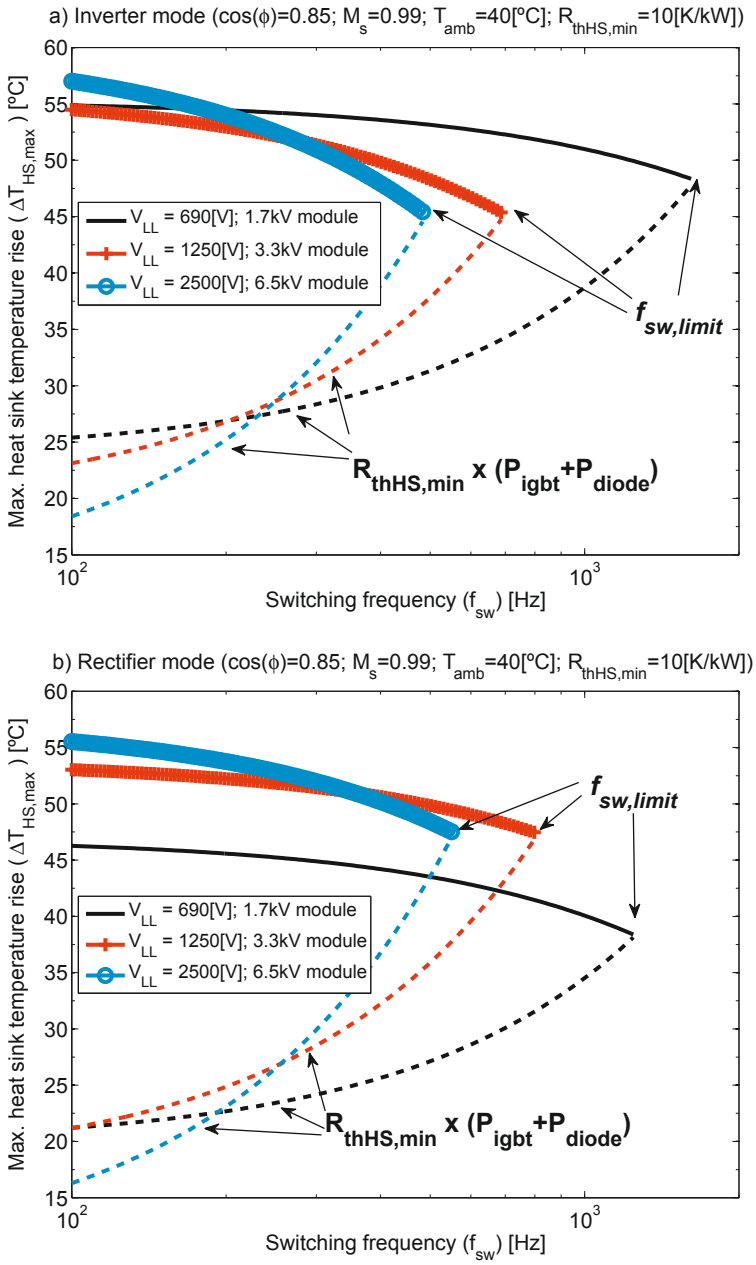


Figure 6.7: Maximum allowable heat sink temperature increases as function of the switching frequency for a 2 MW 2L-VSC with SVPWM modulation and three designs with different nominal line-to-line voltage for each semiconductor power module from Table 3.2 (one module per switch is considered); a) Inverter mode of operation; b) Rectifier mode of operation.

junction temperature in the worst conditions is lower than the $R_{thHS,min}$ given by heat sink technology (restriction from equation 3.38).

By comparing Figure 6.7a with Figure 6.7b, we can see how the converter operation mode affects the thermal design of the converter, which is influenced mainly by the semiconductor parameters (IGBT and diode). Furthermore, since power modules with higher blocking voltages have stronger frequency dependency (they require thicker silicon, which gives higher switching losses [29]), the switching frequency limit is lower for high blocking voltage modules than for low blocking voltage modules, as seen in Figure 6.7.

If the converter is designed to operate with a higher f_{sw} than $f_{sw,limit}$, the number of parallel connected devices should be higher than the minimum value from equation 6.44. Figure 6.8 shows the limit switching frequency as a function of the number of modules connected in parallel for a 2 *MW* 2L-VSC with the same design used in Figure 6.7. From Figure 6.8, it can be noted that the $f_{sw,limit}$ vs. n_p curve shows asymptotic behaviour, and the switching frequency asymptote decreases as the required blocking voltage is increased. Hence, this characteristic will reduce the use of high blocking voltage devices for designs with high switching frequencies.

Figure 6.8a shows how the converter operation mode influences the limit switching frequency. For 1.7 *kV* modules, the inverter mode allows a higher limit switching frequency than the rectifier mode, but this difference decreases as n_p increases. However, for 3.3 *kV* and 6.5 *kV* modules, the influence of the operation mode is less predictable, and the rectifier mode allows a higher limit switching frequency than the inverter mode.

Additionally, Figure 6.8b shows how the modulation technique influences the limit switching frequency. In all the cases, SFTM allows higher limit switching frequencies for the design parameters and constraints considered. Also from Figure 6.8b, it can be noted that the influence of the modulation technique is less notorious for devices with higher blocking voltage.

Finally, a constraint related to the maximum switching frequency should be taken into account to limit the use of power modules to the range of switching frequencies that the module can manage without destruction and to ensure that the relative time that the module takes to change state (turn-on and turn-off times) does not surpass a practical limit (for example 2%). Table 3.2 shows the maximum switching frequency for each module, which is calculated to ensure that the conduction time per switching period is higher than 98% of the switching period.

Figure 6.9 shows an example of a power loss evaluation per module as a function

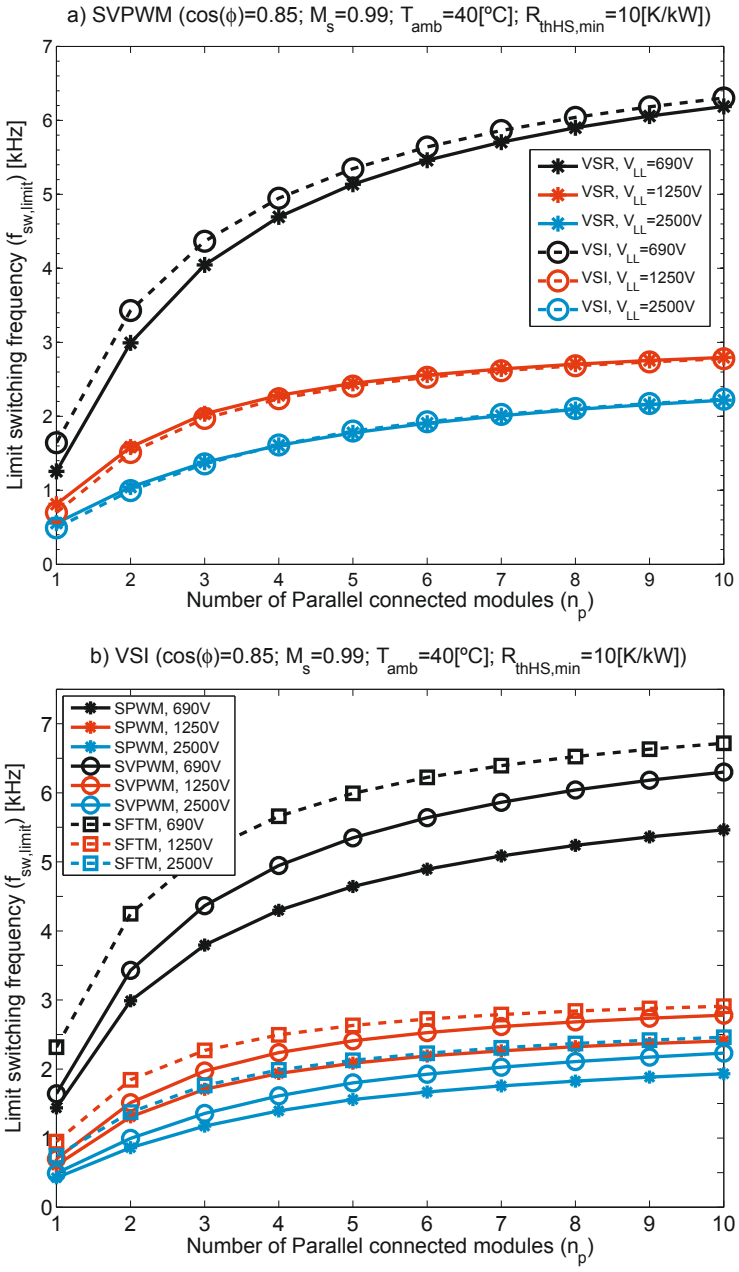


Figure 6.8: Limit switching frequency as a function of the number of parallel connected semiconductor modules for a 2 MW 2L-VSC with different nominal line-to-line voltage; a) Comparison of converter operation mode (rectifier and inverter) with SVPWM; b) Comparison of modulation technique for inverter mode.

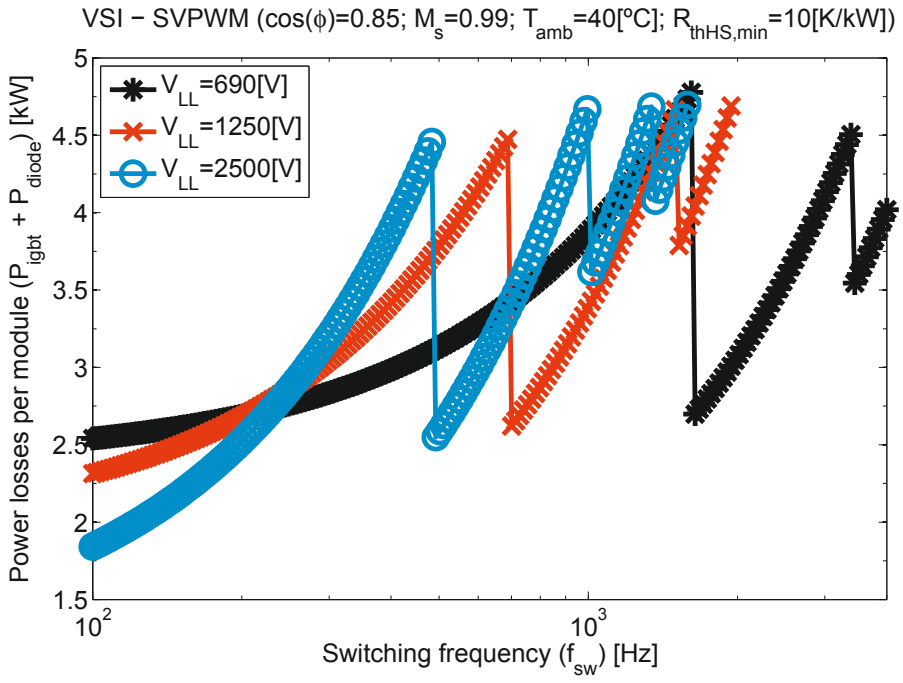


Figure 6.9: Example of power losses per module as a function of the switching frequency for a 2 *MW* 2L-VSC operated as an inverter and with SVPWM. Design with three different nominal line-to-line voltages are considered, each with different power modules and a different number of modules connected in parallel to fulfil heat sink thermal constraints.

of the switching frequency for a 2 *MW* 2L-VSC operated as an inverter and with SVPWM and the same design used in Figure 6.7. In addition, Figure 6.10 shows an example of a power loss evaluation per valve and the number of modules connected in parallel as a function of the switching frequency for the same converter design shown in Figure 6.9. The maximum switching frequencies considered for the 1.7 *kV*, 3.3 *kV* and 6.5 *kV* modules are 4 *kHz*, 2 *kHz* and 1.5 *kHz*, respectively.

6.4 Evaluation of the power losses, volume and mass of the 2L-VSC

For a given set of design parameters, constraints and variables, the total losses of the 2L-VSC are calculated by equation 6.45, via the summation of switch valves losses (P_{valve}), AC filter inductor losses (P_{LF}) and DC-link capacitor losses (P_{CDC}):

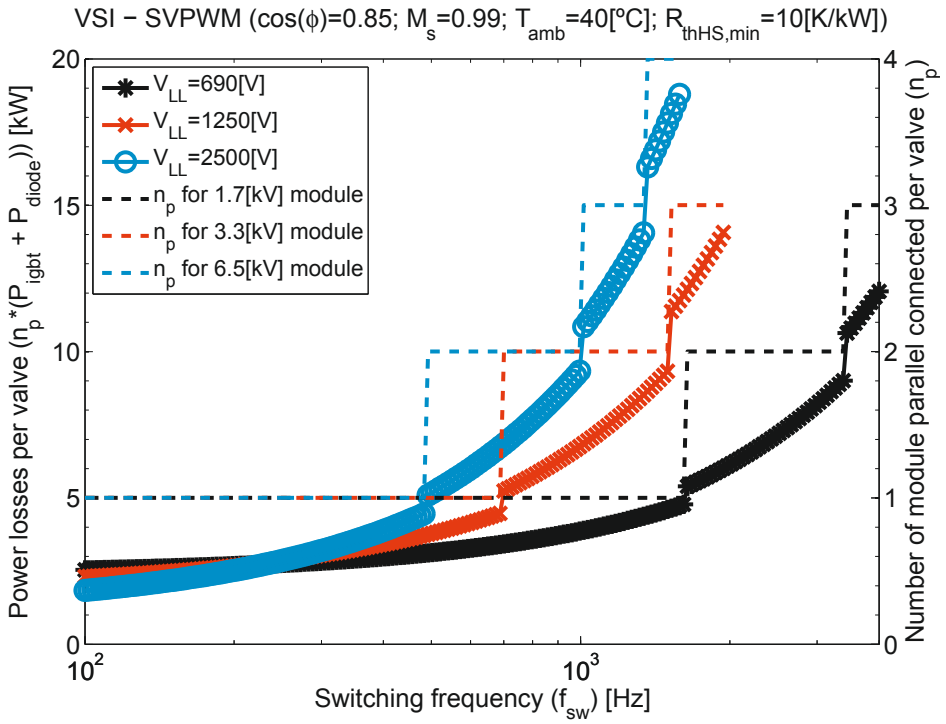


Figure 6.10: Example of power losses per valve and the number of modules connected in parallel as a function of the switching frequency for a 2 *MW* 2L-VSC operated as an inverter and with SVPWM.

$$P_{losses,VSC} = 6 \cdot P_{valve} + P_{LF} + P_{CDC} \tag{6.45}$$

$$P_{valve} = n_p \cdot (P_{igbt} + P_{diode}) \tag{6.46}$$

$$P_{LF} = P_{wLF} + P_{cLF} \tag{6.47}$$

$$P_{CDC} = P_{\varepsilon C} + P_{\Omega C} \tag{6.48}$$

In this case, the converter has six switch valves, each implemented by n_p modules (IGBT with an anti-parallel diode) connected in parallel with the IGBT, and diode power losses defined in chapter 3 by equations 3.36, and 3.37 at nominal current. The losses of the AC filter inductor are composed of winding and core losses which can be calculated by equations 4.20 and 4.32, respectively. The losses of the DC-link capacitor are calculated by adding the dielectric losses and the resistive losses, defined by equations 4.44 and 4.46, respectively.

The total VSC volume (Vol_{VSC}) is calculated by equation 6.49, via the summation of the individual volumes of switch valves (Vol_{valve} from equation 3.31), the three-phase inductor (Vol_{LF} from equation 4.5) and the DC-link capacitor (Vol_{CDC} from equation 4.41). A volume utilization factor C_{PV} of 0.6 is considered for the 2L-VSC. Similarly, the total VSC active mass ($Mass_{VSC}$) is obtained by equation 6.50, with valve mass ($Mass_{valve}$) calculated by equation 3.40, the inductor mass ($Mass_{LF}$) by equation 4.6 and the DC-link capacitor mass ($Mass_{CDC}$) by equation 4.42.

$$Vol_{VSC} = \frac{1}{C_{PV}} \cdot (6 \cdot Vol_{valve} + Vol_{LF} + Vol_{CDC}) \tag{6.49}$$

$$Mass_{VSC} = 6 \cdot Mass_{Valve} + Mass_{LF} + Mass_{CDC} \tag{6.50}$$

Once the total power losses, the total volume and total active mass are evaluated, then the η, ρ and γ can be calculated by equation 2.7, 2.8 and 2.9, respectively.

6.5 Design example and Pareto-Front

The design of a 1 *MW* 2L-VSC is considered as an example to illustrate how the proposed methodology should be applied. The system parameters, design constraints and references models used in the example are indicated in Table 6.1 and

Table 6.1: System parameters for the design example 1 *MW* 2L-VSC.

Parameter	Symbol	Value
Nominal Power	P_N	1 [MW]
Nominal line-to-line RMS voltage	$V_{LL,N}$	690 [V]
Power factor	$cos(\phi)$	0.85
Fundamental frequency	f_1	50 [Hz]
Equivalent machine inductance per phase	L_M	50 [μH]
Overload factor	k_{olf}	0.3
Volume utilization factor	C_{PV}	0.6
Relative input DC-link current ripple	δ_{Iin}	0.3
Nominal modulation index	$M_{S,nom}$	0.99
Ambient temperature	T_{amb}	40 [C]

Table 6.2. The three modulation strategies presented in section 6.1 are compared for each operation mode of the 2L-VSC (Rectifier and Inverter). Furthermore, to simplify the selection of the devices, only the IGBT modules presented in Table 3.2 with ratings: *1.7kV/3600A*, *3.3kV/1500A* and *6.5kV/750A* are considered.

Although previous studies [47, 46, 30, 33, 50, 32] show that SPWM modulation is less efficient than SVPWM and SFTM modulation, SPWM modulation is first considered here to show how the choice of modulation strategy influences the performance indices considered in this thesis. The modulation strategies will be compared later.

6.5.1 Pareto-Front of the 1 *MW* 2L-VSC with SPWM modulation

First, the impact of the switching frequency and the relative AC current ripple (δ_{iL}) on the total volume, the nominal power losses and total active mass are analysed for the 2L-VSC operated as a rectifier (interfacing a generator). A switching frequency variation from 500[Hz] to 4 *kHz* (or the maximum switching frequency that the IGBT module can be switched) is considered, but configurations which do not correspond to the thermal and frequency requirements of the IGBT modules are not shown.

Figure 6.11 shows the nominal power losses, the total volume and the total active mass as a function of the switching frequency of the converter with SPWM modulation that is considered to be operated mainly as a rectifier. SPWM with a nominal line-to-line voltage of 690 *V* is considered therefore, the *3.3kV/1500A* IGBT module should be used (as shown by Figure 6.4a) and the switching frequency is lim-

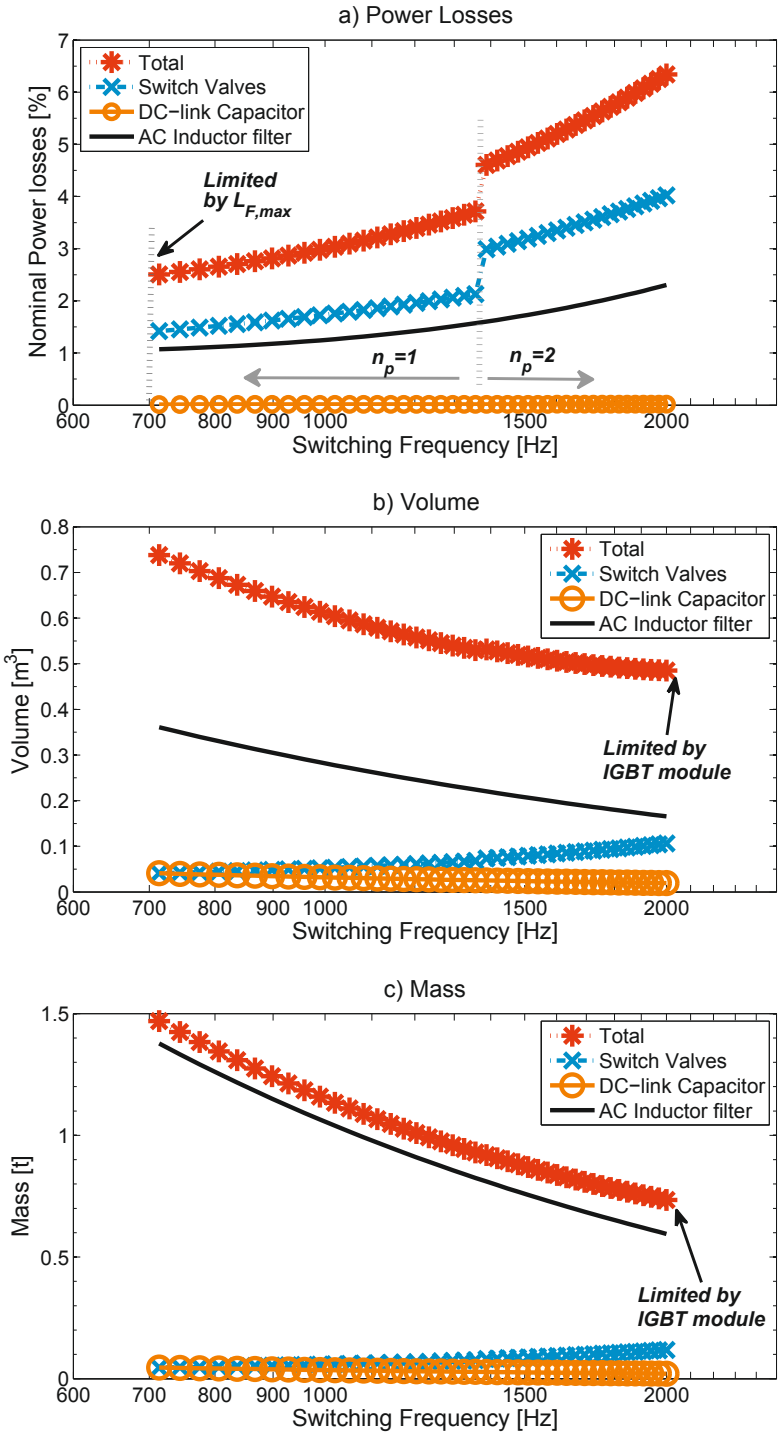


Figure 6.11: Design example of a 1MW-690V 2L-VSC showing the evaluation of power losses, volume and mass as a function of the switching frequency for SPWM modulation in rectifier operation mode; a) Power Losses; b) Volume; c) Mass.

Table 6.2: Design constraints and references models for the design example 1 *MW* 2L-VSC

Constraint	Symbol	Value
Safety factor for DC voltage	k_{vdc}	0.65
Safety factor for peak voltage	k_{vp}	0.8
Safety factor of thermal design	K_{SFT}	0.85
Max. relative inductor voltage	$\delta_{VL,max}$	0.3
Max. relative heat sink volume	$\delta_{HS,max}$	6
Max. relative AC-current ripple	$\delta_{iL,max}$	0.2
Max. Relative DC-link ripple	$\delta_{Vdc,max}$	0.02
Heat sink model	DAU series BF-XX with axial fan SEMIKRON series SKF-3XX at 10 *m/s*	
Inductor model	Siemens series 4EUXX – Cu.	
Capacitor model	TDK series MKP-B256xx	

ited to 2 *kHz*. In addition, the minimum switching frequency is limited to around 700 *Hz* because of the maximum relative inductor voltage constraint (which requires the maximum inductance value [$L_{F,max}$] for the given relative AC-current ripple of 20%).

Figure 6.11a shows how the different components contribute to the total nominal losses. Figure 6.11a shows that the contribution of the capacitor losses is much lower than that of the inductor and switch valves losses. Furthermore, it can be noted that increasing the switching frequency beyond around 1.36 *kHz* will require the connection of two modules in parallel per valve, which abruptly increases the valve losses.

Figure 6.11b and Figure 6.11c show the total volume and active mass, respectively, and the contribution of each component. It can be observed from these figures that the inductor contributes most to the total mass and volume in the 2L-VSC with the characteristics indicated in Table 6.1. In addition, the required inductance and capacitance value decreases as the switching frequency increases; therefore, the inductor/capacitor volume and mass are low at high switching frequencies.

The evaluation of the nominal η, the ρ and the γ as a function of the switching frequency is shown in Figure 6.12. It can be noted from Figure 6.12 that maximisation of the η and the ρ (or γ) are two conflicting objectives. The maximum η of 97.5% is obtained for a converter design with a switching frequency of 700 *Hz*, but the same switching frequency provides the minimum values ofρ and γ.

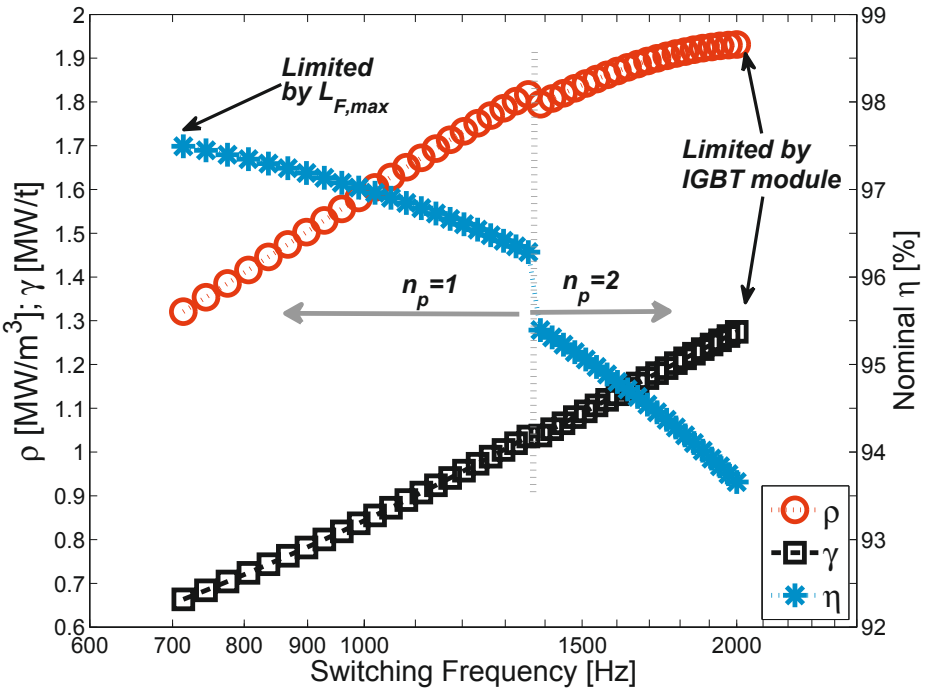


Figure 6.12: Design example of a 1MW-690V 2L-VSC; evaluation of the nominal η (left axis), the ρ and γ (right axis) as a function of the switching frequency for SPWM modulation in rectifier operation mode.

By contrast, Figure 6.12, shows that the maximum values of ρ and γ ($1.93\,MW/m^3$ and $1.28\,MW/t$, respectively) are obtained when the maximum switching frequency (2 *kHz*) is considered; however, a considerable reduction in the nominal η (from 97.5% to 93.7%) is necessary if the converter is switched at 2 *kHz*.

The influence of the maximum relative AC current ripple ($\delta_{iL,max}$) on the nominal power losses, the total volume and total active mass is illustrated in Figure 6.13, in which a switching frequency of 1.25 *kHz* is kept constant in the converter. It can be noted from Figure 6.13, that variation in $\delta_{iL,max}$ only influences the design of the AC inductor filter. The inductor mass and volume decrease because the converter design allows a higher δ_{iL}, but the inductor losses increases.

Figure 6.14 shows the evaluation of the nominal η, ρ and γ as a function of the $\delta_{iL,max}$ for a f_{sw} of 1.25 *kHz*. Similar to switching frequency variation (Figure 6.12), it can be noted from Figure 6.14 that the maximisation of the η and the ρ (or γ) are two conflicting objectives from the point of view of the $\delta_{iL,max}$ restriction. A 10% reduction of the $\delta_{iL,max}$ restriction (from 20% to 30%) results in a 0.75% reduction of η and 23% and 33% increase of the ρ and γ of the converter, respectively.

Finally, the optimised design of the 1*MW*-690*V* 2L-VSC with SPWM operated as a rectifier, taking into account different switching frequencies and relative AC current ripples, is plotted in Figure 6.15. The designs shown in Figure 6.12 ($d_{iL} = 0.2$) and Figure 6.14 ($f_{sw} = 1.25\,kHz$) are also included in Figure 6.15. The relationship between η and ρ for the space of solution is presented in Figure 6.15a, which also shows the $\eta - \rho$ Pareto-Front for the rectifier mode 2L-VSC (black curve). The $\rho - \gamma$ Pareto-Front and the ρ and γ relationship for the space of solution are presented in Figure 6.15b.

It is possible to observe from 6.15a, that variations of δ_{iL} have a strong impact on ρ, but only a small influence on the nominal η, when the f_{sw} is kept constant. Furthermore, it can be noted from Figure 6.15a, that the n_p needed to fulfil thermal the constraints significantly affects the $\eta - \rho$ space of solutions, which is clearly divided according to n_p with the highest efficiency for the solutions with one module connected in parallel. Additionally, if two IGBT modules are connected in parallel, an increase in the f_{sw} has a small impact on the ρ but a high influence on the nominal η.

By contrast, an increase in f_{sw} or $\delta_{iL,max}$ will improve the ρ and γ of the converter, as observed in Figure 6.15b, but it decreases the nominal η of the solution, as shown in Figure 6.15a. Furthermore, variation in the f_{sw} has more impact on the γ than the ρ of the converter, as seen in Figure 6.15b. The $\rho - \gamma$ Pareto-Front

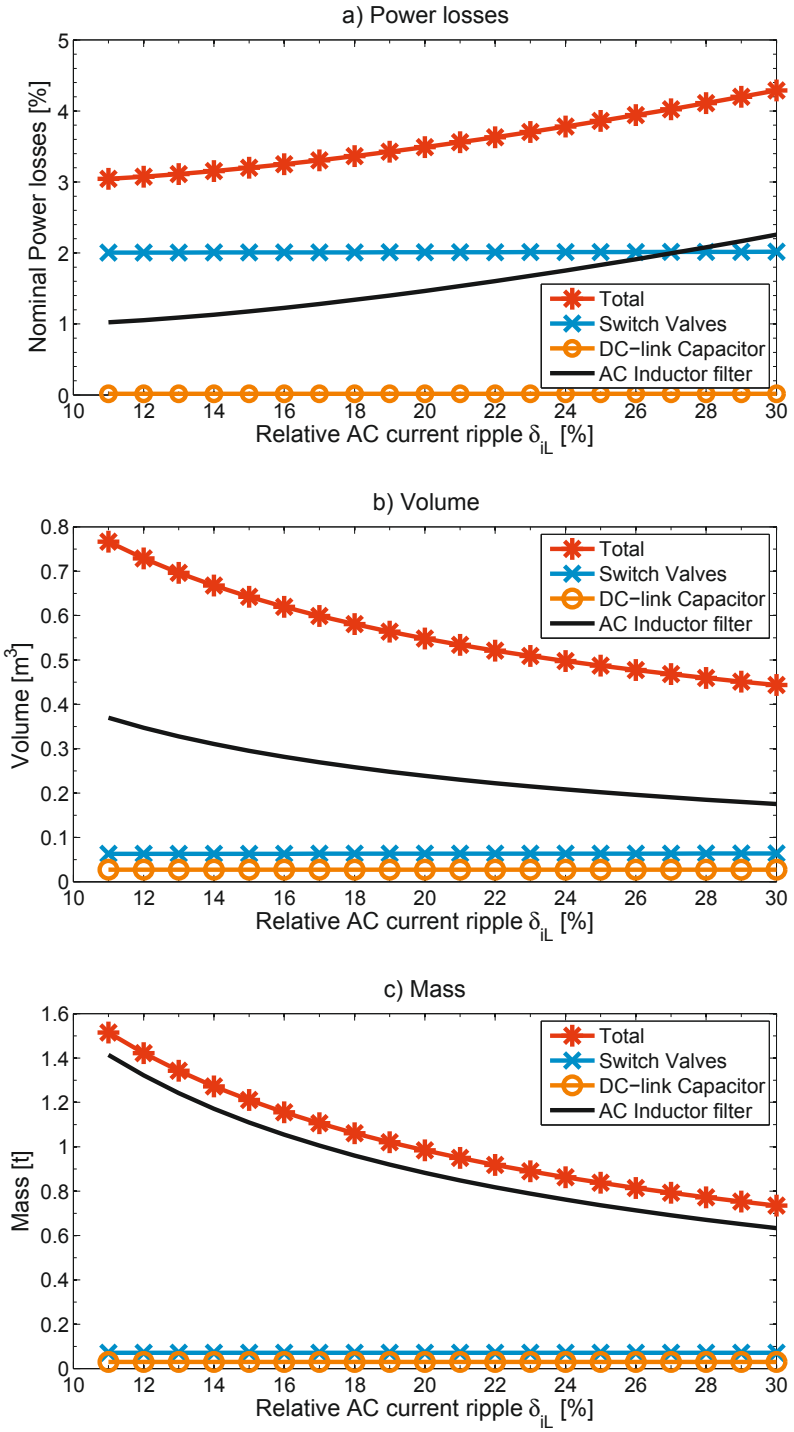


Figure 6.13: Design example of a 1MW-690V 2L-VSC with a switching frequency of 1.25[kHz], evaluation of power losses, volume and mass as a function of the relative AC current ripple for SPWM modulation in rectifier operation mode; a) Power Losses; b) Volume; c) Mass.

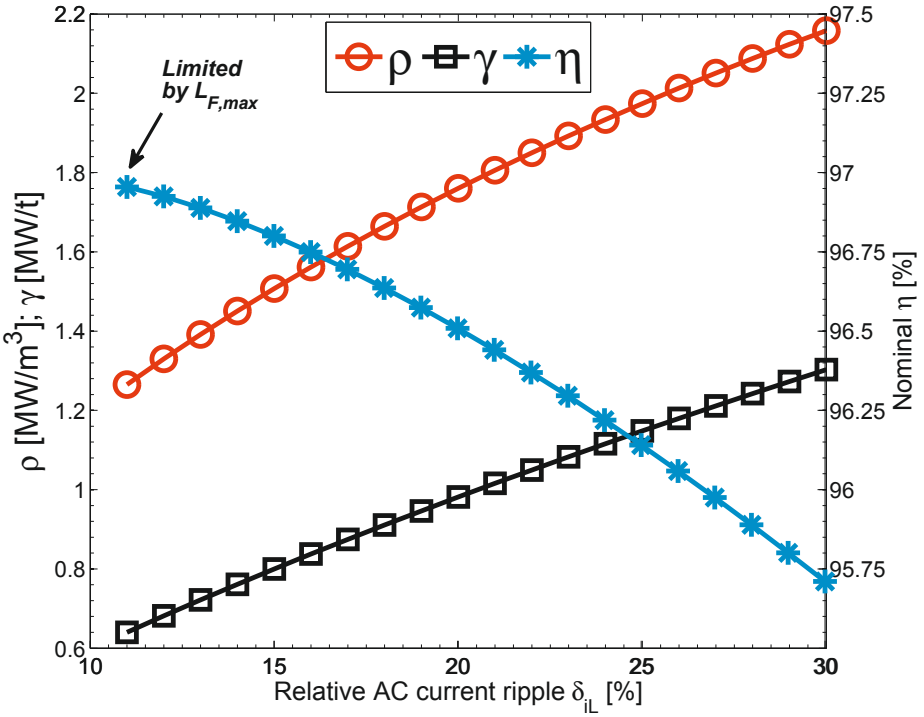


Figure 6.14: Design example of a 1MW-690V 2L-VSC with a switching frequency of 1.25[kHz]; evaluation of the nominal η (left axis), the ρ and γ (right axis) as a function of the maximum relative AC current ripple for SPWM modulation in rectifier operation mode.

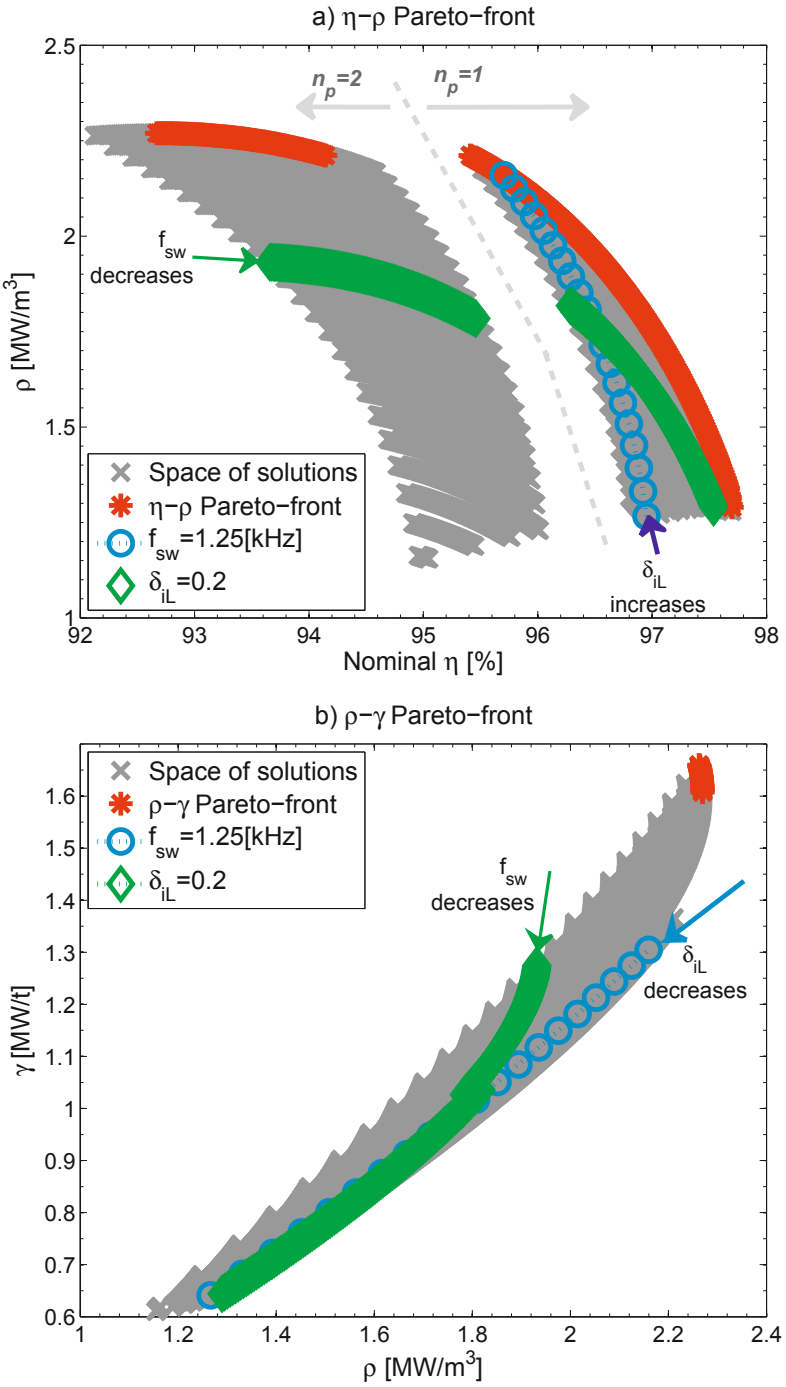


Figure 6.15: Pareto-Front for the design example of a 1MW-690V 2L-VSC rectifier in operation mode with SPWM modulation; a) η versus ρ; b) ρ versus γ

(in Figure 6.15b) of the solutions is shorter than the $\eta - \rho$ Pareto-Front (in Figure 6.15a), which shows that ρ and γ are highly correlated.

6.5.2 Comparison of modulation techniques

The three modulation strategies are compared in section 6.1 based on the three performance indices (η, ρ, γ) considered in this thesis. The system parameters, design constraints and reference models used in the comparison are indicated in Table 6.1 and Table 6.2.

Figure 6.16 and Figure 6.17 show a comparison of the three modulation strategies (SPWM, SVPWM and SFTM) in terms of the η (top), the ρ (middle) and the γ (bottom) as a function of the f_{sw} for the Voltage Source Rectifier (VSR) and Voltage Source Inverter (VSI) operation mode, respectively. From Figure 6.16 and Figure 6.17, it can be noted that solutions based on SVPWM and SFTM modulations are better than those based on SPWM modulation for the range of f_{sw} considered. Furthermore, SVPWM and SFTM modulation enables the use of *1.7kV/3600A* IGBT modules for the $V_{LL,N}$ of 690 *V*, as shown in Figure 6.4b; therefore, frequencies higher than 2 *kHz* can be considered.

SFTM appears to be the best modulation method in terms of the three performance indices, as can be noted from Figure 6.16 and Figure 6.17, for VSR and VSI operation modes, respectively. Comparison of Figure 6.16 and Figure 6.17 shows that the VSI can achieve higher values for each performance index than the VSR. However, this conclusion is limited to the system parameters and design constraints considered (Table 6.1 and Table 6.2).

As described previously for the SPWM, an increase in f_{sw} improves the ρ and γ of the converter, but reductes the nominal η . However, from Figure 6.16 and Figure 6.17, it can be noted that there is an optimal value of f_{sw} beyond which the ρ or γ will decrease. In the case of VSR with SFTM, the maximum ρ ($3.55\,MW/m^3$) and γ ($2.62\,MW/t$) are obtained for the same f_{sw} of 3.79 *kHz*. In the case of VSI with SFTM, the maximum ρ ($3.76\,MW/m^3$) is obtained for $f_{sw} = 3.79\,kHz$, but the maximum γ ($2.77\,MW/t$) is obtained for the maximum possible f_{sw} (4 *kHz*), which indicates that IGBT technology limits the maximum γ .

Figure 6.18 shows how the modulation method influences the $\eta - \rho$ Pareto-Front of the VSR (Figure 6.18a) and VSI (Figure 6.18b). It is clear that SFTM results in the best trade-off between η and ρ, and only comparable solutions are obtained with SVPWM for small values of f_{sw}, which imply low ρ.

The $\rho - \gamma$ Pareto-Front of 2L-VSC with the three modulation strategies is shown in Figure 6.19a and Figure 6.19b for the VSR and VSI, respectively. Again, SFTM

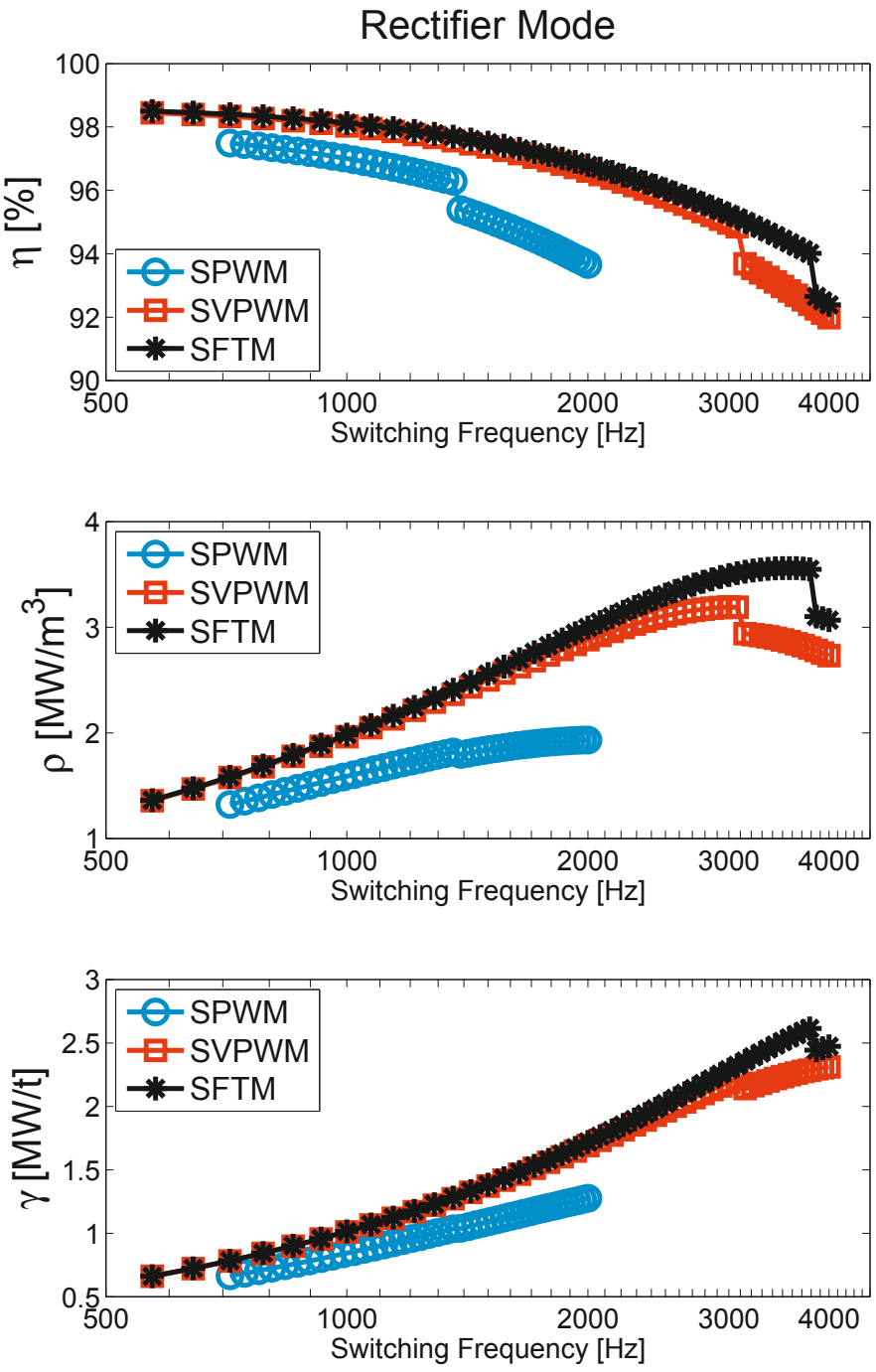


Figure 6.16: Comparison of modulation methods in the design example of the 1MW-690V 2L-VSC in rectifier operation mode. Evaluation of the nominal η (top), the ρ (middle) and the γ (bottom) as a function of the switching frequency.

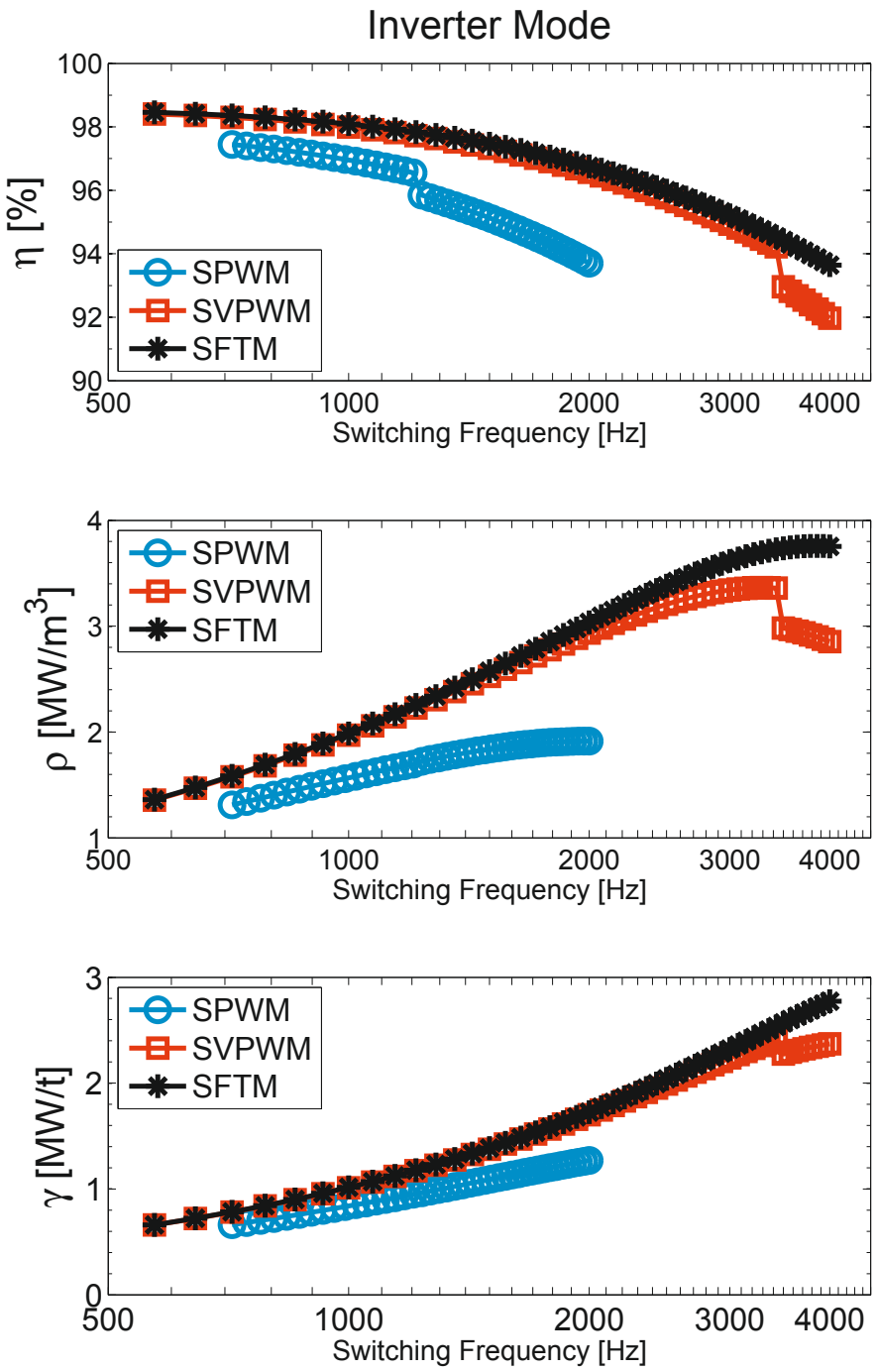


Figure 6.17: Comparison of modulation methods in the design example of the 1MW-690V 2L-VSC in inverter operation mode. Evaluation of the nominal η (top), the ρ (middle) and the γ (bottom) as a function of the switching frequency.

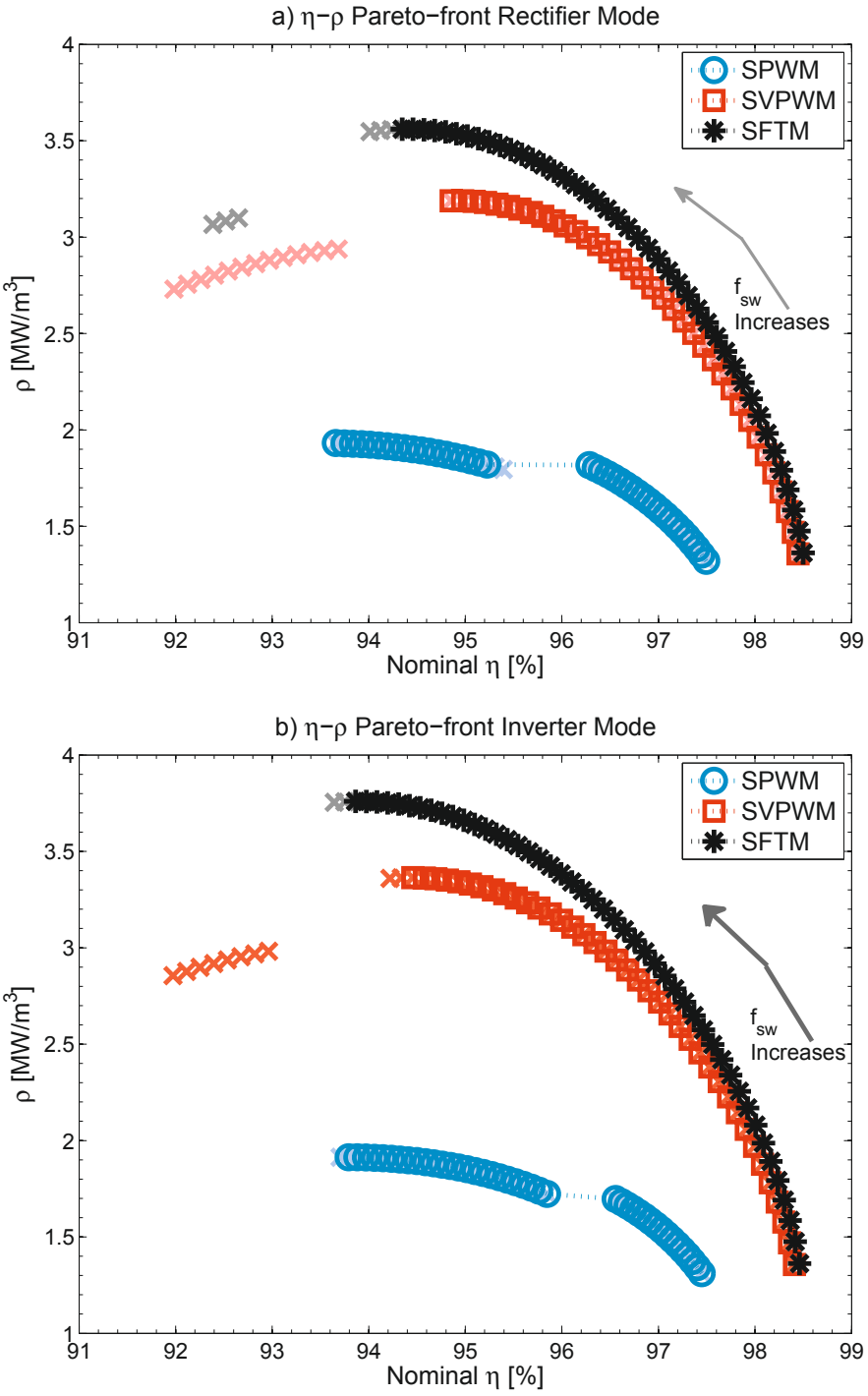


Figure 6.18: Influence of the modulation method on $\eta - \rho$ Pareto-Front for the design example of the 1MW-690V 2L-VSC; a) Rectifier operation mode; b) Inverter operation mode.

Table 6.3: Results of the optimal selection of switching frequency follows the objective function (equation 6.51) for the 1 *MW* 2L-VSC.

Modulation	Operation mode	f_{sw} kHz	η %	ρ MW/m^3	γ MW/t	Λ
SVPWM	VSR	3.107	93.68	2.938	2.141	2.927
	VSI	3.437	94.22	3.36	2.409	2.956
SFTM	VSR	3.807	94.01	3.547	2.615	2.950
	VSI	4.000	93.64	3.754	2.773	2.950

produces the best trade-off between ρ and γ, and the Pareto-Front is obtained for the solution with the highest switching frequency.

6.6 Optimal selection of the switching frequency in a 2L-VSC

From Figure 6.16 and Figure 6.17, it can be noted that the nominal η decreases with switching frequency, but there is a switching frequency that maximizes the ρ (or the γ). The optimal switching frequency can be obtained for a given set of system parameters and design constraints. The switching frequency should be selected by maximising the following objective function (Λ, 'Lambda'):

$$\Lambda = \frac{\eta}{\eta_{max}} + \frac{\rho}{\rho_{max}} + \frac{\gamma}{\gamma_{max}} \tag{6.51}$$

where η_{max}, ρ_{max} and γ_{max} are the maximum values of nominal η, ρ and γ, respectively, for a set of design parameters and constraints. Figure 6.20 shows the objective function as a function of the switching frequency for the design example of the 1 *MW* 2L-VSC with SVPWM (Figure 6.20a) and SFTM (Figure 6.20b) for each operative mode (VSR and VSI). Table 6.3 shows the performance indices when the switching frequency is selected to maximize equation 6.51.

Finally, an optimized design of a 2L-VSR is selected for the different converter nominal powers and the parameters and constraints shown in Table 6.1 and Table 6.2. It is assumed that the 2L-VSR interfaces a wind power generator with an equivalent generator inductance per phase of 1e-4 per unit, which is assumed to be the same value for all nominal powers.

Figure 6.21 shows the results of the optimized selection of the switching frequency as a function of the nominal power when the SVPWM is selected for the 2L-VSR. Figure 6.21a shows the selection of the switching frequency based on four criteria to maximize η, ρ, γ or Λ. Figure 6.21b shows the number of IGBT modules connected in parallel that are needed when the switching frequency is selected to

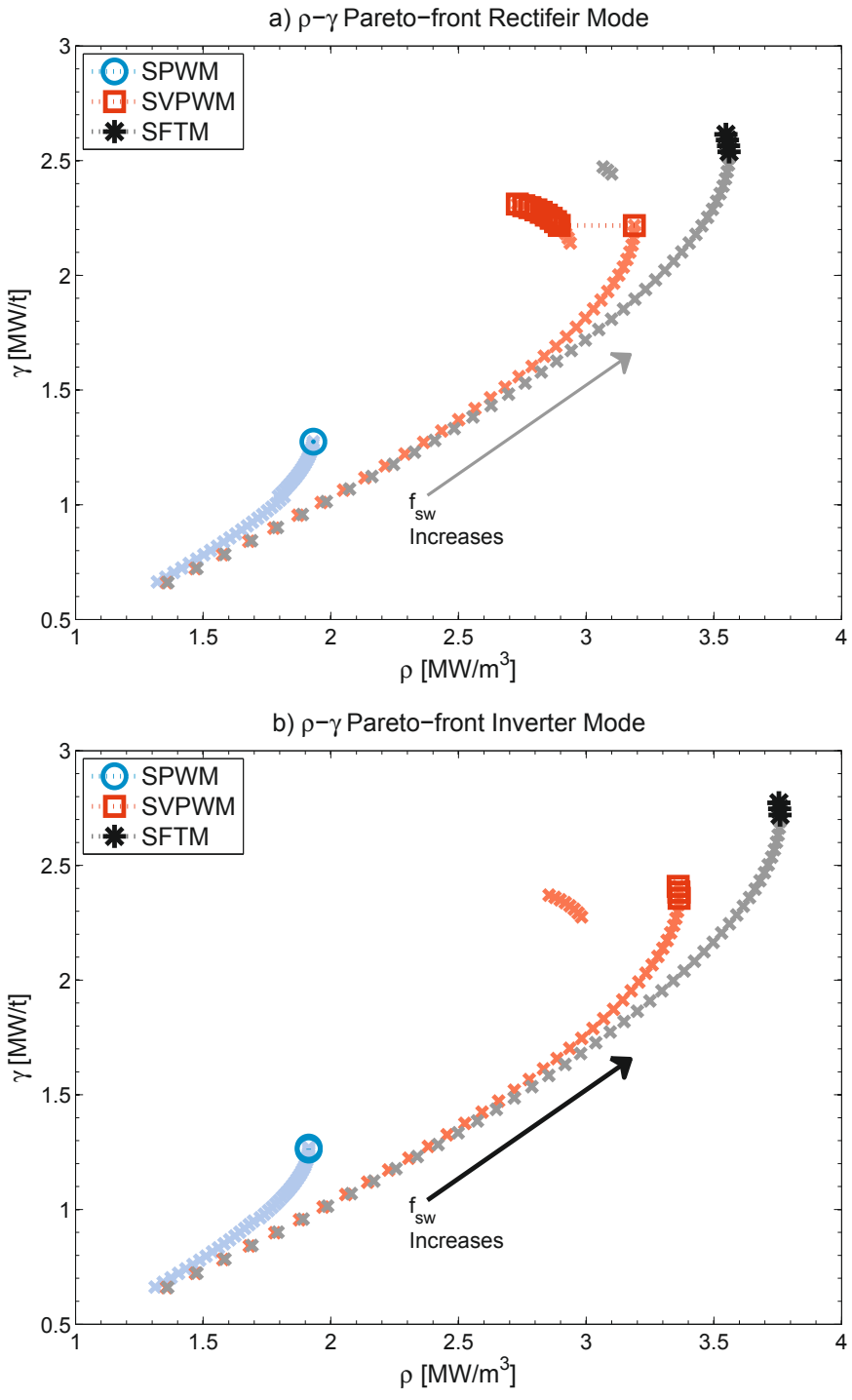


Figure 6.19: Influence of the modulation method on $\rho - \gamma$ Pareto-Front for the design example of the 1MW-690V 2L-VSC; a) Rectifier operation mode; b) Inverter operation mode.

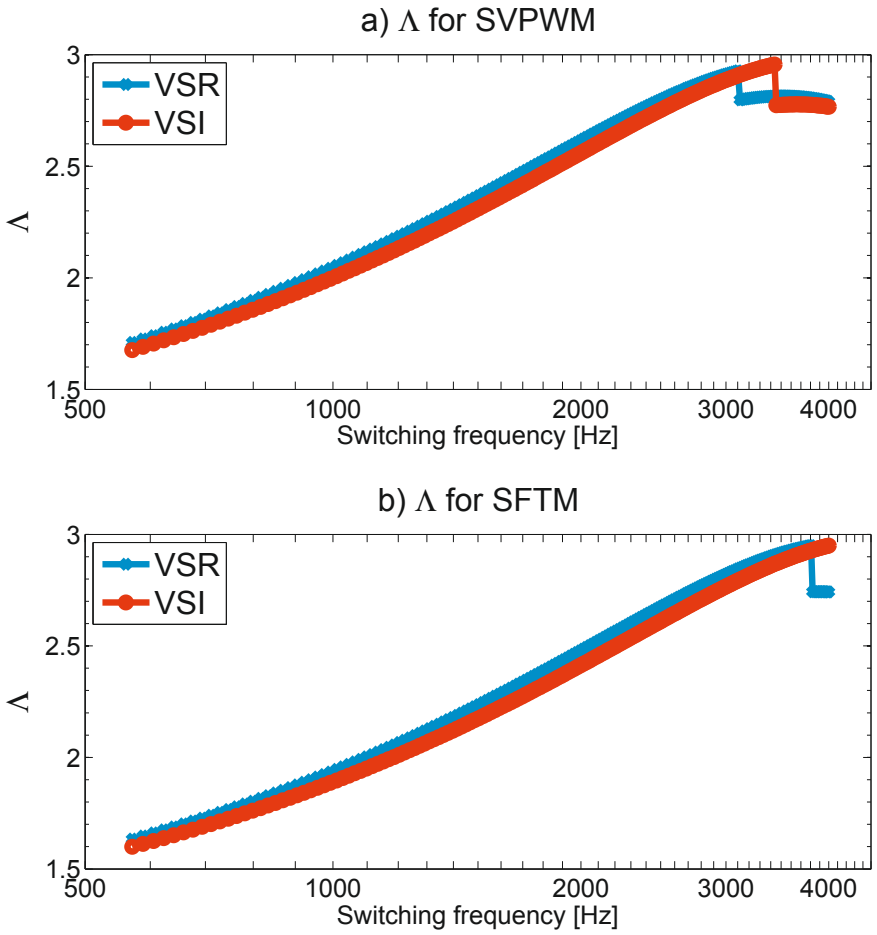


Figure 6.20: Objective function as a function of switching frequency for the design example of the 1MW-690V 2L-VSC; a) SVPWM b) SFTM

maximize Λ.

The nominal η, the ρ, and the γ as a function of the nominal power are shown in Figure 6.21c, Figure 6.21d and Figure 6.21e, respectively. Each of these figures include the maximum possible value (by selection of the corresponding f_{sw} on Figure 6.21a) and the value obtained when the switching frequency is selected to maximize Λ.

The results of the optimized selection of the switching frequency as a function of the nominal power when the SFTM is selected for the 2L-VSR are shown in Figure 6.22. SFTM produces a higher η than SVPWM for the given power factor (0.85); therefore, higher switching frequencies can be used for SFTM and higher values of ρ and γ are obtained with the same nominal η.

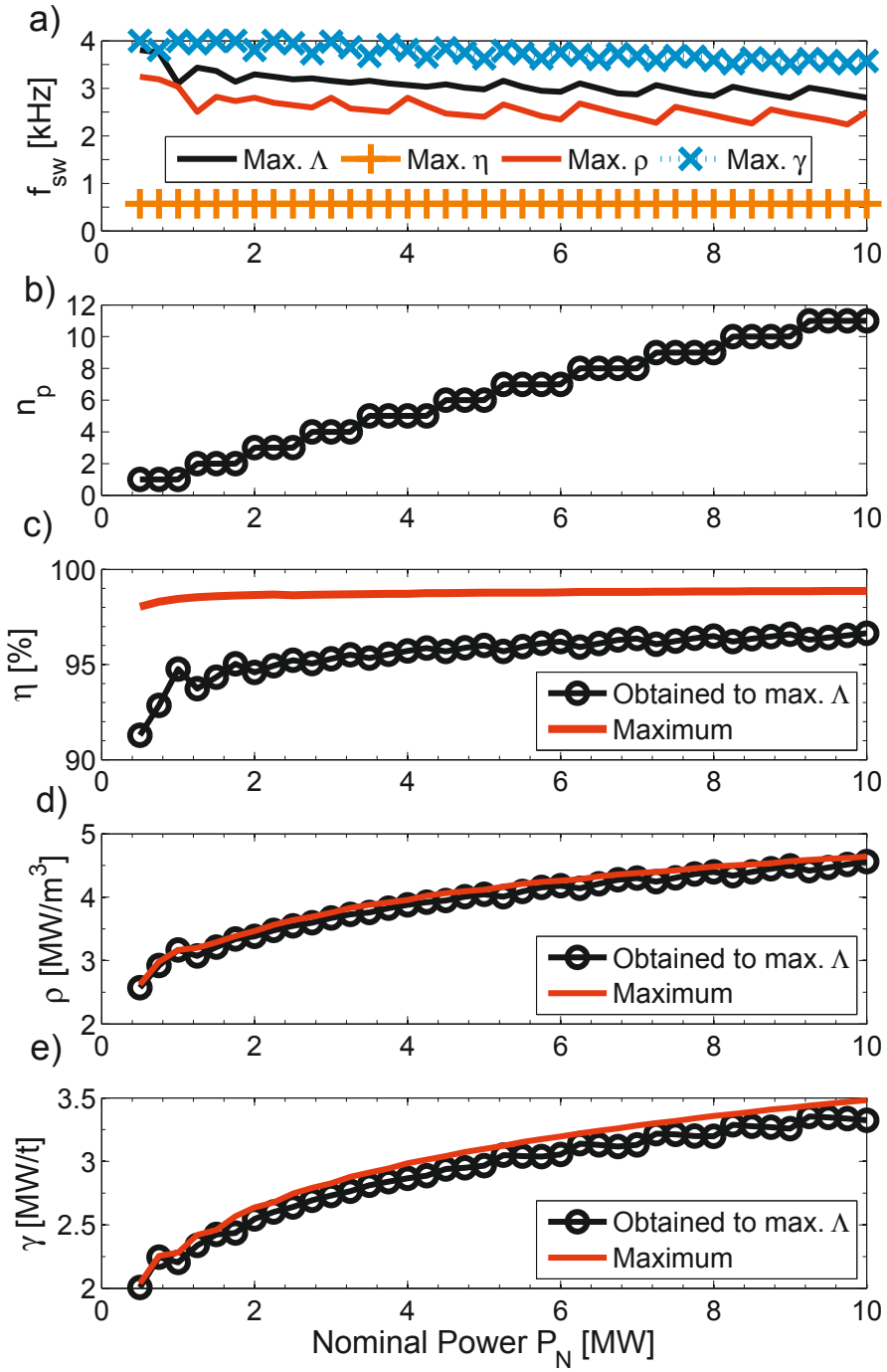


Figure 6.21: Results for the design of a 2L-VSR as a function of the nominal power when SVPWM is selected; a) Switching frequency; b) Number of IGBT modules connected in parallel; c) Nominal efficiency; d) Power density; e) Power-to-mass ratio.

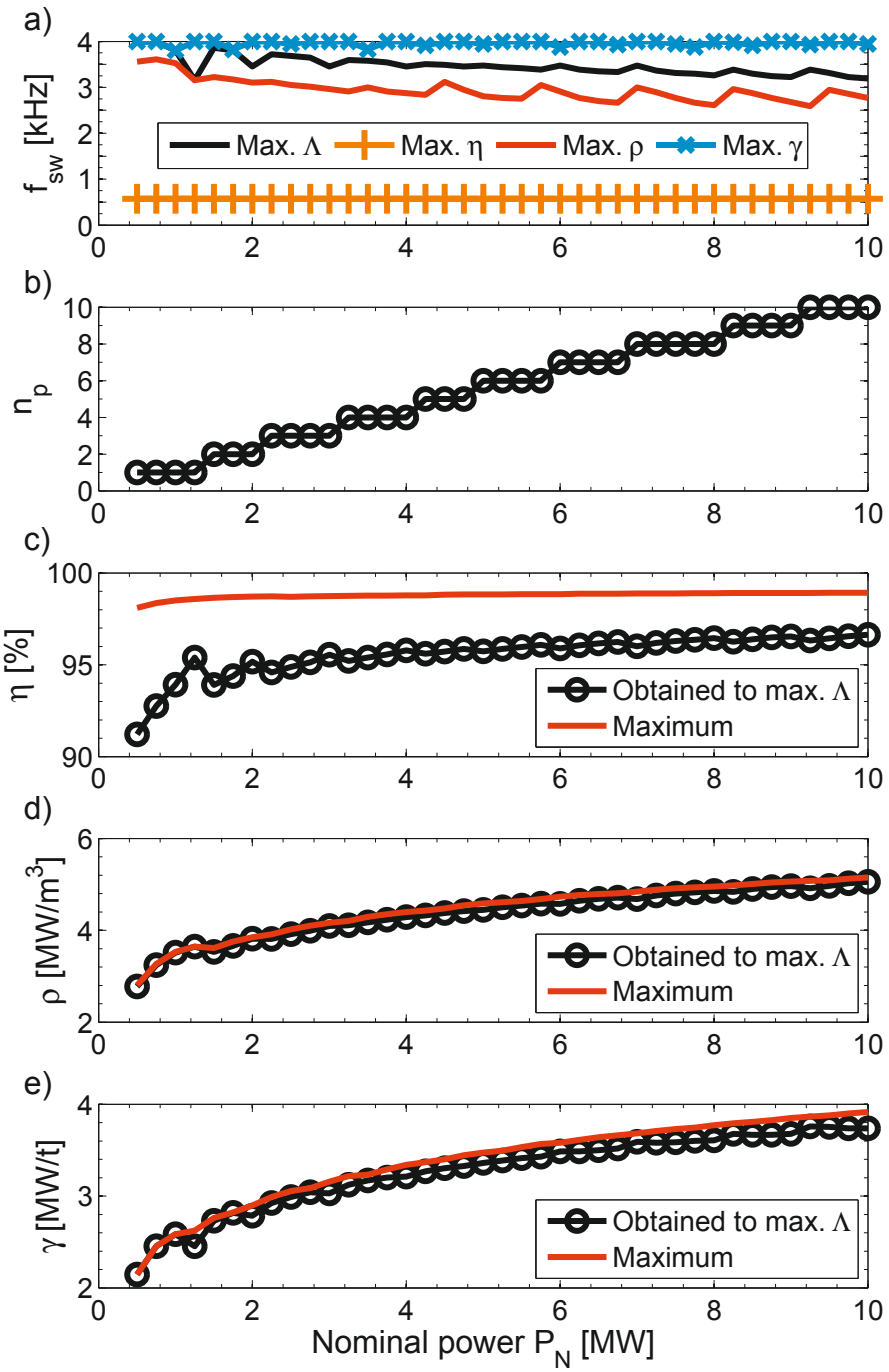


Figure 6.22: Results for the design of a 2L-VSR as a function of the nominal power when SFTM is selected; a) Switching frequency; b) Number of parallel connected IGBT modules; c) Nominal efficiency; d) Power density; e) Power-to-mass ratio.

Chapter 7

Wind Turbine Power Converters Based on Medium Frequency AC-Link for Offshore DC-Grids

7.1 Wind Turbine Power Converters for Offshore DC-Grids

Recent improvements to power electronics technology, in addition to the advantages of DC-grids over AC-grids, such as reactive power and harmonics [51], provide compelling arguments to consider the use of DC-grids in future offshore wind park layouts. Indeed, power collection systems using a DC-grid within a wind farm are a hot topic in offshore wind applications[51, 52, 6, 53, 54, 55, 56, 57, 58]. Moreover, DC WTs connected in series, as presented in [6, 59, 57, 58], are an attractive option if converter technology in the WT can maximize η and reduce investment costs. From [6], Figure 7.1 shows a DC offshore wind park layout where the WTs are connected in series. This layout is also considered in this paper. In [6], an all-DC offshore wind farm with WTs connected in series is proposed as an alternative to the classical parallel AC model. This all DC-based model reduces investment costs and power losses because the length of cable is shorter than in models connected in parallel and the expensive offshore platform is not required. [6] reported that for 10 *MW* WTs, the DC series park had approximately 10% lower losses than the AC radial park, but these results are linked to the choice of a high η converter topology in the WECS of each WT.

Two types of full-scale WECSs have been described for DC wind parks connected in series: those including a MFT [56, 55, 60, 59, 61, 6] and a WECS without transformers [5, 62, 63, 64]. In this chapter, the WECS based on a full-scale con-

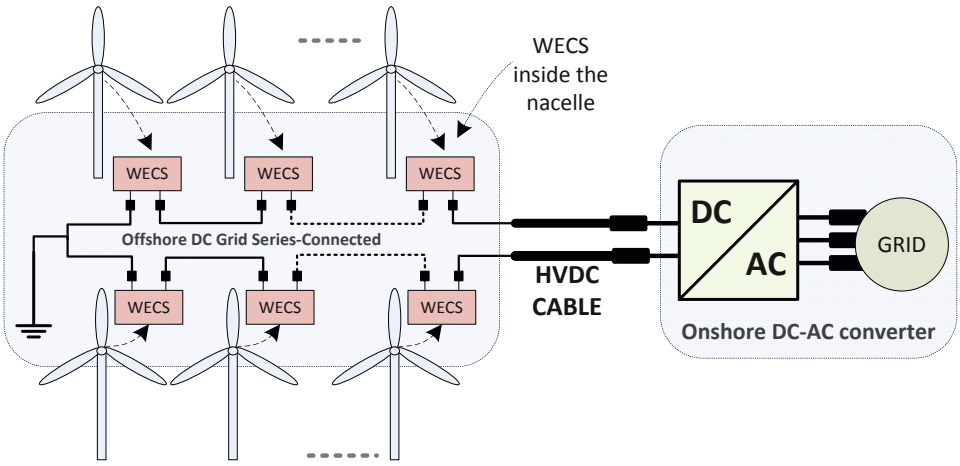


Figure 7.1: A DC Offshore wind park layout with series-connected turbines and HVDC transmission.

verter and MFT are considered. A converter based on MFT was selected to ensure that the generator voltage can be increased to the desired high output DC voltage, and to enable galvanic isolation between the generator and DC-grid. This system also limits the size and weight of the magnetic components [1], which enables the power converter to be placed inside the nacelle, thus reducing complexity and the cost of the structure and foundation of the WT [65].

Two main converter architectures have been described for a WECS based on MFT: those displaying an intermediate DC link which connects an AC/DC converter with an DC/DC converter [55, 56, 52, 53, 58, 66], and a WECS with a direct AC/AC converter between the generator and MFT without an intermediate DC link [6, 61, 59, 65, 13].These architectures are shown in Figure 7.2. Various DC/DC converters have been proposed and compared for the WECS with an intermediate DC link (see top of Figure 7.2). For example, in [56], 5 *MW* WECS including a controlled VSC connected to a DC/DC converter were studied, and the energy η of three different DC/DC converter topologies were compared: the Full-Bridge (FB) converter with phase-shift control, the Single Active Bridge (SAB) converter and the Series Parallel Resonant converter. This comparison found that the FB converter is the best choice regarding losses, contribution to the energy production cost, simplicty of design and ease of control. [66] compared the FB converter with a full bridge isolated boost converter topology and reported similar conclusions.

A WECS with a direct AC/AC converter (see bottom of Figure 7.2) based on Reduced Matrix Converter (RMC) topology was subsequently proposed in [60], and

a comparison between the RMC and a WECS including a SAB DC/DC converter is presented in [67] for a 20 *kVA* system, and in [4] for a 2 *MW* WT. The η in a RMC for offshore wind farms was studied in depth in [59], to define the most suitable modulation and operation modes for WTs connected in series or in parallel. These studies show that for series-connected WTs and Current Source Operation (CSO) of the WECS, the RMC topology is more efficient than a WECS based on SAB converter when the AC-link frequency (nominal frequency of the MFT) increases above 6 kHz for a 2 *MW* WT. However, this comparison did not include the FB converter, which was reported previously to be more efficient than SAB converter [56, 66]. Additionally, all these results depend on the WT power rating, and since there is a clear trend toward increasing the turbine rating, a 10 *MW* rating may be more suitable than a 2 *MW* rating in offshore wind parks. Furthermore, all the mentioned solutions claim that the use of MFT improves the ρ of the WECS because an increase of AC-link frequency enables the volume/weight of the MFT to be reduced; however, higher frequencies in the power electronic components will generate higher switching losses and therefore deteriorate the η of the system. Thus, higher η and ρ are two conflicting objectives from a design perspective, and should be taken into account when WECS are compared. Few studies in the literature have included these performance indicators when comparing WECS for offshore DC WTs connected in series.

Furthermore, the above-mentioned solutions are based on a single-phase MFT and some studies suggest that a three-phase MFT may reduce size/weight compared to single-phase schemes. This was the conclusion of [6], who proposed three WECS solutions including a three-phase MFT and compared them in terms of η; however, the size/weight characteristics of the solution were not presented, and moreover, these solutions were not compared with single-phase schemes. The WECS compared in [6] were: the Direct Matrix Converter (DMC), the Indirect Matrix Converter (IMC), and a WECS including an intermediate DC-link with two Back-to-Back VSCs (B2B) and a sinusoidal output waveform (referred to here as B2B3p). This study found that for 10 *MW* turbines, the DMC is more efficient than the other considered solutions if the bidirectional switches are implemented with low rating IGBTs connected in series and parallel. However, combinations of series and parallel connections for IGBTs are rare in real-world applications, where high rating IGBTs are connected in parallel at the low voltage side of the converter, and at the high voltage side, the semiconductor devices are connected in series to reach the required blocking voltage. Furthermore, the analysis was performed for a WECS with a modular architecture, in which the converter modules are connected in parallel to reach high power levels as in the 2.5 *MW* Liberty WT [68]. Finally, modules of 625-kW rating (16 modules connected in parallel to reach a total rating of 10 *MW*) were assumed with no clear justification, even though the η and ρ of a

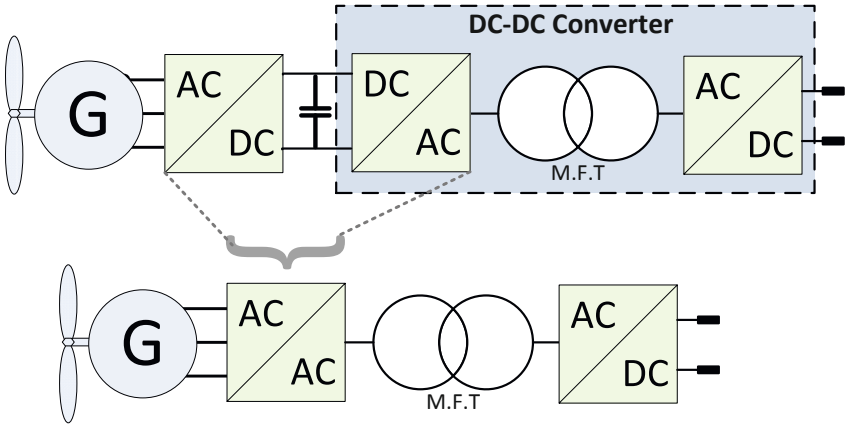


Figure 7.2: Possible configurations for the WECS based on MFT. Top: WECS with an intermediate DC link and a DC/DC converter; bottom: WECS with a direct AC/AC converter without a DC link.

modular converter depend on the number of modules selected, as shown in [33], in which an optimized design of a two and three level full-scale VSC for multi-MW WTs in an AC-grid park layout was presented.

This chapter investigates how the AC-Link frequency and the number of modules (N_m) of the power converter influences the power losses, the volume and the mass of the WECS of Figure 7.3, when a total rated power of 10 *MW* is required. In the proposed WECS, each unit consists of a turbine, a PMSG with N_m insulated stars or a split drive train feeding N_m PMSGs, and a modular power converter consisting of N_m AC/DC converter modules. The AC/DC converter module based on MFT, shown in Figure 7.3 (at bottom), is composed of three main stages: an AC/AC converter (which may or may not include an intermediate DC-link), an MFT, and a Full-Bridge Diode Rectifier (FBD) with an LC output filter to convert the medium frequency voltage waveform into a DC one. The analysis is carried out for six potential solutions based on different AC/AC converters (B2B vs. matrix topologies), AC-Link waveforms (sinusoidal vs. square) and phases of the MFT (single vs. three phase). The three WECS solutions presented in [6] are considered in this chapter: B2B3p, DMC and IMC. Additionally, the other three WECS solutions are based on: RMC, FB converter (referred to here as B2B1p), and the B2B with a three-phase Squared waveform (B2B3pSq). This chapter also presents a comprehensive comparison of the most relevant WECS based on MFT found in the literature. Analytical models as well as numerical simulations have been considered to determine the main representative variables of these topologies as a function of the AC-Link operating frequency and N_m.

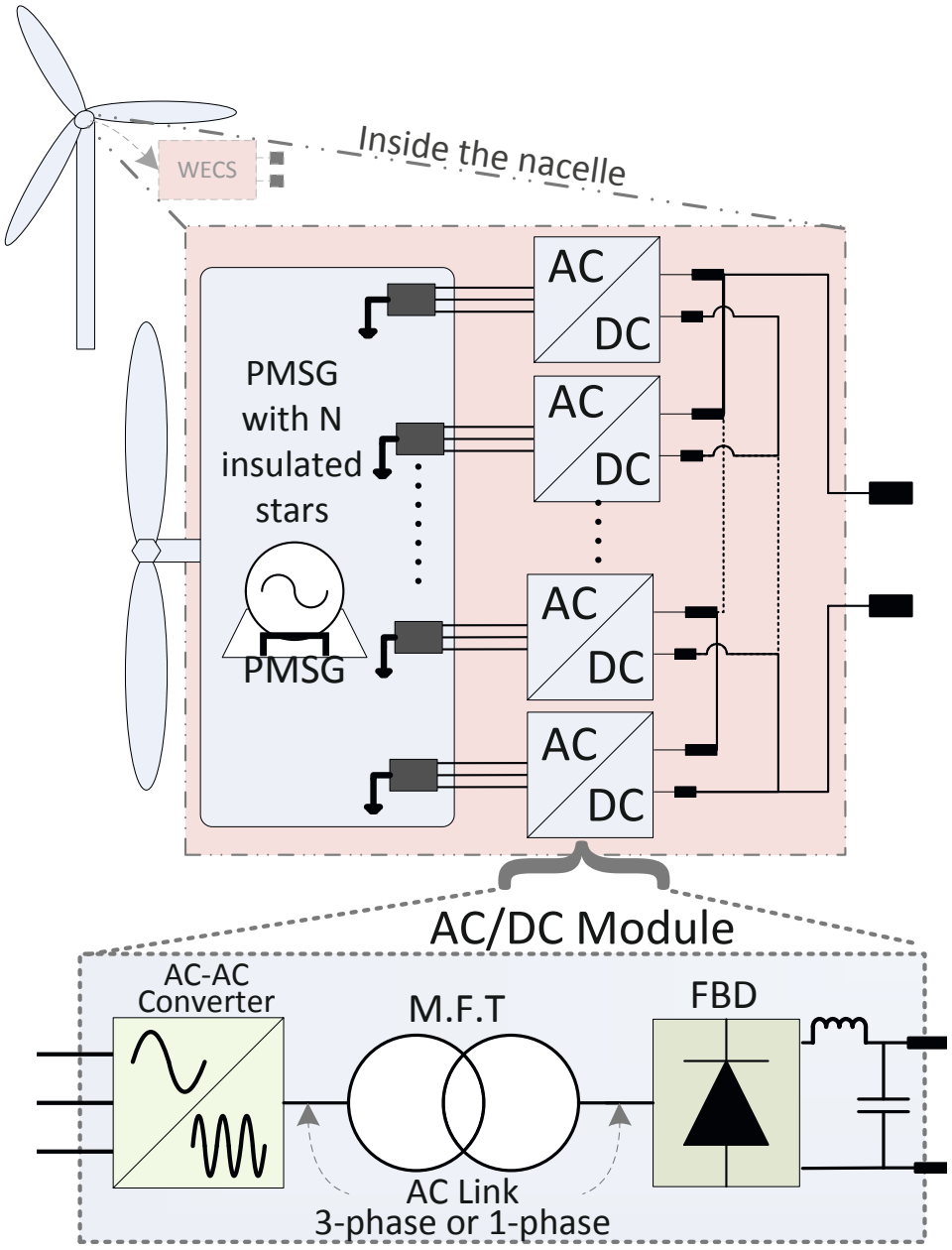


Figure 7.3: WECS architecture inside the turbine nacelle. Modular power converter based on medium frequency AC-Link for an offshore WT.

The main models, design constraints and parameters presented in chapter 3 are considered to evaluate the power losses, volume and mass of the power switches and diodes. The basic relationship between volume, mass and losses of inductor and capacitors presented in chapter 4 are considered. The MFT design methodology presented in chapter 5 is also considered. The design criteria of the compared topologies are derived in section 7.2 and section 7.3 for B2B and matrix topologies, respectively. The results of the six modular WECS solutions and their direct comparison are shown in Section 7.7. Finally, in section 8.1, the key findings are summarized.

7.2 Back-to-Back Topologies

In this chapter, the conventional B2B converter is taken as the reference topology because it is a well-established technology[50]. It features a DC-link capacitor separating the two VSI and smoothing inductors. Three converter topologies are compared in this study, based on the variation of the number of phases and waveform in the output: B2B3p, B2B3pSq and B2B1p. Figure 7.4 shows the considered B2B topologies in which the transformer side VSI has been modified to obtain the target output waveform. The space vector PWM modulation presented in [46] has been used for each VSI in the B2B3p. This modulation technique is also considered in [6] for a B2B topology in an offshore WECS based on MFT. The characteristics of these topologies are briefly discussed below.

7.2.1 Generator Side VSI and input filter

The generator side VSI and the input filter are common components in these three topologies. Given that the DC-Link capacitor provides decoupling in switching operation, the generator side converter can be operated at switching frequencies different from those of the transformer side converter. The main design guidelines presented in section 6.3 are considered. The DC-Link capacitance is designed according to suggestions presented in [48], which were derived with the knowledge that in one switching cycle, the input power drops to zero whereas the inverter maintains maximum output power, or vice versa:

$$C_{B2B} = \frac{P_m}{V_{DC1}^2 \cdot (\delta_{Vdc1} + 0.5 \cdot \delta_{Vdc1}^2) \cdot f_{sw1}} \tag{7.1}$$

where δ_{Vdc1} is the relative peak-to-peak DC-link ripple (limited to 5%), V_{DC1} is the DC-Link voltage of the B2B converter, P_m is the input power of the module, and f_{sw1} is the switching frequency of the generator side VSI. The input inductance is sized according to [50], in which a theoretical derivation is presented based on the current ripple at the switching frequency for a given input voltage amplitude

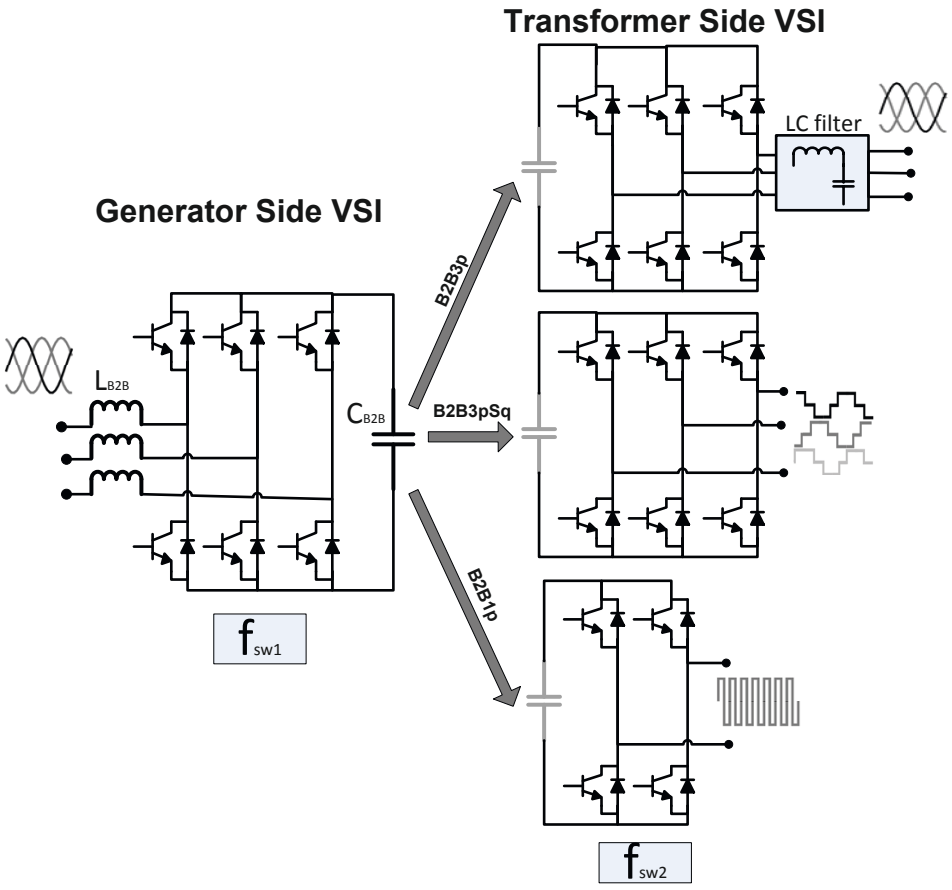


Figure 7.4: Back-to-Back Topologies

and a DC-Link voltage. The inductance value is calculated as follows:

$$L_{B2B} = \frac{V_g^2 \cdot \cos(\theta_g)}{\sqrt{2} \cdot P_m \cdot \delta_{iLin} \cdot f_{sw1}} \left(1 - \frac{\sqrt{3} V_g}{2 \cdot V_{DC1}}\right) \tag{7.2}$$

where δ_{iLin} is the relative peak-to-peak current ripple of the input current (limited to 3%), V_g is the RMS line-to-line generator voltage, and $\cos(\theta_g)$ is the power factor at the generator side. The DC voltage is related to the generator voltage by:

$$V_{DC1} = \frac{2\sqrt{2} \cdot V_g}{\sqrt{3} \cdot m_{S1}} \tag{7.3}$$

where m_{S1} is the modulation index of the converter. A 10% safety margin on the operation of the VSI ($m_{S1} = 0.9$) is taken into account during the design of the DC voltage.

The power losses at this stage are defined by equation 6.45, which has been re-written in this chapter by equation 7.4, where the DC-link capacitor losses are neglected, as shown in chapter 6:

$$P_{loss,VSg} = 6 \cdot n_{pg} \cdot (P_{igbt,VSg} + P_{diode,VSg}) + P_{LF,B2B}, \tag{7.4}$$

where n_{pg} is the number of IGBT modules connected in parallel at the generator side VSI, $P_{LF,B2B}$ is the inductor losses (Equations 4.20 and 4.32), and $P_{igbt,VSg}$ and $P_{diode,VSg}$ are the IGBT and diode losses of one switch at the generator side VSI, defined by 3.36 and 3.37, respectively. The average and RMS collector current (I_C) of each switch is calculated according to the models presented in section 6.2 for SVPWM modulation [46].

The volume and mass are calculated by equations 6.49 and 6.50, which are rewritten here:

$$Vol_{VSg} = 6 \cdot n_{pg} \cdot Vol_{sw} + Vol_{LF,B2B} + Vol_{cap,B2B},$$

$$Mass_{VSg} = 6 \cdot n_{pg} \cdot Mass_{sw} + Mass_{LF,B2B} + Mass_{cap,B2B}.$$

From the models presented in chapters 3 and 4, it is possible to evaluate the power losses, volume and mass for the VSI at the generator side as a function of the

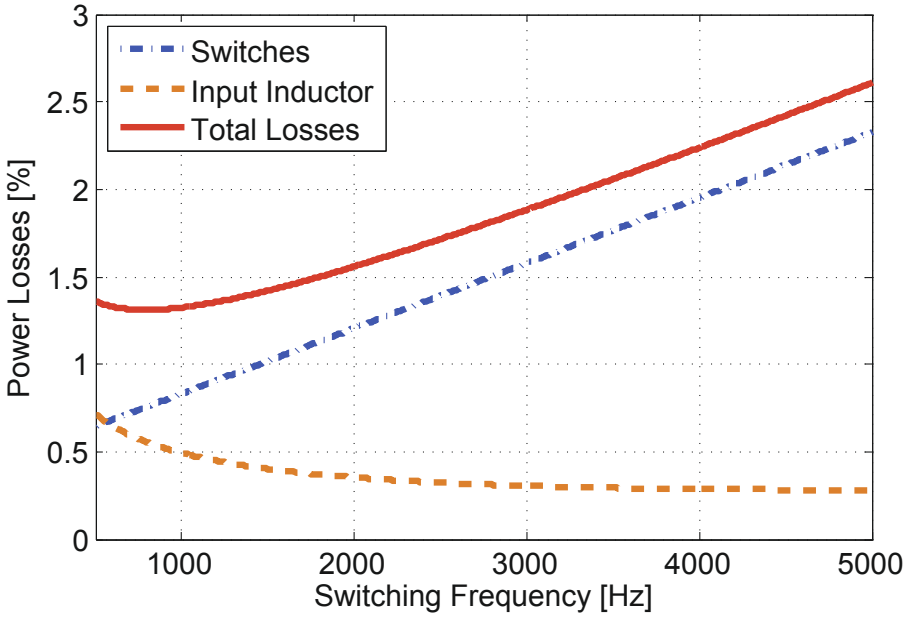


Figure 7.5: Evaluation of Power losses for generator side VSI. Example for 1 *MW* output power and different switching frequencies.

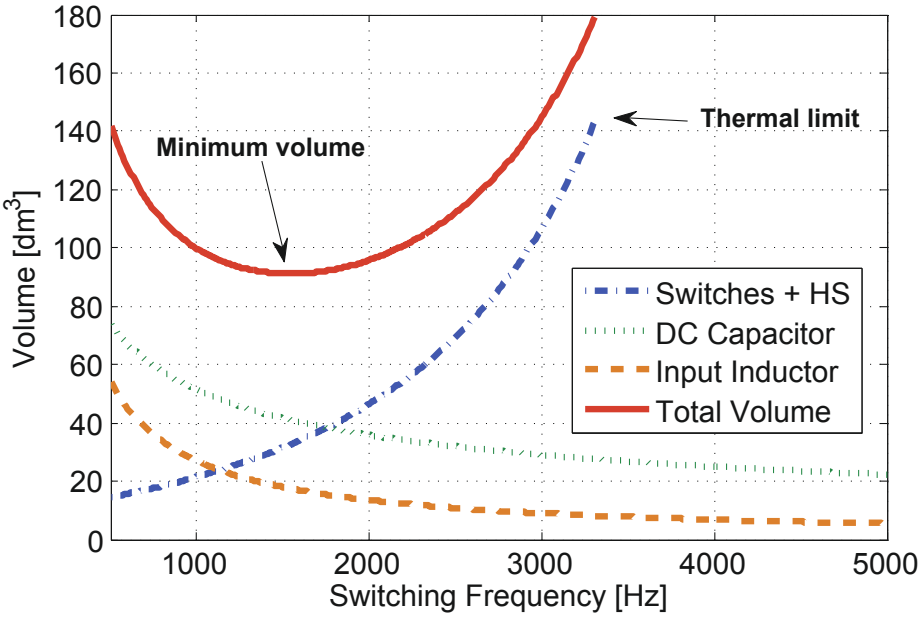


Figure 7.6: Evaluation of Total Volume for generator side VSI. Example for 1 *MW* output power and different switching frequencies.

switching frequency (f_{sw1}) and the input power of the module (P_m). Figure 7.5 shows an example of the power losses of the VSR as a function of the switching frequency for an output power of 1 *MW*. The total volume of the VSR as a function of the switching frequency is shown in Figure 7.6. Due to limited space, evaluation of the mass is not shown, but its behaviour is similar to the volume of Figure 7.6. As stated in chapter 6 and from Figure 7.5, it can be noted that power losses increase with switching frequency, but there is a switching frequency that minimizes the volume (and also the mass). The optimal switching frequency can then be obtained for each nominal power of the module. In this chapter, the switching frequency has been selected to minimize the following function:

$$OF_g = \frac{P_{loss,VSg}}{min\{P_{loss,VSg}\}} + \frac{Vol_{VSg}}{min\{Vol_{VSgen}\}} + \frac{Mass_{VSg}}{min\{Mass_{VSg}\}},$$

Figure 7.7 and Figure 7.8 show the results of this sub-optimization. Figure 7.7 presents the selected optimal switching frequency as a function of the module nominal power. The switching frequencies minimizing the power losses, volume and mass are also shown in Figure 7.7. Discontinuities in the curves are caused by the different number of IGBT modules connected in parallel (n_{pg}), which is indicated in each figure. Figure 7.8 shows the volume, mass and relative power losses for different nominal power ratings evaluated at optimal switching frequency.

7.2.2 Conventional B2B with sinusoidal output (B2B3p)

The B2B3p topology is shown in Figure 7.4 (at the top right). This is the converter that is traditionally used for AC-AC conversion. An output LC-filter is used to smooth the waveform in the transformer input and also allows unity input displacement factor operation at the maximum voltage transfer ratio. The LC-filter is sized according to [69], where equations are derived to obtain the minimum displacement angle at the transformer terminals. Inductance and capacitance are then calculated by:

$$C_{OF} = \frac{P_m}{3 \cdot \pi \cdot f_{cut} \cdot V_\varphi^2}; \quad L_{OF} = \frac{3 \cdot V_\varphi^2}{4 \cdot \pi \cdot f_{cut} \cdot P_m} \tag{7.5}$$

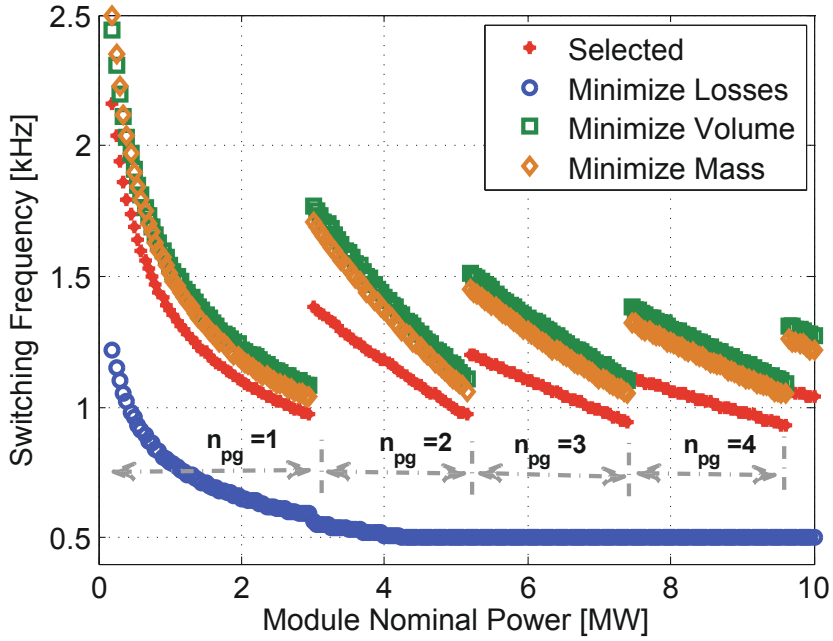


Figure 7.7: Selection of the optimal switching frequency. Results of sub-optimization of generator side VSI. Discontinuity in the curves are due to different number of IGBT modules parallel connected (n_{pg})

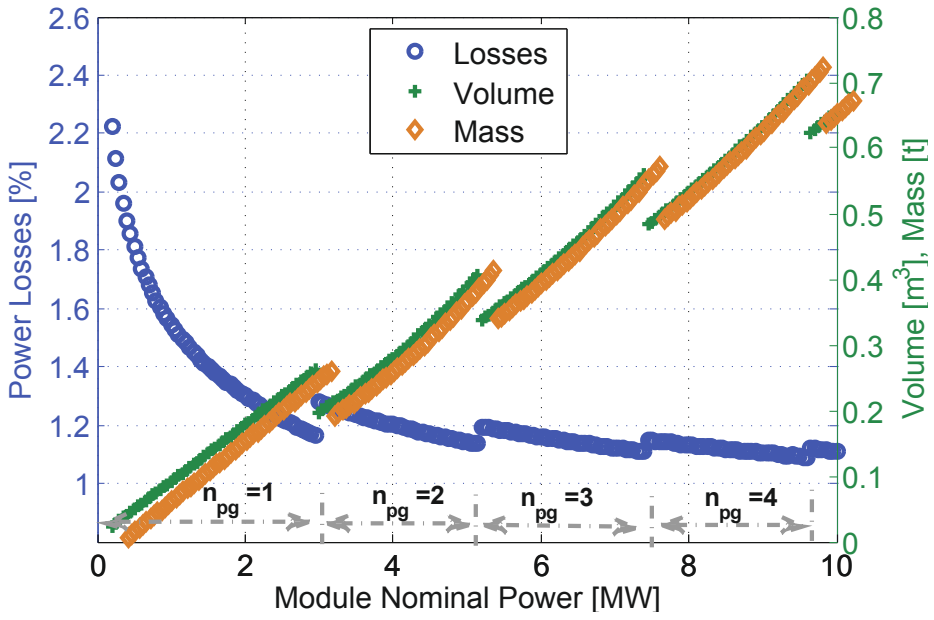


Figure 7.8: Mass (Yellow), Volume (green) and Power losses (blue) evaluated at optimal switching frequency. Results of sub-optimization of generator side VSI. Discontinuity in the curves are due to different number of IGBT modules parallel connected (n_{pg})

where f_{cut} is the cut-off frequency, set at twice the AC-Link frequency (f_{tr}), and V_{φ} is the output phase voltage of the converter. The switching frequency in the DC/AC converter (transformer side, f_{sw2}) is set at 8 times higher than the AC-Link frequency. The output voltage of the converter is related to the DC voltage by:

$$V_{DC1} = \frac{2\sqrt{2} \cdot V_{\varphi}}{m_{S2}} \tag{7.6}$$

where m_{S2} is the modulation index of the converter. A 10% safety margin for the operation of the VSI is applied ($m_{S2} = 0.9$), consistent with the criteria used for the generator side of the converter. Thus, the output voltage at nominal operation equals the nominal generator voltage ($\sqrt{3} \cdot V_{\varphi} = V_g$). The three phase transformer turn ratio for this topology is calculated by (7.7), where it is assumed that the transformer is D-Y connected and the LC-filter output voltage equals the converter output voltage.

$$N_{Tr-B2B3p} = \frac{\pi \cdot V_{DCout}}{3 \cdot \sqrt{6} \cdot V_g}. \tag{7.7}$$

The DC Output LC-filter is designed to fulfil the requirements of relative peak-to-peak current ripple of the output current (δ_{iDC}, limited to 10%) and the relative peak-to-peak DC-voltage ripple (δ_{vDC}, limited to 5%). Thus, if we consider a sinusoidal voltage at the second side of transformer, the following expression can be obtained by theoretical derivation:

$$L_{DC-B2B3p} = \frac{\left(6 - \sqrt{3} \cdot \pi\right) \cdot V_{DCout}^2}{36 \cdot \pi \cdot \delta_{iDC} \cdot f_{tr} \cdot P_m}, \tag{7.8}$$

$$C_{DC-B2B3p} = \frac{\delta_{iDC} \cdot P_m}{12 \cdot \pi \cdot f_{tr} \cdot \delta_{vDC} \cdot V_{DCout}^2}. \tag{7.9}$$

7.2.3 B2B with single-phase Square wave output (B2B1p)

The converter topology analysed for B2B1p is shown in Figure 7.4 (at the bottom right). The main difference between this topology and the B2B3p topology is that the output in the B2B1p topology is square wave form, such that the filter can be suppressed in the output. The B2B1p topology uses fewer switches than the B2B3p topology and the switching frequency in the DC/AC converter (transformer side) equals the AC-Link frequency. This topology, including the transformer side

VSI, a transformer and an FBD, is normally called the FB converter. Phase-shift modulation is the most efficient approach for this type of topology [56, 70]; therefore, this modulation scheme is considered in this chapter for B2B1p topology. The design guidelines reported in [55] for this type of converter with phase-shift modulation are considered. First, the transformer leakage inductance (l_{sk1}) should be considered to limit the amount of duty loss (D_{l1}):

$$l_{sk1} \leq \frac{V_{DC1}^2 \cdot D_{l1} \cdot (D_{n1} - D_{l1})}{4 \cdot P_m \cdot f_{tr}} \tag{7.10}$$

where D_{n1} is the duty cycle ($D_{l1} < D_{n1} \leq 1$), which is designed to be 0.9 at nominal operation with a duty loss of 0.1. The single-phase transformer turn ratio is then calculated by:

$$N_{Tr-B2B1p} = \frac{V_{DCout}}{D_{ef1} \cdot V_{DC1}} \tag{7.11}$$

where D_{ef1} is the effective duty cycle, defined as the difference between duty cycle and duty loss ($D_{ef1} = D_{n1} - D_{l1}$). The DC output filter inductor and capacitor for this topology are calculated based on the theoretical derivations presented in [55], as follows:

$$L_{DC-B2B1p} = \frac{(1 - D_{ef1}) \cdot V_{DCout}^2}{2 \cdot \delta_{iDC} \cdot P_m \cdot f_{tr}}, \tag{7.12}$$

$$C_{DC-B2B1p} = \frac{\delta_{iDC} \cdot P_m \cdot D_{ef1}}{f_{tr} \cdot \delta_{vDC} \cdot V_{DCout}^2}. \tag{7.13}$$

7.2.4 B2B with Three-phase Square wave output (B2B3pSq)

Figure 7.4 (at the middle right) shows the topology of the B2B3pSq. In this case, the output filter is not required because the square wave output voltage is applied to the transformer winding. Furthermore, in this topology, the switching frequency in the transformer side converter (f_{sw2}) equals the AC-Link frequency. The phase-shift modulation scheme reported in [71] is used here for this topology. Following the same design process used for B2B1p topology, the transformer leakage inductance per phase (l_{sk3}) should be considered to limit the amount of duty loss (D_{l3}):

$$l_{sk3} \leq \frac{V_{DC1}^2 \cdot D_{l3}}{3 \cdot (D_{n3} - D_{l3}) \cdot P_m \cdot f_{tr}} \tag{7.14}$$

$$D_{l3} < D_{n3} \leq 1/3 - D_{l3} \cdot \frac{(1+\delta_{iDC})}{(1-\delta_{iDC})}$$

where D_{n3} is the duty cycle, which is designed to be 0.2633 at nominal operation with a duty loss of 0.0333. The three-phase transformer turn ratio is then calculated by:

$$N_{Tr-B2B3pSq} = \frac{V_{DCout}}{6 \cdot D_{ef3} \cdot V_{DC1}} \tag{7.15}$$

where D_{ef3} is the effective duty cycle, defined as the difference between duty cycle and duty loss ($D_{ef3} = D_{n3} - D_{l3}$). The output DC filter inductor and capacitor for this topology are calculated with the same criteria used for the B2B1p, with theoretical derivations given by:

$$L_{DC-B2B3pSq} = \frac{(1 - 3 \cdot D_{ef3}) \cdot V_{DCout}^2}{3 \cdot \delta_{iDC} \cdot P_m \cdot f_{tr}}, \tag{7.16}$$

$$C_{DC-B2B3pSq} = \frac{\delta_{iDC} \cdot P_m \cdot D_{ef3}}{f_{tr} \cdot \delta_{vDC} \cdot V_{DCout}^2}. \tag{7.17}$$

7.3 Matrix converter Topologies

7.3.1 The Direct and Indirect Matrix Converter (DMC/IMC)

The DMC, in Figure 7.9 is a direct AC-AC converter. Unlike the B2B, the DMC does not feature a DC link capacitor, which saves volume and may increase lifetime. The IMC, in Figure 7.10, possesses a DC bus stage, but no capacitor. The modulation scheme used for both matrix converters is the Indirect Space Vector (ISV) Modulation scheme explained in [72], which is a convenient modulation scheme for this application. Bidirectional switches are required in the DMC and in the Current Source Rectifier (CSR) part of the IMC. A bidirectional switch can be implemented by two IGBTs and two diodes connected as shown in Figure 7.9. The switching frequency (f_{swMC}) is selected to be 8 times the frequency of the AC Link (f_{tr}) [73]. The output line-to-line voltage of the matrix converter is related to the generator voltage by:

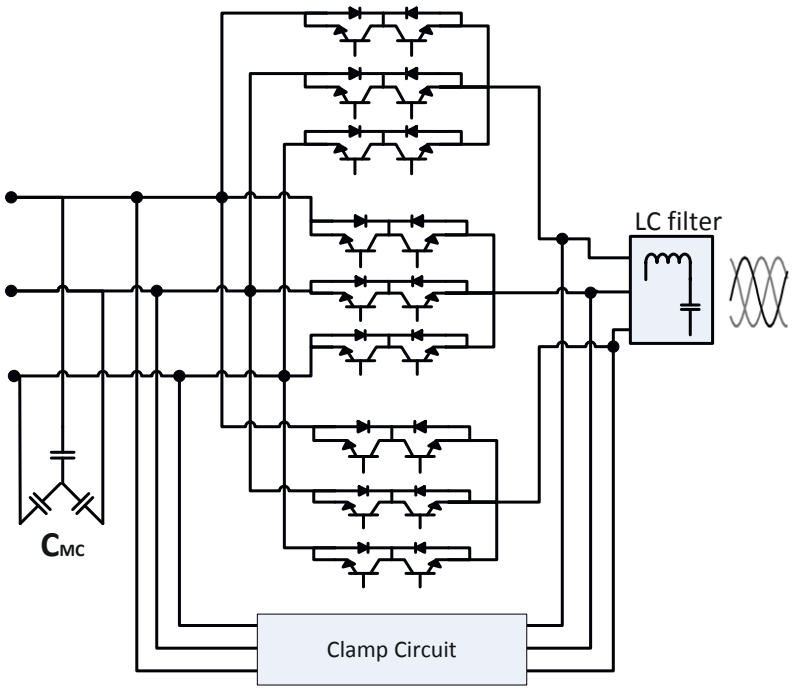


Figure 7.9: Direct Matrix Converter (DMC)

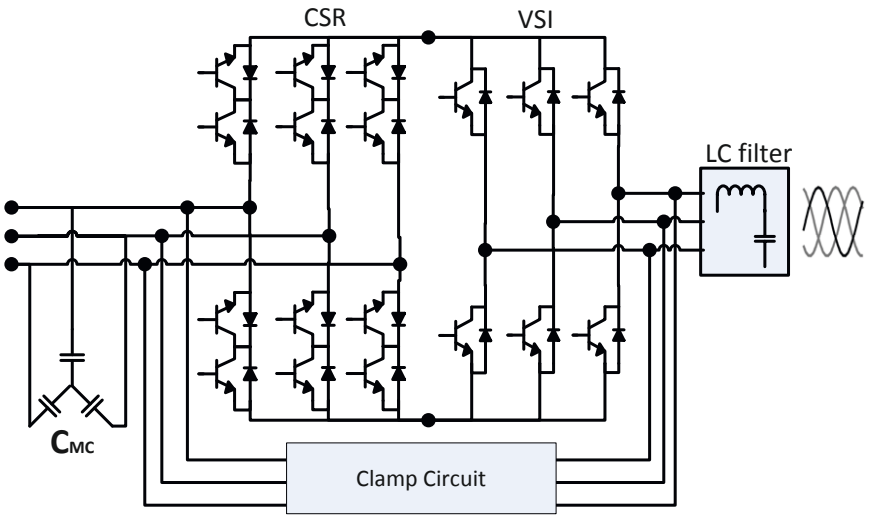


Figure 7.10: Indirect Matrix Converter (IMC)

$$V_{omc} = m_{Smc} \cdot V_g \tag{7.18}$$

where m_{Smc} is the modulation index of the matrix converter ($0 < m_{Smc} \leq \sqrt{3}/2$). Following the same criteria described for the B2B converter, a 10% safety margin on the nominal operation of the converter is considered ($m_{Smc} = 0.78$). Thus, the output voltage at nominal operation is 0.78 times the nominal generator voltage. The input capacitor of the matrix topologies is chosen according to the capacitor voltage ripple criteria presented in [50], which are based on both empirical engineering approximations and theoretical derivation:

$$C_{MC} = \frac{P_{omc}}{4 \cdot m_{Smc} \cdot V_g^2 \cdot f_{swMC} \cdot \delta_{Vmc} \cdot cos(\theta_{omc})} \tag{7.19}$$

where $cos(\theta_{oMC})$ is the power factor at the output of the matrix converter, and δ_{Vmc} is the relative peak-to-peak capacitor voltage ripple of the input voltage, which is limited to 10% as in [50]. An output LC-filter is also needed to filter out switching frequency harmonics. The inductance and capacitance of the LC-filter are designed with the same criteria used for the B2B3p converter with (7.5).

The three phase transformer turn ratio for this topology is calculated by (7.20), where it is assumed that the transformer is D-Y connected and the LC-filter output voltage equals the converter output voltage. The DC output LC-filter is designed with the same assumptions used for the B2B3p converter and the values are calculated with (7.8) and (7.9).

$$N_{Tr-MC} = \frac{\pi \cdot V_{DCout}}{3 \cdot \sqrt{6} \cdot V_{omc}} = \frac{N_{Tr-B2B3p}}{0.78}. \tag{7.20}$$

7.3.2 Reduced Matrix Converter (RMC)

The RMC is a direct AC-AC converter with a three-phase sinusoidal wave as an input and single-phase high frequency square wave as an output. This topology has been widely studied [4, 59, 74] and its basic scheme is shown in Figure 7.11. The RMC is operated as a current source converter, and the modulation schemes for the RMC are presented and analysed by [4]. SVM was reported to be the most efficient modulation scheme; therefore, it is considered in this comparison and its characteristics and parameters are taken from this study. The input capacitor of the RMC is chosen in the same way as for the DMC and IMC converters, see (7.19).

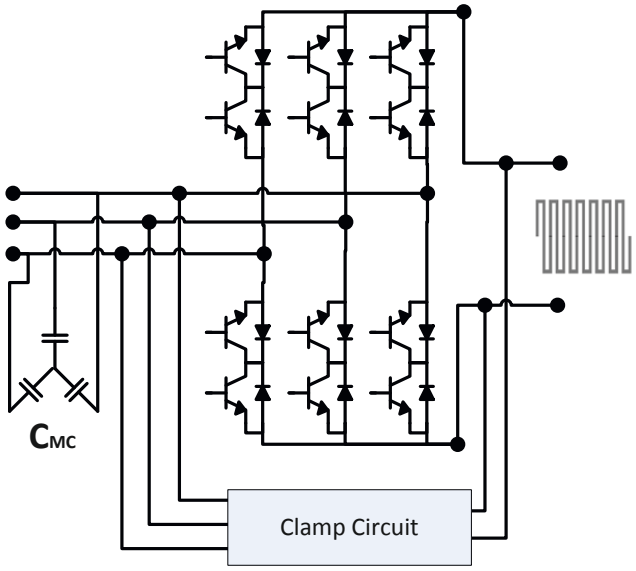


Figure 7.11: Reduced Matrix Converter (RMC)

Following the criteria presented in [4], the single-phase transformer turn ratio is calculated by:

$$N_{Tr-RMC} = \sqrt{\frac{2}{3}} \cdot \frac{V_{DCout}}{m_{S_R} \cdot V_g \cdot cos(\theta_g)} \tag{7.21}$$

where m_{S_R} is the modulation index of the RMC ($0 < m_{S_R} \leq 1$), which is considered to be 0.9 at nominal operation to keep a safety margin of 10%, like in the other converters. The DC output filter inductor and capacitor for this topology are considered to be the same as for B2B1p topology, and are calculated by (7.12) and (7.13).

7.3.3 Clamp Circuit

All matrix converter topologies considered in this chapter require a clamp circuit because unlike the B2B converter, they do not have a natural free-wheeling path in case of converter shut-down [75]. The protection scheme (clamp circuit) presented in [59] is considered in this study, and is shown in Figure 7.12. The criterion that must be considered for the design of the clamp circuit capacitor is that the energy accumulated in the machine, when an abnormal operation is forced, must be transferred to the capacitor, which is connected to an increase in voltage given

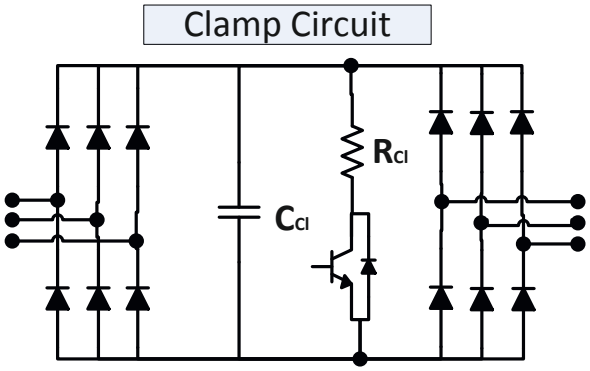


Figure 7.12: Considered protection scheme for matrix topologies

by:

$$C_{cl} \cdot \left(V_{clMax}^2 - V_{cl}^2\right) = 3 \cdot L_g \cdot \left(\frac{P_m}{\sqrt{3} \cdot V_g \cdot cos(\theta_g)}\right)^2 \tag{7.22}$$

where V_{cl} is the clamp circuit steady state voltage ($V_{cl} \approx \sqrt{2}V_g$), V_{clMax} is the maximum voltage of the circuit, and L_g is the phase inductance of the generator. The maximum voltage V_{clMax} is limited to protect the semiconductor devices in the matrix converter. Since 1.7 kV IGBTs are used to implement the power switches, 1.36 kV ($0.8 \cdot V_{CEblock}$) is selected as the maximum voltage. The clamp capacitor can be calculated from (7.22) for a given power, and volume and mass can be evaluated using (4.41) and (4.42), respectively.

Current and voltage ratings of semiconductor devices in the clamp circuit are assumed to be the same as in the main converter. Two bridge diode rectifier modules are considered for clamp circuits of matrix converter topologies. The main parameters are shown in Table 3.3. The clamp circuit does not consume any power during the normal operation of the system; therefore, clamp circuit power losses are not included in the calculation of total losses. It is also assumed that the clamp circuit module is cooled by mounting it on top of the heat sink of the main switches of the converter. The volume and mass of the clamp circuit are calculated by adding the volumes and masses of the FBDs, clamp capacitor and IGBT module:

$$Vol_{clamp} = 2Vol_{BDR} + Vol_{C,clamp} + Vol_{mod,clamp},$$

Table 7.1: General transformer design parameters

Parameter	Value
Magnetic Material	Metglas alloy 2605SA1
Saturation Flux density	B_{sat}=1.56 T
Flux density safety factor	$^{B_m}/_{B_{sat}}$=0.8
coefficients [α_C, β_C]	[1.47, 1.52]
Maximum temperature rise	$\triangle T_{Tr}$=80 ^oC
Minimum strand diameter	$d_{smin} = 0.0251mm$
Maximum Current Density	$J_{max} = 4\ ^{\mathrm{A}}/_{\mathrm{mm}^2}$
Maximum number of layers	$p_{layer1Max} = 10$
	$p_{layer2Max} = 40$
Ambient temperature	40 ^oC

$$Mass_{clamp} = 2Mass_{BDR} + Mass_{C,clamp} + Mass_{mod,clamp}.$$

7.4 Transformer Volume and Mass evaluations for different converter topologies

The design methodology presented in chapter 5 is used here to evaluate the volume, mass and power losses of the MFT for the different converter topologies. General parameters used in the transformer design are presented in Table 7.1. Metglas alloy 2605SA1 was chosen as a core material, as suggested for offshore wind farms in [1]. Besides the parameters presented in Table 7.1, other parameters also depend on the converter topology, including: the transformer turn ratio (N_{Tr}), the waveform factor (K_{wf}), the RMS primary voltage (V_{prms}), the total apparent power (S_m) and the maximum primary current (I_{pmax}). Table 7.2 compares these parameters for the considered converter topologies; some of these parameters are normalized to facilitate the comparison.

As an example, the volume/mass has been evaluated for a 3.3 *MW* power transformer with the design parameters for the six different converters in Figure 7.13. Figure 7.13 also shows how the volume-mass of the transformer depends on the frequency when it increases from 500 *Hz* to 20 *kHz*. The values in Figure 7.13 result from the design of the transformer, which minimizes objective function (5.7) for each frequency. In general, transformer volume and mass decrease as frequency

Table 7.2: Comparison of transformer design parameters for different topologies

Parameter / Topology↓	$\frac{N_{Tr}}{(V_{DCout}/V_g)}$	K_{wf}	$\frac{V_{prms}}{V_g}$	$\frac{S_m}{P_m}$	$\frac{I_{pmax}}{(P_m/V_g)}$
B2B3p	$\frac{\pi/3}{\sqrt{6}} \approx 0.43$	1.11 (sine)	1	$\frac{1}{PF_{Tr}} \approx 1.11$	$\frac{\pi\cdot\left(1+\frac{\delta_{iDC}}{2}\right)}{3\sqrt{6}} \approx 0.45$
B2B1p	$\frac{m_{S_1}\sqrt{3/2}}{2D_{ef1}} \approx 0.69$	$\frac{\sqrt{D_{n1}}}{D_{ef1}} \approx 1.19$	$\frac{\sqrt{8D_{n1}}}{m_{S_1}\sqrt{3}} \approx 1.72$	$K_{wf}\cdot\sqrt{\frac{3-D_{l1}}{3}} \approx 1.17$	$\frac{m_{S_1}\left(1+\frac{\delta_{iDC}}{2}\right)}{2D_{ef1}\sqrt{\frac{2}{3}}} \approx 0.72$
B2B3pSq	$\frac{m_{S_1}}{D_{ef3}\sqrt{96}} \approx 0.4$	$\frac{\sqrt{\frac{D_{n3}}{2}}}{D_{ef3}} \approx 1.58$	$\frac{\sqrt{16D_{n3}}}{m_{S_1}\sqrt{3}} \approx 1.32$	$\sqrt{\frac{K_{wf}^2\left(1-\frac{D_{l3}(4+2\delta_{idc})}{(1-\delta_{idc})}\right)}{1.5}} \approx 1.2$	$\frac{m_{S_1}\left(1+\frac{\delta_{iDC}}{2}\right)}{D_{ef3}\sqrt{96}} \approx 0.42$
DMC/IMC	$\frac{\pi/3}{\sqrt{6}m_{Smc}} \approx 0.55$	1.11 (sine)	$m_{S_{mc}} = 0.78$	$\frac{1}{PF_{Tr}} \approx 1.11$	$\frac{\pi\cdot\left(1+\frac{\delta_{iDC}}{2}\right)}{3\sqrt{6}m_{Smc}} \approx 0.58$
RMC	$\frac{\sqrt{2/3}}{m_{S_R}\cdot PF_g} \approx 1.01$	≈ 1.06*	$\frac{m_{S_R}\cdot PF_g}{\sqrt{2/3}} \approx 0.99$	$\frac{1}{1-D^*_{loss}} \approx 1.20$	$\frac{\sqrt{\frac{2}{3}}\left(1+\frac{\delta_{iDC}}{2}\right)}{m_{S_R}\cdot PF_g} \approx 1.06$

**RMC waveform factor and duty loss are the average value calculated from simulation data*

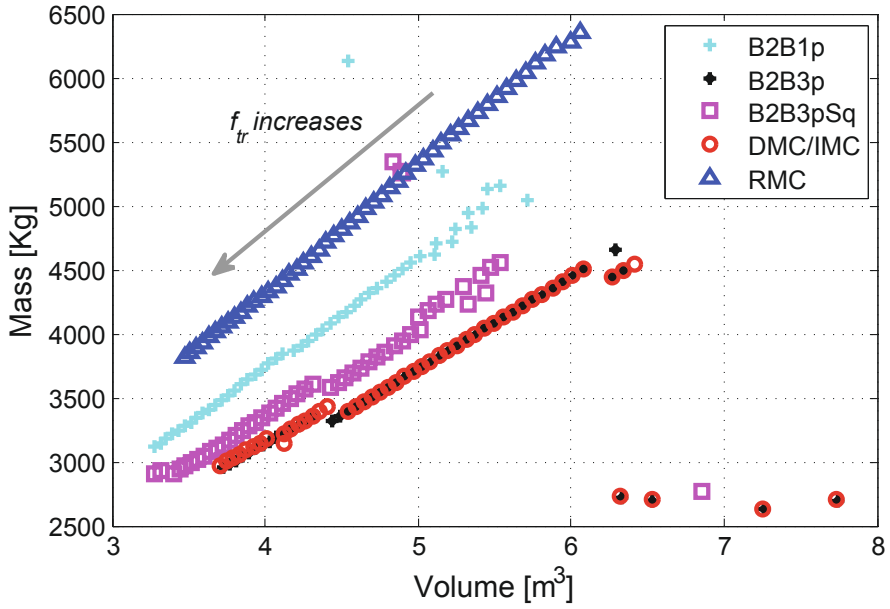


Figure 7.13: Transformer volume-mass frontier variation with AC-link frequency for 3.33 *MW* transformer

increases. Furthermore, solutions with a single-phase transformer (B2B1p and RMC) have a higher volume and mass than those with a three-phase transformer (B2B3p, B2B3pSq and DMC/IMC).

7.5 Full Bridge Diode Rectifier

The FBD is implemented by discrete diodes, and diodes connected in series have been considered to fulfil the output voltage. An output LC-filter limiting the DC-voltage and DC-current ripple is also considered. The parameters of the Infineon Diode modules are shown in Table 3.3 and they have been used here to estimate power losses, volume and mass with the models presented in chapter 3. The power losses, volume and mass of the DC capacitor and Inductor are calculated by the method shown in chapter 4.

7.6 Simplification of switching losses

To reduce the complexity of the evaluation of equations 3.11 and 3.12, in this chapter, the switching losses in the IGBTs and diodes are calculated with a slightly simpler loss model that involves only linear functions:

$$E_{sw} = \frac{E_{test}}{V_{test} \cdot I_{test}} \cdot V_{CE}^{*} \cdot I_{C}^{*} = K_E \cdot V_{CE}^{*} \cdot I_{C}^{*}$$

where V_{CE}^{*} is the voltage in the switch device at moment before it is turned on or after it is turned off and I_{C}^{*} is the current through the switch device at moment before it is turned off or after it is turned on. The values of E_{test}, V_{test} and I_{test} can be found in the data-sheet of the devices for each type of commutation (turn on, turn off or reverse recovery [rr]). The parameter K_E is included in Table 3.3 for each type of commutation. To calculate the average switching loss, the sum of each commutation energy (E_{sw}) over a time period and divided by the time period are computed and added:

$$P_{sw} = \frac{1}{T} \sum \left(E_{sw,on} + E_{sw,off} + E_{sw,rr} \right). \tag{7.23}$$

To reduce the complexity of the evaluation of (7.23), (7.23) has been approximated by empirical engineering based on simulation data for each topology. The following expression can then be used:

$$P_{sw} \approx (K_{E,on} + K_{E,off} + K_{E,rr}) \cdot V_{in} \cdot I_o \cdot Sfun(f_{sw}), \tag{7.24}$$

$$Sfun(f_{sw}) = kp_1 \cdot f_{sw} + kp_0$$

where V_{in} is the RMS input voltage of the VSI or Matrix Converter (MC), I_o is the RMS output current of the VSI or MC, depending on the case, f_{sw} is the switching frequency, and kp_i are the polynomial regression coefficients as a function of the topology, modulation strategy and power factor. As an example, Fig. 7.14 shows the function $Sfun(f_{sw})$ for different converter topologies with a 0.9 power factor and the modulation strategies described in section 7.2. In Fig. 7.14, VSI-SVPWM refers to a VSI with sinusoidal output and SVPWM modulation [46], DMC-ISV to the DMC with ISV modulation [73, 72], IMC-CSR-ISV to the current source rectifier of the IMC with ISV modulation [73, 72], IMC-VSI-ISV to the VSI of the IMC with ISV modulation [73, 72], RMC-SVM to the RMC with space vector modulation [59], and VSI-1SQ to a VSI with single phase square wave output [55].

7.7 Comparative Analysis

The volume, mass and power losses are evaluated here for a 10 *MW* complete modular power converter with a different number of modules. The WECS shown

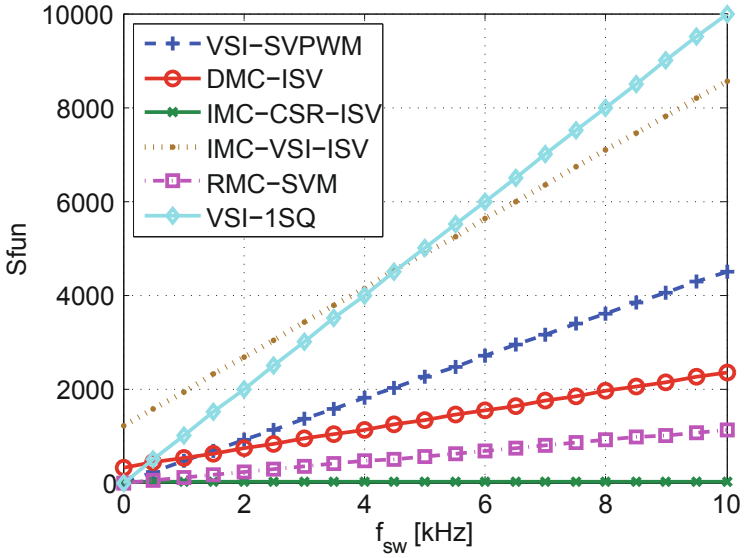


Figure 7.14: Function *Sfun* for different converter topologies.

in Figure 7.3 and the topologies for the AC-AC converter shown in Figure 7.4 and Figures 7.9-7.11 are compared. The system parameters and design constraints used in the comparison are indicated in Tables 7.1, 7.2, 7.3 and 7.4. Configurations that do not correspond to the requirements in the thermal and magnetic design are not shown. The FBD is implemented by discrete diodes and one output LC-filter is considered to limit the DC-voltage and DC-current ripple. The parameters of the Infineon Diode modules are shown in Table 3.3 and they are used here to estimate the power losses, volume and mass with the models presented in chapter 3. The volume and mass of the DC capacitor and Inductor are calculated by the method presented in chapter 4.

7.7.1 Minimum losses

First, an optimization problem has been solved to find the solutions with the smallest power losses as a function of the AC-Link frequency and the number of modules. Figure 7.15 and Figure 7.16 show the solutions with minimum power losses for each converter topology analysed. From Figure 7.15, it can be noted that power losses increase exponentially with AC-link frequency. In general, topologies based on a squared waveform are more efficient than those based on a sinusoidal waveform, mainly because sinusoidal waveforms require higher switching frequencies in the AC-AC converter. Figure 7.16 shows the realtionship between power losses and the number of modules. Power losses increase with the number of modules for

Table 7.3: System parameters and design variables for the 10[MW] modular converter

Parameter	Symbol	Value
Total Power	P_{Total}	10 *MW*
Input Voltage line-line	V_g	690 *V*
Output DC Voltage	V_{DCout}	33 kV
AC-Link Freq.	f_{tr}	(500 *Hz*,...,20 *kHz*)
Number of modules	N	(1,...,25)
Input Power Factor	PF_g	0.9
Nominal generator frequency	f_1	50 *Hz*
Equivalent gen. inductance per phase	L_M	1e-4 *pu*
Overload factor	k_{olf}	0.3
Ambient temperature	T_{amb}	40 *ºC*
Volume utilisation factor	C_{PV}	0.6

Table 7.4: Design constraints and references models for the 10 MW modular converter

Constraint	Symbol	Value
Safety factor for DC voltage	k_{vdc}	0.6
Safety factor for peak voltage	k_{vp}	0.8
Safety factor of thermal design	K_{SFT}	0.8
Relative Input current ripple	δ_{iLin}	3%
Relative DC-voltage ripple	δ_{vDC}	5%
Relative DC-current ripple	δ_{iDC}	10%
Relative input voltage ripple	δ_{Vmc}	10%
Max. relative inductor voltage	$\delta_{VL,max}$	30%
Max. relative heat sink volume	$\delta_{HS,max}$	5
Min. heat sink thermal resistance	$R_{thHS,min}$	15 *K/kW*
Heat sink model	DAU series BF-XX with axial fan SEMIKRON series SKF-3XX at 10m/s	
DC Inductor model	Siemens series 4EUXX – Cu.	
AC Inductor model	CWS series TPC - Cu.	
DC Capacitor model	MKP DC B256xx-series	
AC Capacitor model	MKP AC B2536-series	

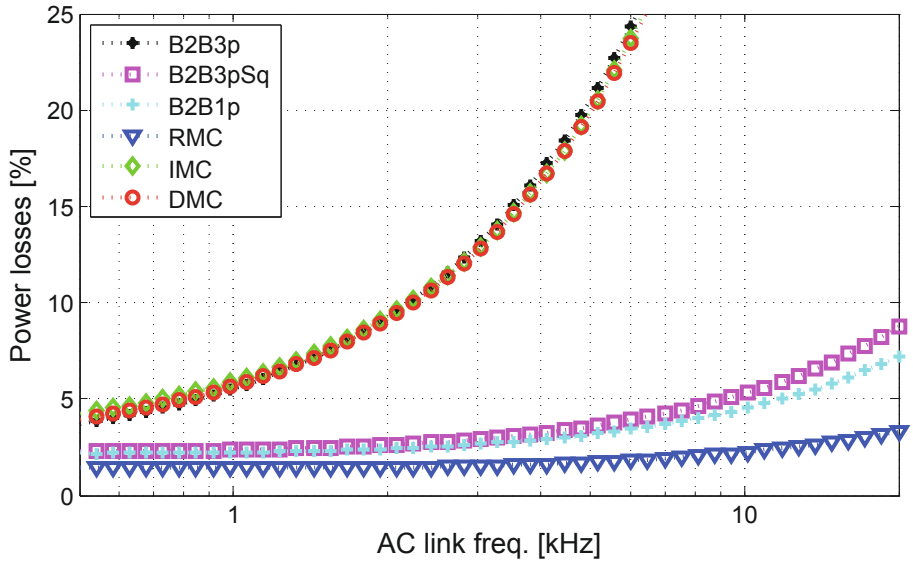


Figure 7.15: Minimum Power losses vs AC-Link frequency for the complete modular converter with a rated power of 10 *MW*

solutions based on B2B topologies; however, for solutions based on matrix topologies, a small increase in the number of modules reduces total power loss, and 5, 6 and 3 modules produce the smallest power losses in solutions with IMC, DMC and RMC topologies, respectively. Solutions based on RMC are the most efficient for all frequencies and any number of modules selected. The smallest loss (1.41%) is achieved for the RMC when the number of modules is 3 and the frequency is 1.062 *kHz*.

7.7.2 Minimum Volume

Figure 7.17 and Figure 7.18 show the total volume of the converters as a function of of AC-link frequency and the number of modules, respectively. From Figure 7.17, it can be observed that the most compact solutions are achieved with RMC topology and AC-link frequencies above 7 *kHz*. However, in contrast with RMC solutions, solutions based on B2B3pSq topology show volume increases of around 16% in frequencies ranging between 2 *kHz* and 3 *kHz*. Although RMC topology

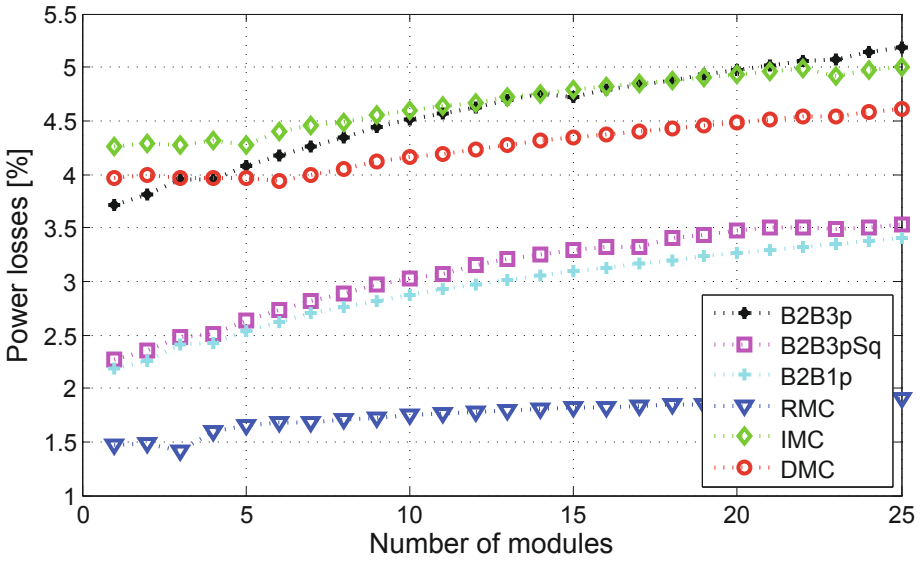


Figure 7.16: Minimum Power losses vs Number of modules for the complete modular converter with a rated power of 10 *MW*

produces the most compact solution, it can be noted from Figure 7.17 that RMC topologies give rise to the bulkiest solutions for frequencies below 3 *kHz*, at which solutions based on B2B3pSq and DMC topologies show lower volumes.

From Figure 7.18, it can be noted that for RMC topologies, solutions with one module are less compact than those with several modules. In fact, the most compact solution when one module is selected is achieved with B2B1p topology. In addition, it can be noted that the minimun volume for all topologies is achieved for a number of modules ranging between 12 and 15.

Finally, the RMC topology achieves its lowest volume of $9.48\,m^3$ with 12 modules and an AC-Link frequency of 20 *kHz*. By contrast, the B2B3pSq solution achieves its lowest volume of $11.01\,m^3$ when the number of modules is 14 and the frequency is 2.62 *kHz*, whereas the DMC solution achieves its lowest volume of $11.45\,m^3$ (21% more than the minimum volume for RMC topology) with 14 modules and a frequency of 1.8 *kHz*.

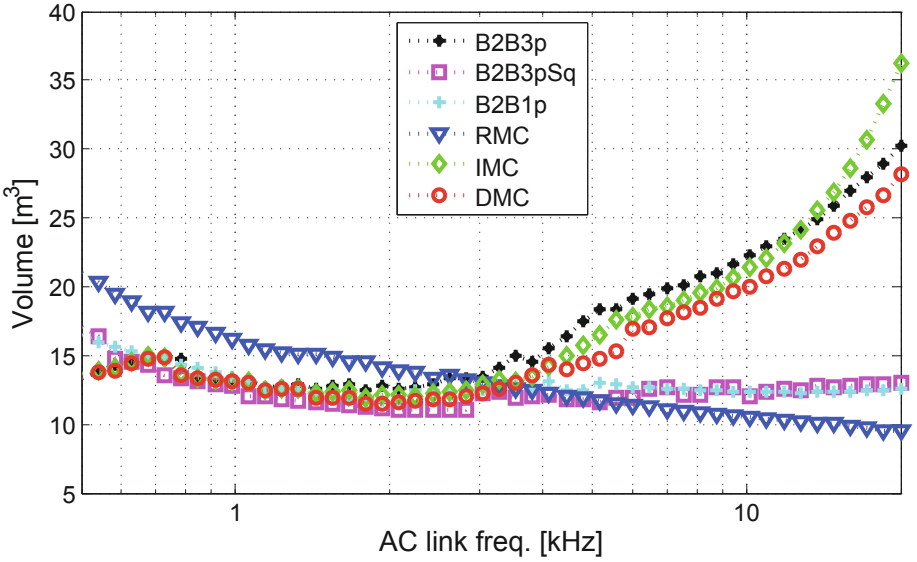


Figure 7.17: Minimum volume vs AC-Link frequency for the complete modular converter with a rated power of 10 *MW*

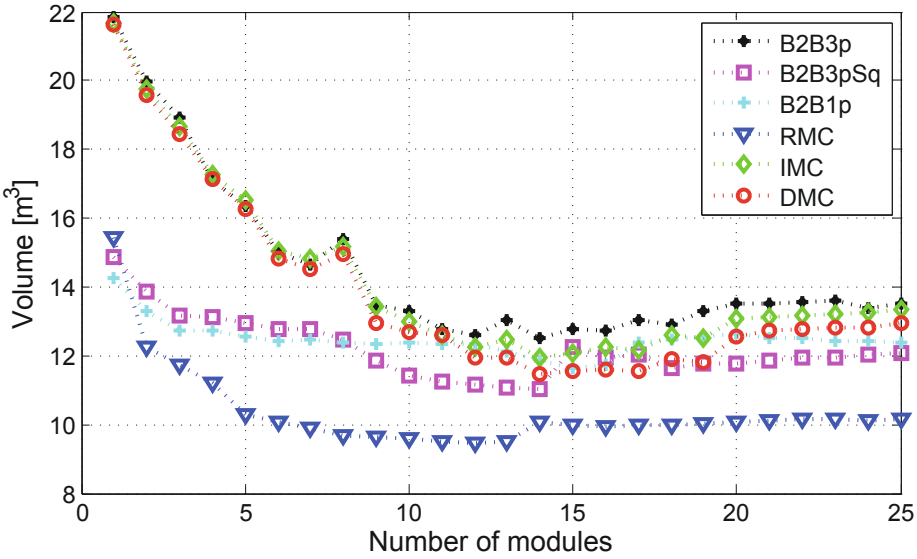


Figure 7.18: Minimum volume vs number of modules for the complete modular converter with a rated power of 10 *MW*

7.7.3 Minimum Mass

A third optimization problem has been solved to find the solutions with minimum mass as a function of the AC-Link frequency and the number of modules, as shown in Figure 7.19 and Figure 7.20. From Figure 7.19, it can be observed that an increase in frequency is beneficial for solutions based on a square waveform but not for the other solutions (based on a sinusoidal waveform). The solutions with the lowest possible mass are achieved with B2B3p and DMC topologies for AC-link frequencies below 1 *kHz*. However, solutions based on B2B3pSq and B2B1p topologies show mass increases of around 20% for frequencies above 10 *kHz*. Furthermore, it can be noted from Figure 7.19 that RMC topology produces solutions of high mass for frequencies below 4 *kHz*, but for frequencies above 16 *kHz*, the resulting mass with RMC topology is similar to that with B2B3pSq topology (around 21% more).

From Figure 7.20, it can be noted that solutions with B2B3p or DMC topologies produce the solutions with the lowest mass for any given number of modules. In addition, an increase in the number of modules will increase the total mass of the solution, except for B2B1p and B2B3pSq topologies, for which minimum mass is achieved when 3 modules are used. From Figure 7.19 and Figure 7.20, it can be noted that solutions with similar waveforms show similar behaviour regarding the dependency of total mass on frequency and the number of modules.

Finally, B2B3p topology achieves its lowest mass of $10.15\,t$ with 1 module and an AC-Link frequency of 600 *Hz*. By contrast, DMC topology attains its lowest mass of $10.78\,t$ (6% more than B2B3p) when the frequency is 630 *Hz* and the number of modules is 3. Additionally, the B2B3pSq solution achieves its lowest mass of $12.23\,t$ (20% more B2B3p) when the number of modules is 3 and the frequency is 12.73 *kHz*, whereas that RMC solution attains its lowest mass of $12.81\,t$ (26% more than the minimum found for B2B3p) with 1 module and a frequency of 20 *kHz*.

7.8 Comparison of the optimal solutions – Pareto Front

From Figure 7.15 to Figure 7.20, it can be observed that there is no single solution that minimizes all performance indexes. Instead of one solution, there is a set of solutions that provide the best trade-off between the volume, mass and power

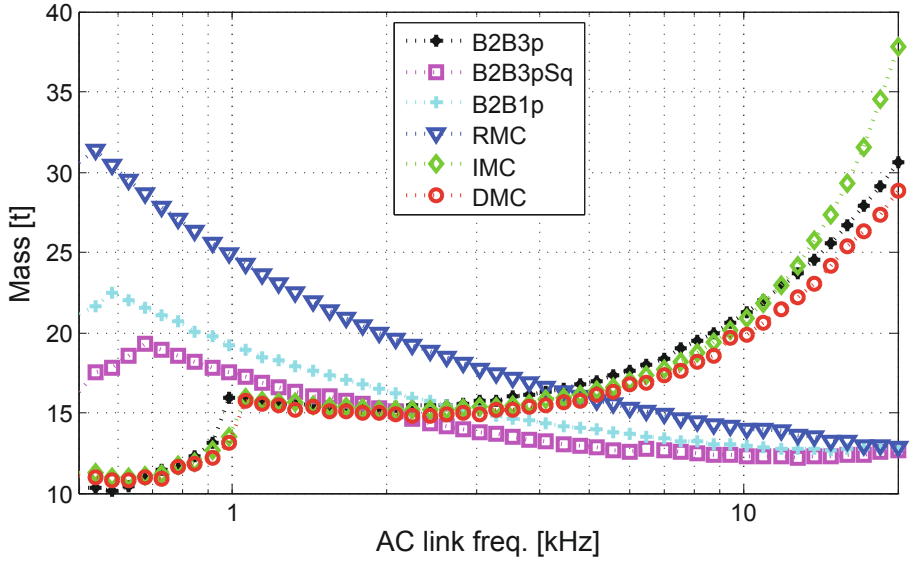


Figure 7.19: Minimum Mass vs AC-Link frequency for the complete modular converter with rated power of 10 *MW*

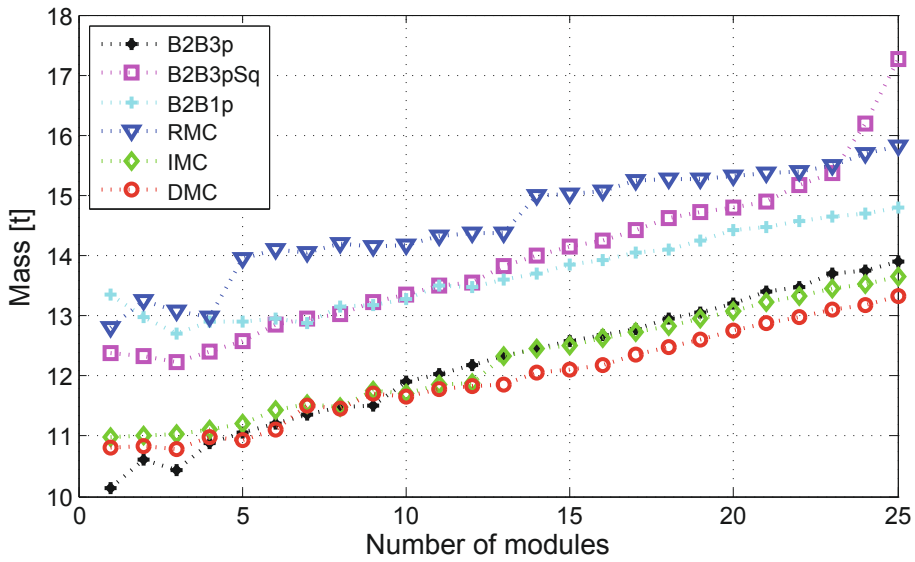


Figure 7.20: Minimum Mass vs number of modules for the complete modular converter with rated power of 10 *MW*

losses. This set of solutions is called the Pareto set, and if there are three performance indexes, it is called a Pareto surface. Figure 7.21 shows the Pareto surface of the performance indices (P_{Loss}, Vol_{Total}, $Mass_{Total}$). Figures 7.22-7.24 show the projection of the Pareto surface onto the two-dimensional planes creating the Pareto-Front of each couple of performance indicators: power losses vs. volume (Figure 7.22), power losses vs. mass (Figure 7.23) and volume vs. mass (Figure 7.24).

From Figure 7.22, it is evident that solutions based on RMC topology produce the best trade-off between volume and power losses and between η and ρ. Moreover, the slope of the Pareto-Front in RMC solutions suggests that even more compact solutions can be achieved without substantially increasing the total power losses. Indeed, this improvement can be achieved by increasing the AC-link frequency above 20 *kHz*, as observed from Figure 7.17. In terms of mass and power losses, two topologies constitute the Pareto-Front, B2B3p and RMC, as shown in Figure 7.23. However, only two solutions based on B2B3p are in the Pareto-Front, whereas the Pareto-Front includes several solutions based on RMC topology. By contrast, when only mass and volume are considered, as shown in Figure 7.24, the Pareto-Front is composed of solutions based on four topologies: B2B3p, DMC, B2B3pSq and RMC. Finally, solutions based on RMC topology belong to all Pareto-Fronts presented in Figures 7.22-7.24, and solutions based on IMC topology do not belong to any Pareto-Front.

The following equation can be used to quantify the trade-off between the three performance indexes and to choose a representative solution for each topology:

$$\Lambda = \frac{P_{Loss}}{P_{lossMin}} + \frac{Vol_{Total}}{Vol_{Min}} + \frac{Mass_{Total}}{Mass_{Min}} \tag{7.25}$$

where $P_{LossMin}$, Vol_{Min} and $Mass_{Min}$ are the minimum power losses, volume and mass, respectively. In this study, $P_{LossMin} = 1.41\%$, $Vol_{Min} = 9.48m^3$ and $Mass_{Min} = 10.15t$ have been selected based on the results presented in Figure 7.15, 7.17 and 7.19. The representative solution for each topology is then selected to minimize (7.25), and these are highlighted in grey in Figure 7.21. Of note, representative solutions do not belong to all Pareto-Fronts.

Finally, the resultant main properties of the representative solutions of the B2B3p, B2B3pSq, DMC and RMC are summarized in Table 7.5 and six characteristic performance indicators are presented in Figure 7.25. In this last comparison, IMC and B2B1p topologies are not considered because these solutions do not belong to the Pareto-Surface. The two additional performance indicators are defined as follows:

- Normalized total cost of the semiconductor modules in the AC-AC converter:

$$\bar{C}_{PM} = N_m \cdot \sum N_{sw} \cdot n_p \cdot \frac{I_{npm}}{I_{ref1}} \tag{7.26}$$

where N_{sw} is the number of unidirectional switches in the AC-AC converter, I_{npm} is the nominal current of the power module, and I_{ref1} is a reference current rating for IGBT modules ($I_{ref1} = 3.6\,kA$ is considered). This performance indicator assumes that the cost of semiconductor module is proportional to the semiconductor power rating.

- Normalized total cost of the power diodes in the FBD:

$$\bar{C}_{FBD} = N_m \cdot \sum N_D \cdot n_s \cdot \frac{I_{nD}}{I_{ref2}} \tag{7.27}$$

where N_D is the number of diodes in the FBD (6 in three-phase and 4 in single-phase), I_{nD} is the nominal current of the power diode, and I_{ref2} is a reference current rating for power diodes ($I_{ref2} = 750A$ is considered). This performance indicator assumes that the cost of the power diode is proportional to the diode power rating.

In Figure 7.25, the area spanned by the polygon curves can be considered to be a relative measure for comparison. The better the solution is, the smaller the area.

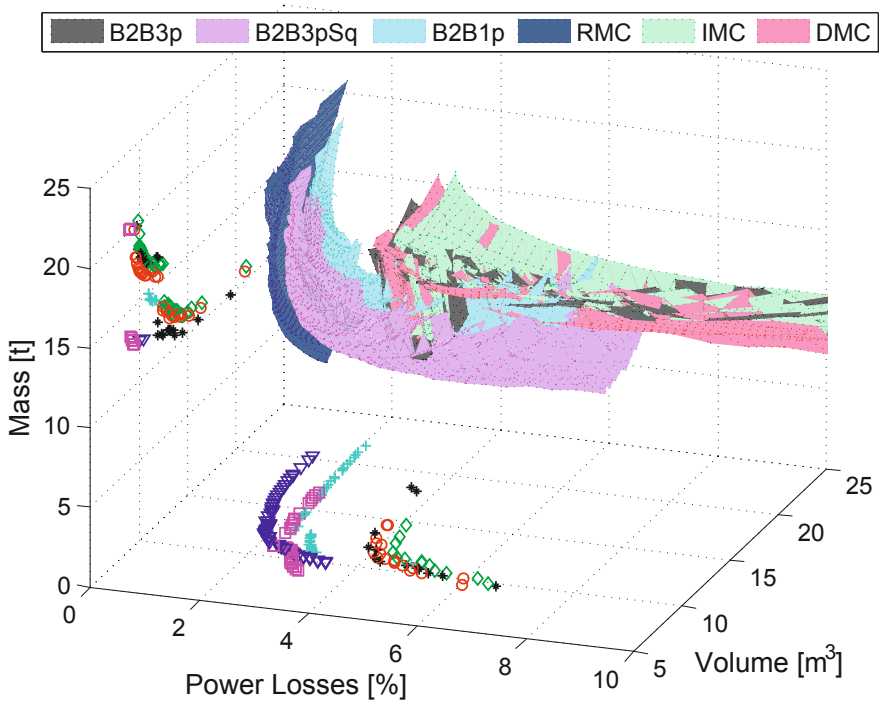


Figure 7.21: Pareto surface of the performance indicators for a 10 *MW* modular power converter and considering different topologies.

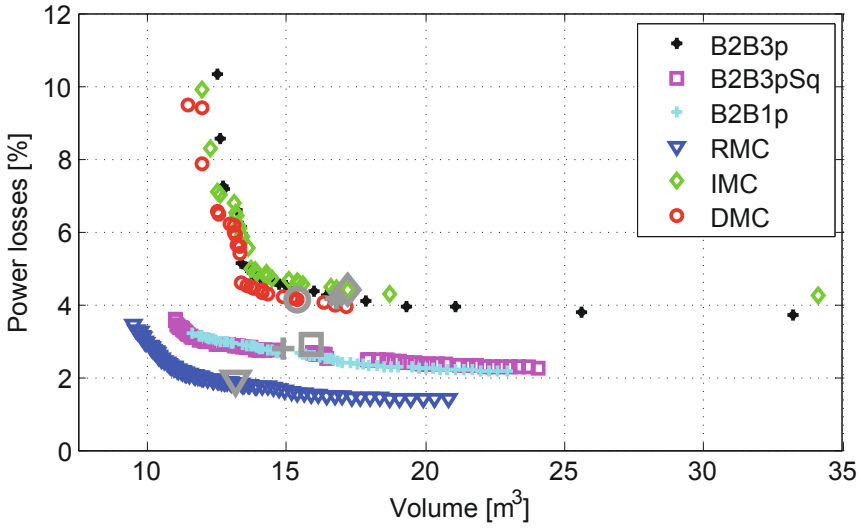


Figure 7.22: Power losses vs. volume. Projection of the Pareto surface to the two-dimensional planes P_{Loss}- Vol_{Total} creating the Pareto-Front for a 10 *MW* modular power converter and considering different topologies.

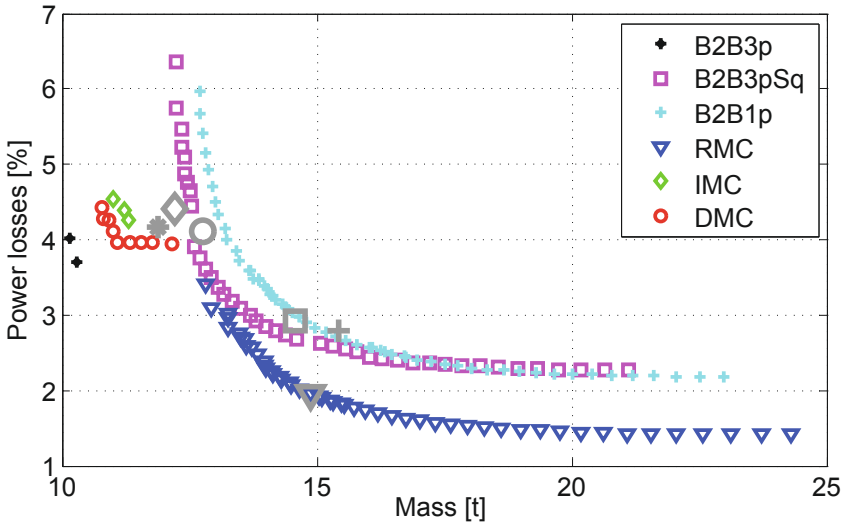


Figure 7.23: Power losses vs. mass. Projection of the Pareto surface to the two-dimensional planes P_{Loss}- $Mass_{Total}$ creating the Pareto-Front for a 10 *MW* modular power converter and considering different topologies.

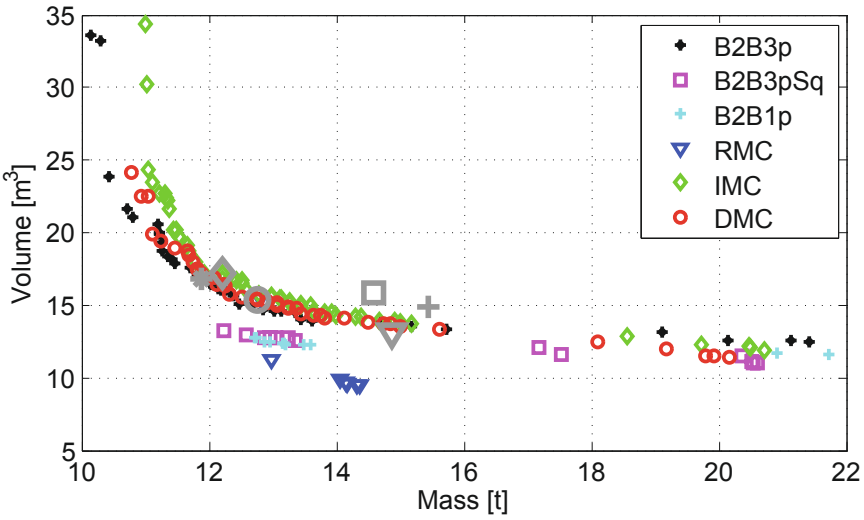


Figure 7.24: Volume vs. mass. Projection of the Pareto surface to the two-dimensional planes Vol_{Total} - $Mass_{Total}$ creating the Pareto-Front for a 10 *MW* modular power converter and considering different topologies.

Table 7.5: Summary of representative solutions properties.

Topology	B2B3p		B2B3pSq		DMC	RMC
	VSg	VStr	VSg	VStr(U,L)*		
n_p	1	2	1	(4, 2)	1	2
$I_{npm}\,(kA)$	2	2.69	2	(3.1, 3.1)	2.3	2.8
N_{sw}	6	6	6	(3, 3)	18	12
$\bar{C}_{PM}$	73.8		56.1		103.4	74.8
n_s	17		19		17	17
$I_{nD}\,(A)$	43.1		80.4		28.7	64.7
$\bar{C}_{FBD}$	35.2		36.6		35.2	23.4
N_m	6		3		9	4
$f_{tr}\,(kHz)$	0.5		2.43		0.5	6.97
$P_{Loss}\,[\%]$	4.17		2.92		4.12	1.95
$Vol_{Total}\,(m^3)$	16.79		15.9		15.38	13.18
$Mass_{Total}\,(t)$	11.87		14.58		12.75	14.87
Λ	5.9		5.18		5.8	4.24

**VSg: VSI gen. side; VStr: VSI transf. side; U: upper switches; L: lower switches.*

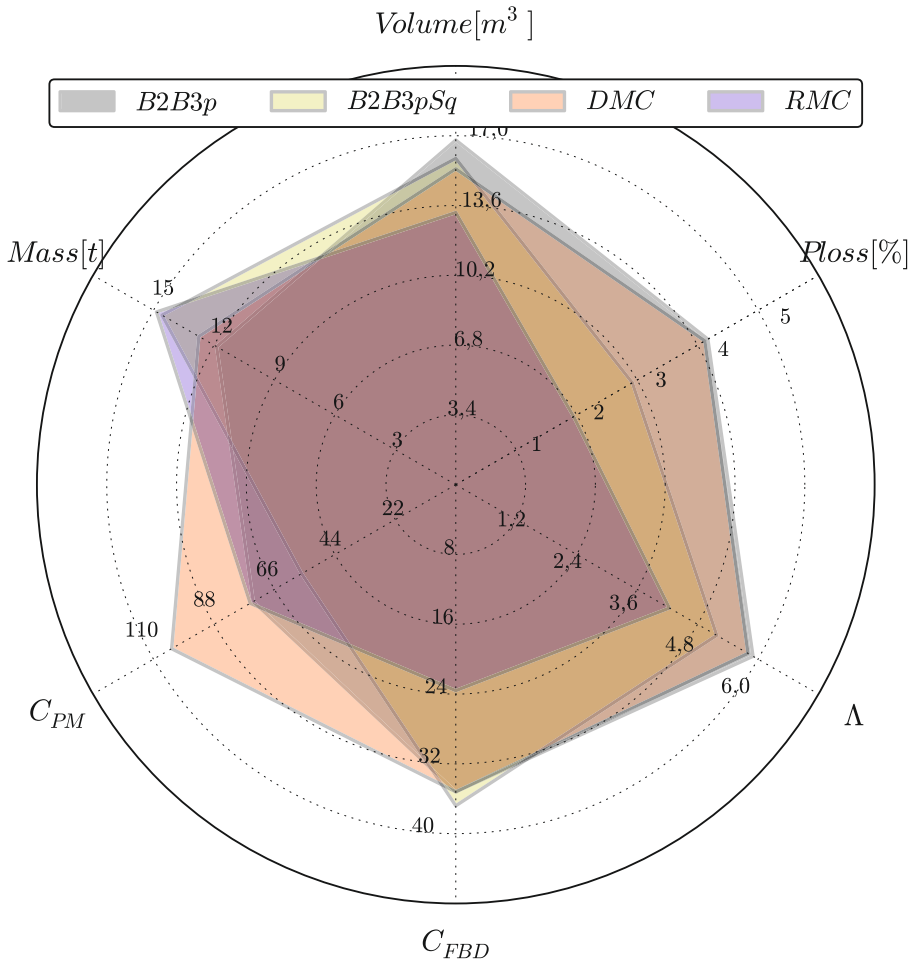


Figure 7.25: Comparison of the representative solutions using six performance indicators.

Chapter 8

Conclusions

In this thesis, a meta-parametrised approach and main component meta-modelling were used to evaluate the power loss, volume and mass of the high power WECS [12, 13, 15]. Although the proposed method has been designed for an offshore wind energy system, it is applicable to a wide variety of systems based on power electronics components, such as automotive electric conversion system, smart grid systems and renewable energy applications such as, inter alia, wind, wave and solar energy systems. The method has been designed with flexibility to be able to integrate the properties of new semiconductor devices such as wideband gap (Silicon Carbide, Gallium Nitride) and/or new materials such different core materials for transformers.

In the proposed method, the system is first characterised, then a set of figures of merits are evaluated for a set of design parameters. Finally, a multi-objective optimisation is performed and the Pareto concept is used to present the set of solutions (for different sets of parameters) to identify the best trade-off of the performance indicators. Therefore, the approach does not identify a unique solution; instead, a set of solutions are obtained and other criteria can be used to choose the final solution, thus giving freedom in the design process and flexibility in the final decision.

8.1 Comparative Study of WECS Based on a Medium Frequency AC-Link for Offshore DC-Grids

In chapter 7, the approach presented in this thesis and required to evaluate the power losses, volume and mass of six different WECS based on MFT with the scheme of Figure 7.3 was applied to compare B2B3p, B2B3pSq, B2B1p, DMC,

IMC and RMC topologies in the AC-AC converter stage for a 10 MW WECS with a PMSG that is suitable for offshore DC-grids. A modular approach in the power converter was considered and the impact of the number of modules on variation in the performance indicators was studied.

All six AC-AC converters are designed to be connected to a PMSG with a line-to-line voltage of 3x690 V *(RMS)*, 50 Hz and a power factor of 0.9 at nominal operation. Three performance indicators (power losses, volume and mass) are investigated for an AC-link frequency in the range of 500 Hz to 20 kHz. Furthermore, 1.7 kV IGBT4 modules and 3.3 kV diodes (Infineon) were used to obtain the main parameters of the semiconductor devices as a function of their nominal current. The semiconductor device cooling system was designed such that at nominal operation, the maximum junction temperature does not exceed 135 ^oC with a worst case scenario of 30K variation in maximum junction temperature. IGBT modules connected in parallel were considered and the main effects of this connection on power losses in the switches were determined.

The considered MFT design method takes into account different parameters. It was shown how these parameters vary according to the type of AC-AC converter topology. The magnetic alloy 2605SA1 from Metglas was considered to be the core material of the MFT; however, other magnetic materials can be considered in future studies applying the method presented here, because the volume/mass of the transformer at the lower frequencies of the range considered make up more than 60% of the total volume/mass (in most cases) and the use of amorphous or nano-crystalline core materials can improve the ρ of the MFT.

The modulation technique selected for each topology strongly affects the comparison because power losses of the converter depend on modulation. The most efficient modulation techniques for each topology were selected from previous work on the same application area (offshore DC-grid WTs connected in series). However, more efficient modulation techniques for the B2B3p topology have been reported in other types of application [46]. These techniques may be considered in future work to study further how the modulation technique affects the performance metrics considered in this thesis.

RMC topology was selected as the topology of the AC-AC converter in Figure 7.3 because it provides the most efficient solution for any frequency (within the considered AC-link frequency range of 500 Hz to 20 kHz) and number of modules connected. RMC topology results in more than 1.5 times lower power losses than B2B topologies based on a squared waveform and more than 2.6 times lower power losses than topologies based on an AC-link sinusoidal waveform (cf. Figure 7.15). Furthermore, it was shown that power converters with RMC topology produce the

most compact solution when more than one module is connected and the AC-link frequency is higher than 7 *kHz*. In general, an increase in frequency above 500 *Hz* reduces the total volume, but this behaviour is limited until around 3 *kHz* (except for RMC topology), above which the volume increases with frequency. This trend is more predominant for topologies with a sinusoidal waveform (cf. Figure 7.17), which require more switches connected in parallel and a bulky cooling system because of losses in the converter. RMC topology enables a 1.16 times lower volume than the lowest volume achieved with any other topology.

Although RMC topology produces the most efficient and compact solution, this topology also results in the heaviest solutions for frequencies below 4 *kHz*. Indeed, at frequencies above 4 *kHz,* RMC topology produces solutions with a 1.26 times higher mass than those of B2B3p topology, which is the topology that produces the lowest mass at low frequencies. Therefore, no unique solution exists that minimises all performance indicators.

Finally, the use of an additional indicator which quantifies the trade-off between the three performance indexes was suggested. Representative solutions for B2B3p, B2B3pSq, DMC and RMC topology, selected to minimise the suggested indicator, were compared. The representative solution based on RMC topology enables 41% less volume and 2.14 times lower losses than that based on B2B3p topology, although this solution has 1.25 times lower mass than the RMC solution. The DMC representative solution is 17% lighter than the RMC solution, but has 17% more volume and 2.1 times more losses. By contrast, the B2B3pSq representative solution enables only a 2% reduction in mass, despite having 20% more volume and 1.5 times more losses than the RMC solution. Furthermore, when two additional performance indicators regarding the cost of semiconductors in the AC-AC converter and the FBD were taken into account, the RMC solution enabled around a 50% reduction in the cost of FBD devices compared to the other topologies. The cost of the IGBT modules for the RMC solution was approximately equal to, 1.38 times lower than and 1.33 times higher than that for the B2B3p, DMC and B2B3pSq solutions, respectively (cf. Figure 7.25). From the perspective of the considered performance indicators, the RMC clearly is the preferred choice for WT modular converters based on a medium frequency AC-link with the Metglas alloy 2605SA1 as the core material of the MFT and the system parameters considered in chapter 7. However, the total cost of the converter and the reliability and complexity of the considered solutions may influence the obtained conclusion, and these performance indicators should be taken into account in future work to obtain the most generalised conclusion.

8.2 Future work

Some of the possible applications for the proposed approach are:

- To determine partially, the best solutions for a new application regarding state-of-the-art converter topologies, modulation strategies, component technologies and system parameters.
- To detect key components/parameters to optimise a standard solution.
- To quantify the impact of a new component technology on the state-of-the-art solutions for a given application.

Although power switch valves based on IGBT semiconductors were considered in the present research, the models can be easily extended to include other types of semiconductors like IGCT, MOSFET or JFET. Given that detailed models including parameters to quantify the effects of parallel connection of semiconductors were used, low rating devices connected in parallel can be considered. Moreover, the model also includes devices connected in series, which ensure that the voltage rating of the application is reached. These hybrid models can identify the most relevant semiconductor parameters in a given application and assign them as inputs/requirements for the development of future or new types of semiconductor devices.

Furthermore, the simplified design process of the MFT developed in the present research can be used in future research because the MFT is the most important component in the Solid State Transformer (SST), which is the key component in most applications with insulated DC/DC converters, like future power distribution systems interfacing energy storage systems, VAR compensation, harmonic filtering and voltage conversion (renewable energy systems interfaced by SST). The use of new core materials in combination with new semiconductor devices can also be investigated and the synergistic effect of their combination will enable the creation of new compact and high η solutions leading to a major breakthrough in this field.

Bibliography

[1] S. Meier, T. Kjellqvist, S. Norrga, and H. P. Nee, "Design considerations for medium-frequency power transformers in offshore wind farms," in *13th European Conference on Power Electronics and Applications, 2009. EPE '09*. IEEE, Sep. 2009, pp. 1–12. (document), 1, 5.1, 5.2, 5.4, 7.1, 7.4

[2] J. W. Kolar, J. Biela, S. Waffler, T. Friedli, and U. Badstuebner, "Performance trends and limitations of power electronic systems," in *2010 6th International Conference on Integrated Power Electronics Systems (CIPS)*. IEEE, Mar. 2010, pp. 1–20. (document), 1, 2.1, 2.1, 2.2, 2.3, 2.3

[3] M. Liserre, R. Cardenas, M. Molinas, and J. Rodriguez, "Overview of Multi-MW Wind Turbines and Wind Parks," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 4, pp. 1081–1095, Apr. 2011. 1

[4] A. Garces Ruiz, "DESIGN, OPERATION AND CONTROL OF SERIES-CONNECTED POWER CONVERTERS FOR OFFSHORE WIND PARKS," dissertation, Norwegian University of Science and Technology, 2012, oFFSHORE wind farms need to develop technologies that fulfill three main objectives:Efficiency, power density and reliability. The purpose of this thesisis to study an HVDC transmission system base ... [Online]. Available: http://ntnu.diva-portal.org/smash/record.jsf?pid=diva2:541812 1, 7.1, 7.3.2

[5] S. Gjerde, P. Olsen, K. Ljokelsoy, and T. Undeland, "Control and Fault Handling in a Modular Series-Connected Converter for a Transformerless 100 kV Low-Weight Offshore Wind Turbine," *IEEE Transactions on Industry Applications*, vol. 50, no. 2, pp. 1094–1105, Mar. 2014. 1, 7.1

[6] N. Holtsmark, H. Bahirat, M. Molinas, B. Mork, and H. Hoidalen, "An All-DC Offshore Wind Farm With Series-Connected Turbines: An Alternative

to the Classical Parallel AC Model?" *IEEE Transactions on Industrial Electronics*, vol. 60, no. 6, pp. 2420–2428, Jun. 2013. 1, 7.1, 7.1, 7.2

[7] J. W. Kolar, J. Biela, and J. Minibock, "Exploring the pareto front of multi-objective single-phase PFC rectifier design optimization - 99.2% efficiency vs. 7kw/din3 power density," in *Power Electronics and Motion Control Conference, 2009. IPEMC '09. IEEE 6th International*. IEEE, May 2009, pp. 1–21. 1

[8] J. Knowles and H. Nakayama, "Meta-Modeling in Multiobjective Optimization," in *Multiobjective Optimization*, J. Branke, K. Deb, K. Miettinen, and R. Slowinski, Eds. Berlin, Heidelberg: Springer Berlin Heidelberg, 2008, vol. 5252, pp. 245–284. [Online]. Available: http://www.springerlink.com/content/w018jnj76p556209/export-citation/ 1

[9] J. Biela, U. Badstuebner, and J. W. Kolar, "Impact of Power Density Maximization on Efficiency of DC/DC Converter Systems," *IEEE Transactions on Power Electronics*, vol. 24, no. 1, pp. 288–300, Jan. 2009. 1

[10] Hayashi, K. Takao, T. Shimizu, and H. Ohashi, "An effective design method for high power density converters," in *Power Electronics and Motion Control Conference, 2008. EPE-PEMC 2008. 13th*, Sep. 2008, pp. 2445 –2451. 1

[11] D. Huang, D. Gilham, W. Feng, P. Kong, D. Fu, and F. C. Lee, "High power density high efficiency dc/dc converter," in *2011 IEEE Energy Conversion Congress and Exposition (ECCE)*. IEEE, Sep. 2011, pp. 1392–1399. 1

[12] R. Barrera-Cardenas and M. Molinas, "Comparative Study of Wind Turbine Power Converters Based on Medium Frequency AC-Link for Offshore DC-Grids," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. PP, no. 99, pp. 1–1, 2014. 1.4, 8

[13] ——, "Multi-objective Design of a Modular Power Converter based on Medium Frequency AC-link for Offshore DC Wind Park," *Energy Procedia*, vol. 35, pp. 265–273, 2013. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S1876610213012654 1.4, 7.1, 8

[14] ——, "Optimal LQG Controller for Variable Speed Wind Turbine Based on Genetic Algorithms," *Energy Procedia*, vol. 20, pp. 207–216, 2012. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S1876610212007515 1.4

[15] ——, "A Simple Procedure to Evaluate the Efficiency and Power Density of Power Conversion Topologies for Offshore Wind Turbines,"

Energy Procedia, vol. 24, pp. 202–211, 2012. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S1876610212011423 1.4, 8

[16] ——, "A comparison of WECS based on medium frequency AC-link for offshore DC Wind Park," in *PowerTech (POWERTECH), 2013 IEEE Grenoble*, 2013, pp. 1–7. 1.4

[17] ——, "Wind energy conversion systems for DC-series based HVDC transmission," in *XV ERIAC - CIGRE*. Foz do IguazÃº, Brazil: CIGRE, May 2013. [Online]. Available: http://www.cigre.org.br 1.4

[18] ——, "Comparison of wind energy conversion systems based on high frequency AC-Link: Three-phase Vs. single-phase," in *Power Electronics and Motion Control Conference (EPE/PEMC), 2012 15th International*, Sep. 2012, pp. LS2c.4–1 –LS2c.4–8. 1.4

[19] ——, "Optimized design of wind energy conversion systems with single-phase AC-link," in *2012 IEEE 13th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Jun. 2012, pp. 1 –8. 1.4

[20] ——, "Comparative study of the converter efficiency and power density in offshore wind energy conversion system with single-phase transformer," in *2012 International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM)*, Jun. 2012, pp. 1085 –1090. 1.4

[21] R. Barrera-Cardenas, N. Holtsmark, and M. Molinas, "Comparative study of the efficiency and power density of offshore WECS with three-phase AC-link," in *2012 3rd IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, Jun. 2012, pp. 717 –724. 1.4

[22] J. Van Sickel, P. Venkatesh, and K. Lee, "Analysis of the pareto front of a multi-objective optimization problem for a fossil fuel power plant," in *2008 IEEE Power and Energy Society General Meeting - Conversion and Delivery of Electrical Energy in the 21st Century*, Jul. 2008, pp. 1–8. 2.2

[23] M. Li, S. Yang, and X. Liu, "Diversity Comparison of Pareto Front Approximations in Many-Objective Optimization," *IEEE Transactions on Cybernetics*, vol. 44, no. 12, pp. 2568–2584, Dec. 2014. 2.2

[24] D. Xu, H. Lu, L. Huang, S. Azuma, M. Kimata, and R. Uchida, "Power loss and junction temperature analysis of power semiconductor devices," *IEEE Transactions on Industry Applications*, vol. 38, no. 5, pp. 1426– 1431, Oct. 2002. 3.1.1

[25] M. Mirjafari and R. Balog, "Survey of modelling techniques used in optimisation of power electronic components," *IET Power Electronics*, vol. 7, no. 5, pp. 1192–1203, May 2014. 3.1.1, 4.2.3

[26] Infineon, "Technical information IGBT-modules FZ1500r33he3," Infineon, Datasheet FZ1500R33HE3, 2013. [Online]. Available: http://www.infineon.com/ 3.1.1, 3.1.2

[27] F. E. Co., "Fuji IGBT Modules application manual," May 2011. [Online]. Available: http://www.fujielectric.com 3.2, 3.2, 3.2, 3.3

[28] A. Volke and M. Hornkamp, *IGBT Modules: Technologies, driver and application.*, 2nd ed. Munich, Germany: Infineon Technologies AG, 2012. [Online]. Available: http://www.infineon.com 3.3

[29] B. Backlund, M. Rahimo, S. Klaka, and J. Siefken, "Topologies, voltage ratings and state of the art high power semiconductor devices for medium voltage wind energy conversion," in *IEEE Power Electronics and Machines in Wind Applications, 2009. PEMWA 2009.* IEEE, Jun. 2009, pp. 1–6. 3.3, 6.3.1, 6.3.1, 6.3.3

[30] B. Wen, D. Boroyevich, and P. Mattavelli, "Investigation of tradeoffs between efficiency, power density and switching frequency in three-phase two-level PWM boost rectifier," in *Proceedings of the 2011-14th European Conference on Power Electronics and Applications (EPE 2011).* IEEE, Aug. 2011, pp. 1–10. 3.4, 6.5

[31] U. Drofenik and J. W. Kolar, "A General Scheme for Calculating Switching- and Conduction-Losses of Power Semiconductors in Numerical Circuit Simulations of Power Electronic Systems," in *Proceedings of the 2005 International Power Electronics Conference*, Niigata, Japan, 2005, pp. 4–8. [Online]. Available: https://www.pes.ee.ethz.ch/uploads/tx_ethpublications/drofenik_id356_IPEC05.pdf 3.4

[32] K. Lee, K. Jung, Y. Suh, C. Kim, H. Yoo, and S. Park, "Comparison of high power semiconductor devices losses in 5mw PMSG MV wind turbines," in *2014 Twenty-Ninth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2014, pp. 2511–2518. 3.5, 6.5

[33] M. Preindl and S. Bolognani, "Optimized design of two and three level full-scale voltage source converters for multi-MW wind power plants at different voltage levels," in *IECON 2011 - 37th Annual Conference on IEEE Industrial Electronics Society*. IEEE, Nov. 2011, pp. 3634–3639. 3.5, 4.1.3, 6, 6.5, 7.1

[34] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics: Converters, Applications, and Design*, 3rd ed. Wiley, Oct. 2002. 4.1.1, 4.1.2, 5.2, 6.1

[35] C. Sullivan, "Optimal choice for number of strands in a litz-wire transformer winding," *IEEE Transactions on Power Electronics*, vol. 14, no. 2, pp. 283–291, Mar. 1999. 4.1.3, 4.1.3, 4.1.3

[36] W.-J. Gu and R. Liu, "A study of volume and weight vs. frequency for high-frequency transformers," in *Power Electronics Specialists Conference, 1993. PESC '93 Record., 24th Annual IEEE*, Jun. 1993, pp. 1123 –1129. 4.1.3, 5.1, 5.1

[37] W. Hurley, E. Gath, and J. Breslin, "Optimizing the AC resistance of multilayer transformer windings with arbitrary current waveforms," *IEEE Transactions on Power Electronics*, vol. 15, no. 2, pp. 369–376, Mar. 2000. 4.1.3, 5.2

[38] W. G. Hurley, W. H. Wolfle, and J. G. Breslin, "Optimized transformer design: inclusive of high-frequency effects," *IEEE Transactions on Power Electronics*, vol. 13, no. 4, pp. 651–659, Jul. 1998. 4.1.4, 5.1, 5.2, 5.2, 5.3, 5.4

[39] TDK, "EPCOS Product Profile 2012, Power Capacitors for Industrial Applications and Renewable Energy," 2012. [Online]. Available: www.tdk-epc.com 4.2.2, 4.2.3, 4.2.3, 4.2.3

[40] M. Mirjafari and R. Balog, "Multi-objective design optimization of renewable energy system inverters using a Descriptive language for the components," in *2011 Twenty-Sixth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2011, pp. 1838–1845. 4.2.3

[41] EPCOS, "Installation and maintenance instructions for PFC capacitors," 2009. [Online]. Available: http://www.epcos.com 4.2.3

[42] W. G. Hurley, "Optimizing core and winding design in high frequency transformers," in *Power Electronics Congress, 1996. Technical Proceedings. CIEP '96., V IEEE International*. IEEE, Oct. 1996, pp. 2–13. 5.1, 5.3

[43] R. A. Jabr, "Application of geometric programming to transformer design," *IEEE Transactions on Magnetics*, vol. 41, no. 11, pp. 4261– 4269, Nov. 2005. 5.2, 5.3

[44] C. Versele, O. Deblecker, and J. Lobry, "Multiobjective optimal design of transformers for isolated switch mode power supplies," in *2010 International Symposium on Power Electronics Electrical Drives Automation and Motion (SPEEDAM)*. IEEE, Jun. 2010, pp. 1687–1692. 5.2

[45] J. Chivite-Zabalza, C. Girones, A. Carcar, I. Larrazabal, E. Olea, and M. Zabaleta, "Comparison of power conversion topologies for a multi-megawatt off-shore wind turbine, based on commercial Power Electronic Building Blocks," in *IECON 2013 - 39th Annual Conference of the IEEE Industrial Electronics Society*, Nov. 2013, pp. 5242–5247. 6

[46] L. Helle, "Modeling and Comparison of Power Converters for Doubly Fed Induction Generators in Wind Turbines," info:eu-repo/semantics/doctoralThesis, publishedVersion, Institut for Energiteknik, Aalborg Universitet, 2007. 6.1, 6.1, 6.2, 6.2, 6.2, 6.5, 7.2, 7.2.1, 7.6, 8.1

[47] J. Kolar, H. Ertl, and F. C. Zach, "Influence of the modulation method on the conduction and switching losses of a PWM converter system," *IEEE Transactions on Industry Applications*, vol. 27, no. 6, pp. 1063–1075, Nov. 1991. 6.1, 6.1, 6.2, 6.2, 6.5

[48] R. Lai, F. Wang, R. Burgos, Y. Pei, D. Boroyevich, B. Wang, T. Lipo, V. Immanuel, and K. Karimi, "A Systematic Topology Evaluation Methodology for High-Density Three-Phase PWM AC-AC Converters," *IEEE Transactions on Power Electronics*, vol. 23, no. 6, pp. 2665–2680, Nov. 2008. 6.3.1, 7.2.1

[49] J. Kolar and S. Round, "Analytical calculation of the RMS current stress on the DC-link capacitor of voltage-PWM converter systems," *Electric Power Applications, IEE Proceedings* -, vol. 153, no. 4, pp. 535–543, Jul. 2006. 6.3.1, 6.3.1, 6.3.1

[50] T. Friedli, J. Kolar, J. Rodriguez, and P. Wheeler, "Comparative Evaluation of Three-Phase AC-AC Matrix Converter and Voltage DC-Link Back-to-Back Converter Systems," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 12, pp. 4487–4510, Dec. 2012. 6.3.2, 6.5, 7.2, 7.2.1, 7.3.1, 7.3.1

[51] C. Meyer, M. Hoing, A. Peterson, and R. De Doncker, "Control and Design of DC Grids for Offshore Wind Farms," *IEEE Transactions on Industry Applications*, vol. 43, no. 6, pp. 1475–1482, Nov. 2007. 7.1

[52] W. Chen, A. Q. Huang, C. Li, G. Wang, and W. Gu, "Analysis and Comparison of Medium Voltage High Power DC/DC Converters for Offshore Wind Energy Systems," *IEEE Transactions on Power Electronics*, vol. 28, no. 4, pp. 2014–2023, Apr. 2013. 7.1

[53] F. Deng and Z. Chen, "Control of Improved Full-Bridge Three-Level DC/DC Converter for Wind Turbines in a DC Grid," *IEEE Transactions on Power Electronics*, vol. 28, no. 1, pp. 314–324, Jan. 2013. 7.1

[54] J. Robinson, D. Jovcic, and G. Joos, "Analysis and Design of an Offshore Wind Farm Using a MV DC Grid," *IEEE Transactions on Power Delivery*, vol. 25, no. 4, pp. 2164 –2173, Oct. 2010. 7.1

[55] L. MAX, "Design and Control of a DC Collection Grid for a Wind Farm," THESIS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY, CHALMERS UNIVERSITY OF TECHNOLOGY, Sweden, 2009. [Online]. Available: http://webfiles.portal.chalmers.se/et/PhD/MaxLenaPhD.pdf 7.1, 7.2.3, 7.2.3, 7.6

[56] L. Max and S. Lundberg, "System efficiency of a DC/DC converter-based wind farm," *Wind Energy*, vol. 11, no. 1, pp. 109–120, Jan. 2008. [Online]. Available: http://onlinelibrary.wiley.com/doi/10.1002/we.259/abstract 7.1, 7.2.3

[57] C. Meyer, *Key Components for Future Offshore DC Grids*. Shaker, 2007. 7.1

[58] S. Lundberg, "Wind Farm Configuration and Energy Efficiency Studies - Series DC versus AC Layouts," Doctoral thesis, Chalmers University of Technology, 2006. [Online]. Available: http://publications.lib.chalmers.se 7.1

[59] A. Garces and M. Molinas, "A Study of Efficiency in a Reduced Matrix Converter for Offshore Wind Farms," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 1, pp. 184–193, Jan. 2012. 7.1, 7.3.2, 7.3.3, 7.6

[60] A. Mogstad, M. Molinas, P. Olsen, and R. Nilsen, "A power conversion system for offshore wind parks," in *34th Annual Conference of IEEE Industrial Electronics, 2008. IECON 2008*, Nov. 2008, pp. 2106–2112. 7.1

[61] N. Holtsmark and M. Molinas, "Thermal analysis of matrix and Back-To-Back converters for series-connected wind turbines," in *IECON 2013 - 39th Annual Conference of the IEEE Industrial Electronics Society*, Nov. 2013, pp. 4967–4972. 7.1

[62] E. Veilleux and P. Lehn, "Interconnection of Direct-Drive Wind Turbines Using a Series-Connected DC Grid," *IEEE Transactions on Sustainable Energy*, vol. 5, no. 1, pp. 139–147, Jan. 2014. 7.1

[63] H.-J. Lee and S.-K. Sul, "Wind power collection and transmission with series connected current source converters," in *Proceedings of the 2011-14th European Conference on Power Electronics and Applications (EPE 2011)*, Aug. 2011, pp. 1–10. 7.1

[64] S. Nishikata and F. Tatsuta, "A New Interconnecting Method for Wind Turbine/Generators in a Wind Farm and Basic Performances of the Integrated System," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 2, pp. 468–475, Feb. 2010. 7.1

[65] M. R. Hanssen, A. G. Ruiz, and M. Molinas, "Operation features of a reduced matrix converter for offshore wind power," in *2010 IEEE International Symposium on Industrial Electronics (ISIE)*. IEEE, Jul. 2010, pp. 2443–2448. 7.1

[66] J. Esteban, "Study and design of a DC/DC converter for series connected wind farms," Master's Thesis, 2005. [Online]. Available: http://studentarbeten.chalmers.se 7.1

[67] A. Garces and Molinas, M., "Electrical conversion system for offshore wind turbines based on high frequency ac link," in *IX International Conference and Exhibition of Renewal Energy and Ecological Vehicles EVER2009*, Monaco, Mar. 2009. 7.1

[68] "Clipper Windpower - Wind Turbine Manufacturer," 2011. [Online]. Available: http://clipperwind.com/ 7.1

[69] M. hamouda, F. Fnaiech, and K. Al-Haddad, "Input filter design for SVM Dual-Bridge Matrix Converters," in *2006 IEEE International Symposium on Industrial Electronics*, vol. 2. IEEE, Jul. 2006, pp. 797–802. 7.2.2

[70] C. Versele, O. Deblecker, and J. Lobry, "Multiobjective optimal choice and design of isolated dc-dc power converters," in *Power Electronics and Applications (EPE 2011), Proceedings of the 2011-14th European Conference on*, Sep. 2011, pp. 1 –10. 7.2.3

[71] C. P. Dick, A. Konig, and R. W. De Doncker, "Comparison of Three-Phase DC-DC Converters vs. Single-Phase DC-DC Converters," in *7th International Conference on Power Electronics and Drive Systems, 2007. PEDS '07*. IEEE, Nov. 2007, pp. 217–224. 7.2.4

[72] N. Holtsmark and M. Molinas, "Matrix converter efficiency in a high frequency link offshore WECS," in *IECON 2011 - 37th Annual Conference on*

IEEE Industrial Electronics Society. IEEE, Nov. 2011, pp. 1420–1425. 7.3.1, 7.6

[73] ——, "Matrix converter modulation for series-connected wind turbines with high frequency link," in *IECON 2013 - 39th Annual Conference of the IEEE Industrial Electronics Society*, Nov. 2013, pp. 4880–4885. 7.3.1, 7.6

[74] A. Garces and M. Molinas, "Comparative investigation of losses in a reduced matrix converter for off-shore wind turbines," in *5th IET International Conference on Power Electronics, Machines and Drives (PEMD 2010)*. IET, Apr. 2010, pp. 1–6. 7.3.2

[75] P. W. Wheeler, J. Rodriguez, J. C. Clare, L. Empringham, and A. Weinstein, "Matrix converters: a technology review," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 2, pp. 276–288, Apr. 2002. 7.3.3