A Two-stage Area-efficient High Input Impedance CMOS Amplifier for Neural Signals

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***Abstract*—In this article, a two-stage area-efficient high input impedance neural amplifier is proposed. It has been shown that two single-stage amplifiers with low gain will consume less area in comparison with a single-stage high gain amplifier for capacitively coupled amplifiers. Besides, splitting a high gain amplifier into two single-stages in this structure leads to achieving a higher input impedance at the end. Furthermore, it helps to boost the input impedance at a higher frequency. The robustness of the proposed structure is investigated by process and mismatch Monte Carlo simulations. All the simulations are run using in a commercially available 0.18 µm CMOS technology. Based on post-layout simulation, the proposed two-stage amplifier has 53 dB mid-band gain in the bandwidth of 5 Hz to 10 kHz. The input impedance is 2.8 GΩ and 56 MΩ at 1 kHz and 10 kHz, respectively. In comparison to a single-stage amplifier, the proposed structure boosted the input impedance at frequencies up to 1 kHz by a factor of 10 while the power consumption increased only 0.5 µW. Furthermore, the proposed two-stage neural amplifier area consumption is 0.02 mm^2 without pads which decreased area consumption by a factor of 3.**

***Index Terms*—High input impedance, Area efficient, neural amplifier, low power, low noise**

I. Introduction

The importance of neural interfaces is increasing rapidly. Nowadays, their importance is not limited only to diagnosis and treatment, they are also used for various BCI applications and even for entertainment. Neural signals have frequency up to 10 kHz and magnitude up to few millivolts. For instance, action potential signal frequency is up to 10 kHz while their amplitude is approximately up to a few hundred microvolts [1].

Area consumption is one of the important parameters in designing an integrated circuit since it affects the cost of production. CMOS (complementary metal-oxide-semiconductor) technologies helped to put more transistors in a single die. For implantable devices and specially high-density neural application, the maximum area consumption is stringent [2].

The other important parameter for neural applications is their input impedance. Limited input impedance causes signal attenuation. Especially for neural signals with very limited amplitude, a little attenuation might lead to signal loss. Therefore, it is necessary to have a very high input impedance to capture signals with the minimum signal attenuation [3].

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Capacitively-coupled amplifiers (CCAs) have been widely used to block input DC offset and many other nice properties. In this structure, most of the area is consumed by the input capacitors, even though the input transistors usually have large W and L to minimize flicker noise. For a higher closed-loop gain, the input capacitors become more dominant. The input impedance of CCAs is limited to the input capacitor. Larger input capacitor means lower input impedance [2]. It is worth mentioning that very small input capacitor will increase input-referred noise which be discussed in the next section. Therefore, the input capacitors is usually in the range of a few picofarads.

Therefore, a positive feedback loop [4] and auxiliary path [5] are proposed to boost the input impedance. In [6], it was shown that the boosted input impedance factor decreases for high frequencies and it is related to bandwidth of the open-loop amplifier. For single-stage amplifiers, there is not so much freedom to increase the bandwidth of the amplifier to achieve better input impedance boosting.

In this article, a two-stage amplifier is proposed to divide the gain into two low-gain stages. First, a single-stage CCA is analyzed in the system overview section. Then, based on the challenges of a single-stage CCA, the proposed technique is discussed in terms of with its advantages and disadvantages with possible solutions in the proposed technique section. To illustrate the advantages and disadvantages of the proposed technique, both single-stage, and two-stage amplifiers are simulated and compared with each other in the simulation section. Finally, in the simulation section, the schematic and post-layout simulation are compared to demonstrate the effect of parasitic elements.

II. Systematic Overview

A single-stage CCA is shown in Fig. 1 with an additional positive feedback loop to boost the input impedance. The closed-loop gain of this structure can be approximated by Eq. 1 and the input impedance is defined as Eq. 2 without C_{pf}.

$$A_{CL} = \frac{C_{in}}{C_f} \tag{1}$$

$$Z_{in} \approx 1/sC_{in} \tag{2}$$

For applications with a very low amplitude input signal, a high gain amplifier is required before converting the signal to the digital domain. Higher gain requires larger C_{in}. Mostly the area of a single-stage CCA is occupied with C_{in} when the gain is large even with the large W and L. Consequently,

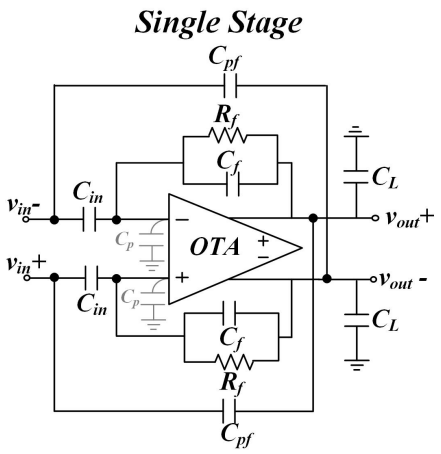

Fig. 1. A single-stage capacitively-coupled neural amplifier with an input impedance boosting loop.

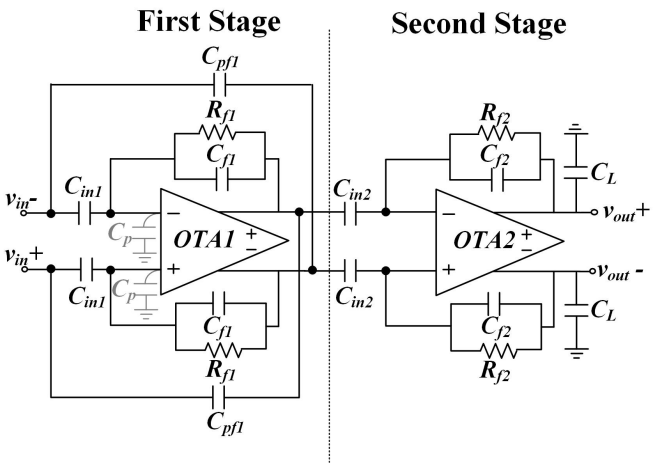

Fig. 2. A two-stage capacitively-coupled amplifier.

Larger C_{in} decreases the input impedance as it is shown in Eq. 2.

Neural signal frequency is up to 10 kHz [1]. In such a low frequency, the flicker noise is dominant. To minimize the flicker noise of amplifier, W and L of the input transistors should be relatively large. It means that the parasitic capacitor which has been shown in Fig. 1 will be large which will affect the total input-referred noise of the amplifier according to Eq. 3.

$$V_{ni,amp}^2 = (\frac{C_{in} + C_f + C_p}{C_{in}})^2 V_{ni}^2 \tag{3}$$

where V_{ni}^2 indicate total input-referred noise of the operational transconductance amplifier (OTA). The input impedance transfer function before utilizing positive feedback has a single pole at DC frequency as it is shown in Eq. 2. In the transfer function, exploiting a positive feedback loop adds a zero at the lower cut-off frequency of the amplifier as shown in Eq. 4 if the input of the amplifier is considered a virtual ground. It means that the input impedance is expected to be constant after the lower cut-off frequency.

$$Z_{in} = \frac{1 + sR_fC_f}{sC_{in}} \tag{4}$$

In practice, the input impedance starts to decrease after a definite frequency [4]. Therefore the more accurate transfer function of the boosted input impedance can be derived according to Eq. 5 by considering signal at the input nodes of the amplifier where the $A(s)$ is the transfer function of the open-loop amplifier and $Z_f(s)$ is the parallel impedance of R_f and C_f. Besides, it can be shown that the second pole in the transfer function which decreases input impedance is approximately equal to Eq. 6 [6].

$$Z_{in} = \approx \frac{1}{sC_{in}} \frac{1 + A(s) + sC_{in}Z_f}{1 + A(s)(1 - sC_{pf}Z_f)} \tag{5}$$

$$\omega_{p2} \approx \frac{-(R_LC_L + R_fC_f)}{R_LC_LR_fC_f} \tag{6}$$

where R_L is the output impedance of the open-loop amplifier. This frequency is dependent on the output pole of the open-loop amplifier. Besides the closed-loop upper cut-off is according to Eq. 7 where β is the feedback gain, f_{OU} is the open-loop upper cut-off frequency which is equal to $1/2\pi R_LC_L$ and f_{CU} is the closed-loop upper cut-off frequency. If the open-loop gain is much higher than β, the A_{CL} will be equal to $1/\beta$. Therefore, for a definite gain and closed-loop bandwidth, there is not that much freedom to choose R_LC_L.

$$f_{CU} = (1 + A(s)\beta)f_{OU} \tag{7}$$

III. PROPOSED TECHNIQUE

In this section, the proposed technique is explained with its advantages and disadvantages. First, the advantages are described. After that, the disadvantages are discussed in detail and for each challenge, a solution is presented.

A. Advantages

Adding a second stage as it is shown in Fig. 2 can help to divide a high gain into two low-gain stages to minimize the required input capacitor value. For instance, instead of having a gain of 400, this gain can be achieved by dividing it into two stages with a gain of 20. If the input capacitors are completely dominant, the area consumption drops from 400x to (20x + 20x) when x is the area consumption of single capacitors. Therefore, the area will be reduced by a factor of 10 by this technique. Besides, the input impedance is expected to be improved by a factor of 20 according to Eq. 2 when there is no input impedance boosting loop.

C_L is mostly the dominant capacitor in these circuits which defines the bandwidth. In this structure, this capacitor is at the second stage output node. Therefore, the first stage has a wider bandwidth than before. Therefore, the proposed technique in this article provides the freedom to increase the bandwidth of

the first stage so that the boosted input impedance achieves higher input impedance at high frequencies.

B. Disadvantages and solutions

The first concern might be related to the transferred noise of the additional stage to the input nodes which might force the designer to consume much power in the second stage. But the second stage noise will be divided by the gain of the first stage to refer to the input. Therefore, the second stage does not need to consume that much power and it will not affect the total power consumption considerably. In addition, by allocating larger gain to the first stage, this problem will be alleviated.

The main disadvantage of the proposed systematic technique to boost the input impedance and reducing area consumption is related to the coefficient factor of input-referred noise in the input-referred noise equation as it is calculated in Eq. 3. By decreasing the input capacitors, the parasitic capacitor becomes dominant. Finally, the total input-referred noise of the two OTAs will be multiplied by a factor larger than one. Fortunately, the parasitic capacitor value can be minimized by utilizing a chopping technique after capacitors. Therefore, this problem can be alleviated by utilizing chopping in future work.

IV. Simulation Results

In the first sub section, the proposed amplifier is compared with two different single-stage amplifiers with the same load capacitor. One is with the same gain and the other one is with the same input capacitor. In the second subsection, the proposed amplifier is compared with state-of-the-art and the post-layout simulation is reported in this part.

A. Schematic analysis on single-stage and two-stage CCA

The proposed structure is compared with two single-stage amplifiers with different input capacitors in Table I, and the proposed two-stage amplifier has highest input impedance at all frequencies. The two-stage amplifier has a gain of 40 at the first stage and 10 at the second stage. It not only makes the second stage relaxed but also reduces the coefficient of the transferred input-referred noise in Eq. 3. They are all implemented in a commercially available 0.18 µm CMOS technology. Besides, all OTAs exploiting identical structure which is proposed in [7] as the first stage. In the second stage, the structure is the same but with different dimensions because of different biasing.

The input capacitor value defines input impedance at the low frequencies. Therefore, both the single-stage and the two-stage amplifiers have much higher input impedance. But as the frequency increases to 1 kHz, the effect of the second pole will be visible. Therefore, the input impedance of the proposed architecture is 10 and 3 times higher at 1 kHz and 10 kHz, respectively with even the same input capacitor (4 pF).

The input impedance versus frequency is depicted in Fig. 3. The green lines represent the input impedance of the single-stage amplifier with a 40 pF input capacitor while the red line is related to a single-stage amplifier with a 4 pF capacitor. Finally, the blue line represents the input impedance of the proposed structure which is higher than others at all frequencies. There are two lines with the same color which represent the input impedance at GV/A and dB scale.

TABLE I
Comparison between single-stage and proposed CCA

Parameters	single-stage Amp. (C_{in}=40 pF)	single-stage Amp. (C_{in}=4 pF)	Two-stage Amp. (C_{in}=4 pF)
Input Impedance (GΩ) @ 10 Hz	4.7	44	**44**
Input Impedance (GΩ) @ 100 Hz	4.5	20.5	**20.5**
Input Impedance (GΩ) @ 1k Hz	0.2	1.2	**2.2**
Input Impedance (GΩ) @ 10 kHz	0.01	0.02	**0.06**
Gain (V/V)	400	40	**400**
Bandwidth (Hz)	3-1.2k	2-7k	**3-10k**
Power (µW)	**1.32**	**1.32**	1.8
IR Noise (μV_{rms})	**2**	4	4.3
NEF	2.4	**2**	2.1
Area (mm^2)	0.068	**0.01**	0.019

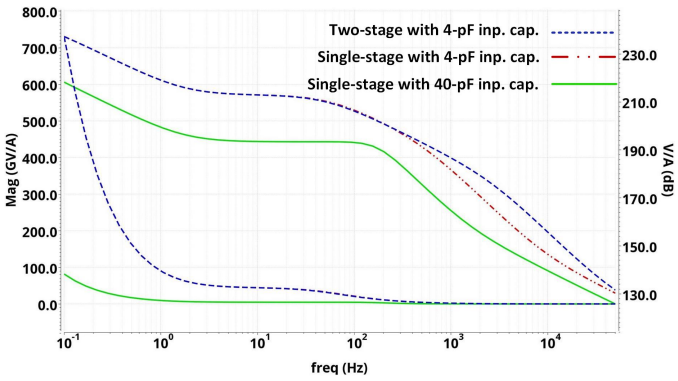

Fig. 3. Input impedance versus frequency for a single-stage with 4 pF and 40 pF input capacitor and two-stage amplifier with 4 pF input capacitor.

The area consumption is decreased by a factor of 3 whereas the power increased a little bit. NEF (noise efficiency factor) [8] is utilized as a figure of merit to combine noise, bandwidth, and current consumption to make a better comparison. The NEF shows that the proposed structure does not affect the noise efficiency of the system considerably and it is still in a relatively good range.

B. Post-layout simulation result

The layout of the proposed structure is shown in Fig. 4. Due to the parasitic elements, the input impedance dropped by a factor of approximately 2 between 1 and 100 Hz as it is depicted in Fig. 5. The black line represents the input impedance after the post layout while the blue line represents the input impedance for schematic simulations.

The effect of process and mismatch for 500 runs on input impedance at 1 kHz is shown in Fig. 6. Approximately, for all frequencies, the deviation was less than 5% of the mean value which shows the robustness of this technique. This high

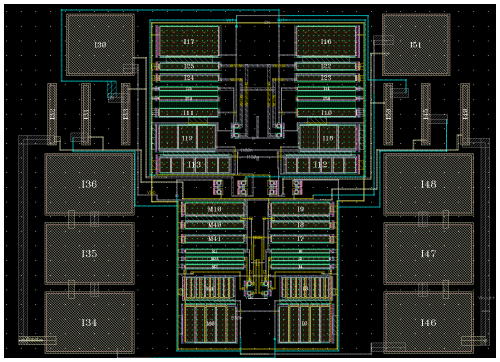

Fig. 4. The layout of the proposed neural amplifier (160 µm× 120 µm).

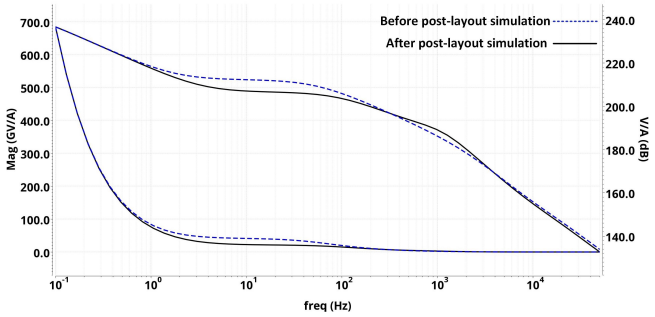

Fig. 5. The effect of parasitic elements on the input impedance of the proposed two-stage amplifier.

input impedance assures to boost the input signal for different electrode types with minimum signal attenuation.

Finally, the proposed work is compared with the state-of-the-art in Table II. The input impedance is much higher for the proposed technique in comparison with the state-of-the-art CCAs. Smaller input capacitor leads to higher input impedance, and lower capacitance at the output node of the first stage lead to wider bandwidth for boosting input impedance. Besides, the input-referred noise from 5 Hz to 200 Hz is 2.5 μV_{rms}. From 200 Hz to 10 kHz the total input-referred noise is 3.6 μV_{rms}. Thus, if the bandwidth of LFP and AP signals assumed to be equal to these frequencies, the

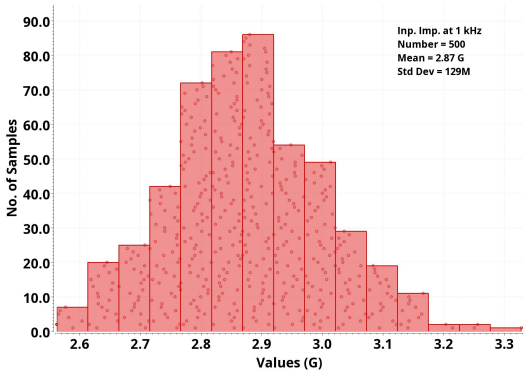

Fig. 6. The effect of process and mismatch on the input impedance variation at 1 kHz.

TABLE II
COMPARISON THE PROPOSED HIGH INPUT IMPEDANCE AMPLIFIER WITH THE STATE-OF-THE-ART CAPACITIVELY-COUPLED NEURAL AMPLIFIERS

Specs	[9]	[5]	[4]	This Work
Technology (nm)	180	40	180	180
Supply Voltage (V)	0.8	1.2	1.8	1.2
Power (µW)	0.29	2.8	19.8	1.8
Gain (dB)	34	25.7	40	53
Bandwidth (Hz)	1-400	1-5k	0.5-100	5-10 k
IR Noise (μV_{rms})	8.26	7.1	0.8	4.5
NEF	8.3	6.1	12.3	**2.1**
Input Impedance GΩ @ 100 Hz	10	1	0.05	**15**
Input Impedance GΩ @ 1k Hz	0.2	0.1	-	**2.8**
Area (mm^2)	1.9	0.069	6.5	**0.019**
Sim./Meas.	Meas.*	Meas.	Meas.	Post Layout Sim.

*With ADC and buffer

NEF in the bandwidth of LFP and AP signals is equal to 3.8 and 1.76, respectively.

V. CONCLUSION

The proposed amplifier is suitable for applications when input impedance and area consumption are stringent. The main idea is to divide a single-stage high gain amplifier into a two-stage amplifier. Accordingly, the area consumption will be decreased since the required capacitors will become smaller. In addition, the input capacitors define the input impedance. Therefore, the proposed systematic technique not only decreases the area consumption but also increases the input impedance. In the two-stage amplifier, the first stage can have much higher bandwidth which leads to much higher input impedance at high frequencies.

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