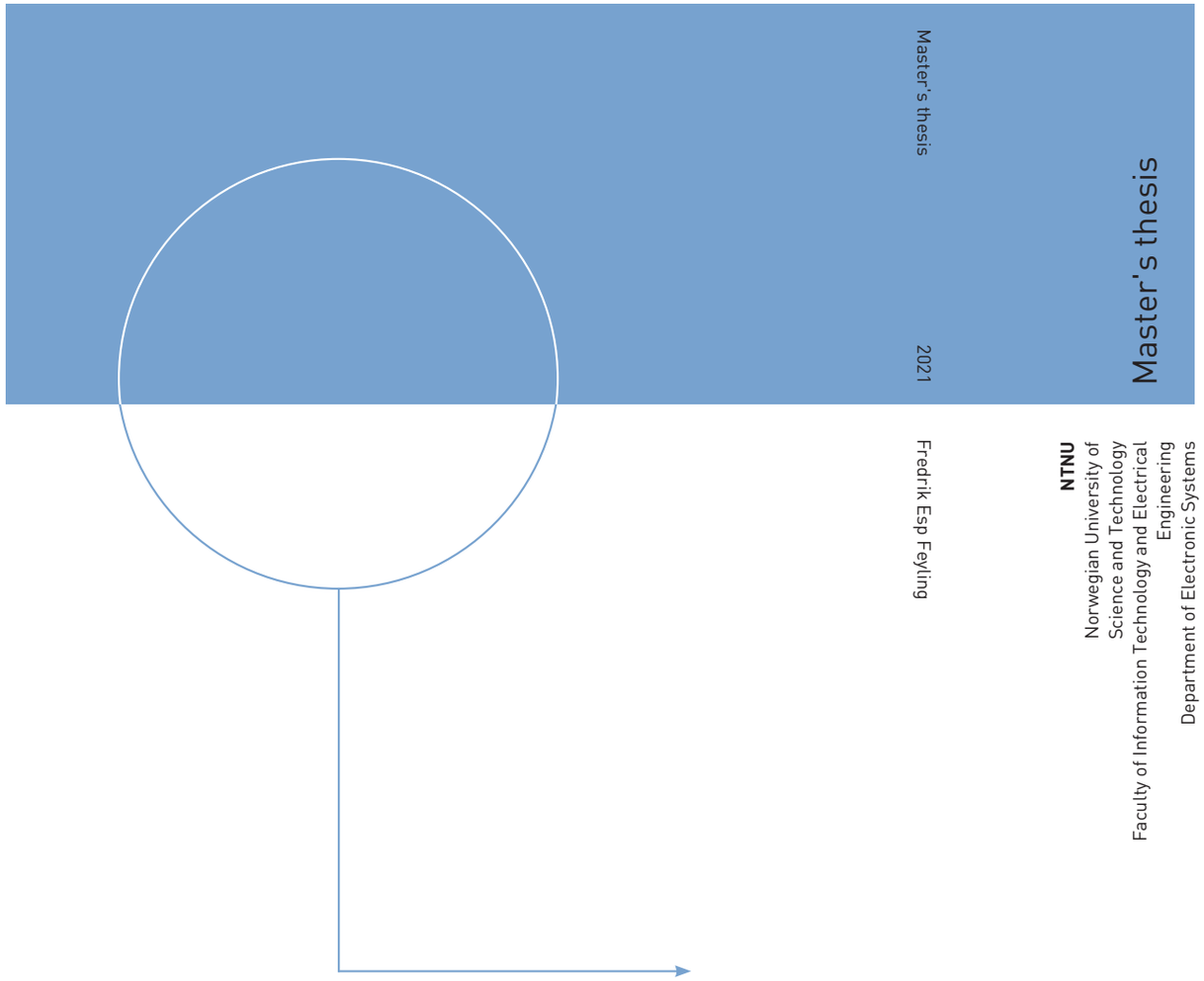

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Design Considerations for a Low-Power Control-Bounded A/D Converter

Fredrik Esp Feyling

Electronics Systems Design and Innovation
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Supervisor: Trond Ytterdal
Co-supervisor: Carsten Wulff

Norwegian University of Science and Technology
Department of Electronic Systems

Preface

First of all, I would like to thank my supervisors Professor Trond Ytterdal and Associate Professor Carsten Wulff for all the great support and guidance along the way. I am always looking forward to our meetings and I am very excited to continue this project as a Ph.D.-student under your supervision.

Secondly, I want to thank Dr. Hampus Malmberg for all the interesting and inspiring conversations throughout the year. Our collaboration have been an important motivational factor and this work would not have been possible without your support.

I would also like to thank David André Bjerkan Mikkelsen for your research and contributions on the implementation of the digital estimation filter and Christian Rosioara Steinsland for contributing on the python tools.

Abstract

Control-bounded analog-to-digital converter (ADC) is a recently introduced concept that approaches the conversion problem differently compared to most conventional ADC architectures. While the promising properties of the these converters have been studied on a theoretical level for a few years, no transistor level implementation have, to the author's knowledge, been reported so far.

In this thesis, we bring control-bounded conversion concept one step closer to a complete transistor level implementation. The established theoretical framework is expanded and applied in the analysis of the considered circuit implementations. A custom software library is developed, facilitating efficient design, simulation and evaluation of control-bounded converters. The theoretical analysis is supported by circuit simulations.

Rather than achieving a complete transistor-level implementation, the goal of this thesis is to explore possible low-power designs of a scalar control-bounded converter. The main result is therefore the overview of, and some possible solutions to, critical design challenges associated with the considered high-level architecture.

Specifically, a low-noise amplifier (LNA) driven, passive integrator is proposed as an alternative to placing the amplifier outside the ADC. The remaining stages could be implemented with low-power Gm-C integrators and their current consumption depends on the load capacitance seen at the transconductors output. Design challenges regarding accurate analog signal summation with small capacitors are studied in detail.

Floating-gate, voltage addition requires less active components, but voltage buffers might be required to disable unwanted charge flow in the circuit. An output resistance of about 1kΩ is required for the buffers not to disturb the capacitive voltage division and degrade performance. Output current summation avoids this issue, but some additional complexity might be required to implement the small transconductance necessary for

low power consumption. Finally, it is discovered that comparator offset voltage will trigger even order harmonic distortion in the transconductors and comparator offset cancellation is therefore required.

To address the question of whether a control-bounded converter is suited for outperforming current state-of-the-art ADCs, more detailed research on transistor level is required. Hopefully, this thesis provide a useful background for doing exactly that.

Sammendrag

Kontrollbegrenset analog-til-digital omforming (control-bounded ADC) er et nylig introdusert konsept som skiller seg fundamentalt fra de fleste konvensjonelle omformingsarkitekturer. Disse omformerne har blitt studert på et teoretisk nivå i flere år, men det er, så vidt forfatteren vet, foreløpig ikke rapportert noen implementasjon av en slik omformer på transistornivå.

I denne avhandlingen fører vi dette nye konseptet ett steg nærmere en fullstendig implementasjon på transistornivå. Det etablerte teoretiske rammeverket er utvidet og anvendt i analyser av ulike kretsimplementasjoner. Et egenutviklet programvarebibliotek bidrar til å effektivisere prosessen med design, simulering og evaluering av kontrollbegrensede A/D-omformere. Kretssimuleringer støtter oppunder resultatene fra den teoretiske analysen.

Målet med denne avhandlingen er ikke å presentere en fullstendig implementasjon, men å utforske mulige design av en skalar, kontrollbegrenset A/D-omformer, optimalisert for lavt effektforbruk. Det viktigste resultatet fra denne avhandlingen er derfor oversikten over, og noen mulige løsninger til, kritiske designutfordringer assosiert med den aktuelle høynivåarkitekturen.

Nærmere bestemt foreslås en passiv integrator, drevet av en lavstøyforsterker, som et alternativ til å plassere forsterkeren fullstendig på utsiden av A/D-omformeren. De resterende trinnene kan realiseres med Gm-C-integratorer, hvis strømforbruk vil være avhengig av den totale kapasitansen sett fra utgangen av transkonduktoren. Designutfordringer vedrørende presis addisjon av analoge signaler med små kondensatorer er studert i detalj.

Spenningsaddisjon med flytende styreelektrode (eng. *gate*) krever færre aktive komponenter, men spenningsbuffere kan være nødvendig for å unngå problemer med uønsket ladningsflyt i kretsen. For ikke å forstyrre den kapasitive spenningsdelingen og dermed redusere ytelsen, må disse

bufferene ha en utgangsmotstand på om lag 1 kΩ. En alternativ løsning kan være å summere strømmer på transkonduktorenes utganger. Dette eliminerer behovet for spenningsbuffere, men noe ekstra kompleksitet kan være nødvendig for å implementere en liten nok transkonduktans, som er en forutsetning for lavt effektforbruk. Det er også oppdaget at en forsyvning i komparatorenes terskelspenning vil trigge harmonisk forvrengning av partals orden. Kansellering av denne terskelspenningsforsyvningen vil derfor være nødvendig i en fremtidig implementasjon.

Mer detaljert forskningsarbeid på transistornivå er nødvendig for å besvare spørsmålet om hvorvidt en kontrolbegrenset A/D-omformer er egnet for å utkonkurrere de fremste av dagens løsninger innenfor A/D-omforming. Vi håper at denne avhandlingen vil tjene som et nyttig utgangspunkt for å gjøre nettop det.

Contents

Definitions and Symbols

Matrices and Vectors

a	a scalar value
$\boldsymbol{a}$	a column vector $(a_1 \ \cdots \ a_N)^\mathsf{T} \in \mathbb{R}^N$
$\mathbf{0}_N$	an all-zero column vector of length N
$\boldsymbol{A}$	a matrix $\begin{pmatrix} a_{11} & \cdots & a_{1N} \\ \vdots & \ddots & \vdots \\ a_{M1} & \cdots & a_{MN} \end{pmatrix} \in R^{M \times N}$
$\boldsymbol{I}_N$	an N-by-N identity matrix
$()^\mathsf{T}$	transpose
$()^\mathsf{H}$	Hermetian transpose
$\lvert a \rvert$	absolute value
$\lvert\lvert \boldsymbol{b} \rvert\rvert_p$	p-norm $(\Sigma_i \lvert b_i \rvert^p)^{1/p}$
$\lvert\lvert \boldsymbol{c} \rvert\rvert_\infty$	max norm, equivalent to $\max(\lvert c_1 \rvert, \lvert c_2 \rvert, \cdots \lvert c_N \rvert)$
$\dot{\boldsymbol{x}}$	elementwise time derivative $\frac{d}{dt}\boldsymbol{x}(t)$
$(\boldsymbol{a} * \boldsymbol{b})(t)$	elementwise convolution

Sets

$\mathbb{R}$	the real numbers
$\mathbb{C}$	the complex numbers

Matrix Inverse

The following definitions and symbols applies to square matrices $\boldsymbol{A} \in \mathbb{C}^{N\times N}$.

$\boldsymbol{A}^{-1}$	The *inverse* of a matrix $\boldsymbol{A}$ defined such that $\boldsymbol{A}\boldsymbol{A}^{-1} = \boldsymbol{A}^{-1}\boldsymbol{A} = \boldsymbol{I}_N$
$\det(\boldsymbol{A})$	The *determinant*, defined recursively as $\det(\boldsymbol{A}) \triangleq \sum_{j=1}^{N}(-1)^{j+1}A_{1j}\det([\boldsymbol{A}]_{1j})$
$[\boldsymbol{A}]_{ij}$	The $(N-1)\times(N-1)$ submatrix obtained by deleting the ith row and jth column of $\boldsymbol{A}$
$\mathrm{cof}(\boldsymbol{A}, i, j)$	The (i,j) *cofactor*, $\mathrm{cof}(\boldsymbol{A}, i, j) \triangleq (-1)^{i+j}\det([\boldsymbol{A}]_{ij})$
$\mathrm{cof}(\boldsymbol{A})$	The *matrix of cofactors*, $\mathrm{cof}(\boldsymbol{A}) \triangleq \begin{pmatrix} \mathrm{cof}(\boldsymbol{A}, i, 1) & \cdots & \mathrm{cof}(\boldsymbol{A}, 1, N) \\ \vdots & \mathrm{cof}(\boldsymbol{A}, i, j) & \vdots \\ \mathrm{cof}(\boldsymbol{A}, N, 1) & \cdots & \mathrm{cof}(\boldsymbol{A}, N, N) \end{pmatrix}$
$\mathrm{adj}(\boldsymbol{A})$	The *adjoint* matrix, $\mathrm{adj}(\boldsymbol{A}) \triangleq (\mathrm{cof}(\boldsymbol{A}))^{\mathsf{T}}$

Control-Bounded Conversion

T	control period
$\mathcal{B}$	frequency band of interest
N	system order
β	integrator gain
κ	control gain
α	feedback factor
ρ	integrator leakage term, modelling finite DC-gain
$\boldsymbol{A}$	system matrix
$\boldsymbol{B}$	input matrix
$\boldsymbol{C}$	signal observation (output) matrix
$\boldsymbol{\Gamma}$	control input matrix
$\tilde{\boldsymbol{\Gamma}}$	control observation matrix
$u(t)$	input signal
$\hat{u}(t)$	estimated/reconstructed input signal
$\boldsymbol{x}(t)$	state vector
$\boldsymbol{s}[k]$	control signal
$\boldsymbol{s}(t)$	control contribution
$\tilde{\boldsymbol{s}}(t)$	control observation
$\boldsymbol{y}(t)$	signal observation
$\breve{\boldsymbol{y}}(t)$	fictional, "open-loop", signal observation
$\boldsymbol{q}(t)$	the control signal, seen at the output of the analog system
$\boldsymbol{G}(\omega)$	analog transfer function (ATF) vector
$\boldsymbol{g}(t)$	analog impulse response vector
$\boldsymbol{H}(\omega)$	noise transfer function (NTF) vector
$\boldsymbol{h}(t)$	continuous-time impulse response of reconstruction filter
$\boldsymbol{G}(\omega)\boldsymbol{H}(\omega)$	signal transfer function (STF) vector
b_u	largest permissable magnitude for the input signal
$b_{\boldsymbol{x}}$	largest permissable magnitude for the elements of $\boldsymbol{x}(t)$

Acronyms

ADC analog-to-digital converter

ATF analog transfer function

ASE average square error

CMFB common-mode feedback

DAC digital-to-analog converter

HD2 second order harmonic distortion

HD3 third order harmonic distortion

LNA low-noise amplifier

MC Monte Carlo

NRZ non-return to zero

NTF noise transfer function

OTA operational transconductance amplifier

PSD power spectral density

PVT process, voltage and temperature

RMS root mean square

RTL register-transfer level

SAR successive approximation register

SFDR spurious-free dynamic range

SNDR signal-to-noise-and-distortion ratio

SNR signal-to-noise ratio

STF signal transfer function

Chapter 1

Introduction

The need for digitalization of weak analog sensor outputs is present in any electronic system processing information from its physical surroundings. For most applications, the amount of energy spent on this operation is critical, and a lot of research is invested in the design of power efficient receiver front-ends.

Although many variations exist, a common approach is to have an ADC preceded by a LNA and possibly an anti-aliasing filter. The LNA will ease the ADC requirements in terms of noise, distortion and input impedance. This simplifies the ADC design, and even though the LNA will consume a considerable amount of power itself, the total power consumption of the receiver front-end might be reduced.

As an example, using an LNA with a gain of 10 would reduce the signal-to-noise ratio (SNR) requirements of the ADC by 20 dB. As discussed in e.g. [1], the power consumption of high SNR A/D converters tend to quadruple per extra bit of accuracy. Including the LNA could therefore be an attractive alternative to increasing the ADC accuracy.

However, it is important to remember that the performance of the receiver front-end is determined solely by how accurately the digital output of the ADC resembles the analog input signal. The LNA serves as an intermediate step in the conversion process and its presence is needed because of limitations associated with many conventional A/D converters. Potentially reduced power consumption could therefore be gained by using a different architecture, better suited for handling the sensor output directly. A promising candidate is the newly introduced concept called *control-bounded conversion*.

1.1 Control-Bounded Conversion

Control-bounded A/D conversion [2–5] offers an interesting perspective on the aforementioned challenge. As emphasized in [5, 6], the main ingredient of a control-bounded ADC is analog gain, stabilized by a digital control. The performance of the overall ADC is linked to the amount of gain in the analog system, and how tight the digital control manages to bound its internal voltage and current signals.

The increased signal magnitude obtained by placing an LNA outside the ADC will challenge the linearity of the following active component. In a control-bounded converter, the same amount of gain could be used to activate a digital control, thereby limiting the magnitude processed by the next stage. As a consequence of its output being digitally stabilized, the amplifier would contribute directly to the conversion process, while still relaxing the noise and linearity requirements on the following components by the same amount. The control-bounded converter could therefore seem to be naturally well-suited for the problem of digitizing weak sensor outputs.

1.1.1 High-Level Design Strategy

The control-bounded converter builds on the fact that analog amplification in combination with digital control amounts to an implicit A/D conversion. As explained by Hampus Malmberg [5]:

> *The digital control might be primitive, but as it systematically offloads fixed-sized portions of the accumulated internal analog system states over time, its combined effect results in a sophisticated digital representation of the internal analog system state trajectory.*

The final digital output signal is obtained by filtering these control signals through a digital estimator. The digital estimator solves the inverse problem by figuring out which analog input that most likely triggered the observed sequence of control actions.

This inverse problem could only be solved precisely if the behaviour of the system is known. This knowledge could be ensured by designing the analog system such that it accurately implements a pre-defined transfer function. However, this approach would quickly result in a circuit consuming more power than strictly necessary for realizing the desired behaviour.

An alternative is to rely of digital calibration to measure the behaviour of the analog system. In conventional A/D converters, digital calibration is often realized by measuring errors in critical component values, before correcting the digital output codes in an additional post-processing step. As an example, in [7], a 9 bit successive approximation register (SAR) ADC calibrates it self at start-up by using the 5 smallest capacitors to measure the errors on the 5 most significant ones.

For a control-bounded converter, it does not make sense to refer to these component variations as errors. While the quantization accuracy of a SAR ADC relies on precise capacitor matching, the performance of a control-bounded converter simply depends on the amount of analog amplification. Component variations will certainly affect the analog transfer function, but different does not necessarily mean worse. Rather than correcting errors, a digital calibration would synchronize the assumptions of the digital estimator with the true behaviour of the analog system.

This forms the background for the proposed design strategy. Instead of fighting against component variations with clever design techniques, we accept these variations as a natural part of the analog system. The goal is to save power and area by avoiding extra circuitry whose only objective is to make the system behaviour robust against process, voltage and temperature (PVT) variations. A digital calibration is then assumed to measure the resulting analog system behaviour.

1.2 Scope

The goal of this thesis is to provide a useful background for a future low-power implementation of a control-bounded converter. The conversion concept has been studied on a theoretical level for several years, but no transistor-level implementation is reported so far. In this thesis, we consider possible low-power implementations for the analog system and the digital control for a scalar control-bounded converter. Design challenges regarding the transistor-level implementations of the individual active components, as well as the interaction between them, are considered.

The Leapfrog ADC, proposed in [5], serves as the high-level architecture for the analog system. The main objective of the presented work is to explore power efficient solutions for the implementation of this system on transistor-level. Circuit schematics are not presented as a proposed implementation, but serves as a useful basis for discovering implementation challenges not previously thought of. The ultimate goal is to provide

a better overview of the critical implementation challenges for a future implementation of a power efficient, control-bounded converter.

In line with the proposed design strategy, a digital calibration algorithm will be assumed to measure the resulting behaviour of the analog system. The implementation of this calibration is part of an ongoing research project at ETH Zürich and is beyond the scope of this thesis. The implementation of the digital estimator is not considered, but a rough estimate of the digital power consumption is discussed together with some ideas for future improvement.

1.3 Specifications

The application setting the specifications for the presented work is medical ultrasound imaging. The ADC is designed to interface directly with a piezoelectric transducer element providing a single-ended output signal. The transducer has a resonance frequency of 4.8 MHz, at which the output capacitance is about 700 fF and the output rms noise voltage is $16\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$. The maximum output swing is 40 mV peak-to-peak. The specifications are summarized in table 1.1.

Table 1.1: Design specifications

Parameter	Symbol	Value	Comment
Center Frequency	f_{ca}	5 MHz	
Bandwidth	$\mathcal{B}$	5 MHz	$2.5 - 7.5$MHz
Maximum signal swing	b_u	40 mV	Peak-to-peak
Input ref. noise voltage	$v_{ni}(f)$	$< 16\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$	Noise figure 3dB
Input capacitance	C_{in}	$<$ 10fF	At 5MHz
Signal to noise ratio	SNR	$>$ 68 dB	Full scale input
Second harmonic distortion	HD2	< -50 dBc	
Technology		22 nm	FDSOI CMOS

1.4 Main Contributions

The main contributions of this thesis are the insight obtained by considering a low-power implementation of a control-bounded converter on transistor level, together with the theoretical analysis and developed software tools. In particular, we highlight the following contributions:

- An LNA driven, passive integrator is proposed as a solution for the first integration stage. This approach achieves the input impedance, noise and linearity performance of a conventional LNA, while simultaneously contributing to the conversion process as its output is stabilized by a digital control.
- An overview of design challenges associated with low-power, analog signal summation with Gm-C integrators is obtained. Floating-gate voltage summation requires voltage buffers (or possibly other techniques) to disable unwanted charge flow in the system. Output current summation comes with the challenges of realizing small transconductors and attenuation circuits might be required.
- It is discovered that comparator offset voltage will trigger even order harmonic distortion in the open-loop transconductors, and offset cancellation is required for future development.
- The analytical stability guarantee of [5] is extended to the considered Leapfrog architecture. The analysis consider more general transfer functions and include several non-ideal effects such as comparator offset, digital delay and clock jitter.
- A custom python framework for general purpose analog circuit design is written and used to interface with existing resources for simulating control-bounded converters. Together with the experience of "best practice" python based, analog design methodology, these tools provides a platform efficient development in the future.

1.5 Related Work

This thesis is in many ways a continuation of a previous project presented in [6]. That project was the author's first introduction to control-bounded conversion and a significant part of the work was dedicated to understanding the concept. The remaining part of the thesis was centered around architectures particularly suited for multi-channel receiver systems.

This work builds on the previous project in the sense that we assume the reader to be somewhat familiar with the control-bounded conversion concept. However, instead of focusing on multi-input A/D converters, this thesis is concerned with the scalar input case.

Furthermore, the doctoral thesis of Hampus Malmberg [5] constitutes the main source of information on the topic. His thesis gives a comprehensive

introduction to control-bounded converters and proposes several ADC architectures suited for various applications. One of them is the Leapfrog ADC, which forms the background for the high-level architecture considered in this thesis. The Leapfrog ADC is an extension of the Chain-of-integrators ADC, treated in both [6] and [5]. This basic architecture is a useful textbook-example of a control-bounded converter and certain results obtained in this work is compared to the Chain-of-integrators for reference.

1.5.1 References to Conventional Converters

As discussed in [6], the control-bounded converter shares some similarities with conventional oversampling A/D converters, in particular the continuous-time $\Sigma\Delta$ ADC. Being familiar with these converters is not at all a prerequisite for following this thesis and they are therefore not treated as a part of the background material. However, in order to connect the presented material to already existing knowledge, certain parts of the thesis will contain references to the design of $\Sigma\Delta$ converters. We point out similarities to place the control-bounded converter in a familiar context, and we discuss differences to highlight the potential for innovative solutions and increased performance. For an introduction to topic, several excellent sources exist, e.g [8] or [9].

1.6 Outline

The remaining part of the thesis is structured as follows.

- **Chapter 2** gives a concise introduction to the control-bounded conversion concept. The material is a less comprehensive version of chapter 3 in [6] and is included here to establish the necessary terminology and background theory.
- **Chapter 3** presents the proposed high-level hardware architecture together with an analysis of important non-idealities.
- In **Chapter 4**, we present a short description of the software tools used for the presented simulations.
- **Chapter 5** presents the considered low-power circuit implementation. Simulation results are presented along the way to support the theoretical analysis.
- **Chapter 6** Provides a discussion of digital power consumption and relevant topics that did not fit naturally in the other parts of the thesis.
- Finally, **Chapter 7** concludes the thesis and presents the current plan for future development.

Chapter 2

Control-Bounded A/D Conversion

This thesis is a continuation of the work presented in [6] and the reader is therefore assumed to be somewhat familiar with the control-bounded conversion concept. However, for the sake of completeness, a concise introduction is given in this chapter.

The control-bounded conversion concept is developed by prof. Hans-Andrea Loeliger et al., at the Signal and Information Processing Laboratory (ISI), ETH Zürich. The latest contribution to the topic is the doctoral thesis of Hampus Malmberg [5] which serves as the main source of information for this chapter.

This chapter is structured as follows. The fundamental principle of the control-bounded converter is introduced with an intuitive analogy to negative feedback amplifiers in section 2.1. In section 2.2 the basic building blocks of the converter is presented, before each of them are studied independently in sections 2.3 to 2.5.

2.1 An Intuitive Analogy

Before establishing the formal language used to describe the control-bounded converter, an intuitive analogy is given in this section. Consider the classic negative feedback amplifier of figure 2.1, where a fraction of the output is fed back to amplifiers inverting input. By assuming the amplifier has infinite gain, this will at any time equalize the voltage on its two inputs. In other words, the amplifier will do what ever necessary

to make $x(t) = 0$ for all times t. What the amplifier does to accomplish this is what we observe as the output $y(t)$.

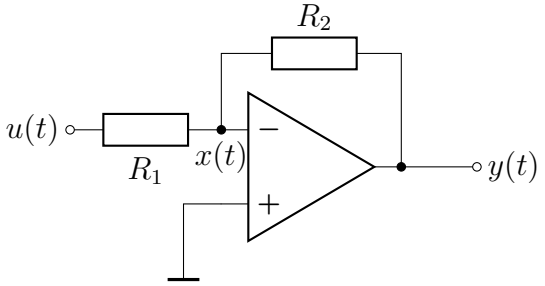


Figure 2.1: A negative feedback amplifier

The beauty of this approach lies in the fact that the observed amplification is nearly independent of the internal characteristics of the amplifier. Given that the amplifier has sufficiently high gain within the bandwidth of interest, the amplification is given solely by the feedback network. In the circuit of figure 2.1, *what the amplifier does* will depend on how we choose the resistors R_1 and R_2, yielding an effective amplification of

$$\frac{y(t)}{u(t)} = -\frac{R_2}{R_1} \tag{2.1}$$

When the true gain of the amplifier is not infinite, the negative input will have some small non-zero value, and the gain-error is the value of $x(t)$ seen at the output $y(t)$.

Intuitively, the control-bounded converter could be thought of as the concept of negative feedback amplification, extended to A/D conversion. In a control-bounded converter, we use digital feedback to force the analog inputs, $\boldsymbol{x}(t)$, of several amplifying elements to zero. The system responsible for this operation is called the digital control. The analog input of the ADC is digitalized by observing *what the digital control does* to ensure $\boldsymbol{x}(t) = \mathbf{0}$ for all times t. As for negative feedback amplifiers, $\boldsymbol{x}(t)$ will always have some non-zero value and the quantization error of the ADC is exactly the magnitude of $\boldsymbol{x}(t)$ observed at the output.

In a negative feedback amplifier, *what the amplifier does* to force $x(t) = 0$ is the output $y(t)$ directly. However, in a control-bounded converter, the amplification happen over multiple stages and the voltage on several nodes of the analog system is forced to zero by multiple digital control actions. In consequence, *what the digital control does* is only indirectly related to the final ADC output, and a (rather complicated) digital filter is required to reconstruct the output from these digital control signals.

Despite these practical complications, the fundamental principle of operation closely resemble that of a negative feedback amplifier. The analogy could therefore be useful to keep in mind while studying the formal introduction to control-bounded conversion in the remainder of this chapter.

2.2 Fundamentals

A control-bounded ADC consists of three main components; an analog system (AS), a digital control (DC) and a digital estimator (DE). Their interaction is illustrated in figure 2.2. The input signal $u(t)$, here assumed to be scalar, enters the analog system which provides amplification within the frequency band of interest. The internal states of the analog system is observed by the digital control through the (vector valued) *control observation* $\tilde{\boldsymbol{s}}(t)$. The control observation is sampled and quantized, resulting in the *control signal* $\boldsymbol{s}[k]$. The analog version of this signal is called the *control contribution* $\boldsymbol{s}(t)$ and is applied to the analog system to counteract the internal state growth. The digital estimator observes the control signals $\boldsymbol{s}[k]$, from which it reconstructs an estimate $\hat{u}(t)$ of the input signal $u(t)$.

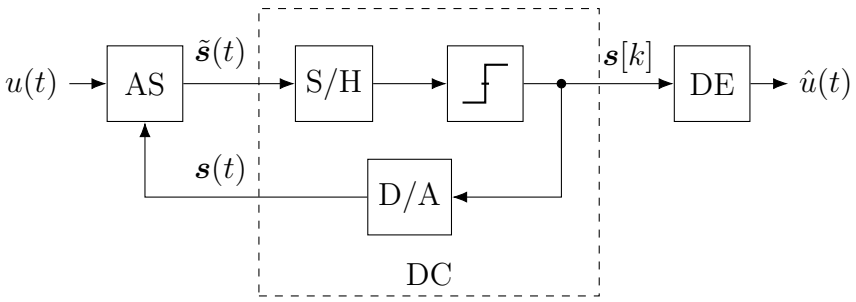


Figure 2.2: The main building blocks of a control-bounded ADC. Figure from [6].

2.3 Analog System

The analog system is described using the state-space model notation as illustrated in figure 2.3.

The core of the analog system is the *state vector* $\boldsymbol{x}(t) \in \mathbb{R}^N$ which is related to the input signal $u(t)$ and the control contribution $\boldsymbol{s}(t) \in \mathbb{R}^M$ by the differential equation system

$$\dot{\boldsymbol{x}}(t) = \boldsymbol{A}\boldsymbol{x}(t) + \boldsymbol{B}u(t) + \boldsymbol{\Gamma}\boldsymbol{s}(t). \tag{2.2}$$

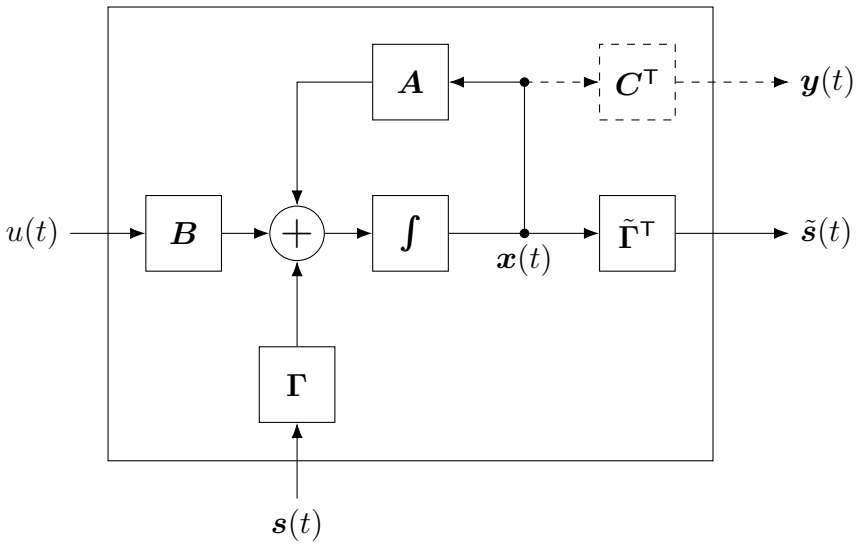


Figure 2.3: State space model of the analog system. The dashed lines represent conceptual signals that only exist inside the digital estimator. Figure from [5].

The components of $\boldsymbol{x}(t)$ represents internal currents or voltages on different nodes of the analog system, and the *system matrix* $\boldsymbol{A} \in \mathbb{R}^{N\times N}$ describes how the state vector evolves over time. The two inputs, $u(t)$ and $\boldsymbol{s}(t)$, enters the system through the *input matrix* $\boldsymbol{B} \in \mathbb{R}^{N\times 1}$ and the *control input matrix* $\boldsymbol{\Gamma} \in \mathbb{R}^{N\times M}$ respectively. The dimension of the state vector, N, is sometimes referred to as the *system order*.

The control observation $\tilde{\boldsymbol{s}}(t) \triangleq \tilde{\boldsymbol{\Gamma}}^\mathsf{T}\boldsymbol{x}(t) \in \mathbb{R}^M$ is related to the state vector through the *control observation matrix* $\tilde{\boldsymbol{\Gamma}}^\mathsf{T}$. The *output signal* $\boldsymbol{y}(t) \triangleq \boldsymbol{C}^\mathsf{T}\boldsymbol{x}(t) \in \mathbb{R}^{\tilde{N}}$ is a purely conceptual quantity that is used by the digital estimator to reconstruct the estimate $\hat{u}(t)$ of $u(t)$.

The system of differential equations (2.2) results in an analog transfer function (ATF) vector, where the i-th element gives the transfer function from $u(t)$ to output i. The transfer function is given by

$$\boldsymbol{G}(\omega) = \boldsymbol{C}^\mathsf{T}\left(j\omega\boldsymbol{I}_N - \boldsymbol{A}\right)^{-1}\boldsymbol{B} \in \mathbb{C}^{\tilde{N}\times 1}, \tag{2.3}$$

and the analog impulse response vector is then obtained from the inverse Laplace transform as

$$\boldsymbol{g}(t) = \boldsymbol{C}^\mathsf{T}\exp(\boldsymbol{A}t)\boldsymbol{B} \in \mathbb{R}^{\tilde{N}\times 1}, \tag{2.4}$$

where exp(.) refers to the matrix exponential.

2.4 Digital Control

The digital control stabilizes the analog system by forcing the magnitude of the state vector $\boldsymbol{x}(t)$ to stay within some predefined boundary. A conceptual block diagram is shown in figure 2.2, where the digital control consist of a sample-and-hold circuit, a one-bit quantizer and a digital-to-analog converter. Although a practical implementation may realize all the functionality in a single component, this structure is a useful illustration.

The control signal $\boldsymbol{s}[k]$ is generated by sampling and quantizing the control contribution $\tilde{\boldsymbol{s}}(t)$ with a clock period T, and passed on to the digital estimator. The second output of the digital control is the analog control contribution $\boldsymbol{s}(t)$, which in this thesis is assumed to be generated by a non-return to zero (NRZ) D/A converter.

2.4.1 Effective Digital Control

To quantify the performance of the digital control, we introduce the boundaries b_u and $b_{\boldsymbol{x}}$. We say that the input signal is bounded if

$$|u(t)| \leq b_u \ \forall t \tag{2.5}$$

and equivalently that the state vector is bounded if it satisfies

$$||\boldsymbol{x}(t)||_\infty \leq b_{\boldsymbol{x}} \ \forall t. \tag{2.6}$$

The digital control is then called effective if it manages to keep the state vector bounded, given a bounded input. The system is called *unstable* at a time t, if the magnitude of an element of $\boldsymbol{x}(t)$ exceeds $b_{\boldsymbol{x}}$.

As shown in appendix A, the solution to the state-space equations (2.2) may be written as

$$\boldsymbol{x}(t) = \tilde{\boldsymbol{g}}(t) \cdot \boldsymbol{x}(0) + (\tilde{\boldsymbol{g}} * \boldsymbol{B}u)(t) + (\tilde{\boldsymbol{g}} * \boldsymbol{\Gamma}\boldsymbol{s})(t), \tag{2.7}$$

where

$$\tilde{\boldsymbol{g}}(t) \triangleq \exp(t\boldsymbol{A}), \tag{2.8}$$

and exp(.) refers to the matrix exponential. In (2.7) $\boldsymbol{x}(0)$ is the value of the state vector at the beginning of a control period $t \in [0, T)$.

Let

$$\mathcal{X} \triangleq \{\tilde{\boldsymbol{x}}(t) : ||\tilde{\boldsymbol{x}}(t)||_\infty < b_{\boldsymbol{x}} \ \forall t\} \tag{2.9}$$

be the set of all bounded state vectors, and let

$$\mathcal{U} \triangleq \{v(t) : |v(t)| < b_u \ \forall t\} \tag{2.10}$$

be the set of all bounded input signals. The condition for effective control may then be expressed as

$$\max_{\boldsymbol{x}(t)\in\mathcal{X},u(t)\in\mathcal{U},t\in[0,T)} ||\tilde{\boldsymbol{g}}(t)\cdot\boldsymbol{x}(0)+(\tilde{\boldsymbol{g}}*\boldsymbol{B}u)(t)+(\tilde{\boldsymbol{g}}*\boldsymbol{\Gamma s})(t)||_\infty < b_{\boldsymbol{x}}. \quad (2.11)$$

By the triangle inequality, this expression is upper bounded as

$$\max_{\boldsymbol{x}(t)\in\mathcal{X},u(t)\in\mathcal{U},t\in[0,T)} ||\tilde{\boldsymbol{g}}(t)\cdot\boldsymbol{x}(0)+(\tilde{\boldsymbol{g}}*\boldsymbol{B}u)(t)+(\tilde{\boldsymbol{g}}*\boldsymbol{\Gamma s})(t)||_\infty \leq$$
$$\max_{\boldsymbol{x}(t)\in\mathcal{X},t\in[0,T)} ||\tilde{\boldsymbol{g}}(t)\cdot\boldsymbol{x}(0)+(\tilde{\boldsymbol{g}}*\boldsymbol{\Gamma s})(t)||_\infty + \max_{u(t)\in\mathcal{U},t\in[0,T)} ||(\tilde{\boldsymbol{g}}*\boldsymbol{B}u)(t)||_\infty. \quad (2.12)$$

From the right side of (2.12) we define

$$R(t) \triangleq \max_{||\boldsymbol{x}(0)||_\infty\in[-b_{\boldsymbol{x}},b_{\boldsymbol{x}}]} ||\tilde{\boldsymbol{g}}(t)\cdot\boldsymbol{x}(0)+(\tilde{\boldsymbol{g}}*\boldsymbol{\Gamma s})(t)||_\infty \quad (2.13)$$

and

$$G(t) \triangleq \max_{u(t)\in\mathcal{U}} ||(\tilde{\boldsymbol{g}}*\boldsymbol{B}u)(t)||_\infty \quad (2.14)$$

as the *remainder term* and *growth term* respectively.

The remainder term itself consists of two components, $\tilde{\boldsymbol{g}}(t)\cdot\boldsymbol{x}(0)$ and $(\tilde{\boldsymbol{g}}*\boldsymbol{\Gamma s})(t)$. The fist part, $\tilde{\boldsymbol{g}}(t)\cdot\boldsymbol{x}(0)$, describes the part of the evolution of the analog state vector coming from the initial state at the beginning of the control period. The digital control observes a quantized version of $\tilde{\boldsymbol{\Gamma}}\boldsymbol{x}(0)$ and produces $\boldsymbol{s}(t)$ in response. The second term, $(\tilde{\boldsymbol{g}}*\boldsymbol{\Gamma s})(t)$, expresses the effect of this control contribution on the state trajectory. The goal of the digital control is to make the sum of these contributions as small as possible, which is achieved by minimizing $R(t)$ for $t\in[0,T)$.

The growth term gives the contribution of the input signal $u(t)$ to $||\boldsymbol{x}(t)||_\infty$ at a time $t\in[0,T)$. As this contribution is not visible to the digital control until the beginning of the next control period, the magnitude of $G(t)$ must be kept sufficiently low by properly scaling the gain of the analog system and the length of the control period, T.

Using these terms, the condition for effective digital control is given by,

$$\max_{t\in[0,T)} (R(t)+G(t)) < b_{\boldsymbol{x}}. \quad (2.15)$$

For certain architectures, this expression could be translated into a set of design equations, and an analytical stability guarantee may be achieved. This will be exemplified in section 3.5. Finally, note that it is sufficient to ensure $(R(t)+G(t)) < b_{\boldsymbol{x}}$ for a single control period $t\in[0,T)$, as this would imply that the initial state of any subsequent control period would also be bounded (given a bounded input).

2.5 Digital Estimator

The digital estimator is producing the final output of the ADC by reconstructing an estimate $\hat{u}(t)$ of $u(t)$. Although the actual output of the ADC will be discrete in time, the output estimate is denoted as a continuous-time signal. This notation is chosen because the digital estimator creates a continuous-time mathematical model of the input signal, and the final digital output estimates may be computed from this model at an arbitrary time interval, independent of the control period T.

The estimate is based on the control signals $\boldsymbol{s}[k]$, and the knowledge of the the corresponding control contribution $\boldsymbol{s}(t)$ and the analog system parameters. As the implementation of the digital estimator is beyond the scope of this thesis, a detailed description of the estimation filter is not part of the necessary theoretical background for the remaining chapters. Instead of providing a formal treatment of the estimation filter problem, this section is therefore limited to an intuitive explanation of the operation principles, and the reader is referred to [6] or [5] for details. The key takeaways from this section are the filter properties that influence the overall ADC performance such as bandwidth and signal-to-noise ratio.

As emphasized in the beginning of this chapter, digitally stabilized analog gain amounts an implicit A/D conversion. The analog system is designed such that, in the absence of any control, its internal states would quickly saturate when fed an input signal. The digital control prevents this from happening by applying the control contribution $\boldsymbol{s}(t)$ to counteract the internal state growth. The combined effect of these control actions over time contains information about the input signal, available to the digital estimator by solving the inverse problem. In other words, by combining the observed control actions with the knowledge of the complete system behaviour, it figures out which input signal that most likely triggered the observed $\boldsymbol{s}[k]$.

2.5.1 Transfer Functions and Filter Bandwidth

The filter that solves this problem happens to be a Wiener filter. The impulse response and frequency response vector of this filter is denoted by $\boldsymbol{h}(t) : \mathbb{R} \to \mathbb{R}^{\tilde{N}\times 1}$ and $\boldsymbol{H}(\omega) : \mathbb{R} \to \mathbb{C}^{\tilde{N}\times 1}$ respectively. In practice, the filter is implemented recursively as a variation of the Kalman smoothing algorithm, and the impulse response is not used directly in the computation of $\hat{u}(t)$. However, a study of the frequency response vector $\boldsymbol{H}(\omega)$ reveals useful insight in critical aspects of the ADC performance and is therefore included in this section.

It was shown in [6] that the final output of the estimation filter may be written as

$$\hat{u}(t) = (\boldsymbol{h} * \boldsymbol{g} * u)(t) - (\boldsymbol{h} * \boldsymbol{y})(t) \tag{2.16}$$

where $\boldsymbol{h}(t)$ and $\boldsymbol{g}(t)$ are the impulse response vector of the estimation filter and the analog system respectively, and $u(t)$ and $\boldsymbol{y}(t)$ are the true input signal and the (conceptual) output of the analog system. As the analog system is assumed to greatly amplify the input signal, $||(\boldsymbol{g} * u)(t)||_\infty$ is assumed to be large compared to $||\boldsymbol{y}(t)||_\infty$. This justifies the approximation

$$\hat{u}(t) = (\boldsymbol{h} * \boldsymbol{g} * u)(t) - (\boldsymbol{h} * \boldsymbol{y})(t) \tag{2.17}$$

$$\hat{u}(t) \approx (\boldsymbol{h} * \boldsymbol{g} * u)(t), \tag{2.18}$$

which forms the basis of the derivation of $\boldsymbol{h}(t)$. Any deviation of $\boldsymbol{y}(t)$ from $\mathbf{0}$ will introduce an error in the estimate, meaning that $-\boldsymbol{y}(t)$ is the conversion error seen at the output of the analog system. This error does not add directly to the final estimate, but is filtered by $\boldsymbol{h}(t)$. From the Fourier transform of (2.17),

$$\hat{\boldsymbol{U}}(\omega) = \underbrace{\boldsymbol{H}(\omega)\boldsymbol{G}(\omega)}_{\text{STF}}\boldsymbol{U}(\omega) - \underbrace{\boldsymbol{H}(\omega)}_{\text{NTF}}\boldsymbol{Y}(\omega), \tag{2.19}$$

we recognize $\boldsymbol{H}(\omega)$ and $\boldsymbol{G}(\omega)\boldsymbol{H}(\omega)$ as the noise transfer function (NTF) and signal transfer function (STF) vector respectively.

With $\hat{\boldsymbol{u}}(t)$ as in (2.17), the estimation filter is determined by

$$\boldsymbol{h}(t) = \underset{\bar{\boldsymbol{h}}}{\operatorname{argmin}}\, \mathrm{E}[(\hat{\boldsymbol{u}}(t) - \boldsymbol{u}(t))^2], \tag{2.20}$$

when $\boldsymbol{u}(t)$ and $\boldsymbol{y}(t)$ are modelled as independent, centered and wide-sense stationary stochastic processes. The resulting frequency response vector is given by

$$\boldsymbol{H}(\omega) = \mathrm{NTF} = \frac{\boldsymbol{G}^{\mathsf{H}}(\omega)}{||\boldsymbol{G}(\omega)||_2^2 + \eta^2}, \tag{2.21}$$

and the signal transfer function becomes

$$\mathrm{STF} = \boldsymbol{H}(\omega)\boldsymbol{G}(\omega) = \frac{||\boldsymbol{G}(\omega)||_2^2}{||\boldsymbol{G}(\omega)||_2^2 + \eta^2} \in \mathbb{R}. \tag{2.22}$$

The parameter η is used as a design variable to set the bandwidth of the estimation filter. We define the bandwidth of the filter in terms of the *critical frequency* ω_c as

$$||\boldsymbol{G}(\omega_c)||_2^2 = \eta^2. \tag{2.23}$$

This definition is meaningful for systems where there exist only one $\omega_c > 0$ such that $||\boldsymbol{G}(\omega_c)||_2^2 = \eta^2$ and $||\boldsymbol{G}(\omega)||_2^2 > ||\boldsymbol{G}(\omega_c)||_2^2 \; \forall \; \omega \in [0, \omega_c)$.

When designing the analog system, it might not be intuitive what value of η that results in the desired filter bandwidth. Hence it is usually more efficient to work with ω_c, or equivalently $f_c = \frac{\omega_c}{2\pi}$, directly and then calculate the corresponding η from (2.23) when the ATF is known.

2.5.2 Conversion Noise Power

An analytic treatment of the conversion noise power seen at the output of a control-bounded ADC is found in [5]. The analysis approximates the conversion error signal, $\boldsymbol{y}(t)$, as being a stationary stochastic process, bandlimited to a bandwidth $\mathcal{B}$. Hence, the PSD matrix of $\boldsymbol{y}(t)$ is approximated by

$$\boldsymbol{S}_{\boldsymbol{y}\boldsymbol{y}^\mathsf{T}} \approx \sigma^2_{\boldsymbol{y}|\mathcal{B}} \boldsymbol{I}_M, \tag{2.24}$$

where $\sigma^2_{\boldsymbol{y}|\mathcal{B}}$ is the standard deviation of $\boldsymbol{y}(t)$ within the bandwidth of interest.

From this approximation, the conversion noise power observed at the ADC output is given by

$$\boldsymbol{P}_{\epsilon|\mathcal{B}} \approx \frac{\sigma^2_{\boldsymbol{y}|\mathcal{B}}}{2\pi} \int_{\omega \in \mathcal{B}} \frac{1}{||\boldsymbol{G}(\omega)||_2^2} d\omega. \tag{2.25}$$

Although the validity of this approximation is limited, it reveals a useful insight in the parameters affecting the overall ADC performance. As $\sigma^2_{\boldsymbol{y}|\mathcal{B}}$ is related to the magnitude of the analog state vector $\boldsymbol{x}(t)$, it is minimized by tightening the state boundary $b_{\boldsymbol{x}}$. The value of the integral is minimized by increasing the gain of the analog system. Equation (2.25) therefore show that low conversion noise is achieved by the combination of high analog gain and a tight state bound.

The bandwidth of the estimation filter will also influence the amount of conversion noise seen at the ADC output. In conventional oversampled converters, lowering the cut-off frequency of the decimation filter would decrease the total conversion noise, at the expense of reduced bandwidth. The same trade-off is also present in control-bounded ADCs, which is seen by considering the ratio between the STF and NTF at the critical

frequency,

$$\frac{\mathrm{STF}(\omega_c)}{||\boldsymbol{H}(\omega_c)||_2} = \frac{||\boldsymbol{G}(\omega_c)||_2^2}{||\boldsymbol{G}(\omega_c)||_2^2 + \eta^2} \left(\frac{||\boldsymbol{G}(\omega_c)||_2}{||\boldsymbol{G}(\omega_c)||_2^2 + \eta^2} \right)^{-1} \tag{2.26}$$

$$= ||\boldsymbol{G}(\omega_c)||_2 \tag{2.27}$$

$$= \eta. \tag{2.28}$$

2.5.3 Thermal Noise

The influence of thermal noise on the final ADC output is analysed in [5]. In the analysis, a single thermal noise source, $z(t)$, is modelled as a stationary stochastic process with flat PSD

$$S_z(\omega) = \sigma_{z|\mathcal{B}}^2, \tag{2.29}$$

within the frequency band of interest $\mathcal{B}$. The noise source enters at some point in the analog system, and $\boldsymbol{g}_z(t)$ denotes the vector of impulse responses from this noise source to the output $\boldsymbol{y}(t)$. It is shown in [5] that the thermal noise error signal seen at the ADC output is given by

$$\epsilon_z(t) = (\boldsymbol{h}(t) * \boldsymbol{g}_z(t) * z)(t). \tag{2.30}$$

The contribution to the output noise power is then given by

$$P_{\epsilon_z} \triangleq \mathrm{E}[\epsilon_z(t)^2] \tag{2.31}$$

$$= \frac{\sigma_{z|\mathcal{B}}^2}{2\pi} \int_{\mathcal{B}} \boldsymbol{H}(\omega)\boldsymbol{G}_z(\omega)\boldsymbol{G}_z(\omega)^{\mathsf{H}}\boldsymbol{H}(\omega)^{\mathsf{H}} d\omega \tag{2.32}$$

$$= \frac{\sigma_{z|\mathcal{B}}^2}{2\pi} \int_{\mathcal{B}} \frac{|\boldsymbol{G}(\omega)^{\mathsf{H}}\boldsymbol{G}_z(\omega)|}{\left(||\boldsymbol{G}(\omega)||_2^2 + \eta^2\right)^2} d\omega, \tag{2.33}$$

where $\boldsymbol{G}_z(\omega)$ is the elementwise Fourier transform of $\boldsymbol{g}_z(t)$. Assuming uncorrelated noise sources, the total contribution of multiple such thermal noise sources $z_1(t), z_2(t), \ldots$ is given by $P_{\epsilon_{z_1}} + P_{\epsilon_{z_2}} + \ldots$.

2.5.4 Instability

As a final remark, we include a short qualitative discussion of the estimation filters behaviour when the analog systems becomes unstable. As the estimator makes the assumption $||\boldsymbol{x}(t)||_\infty < b_{\boldsymbol{x}}\ \forall t$, the estimator will not be able to detect state vector magnitudes above this threshold. If $|x_i(t)| > b_{\boldsymbol{x}}$ for a certain period of time, the estimator will assume

$|x_i(t)| = b_{\boldsymbol{x}}$ during that time interval. This assumption limits the detectable magnitude of the input signal.

However, due to the low-pass behaviour of $\boldsymbol{H}(\omega)$, the estimator will always provide a smooth output. If for instance $u(t)$ is a sinusoidal signal with a magnitude $|u(t)| > b_u$, causing $|x_1(t)|$ to periodically exceed $b_{\boldsymbol{x}}$, the output will still be approximately harmonic and no sharp clipping will occur. If $|u(t)| >> b_u$, the magnitude of $u(t)$ will be estimated with very poor precision and harmonic distortion will appear in the output spectrum. However, if $||\boldsymbol{x}(t)||_\infty$ barely exceeds $b_{\boldsymbol{x}}$ for a short period, the event might not even be noticeable at the output. In other words, the instability of a control-bounded converter is a non-binary thing, where the quality of the output is gradually reduced with the degree of instability.

Chapter 3

High-Level Architecture

In [6], the Chain-of-integrators ADC was presented as the first example of a control-bounded A/D converter. The simple structure is convenient for analysis as well as implementation purpose. However, a disadvantage of the simple chain structure is ths lack of feedback between the different states. Any error introduced early in the chain will add directly to the output. Moreover, the transfer function of the analog system has real poles only, limiting the achievable frequency response to the familiar $-20N$dB per decade.

The Leapfrog ADC presented in [5] addresses the mentioned issues by implementing the analog system as a Leapfrog filter, treated in e.g. [10]. In the Leapfrog filter, all states are connected to each other through the parallel arrangement of a forward and a backward chain structure. The filter has the convenient property of minimum sensitivity of components variations on the transfer function in the pass band [10]. This structure also enable complex pole pairs in the transfer function and hence a sharper transition between the pass- and stop-band. As expected from conventional feedback theory, this structure shows improved tolerance to harmonic distortion at the expense of reduced DC-gain.

3.1 General Structure

The general structure of the analog system is illustrated in figure 3.1. The integrators of the analog system are represented by their respective transfer function $\frac{\beta}{s+\rho}$. The *integrator gain*, β, relates to the unity gain frequency, f_u, of the integrator by $\beta = 2\pi f_u$. The finite DC-gain of integrator i is represented by ρ_i, and the DC-gain of the integrator is given

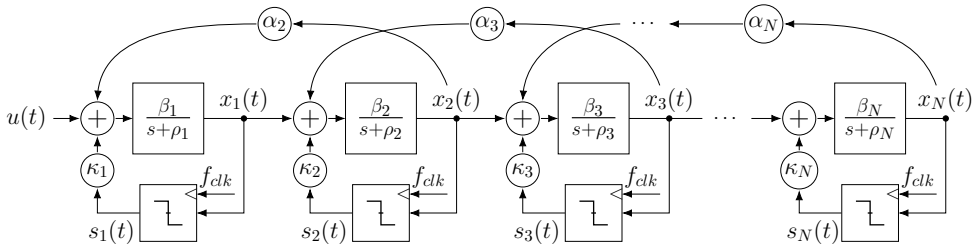


Figure 3.1: The general structure of the Leapfrog ADC

by $A_{0i} = {}^{\beta_i}/_{\rho_i}$.

The Leapfrog ADC differs from the Chain-of-integrators by the additional feedback paths between neighboring states. The feedback from x_i to x_{i-1} is achieved through α_i, feeding a portion of x_i back to the input of integrator $(i-1)$. Each integrator is stabilized by a local digital control, which is represented by a clocked comparator in figure 3.1. The output of comparator i is the control-contribution $s_i(t)$ which is scaled by a factor κ_i before entering the integrator input.

3.2 Parametrization

The evolution of the state vector is described by

$$\dot{\boldsymbol{x}}(t) = \boldsymbol{A}\boldsymbol{x}(t) + \boldsymbol{B}u(t) + \boldsymbol{\Gamma}\boldsymbol{s}(t), \tag{3.1}$$

where

$$\boldsymbol{A} = \begin{pmatrix} -\rho_1 & \beta_1\alpha_2 & & & \\ \beta_2 & -\rho_2 & \beta_2\alpha_3 & & \\ & \beta_3 & -\rho_3 & \ddots & \\ & & \ddots & \ddots & \beta_{N-1}\alpha_N \\ & & & \beta_N & -\rho_N \end{pmatrix}, \tag{3.2}$$

$$\boldsymbol{B} = \begin{pmatrix} \beta_1 & \cdots & 0 \end{pmatrix}^{\mathsf{T}}, \tag{3.3}$$

and

$$\boldsymbol{\Gamma} = \begin{pmatrix} \kappa_1\beta_1 & & \\ & \ddots & \\ & & \kappa_N\beta_N \end{pmatrix}. \tag{3.4}$$

For this local digital control, the control observation $\tilde{\boldsymbol{s}}(t)$ coincides with the state vector $\boldsymbol{x}(t)$ meaning that the control observation matrix $\tilde{\boldsymbol{\Gamma}}^{\mathsf{T}} =$

$\boldsymbol{I}_N$. As discussed in [6], the output matrix is either

$$\boldsymbol{C}^\mathsf{T} = \boldsymbol{C}_s^\mathsf{T} \triangleq \begin{pmatrix} 0 & \cdots & 0 & 1 \end{pmatrix} \in \mathbb{R}^{1\times N} \tag{3.5}$$

or

$$\boldsymbol{C}^\mathsf{T} = \boldsymbol{C}_m^\mathsf{T} \triangleq \boldsymbol{I}_N, \tag{3.6}$$

where the latter gives the best performance while the former is convenient for theoretical analysis.

3.3 Transfer Function Analysis

As one of the main motivations for the Leapfrog ADC was the ability to implement complex poles in the transfer function, the mathematical relationship between the system parameters and the ATF is a necessary design tool. However, a complete analytical analysis of the ATF with arbitrary parameters β_i, ρ_i and α_i would result in a rather complex expression, obscuring the essential principles determining the system behaviour. The approach of this section is therefore to consider a simple special case of the analog system, and treat any deviations as perturbations of this starting point. This way, we also reduce the large number of parameters in (3.2) to a few degrees of freedom, facilitating a more efficient design process.

The general expression for the transfer function of the analog system is given by equation (2.3) and may be written as

$$\boldsymbol{G}(\omega) = \boldsymbol{C}^\mathsf{T} \left(j\omega \boldsymbol{I}_N - \boldsymbol{A}\right)^{-1} \boldsymbol{B} \tag{3.7}$$

$$= \boldsymbol{C}^\mathsf{T} \frac{\operatorname{adj}\left(j\omega \boldsymbol{I}_N - \boldsymbol{A}\right)}{\det\left(j\omega \boldsymbol{I}_N - \boldsymbol{A}\right)} \boldsymbol{B}, \tag{3.8}$$

where $\operatorname{adj}(\boldsymbol{A})$ and $\det(\boldsymbol{A})$ denotes the adjoint and determinant of a matrix $\boldsymbol{A}$ respectively. To simplify the analysis, only the scalar output case, i.e. $\boldsymbol{C}^\mathsf{T} = \boldsymbol{C}_s^\mathsf{T}$ is considered. In this case the ATF is a scalar and it was shown in [5] that it may be written as

$$G(\omega) = \frac{\prod_{\ell=1}^{N} \beta_\ell}{p_N(\omega)}, \tag{3.9}$$

where

$$p_N(\omega) = \det\left(j\omega \boldsymbol{I}_N - \boldsymbol{A}\right) \tag{3.10}$$

is the N-th order polynomial obtained from computing the determinant of $(j\omega \boldsymbol{I}_N - \boldsymbol{A})$.

3.3.1 A Special Case

The remaining part of the analysis will be centered around the special case where

$$\beta_1 = \beta_2 = \cdots = \beta_N = \beta, \tag{3.11}$$

$$\alpha_2 = \alpha_3 = \cdots = \alpha_N = -\frac{\omega_p^2}{4\beta^2}, \tag{3.12}$$

and

$$\rho_1 = \rho_2 = \cdots = \rho_N = 0. \tag{3.13}$$

According to [5], the poles of this system is given by

$$p_N(\omega) = \prod_{k=1}^{N} \left(j\omega - j\omega_p \cos\left(\frac{k\pi}{N+1} \right) \right). \tag{3.14}$$

This particular parametrization describes a system where all integrators have infinite DC-gain and the same integrator gain β. Moreover, the feedback coefficient α is equal for all integrators and relates to β through the pole frequency parameter ω_p by equation (3.12).

From equation (3.14) it is clear that this system has complex conjugated pole pairs, placed at the imaginary axis in the s-plane. Additionally, for odd numbers of N there will also be a pole at the origin. The highest frequency pole, given by $\omega_{p,max} = \omega_p \cos\left(\frac{N\pi}{N+1}\right)$, will approach ω_p asymptotically as the system order N is increased. The lower frequency poles will be distributed according to (3.14), and the spacing between the poles will decrease with pole frequency.

Figure 3.2 shows the ATF, NTF and STF of the Leapfrog ADC for $N = 3, N = 5$ and $N = 8$. In this system, $\beta = 2\pi 40\,\text{MHz}$, the bandwidth is set to $f_c = 10\,\text{MHz}$, cf. (2.23), and $\omega_p = 2\pi f_c$. The figure confirms the above analysis, showing that the highest pole frequency approaches the cut-off frequency of the STF as the filter order is increased.

To see the advantage of complex poles in the NTF, consider figure 3.3, which compares the transfer functions of a 4th order Leapfrog to that of a Chain-of-integrators. The parameters β, ω_p and f_c are the same as in figure 3.2. The figure shows that the peak of the NTF is approximately 10dB higher for the Chain-of-integrators than for the Leapfrog. The DC gain of the plain chain structure is higher due to the lack of negative feedback, causing a much greater suppression of conversion noise for low frequencies compared to the Leapfrog. However, the more evenly

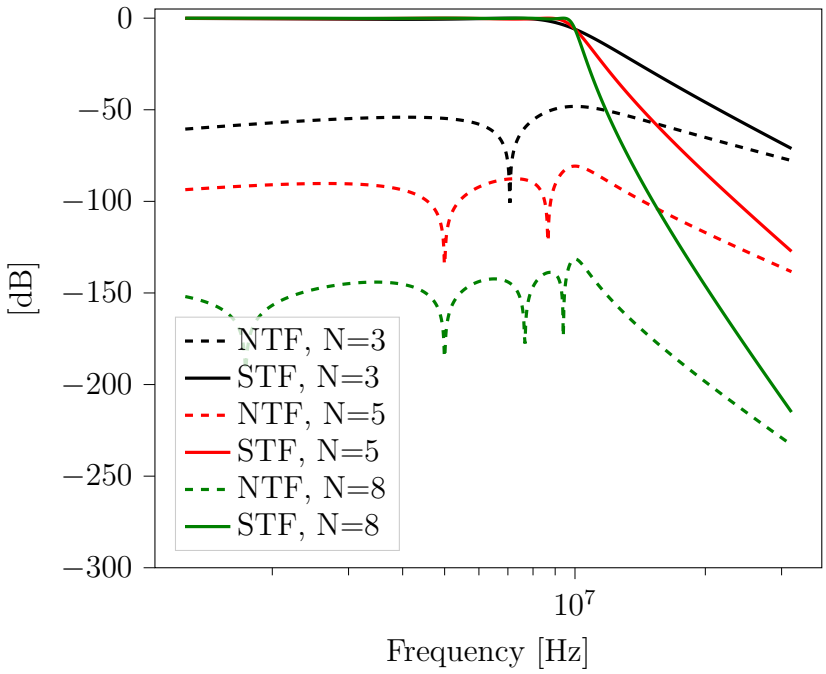


Figure 3.2: Comparison of Leapfrog noise and signal transfer functions for different system orders

distributed quantization noise suppression of the Leapfrog will typically increase the overall performance in the presence of thermal noise.

Finally it should be noted that the Leapfrog ADC will have ripples in the pass band. The origination of these ripples is understood from equation (2.22) when considering that $\boldsymbol{G}(\omega)$ is not strictly decreasing in ω. At the pole frequencies, $||\boldsymbol{G}(\omega)||_2 = \infty$ and STF $= 1$. Between the pole frequencies, $||\boldsymbol{G}(\omega)||_2 < \infty \implies$ STF < 1, which is seen as pass band ripples.

For a given bandwidth, the amount of ripples depends on the parameter ω_p. Figure 3.4 shows the NTF and STF for the 4th order Leapfrog with three different choices of ω_p for the same f_c. The ripples may be limited by reducing ω_p at the expense of a weaker quantization noise suppression. In this thesis, $\omega_p = 2\pi f_c$ is considered an adequate trade-off.

3.3.2 On the Choice of High-Level Architecture

The Leapfrog filter is one example of an analog system that enables the implementation of an arbitrary transfer function $\boldsymbol{G}(\omega)$. As for $\Sigma\Delta$ modulators, a target loop-filter transfer function could be realized with

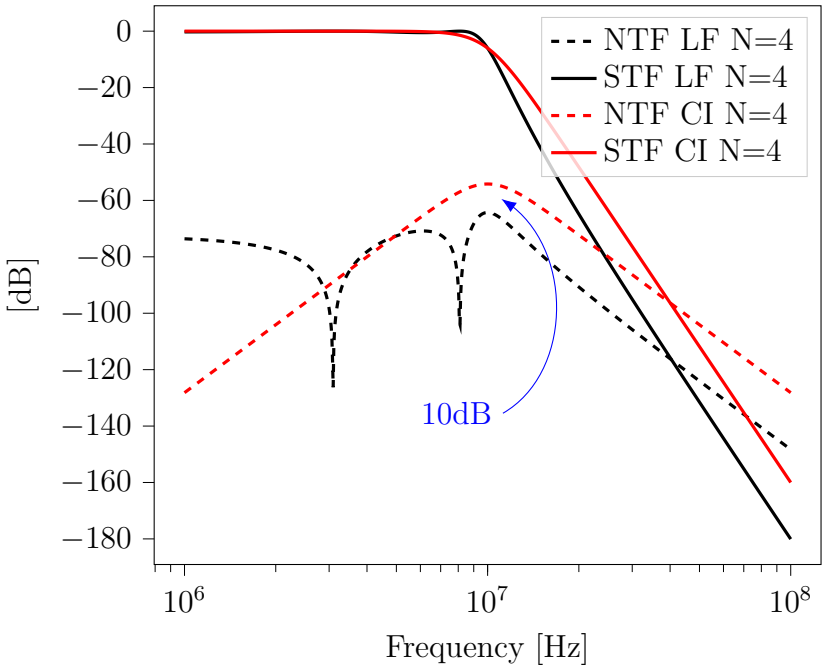
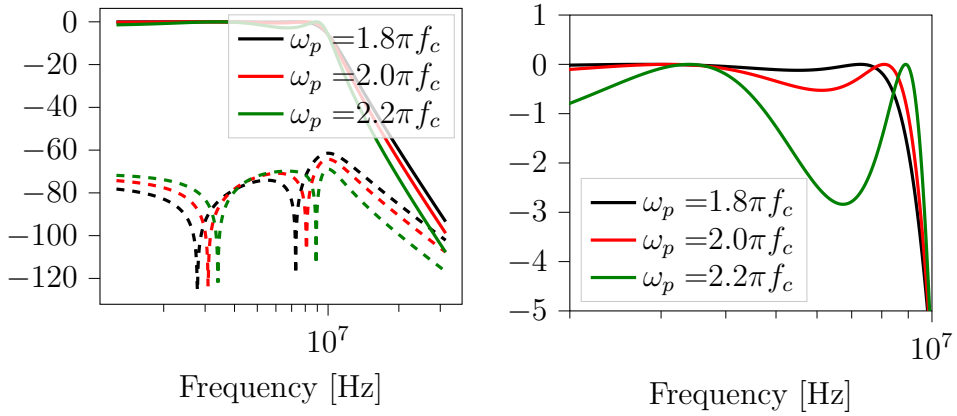


Figure 3.3: Comparison between the noise and signal transfer function of the Leapfrog and the Chain-of-integrators ADC, for a 4th order system



(a) Noise and signal transfer function (b) Ripples in STF pass band enlarged

Figure 3.4: STF and NTF of the Leapfrog ADC for different choices of ω_p

a number of different architectures. However, the choice of architecture in a $\Sigma\Delta$ modulator is mainly related to practical considerations such as linearity and stability [8]. These issues arise from the fact that a (single stage) higher order $\Sigma\Delta$ modulator has only one quantizer in combination with a rather complex loop filter. The choice of architecture will have significant impact on the signal magnitudes processed by different active components, and consequently the linearity and system stability.

As each gain element of the control-bounded converter is stabilized by a dedicated control-loop, its stability and linearity is not as sensitive to the choice of architecture, compared the $\Sigma\Delta$ modulator. There are probably other analog systems than the Leapfrog with interesting and favorable properties, but we argue that the choice of architecture is not as critical for the design of a control-bounded converter as for a $\Sigma\Delta$ modulator. The Leapfrog structure was chosen for the sake of convenient implementation and because a theoretical analysis already exists.

Furthermore, the special case given by equations (3.11) to (3.13) is a considerable limitation of the design space associated with the Leapfrog analog system. Except for tuning ω_p to set the trade-off between pass-band ripples and quantization noise suppression, no effort has been made to find an optimal pole placement.

As highlighted previously in this thesis, a key part of the design strategy is to rely on digital calibration to avoid spending power on implementing high-precision analog circuitry. The involved parameters will be allowed to have significant variations over process, voltage and temperature and the analog transfer function should be designed with a sufficient performance margin to account for these variations. With this design strategy, finding an optimal set of parameters is of limited interest, as the resulting implementation will have considerable variations around this optimum anyway.

3.4 Deviations from Ideality

The special case treated above is considered the ideal case for the Leapfrog ADC, as all integrators have infinite DC gain. This can of course not be the case for real integrators, and the effect of finite DC gain is therefore analysed in this section. We also study the effect of nonlinearities in the integrators on the overall ADC performance.

3.4.1 Finite DC Gain

The effect of finite DC-gain could be treated analytically be computing 3.10 for $\rho_{1-N} \neq 0$. In the special case of $\rho_1 = \rho_2 = \cdots = \rho_N = \rho$, the poles of the system are given by

$$p_N(\omega) = \prod_{k=1}^{N} \left((j\omega + \rho) - j\omega_p \cos\left(\frac{k\pi}{N+1}\right)\right). \tag{3.15}$$

In this case, all poles have the same frequency as in the case of infinite DC-gain, but their position is shifted to the left of the imaginary axis by ρ Hz. When the integrators have different DC-gain, the expression for $p_N(\omega)$ is more involved, but the intuition is the same; the poles are shifted off the imaginary axis, causing more shallow notches in the noise transfer function.

The effect on the noise and signal transfer functions is illustrated in 3.5, for different values of the DC-gain A_0. The transfer functions are computed for a 4th order system where β and ω_p is the same for all integrators. The pole displacement off the imaginary axis is clearly seen for the case of $A_0 = 100$. The poles are visible in the NTF, but the notches are not as deep as for the system having a DC-gain of 1000. When $A_0 = 10$, the poles are no longer visible in the transfer function. Note also that due to the small $||\boldsymbol{G}(\omega)||_2$, $STF < 1$ for $\omega < \omega_c$.

For reasons that will be clear when considering transistor level implementations in a later chapter, it is of special interest to analyze the transfer functions of a system with very small DC-gain only in the first integrator stage. The transfer functions of such a system is illustrated in figure 3.6. The figure shows a system where the first integrator has a DC-gain of $A_{01} = 10$ while the remaining 3 integrators has a DC-gain of $A_{0(2-4)} = 100$. The system where $A_0 = 100$ for all integrators is included for reference. Although the shape of the NTF is clearly affected by the small A_{01}, the STF is almost identical for the two systems. The key takeaway from this figure is that a small DC-gain of the first integrator could be tolerated, conditioned on a higher A_0 in the later stages.

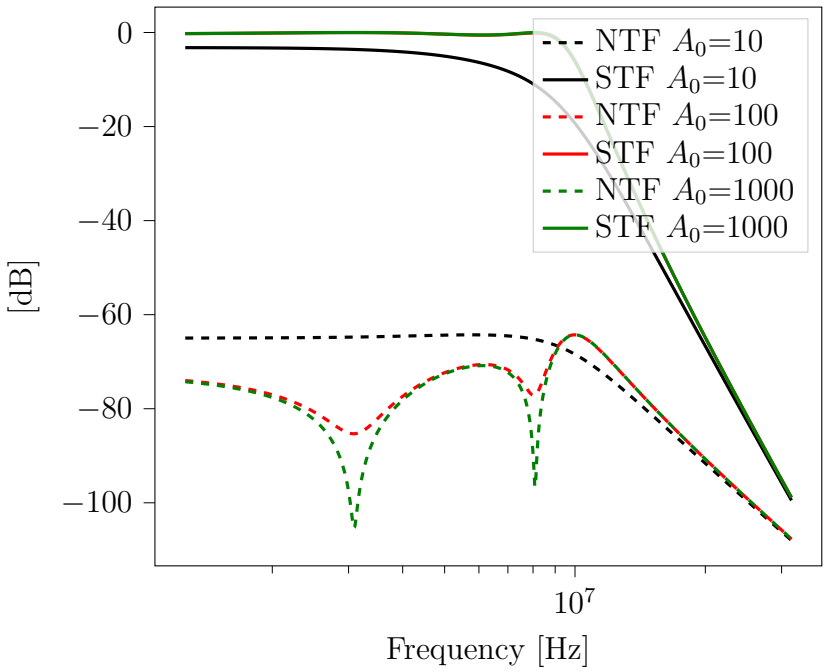


Figure 3.5: Noise and signal transfer functions for various DC-gain A_0

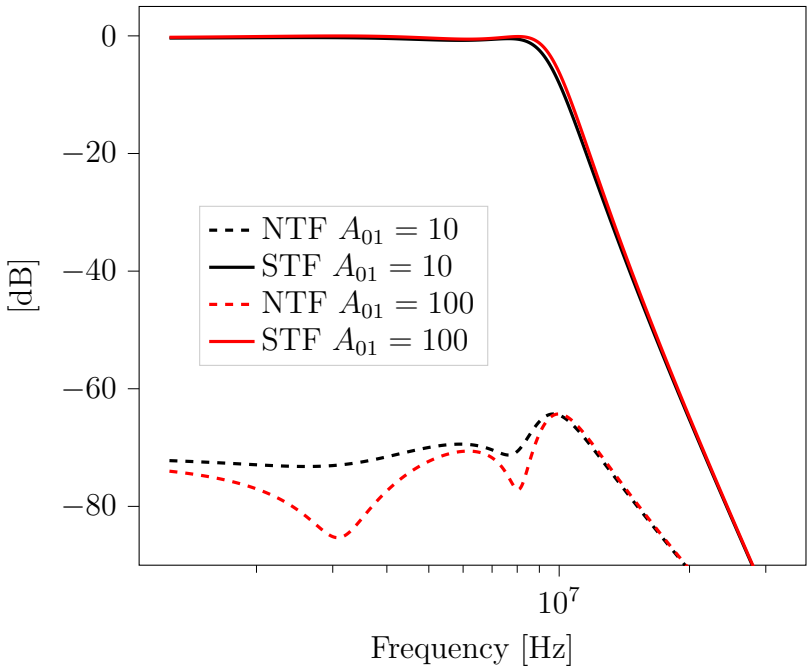


Figure 3.6: Noise and signal transfer functions for a system with $A_0 = 10$ in the first integrator, and $A_0 = 100$ in the other integrators. A system with $A_0 = 100$ for all integrators is included for reference.

3.4.2 Harmonic Distortion

The effect of nonlinear integrators on the overall system performance is, to the best of our knowledge, not treated in literature. This is studied by evaluating a behavioural simulation of the analog system using the Spectre circuit simulator [11]. In this simulation, the integrators are implemented as Gm-C integrators, where the transconductors are modelled as ideal voltage-controlled current-sources and the input voltage of the transconductor is integrated by charging the capacitor C, as shown in figure 3.7. In the ideal case, $i_o(t) = G_m v_i(t)$ and

$$v_o(t) = \frac{1}{C} \int_0^t G_m v_i(\tau) d\tau. \tag{3.16}$$

The nonlinear behaviour is studied by including a second order term in the I-V relationship of the transconductor, such that

$$i_o(t) = G_m v_i(t) + G_2 v_i^2(t). \tag{3.17}$$

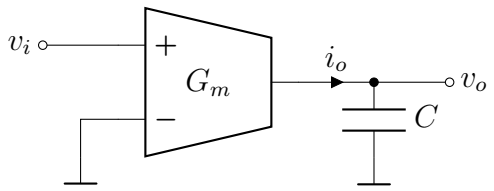


Figure 3.7: Ideal Gm-C integrator used to study nonlinearity

If we assume the input $v_i(t)$ to be a sinusoidal given by $v_i(t) = A\cos(\omega t)$, then

$$i_o(t) = G_m A \cos(\omega t) + G_2 A^2 \cos^2(\omega t) \tag{3.18}$$

$$= \frac{1}{2} + G_m A \sin(\omega t) + G_2 \frac{A^2}{2} \cos(2\omega t). \tag{3.19}$$

The second order harmonic distortion of the transconductor is then given by

$$\mathrm{HD2} = \frac{A}{2} \frac{G_2}{G_m}. \tag{3.20}$$

The actual inputs to the integrators of figure 3.1 is however far from sinusoidal. Even with a one-tone test signal, the one-bit control loop will typically dominate the integrator inputs, making the analysis non-trivial. Nevertheless, the simple result of (3.20) is still useful as a basis for comparison with simulation results.

The effect of nonlinearity is studied by simulating a 4th order Leapfrog ADC, where all integrators are modelled with infinite DC-gain of $A_0 = 100$. The bandwidth is $f_c = 10\,\text{MHz}$, all integrators has $\beta = 2\pi 40\,\text{MHz}$ and $\omega_p = 2\pi f_c$. A second order coefficient $G_2 = {}^{Gm}/_{10}$ is added to the transconductor model of one of the integrators. A sinusoidal with an amplitude of 100mV is applied to the input. The estimated power spectral density (PSD) of $\hat{u}(t)$ is shown in figure 3.8, when the nonlinearity is introduced in the first (black), second (red) and third (green) integrator. The theoretical NTF is included for reference. A quantitative summary is given in table 3.1.

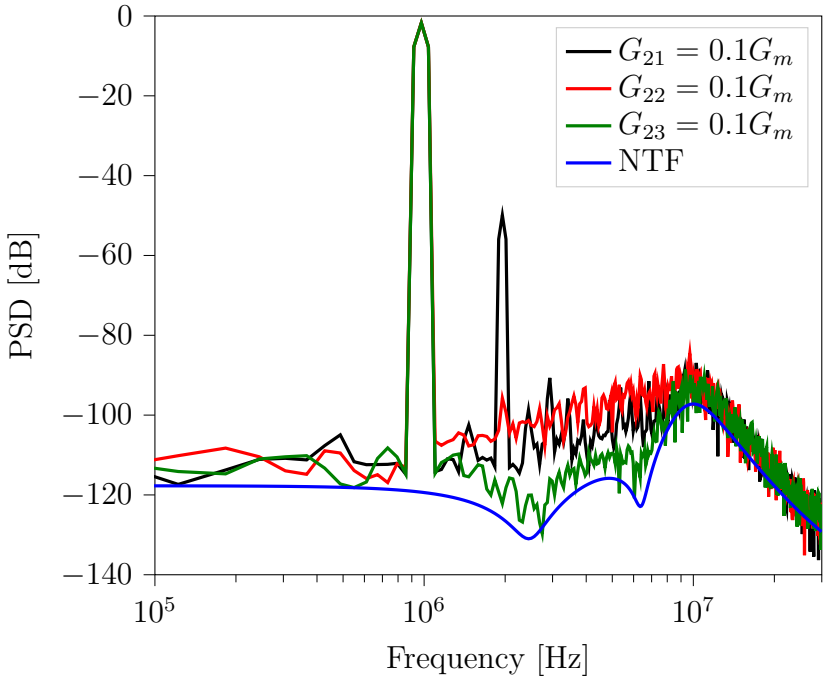


Figure 3.8: Simulated PSD of $\hat{u}(t)$ for the Leapfrog ADC, when the first (black), second (red) and third (green) integrator has a nonlinear coefficient of $G_2 = {}^{G_m}/_{10}$

As expected, the system is mostly sensitive to nonlinearities introduced in the first integrator. When only the first integrator has a nonlinear term of $G_2 = {}^{G_m}/_{10}$, an $\text{HD2}_1 = -48\text{dB}$ appear in the PSD of the ADC output. As a reference, the theoretical expression of equation (3.20) evaluates to

$$\text{HD2}_{r1} = 20\log\left(\frac{100\,\text{mV}}{2}\frac{1}{10}\right) = -46\,\text{dB}. \tag{3.21}$$

Hence, the harmonic distortion generated by the first integrator seem to add more or less directly to the final ADC output. The fact that

Table 3.1: Summary of Nonlinearity Analysis

Parameter	Non-Linear Integrator		
	First	Second	Third
HD2	−48dB	−94dB	N.A.
SNR	−74dB	−72dB	−75dB
SNDR	−48dB	−71dB	−75dB

the $\mathrm{HD2}_1 < \mathrm{HD2}_{r1}$ could be understood by considering that the control contribution constantly counteracts the state growth, such that the magnitude processed by the first integrator will always be somewhat less than the amplitude of the input signal.

Furthermore, due to the feedback-loops of the system, part of the second harmonic energy is "smeared out" in the power spectrum, giving rise to an increased noise floor compared to the theoretical NTF. This effect is particularly evident when the nonlinear term is introduced in the second integrator. In this case, the HD2 is reduced to $-94\,\mathrm{dB}$ at the expense of a slight increasement in conversion noise. As a result, the SNR is almost equal to the signal-to-noise-and-distortion ratio (SNDR) in this case.

To put this number in perspective, consider the HD2 obtained by dividing $\mathrm{HD2}_1$ by the DC-gain of the first integrator. This would give a second harmonic of

$$\mathrm{HD2}_{r2} = -48\,\mathrm{dB} - 20\log(100) = -88\,\mathrm{dB}, \tag{3.22}$$

which is $6\,\mathrm{dB}$ higher than the observed $\mathrm{HD2}_2$.

When only the third integrator has a nonlinear contribution, the HD2 is no longer visible in the final output of this simulation, and the power spectrum follows the theoretical NTF closely.

In summary, harmonic distortion generated by the first integrator of the analog system appear to add more or less directly to the final ADC output. The components implementing this integrator should therefore have as good linearity performance as the overall ADC. However, the Leapfrog ADC seem to be very robust against harmonic distortion introduced by the remaining integrators, which could therefore be implemented with relaxed requirements.

3.5 Stability

In [5], an analytical analysis of the conditions for effective digital control for the Chain-of-integrators ADC is given. It is shown that the local digital control ensures global stability by recursively bounding each state of the analog system, and conditions for the parameters T, β and κ are given.

In this section we extend the analysis to cover the Leapfrog analog system. We show that the same recursive argument applies, even though there are additional feedback paths in the analog system. Although an ideal integrator is a simple first order system, any physical implementation will have additional poles and zeros in the transfer function. The analysis will therefore consider a more general transfer function for the integrators. The implications of digital delay, clock jitter and comparator offset on the stability will also be considered.

The overall goal of this section is show the following:

- For any practical integrator implementation, effective control may be guaranteed by proper choice of control gain κ and control period T.
- With the same conditions on κ and T, if the system becomes unstable due to a strong input signal, the system will always recover to a stable state when the magnitude of the input is decreased.

3.5.1 Conditions for Effective Digital Control

The conditions for effective digital control could in principle be found from (2.15), by evaluating $R(t)$ and $G(t)$ for the system described by (3.2)-(3.4). However, the calculation would be rather involved due to the matrix exponential in $\tilde{\boldsymbol{g}}(t) = \exp(t\boldsymbol{A})$, and a recursive approach is therefore preferred for the sake of a tractable analysis.

Initial Assumptions

The stability of the system could be analyzed recursively by treating $x_2(t)$ as a second input signal, independent of $x_1(t)$. Although this assumption is obviously not true, it can only make the analysis more conservative as stability in this case must be ensured for the worst possible $x_2(t)$. The situation is illustrated in figure 3.9, which shows the first stage of the Leapfrog analog system with $x_2(t)$ modelled as an extra input and the integrator gain, β_1, factorized out of the integration node.

When β_1 is factorized out of the impulse response, we refer to the remaining factor as the *normalized impulse response*, denoted by $\tilde{g}_1(t)$. For an ideal integrator with an infinite DC-gain, $\tilde{g}_1(t) = 1$. However, a finite DC-gain could be represented by a leakage term, ρ, in the normalized impulse response, such that $\tilde{g}_1(t) = e^{-\rho t}$. Furthermore, the normalized step response will be denoted by

$$\text{step}_1(t) = (\tilde{g}_1 * u_h)(t), \tag{3.23}$$

where $u_h(t)$ refers to the Heaviside step function.

In the following analysis, the normalized impulse response is assumed to be non-negative and upper bounded as

$$0 \leq \tilde{g}_1(t) \leq 1 \ \forall t \in [0, T). \tag{3.24}$$

A justification of this assumption is given in appendix B.

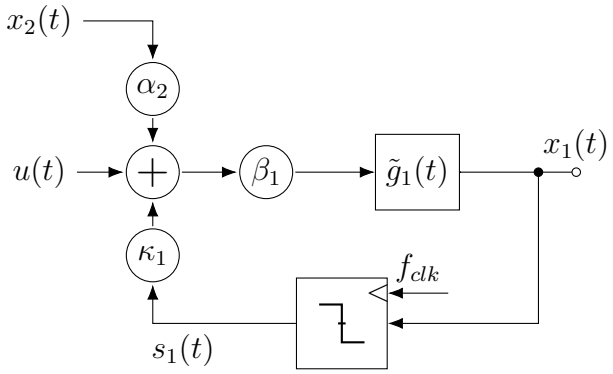


Figure 3.9: The first stage of the Leapfrog analog system, when the integrator gain β_1 is factorized out of the integration node and $x_2(t)$ is modelled as an additional independent input signal.

Evaluating the Growth and Remainder Term

Let

$$R_1(t) = \max_{x_1(0) \in [-b_{\boldsymbol{x}}, b_{\boldsymbol{x}}]} |\tilde{g}_1 \cdot x_1(0) + (\tilde{g}_1 * \beta_1 \kappa_1 s_1)(t)|, \tag{3.25}$$

and

$$G_1(t) = \max_{u(t) \in \mathcal{U}, x_2(t) \in \mathcal{X}} |(\tilde{g}_1 * \beta_1 u)(t) + (\tilde{g}_1 * \beta_1 \alpha_2 x_2)(t)| \tag{3.26}$$

denote the growth and remainder term for the first stage, respectively. By the assumption of equation (3.24), the remainder term is bounded as

$$R_1(t) \leq \max_{x_1(0)\in[-b_{\boldsymbol{x}},b_{\boldsymbol{x}}]} |x_1(0) + (\tilde{g}_1 * \beta_1\kappa_1 s_1)(t)|, \tag{3.27}$$

By the triangle inequality, $G_1(t)$ is upper bounded as

$$G_1(t) \leq G_1^u(t) + G_1^{x_2}(t), \tag{3.28}$$

where

$$G_1^u(t) \triangleq \max_{u(t)\in\mathcal{U}} |(\tilde{g}_1 * \beta_1 u)(t)| \tag{3.29}$$

and

$$G_1^{x_2}(t) \triangleq \max_{x_2(t)\in\mathcal{X}} |(\tilde{g}_1 * \beta_1\alpha_2 x_2)(t)| \tag{3.30}$$

is the growth term contribution from the input $u(t)$ and the second state $x_2(t)$ respectively. The condition for effective digital control is then written as

$$\max_{t\in[0,T)} (G_1^u(t) + G_1^{x_2}(t) + R_1(t)) < b_{\boldsymbol{x}}. \tag{3.31}$$

Before (3.31) can be evaluated, the worst case (but bounded) signals $u(t)$ and $x_2(t)$, for $t \in [0, T)$, must be determined. For a system with normalized impulse response $\tilde{g}_1(t)$, $\max_{t\in[0,T)} |x_1(t)|$ is maximized by the input signal

$$u(t) = \begin{cases} b_u & \text{if } \tilde{g}_1(t) \geq 0 \\ -b_u & \text{if } \tilde{g}_1(t) < 0 \end{cases} \tag{3.32}$$

and

$$x_2(t) = \begin{cases} b_{\boldsymbol{x}} & \text{if } \tilde{g}_1(t) \geq 0 \\ -b_{\boldsymbol{x}} & \text{if } \tilde{g}_1(t) < 0 \end{cases} \tag{3.33}$$

Hence, by the assumption of equation (3.24), the growth terms is evaluated as

$$G_1^u(t) = \max_{u(t)\in\mathcal{U}} |(\tilde{g}_1 * \beta_1 u)(t)| = b_u\beta_1 \mathrm{step}_1(t) \tag{3.34}$$

and

$$G_1^{x_2}(t) = \max_{x_2(t)\in\mathcal{X}} |(\tilde{g}_1 * \beta_1\alpha_2 x_2)(t)| = b_{\boldsymbol{x}}\beta_1\alpha_2 \mathrm{step}_1(t) \tag{3.35}$$

In the following, assume that the threshold of the digital control is such that

$$s_1(t) = \begin{cases} +1 & \text{if } x(0) \geq 0 \\ -1 & \text{if } x(0) < 0 \end{cases} \tag{3.36}$$

When evaluating the remainder term, two extreme cases must be considered. The first case is when $x(0) \approx 0$, causing the contribution from the control to superimpose with the growth term. The second extreme case is when $x(0) = b_{\boldsymbol{x}}$, at which the control must reduce the magnitude of the state at a rate higher than the growth rate. As a result, the remainder term could be expressed as

$$R_1(t) = \max_{x_1(0)\in[-b_{\boldsymbol{x}},b_{\boldsymbol{x}}]} |\tilde{g}_1(t) \cdot x_1(0) + (\tilde{g}_1 * \beta_1\kappa_1 s_1)(t)| \tag{3.37}$$

$$\leq \max_{x_1(0)\in[-b_{\boldsymbol{x}},b_{\boldsymbol{x}}]} \{\kappa_1\beta_1 \text{step}_1(t), b_{\boldsymbol{x}} - \kappa_1\beta_1 \text{step}_1(t)\} \tag{3.38}$$

The Conditions for Effective Control

The conditions for effective control is then found by evaluating the expression (3.31) for the two extreme cases, giving

$$(b_u + \alpha_2 b_{\boldsymbol{x}} + \kappa_1) \cdot \beta_1 \text{step}_1(T) < b_{\boldsymbol{x}} \tag{3.39}$$

and

$$(b_u + \alpha_2 b_{\boldsymbol{x}} - \kappa_1) \cdot \beta_1 \text{step}_1(T) + b_{\boldsymbol{x}} < b_{\boldsymbol{x}}, \tag{3.40}$$

which may be simplified to

$$\kappa_1 > b_u + \alpha_2 b_{\boldsymbol{x}} \tag{3.41}$$

$$\text{step}_1(T) < \frac{1}{\beta_1} \frac{b_{\boldsymbol{x}}}{b_u + \alpha_2 b_{\boldsymbol{x}} + \kappa_1}. \tag{3.42}$$

For a given integrator, the control gain κ_1 could then be chosen according to (3.41) and finally the control period T according to (3.42). This approach will ensure that the next node of the system also receive a bounded input. By applying this approach to each stage, an effective control is recursively guaranteed for the whole analog system.

Finally, it is worth to note that for systems with $\alpha < 0$, the additional feedback paths of the Leapfrog analog system reduces the requirements on the digital control, relative to that of the Chain-of-integrators. In other words, if a digital control is effective on a Chain-of-integrators analog system, introducing feedbacks $\alpha < 0$ will only improve the stability.

3.5.2 Digital Delay and Clock Jitter

Let $t = 0$ denote the time when a new control contribution enters the analog system. If the control loop was completely delay-free, then $\boldsymbol{s}(t), t \in$

$[0, T)$ would be produced by the digital control as a response to $\tilde{\mathbf{\Gamma}}\boldsymbol{x}(0)$. However, in a real system there will be some delay ΔT from the digital control is activated by the clock signal, to the control contribution enters the analog system. This could be accounted for by replacing $x_1(0)$ by $x_1(-\Delta T)$ in the above analysis, which would not change the result.

Clock jitter will cause the control period to vary with time. A stability margin could be introduced to account for this effect by lowering the (target) clock period T. An effective control could then be guaranteed, also when T is increased from its nominal value.[1]

3.5.3 Comparator Offset Voltage

In the analysis of section 3.5.1, the digital control observing $x_1(t)$ was assumed to have a threshold at $x(0) = 0$. In a real circuit implementation however, there will be an offset on the threshold voltage. By returning to the two worst-case scenarios of the remainder term, equation (3.37), it is evident that a threshold offset will only influence the case when $x(0) \approx 0$. Assume the (worst case) threshold voltage of the comparator is δ_c, such that equation (3.36) modifies to

$$s_1(t) = \begin{cases} +1 & \text{if } x(0) \geq \delta_c \\ -1 & \text{if } x(0) < \delta_c \end{cases} \tag{3.43}$$

In consequence, the conditions for effective control modifies to

$$\kappa_1 > b_u + \alpha_2 b_{\boldsymbol{x}} \tag{3.44}$$

$$\text{step}_1(T) < \frac{1}{\beta_1} \frac{b_{\boldsymbol{x}} - |\delta_c|}{b_u + \alpha_2 b_{\boldsymbol{x}} + \kappa_1}. \tag{3.45}$$

Equation (3.45) shows that an offset in threshold voltage could be accounted for by reducing the βT product. To maintain the stability guarantee, a reduction of $\frac{|\delta_c|}{b_u + \alpha_2 b_{\boldsymbol{x}} + \kappa_1}$ is required. Reducing T, by increasing the clock frequency, will typically increase the power consumption, whereas reducing β amounts to increased conversion noise power, cf. (2.25). The required reduction in the βT product could be reduced by allowing a larger state magnitude, i.e. increasing $b_{\boldsymbol{x}}$. This would however also increase conversion noise according to equation (2.25).

[1] It is worth to note that although digital delay and clock jitter is not a big issue from a stability point of view, it would have a significant impact on the quality $\hat{u}(t)$ if not accounted for by the digital estimator.

However, if the system is designed such that an offset of δ_c does not make the control ineffective, the quality of $\hat{u}(t)$ will not be affected at all. Note also that this holds for static as well as time-varying offsets, given that the maximum offset voltage is upper bounded by δ_c.

3.5.4 Return to Stability

It is a common issue that if a higher order $\Sigma\Delta$ modulator becomes unstable, it might never return to stability, even when the magnitude of $u(t)$ is decreased [9]. We now show that if κ_1 and T is chosen according to (3.41) and (3.42), the Leapfrog analog system will always return to stability if $|u(t)|$ is reduced below b_u.

Let $\kappa_1 = b_u + \alpha_2 b_{\boldsymbol{x}} + \delta_\kappa$, where $\delta_\kappa > 0$ is the margin on the control gain cf. equation (3.41). From (3.42), the control period is then upper bounded by

$$\begin{aligned} \text{step}_1(T) &< \frac{b_{\boldsymbol{x}}}{\beta_1 \left(b_u + \alpha_2 b_{\boldsymbol{x}} + \kappa_1\right)} && (3.46) \\ &= \frac{b_{\boldsymbol{x}}}{\beta_1 \left(2(b_u + \alpha_2 b_{\boldsymbol{x}}) + \delta_\kappa\right)} && (3.47) \\ &= \frac{1}{\beta_1 \left(2\left(\alpha_2 + \frac{b_u}{b_{\boldsymbol{x}}}\right) + \frac{\delta_\kappa}{b_{\boldsymbol{x}}}\right)} && (3.48) \end{aligned}$$

Assume that $|x_2(0)| = b_{\boldsymbol{x}} + \delta_{x2} > b_{\boldsymbol{x}}$ due to the recent presence of an unbounded input signal. To show that the system will return to stability, we again consider the two extremes, i.e. when $|x_1(0)| \approx 0$ and when $|x_1(0)| = b_{\boldsymbol{x}} + \delta_{x1}$. For the first case, it must be shown that $|x_1(T)| < b_{\boldsymbol{x}} + \delta_{x2}$ for $|x_1(0)| = 0$. This would imply that the next input to the subsequent stage is less than its previous output, which by recursion ensures that the system will return to stability. In this case, $|x_1(T)|$ is

given by

$$
\begin{aligned}
|x_1(T)| &< (b_u + \alpha_2(b_{\boldsymbol{x}} + \delta_{x2}) + \kappa_1)\beta_1 \cdot \mathrm{step}_1(T) && (3.49)\\
&= \alpha_2\delta_{x2}\beta_1 \cdot \mathrm{step}_1(T) + \underbrace{(b_u + \alpha_2 b_{\boldsymbol{x}} + \kappa_1)\beta_1 \cdot \mathrm{step}_1(T)}_{<b_{\boldsymbol{x}} \text{ by } (3.39)} && (3.50)\\
&< \alpha_2\delta_{x2}\beta_1 \cdot \mathrm{step}_1(T) + b_{\boldsymbol{x}} && (3.51)\\
&< \alpha_2\delta_{x2}\beta_1 \cdot \frac{1}{\beta_1\left(2\left(\alpha_2 + \frac{b_u}{b_{\boldsymbol{x}}}\right) + \frac{\delta_\kappa}{b_{\boldsymbol{x}}}\right)} + b_{\boldsymbol{x}} && (3.52)\\
&= \delta_{x2}\frac{\alpha_2}{2\left(\alpha_2 + \frac{b_u}{b_{\boldsymbol{x}}}\right) + \frac{\delta_\kappa}{b_{\boldsymbol{x}}}} + b_{\boldsymbol{x}} && (3.53)\\
&< \delta_{x2} + b_{\boldsymbol{x}} && (3.54)
\end{aligned}
$$

For the other extreme scenario, $|x_1(0)| = b_{\boldsymbol{x}} + \delta_{x1} > b_{\boldsymbol{x}}$. It must now be shown that $|x_1(T)| < b_{\boldsymbol{x}} + \delta_{x2} + \delta_{x1}$, as this would by the same argument ensure that the system returns to stability. $|x_1(T)|$ is now given by

$$
\begin{aligned}
|x_1(T)| &< (b_u + \alpha_2(b_{\boldsymbol{x}} + \delta_{x2}) - \kappa_1)\beta \cdot \mathrm{step}_1(T) + b_{\boldsymbol{x}} + \delta_{x1} && (3.55)\\
&= \underbrace{\alpha_2\delta_{x2}\beta_1 \cdot \mathrm{step}_1(T)}_{<\delta_{x2}} + \underbrace{(b_u + \alpha_2 b_{\boldsymbol{x}} - \kappa_1)\beta \cdot \mathrm{step}_1(T) + b_{\boldsymbol{x}}}_{<b_{\boldsymbol{x}} \text{ by } (3.40)} + \delta_{x1} && (3.56)\\
&< b_{\boldsymbol{x}} + \delta_{x2} + \delta_{x1}, && (3.57)
\end{aligned}
$$

which concludes the proof.

3.5.5 Tuning Parameters by Computer Simulations

As seen from expression (2.25), the overall performance of the ADC is improved by increasing the gain of the analog system. Increasing the gain for a given control period T, would imply increasing the $\beta\mathrm{step}_1(T)$ product. The conditions (3.41) and (3.42) guarantees that the system will remain stable for any combination of a bounded input signal and initial state vector. Designing the system for a stability guarantee will for most of the time result in a large stability margin, meaning that there are potential performance increasement not being utilized. The preferred way of tuning κ and T is therefore through extensive use of computer simulations, thereby accepting a risk of instability for certain bounded input signals. The theoretical conditions presented above will however still serve as a useful starting point.

It should be noted that even though the conditions for effective control is violated, the system will still recover to stability the same way as shown in section 3.5.4. To see this, assume that κ_1 and T is such that condition (3.41) and (3.42) is violated. Furthermore, assume that the system is self-stable, i.e. stable when $u(t) = 0\ \forall t$, which requires $\text{step}_1(T) < {}^1/_{\beta\kappa}$. Given that the assumption of equation (3.24) still holds, there will exist other boundaries $\hat{b}_u < b_u$ and $\hat{b}_{\boldsymbol{x}} < b_{\boldsymbol{x}}$ for which an effective control is still guaranteed. Suppose that $||\boldsymbol{x}(t)||_\infty$ exceeds $b_{\boldsymbol{x}}$ at some time t due to a an input $\hat{b}_u < |u(t)| < b_u$. By replacing b_u and $b_{\boldsymbol{x}}$ by $\hat{b}_u$ and $\hat{b}_{\boldsymbol{x}}$, the same argumentation as above could be used to show that the system will return to stability when the magnitude of the input signal is reduced.

Chapter 4

Software Tools

The scope of this thesis is limited to design considerations for the analog system and the digital control of the Leapfrog ADC. However, as the control signals $\boldsymbol{s}[k]$, relates to the final ADC output $\hat{u}(t)$ in a nontrivial way, an offline implementation of the digital estimator is needed for evaluating the performance of these systems. For this purpose, we use the recently published Python package *Control-Bounded A/D Conversion Toolbox*, written by Hampus Malmberg [12]. The package provides tools for simulating a parametric system on a state-space equation level, evaluating transfer functions as well as several different implementations of the digital estimation filter.

4.1 Python Based Analog Design Environment

To interface with this toolbox, a custom Python framework for analog circuit simulation, called *Python based Analog Design Environment* (PADE), is developed. The package is primarily written for personal usage and the documentation is currently thereafter. The curious reader might check out the latest version on github [13]. The package aims to provide a Python-alternative to the most essential functionality of the Cadence Virtuoso Analog Design Environment, which is considered the industry standard of software tools for analog circuit design. The package covers three main topics, schematic generation, simulation and evaluation.

Circuit schematics are generated in an object-oriented way, using the four abstract classes Design, Cell, Terminal and Net. A component is

declared as a new class inheriting from Cell. In the constructor, subcells are instantiated and stored as attributes, by connecting their terminals to internal nets of the cell. Finally, a testbench is declared as a new class by inheriting from Design. Inside its constructor, components, stimuli and supply voltage are connected to nets, similar to the construction of a cell.

The convenience of this approach is that the design procedure could easily be parameterized and repetitions can be executed in for-loops. This way, major changes on both component and system level may be achieved by modifying a few parameters on top level. Chain-structures like the Leapfrog analog system is particularly well-suited for this design methodology, as the order of the system is controlled by a single parameter N. The unity-gain frequencies of the different integrators could also be controlled efficiently by parameterizing $^{W}/_{L}$ ratios of the transistors, bias currents and capacitor values. This approach has shown to be significantly time-saving, compared to the conventional method of manually drawing circuit schematics in a graphical user interface.

Spectre is used for circuit simulations in this project, and the interface to the simulator is handled by the a custom Spectre class. The constructor takes a design object, a list of analyses to run and eventual options and info statements. The Spectre object compiles the netlist and runs the simulation using the command line interface, typically at a remote server.

The raw simulation data are parsed using the psf-utils python package written by Ken Kundert [14]. The functionality of this package is wrapped in a custom PSFParser class, which includes some additional helper functions for accessing traces from different analyses, corner simulations etc. The framework integrates with Numpy and Scipy for evaluation raw data, and Pandas for convenient representation of results.

Monte Carlo (MC) simulations is performed using the montecarlo analysis statement of spectre. For corner simulations, the same simulation is run several times with different settings specified for process file, temperature and eventually supply voltage.

To limit the amount of code needed for a single simulation script, this functionality is handled in the high-level Test class. For the reader that is experienced with Cadence Virtuoso, the Test class is equivalent to the Explorer view. A Test object is instantiated with a Design, analyses, corners (or MC) settings and expressions. By running the test, the expressions are evaluated for each corner/MC run and a result table is generated. The complexity of the expression could be anything from a

simple np.abs() to a function performing offline calibration, running the reconstruction filter, calculating PSD and returning SNR and harmonic distortion. Due to the versatility of the Test class, the amount of code needed for simulating a new design is limited, and a single top-level script could be used on several different designs.

The simulation process typically start by declaring a testbench class inheriting from Design. This testbench class is then instantiated in a top level script, from which simulation, parsing and evaluation is handled. A few examples are available on GitHub.

4.2 Offline AC Calibration

The digital estimator is parameterized by the matrices $\boldsymbol{A}, \boldsymbol{B}, \boldsymbol{C}^{\mathsf{T}}, \boldsymbol{\Gamma}, \tilde{\boldsymbol{\Gamma}}$, the bandwidth parameter η and the control period T. Even for a nominal computer simulation, finding the matrix coefficients that actually describes the implemented system might be cumbersome, as several capacitors and transistor parameters will be involved. Furthermore, even minor changes in the circuit might affect several parameters and recalculation of matrix coefficients would therefore be time a consuming task.

The fact that the parametrization of the digital estimator at any time need to match the behaviour of the analog system, introduce an additional complicating factor when working with control-bounded converters. Errors due to wrong filter coefficients could show up as harmonic distortion or increased noise floor in the power spectrum of $\hat{u}(t)$. It could therefore be hard to tell if the observed errors comes from the actual circuit implementation, or just the wrong filter coefficients.

To address these issues, an offline calibration algorithm is implemented. The algorithm calibrates the system in the frequency domain using a linearized ac analysis. The algorithm calibrates the $\boldsymbol{A}$ and $\boldsymbol{B}$ matrices, but the control matrix $\boldsymbol{\Gamma}$ is still calculated manually. The $\boldsymbol{A}$ and $\boldsymbol{B}$ matrices are calibrated using a simple ac source at the input of the analog system and the system does not need any modifications before calibration. Calibrating the control matrix $\boldsymbol{\Gamma}$ would on the other hand require multiple runs, with an ac source connected to one of the control signal inputs for each run. As the coefficients of $\boldsymbol{\Gamma}$ typically relates to β by some scale factor, it was considered more convenient to calculate these parameters manually.

The ac analysis performs a frequency sweep of length L from f_1 to f_L.

The input vector

$$\boldsymbol{U}(j\omega) = (U(j\omega_1), U(j\omega_2), \cdots U(j\omega_L)) \in \mathbb{C}^{1\times L}, \tag{4.1}$$

the state matrix

$$\boldsymbol{X}(j\omega) = \begin{pmatrix} X_1(j\omega_1) & X_1(j\omega_2) & \cdots & X_1(j\omega_L) \\ X_2(j\omega_1) & X_2(j\omega_2) & \cdots & X_2(j\omega_L) \\ & \vdots & & \\ X_N(j\omega_1) & X_N(j\omega_2) & \cdots & X_N(j\omega_L) \end{pmatrix} \in \mathbb{C}^{N\times L} \tag{4.2}$$

and its derivative

$$\dot{\boldsymbol{X}}(j\omega) = \begin{pmatrix} j\omega_1 X_1(j\omega_1) & j\omega_2 X_1(j\omega_2) & \cdots & j\omega_L X_1(j\omega_L) \\ j\omega_1 X_2(j\omega_1) & j\omega_2 X_2(j\omega_2) & \cdots & j\omega_L X_2(j\omega_L) \\ & \vdots & & \\ j\omega_1 X_N(j\omega_1) & j\omega_2 X_N(j\omega_2) & \cdots & j\omega_L X_N(j\omega_L) \end{pmatrix} \in \mathbb{C}^{N\times L} \tag{4.3}$$

is created from the simulation output.

From (2.2) we write

$$\dot{\boldsymbol{X}}(j\omega) = \boldsymbol{B}\boldsymbol{U}(j\omega) + \boldsymbol{A}\boldsymbol{X}(j\omega) \tag{4.4}$$

$$\dot{\boldsymbol{X}}(j\omega) = \begin{bmatrix}\boldsymbol{B} & \boldsymbol{A}\end{bmatrix} \begin{bmatrix}\boldsymbol{U}(j\omega) \\ \boldsymbol{X}(j\omega)\end{bmatrix} \tag{4.5}$$

$$\begin{bmatrix}\boldsymbol{U}(j\omega)^\mathsf{T} & \boldsymbol{X}(j\omega)^\mathsf{T}\end{bmatrix} \begin{bmatrix}\boldsymbol{B}^\mathsf{T} \\ \boldsymbol{A}^\mathsf{T}\end{bmatrix} = \dot{\boldsymbol{X}}(j\omega)^\mathsf{T} \tag{4.6}$$

The system of linear equations (4.6) will typically not have an exact solution. Let

$$\hat{\dot{\boldsymbol{X}}}(j\omega)^\mathsf{T} \triangleq \begin{bmatrix}\boldsymbol{U}(j\omega)^\mathsf{T} & \boldsymbol{X}(j\omega)^\mathsf{T}\end{bmatrix} \begin{bmatrix}\boldsymbol{B}^\mathsf{T} \\ \boldsymbol{A}^\mathsf{T}\end{bmatrix}. \tag{4.7}$$

We then formulate the calibration as a least squares problem and find the coefficients of $\boldsymbol{A}$ and $\boldsymbol{B}$ such that the average square error (ASE)

$$\text{ASE} = \frac{1}{NL}\sum_{n,\ell} \left| \hat{\dot{\boldsymbol{X}}}(j\omega)^\mathsf{T}_{n,\ell} - \dot{\boldsymbol{X}}(j\omega)^\mathsf{T}_{n,\ell} \right|^2 \tag{4.8}$$

is minimized. The matrix $[\boldsymbol{B}\ \boldsymbol{A}]^\mathsf{T}$ that minimizes (4.8) is given by the linear equations

$$\begin{bmatrix}\boldsymbol{U}(j\omega)^\mathsf{T} & \boldsymbol{X}(j\omega)^\mathsf{T}\end{bmatrix}^\mathsf{H} \hat{\dot{\boldsymbol{X}}}(j\omega)^\mathsf{T} = \begin{bmatrix}\boldsymbol{U}(j\omega)^\mathsf{T} & \boldsymbol{X}(j\omega)^\mathsf{T}\end{bmatrix}^\mathsf{H} \dot{\boldsymbol{X}}(j\omega)^\mathsf{T} \tag{4.9}$$

which is solved using the Scipy linear algebra package (see e.g. [15] for reference on higher dimensional least squares problems).

The choice of start and stop frequency, f_1 and f_L, and the number of frequency points, L, will have a significant impact on the quality of the calibration. The frequency range should at least include the unity gain frequency of the integrators as well as any pole frequencies. The frequency range used in this implementation was $f_1 = 100\text{kHz}$ and $f_2 = 1\text{GHz}$. Increasing L will typically yield better performance at the expense of increased simulation and computation time. $L = 1000$ is considered an adequate trade-off in this thesis.

The calibration algorithm has shown to estimate the parameters β, α, κ and ρ with very high precision. The remaining matrix coefficients however, whose true value is zero, might be given with large non-zero values. These coefficients are therefore manually zeroed before initializing the digital estimator.

4.3 Project Specific Software

As PADE is written to be a general purpose toolbox for analog circuit design, any control-bounded ADC specific functionality is placed in a separate repository. Due to confidential, technology-specific information, this repository is not available to the public.

The repository contains top-level scripts, project-specific libraries and utility functions. The library contains class declarations inheriting from Design (testbenches) and Cell (components). It has been find convenient to keep the top-level scripts as general as possible and keep architecture specific parameters inside the testbench classes. The ac calibration algorithm described above is placed in the utility module together with functions for running the estimation filter, evaluating PSD etc.

Chapter 5

Design Considerations

Chapter 3 introduced the Leapfrog analog system and digital control on a behavioural level. The essential theoretical background and effects of important non-idealities on the transfer function was studied. In this chapter we explore the design space associated with the implementation of this system on transistor level.

Several crucial design choices remains for the transition from this system of state-space equations to an electrical circuit implementation. Up until this point of the thesis, we have treated all signals, $u(t)$, $\boldsymbol{x}(t)$, $\boldsymbol{s}(t)$ etc., as unitless, information carrying quantities. When creating a circuit implementation of the desired state-space model, these information signals must be assigned to currents or voltages of different nodes of the analog system. The different physical properties of the two domains introduce an additional complicating factor into the design process.

In a future continuation of this project, a complete ADC will be designed to meet the specifications listed in table 1.1 with the smallest possible power consumption. Rather than achieving a complete functional implementation, the primary focus of this work have been to look for unconventional solutions exploiting the unique properties of the control-bounded conversion framework. By exploring challenges and opportunities with different architectures we seek to provide a useful background for future development.

The chapter is structured as follows. Section 5.1 is concerned with the choice of integrator topology for the first stage of the system. In section 5.2, we study architectural implementation challenges associated with the implementation of the summation nodes and behavioural simulation results is presented. section 5.3 presents circuit ideas for the in-

volved active components and the effect of their non-ideal behaviour on the overall ADC performance is studied. Finally, section 5.4 concludes the chapter and summarize the key results of the design considerations.

5.1 The First Integrator

As with most conventional low-power ADCs, thermal noise will be a major performance limiting factor. The general effect of thermal noise was analyzed in section 2.5.3 and equation (2.33) gives the contribution to the total output noise power for a thermal noise source entering at some position of the analog system. As expected, the noise contribution is most significant for the sources entering early in the signal flow, where $||\boldsymbol{G}_z(\omega)||_2$ is largest. Although the effect of non-linear active components is not analysed analytically, we showed in section 3.4.2 that the output estimate is mostly sensitive to harmonic distortion in the first stage. Together with the need for single-ended to differential conversion, these requirements makes the first integrator a critical design challenge.

The analog system of a control-bounded converter shares several similarities with the loop filter of continuous-time $\Sigma\Delta$ modulators in terms of the analog signal processing tasks required. State-of-the-art solutions for these modulators is therefore a natural place to look for inspiration on the design of the control-bounded converters analog system.

5.1.1 Discussion of Prior Works

For applications where a low input impedance is tolerated, an operational transconductance amplifier (OTA)-RC based integrator is a popular choice due to its excellent linearity performance [16]. However, according to the specifications of table 1.1, high capacitive input impedance is required, which excludes this topology at least for the first stage.

Gm-C based integrators on the other hand, provides inherently high input impedance, but additional linearization techniques are typically required due to the non-linear open-loop Gm-cell. Source degeneration is a popular way of linearizing the transconductor at the expense of increased current consumption. A spurious-free dynamic range (SFDR) of about 90 dB is reported in state-of-the-art Gm-C based $\Sigma\Delta$ modulators [17–19]. For a degeneration resistance of R_s, an effective transconductance of $G_{m,eff} \approx \frac{1}{R_s}$ is achieved, given that $g_{m1} >> \frac{1}{R_s}$ when g_{m1} is the transconductance of the input transistors. However, this implies that the noise generated by this resistor will add directly to the input referred

noise voltage of the transconductor [20]. Reducing this noise contribution by reducing R_s would require a higher g_{m1} for the same linearity performance. A significant bias current would therefore be required in order to simultaneously achieve sufficient linearity and noise performance.

A discussion of additional linearization techniques for Gm-C based $\Sigma\Delta$ modulators is found in [20]. These are all based on using the feedback DAC of the modulator to reduce the input voltage magnitude processed by the transconductor. As the digital control of the Leapfrog ADC provides a one-bit feedback, the voltage swing reduction achievable from this approach is in our case limited.

An alternative approach is to use an RC low-pass filter as a passive integrator, which is shown to be an energy-efficient alternative to a power-hungry OTA at the ADC input [21, 22]. However, due to the resistive input impedance, this solution cannot be applied directly when a high capacitive input impedance is needed.

5.1.2 LNA Driven, Passive Integrator

The proposed solution is shown in figure 5.1. It comprises a passive RC integrator, driven by an LNA. This approach achieves single ended to differential conversion and utilizes the good linearity and low noise performance of the OTA, without the need for a resistive input. The input signal $u(t)$ is amplified by $-\frac{C_1}{C_2}$ and the integration is obtained by charging $C_{\beta 1}$ through the resistor $R_{\beta 1}$. The voltage on this capacitor is treated as the first stage signal $x_1(t)$, which is observed and stabilized by a local digital control.

Two solutions are considered for the interface between the control signal $s_1(t)$ and the state $x_1(t)$. The architecture presented in [21] use a resistive DAC (RDAC) for the modulator feedback. Adapting this solution to the 1-bit control-bounded converter would result in the implementation marked red on figure 5.1. The main disadvantage of this approach is that the comparator used for digital control would need to drive a resistive load, and a voltage buffer would be required at its output. Moreover, connecting an additional resistor to the x_1 node would influence the behaviour of the passive integrator. This might not be a fundamental problem, but the reconstruction filter would need some modifications in order to account for this effect.

A simpler solution from an implementation point of view, is to feed the control signal to the virtual ground of the OTA via a capacitor $C_{\kappa 1}$ (in-

dicated in blue on figure 5.1). As $C_{\kappa 1}$ could be very small, the design requirements on the comparator is relaxed, enabling a more power efficient implementation. The two main disadvantages of this approach is related to noise and OTA bandwidth requirements. The binary control contribution requires the OTA output to settle within a small fraction of the control period T. Furthermore, the control signal $s_1(t)$ will be connected to either positive or negative supply, and the noise on these lines will add in parallel to the input signal. Whether or not this can be tolerated needs further investigation and will depend on the application.

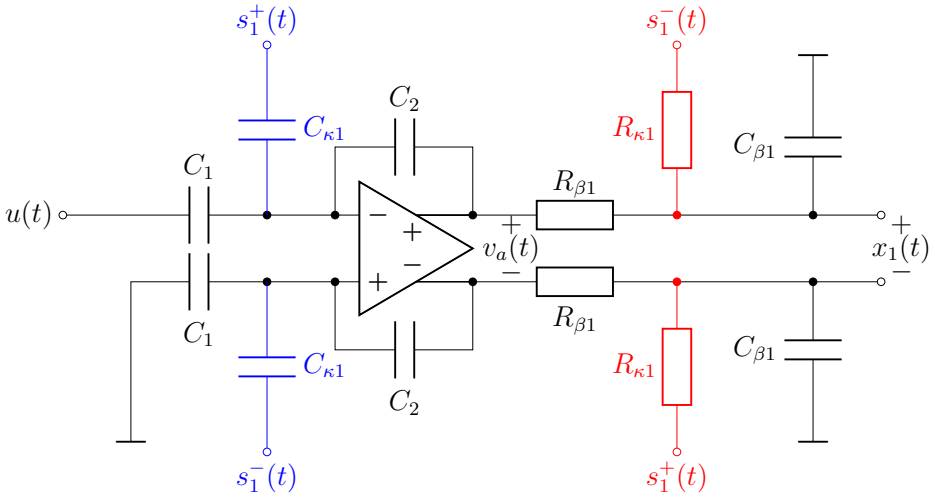


Figure 5.1: A schematic of the LNA driven, passive integrator. Two different solutions for the interface to the control signal $s_1(t)$ are indicated in red and blue.

With the capacitive control input, the frequency domain relation between $u(t)$, $x_1(t)$ and $s_1(t)$ of figure 5.1 is obtained as

$$X_1(j\omega)\left(j\omega + \underbrace{\frac{1}{R_\beta C_\beta}}_{\rho_1}\right) = U(j\omega)\underbrace{\frac{C_1}{C_2}\frac{1}{R_\beta C_\beta}}_{\beta_1} + S_1(j\omega)\underbrace{\frac{C_\kappa}{C_2}\frac{1}{R_\beta C_\beta}}_{\kappa_1\beta_1}. \quad (5.1)$$

By comparison with (3.1) we recognize $\rho_1 = \frac{1}{R_\beta C_\beta}$, $\beta_1 = \frac{C_1}{C_2}\frac{1}{R_\beta C_\beta}$ and $\kappa_1 = \frac{C_\kappa}{C_1}$. The DC-gain of the integrator, A_0, is the same as the closed loop gain of the LNA. The maximum closed loop gain of the LNA is limited by the supply voltage and the maximum swing of the input signal.

5.2 Subsequent Integrators

The relaxed design requirements of the remaining integrators should be utilized for minimal power consumption. It will become apparent that a main challenge with the considered architectures is the implementation of the summation node. OTA-RC integrators would in this sense have been an attractive alternative as currents could easily be summed at the virtual ground of the OTA. However, the negative feedback requires the amplifier to have a unity gain frequency much greater than that of the integrator, limiting the integrator's power efficiency [22]. Furthermore, a power-area trade-off is unavoidable when determining the resistor values. Although decent performance could probably be achieved with proper circuit design, solutions involving resistors and negative feedback amplifiers are not considered for the remaining integrators in this thesis.

The Gm-C integrator could on the other hand allow for high power efficiency due to the open-loop configuration and is considered as a promising candidate for the remaining integrators of the analog system. Analog summation is however not straightforward with this integrator topology and linearity requires some extra attention. The remainder of this section is concerned with the challenges associated with signal summation, and linearity is revisited together with circuit ideas and simulation results later in this chapter.

The two approaches for analog summation with Gm-C integrators considered in this thesis, are floating-gate voltage summation and output current summation. Each approach is analyzed analytically, and expressions for the parameters β, α and κ are given. Based on the analysis, a discussion of potential implementation challenges is provided together with behavioural simulations.

5.2.1 Floating-Gate Voltage Summation

Figure 5.2 shows one section of (a single ended equivalent of) the Leapfrog analog system, when the summation nodes are realized using floating gate voltage summation. Let $v_{fg,k}$ denote the voltage on the floating gate node. Furthermore, let $\overleftarrow{C}_{\beta k}$, $\overleftarrow{C}_{\alpha(k+1)}$ and $\overleftarrow{C}_{\kappa k}$ denote the effective capacitance seen from $v_{fg,k}$ towards $C_{\beta k}$, $C_{\alpha(k+1)}$ and $C_{\kappa k}$ respectively. $C_{\kappa k}$ is assumed to be driven by an ideal voltage source, such that $\overleftarrow{C}_{\kappa k} = C_{\kappa k}$. $C_{\alpha(k+1)}$ will be connected to $C_{L(k+1)}$, but by assuming $C_{\alpha(k+1)} << C_{L(k+1)}$, we

approximate $\overleftarrow{C}_{\alpha(k+1)} \approx C_{\alpha(k+1)}$. $\overleftarrow{C}_{\beta k}$ is given by

$$\overleftarrow{C}_{\beta k} = \frac{C_{L(k-1)} \cdot C_{\beta k}}{C_{L(k-1)} + C_{\beta k}} \tag{5.2}$$

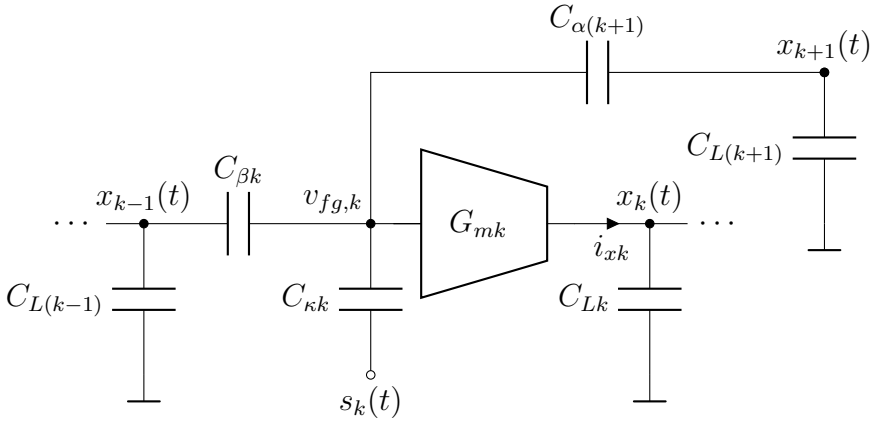


Figure 5.2: A single ended equivalent of one section of the Leapfrog analog system, realized with Gm-C integrators and floating-gate voltage summation.

Establishing Voltage Relations

When the voltage on, e.g. x_{k-1}, changes by $\Delta v_{x(k-1)}$, a charge $\Delta Q_{\beta k} = C_{\beta k}(\Delta v_{x(k-1)} - \Delta v_{fg,k})$ will flow through the capacitor $C_{\beta k}$. This charge will be distributed among the remaining capacitance connected to the floating-gate node, inducing a voltage change $\Delta v_{fg,k} = \frac{\Delta Q_{\beta k}}{C_{\kappa k}+C_{\alpha(k+1)}}$. As a result, the contribution from x_{k-1} to the floating-gate voltage is given by

$$\frac{v_{fg,k}}{v_{x(k-1)}} = \frac{C_{\beta k}}{C_{\kappa k} + C_{\alpha(k+1)} + C_{\beta}} \tag{5.3}$$

By similar arguments, the feedback contribution from x_{k+1} and the control contribution from s_k are given by

$$\frac{v_{fg,k}}{v_{x(k+1)}} = \frac{C_{\alpha(k+1)}}{C_{\kappa k} + C_{\alpha(k+1)} + \overleftarrow{C}_{\beta k}}, \tag{5.4}$$

and

$$\frac{v_{fg,k}}{v_{sk}} = \frac{C_{\kappa k}}{C_{\kappa k} + C_{\alpha(k+1)} + \overleftarrow{C}_{\beta k}} \tag{5.5}$$

respectively.

Let $\overrightarrow{C}_{Lk}$ denote the effective load capacitance seen from the output of transconductor k. The matrix coefficients β_k, $\beta_k\alpha_{k+1}$ and $\beta_k\kappa_k$ are then given by multiplying equations (5.3) to (5.5) by ${}^{G_{mk}}/_{\overrightarrow{C}_{Lk}}$.

In contrast to s_k, the voltage on x_{k-1} and x_{k+1} is not generated by voltage sources, but by capacitors being charged by current sources. In consequence, the voltage on these nodes will also be affected by any voltage change on $v_{fg,k}$. The contribution from s_k to x_{k-1} and x_{k+1} is given by

$$\frac{v_{x(k-1)}}{v_{sk}} = \frac{v_{fg,k}}{v_{sk}}\frac{v_{x(k-1)}}{v_{fg,k}} = \frac{C_{\kappa k}C_{\beta k}}{C_{\beta k}C_{L(k-1)} + (C_{\kappa k} + C_{\alpha(k+1)})(C_{\beta k} + C_{L(k-1)})} \tag{5.6}$$

and

$$\frac{v_{x(k+1)}}{v_{sk}} = \frac{v_{fg,k}}{v_{sk}}\frac{v_{x(k+1)}}{v_{fg,k}} = \frac{C_{\kappa k}C_{\alpha(k+1)}}{(\overleftarrow{C}_{\beta k} + C_{\alpha(k+1)} + C_{\kappa k})(C_{\alpha(k+1)} + C_{L(k+1)})}, \tag{5.7}$$

respectively. A similar contribution exist from x_{k+1} to x_{k-1} via $C_{\alpha(k+1)}$.

Parasitic Paths

The contribution from s_1 described by (5.6) and (5.7) does not fit the state-space model described by (3.1). These signal paths are in this thesis referred to as *parasitic paths* and their implications on the system behaviour is analysed in the following.

The voltage on x_{k-1} is being monitored by a local digital control and the disturbance caused by s_k will affect the decision made by this control loop. This effect is could be modelled as a time-varying offset voltage in the comparator observing the voltage on x_{k-1}. Assume $s_k(t) \in \{+V_{dd}, -V_{dd}\}$. The maximum effective offset voltage, $\delta_{c\kappa}$, caused by this parasitic path is then given by

$$\delta_{c\kappa} = V_{dd}\frac{C_{\kappa k}C_{\beta k}}{C_{\beta k}C_{L(k-1)} + (C_{\kappa k} + C_{\alpha(k+1)})(C_{\beta k} + C_{L(k-1)})}. \tag{5.8}$$

As shown in section 3.5.1 this effect could be accounted for by adjusting the parameters T, β and κ according to equations (3.44) and (3.45).

As the contribution from s_k to x_{k-1} goes via $v_{fg,k}$, this parasitic path does not influence the system beyond the modulated offset voltage. [1]. In

[1] If another feedback capacitor $C_{\alpha(k-1)}$ is connected to x_{k-1}, this statement is not strightly true, as a part of the contribution from s_k would flow through this capacitor and influence x_{k-2}. However, this effect would typically be very small and is considered negligible for the sake of a tractable analysis.

other words, the effect of this parasitic path is only related to stability, and the contribution from s_k to x_k, and thereby the rest of the system, is unaffected.

However, for the contribution from s_k to x_{k+1} via $C_{\alpha(k+1)}$, the situation is different. In addition to modulating the offset voltage of the comparator observing this node, the contribution will propagate further via $C_{\beta k+1}$. Even though this contribution will be small, if the effect is not modelled by the digital estimator, it will introduce error in the reconstruction of $\hat{u}(t)$.

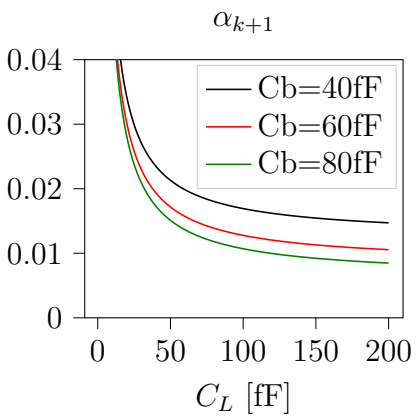
Determining Capacitor Values

The integrator gain β, the control gain κ and the feedback factor α are all dependent on the ratio between the capacitors $C_\beta, C_\kappa, C_\alpha$ and C_L. In section 3.3.1, $\omega_p = 2\pi f_c$ was considered a reasonable value for the pole frequency parameter, ω_p. Furthermore, to maintain sufficient quantization noise suppression over the full filter bandwidth, an initial value for the unity gain of the integrators could be $f_u = 4f_c \Longrightarrow \beta = 4\omega_p$. From equation (3.12), the resulting feedback factor α is given by

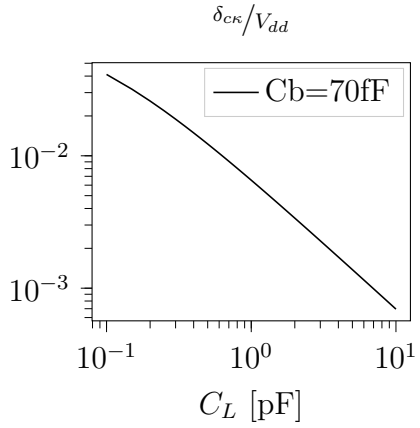
$$|\alpha| = \frac{\omega_p^2}{4\beta^2} \approx \frac{1}{4 \cdot 4^2} \approx 0.015 \tag{5.9}$$

In figure 5.3a, α_{k+1} is plotted against the load capacitor $C_{L(k-1)}$ for different values of $C_{\beta k}$. $C_{\alpha(k+1)}$ is set to 0.5fF which is assumed to be close to the minimum capacitor value of the technology. The control gain is set to $\kappa = 0.1$, which amounts to a state-boundary $b_{\boldsymbol{x}} \approx {}^{V_{dd}}/_{10}$ cf. equation (3.41). Based on these values for $C_{\alpha(k+1)}$ and κ, equations (5.2) to (5.5) are used to evaluate α_{k+1} as a function of $C_{L(k-1)}$, for different values of $C_{\beta k}$. It is clear from the plot that a $C_{\beta k}$ of about $60 - 70$fF is required in order achieve a sufficiently small feedback factor α of about 0.015.

Figure 5.3b shows the induced comparator offset $\delta_{c\kappa}$, normalized to V_{dd}, as a function of $C_{L(k-1)}$ for $C_{\beta k} = 70$fF. To limit the required reduction in the βT product, a reasonable limit for the tolerable induced offset could be $\delta_{c\kappa} < {}^{b_{\boldsymbol{x}}}/_{100}$. Assuming $b_{\boldsymbol{x}} = {}^{V_{dd}}/_{10}$, figure 5.3b shows that a load capacitor of several pF would in this case be required. Such a big load capacitor would have a significant impact on the power consumption of the transconductors.



(a) The feedback parameter α plotted against $C_{L(k-1)}$ for three different values of $C_{\beta k}$



(b) The induced comparator offset $\delta_{c\kappa}$, normalized to V_{dd}, plotted against $C_{L(k-1)}$ for $C_{\beta k} = 70$fF

Figure 5.3: Evaluation of $\delta_{c\kappa}$ and α_{k+1} for different capacitor values

Parasitic Path and Passive Integrator

As a final note on the floating-gate voltage summation, we consider the parasitic path in combination with the passive integrator described previously in this chapter. Figure 5.4 gives a simplified picture of the situation when an LNA driven, passive integrator of the first stage is connected to a transconductor with floating-gate voltage summation at the input. The LNA is modelled as an ideal voltage source, v_a, and $x_1(t)$ is integrated by charging $C_{\beta 1}$ through the resistor $R_{\beta 1}$.

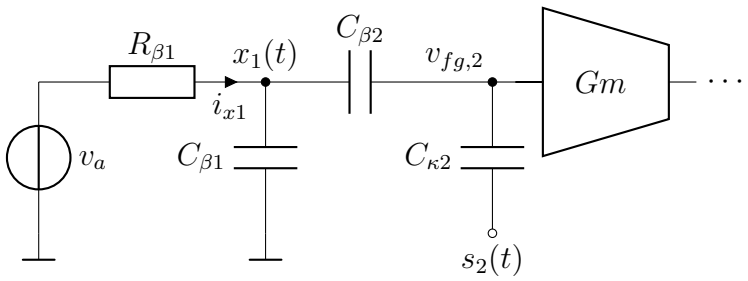


Figure 5.4: An LNA driven, passive integrator connected to a transconductor with floating-gate voltage summation

The charge feedthrough from the control contribution $s_2(t)$ via $C_{\beta 2}$ will influence the voltage on x_1. In addition to inducing an offset on the comparator monitoring $x_1(t)$, this will also influence the current flowing through the resistor $R_{\beta 1}$. This effect is more problematic than the induced

offset voltage, as the fundamental behaviour of the passive integrator is modulated by the control contribution $s_2(t)$.

Behavioural Simulations

To support the statements of this section, a behavioural simulations of the considered architecture is presented. The simulations are all obtained using the Cadence library *analoglib*, which provides ideal models for amplifiers (voltage-controlled voltage source), transconductors (voltage-controlled current source) etc. The comparator is implemented in VerilogA and the code is given in appendix C. Figure 5.5 shows a single ended equivalent of the system used to obtain the following simulation results. Table 5.1 shows the essential simulation parameters. The spectre netlist, which also contains all source and component values, is given in appendix D.1.

To disable the parasitic paths described above, ideal voltage buffers are inserted as indicated in the figure. The comparators with input $x_k(t)$ and output $s_k(t)$ are excluded from the illustration. Note the absence of feedback from $x_2(t)$ to $x_1(t)$. This feedback path is removed due to equation (5.9) which would have required C_1 and C_2 to be very large in order to achieve a sufficiently small feedback factor.

Table 5.1: Parameters used for the behavioural simulation

Parameter	Symbol	Value	Comment
Supply voltage	V_{dd}	0.8V	
Input amplitude	b_u	10mV	Sinusoidal
Filter bandwidth	f_c	10 MHz	
Control period	T	2ns	$f_s = 500\,\text{MHz}$
Integrator gain	β	$2\pi 40\,\text{MHz}$	All integrators
Control gain	κ	10mV	All integrators
Feedback factor	α	-0.015	$\beta = 4\omega_p = 8\pi f_c$
FFT length		16384 samples	

Figure 5.6 shows the estimated PSD of $\hat{u}(t)$ together with the theoretical NTF, given by equation (2.21). The estimated SNR and SNDR is 80dB and 79dB respectively.

This ideal simulation verifies the operating principle of the considered high-level architecture and serves as a basis of comparison for other simulations presented later in this thesis. Furthermore, this simulation gives

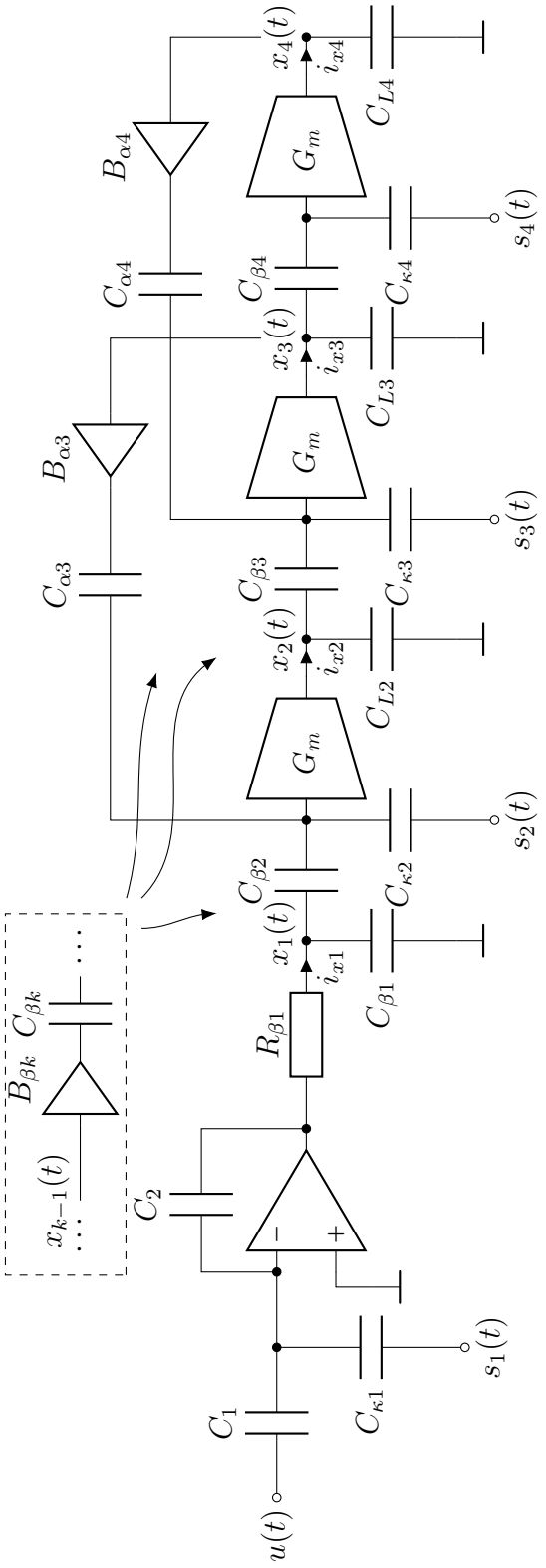


Figure 5.5: Single ended equivalent of the 4th order Leapfrog analog system, with LNA driven, passive integrator and Gm-C integrators with floating-gate voltage summation.

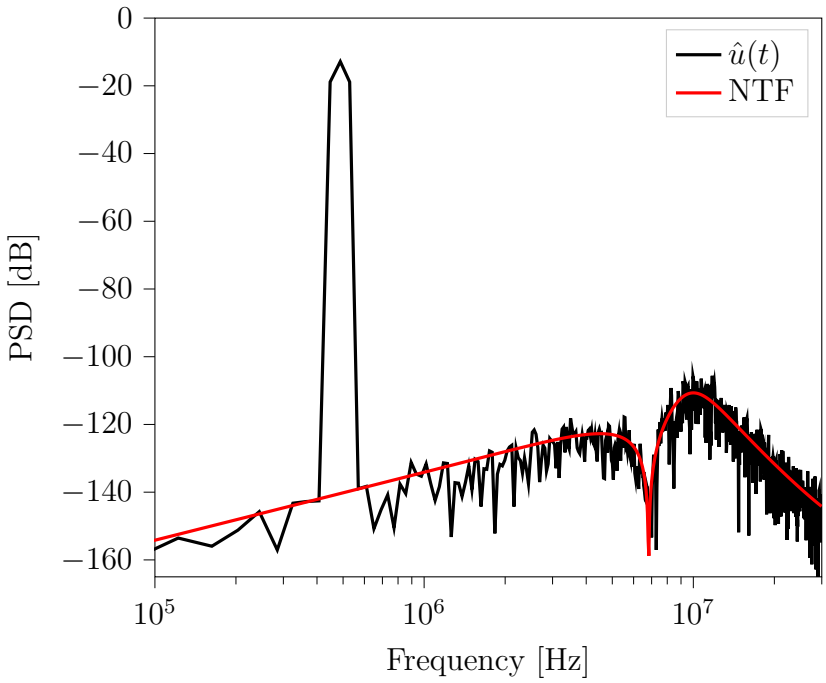


Figure 5.6: Estimated PSD of $\hat{u}(t)$ plotted together with corresponding theoretical NTF. Obtained from an ideal circuit simulation of a 4th order Leapfrog ADC with LNA driven, passive integrator and floating-gate voltage summation

a demonstration of the AC calibration algorithm described in section 4.2 which is used to determine the filter coefficients before reconstructing $\hat{u}(t)$ from $\boldsymbol{s}[k]$.

To see the effect of the induced comparator offset discussed above, consider figure 5.7 which shows a snapshot of $x_2(t), x_4(t)$ and $s_3(t)$ for different values of C_β when $C_L = 40\text{fF}$. In this simulation, the buffers $B_{\beta 3}$ and $B_{\beta 4}$, cf. figure 5.5, is removed from the simulation, enabling the parasitic path from $s_4(t)$ to $x_3(t)$ and from $s_3(t)$ to $x_2(t)$. To more clearly illustrate the effect of $\delta_{c\kappa}$, the feedback paths are disabled by zeroing $C_{\alpha 3}$ and $C_{\alpha 4}$.

In figure 5.7a, $C_\beta = 100\text{fF}$, causing a large induced comparator offset $\delta_{c\kappa}$, in line with the plot of figure 5.3b. The effect of $\delta_{c\kappa}$ is clearly visible in figure 5.7a, as $s_3(t)$ has a significant impact on $x_2(t)$. In consequence, the digital control fails to ensure $|x_2(t)| < b_{\boldsymbol{x}}$. As seen in the lower window of figure 5.7a, the increased magnitude of $x_2(t)$ propagates further, causing even greater stability problems for $x_4(t)$.

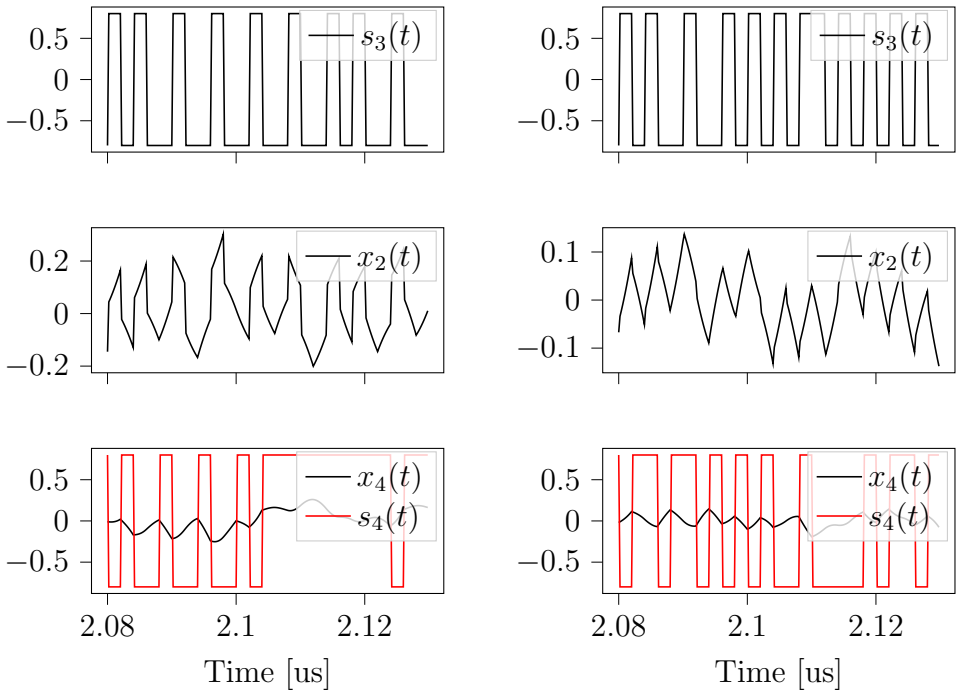
In figure 5.7b $C_\beta = {}^{C_L}/_{10}$ and the effect of $\delta_{c\kappa}$ is barely visible in the snapshot of $x_2(t)$. Hence, $x_2(t)$ is properly bounded by $s_2(t)$ and an effective control is also observed for the last state of the system, $x_4(t)$.

The estimated power spectra corresponding to the simulations of figure 5.7 are shown in figure 5.8 together with the theoretical NTF. Note that this system has all poles at the origin, as the feedback paths through the C_α's are disabled. For $C_\beta = 4\text{fF}$ the PSD closely follow the NTF, indicating that the performance of the ADC is not notably affected by the induced comparator offset $\delta_{c\kappa}$. However, for $C_\beta = 100\text{fF}$, the stability issue caused by the (in this case large) $\delta_{c\kappa}$ degrades the quality of the output estimate. This simulation supports the statement that the induced comparator offset is a stability issue only, and that the amount of influence from $s_k(t)$ to $x_{k-1}(t)$ that could be tolerated depends on the stability margin of the system.

Buffer Output Resistance

The behavioural simulations above use ideal voltage buffers to disable the parasitic signal paths. If the voltage buffers were to be implemented as source-followers, they would have a gain less than unity and a non-zero output impedance. The reduced gain would reduce the value of the parameters β and α, but this would not be a fundamental problem for any reasonable gain slightly less than 1.

The non-zero output impedance, is on the other hand more problem-



(a) $C_\beta = 100\text{fF}$ (b) $C_\beta = 4\text{fF}$

Figure 5.7: Snapshot of $x_2(t), x_4(t)$ and $s_3(t)$ for $C_L = 40\text{fF}$ and different values of C_β, illustrating the induced comparator offset $\delta_{c\kappa}$.

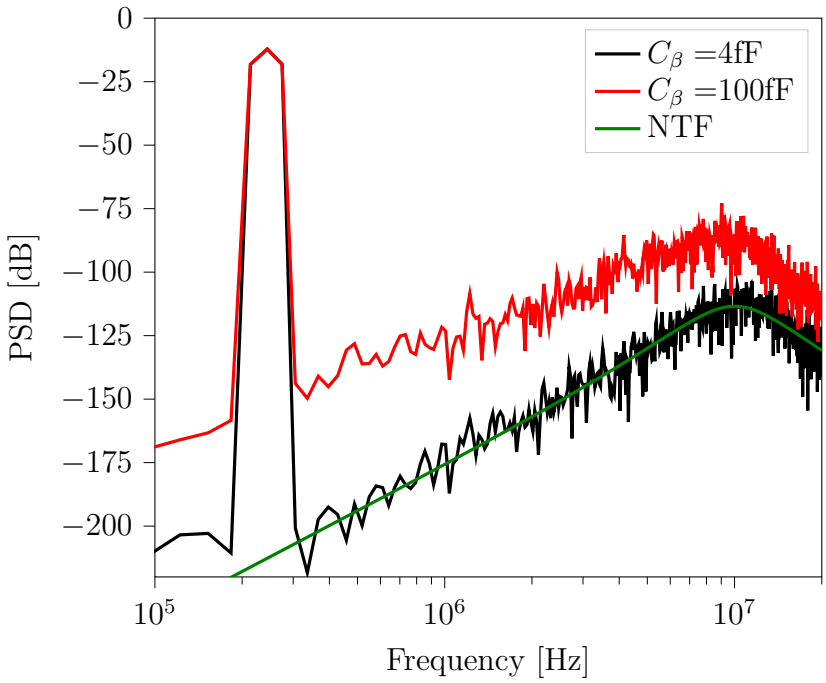


Figure 5.8: Estimated PSD of $\hat{u}(t)$ corresponding to the simulations of figure 5.7

atic. Figure 5.9 illustrates a section of the system when the buffers has a non-zero output impedance R_o. This resistance will introduce an exponential settling of the voltage $v_{fg,k}$. As this behaviour is not modelled by the reconstruction filter, the accuracy of the final ADC output will be reduced.

To see this effect, consider figure 5.10 which shows the estimated SNR and SNDR as a function of the buffer output resistance. Apart from the modified buffers, the simulation setup is identical to that of figure 5.6. When the output resistance is less than 1kΩ, the quality of the output is not notably affected. However, as R_o approaches 10kΩ the SNR and SNDR falls of rapidly.

In this simulation, C_κ and C_α was 1.6 fF and 1 fF respectively. An even smaller output resistance would be required for higher capacitors, in order to obtain the same settling time.

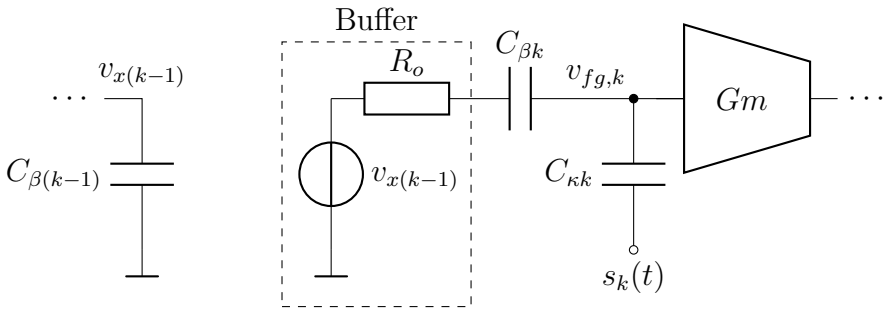


Figure 5.9: One section of the system in figure 5.5, when the buffer $B_{\beta k}$ has a non-zero output resistance R_o.

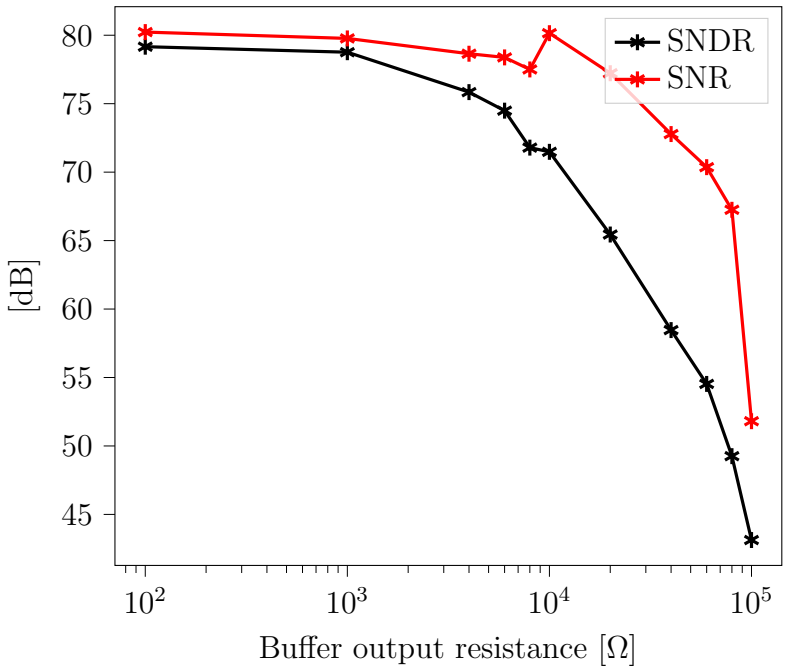


Figure 5.10: Estimated SNR and SNDR as a function of buffer output resistance.

5.2.2 Output Current Summation

An alternative to input voltage summation is to add currents at the output of the transconductors. Figure 5.11 shows the single ended equivalent of one section of the analog system, when the summation node is realized at the transconductor output. In this implementation, β, α and κ are given by

$$\beta_k = \frac{G_{m\beta k}}{C_{Lk}}, \quad \alpha_k = \frac{G_{m\alpha k}}{G_{m\beta k}}, \quad \text{and} \quad \kappa_k = \frac{G_{m\kappa k}}{G_{m\beta k}}. \tag{5.10}$$

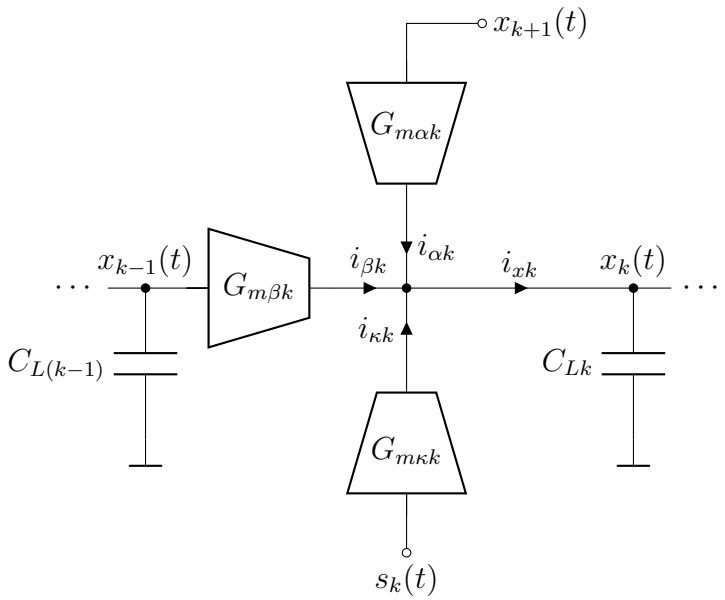


Figure 5.11: A single ended equivalent of one section of the Leapfrog analog system, realized with Gm-C integrators and output current summation.

The advantage of this approach is that the contributions from $s_k(t)$ and $x_{k+1}(t)$ is actually confined to $x_k(t)$. Hence, the issues with the parasitic paths discussed above is omitted.

A disadvantage however, is the increased number of active components required. To minimize the power consumption, it is desirable to keep C_{Lk} as small as possible, such that the same β_k could be realized with a lower $G_{m\beta k}$. However, equation (5.9) implies that $G_{m\alpha k}$ should be almost 100 times smaller than $G_{m\beta k}$. There will presumably be a practical lower limit for $G_{m\alpha k}$, below which transistors must be made impractically long for the transconductor to function properly. It might therefore be necessary

to increase $G_{m\beta k}$ and C_{Lk}, and consequently power consumption, because of design issues related to $G_{m\alpha k}$.

Furthermore, as $G_{m\kappa k}$ is driven by the binary control contribution $s_k(t)$, it is in fact acting as a 1-bit current digital-to-analog converter (DAC), driving a high-impedance load. To limit errors due to charge feedthrough and charge injection, it might be necessary to reduce the swing of the voltage signal driving $G_{m\kappa k}$ [23]. Some additional complexity might therefore be required for implementing this solution.

Behavioural Simulations

A single ended equivalent of a 4th order Leapfrog analog system with output current summation is shown in figure 5.12. The spectre netlist used for simulating this system on a behavioural level is given in appendix D.2 and the quantitative performance of this simulation is equal to that of figure 5.5 for the same parameters β, κ and α.

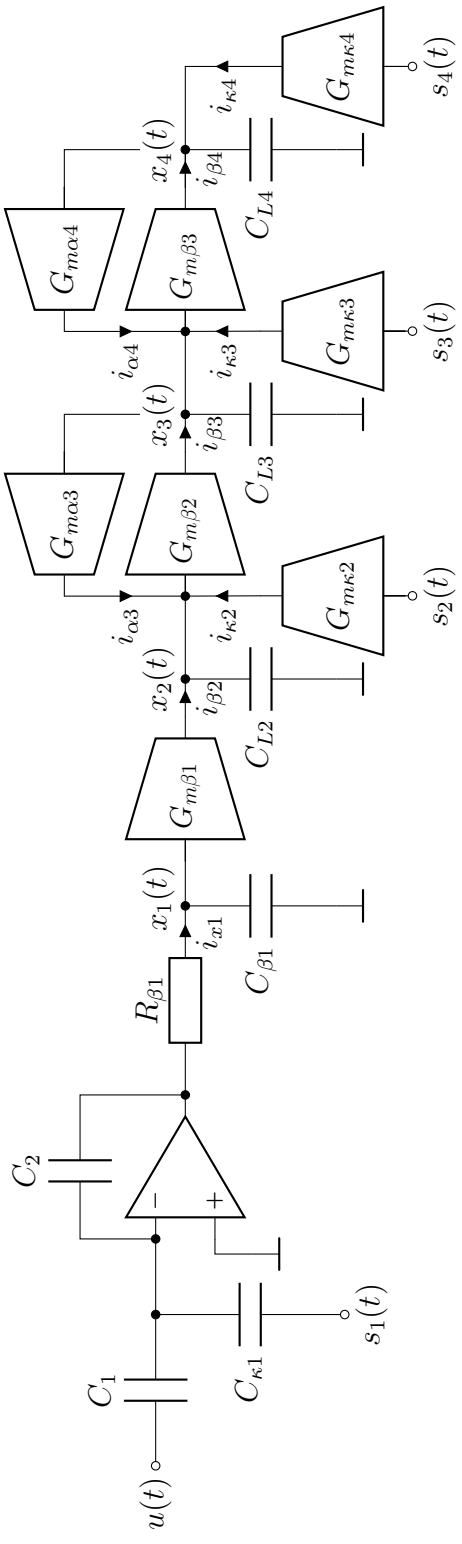


Figure 5.12: Single ended equivalent of the 4th order Leapfrog analog system, with LNA driven, passive integrator and Gm-C integrators with output current summation.

5.2.3 Conclusions on Analog Signal Summation

In this section, design challenges associated with the implementation of the Leapfrog analog system using Gm-C integrators has been studied. The underlying motivation has been to utilize the relaxed requirements on these components for minimal power consumption. In general, the effective G_m is proportional to the bias current of the transconductor. As the integrator gain is given by $\beta = {}^{G_m}/_{C_L}$, the power efficiency of the Gm-C integrator is ultimately determined by the size of the load capacitor seen by the transconductor. Realizing analog signal summation with very small capacitors is however not trivial, and two different approaches is studied in detail; output current summation and floating-gate voltage summation.

Summing currents at the transconductors outputs requires additional transconductors for converting the voltage signals $\boldsymbol{x}(t)$ and $\boldsymbol{s}(t)$ into the current domain. For the transconductor driven by the 1-bit comparator, $G_{m\kappa}$, some additional complexity will be required to reduce the input voltage swing and avoid charge injection errors. Due to the small feedback factor α, the feedback transconductor, $G_{m\alpha}$, would be required to have an effective transconductance about 100 times smaller than that of the main transconductor, $G_{m\beta}$. The current consumption of $G_{m\beta}$ might therefore be limited by a practical lower limit for $G_{m\alpha}$. Alternatively, the input of $G_{m\alpha}$ could be attenuated at the cost of additional complexity.

The additional transconductors could be avoided by summing voltage signals directly at the floating-gate input of the transconductors, using capacitive voltage division. However, due to the bidirectional nature of the capacitors, this approach is giving rise to what we refer to as parasitic signal paths in the system. A brute force way of handling this issue is to increase the load capacitors of the Gm-C integrators, at the cost of a significant increasement in power consumption. Voltage buffers could be implemented to disable the parasitic paths, but a considerable power consumption could be required for sufficiently low output impedance.

From the discussion above, it is evident that more research is needed to decide on an optimum solution. The challenges associated with the implementation of the mentioned buffers, transconductors and attenuators should be investigated to obtain an impression of required power consumption. It could also be desirable to combine the considered architectures, by using e.g. voltage summation for the control contributions and current summation for the feedback contribution. Furthermore, the summation need not be performed the same way throughout the chain. It

could be favorable to use e.g. current summation for the more sensitive, early stages, and voltage summation towards the end of the system.

5.3 Circuit Ideas

This section presents transistor level circuit ideas for the implementation of the active components involved in the architectures considered in this thesis. Specifically, circuit schematics and (pre-layout) simulation results for the OTA, transconductor and a clocked comparator is provided. Rather than optimizing the design of a few components, the goal of this work has been to seek an overview of the critical implementation challenges associated with the considered architecture. The schematics are therefore not presented as a proposed implementation, but as examples providing increased insight in practical design issues. Last but not least, the presented transistor level simulations verifies several analytical results presented earlier in the thesis.

The specifications listed in table 1.1 forms the background for the requirements on the components considered in this section. In particular, the target bandwidth is 10 MHz, the total input referred noise voltage of the whole ADC should be less than $16\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ and the second order harmonic distortion should be below $-50\,\mathrm{dBc}$. The specifications form a basis for the initial circuit design, although they will not be completely satisfied by the circuit ideas presented in this chapter. No particular effort have been made to find an optimum division of the noise budget in this thesis, but it is reasonable to allow the first integrator to contribute with the main bulk of the total noise.

Throughout this section, several simulation results is presented to verify and illustrate different properties of the considered implementations. If not specified otherwise, the following applies to all simulations of this section:

- The architecture is a differential version of the system described by figure 5.5 and the essential simulation parameters are given by table 5.1.
- Ideal models are used for all components. The OTA, transconductors and voltage buffers are implemented using ideal models for voltage-controlled voltage and current sources. The verilogA model for the comparator is given in appendix C.
- Nominal values are used for process parameters and component

mismatch and transient noise is disabled in the simulation.

5.3.1 OTA

The amplifier used in the simulations of this section is an inverter based, current-mirror OTA, with local positive feedback. The schematic is shown in figure 5.13 and spectre netlist and some additional design details are given in appendix E.

The current-mirror amplifier with local positive feedback is chosen as an initial architecture because of its high energy efficiency. The transistor M_4 provides a local positive feedback, boosting the impedance on the drain of M_3. As a result, the small-signal current-mirror ratio is enhanced without altering the large signal ratio, increasing the effective transconductance, $G_{m,eff}$, for the same bias current [24]. Inverter-based OTAs are popular in low-power applications [25, 26] and inverters are used at the input to further increase $G_{m,eff}$ for the same bias current. Some key performance metrics of the OTA is given in table 5.2.

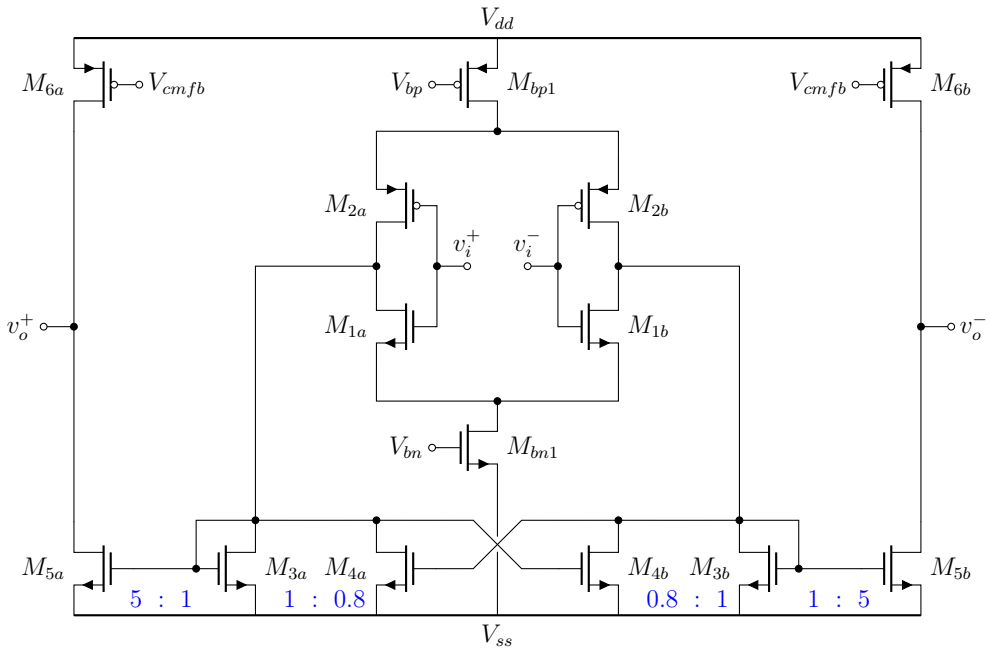


Figure 5.13: Schematic for inverter based, current-mirror OTA with local positive feedback.

Figure 5.14 shows the estimated PSD obtained by a simulation when the ideal amplifier is substituted by the current-mirror OTA. It is evident

Table 5.2: OTA performance metrics

Parameter	Symbol	Value	Comment
Input referred noise voltage	V_{ni}	$25\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$	At 5 MHz
Open-loop gain	A_{v0}	700V/V	At DC
Unity gain frequency	f_u	2.5GHz	$C_L = 20\mathrm{fF}$
Current consumption	I_{DC}	30µA	

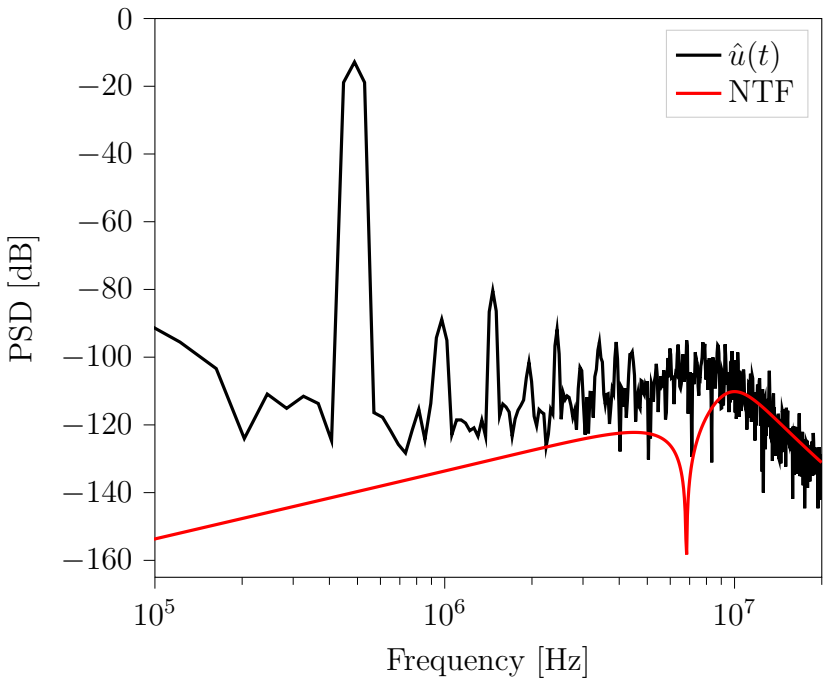


Figure 5.14: Estimated PSD of $\hat{u}(t)$ plotted together with corresponding theoretical NTF. Obtained by simulating the system of figure 5.5 when ideal models are used for all components except for the OTA.

that the amplifier suffers from significant harmonic distortion. From this particular simulation, the second and third harmonic was estimated to HD2 = −76dB and HD3 = −68dB respectively. The second (an other even order) harmonic arises from the single-ended to differential conversion, as the inputs does not perfectly track each other when the amplifier has a finite open-loop gain. Note that the spectrum of figure 5.14 does not follow notch of the theoretical NTF as expected from the linearity analysis of section 3.4.2.

The actual linearity performance of the OTA should be evaluated over component mismatch and process variations. However, as the harmonic distortion is significant even in the nominal corner without mismatch, the linearity should probably be improved for a future implementation.

As seen from table table 5.2, the input referred noise voltage of the OTA alone exceeds the specifications for the complete ADC given by table 1.1 and the thermal noise performance therefore needs improvement. Furthermore, flicker noise is not considered in this work and chopping might be required to reduce the in-band $1/f$ noise.

Feeding the control contribution $s_1(t)$ to the amplifier input will constantly challenge its transient response. A snapshot of the OTA output $v_a(t)$ and the first state signal $x_1(t)$ is shown in figure 5.15. It is clear that the step response of the OTA oscillates before settling. Although the frequency of these oscillations are far beyond the unity-gain frequency of the passive integrator, the non-ideal waveform of $v_a(t)$ might have a non-negligible effect on the state-signal $x_1(t)$.

Part of the errors observed in the spectrum of figure 5.14 could therefore originate from transient effects, such as ringing and slew-rate limitations, rather than harmonic distortion generated by the amplifier. Setting requirements for the transient behaviour and analyzing the impact on the final ADC output remains for a future implementation.

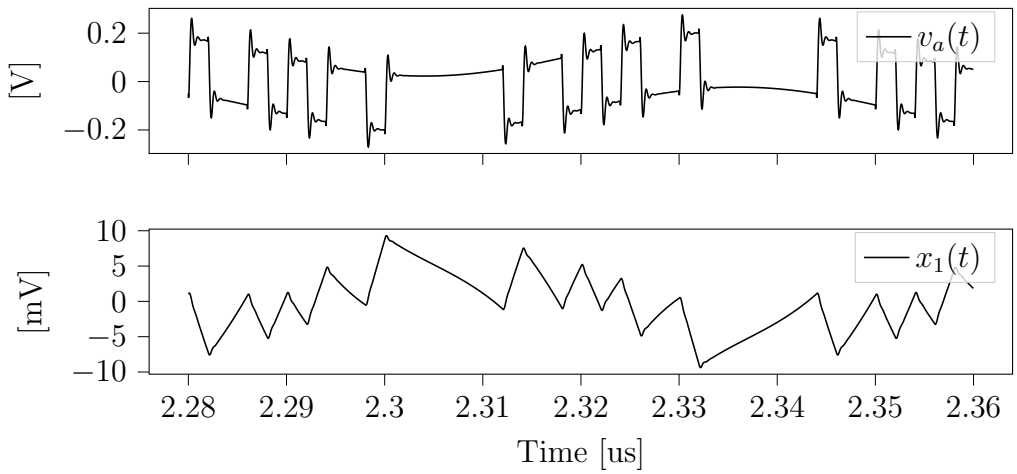


Figure 5.15: Snapshot of OTA output $v_a(t)$ and the first state-signal $x_1(t)$

5.3.2 Transconductor

The main objective for the design of the transconductor used in the Gm-C integrators of figure 5.5 is to utilize the relaxed requirements on noise and linearity for reduced power consumption. The maximum input magnitude processed by a certain transconductor, which depends on the unity gain of the preceding integrator and the control period T, is in this thesis considered a design variable. Power demanding linearization techniques could then be avoided by co-optimizing the transconductors inherent linearity and the state boundary $b_{\boldsymbol{x}}$.

The schematic for the transconductor considered in this thesis is given in figure 5.16. Spectre netlist and some additional design details are given in appendix F and a summary of some key performance metrics is listed in table 5.3.

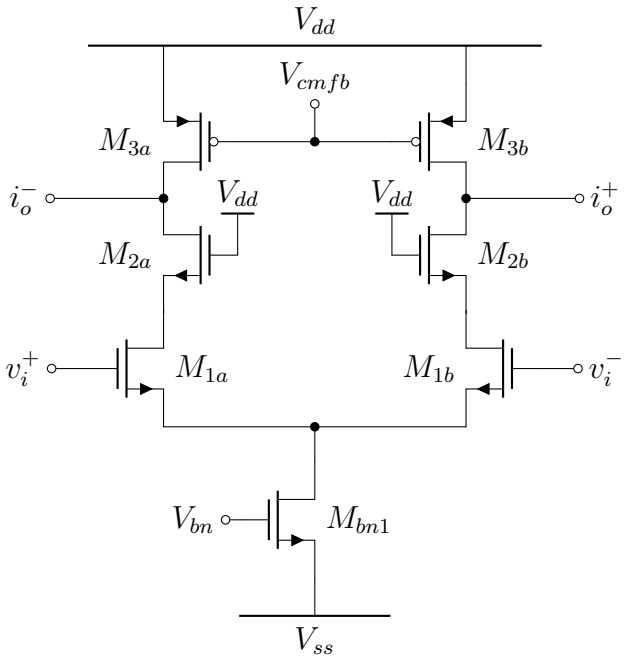


Figure 5.16: Transconductor schematic

The transconductor comprises a single differential pair (M_1) with an active load (M_3). The cascode/common-gate transistors, M_2, are included to limit the Miller-effect on the gate-drain capacitor C_{gd1} of the input transistors. The transconductor achieves a DC-gain of about 150. In the absence of M_2, C_{gd1} would have been boosted from about 200aF to more than 20fF, thereby becoming a dominating capacitor at the floating gate node. The DC-gain, and thereby the gate-drain capacitance, follow

the same frequency response as the overall Gm-C integrator. When the transconductor is used together with floating-gate voltage summation, as in figure 5.5, this effect would introduce a significant frequency dependency in the voltage division described by equations (5.3) to (5.5). With the cascode transistor, the voltage-gain from the gate to the drain of M_1 is reduced well below 10, considerably reducing this unwanted effect.

Table 5.3: Transconductor performance metrics

Parameter	Symbol	Value	Comment
Input referred noise voltage	V_{ni}	$70\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$	At 5 MHz
DC-gain	A_0	150V/V	
Load capacitor	C_L	20fF	
Unity gain frequency	f_u	43MHz	
Current consumption	I_{DC}	0.5µA	Bias current

A trade-off between noise and linearity exist when determining the ratio between the effective transconductance and the bias current, $^{G_m}/_{I_b}$. Figure 5.17 shows the simulated G_m as a function of differential input voltage for different values of $^{G_m}/_{I_b}$. The result is obtained by sweeping the differential input voltage of a single transconductor, and evaluating the current flowing between the shorted outputs. G_m is then found as the derivative of the I-V relationship. $^{G_m}/_{I_b}$ is varied by changing the $^{W}/_{L}$ ratio of the input transistors.

As expected, the figure shows that the effective transconductance decays more rapidly with input voltage for higher values of $^{G_m}/_{I_b}$. The input referred noise voltage is on the other hand reduced by increasing G_m for a given bias current. In this thesis, $^{G_m}/_{I_b} = 12$ is chosen as an initial value. However, for a future implementation, optimizing this trade-off will be an important part of the system design.

For a given transconductor a suitable value for the state boundary $b_{\boldsymbol{x}}$ must be determined. This parameter could be modified by varying the integrator gain β for a given control period T. As increasing the gain of the analog system reduces the conversion noise power (cf. equation (2.25)), it is in generally favorable to use as high $b_{\boldsymbol{x}}$ as possible.

Figure 5.18 shows the simulated SNDR as a function input signal amplitude b_u, when the transconductors are implemented as in figure 5.16 and ideal models are used for the remaining components. For each value of b_u, the control gain κ is scaled such that $b_{\boldsymbol{x}} = b_u$. This way, the magnitude processed by the integrators is decreased in proportion to the input

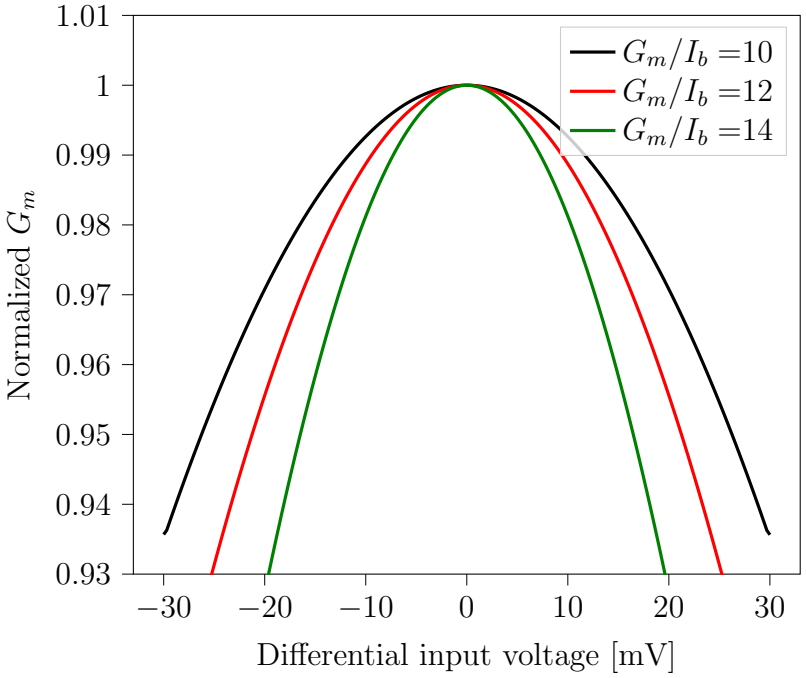


Figure 5.17: Effective transconductance G_m (normalized to its maximum value) as a function of differential input voltage, for different values of G_m/I_b

signal. As the conversion noise power is proportional to the magnitude of the state vector (cf. equation (2.25)), the expected behaviour from this simulation is that the SNDR remains more ore less constant up to a point where distortion generated by the transconductors begin to dominate the conversion error.

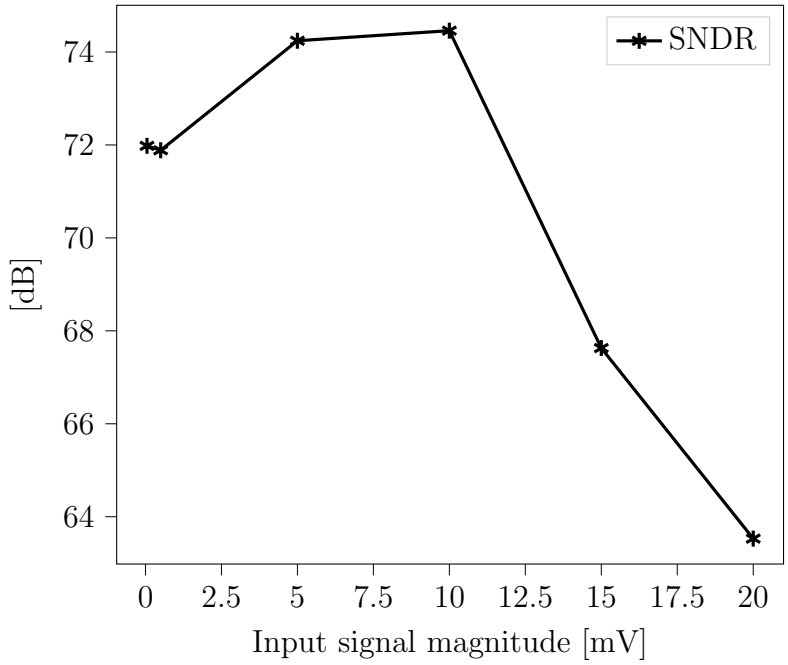


Figure 5.18: Simulated SNDR as a function of input signal amplitude b_u.

The simulation shows that this is indeed the case. The estimated SNDR stays well above 70 dB for $b_u \leq 10\,\text{mV}$ and drops rapidly higher values of b_u. For this particular transconductor, $b_{\boldsymbol{x}} = 10\,\text{mV}$ seem to be a reasonable value for the state boundary.

Thermal Noise

The effect of thermal noise for a general control bounded converter was analysed in section 2.5.3. Although equation (2.33) shows that the ADC is most sensitive to noise sources entering early in the system, translating the expression into a simple and useful design equation is not trivial. However, based on general experience with chain-structures, it is reasonable to expect that the input referred noise voltage generated by the second integrator is divided by the DC-gain of the first integrator when referred back to the input of the ADC. Using the considered OTA and transconductor implementation, we now test this assumption.

In the following simulation, the OTA driven, passive integrator is implemented with a DC-gain of 10. A conservative estimate for the expected thermal noise power is obtained by only considering the contribution from the first two integrators, with a noise bandwidth equal to the filter bandwidth $f_c = 10\,\mathrm{MHz}$. The expected value for the input referred noise power is then

$$P_n = \left[(25\,\mathrm{nV}/\sqrt{\mathrm{Hz}})^2 + (7\,\mathrm{nV}/\sqrt{\mathrm{Hz}})^2\right] \cdot 10\,\mathrm{MHz}. \tag{5.11}$$

By applying a sinusoidal input with amplitude 10 mV, and consequently a signal power of $P_s = \frac{1}{2}(10\mathrm{mV})^2$, the expected SNR is

$$\mathrm{SNR} = 10\log\left(\frac{P_s}{P_n}\right) = 38.7\mathrm{dB}. \tag{5.12}$$

Thermal noise performance is studied by simulating the system of figure 5.5 with transistor implementations of the OTA and all the transconductors, and ideal models for the comparators. A noise bandwidth of $f_n = 2f_s = 1\mathrm{GHz}$ was specified in the simulation [2].

The estimated SNR of the final output of this simulation was 39.2dB, i.e. 0.56 dB higher than the theoretically expected value. This indicates that dividing the input referred noise voltage by the accumulated DC-gain of the previous integrators, gives a reasonably accurate estimate of the contribution to the total noise power.

[2] This noise bandwidth was chosen by varying the bandwidth over several simulation runs, finding a frequency beyond which the SNR did no longer decrease.

5.3.3 Comparator

According to the analysis of section 3.5.3, the performance of the comparator comprising the local digital control, is only indirectly related to the quality of the final ADC output. Noise (in terms of a time-varying input offset voltage) and (static) offset voltage will require a reduction in the βT product and/or the state boundary $b_{\boldsymbol{x}}$, in order to maintain an effective control. According to equation (2.25), these adjustments will increase the conversion noise power, and the properties of the comparator will therefore somehow influence the performance of system. However, the increased conversion noise obtained by e.g. lowering the integrator gain β, could be compensated by extending the system order. As there is no direct path from the comparator noise to the final ADC output, the approach of this thesis is to realize the comparator with a minimal power consumption, and compensate for increased conversion noise on a system level.

The comparator considered in this thesis is a standard StrongARM latch [27]. The schematic of the comparator core and the output latch is shown in figure 5.19 and the spectre netlist is given in appendix G. The StrongARM latch is chosen because of low static power consumption and rail-to-rail output. As an initial value, chosen for low dynamic power consumption, all devices have the same dimension $\frac{W}{L} = \frac{150\,\mathrm{nm}}{20\,\mathrm{nm}}$.

Some key performance metric is given in table 5.4. The standard deviation of the offset voltage is estimated by running 1000 Monte Carlo simulations with statistical distributions for component mismatch and the root mean square (RMS) noise voltage is estimated from multiple transient simulations with a noise bandwidth of 200GHz.

The average current consumption is estimated by simulating the comparator with a sinusoidal input, with amplitude 10 mV and a frequency equal to half the clock frequency $f_s = 500\,\mathrm{MHz}$. This input signals forces all inverters to toggle every clock period, and the estimate therefore serves as an upper limit for the power consumption. Out of the total current consumption of 5.3 µA, about 1.2 µA was consumed by the StrongARM latch core, while 4.1 µA was consumed by the inverters and the output latch. No particular effort has been made to optimize this design and there are probably room for reducing the current consumption of the comparators digital output components.

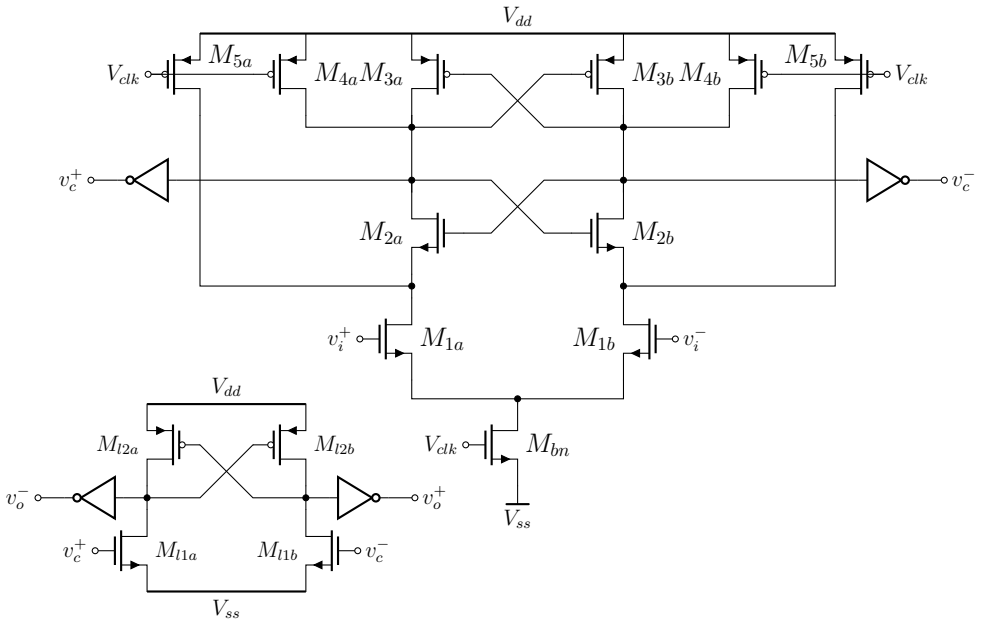


Figure 5.19: StrongARM latch core and output latch

Table 5.4: StrongARM latch performance metrics

Parameter	Symbol	Value	Comment
Input referred noise voltage	V_{ni}	1.82 mV	RMS
Offset voltage	σ_{vo}	28 mV	Std. dev.
Avg. current consumption, tot	I_0	5.3µA	

Comparator Offset Voltage

While section 3.5.3 analysed the effect of comparator offset voltage on an architectural level, the analysis did not take nonlinearities of the integrators into account. When the comparators have a static offset voltage, the elements of $\boldsymbol{x}(t)$ will swing around some constant DC-value instead of being centered around zero. When the integrators are implemented with open-loop transconductors, this DC-offset will introduce an asymmetry in the operating point of the transconductors, leading to even order harmonic distortion in the I-V relationship.

To study this effect, the system is simulated with a static offset voltage included in the ideal comparator model and all Gm-C integrators are implemented with transistor level transconductors. The comparator offset voltage is swept from -8mV to 8mV. For each offset value, the second and third order harmonic distortion is evaluated from the PSD of $\hat{u}(t)$. The result of this simulation is shown in figure 5.20. The simulation shows that third order harmonic distortion (HD3) is dominating over second order harmonic distortion (HD2) for very small offset voltages. When the offset voltage increase above a few millivolt, the two harmonic components become comparable in magnitude.

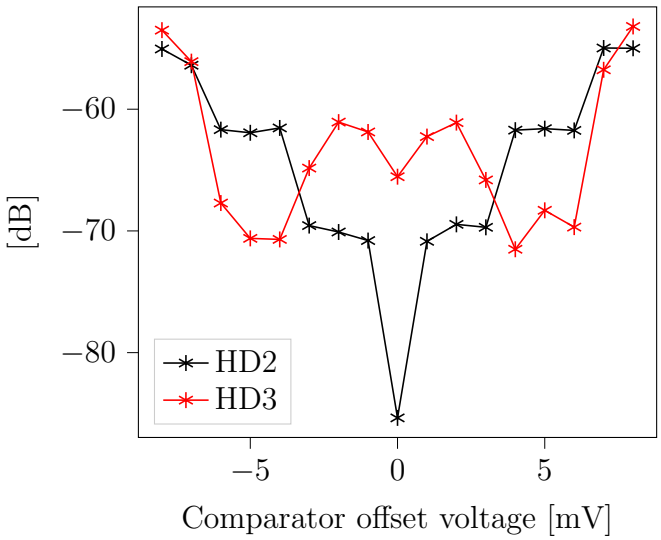


Figure 5.20: Simulated harmonic distortion generated by transconductors as a function of comparator offset voltage

The amount of offset that could be tolerated will depend on the linearity of the transconductors and a higher offset voltage could typically be accepted at the expense of increased power consumption. However,

linearizing the transconductors to handle a large DC-offset would imply extending its linear region, without utilizing this for increased gain and state vector magnitude. It is therefore probably more efficient to minimize the offset voltage in the comparator itself, and utilize the linear region of the transconductors for actual signal swing.

By comparing the plot of figure 5.20 to the estimated σ_{vo} of table 5.4, it is evident that the comparator would need some kind of offset cancellation in order to function properly with the open-loop transconductors. Techniques for offset cancellation is described in e.g. [27, 28] and should be studied in a future implementation.

Simulation Results

The estimated SNR/SNDR obtained by replacing the ideal comparator with the StrongARM latch was 52 dB/36 dB. Compared to the behavioural simulation, this simulation is therefore showing a significant increasement in both noise floor and harmonic distortion.

As discussed in the introduction of this section, the theoretical analysis suggest that the comparator comprising the digital control of a control-bounded converter is a less critical component, as noise and offset voltage could be compensated on a system level. The key take-away from the results of this section is that the comparator requires more careful attention than what is suggested by the theoretical analysis. Understanding the root cause of the observed performance degradation and investigating possibilities for efficient comparator implementation is highlighted as an important topic for future development.

5.4 Conclusions on Design Considerations

In this chapter, various design challenges associated with the implementation of a Leapfrog ADC has been considered. The underlying motivation for the considered design choices has been to reach the specifications of table 1.1 with the lowest possible power consumption. Practical issues related to the implementation of the individual components, as well as the interaction between them, have been studied. We now summarize the most important findings of this chapter.

For the first integrator of the analog system, an (to the best of our knowledge) unconventional LNA driven, passive integrator is considered a promising alternative to placing the LNA completely outside the ADC. By low-pass filtering and bounding the amplifier output with a digital

control, the LNA contributes directly to the conversion process while simultaneously limiting the signal magnitude processed by the following node of the system. Even when this integrator has a DC-gain of only 10, the requirements on the subsequent integrator is significantly relaxed.

These relaxed requirements should be utilized for reduced power consumption, and open-loop transconductors is considered a promising candidate for the remaining integrators. The two considered approaches for signal summation both has some additional challenges that needs further investigation. Implementation of voltage buffers and additional transconductors, together with investigating an optimized combination of the two summation techniques, is highlighted as an important part of the future development.

Additional design challenges has been discovered by considering circuit examples for the involved active components. When the control contribution, $\boldsymbol{s}(t)$, is fed to the input of the LNA, transient effects such as overshoot and slew-rate might have a considerable impact on the integrator performance. These properties must be considered together with noise and linearity. As an alternative approach, $\boldsymbol{s}(t)$ could be inserted as a current signal at the amplifier output, at the expense of tougher requirements on the comparator.

The considered transconductor implementation seem to be sufficiently linear when the state-vector is bounded by $\pm 10\,\mathrm{mV}$, without any additional linearization techniques. The thermal noise could be reduced by increasing the transconductors ${}^{G_m}/_{I_b}$, at the expense of reduced linearity. This trade-off should be considered together with tuning the state boundary $b_{\boldsymbol{x}}$ for an optimum solution.

An interesting discovery is that offset voltage in the comparator will trigger even order harmonic distortion in the transconductors, and offset cancellation is therefore required for the comparators. A simulation with the comparators implemented as a standard StrongARM latch showed a significant reduction of SNDR. A deeper understanding of how the properties of the comparator relates to the overall ADC performance is required for a future implementation.

Chapter 6

Final Discussions

Some final discussions that did not fit naturally in other parts of the thesis are given in this section.

6.1 Digital Power Consumption

The implementation of the digital estimator is not considered in this thesis. However, in a future implementation of a complete control-bounded ADC, the power consumed by the digital filtering must be considered in the total power budget. All simulations presented in this thesis have used a control of $f_s = 500\,\text{MHz}$, which correspond to an oversampling ratio of 25.

To obtain a rough estimate of the required digital power consumption, an implementation of the reconstruction corresponding to a third order Leapfrog ADC is considered [1]. The filter was synthesized in 28nm CMOS from a SystemC implementation using the Stratus high-level synthesis software tool [29]. The resulting filter had about 5500 logical gates and the estimated power consumption was approximately 1.3mW for a clock frequency $f_s = 500\,\text{MHz}$ and 0.8V supply voltage.

To obtain a rough model for the digital power consumption, let $Q = C_L V_{dd}$ be the charge that flows during the switching of a single logic gate, for a total load capacitance C_L. With a clock frequency f_s, the dynamic current consumption could be estimated as $I_d \approx f_s C_L V_{dd}$ and consequently the power consumption as

$$P = V_{dd} \cdot I_d \approx f_s C_L V_{dd}^2. \tag{6.1}$$

[1] The filter was implemented and synthesized by David André Bjerkan Mikkelsen.

Assuming 1 fF per logic gate, this model would predict a power consumption of about 1.8mW, for the synthesized filter with 5500 gates.

With a reconstruction filter consuming at the order of 1mW, the analog power will make up a small fraction of the total power consumption. Fortunately, several ideas exist for reducing the digital power consumption that was not considered in the implementation referenced here.

6.1.1 Downsampling and FIR Filter

First of all, the mentioned filter implementation produced full resolution output samples at a rate equal to the clock frequency. This is would normally not be necessary and incorporating decimation into the reconstruction filter would yield a significant reduction in the amount of computations required.

Furthermore, in [5], various implementations of the digital estimator is proposed. The algorithm used in the mentioned filter implementation was a parallel IIR version, but an FIR version is also available. As the control signals are $\{+1, -1\}$-valued, the FIR version offers zero multiplications, at the expense of more additions. The FIR version is also convenient for downsampling, as this would amount to computing the output estimates at a rate lower than the acquisition rate of the digital estimator. Determining the most power efficient filter algorithm and incorporating downsampling is a topic for a future project.

6.1.2 Technology Scaling and Low-Level Synthesis

As the considered filter implementation was synthesized from SystemC, the number of gates could probably be reduced by writing register-transfer level (RTL)-code directly. In addition, implementing the filter in the same 22nm process (rather than 28nm) is also expected to reduce the power consumption as the total capacitance decrease with smaller transistors.

6.1.3 Overcomplete and Phase Delayed Digital Control

To reduce the required sampling frequency, conventional oversampling converters often utilize multi-bit quantizers, at the expense of increased linearity requirements [9]. Multi-bit quantizers could have been employed in control-bounded converters as well, but the required component preci-

sion would increase in a similar manner as for conventional oversampling converters [5].

As an alternative to multi-bit quantizers, the overcomplete digital control is proposed in [5]. The basic idea is to have several single-bit quantizers jointly stabilizing the entire analog system (in contrast to the local control loops considered in this thesis). In an overcomplete digital control, each quantizer will observe a mixture of all the analog state vector components. This is achieved by mapping $\boldsymbol{x}(t)$ to a higher dimension via the control observation matrix $\tilde{\mathbf{\Gamma}} \in \mathbb{R}^{N\times M}$, where $M > N$. The output of these quantizers are then combined via $\mathbf{\Gamma} \in \mathbb{R}^{N\times M}$ before entering the nodes of the analog system.

It is shown in [5] that the overcomplete control has a similar effect on conversion noise as the use of multi-bit quantizers, but without the increased linearity requirements. The cost is the increased number of single-bit quantizers as well as the necessary analog implementation of the matrices $\mathbf{\Gamma}$ and $\tilde{\mathbf{\Gamma}}$. The gain from overcomplete control could presumably be further enhanced by combination with a multiphase clock, such that the quantizers operate with a phase delay relative to each other.

These are new concepts that is part of an ongoing research project at ETH Zürich, but they are mentioned here to show some existing ideas for reducing clock frequency and digital power consumption. A lot of research remains to determine wether or not this will be an effective solution for an integrated circuit implementation. However, these are interesting ideas that truly utilize the flexibility of the control-bounded conversion framework, and associated design challenges should be investigated for a future implementation.

6.2 Flicker Noise

The noise analyses and simulations of this thesis has only taken thermal noise into account. Flicker noise may be a dominating noise source within the frequency band of interest and chopping might be considered, at least for the first integrator. However, chopping will typically reduce the effective input impedance [20]. This and other practical issues needs further investigation in a future development and should be considered together with the final choice of integrator topology.

Chapter 7

Conclusions and Future Work

In this thesis, design challenges associated with the implementation of (the analog part of) a control-bounded converter have been studied. The considered high-level architecture is a Leapfrog analog system with a scalar input and a local digital control. With the goal of minimal power consumption, possible circuit implementations is analysed analytically and theoretical results are supported by (pre-layout) schematic simulations.

An effective design process is facilitated by a custom made python framework, supporting design, simulation and evaluation of analog circuits on a schematic level. The python package is written as a general purpose, python based analog design environment, but the object-oriented design methodology has appeared to particularly well-suited for control-bounded converters. By doing the analog circuit design entirely in python, it is possible to integrate with other useful resources such as the control-bounded conversion toolbox [12], which is used for transfer function analysis and post-filtering.

The already existing theoretical background of the Leapfrog ADC has been expanded with the analysis of several non-idealities, not previously treated in literature. The effect of nonlinear integrators on the overall ADC performance is analyzed and the analytical stability guarantee has been extended to include comparator offset voltage, digital delay and clock jitter. The effect of finite DC-gain in the integrators is studied and it has been shown that a small DC-gain of 10 could be tolerated in the first integration stage, conditioned on higher DC-gain in the remaining integrators.

The theoretical analysis led to the proposal of the LNA driven, passive in-

tegrator, achieving the linearity and noise performance of a conventional LNA, while being stabilized by a local digital control loop. Gm-C integrators have been considered for the remaining integration nodes. By designing for a low $^{G_m}/_{I_b}$, the considered transistor-level implementation is sufficiently linear for handling a peak-to-peak input magnitude of 20 mV, without any additional linearization techniques. Increased thermal noise performance could be traded for reduced linearity, which in turn could be compensated by lowering the analog state vector boundary.

Considering transistor-level implementations of the involved active components has revealed new implementation challenges. For example, reducing the number of active elements by using capacitors for voltage summation comes with the challenge of unwanted charge-flow, degrading the system performance. Current summation avoids this issue, but requires additional transconductors and attenuation circuits. Offset voltage in the comparator will trigger even order harmonic distortion when the integrators are implemented as open-loop transconductors.

By discovering these implementation issues, we have gained a better understanding of the fundamental challenges limiting the achievable power efficiency of the considered architecture. Together with convenient software framework and the theoretical analysis, this thesis will hopefully provide a useful background for future development.

7.1 Future Work

The implementation of a low-power, control-bounded ADC will be continued in Ph.D-project, starting in September 2021. In this thesis, several implementation challenges is pointed out together with some possible solutions for the analog part of the converter. In order to limit the power consumption of the overall ADC, it has also become apparent that the clock frequency must be reduced in order to lower the digital power consumption. A key challenge is therefore to choose between the existing ideas for future improvement, such that some of the low-power potential of the control-bounded ADC could be demonstrated within a reasonable implementation time.

Despite the remaining challenges, the considered implementation of the analog system seem to be a promising low-power solution. By investigating possible implementations of the mentioned voltage buffers, attenuation circuits and low-G_m transconductors, a reasonably power-efficient analog system could probably be realized. The comparator requires some

more attention, and other architectures than the StrongARM latch should be considered. In particular, a power- and area-efficient offset cancellation is required.

The overcomplete control is highlighted as a promising solution for reducing clock frequency and possible low-power implementations should be investigated in a future development. A functional analog system would be necessary for demonstrating this functionality. However, showing possible solutions for reduced power consumption on the digital side should probably be prioritized rather than pushing the power consumption of the analog system to a minimum.

Appendix A

Solution to the State-Space Equations

The solution to the system of ordinary differential equations (2.2) may be evaluated using the Laplace transform and the matrix exponential function. The Laplace transformation of (2.2) gives

$$j\omega \boldsymbol{X}(j\omega) - \boldsymbol{x}(0) = \boldsymbol{A}\boldsymbol{X}(j\omega) + \boldsymbol{B}U(j\omega) + \boldsymbol{\Gamma}\boldsymbol{S}(j\omega) \tag{A.1}$$

$$\boldsymbol{X}(j\omega) = (j\omega \boldsymbol{I} - \boldsymbol{A})^{-1} (\boldsymbol{x}(0) + \boldsymbol{B}U(j\omega) + \boldsymbol{\Gamma}\boldsymbol{S}(j\omega)) \tag{A.2}$$

The term $(j\omega \boldsymbol{I} - \boldsymbol{A})^{-1}$ can be written as a power series

$$(j\omega \boldsymbol{I} - \boldsymbol{A})^{-1} = \frac{1}{j\omega}\left(\boldsymbol{I} - \frac{\boldsymbol{A}}{j\omega}\right)^{-1} = \frac{\boldsymbol{I}}{j\omega} + \frac{\boldsymbol{A}}{(j\omega)^2} + \frac{\boldsymbol{A}^2}{(j\omega)^3} + \cdots . \tag{A.3}$$

From the inverse Laplace transform of (A.3), we define

$$\tilde{\boldsymbol{g}}(t) \triangleq \mathcal{L}^{-1}\left\{(j\omega \boldsymbol{I} - \boldsymbol{A})^{-1}\right\} = 1 + t\boldsymbol{A} + \frac{(t\boldsymbol{A})^2}{2!} + \cdots = \exp(t\boldsymbol{A}), \tag{A.4}$$

where exp(.) refers to the matrix exponential.

The time-domain solution to (2.2) is then given by

$$\mathcal{L}^{-1}\left\{\boldsymbol{X}(j\omega)\right\} = \mathcal{L}^{-1}\left\{(j\omega \boldsymbol{I} - \boldsymbol{A})^{-1} (\boldsymbol{x}(0) + \boldsymbol{B}U(j\omega) + \boldsymbol{\Gamma}\boldsymbol{S}(j\omega))\right\} \tag{A.5}$$

$$\boldsymbol{x}(t) = \tilde{\boldsymbol{g}}(t) \cdot \boldsymbol{x}(0) + (\tilde{\boldsymbol{g}} * \boldsymbol{B}u)(t) + (\tilde{\boldsymbol{g}} * \boldsymbol{\Gamma}\boldsymbol{s})(t) \tag{A.6}$$

Appendix B

On the Impulse Response of a Non-ideal Integrator

This appendix gives a justification of the assumption of equation (3.24) used in the stability analysis of section 3.5. The analysis assume the normalized impulse response of the integrator to be non-negative and upper bounded by 1 throughout the control period T.

An ideal integrator with infinite DC-gain has a normalized impulse response $\tilde{g}(t) = 1\ \forall t$, and a finite DC-gain could be modelled by including the leakage term ρ, such that $\tilde{g}(t) = e^{-\rho t}$. However, any real circuit implementation will have additional poles and zeros in the transfer function, giving rise to a more complex impulse response. The purpose of this appendix is to support the assumption $0 \geq \tilde{g}(t) \leq 1\ \forall t \in [0, T)$, even when the integrator is realized by a real circuit implementation.

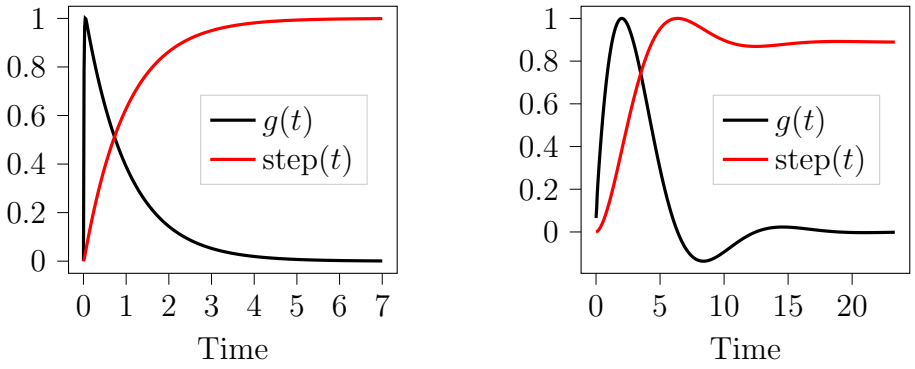
First of all, the assumption $\tilde{g}(t) \leq 1\ \forall \in [0, T)$ follows from the definition of the normalized impulse response $\tilde{g}(t)$. For an integrator with impulse response $g(t) = \beta e^{-\rho t}$, the normalized impulse response $\tilde{g}(t) = e^{-\rho t}$ is clearly upper bounded by 1. For a system with a more complicated impulse response, we define

$$\beta \triangleq \max_{t \geq 0} g(t) \tag{B.1}$$

such that $\tilde{g}(t) \leq 1\ \forall t$ is still satisfied.

The second part of the assumption, $\tilde{g}(t) \geq 0\ \forall t \in [0, T)$, might not be true for certain implementations. Figure B.1a shows the normalized magnitude of the impulse and step response of a system whose transfer function has real poles only. In consequence, the step response settles

exponentially without any oscillations and $\tilde{g}(t) \geq 0 \ \forall t$. Figure B.1b on the other hand, shows the impulse and step response of a system with a mixture of real and complex conjugated poles and zeros in the transfer function. As a result, the step response oscillates before settling, causing a periodic sign change in $\tilde{g}(t)$.



(a) A system with real poles only

(b) A system with complex poles

Figure B.1: Impulse response and step response, normalized to their maximum amplitude.

For a system where $\tilde{g}(t)$ oscillates around zero, we assume the control period T to be chosen such that $\tilde{g}(t) \geq 0 \ \forall t \in [0, T)$. This might not be true for certain implementations, but we argue that this will be a reasonable assumption for most systems approximating the behaviour of an ideal integrator.

Appendix C

VerilogA Model for the Ideal Comparator

```
module comparator_fd(in_p, in_n, clk, gnd, vdd, out_p, out_n, rst_n);
        parameter dly = 0, ttime = 10p;
        input in_p, in_n, clk, gnd, vdd, rst_n;
        output out_p, out_n;
        electrical in_p, in_n, clk, gnd, vdd, out_p, out_n, rst_n;
        real val_p, val_n, thresh;
        real sample_p, sample_n, vrst;

        analog begin
                thresh = V(vdd) / 2;
                @(cross(V(clk)-thresh, -1)) begin
                        vrst = V(rst_n);
                        if (vrst > thresh) begin
                                sample_p = V(in_p);
                                sample_n = V(in_n);
                                if (sample_p >= sample_n) begin
                                        val_p = V(vdd);
                                        val_n = 0;
                                end
                                else begin
                                        val_n = V(vdd);
                                        val_p = 0;
                                end
                        end
                        else begin
                                val_p = thresh;
                                val_n = thresh;
                        end
                end
                V(out_p) <+ transition(val_p, dly, ttime);
```

```
                V(out_n) <+ transition(val_n, dly, ttime);
        end
endmodule
```

Appendix D

Spectre Netlist for Behavioural Leapfrog Simulations

D.1 Floating-Gate Voltage Summation

```
// Generated for: spectre
// Design library name: CBC
// Design cell name: tb_lf_ideal
simulator lang=spectre
global 0
include "$SPECTRE_MODEL_PATH/design_wrapper.lib.scs" section=
    tt_pre


// Library name: CBC
// Cell name: ideal_ota
// View name: schematic
subckt ideal_ota avdd avss vin vip vop von
A vop von vip vin vcvs gain=10.0k
ends ideal_ota

ahdl_include "/home/fredrief/projects/veriloga/comparator_fd/
    veriloga/veriloga.va"
// Library name: CBC
// Cell name: comparator_ideal
// View name: schematic
subckt comparator_ideal in_p in_n clk gnd vdd out_p out_n
    rst_n
parameters dly ttime
Q0 in_p in_n clk gnd vdd out_p out_n rst_n comparator_fd dly
```

```
    =0 ttime=ttime
ends comparator_ideal

// Library name: CBC
// Cell name: gm_fd_ideal
// View name: schematic
subckt gm_fd_ideal in_p in_n out_p out_n gnd
parameters gm
G0 out_n out_p in_p in_n vccs type=vccs gm=gm
ends gm_fd_ideal

// Design library name: CBC
// Design cell name: tb_lf_ideal
VDD vdd 0 vsource dc=800.0m type=dc
VCLK clk 0 vsource type=pulse val0=800.0m val1=0 period=2.0n
    rise=1.0p fall=1.0p
VS u 0 vsource type=sine sinedc=0 ampl=10.0m freq=488.28125k
    mag=1 delay=2e-06
VSTUP vstup 0 vsource type=pulse val0=0 val1=800.0m period=1
    width=1.0u fall=1p rise=1p
VDELAY vdelay 0 vsource type=pulse val0=0 val1=800.0m period
    =1 width=2.0u fall=1p rise=1p
VDELAY_N vdelay_n 0 vsource type=pulse val0=800.0m val1=0
    period=1 width=2.0u fall=1p rise=1p
VSTUP_N vstup_n 0 vsource type=pulse val0=800.0m val1=0
    period=1 width=1.0u fall=1p rise=1p
C1P u zp capacitor c=20.0f
C1N 0 zn capacitor c=20.0f
C2P zp otaon capacitor c=2.0f
C2N zn otaop capacitor c=2.0f
A0 vdd 0 zn zp otaop otaon ideal_ota
ROP otaop x0n resistor r=300.0k
RON otaon x0p resistor r=300.0k
CL0P x0p 0 capacitor c=132.62911924f
CL0N x0n 0 capacitor c=132.62911924f
Q0 x0p x0n clk 0 vdd s0p s0n vdelay_n comparator_ideal dly=0
    ttime=1p
Ck0p s0p zp capacitor c=312.5a
Ck0n s0n zn capacitor c=312.5a
Gm1 vfg1p vfg1n x1p x1n 0 gm_fd_ideal gm=-2.513274123u
CL1P x1p 0 capacitor c=20.0f
CL1N x1n 0 capacitor c=20.0f
Q1 x1p x1n clk 0 vdd s1p s1n vdelay_n comparator_ideal dly=0
    ttime=1p
xbuf1p x0_bufp 0 x0p 0 vcvs gain=1
xbuf1n x0_bufn 0 x0n 0 vcvs gain=1
Cb1p x0_bufp vfg1p capacitor c=64.0f
Cb1n x0_bufn vfg1n capacitor c=64.0f
Ck1p s1p vfg1p capacitor c=1.6f
Ck1n s1n vfg1n capacitor c=1.6f
```

```
Gm2 vfg2p vfg2n x2p x2n 0 gm_fd_ideal gm=-2.513274123u
CL2P x2p 0 capacitor c=20.0f
CL2N x2n 0 capacitor c=20.0f
Q2 x2p x2n clk 0 vdd s2p s2n vdelay_n comparator_ideal dly=0
    ttime=1p
xbuf2p x1_bufp 0 x1p 0 vcvs gain=1
xbuf2n x1_bufn 0 x1n 0 vcvs gain=1
Cb2p x1_bufp vfg2p capacitor c=64.0f
Cb2n x1_bufn vfg2n capacitor c=64.0f
rbuf2p vr2p 0 x2p 0 vcvs gain=1
rbuf2n vr2n 0 x2n 0 vcvs gain=1
Cr2p vr2n vfg1p capacitor c=1.0f
Cr2n vr2p vfg1n capacitor c=1.0f
Ck2p s2p vfg2p capacitor c=1.6f
Ck2n s2n vfg2n capacitor c=1.6f
Gm3 vfg3p vfg3n x3p x3n 0 gm_fd_ideal gm=-2.513274123u
CL3P x3p 0 capacitor c=20.0f
CL3N x3n 0 capacitor c=20.0f
Q3 x3p x3n clk 0 vdd s3p s3n vdelay_n comparator_ideal dly=0
    ttime=1p
xbuf3p x2_bufp 0 x2p 0 vcvs gain=1
xbuf3n x2_bufn 0 x2n 0 vcvs gain=1
Cb3p x2_bufp vfg3p capacitor c=64.0f
Cb3n x2_bufn vfg3n capacitor c=64.0f
rbuf3p vr3p 0 x3p 0 vcvs gain=1
rbuf3n vr3n 0 x3n 0 vcvs gain=1
Cr3p vr3n vfg2p capacitor c=1.0f
Cr3n vr3p vfg2n capacitor c=1.0f
Ck3p s3p vfg3p capacitor c=1.6f
Ck3n s3n vfg3n capacitor c=1.6f

dc dc maxiters=150 maxsteps=10.0k write="spectre.dc" annotate
    =status
ac ac start=1.0M stop=100.0M annotate=status save=selected
    log=1.0k force=all
tran tran cmin=0 write="spectre.ic" writefinal="spectre.fc"
    method=gear2only annotate=status maxiters=5 save=selected
    stop=34.768u skipdc=no strobefreq=500.0M acnames=ac
    actimes=1.5e-06 strobedelay=1.0n

ic x0p=0.4 x0n=0.4 x1p=0.4 x1n=0.4 x2p=0.4 x2n=0.4 x3p=0.4
    x3n=0.4
simulatorOptions options psfversion="1.1.0" reltol=1e-6
    vabstol=1e-9 iabstol=1e-12 gmin=1e-42
save s0p s0n s1p s1n s2p s2n s3p s3n x0p x0n x1p x1n x2p x2n
    x3p x3n u
TempOp options temp=27
```

D.2 Output Current Summation

```
// Generated for: spectre
// Design library name: CBC
// Design cell name: tb_lf_cs
simulator lang=spectre
global 0
include "$SPECTRE_MODEL_PATH/design_wrapper.lib.scs" section=
    tt_pre


// Library name: CBC
// Cell name: ideal_ota
// View name: schematic
subckt ideal_ota avdd avss vin vip vop von
A vop von vip vin vcvs gain=10.0k
ends ideal_ota

ahdl_include "/home/fredrief/projects/veriloga/comparator_fd/
    veriloga/veriloga.va"
// Library name: CBC
// Cell name: comparator_ideal
// View name: schematic
subckt comparator_ideal in_p in_n clk gnd vdd out_p out_n
    rst_n
parameters dly ttime
Q0 in_p in_n clk gnd vdd out_p out_n rst_n comparator_fd dly
    =0 ttime=ttime
ends comparator_ideal

// Library name: CBC
// Cell name: gm_fd_ideal
// View name: schematic
subckt gm_fd_ideal in_p in_n out_p out_n gnd
parameters gm
G0 out_n out_p in_p in_n vccs type=vccs gm=gm
ends gm_fd_ideal

// Design library name: CBC
// Design cell name: tb_lf_cs
VDD vdd 0 vsource dc=800.0m type=dc
VCLK clk 0 vsource type=pulse val0=800.0m val1=0 period=2.0n
    rise=1p fall=1p
VS u 0 vsource type=sine sinedc=0 ampl=10.0m freq=488.28125k
    mag=1 delay=2e-06
VSTUP vstup 0 vsource type=pulse val0=0 val1=800.0m period=1
    width=1.0u fall=1p rise=1p
VDELAY_N vdelay_n 0 vsource type=pulse val0=800.0m val1=0
    period=1 width=2.0u fall=1p rise=1p
VSTUP_N vstup_n 0 vsource type=pulse val0=800.0m val1=0
```

```
    period=1 width=1.0u fall=1p rise=1p
C1P u zp capacitor c=20.0f
C1N 0 zn capacitor c=20.0f
C2P zp otaon capacitor c=2.0f
C2N zn otaop capacitor c=2.0f
A0 vdd 0 zn zp otaop otaon ideal_ota
ROP otaop x0n resistor r=100.0k
RON otaon x0p resistor r=100.0k
CL0P x0p 0 capacitor c=397.88735773f
CL0N x0n 0 capacitor c=397.88735773f
Q0 x0p x0n clk 0 vdd s0p s0n vdelay_n comparator_ideal dly=0
    ttime=1p
CK0P s0p zp capacitor c=625.0a
CK0N s0n zn capacitor c=625.0a
Gm1 x0p x0n x1p x1n 0 gm_fd_ideal gm=-2.513274123u
CL1P x1p 0 capacitor c=20.0f
CL1N x1n 0 capacitor c=20.0f
Q1 x1p x1n clk 0 vdd s1p s1n vdelay_n comparator_ideal dly=0
    ttime=1p
IDAC1 s1p s1n x1p x1n 0 gm_fd_ideal gm=-39.26990817n
Gm2 x1p x1n x2p x2n 0 gm_fd_ideal gm=-2.513274123u
CL2P x2p 0 capacitor c=20.0f
CL2N x2n 0 capacitor c=20.0f
Q2 x2p x2n clk 0 vdd s2p s2n vdelay_n comparator_ideal dly=0
    ttime=1p
IDAC2 s2p s2n x2p x2n 0 gm_fd_ideal gm=-39.26990817n
GMA2 x2p x2n x1p x1n 0 gm_fd_ideal gm=39.26990817n
Gm3 x2p x2n x3p x3n 0 gm_fd_ideal gm=-2.513274123u
CL3P x3p 0 capacitor c=20.0f
CL3N x3n 0 capacitor c=20.0f
Q3 x3p x3n clk 0 vdd s3p s3n vdelay_n comparator_ideal dly=0
    ttime=1p
IDAC3 s3p s3n x3p x3n 0 gm_fd_ideal gm=-39.26990817n
GMA3 x3p x3n x2p x2n 0 gm_fd_ideal gm=39.26990817n

dc dc maxiters=150 maxsteps=10.0k write="spectre.dc" annotate
    =status
ac ac start=1.0M stop=100.0M annotate=status save=selected
    log=1.0k force=all
tran tran cmin=0 write="spectre.ic" writefinal="spectre.fc"
    method=gear2only annotate=status maxiters=5 save=selected
    stop=34.768u skipdc=no strobefreq=500.0M acnames=ac
    actimes=1.5e-06 strobedelay=1.0n

simulatorOptions options psfversion="1.1.0" reltol=1e-6
    vabstol=1e-9 iabstol=1e-12 gmin=1e-42
save s0p s0n s1p s1n s2p s2n s3p s3n x0p x0n x1p x1n x2p x2n
    x3p x3n u
TempOp options temp=27
```

Appendix E

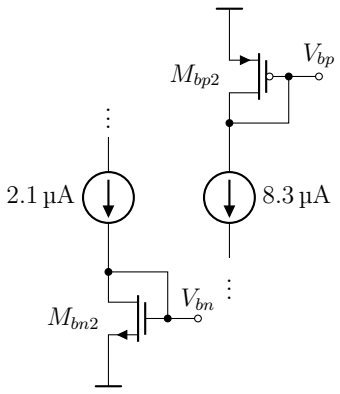
OTA Details

To provide a complete background for how the simulation results of section 5.3.1 was obtained, some additional design details for the OTA of figure 5.13 is given in this appendix.

Because the OTA is used with capacitors in both feedback and feed-forward (cf. figure 5.1), there is no DC-path from the gate of the input transistors $M_{1,2}$ to ground. Gate-leakage of M_1 and M_2 would therefore cause the input common-mode voltage to drift towards one of the rails. To avoid this issue, thick-oxide I/O devices are used for the input transistors. To set the desired voltage on the input node, the input inverters are reset during start-up, by connecting the gate and drain of $M_{1,2}$ using ideal switches.

Furthermore, to keep the bias transistor M_{bp1} from entering the triode-region, the threshold voltage of M_2 is lowered by connecting its bulk to -2V. As a rather complex circuit would be required for generating a stable voltage of -2V in a real implementation, a different solution is preferred in a future development.

The bias voltages, V_{bn} and V_{bp}, are generated by the circuit of figure E.1a, and ideal models are used for the current sources. All device dimensions are given in figure E.1b. The common-mode feedback (CMFB) network is realized by two ideal, noiseless resistors of 1 MΩ, connected between the outputs and the V_{cmfb} node of figure 5.13. The complete spectre netlist for the OTA is given in appendix E.1.



(a) Bias circuit for OTA

(b) OTA transistor dimensions

Device	Size (W/L)	Unit
M_1	$^{508}/_{100}$	nm
M_2	$^{2830}/_{100}$	nm
$M_{3,4,5}$	$^{112}/_{200}$	nm
M_6	$^{414}/_{200}$	nm
M_{bn}	$^{115}/_{200}$	nm
M_{bp}	$^{1280}/_{200}$	nm

Figure E.1: OTA bias circuit and device dimensions.

E.1 Netlist

```
// Library name: CBC
// Cell name: OTA
// View name: schematic
subckt OTA gnd inn inp outn outp vdd vstup
VNEG vneg 0 vsource dc=-2 type=dc
M1A outp1 inn dn vdd nch_io m=1 w=508.0n l=100.0n
M1B outn1 inp dn vdd nch_io m=1 w=508.0n l=100.0n
M2A outp1 inn dp vneg pch_io m=1 w=2.83u l=100.0n
M2B outn1 inp dp vneg pch_io m=1 w=2.83u l=100.0n
MBN dn biasn gnd gnd nch m=1 w=115.6n l=200.0n
MBP dp biasp vdd gnd pch m=1 w=1.28u l=200.0n
M3A outp1 outp1 gnd vdd nch m=1 w=111.8n l=200.0n
M3B outn1 outn1 gnd vdd nch m=1 w=111.8n l=200.0n
M4A outn outp1 gnd vdd nch m=5 w=111.8n l=200.0n
M4B outp outn1 gnd vdd nch m=5 w=111.8n l=200.0n
M5A outn bp vdd gnd pch m=1 w=414.0n l=200.0n
M5B outp bp vdd gnd pch m=1 w=414.0n l=200.0n
M6A outp1 outn1 gnd vdd nch m=800.0m w=111.8n l=200.0n
M6B outn1 outp1 gnd vdd nch m=800.0m w=111.8n l=200.0n
IBN vdd biasn isource dc=2.1u type=dc
IBP biasp gnd isource dc=8.3u type=dc
MBN2 biasn biasn gnd gnd nch m=1 w=115.6n l=200.0n
MBP2 biasp biasp vdd gnd pch m=1 w=1.28u l=200.0n
RCMFBA outp vcmfb resistor r=1.0M
RCMFBB outn vcmfb resistor r=1.0M
SWIN outp1 inn vstup 0 relay ropen=100.0P rclosed=1.0
SWIP outn1 inp vstup 0 relay ropen=100.0P rclosed=1.0
ends OTA
```

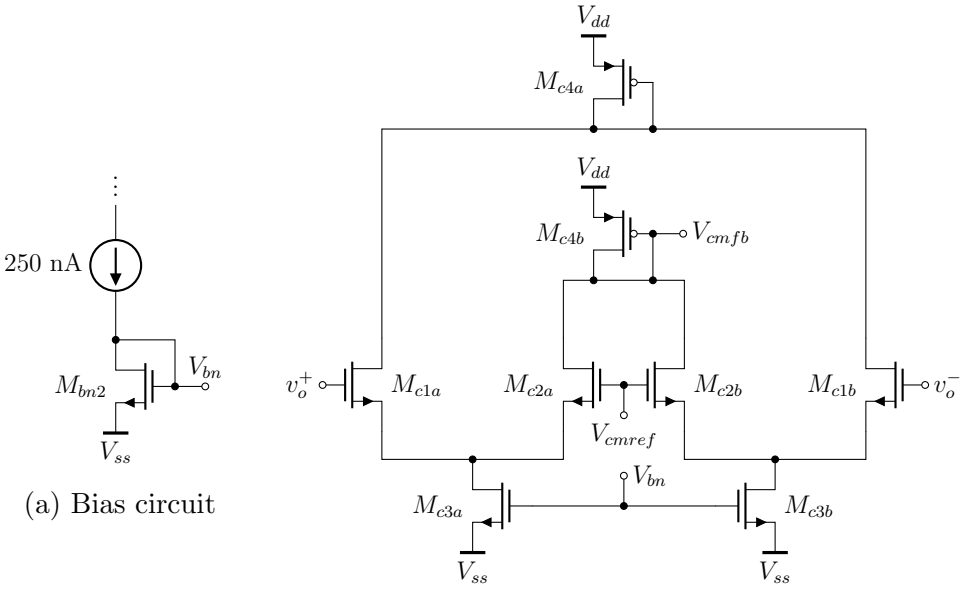
Appendix F

Transconductor Details

Some additional design details for the transconductor of figure 5.16 is given in this appendix.

As the transconductor is used with floating-gate voltage summation, thick-oxide I/O devices are used for the input transistors M_1 to limit the gate-leakage. The DC-voltage of the floating input is set by connecting the transconductors input and output during start-up. The bias circuit generating the voltage V_{bn} is shown in figure F.1a. The same bias voltage is used for the continuous-time CMFB circuit shown in figure F.1b. The common-mode reference voltage, V_{cmref}, is set to 500 mV.

The spectre netlist for the transconductor and the CMFB circuit, which also contains all device dimensions, are given in appendices F.1.1 and F.1.2.



(a) Bias circuit

(b) Common-mode feedback circuit

Figure F.1: Schematic for bias and CMFB circuit

F.1 Netlist

F.1.1 Transconductor

```
subckt gm_basic_nch vip vin outp outn avss avdd vbp vstup_n
parameters Ib
m0 tail vbn avss avss nch m=2 w=300.0n l=1.0u
m0c vbn vbn avss avss nch m=1 w=300.0n l=1.0u
m1a casa vip tail avdd nch_io m=1 w=300.0n l=300.0n
m1b casb vin tail avdd nch_io m=1 w=300.0n l=300.0n
m2a outn avdd casa avss nch m=1 w=200.0n l=1.2u
m2b outp avdd casb avss nch m=1 w=200.0n l=1.2u
m3a outn vbp avdd avdd pch m=1 w=400.0n l=400.0n
m3b outp vbp avdd avdd pch m=1 w=400.0n l=400.0n
SWA outn vstup_n vip 0 pch m=1 w=40.0n l=20.0n
SWB outp vstup_n vin 0 pch m=1 w=40.0n l=20.0n
IB avdd vbn isource dc=Ib type=dc
VOCM vocm avss vsource dc=400.0m type=dc
CMFB avdd avss outp outn vbp vocm CMFB Ib=250.0n
ends gm_basic_nch
```

F.1.2 Common-Mode Feedback

```
subckt CMFB avdd avss vop von vcmfb vcmref
parameters Ib
m1a d1 vop taila avss nch_io m=1 w=500.0n l=300.0n
m1b d1 von tailb avss nch_io m=1 w=500.0n l=300.0n
m2a vcmfb vcmref taila avss nch_io m=1 w=500.0n l=300.0n
m2b vcmfb vcmref tailb avss nch_io m=1 w=500.0n l=300.0n
m3a taila vbn avss avss nch m=1 w=300.0n l=1.0u
m3b tailb vbn avss avss nch m=1 w=300.0n l=1.0u
m4a d1 d1 avdd avdd pch m=1 w=300.0n l=300.0n
m4b vcmfb vcmfb avdd avdd pch m=1 w=300.0n l=300.0n
IB avdd vbn isource dc=Ib type=dc
m3c vbn vbn avss avss nch m=1 w=300.0n l=1.0u
ends CMFB
```

Appendix G

StrongARM Latch Netlist

G.1 StrongARM Latch Core

```
subckt salms avdd dvdd avss clk inn inp outn outp bulkn bulkp
mn1 vipdrain inp s bulkn nch m=1 w=150.0n l=20.0n
mn2 vindrain inn s bulkn nch m=1 w=150.0n l=20.0n
mn3 latchp latchn vipdrain bulkn nch m=1 w=150.0n l=20.0n
mn4 latchn latchp vindrain bulkn nch m=1 w=150.0n l=20.0n
mp1 latchp latchn avdd bulkp pch m=1 w=150.0n l=20.0n
mp2 latchn latchp avdd bulkp pch m=1 w=150.0n l=20.0n
mnck s clk avss bulkn nch m=1 w=150.0n l=20.0n
mpsw1 vipdrain clk avdd bulkp pch m=1 w=150.0n l=20.0n
mpsw2 latchp clk avdd bulkp pch m=1 w=150.0n l=20.0n
mpsw3 latchn clk avdd bulkp pch m=1 w=150.0n l=20.0n
mpsw4 vindrain clk avdd bulkp pch m=1 w=150.0n l=20.0n
inv1 dvdd avss latchp inv1n inv w=150.0n l=20.0n m=1
inv2 dvdd avss latchn inv1p inv w=150.0n l=20.0n m=1
latch dvdd avss inv1n inv1p lop lon reset_latch
inv3 dvdd avss lop outn inv w=150.0n l=20.0n m=1
inv4 dvdd avss lon outp inv w=150.0n l=20.0n m=1
ends salms
```

G.2 Reset Latch

```
subckt reset_latch dvdd avss inp inn outp outn
m1a outn inp avss avss nch m=1 w=150.0n l=20.0n
m1b outp inn avss avss nch m=1 w=150.0n l=20.0n
```

```
m2a outn outp dvdd dvdd pch m=1 w=150.0n l=20.0n
m2b outp outn dvdd dvdd pch m=1 w=150.0n l=20.0n
ends reset_latch
```

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