ACS Photonics

pubs.acs.org/journal/apchd5

Article

GaAs/AlGaAs Nanowire Array Solar Cell Grown on Si with Ultrahigh Power-per-Weight Ratio

Anjan Mukherjee, Dingding Ren, Per-Erik Vullum, Junghwan Huh, Bjørn-Ove Fimland, and Helge Weman*

Cite This: *ACS Photonics* 2021, 8, 2355−2366

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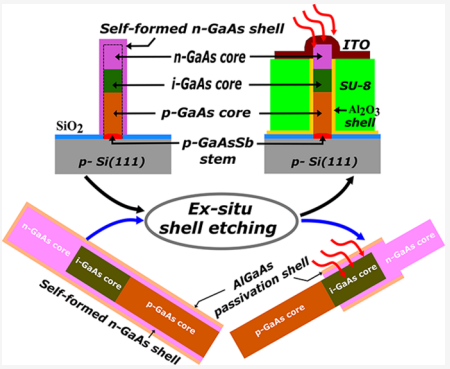
ABSTRACT: Here we demonstrate a more effective use of III−V photoconversion material to achieve an ultrahigh power-per-weight ratio from a solar cell utilizing an axial p-i-n junction GaAs/AlGaAs nanowire (NW) array grown by molecular beam epitaxy on a Si substrate. By analyzing single NW multicontact devices, we first show that an n-GaAs shell is self-formed radially outside the axial p- and i-core of the GaAs NW during n-core growth, which significantly deteriorates the rectification property of the NWs in the axial direction. When employing a selective-area ex situ etching process for the n-GaAs shell, a clear rectification of the axial NW p-i-n junction with a high on/off ratio was revealed. Such a controlled etching process of the self-formed n-GaAs shell was further introduced to fabricate axial p-i-n junction GaAs NW array solar cells. Employing this method, a GaAs NW array solar cell with only ∼1.3% areal coverage of the NWs shows a photoconversion efficiency of ∼7.7% under 1 Sun intensity (AM 1.5G), which is the highest achieved efficiency from any single junction GaAs NW solar cell grown on a Si substrate so far. This corresponds to a power-per-weight ratio of the active III−V photoconversion material as high as 560 W/g, showing great promise for high-efficiency and low-cost III−V NW solar cells and III−V NW/Si tandem solar cells.

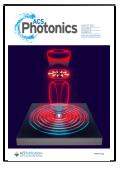


KEYWORDS: *nanowire, solar cell, GaAs on Si, axial junction, shell etching, power-per-weight, molecular beam epitaxy*

Epitaxially grown III−V semiconductor nanowire (NW) arrays have become an emerging solar cell architecture with great promise toward high-efficiency and low-cost solar energy harvest devices.[1] In NW arrays with dimensions comparable to the wavelength of solar radiation, the light−NW interaction can be controlled by both the NW geometry and the pitch of the NW array in order to enhance the solar cell efficiency beyond the Shockley−Queisser theoretical limit from a single planar junction solar cell.[2−6] In addition, the nanoscale footprints of NWs can accommodate lattice mismatch efficiently, resulting in a superior quality of the interface for heteroepitaxial integration and, for example, allow for high-performance III−V semiconductors on a Si platform.[7−9] Since the first demonstrations of self-catalyzed GaAs NW growth by molecular beam epitaxy (MBE)[10−13] with high crystal phase purity through catalyst contact angle engineering[14,15] and compositional modulation,[16,17] significant efforts have been made to achieve high GaAs NW solar cell efficiencies on Si substrates.[18−20] Although MBE has shown an excellent capability for both high-efficiency solar cells in thin-film architecture with an axial p-i-n junction and monolithic integration of III−V NWs on Si, most of the reported NW solar cells grown on Si using MBE have radial p−n junctions.[18−22] Considering the state-of-the-art axial junction GaAs NW devices[23,24] and their flexibility in forming a dual-junction tandem structure monolithically on a Si solar cell, the highest solar cell performance is most likely to be achieved if the GaAs NWs are realized through self-catalyzed MBE growth due to the very high structural quality of the NWs with this method.

In order to improve the solar cell photoconversion efficiency (PCE), it is important to follow an optimized simulated design for a NW array, that is, with a fixed NW diameter, pitch, and length, to achieve enhanced light absorption and light trapping.[25,26] In reality, however, with NW-to-NW inhomogeneities and defects, the contribution of the individual NWs to the whole NW array device performance is an unknown parameter. This can in fact be a limiting factor in a NW array, where the NWs are connected parallel to each other, since the total current from the overall device will be governed by the distribution of individual NW resistances. In a NW array, if a fraction of the NWs is electrically inactive or a fraction of the NWs is electrically shorted due to imperfections arising from

Received: April 6, 2021
Published: August 9, 2021



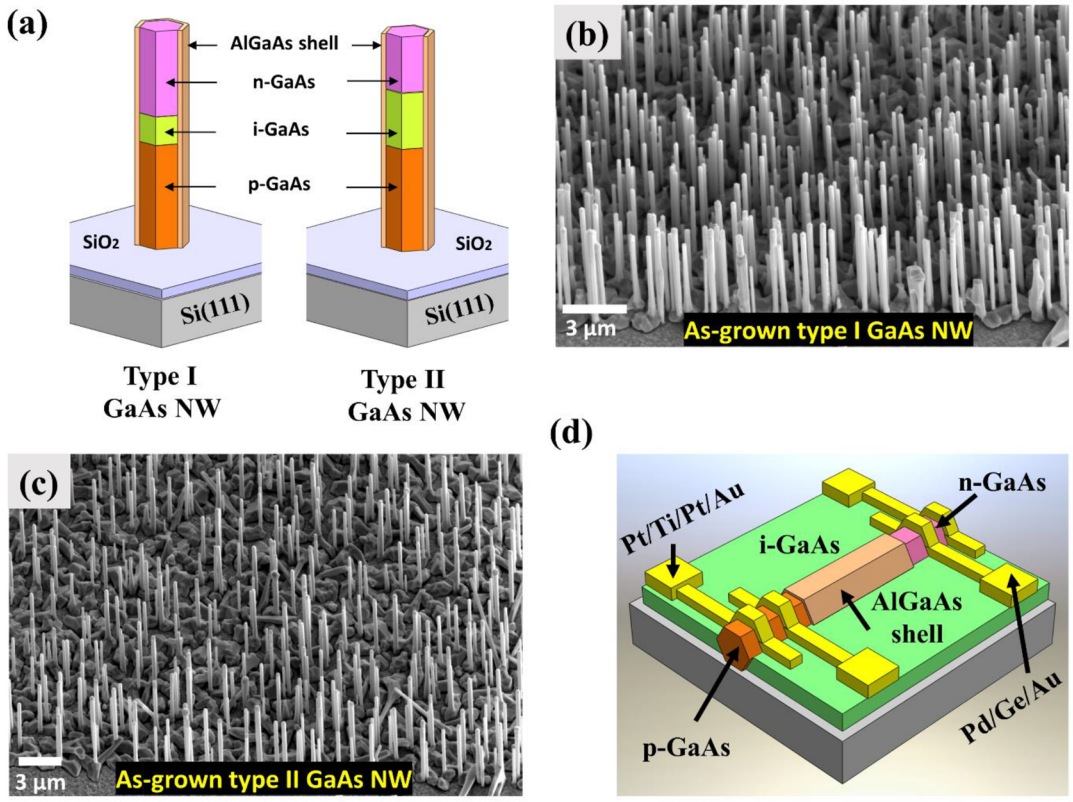


Figure 1. (a) Schematic representation of intended as-grown type I and type II axial p-i-n junction GaAs NWs with a radial $Al_xGa_{1-x}As$ passivation shell (including a thin GaAs capping layer), where the p-, i-, and n-segment length ratios in the type I and type II NWs were 4:1:3 and 4:2:2, respectively. (b, c) Tilted view SEM images of as-grown type I and type II axial p-i-n junction GaAs NWs. (d) Schematic representation of a selective-area shell-etched single GaAs planar NW solar cell device, with the p- and n-GaAs part NW segments shown in dark-orange and pink color, respectively, and the active region (i-GaAs) covered with a radial $Al_xGa_{1-x}As$ passivation shell shown in light-orange color. The position of the p- and n-GaAs NW metal contact electrodes on top of the NW, is shown in yellow color. The green colored layer represents the cured photoresist in which the NW is partly embedded.

the growth or processing, this could affect the overall device performance to a large degree. For example, Mikulik et al. have reported on how the inhomogeneity in the electrical properties of individual GaAs NWs in a NW array can lead to a lowered device performance. By analyzing the individual NW conductance with a conductive atomic force microscopy (C-AFM) mapping technique, they found that almost half of the NWs in a NW array were electrically dead.[27] At the same time, Krogstrup et al. have demonstrated that a vertical single GaAs NW solar cell is capable of achieving a PCE beyond the theoretical Shockley−Queisser limit if the single NW has a well optimized design.[19] It is thus not enough to have a high density of NWs in a NW array according to an optimized simulation design; in addition, a majority of the NWs must have homogeneous characteristics over the active device area in order to efficiently contribute to the overall device performance. For axial junction NW arrays grown by MBE, some of such unwanted NW-to-NW inhomogeneity arises due to an undesired radial shell growth,[28] which can give rise to electrical shortening in the NW solar cell. For example, it has been reported that there is severe radial shell growth induced for self-catalyzed Te-doped GaAs NWs grown by MBE.[28] This could be due to an enhanced binding energy of surface-diffused Ga adatoms on the GaAs NW sidewalls in the presence of Te.[16] In such cases it is crucial to remove this self-formed radial shell from the NW through an in situ or ex situ etching process in order to enhance the PCE of the device.[29,30]

In a metal−organic vapor-phase epitaxy (MOVPE) reactor, a hydrogen chloride (HCl) etching agent with a H_2 carrier gas can be introduced in situ to etch the self-formed radial shell during the growth of the NW.[31] Meanwhile, the NW crystal quality can also be improved through the removal of crystal defects that arise during such unintentional radial growth.[31] However, such an in situ etching strategy cannot be applied for MBE grown NWs due to the ultrahigh vacuum conditions. Successful realization of axial junction GaAs NW solar cells grown by MBE is thus challenging since the self-formed radial shell needs to be removed ex situ, which has not been reported so far.

In this work, we present an ex situ radial shell-etching process applied to axial p-i-n junction GaAs/AlGaAs NWs grown by MBE, leading to clear rectification behavior with high on/off ratio in both single NW and NW array solar cell devices. First, single axial p-i-n junction GaAs NW solar cell (NWSC) devices were fabricated, and an ex situ selective-area etching process was applied to successfully remove the radial $Al_{0.33}Ga_{0.67}As$ passivation layer and the self-formed radial n-GaAs shell. A significantly improved rectification behavior was observed through electrical measurements of the single NW devices by introducing an optimized ex situ etching process compared to the NWs processed without any etching or an insufficient etching step. Such ex situ etching has been further employed to axial p-i-n junction GaAs NW arrays epitaxially grown on a Si(111) substrate. Implementation of this method

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ACS Photonics 2021, 8, 2355−2366

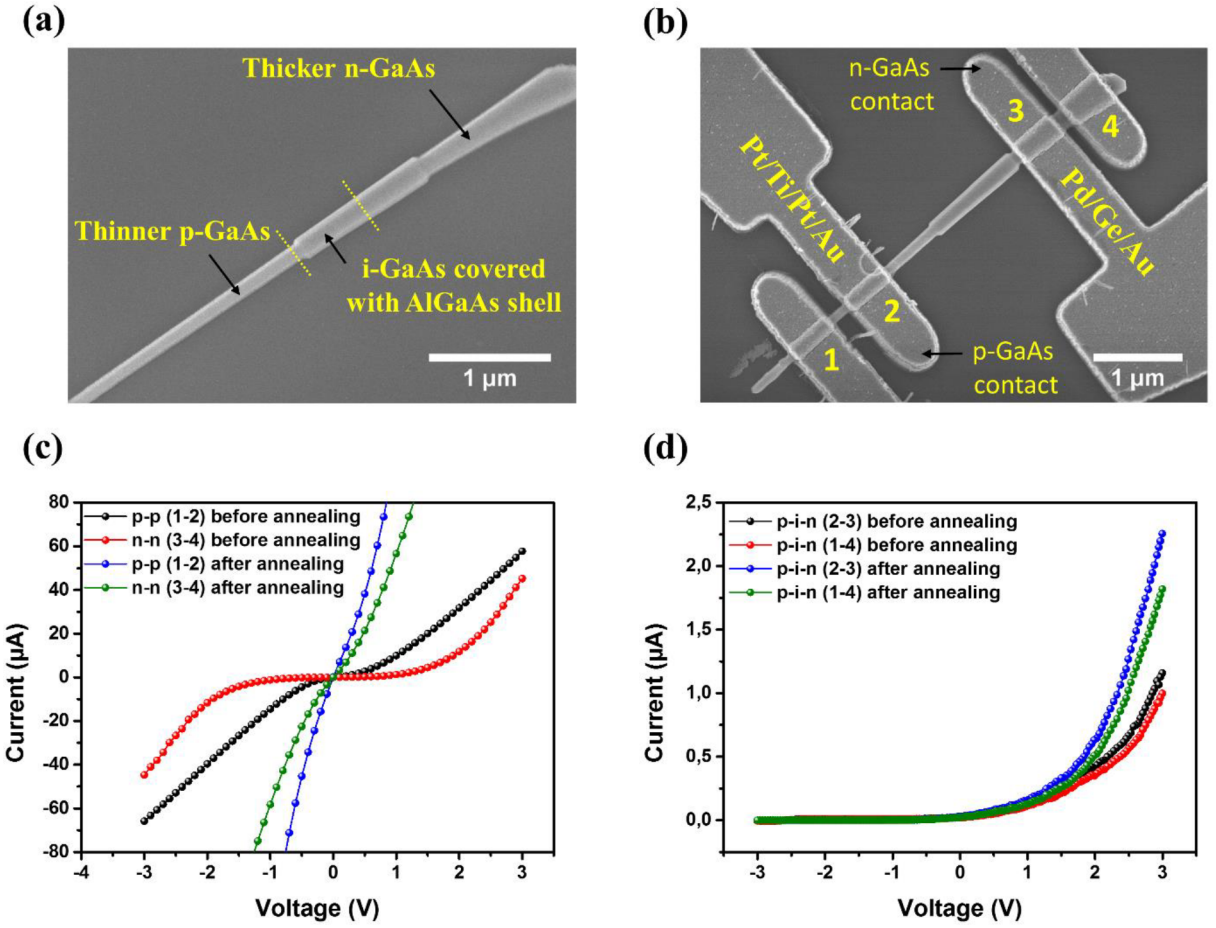

Figure 2. Asymmetrically etched type I single GaAs/AlGaAs NW device: (a) Top view SEM image after $H_3PO_4/H_2O_2/H_2O$ selective-area shell etching for 2.5 and 4.5 min at the n-GaAs and p-GaAs segment part, respectively. The thicker part in the middle of the NW shows the unetched $Al_xGa_{1-x}As$ shell around the active i-GaAs region, whereas the thinner shell-etched part from the n- and p-GaAs segment regions are seen above and below the unetched i-GaAs region. (b) SEM image of the same NW after metal contact fabrication. (c) Dark mode current−voltage characteristics between contacts 1 and 2 (p-p contacts) and contacts 3 and 4 (n-n contacts) before and after contact annealing, respectively. (d) Dark mode current−voltage characteristics between contacts 2 and 3 (inner p-i-n junction) and contacts 1 and 4 (outer p-i-n junction) before and after annealing, respectively.

translates a nonrectifying and poorly performing NW array solar cell (NWASC) to a highly rectifying device with largely improved photovoltaic performances. Based on this, we demonstrate an axial p-i-n junction GaAs NWASC with PCE ∼ 7.7% at 1 Sun intensity (AM 1.5G) from only 1.3% areal coverage of the NWs, corresponding to a class-leading power-per-weight value as high as ∼560 W/g for the active III−V NW photoconversion material.

RESULTS AND DISCUSSION

Structural and Electrical Properties of Selective-Area Shell-Etched Single NWSCs. The intended as-grown structural design of two different axial p-i-n junction GaAs/AlGaAs NWs (type I and type II NWs) grown on a Si(111) substrate and used for the fabrication of single NWSCs are schematically presented in Figure 1a. SEM images (tilted view) of as-grown type I and type II NWs are shown in Figure 1b and c, respectively. The detailed growth mechanism and geometrical dimensions of the NWs are provided in Methods. Figure 1d illustrates the schematic design of a selective-area shell-etched single NWSC device, where p-p and n-n contacts are used to measure the electrical transport properties of the p- and n-segments of the NW and the rectifying characteristics of the p-i-n junction separately. A highly controlled and homogeneous shell etching along the NW length can be observed in a symmetrically shell-etched type I single NW using a multicontact single NW device (see Figure S1(a, b) in the Supporting Information), in which the hexagonal morphology of the NW is found to be intact throughout the shell-etched region. The detailed process for the selective-area etching and precise removal of the shell from the single NW and the fabrication process of a single NWSC device with p- and n-GaAs electrical contacts are explained in Methods.

Interestingly, almost identical dark $I-V$ characteristics measured for p-p (1−2) and n-n (3−4) NW segments, absence of rectification behavior from p-i-n junctions, a rapid increment in the measured current level only for the n-n transport characteristics when contacts are annealed (even though all the contacts were annealed), and the consistency of such a trend in the measured $I-V$ characteristics from NW-to-NW lead to a suspicion that a relatively thick radial n-GaAs shell is formed along the whole NW length during the final axial growth of the n-GaAs core (for details, see Section 1 in the Supporting Information). This results in an electrically shorted axial p-i-n junction, where the axial p- and n-GaAs part of the NW is connected through a conducting radial n-GaAs

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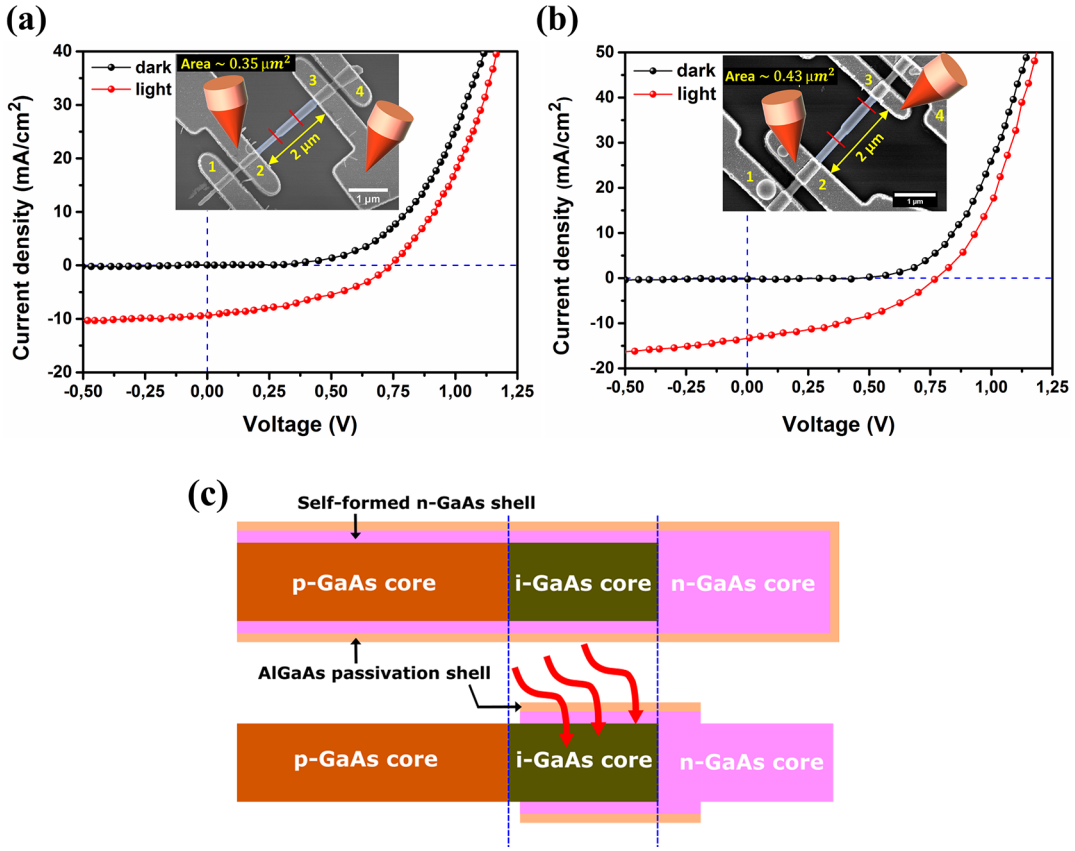

Figure 3. Current density−voltage ($J-V$) characteristics of a planar single NW solar cell device of (a) type I and (b) type II, measured in the dark mode and at 1 Sun intensity. A SEM image for each device is shown in their respective insets. $J-V$ characteristics for both dark mode and at 1 Sun intensity are measured between contacts 2 and 3. The measured area of the single NW solar cell device between contacts 2 and 3 is highlighted with a light blue color in the SEM image for each device. The length of the active device area of these single NW solar cells is ~2 μm (the length between contacts 2 and 3). The i-GaAs NW region in the type I and type II single NW solar cells are between the two solid red lines in the SEM images. (c) Schematic representation of the experimentally concluded single NW geometry before (top) and after (bottom) selective-area shell etching, showing the relative positions of the p-, i-, and n-GaAs NW core segments w.r.t. the AlGaAs-passivation shell and self-formed radial n-GaAs shell.

shell leading to charge carriers leaking through a relatively less resistive n-GaAs shell path instead of passing through the axial p-i-n junction. Due to this, most likely all the metal contacts (Pt/Ti/Pt/Au and Pd/Ge/Au) used as p- and n-GaAs electrodes in the symmetrically shell-etched NW device were therefore deposited onto the radial n-GaAs shell instead of on the axial p- and n-GaAs NW segments separately.

However, by making an intentional asymmetric etching profile in the single NW (type I), where an overetching on the p-GaAs segment side was made until the n-GaAs and p-GaAs segment part electrically separates from each other (a relatively thinner p-GaAs than n-GaAs segment and an unetched intrinsic part covered with an AlGaAs passivation shell can be noticed in Figure 2a,b), nonidentical $I-V$ characteristics were revealed from the p-p (contacts 1 and 2) and n-n (contacts 3 and 4) parts of the NW device and found to be consistent when both the contacts were annealed, as shown in Figure 2c. Both the p-p and the n-n contact pairs turned out to be near ohmic after the contact annealing, suggesting a complete removal of the n-GaAs shell from the p-GaAs segment, which allows the formation of a more proper ohmic p-contact with a p-metal (Pt/Ti/Pt/Au) electrode[32] (see Figures 2c and S1(c) in the Supporting Information).

The near ohmic behavior of the p-p and n-n contacts lead to good rectifying $I-V$ behavior for both the inner (contacts 2 and 3) and outer (contacts 1 and 4) p-i-n junction contact pairs with a high on/off ratio of ~2.6×10^2 at ±3 V, as seen in Figure 2d. More than a 20× improvement in the on/off ratio (~5.9×10^3 at ±3 V) was observed after contact annealing. This clearly suggests that a well optimized selective-area shell etching is essential in axial p-i-n junction GaAs NW devices grown by MBE in order to avoid any shorting or leakage due to the radial n-GaAs shell self-formed during the growth of the axial n-GaAs NW core (see Figures 2d and S1(d)).

Analysis of Single NWSC Devices (Type I and Type II NWs). SEM images of a planar single GaAs NWSC type I and type II device are shown in Figure 3a and b, respectively. The inner contact pair of the device (contacts 2 and 3) was used to measure the photovoltaic performance at 1 Sun intensity such that the series resistance from the uncontacted part of the p- and n-GaAs NW is minimized. The measured area of these single NWSC devices between contacts 2 and 3 is indicated by the light-blue colored area shown in Figure 3a,b. The experimentally concluded single NW geometry in planar configuration before (top) and after (bottom) selective-area shell-etching is schematically presented in Figure 3c, where the relative positions of p-, i-, and n-GaAs core w.r.t. the AlGaAs-passivation shell and the self-formed n-GaAs shell are indicated. At 1 Sun intensity, an open-circuit voltage (V_{oc}) of ~0.72 and ~0.77 V and a short-circuit current density (J_{sc}) of

https://doi.org/10.1021/acsphotonics.1c00527
ACS Photonics 2021, 8, 2355−2366

~9.7 and ~14 mA/cm^2 are observed from the type I and type II single NWSC devices, respectively. The Filling Factor (FF) was measured to be around 40% for both devices, which results in a PCE of 2.83% and 4.34% from the type I and type II devices, respectively. In order to check the consistency of type I and type II single NW devices, five single NWSC devices were measured for each type of NW in this work. The devices presented in Figure 3a,b are the ones with the maximum PCE. In summary, single NWSCs show a V_{oc} ~ 0.67 ± 0.06 V (type I) and ~0.78 ± 0.05 V (type II), J_{sc} ~ 9.4 ± 0.4 mA/cm^2 (type I) and ~13.5 ± 0.5 mA/cm^2 (type II), FF ~ 40.4 ± 0.9% (type I) and 40.1 ± 0.9% (type II), PCE ~ 2.54 ± 0.3% (type I) and 4.19 ± 0.15% (type II), respectively. Key performance parameters from these sets of single NWSCs are summarized in Table S1 in Section 2, Supporting Information.

The single NW devices were grown with an extra-long p- and n-GaAs segment length such that multicontact electrodes could be fabricated, as these devices were also intended to be used for the investigation of the detrimental effect on the electrical properties of the NWs due to the self-formed radial n-GaAs shell, as described earlier. Although the total length for both type I and type II NWs are ~5.2 μm, the active device length of the single NWSCs is designed to be ~2 μm, defined by the relative positions of the n- and p-GaAs inner contacts, as shown in Figure 3a,b. The active segment lengths of the p-, i-, and n-GaAs parts of type I and type II single NWSCs are summarized in Table 1. The relatively higher PCE in the type II device compared to the type I device is mainly due to the higher J_{sc} value, which is attributed to two factors. First, the active absorber (i-GaAs) is about twice as long in the type II NW (~1.3 μm) compared to the type I NW (~0.65 μm), which will result in a higher amount of carrier generation in the active region.

Table 1. Active p-, i-, and n-GaAs Segment Lengths in Type I and Type II Single NWSCs

single NWSC structure	active p-GaAs length (nm)	i-GaAs length (nm)	active n-GaAs length (nm)
type I	650	650	650
type II	650	1300	200

Second, due to the shorter emitter length (active n-GaAs part) in the type II NW (~200 nm) compared to the type I (~650 nm), the distance between the i-GaAs/n-GaAs interface and n-contact is much shorter (see Table 1) in the type II single NWSC device, which leads to a higher carrier collection efficiency due to a reduced amount of carrier recombination loss during charge carrier transport through the emitter region.[33] On the other hand, carrier loss at the metal−contact/NW interface is expected to be roughly the same and insignificant for both the type I and type II single NWSCs since the measured $I-V$ values for p-p and n-n contacts do not show any Schottky-like behavior, which is essential for good device performances.

Analysis of NWASC Performance. By analyzing the single NWSC characteristics, the importance of the removal of the self-formed n-GaAs shell from the NW is recognized and thus further implemented to an as-grown GaAs NW array grown on a Si(111) substrate. Growth details for the NW array (type III NW), used for the fabrication of NWASCs can be found in the Methods. A schematic representation of the NWASC device structure with metal bottom-contact, transparent-dielectric filler and transparent-conducting electrode (TCE) for top-contact is presented in Figure 4a. A 30° tilted view SEM image of the shell-etched NW array embedded in a SU-8 etch-back filler and an ITO top-contact is presented in Figure 4b and c, respectively. Furthermore, a cross-sectional TEM image of a fabricated NWASC device processed through ex situ shell etching, is shown in Figure 4d. The detailed process for the preparation of a cross-sectional TEM lamella from a NWASC device is given in Methods. A detailed analysis of the TEM data can be found in Section 5 in the Supporting Information. The fabricated ITO dome-structured top-contact can be noticed both in the SEM and TEM image in Figure 4c,d. See Methods for the detailed process for the fabrication of the NWASC device. As seen in the dark $J-V$ characteristics in Figure 4e, the NWASC device (array #2) shows a clear rectification with an on/off ratio ~866 at ±1 V. On the other hand, no dark mode rectification was detected from the NWASC device processed without a shell etching (array #1; see Figure S3 in Supporting Information), which again indicates the formation of a self-formed n-GaAs radial shell and signifies the importance of using an ex situ shell-etching process to achieve rectification from an MBE grown axial p-i-n-junction GaAs NW.

Measured $J-V$ characteristics of the NWASC device (array #2) at 1 Sun intensity is shown in Figure 4e. A V_{oc} of ~0.62 V and a J_{sc} of ~21.2 mA/cm^2 was measured with a FF of ~59%, resulting in a PCE of ~7.74%.

All the key performance parameters from the measured NWASC and single NWSCs are summarized in Table 2. It is interesting to note that the single NWSCs show a relatively higher V_{oc} of ~0.75 V (average value) compared to the NWASC (array #2) device (~ 0.62 V). This is mainly due to that the single NWSC devices have a radial AlGaAs passivation shell around the active absorber (i-GaAs core) region, which reduces carrier recombination at the single NW surface.[34]

In this work we put an emphasis on enhancing the power-per-weight ratio from a GaAs NWASC device. Thus, the diameter of the NW used in the NWASC device was chosen to be around 150 nm (the NW diameter after shell etching is ~120 nm), such that it lies close to the first absorption peak according to simulation,[25,26] and therefore much less material is utilized for the active III−V material. Through electron beam induced current (EBIC) analysis on vertically standing axial p-i-n junction GaAs NW, Åberg et al. have qualitatively shown that if the n-GaAs emitter and p-GaAs collector segment length in the NW becomes longer than 200 nm and 1 μm, respectively, the minority carrier diffusion length reduces drastically.[23] It suggests that an emitter (n-GaAs) and collector (p-GaAs) segment length in a GaAs NW longer than those values will strongly reduce the carrier collection efficiencies due to the high carrier recombination during their transport through the emitter and collector region. Thus, in this work a segment length of ~200 nm for the n-GaAs and ~1 μm for the p-GaAs was chosen for the type III NWASC device with a similar n-GaAs and p-GaAs doping level as was used by Åberg et al.

The PCE ~ 7.74% from the NWASC device is the highest achieved PCE from any single junction GaAs NW solar cell grown on a Si substrate. Considering that the areal footprint of the NWs only covers around 1.3% of the total surface area of the device, this is a very high value and indicates a very effective use of the active III−V solar cell material. Thus, we have also calculated the III−V material usage and power-per-

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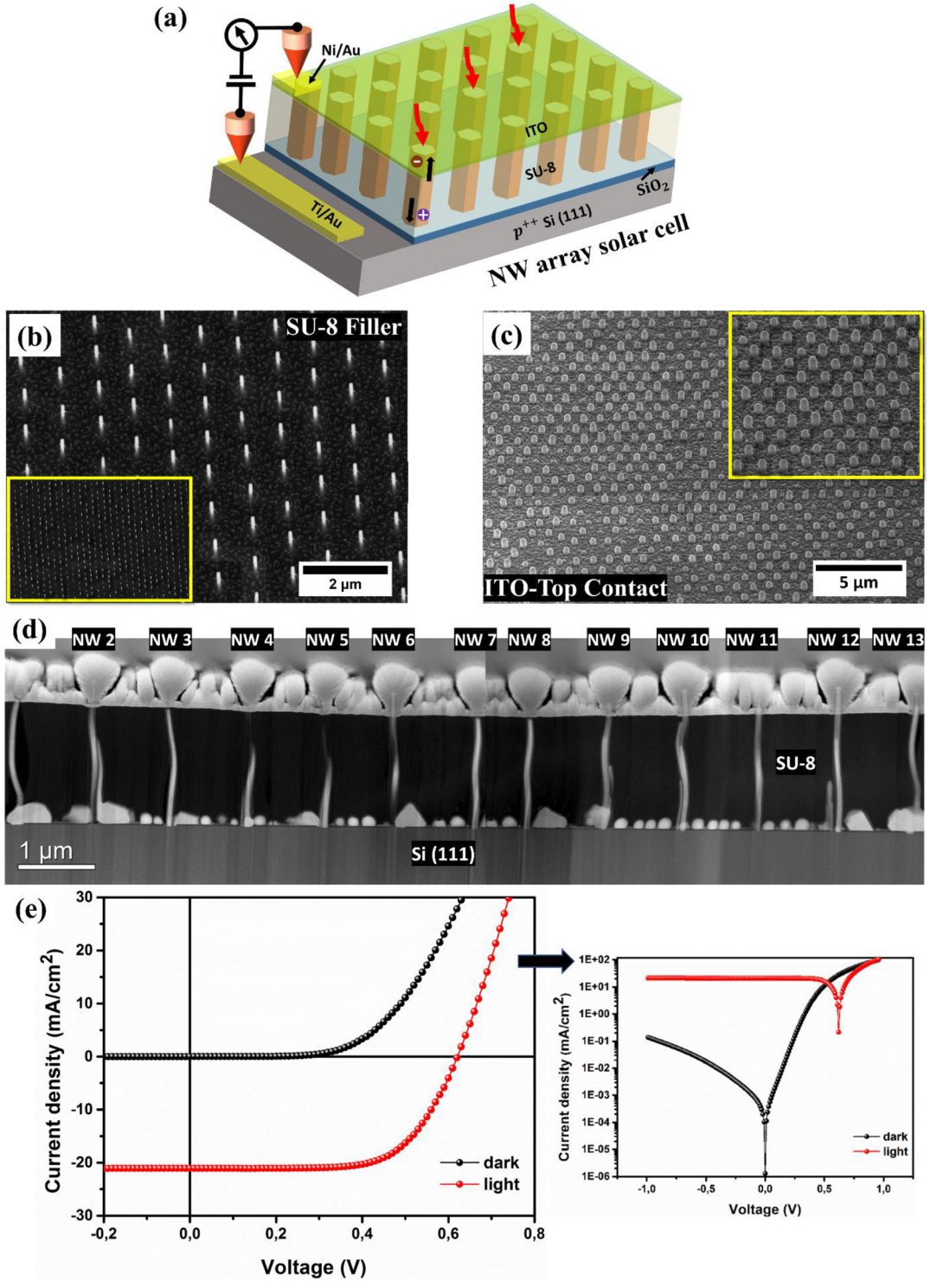

Figure 4. Axial p-i-n junction GaAs NW array solar cell grown on a Si substrate. (a) Schematic representation of a NW array solar cell device with ITO (top) contact, Ti/Au (bottom) contact, and SU-8 filler; (b) 30° tilted view SEM image of the NW array after ALD deposition of 15 nm of Al_2O_3 and the SU-8 filler; (c) 30° tilted view SEM image and (d) cross-sectional HAADF STEM image of the fully fabricated NW array solar cell device including the dome-shaped ITO top-contact (note that there is a stitching error in image (d) between NW 7 and NW 8). The slight wavy bending nature of the NWs in (d) is due to the high temperature curing of SU-8. (e) Current density−voltage (J−V) characteristics of the NW array solar cell device measured in dark mode and at 1 Sun intensity. Log-scale dark- and light-mode J−V curves of the solar cell are shown to the right.

weight ratio of the NWASC device and compared it with other recently demonstrated III−V NW array and thin-film based single junction solar cell devices. The NWASC device in this work shows a power-per-weight value of ∼560 W/g (with a III−V material usage of ∼137 mg/m^2), which is more than three times higher than any other III−V-based single junction solar cell published in the literature, including thin film and NW-based ones. The detailed calculations of the power-per-

https://doi.org/10.1021/acsphotonics.1c00527
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Table 2. Summary of Key Performance Parameters from the Two Single NW Solar Cells (Types I and II) and the NW Array Solar Cell Studied in This Work

parameter	single NW device (type I)	single NW device (type II)	NW array device
device area[a]	0.35 μm^2	0.43 μm^2	500 μm × 500 μm
V_{oc} (V)	0.72	0.77	0.62
I_{sc} (A)	34 pA	60.2 pA	53 μA
J_{sc} (mA/cm^2)	9.7	14.0	21.2
V_{max} (V)	0.51	0.58	0.48
J_{max} (mA/cm^2)	5.5	7.5	16.3
FF (%)	40.6	40.3	58.9
PCE (%)	2.83	4.34	7.74

[a]Note that the NW arrays only cover ∼1.3% of the device area.

weight ratio and areal footprint coverage of the NWs are shown in Section 3, Supporting Information. Table 3 summarizes calculated power-per-weight ratios of this work together with other published III−V based single junction NW and thin film solar cell structures.

At this point, if we particularly compare our work with the previously reported articles summarized in Table 3, the present work has the highest achieved PCE from a GaAs NWASC grown on Si substrate so far. In this work, however, we especially emphasize to also have a very high solar power-per-weight ratio from the GaAs NWASC device, and thus focus on the first order optical absorption peak (∼150 nm) in the GaAs NW rather than on its second absorption peak (∼400 nm), which is more commonly used in the previously reported work, such that much less III−V material consumption is utilized. Thus, arrays with relatively thinner and shorter NWs and larger pitch are used in this work compared to other reported works.

In this regard, one should also pay attention to the fact that the optical modes in a NW array strongly depends on the NW diameter and much less on the array pitch and NW length.[26,35,36] This indicates that the light absorption due to the optical antenna effect is much stronger than the contribution of the light trapping effect in the NW array. This also means that the optical modes are inherent to the single NWs, and several earlier studies show that they do in fact originate from the HE_{1n} waveguide mode in individual NWs.[36−38] This is also supported by the work of Krogstrup et al., who reported that a single vertical GaAs NWSC absorb light from an area much larger than its physical cross-section.[19] In addition to this, there are a few other factors that can contribute to the high PCE in the NWASC, such as the optical antenna effect of the dielectric shell applied through the Al_2O_3 dielectric encapsulation (a continuous Al_2O_3 shell can be seen to cap the vertical GaAs NW in Figure S7(a) in the Supporting Information), surface cleaning (applied through the ex situ wet etching), the ITO-dome structure on top of the NW array, and so on. It has been theoretically and experimentally shown that a dielectric shell with a lower refractive index creates an optical antenna around the NW enabling a doubling of the J_{sc}.[39,40] On the other hand, Cui et al. have shown that an ex situ surface cleaning process can reduce the surface states and enhance the J_{sc} of a NWASC more than three times.[41] This indicates that the ex situ shell etching as presented here is not only allowing removing the self-formed radial n-GaAs shell to achieve rectification from the NWASC device, but also provides efficient surface passivation. In addition to this, the ITO-dome structured top contact of the NWASC device can act as a subwavelength lens, creating an additional enhancement of the optical absorption in the NW array.[42]

CONCLUSION

In summary, we have demonstrated axial p-i-n junction GaAs/AlGaAs NWSC devices grown on a Si substrate by MBE employing an ex situ shell-etching technique. The shell-etching technique was first adopted to single GaAs NWs via selective-area shell etching from the p- and n- GaAs segment side of the NW in a planar embedded NW configuration. The presence of a relatively thick self-formed radially grown n-GaAs shell in the NW structure was concluded from the electrical measurements, and its detrimental shorting effect through enhanced leakage current was explained. The single NW structure has been improved via overetching of the n-GaAs shell from the p-GaAs NW core part, which caused carriers to flow through the p-i-n junction as intended and make the device functional. The shell-etching technique was further implemented to the as-grown axial junction GaAs NW array to produce a NWASC device, which shows a PCE of ∼7.74% with a class-leading power-per-weight ratio as high as ∼560 W/g, achieved from only a ∼1.3% footprint areal coverage of the NW array. We believe that the PCE of the NWASC device can be improved even further (with a maintained ultrahigh power-per-weight ratio) in future studies through further optimization of the NW yield, pitch, diameter, and length.

METHODS

NW Growth Details Used for Single NWSCs (Type I and Type II NWs). Ga self-catalyzed GaAs/AlGaAs NWs were grown in a solid-source Veeco GEN930 MBE system. A heavily p-type doped Si(111) wafer with a 40 nm thermally grown oxide was used as a substrate. Before the growth, electron beam lithography (EBL) and a 30:1 buffered oxide etchant (BOE) was used to pattern the substrate into a nano hole-mask array with triangular lattice structure for the subsequent NW growth. For single NW solar cell devices, two types of axial p-i-n junction structures with different lengths of the i- and n- segments were studied. Both types of NWs have the same Be-doped p-type segment with a nominal length around 2.6 μm, while the lengths of the i-segment and the Te-doped n-segment are around 0.65 and 2 μm, respectively, for type I NWs and 1.3 and 1.3 μm, respectively, for type II NWs. For the NW growth, a Ga flux of 0.7 ML/s and an As_2 flux of 2.5 × 10^{-6} Torr were used at a growth temperature of 625 °C. Carrier concentrations of around 2.4 × 10^{18} cm^{-3} and 2 × 10^{18} cm^{-3} are estimated for the p- (Be-doped) and n- (Te-doped) segments, respectively, calibrated using GaAs thin film values. After the axial part of the NW growth was finished, the Ga catalyst droplet was solidified under an As_2 flux of 1 × 10^{-5} Torr. Following a 2 min congruent evaporation process with the As shutter closed[53] (used to minimize an unwanted n-type radial shell), an undoped radial AlGaAs shell (∼30 nm) were subsequently grown followed by a final thin GaAs (∼5 nm) surface passivation layer.[16]

NW Growth Details Used for NWASCs (type III NW). For the NW array solar cell device, an additional initial Be-doped p-GaAsSb nucleation-stem (∼125 nm) was grown with an Sb flux of 1 × 10^{-7} Torr to improve the growth yield of the vertical NWs in the array.[16] Here, the axial structure of the p-,

https://doi.org/10.1021/acsphotonics.1c00527
ACS Photonics 2021, 8, 2355−2366

Table 3. Power-per-Weight Ratios for III−V Semiconductor NW and Thin-Film-Based Single Junction Solar Cells[a]

Nanowire														
material	substrate	growth method	geometry	NW length (μm)	NW diameter (nm)	NW pitch (nm)	active device area	V_{OC} (V)	J_{SC} (mA/cm^2)	FF	PCE (%)	material usage (mg/m^2)	power-per-weight ratio(W/g)	ref
InP	p-InP(111)B	MOVPE catalyst free	axial p-i-n	2.3	150	513	500 μm × 500 μm	0.73	21	0.73	11.1	856	130.7	41
InP	p-InP(111)B	MOVPE Au-catalyzed	axial p-i-n	1.5	190	470	1 mm × 1 mm	0.779	24.6	0.72	13.8	1068	129.2	1
InP	p-InP(111)A	MOVPE catalyst free	core−shell p-n	2.0	210	400	2 mm × 2.6 mm	0.43	13.7	0.57	3.37	2401	13.97	43
GaAs	GaAs(111)B	MOVPE Au-catalyst	axial p-i-n	3.0	215	400	9 mm × 11 mm	0.906	21.3	0.79	15.3	4179	36.47	23
GaAs	p-GaAs(111)B	MOVPE catalyst free	core−shell p-n	0.9	320	600	500 μm × 500 μm	0.39	17.6	0.37	2.54	1232	20.48	44
GaAs	n-GaAs(111)B	MOVPE catalyst free	core−shell p-n/InGaP passivation	1.3	260	600	500 μm × 500 μm	0.44	24.3	0.62	6.63	1172	56.55	45
GaN	n-Si(111)	CVD Au-catalyzed	p-NW/n-substrate	1.0	100	500	1 cm × 2 cm	0.95	7.6	0.38	2.73	223	61.54	46
InGaAs	p-Si(111)	MOVPE catalyst free	n-NW/p-substrate	3.0	90	200	1 mm × 3 mm	0.37	12.9	0.5	2.4	3023	7.89	47
GaAsP	n-Si(001)	MOVPE Au-catalyzed	core−shell n-p	2.0	320	360	100 μm × 100 μm	0.5	4.54	0.32	0.75	6700	1.08	48
GaAs	p-Si(111)	MBE self-catalyzed	axial p-i-n	2.0	120	1000	500 μm × 500 μm	0.62	21.2	0.59	7.74	137	560.4	this work

Thin Film											
material	substrate	growth method	geometry	thickness (nm)	active device area	V_{OC} (V)	J_{SC} (mA/cm^2)	FF	PCE (%)	material usage (mg/m^2)	power-per-weight ratio (W/g)	ref
GaAs	GaAs	MOVPE	GaAs p-n	>1000	1 cm × 1 cm	1.12	29.8	0.86	29.1	>5320	<53.9	49
GaAs	GaAs substrate and Si carrier	MOVPE	GaAs cell sandwiched b/w InGaP	300	300 μm × 300 μm	1.0	24.5	0.77	19.1	1588	118.7	50
GaAs	glass	MBE	GaAs cell with TiO_2 nanopillar contacts	200	500 μm × 500 μm	0.94	22.0	0.78	16.2	1060	152.1	51
GaAs	GaAs	MOVPE	GaAs cell with Ag nanostructured back reflector	205	2 mm × 2 mm	1.02	24.6	0.79	19.9	1090	181.8	52

[a]Solar power = $V_{OC} \times I_{SC} \times FF$.

https://doi.org/10.1021/acsphotonics.1c00527
ACS Photonics 2021, 8, 2355−2366

Table 4. Summary of Different Dimensions of Type I, Type II, and Type III NWs[a]

NW	p-GaAsSb-stem (nm)	p-GaAs (μm)	i-GaAs (μm)	n-GaAs (μm)	AlGaAs passivation shell (nm)	GaAs cap (nm)
type I	X	2.6	0.65	2.0	30	5
type II	X	2.6	1.3	1.3	30	5
type III	125	1.0	0.8	0.2	X	X

[a]Note: all the segment lengths and shell thicknesses are estimated from nominal growth rate.

i-, and n-segment has an estimated length of 1, 0.8, and 0.2 μm (type III NW), respectively, grown using the same growth temperature and doping concentration as for the type I and type II NWs. To minimize the self-formed n-type radial growth (during the n-GaAs core growth) over the intrinsic region of the NW, the Ga, As_2 and GaTe shutters were opened separately (shutter opening sequence: Ga → (As_2, GaTe) → Ga → (As_2, GaTe)) for 10 s each with a 10 s interval for a total of 6 iterations. No AlGaAs passivation layer was grown for the type III NW sample. The NWs were grown on a 0.5 mm × 0.5 mm oxide hole patterned area with 100 nm hole diameter and 1 μm pitch. Different dimension of the p-, i-, and n- NW segments and shell are summarized in Table 4.

Fabrication of Planar Single NW Solar Cell. Planar single axial p-i-n junction GaAs NW solar cell (NWSC) devices were fabricated utilizing EBL and a selective-area shell-etching process for both type I and type II GaAs NWs. In order to employ a controlled and homogeneous AlGaAs/GaAs shell etching from the single GaAs NW, a $H_3PO_4/H_2O_2/H_2O$ (1:1:200) wet etching recipe was used.[54] For the type I single NWs, an asymmetric etching profile was created, where the AlGaAs/GaAs shell around the NW was etched for 2.5 min with an intentional overetching for 2 min carried out on the p-GaAs segment side additionally. In contrast to this, a symmetric etching for 1.5 min was employed to both the p- and n-segment sides for the type II single NWs. After a successful etching of the shell, single NWs were partially embedded in a curable photoresist layer by employing a resist etch-back method using O_2-plasma ashing.[55] A planar embedded configuration of single NWs has recently been reported as a superior structure compared to a conventional nonembedded structure when an ohmic contact between a NW and its contact electrode is desired.[56] Metal contact electrodes were fabricated to the shell-etched p- and n-parts of the NW by using two successive EBL and lift-off processes, where Pt (5 nm)/Ti (10 nm)/Pt (10 nm)/Au (150 nm) and Pd (20 nm)/Ge (40 nm)/Au (150 nm) metal stacks were deposited on the p- and n-sides of the NW, respectively.[32,57] All metal contacts were annealed at 280 °C for 30 s to form ohmic contacts between the NW and the metal electrodes.[32,57]

Fabrication of NW Array Solar Cell Device. To fabricate a NW array solar cell (NWASC) device, two type III GaAs NW arrays (arrays #1 and #2) were used. The two NW arrays were grown on one sample piece and then separated into two independent sample pieces by scribing and breaking of the substrate. The ex situ shell-etching method, as used for the single NWSCs, was then subsequently applied to the as-grown NW array #2 for 45 s, whereas no shell etching was carried out on NW array #1. In order to provide good surface passivation and to form a dielectric shell acting as an optical antenna around the NWs, an ∼15 nm thin conformal Al_2O_3 layer was deposited on both NW arrays using atomic layer deposition (ALD). A cured SU-8 etch-back layer was then employed as a transparent and insulating filler in order to isolate the bottom p-GaAs NW from the top n-GaAs NW contacts. The SU-8 layer was etched back until the neck of the vertically standing NWs such that the Al_2O_3 dielectric shell is protected by SU-8 except for the top part of the NW. The Al_2O_3 shell from the NW top was then subsequently removed using a dry etch process such that a top electrical contact could be formed at the n-GaAs top of the NW. A bilayer indium tin oxide (ITO) was then deposited by sputtering forming a conformal, transparent, and conducting top electrode (TCE) to the NW array. The bilayer ITO stack is first formed by depositing a ∼5−10 nm thin and highly conducting ITO layer at 80 °C with very low oxygen concentration in order to aid the formation of an ohmic contact with the n-GaAs NW top. On top of this layer an ∼300 nm thick ITO layer was then deposited with higher oxygen concentration at 180 °C in order to provide better transparency. By using this process, the NW arrays were embedded in the SU-8 layer in such a way that an ITO dome-structured array could be fabricated as a top-contact.[42] The active area for the NWASC device in this work is defined in such a way that it does not include the actual physical edge of the nanopattern area, where the last rows of the NW array are not in contact with top ITO layer. This helps to reduce the leakage current in the overall device arising from the imperfection in nanopatterning and/or growth at the boundary of the NW array. A Ni (20 nm)/Au (200 nm) metal stack was then deposited on the ITO outside of the active device area and a Ti (20 nm)/Au (200 nm) bottom contact was formed to the p-Si substrate (after etching out the SiO_2 mask far away from the active device area).

Electrical Characterization of the Single NW and NW Array Solar Cell Devices. The fabricated single NWSC devices comprising either type I or type II NWs, were first characterized through current−voltage ($I-V$) measurements at dark mode using a Keithley 2636A source meter at room temperature. The p-p, n-n, and p-i-n counter parts of each single NWSC device were measured separately before and after the contact annealing process. On the other hand, for the NWASC device, the dark $I-V$ characteristics of the overall device was measured between the top Ni/Au and bottom Ti/Au contact. $I-V$ characteristics for both the single NWSC (type I and type II NWs) and NWASC (type III NW) devices were then measured in a solar simulator at 1 Sun intensity@ AM1.5G using a tungsten-halogen lamp as a white illumination source.

Structural Characterization of the Fabricated NW Array Solar Cell Device. In order to understand the detailed growth mechanisms and structural quality of the NWs, a cross-sectional TEM sample of a processed NWASC device (array #2) was carried out. The cross-section TEM lamella was prepared by focused ion beam (FIB) using a FEI Helios G4 UX system. C layers (e-beam assisted deposition for the first layer) were deposited on top of the region of interest as a protection layer during the Ga^+ ion-beam thinning. The lamella was transferred to a dedicated Cu TEM half-grid by standard lift-out. Coarse thinning was performed with 30 kV acceleration voltage for the Ga^+ ions. Final thinning was done

https://doi.org/10.1021/acsphotonics.1c00527
ACS Photonics 2021, 8, 2355−2366

at 5 and 2 kV on either side of the lamella to minimize surface damage. TEM was performed with a double Cs aberration corrected coldFEG JEOL ARM 200F, operated at 200 kV and equipped with a large solid angle (0.98 srad) Centurio detector for energy-dispersive X-ray spectroscopy (EDS) and a Quantum ER for dual electron energy loss spectroscopy (EELS).

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsphotonics.1c00527.

(1) Symmetrically shell-etched planar single NW devices (type I NW) and their electrical properties. (2) Dark-mode *I*−*V* characteristics of planar single NWSC (type II NW) and NWASC (array #1) devices. (3)Detailed calculation for power-per-weight ratio and areal footprint coverage of NWASC device. (4) The role of the p-Si/p-GaAs interface on device performance and impact of GaAsSb nucleation stem on P-GaAs NW array with electrical data. (5) TEM analysis of the NWs and fabricated NWASC device (array #2) (PDF)

■ AUTHOR INFORMATION

Corresponding Author

Helge Weman − *Department of Electronic Systems, Norwegian University of Science and Technology (NTNU), NO-7491 Trondheim, Norway;* orcid.org/0000-0001-5470-9953; Email: helge.weman@ntnu.no

Authors

Anjan Mukherjee − *Department of Electronic Systems, Norwegian University of Science and Technology (NTNU), NO-7491 Trondheim, Norway*

Dingding Ren − *Department of Electronic Systems, Norwegian University of Science and Technology (NTNU), NO-7491 Trondheim, Norway*

Per-Erik Vullum − *SINTEF Industry, NO-7465 Trondheim, Norway*

Junghwan Huh − *Department of Electronic Systems, Norwegian University of Science and Technology (NTNU), NO-7491 Trondheim, Norway*

Bjørn-Ove Fimland − *Department of Electronic Systems, Norwegian University of Science and Technology (NTNU), NO-7491 Trondheim, Norway*

Complete contact information is available at: https://pubs.acs.org/10.1021/acsphotonics.1c00527

Author Contributions

A.M. designed, fabricated and characterized the NW devices. D.R. designed and grew the NWs. J.H. fabricated p-GaAs NW array contact devices. P.E.V. performed TEM studies on the fabricated NWASC device. A.M. wrote the manuscript with contribution from all authors. B.O.F. and H.W. supervised the project.

Notes

The authors declare no competing financial interest.

■ ACKNOWLEDGMENTS

Mr. Halvor Dolva is acknowledged for assisting the solar simulator measurements performed at MinaLab, University of Oslo and Mr. Gaurav Sharma is acknowledged for the wire bonding of the NW devices done at NTNU NanoLab. We also acknowledge the financial support from the Research Council of Norway through the NANO2021 Program (Grant Nos. 228758 and 239206) and the Norwegian Micro- and Nano-Fabrication Facility, NorFab (Grant No. 295864). The TEM work was carried out on NORTEM infrastructure (Grant No. 197405), TEM Gemini Centre, Norwegian University of Science and Technology (NTNU), Norway.

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