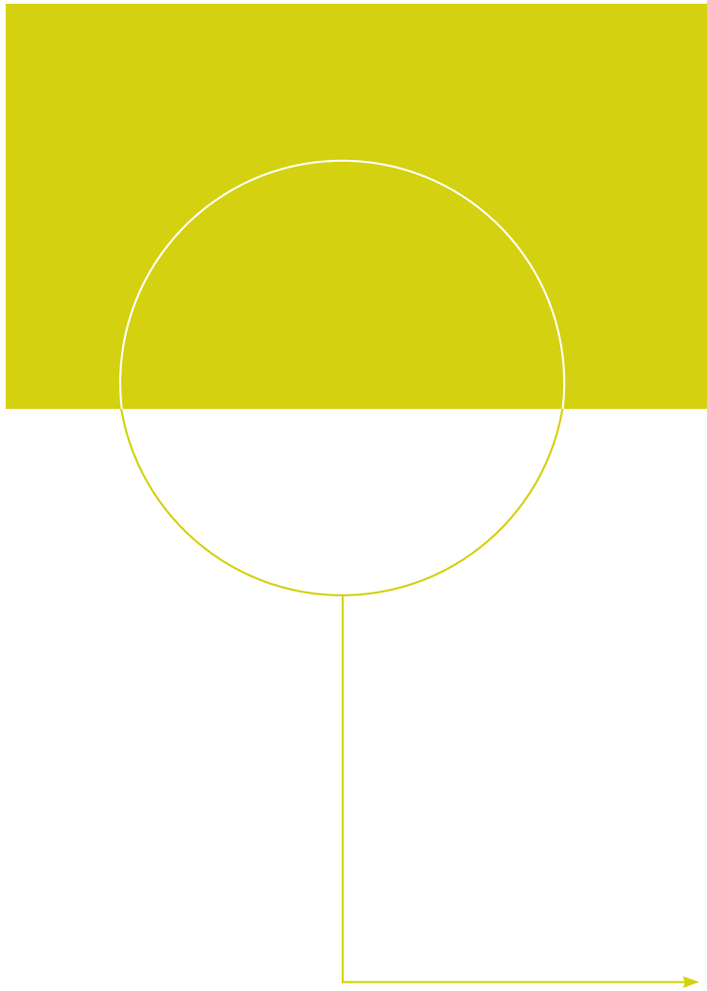

Master's thesis

2020

Gabriela Kazimiera Warden

NTNU
Norwegian University of
Science and Technology
Faculty of Natural Sciences
Department of Materials Science and Engineering

Gabriela Kazimiera Warden

Study and investigation of oxygen related defects in Czochralski silicon ingots

July 2020

NTNU
Norwegian University of
Science and Technology

NTNU
Norwegian University of
Science and Technology

NTNU

Norwegian University of
Science and Technology

Study and investigation of oxygen related defects in Czochralski silicon ingots

Gabriela Kazimiera Warden

Materials Science and Engineering
Submission date: July 2020
Supervisor: Marisa Di Sabatino, NTNU
Co-supervisor: Daniela Cavalcoli, University of Bologna
Mari Juel, SINTEF

Norwegian University of Science and Technology
Department of Materials Science and Engineering

Preface

This thesis has been written for final submission for the course TMT4905 Materials Technology, Master's Thesis from January 2020 to July 2020 and it is the result of a research collaboration between the Norwegian University of Science and Technology, University of Bologna and SINTEF. The experiments in this paper have been conducted at the Department of Materials Science and Engineering in Trondheim, Norway and at the Department of Physics and Astronomy in Bologna, Italy. The main supervisors for this project were Prof. Marisa Di Sabatino from NTNU and Prof. Daniela Cavalcoli from UniBo. This project has also been co-supervised by Dr. Mari Juel from SINTEF Industry.

This work would not be possible to exist without the people involved in it and people that have supported me throughout this experience. I would now like to place some thanks to them.

First of all, I would like to thank my two main supervisors, Prof. Marisa Di Sabatino and Prof. Daniela Cavalcoli. I feel grateful for sharing their knowledge with me along the way. I appreciate their guidance and patience with me and the motivation I have received from both of them. I feel very lucky to have been able to write my master's thesis under their supervision.

Next to them, I would like to thank Mari Juel who has supported this project with her knowledge, experience and guidance. Her input into this work is highly appreciated. To Giovanni Armaroli I would like to thank especially for his patience with me during our long lab sessions and sharing his valuable knowledge from the beginning to the very end of my stay in Bologna.

Finally, I would like to place some thanks to the people near to me and my fellow students. First, to the Semiconductor Physics Group at the University of Bologna for our daily lunch meetings, quizzes and discussions that have made me feel like home. Secondly, to my kind flatmate, Marina for her "winning starts in your head" motto, our long Skype sessions, her support and tea-times. To my other flatmate, Lukas I need to thank for his emotional support (especially during lockdown), our conversations, his advises and the connection we have made for life in the most crazy time of our lives. A big thank you should also be directed to my landlords in Bologna, Giuliano and Patrizia, for the sweet surprises, their help and support during lockdown. To my dear friend Pierpaolo I would like to thank for two wonderful semesters spent together in the labs and our mutual support to each other. To my parents, Katarzyna and Jacek, and my sister Martyna I need to thank for cheering on me and not letting me give up. To my partner Agnieszka I would like to thank for her support, her love, her humor and understanding and for motivating me to do my best. And finally a big thank you to all my other friends and family members that have helped me in a significant way to get through the hard moments: Eva, Agnieszka, Kinga, Lisa, Joanna, Alicja, Güney, Helena, Renil.

Abstract

As the attention to the climate crisis has been getting larger in the past years, the interest in better performing green energy sources has been increasing accordingly. An example of such a source are monocrystalline silicon solar cells, for which the silicon is often produced by the Czochralski process. Investigating ingots produced by this method is the key for further improvement of the production process, which is needed to fulfill the increasing material demand.

Oxygen defects are one of the main sources for lifetime deterioration in monocrystalline Czochralski silicon for solar cell applications. The amount and distribution of interstitial oxygen in two silicon ingots, produced with different pulling speeds by NorSun AS, were previously studied for the purpose of TMT4500, Specialization Project. This master's thesis work was therefore aiming to study the effect of oxygen content and oxygen related defects on the electrical properties of the samples, by the use of Deep Level Transient Spectroscopy (DLTS) and Atomic Force Microscopy (AFM). The samples were varying in terms of thermal history, different position in the ingot, and the pulling speed at which the ingot was produced. In total sixteen samples were prepared for the investigation; eight to be made into diodes, and further studied for the presence of deep level defects by the DLTS-technique, and another eight were meant to be studied for the surface topography and current maps by the use of conductive Atomic Force Microscopy (c-AFM). The performance of the prepared diodes was studied by IV- and CV-measurements which revealed problems with the diode preparation.

As a result of these measurements a more stable method for diode preparation has been proposed, which is the most important result of this thesis. A direct correlation between the interstitial oxygen content and the electrical properties measured in this project, has not been found. It has been found that in general the heat treated samples show a more unstable behaviour during the measurements, however a certain conclusion to this mechanism could not been drawn due to unreliable results. No clear correlation between the pulling speed or the original position in the ingot and the electrical properties has been found, despite obtaining different results for the different samples. A further investigation of this topic should be performed using the proposed new method of diode preparation.

Keywords: CZ-silicon, diode-preparation, thermal donors, oxygen related defects.

Sammendrag

Etter hvert som oppmerkshomheten mot klimakrisen har økt de siste årene, har også interessen for bedre ytelse til grønne energikilder økt. Et eksempel på slike energikilder er monokrystallinske silisium solceller, for hvilke silisiumet produseres ofte ved Czochralski-prosess. Undersøkelse av blokker produsert ved denne metoden er nøkkelen til ytterligere forbedring av prosessen, noe som er viktig for å møte det økende materialbehovet.

Oksygendefekter er en av hovedkildene til forverring av levetiden til monokrystallinske Czochralski silisium blokker for solcelleproduksjon. Innholdet og distribusjon av interstitiell oksygen i to silisium blokker produsert med forskjellige trekkhastigheter av Norsun AS, ble tidligere undersøkt i forbindelse med emnet TMT4500, Fordypningsprosjekt. Denne masteroppgaven hadde da som formål å studere effekten av oksygeninnhold og oksygenrelaterte defekter på elektriske egenskaper til prøvene ved bruk av Deep Level Transient Spectroscopy (DLTS) og Atomic Force Microscopy (AFM). Prøvene som ble karakterisert i denne oppgaven var varierende med hensyn til termisk historie, posisjon i blokken og trekkhastigheten som ble brukt ved produksjonen. Totalt seksten prøver ble preparert for undersøkelsene; åtte som ble gjort om til dioder og videre undersøkt for dypt liggende defekter ved bruk av DLTS-teknikken, og ytterligere åtte var ment til å bli studert for overflate-topografi og strømkart ved bruk av conductive Atomic Force Microscopy (c-AFM). Ytelsen av de preparerte diodene var studert ved IV- og CV-målinger som avdekket problemer med diode-preparering.

Som resultat av de ovennevnte målingene ble en ny og mer stabil metode for diode-prepareing foreslått, som er det viktigste resultatet av denne masteroppgaven. Ingen direkte sammenheng ble funnet mellom interstitiell oksygeninnhold og de elektriske egenskapene karakterisert i oppgaven. Generelt ble det observert at de varmebehandlede prøvene viste en mer ustabil oppførsel under målingene, men en sikker konklusjon for denne mekanismen kunne ikke bli trukket på grunn av usikre resultater. Ingen klar sammenheng ble funnet mellom trekkhastigheten eller posisjon i blokken og de elektriske egenskapene, selv om det var forskjeller i resultater mellom prøvene. Videre undersøkelser av dette emnet bør utføres ved bruk av den nye foreslåtte metoden for diode-preparering.

Nøkkelord: CZ-silisium, diode-preparering, termiske donorer, oksygenrelaterte defekter.

List of Acronyms

A- area
A_{eff}- effective emission area
AFM- Atomic Force Microscopy
$BH_{high}A$- Higher Pulling Speed Heat Treated Body sample for AFM
$BH_{high}D$- Higher Pulling Speed Heat Treated Body sample for DLTS
$BH_{low}A$- Lower Pulling Speed Heat Treated Body sample for AFM
$BH_{low}D$- Lower Pulling Speed Heat Treated Body sample for DLTS
$BU_{high}A$- Higher Pulling Speed Untreated Body sample for AFM
$BU_{high}D$- Higher Pulling Speed Untreated Body sample for DLTS
$BU_{low}A$- Lower Pulling Speed Untreated Body sample for AFM
$BU_{low}D$- Lower Pulling Speed Untreated Body sample for DLTS
C- capacitance
C_0- capacitance at reverse bias
c-AFM- conductive Atomic Force Microscopy
CB- conduction band
$CH_{high}A$- Higher Pulling Speed Heat Treated Crown sample for AFM
$CH_{high}D$- Higher Pulling Speed Heat Treated Crown sample for DLTS
$CH_{low}A$- Lower Pulling Speed Heat Treated Crown sample for AFM
$CH_{low}D$- Lower Pulling Speed Heat Treated Crown sample for DLTS
CNR- Area della Ricerca di Bologna, Consiglio Nazionale delle Ricerche
c_n- capture time constant of the carriers
COP- crystal originated particle
$CU_{high}A$- Higher Pulling Speed Untreated Crown sample for AFM
$CU_{high}D$- Higher Pulling Speed Untreated Crown sample for DLTS
$CU_{low}A$- Lower Pulling Speed Untreated Crown sample for AFM
$CU_{low}D$- Lower Pulling Speed Untreated Crown sample for DLTS
CV- capacitance voltage
CZ- Czochralski
DAQ- data acquisition
DLTS- Deep Level Transient Spectroscopy
$E_{C,min}$- conduction band minimum
EDS- energy-dispersive X-ray spectroscopy
E_F- Fermi energy
E_g- energy gap
e_n- electron emission rate
e_p- hole emission rate
E_T- Energy of deep level state
$E_{V,max}$- Valence band maximum
f- frequency FPP- Four Point Probe
FTIR- Fourier Transform Infrared Spectroscopy
FZ- Float Zone
G- temperature gradient
HPS- Higher Pull Speed
I- current

I_0- dark saturation current
IV- current voltage
J- current density
k- Boltzmann constant
k_c- spring constant
LDLTS- Laplace deep level transient spectroscopy
LPS- Lower Pulling Speed
n_T- density of filled traps
N_T- total density of deep states
N_A- acceptor concentration
N_d- donor concentration
NTD- new thermal donor
OFS- oxidation induced stacking fault
O_i- interstitial oxygen
OIFS- oxidation induced stacking fault
OTD- old thermal donor
P-bronze- phosphorus bronze
PSPD- position sensitive photon detector
PV- photovoltaic
q- magnitude of the electron charge
Q_C- heat from crystal
Q_M- heat from melt
Q_H- heat from heater
Q_L- latent heat
SF- stacking fault
T- temperature
t- time
TD- thermal donor
TDD- thermal double donor
TEM- transmission electron microscopy
V- growth rate (Chapter 4)
V- voltage (from Chapter 6 on)
V_b- built-in voltage VB- valence band
W- depletion layer width
w- depletion layer width Z- complex impedance
δ_c- cantilever deflection
ϵ- material's relative permittivity
τ- time constant

List of Figures

List of Tables

Contents

1 Introduction

1.1 Motivation and background

Affordable and clean energy is one of the seventeen sustainable development goals listed as number seven by the United Nations [14]. Solar energy is one of the most important renewable energy sources. The solar cell market is dominated by silicon based solar cells which make up for over 90% of the total market share. Monocrystalline silicon solar cells make up for 24% of the total market share and it has continued to increase in the last years, according to several sources [15, 16, 17]. As the predictions suggest that the number is only going to increase, there is a need for further investigation of some of the material's characteristics that can affect its performance.

Oxygen related defects are the most important for material's performance in the case of monocrystalline silicon solar cells. Despite wide and extensive research work, there is still a need to understand the mechanisms of these defects, their role on the electrical properties of the solar cells and their link to process parameters, e.g. pulling speed and temperature. Especially thermal donors, electrically active oxygen clusters that display a donor behaviour in silicon, are of interest for the research. It is commonly known that their formation depend on the thermal history of the material, both under production and possible further heat treatment. It is however, still not well understood what the effect of pulling speed could be. Investigating the combination of varying pulling speeds, thermal history and initial oxygen content is therefore an interesting approach to understanding the formation of oxygen related defects and their effect on material's properties.

1.2 Aim and scope of the project

This master's thesis aims to characterize the nature of oxygen related defects in Czochralski grown single silicon crystals. In a sense, it is a continuation of the research made for the specialization project "Effect of Pulling Speed on oxygen distribution in Czochralski silicon ingots". The goal of this master's thesis is to characterize the electrical properties of samples with different origin and treatment to study the effect and the nature of oxygen related defects.
This work will provide a short theoretical introduction into the topic, followed by introduction to the main characterization techniques, such as DLTS and c-AFm. Further a detailed description of the experimental work will be presented, which will be followed by a section where the results will be shared. Due to the international health crisis, the experimental work could not be finished as planned, hence the master's thesis includes also a literature review on the topic of thermal donors and other relevant studies, and some data analysis of the measurements done during the specialization project work. Finally, the results will be discussed and concluded. The final section will be dedicated to possible further work which could have been performed.

2 Concepts from Semiconductors Physics

In order to understand the purpose of the experiments performed in this thesis, a few theoretical chapters will be provided, starting with an introduction to semiconductors physics. Here, p-n junction will be described since its physics is crucial to understanding the behaviour of the samples during the measurements. In addition, some other basic topics will be covered.

2.1 Band structure

The concept of band structure has been previously explained explicitly in the specialization project. Here, only the most important concepts will be highlighted, starting with the difference between an intrinsic and an extrinsic semiconductor.

An intrinsic semiconductor is a pure material which does not contain any foreign elements. The band diagram of this type of semiconductor is often compared to the ones of a metal and an insulator, similar to Figure 1 and it is used to explain the conductive behavior of each of the material types.

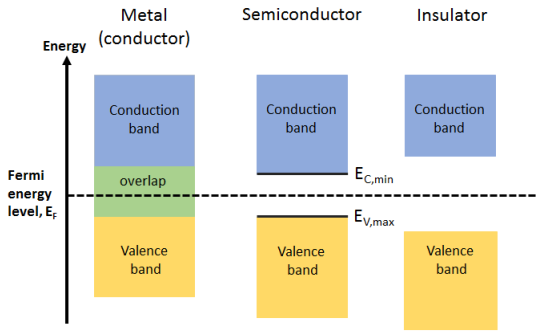

Figure 1: Schematic illustration of band diagrams of a metal, a semiconductor and an insulator, from [1].

For each of the types two distinct bands are presented: conduction band (CB) and valence band (VB) and a schematic position of the Fermi level (E_F) is indicated. Conduction in band is the lowest unoccupied electrons band, while valence band is the highest occupied electron band. Fermi level can be considered as the maximum level where the electrons can gather at absolute zero temperature [3].
In general a material is considered to be conductive when a transfer of electrons

is possible from one band to the other, which is the case for metals where both of the bands overlap.
When it comes to semiconductors and insulators, the two bands are separated by an energy gap (E_g). In the case of insulators the energy gap is so large that the electron transfer is not possible, which results in the material being not electrically conductive.
The size of E_g in semiconductors is smaller than in insulators, allowing the electrons to pass from VB to CB, for instance when temperature is increased. The existence of the band gap is crucial for the photovoltaic application as it enables the electrons to stay in higher energy states to be exploited [3]. As indicated in Figure 1, two energy levels are often noted in the band diagram of semiconductor materials and these are the maximum of the valence band, $E_{V,\,max}$, and the minimum of the conduction band, $E_{C,\,min}$. If those occur at the same crystal momentum, as indicated in Figure 2a), the material is a direct semiconductor (such as GaAs), meaning that an input of energy equal to the value of E_g would be enough to excite an electron from VB to CB. An indirect semiconductor on the other hand, such as silicon, has $E_{V,\,max}$ and $E_{C,\,min}$ occurring at different crystal momenta. In this case, the electron excitation must be accompanied by a phonon, in the form of lattice vibrations so that the change in momentum and energy is conserved [3, 18].

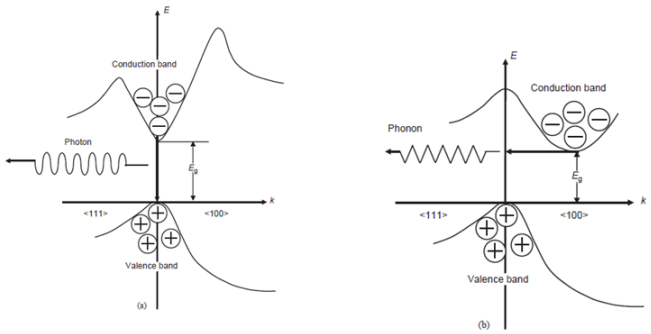

Figure 2: Schematic illustration of: (a) direct band gap semiconductor, (b) indirect band gap semiconductor, modified from [2].

An extrinsic semiconductor is a material which contains foreign elements that introduce new energy levels in the band structure. Foreign elements can be introduced into the material intentionally (doping) or unintentionally (during production process). In this section only the effect of intentionally added impurities on the band diagram will be covered. Figure 3 shows schematically the introduction of new energy levels in the two types of doping which, generally speaking, is caused by an in-balance in the number of charge carriers. In an intrinsic semiconductor the number of holes (positive charge carriers) is equal to the number of the electrons (negative charge carriers) which will be disrupted upon addition of a foreign element [3, 18].

In the case of p-type doping, the new energy level will be introduced by addition of a foreign element having less valence electrons than the matrix element and the new energy level (often described as acceptor energy level) will lie near the valence band. In this case the Fermi level will be located between the acceptor energy level and the valence band and the majority charge carriers will be holes [3].

An n-type doping will introduce a donor energy level that will be located close to the conduction band. In this case the Fermi level will be located between the new energy level and the conduction band. The elements used for n-type doping have more valence electrons than the matrix material, resulting in the release of excess electrons into the material [3].

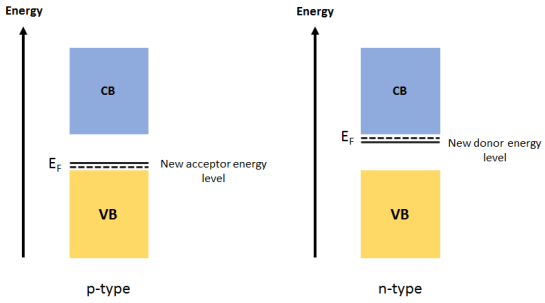

Figure 3: Schematic illustration of the effects of the two types of doping on a band diagram, from [1].

2.2 p-n junction

A p-n junction is created by combining both of the above mentioned types of doping in one system by doping different regions of the same material differently, meaning that one region would be p-doped and the other n-doped. Figure 4 is a schematic illustration representing the band diagrams of (a) p-doped and n-doped materials not in contact and (b) a p-n junction in equilibrium, and this figure is going to be used to explain the details of a p-n junction.

As it can be seen from Fig. 4(a) the p-side of the junction has a higher value of the work function than the n-side, and the electrostatic potential must then be smaller on the n-side [3]. Since in equilibrium, there is a difference in the concentration of the opposing charge carriers, the holes will diffuse from the p-side to the n-side and the electrons will move from the n-side to the p-side of the junction. This leads to the charged impurities being uncovered which results in establishment of an electric field which limits the diffusion of the charges [18].

The region between the two doped regions is called depletion region and it is characterized by lack of the charge carriers and it is a sort of barrier for the majority charge carriers and a low resistance path for the minority carriers [3, 18].

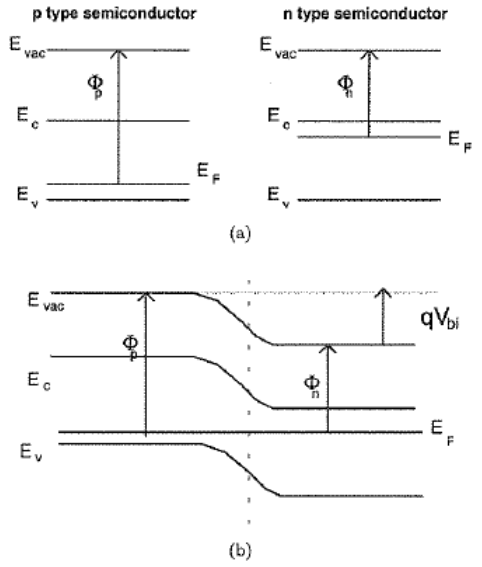

Figure 4: Schematic illustration of the band diagram of (a) a p-doped and n-doped semiconductor material in isolation, (b) a p-n junction in equilibrium, from [3].

3 Solidification of monocrystalline silicon

This section is dedicated to introduce the industrialized production process of monocrystalline silicon ingots called the Czochralski process, followed by a section on incorporation of oxygen during the production process.

3.1 Czochralski process

The process of growing single crystals was first discovered by Jan Czochralski in the 1910's, and it was first used for the production of monocrystalline silicon ingots in 1952 by Teal and Buehler [19]. Since then, the technique has grown to become the most popular method of growing silicon single crystals for photovoltaic applications due to relatively low production costs in comparison to other production methods [20].

An illustration of the production furnace used in Czochralski process is shown in Figure 5 and the most important elements are marked. The design of the furnace is highly advanced to ensure the temperature control during the process. The carbon heater surrounding the crucible is installed to heat the silicon inside the crucible. The heat shield outside carbon heater will ensure that the heat from the carbon heater is not transferred outside of its designated place to the rest of the furnace and it is supported by a water cooled chamber. There is also another heat shield placed above the melt that is not illustrated here. Its role is the reduce the heat flow from the melt to the solidified ingot. This well thought design is allowing the temperature inside the crucible high enough to keep silicon molten, while the temperature outside of the crucible is low enough to ensure sufficiently fast solidification of the pulled ingot. Another part of the system is a so-called cooling jacket. Its exact placement is not widely known, as this technology has mostly been developed "in-house", hence it is not shown on the figure. It is known however, that a cooling jacket must be placed somewhere next to the growing crystal, making the heat extraction from the ingot even more efficient, allowing faster pulling speeds.

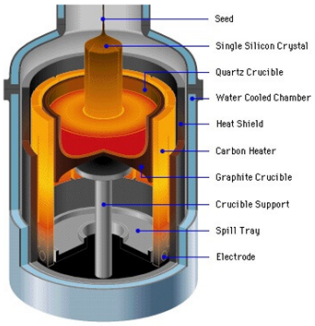

Figure 5: Illustration of the furnace used in Czochralski process, from [4].

The first step of the Czochralski process is feeding the quartz crucible with polycrystalline silicon feedstock. The temperature is then raised above the melting temperature of silicon of 1414 °C to ensure complete melting inside the crucible. The polycrystalline silicon feedstock can only be used for the production of solar grade monocrystalline silicon, since the purity requirements are lower than in the case of silicon produced for electrical industry [2, 21].

After the silicon in the crucible is melted a $< 100 >$- oriented monocrystalline silicon seed is dipped inside the melt, in the case of monocrystalline silicon for solar cell applications. In theory also a $< 111 >$ could be used, but it is not popular. The seed and the crucible with molten silicon are rotating in opposite directions and the pulling can only be started when an equilibrium state between the melt and the seed is reached. This is done by lowering the temperature and when the melt starts to solidify the pulling can be started.

Necking is a process step that must be done in the beginning of the pulling process to ensure a dislocation-free growth throughout the process. When the seed with temperature lower than the melt's temperature is dipped, thermal shocks will introduce some dislocations in the first few centimeters of the pulled ingot. They would usually propagate on the $\{111\}$ planes that are oblique to the $\{100\}$ plane that is usually used for the PV-applications. Necking would eliminate propagation of those dislocations and it is done by increasing the pulling speed in the beginning of the pulling process which can be seen by the existence of so-called "ridges" formed on the crystal [2, 21, 22].

After the necking process is successfully done, the pulling speed is lowered and the process of increasing the diameter is started, forming the crown until the desired diameter is achieved. At this point it is also important to control the temperature; if it is too high, the diameter will be smaller than desired, while too low temperature will result in larger diameter. When the desired diameter is achieved, the pulling speed is increased and the shoulder is formed. Further, the ingot will be pulled at constant speed forming the body. It is however, lowered in the beginning of body formation to control the defect formation and oxygen incorporation. In this part of the process the diameter size is controlled by observing the meniscus of the solid-liquid interface with a camera. If a change in the meniscus is noted, the pulling speed and/or the melt temperature can be adjusted accordingly [18].

When the ingot has reached the desired length, the pulling speed is increased once again to form the tail. The diameter of the tail should be small enough so that the separation from the crucible does not induce dislocations inside the grown crystal. The separated crystal is then left inside the furnace until it cools down to a sufficiently low temperature at which thermal shocks want be a risk when the ingot is removed from the furnace [18].

3.2 Incorporation of oxygen

The most common unintentionally added impurity in monocrystalline silicon ingots is oxygen which comes primarily from the crucible. As oxygen content has an effect on the final material's properties, its incorporation into the crystal is crucial to understand.

As mentioned above, the source of the oxygen contamination is the dissolution of the quartz crucible and in general, more dissolved oxygen in the melt would result in more incorporated oxygen inside the crystal. However, the amount of oxygen incorporated inside the crystal is only about 1% of the oxygen dissolved in the melt, according to Müller [5]. The rest of the oxygen from the melt will be evaporated to the furnace environment not being able to be incorporated in the crystal. Figure 6 illustrates the transport of oxygen inside the Czochralski furnace.

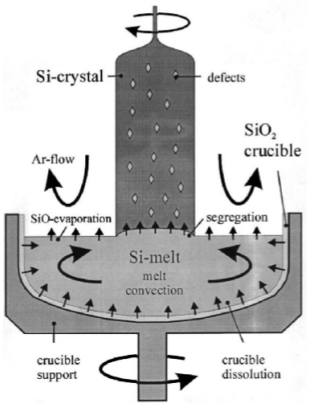

Figure 6: A schematic illustration of oxygen transport during the Czochralski crystal growth, from [5].

It has been found that the oxygen content inside the crystal is not only strongly related to the amount of oxygen inside the melt, but also to the melt area covered by the growing crystal. It has been proven by Lin and Benson and the relationship between the crystal diameter and the oxygen content inside the crystal is presented in Figure 7. The tendency is the most visible in the first stage of diameter growth as the oxygen concentration increases quite dramatically. Later, after the diameter reaches over 200 mm the oxygen content becomes more constant [6]. This has been connected to the evaporation of oxygen from the melt; when the diameter is relatively small (< 125 mm), the melt area is large so that a great amount of oxygen is evaporated and when the crystal diameter is covering a larger melt area, the evaporation from the melt is quite constant and more oxygen is incorporated inside the ingot.

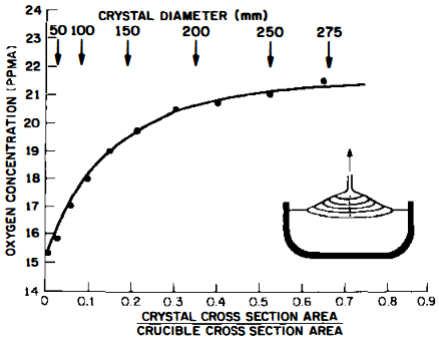

Figure 7: Variation in oxygen concentration as a function of crucible diameter covered by the growing crystal, from [6].

The oxygen incorporation inside the growing crystal is also affected by the heat distribution patterns illustrated in Figure 8. In the figure it is shown that the heaters surrounding the crucible are heating the melt inside the crucible by radiation (Q_H). The heat from the crystal (Q_C) and the melt (Q_M) is also transported in form of radiation. The latent heat (Q_L) from solidification is also indicated in the figure. Lin and Benson describe that the thermal convection inside the melt is the way the oxygen is transported inside the melt and eventually reaches the solid/liquid interface. In addition, the rotation of crucible is generating a flow pattern similar to the thermal convection pattern and can be then used as a way of control of oxygen enhancement (due to faster rotation) or oxygen retardation (slower rotation) inside the crystal [1, 5, 6].

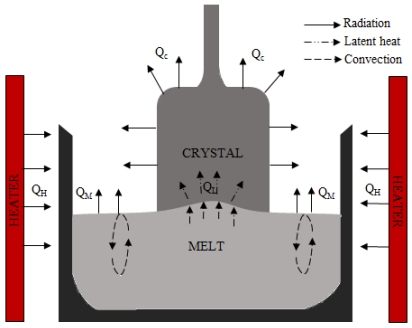

Figure 8: Schematic illustration of the heat balance during the Czochralski process, modified from [7]. Q_C stands for heat from crystal, Q_M stands for heat from melt, Q_H stands for heat from heater, Q_L stands for latent heat, from [1].

4 Defects and Impurities

As it was briefly mentioned in Chapter 2.1 defects and impurities, either added intentionally or unintentionally, will affect the band structure of the material and as a result also the material's properties. In the case of monocrystalline silicon, it has also been previously mentioned that oxygen is the most common unintentional impurity. That is why in this chapter first the general theory on defect classification and formation will be presented, which later will be followed by a section on the role of oxygen.

4.1 Defect classification

One of the most recognized classification methods for defects in monocrystalline silicon is to categorize them by their dimensions and shapes. Figure 9 presents an illustration of the different defect types that can be found in a Czochralski grown silicon crystal.

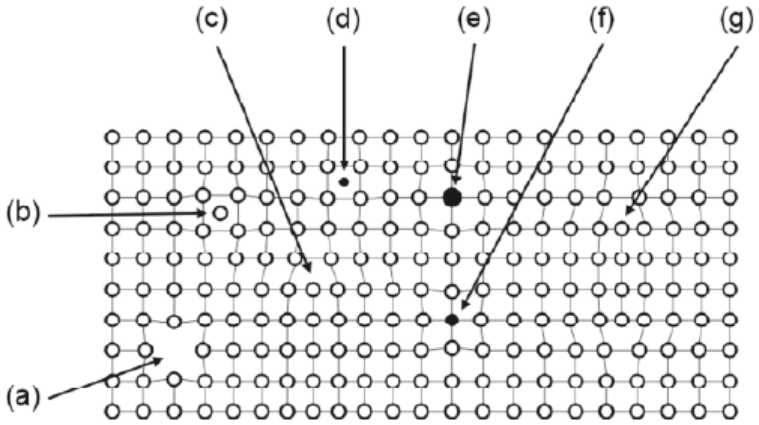

Figure 9: Schematic illustration of the different defects in silicon lattice: (a) Vacancy, (b) self-interstitial atom, (c) edge dislocation, (d) interstitial impurity atom, (e) substitutional impurity atom of larger atomic radius, (f) substitutional impurity atom of smaller atomic radius, (g) extrinsic stacking fault, from [8].

The first group of defects are 0D-defects or point defects. Vacancies, self-intersistials, interstitial impurities and substitutional impurities are all part of this group of defects. While self-intersitials (an extra Si-atom in the lattice) and vacancies (lack of an Si-atom in the lattice) are often referred to as intrinsic point defects, interstitial and substitutional impurities are referred to as extrinsic point defects. The extrinsic point defects can be for instance intentionally added dopants, such as boron or galium. Another possibility are unintentionally impurities, such as oxygen and carbon [7, 8].

The next group are 1D-defects (line defects), such as dislocation loops, edge and screw dislocations. Those are mostly incorporated during the wafer manufacturing process, hence they will not be covered any further in this paper. It is possible that these kind of defects form also during the growth process. Such ingots are however, melted as they will not be single crystals due to the dislocations.

2D-defects, called also planar defects are in the case of silicon primarily extrinsic stacking faults formed by excess atomic planes. They will be presented in greater detail in Chapter 4.3 since their presence and formation mechanism is strongly related to the presence of oxygen.

The last group of defects in Czochralski silicon crystals are 3D-defects or bulk defects which are agglomerates of point defects or precipitates of foreign particles. When talking about agglomerates of point defects, it is important to make a distinction between voids (agglomerates of vacancies) and swirls (agglomerates of interstitial point defects) due to differences in their origin. The most important example of precipitates of foreign elements are thermal donors which will be covered in the literature review Chapter 5.

4.2 Defect formation

This section is devoted to describe the most recognized theory on defect formation proposed by Voronkov in 1982 [23].

To understand this theory it is crucial to introduce the two most important parameters that it is based on: V, being the growth rate and G, being the temperature gradient. The ratio between those two, V/G-ratio, was used by Voronkov to distinguish between two different crystal growth modes: vacancy and interstitial mode. It means that the grown crystal would, according to Voronkov, have a predominance of either vacancy point defects or interstitial point defects. In general if the V/G-ratio is above a certain critical value, there will be a predominance of vacancies, while for V/G-ratio below the critical value, there will be a predominance of interstitials in the structure [23]. The critical value of the V/G-ratio is about 0.2 mm^2/min K, although it can also be somewhat lower [24]. Modern produced Czochralski silicon ingots contain usually a mixture of both intersitial and vacancy type microdefects. Due to radial variation in G, the central region would be rich in vacancies due to higher V/G-ratio, while the peripheral region would be rich in interstitials due to lower V/G-ratio [24]. Ingots produced for solar cell application would usually contain more vacancies than interstitials.

Voronkov presents several stages of microdefects formation, starting with recombination and diffusion of interstitials near the crystallization front. The next stage is interstitial annealing at the crystal surface in which the microdefect formation can be stopped at low enough growth rate values because the

insterstitials will be annealed completely. Further, there is the nucleation of primary clusters in a narrow temperature interval depending on V,G and R (the crystal radius). The next step in the process is the growth of the primary clusters which is also referred to as consumption of interstitials. Further, the growing clusters can grow large enough to form dislocation loops or incoherent particles of dense silicon phase [23]. The vacancy type defects would form to larger voids, stacking faults and dislocation loops [9].

The different microdefect-bands are illustrated in Figure 10, where it can be seen that increasing growth rate leads to a change from intersitial type (A/B-defects) to vacancy type (D-defects) defects which are separated by a defect free gap and two defect gaps: P-band (particle band) and B-band (containing swirl defects) [9, 25]. The P-band will be further described in Chapter 4.3.

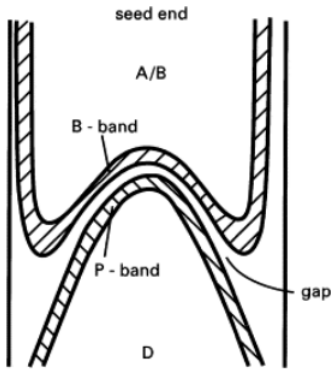

Figure 10: Illustration of grown-in defect sequence at gradually increasing growth rate, from [9].

According to this theory, pulling at higher pulling speeds would increase the V/G-ratio, making the crystal more rich in vacancies. However, a complete study of thermal history of the ingot would be needed in addition to the pulling speed in order to understand what type of microdefects can be included in the crystal [23, 24, 26].

4.3 Role of oxygen

In general, the oxygen has three important roles in monocrystalline silicon ingots and those are: thermal donors formation, precipitate formation and intrinsic gettering; and mechanical strength of the crystal [7]. As previously mentioned oxygen is the most common unintentionally added impurity in Czochralski pulled silicon ingots and its presence can be detrimental for the material's properties. Its importance was also described in Chapter 4.1 in the case of defect classification. This section aims to closer describe the role of oxygen in defect

formation which will give a base for the understanding of Chapter 5 in which a literature review on thermal donors will be provided.

First, the P-band formation presented in Figure 10 will be described. It is located at the periphery between A/B- and D-defects; interstitial and vacancy defects. The vacancies will form agglomerates with oxygen, forming oxide particles of density 10^8 cm^{-3} [25, 27]. The particles will consume a large number of vacancies, hence the residual vacancy density in the P-band will be relatively low. The particles formed in this band would survive heat treatments at temperatures as high as 1200 °C. The P-band is the source of OISF-ring described further below in this section [25, 27].

Oxygen content is strongly related to the presence of stacking faults. Often the stacking faults can originate from the presence of oxygen in the substrate, as the oxide precipitates tend to be a preferable nucleation site for this type of defects because of the stress field around the oxygen precipitates. They will not form around oxygen in the interstitial position. Particularly one type of stacking faults is important to relate to the presence of oxygen and this is oxidation induced stacking fault (OSF or OISF) which often originate during device fabrication and are usually absent in as grown silicon. The growth of stacking faults is a function of annealing time and temperature. It is interesting to mention that it has been shown that the density and distribution of SF can be linked to the rotation rate of the crystal, as seen in Figure 11. It is shown that increasing the crystal rotation rate results in lower SF density, especially when the increase is significantly large, hence it has been deduced that the change in distribution of SF must be related to the interface change produced by changes in rotation [7].

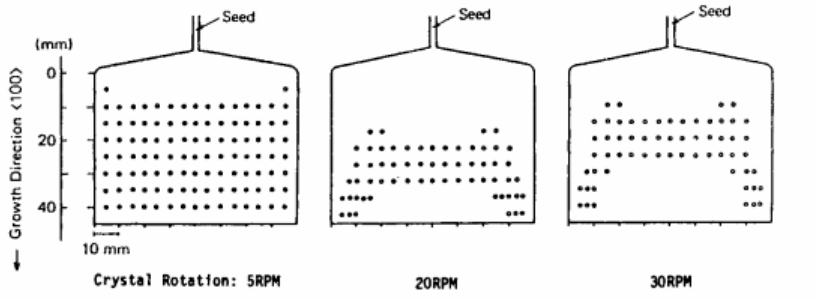

Figure 11: The effect of increasing crystal location on the distribution of OSF, from [7]

An interesting fault worth mentioning in relation to oxygen precipitates, is formation of an OISF ring. It is formed due to rapid oxidation of the crystal surface results in injection of silicon interstitials below the oxidized surface.

They can further grow into stacking faults on oxide precipitates in the peripheral region. This results in a possible formation of a OISF ring; stacking faults are formed between the vacancy-interstitial boundary, the P-band[8]. Figure 12 shows an illustration of an OISF ring in the crystal and an actual photograph using an optical microscope [8].

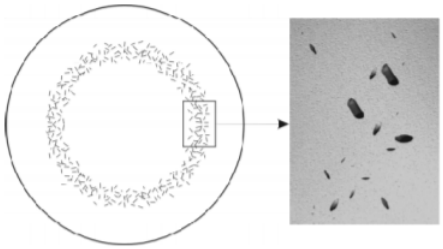

Figure 12: OISF ring: illustrated and under the optical microscope, from [8].

5 Literature Review

This section will present some of the most important literature on the following topics: thermal donor formation and their influence on the material's properties; the DLTS measurements on silicon; the AFM imaging of silicon samples. The chapter will be concluded with a section summarizing the most important findings of the review.

5.1 Thermal Donors

This section is meant to give a broader understanding into the concept of thermal donors. It will be divided into two subsections, the first one introducing the general theory on TDs, and the other will be presenting the most interesting literature about the topic.

5.1.1 General Theory

Thermal donors are one of the most important oxygen related defects in Czochralski silicon, influencing the material's electrical properties, such as lifetime or resistivity. This behaviour is related to their influence on the free carrier concentration which can be either increased or decreased, depending on the form of doping [28]. In the case of the material investigated in this project, the formation of TDs would lead to an increase in the free carrier concentration, as the material is n-doped.

The concentration of TDs has been linked to the interstitial oxygen content and the thermal history of the ingot. They are initially formed during cooling of the ingot after pulling end their formation is strongly related to the interstitial oxygen content and time spent at critical formation temperature [28, 29]. It is common to distinguish between two types of thermal donors: old thermal donors (OTDs) and new thermal donors (NTDs). They are formed in different temperature ranges: 350-500 °C for the case of OTDs and 600-900 °C for NTDs. The maximum generation rate of OTDs occurs at 450 °C and for NTDs it is at 800 °C. A certain procedure of heat treating could be used to perform a process called donor killing, in which the amount of TDs is reduced significantly. Donor killing of OTDs occurs at temperatures above 600 °C, while for NTDs the temperature must be higher as 1100 °C [30, 31, 32, 33].

The presence of OTDs in silicon would introduce two new energy levels in the band gap located at 75 meV and 150 meV below the conduction band [34]. As it was mentioned above, TDs would display a donor like behaviour in the material and as it can be seen, OTDs can behave as double donors, depending on the electrons concentration. If the electron concentration is lower than $5 \cdot 10^{15}$ cm^{-3}, the OTDs would display a double donor behaviour and the carrier concentration would be effected as follows:

$$n = N_D^+ + 2 \cdot [TD^{2+}], \tag{1}$$

where n is the carrier concentration, N_D^+ is the donor free carrier concentration and $[TD^{2+}]$ is the concentration of double ionized TDs [1, 35].
If the electron concentration is higher than $5 \cdot 10^{15}$ cm^{-3}, the OTDs would display a single donor behaviour and the carrier concentration would be effected following this formula:

$$n = N_D^+ + 2 \cdot [TD^{2+}] + [TD^+], \tag{2}$$

where $[TD^+]$ is the concentration of single ionized TDs [35]. The material properties are hence affected by the presence of TDs as the total carrier concentration changes.

As it was mentioned above the formation of thermal donors was linked to the concentration of interstitial oxygen and it is commonly accepted that TDs are electrically active oxygen agglomerates. It was suggested by Kaiser et al. that TDs are oxygen clusters formed out of four oxygen atoms as they found a fourth power dependence to the interstitial oxygen concentration [36, 37]. Some of the literature presented in the next section is dealing with the topic of formation of TDs.

5.1.2 Literature review on TDs

In this subsection papers touching on the presence of thermal donors in silicon will be presented. Some of them include studies performed by the use of DLTS which could also be presented in Chapter 5.2. They were however, chosen to be presented here because of the relation to the topic of thermal donors.

The first paper presented here deals with the TDs in silicon investigated by DLTS and the Hall effect [38]. In the study boron-doped Czochralski silicon wafers were annealed for 20 hours at 450 °C in Ar atmosphere to grow the thermal donors. After annealing, the doping type was changed into n-type due to an increase in donor concentration due to the presence of TDs, and those samples were studied by the Hall effect. The diodes for DLTS were prepared from a phosphorus doped Czochralski silicon, annealed in the same way as the boron-doped in order to grow thermal donors. The diodes were made by applying a gold layer for the Schottky contact and InGa-alloy for the Ohmic, similarly to the diodes prepared in this thesis. One of the important results of this study showed that prolonged annealing decreases the thermal donor energy. Further, the DLTS-measurements found the two thermal donor energy levels mentioned in Chapter 5.1.1. A correlation between the Hall energies and DLTS-energy level was found and it was found that the two main Hall-levels could not be found in DLTS and one the DLTS-level at 120 meV was not easily detected in

the Hall measurements. This gives the idea that investigating thermal donors requires the use of several techniques [38].

Further, Pensl et al. investigated the NDs and oxygen related precipitates in Czochralski silicon by DLTS and TEM [39]. The wafers used in this study had different interstitial oxygen concentration and were annealed in different ways in order to promote NTDs formation. The TEM studies revealed different types of defects inside the material, depending on the initial oxygen content and the annealing process. The observed defects included: 100 platelets formed from amourphous SiO_x oxide (growing at temperatures from 600 to 900 °C), long ribbon like defects (agglomerations of silicon interstitials), interstitial dislocation loops and extrinsic stacking faults. It was found that the interstitial oxygen concentration decreases with increasing precipitate concentration and at higher temperatures the oxygen related platelets and other defects can be dissolved at temperatures above 1100 °C, increasing the O_i concentration again. In addition, it was found that generation of NDs decreases the concentration of O_i. Further, concentration of NDs and their energy levels were studied, leading to the conclusion that the ND traps are cause by oxygen related precipitates. The most important conclusion of this work is perhaps that a correlation between annealing time, the oxygen concentration, the NDs concentration and observed defects was found [39].

The study of McQuaid et al. focuses on the oxygen loss during old thermal donors formation in CZ-silicon in the temperature range between 350 °C and 500 °C [40]. The samples measured here were subjected to different annealing processes and the interstitial oxygen content was determined. The measured loss in O_i concentration and TD formation led to important conclusions about the mechanisms of oxygen diffusion. First, the dimerization of O_i-O_i was shown to be the rate limiting step in the loss of oxygen from solution at temperatures below 500 °C. For annealing processes at temperatures above 400 °C, it was found that that the rate of O_i loss is reduced, while the order of O_i loss is increased, meaning that more oxygen interstitials are lost despite the reduction in the rate of loss. Prelonged annealing time was found to not be co-related with the O_i loss which was explained by the rate of dimers dissociation which was not increased during anneals. It was found that the O_i loss varies as the formation and dissociation of the dimers vary. The highest rate of dependence of the change in interstitial oxygen concentration on the intersitial oxygen concentration was found in high anneal temperatures (around 500 °C) and it was explained by dimer clustering resulting in the formation and growth of large clusters. The TDs formation should be associated with different size of oxygen clusters [40].

Next, a paper touching on the subject of the role of hydrogen in thermal donors formation in Czochralski silicon studied by Huang et al., will be presented [41]. The material used in this work was boron doped Czochralski silicon wafers with relatively high oxygen content. The wafers were pre-annealed for

10 min in 700 °C to kill the residual thermal double donors (TDDs). They were further plasma-hydrogenated after HF-etching to remove the native oxide layer. Then, they were annealed between 350 and 450 °C at different times. It was found that in all the samples the TDD formation was enhanced due to the presence of hydrogen and the lower boundary for the enhancement of oxygen diffusion was deduced for the temperature ranges of 200-500 °C and 700-1200 °C. The lower boundary of hydrogen concentration for the enhancement of TDD formation was also found for the temperature range of 300-500 °C. It was also suggested that the TDD formation was enhanced due to the hydrogen enhancing the diffusion of oxygen atoms, rather than the enhancement of oxygen dimers [41].

The formation of thermal donors via isothermal annealing was studied by Bruzzi et al. and it is the next paper presented in this section [34]. In this study the samples originated from a p-type magnetic CZ-silicon crystal and were made into diodes for characterization by DLTS. The samples were then subjected to isothermal annealing from 45 to 120 mins in 430 °C. The characterization of the diodes revealed two energy levels coming from the TD-centers at 70 $\pm$ 5 meV and 170 $\pm$ 5 meV. The results of this work showed that the activation of thermal donors is responsible for the compensation of the B-doping during annealing and at the longest annealing overcompensation occurred and the sign of space charge was changed due to the ionization of TDDs [34].

Miyamura et al. studied the relationship between TDs and lifetime of the CZ-silicon wafers [42]. The crystals for this experiment were produced in the laboratory and phosphorus doped to form n-type doping. One of the crystals was removed directly from the furnace after pulling, while the other was left to cool down in the furnace for 4 h. The difference in the thermal history naturally resulted in different thermal donor concentration. It is important to mention than in this work the TDs will assumed to act as single donors. Both resistivity, O_i content, metallic impurities content and lifetime were measured. By investigating the donor concentration in both crystals and their lifetime, the study concluded that thermal donors act as defects and not as recombination centers in the range below 10^{13} cm^{-3}, so it was concluded that they do not affect the lifetime greatly [42].

The next paper presented in this section by Olsen et al. was an investigation of spectral and radial characteristics of thermal donors in n-type Czochralski silicon [43]. Two CZ-silicon ingots were studied. The samples had different interstitial oxygen concentration and came from two different regions: tail and seed. The samples were annealed in nitrogen atmosphere after etching in HF for 24, 66 and 99 hours at 450 °C which is the temperature for the largest growth rate of OTDs. Other samples were also annealed at 650 °C after a preannealing at 450 °C. They were later studied by hyperspectral photoluminescence imaging. It was found that the seed samples contained TDs after manufacture distributed in a ring like pattern, which was not the case for the tail samples. Further, it

was shown that annealing at 450 °C made the emission related to band to band recombination stronger. This was further reduced by annealing at 650 °C. Overall, the results were found to support the main formation mechanisms of TDs [43].

The final paper presented in this section is the study by Jiyang et al. on the effect of the presence of TDs on the performance of heterojunction solar cells [44]. Phosphorus doped CZ-wafers with different position origin and O_i concentration were characterized. Some of the wafers were subjected to annealing at 450 °C for varying time up to 50 hours in order to grow the TDs. The resistivity was measured by FPP before and after heat treatment. Further annealing at 650 °C allowed to find the initial TD concentration from the resistivity measurements. FTIR, DLTS and the Hall effect were used to further characterization of the samples and the nature of TDs. Further, the solar cells for investigation were fabricated in a standard process. The investigations showed that TDs have negative influence on the heterojunction solar cell performance. It has been linked to a decrease of minority carrier lifetime. The energy levels of TDs were found by DLTS. They were found to have a significant effect on reduction of fill factor and open circuit voltage, two important parameters for good performance of a solar cell [44].

5.2 DLTS

This section will introduce some of the relevant papers that have investigated the deep level defects in silicon by the use of the DLTS-technique.

The first paper presented in this section will be on the effect of oxygen related defects in n-type Czochralski silicon on the lifetime of minority carriers, a study by Kolevatov et al. performed using various techniques, including DLTS [45]. The paper is investigating samples coming from an n-type CZ-crystal grown in vacancy mode with possibly degrading regions, and comparing them to samples coming from an ingot that should not have the same degrading regions. They were annealed to simulate a cell fabrication. The samples were later fabricated into diodes with gold evaporated on top, and used for the DLTS characterization. The DLTS measurements of the reference crystal and the crystal grown in vacancy mode revealed that both contain four trap levels, the most intense one originating from the presence of TDs. The two others were linked to nuclei of oxygen precipitates, while the last remain of unknown origin. It was concluded that strained plate-like oxygen precipitates are the reason for lower recombination activity in the degrading areas, affecting the lifetime of the minority carriers [45].

Process induced deep level defects and their influence on material's performance were studied in DLTS by Astrova et al. [46]. Both p-doped and n-doped float zone (FZ) produced monocrystals were characterized in this study. The

samples used for DLTS-measurements underwent heat treatment experiments and were made into diodes (ohmic contact was done by chemical Ni deposition annealing, while Schottky for n-type samples was made by gold evaporation and for p-type samples Sb was used). The obtained DLTS-spectra for n-type samples revealed peaks originating from the donor energy levels. For both of the types of the samples electron and hole traps were revealed by DLTS. Overall, it was found that the process induced defects are found in all the samples, and the biggest defect concentration was that of donor type defects. The defects were found to cause a resistivity drop of n-type silicon and conductivity inversion in p-type silicon. Ionization of the deep level traps found by DLTS, lead to decrease in breakdown voltage [46].

Evans-Freeman et al. studied extended defects in CZ-silicon by DLTS and high resolution Laplace DLTS (LDLTS) [47]. They used p-type CZ-silicon wafers and intentionally introduced defects into the structure by Vickers diamond tip and four point bend at 550 °C. The origin of the wafers was not specified, so it is unknown if they were produced from a region close to body or crown. The samples were later annealed at 500 °C for different times and later made into diodes by Ti and Al evaporation on top. The oxygen atoms concentration per unit length of the dislocation or unannealed samples was found to be in the order of 10^6 cm^{-1}. For the shorter annealing time it was found to be 10^7 cm^{-1} and for the longer anneal time it was $2 \cdot 10^7$ cm^{-1}. Investigation by DLTS revealed differences in the spectra between the annealed and unannealed samples and it was concluded that the lack of annealing means that the dislocations are not immobilized by oxygen. It was concluded that some the peaks in this work were not related to the formation of TDDs as the temperature was possibly too high and the annealing time was too short. Further, by studying both DLTS and LDLTS, deep level defects related to the presence of oxygen were found and that some emissions are related to deep states with neighbouring dislocations when those are not oxygen locked [47].

The next paper covers the topic of micro- and nanostructures in CZ-silicon studied by both DLTS and AFM [48]. Here, the results of DLTS-measurements will be presented. In this study several types of silicon samples were investigated: as-grown boron-doped CZ-silicon samples; oxygen-precipitated silicon; plastically deformed CZ-Si with dislocations and deformation induced clusters; plastically deformed CZ-Si with straight, 60 °dislocations, oxygen- segregated 60 °dislocations; plastically induced deformed float zone Si with dislocations. The samples were subjected to different heat treating procedures. Four deep levels were found in the samples from the oxygen-precipitated silicon, float zone samples and CZ-si with dislocation and deformation induced point defect clusters. Further, three deep traps and two shallow traps were found in the other type of CZ-silicon. The authors linked the presence of the defects to the presence of Fe in the material since some of the traps were detected in all of the samples, independent on the treatment. Two oxygen defects were found: one related to impurities in the strain field of defects, the other related to defects at interfaces

between the silicon and the oxide. The main trap level surviving all types of annealing was related to the presence of dislocations. Point defects formed during deformation produced several trap levels, while dislocations would introduce also shallow traps after annealing procedure due to oxygen segregation (in addition to the deep traps) [48].

The study by Capan et al. focused on the vacancy-related defects in Czochralski silicon after implantation of heavy accelerated ions in the MeV range [49]. n-doped Czochralski silicon wafers were used for diodes fabrication by gold evaporation on top and Al- evaporation on the back. The finished diodes were then implanted with different ions, O, Si and Ge. The samples were then characterized by DLTS and it was found that heavy implantation leads to formation of a dominant electron trap which was related to a single acceptor state of divacancy.The observed broadening of the DLTS peaks was explained by the perturbation of vacancy due to local defects. The observed suppression of DLTS signal in low doping samples was explained with two possible mechanisms: depletion of carrier concentration in the disordered regions and the effect of ion implantation [49].

The last paper presented in this section talks about the study of OTDs in plasma-hydrogenated CZ-silicon [50]. Phosphorus doped magnetic CZ-silicon samples were hydrogenated by exposure to hydrogen plasma at 270 °C for 2 hours and later annealed at temperatures between 275 °C and 450 °C to form OTDs. Here, the use of word magnetic is used to describe the production process, being done in magnetic field. It is important to specify that silicon itself is not magnetic. The diodes for DLTS analysis were done by applying an Ohmic contact in the back and evaporation of Au on the front for the Schottky contact. In total 9 kinds of deep levels were measured by the DLTS and analyzed. Two out of the nine were found to arise from the OTD formation, and two others were found to originate from C-O-H complexes. It has been found that the OTD formation in magnetic CZ-silicon is not as strongly catalyzed by the presence of hydrogen, as it is in the case of p-type CZ-silicon [50].

5.3 AFM

The AFM-technique is a powerful characterization tool, and this section will present some interesting literature to introduce some of the possibilities of this technique. The samples in this project were meant to be studied for their surface morphology and electric properties by obtaining current maps in the conductive mode. Hence, the papers presented here will be touching upon the subject of AFM-characterization in the conductive mode both in CZ-silicon and other types of materials for which results can be relevant.

First, the study of Nishikawa et al. which investigated the formation of grown-in defects in CZ-silicon [51]. For the experimental procedure two CZ-

crystals produced with the same pulling speed were subjected to two different thermal histories; one of the crystals was quenched by removing it from the furnace directly, while the other was left to cool down in the furnace for 5h and was then quenched by removal from the furnace. The quenching process was performed in order to "freeze" the grown-in defects which were investigated using several techniques. AFM was used to study the crystal originated particles (COPs) which are large vacancy agglomerates. Some differences between the COPs pits for the two crystal were observed, both by the means of size and shape that were linked to the presence of oxygen in only one of the crystals (measured by EDS). It was the crystal that was held inside the furnace which showed a contrast at the edge of the COP which has been eliminated after HF dipping. Oxygen was only detected in the same sample, showing that the contrast was due to the SiO_2 film building up on the COP edge. Another type of COP, a hillock, was observed in the crystal held inside the furnace. It was observed after 10 times of standard cleaning process and after repeating the cleaning process two more times, the COP changed into an ordinary pit which is observed also in conventional crystals. It was therefore concluded that the COPs inside the bulk of this crystal should be voids surrounded with a thick SiO_2 film [51].

The next study presented in this section is from Umeno et al. investigating the dependence of grown-in defect behaviour on oxygen concentration in CZ-silicon [52]. In the study eight wafers with different interstitial oxygen and thermal histories were prepared and used for characterization by various techniques, one of them being AFM. One of the results of this work drawn by the AFM-image analysis, is that decreasing oxygen content increases the concentration of COPs and that oxygen is one of the determining factors of the void defects structure. Further, it was found that cooling rate was possibly not the most important factor to determine the void structure, however slower cooling rates could result in larger COPs. It was also observed that higher oxygen content would result in more not-singular COPs. AFM-imaging in as-grown, annealed in nitrogen and annealed in oxygen wafers with high oxygen content showed that the oxide film is growing on the COP edges in the N_2 atmosphere, while in the O_2 atmosphere the voids are filled. Investigating low oxygen contet wafers after annealing in nitrogen atmosphere showed that the oxide film was not grown on the COP edges and no COPs were observed after annealing in oxygen atmosphere. It was therefore concluded that in the case of high oxygen content and annealing in oxygen atmosphere the oxide growth is enhanced by the injection of interstitial silicon atoms. In the case of low oxygen content void shrinkage will occur due to incorporation of interstitial silicon atoms [52].

Düngen et al. studied the hydrogen-related defects in Czochralski silicon by, among others, AFM-imaging of the surface morphology [53]. Although this study is not particularly directly related to the main topic of this thesis, it is a great example of what AFM can be used for when investigating CZ-silicon. In this study p-type CZ-silicon wafers were implanted with H^+-ions and annealed

at various temperatures. The differently annealed samples were then studied under atomic force microscope which revealed bulges due to blistering of newly formed microactivities on the surface. Further, also the size and shape of the blisters was observed and measured in the AFM and it was found that increasing annealing temperature resulted in fewer, but larger blisters. The obtained AFM-images could be used to a conclusion that the blister formations' precursor is the hydrogen terminated divacancy [53].

An example of the use of c-AFM technique for investigation of electrical properties is the study by Miwa et al. investigating dark current characteristics of amorphous silicon layer deposited on pyramidal-textured crystalline silicon substrate [54]. The samples were studied in order to obtain current maps and surface morphology images at the same time. A correlation between the obtained morphology images and current maps has been found for the samples that were deposited on the textured surface, contrary to the samples which were deposited on flat surface. Hence, c-AFM allowed a thorough investigation of the relationship between surface morphology and the electrical properties [54].

Gianazzo et al. studying stacking faults in cubic silicon carbide is another example of the use of c-AFM technique for investigation of defects [55]. In this paper cubic silicon carbide films deposited by chemical vapor deposition on silicon substrate were investigated for both their morphology and electrical properties, such as current maps and local IV-curves, which is one of the features of c-AFM. The defects were investigated in both forward and reverse bias conditions. Stacking faults were clearly observed in the current maps which in combination with obtained IV-curves and calculations, was used to explain the electronic transport in the material. It was concluded that the SFs are preferential current paths which are linked to reduced voltage under the forward bias conditions in this material. It is a clear example of how c-AFM can be used to obtain important information and finding a correlation between samples morphology and its electrical properties [55].

The last paper presented in this Chapter is investigation of stacking faults in $Mo_xW_{1-x}Se_2$ by c-AFM [56]. The material in this study was synthetic $Mo_xW_{1-x}Se_2$ obtained from high quality graphene where x was 0.3 and 0.7. Running an AFM experiment in the conductive mode allowed to gather data about the sample morphology and current maps simultaneously, which revealed the difference in conductance of the different surface features, such as wedges.The paper concludes that stacking faults and step edges have a great influence on the surface conductivity, and the conductivity in general is dominated by the morphological features. In addition, also information about phase segregation were obtained. This paper presents a great amount of high quality c-AFM current maps, showing the powerful possibilities of using this instrument [56].

5.4 Summary

This literature review presented some of the relevant literature on the topic of thermal donors, oxygen and related to it defects in silicon. It is clear that it is a widely studied topic and the selected papers are only a fraction of the existing literature. The findings of this review will be summarized in this section.

For the case of TDs formation mechanisms, it was found that the initial oxygen concentration and size of precipitates are some of the crucial variables for the formation of TDs. The annealing time and temperature were also confirmed to play an important role in the formation of TDs. Further the relationship between the presence of TDs and the defects formed in the material was found. Another important aspect was the role of hydrogen in the TDs formation which was found to enhance the oxygen diffusion and hence also the TDs formation. The effect of TDs on the electrical properties, such as lifetime was found to be significant when the TDs concentration is above 10^{13} cm^{-3}.

The findings from papers presented in Chapter 5.2 will be summarized in the table form in Table 1.

The AFM-literature review presented some interesting papers about defects observed by this technique. It revealed some interesting findings about the different types of defects forming due to different annealing or oxygen concentration. It was revealed that the formation, behaviour, shape and size of crystal originated defects in CZ-silicon are varying with oxygen concentration and annealing procedure. The paper of Gianazzo et al. showed also the effect of stacking faults on the electrical properties using c-AFM, which was the reduction of voltage under forward bias conditions.

As the effect of pulling speed has not yet been widely investigated in relation to the TDs formation, the deep levels and the sample morphology, this thesis could be a great opportunity for this study. In addition, the obtained values for deep level traps obtained in this thesis could be compared to the ones found by other authors presented in Table 1. As this thesis could cover a broad spectrum of samples with different origins (varying annealing, oxygen content and pulling speed) it would be an interesting contribution to the existing literature.

Table 1: Summary of energy levels and their origin found by different authors.

Author	Energy level value	Origin
Bruzzi et al.	0.075 eV	OTD
	0.15 eV	OTD
Pensl et al.	0.019-0.06 eV	activation energy for NTDs
	0.03-0.12 eV	activation energy for NTDs
	0.55 eV	undetermined bulk trap
	0.35 eV	undetermined bulk trap
	0.13 eV	undetermined bulk trap
Kolevatov et al.	0.075 eV	TD
	0.33 eV	oxygen nuclei
	0.365 eV	oxygen nuclei
	unknown (low signal)	unknown
Astrova et al.	0.28 eV	single donor
	0.54 eV	double donor
	0.34 eV	electron trap
	0.33 eV	hole trap
	0.43 eV	hole trap
Evans-Freeman et al.	0.25 eV	oxygen (longer annealing time)
	0.28 eV	oxygen (shorter annealing time)
Cavalcoli et al.	0.27-0.28 eV	dislocation or O-precipitates
	0.42-0.45 eV	Si/SiO_2 interface
	0.40 ev	iron contamination
	0.38 eV	deep hole trap
Capan et al.	0.18 eV	vacancy
	0.4 eV	divacancy
	0.38 eV	divacancy after O-implantation
	0.39 eV	divacancy after Si-implantation
	0.40 eV	divacancy after Ge-implantation
	0.41 eV	divacansy after Er-implantation
Huang et al.	0.07 eV	OTDs
	unspecified	undetermined
	0.14 eV	C-O-H complexes
	0.15 eV	C-O-H complexes
	0.16 eV	undetermined
	0.08 eV	undetermined
	0.52 eV	undetermined
	0.12 eV	OTDs
	0.42 eV	undetermined

6 Characterization Techniques

The samples in this project were characterized for their electrical properties using various techniques. The theory for each technique will be provided in the following sections. Since the samples for characterization were diodes, their characteristics in each technique will be highlighted.

6.1 Current-voltage measurements (IV-measurements)

The current-voltage measurements are performed in order to get information about the sample's electrical behaviour and asset the sample's performance, in this project's case: a diode device. The diodes in this project were done by evaporating a gold layer on top of the silicon sample and applying an InGa layer on the back of the sample, forming a p-n junction. This chapter will therefore focus on the IV-characteristics for this type of junction.

The relationship between current and voltage for a p-n junction is described by the Shockley equation:

$$I = I_0 \left[\exp\left(\frac{qV}{kT}\right) - 1 \right], \tag{3}$$

where I is the current, I_0 is the dark saturation current, q is the magnitude of the electron charge, V is the voltage, k is the Boltzmann constant and T is the temperature [57]. Figure 13 shows the ideal p-n junction diode behavior in both linear and semilogarithmic scale.

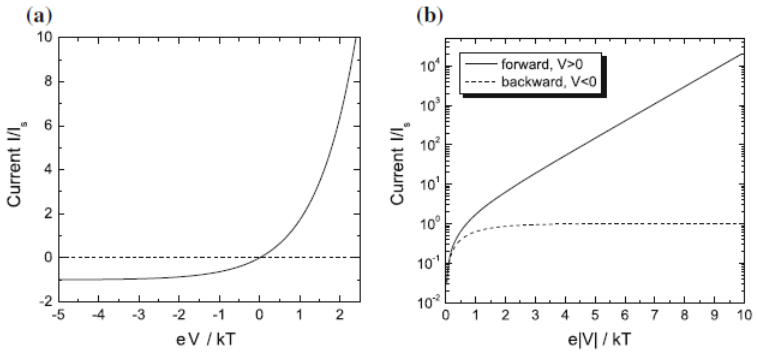

Figure 13: The ideal p-n junction diode IV-curves in: (a) linear scale, (b) semilogarithmic scale, from [10].

The main purpose of the IV-measurements performed in this project was to asset the diode characteristics of the samples by comparing the obtained IV-curves with the ideal p-n junction diode IV-curve presented in Figure 13(a). This was done using the Keithley SourceMeter 2400 by connecting the sample placed in the Faraday box by a BNC-connection. The experimental procedure

is further explained in Chapter 7.3.

6.2 Capacitance-voltage profiling (CV-profiling)

Capacitance-voltage measurements give information about the sample's electrical properties, such as the free carrier concentration and spatial distribution. In addition, it is also the base for further understanding of the DLTS-technique. The CV-measurements in this work were performed using an LCZ capacitance meter, thus the theory provided in this section will focus on how this type of measurement works.

An LCZ meter measures the capacitance by applying an oscillating potential to the device and measures the imaginary component of the complex impedance. From Ohm's law given in Equation 4 it can be seen how the impedance is correlated with current and voltage:

$$V = Z \cdot I = |Z| \exp(j\theta) \cdot I, \tag{4}$$

where V is the voltage, I is the current, $|Z|$ is the magnitude of impedance, θ is the phase angle between the current and voltage and j is the imaginary unit. The complex impedance is often given by the following formula:

$$Z(\omega) = Re(Z) + jIm(Z). \tag{5}$$

The imaginary part of the equation is calculated by measuring the current flowing through the sample, and the phase angle between the measured current and the voltage biased by the instrument [58, 59]. The capacitance is then calculated using this formula:

$$C = \frac{1}{2\pi f |Z|}, \tag{6}$$

where f is the frequency of the oscillating potential applied to the device. Further, Equation 7 can be used for approximating the free carrier concentration in a Schottky diode:

$$C = \sqrt{\frac{eN_d\epsilon_s}{2(V_{bi} - V - \beta^{-1})}} = \frac{\epsilon_s}{w}, \tag{7}$$

from which the depletion layer width, w, can be extracted since both capacitance C and the permittivity ϵ_s are known. The free carrier concentration is then calculated by the following equation:

$$N_d = -\frac{2}{e\epsilon_s}\left[\left(\frac{d}{dV}\right)\left(\frac{1}{C^2}\right)\right]^{-1}, \tag{8}$$

where e is the elemental charge, ϵ_s is the permittivity, $\frac{d}{dV}$ is the change in the bias potential and $\frac{1}{C^2}$ is the slope of the CV-curve.

Figure 14 shows an example of a CV-curve of a Schottky diode and the free carrier concentration profile. It is worth mentioning that it represents the case of homogeneous doping, hence the slope is perfectly linear. In the case of inhomogeneous doping, which is the case of the samples characterized in this project, the slope is not expected to be ideally linear [10, 58, 60].

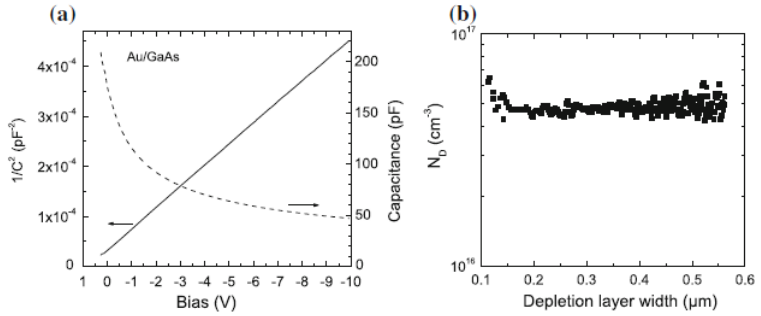

Figure 14: (a) In dashed line: CV-profile of a Schottky diode, In solid line: the slope of the CV-profile; (b) The free carrier concentration calculated using the equations and the slope, from [10].

In this project the LCZ-meter 3330 produced by Keithley was used to perform the CV-profiling at room temperature inside the Faraday box. A more detailed description of the experimental setup is provided in Chapter 7.4.

6.3 Deep Level Transient Spectroscopy (DLTS)

Deep Level Transient Spectroscopy is a characterization technique used to investigate deep level defects present in semiconductor materials. This section is dedicated to present the theory of this technique for further understanding of the experimental details presented in Chapter 7.5.

A DLTS measurements is based on the changes in capacitance upon applying a perturbation in form of a sudden change in voltage. This change in capacitance has two contributions, one of them being the change in the in minority carrier concentration (diffusion capacitance), while the other being the change in the depletion width (called junction capacitance). Under reverse bias conditions the junction capacitance will be dominant, while under forward bias conditions the dominant capacitance will be the one related to the minority carriers [11, 61].

For further consideration, a parameter E_T is given, being the energy of deep level state present in the material and the p-n junction is assumed to

be asymmetric, meaning that one side is more heavily doped than the other. In steady state, there is no net flow across the trap and the carrier densities are negligible within the depletion region. The following formula is then given describing the relationship between the density of deep states (N_T) and the density of filled traps (n_T):

$$e_p n_T = (e_n + e_p) N_T, \tag{9}$$

where e_p is the whole emission rate, n_T is the density of filled traps, $e_n$is the electron emission rate and N_T is the total density of deep states. Upon applying a perturbation, n_T will change leading to a change in the total charge in the depletion region which again leads to a change in capacitance which is only related to deep levels [11].

Figure 15 is a schematic illustration of capacitance transient generation due to perturbations. Point (1) represents the diode conditions under reverse bias in which the traps are empty since there is no free carriers available for capture [11]. Further, point (2) represents the majority carrier filling pulse condition at which the applied potential is changed. The depletion layer width is reduced, thus the capacitance increases dramatically. Here, the carriers are getting trapped in the deep levels and the change in the density of filled traps is given by the following formula:

$$\frac{dn_T}{dt} = c_n(N_T - n_T), \tag{10}$$

where c_n is the capture time constant of the carriers. The next point (3) represents the beginning of the transient upon the restoration of the reverse bias conditions after the pulse has been held for a time long enough to get an equilibrium between the density of filled traps and the density of deep levels, i.e. $n_T = N_T$, meaning that all deep levels are filled. The capacitance drops to a minimum value due to the carriers being trapped. Finally, point (4) shows the decay of transient due to thermal emission of the trapped carriers [11]. The n_T will vary with time following this equation (when $n = p = 0$):

$$\frac{dn_T}{dt} = e_p N_T - (e_n + e_p) n_T \tag{11}$$

to which the solution is as follows:

$$n_T(t) = \begin{cases} \left[\frac{e_p}{e_n+e_p} N_T + \frac{e_n}{e_p+e_n} N_T \exp\left(-(e_n+e_p)t\right)\right] & \text{for } t < 0 \\ N_T & \text{for } t > 0. \end{cases} \tag{12}$$

It can be observed that n_T will decrease exponentially with a time constant of:

$$\tau = \frac{1}{e_n + e_p}, \tag{13}$$

and that for an emitting center $e_n >> e_p$, equation 12 is reduced to:

$$n_T = N_T \exp(-e_n t). \tag{14}$$

The amplitude of the transient describing the filled level occupancy is thus related to the trap concentration, while the emission rate of electrons can be related to the time constant as:

$$\tau = \frac{1}{e_n}. \tag{15}$$

Combining these equations with equations describing the change in capacitance gives a possibility to relate the changes in capacitance to the deep states. The capacitance of a p-n junction can be described with the formula for a parallel plate capacitor:

$$C = \frac{\epsilon A}{W}, \tag{16}$$

where W is the depletion layer width and it is described by the following equation:

$$W^2 = \frac{2\epsilon(V_b - V)(N_D + N_A)}{qN_D N_A}, \tag{17}$$

where ϵ is the material's relative permittivity, V_b is the built-it voltage, V is the applied voltage, N_D and N_A are the donor and acceptor concentrations and q is the elemental charge. When the filled traps are included this expression becomes as follows:

$$W^2 = \frac{2\epsilon(V_b - V)}{qN_D^*}, \tag{18}$$

where $N_D^* = N_d - n_T$. If now $n_T << N_D$ the following expression can be obtained:

$$C = C_0\left(1 - \frac{n_T}{2N_D}\right), \tag{19}$$

where C_0 is the capacitance at revers bias. Taking into consideration the time variation of n_T the following equation is obtained:

$$C(t) = C_0\left[1 - \frac{N_T}{2N_D}\exp\left(-\frac{t}{\tau}\right)\right]. \tag{20}$$

Hence both the emission rates and trap concentrations can be estimated from the changes in the capacitance as a result of voltage changes [11, 61].

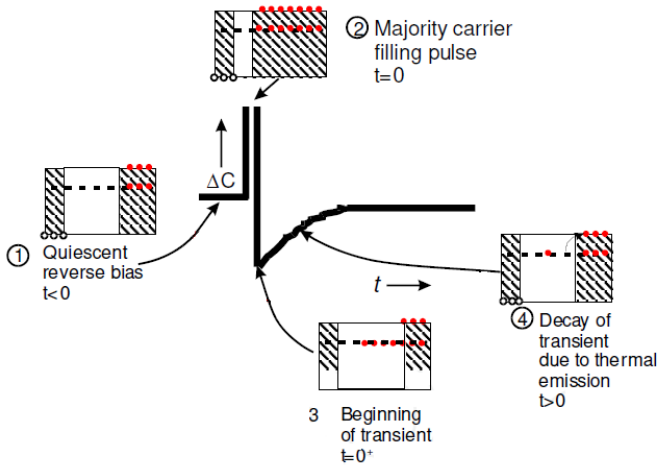

Figure 15: Schematic illustration of capacitance transient generation. (1) The p-n junction is being held in reverse bias conditions, no free carriers; (2) After a perturbation (change in the applied potential) the depletion layer is reduced, resulting in the sharp increase of capacitance and capture of carriers inside the traps; (3) The beginning of transient after the reverse bias conditions are restored, capacitance reaches a minimum value due to trapped carriers; (4) Decay of transient due to thermal emission of trapped carriers, modified from [11].

The formulas presented so far allow the estimation and analysis of one transient at a time for a given temperature, hence to obtain a wide range of emission rates, a more smooth approach is possible using DLTS. For this reason, the DLTS technique uses a parameter called rate window which allows getting an output from the aparatus only if a transient occurs with a rate within the window. Varying the sample temperature at a constant rate the emission rate of carriers from defects will vary and the when it appears in the given rate window, there will be a response from the instrument. In other words, the output peak will only be present if the transient has a time constant which is consistent with the rate window. The output will be proportional to the amplitude of the transient, thus it gives the possibility of exciting the device while varying the temperature over a large temperature range, obtaining information about the deep levels present and their concentration. Using different time/rate windows can be used to obtain thermal activation energies of the deep states [11].

Choosing the right rate window is done using a boxcar integrator which is illustrated in Figure 16 (b). The obtained transients obtained at various temperatures are fed into to boxcar with gates set to t_1 and t_2 at which the capacitance is measured and the difference between them is calculated ($C(t_1) - C(t_2) = \Delta C$). As ΔC goes through the maximum value, it is used to calculate the DLTS output S(T) as follows:

$$S(T) = \Delta C_0 \left[\exp\left(-\frac{t_1}{\tau} \right) - \exp\left(-\frac{t_2}{\tau} \right) \right], \tag{21}$$

where ΔC_0 is the capacitance change due to the pulse time at t=0. As S(T) is dependent on the time constant τ, it is possible to find the value of τ_{max} by differentiating S wrt t and setting the derivative to zero, which results in:

$$\tau_{max} = \frac{t_1 - t_2}{\ln \frac{t_1}{t_2}} = \frac{(x-1)t_1}{ln(x)}, \tag{22}$$

where $x = t_2/t_1$. It is then possible to achieve the value of S_{max} by substitution and it is:

$$S_{max} = \Delta C_0 \left[\exp\left(-\frac{\ln x}{x-1} \right) - \exp\left(-\frac{x \ln x}{x-1} \right) \right]. \tag{23}$$

What can be seen is that the maximum value of S is then dependent on the ratio between t_1 and t_2 rather than their actual values. It is also proportional to the capacitance, hence also N_T and thus tere is a correlatin between the DLTS peak height and the defect center concentration [11].

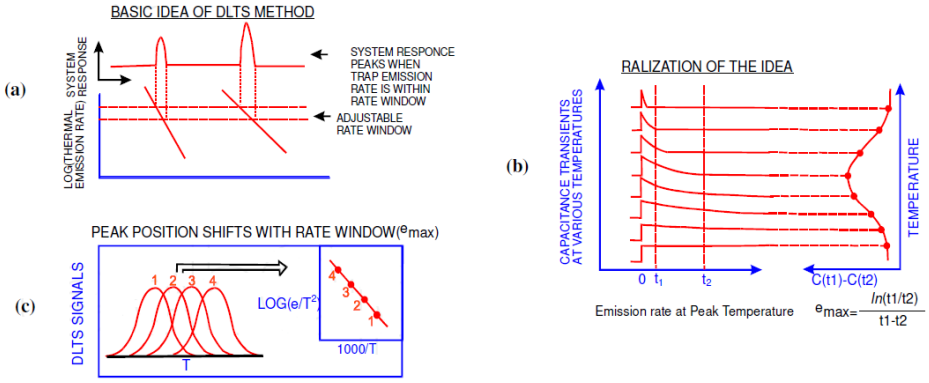

Figure 16: Illustration of the basic DLTS technique concepts: (a) the concept of rate window: response from the system when emission rate is within the rate window, (b) choosing of rate window (c) shifting of the peaks due to shift in rate window and temperature. The Arhenius plot is constructed to determine the energy of the state from the slope, modified from [11].

6.4 Atomic Force Microscopy (AFM)

Atomic Force Microscopy is a powerful characterization technique that allows investigation of both topography and other parameters, such as heat capacitance or conductivity, at the same time. This section will give a brief introduction into this technique and present the general concept of it, while the technique used in

this project, conductive Atomic Force Microscopy (c-AFM), will be presented in the next section.

The basic concept of the AFM-technique is presented in Figure 17. Unlike to other microscopy types, such as optical microscopy, here the topography is imaged by probing the real surface topography when the tip is in contact with the sample surface. The tip is mounted on a cantilever close to the sample surface and the sample area in the xy-plane. While the cantilever is moving, the difference in its height is recorded using a photodiode which senses the change in the intensity of the beam focused on the cantilever. The topography can then be imaged by quantifying the differences in the z-direction during the measurements. As the cantilever is being operated with a constant force and the deflection is measured, the interaction force between cantilever and the sample can be calculated by the following formula:

$$F = -k_c \cdot \delta_c, \tag{24}$$

where k_c is the spring constant of the cantilever and δ_c is the deflection on the cantilever. During a scan along the interaction force data is being collected and process by a software to produce a topography map of the sample [13, 62].

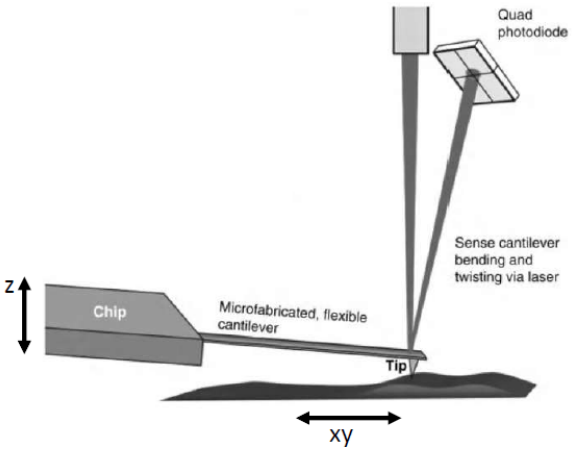

Figure 17: The basic concept of an AFM topography experiment: the tip mounted on a cantilever is moved around the sample in the xy-plane and the difference in height of the cantilever is sensed by the photodiode reading the beam deflection on the cantilever, allowing the software to map the topography; from [12].

To avoid collision between the tip and a possible "bump" on the sample surface, the system is equipped with a controller. In addition, the AFM-setup

should also be equipped with an anti-vibration system that protects the AFM-system from external influences [62].

6.4.1 Conductive Atomic Force Microscopy (c-AFM)

An AFM experiment performed in the conductive mode can give information about the sample's electrical properties that resulting from defects or doping [62]. Figure 18 shows a schematic overview over the most important system components used in a c-AFM experiment.

One of the crucial system elements in the conductive mode is the use of a conductive tip (in the case of this project: a platinum tip). The sample itself must also be conductive, a preamplifier is needed to convert the analog signal to the digital one sent to the computer and a voltage source is required to apply a potential difference between the sample and the tip [62].

When a potential difference between the sample and the tip is applied, it will generate an electrical field resulting in a current flowing between the two components and it is expressed by the following equation:

$$I = J \cdot A_{eff}, \tag{25}$$

where I is the total current flow at the nanojunction between the tip and the sample, J is the current density and A_{eff} is the effective emission area of the electrons, which is not the same as the actual contact area of the tip and the sample [62].

The analog current is sent to the preamplifier that transforms it into the digital signal and then it is read by the data acquisition card on the PC and the current map is then plotted by the software. The obtained current maps can reveal some local defects and/or doping inhomogeneities that are affecting the sample's electrical properties [13, 62].

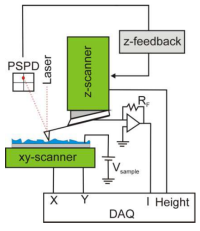

Figure 18: A schematic overview over the system components in a c-AFM experiment. A voltage source applies a potential difference between the sample and the conductive tip, the preamplifier transforms the data from analog to digital and the DAQ reads the data. The rest of the system works as in a conventional AFM experiment; from [12].

7 Experimental Details

In order to be able to characterize the samples by previously described techniques, several sample preparation steps were required, including cutting, grinding, polishing, etching, among others. The preparation steps will be described in this chapter, together with information about the samples' origin. Further, the experimental details on the experimental setup will be described.

7.1 Information about the samples

The samples characterized in this project were obtained from two monocrystalline silicon ingots provided by NorSun AS and have been previously described in the specialization project, [1]. The ingots were produced by Czochralski method with different pulling speeds and the difference in the average pulling speed was around 0.12 mm/min. The received parts of the ingots had the diameter of 17.78 cm and height of 25 cm. The ingots are P-phosphorous doped, hence they are n-type and the expected doping concentration, according to the producer, should be in the order of 10^{15}-10^{16} cm^{-3}. It is important to mention that from each ingot two vertical slices, obtained during previous project work, have been used in this work. The slices used here are the ones closest to the center and the following ones, 3.4 mm away from the center, as shown in Figure 19 [1].

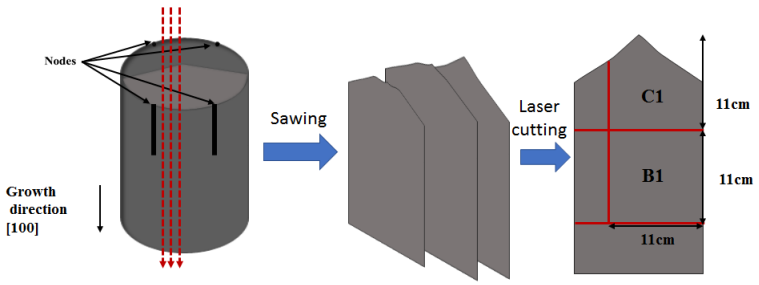

Figure 19: Schematic illustration of the sawing and cutting process. First (to the left), the cuts have been done between the nodes along the red dashed lines and three parallel vertical slices have been achieved (middle). Further each of the slices have been cut with a laser along the red lines (to the right) to achieve samples of 11 cm x 11 cm, from [1].

7.2 Sample preparation

The following sections will describe the sample preparation steps, including cutting, grinding, gold evaporation and making of electrical contacts.

7.2.1 Cutting

The samples that were characterized in the specialization project, [1], needed to be cut further to smaller pieces since the DLTS instrument requires the samples of size 1 cm x 0.5 cm. The initial sample size was 11 cm x 11 cm, therefore there was a need to choose the most interesting area for the DLTS measurements.

Considering the research made during the specialization project, the most interesting area for defect investigation seemed to be regions with high and low interstitial oxygen concentration before and after heat treatment. Since both of the two crown samples in the specialization project have been found to contain a region with bad electrical properties that corresponded well with the presence of oxygen, it was decided to cut samples from that region, i.e. 7 cm from the top of the crown. This has been done for the two heat treated samples and their parallels that have not been heat treated.

As for the samples containing low levels of oxygen, it has been found that the lowest oxygen content was at the bottom of the body-samples studied before. Therefore the samples for DLTS were located around 1 cm from the bottom edge of the sample, both for the heat treated samples and their untreated parallels.

For AFM-characterization there was a need to choose different samples as the ones used for DLTS. For this purpose, as illustrated in Figure 20, the area right above the DLTS sample was chosen.

The first step of cutting process was done using a laser cutter. This step is illustrated on the left side on Figure 20, where the dashed lines indicate cutting lines and the blue rectangles represent the location and size of the desired sample shape. As the samples were quite thick (around 2 mm), it was not possible to achieve the samples with the dimensions desired for DLTS by laser cutting. The further cutting process was performed at Area della Ricerca di Bologna, Consiglio Nazionale delle Ricerche (CNR) using a mechanical saw of type ADT7100 from VECTUS Dicing series Vectus/Fortis Model Types with Software Version 5.4. Each sample was cut individually using a blade of type Resin Hubless with exposition 1.8 mm and thickness of 200 mm. The obtained samples for AFM characterization had dimensions of 0.5 x 1 cm, while the DLTS samples had dimesions of 0.5 x 0.8 cm.

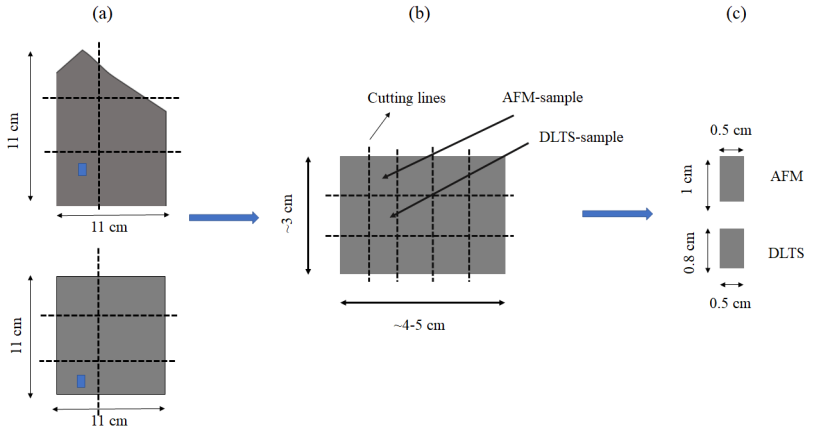

Figure 20: Schematic illustration of the cutting process; dashed lines symbolize the cutting lines. (a) The primary dimensions of the samples were 11 cm x 11 cm. On top the crown sample, in the bottom the body sample. (b) Intermediate cutting step. The sample sizes were slightly different from each other and varied between 3 cm x 4 cm to 3 cm x 5 cm. (c) The final cutting step. The final dimensions for AFM samples (shown on top) were around 0.5 cm x 1 cm, and for DLTS samples (shown in the bottom) 0.5 cm x 0.8 cm.

As a result, 16 samples were obtained; 8 for the IV-, CV- and DLTS- measurements and 8 for the AFM-imaging. The table below shows the sample names and their explanation.

Table 2: Overview of the samples with their name and description.

DLTS samples	AFM samples	Sample explanation
$CU_{low}D$	$CU_{low}A$	Lower Pulling Speed Untreated Crown
$CH_{low}D$	$CH_{low}A$	Lower Pulling Speed Heat Treated Crown
$BU_{low}D$	$BU_{low}A$	Lower Pulling Speed Untreated Body
$BH_{low}D$	$BH_{low}A$	Lower Pulling Speed Heat Treated Body
$CU_{high}D$	$CU_{high}A$	Higher Pulling Speed Untreated Crown
$CH_{high}D$	$CH_{high}A$	Higher Pulling Speed Heat Treated Crown
$BU_{high}D$	$BU_{high}A$	Higher Pulling Speed Untreated Body
$BH_{high}D$	$BH_{high}A$	Higher Pulling Speed Heat Treated Body

7.2.2 Grinding and Polishing

For both AFM and DLTS-techniques, it was required that the sample's surface is optically clean which was achieved by manual grinding and polishing. The surface was checked under an optical microscope. In addition, for the DLTS-

measurements, grinding was used to reduce the thickness of the samples from around 2 mm to less than 1 mm.

The lapping machine used in this work for grinding and polishing was semi-automatic; the rotating disk for sandpaper and polishing disk, was controlled by the machine, while the position, rotation and pressure applied from the sample holder on the rotating disk was controlled by the operator. This has resulted in the prolonged time of polishing steps to ensure an evenly polished surface, see Table 3.

The samples were attached to the glass sample holder with apiezon wax. First, the sample holder was placed on a heating plate and heated up until it was hot enough to melt the wax (over 90 °C). A thin layer of wax was then applied and the sample was placed on top. When the wax was solidified and the sample holder was cooled down, it was placed inside of a sample holder that was 3D-printed to secure a more firm grip. The dimensions of the bottom part of the 3D-printed holder were such that the glass sample holder would fit accurately.

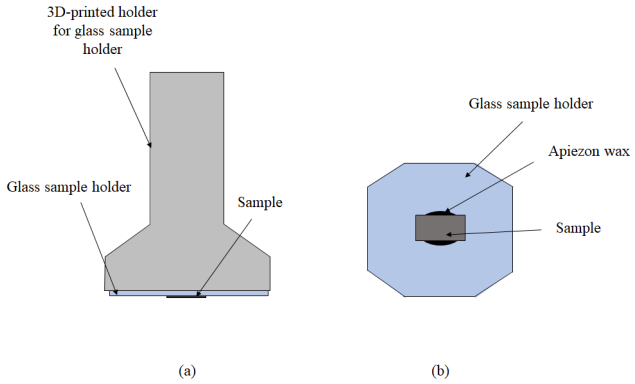

Figure 21: (a) Side view on the 3D- printed sample holder with inserted glass sample holder on the bottom. (b) Top view on the glass sample holder. Apiezon wax is used to hold the sample in place.

After the polishing has been observed to be sufficient enough (evenly polished surface), the sample holder was removed using tweezers and put into a glass beaker with toluene in order to remove the apiezon. The sample was then cleaned further with acetone to remove any eventual wax and toluene residuals.

Table 3 shows the grinding and polishing steps. As the samples had a relatively small area, it was enough to use sand paper with high fineness to grind the samples to the desired thickness.

Table 3: Grinding and polishing sequence

Sand Paper Fineness	Diamond Paste Fineness	Time
2400	-	15 min
-	6 μm	7.5 min
-	3 μm	7.5 min
-	1 μm	10 min
-	0.25 μm	3 min

7.2.3 Etching

This step of sample preparation has been done in order to remove the SiO_2 layer from the sample surface that builds up when silicon is in contact with air. While for the DLTS samples this was an important preparation step before gold evaporation to ensure that gold is deposited on the silicon without the native oxide layer, for the AFM samples it was necessary to remove the layer to ensure that the whole sample surface was conductive when the c-AFM tip touched the sample.

To find the ideal etching time to ensure the complete removal of the oxide layer, one of the heat treated samples has been used as a test sample. The heat treatment procedure has been presented in Warden [1] and it was performed in a mixture of oxygen and nitrogen. This caused the oxygen layer on top of the heat treated samples to be quite thick. As the heat treated samples were blue on the surface, the way to find the ideal etching time, was to submerge the heat treated sample into the etching solution (10% HF) and wait until the blue color was gone. It has been observed that the layer was removed after around 60 seconds, thus the rest of the samples was then submerged into the 10% HF-solution one by one for this amount of time.

7.2.4 Ohmic contacts

To determine defective states by DLTS a Schottky junction must be prepared on each sample, thus a Schottky barrier (gold evaporation on top) and an ohmic contact (InGA paste on the back) need to be prepared. The latter was the next step after the samples had been etched in the HF-solution.

The InGa-mixture used for the ohmic contact, was prepared by mixing approximately equal amounts of solid In and Ga. Each of the DLTS samples were scratched on the back side using a diamond tip. A thin layer of InGa-mixture was applied on the scratched surface. It was then left for a couple of minutes to solidify to ensure that the contact stabilization.

7.2.5 Schottky barrier

As the silicon samples were n-type, gold evaporation was performed to produce a Schottky barrier. The process consists of several steps, starting with masks preparation.

The masks for gold evaporation were made out of a thin aluminium plate. First, a stripe of around 12 x 1.5 cm was cut from the plate. It was further cut into smaller pieces, such that they could cover the whole sample surface when put on top of it, hence the dimensions of the masks were around 1 x 1.5 cm. Later, two holes of around 2 mm in diameter were drilled in order to create two gold contacts on each sample.

For this evaporation process, 268 mg of gold was weighted using a digital scale. Around 5 cm of gold wire was cut from a spool and swathed around a toothpick; this made it easier for mounting the folded gold wire on the tungsten basket inside the evaporation chamber. The gold was then put inside a glass beaker and filled with acetone to a point where the gold was completely submerged. The beaker was covered with aluminium foil and put inside a sonication bath for 15 minutes. After the sonication bath the gold was dried using a nitrogen gas gun and put back again into a clean beaker. The beaker was filled with isopropanol to completely submerge the gold inside, and the process of sonication was repeated for another 15 minutes. The gold was then dried again using the nitrogen gas gun and was ready to be mounted into the tungsten basket.

While the gold was put into sonication, the samples could be put on the sample holder used for gold evaporation. Figure 22 shows a schematic illustration of how the samples were distributed around the sample holder. Note that the empty space was occupied by other samples. The samples were placed with the Ohmic contact on the back and the masks were located in such a way that the evaporated gold dots would be located approximately in the middle of the sample, not close to the edges. The masks were then secured in place with tape around all four edges which also secured that the gold would only be evaporated on the spots defined by the holes in the masks.

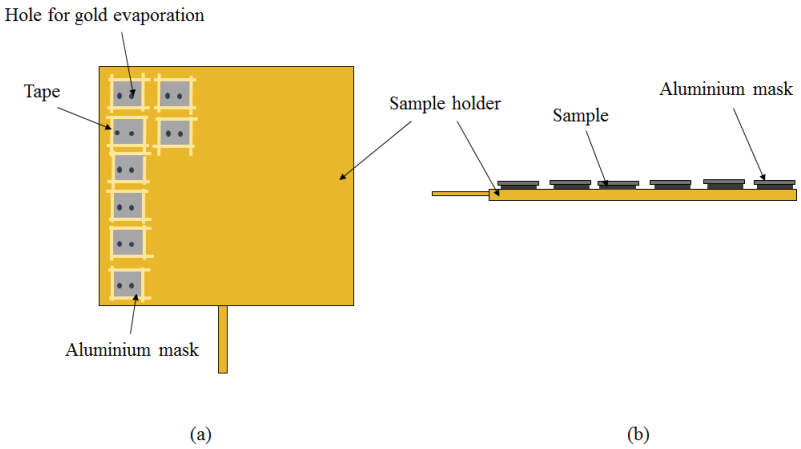

Figure 22: (a) Top view on the sample holder. The samples are placed below the aluminium mask with two holes drilled for the evaporated gold. Tape is used to secure gold evaporation in the designated place and keeping the samples and the masks in place. The empty space was taken by other samples. (b) Side view on the cross section of the sample holder.

When all the samples were mounted, the sample holder was moved to the evaporation chamber and mounted as shown in Figure 23. The gold was placed on the tungsten basket which was then inserted in the gate. The whole chamber was then closed by the glass cover, and the shutter was moved into the start position (above the gates) using a magnet through the glass cover.

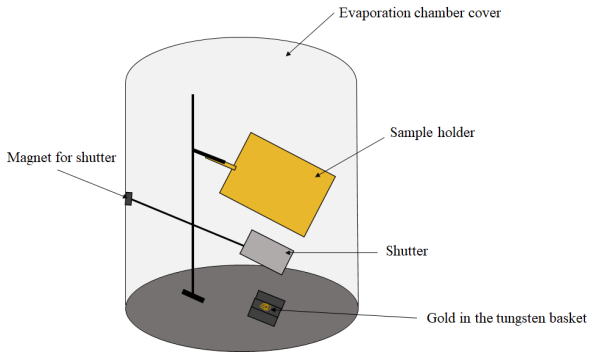

Figure 23: A schematic illustration of the evaporation chamber with some crucial system elements, from the top: evaporation chamber cover, sample holder placed with the samples facing the bottom of the chamber, shutter controlled by magnet and placed above the tungsten basket, and finally the tungsten basket with gold.

When all the system elements were set in the starting position, the pump system for creating vacuum inside the chamber could be started according to a standard procedure. The vacuum system consists of a rotary pre-vacuum pump and a turbomolecular pump. An actual picture of the evaporation chamber with the pump system is shown in Figure 24.

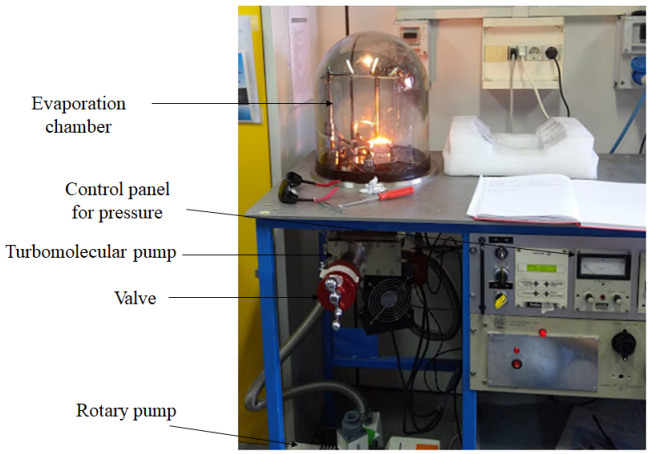

Figure 24: Picture of the complete evaporation system with some of the important elements indicated.

When a vacuum level of around $6 \cdot 10^{-7}$ mbar was reached, the evaporation process was started. The current flowing into the tungsten basket in the gate was increased with a knob by 5% every 15 seconds until it reached 20%. Until this point the shutter was kept in the same position to protect the samples from getting a deposition of unwanted species coming from the gold surface. The shutter was removed from the start position using the magnet. Once the shutter was removed, the current was being increased again by 5% every 15 seconds. At around 35% the gold started to evaporate and the basket was empty at 50%. The maximum current during this evaporation was 20A. It is worth commenting that the percentage on the knob does not correspond to the actual current used, the numbers are used only to control the current.

After the basket was empty the current was gradually decreased to 0 with 5% every 30 seconds. Further, the pump system was turned off in the correct order, the cover was removed and the sample holder could be taken out. The thickness of the gold layer was measured by AFM to be around 38 nm.

7.2.6 Electrical contacts

The next step of sample preparation for DLTS-characterization was to make electrical contacts between the sample holder and the Schottky and Ohmic con-

tacts. The complete setup is shown in Figure 25 and it will now be explained in detail.

Firstly, the sample holder is presented. It consists of three conductive islands separated by insulating stripes. The Ohmic contact was placed on the central island, while the Schottky could be put on either of the two separated islands.

The contact between the Ohmic and the sample holder was done by applying a thin layer of a bi-component silver paste onto the central island on sample holder and placing the sample on top of it. By doing so, the whole rectangular area of the sample holder (the central island) (see Figure 25 b)) was in contact with the sample's Ohmic contact, while the two outer islands of the sample holder separated by a valley were not connected to the Ohmic contact.

One of the outer islands was then used to form the connection to the Schottky contact on top of the sample. This was primarily done by using a P-bronze clamp soldered to the sample holder and going onto to the gold contact. This setup was then changed due to lack of meaningful results and the P-bronze clamp was changed to a copper clamp. Again, this turned out to be not ideal, as the measured values for capacitance seemed to be too low (this is further described in Chapters 8 and 9). That is why it was suggested to try a different setup; using bi-component silver paste on top of the gold contact and connecting a thin gold wire from there to the sample holder, heating the system at 80 °C to ensure complete attachment of all elements. This however, could not be performed, as further described in Chapter 11.

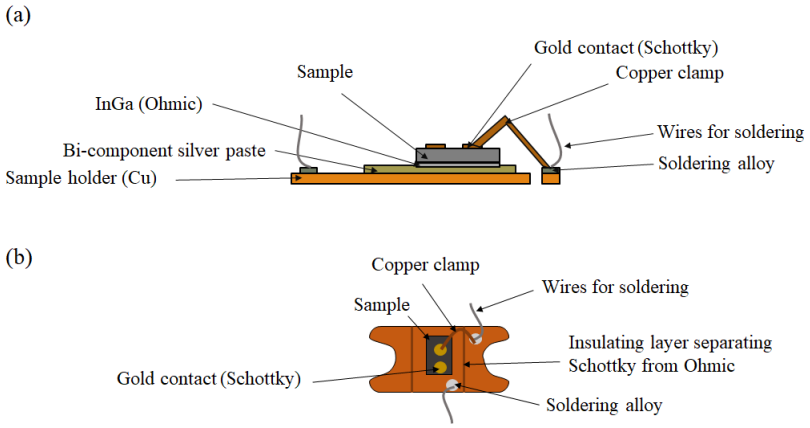

Figure 25: Schematic illustration of the electrical contacts from: (a) side view, (b) top view.

7.3 Current-voltage measurements

Figure 26 shows a simplified illustration of the experimental setup for IV-, CV- and DLTS- measurements with indicated the most important setup components.

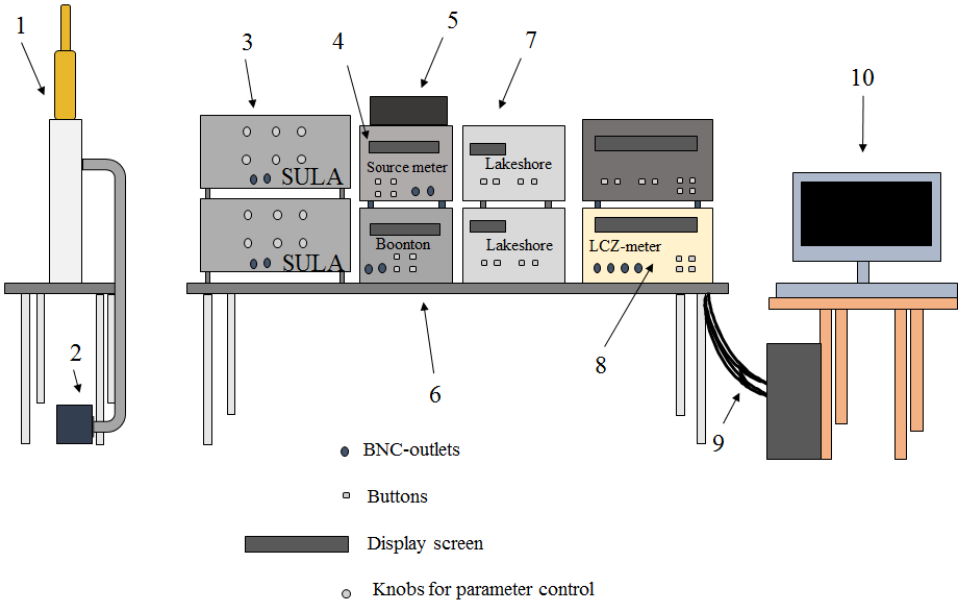

Figure 26: Illustration of the experimental setup for the IV-, CV- and DLTS-measurements. The most important setup elements are indicated with numbers: 1. Cryostat connected to the rotary pump, 2. Rotary pump, 3. SULA instrument for DLTS measurements, 4. Source meter for IV measurements, 5. Faraday box with a sample inside, 6. Boonton capacitance meter for CV measurements and applying of external bias, 7. Lakeshore temperature controllers, 8. LCZ instrument for CV measurements, 9. Cables connected to the PC, 10. Computer system with installed LabView programs.

Current-voltage measurements (IV-measurements) were the first step for checking the performance of the prepared diodes. The IV-curves were measured by connecting the sample to a Faraday box by soldering. Figure 27 represents the setup inside the Faraday box. As it can be seen, the sample was connected to the box using the two loose wires soldered to the sample holder (one in the Ohmic part, the other in the Schottky). Further the box was connected by a BNC-connection to the Keithley SourceMeter 2400. The Schottky contact was connected to the "HI INPUT" (positive), while the Ohmic contact was connected to the "LO INPUT" (negative). Before measuring the IV-curves, the box was closed with a cover to shield the sample from external electromagnetic interference and from ambient light.

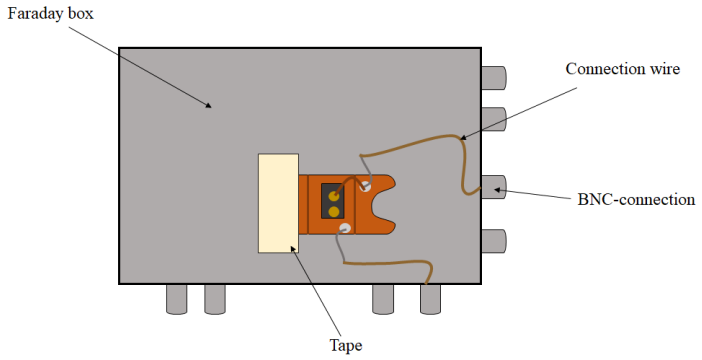

Figure 27: Schematic illustration of top view on the setup inside the Faraday box used for IV- and CV-measurements. The sample was connected to the BNC-connector through a wire that was with both ends by soldering. The sample holder was held in place by a piece of tape.

The SourceMeter was connected by a GPIB-connection to the computer with software dedicated to IV-measurements. The software was a LabView program developed specifically for this setup where the user can vary several variables, such as the start voltage, to end voltage and the step. The voltage range in which the IV-curves were measured was from -5 to 5 V with the step of 0.1 V.

7.4 Capacitance- voltage measurements

For the CV-measurements the same setup in the Faraday box was used. Here, the sample was connected to the LCZ-meter 3330 Keithley. In this case the Schottky contact was connected to "HPOT" and "HCUR" outputs, while the Ohmic was connected to "LPOT" and "LCUR" outputs. Figure 28 shows a simple sketch of how the sample is connected for this type of measurements.

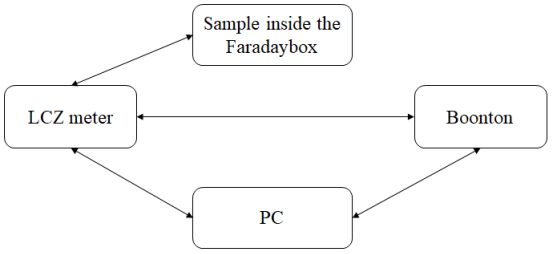

Figure 28: A sketch of the connections for the CV-measurements done by the LCZ meter. The sample inside the Faraday box is connected to the LCZ meter, LCZ is connected to the Boonton and the PC and the Boonton is connected to both the LCZ meter and the PC.

Since the LCZ-meter needs an external device to generate bias, it was connected to 7200 Capacitance Meter produced by Boonton (later referred to as Boonton) by a GPIB-connection. Further the LCZ-meter was connected to the computer and the measurements were performed using a specifically developed LabView program. The variables that could be chosen were: frequency, initial bias, final bias, bias step, initial and step delay. The frequency was set to the maximum of 10 kHz, initial bias was 0 V, final bias was set to -5 V, the step was set -0.1 V and the initial and step delay were both set to 1000 ms.

7.5 DLTS-measurements

For DLTS measurement, the sample was mounted on a cryostat, shown in Figure 29 where the most crucial system elements are indicated. Starting from the top, there is an inlet for liquid nitrogen that is used to cool down the cryostat. Further down there are two BNC-connectors, one for the Ohmic and one for the Schottky contacts. At almost the same height there is a connection to the vacuum pump and the outputs two thermocouples used for monitoring the temperature. They are connected next to the cold finger, one close to the heater (for temperature ramp control) and the other next to the sample (for sample temperature control). In addition, on the same level there is a connection to the heater. The heater is connected to the cold finger where sample is placed in order to heat up the samples during the measurements. Further there is the cryostat chamber where nitrogen is stored that is thermally isolated with teflon. At the bottom, a cold finger connected to the nitrogen chamber serves as sample holder.

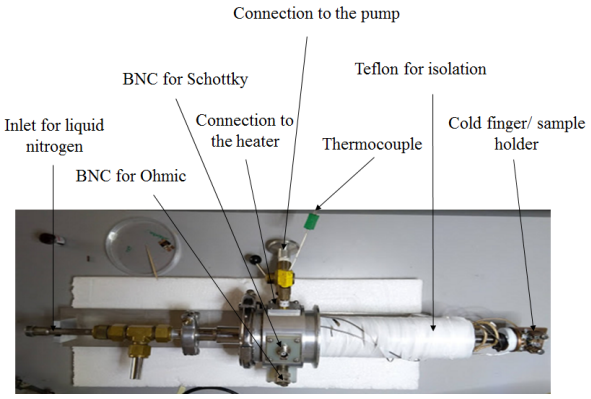

Figure 29: Cryostat outside of the vacuum chamber. The most crucial system elements are indicated in the figure. From the top: inlet for liquid nitrogen, two BNC connectors, connection to the vacuum pump, thermocouple, nitrogen chamber covered with teflon for isolation and finally close finger that serves as sample holder.

The sample was mounted on the designated place by first applying a thin layer of a thermal paste where the sample holder was placed. Further the two loose wires on the sample holder were connected to BNC-cables, whose signal is measured through the outlets described above. It was done by applying a droplet of a silver paste that connected the wire from the sample to the wire from the cryostat. It was then left to dry for a couple of minutes before mounting the cryostat into the vacuum chamber. Figure 30 shows how the sample is mounted onto the cryostat.

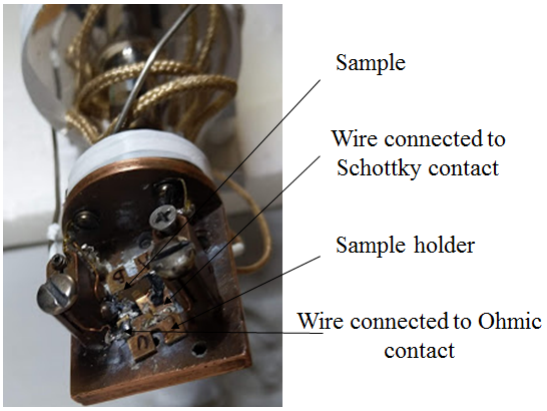

Figure 30: Sample mounted onto the cryostat.

When the silver paste was dry, the cryostat was mounted inside the vacuum chamber with sample in vertical postion. Then, the vacuum pump was connected to the inlet and the thermocouple and heater connections were sent to the temperature controllers. Once a vacuum of around $2 \cdot 10^{-5}$ bar was reached, liquid nitrogen was poured into the chamber.

The instrument used in the DLTS-measurements was a DLTS-instrument from SULA Technologies, further referred to as SULA. The analog signal from SULA was converted using an acquisition box. The previously mention thermocouples were connected to two temperature controllers Lakeshore 331 and Lakeshore 332. The cryostat was connected to SULA by the two BNC-outlets. The complete setup of the cryostat for the DLTS-measurements is shown in Figure 31.

The DLTS-measurements were done using a LabView program designed specifically for this setup. The parameters had to be set manually from the instrument, and then transcribed into the software. The parameters in this measurement are: pulse width, period, offset, amplitude, acquisition time, pretrigger acquisition time, pulse end time. They were set to: 50 ms, 100 ms, -1V, -0.1V, 100 ms, 2 ms and 6 ms, respectively.

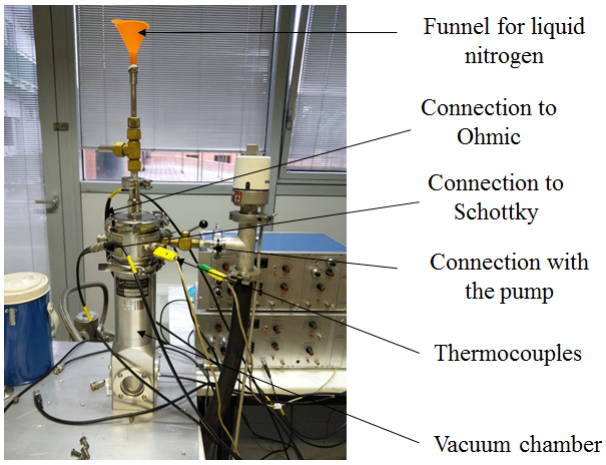

Figure 31: Cryostat mounted into the vacuum chamber and connected to the SULA instrument. On top a funnel for liquid nitrogen is mounted to the inlet, further down there are the two BNC-connectors connected to the SULA. There is also the vacuum pump connected and the two thermocouples. The vacuum chamber is also indicated in the figure.

7.6 Test measurements

7.6.1 Measurements on the test diode

During the measurements of the silicon samples, it was discovered that the obtained results did not fit with the known theory. It was obvious that the problem was either due to a problem with the measuring equipment or due to poor sample preparation. Therefore, it was decided to run the same set of measurements on a test diode that was sure to be working.

The device was an industrially produced p-doped diode with an aluminium layer on top. It was mounted on a sample holder using the bi-component silver paste. On one of the outer parts of the sample holder, a copper clamp was soldered and directed onto the top of the sample to make contact with the aluminium layer. The setup is shown graphically in Figure 32.

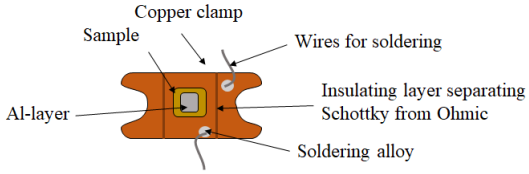

Figure 32: Schematic illustration of the test diode on the sample holder that was used for test measurements.

The sample holder was then placed inside the Faraday box and the IV, CV. In this case the Schottky contact was connected to the negative outputs of the measuring devices (e.g. "LO INPUT" in the SourceMeter), while the Ohmic contact was connected to the positive outputs (e.g. "HI INPUT" in the SourceMeter).

Further, the DLTS measurements were also repeated for this sample, but this time the test diode was left inside the Faraday box, meaning that the C vs t curve was only measured once, in the room temperature.

7.6.2 Measurements with clamp touching silicon

As it was mentioned above, the results obtained using a copper clamp on top of the Schottky contact did not give meaningful results. It was suggested that it could be due to the gold layer being destroyed by the clamp upon attaching it to the system, so that during the measurement the clamp is in contact with the silicon surface and not the gold layer.

To test this hypothesis, the clamp was moved a bit further from the gold contact where it was sure it would only touched the silicon. The new setup is presented in Figure 33. The test sample in this case was sample $CH_{high}D$.

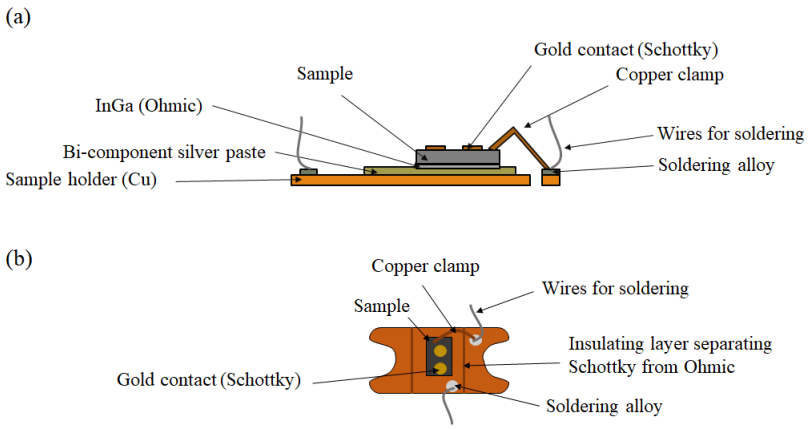

Figure 33: Schematic illustration of the electrical contacts for the clamp test: (a) side view, (b) top view. Note that in this case the clamp is placed directly on the silicon surface.

7.7 AFM imaging

The samples used for AFM-imaging come from the area slightly above the samples used for the electrical properties characterization, as can be seen in Figure 20. The sample size was around 0.5 x 1 cm. The untreated samples

needed to be polished to achieve optically clean surface, while the surface of the heat treated ones seemed to be clean enough. The grinding and polishing sequence was as presented in Table 3.

The samples were then placed on sample holders (magnetic disks) and held in place using a double-sided type. Since the experiment was supposed to be done in the conductive AFM-mode, an electrical connection between the sample's surface (which was to be investigated) and the sample holder was needed. The two surfaces were connected using a silver paste that was applied on the edges and a small part of the sample's surface and the sample holder. The sample setup is presented in Figure 34.

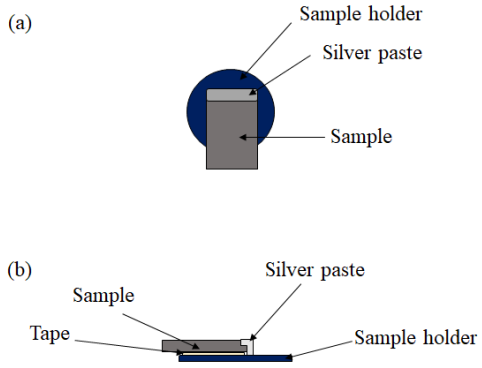

Figure 34: Schematic illustration of the sample setup for a conductive AFM-experiment; (a) view from top, (b) view from side. Double-sided tape is used for fixing the sample in place on the sample holder and the silver paste is applied on top, the edges of the sample and the sample holder next to the sample to make an electrical contact between the sample holder and the sample's surface.

The AFM-equipment used in this work consists of the following components: Park-NX10 Main System and Control Electronics, monitors, PC and an active vibration isolation table. The software controlling the system was NX10 Software Smart Scan (further referred to as Smart Scan). The experiments were performed in the conductive mode described in Chapter 6.4.1 using a platinum tip of type Rocky Mountain 25Pt300B.

The first step of an AFM-experiment is always to turn on the anti-vibration table and unmount the AFM-head from the instrument. For that, it is important to swtich of the beam. In a conductive AFM-experiment a platinum tip is often used and it must be inserted carefully onto the head which is then placed inside the instrument. In the case of conductive AFM, the head must be also equiped with a current amplifier. When all these steps were done, the sample was also placed inside the system.

While the beam was still switched off, the next step was to focus the optical microscope integrated in the system onto the cantilever. The beam was then switched on and directed onto the cantilever using the alignment knobs. Further, the beam was once again switched off and the cantilever was aligned with the microscope. The beam was again switched on and it was aligned with position sensitive photon detector (PSPD), which concludes the practical experimental setup.

The next step was to choose the right AFM-mode, which in this case was I-AFM and the probe parameters were selected in the Smart Scan software for the chosen platinum tip. Further, scanning parameters were selected and they are presented in Table 4 below.

Table 4: Scan parameters for the AFM-imaging.

Parameter	Value
Scan Rate	0.30 Hz
Z-slope	0.00 °
Size	50 x 50 μm
Pixels	256 x 32

Since use of the current amplifier would generate a voltage when the tip is not in contact in the sample, there was a need to correct for the current offset. It needed to be done for each sample individually.

During this experiment three channels were monitored: Z-height, error signal and current. When all the parameters were selected and offset was corrected, the Z/F stage was approached near the sample and stopped around 2 mm above it and it was further approached using Smart Scan automatically. If the PSPD alignment was still good, the experiment could be started. In the case of misalignment, the Z/F stage was lifted above by around 40 μ and approached slowly again. The experiment was then performed.

It is important to note that the scan parameters and the current amplifier offset must be corrected/chosen appropriately for each individual sample. The scan parameters shown in Table 4 are the start parameters for each of the samples which could be corrected if the obtained scans were not satisfactory. From this settings and parameters both a topography map and a current map could be obtained.

8 Results

This chapter will present the results obtained during the experiments described in the previous section. It will be divided into four sections corresponding to the characterization techniques and each of the section will be further divided into subsections corresponding to the samples' origin. This chapter will also include a section containing some of the results from the specialization project that are going to be used for further discussion in Chapter 9 [1].

8.1 IV-curves

The results presented in this section show the IV-characteristics of each of the obtained diodes, the test diode and the case in which the clamp was located on top of the silicon surface as seen on Figure 33. All of the measurements were done in Faraday box under dark conditions.

8.1.1 Lower Pulling Speed body samples

Figure 35 presents the IV-curves measured for both heat treated and untreated Lower Pulling Speed body samples: $BU_{low}D$ (blue curves) and $BH_{low}D$ (red curves) in both linear and semilogarithmic scale. As mentioned in Chapter 7 the diode was first made using a P-bronze clamp which was later changed to a copper clamp. The following graphs will therefore present a comparison between the two curves obtained using different materials, where the P-bronze case will be represented with a continuous line, while the case of copper will be represented with stars. Note that the second letter in the sample name is used to identify whether the sample was heat treated or not. "U" means that the sample was untreated, while "H" stands for heat treated.

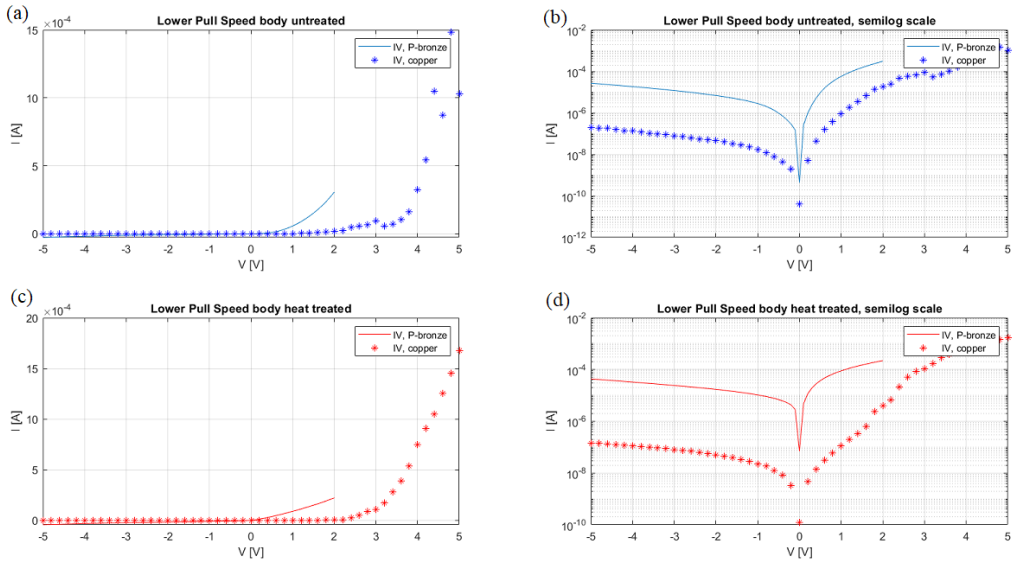

Figure 35: IV-curves of the Lower Pulling Speed body samples: (a) Untreated in linear scale; (b) Untreated in semilogarithmic scale; (c) Heat treated in linear scale; (d) Heat Treated in semilogarithmic scale. The continuous line on each graph represents the measurements done using a P-bronze clamp, while the stars represent the measurements done using a copper clamp. The x-axis represent the applied voltage measured in Volts, while the y-axis shows the measured current in Ampers.

8.1.2 Higher Pulling Speed body samples

The IV-curves of samples $BU_{high}D$ (untreated HPS body sample) and $BH_{high}D$ (heat treated HPS body sample) are presented in Figure 36 in both linear and logarithmic scale. Note that in the case of $BU_{high}D$ the IV-curve for the case of P-bronze clamp has the exact same values for voltage range -5 V to 2 V, hence it appears somehow behind the curve for the case of copper clamp.

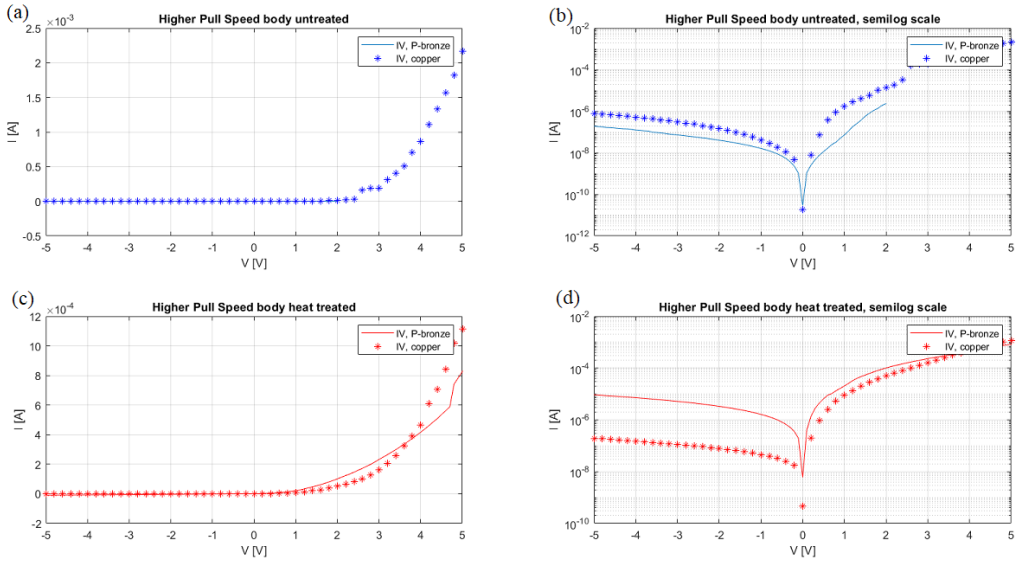

Figure 36: IV-curves of the Higher Pulling Speed body samples: (a) Untreated in linear scale; (b) Untreated in semilogarithmic scale; (c) Heat treated in linear scale; (d) Heat Treated in semilogarithmic scale. The continuous line on each graph represents the measurements done using a P-bronze clamp, while the stars represent the measurements done using a copper clamp. The x-axis represent the applied voltage measured in Volts, while the y-axis shows the measured current in Ampers.

8.1.3 Lower Pulling Speed crown samples

Figure 37 shows the IV-curves of samples $CU_{low}D$ and $CH_{low}D$ in both linear and logarithmic scale.

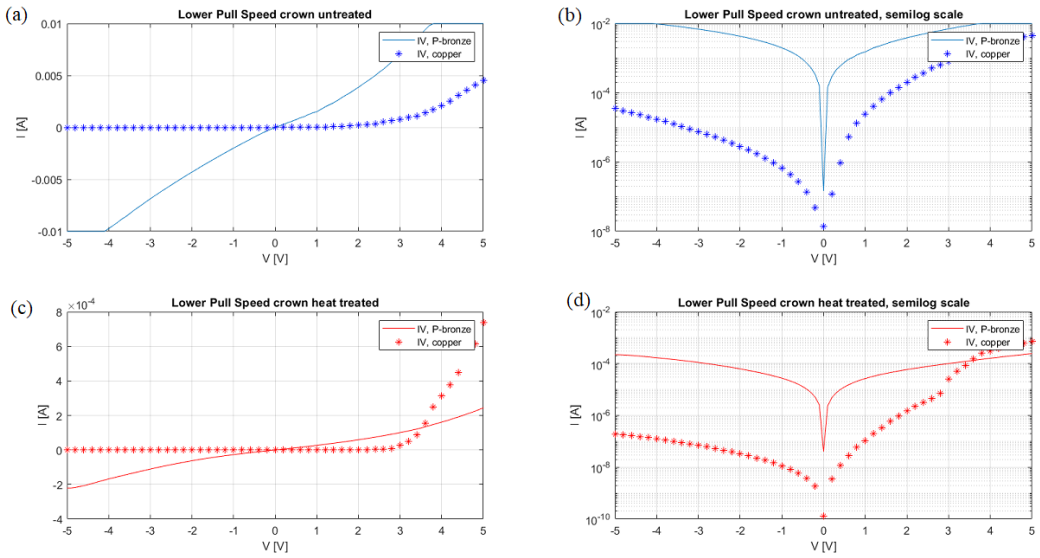

Figure 37: IV-curves of the Lower Pulling Speed crown samples: (a) Untreated in linear scale; (b) Untreated in semilogarithmic scale; (c) Heat treated in linear scale; (d) Heat Treated in semilogarithmic scale. The continuous line on each graph represents the measurements done using a P-bronze clamp, while the stars represent the measurements done using a copper clamp. The x-axis represent the applied voltage measured in Volts, while the y-axis shows the measured current in Ampers.

8.1.4 Higher Pulling Speed crown samples

The results of IV-measurements performed on samples $CU_{high}D$ and $CH_{high}D$ are shown in Figure 38. Similarly to $BU_{high}D$ the IV-curve for the case of the P-bronze clamp have shown the same values as for the copper clamp case, hence this graph seems to appear behind the one for the copper clamp.

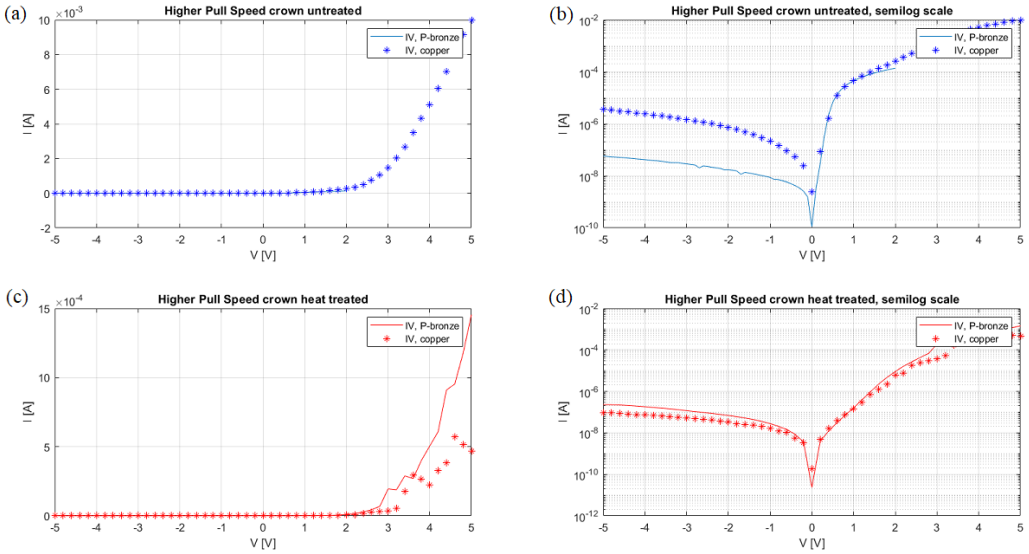

Figure 38: IV-curves of the Higher Pulling Speed crown samples: (a) Untreated in linear scale; (b) Untreated in semilogarithmic scale; (c) Heat treated in linear scale; (d) Heat Treated in semilogarithmic scale. The continuous line on each graph represents the measurements done using a P-bronze clamp, while the stars represent the measurements done using a copper clamp. The x-axis represent the applied voltage measured in Volts, while the y-axis shows the measured current in Ampers.

8.1.5 Test diode

Figure 39 shows the result of IV-measurements performed on the test diode.

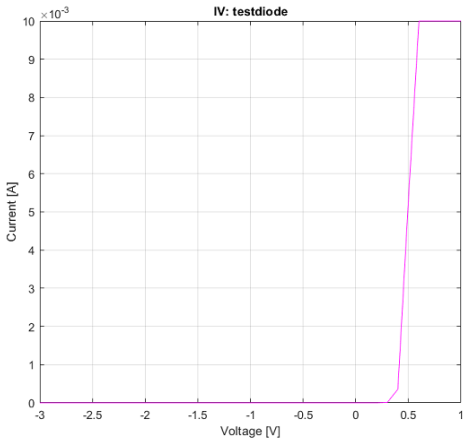

Figure 39: IV-curve of the test diode: the x-axis represent the applied voltage measured in Volts, while the y-axis shows the measured current in Ampers.

8.1.6 Clamp test

Figure 40 presents the IV-curve of the system presented in Figure 33 where the copper clamp is touching the silicon surface directly.

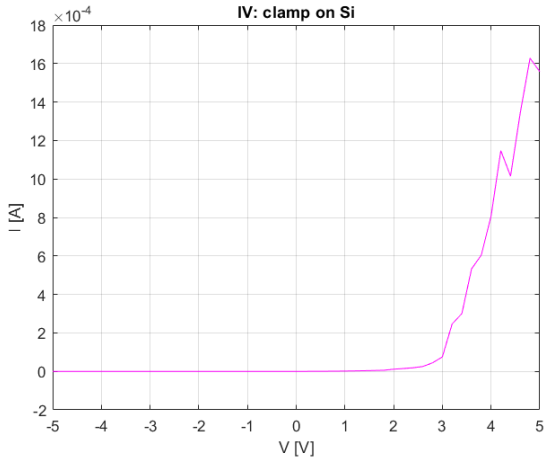

Figure 40: IV-curve of the system where clamp is touching the silicon surface directly: the x-axis represent the applied voltage measured in Volts, while the y-axis shows the measured current in Ampers.

8.2 CV-profiles

The following sections present the results of CV-measurements performed on the diodes, the calculated $1/C^2$ vs V relationship and finally the calculated free carrier concentration for each of the samples, excluding the test diode and the device presented in Figure 33, where the copper clamp is in direct contact with the silicon surface.

8.2.1 Lower Pulling Speed body samples

Figure 41 shows the results of CV-measurements done on the LPS body samples, $BH_{low}D$ and $BU_{low}D$. The results are presented in four graphs: two of them show the case of P-bronze clamp, while the other two show the case of copper clamp.

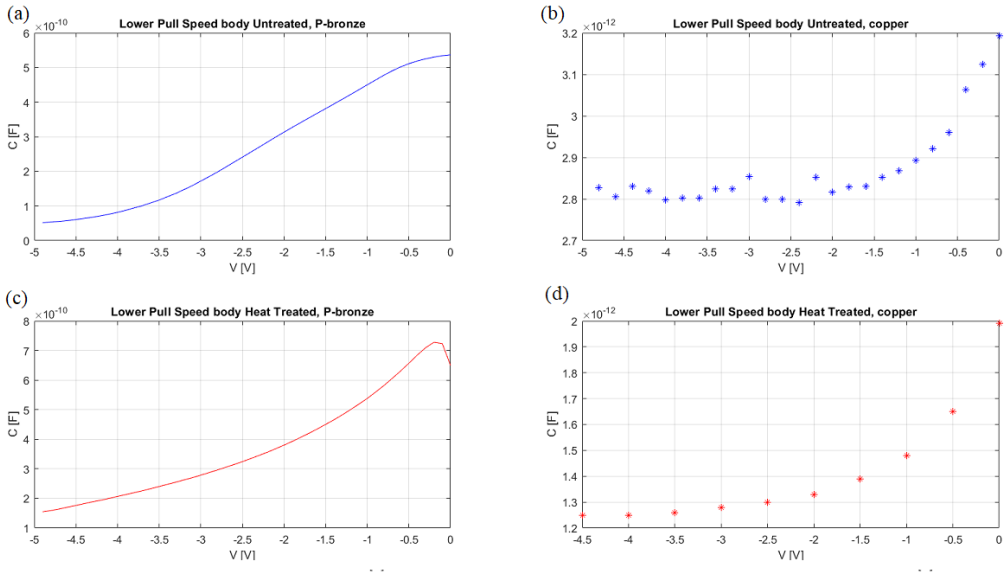

Figure 41: CV-curves of the Lower Pulling Speed body samples: (a) Untreated with P-bronze contact; (b) Untreated with copper contact; (c) Heat treated with P-bronze contact; (d) Heat Treated with copper contact. The x-axis represent the applied voltage measured in Volts, while the y-axis shows the measured capacitance in Farads.

The calculated slopes of $1/C^2$ for the two LPS body samples are presented in Figure 42. Again, both the case of using P-bronze and copper as the clamp material are presented for both the heat treated and untreated samples.

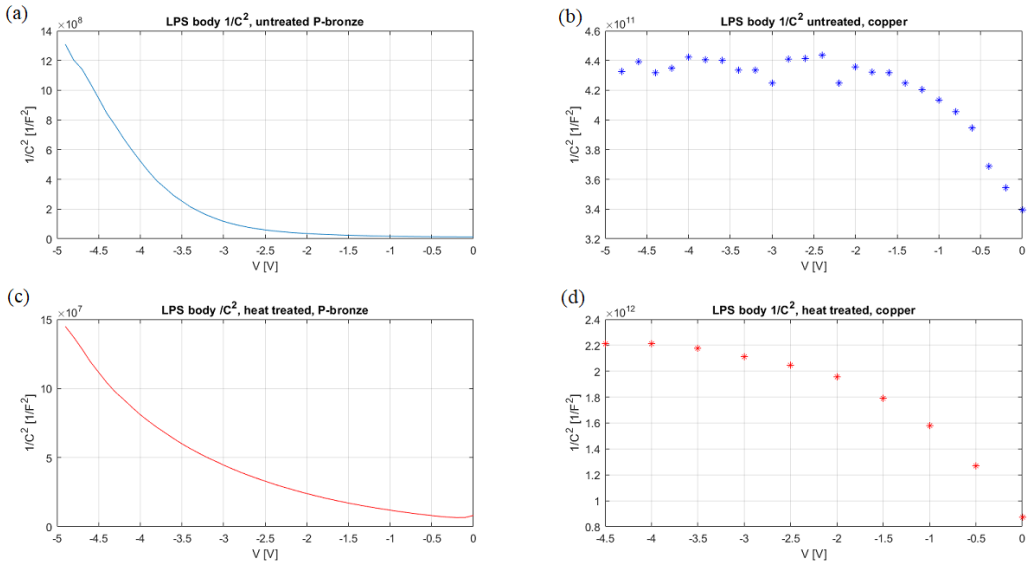

Figure 42: $1/C^2$-curves of the Lower Pulling Speed body samples: (a) Untreated with P-bronze contact; (b) Untreated with copper contact; (c) Heat treated with P-bronze contact; (d) Heat Treated with copper contact. The x-axis represent the applied voltage measured in Volts, while the y-axis shows the $1/C^2$ in $1/F^2$.

Further, the free carrier concentration was calculated according to Equation 8 presented in Chapter 6.2. The free carrier concentration profiles as a function of depletion layer width for the Lower Pull Speed body samples are presented in Figure 43.

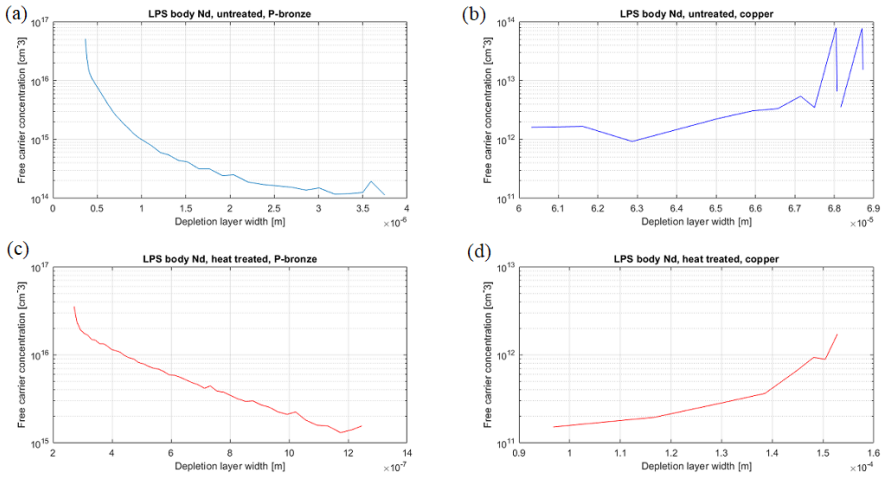

Figure 43: Free carrier concentration curves of the Lower Pulling Speed body samples: (a) Untreated with P-bronze contact; (b) Untreated with copper contact; (c) Heat treated with P-bronze contact; (d) Heat Treated with copper contact. The x-axis represents the depletion layer width in meters, while the y-axis shows the calculated free carrier concentration in m^{-3}.

8.2.2 Higher Pulling Speed body samples

The CV-curves of $BH_{high}D$ and $BU_{high}D$ samples are presented in Figure 44, following the same presentation structure as the one in Chapter 8.2.1. Figure 45 presents the calculated $1/C^2$-slope and finally Figure 46 shows the calculated free carrier concentration profiles for the two High Pulling Speed body samples.

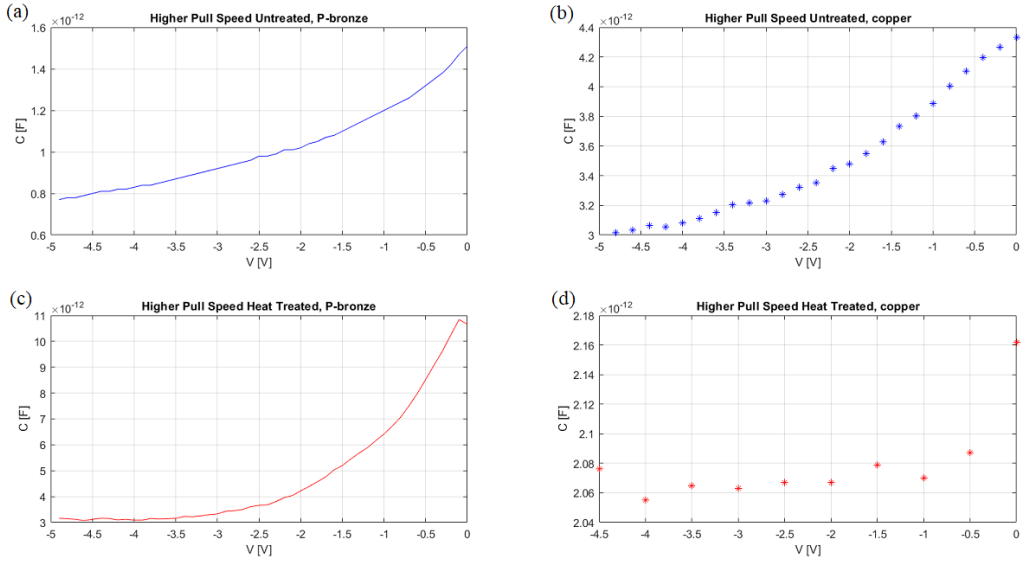

Figure 44: CV-curves of the Higher Pulling Speed body samples: (a) Untreated with P-bronze contact; (b) Untreated with copper contact; (c) Heat treated with P-bronze contact; (d) Heat Treated with copper contact. The x-axis represents the applied voltage measured in Volts, while the y-axis shows the measured capacitance in Farads.

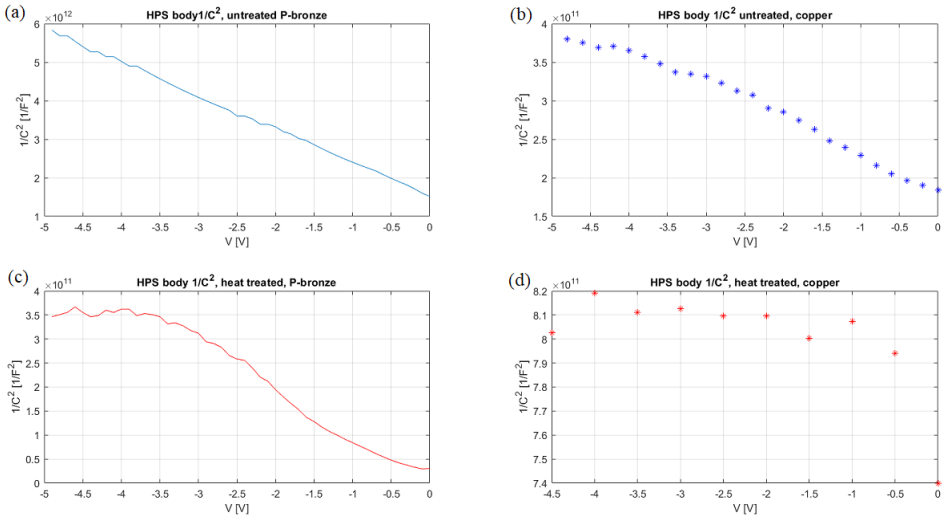

Figure 45: $1/C^2$-curves of the Higher Pulling Speed body samples: (a) Untreated with P-bronze contact; (b) Untreated with copper contact; (c) Heat treated with P-bronze contact; (d) Heat Treated with copper contact. The x-axis represents the applied voltage measured in Volts, while the y-axis shows the $1/C^2$ in $1/F^2$.

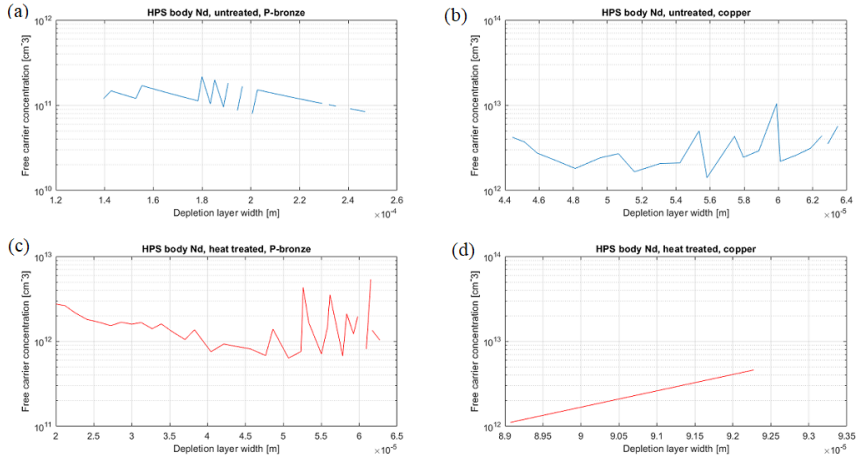

Figure 46: Free carrier concentration curves of the Higher Pulling Speed body samples: (a) Untreated with P-bronze contact; (b) Untreated with copper contact; (c) Heat treated with P-bronze contact; (d) Heat Treated with copper contact. The x-axis represents the depletion layer width in meters, while the y-axis shows the calculated free carrier concentration in m^{-3}.

8.2.3 Lower Pulling Speed crown samples

The CV-profiles for $CU_{low}D$ and $CH_{low}D$ are presented in Figure 47. In this case only the curves measured using the copper clamp setup are presented, hence the Figure consists only of two graphs. Further, Figure 48 shows the $1/C^2$ slopes for the two samples and the free carrier concentration profiles are shown in Figure 49.

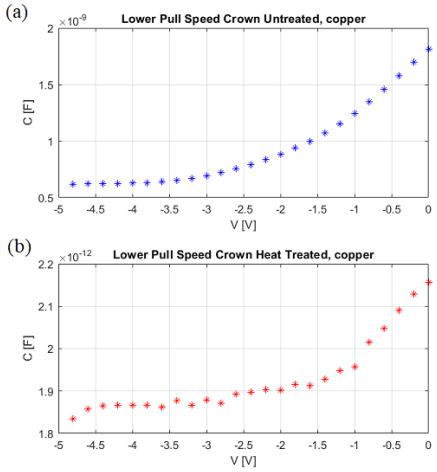

Figure 47: CV-curves of the Lower Pulling Speed crown samples: (a) Untreated with copper contact; (b) Heat treated with copper contact. The x-axis represents the applied voltage measured in Volts, while the y-axis shows the measured capacitance in Farads.

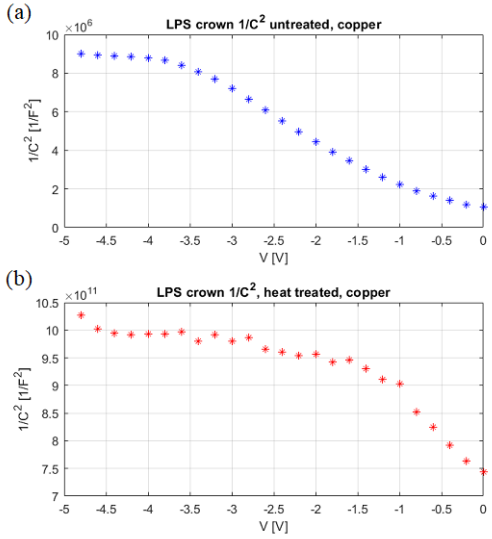

Figure 48: $1/C^2$-curves of the Lower Pulling Speed crown samples: (a) Untreated with P-copper contact; (b) Heat treat with copper contact. The x-axis represents the applied voltage measured in Volts, while the y-axis shows the $1/C^2$ in $1/F^2$.

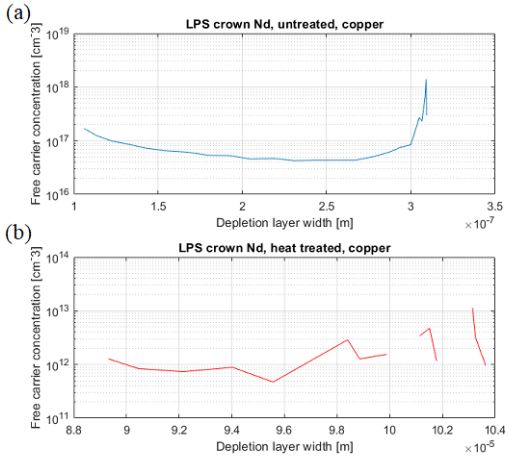

Figure 49: Free carrier concentration curves of the Lower Pulling Speed crown samples: (a) Untreated with copper contact; (b) Heat treated with copper contact. The x-axis represents the depletion layer width in meters, while the y-axis shows the calculated free carrier concentration in m^{-3}.

8.2.4 Higher Pulling Speed crown samples

Similar to their lower pulling speed equivalents, the Higher Pulling Speed crown samples, $CH_{high}D$ and $CU_{high}D$ were only measured in the copper clamp setup, hence Figure 50 shows only two CV-profiles. Next, Figure 51 shows the calculated $1/C^2$-slopes and finally Figure 52 presents the calculated free carrier concentration profile for the two samples.

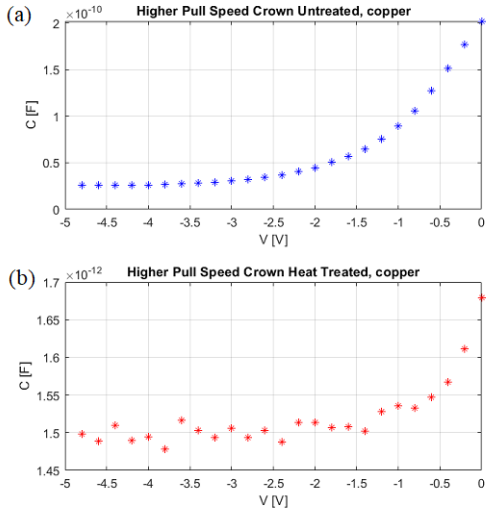

Figure 50: CV-curves of the Higher Pulling Speed crown samples: (a) Untreated with copper contact; (b) Heat treated with copper contact. The x-axis represents the applied voltage measured in Volts, while the y-axis shows the measured capacitance in Farads.

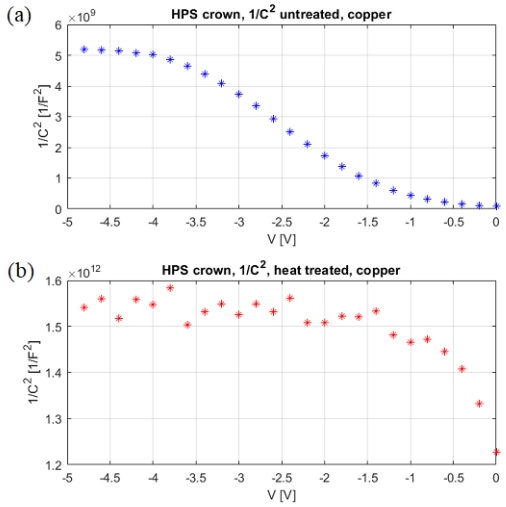

Figure 51: $1/C^2$-curves of the Higher Pulling Speed crown samples: (a) Untreated with P-copper contact; (b) Heat treat with copper contact. The x-axis represents the applied voltage measured in Volts, while the y-axis shows the $1/C^2$ in $1/F^2$.

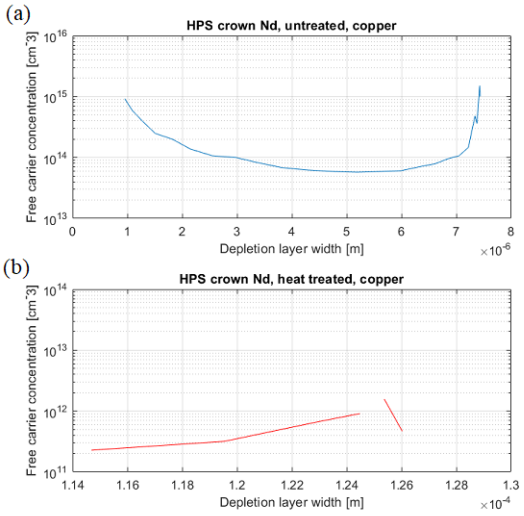

Figure 52: Free carrier concentration curves of the Higher Pulling Speed crown samples: (a) Untreated with copper contact; (b) Heat treated with copper contact. The x-axis represents the depletion layer width in meters, while the y-axis shows the calculated free carrier concentration in m^{-3}.

8.2.5 Test diode

The CV-profile of the test diode is presented in Figure 53.

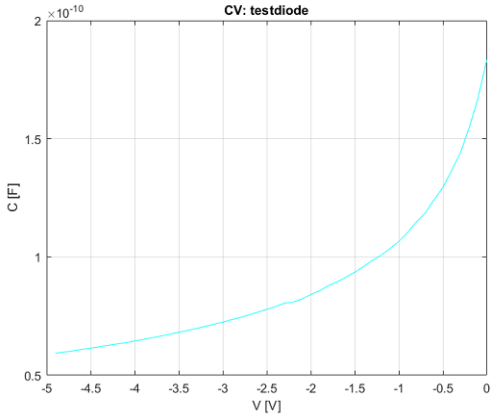

Figure 53: CV-curve of the test diode: the x-axis represents the applied voltage measured in Volts, while the y-axis shows the measured capacitance in Farads.

8.2.6 Clamp test

The result of the test CV-measurement for the setup with clamp directly touching the silicon surface is presented in Figure 54.

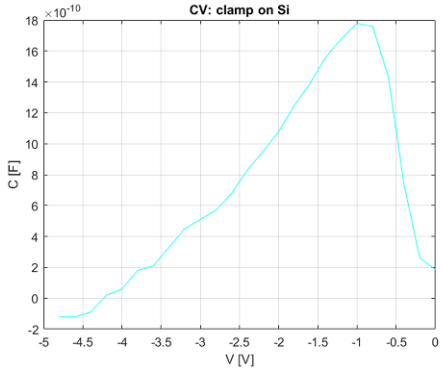

Figure 54: CV-curve of the system where clamp is touching the silicon surface directly: the x-axis represents the applied voltage measured in Volts, while the y-axis shows the measured capacitance in Farads.

8.3 DLTS-measurements

The results presented in this section are the measured the measured capacitance as function of time, and the observed transients for $CU_{low}D$, $CU_{high}D$ and the test diode. As the transients obtained for the two crown samples did not match the theory, the DLTS-measurements could not be started, hence this section will not present any DLTS-spectra. It will be further discussed in Chapter 9.

8.3.1 Lower Pulling Speed crown untreated

Figure 55 presents an image of C vs t curve, obtained for the $CU_{low}D$ sample where a transient is observed. The reason for this curve being presented as an image is that it was not known that the data could be saved in a file.

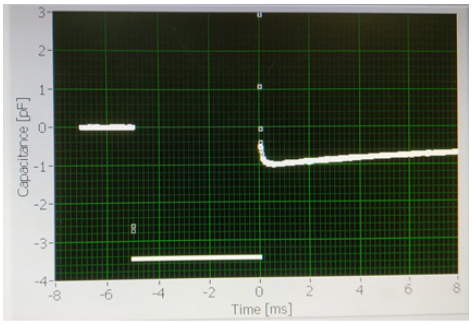

Figure 55: An image of the measured C vs t curve showing a transient for Lower Pulling Speed crown untreated sample. The x-axis shows time measured in ms, while y-axis shows the measured capacitance in pF.

8.3.2 Higher Pulling Speed crown untreated

The C vs t curve obtained for the $CU_{high}D$ is shown in Figure 56 which includes the transient for this sample.

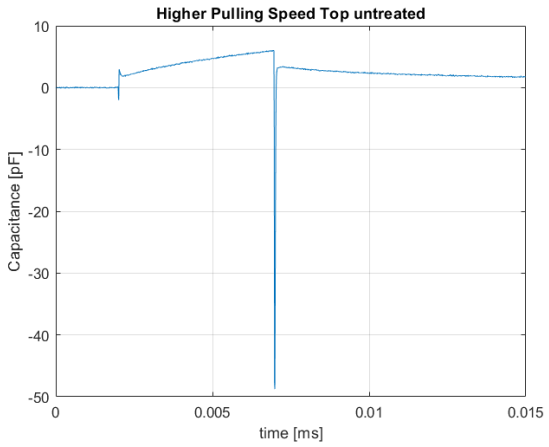

Figure 56: C vs t curve showing a transient for the Higher Pulling Speed crown untreated sample. The x-axis shows time measured in ms, while y-axis shows the measured capacitance in pF.

8.3.3 Test diode

The test diode's C vs t curve is presented in Figure 57 showing the transient profile for this sample.

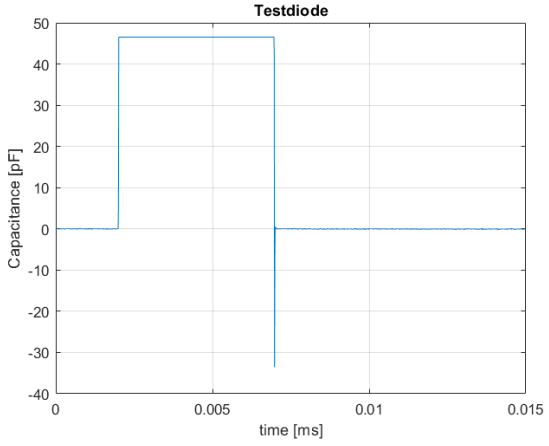

Figure 57: C vs t curve showing a transient for the test diode. The x-axis shows time measured in ms, while y-axis shows the measured capacitance in pF.

8.4 AFM imaging

This section will present the images obtained during the c-AFM experiments.

8.4.1 Lower Pulling Speed Body untreated sample

Figure 58 presents the obtained current map, Z-map and error signal map for $BU_{low}A$ in reverse bias. Note that the maps are not completed due to the lack of contact between the tip and the sample surface. The maps in forward bias are presented in Figure 59.

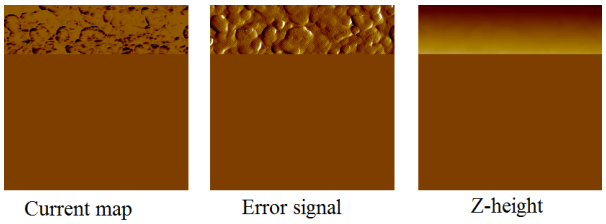

Figure 58: From left to right: current map, error signal map, Z-height map in reverse bias for $BU_{low}A$. The size of the images is 50 μm x 50 μm.

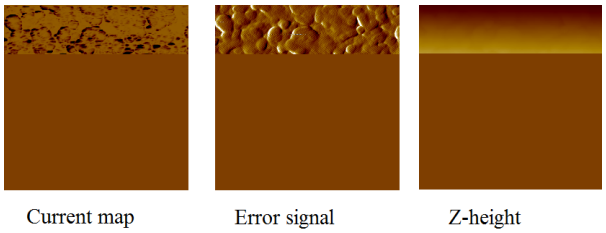

Figure 59: From left to right: current map, error signal map, Z-height map in forward bias for $BU_{low}A$. The size of the images is 50 μm x 50 μm.

8.4.2 Higher Pulling Speed Body heat treated sample

For this sample, a microscopy surface image was obtained in addition to the maps. It is shown in Figure 60. Figure 61 presents the obtained current map, Z-map and error signal map for $BH_{high}A$ in reverse bias. Note that the maps are not completed due to the lack of contact between the tip and the sample surface. The maps in forward bias are presented in Figure 62.

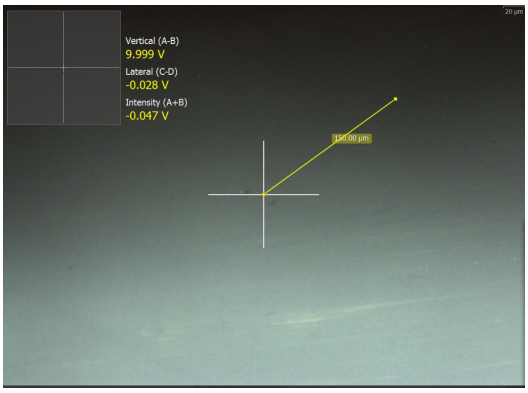

Figure 60: Microscopy image of the sample's surface before the AFM-measurement. Visible scratches are located at the bottom of the image.

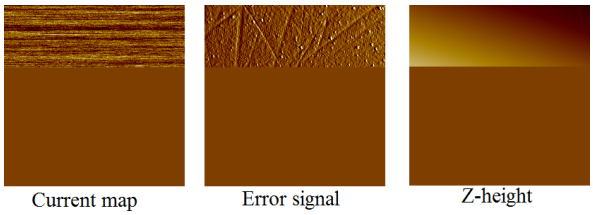

Figure 61: From left to right: current map, error signal map, Z-height map in reverse bias for $BH_{high}A$. The size of the images is 50 μm x 50 μm.

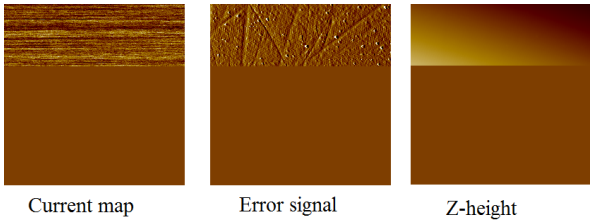

Figure 62: From left to right: current map, error signal map, Z-height map in forward bias for $BH_{high}A$. The size of the images is 50 μm x 50 μm.

8.5 Results from specialization project

This section is presenting the two most important graphs from the specialization project, [1], that are going to be used in the discussion of the obtained results in Chapter 9. In addition, it will also provide two graphs in which the results from the specialization project are compiled with the on/off current ratio for all the eight samples.

8.5.1 Interstitial oxygen content- FTIR

The samples characterized in specialization project, [1], have been previously describe in Chapter 7.2.1 to be 11 cm x 11 cm. The interstitial oxygen content was measured along the same line that was the center of the ingot with 1 cm distance between each measurement. Figure 63 shows the result of those measurement for the four samples before and after heat treatment. Figure 63 (a) shows the result for Higher Pulling Speed ingot samples, where the heat treated samples are represented by the red line, while the samples before heat treatment are represented by the blue line. The crown sample measuring points are represented by the points up to 11 cm distance and the body sample measuring points are represented by the points after the distance of 11 cm.

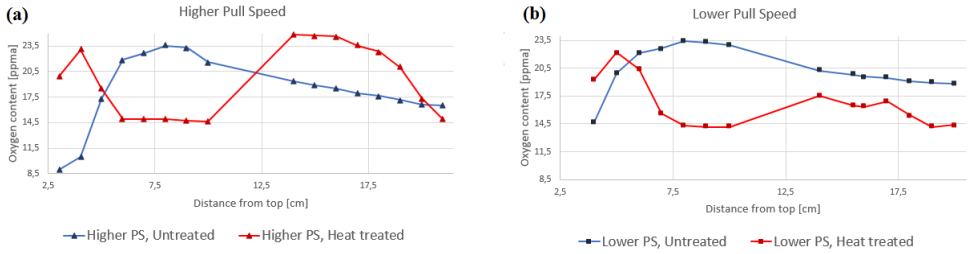

Figure 63: Oxygen content before and after heat treatment for: (a) samples with higher pull speed, (b)samples with lower pull speed.The x-axis shows the distance from the top of the ingot in cm, while the y-axis shows the interstitial oxygen content in ppma; from [1].

8.5.2 Resistivity- FPP

The results of the resistivity measurements before and after heat treatment done using the FPP-technique are presented in Figure 64. The logic behind the presentation of the results is the same as presented in the previous section.

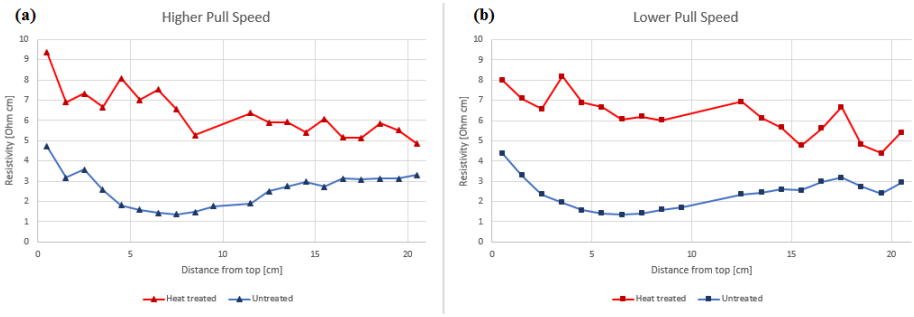

Figure 64: The results of FPP measurements performed after heat treatment. The measurements before and after are set together for: (a) samples with higher pull speed, (b) samples with lower pull speed. The x-axis shows the distance from the top of the ingot in cm, while the y-axis shows the measured resistivity in [Ohm cm^{-}1; from [1].

8.5.3 Current ratio vs. oxygen content

Figure 65 presents the on/off current ratio for each diode prepared using the P-bronze clamp as the function of the interstitial oxygen concentration. The cyan colour represents the body samples, while the crown samples are represented with the magenta colour.

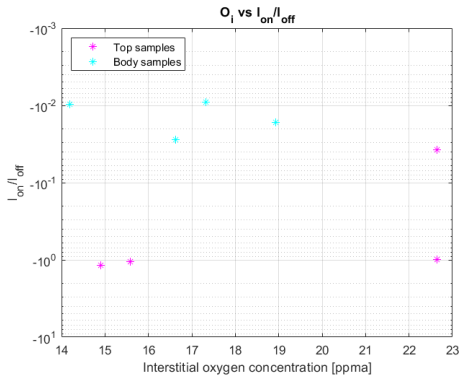

Figure 65: The graph is showing the relationship between the interstitial oxygen (x-axis) and the ratio between on and off current (y-axis). The cyan stars represent the body samples, while the top samples are represented with magenta stars.

8.5.4 Current ratio vs. resistivity

Current ration vs. resistivity relationship is shown in Figure 66, where the cyan stars represent the body samples, while the crown samples are represented by the magenta stars.

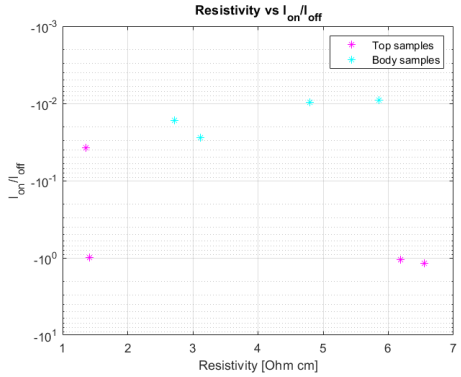

Figure 66: The graph is showing the relationship between the measured resistivity (on the x-axis) and the on-off current ratio (y-axis). The cyan stars represent the body samples, while the top samples are represented with magenta stars.

9 Discussion

The results presented in Chapter 8 are going to be further explained and discussed in this section, following the order in which they were presented, starting with the IV-measurements.

9.1 IV-curves

The first thing to be noticed in the IV-curves presented in the linear scale: Figure 35 (a) and (c), Figure 36 (a), Figure 37 (a) and Figure 38 (a), are the difference in voltage ranges between the P-bronze (from -5 V to 2 V) and the copper curves (from -5 V to 5 V). This is simply due to different parameter settings and it does not effect the shape of the curve. Note that the ideal IV-curve of a diode was previously presented in Figure 13, and the phrase "diode like behaviour" in this chapter is referring to the behaviour presented in this figure.

It can be seen on Figure 35 that both the heat treated and the untreated Lower Pull Speed body samples show diode-like behaviour, as shown in Figure 13, for both the case of P-bronze clamp and the case of copper clamp. There is however, a difference between the cut-in voltage depending on which clamp material is used.

For the case of Higher Pull Speed body samples, presented in Figure 36 it can be seen that again both the heat treated and the untreated sample show diode-like behaviour independent on the clamp material. Interestingly, the cut-in voltage for each of the samples is also the same, indepent on the clamp material. In addition, the values for the case of $BU_{high}D$ are identical in the two different cases.

Lower Pull Speed crown samples, presented in Figure 37 only show diode behavior for the case of copper as clamp material, while for the case of P-bronze as clamp material the samples were showing the Ohmic behaviour. It should be mentioned here that it was the improvement observed on this samples when switching the clamp material to copper, that was the reason for choosing the copper material for all the other samples.

$CU_{high}D$ and $CH_{high}D$, untreated and heat treated crown HPS crown sample, shown in Figure 38, both show the diode-like behaviour for both of the clamp materials. Interestingly, it can be observed that the cut-in voltage for each of the samples seems also to not be dependent on the material choice, similar to what could be observed for the body samples from the same ingot.

In the case of the test diode, the IV-curve presented in Figure 39 shows almost the ideal shape and the value for cut-in voltage is much lower than what

is observed for the diodes prepared in this project.

Figure 40 showing the IV-curve for the case of the copper clamp being in direct contact with silicon surface of the sample $CH_{high}C$. The curve is presenting a diode-like behaviour and the values are almost identical as the one for the case of the diode made with the copper clamp (ideally) touching the gold layer, presented in Figure 38 (c). Also, the cut-in voltage seems to be similar in both graphs. This can lead to a conclusion that perhaps for some of the samples the clamp was in fact in direct contact with silicon surface and not with the Schottky barrier.

In general, it can be observed that the body samples seem to present a more stable behaviour for most of the samples. Some of the heat treated samples showed a more irregular behaviour (more scattering). However, it cannot be concluded if those preliminary comparisons between crown vs. body and heat treated vs. untreated, are certain. This is due to the problem with diode fabrication and material choice.

9.2 CV-profiles

Moving on to the presentation and discussion of the results of CV-measurements presented in Chapter 8.2, Figure 41 will first be discussed. What is important to note here is the difference in the shape of CV-profiles depending on the clamp material used. Comparing the CV-profiles obtained during the measurements to the CV-profile presented in Figure 14, it can be seen that the curves obtained using the copper clamp show a more "ideal-like" behaviour. However, the values for the case of copper are much lower than for the case of P-bronze. Further, looking at Figure 48 it can be seen that the $1/C^2$ slope for the case of the heat treated sample shows a more linear behaviour for the case of copper clamp. The non-linear shape of the curves can mean that the free carrier concentration is not homogeneous. It is true in particular in Figure 43 where the free carrier concentration is not homogeneous. Interestingly, the calculated free carrier concentration seems to be more reliable for the case of using a P-bronze clamp (approx. 10^{16} cm^{-3} for untreated and approx. 10^{15} cm^{-3} for heat treated), even though the CV-profiles and the $1/C^2$-slopes did not seem to look ideal. For the case of copper, the calculated free carrier concentrations (approx. 10^{12} cm^{-3} for untreated and approx. 10^{12} cm^{-3} for heat treated) seem to be too low which is expected when looking at the capacitance values shown in the CV-profiles. Based on the data given by the company, the doping concentration should be in the order of 10^{15}-10^{16} cm^{-3}. Note that the graphs are presenting the free carrier concentration and not the doping concentration.

Higher Pull Speed body samples show almost the same behaviour for the two clamp materials in Figure 44. The capacitance values are also in the same order of magnitude, but lower for the P-bronze clamp. Further, it is interesting to note the linear $1/C^2$-slope for the case of $BU_{high}D$ sample, which could mean

a more homogeneous free carrier concentration. This is somehow confirmed by investigating the free carrier concentration curves presented in Figure 46, especially for the case of P-bronze clamp. As for the other $1/C^2$-slopes and the corresponding free carrier concentration, it is observed that the carrier concentration is not homogeneous. As it could be expected from the low capacitance values, the calculated free carrier concentration from Figure 46 seems to be low for both of the Higher Pull Speed body samples, and they were: approx. 10^{11} cm^{-3} for the case of untreated P-bronze case, approx. $5 \cdot 10^{12}$ cm^{-3} for the untreated copper case, approx. 10^{12} cm^{-3} for the heat treated P-bronze case and approx. 10^{12} cm^{-3} for the heat treated copper case.

As the Lower Pull Speed crown samples were only working diodes when using the copper clamp, it was only possible to measure the CV-profiles for this contact setup and the profiles. Figure 47 shows the CV-profiles for the two samples, where both the untreated and the heat treated sample seem to have the correct shape. However, the values for the heat treated sample are three orders of magnitude lower compared to the untreated sample. The $1/C^2$-slopes from Figure 48 are not linear in either case, meaning that the free carrier concentration would probably be inhomogeneous, which is confirmed by the free carrier concentration profiles in Figure 49. Here, it is interesting to note that the value of free carrier concentration seems to be reliable in the untreated sample (approx. $5 \cdot 10^{16}$ cm^{-3}), while for the heat treated sample it is again too low (approx. 10^{12} cm^{-3}).

Similarly for the Lower Pull Speed crown samples, the crown samples from the Higher Pulling Speed ingot were only measured with the copper clamp due to irregular CV-profiles obtained using the P-bronze clamp, hence Figure 44 consists of two CV-profiles. Interestingly, they show similar behaviour to the Lower Pulling Speed crown samples where the untreated crown sample shows almost an ideal CV-profile with reliable values, while the heat treated sample shows a more irregular behaviour with lower capacitance values. The $1/C^2$-slopes in Figure 51 are also very similar to the ones obtained for the other crown samples, where the untreated one shows a more linear shape. Again, the free carrier concentration profile from Figure 52 of the untreated sample seem to be more homogeneous and the values are also quite meaningful (approx. 10^{14} cm^{-3}). Again, the heat treated sample show very low free carrier concentration (approx. 10^{11} cm^{-3}) due to the low capacitance values.

It is worth commenting the empty regions in the free carrier concentration graphs where the graph is broken. Since the free carrier concentration is calculated according to Equation 8, it can be seen that when the derivative is 0, the equation cannot be calculated. The irregularities and/or flat regions in the $1/C^2$-slopes are therefore the source of the "holes" in the free carrier concentration profiles.

Further, the CV-profile of the test diode shown in Figure 53 seems to be

ideal, similarly to the IV-curve for this sample and the capacitance values are also meaningful. As this was only a test sample, the slope and free carrier concentration was not calculated.

Further, the test CV-profile of the case of the clamp being in direct contact with silicon surface is presented in Figure 54. It is clear that the shape of the curve is rather strange due to the behaviour observed for voltages between -1 V and 0 V. However, what is interesting are the capacitance values being in the same order of magnitude as those found for the cases of the clamp in contact with the Schottky gold contact.

9.3 Transients

Chapter 8.3 presented the obtained transients for three of the samples: $CU_{low}D$, $CH_{low}D$ and the test diode. As mentioned before, the transient of the Lower Pulling Speed untreated crown sample was only saved as an image because it was not known that the data could be saved in a text file that could be later plotted. This was fixed for the two next samples for which the data were plotted in Matlab.

Even though the transient obtained for the $CU_{low}D$ sample was only saved as an image, it is clearly seen that the transient does not fit the expected shape of a transient presented in Figure 15. What is interesting is that the transient obtained for this sample is almost a mirror reflection of the transient presented in Figure 15. This type of transient showing negative capacitance values in the flat region is not widely known or described in literature. A consultation with an expert on the DLTS-technique did not give a concrete answer for this behaviour [63]. It was however suggested that a possible reason for it was some kind overload in the instrument during capacitance measurements, which could be an effect of a large pulse width value applied as listed in Chapter 7.5. To test this hypothesis it was suggested to decrease the pulse width and observe the resulting transient. It was, however not possible to perform this test because of the sudden restrictions imposed by the Italian government due to the Covid-19 crisis.

The other diode that was characterized using SULA was the $CU_{high}D$ for which the transient is presented in Figure 56. Again, the transient does not compile well with the transient presented in Figure 15, however its shape is very different than the one obtained for the previous sample. The strange behaviour here is the shape of the "flat region" of the curve which in this case is not flat, but seems to grow linearly. This graph seems to be more similar to the ideal case. It is however still not something that has been widely described in the literature, so there is no clear answer to why this transient was obtained. Again, it could be related to a possible overload of the equipment during the capacitance measurements. The fact that the transient is bent towards the positive capacitance, a so-called positive transient could be explained by the fact

that it is due to the minority carrier traps, as presented in [64].

Figure 57 shows the measured capacitance as a function of time, obtained for the test diode with the transient, or rather the lack of it. The reason for this is most probably due to lack of deep traps in this diode which are the source of a transient. Here, the flat region is corresponding perfectly with Figure 15. The overall shape to this curve leads to the conclusion that the equipment is working perfectly, hence the problem with the previously described curves lies mostly within poor sample preparation.

The reason for presentation of C vs t curves for only two diodes that were prepared in this work, is that the other six diodes have shown similar behaviour to the one presented in Figure 55, even though their corresponding CV-profiles were different to the ones of $CU_{low}D$. In addition, investigating the IV-curves and the CV-profiles of all the diodes gave a perhaps false idea that only $CU_{low}D$ and CU_{high} were good enough diodes that could be used for the DLTS analysis, which was not the case.

It cannot be easily concluded what was the exact reason for the obtained results. One possible reason is gold layer was too thin and hence point Schottky contact was made between the clamp and silicon, and not clamp and gold (this could be supported by the values obtained for the test IV- and CV-measurement when clamp was in contact with the surface).

The suggested approach towards new diode fabrication, was to use the bi-component silver paste to fix the contact between the clamp and the evaporated gold layer on top of the samples. In addition, instead of the copper clamp, it was suggested to try using a thin gold wire which probably would not be detached while going to lower temperatures. The new setup is presented in Figure 67.

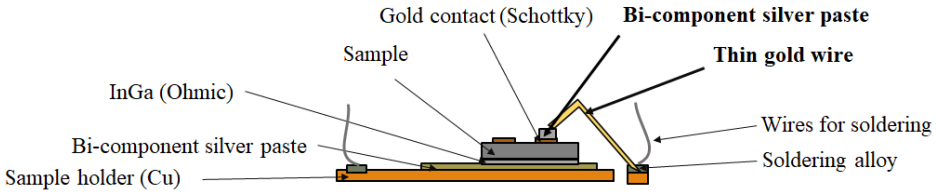

Figure 67: Schematic illustration of the new setup with bi-component silver paste between the gold contact and the clamp to ensure better stability.

9.4 c-AFM imaging

Now, for AFM-imaging, only two samples were investigated, both from the body regions, namely $BU_{low}A$ and $BH_{high}A$. The achieved results are not meaningful for either of the samples. First, the LPS body untreated sample is going to be presented. The current, error signal and Z-height maps in reverse and forward bias are presented in Figure 58 and Figure 59, respectively. As it was mentioned, the full maps were not obtained because the measurement was stopped manually due to an observation that the maps were not meaningful. Hence, only the upper line of the maps is of interest for this discussion. For both current and error signal maps a sort of grain structures can be observed. However, this does not represent the actual structure and/or features of the material and it is simply an artifact of the measurement, related to the surface roughness [13]. This is due to some irregularities on the sample surface that are imaged in the current maps as regions of improved electrical properties (black regions). Figure 68 shows the reason behind this; at position (2) the proportion of the tip-surface area in close proximity to the surface is larger than in position (1), which will increase the measured current [13]. Oliver et al. have previously explained that imaging the same features in both topography (error signal map) and electrical mode (current map) should not be taken for certain due to this exact problem [13]. Hence, it is concluded that the results for this sample are not meaningful, as the maps do not show any relevant features besides the ones described above. The sample is therefore showing homogeneous resistivity. This is most probably due to the presence of the native oxide layer on the surface, as the samples were not etched before the AFM-imaging experiments.

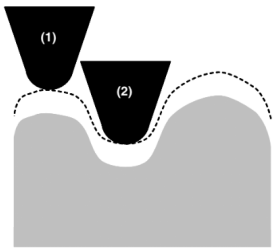

Figure 68: Contact area between tip and surface in close proximity to the surface is greater in position (2) than in position (1), giving the reason for the increase in the measured current, from [13].

Figure 60 shows the micrograph of the sample surface taken before the measurements on sample $BH_{high}A$. Some horizontal lines are observed on the surface and those are probably some scratches due to the mechanical polishing. The current, error signal and Z-height maps for this sample in reverse and forward bias are presented in Figure 61 and Figure 62, respectively. Here, there are differences between the features observed on the error signal and current maps.

However, they do not seem to be reliable. That is because of the "features" imaged in the current map. The features displayed there are simply a noise signal. The error signal map shows some lines that could possibly connected to some scratches on the surface, however this is not certain. As for the other sample, an etching process should be performed before the AFM-investigation.

In addition to the presence of the native oxide layer, there was also another problem with AFM-measurements. As those are measurements done at very high magnification, one should have an idea about the possible defects prior to measurement. This could be done by performing an optical microscopy analysis of etched samples in order to map the interesting regions that could be further investigated under AFM.

9.5 Previous results

Moving further to the results from the specialization project presented in Chapter 8.5, Figure 63 showing the interstitial oxygen content before and after heat treatment, is of great importance in the discussion of the results obtained in this thesis. The most important here is the difference in changes of the O_i concentration after heat treatment for the two different pulling speeds. While for the case of higher pulling speed ingot, the O_i concentration in body sample has increased, the contrary is observed for the lower pulling speed ingot where the concentration is decreased. The possible reasons for this were discussed in [1], one of which being that there might be a critical value of the O_i concentration that decides whether the heat treatment will lead to a decrease or an increase in the interstitial oxygen content. In addition, it was also suggested that this behaviour was probably related to the size and density of the oxygen nuclei. Further, it was suggested that it is the correlation between thermal donor formation during heat treatment and the initial interstitial oxygen concentration that is the reason for this behaviour; the TDs can grow on behalf on the interstitial oxygen concentration. As it was mentioned in Chapter 5.1 the TDs formation will for some temperature regimes, decrease the O_i content, while for higher temperatures the precipitates could be dissolved, increasing the O_i concentration [39].

Further, Figure 64 is presenting the resistivity values for the samples before and after heat treatment. Overall, an increase in resistivity after heat treatment is observed and the samples seem to follow similar pattern. The increase in resistivity is linked to the increase in the concentration of donor species after heat treatment. The irregularities in the graph can be explained by the sample preparation of the heat treated samples which contained of simply grinding away the oxide layer formed during heat treatment.

As the first prepared diodes using P-bronze were showing very irregular IV-characteristics, it was of interest to examine if there might be a correlation

between the interstitial oxygen content and this type of behaviour. For that reason the on/off current ratio for each diode was plotted against the interstitial oxygen content from Figure 63, where the I_{on}/I_{off} ratio was calculated by the following formula:

$$I_{on}/I_{off} = \frac{I(2V)}{I(-2V)}. \tag{26}$$

The general idea is that if the ratio is 1 or close to 1, the diode is showing an Ohmic like behaviour, and the further the ratio values is from 1, the better diode like behaviour is obtained [65]. Figure 65 shows the result of this analysis and it can be observed that there is no clear correlation between the interstitial oxygen content and the on/off current ratio. It is also observed that while all body samples were working as diodes, three out of four crown samples were not. Note that this analysis was obtained in the P-bronze clamp configuration.

It was also of interest to investigate whether or not the resistivity measured in specialization project and shown in Figure 64, could be correlated to the on/off current ratio measured in the P-bronze clamp configuration. The result of this analysis is presented in Figure 66 where again, no clear correlation was found.

The effect of heat treatment on thermal donors formation and their affect on the electrical properties has been previously presented in Chapter 5. It is well known that the thermal donors would influence the electrical properties of the material, however it is not clear if the irregularities observed for the measurements on the heat treated samples can be explained by the possible TDs formation. It can be related to the strain inside the crystal upon the formation of defects and oxygen precipitates [66].

If the relative difference in the free carrier concentration between the untreated and heat treated samples would correct, it could be explained by the formation of oxygen precipitates during heat treatment which would strongly affect the donor effect and hence the calculated free donor concentration would be lower.

The literature review in Chapters 5.1 and 5.2 have presented some results that could also be obtained in this work if the problems with the diode fabrication could be solved. The obtained DLTS-spectra could reveal differences in the trap levels for both heat treated vs. untreated samples, body vs. crown samples and higher vs. lower pulling speed samples. A comparison between the different positions, pulling speeds and treatments could help with understanding the mechanisms behind the thermal donor and precipitate formation during heat treatment.

10 Conclusion

Although the work presented in this thesis was not finished according to the original plan, the achieved results have provided a very interesting source for the discussion that has led to some very important points that are going to be summarized in this chapter.

First of all the important findings of this work is that the choice of the clamp material and sample preparation are crucial for the diode performance. What may seem like a trivial conclusion, it is actually a very important feature to be noted, as the graphs and values obtained for the two different diode configurations are very different from each other. It has become clear that each step of the diode preparation should be performed carefully, but perhaps the most important steps for the eventual diode performance would be the etching and gold evaporation steps. It is believed that a thicker gold layer could improve the diode stability and sensitivity upon making of the electrical contacts.

Further, no clear correlation between the interstitial oxygen content and the diode performance has been found, leading to the conclusion that the O_i content does not affect the electrical properties studied in this work. However, one should be critical in drawing a certain conclusion based on the results presented in Chapter 8, as their reliability is rather questionable.

Another possible conclusion of the obtained results is related to the measurements obtained for the heat treated samples that show a more unstable behaviour. Again, it is not clear if this is solely related to the mechanisms of TDs formation, oxygen precipitation etc. during the heat treatment experiment or if this should be blamed on the poor sample preparation. This conclusion is therefore not to be taken as certain.

Summarizing, it is not clear what the exact mechanisms behind the strange behaviour of the samples selected and investigated in this work, can be related to. However, a good and stable method for sample preparation is a result of this project work and it should not be undervalued since as of now on, the diode preparation should be a more easy step towards obtaining more reliable data for this kind of characterization.

11 Further work

Due to the global Covid-19 crisis the work in this master's thesis could not be continued and finished as planned. As Italy was one of the most afflicted countries, the work here was interrupted abruptly. There was a hope of returning back to the usual way of research work. It has however, proved itself to be a too optimistic approach. This section is therefore meant to present to the reader the further work that was planned and also present some ideas for further research.

As mentioned in Chapters 8 and 9, the obtained results are not satisfactory due to both poor sample preparation and some problems with the equipment. Once a possible solution to those problems was found, the Italian government has ordered a strict lockdown, which has affected the research in such a way that it was no longer possible to enter the university area as everyone has been asked to stay at home and go out only to buy the essential products. That is why it was not possible to implement the solutions that could have helped with finishing the project.

First, the solution to the problems with diodes preparation will be presented. As two of the diodes were working properly and gave quite reasonable results in room temperature, it was clear that a mistake must have been made during the sample preparation. This was confirmed by running tests on a test diode which gave reasonable results in both room temperatures and lower temperatures. A new approach for sample preparation was then suggested by a DLTS-expert from CNR in Parma, which was supposed to help with stability of the diodes at all temperatures [63]. It was previously presented in Chapter 9.

Before applying the silver paste on top of the gold contact, it was also suggested to repeat the etching and gold evaporation step since the gold layer could have been damaged due to clamp mounting. After a successful gold evaporation the bi-component silver paste would be applied on top of the contact. Then a thin gold wire would be put on top of the bi-component silver paste with one end, while other end would be placed on the sample holder using bi-component silver paste. Further, the diodes produced using this setup would be placed in the oven and heated up to 80 °C to ensure stability of the system.

Such prepared diodes should work in different temperatures, so the next step would be to test the system, first at room temperature using the Faraday box. The test should consist of measuring both the IV- and CV-curves, as well as the C vs t- curve using SULA. If the problems with SULA, discussed in Chapter 9 would appear again, it was suggested to reduce the pulse width. Further, if all the test would give reasonable results, the DLTS-measurements could be performed individually for each sample.

As mentioned earlier in this thesis, in addition to the measurements of electrical properties, it was also planned to do conductive AFM imaging. The

procedure was described in Chapter 7.7 and it was mentioned that the experiment did not go as expected. A possible solution to the problems encountered during the experiment, would be to perform a sufficiently long etching of all the samples, following the procedure described in Chapter 7.2.3. The imaging should be performed quite fast after the etching, so that the oxide layer is not too thick for the probe to penetrate it. Ideally, the samples should be etched one by one and investigated immediately after the etching. This could however become problematic since the HF acid would be used for the process. Since the procedures for working with this acid are very strict and one should not be exposed to it for too long the experiments should be planned precisely with adequate time in between the experiments. Another improvement for the AFM-imaging would be to perform a preliminary optical microscopy analysis of the etched sample surface; this could reveal the areas of interest for further investigation under AFM, such as stacking faults, pits etc.

In addition to these two experiments, it was also planned to do more experimental work after the return to Norway. However, due to complications with finding a flight back, the return kept on being postponed for more than a month after the decision of return was made. This resulted in too little time for any form of experimental work. The next paragraph explains the initial plan for the experimental work at NTNU.

As seen in Figure 19 initially three vertical slices were obtained from cutting of the ingots during the work on specialization project [1]. Out of those three, the two closest to center of the ingot were used in either the specialization project, the master's thesis or both. The last remaining slice was thought to be used for investigation of the surface by microscopy, possibly optical and SEM. For this purpose the vertical slice should be cut by laser to achieve slices similar to the ones used in the specialization project (11 x 11 cm). Then, the samples would be grinded and polished to achieve the thickness of around 2 mm. The microscopy experiments on untreated samples could now be performed to investigate any possible defects at the sample surface. Further, it was planned to perform the same heat treatment experiment as in specialization project [1]. The steps of the heat treatment procedure are presented in Table 5.

Table 5: Heat treatment process steps, from [1].

Heating from temperature [°C]	Heating to temperature [°C]	Time step [min]
Room Temperature	750	50
750	750	240
750	1050	30
1050	1050	960
1050	500	110
500	121	END

The heat treated samples would then be etched again and investigation under the microscope would be performed again. This would be done in order to see whether or not the heat treatment affects the defects in a significant way. The results of this type of investigation could be compared to the findings made by AFM-imaging.

In addition to the work that has been planned, possibilities for further research have also been discussed. Assuming that the new suggested approach of diode preparation would be working, a few more possible characterization techniques have been proposed, such as impedance spectroscopy to obtain the electrical impedance as a function of frequency.

Another interesting characterization technique that could be used for investigation of oxygen presence in the material, would be the AFM-IR technique which can be seen as a combination of AFM and FTIR. Using this technique, it would be possible to investigate the infrared absorption to identify the chemical composition inside the sample. Combining FTIR and AFM could possibly reveal the exact placing and size of oxygen precipitates and related defects.

An experimental approach towards investigation of thermal donors would also be very interesting in connection to the topic of this thesis to combine it with the literature review presented here. It would be interesting to see if it is possible to find a clear correlation between the thermal donors formation, distribution, amount, the ingot's thermal history and the pulling speed used during ingot production.

It would also be of great interest to perform this type of characterization presented in both the specialization project and the master's thesis on more samples of different origin to gather enough data to perform a statistical analysis. For that, more samples produced with the same pulling speed would be needed. This type of statistical data gathering could also be useful to find a correlation between the initial size of oxygen precipitates.

Overall, it is clear that this topic is very interesting and of industrial relevance. Further investigation of the correlation between pulling speed, material's properties and oxygen presence is needed in order to improve the monocrystalline silicon solar cell technology.

12 Acknowledgements

In addition to the people I already placed my thanks to in the Preface, I would also like to acknowledge some people from the academic staff at both NTNU and University of Bologna and this section is designated to thank those that were involved in the project. I would also like to acknowledge some of the people that had been helping me during my specialization project from both NTNU and SINTEF. Without their help then, I would not be able to continue with my master's thesis. In addition, and maybe most importantly, I would like to greatly thank Yu Hu from Norsun AS who provided the material investigated in both the specialization project and the master's thesis and also for his input to the research.

As the experimental work presented in this thesis was fully performed at the University of Bologna, I would like to acknowledge some of the academic staff that have been of great help during my stay here. First of all, I would like to deeply thank my "guardian" Giovanni Armaroli whose help was crucial for the laboratory work. I will forever cherish our long lab sessions during which we tried to find the reasons for why things did not work in the way they should. Next, I would like to thank Matteo Verdi for spending his free time on designing and producing the sample holder for polishing. Further, to Ferdinand Lédée for sharing his deep chemistry knowledge with me when I needed it for my project. Next, to Francesco Decataldo and Luca Possanzini I would like to thank for their time spent with me in the evaporation lab. Also, to Andrea Ciavatti, I need to express my deepest gratitude for the countless times he helped us with etching of the samples, figuring out the problems we encountered etc. Finally to Tobias Cramer I would like to thank for his lectures on the AFM-technique and his help during the lab sessions in the AFM-lab. And to everyone and every single one of the people I mentioned here, I would like to place a special thank you for always making me feel welcome.

As mentioned, I would also like to thank some of the staff at my home university and SINTEF Materials and Chemistry. From SINTEF many thanks to Birgitte Karlsen, Pål Tetlie, Irene Bragstad and John Atle Bones for their help with the preparation of the samples and for explaining to me the characterization techniques and allowing me to use their equipment. From NTNU I would like to thank Jochen Busam, Rania Hendawi, Bartlomiej Gawel and Berit Vinje Kramer for sharing with me their knowledge on the equipment and characterization techniques and their time spent with me in the labs. At the end, I would like to acknowledge also Maren Elise Juul, the student advisor at the Department of Material Science and Engineering for her help during those difficult times of uncertainty and her help towards finishing this project.

I would love to thank each and everyone of these people personally and I hope our paths will cross more than once in the future.

References

[1] G. K. Warden. *Effect of Pulling Speed on oxygen distribution in Czochralski silicon ingots*. Tech. rep. Department of Materials Science, Norwegian University of Science and Technology, 2020.

[2] V. K. Khanna. "Physical understanding and technological control of carrier lifetimes in semiconductor materials and devices: A critique of conceptual development, state of the art and applications". In: *Progress in Quantum Electronics* 29.2 (2005), pp. 59–163.

[3] J. Nelson. "The Physics of Solar Cells". In: *The physics of solar cells, by Jenny Nelson. London: Imperial College Press, 2003* 57 (Jan. 2003).

[4] S. Meroli. URL: `https://meroli.web.cern.ch/Lecture_silicon_floatzone_czochralski.html`.

[5] G. Müller et al. "Study of oxygen transport in Czochralski growth of silicon". In: *Microelectronic Engineering* 45.2 (1999), pp. 135–147.

[6] W. Lin and K. E. Benson. "The Science and Engineering of Large- Diameter Czochralski Silicon Crystal Growth". In: *Annual Review of Materials Research* (1987).

[7] W. C. O'Mara, R. B. Herring, and L. P. Hunt. *Handbook of semiconductor silicon technology*. 1990.

[8] L. Válek and J. Šik. "Defect Engineering During Czochralski Crystal Growth and Silicon Wafer Manufacturing". In: *Modern Aspects of Bulk Crystal and Thin Film Preparation*. Ed. by Nikolai Kolesnikov and Elena Borisenko. Rijeka: IntechOpen, 2012. Chap. 3.

[9] V. V. Voronkov and R. Falster. "Vacancy-type microdefect formation in Czochralski silicon". In: *Journal of Crystal Growth* 194.1 (1998), pp. 76–88.

[10] M. Grundmann. *The Physics of Semiconductors*. 2016.

[11] A. Khan and Y. Masafumi. "Deep Level Transient Spectroscopy: A Powerful Experimental Technique for Understanding the Physics and Engineering of Photo-Carrier Generation, Escape, Loss and Collection Processes in Photovoltaic Materials". In: 2015.

[12] T. Cramer. *Lecture notes in Atomic Force Microscopy*. Jan. 2020.

[13] R.A. Oliver. "Advances in AFM for the electrical characterization of semiconductors". In: 71.7 (June 2008), p. 076501.

[14] United Nations. *Sustainable Development Goals*. URL: `https://www.un.org/sustainabledevelopment/sustainable-development-goals/`.

[15] M.H. Shubbak. "Advances in solar photovoltaics: Technology review and patent trends". In: *Renewable and Sustainable Energy Reviews* 115 (2019).

[16] A. Jäger-Waldau. *PV Status Report 2019*. Nov. 2019.

[17] Fraunhofer Institue for Solar Energy Systems. *Photovoltaics Report*. 2020. URL: https://www.ise.fraunhofer.de/content/dam/ise/de/documents/publications/studies/Photovoltaics-Report.pdf.

[18] "Front Matter". In: *Handbook of Photovoltaic Science and Engineering*. John Wiley & Sons, Ltd, 2011, pp. i–xxxii.

[19] G. K. Teal and E. Buehler. "Growth of Silicon Single Crystals and Single Crystal Silicon p-n Junctions". In: *87* (1952).

[20] A. E. Brooks. "Chapter 18 - Solar Energy: Photovoltaics". In: *Future Energy (Second Edition)*. Ed. by Trevor M. Letcher. Second Edition. Boston: Elsevier, 2014, pp. 383–404.

[21] L. Arnberg, M. Di Sabatino, and E. J. Øvrelid. "State-of-the-art growth of silicon for PV applications". In: *Journal of Crystal Growth* 360 (2012). 5th International Workshop on Crystal Growth Technology, pp. 56–60.

[22] W. C. Dash. "Growth of Silicon Crystals Free from Dislocations". In: *Journal of Applied Physics* 30.4 (Apr. 1959), pp. 459–474.

[23] V. V. Voronkov. "The mechanism of swirl defects formation in silicon". In: *Journal of Crystal Growth* 59.3 (1982), pp. 625–643.

[24] V. V. Voronkov and R. Falster. "Grown-in microdefects, residual vacancies and oxygen precipitation bands in Czochralski silicon". In: *Journal of Crystal Growth* 204.4 (1999), pp. 462–474.

[25] Y. Hu. "Characterization of Defects in N-type Cz Silicon for Solar Cells". In: 2012.

[26] Friedrich J. et al. "Considerations on the limitations of the growth rate during pulling of silicon crystals by the Czochralski technique for PV applications". In: *Journal of Crystal Growth* (2019).

[27] R. Falster, V. Voronkov, and F Quast. "On the Properties of the Intrinsic Point Defects in Silicon: A Perspective from Crystal Growth and Wafer Processing". In: *phys. stat. sol* 222 (Nov. 2000).

[28] J. Paloheimo. "Chapter 3 - Properties of Silicon Crystals". In: *Handbook of Silicon Based MEMS Materials and Technologies (Second Edition)*. Ed. by Markku Tilli et al. Second Edition. Micro and Nano Technologies. Boston: William Andrew Publishing, 2015, pp. 56–85.

[29] H. J. Möller. "New Materials: Semiconductors for Solar Cells". In: *Materials Science and Technology*. American Cancer Society, 2013.

[30] W. Wijaranakula. "Formation kinetics of oxygen thermal donors in silicon". In: *Applied Physics Letters* 59.13 (1991), pp. 1608–1610.

[31] V. Cazcarra and P. Zunino. "Influence of oxygen on silicon resistivity". In: *Journal of Applied Physics* 51.8 (1980), pp. 4206–4211.

[32] C. S. Fuller et al. "Resistivity changes in silicon single crystals induced by heat treatment". In: *Acta Metallurgica* 3.1 (1955), pp. 97–99.

[33] A. Kanamori and M. Kanamori. “Comparison of two kinds of oxygen donors in silicon by resistivity measurements”. In: *Journal of Applied Physics* 50.12 (1979), pp. 8095–8101.

[34] M. Bruzzi et al. “Thermal donors formation via isothermal annealing in magnetic Czochralski high resistivity silicon”. In: *Journal of Applied Physics* 99.9 (2006), p. 093706.

[35] J. Veirman et al. “A Fast and Easily Implemented Method for Interstitial Oxygen Concentration Mapping Through the Activation of Thermal Donors in Silicon.” In: *Energy Procedia* 8 (2011). Proceedings of the SiliconPV 2011 Conference (1st International Conference on Crystalline Silicon Photovoltaics), pp. 41–46.

[36] W. Kaiser, H. L. Frisch, and H. Reiss. “Mechanism of the Formation of Donor States in Heat-Treated Silicon”. In: *Phys. Rev.* 112 (5 Dec. 1958), pp. 1546–1554.

[37] K. Torigoe and T. Ono. “Formation of thermal donor enhanced by oxygen precipitation in silicon crystal”. In: *AIP Advances* 10.4 (2020), p. 045019.

[38] W. Keller and Wünstel K. “Thermal donors in silicon: Consistent interpretation of Hall-effect and capacitance transient spectroscopy”. In: *Applied Physics* 31 (1983), pp. 9–12.

[39] G. Pensl et al. “New oxygen donors in silicon”. In: *Applied Physics* 48 (1989), pp. 49–57.

[40] S. A. McQuaid et al. “Oxygen loss during thermal donor formation in Czochralski silicon: New insights into oxygen diffusion mechanisms”. In: *Journal of Applied Physics* 77.4 (1995), pp. 1427–1442.

[41] Y. L. Huang et al. “The lower boundary of the hydrogen concentration required for enhancing oxygen diffusion and thermal donor formation in Czochralski silicon”. In: *Journal of Applied Physics* 98.3 (2005), p. 033511.

[42] Y. Miyamura et al. “Do thermal donors reduce the lifetimes of Czochralski-grown silicon crystals?” In: *Journal of Crystal Growth* 489 (2018), pp. 1–4.

[43] E. Olsen et al. “Spectral Characteristics and Spatial Distribution of Thermal Donors in n-Type Czochralski-Silicon Wafers”. In: *Physica Status Solidi (a)* 217.6 (2020), p. 1900884.

[44] Jiyang Li et al. “Effects of oxygen related thermal donors on the performance of silicon heterojunction solar cells”. In: *Solar Energy Materials and Solar Cells* 179 (2018), pp. 17–21.

[45] I. Kolevatov et al. “Oxygen-related defects: minority carrier lifetime killers in n-type Czochralski silicon wafers for solar cell application”. In: *Physica Status Solidi.C: Current Topics in Solid State Physics* 12.8 (Aug. 2015), pp. 1108–1110.

[46] E V Astrova et al. “Process induced deep-level defects in high purity silicon”. In: *Semiconductor Science and Technology* 13.5 (May 1998), pp. 488–495.

[47] J. H. Evans-Freeman et al. “High resolution deep level transient spectroscopy applied to extended defects in silicon”. In: *Journal of Physics: Condensed Matter* 17.22 (May 2005), S2219–S2227.

[48] D. Cavalcoli et al. “Micro-and nano-structures in silicon studied by DLTS and scanning probe methods”. In: *Semiconductors* 41 (Apr. 2007), pp. 421–426.

[49] I. Capan et al. “Vacancy-related defects in n-type Si implanted with a rarefied microbeam of accelerated heavy ions in the MeV range”. In: *Nuclear Instruments and Methods in Physics Research.Section B.Beam Interactions with Materials and Atoms* 372 (Apr. 2016), pp. 156–160.

[50] Y. Huang et al. “A DLTS study on plasma-hydrogenated n-type high-resistivity magnetic Cz silicon”. In: *Journal of Materials Science: Materials in Electronics* 18 (July 2007).

[51] H. Nishikawa et al. “Formation of Grown-in Defects during Czochralski Silicon Crystal Growth”. In: *Japanese Journal of Applied Physics* 36.Part 1, No. 11 (Nov. 1997), pp. 6595–6600.

[52] S. Umeno et al. “Dependence of Grown-in Defect Behavior on Oxygen Concentration in Czochralski Silicon Crystals”. In: *Japanese Journal of Applied Physics* 38.Part 1, No. 10 (Oct. 1999), pp. 5725–5730.

[53] W. Düngen et al. “Thermal evolution of hydrogen related defects in hydrogen implanted Czochralski silicon investigated by Raman spectroscopy and atomic force microscopy”. In: *Journal of Applied Physics* 100.3 (2006), p. 034911.

[54] H. Miwa et al. “Conductive Atomic Force Microscopy Measurements of Localized over Dark Current along Pyramidal Ridge Lines of Intrinsic Hydrogenated Amorphous Silicon Layer on Textured Crystalline”. In: *MATERIALS TRANSACTIONS* (Jan. 2017).

[55] F. Giannazzo et al. “Impact of Stacking Faults and Domain Boundaries on the Electronic Transport in Cubic Silicon Carbide Probed by Conductive Atomic Force Microscopy”. In: *Advanced Electronic Materials* 6.2 (Jan. 2020), p. 1901171.

[56] P. Bampoulis et al. “Local Conduction in MoxW1–xSe2: The Role of Stacking Faults, Defects, and Alloying”. In: *ACS Applied Materials & Interfaces* 10.15 (2018). PMID: 29578328, pp. 13218–13225.

[57] W. Shockley. “The Theory of p-n Junctions in Semiconductors and p-n Junction Transistors”. In: *Bell System Technical Journal* 28.3 (1949), pp. 435–489.

[58] Keithley. “User’s Manual Model 3321 LCZ Meter”. In: *Keithley Instruments Inc.* ().

[59] A. Bouaicha et al. “Study and design of a controlled oscillator for an embedded system to measure the complex impedance of PEM fuel cell”. In: *2017 18th International Conference on Sciences and Techniques of Automatic Control and Computer Engineering (STA)*. Dec. 2017, pp. 173–178.

[60] *Physics of Semiconductor Devices*. John Wiley and Sons, Ltd, 2006.

[61] *Semiconductor Physical Electronics*. Springer-Verlag New York, 2006. Chap. 6.

[62] Ch. Pan et al. “History and Status of the CAFM”. In: *Conductive Atomic Force Microscopy*. John Wiley and Sons, Ltd, 2017. Chap. 1, pp. 1–28.

[63] *Private conversation with Enos Gombia*. Mar. 2020.

[64] I. Khan et al. “Study of defects in polycrystalline CdTe using DLTS”. In: June 2017, pp. 1–4.

[65] T.S. Natarajan. “16 - Functional nanofibers in microelectronics applications”. In: *Functional Nanofibers and their Applications*. Ed. by Qufu Wei. Woodhead Publishing Series in Textiles. Woodhead Publishing, 2012, pp. 371–410.

[66] V. Lang et al. “Spin-dependent recombination in Czochralski silicon containing oxide precipitates”. In: *Journal of Applied Physics* 111.1 (2012), p. 013710.