Master's thesis

NTNU
Norwegian University of Science and Technology
Faculty of Information Technology and Electrical Engineering
Department of Electric Power Engineering

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Design Considerations and Modeling of a VSC Assisted Resonant Current DC Circuit Breaker for MVDC Applications

Master's thesis in Energy and Environmental Engineering
Supervisor: Dimosthenis Peftitsis
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Preface and Acknowledgment

This master's thesis completes my MSc degree in Energy and Environmental Engineering at the Norwegian University of Science and Technology (NTNU). It has been carried out at the Department of Electric Power Engineering during the spring semester of 2020. The thesis investigates the voltage source converter assisted resonant current circuit breaker (VARC-CB) for medium-voltage DC (MVDC) applications. The VARC-CB was found to be a particularly interesting and promising concept when studying different MVDC circuit breaker designs in my specialization project work [1] during the fall semester of 2019.

I would like to thank my supervisor, Associate Professor Dimosthenis Peftitsis, for providing guidance and valuable input throughout my work, and for pushing and motivating me. I would also like to express my gratitude to my co-supervisor, PhD Candidate Andreas Giannakis, for always being available for questions and discussion, for believing in my work, and for spending numerous of hours helping me with my simulation model. I am also grateful to Professor Kaveh Niayesh for showing interest in my project, and for providing me with insights into the area of vacuum interrupters.

I would like to thank my mom and brother for great support and patience, in particular during my final week of thesis writing. I would also like to thank my fellow students at NTNU, who have made my years in Trondheim unforgettable. A particular thanks goes to Mona Martinsen and Nina Lindholm for being fantastic flatmates during the special and challenging spring 2020 semester. Finally, a huge thanks goes to Sigrid Sollie Kornstad for great help with proofreading my thesis.

Mathilde Bergerskogen

Oslo, June 2020

Abstract

Medium-voltage DC (MVDC) power grids offer many beneficial features compared to the medium-voltage AC (MVAC) counterpart, and are considered well-suited for a wide range of application areas. However, one of the main hindrances towards a widespread of MVDC power grids is associated with the handling of short-circuit (SC) faults. In particular, the lack of high-performance MVDC circuit breakers (CBs) is a key challenge. To address this barrier, the main purpose of this master's thesis is to investigate a particularly interesting and promising DC circuit breaker (DCCB) concept: the voltage source converter (VSC) assisted resonant current circuit breaker (VARC-CB). The VARC-CB is originally proposed for high-voltage DC (HVDC), however this thesis investigates the VARC-CB concept for MVDC applications.

The thesis studies and analyzes the MVDC VARC-CB in detail. A thorough theoretical foundation is given, exploring MVDC power grids and their SC fault protection. Furthermore, operating principles, features, and subcomponents of a variety of DCCB concepts suggested in literature are examined, with a special focus on the VARC-CB. This creates a basis for the subsequent in-depth analytical investigation of the MVDC VARC-CB. The analysis takes several design principles and component limitations into account, upon which a full set of design strategies are derived. Furthermore, a complete, parameterized Simulink® simulation model of the VARC-CB concept employed in an MVDC power grid is developed, where the component-level model of the MVDC VARC-CB is parameterized using the derived design equations. Through simulations, the analytical investigations, the proposed design strategies, and the developed simulation model are validated. Weaknesses and shortcomings of the analysis and modeling processes are pointed out and discussed, and possible revisions are proposed. In addition, suggestions of improvements in the MVDC VARC-CB design are made.

The main contributions of this thesis are a complete set of design strategies to be used when designing the parameters of the MVDC VARC-CB, a Simulink model of the VARC-CB employed in an MVDC grid, and suggestions of possible improvements in the MVDC VARC-CB design.

Sammendrag

Mellomspente likestrømsnett (MVDC-nett) har mange fordeler sammenlignet med mellomspente vekselstrømsnett (MVAC-nett), og betraktes som velegnet til et bredt spekter av bruksområder. Håndteringen av kortslutningsfeil er imidlertid et av de viktigste hindrene for utbredelsen av MVDC-nett; spesielt er mangelen på MVDC-effektbrytere en fundamental utfordring. Hovedhensikten med denne masteroppgaven er å adressere denne barrieren ved å undersøke et spesielt interessant og lovende effektbryterkonsept: Spenningskildeomformerassistert resonansstrømeffektbryter (VARC-CB). Effektbryteren er opprinnelig foreslått for høyspente DC (HVDC)-applikasjoner, men denne avhandlingen utforsker VARC-CB-konseptet for MVDC-bruk.

Avhandlingen studerer og analyserer VARC-CB-konseptet for MVDC i detalj. Først legges et teoretisk fundament for oppgaven ved å utforske MVDC-nett og beskyttelsen mot kortslutningsfeil i disse. Videre utforskes et utvalg effektbryterkonsepter for MVDC fra litteraturen, inkludert konseptenes virkemåter, karakteristikker og delkomponenter, med et særlig fokus på VARC-bryteren. Dette danner grunnlaget for den påfølgende analytiske undersøkelsen av VARC-CB-konseptet for MVDC. I analysen utledes et fullstendig sett med designstrategier basert på etablerte designprinsipper og -begrensninger. Videre utvikles en komplett, parametrisert Simulink®-simuleringsmodell, hvor VARC-bryteren opererer i et MVDC-nett. Effektbryterens komponentmodell er parametrisert ved å bruke de utledede designligningene. Deretter valideres den utførte analysen, de foreslåtte designstrategiene og den utviklede simuleringsmodellen gjennom simuleringer. Basert på resultatene blir svakheter og mangler ved analyse- og modelleringsprosessene påpekt og diskutert, og mulige revisjoner blir vurdert. Potensielle forbedringer av VARC-CB-konseptet blir også foreslått.

Masteroppgavens hovedbidrag er et komplett sett med designstrategier som kan brukes til å designe parameterne til VARC-effektbryteren for MVDC, en Simulink-modell av effektbryteren i et MVDC-nett, samt forslag til mulige forbedringer av VARC-CB-konseptet.

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Abbreviations

AC	=	Alternating Current
ACCB	=	Alternating Current Circuit Breaker
BESS	=	Battery Energy Storage System
BIGT	=	Bi-Mode Insulated Gate Transistor
CB	=	Circuit Breaker
DC	=	Direct Current
DCCB	=	Direct Current Circuit Breaker
DER	=	Distributed Energy Resources
ESR	=	Equivalent Series Resistance
EV	=	Electric Vehicle
FB-HCB	=	Full-Bridge Based Hybrid Circuit Breaker
HCB	=	Hybrid Circuit Breaker
HV	=	High-Voltage
HVDC	=	High-Voltage Direct Current
IEEE	=	Institute of Electrical and Electronics Engineers
IGBT	=	Insulated Gate Bipolar Transistor
IGCT	=	Integrated Gate-Commutated Thyristor
ITIV	=	Initial Transient Interruption Voltage
LCS	=	Load Commutation Switch
MCB	=	Mechanical Circuit Breaker
MOSFET	=	Metal-Oxide Semiconductor Field Effect Transistor
MOV	=	Metal-Oxide Varistor
MS	=	Mechanical Switch
MV	=	Medium-Voltage
MVAC	=	Medium-Voltage Alternating Current
MVDC	=	Medium-Voltage Direct Current
NTNU	=	Norwegian University of Science and Technology
P-HCB	=	Proactive Hybrid Circuit Breaker
PV	=	Photovoltaic
PG-HCB	=	Hybrid Circuit Breaker with Pulse Generator
RCB	=	Residual Current Breaker
RRDS	=	Rate of Rise of the Dielectric Strength
RRITIV	=	Rate of Rise of the Initial Transient Interruption Voltage
RRRV	=	Rate of Rise of the Transient Recovery Voltage
RRTIV	=	Rate of Rise of the Transient Interruption Voltage
SC	=	Short-Circuit
SCR	=	Silicon-Controlled Rectifier
SF_6	=	Sulfur Hexafluoride
SSCB	=	Solid-State Circuit Breaker

TD-HCB	=	Hybrid Circuit Breaker with Time-Delaying Branches
TIV	=	Transient Interruption Voltage
TRV	=	Transient Recovery Voltage
UFD	=	Ultra-Fast Mechanical Disconnector
VARC-CB	=	Voltage Source Converter Assisted Resonant Current Circuit Breaker
VI	=	Vacuum Interrupter
VSC	=	Voltage Source Converter
WBG	=	Wide-Bandgap
WCS	=	Worst Case Scenario
ZCS	=	Zero Current Switching
ZnO	=	Zinc Oxide

Chapter 1

Introduction

1.1 Background and Perspective

Except for the final paragraph, this section is reused, with modifications, from the specialization project report [1].

The DC technology was originally declared the losing part in The War of Currents in the late 1800s, where Thomas Edison fought for DC on the one side, while Nikola Tesla and George Westinghouse defended AC on the other [2]. The tipping point was the invention of the AC transformer, enabling simple conversion between different AC voltage levels. This facilitated transmission of electrical power using AC with high voltages and low currents, hence minimizing losses. As corresponding DC conversion technology did not exist, AC was the most economical alternative for electrification. Since then, systems for electricity transmission and distribution worldwide have mainly been based on AC.

However, over the past decades, advancements in semiconductor devices and converter technologies have marginalized the main advantage of AC systems. Since the 1970s, DC conversion technologies have been maturing [3], making both AC/DC and DC/DC conversion increasingly cost-effective. Consequently, the ability to step voltages up and down is now not only reserved for AC systems, hence renewing the interest in employing DC in electrical power systems.

The attractiveness of DC is also increasing due to changes in how we produce and use electrical energy. A growing share of electrical power is generated by renewable energy sources and other distributed energy resources (DER), of which many are DC-sources by nature [4], such as photovoltaic (PV) systems and fuel cells. Battery energy storage systems (BESS), which also are DC operated, are penetrating the power grids. The number of loads and equipment powered by DC keeps growing, such as light-emitting diode lighting, data centers, DC motors and consumer electronics [2, 3]. In addition, DC power must be supplied for charging the increasing amount of electric vehicles (EVs) and electric ferries.

The interest in DC power systems also stems from their advantages compared to systems based on AC. Multiple benefits can be listed, such as higher efficiency, controllability and simplicity, as well as no need for reactive power compensation nor phase synchro-

nization [5]. Especially for transferring bulk power over huge distances, high-voltage DC (HVDC) is the natural choice of technology, due to lower losses and cost [6].

HVDC is already a well-established technology, and medium-voltage DC (MVDC) grids are also gaining increased attention. Similar to HVDC, the MVDC technology offers several beneficial features over its AC counterpart, and MVDC grids are considered well-suited for a wide range of application areas [4].

MVDC power grids are, however, still at an early stage of development, and some hindrances and challenges remain [3, 5]. One crucial design barrier is associated with the handling of short-circuit (SC) faults. Robust protection methods against SC faults must be developed in order to enable MVDC grids with satisfactory reliability. In particular, high-performance MVDC circuit breakers (CBs) are a key enabling technology [5, 7]. Today, no CBs for MVDC are commercially available, which currently is an important showstopper for MVDC grids.

This master's thesis builds upon the work presented in the specialization project report [1], where a comprehensive literature overview of and a comparison of DC circuit breaker (DCCB) concepts suitable for MVDC are given. In this thesis, one of the more promising and interesting DCCB topologies examined in the specialization project has been selected for a more detailed study: the voltage source converter (VSC) assisted resonant current CB (VARC-CB). The VARC-CB is a topical, promising technology currently under development, with several prominent beneficial features. Through an analytical investigation of the breaker, design equations and constraints are derived. These constitute a complete set of design strategies, which can be used for designing the VARC-CB for MVDC applications. A Simulink® simulation model of the VARC-CB employed in a simplified MVDC grid is also developed, and the model is parameterized using the derived design strategies. The results from several simulation cases are presented. On this basis, the robustness of the developed strategies and models is evaluated, and possible improvements in the MVDC VARC-CB design are proposed.

1.2 Objectives

The scope of this thesis is limited by the main objectives given in the following list:

1. Present and discuss the operating principles of the VARC-CB concept
2. Analytically investigate the MVDC VARC-CB, taking design principles and design limitations into consideration
3. Propose a complete set of design strategies for the MVDC VARC-CB
4. Develop a simulation model, including a component-level model of the VARC-CB and a simplified MVDC grid model, by using the physical modeling provided by the Simscape™ toolbox within the Simulink® environment
5. Validate the performed analysis, the proposed design strategies, and the developed model through Simulink simulations
6. Suggest possible improvements in the MVDC VARC-CB design

1.3 Report Outline

The thesis is divided into seven chapters. Chapter 2 sets the theoretical foundation upon which the rest of the thesis will be based. An overview of the concept of MVDC power grids is presented, and the benefits, possible application areas, and remaining challenges of the MVDC technology are discussed. A special focus is given to the challenge of SC fault handling, and a theoretical background on DC fault interruption and DCCB requirements is given. Furthermore, basic theory of three components found in many suggested DCCB topologies – the conventional mechanical AC circuit breaker (ACCB), the ultra-fast disconnector (UFD), and the metal-oxide varistor (MOV) – is provided. Finally, an overview of MVDC CB concepts proposed in literature is presented. Particular attention is given to the hybrid circuit breakers (HCBs), as the VARC-CB falls into this category.

Chapter 3 goes into details on the operating principles of the MVDC VARC-CB. Typical current- and voltage waveforms during an interruption process are shown, and a typical timing sequence is presented and described.

In Chapter 4, the MVDC VARC-CB is analytically investigated, and its design is examined. A set of design goals and a design system are first defined. Thereafter follows an analysis of each subcomponent of the breaker topology, taking design considerations and limitations into account. On the basis of these analyses, a full set of design strategies for the MVDC VARC-CB are derived.

Chapter 5 presents a complete, parameterized Simulink simulation model of the VARC-CB concept employed in an MVDC power grid. The modeling and parameterization processes are described and discussed in detail.

Chapter 6 includes simulation results and a following discussion of these. Through three main simulation cases, the performance of the developed simulation model is verified, and the derived design strategies are validated. Weaknesses and shortcomings of the modeling and analyses performed are also pointed out. In addition, two suggestions for improvements in the MVDC VARC-CB design are made and discussed

Finally, Chapter 7 concludes the thesis. The main findings and results are summarized, and recommendations for further work on the VARC-CB concept are made.

Chapter 2

Theoretical Background

The aim of this chapter is to provide a theoretical background and framework for the rest of the thesis. The first two sections include text and figures which are reused, with modifications, from the specialization project report [1]. The very first section gives an overview of the concept of MVDC power grids, including the benefits, promising application areas, and remaining challenges of the MVDC technology. The second section focuses on the main challenge of handling DC faults, with particular attention paid to operating principles and requirements of DCCBs employed for DC fault interruption. Subsequently, sections three and four present the physics and characteristics of three components found in many suggested DCCB topologies: the conventional mechanical AC circuit breaker (ACCB), the ultra-fast disconnector (UFD), and the metal-oxide varistor (MOV). The final section summarizes some of the main findings from the specialization project work. It gives a comprehensive but condensed overview of the main DCCB concepts suggested in literature, including their basic operating principles, their most essential beneficial features, and their drawbacks/challenging aspects. Some of the text is reused, with modifications, from the specialization project report. The literature review has, however, been updated, to provide a more accurate presentation of the state of the art. Furthermore, all the figures have been redrawn in order to present clearer explanations. The very last subsection of the chapter narrows the scope down to the breaker concept investigated in this thesis, the VARC-CB, giving a brief reasoning for the choice of the DCCB concept.

2.1 MVDC Power Grids

The term *MVDC power grid* refers to an interconnection of more than two power electronic converter stations using medium-voltage DC links [8]. The voltage range for MVDC is not yet standardized: [3] uses a range of 1.5–30 kV, [9] employs 10–70 kV, and the IEEE standard 1709-2010 for MVDC power systems on ships provides 1–35 kV [10]. Based on existing literature, the potential lower and upper limits for medium-voltage DC thus seems to be around 1 kV and 70 kV, respectively.

2.1.1 Beneficial Features

When comparing MVDC and MVAC systems, several advantages of the former can be listed. The most important ones are the following:

- **Losses.** MVDC connections offer lower losses than MVAC connections of similar voltage level [11]. This is mainly due to the absence of skin and proximity effects in DC links, no electrical hysteresis nor dielectric losses, less corona losses, and the fact that only active power is transmitted [3]. Consequently, the power transfer capability for the same voltage level is higher when employing MVDC.
- **Reactive compensation.** As DC links neither produce nor absorb reactive power, the need for reactive power compensation, which is present in many AC systems, is eliminated [11].
- **Interconnection.** The ease of integrating multiple sources and loads is an essential advantage of MVDC systems. When connecting a power source or load to an MVAC grid, the phase, magnitude and frequency of its voltage must be synchronized with the grid voltage. On the other hand, integration of a source or load into an MVDC system only requires voltage control [12].
- **Controllability.** The use of power electronic converters, rather than conventional transformers employed in AC systems, enables dynamic control of the power flow through the DC links [13]. Consequently, MVDC systems provide a higher degree of controllability, and hence also flexibility, than MVAC systems [14].
- **Conversion steps.** In many application areas, MVDC requires fewer conversion stages between sources and loads. Due to this, MVDC can offer increased efficiency, increased reliability, and a smaller footprint [2].
- **Size and weight.** Compared to an MVAC grid, the accumulated size and weight of an MVDC power grid can in many cases be smaller. One of the main reason thereof is that the bulky 50 and 60 Hz AC transformers are eliminated [10]. In addition, the number of conversion steps is possibly lower. Furthermore, MVDC offers higher power capability for the same voltage level, as discussed earlier. Consequently, choosing MVDC links over MVAC links can diminish the required space, and hence reduce environmental impacts [11].

2.1.2 Promising Application Areas

Many application areas for MVDC power grids have been suggested in literature. Some of the more promising are power systems on ships [15, 16], aircraft power systems [4, 17], and collector grids for solar- and wind farms [2, 18]. Distribution grids with many different sources and loads, and large penetrations of DER and BESS are another area of interest for MVDC employment [2, 4]. A more detailed investigation of how these application areas can benefit from the many advantageous features of MVDC grids can be found in [1].

2.1.3 Challenges and Barriers

Despite the many benefits and promising application areas, some challenges remain before MVDC power grids can be widely deployed. The main barriers are listed below.

- **Standardization.** One important obstacle is the lack of standards, regulations and guidelines for MVDC grids [19]. The lack of an established voltage range, which was discussed in the beginning of the current section, is an example of this challenge. Some standards for specific applications exist, such as the IEEE Standard 1709-2010 for MVDC systems on ships [10]. However, application-independent regulations targeted at design and operation of MVDC power grids are nonexistent [5].
- **Cost.** When compared to the conventional 50 and 60 Hz transformers employed in AC systems, the less mature power electronic converters required for DC grids are more costly [20]. However, this price difference is rapidly decreasing due to developments in semiconductor devices and converter technologies [5].
- **Fault handling.** A significant challenge is developing proper protection schemes suitable for MVDC power grids [21]. In particular, handling SC faults is a main difficulty in the design and operation of MVDC systems. This challenge will be examined in further detail in Section 2.2.
- **Equipment.** Electrical infrastructure and equipment specifically designed for medium-voltage DC must be developed in order to establish MVDC grids. One example is the need for proper MVDC cables [22]. Another crucial challenge is the lack of high-performance DCCBs [16]. This is one of the main hindrances towards MVDC grid deployment today, and is considered a key enabling technology [7].

2.2 Fault Handling in MVDC Power Grids

In any electrical power system, protection against faults is required in order to ensure reliable and safe system operation. This is also necessary for preventing damage to components and people. At the occurrence of a fault, a well-functioning protection scheme should be able to eliminate the fault, while limiting the impact on the healthy parts of the system. Two important steps in the elimination process are to detect and to locate the fault. These steps are, however, beyond the scope of this study. When the fault has been identified, the protection system must ensure fault interruption and isolate the faulted parts of the grid. The main emphasis of this section will be to present different methods for DC fault interruption, with a particular focus on DCCBs.

2.2.1 Three Methods for DC Fault Interruption

There are three main approaches to provide DC fault interruption, each relying on different devices: ACCBs, converters with fault-blocking capabilities, or DCCBs. The first strategy has been a common way to clear DC faults in point-to-point HVDC transmission systems based on voltage source converters (VSCs), and is based on utilizing the ACCBs of the AC/DC converters at each end [4, 23]. This is an economical and simple solution, but not

optimal for multi-terminal DC grids, as it is slow and leads to an outage of the whole grid [24]. In the second approach, power converters with inherent fault interruption capabilities are employed. This approach may be well-suited in certain application areas, as it can be space- and weight-efficient [25]. However, it is a costly and relatively slow method, and it involves grid deenergization, just as the ACCB approach [26, 27]. The third strategy is to install DCCBs at all line ends, which, as opposed to the two prior strategies, provides selective grid protection [26]. Using DCCBs for DC fault clearance is the main area of interest in this thesis, and is explored in more detail below.

2.2.2 Basic DCCB Operating Principles and Requirements

Developing CBs for DC fault clearance is not straightforward. DC fault interruption is a challenging task, imposing demanding requirements on the breaker design and operation. These challenges, and the resulting DCCB operation principles required, are examined in the following by means of an illustrative example.

Figure 2.1 represents a simplified DC system experiencing a pole-to-pole SC fault. The system consists of a constant DC voltage source V_{DC}, a line inductance L_{line}, an ideal DCCB, and a resistive load R_{load}. v_L and i_L are, respectively, the voltage across and the current through the line inductance, while v_{CB} is the terminal voltage of the CB. Inspired by [28], the idealized waveforms in Figure 2.2 represent i_L and v_{CB} during the fault.

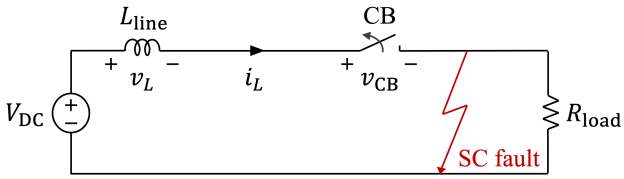


Figure 2.1: Simplified DC system experiencing an SC fault.

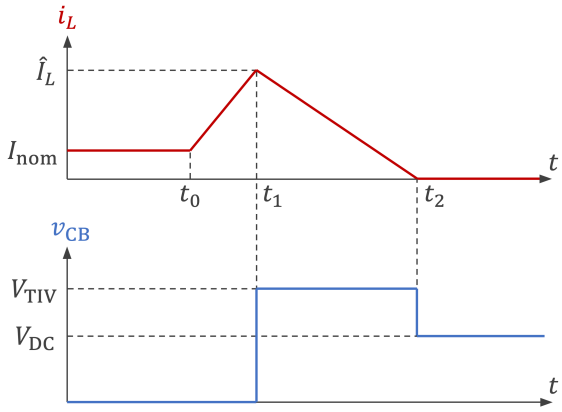


Figure 2.2: Fault current (red) and DCCB voltage (blue) during the SC fault in Figure 2.1.

The SC fault occurs at the time instant t_0, at which i_L starts to increase from its nominal value I_{nom}. At t_1, v_{CB} rises above the nominal system voltage, the CB neutralizes the fault, and i_L starts to decrease from its peak value $\hat{I}_L$ towards zero. The fault current reaches zero at t_2, at which the CB voltage drops to the nominal system voltage V_{DC}.

One of the main reasons that DC fault interruption is a demanding task is the absence of natural current zero-crossings in DC systems. Thus, unlike ACCBs, DCCBs must be capable of forcing the fault current to zero. This is normally done by the DCCB generating a counter-voltage with an amplitude exceeding the source voltage. Hence, the voltage across the line inductance becomes negative, resulting in a negative time derivative of the line current, as deduced from Equation (2.1). Consequently, the line current will decrease to zero. This phenomenon can be observed in the time interval t_1–t_2 in Figure 2.2.

$$\frac{di_L}{dt} = \frac{V_{\text{DC}} - v_{\text{CB}}}{L_{\text{line}}} \tag{2.1}$$

According to Equation (2.1), there will be an overvoltage induced across the circuit breaker during the decrease of the fault current. This overvoltage is referred to as the transient interruption voltage (TIV) [29], and is shown as V_{TIV} in Figure 2.2. V_{TIV} can be calculated by:

$$V_{\text{TIV}} = V_{\text{DC}} + L_{\text{line}} \left| \frac{di_L}{dt} \right| \tag{2.2}$$

The DCCB must have sufficient voltage withstand capability to handle the TIV. From Equation 2.2, it is evident that a larger V_{TIV} value means a higher line current time derivative, as V_{DC} is constant. Consequently, an increase in V_{TIV} will result in the fault current decreasing more rapidly to zero. The downside is that this requires a larger voltage withstand capability for the DCCB.

Another challenging aspect of DC fault interruption is the handling of the magnetic energy stored in the DC system during the fault. In AC systems, the stored energy drops to zero at each zero crossing of the current. Consequently, an AC system is demagnetized periodically [30]. This is not the case for a DC system, as it lacks current zeros. Unlike an ACCB, a DCCB must thus include means for energy dissipation. For the system in Figure 2.1, the CB must be able to absorb the total energy W_{total} given by Equation (2.3) [29].

$$W_{\text{total}} = \frac{1}{2} L_{\text{line}} \hat{I}_L + \int_{t_1}^{t_2} V_{\text{DC}} i_L(t) dt \tag{2.3}$$

The first term on the right-hand side of Equation (2.3) is the magnetic energy stored in the line inductance during the fault. The second term is the energy fed into the network by the DC source during the fault current decrease between t_1 and t_2. Both energy contributions must be dissipated by the DCCB, leading to energy stress on the breaker [29].

The low network inductance of DC grids is also contributing to the complexity of DC fault interruption. Normally, DC network inductances are considerably lower than those of AC grids. This is mainly due to the lack of transformer leakage inductances and the lower DC line/cable inductances [5]. A low network inductance gives a high rising rate of the fault current during t_0–t_1 in Figure 2.2. To prevent the current from reaching

detrimentally high values, the CB must quickly neutralize the fault (stop the current from increasing). Preferably, the time from the trip order is received by the breaker until the fault is neutralized should be in the range of a few milliseconds for a DCCB operating in an MVDC grid [31]. In comparison, the corresponding time for conventional ACCBs operating in AC systems is typically in the range of several tens of milliseconds [32].

The final factor complicating the process of fault interruption in MVDC grids is the sensitivity of power electronic equipment. Power converters are essential building blocks of MVDC power grids, and the power electronic components employed in these converters are sensitive to overloads. They must therefore be protected against overcurrents [33]. This results in demanding requirements regarding the operating speed of DCCBs.

To summarize, a DCCB operating in an MVDC power grid is required to:

1. Neutralize the fault current within a few milliseconds from its trip order
2. Force the fault current down to zero
3. Dissipate the residual energy of the network
4. Withstand the transient interruption voltage (TIV)

In addition to these core requirements comes the desired features of a DCCB. Several features can be listed, and all of them may used as DCCB performance parameters. Inspired by the discussion on DCCBs in [4], some key features are low power losses, high reliability, low complexity, low cost, compact size, and low weight. The importance of each feature depends on the application area and the grid topology under consideration.

2.3 Mechanical Switches

Several proposed DCCB designs include mechanical switches (MS) in their topologies. In these designs, one out of two MS types are normally used: some DCCBs employ a conventional mechanical ACCB, while others make use of an ultra-fast mechanical disconnector (UFD). In this section, the physical behavior and characteristics of the two MS types are examined, and their design and applications are briefly discussed.

2.3.1 Conventional Mechanical AC Circuit Breakers

Conventional ACCBs are mechanical devices capable of initiating, carrying and interrupting the flow of current in an AC circuit under normal conditions and under specified abnormal conditions, such as those of an SC fault [34, 35]. The basic configuration of an ACCB consists of two metallic contacts, i.e. electrodes, placed in a container with an insulating medium [36]. One of the electrodes is fixed, whereas the other is movable. When the CB is in its closed state, the two electrodes are in galvanic contact, creating a very low-resistive path for the current. When the CB is to perform a current interruption, a driving mechanism separates the electrodes. This results in a conductive plasma, i.e. an electric arc, being formed in the contact gap. The current continues to flow through the arc, and will keep flowing as long as the arc is burning. Because of this, a prerequisite of the current interruption in ACCBs is that the electric arc must be extinguished [34].

2.3.1.1 The Insulating Medium

The electrode separation and arc burning in an ACCB takes place in an insulating medium. This medium has two main tasks: the first is to ensure successful arc extinction, and the second is to provide insulation between the separated electrodes and between each electrode to earth [35]. A proper insulating medium should have high thermal and chemical stability, good arc-quenching properties, and high dielectric strength. Different mediums possess these characteristics, and the ones most commonly used in ACCBs are air, oil, sulfur hexafluoride (SF_6) and vacuum. Previously, air and oil were the leading technologies for insulating mediums in ACCBs rated above 1000 V [34]. Today, vacuum and SF_6 are dominating, with vacuum CBs being the most widely deployed CB type for voltages up to 72.5 kV [36], whereas SF_6-based ACCBs prevail at higher voltage levels [34].

2.3.1.2 Arc Extinction and Current Interruption

The arc in the contact gap of an ACCB exists as long as it remains stable, which is satisfied when its energy input is able to compensate for its energy losses [37]. As the arc's energy input is given by the time integral of the product of arc voltage and arc current, the arc experiences unstable conditions if its current crosses zero. At such points the energy input will temporarily be zero, causing the arc to extinguish for a brief period [35, 36].

Due to the oscillatory behavior of an AC system, the current runs periodically through zero, causing arc extinction to occur naturally. This property of AC circuits is exploited in conventional ACCBs, which perform current interruption when the arc current passes through zero. The main task of the ACCB is therefore to prevent the arc from reigniting after it has extinguished at a current zero-crossing [34].

After the arc is extinguished, there is still a considerable amount of charge carriers present in the contact gap and the temperature is high. Hence, the gap still has some remaining electrical conductivity, and its voltage withstand capability is low [35]. At the same time, a voltage produced by the surrounding power system – the recovery voltage – starts to rise across the breaker contacts. If the free charge carriers in the contact gap are not rapidly removed, the applied recovery voltage will cause a dielectric breakdown in the gap, hence reigniting the arc. The core of preventing reignition is therefore to eliminate the remaining electrons and ions. This will recover the dielectric strength of the insulating medium in the gap, so it can withstand the applied recovery voltage.

Figure 2.3 illustrates a typical recovery voltage waveform after a successful current interruption. An idealized arc current curve is also included. When the arc current is interrupted, the recovery voltage oscillates towards the power frequency system voltage in the course of a transient period, as seen in the figure. The breaker voltage during this period is called the transient recovery voltage (TRV).

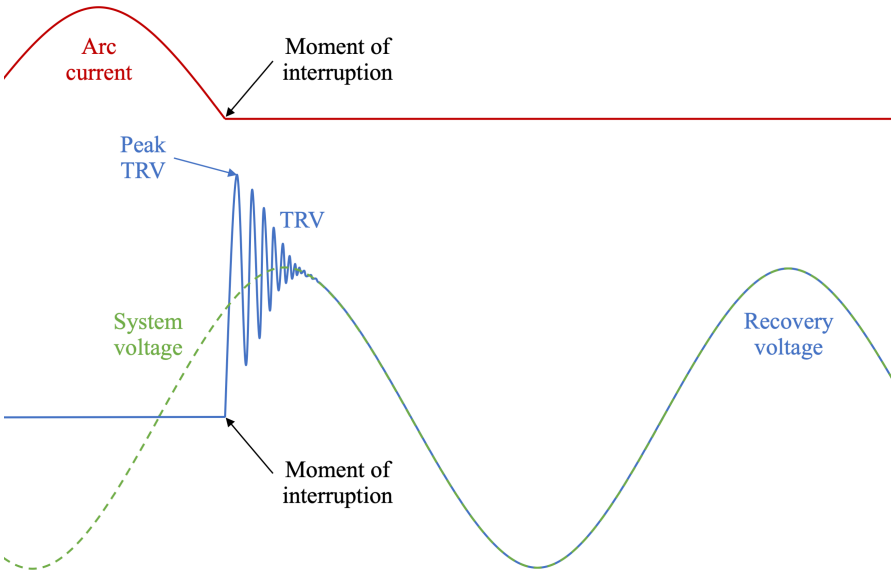


Figure 2.3: Typical terminal voltage (blue) and arc current (red) waveforms of an ACCB around the moment of interruption.

The peak TRV value, together with the breaker's gap distance at arc current zero, affect whether a reignition is prevented or not. As the dielectric strength of the breaker increases with the distance between its electrodes, the gap distance is decisive for the maximum voltage withstand capability the gap can recover to [35]. Ergo, to achieve a successful current interruption, the gap length at the instant of arc extinction must correspond to a capability higher than the maximum value the TRV attains.

The rate of rise of the TRV (RRRV) and the rate of rise of dielectric strength (RRDS), i.e. the dv/dt capability of the breaker, are also factors playing important roles in the success or failure of the current interruption [38, 39]. Favorable interruption conditions in terms of RRRV and RRDS are illustrated in Figure 2.4, in which the arc current is assumed to cross zero at $t = 0$. The black line represents a typical capability curve of an ACCB, which has a slope of RRDS. The blue curve represents the course of a typical oscillatory TRV, and the orange line illustrates the RRRV. For the case displayed, RRRV $<$ RRDS, hence the dv/dt capability of the ACCB is not exceeded. However, if the build-up of the dielectric strength was slower than the TRV rising rate, i.e. RRRV $>$ RRDS, the TRV would at some point have surpassed the recovered voltage withstand capability. This would result in a dielectric reignition and an unsuccessful current interruption. For a successful interruption, it is therefore essential that the TRV is kept below the capability curve of the breaker, meaning the RRDS must be equal to or higher than the RRRV.

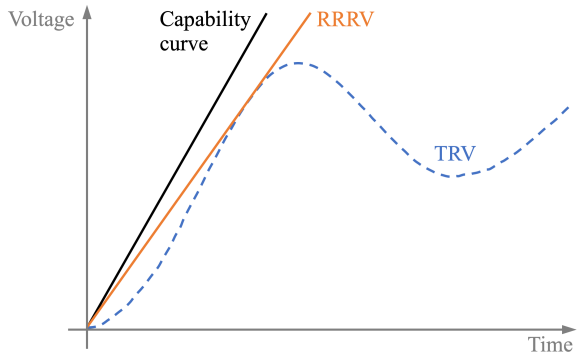


Figure 2.4: Illustrative curves showing the capability curve (black) of a theoretical ACCB, together with the TRV (blue) applied across the breaker terminals, and a line representing the RRRV (orange).

Another factor decisive for the successfulness of the current interruption is the current steepness, i.e. di/dt, at current zero [37]. A higher di/dt-value shortens the time available for the gap to start the recovery of its voltage withstand capability before the TRV is applied. Consequently, each ACCB has a maximum di/dt-limit, above which the breaker will not be able to quench the electric arc.

2.3.1.3 Arc Characteristics and Arc Models

Usually, switching arcs in ACCBs are divided into two categories: high-pressure arcs and low-pressure arcs. The first category includes arcs existing at or above atmospheric pressure, which is the case in gas- and oil-based ACCBs. The latter comprises arcs formed at pressures below the atmospheric, which is the case in ACCBs using vacuum as the insulating medium [34, 37].

The high-pressure arc in gas- and oil-based ACCBs is created through ionization of the insulating medium between the breaker contacts. As the insulting medium is the source of plasma, the properties of a high-pressure arc is determined by the surrounding gas or oil [37]. In vacuum-based ACCBs, on the other hand, there is no ionizable medium present in the contact gap. Instead, the substance forming a vacuum arc is a metal vapor which is boiled off from the electrodes [40]. The characteristics of a vacuum arc are therefore solely determined by the electrode material [37].

Figure 2.5 displays the typical shape of the V-I characteristic belonging to a *stationary* high-pressure arc [37]. It should be noted that ACCBs always deal with arcs which are *dynamic*, as the arc current and voltage vary with time. The characteristics and physical behavior of a dynamic arc are, however, rather complex. Therefore, a common simplifying assumption is that the arc behavior is static within a time interval. As can be seen in Figure 2.5, the static V-I characteristic is very nonlinear. At low current values, the voltage decreases with increasing current, i.e. the arc exhibits negative differential resistance. Then follows a current range in which the arc voltage is relatively constant. For this flat portion of the V-I curve, normal voltage values lie in the range of a few hundred volts to a few kilovolts. At high current values, the differential arc resistance turns positive; the arc voltage increases with the arc current.

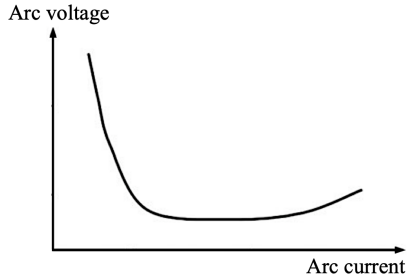


Figure 2.5: Typical static V-I characteristics of a high-pressure arc, adapted from [37].

Many mathematical models have been developed for describing the V-I characteristics of high-pressure arcs. Two well-known, classic black box models are the ones of Cassie and of Mayr [37, 40]. Both models are founded on the premise of arc conductance being strongly affected by the energy stored in the arc. Several new, more advanced models have also been developed, using the Mayr and Cassie models as foundations.

The mentioned analytical models can, however, not be used for describing the behavior of arcs formed in vacuum-based ACCBs, as vacuum arcs show some important differences from high-pressure arcs [40]. One unique characteristic of vacuum arcs is that they have two modes in which they can exist: diffuse mode and constricted mode [37]. The transition from the diffuse to the constricted mode happens when the arc current exceeds a certain limit. This limit depends on the electrode material and geometry, but is typically in a range of 10–15 kA. The physical details of these arc modes will not be elaborated on. However, an important aspect to highlight is that the longer time the arc is in the diffuse mode prior to current zero, the greater the likelihood of a successful current interruption [34].

When in the diffuse mode, vacuum arcs have a V-I relationship quite different from the one shown in Figure 2.5. The diffuse vacuum arc voltage is fairly constant, and almost independent of the arc current magnitude [36, 37]. It is also considerably lower than the arc voltages observed for high-pressure switching arcs. Typically, the arc voltage is approximately 20–40 V, and it varies slightly with the electrode material used [34, 37]. When in the constricted mode, on the other hand, the vacuum arc appears quite similar to that of a high-pressure arc [40]. In this mode, the arc voltage varies intermittently, and has an average value significantly higher than in the diffuse mode [37].

Another special feature of vacuum arcs is a phenomenon called *current chopping*. It can, under certain conditions, occur in other ACCB types, but it is considered a typical vacuum CB phenomenon [37]. Current chopping occurs when the arc current approaches zero. When reaching a certain low current level, the arc abruptly collapses due to instability; the arc extinction occurs before the current has reached zero [41]. This is highly unwanted, as the abrupt current cut-off can cause overvoltages in the circuit [37]. Low chopping current levels are therefore desirable. This level is determined by the electrode material, and is typically in the range of 1–15 A for conventional vacuum ACCBs [34].

2.3.2 Ultra-Fast Disconnectors

A disconnector is a mechanical device normally used to isolate a part of an electrical system from the rest [42, 43]. Disconnectors are capable of continuously carry rated current, and they can carry SC currents for a specified duration. They also have the ability of performing no-load switching, but in contrast to ACCBs, disconnectors are not designed for interrupting electric arcs of significant magnitude [42]. Consequently, disconnectors have very low current breaking capabilities compared to ACCBs [42, 43]. .

The basic construction and operating principles of a disconnector have many similarities to those of an ACCB. A disconnector has two metallic electrodes, of which one is fixed and the other is movable [44]. Under closed operation, the electrodes are in contact, providing a path for the current with very low resistance. At an opening signal, an actuator separates the electrodes, hence exposing the insulating medium in which the electrodes are placed (e.g. SF_6, air or vacuum). The electrode distance is then increased until the contact gap has obtained a voltage withstand capability that meets the isolation requirement.

Just as for ACCBs, it is important that during opening, the voltage applied to the disconnector terminals does not at any point exceed the obtained voltage withstand capability of the contact gap. If this happens, it will cause a dielectric breakdown of the gap [45].

The disconnectors in DCCB designs in literature usually employ Thomson coil actuators. These actuators are based on electromagnetic repulsion forces, which results in very fast mechanical operation, hence the name *ultra-fast* disconnectors [46, 47]. The operating principles, modeling and design of a Thomson coil-based UFD can be found in [46].

2.4 The Metal-Oxide Varistor

The metal-oxide varistor (MOV) is a vital component in most DCCB designs. It is a variable resistor, and its circuit symbol is shown in Figure 2.6a. Figure 2.6b displays an example MOV V-I curve similar to that typically provided in MOV datasheets. Only one quadrant is shown, as the characteristic is symmetrical [48, 49].

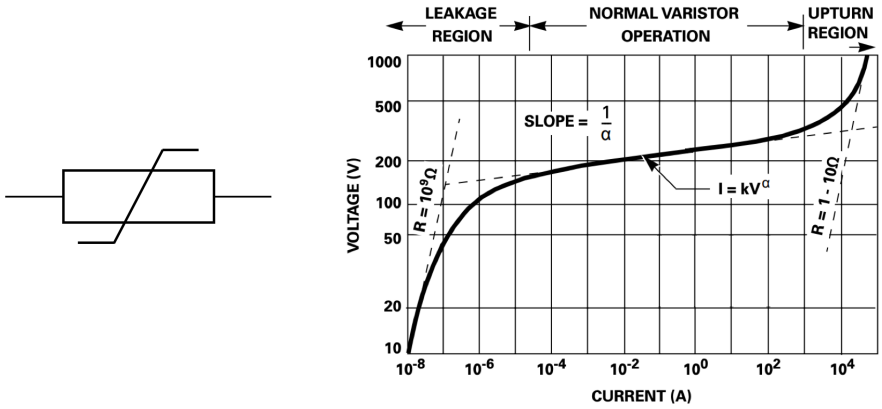


Figure 2.6: (a) MOV symbol, (b) Typical MOV V-I curve, adapted from [49].

In Figure 2.6b, three regions of MOV operation are clearly illustrated: the leakage-, the normal varistor-, and the upturn regions. In the leakage region, the MOV exhibits high resistance and approaches a linear V-I relationship [49]. The effective resistance value of the MOV in this region is typically in a range of 10^7–10^9 Ω. Resultantly, the MOV behaves almost as an open circuit, with only a small leakage current flowing. As the MOV voltage increases above a certain level, normally known as the clamping voltage of the MOV, a transition to the normal varistor operation region, i.e. the clamping region, is observed. In this region, the V-I characteristic is clearly non-linear, with the effective MOV resistance decreasing in response to an increase in current. As seen, the MOV voltage remains relatively constant for a large current range. When the current approaches the maximum rating of the MOV, the effective MOV resistance approaches the constant resistance of the zinc oxide (ZnO) grains of which the MOV consists. This resistance is normally in a range of 1–10 Ω. As a result, the MOV moves into the upturn region, where a linear V-I relationship again is observed.

In addition to the nonlinear resistance, an important MOV feature is its high energy absorption capability. The energy absorption in a time interval of t_a–t_b is given by:

$$W_{\text{MOV}} = \int_{t_a}^{t_b} v_{\text{MOV}}(t) i_{\text{MOV}}(t) dt \tag{2.4}$$

2.4.1 Equivalent Circuit

Figure 2.7 depicts the simplified equivalent circuit representing an electrical model of an MOV [48, 49]. The variable R_{VAR} reflects the non-linear resistive properties of the MOV, and the constant R_{ON} is the ohmic bulk resistance of the ZnO grains. The capacitor C represents the dielectric properties of the MOV. L models the lead inductance.

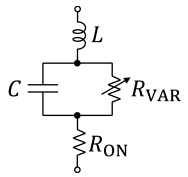


Figure 2.7: Equivalent circuit of an MOV.

2.4.2 Metal-Oxide Varistor Applications

Because of their non-linear resistivity and their high energy absorption capabilities, MOVs are used to protect other equipment against surge voltages. When connected in parallel to a component, the MOV behaves like an open circuit during normal operation. However, at the occurrence of a voltage transient exceeding a certain value, the MOV forms a low-resistance shunt, due to the sharp reduction in its resistivity. As a result, the MOV clamps the overvoltage and dissipates the energy of the transient pulse. In this way, the MOV protects the component from potentially damaging voltage and energy exposure [48, 49].

The voltage clamping and energy absorption capabilities are also the reasons why MOVs are used in DCCB designs presented in literature. In many of these designs the MOV is responsible of clamping the voltage at a level higher than the nominal value, hence providing the counter voltage needed to force the fault current to zero. In addition, the MOV usually also functions as an energy absorber, dissipating the magnetic energy stored in the network during the fault, ref. Equation (2.3).

2.5 DC Circuit Breakers Presented in Literature

A main objective of the specialization project was to present and discuss MVDC CB concepts proposed in literature. Hence a comprehensive literature overview can be found in [1]. This section presents a summary of this work, with some additions and modifications. In literature, DCCB topologies are usually classified using three main categories: mechanical circuit breakers (MCBs), solid-state circuit breakers (SSCBs), and hybrid circuit breakers (HCBs). In this section, particular attention is given to the HCBs, as the topology chosen to be studied in this thesis, the VARC-CB, falls into this category.

2.5.1 Mechanical DC Circuit Breakers

The MCBs, of which the generic concept is shown in Figure 2.8, are based on conventional mechanical ACCBs. During normal operation, the line current flows solely through the main branch via the ACCB. Once a fault occurs, the ACCB opens, and an arc is created between its contacts. However, with the absence of current zero-crossings in DC systems, the arc current will not naturally extinguish. In order to obtain arc extinction, an artificial arc current zero must thus be generated. This is provided by the current injection branch, which is based on either a passive or an active resonance circuit.

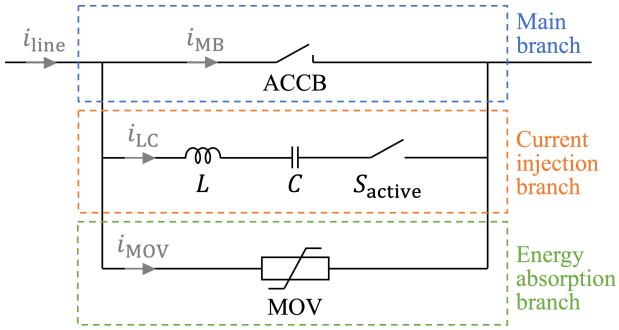


Figure 2.8: Mechanical DC circuit breaker with passive/active current injection.

In the passive MCB, the ACCB is of the high-pressure type, and the making switch S_{active} is not included [50]. When the ACCB opens, an arc with similar V-I characteristics as in Figure 2.5 is created. The high arc voltage excites a resonance in the passive LC circuit, and due to the negative differential arc resistance, a resonant current with growing amplitude results [51]. When its magnitude reaches that of i_{line}, the sum $i_{\text{MB}} = i_{\text{line}} - i_{LC}$ becomes zero, and the arc extinguishes. This causes i_{line} to commutate into the current injection branch and to charge C. When the capacitor voltage reaches the MOV clamping voltage, i_{line} commutates into the energy absorption branch. The residual network energy is then dissipated, and the MOV's counter voltage forces the line current to zero.

The active MCB is very similar to the passive, but S_{active} is included, and C is precharged (typically to the DC line voltage [50]). When the ACCB opens, S_{active} is closed. The precharged C-voltage excites a resonance in i_{LC}, with a frequency typically significantly higher than in the passive MCB. Due to the high precharged voltage, the amplitude

of the first i_{LC} cycle exceeds the i_{line} level, hence a zero in i_{MB} is generated in either 1/4 or 3/4 of a cycle, depending on the direction of i_{line}. The ACCB in the active MCB is typically based on vacuum, due to the low arc voltage and the superior high-frequency interruption performance of vacuum CBs [50, 52].

As the current during normal operation is conducted through mechanical contacts, the MCBs have the key advantage of very low steady-state power losses. Low cost and a simple and robust design are other advantages. A drawback of the passive MCBs is their limited current interruption capability, which is due to the differential resistance turning positive at high currents (ref. Figure 2.5) [53]. Another significant drawback of the passive version is slow operation. The resonant frequency is typically 1–3 kHz, resulting in breaker operation times of several tens of milliseconds [50, 54]. The active MCBs, on the other hand, are faster due to their higher resonant frequencies, and demonstrate operation times of a few milliseconds [50]. A drawback of the active MCBs, however, is the considerable capacitor size they require [53].

2.5.2 Solid-State DC Circuit Breakers

The SSCBs are DCCBs without any mechanical switches, which rely on power electronic devices for breaker operation. Power semiconductor devices commonly found in proposed high-power SSCBs (and also in proposed HCBs) are power diodes, silicon-controlled rectifiers (SCRs) (also known as thyristors), integrated gate-commutated thyristors (IGCTs), metal-oxide semiconductor field effect transistors (MOSFETs), insulated gate bipolar transistors (IGBTs), and bi-mode insulated gate transistors (BIGTs) [1]. A detailed investigation of the operating principles and characteristics of these devices is given in [1].

The use of semiconductor devices for current breaking in SSCBs results in some key benefits compared to the MCBs. The main advantage is very high operation speed. Due to the fast switching of the semiconductor components, fault clearance within 100 μs can be obtained [7]. Other advantages are arcless operation, great acoustic performance, and low maintenance due to no mechanical parts [55]. The main disadvantage is the high power losses. Due to SSCBs having semiconductor devices in their main current path, the on-state resistance of an SSCB is in the order of a few milliohms. As a consequence, employing SSCBs requires the use of an efficient cooling system for dissipation of the generated heat [7]. Another drawback compared to MCBs is the higher cost [4]. This is caused by the cooling requirements, as well as the use of expensive semiconductor devices instead of low-cost mechanical breakers. Furthermore, some SSCB topologies are considerably more complex than the MCB design. A thorough investigation and comparison of different SSCB topologies can be found in [1].

2.5.3 Hybrid DC Circuit Breakers

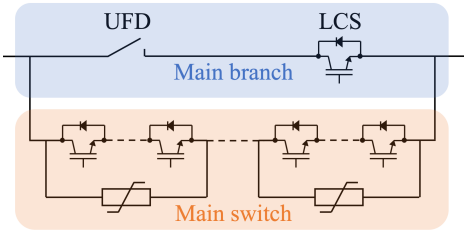
The HCB concept is a hybrid of the two other DCCB categories, and combine the use of mechanical switches and power electronic circuitry. The HCBs are therefore able to combine the strengths of the two other DCCB types [4]. Similar to the MCBs, the HCBs have significanly lower losses than the SSCBs. Many HCB topologies employ some semiconductor devices in their main current path, although the number of devices is usually smaller than in the main path of an SSCB. Resultantly, lower conduction losses are achieved. Due

to the use of mechanical switches, HCBs are significantly slower than SSCBs. They do, however, provide higher operation speeds than the passive MCBs. Typically, breaker operation times in the same range as for the active MCBs are achieved. What is often presented as main drawbacks of the HCB category is that the topologies typically are more complex, require more complicated control, and may be more expensive than MCBs and SSCBs [4].

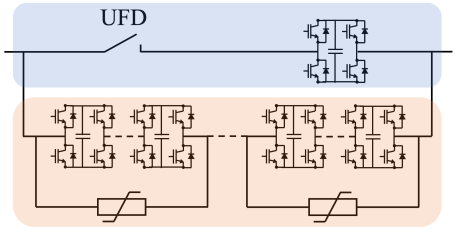
Many different HCB topologies are suggested in literature. A possible classification approach is to differ between mechanical HCBs and solid-state HCBs, where the topologies in the first category employ no power electronic devices in their main path, whereas the topologies in the second do [53]. Furthermore, the mechanical HCBs are based on ACCBs as the type of mechanical switch, whereas the solid-state HCBs are UFD-based.

It should be noted that when S_{active} for the active MCB in Figure 2.8 is realized using power semiconductor devices, the active MCB is sometimes classified as an HCB [56].

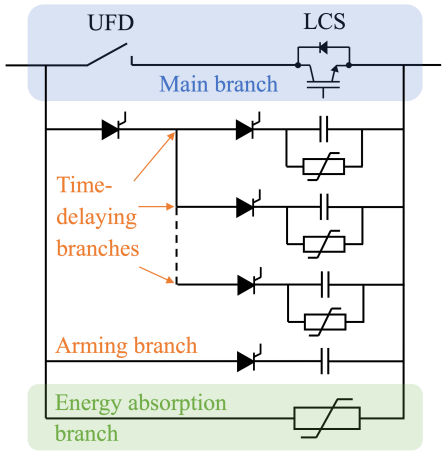
The HCB topologies investigated in the specialization project [1] are included in Figure 2.9, where 2.9a, 2.9b, and 2.9c are solid-state HCBs, whereas 2.9d and 2.9e are mechanical HCBs. The breaker concepts in Figures 2.9a and 2.9c are illustrated with their unidirectional versions, however they can also be made bidirectional. It should be noted that most of these topologies are originally proposed for HVDC applications. However, the basic operation principles and the techniques used are applicable for MVDC systems as well, if proper down-scaling is performed [57].



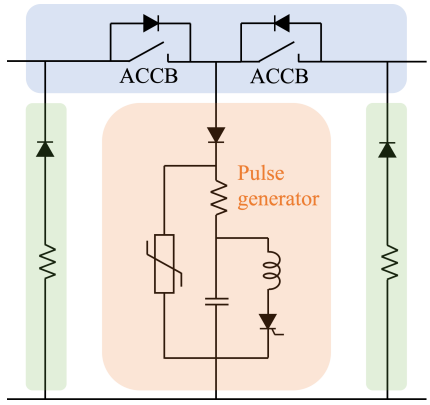
(a) Proactive HCB (P-HCB).



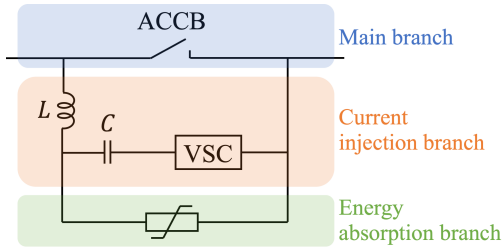
(b) Full-bridge based HCB (FB-HCB).



(c) HCB with time-delaying branches (TD-HCB).



(d) HCB with pulse generator (PG-HCB).



(e) VSC assisted resonant current HCB (VARC-CB).

Figure 2.9: Various HCB topologies suggested in literature.

The proactive HCB (P-HCB) is described in [8, 58], and is illustrated in Figure 2.9a. When receiving a trip order, the low-voltage semiconductor load commutation switch (LCS) turns off. Resultantly, the line current commutates into the main switch, which contains series-connected fully controllable semiconductor devices, here shown as IGBTs. When the current has fully commutated, the UFD can begin its opening process. The semiconductor devices turn off once the UFD has reached sufficient voltage withstand capability, at which the line current is transferred into the parallel MOVs. The MOVs absorb the residual system energy, and their accumulated counter voltage forces the line current to zero. Main advantages of the P-HCB are the simple design, the possibility of proactive control of the breaker [8], and high controllability of the breaker current. Another benefit is arcless operation, due to the UFD opening at zero-current conditions [4]. A disadvantage of the P-HCB concept is high current stress on the semiconductor devices in the main switch [59]. Another drawback is relatively high steady-state power losses caused by the LCS introducing semiconductor devices into the normal current path.

A similar concept to the P-HCB is the full-bridge based HCB (FB-HCB) in Figure 2.9b, in which the single semiconductor switches in the P-HCB have been replaced by full-bridge submodules [60, 61]. The basic operation principles are similar to those of the P-HCB, and the FB-HCB offers the same advantages of arcless operation, possibility of proactive breaker control, and high current controllability. However, the FB-HCB offers lower current stress on its semiconductor devices when compared to the P-HCB, allowing for devices with lower current capabilities [61]. The main drawback of the FB-HCB is the high number of semiconductor switches required. Another disadvantage is the relatively high power losses caused by the semiconductor devices present in the normal current path.

Figure 2.9c illustrates an HCB with time-delaying branches (TD-HCB), which is described in [30, 62]. Its main operating principle is to commutate the fault current in steps during the opening time of the UFD. The time-delaying branches with their capacitors and MOVs are inserted sequentially using the SCRs. This results in a gradual increase in the UFD voltage. Eventually, the fault current is commutated from the last time-delaying branch into the arming branch. Here, the capacitor is charged to the clamping voltage of the MOV in the energy absorption branch. At this point, the UFD has reached sufficient voltage withstand capability to handle the counter voltage of the MOV. The MOV dissipates the system energy and forces the line current to zero. An advantage of the TD-HCB is its use of the SCR as the main semiconductor switch, which is a mature, reliable, and inexpensive technology [63] that gives a robust design [62]. Current controllability and

arcless operation are other advantages of the TD-HCB, similar to the P-HCB and the FB-HCB. A drawback is the long recovery time of the SCRs [64], which must be accounted for. Additional disadvantages are relatively high power losses, a relatively high number of semiconductor devices [65], and high capacitive energy-storage requirements [64, 65].

The bidirectional T-type breaker illustrated in Figure 2.9d is a mechanical HCB topology with an SCR-based pulse generator (PG-HCB) [66, 67]. When receiving a trip order, both ACCBs open. When they are fully open, the PG is triggered as the SCR is fired. This causes the precharged capacitor to discharge against the inductor, leading to high pulse currents through each of the ACCBs, causing zero-crossings and arc extinctions. Due to the anti-parallel diodes, the line current continues to flow, recharging the capacitor until the MOV becomes conductive. The MOV forces the line current to zero, and dissipates the source side network energy. The shunt branch (green) on the load side dissipates the load side energy. A key advantage of the PG-HCB compared to the solid-state HCBs is the negligible power losses, due to no semiconductor devices in the main branch. Another benefit is the use of the SCR as the main semiconductor switch. Furthermore, the PG-HCB design is simple, and it offers an inherent overvoltage protection of the DC-line [65]. The PG-HCB also has the benefit of separating the source and load sides, preventing the fault current from being reflected to the source side. An important drawback, however, is the high current stress on the SCRs, caused by the very high peak value of the current pulse being generated [66, 59]. Another disadvantage compared to the solid-state HCBs is the increased maintenance requirements due to arcing in the ACCBs. Furthermore, the use of a precharged capacitor can be a drawback, as a reliable charging solution may be challenging to obtain in some applications [68].

The voltage source converter assisted resonant current HCB (VARC-CB) shown in Figure 2.9e is a bidirectional breaker currently under development by the Swedish company SCiBreak AB. The concept was first discussed in [59]. [69, 70] present the most recent work on the breaker, including simulation and experimental results, which were performed within the PROMOTioN EU project. The breaker topology is very similar to that of the MCB in Figure 2.8, but the making switch S_{active} is replaced by a VSC. Correspondingly, the operating principles have many similarities. At a trip order, the ACCB opens. The ACCB is typically a vacuum interrupter (VI), just as for the active MCB. The current zero in the VI is achieved by the VSC performing successive reversals of its output voltage polarity, which excites a resonance in the passive LC circuit. As the VSC operates synchronously with the resonance, an oscillating current of increasing amplitude results, just as in the passive MCB scheme. However, as the resonant circuit current magnitude is controlled by the fast VSC switching, the magnitude build-up of the VARC-CB is significantly faster than for the passive MCB. At the current zero, the line current commutates to the current injection branch, charging C until the MOV clamping voltage is reached. The MOV then suppresses the line current to zero and dissipates the residual network energy. One challenging aspect of the VARC-CB topology is that the maintenance requirements are higher than for the solid-state HCBs due to arcing. A second challenge is the need for a reliable precharging method for the VSC capacitor. The key benefits of the concept are discussed below.

2.5.4 Choice of DCCB Concept for Further Study

The DCCB concept chosen for further study is the VARC-CB. It is a topical, promising technology currently under development with several prominent beneficial features. A key advantage is its low demand of semiconductor devices compared to several other HCB designs. The repetitive action of the VSC allows for a low VSC output voltage; the accumulated resonant current amplitude equals what would have been generated if the accumulated voltage steps had been applied to the LC circuit simultaneously [71]. As a result, the total voltage rating of the VSC switches is typically only a fraction (10–20%) of the expected maximum TIV level [59, 70, 72]. In comparison, the corresponding rating for the semiconductors of a bidirectional P-HCB is twice the TIV level [58]. Another benefit is the favorable conditions under which the VSC switches operate. As the VSC switching and the resonant current are synchronous, VSC operation close to zero current switching (ZCS) is achieved. Consequently, the VSC switches have very low turn-off current capability requirements. This is in contrast to the P-HCB and the FB-HCB, where the devices must be able to turn off the full or the half of the maximum fault current, respectively. Furthermore, compared to the PG-HCB, the semiconductor devices of the VARC-CB are exposed to considerably less current stress. Other benefits of the breaker topology are its simple design, its negligible steady-state power losses, and its bidirectional nature.

It should be mentioned that the VARC-CB is originally proposed as an HVDC concept, whereas the rest of this report focuses on the MVDC application of the breaker. More specifically, the work to be presented focuses on the operation, analysis, design, and modeling of one single VARC-CB module, similar to the one depicted in Figure 2.9e. The voltage rating of one such module is limited by the maximum voltage ratings of available single-break VIs, which currently is 145 kV [73]. Thus, one module is sufficient for MVDC use, although for HVDC applications, several modules must be series-connected [69]. As an HVDC VARC breaker employs MVDC VARC-CB modules as building blocks, many of the considerations, discussions, and results to be presented in the following chapters are valid and relevant for HVDC applications as well. Nevertheless, the challenges and design considerations related to the series-connection of modules are not considered, all of which must be investigated in detail if the breaker concept is to be applied at higher voltage levels.

Chapter 3

Operating Principles of the MVDC VARC-CB

The aim of this chapter is to explain the operating principles of the MVDC VARC-CB more comprehensively than was done in Subsection 2.5.3. More detailed schematics of the VARC-CB module are presented, and typical current and voltage waveforms, together with a typical timing sequence for the breaker operation are shown and described. These considerations create a basis and framework for the more in-depth analytical investigations of the MVDC VARC-CB to be presented in Chapter 4.

3.1 Breaker Topology

A schematic of the VARC-CB topology is given in Figure 3.1, which also includes the current and voltage directions which will be employed throughout this chapter. As was indicated in Figure 2.9e, the topology has three principal branches: the main branch, the current injection branch, and the energy absorption branch. Different from the schematic in Figure 2.9e, the main branch in Figure 3.1 also includes a current-limiting inductor L_{lim}, and a residual current breaker (RCB). The task of the inductor is to limit the rate of rise of fault currents, and to limit the peak currents to values the VARC-CB module is able to handle. The function of the RCB is to provide galvanic isolation by opening when the VARC-CB has forced the line current to zero. The RCB is not capable of breaking nominal DC currents, but can break small residual currents which may be present after the VARC-CB has performed a successful interruption process [8].

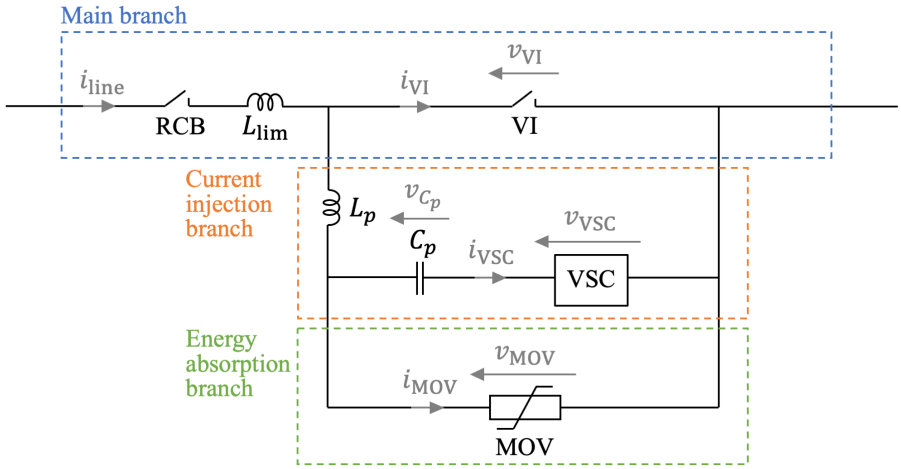


Figure 3.1: Topology of the MVDC VARC-CB module.

Details of the VSC structure are displayed in Figure 3.2, showing that the VSC is a full-bridge single-phase converter topology with four switch positions. The VSC is illustrated with switch positions consisting of IGBTs (S_1–S_4) with anti-parallel diodes (D_1–D_4), as this is the semiconductor device technology proposed in the existing literature on the VARC-CB. A DC link is connected between the two bridge legs of the converter. The link contains an energy storage capacitor, C_{DC}, together with its charging circuit. The charging circuit consists of a DC voltage supply, V_{DC}, a charging resistor, R_{CH}, and a switch, S_{CH}.

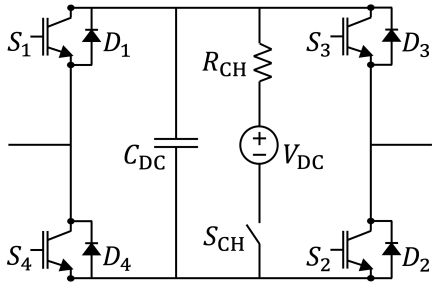


Figure 3.2: Structure of the VSC in the VARC-CB topology.

3.2 Operating Principles and Timing Sequence

Figure 3.3 includes relevant current and voltage waveforms of the breaker during a typical fault current interruption process. The directions of the currents and voltages included in the figure are all indicated in the schematic in Figure 3.1.

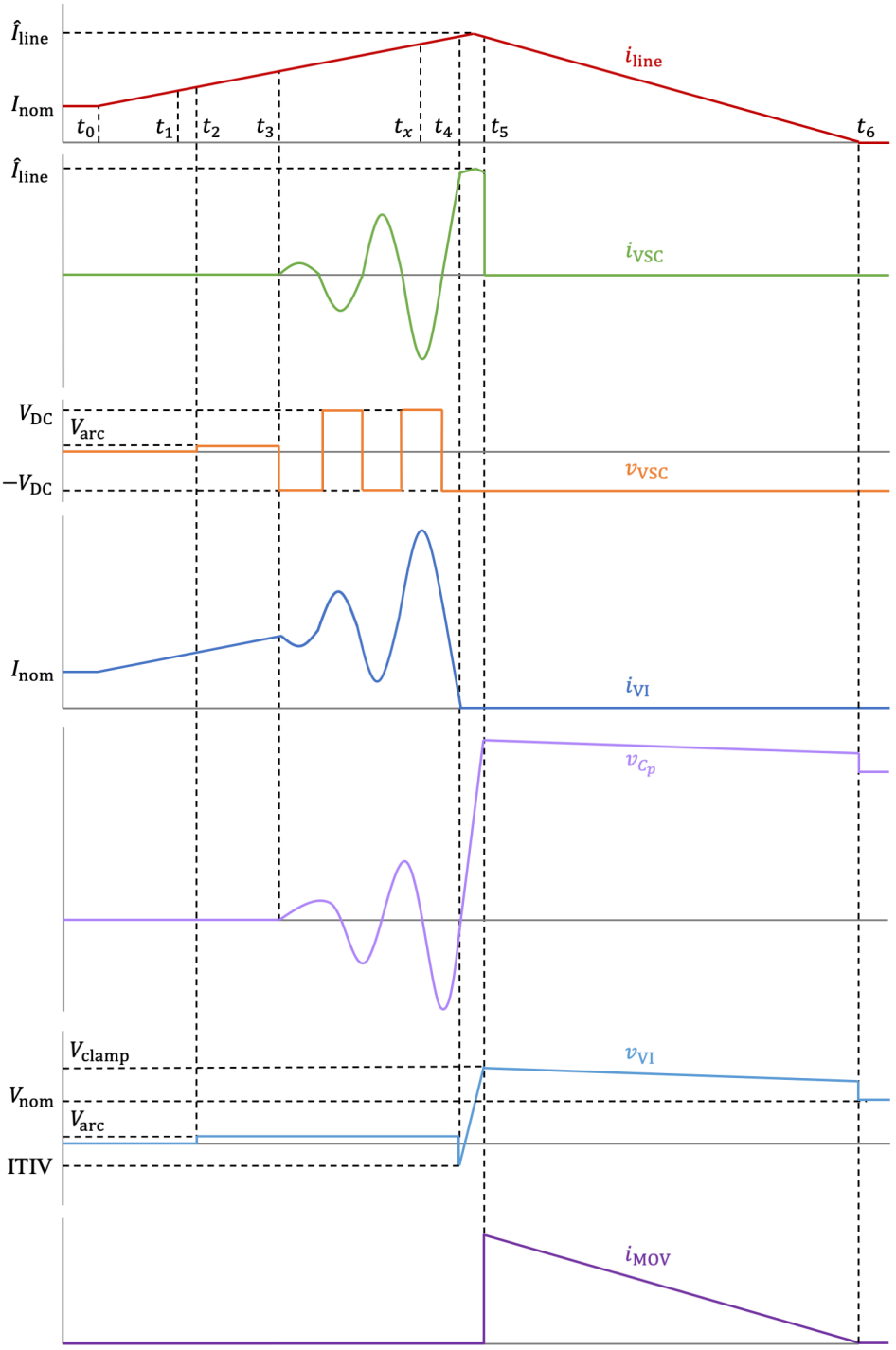


Figure 3.3: Current and voltage waveforms illustrating the operation of the VARC-CB.

Table 3.1 provides a short explanation of the operation sequence in Figure 3.3 by describing and defining essential time instants and intervals. In the subsections which follow, the operating principles of the VARC-CB module are explained and investigated using Figure 3.3 and Table 3.1 as a basis.

Table 3.1: Operation sequence of the VARC-CB during a typical fault current interruption process, as presented in Figure 3.3.

Time instant/ interval	**Notation**	**Description**
Before t_0	-	Steady state
t_0	-	Fault inception
t_0–t_1	t_{rel}	Relay time
t_1	-	VI receives trip signal from the relay
t_1–t_2	t_{act}	VI actuation delay
t_2–t_x	t_{open}	VI opening time, $t_x \leq t_4$
t_2–t_3	$t_{\text{VSC,delay}}$	Delay of VSC triggering w.r.t. the initial VI contact separation
t_3	-	VSC activation
t_3–t_4	t_{VSC}	VSC operation time
t_4	-	Local current interruption in the VI, i_{line} commutates to current injection branch
t_4–t_5	-	i_{line} charges C_p until clamping voltage of MOV is reached
t_5	-	Clamping voltage of MOV reached, i_{line} commutates to energy absorption branch
t_5–t_6	-	MOV operation time
t_6	-	Line current zero

It should be pointed out that the illustration in Figure 3.3 demonstrates idealized and somewhat simplified waveforms of the VARC-CB, as the purpose of the figure is to show the principal operation of the breaker. In particular, the proportions in the figure are not to scale, and some particularities of the breaker behavior are left out.

3.2.1 Before t_0: Steady State and Charging of the DC Link

Prior to the fault inception, the VARC-CB operates in steady state, and the nominal system current, I_{nom}, flows through the breaker. In this state, the contacts of the VI and of the RCB are closed, providing a current path of very low resistance. The four switch positions in the VSC are all in their off-state. In practice, there will be small leakage currents flowing in the current injection and energy absorption branches. However, the voltage across these

branches during steady state equals the VI voltage drop, which is very small: assuming a nominal current in the kiloampere range, the VI voltage drop will typically be in the range of millivolts. Consequently, the leakage currents in the current injection and energy absorption branches can be regarded as negligible, and the full line current can be assumed to pass through the main branch.

In order for the VARC-CB to operate properly during a current interruption process, the DC link capacitor, C_{DC}, must be precharged. The charging of C_{DC} must therefore happen before t_0. The charging is initiated by closing the switch S_{CH}, at which a charge transfer from the voltage supply to the capacitor begins. The capacitor will then gradually charge up through the charging resistor R_{CH}, with a charging rate described by the time constant $\tau_{\text{CH}} = R_{\text{CH}}C_{\text{DC}}$. When the capacitor voltage reaches the supply voltage V_{DC}, the charging current approaches zero asymptotically. At this point, S_{CH} is opened, hence disconnecting the charging circuit, to prevent it from interfering with the breaker operation.

3.2.2 $\mathbf{t_0}$: Fault Inception

At t_0 a fault occurs in the system in which the VARC-CB is connected, causing the line current to rise from its nominal value. The rate of rise of the line current is dictated by the total inductance it encounters, including L_{lim}, line/cable inductance, and stray inductances of various components in the system.

3.2.3 $\mathbf{t_0}$–$\mathbf{t_1}$: Relay Time

The time between t_0 and t_1, the relay time, is the time required by the protective relays in the system for fault detection, discrimination and coordination. This time interval also includes signal delays in the protection and detection circuitry. The relaying can be implemented using different techniques, e.g. direct measurement methods such as distance, differential or overcurrent protection, or signal processing methods such as protection based on traveling waves, derivatives, wavelets or neural networks [74]. Regardless of the method applied, there will be a finite time interval between the occurrence of the fault, t_0, and the instant at which the VARC-CB receives a trip signal sent from the relay, t_1.

3.2.4 $\mathbf{t_1}$–$\mathbf{t_2}$: VI Actuation Delay

At t_1 the VI of the VARC-CB receives the trip signal, and its actuator initiates the VI opening process. There will, however, be a short delay in the operation of the actuator, meaning that the initial contact separation is slightly delayed with respect to the trip instant [69, 75]. The contacts start to separate at t_2.

3.2.5 $\mathbf{t_2}$–$\mathbf{t_3}$: VI Opening, VSC Not yet Activated

When the VI starts to open at t_2, an electric arc is formed between its contacts, as explained in Subsection 2.3.1. Resultantly, the voltage across the VI terminals and across the VSC increase from their steady state values of approximately zero to the voltage of the burning arc. This constant value is denoted by V_{arc} in Figure 3.3.

In the time interval between t_2 and t_3 the VI actuator lengthens the interrupter's contact gap towards a distance sufficient for withstanding the TIV. In this time interval, the VSC is not yet activated. As a result, the current passing through the VI, i_{VI}, equals the line current, i_{line}, which keeps rising. The rate of rise of the line current is now lower than prior to t_2, due to the presence of the constant arc voltage. The arc voltage is, however, very low compared to the nominal system voltage, thus too low to affect the rising rate significantly.

3.2.6 t_3–t_4: VSC Switching

At t_3 the VSC is activated, and it starts to execute switching operations. This is continued until t_4. In this time interval, the loop formed by the current injection branch and the VI is of interest, hence a schematic of this loop is displayed in Figure 3.4. As the charging circuit of C_{DC} is disconnected at this point, the elements of this circuit are not shown.

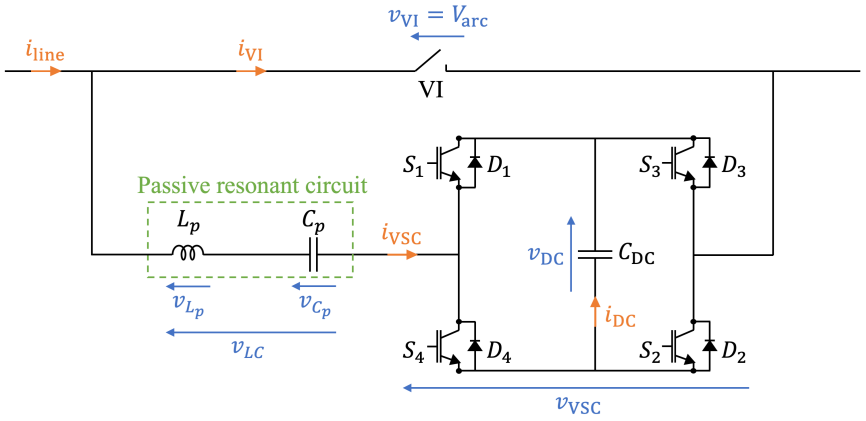


Figure 3.4: The loop formed by the VI and the current injection branch.

The switching of the VSC is carried out with a square wave switching scheme. The frequency of the square wave equals the resonance frequency of the passive resonant circuit, f_{LC}, which is given by Equation (3.1).

$$f_{LC} = \frac{1}{2\pi\sqrt{L_p C_p}} \tag{3.1}$$

In this switching scheme, the switches (S_1, S_2) and (S_3, S_4) are treated as two switch pairs. This means that the two switches within each pair receive identical signals to their gates, and that the pairs are provided with complementary gate signals. In this way, one switch pair is always on, and each pair has a duty ratio of 50%.

Figure 3.5 shows how the current in the injection branch flows in the two possible switching states of the VSC. The green line is the current path when the pair (S_1, S_2) is in its on-state, and (S_3, S_4) in its off-state. The orange path shows the current flow when (S_3, S_4) is on, and (S_1, S_2) is off. As can be seen, the current direction through the passive resonant circuit reverses when the switch pair changes. The current direction through the

DC link, on the other hand, is constant. This has a discharging effect on C_{DC}, meaning that the flow of current results in a decrease of the DC link voltage v_{DC}. However, for the purpose of explaining the basic operating principles during t_3–t_4, the value of v_{DC} will be assumed constant at the precharged level of V_{DC}.

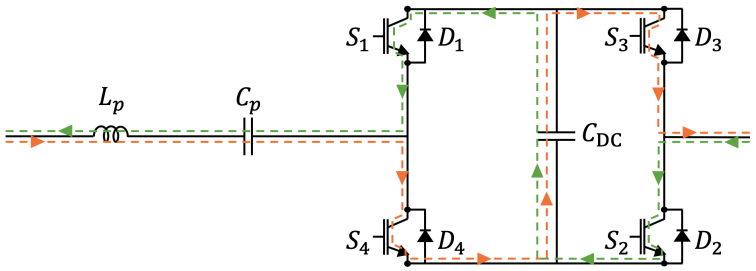


Figure 3.5: Current flow in the current injection branch during VSC switching.

In the case illustrated in Figure 3.3, the switch pair (S_3, S_4) is the first to be turned on. This can be observed by v_{VSC} obtaining the value $-V_{\text{DC}}$ at t_3. By employing Kirchhoff's voltage law in the loop in Figure 3.4, the voltage across the passive resonant circuit can be expressed as $v_{LC} = V_{\text{arc}} - v_{\text{VSC}}$. Consequently, at t_3, v_{LC} experiences a step in its value from zero to $V_{\text{arc}} + V_{\text{DC}}$. However, as the arc voltage will be considerably smaller than V_{DC}, a step from zero to V_{DC} is considered. This step applied to the resonant circuit results in a positive sinusoidal pulse appearing in i_{VSC}, as seen in Figure 3.3. This pulse has a frequency of f_{LC}, and its peak has a magnitude of I_{osc}, which is given by Ohm's law in Equation (3.2). In this equation, Z_{LC} denotes the characteristic impedance of the resonant circuit, i.e its reactance at the resonance frequency. The value of Z_{LC} can be found by means of Equation (3.3).

$$I_{\text{osc}} = \frac{V_{\text{DC}}}{Z_{LC}} \tag{3.2}$$

$$Z_{LC} = \sqrt{\frac{L_p}{C_p}} \tag{3.3}$$

As the VSC switching frequency is f_{LC} and the VSC switch pairs have a duty ratio of 50%, (S_3, S_4) turns off when i_{VSC} crosses zero at $t = t_3 + \frac{1}{2f_{LC}}$. At the same time, ($S_1$, S_2) turns on, hence reversing the value of v_{VSC} from $-V_{\text{DC}}$ to $+V_{\text{DC}}$. Consequently, a voltage step of $-2V_{\text{DC}}$ appears in v_{LC}. This results in a negative current pulse of amplitude $2I_{\text{osc}}$ being added to i_{VSC}, giving an accumulated amplitude of $3I_{\text{osc}}$. This can be seen as the first negative peak of i_{VSC} in Figure 3.3.

Since the VSC switching is synchronized with the oscillations in i_{VSC}, each consecutive switching operation results in an addition of $2I_{\text{osc}}$ to the amplitude of i_{VSC}. Consequently, after the N^{th} switching operation, the amplitude of the oscillating current will be $(2N-1)I_{\text{osc}}$. This corresponds to the peak value of the pulse resulting from *one* voltage step of $(2N-1)V_{\text{DC}}$ being applied to the passive resonant circuit (which is the concept upon which the MCB with active current injection discussed in Subsection 2.5.1 is based).

Having current directions as in Figure 3.4, a positive i_{VSC} pulse with a peak equal to or exceeding i_{line} is needed to create a zero-crossing in i_{VI}. In Figure 3.3, the 5^{th} peak is the first positive peak exceeding i_{line}. At t_4, slightly before i_{VSC} reaches its fifth peak, a current zero thus occurs in i_{VI}, the VI arc is extinguished, and the VI stops conducting.

Since i_{VSC} during t_3–t_4 is a sinusoidal wave of increasing amplitude, v_{C_p} is also sinusoidal with increasing amplitude, lagging the i_{VSC} curve by 90°. Assuming no losses in the i_{VSC} loop and still assuming $v_{\text{DC}} = V_{\text{DC}}$, the first peak of v_{C_p} will have a magnitude of $2V_{\text{DC}}$, and each consecutive VSC switching adds another $2V_{\text{DC}}$ to the peak value. The v_{C_p} amplitude will thus reach $2N \cdot V_{\text{DC}} = 2N \cdot Z_{LC} I_{\text{osc}}$ after the N^{th} switching operation.

It should be noted that the activation of the VSC is delayed a time $t_{\text{VSC,delay}}$ with respect to the initial contact separation in the VI. The reason for this delay is the significant difference in operation time between the VI and the VSC [59, 71]. The opening time of the VI, t_{open}, is in the order of a few milliseconds [75]. As the VSC typically operates at a frequency in the kHz range, it can perform several switching operations during the time interval needed for the VI to mechanically separate its contacts. Due to this fast-acting nature of the VSC, its activation must be delayed to ensure that the zero-crossing in the VI is not generated before the contact gap is of sufficient length to handle the TIV. For the case in Figure 3.3 this means that the time instant t_x, indicating the point at which the VI reaches enough voltage withstand capability, should occur before t_4.

It should also be mentioned that due to the use of an oscillating current to create an i_{VI} zero-crossing, the VARC-CB is bidirectional by nature [71]. As a result, the operation of the VSC, and the VARC-CB in general, could just as well have been explained for a case where i_{line} initially had a direction opposite to that shown in Figures 3.1 and 3.4.

3.2.7 t_4–t_5: Charging of C_p

At t_4 the line current commutates from the VI into the current injection branch, which causes C_p to charge up in the time interval t_4–t_5. As the line current is approximately constant at $\hat{I}_{\text{line}}$ in this interval, the rise in v_{C_p} is close to linear, as seen in Figure 3.3. C_p charges until the MOV voltage, which is given by the sum $v_{C_p} + v_{\text{VSC}}$, reaches the MOV clamping voltage, V_{clamp}. At this point, the MOV becomes conductive, and the line current commutates into the energy absorption branch. This is observed in Figure 3.3 at t_5 by i_{VSC} becoming zero, and i_{MOV} rising from zero to the value of the line current.

At t_4 a drop in the VI voltage is observed: v_{VI} drops down from V_{arc} to the value of the initial transient interruption voltage (ITIV). If neglecting stray components and any impact from the surrounding network, the value of the ITIV is given by the sum of $v_{\text{VSC}}(t_4)$ and $v_{C_p}(t_4)$ ($v_{L_p}(t_4)$ is neglected due to the relatively small di/dt of the line current, which now flows through L_p). The VSC has at this point stopped performing switching operations, as no further excitation of the i_{VSC} amplitude is needed. The VSC is thus left in its switching state prior to t_4, with the switch pair (S_3, S_4) being on. This gives $v_{\text{VSC}}(t_4) = -V_{\text{DC}}$. The value of $v_{C_p}(t_4)$ highly depends on where on the i_{VSC} curve the current interruption in the VI occurs. If $i_{\text{VI}} = 0$ is achieved exactly at the peak of i_{VSC}, the value of $v_{C_p}(t_4)$ will be zero. However, if $i_{\text{VI}} = 0$ occurs slightly before i_{VSC} reaches its positive peak, v_{C_p} will have a finite negative value. In either case, the value of ITIV = $v_{C_p}(t_4) - V_{\text{DC}}$ is negative, causing the voltage drop observed in v_{VI} at t_4.

After reaching the ITIV, v_{VI} rises close to linearly, which is due to the charging of C_p. Still assuming v_{L_p} to be negligible, the VI voltage will be equal to the MOV voltage. Consequently, the maximum v_{VI} value is V_{clamp}, which is reached at t_5 in Figure 3.3.

It should be noted that the size of the time interval t_4–t_5 is exaggerated in Figure 3.3. Due to the high value of the line current and the low value of C_p, the rate of rise of v_{C_p} is high, causing V_{clamp} to be reached rapidly after the arc extinction at t_4. The interval is, however, enlarged in the figure, to be able to display the details of the waveforms clearly.

3.2.8 $\mathbf{t_5}$–$\mathbf{t_6}$: MOV Operation

Slightly before t_5, v_{VI} exceeds the nominal system voltage V_{nom}. At this point, the di/dt of the line current turns negative. Consequently, i_{line} reaches its peak value, $\hat{I}_{\text{line}}$, after which it begins to decline. When V_{clamp} is reached at t_5, the line current commutates into the MOV, and the MOV clamps the voltage across the VARC-CB. As V_{clamp} is higher than V_{nom}, the decrease of i_{line} towards zero continues. $i_{\text{line}} = 0$ is reached at t_6.

During this time interval, the energy stored in and fed into the system is dissipated in the MOV. The time needed, i.e. the duration of t_5–t_6, depends on the system configuration, and also on the characteristics of the MOV.

The decrease of i_{line}, hence the decrease of the MOV current, results in a reduction in the MOV voltage, ref. the normal varistor operation region of the MOV V-I curve in Figure 2.6b. The MOV voltage does therefore not stay constant at V_{clamp} during t_5–t_6, but decreases slightly, as can be seen in v_{VI} in Figure 3.3.

In Figure 3.3 it is assumed that the MOV does not conduct any current before V_{clamp} is reached at t_5. This is, however, not the case. As is shown in Figure 2.6b and discussed in Section 2.4, there is a small leakage current flowing in the leakage operation region of an MOV. In addition, the transition to the normal varistor operation region (the clamping region) is gradual. Consequently, as v_{C_p} increases in amplitude during the VSC operation time, also the amplitude of v_{MOV} increases, resulting in an MOV leakage current growing in magnitude. For simplicity, however, i_{MOV} shown in Figure 3.3 is considered to be zero until V_{clamp} is reached.

3.2.9 $\mathbf{t_6}$: Line Current Zero

At t_6 the line current has been forced to zero by the counter voltage produced by the MOV. Ideally, the VI voltage then drops to nominal system voltage level, and all currents stay at zero, as shown in Figure 3.3. There will, however, be some leakage current flowing through the MOV. In addition, a resonant operation of the capacitance of the VARC-CB module and its series-connected inductance will be initiated, causing a transient response in i_{line}, i_{VSC}, and v_{MOV} [50, 69]. Consequently, there will be some residual current flowing after t_6. When this current reaches a level within the capability of the RCB, it is removed by the RCB opening, and galvanic isolation is provided between the VARC-CB module and the rest of the system. The MOV leakage current, the transient responses, and the RCB opening are not illustrated in Figure 3.3.

Chapter 4

Analytical Investigation and Design of the MVDC VARC-CB

While the previous chapter described the basic operating principles of the VARC-CB, this chapter presents a more in-depth analysis and mathematical modeling of the breaker operation and the breaker's subcomponents, with the aim of proposing design strategies for the VARC-CB module. The first and second sections define a set of design goals and a design system, respectively, hence providing a framework for the analysis and design process. Thereafter follows the main section, where the analytical investigation is performed, and the design strategies are derived. This section investigates and discusses the factors to be taken into account when designing a VARC-CB. In particular, attention is given to how the values of the breaker parameters should be selected in order to satisfy the defined design goals without violating any of the constraints imposed by the breaker's subcomponents. The very last subsection summarizes the derived equations and criteria, providing a complete set of strategies to be used when designing the parameters of an MVDC VARC-CB.

4.1 Design Goals

Before initiating a design process, a set of design goals and objectives should be defined, as this creates a baseline for the process. There might be different design goals when designing DCCBs, and the importance of each goal will depend on the application area in which the CB is to be used. For the purpose of designing a VARC-CB module for MVDC, the following design objectives can be considered significant:

1. **Minimization of total operation time.** The total operation time of the VARC-CB is the time from the VI receives a triggering signal from the relay until the line current has been forced to zero. If the breaker operates rapidly, the relevant section or line will quickly be disconnected from the remaining power grid, and normal operation can be restored. This will limit the stress experienced by system components and also the subcomponents of the breaker.

2. **Minimization of maximum breaker current.** Similar to the total operation time, the peak value of the current to be interrupted by the breaker should be minimized in order to limit the stress experienced by the breaker and other grid components.

3. **Minimization of passive components.** The VARC-CB has passive components in its topology. As high-power passive elements are bulky and costly, designing them as small as possible is beneficial in terms of breaker weight, size, and cost.

4. **Minimization of the number of and ratings of power semiconductor devices.** Power semiconductor devices are, like high-power passive elements, of high cost, with the cost typically increasing with power-handling capability. Furthermore, a large number of devices can complicate the breaker design, in particular if series- and/or parallel connections of devices are needed. It is therefore desirable to limit the number of devices, and also their ratings.

5. **High reliability.** The breaker's reliability is related to the degree of certainty that the breaker will function and perform as expected [76]. If the breaker fails to operate as intended, harmful currents may result, causing excessive stress on or damage to components and equipment. High reliability is thus a wanted feature of the breaker.

6. **Low complexity**. It is desirable that the physical implementation resulting from the final design has low complexity, as high complexity often comes at a cost of reduced reliability. Dependency on highly sophisticated methods or circuitry for realizing the final design should hence preferably be avoided. Low complexity is also desirable for the design process itself, e.g. in terms of easy-to-use equations which are possible to solve without needing highly advanced methods.

4.2 Design System

Figure 4.1 displays the simplified MVDC system considered for the analysis and design process, and also for the Simulink simulations (see Chapter 5), of the VARC-CB module.

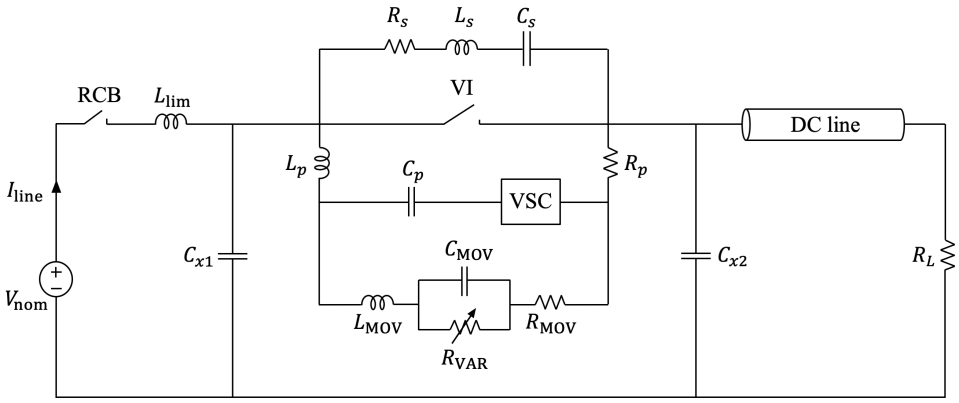


Figure 4.1: Design system.

The system in Figure 4.1 is asymmetric monopole, and contains an MVDC source having a constant voltage equal to the system rating of V_{nom}. The source feeds a nominal current of $I_{\text{line}} = I_{\text{nom}}$ to a purely resistive load R_L through a DC line. The line has a certain resistance, inductance and capacitance per length, which can be denoted by r_{line}, l_{line}, and c_{line}, respectively. Using the total line distance, d_{line}, the accumulated parameter values of the line can be found. These accumulated parameters, which are not displayed in the figure, will be denoted by R_{line}, L_{line}, and C_{line}, respectively.

A VARC-CB module is connected close to the MVDC voltage source. Comparing the module in Figure 4.1 to the simplified schematic presented in Figure 3.1, some topological modifications can be observed. These changes have been made to obtain a more realistic model, hence more accurate breaker behavior. First, the resistance R_p has been added to the topology. This is a stray resistance representing the losses in the lead resistance and in the passive components of the current injection branch, with the inductor losses being predominant [72]. This resistance is, as will become evident in Subsection 4.3.2.3, essential for deriving more realistic dynamics of v_{DC} and i_{VSC} than the ones presented in Subsection 3.2.6. Second, a branch containing R_s, L_s, and C_s has been added in parallel to the VI. This is the stray branch of the VI, representing the parasitic parameters of the VI gap [77, 78]. As this branch impacts the course of v_{VI} after the VI current zero-crossing, it is important to include. Third, the MOV representation has been made more detailed and accurate by employing the equivalent circuit discussed in Subsection 2.4.1.

Two capacitors, C_{x1} and C_{x2}, are included between the VARC-CB and ground, one on each side of the module. They represent the total stray capacitance of all the equipment, such as bushings, busbars, the RCB, lightning arresters, instrument transformers, etc., which will be connected to each side of the module in a real-life DC system [39]. It is crucial that the effect of these stray capacitances are considered in order to obtain realistic voltage stress on the VI after its current zero-crossing. This is discussed in further detail in Subsection 4.3.4.3.

The VARC-CB should be capable of interrupting I_{line} during different scenarios, i.e. the breaker must be able to interrupt a range of currents. Typically, the range covers the minimum and maximum possible fault currents. It can also include currents for a variety of load cases, if the breaker is to be used for interrupting load currents in addition to fault currents. This range is an important input parameter when designing the VARC-CB, and will be denoted by $[I_{i,\text{min}}, I_{i,\text{max}}]$, where $I_{i,\text{min}}$ is the lowest possible/allowable value of I_{line} at the point of interruption ($\hat{I}_{\text{line}}$), whereas $I_{i,\text{max}}$ is the highest.

4.3 Design Strategies

In this section, design strategies for the VARC-CB module are derived. The section has five subsections, with each of the first four presenting a thorough analysis of one subcomponent of the module. For each subcomponent, design considerations for its parameter(s) are discussed, and parameter design equations are deduced. In addition, potential constraints imposed on the breaker design by the subcomponent are identified, upon which design criteria are suggested. The last subsection summarizes all the proposed design strategies.

4.3.1 The Current-Limiting Inductor

The inductance value of the current-limiting inductor, L_{lim}, must be set to limit the maximum value of the line current, $\hat{I}_{\text{line}}$, during interruption. The highest possible value of $\hat{I}_{\text{line}}$ occurs when the total inductance and resistance present to limit the rate of rise of the current is at minimum. This happens for a terminal fault, i.e an SC fault occurring close to the line terminal of the breaker. By assuming the resistance the line current encounters to be negligible, and by neglecting the arc voltage of the VI, the rate of rise of the line current during a terminal SC fault can be approximated by

$$\frac{di_{\text{line}}}{dt} = \frac{V_{\text{nom}}}{L_{\text{lim}}}$$

$\hat{I}_{\text{line}}$ occurs during the time interval t_4–t_5 in Figure 3.3. However as this interval is relatively short, $i_{\text{line}}(t_4) = \hat{I}_{\text{line}}$ is assumed, for simplicity. Assuming $t_0 = 0$, the value of $\hat{I}_{\text{line}}$ is then given by

$$\hat{I}_{\text{line}} = I_{\text{nom}} + \frac{di_{\text{line}}}{dt} \cdot t_4 = I_{\text{nom}} + \frac{V_{\text{nom}}}{L_{\text{lim}}} \cdot t_4$$

As the maximum line current the VARC-CB is to be able to interrupt is $I_{i,\text{max}}$, the following design criterion for L_{lim} can be derived:

$$\hat{I}_{\text{line}} = I_{\text{nom}} + \frac{V_{\text{nom}}}{L_{\text{lim}}} \cdot t_4 \leq I_{i,\text{max}}$$

$$\Rightarrow \quad L_{\text{lim}} \geq \frac{V_{\text{nom}} \cdot t_4}{I_{i,\text{max}} - I_{\text{nom}}} \tag{4.1}$$

Using Equation (4.1) when designing L_{lim} will ensure that $I_{i,\text{max}}$ is not exceeded, regardless of the fault location.

The value of t_4 is given by the sum $t_{\text{rel}} + t_{\text{act}} + t_{\text{VSC,delay}} + t_{\text{VSC}}$: it is the sum of the total time needed for fault detection, discrimination, and coordination, the actuation delay in the VI, the delay of the VSC triggering with respect to initial VI contact separation, and the total operation time of the VSC. Introducing this notation into Equation (4.1) gives

$$L_{\text{lim}} \geq \frac{V_{\text{nom}} \cdot (t_{\text{rel}} + t_{\text{act}} + t_{\text{VSC,delay}} + t_{\text{VSC}})}{I_{i,\text{max}} - I_{\text{nom}}} \tag{4.2}$$

The relay time highly depends on the detection method used, whereas the actuation delay in the VI is decided by the actuator employed for operating the VI. The delay between the initial VI contact separation and the triggering of the VSC, $t_{\text{VSC,delay}}$, and the total VSC operation time, t_{VSC}, are, however, to a large extent determined by the parameter design of the VARC-CB module. This will be discussed in more detail in Subsection 4.3.4.1.

4.3.2 The Voltage Source Converter

The VSC consists of four switch positions together with a DC link capacitor and its associated charging circuit, as displayed in Figure 3.2. This subsection discusses design aspects for each of these subparts, as well as for the switching frequency of the converter.

4.3.2.1 The Switching/Resonance Frequency

As already mentioned in Subsection 3.2.6, the switching operations performed by the VSC are supposed to be in synchronism with the oscillating current they excite. Consequently, the switching frequency of the VSC, f_{sw}, must be equal to the resonance frequency of the passive resonant circuit, f_{LC}:

$$f_{\text{sw}} = f_{\text{LC}} \tag{4.3}$$

f_{LC} is given by Equation (3.1), which is repeated here, for convenience:

$$f_{LC} = \frac{1}{2\pi\sqrt{L_p C_p}} \tag{3.1 revisited}$$

From Equation (3.1) it is seen that a high frequency allows for small values of L_p and C_p. A high switching frequency is therefore in line with the design goal of minimizing the passive components present in the breaker topology.

4.3.2.2 The Power Semiconductor Switches

The type of power semiconductor device and its ratings must be selected to be able to handle the conditions under which it operates in the VARC-CB. At the same time, the design of the VARC-CB parameters must take the switch ratings into account, and ensure that they are not violated. There are mainly three parameters of the VARC-CB which are decisive for the choice of switch type and ratings: the precharged voltage level of the DC link capacitor, the current interruption capability, and the VSC switching frequency.

The initial voltage across the DC link capacitor, V_{DC}, is the maximum voltage the switch positions will be exposed to in their blocking state. A switching device with maximum blocking voltage capability exceeding V_{DC} must therefore be selected. This indicates that a lower value chosen for V_{DC} allows for devices of lower voltage ratings.

An important property of the semiconductor devices employed, is their ability to carry high current. As shown in Figure 3.3, the maximum value of i_{VSC} equals the maximum value of the fault current. The current interruption capability of the VARC-CB therefore defines the maximum current the VSC switches must be able to conduct. It should be noted that the switches are required to carry this maximum current only for a very short time (ref. Figure 3.3). As a result, it is the ability of the switch to carry high pulsed currents which is of interest; the continuous current rating of the switch can therefore be lower than the VARC-CB's interruption capability.

The VSC switches impose an upper limit on the switching frequency of the VSC, as there is a maximum frequency the switches are able to handle. If denoting this maximum frequency limit by $f_{S,\text{max}}$, the following design criterion for the switching/resonance frequency can be formulated:

$$f_{LC} \leq f_{S,\text{max}} \tag{4.4}$$

Typically, the value of $f_{S,\text{max}}$ is limited by thermal constraints of the semiconductor device [79, 80]. A thorough thermal analysis is beyond the scope of this thesis. However, it should be emphasized that the $f_{S,\text{max}}$ of the switches to be utilized in the VARC-CB's VSC can probably be pushed higher than for similar devices used in conventional hard-switched power converters. This is due to the favorable, soft switching conditions of the VSC switches. As the converter switching is in-phase with i_{VSC}, the commutations in the VSC are ideally executed at the zero-crossings of i_{VSC}. However, due to required dead time and possibly some asynchronism between v_{VSC} and i_{VSC}, the switching operations do not occur exactly at current zeros. Nevertheless, the VSC will operate with close to ZCS conditions. This results in low turn-on- and turn-off current capability requirements, and reduced switching energy losses compared to under conventional hard-switched conditions. In addition, the VSC operates seldom (only when the VARC-CB is triggered), and the duration of each operation is short. Consequently, the thermal stress on the VSC switches will be lower than that experienced by switches in typical converter applications, where the semiconductor devices are required to operate continuously.

4.3.2.3 The DC Link

The DC link of the VSC contains a capacitor, of which the capacitance C_{DC}, and the initial, precharged voltage V_{DC} are the parameters to be designed. The C_{DC} and V_{DC} values are decisive for the magnitude of each voltage step applied to the passive resonant circuit during the VSC switching. Consequently, the two parameter values have a significant impact on the growth of the i_{VSC} amplitude.

In Subsection 3.2.6 the DC link voltage, v_{DC}, was assumed constant at V_{DC} throughout the VSC operation time. This will not be the case in reality. Due to energy being transferred from the DC link capacitor, a decrease in v_{DC} during t_3–t_4 results. One part of this energy is brought into the passive resonant circuit, exciting the oscillating current, hence giving rise to the increase of the i_{VSC} amplitude. The rest of the energy is the amount required to cover the losses present in the i_{VSC} loop (the loop displayed in Figure 3.4).

The decrease in v_{DC} results in each VSC switching operation being slightly less effective than the preceding one. Ideally, each switching operation except the very first results in $2V_{\text{DC}}/Z_{LC}$ being added to the i_{VSC} amplitude, as discussed in Subsection 3.2.6. However, with v_{DC} decreasing, the increase in the i_{VSC} retards with time.

The v_{DC} and i_{VSC} dynamics during t_{VSC} can be described using a mathematical model. A simple model can be obtained by disregarding the details of i_{VSC}, and instead only consider the positive i_{VSC} envelope, $\hat{i}_{\text{VSC}}$, as presented in [72]. Letting

$$t^* = t - t_3 \tag{4.5}$$

with $0 \leq t^* \leq t_{\text{VSC}}$, the dynamics of $\hat{i}_{\text{VSC}}$ can be described as

$$\frac{d\hat{i}_{\text{VSC}}(t^*)}{dt^*} = \frac{d\hat{i}^{\text{grow}}_{\text{VSC}}(t^*)}{dt^*} + \frac{d\hat{i}^{\text{loss}}_{\text{VSC}}(t^*)}{dt^*} \tag{4.6}$$

where $d\hat{i}_{\text{VSC}}^{\text{grow}}(t^*)/dt^*$ is an exciting term, and $d\hat{i}_{\text{VSC}}^{\text{loss}}(t^*)/dt^*$ is a loss term. The exciting term represents the amplitude increase due to the boost from the VSC switching, whereas the loss term represents the amplitude growth retardation due to losses in the i_{VSC} loop.

At each VSC switching operation except the very first, a voltage step of $2v_{\text{DC}}(t^*)$ is applied to the passive resonant circuit, and the i_{VSC} amplitude is increased by $2v_{\text{DC}}(t^*)/Z_{LC}$. Equation (4.7) thus results, with N being the number of switching operations:

$$\frac{d\hat{i}_{\text{VSC}}^{\text{grow}}(t^*)}{dN} = \frac{2v_{\text{DC}}(t^*)}{Z_{LC}} \tag{4.7}$$

With a switching frequency of f_{LC}, the number of switching operations is given by $N = 2f_{LC}t^*$. Inserting this into Equation (4.7) gives an expression for the exciting term:

$$\frac{d\hat{i}_{\text{VSC}}^{\text{grow}}(t^*)}{dt^*} = \frac{d\hat{i}_{\text{VSC}}^{\text{grow}}(t^*)}{dN}\frac{dN}{dt^*} = \frac{2v_{\text{DC}}(t^*)}{Z_{LC}} \cdot 2f_{LC} = \frac{4f_{LC}v_{\text{DC}}(t^*)}{Z_{LC}} \tag{4.8}$$

To obtain an expression for the loss term, the losses in the loop in Figure 3.4 must be considered. The loop energy losses are comprised of several contributions, including losses in L_p, C_p, and C_{DC}, losses in S_1–S_4 (mainly conduction losses), and energy dissipated in the VI arc. As the losses in the passive components, in particular the inductor, play the most important role [72], it is assumed that the total loop losses can be described using the stray resistance R_p, which is shown in Figure 4.1. This resistance causes the i_{VSC} amplitude to decay with an exponential factor. Introducing the quality factor $Q = Z_{LC}/R_p$, the exponential factor can, by using RLC circuit theory, be expressed as follows:

$$e^{-\frac{R_p t^*}{2L_p}} = e^{-\frac{Z_{LC} t^*}{2QL_p}} = e^{-\frac{t^*}{2Q}\cdot\frac{1}{\sqrt{L_pC_p}}} = e^{-\frac{\pi f_{LC} t^*}{Q}}$$

As a result, the loss term can be expressed as in Equation (4.9):

$$\frac{d\hat{i}_{\text{VSC}}^{\text{loss}}(t^*)}{dt^*} = -\frac{\pi f_{LC}}{Q} \cdot \hat{i}_{\text{VSC}}(t^*) \tag{4.9}$$

Inserting the expressions from Equations (4.8) and (4.9) into Equation (4.6) gives an expression for the total rate of change of $\hat{i}_{\text{VSC}}(t^*)$, as shown in Equation (4.10).

$$\frac{d\hat{i}_{\text{VSC}}(t^*)}{dt^*} = \frac{4f_{LC}v_{\text{DC}}(t^*)}{Z_{LC}} - \frac{\pi f_{LC}}{Q} \cdot \hat{i}_{\text{VSC}}(t^*) \tag{4.10}$$

The current flowing through the DC link capacitor is given by $i_{\text{DC}}(t^*) = \left|i_{\text{VSC}}(t^*)\right|$, since the current direction through C_{DC} is the same irrespective of the VSC switching state, as illustrated in Figure 3.5. This current can also be expressed using the positive i_{VSC} envelope as follows:

$$i_{\text{DC}}(t^*) = \hat{i}_{\text{VSC}}(t^*) \cdot \left|\sin\left(2\pi f_{LC} t^*\right)\right|$$

As the average value of this DC current is $\frac{2}{\pi} \cdot \hat{i}_{\text{VSC}}(t^*)$, the rate of change of the DC link voltage can be expressed in terms of the i_{VSC} envelope as shown in Equation (4.11):

$$C_{\text{DC}}\frac{dv_{\text{DC}}(t^*)}{dt^*} = -\frac{2}{\pi}\hat{i}_{\text{VSC}}(t^*) \tag{4.11}$$

Summing up, the v_{DC} and i_{VSC} dynamics can be described using the equation system in Equation (4.12). This validates the simple mathematical model derived in [72].

$$\begin{bmatrix} \frac{dv_{\text{DC}}(t^*)}{dt^*} \\ \frac{d\hat{i}_{\text{VSC}}(t^*)}{dt^*} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{2}{\pi C_{\text{DC}}} \\ \frac{4f_{LC}}{Z_{LC}} & -\frac{\pi f_{LC}}{Q} \end{bmatrix} \begin{bmatrix} v_{\text{DC}}(t^*) \\ \hat{i}_{\text{VSC}}(t^*) \end{bmatrix} \tag{4.12}$$

The system has the initial conditions given by Equation (4.13):

$$\begin{bmatrix} v_{\text{DC}}(t^*=0) \\ \hat{i}_{\text{VSC}}(t^*=0) \end{bmatrix} = \begin{bmatrix} V_{\text{DC}} \\ 0 \end{bmatrix} \tag{4.13}$$

Equations (4.12) and (4.13) can be used to decide the values of V_{DC} and C_{DC} when f_{LC}, Z_{LC} and Q are known. The values must then be selected to ensure that the initial energy in C_{DC} is sufficient for exciting $\hat{i}_{\text{VSC}}$ to a certain level. This level must necessarily be equal to or greater than $I_{i,\text{max}}$, and is typically set to $KI_{i,\text{max}}$, where the coefficient K is a safety margin [59, 81]. This makes the VSC capable of exciting a current amplitude higher than the maximum possible $\hat{I}_{\text{line}}$, hence making it able to cope with unexpected situations, such as unexpected delay in the detection circuitry, or the VI failing to interrupt at its first current zero-crossing. The values of V_{DC} and C_{DC} must thus be chosen to ensure that the maximum achievable oscillating current, $\hat{i}_{\text{VSC,max}}$, satisfies Equation (4.14):

$$\hat{i}_{\text{VSC,max}} \geq KI_{i,\text{max}} \tag{4.14}$$

Another aspect to take into account when choosing the values of V_{DC} and C_{DC}, is the resulting voltage ratings required for the VSC switches. As discussed in Subsection 4.3.2.2, a lower V_{DC} value means lower voltage ratings needed. This is in accordance with the fourth design goal defined in Section 4.1. At the same time, decreasing V_{DC} may require increasing C_{DC} in order to satisfy Equation (4.14), hence compromising the third design goal. The design of V_{DC} and C_{DC} thus involves a trade-off between minimization of semiconductor switch ratings and minimization of passive elements.

4.3.2.4 The Charging Circuit

The charging circuit of the DC link consists of a DC voltage supply, a charging resistor and a switch. Its task is to ensure that C_{DC} is precharged to V_{DC} prior to an interruption operation of the VARC-CB. The DC supply must therefore provide a voltage level of V_{DC}. The time required for the capacitor to be fully charged is approximately five time constants, i.e. $5\tau_{\text{CH}} = 5R_{\text{CH}}C_{\text{DC}}$. The value of R_{CH} is thus decisive for the rate at which C_{DC} charges. A low R_{CH} results in fast charging, which ensures that the VARC-CB rapidly can be ready to operate again after a current interruption process is completed. At the same time, the current drawn from the voltage supply is only limited by the equivalent series resistance (ESR) of the capacitor, the internal resistance of the supply, and R_{CH}. The choice of R_{CH} must thus also take the maximum inrush current the DC supply can support into account.

4.3.3 The Metal-Oxide Varistor

The main parameter to design for the MOV is its clamping voltage V_{clamp}. Due to the presence of stray inductances and resistances, the maximum voltage across the VARC-CB will exceed the clamping voltage of the MOV. Nevertheless, the value of V_{clamp} will be decisive for the order of magnitude of the maximum breaker voltage. Consequently, by selecting a larger V_{clamp}, the VI must provide a higher voltage withstand capability, which results in a longer t_{open}. A larger V_{clamp} also means an increase in the maximum voltage step which can occur across the VARC-CB if the arc reignites shortly after the VI current zero. This results in a higher possible amplitude of the reignited current. These two aspects thus suggest that a low V_{clamp} value is advantageous. At the same time, an increased V_{clamp} gives a greater di_{line}/dt during t_5–t_6. This reduces the energy dissipation time interval, hence the line current is more rapidly brought to zero, which is desirable.

Typically, the clamping voltage of the MOV is selected to be 1.3–1.6 times the nominal system voltage [71, 82]. As 1.5 times V_{nom} is repeatedly employed in literature [61, 69, 81, 83], the following design equation is suggested:

$$V_{\text{clamp}} = 1.5 V_{\text{nom}} \tag{4.15}$$

As mentioned in Subsection 3.2.7, there will be leakage current flowing through the MOV prior to the rise towards the clamping voltage is initiated at t_4. The magnitude of this current should be as low as possible, to limit its impact on the breaker operation. To ensure this, it is important that the magnitude of v_{MOV} is kept below V_{clamp} before t_4 [72].

The highest magnitude of $v_{\text{MOV}}(t) = v_{C_p}(t) + v_{\text{VSC}}(t)$ prior to t_4 arises at the very last negative peak of v_{C_p}. This occurs slightly before t_4, as seen in Figure 3.3. At this point, the VSC performs its very last switching operation, changing the polarity of v_{VSC} from positive to negative. The highest magnitude of v_{MOV} prior to t_4 is therefore the sum of $\left|v_{C_p}\right|$ and v_{DC} at the very last negative v_{C_p} peak.

To ensure that this sum is kept below V_{clamp} for all interruption cases, the worst case scenario (WCS) should be taken into account. This means that the highest possible magnitudes for the two addends $\left|v_{C_p}\right|$ and v_{DC} must be considered.

As discussed in Subsection 4.3.2.3, the value of v_{DC} declines from its initial value of V_{DC} during the VSC operation time. For simplicity, however, the WCS v_{DC} value at the very last negative v_{C_p} peak is set to V_{DC}.

For a certain course of the line current, the WCS value of $\left|v_{C_p}\right|$ occurs if a situation like the one illustrated in Figure 4.2 arises. The figure shows i_{VSC}, v_{C_p}, and i_{line} during the last three switching operations of the VSC, as well as immediately after the VI current zero at t_4. Due to the fast switching of the VSC compared to the relatively slow rising rate of the line current, i_{line} is approximated as constant in the time interval displayed (this does not agree with what is indicated in Figure 3.3, however the size of t_3–t_4 in Figure 3.3 is highly exaggerated). The peak value $\hat{I}_{\text{line}}$ is reached slightly after t_4, but due to the short time scale, $i_{\text{line}} \approx \hat{I}_{\text{line}}$ is a reasonable approximation. In the case shown, the positive peak $k-1$ of the VSC current is very close to, but does not reach the level of the line current. This results in two additional switching operations being needed before $i_{\text{VSC}} = i_{\text{line}}$ is achieved, which allows the v_{C_p} amplitude to further increase.

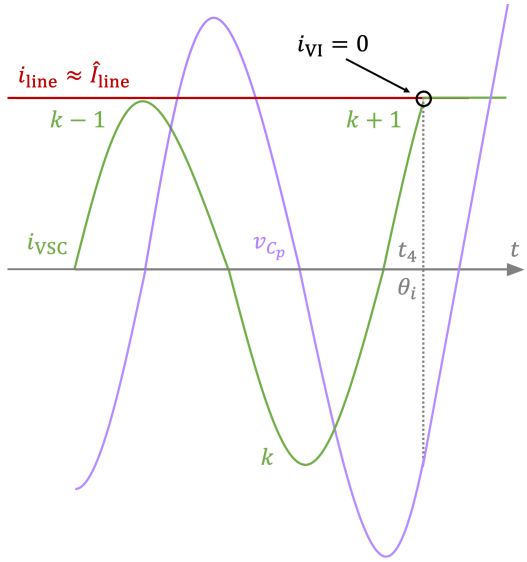


Figure 4.2: Worst case scenario for the maximum $|v_{C_p}|$ value prior to t_4.

Letting I_k and I_{k+1} be the amplitudes of the last two i_{VSC} half-cycles, the magnitude of the last negative peak of the C_p voltage, $|v_{C_p}|_{\text{max}}$, can be approximated by Equation (4.16):

$$|v_{C_p}|_{\text{max}} = Z_{LC} \cdot \frac{I_k + I_{k+1}}{2} \tag{4.16}$$

To obtain the WCS value of $|v_{C_p}|_{\text{max}}$, the highest possible values of I_k and I_{k+1} must be considered. These arise when the VARC-CB interrupts $I_{i,\text{max}}$. In this case, $I_{k-1} \approx I_{i,\text{max}}$, and I_k and I_{k+1} can be approximated by $I_{i,\text{max}} + \Delta I$ and $I_{i,\text{max}} + 2\Delta I$, respectively. As a WCS, v_{DC} can be considered constantly equal to V_{DC}, which results in the following WCS values for I_k and I_{k+1}:

$$I_{k,\text{WCS}} = I_{i,\text{max}} + (\Delta I)_{\text{WCS}} = I_{i,\text{max}} + \frac{2V_{\text{DC}}}{Z_{LC}} \tag{4.17}$$

$$I_{k+1,\text{WCS}} = I_{i,\text{max}} + \frac{4V_{\text{DC}}}{Z_{LC}} \tag{4.18}$$

Inserting $I_{k,\text{WCS}}$ from Equation (4.17) and $I_{k+1,\text{WCS}}$ from Equation (4.18) into Equation (4.16) results in the WCS value of $|v_{C_p}|_{\text{max}}$. Adding this to the WCS value of v_{DC}, which simply is V_{DC}, gives the highest possible MOV voltage magnitude prior to t_4:

$$|v_{C_p}|_{\text{max,WCS}} + v_{\text{DC,WCS}} = (Z_{LC} I_{i,\text{max}} + 3V_{\text{DC}}) + V_{\text{DC}} = Z_{LC} I_{i,\text{max}} + 4V_{\text{DC}} \tag{4.19}$$

The value of the sum in Equation (4.19) should be kept below V_{clamp}. The following design criterion for Z_{LC} thus results:

$$Z_{LC} \leq \frac{V_{\text{clamp}} - 4V_{\text{DC}}}{I_{i,\text{max}}} \tag{4.20}$$

At the same time as Z_{LC} must satisfy Equation (4.20), it is desirable to make Z_{LC} as high as possible, to limit the current pulse amplitude at a potential reignition. If the VI arc reignites after its current zero-crossing, a voltage step will be applied across the current injection branch. The resulting current pulse will essentially only be limited by Z_{LC} [72]. A Z_{LC} value which is high, but still satisfies Equation (4.20), is therefore desirable.

It should be noted that the design criterion given in Equation (4.20) incorporates some safety margin, due to the simplification $v_{\text{DC}} = V_{\text{DC}}$ used when deriving the equation. In reality, v_{DC} will be lower than V_{DC} in the entire time interval displayed in Figure 4.2, causing the actual values of $I_{k,\text{WCS}}$ and $I_{k+1,\text{WCS}}$ to be lower than those presented in Equation (4.17) and Equation (4.18), respectively. This results in the WCS value of the MOV voltage given in Equation (4.19) being an overestimate, giving some safety margin in the upper limit value of Z_{LC} in Equation (4.20). To obtain a more accurate upper limit, the v_{DC} dynamics presented in Equation (4.12) and Equation (4.13) should be taken into account. This will, however, lead to a more complex design criterion. Equation 4.20, on the other hand, is a simple and easy-to-use constraint, thus complying with the design goal of low complexity. In addition, some safety margin is convenient, as the MOV voltage in reality will be higher than $v_{C_p} + |v_{\text{DC}}|$, due to the presence of stray inductances. Using $v_{\text{DC}} = V_{\text{DC}}$ in the derivations can thus be considered a reasonable simplification.

4.3.4 The Vacuum Interrupter

Complying with the design goal of high reliability depends on each subcomponent of the VARC-CB module functioning properly, which for the VI involves that successful arc extinction must be ensured. The design of the VARC-CB parameters should therefore facilitate the conditions required for a successful arc quenching being fulfilled. This is in particular related to the opening time, the di/dt capability, and the dv/dt capability of the VI, which all impose important limitations on the parameter design. This will be investigated in further detail in Subsections 4.3.4.1–4.3.4.3.

4.3.4.1 The Opening Time

As discussed in Subsection 3.2.6, the time interval between t_2 and t_4, i.e. the sum $t_{\text{VSC,delay}}$ + t_{VSC}, must be equal to or greater than the VI opening time, t_{open}, to ensure that the contact gap of the VI has reached a sufficient length to withstand the TIV when i_{VI} crosses zero. The design criterion presented in Equation (4.21) can thus be formulated:

$$t_4 - t_2 = t_{\text{VSC,delay}} + t_{\text{VSC}} \geq t_{\text{open}} \tag{4.21}$$

In an ideal case, t_4 is both the time at which the VSC current reaches the value of the line current, and also the instant where the VI achieves the required contact gap, i.e. $t_4 - t_2 = t_{\text{open}}$. In this case, no additional time, beyond the time needed for the VI opening, is required for the operation of the VSC. As a result, no delay is introduced by the VSC

operation, hence the arcing time of the VI is limited to the minimum necessary. This is therefore in accordance with the design goal of minimizing the total operation time.

To achieve $t_4 - t_2 = t_{\text{open}}$, it must be ensured that $t_{\text{VSC}} \leq t_{\text{open}}$. Furthermore, the triggering instant of the VSC must be adjusted to the course of the line current and the prospective oscillating current, so that $i_{\text{VSC}} = i_{\text{line}}$ occurs exactly when the VI reaches the desired contact gap. This does, however, require the application of sophisticated measurement and calculation methods, which can adapt the $t_{\text{VSC,delay}}$ value to each individual current interruption case. Such methods will make the breaker implementation more complex, hence compromising the last design goal defined in Section 4.1. Consequently, it might be desirable to use a constant $t_{\text{VSC,delay}}$ value, resulting in the VSC triggering always occurring with a fixed delay with respect to the initial VI contact separation. The constant value of $t_{\text{VSC,delay}}$ must then be selected so that $t_{\text{VSC,delay}} + t_{\text{VSC}} \geq t_{\text{open}}$ always is ensured, regardless of the time needed for the VSC operation. Resultantly, the $t_{\text{VSC,delay}}$ value should be selected based on the minimum possible value of t_{VSC}:

$$t_{\text{VSC,delay}} \geq t_{\text{open}} - t_{\text{VSC,min}} \tag{4.22}$$

The operation time of the VSC is at its shortest when the line current to be interrupted is at its lowest possible level, i.e. when the VARC-CB interrupts $I_{i,\text{min}}$. A rough estimation of the t_{VSC} value in this case can be found by assuming v_{DC} to be constant at V_{DC}, hence an amplitude increase of V_{DC}/Z_{LC} at the very first switching operation, and of $2V_{\text{DC}}/Z_{LC}$ at the subsequent ones. This will result in an underestimate of $t_{\text{VSC,min}}$, hence some safety margin. $t_{\text{VSC,min}}$ can then be approximated by the following derivation, where N_i is the number of switching operations performed before current interruption occurs:

$$(2N_i - 1) \cdot \frac{V_{\text{DC}}}{Z_{LC}} \geq I_{i,\text{min}} \quad \Rightarrow \quad (4f_{LC}t_{\text{VSC,min}} - 1) \cdot \frac{V_{\text{DC}}}{Z_{LC}} \geq I_{i,\text{min}}$$

The following lower limit for $t_{\text{VSC,min}}$ results:

$$t_{\text{VSC,min}} \geq \frac{I_{i,\text{min}} Z_{LC} + V_{\text{DC}}}{4 f_{LC} V_{\text{DC}}} \tag{4.23}$$

Inserting this into Equation (4.22) gives a design criterion for the VSC triggering instant with respect to the initial contact separation in the VI:

$$t_{\text{VSC,delay}} \geq t_{\text{open}} - \frac{I_{i,\text{min}} Z_{LC} + V_{\text{DC}}}{4 f_{LC} V_{\text{DC}}} \tag{4.24}$$

4.3.4.2 The di/dt Capability

To ensure successful arc extinction in the VI, the slope of i_{VI} at its zero-crossing cannot be higher than what the VI can handle. It is therefore essential that the limitations imposed by the di/dt capability of the VI are accounted for in the parameter design process.

To obtain design criteria taking the di/dt capability of the VI into account, an expression for the VI current slope at the zero-crossing at $t = t_4$ must be derived and investigated. Utilizing the current directions in Figure 3.4, the VI current is given by $i_{\text{VI}} = i_{\text{line}} - i_{\text{VSC}}$. Assuming a constant slope of the line current, as in Subsection 4.3.1, the VI current slope

at t_4 can be expressed as given in Equation (4.25). In this equation, L_1 is the accumulated line inductance between the breaker module and the fault location.

$$\frac{di_{\text{VI}}(t_4)}{dt} = \frac{di_{\text{line}}(t_4)}{dt} - \frac{di_{\text{VSC}}(t_4)}{dt} = \frac{V_{\text{nom}}}{L_{\text{lim}} + L_1} - \frac{di_{\text{VSC}}(t_4)}{dt} \tag{4.25}$$

Using the notation introduced in Figure 4.2, the positive i_{VSC} pulse resulting from the very last VSC switching operation can be denoted as in Equation (4.26), where $0° \leq \theta \leq 180°$.

$$i_{k+1}(\theta) = I_{k+1} \sin(\theta) \tag{4.26}$$

As indicated in Figure 4.2, the current interruption occurs at $t = t_4$, corresponding to $\theta = \theta_i$. The slope of the VSC current at this point is

$$\frac{di_{\text{VSC}}(t_4)}{dt} = \frac{di_{k+1}(\theta_i)}{dt} = 2\pi f_{LC} I_{k+1} \cos(\theta_i)$$

Inserting this into Equation (4.25) results in Equation (4.27):

$$\frac{di_{\text{VI}}(t_4)}{dt} = \frac{V_{\text{nom}}}{L_{\text{lim}} + L_1} - 2\pi f_{LC} I_{k+1} \cos(\theta_i) \tag{4.27}$$

To obtain a successful arc quenching in the VI, it must be ensured that the sum on the right-hand side of Equation (4.27) is lower than the di/dt capability of the VI for all possible interruption currents of the VARC-CB. Consequently, the inequality in Equation (4.28) must be satisfied, where $(di/dt)_{\text{cap}}$ denotes the VI's di/dt capability:

$$-\left(\frac{di}{dt}\right)_{\text{cap}} \leq \frac{V_{\text{nom}}}{L_{\text{lim}} + L_1} - 2\pi f_{LC} I_{k+1} \cos(\theta_i) \leq \left(\frac{di}{dt}\right)_{\text{cap}} \tag{4.28}$$

To obtain a criterion ensuring that the upper limit in Equation (4.28) is not violated, the minimum possible magnitude of the product $2\pi f_{LC} I_{k+1} \cos(\theta_i)$ should be considered. As the current interruption necessarily must occur during the first half of the positive VSC current pulse, i.e. $0 < \theta_i \leq 90°$, the minimum possible value of the product is $2\pi f_{LC} I_{k+1} \cos(90°) = 0$. A design limit for L_{lim} thus results, with $L_1 = 0$ giving the tightest limit:

$$L_{\text{lim}} \geq \frac{V_{\text{nom}}}{\left(\frac{di}{dt}\right)_{\text{cap}}} \tag{4.29}$$

As an expression for a lower L_{lim} limit already exists in Equation (4.1), Equation (4.29) and Equation (4.1) can be combined into one design criterion for L_{lim}:

$$L_{\text{lim}} \geq \text{argmax} \left[\frac{V_{\text{nom}} \cdot t_4}{I_{i,\text{max}} - I_{\text{nom}}}, \frac{V_{\text{nom}}}{\left(\frac{di}{dt}\right)_{\text{cap}}} \right] \tag{4.30}$$

To obtain a criterion ensuring that the lower limit in Equation (4.28) is not violated, the maximum possible magnitude of the product $2\pi f_{LC} I_{k+1} \cos(\theta_i)$ must be taken into account. More specifically, the maximum possible magnitude of $I_{k+1} \cdot \cos(\theta_i)$ must be considered. For a certain interruption current, $\hat{I}_{\text{line}}$, the highest possible value of I_{k+1} occurs if a situation like the one in Figure 4.2 arises, and its value can be calculated by replacing $I_{i,\text{max}}$ by $\hat{I}_{\text{line}}$ in Equation (4.18):

$$(I_{k+1})_{\text{max}} = \hat{I}_{\text{line}} + \frac{4V_{\text{DC}}}{Z_{LC}} \tag{4.31}$$

The situation in Figure 4.2 is also the scenario giving the lowest possible value of θ_i for a certain value of $\hat{I}_{\text{line}}$. By inserting the I_{k+1} expression from Equation (4.31) into Equation (4.26), this lowest θ_i can be found by

$$i_{k+1}(\theta_{i,\text{min}}) = \left(\hat{I}_{\text{line}} + \frac{4V_{\text{DC}}}{Z_{LC}}\right) \cdot \sin(\theta_{i,\text{min}}) = \hat{I}_{\text{line}}$$

$$\Rightarrow \quad \theta_{i,\text{min}} = \arcsin\left(\frac{1}{1 + \frac{4V_{\text{DC}}}{Z_{LC}\hat{I}_{\text{line}}}}\right) \tag{4.32}$$

For a certain value of $\hat{I}_{\text{line}}$, the maximum possible magnitude of $I_{k+1} \cdot \cos(\theta_i)$ is thus found by using the maximum I_{k+1} expression from Equation (4.31) and the minimum θ_i expression from Equation (4.32). The product then becomes

$$(I_{k+1} \cdot \cos(\theta_i))_{\text{max}} = \left(\hat{I}_{\text{line}} + \frac{4V_{\text{DC}}}{Z_{LC}}\right) \sqrt{1 - \left(\frac{1}{1 + \frac{4V_{\text{DC}}}{Z_{LC}\hat{I}_{\text{line}}}}\right)^2} \tag{4.33}$$

where the trigonometric identity $\cos(\arcsin(x)) = \sqrt{1 - x^2}$ has been used.

The expression on the right-hand side of Equation (4.33) is a strictly increasing function of $\hat{I}_{\text{line}}$. Consequently, the WCS (highest) value of $(I_{k+1} \cdot \cos(\theta_i))_{\text{max}}$ occurs when $\hat{I}_{\text{line}} = I_{i,\text{max}}$. Inserting $\hat{I}_{\text{line}} = I_{i,\text{max}}$ into Equation (4.33), and inserting this into the lower limit expression in Equation (4.28) results in the criterion in Equation (4.34). L_1 has been set equal to L_{line}, as this results in the strictest criterion.

$$2\pi f_{LC}\left(I_{i,\text{max}} + \frac{4V_{\text{DC}}}{Z_{LC}}\right) \sqrt{1 - \left(\frac{1}{1 + \frac{4V_{\text{DC}}}{Z_{LC} I_{i,\text{max}}}}\right)^2} \leq \frac{V_{\text{nom}}}{L_{\text{lim}} + L_{\text{line}}} + \left(\frac{di}{dt}\right)_{\text{cap}} \tag{4.34}$$

From Equation (4.34) it is evident that a higher switching/resonance frequency results in an increase in the maximum possible slope of the VI current at its zero-crossing. Consequently, the VI imposes an upper limit on the switching/resonance frequency. Furthermore, for a certain switching/resonance frequency, the di/dt capability of the VI restricts the value of the quotient between V_{DC} and Z_{LC}.

4.3.4.3 The dv/dt Capability

To avoid reignition of the VI arc after t_4, the magnitude of the TIV must never exceed the recovered voltage withstand capability of the VI. Said with other words, the TIV must stay below the VI's capability curve (ref. the ACCB theory presented in Subsection 2.3.1.2). The dv/dt capability of the VI must therefore be paid attention to when designing the parameters of the VARC-CB module.

In order to obtain design criteria taking the dv/dt capability of the VI into account, an investigation of the TIV waveform, i.e. the course of v_{VI} after $t = t_4$, is required. A simplified analysis was presented in Subsection 3.2.7, where v_{L_p} was neglected due to the relatively low di/dt of the line current, making $v_{\text{VI}}(t > t_4)$ equal to $v_{\text{MOV}} = v_{C_p} - v_{\text{DC}}$. This analysis is, however, too idealized. It is correct that v_{VI} will follow the course of the sum $v_{C_p} - v_{\text{DC}}$, however, a transient oscillatory response will be superimposed onto this sum. This is similar to how the voltage across an ACCB in an AC system after current zero-crossing oscillates towards the power frequency recovery voltage via the TRV, as was discussed in Subsection 2.3.1.2 and shown in Figure 2.3.

The nature of the transient response observed in v_{VI} is determined by the network configuration surrounding the VI, just as is the case for the TRV of an ACCB. Even when using the simplified system representation given in Figure 4.1, determining the transient response in v_{VI} is a difficult task. Due to the presence of many energy storage elements, the response will be a superposition of multiple different frequencies, resulting in complex TIV characteristics. For the determination of TRVs for ACCBs in AC systems, computerized numerical calculations with more detailed system representations are often used in order to obtain a reasonable accuracy [37, 39]. Such an in-depth analysis of the TIV is beyond the scope of this thesis. At the same time, it is desirable to present a complete set of design strategies for the VARC-CB module. A basic analysis of the TIV waveform will therefore be presented, in order to include restrictions imposed by the VI's dv/dt capability in the design process. The simplified MVDC system displayed in Figure 4.1 will be used as a basis, giving an analysis which is idealized, yet more accurate than the one included in Subsection 3.2.7.

In the analysis to be presented, the time interval t_4–t_5 will be considered, and it will be divided into two subintervals. In the first subinterval, v_{VI} decreases from V_{arc} to ITIV. In this subinterval, it is therefore the rising rate of the ITIV (RRITIV), which is measured the same way as RRRV in Figure 4.3, which is of interest. In the second subinterval, v_{VI} rises from ITIV until reaching its maximum value at t_5. In this subinterval, it is the rising rate of the positive part of the TIV, from here denoted by the positive RRTIV, which is of importance. In both subintervals, it must be ensured that the magnitude of v_{VI} is kept below the capability curve of the VI. This means that both the RRITIV and the positive RRTIV must be below the VI's dv/dt capability.

The First Subinterval of t_4–t_5

To obtain design criteria accounting for the VI's dv/dt capability in the first subinterval, expressions for the ITIV value and the RRITIV must be derived and examined. In particular, the highest possible values of ITIV and RRITIV are of interest, representing the WCS in terms of voltage stress applied to the VI during the first subinterval of t_4–t_5.

The presence of capacitance and resistance, both in direct parallel to the VI and phase to ground, reduces the slope of the transient oscillations in the TIV, just as is the case for the TRV of an ACCB employed in an AC system [39]. The WCS (highest) RRITIV value thus occurs for a terminal SC fault, as the capacitance and resistance present to limit the ITIV slope is at minimum.

During a terminal fault, C_{x2}, C_{line}, and R_{line} are all short-circuited, hence they will not contribute to a reduction in the RRITIV. Instead, it is mainly the loop formed by C_{x1}, the VARC-CB module, and the short-circuit which determines the course of the transient response superimposed onto the sum $v_{C_p} - v_{\text{DC}}$. In this case, the series-connection of C_p and the VSC can be considered a voltage "source", which applies a voltage of $v_{C_p} - v_{\text{DC}}$ across the series-connection $L_p + R_p + (C_{x1} || (R_s + L_s + C_s))$. The MOV is not considered, because the value of L_p typically is so high that the MOV is not "seen", as far as the transient response of v_{VI} is concerned. The current flowing through the stray branch of the VI is very low, hence R_s and L_s can be neglected, and C_s can be considered connected in direct parallel with C_{x1}. As a result, the series-connection seen from the terminals of the "source" can be simplified to $L_p + R_p + (C_{x1} || C_s)$. This series-connection gives rise to the frequency f_s, which will be the frequency dominating the oscillatory transient response of the TIV during a terminal fault in the simplified MVDC system:

$$f_s = \frac{1}{2\pi} \sqrt{\frac{1}{L_p \cdot (C_{x1} + C_s)} - \left(\frac{R_p}{2L_p} \right)^2} \tag{4.35}$$

With f_s as the dominating frequency of the oscillations in v_{VI} around $v_{C_p} - v_{\text{DC}}$, the first negative peak of v_{VI}, the ITIV, occurs at $t_4 + \frac{1}{2f_s}$. Due to the high value of f_s, the occurrence of this negative peak happens very shortly after t_4. Consequently, the peak value, i.e. the ITIV value, can be approximated by Equation (4.36), where the exponential factor is included to account for the damping caused by R_p:

$$\text{ITIV} = 2 \cdot (v_{C_p}(t_4) - v_{\text{DC}}(t_4)) \cdot e^{-\frac{R_p}{4L_p f_s}} \tag{4.36}$$

The ITIV magnitude in Equation (4.36) is an overestimate, as the increase in v_{C_p} between $t = t_4$ and $t = t_4 + \frac{1}{2f_s}$ will reduce the magnitude of the negative v_{VI} peak. However, this time interval is, as already pointed out, short due to the high value of f_s, making Equation (4.36) a reasonable ITIV estimate.

Figure 4.3 illustrates the course of v_{VI} immediately after t_4 for the situation just described, i.e. during a terminal fault. The figure illustrates how the VI voltage (the blue curve) oscillates around $v_{C_p}(t) - v_{\text{DC}}(t)$ (black line) with a frequency of f_s, and how the ITIV is reached at $t = t_4 + \frac{1}{2f_s}$. The red line is included to indicate the RRITIV.

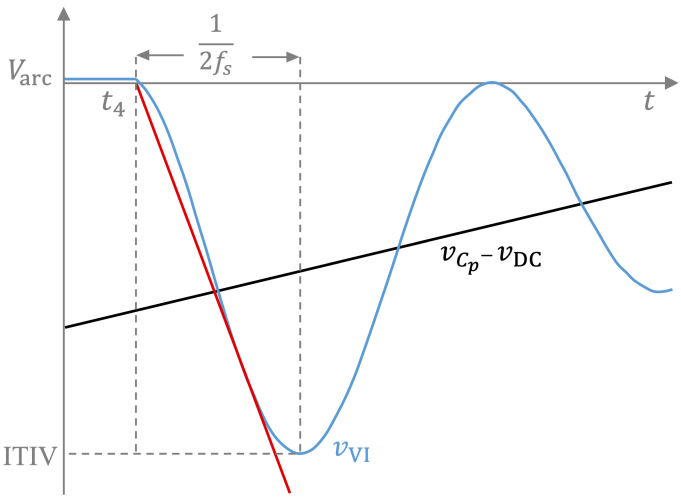


Figure 4.3: The course of the VI voltage (blue curve) immediately after t_4 during a terminal fault. The red line indicates the RRITIV.

By using trigonometry in Figure 4.3, the RRITIV can be found to be:

$$\text{RRITIV} = \frac{\frac{2+\sqrt{2}}{2} \cdot \frac{\text{ITIV}}{2}}{\frac{3}{8f_s}} = \frac{4+2\sqrt{2}}{3} \cdot f_s \cdot \text{ITIV}$$

Letting $(dv/dt)_{\text{cap}}$ denote the dv/dt capability of the VI, the following design criterion for the first subinterval of t_4–t_5 can thus be derived:

$$\frac{4+2\sqrt{2}}{3} \cdot f_s \cdot |\text{ITIV}| \leq \left(\frac{dv}{dt}\right)_{\text{cap}} \tag{4.37}$$

To make Equation (4.37) a useful criterion in the design process, a WCS magnitude for the ITIV should be estimated. This means that the highest possible magnitudes of $v_{C_p}(t_4)$ and $v_{\text{DC}}(t_4)$ are needed, ref. Equation (4.36).

The magnitude of $v_{C_p}(t_4)$ is given by $\left|v_{C_p}\right|_{\text{max}} \cdot \cos(\theta_i)$, where $\left|v_{C_p}\right|_{\text{max}}$ is the magnitude of the very last negative peak of v_{C_p}, as explained in Subsection 4.3.3. Consequently, the highest possible magnitude of $v_{C_p}(t_4)$ occurs for the lowest possible value of θ_i. As previously explained, this happens if the situation in Figure 4.2 arises. The value of θ_i can thus be calculated by Equation (4.32). Based on the v_{C_p} considerations made in Subsection 4.3.3, the value of $\hat{I}_{\text{line}}$ should be set equal to $I_{i,\text{max}}$ to obtain the WCS. Consequently, the results presented in Equations (4.16)–(4.19) can be used, giving the following estimation of the WCS magnitude of $v_{C_p}(t_4)$:

$$\left(v_{C_p}(t_4)\right)_{\text{WCS}} = -Z_{LC}\left(I_{i,\text{max}} + \frac{3V_{\text{DC}}}{Z_{LC}}\right)\sqrt{1-\left(\frac{1}{1+\frac{4V_{\text{DC}}}{Z_{LC}I_{i,\text{max}}}}\right)^2} \tag{4.38}$$

Just as in the analysis presented in Subsection 4.3.3, the WCS magnitude of $v_{\text{DC}}(t_4)$ is set to V_{DC}. By inserting $(v_{\text{DC}}(t_4))_{\text{WCS}} = V_{\text{DC}}$ and Equation (4.38) into Equation (4.36), the WCS ITIV value estimate in Equation (4.39) results:

$$\text{ITIV}_{\text{WCS}} = 2 \cdot \left(-Z_{LC} \left(I_{i,\text{max}} + \frac{3V_{\text{DC}}}{Z_{LC}} \right) \sqrt{1 - \left(\frac{1}{1 + \frac{4V_{\text{DC}}}{Z_{LC} I_{i,\text{max}}}} \right)^2} - V_{\text{DC}} \right) \cdot e^{-\frac{R_p}{4L_p f_s}} \tag{4.39}$$

The design criterion in Equation (4.37) should then be reformulated to the one in Equation (4.40), making Equation (4.40) together with (4.35) and (4.39) the final design criteria from the analysis of the first subinterval of t_4–t_5. The expression on the left-hand side of (4.40) represents the WCS magnitude of the RRITIV.

$$\frac{4 + 2\sqrt{2}}{3} \cdot f_s \cdot |\text{ITIV}_{\text{WCS}}| \leq \left(\frac{dv}{dt} \right)_{\text{cap}} \tag{4.40}$$

The Second Subinterval of t_4–t_5

To obtain a design criterion accounting for the VI's dv/dt capability in the second subinterval of t_4–t_5, the rate of rise of the black line in Figure 4.3, $v_{C_p} - v_{\text{DC}}$, is of interest. During t_4–t_5 v_{DC} is approximately constant, while v_{C_p} increases, as the line current is now flowing through the current injection branch. Due to the short time between t_4 and t_5, the value of i_{line} can be approximated as constant, equal to its peak value $\hat{I}_{\text{line}}$. The slope of the black line in Figure 4.3 can then approximately be given by $\hat{I}_{\text{line}}/C_p$, hence its largest possible value is $I_{i,\text{max}}/C_p$.

To ensure that v_{VI} is kept below the positive capability curve of the VI, the maximum possible slope of $v_{C_p} - v_{\text{DC}}$ should be smaller than the VI's dv/dt capability. This will result in the positive capability curve being parallel to or steeper than the black line in Figure 4.3. Since the capability curve starts from zero at t_4, whereas the black line has a finite negative value, in addition to the fact that the oscillations in v_{VI} are damped, v_{VI} is thus prevented from exceeding the capability curve. The resulting design equation is a design criterion for C_p, which is presented in Equation (4.41):

$$\begin{aligned} \frac{I_{i,\text{max}}}{C_p} &\leq \left(\frac{dv}{dt} \right)_{\text{cap}} \\ \Rightarrow \quad C_p &\geq \frac{I_{i,\text{max}}}{\left(\frac{dv}{dt} \right)_{\text{cap}}} \end{aligned} \tag{4.41}$$

4.3.5 Summary of the Design Strategies for the MVDC VARC-CB

The equations and expressions below sum up the derivations and discussions presented in this chapter, providing a complete set of design strategies for the VARC-CB module.

$$\hat{I}_{\text{line}} \in [I_{i,\text{min}}, I_{i,\text{max}}]$$

$$L_{\text{lim}} \geq \text{argmax} \left[\frac{V_{\text{nom}} \cdot t_4}{I_{i,\text{max}} - I_{\text{nom}}}, \frac{V_{\text{nom}}}{\left(\frac{di}{dt}\right)_{\text{cap}}} \right] \tag{4.30 revisited}$$

$$f_{LC} = \frac{1}{2\pi\sqrt{L_p C_p}} \tag{3.1 revisited}$$

$$f_{\text{sw}} = f_{\text{LC}} \tag{4.3 revisited}$$

$$f_{LC} \leq f_{S,\text{max}} \tag{4.4 revisited}$$

$$Z_{LC} = \sqrt{\frac{L_p}{C_p}} \tag{3.3 revisited}$$

$$t^* = t - t_3 \tag{4.5 revisited}$$

$$Q = \frac{Z_{LC}}{R_p}$$

$$\begin{bmatrix} \frac{dv_{\text{DC}}(t^*)}{dt^*} \\ \frac{d\hat{i}_{\text{VSC}}(t^*)}{dt^*} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{2}{\pi C_{\text{DC}}} \\ \frac{4f_{LC}}{Z_{LC}} & -\frac{\pi f_{LC}}{Q} \end{bmatrix} \begin{bmatrix} v_{\text{DC}}(t^*) \\ \hat{i}_{\text{VSC}}(t^*) \end{bmatrix} \tag{4.12 revisited}$$

$$\begin{bmatrix} v_{\text{DC}}(t^* = 0) \\ \hat{i}_{\text{VSC}}(t^* = 0) \end{bmatrix} = \begin{bmatrix} V_{\text{DC}} \\ 0 \end{bmatrix} \tag{4.13 revisited}$$

$$\hat{i}_{\text{VSC,max}} \geq K I_{i,\text{max}} \tag{4.14 revisited}$$

$$V_{\text{clamp}} = 1.5 V_{\text{nom}} \tag{4.15 revisited}$$

$$Z_{LC} \leq \frac{V_{\text{clamp}} - 4V_{\text{DC}}}{I_{i,\text{max}}} \tag{4.20 revisited}$$

$$t_{\text{VSC,delay}} \geq t_{\text{open}} - \frac{I_{i,\min} Z_{LC} + V_{\text{DC}}}{4 f_{LC} V_{\text{DC}}} \tag{4.24 revisited}$$

$$2\pi f_{LC} \left(I_{i,\max} + \frac{4V_{\text{DC}}}{Z_{LC}} \right) \sqrt{1 - \left(\frac{1}{1 + \frac{4V_{\text{DC}}}{Z_{LC} I_{i,\max}}} \right)^2} \leq \frac{V_{\text{nom}}}{L_{\text{lim}} + L_{\text{line}}} + \left(\frac{di}{dt} \right)_{\text{cap}} \tag{4.34 revisited}$$

$$f_s = \frac{1}{2\pi} \sqrt{\frac{1}{L_p \cdot (C_{x1} + C_s)} - \left(\frac{R_p}{2L_p} \right)^2} \tag{4.35 revisited}$$

$$\text{ITIV}_{\text{WCS}} = 2 \cdot \left(-Z_{LC} \left(I_{i,\max} + \frac{3V_{\text{DC}}}{Z_{LC}} \right) \sqrt{1 - \left(\frac{1}{1 + \frac{4V_{\text{DC}}}{Z_{LC} I_{i,\max}}} \right)^2} - V_{\text{DC}} \right) \cdot e^{-\frac{R_p}{4L_p f_s}} \tag{4.39 revisited}$$

$$\frac{4 + 2\sqrt{2}}{3} \cdot f_s \cdot |\text{ITIV}_{\text{WCS}}| \leq \left(\frac{dv}{dt} \right)_{\text{cap}} \tag{4.40 revisited}$$

$$C_p \geq \frac{I_{i,\max}}{\left(\frac{dv}{dt} \right)_{\text{cap}}} \tag{4.41 revisited}$$

Chapter 5

Modeling and Parameterization of the MVDC VARC-CB

This chapter presents a parameterized simulation model where the VARC-CB concept is employed in an MVDC power grid. A Simulink® model of the design system given in Figure 4.1 has been developed, and its parameter values have been designed. In particular, the parameter values of the VARC-CB module have been selected and calculated in accordance with the design strategies derived in the previous chapter. This chapter describes and discusses in detail how the components and parameters of the design system are realized by means of Simulink components in the simulation model, and how the control circuitry required for simulating the breaker operation is implemented. It also includes considerations and reasoning related to the choice and calculation of parameter values.

It should be noted that the model parameterization performed did not aim for an optimal design. By using optimization techniques for constrained nonlinear problems, the design equations and constraints in Subsection 4.3.5 can be used to obtain optimal breaker designs with respect to certain objectives. This is, however, out of scope of the thesis work. The parameter design described in this chapter is thus not necessarily an optimal one, however it complies with all the strategies derived, hence providing a feasible and adequate design of the VARC-CB module.

The complete model parameterization is summarized in Table C.1 in Appendix C.

5.1 Software Considerations

The software chosen for modeling and simulating the VARC-CB concept was MATLAB®/ Simulink®. The circuitry implementing the control of the breaker operation was implemented using conventional blocks from the standard Simulink libraries, whereas the subcomponents of the MVDC grid and of the breaker were implemented by means of components from the Simscape Electrical™ toolbox. The components used were chosen from the Electrical Block libraries of Simscape, and not from the Specialized Power Systems

library, as the former use a physical modeling approach, hence more correct physical behavior of and conditions for the components may be obtained. In particular, the Electrical Block libraries contain IGBT and diode models providing more accurate physical representations than the equivalent models found in the Specialized Power Systems library.

5.2 Simulation Model

Figure 5.1 shows the design system in Figure 4.1 realized as a Simulink model.

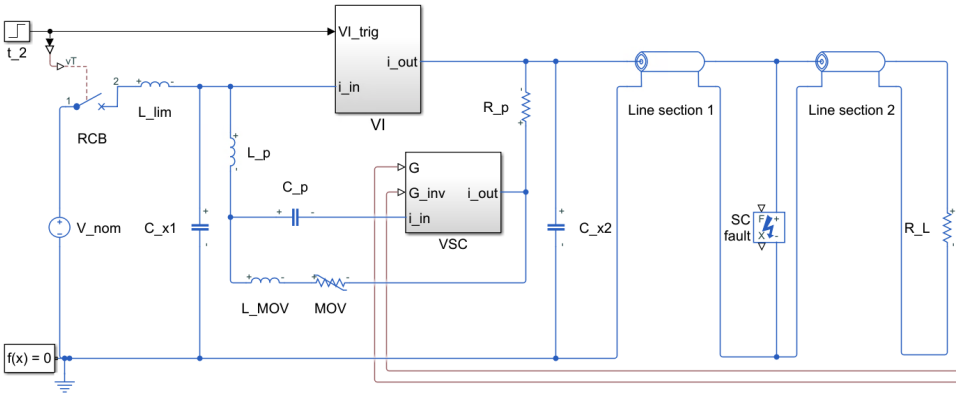


Figure 5.1: Simulation model of the system.

In the following, the modeling and parameterization process for each part and parameter of the model in Figure 5.1 will be described and discussed. Each section concentrates on one subcomponent or -part of the overall model: the power grid, the SC fault, the energy absorption branch of the breaker module, the VI in the breaker module, the RCB, the current injection branch of the breaker module, and the current-limiting inductor.

5.3 Power Grid Modeling and Parameterization

The power grid-related components and parameters include the MVDC source, the nominal current, the current interruption range, the load resistor, the DC line, and the equivalent stray capacitances between the VARC-CB module and ground.

5.3.1 Nominal Voltage, Current and Load

The power source of the MVDC grid under consideration was modelled using the *DC Voltage Source* block, which represents an ideal DC source of constant voltage. The output voltage of this block was set equal to the nominal grid voltage V_{nom}. A nominal voltage of $V_{\text{nom}} = 10$ kV was adopted, which is within the potential range of MVDC grid voltages discussed in Section 2.1. The nominal grid current I_{nom} was selected to be 1 kA. The

nominal load resistance, R_L, was tuned tuned via simulations in order to obtain a steady-state value of the line current equal to I_{nom}. This resulted in $R_L = 10.4\,\Omega$.

5.3.2 Range of Interruption Currents

As discussed when presenting the design system in Section 4.2, the current interruption range is an important input parameter when designing a CB. For the design, modeling, and simulation of the VARC-CB module in Figure 5.1, it was assumed that the module should be capable of interrupting the nominal load current as the minimum current, hence the value of $I_{i,\text{min}}$ was set to $I_{\text{nom}} = 1$ kA. The value of $I_{i,\text{max}}$ was selected based on the fact that in a real-life grid, sensitive power electronics will be present, which must be protected from overcurrents [84]. This is typically ensured if the maximum fault current is limited to 2.0 p.u. [85], hence $I_{i,\text{max}}$ was set equal to 2 kA. The range of interruption currents considered was therefore $[I_{i,\text{min}}, I_{i,\text{max}}] = [1\text{ kA}, 2\text{ kA}]$.

5.3.3 DC Line

For modeling the DC line connecting the MVDC voltage source and the load, the *Transmission Line* block was employed. Based on the study presented in [86], where an MVDC ship distribution system is modeled, the following parameter values were implemented in the model: $r_{\text{line}} = 0.089$ mΩ/m, $l_{\text{line}} = 0.347$ μH/m, and $c_{\text{line}} = 0.307$ nF/m. The insulation conductance per unit length was kept at the default Simscape value, $g_{\text{line}} = 5$ μS/m. A total line length of $d_{\text{line}} = 1$ km was considered.

As can be seen in Figure 5.1, the DC line is divided into two sections using two *Transmission Line* blocks. This is for illustrating the location of a possible pole-to-pole SC fault; the line lengths of the two sections were adjusted according to the desired fault location. When simulating a terminal fault, the length of the second line section was set equal to d_{line}, and the first section was removed from the system, as it is not possible to simulate with a *Transmission line* block having a line length of zero.

The *Transmission Line* block lets the user choose between different transmission line model types. The most accurate one is the *Distributed parameter line*, which is a single frequency model based on the Bergeron's traveling wave method [87]. As this model was not available in the Simulink version used for the simulations, the simpler *Lumped parameter pi-section* model was chosen. However, if implementing a high number of series-connected pi-line segments, the pi-model approaches the distributed model, as the Bergeron method approximately is equivalent to using an infinite number of pi-segments [88]. It was therefore desirable to use a high accumulated *Number of segments* parameter value for the two *Transmission Line* blocks. When simulating, little difference in the results was observed when increasing the total number of segments above 100. The total number of pi-segments implemented was therefore 100, with the segments divided between the two line sections according to their length (i.e. according to the fault location).

5.3.4 Equivalent Stray Capacitance

As mentioned in Section 4.2, the two capacitors C_{x1} and C_{x2} represent the total stray capacitance of all the equipment which, in a realistic DC grid, is connected to each side of the VARC-CB module. This equipment includes bushings, busbars, the RCB, lightning arresters, instrument transformers, etc. Annex B of the IEEE Standard C37.011, *IEEE Guide for the Application of Transient Recovery Voltage for AC High-Voltage Circuit Breakers with Rated Maximum Voltage above 1000 V*, provides a guide for estimating the stray capacitance of various components. Based on the ranges of values given in this guide, it seemed reasonable to implement lumped capacitances in the range of a few nF on each side of the breaker module. 5 nF was selected as the value for both C_{x1} and C_{x2}.

5.3.5 Overview of Power Grid Parameters

Table 5.1 summarizes the preceding section, by presenting an overview of the values of the grid-related parameters implemented in the simulation model. In addition to these parameter values comes the range of interruption currents: $[I_{i,\text{min}}, I_{i,\text{max}}]$ = [1 kA, 2 kA].

Table 5.1: Power grid parameter values for the system in Figure 5.1

V_{nom} [kV]	I_{nom} [kA]	R_L [Ω]	r_{line} [mΩ/m]	l_{line} [μH/m]	c_{line} [nF/m]	g_{line} [μS/m]	d_{line} [m]	C_{x1} [nF]	C_{x2} [nF]
10	1	10.4	0.089	0.347	0.307	5	1000	5	5

5.4 Short-Circuit Fault Modeling and Parameterization

The possibility for simulating an SC fault was implemented by means of a *Fault* block connected pole-to-pole between the two DC line sections. This block represents a fault as an instantaneous resistance change. The unfaulted resistance was kept at the default Simscape value, which is infinity. Based on the work presented in [83], the value of the faulted resistance was set to 0.1 Ω. Temporal triggering was selected as the fault triggering mechanism, with the fault occurring at a specific time instant, t_0. In the fault simulations, t_0 = 100 ms was used, as this ensured a system in steady-state prior to the fault occurrence.

5.5 Modeling and Parameterization of the Energy Absorption Branch

The energy absorption branch of the VARC-CB module was implemented as a series-connection of a *Varistor* block and an inductor, as seen in Figure 5.1. The Simscape *Varistor* block represents a voltage-dependent resistor, and has an equivalent circuit equal to that given in Figure 2.7 minus the inductor (hence the external L_{MOV} in the simulation model). This block lets the user choose between two parameterization options: linear and power-law. The power-law parameterization implements a V-I relationship similar to

the V-I characteristics found in MOV datasheets, with a leakage region, a normal varistor region, and an upturn region, as was shown in Figure 2.6b. As this representation gives a more accurate and physically correct behavior of the MOV compared to the one provided by the linear parameterization, the power-law option was selected.

When using the power-law parameterization of the *Varistor* block, five parameter values defining its V-I behavior must be specified. To be able to obtain reasonable values, it was therefore necessary to find a suitable component, having a datasheet providing its V-I characteristics. "Suitable" here means having adequate ratings, i.e. providing the required clamping voltage at $I_{i,\text{max}}$, and the required energy absorption capability. The required clamping voltage was found using Equation (4.15): $V_{\text{clamp}} = 1.5 \cdot 10 \text{ kV} = 15 \text{ kV}$. The required energy handling was roughly estimated based on experimental results presented in [69]. This paper presents test results for a VARC-CB module of $V_{\text{clamp}} = 40$ kV interrupting $I_{i,\text{max}} = 16$ kA. The energy absorption of the MOV for this module was almost 600 kJ. The energy absorption needed will, naturally, be lower when $V_{\text{clamp}} = 15$ kV and $I_{i,\text{max}} = 2$ kA, however 600 kJ was considered as a rough overestimate.

As it is not possible to find one MOV having a clamping voltage of 15 kV at 2 kA, together with an energy rating as high as 600 kJ, it was necessary to series- and parallel-connect MOVs to obtain a module with the desired ratings. The BB series MOVs from Littelfuse [89], which are their industrial high-energy varistors with the highest voltage ratings, were considered for the basic building block of the module. Using the rule of thumb that an MOV can handle an energy amount of 200 J/cm^3 [81], the total MOV volume required for 600 kJ energy absorption is 3000 cm^3. With the dimensions given for the BB series MOVs in [89], this results in 24 MOVs being needed to provide the required energy rating. The V-I characteristics presented in the datasheet of the BB series is displayed in Figure A.1 in Appendix A. By examining these V-I characteristics, it was found that the aggregated V-I curve resulting from having six parallel columns of four series-connected V142BB60 MOVs has a clamping voltage of approximately 15 kV at 2 kA. A module consisting of six parallel MOV columns, each with four series-connected MOVs of the type V142BB60 was therefore chosen as the suitable component for the energy absorption branch of the VARC-CB module.

To obtain an adequate representation of the chosen MOV module with the power-law parameterization of the *Varistor* block, the five parameter values of the block were tuned until the block's V-I relationship fitted well the aggregated V-I curve of the MOV module. The resulting parameter values are included in Figure A.2 in Appendix A.

In addition to the five mentioned parameter values of the *Varistor* block, the values of R_{MOV}, C_{MOV}, and L_{MOV} had to be decided. As mentioned in Section 2.4, the material bulk resistance of an MOV is usually about 1–10 Ω. With six parallel columns of four MOVs in series, the resulting R_{MOV} is thus in the range 0.67–6.67 Ω. An R_{MOV} of 1 Ω was chosen. C_{MOV} was set to 3 nF, based on a typical capacitance value of 2 nF being given for one MOV in the varistor catalog from Littelfuse [49]. For the estimation of L_{MOV}, the formula presented in [90] was used, where the stray inductance of an MOV cylinder in nH is given by $10h$, where h is the cylinder height. With the dimensions given for the BB series MOVs in [89], L_{MOV} of the MOV module was estimated to 30 nH.

The main MOV parameter values are summarized in Table 5.2.

Table 5.2: MOV parameter values.

V_{clamp} [kV]	R_{MOV} [Ω]	C_{MOV} [nF]	L_{MOV} [nH]
15	1	3	30

5.6 VI Modeling and Parameterizaiton

The Simscape Electrical™ library contains a component named *Circuit Breaker (with arc)*, modeling a single-phase ACCB and its electric arc characteristics. This block could, however, not be used in the modeling of the VI, as it is based on the Mayr arc representation [91]. As was pointed out in Subsection 2.3.1.3, the Mayr formulation is suitable for describing high-pressure arcs. The model is, however, not appropriate for modeling low-pressure (vacuum) arcs, as these arcs exhibit different behavior.

To properly model the VI, it was therefore necessary to implement a model taking the behavior of vacuum arcs into account. Electrical VI modeling is in literature presented as a challenging task. Despite several approaches having been proposed, with different levels of detail and comprehensiveness [77, 92, 93, 94], it is difficult to find a convenient and accurate model [50]. Exact physical arc modeling is, however, beyond the scope of this thesis. At the same time, it was important to include the most essential arc characteristics in the simulation model, in order to obtain realistic operating conditions and performance.

Based on these preceding considerations, the simplified electrical VI model shown in Figure 5.2 was adopted. In this model, the VI is represented as an ideal resistive switch with a parallel branch containing parasitic elements, and it has three operating states: the closed, the arcing, and the open state. The model is inspired by the study of the VARC-CB presented in [69], which includes modeling considerations for the VI.

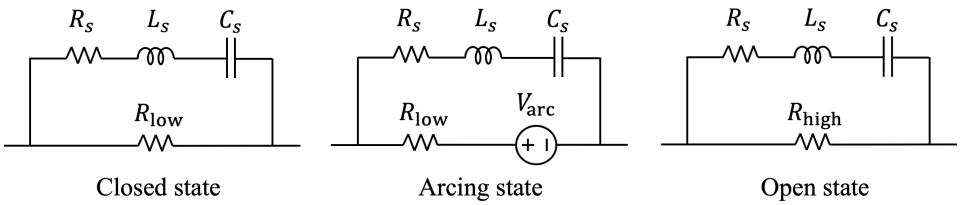


Figure 5.2: Operating states of the electrical model of the VI.

The closed state represents the VI contacts being closed, hence the VI providing a current path of very low resistance. The value of this contact resistance depends on the current rating of the breaker [95], but is typically in the microohm range for conventional mechanical ACCBs [96]. Manufacturers of medium- and high-voltage ACCBs usually specify the maximum contact resistance of the breaker, and through examining different datasheets, a maximum contact resistance of 35 $\mu\Omega$ was found for a 1.2 kA rated MV vacuum circuit breaker [97]. The low resistance value, R_{low}, was therefore chosen to be 35 $\mu\Omega$. For comparison, [69] employs a corresponding resistance value of 80 $\mu\Omega$.

In the arcing state, a constant DC voltage source is connected in series with R_{low}. This represents the unique characteristic of vacuum arcs of having an approximately constant voltage when in the diffuse arc mode. Diffuse arc mode is assumed, as the transition from diffuse to constricted mode usually occurs at an arc current of 10–15 kA, which is significantly higher than the current values encountered in the grid under consideration. As mentioned in Subsection 2.3.1.3, the arc voltage level depends on the electrode material used. If assuming copper electrodes, the typical arc voltage in the diffuse mode is about 20 V [40, 41]. The value of the constant DC source, V_{arc}, was therefore set to 20 V, which is somewhat lower than the 50 V used in [69].

In the open state, simulating the VI blocking the current path, the ideal resistive switch has a very high resistance value, R_{high}. The value of R_{high} was chosen to be 1 TΩ, as this was the value used to model the open state in both [69] and in [81].

The stray components of the VI are explained in [77], which studies the transient and high-frequency behavior of vacuum CBs. In this paper, the stray values are $R_s = 50\ \Omega$, $L_s = 50$ nH, and $C_s = 200$ pF. Similar values for R_s and L_s were chosen for the VI model in Figure 5.2. The same C_s value was, however, not adopted. In [77], reignitions resulting from the contact gap being too short at current zero-crossing are examined. In the VI model presented here, however, the C_s value should correspond to a fully open contact gap. This is because the VI is assumed to have opened completely when a current zero is generated (at which the stray VI branch comes into play). Consequently, the value of C_s should be lower than the 200 pF used in [77]. Based on the previously mentioned Annex B of the IEEE Standard C37.011, a value of 50 pF was chosen for C_s [39].

The electrical VI model in Figure 5.2 was implemented in Simulink as shown in Figure 5.3, where the VI operation is controlled by the control signal VI_{trig}.

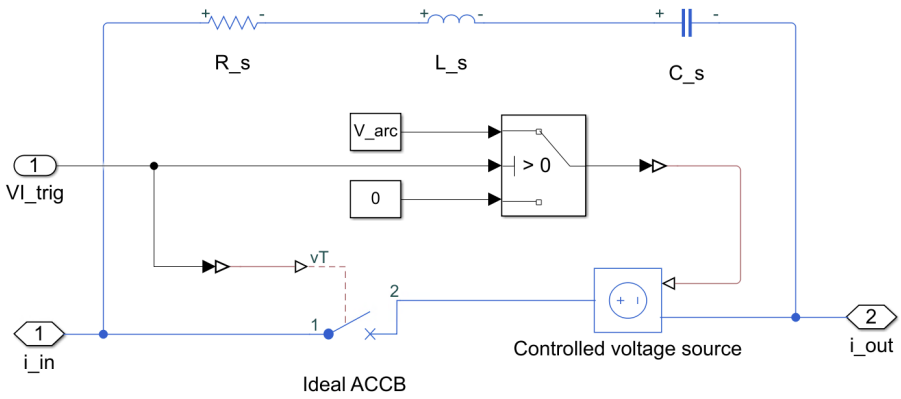


Figure 5.3: Simulation model of the VI.

The ideal ACCB seen in Figure 5.3 is a *Circuit Breaker* block (the one without arc), which models a single-phase ACCB controlled by a control signal *vT*. When *vT* is below a certain threshold value, the breaker is closed, providing a current path of low resistance. The *Closed resistance* parameter value of the block was set to $R_{\text{low}} = 35\ \mu\Omega$. When *vT* exceeds the threshold value, the ACCB breaks the circuit at the next zero-crossing of the current. The value for the *Open conductance* parameter was set to $1/R_{\text{high}} = 1$ pS.

vT is, as seen in Figure 5.3, equal to the control signal VI_{trig}. When VI_{trig} is below a certain threshold value, the ideal ACCB is closed, and the controlled voltage source has zero output voltage. This provides the closed state shown in Figure 5.2. When the control signal exceeds the threshold, on the other hand, the voltage source provides a constant voltage of $V_{\text{arc}} = 20$ V, resulting in the arcing operating state. Simultaneously, the ideal ACCB is triggered, meaning it will break the circuit at the next current zero-crossing. Thus, when the current through the VI crosses zero due to the oscillating current injected by the current injection branch, the resistance of the ideal ACCB changes to R_{high}, hence activating the open operating state.

As seen in Figure 5.1, the control signal VI_{trig} is provided by a *Step* block. When the step block is activated, it outputs a step from zero to one, causing the VI model to leave its closed state operation, and entering the arcing state. The step is activated at $t_2 = t_0 + t_{\text{rel}} + t_{\text{act}}$, as this is the instant where the initial contact separation in the VI takes place, hence where v_{VI} rises from zero to V_{arc} due to the arc creation (ref. Figure 3.3).

5.6.1 Timing Aspects

The timing aspects of the VI include the time instant where the VI receives a trip signal from the relay, t_1 (ref. Table 3.1), its actuation delay (t_{act}), and its opening time (t_{open}).

As discussed in Subsection 3.2.3, the time interval between the fault inception at t_0 and the VI receives a trip signal at t_1 is constituted by the total relay time, t_{rel}. The duration of this interval depends on the relaying technique used, and also on the system conditions and configuration prior to, and those resulting from the fault occurrence. For simplicity, however, a constant relay time was assumed. The same value as used in [50] and [81] was implemented, resulting in $t_{\text{rel}} = 2$ ms.

The actuation delay is decided by the type of actuator employed. For operating the VI of the VARC-CB, the use of a Thomson coil actuator is suggested [69, 75], similar to that discussed for UFDs in Subsection 2.3.2. As both [69] and [75] report an operating delay of around 1 ms when using this actuator type, the value of t_{act} was set to 1 ms.

t_{open} depends on the actuator type used, as well as on the voltage withstand capability required by the contact gap. The higher the voltage withstand capability needed, the greater the gap length has to be, resulting in a longer opening time. The value of the maximum voltage the VI must be able to handle, together with the speed at which the VI contacts are separated are therefore decisive for the value of t_{open}.

In [69], where a Thomson coil actuator is used for the VI of a VARC-CB, a contact separation speed of 3 m/s is assumed. [36] and [93] present 1 m/s as the average opening velocity of a vacuum CB, however the actuator type is not specified. The maximum voltage the VI of the VARC-CB module in Figure 5.1 must be able to handle equals the peak value of the TIV. This peak value is determined by the maximum MOV voltage, together with the transient voltage oscillation in v_{VI}, which were discussed in Subsection 4.3.4.3. The maximum MOV voltage is the sum of the clamping voltage and the maximum possible voltage across R_{MOV}, which is $V_{\text{clamp}} + R_{\text{MOV}} I_{i,\text{max}}$ = 17 kV. To have some safety margin, a conservative estimation of 30 kV can be made for the maximum VI voltage, and 1 m/s for the opening speed. Assuming, for simplicity, a linear dependence between dielectric strength and contact distance, and using 30 kV/mm as the relation [77, 98], an opening time of t_{open} = 1 ms results.

5.6.2 di/dt- and dv/dt capabilities

Neither the di/dt- nor the dv/dt capability of a VI are constant values which can be found in datasheets. The maximum di/dt and the maximum dv/dt the VI can withstand depend on the interruption conditions, and are influenced by factors such as the interruption current, the gap distance, and the arcing time [36, 39, 50]. For simplicity, however, constant values were assumed for the modelled and simulated VI. According to [77], vacuum CBs are able to interrupt currents having maximum di/dt values in the range 150–1000 A/μs. In [81], where a component level model of an MCB with active current injection is presented, 650 A/μs is used as a constant di/dt capability of the employed VI. The authors emphasize that the quenching capability varies with the current magnitude being interrupted, but 650 A/μs can be considered a reasonable critical threshold value. The same constant value was therefore adopted in the modeling and simulations of the VARC-CB module. When it comes to the dv/dt capability of the VI, values in the kV/μs range are normally found in literature. In [99] and [100], 10 kV/μs is given as an upper limit for the dielectric recovery of vacuum CBs, and in [101], medium-voltage VIs are described with having a recovery rate of about 5 kV/μs. It thus seemed reasonable to assume a maximum dv/dt capability of the VI in the range 5–10 kV/μs.

It should be noted that the di/dt- and dv/dt capabilities were not implemented in the simulation model of the VI. Consequently, the modeled VI performs a successful interruption, even if the current and/or voltage stresses exceed the specified capabilities. These aspects were left out to keep the complexity of the model to a reasonable level. In addition, exact physical arc modeling is beyond the thesis scope. Instead, the di/dt- and dv/dt capabilities were accounted for through the parameterization of the model, i.e. by using Equations (4.30), (4.34), (4.40), and (4.41) to ensure di/dt- and dv/dt values within the specified capabilities in the simulations.

5.6.3 Current Chopping

In Subsection 2.3.1.3, current chopping was highlighted as a typical vacuum CB phenomenon. However, it has been reported that generally, only power frequency (50 or 60 Hz) currents are chopped by vacuum CBs, whereas high-frequency oscillating currents are not [41]. Current chopping was therefore not implemented in the simulation model.

5.6.4 Overview of VI Parameterization

Table 5.3 summarize the preceding section, by presenting an overview of the values chosen for the VI parameters and for the VI related timing aspects.

Table 5.3: Values of the VI parameters and the timing aspects related to the VI.

R_{low}	R_{high}	V_{arc}	R_s	L_s	C_s	$\left(\frac{di}{dt}\right)_{\text{cap}}$	$\left(\frac{dv}{dt}\right)_{\text{cap}}$	t_{rel}	t_{act}	t_{open}
[$\mu\Omega$]	[TΩ]	[V]	[Ω]	[nH]	[pF]	[A/μs]	[kV/μs]	[ms]	[ms]	[ms]
35	1	20	50	50	50	650	5–10	2	1	1

5.7 RCB Modeling and Parameterization

The RCB is supposed to isolate the VARC-CB module from the grid supply after the module has performed a current interruption operation. For the purpose of modeling, a standard ACCB can be used, which breaks the circuit at the moment where the line current crosses zero [50]. This was implemented in the simulation model by means of a *Circuit Breaker* block (without arc). The default *Closed resistance* parameter value, 1 mΩ, was kept, which is the same as the one used for simulating the VARC-CB in [82]. The default value for the *Open conductance* parameter, 1 μS, was also kept. As can be seen in Figure 5.1, the control signal provided to the RCB is the same as the triggering signal of the VI. As a result, the RCB will break the circuit when i_{line} has been forced to zero by the VARC-CB module.

5.8 Modeling and Parameterization of the Current Injection Branch

The current injection branch contains L_p, C_p, R_p, and the VSC. L_p, C_p, and R_p were all modeled using standard components from the passive component library in Simscape. Figure 5.4 shows how the VSC was realized as a simulation model.

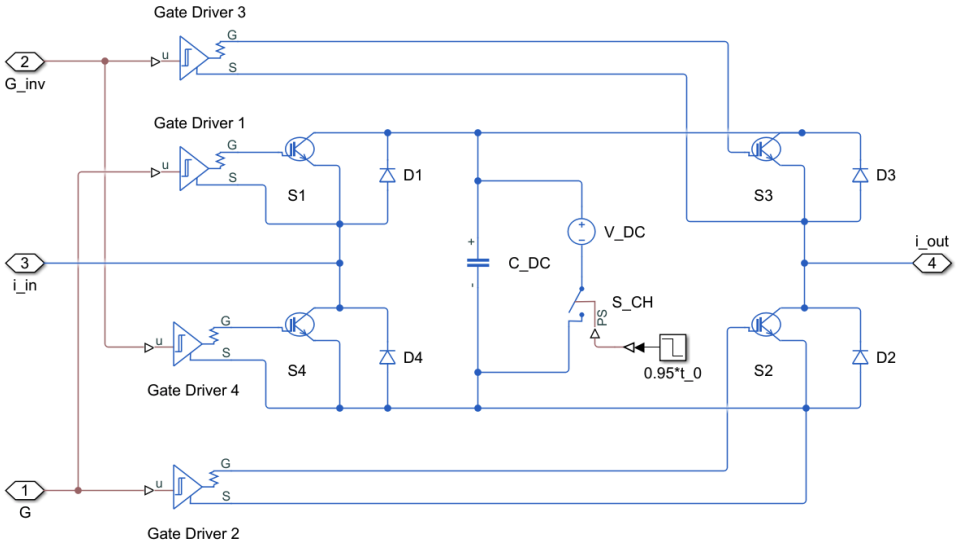


Figure 5.4: Simulation model of the VSC.

5.8.1 Switching Frequency

A main parameter value to decide for the VSC was its switching frequency. When discussing the design considerations for the semiconductor switches of the VSC in Subsection 4.3.2.2, it was highlighted that the switch type chosen imposes a limit on the maximum switching frequency. As IGBT is the device type suggested for the VARC-CB concept, the maximum handleable frequency of IGBTs had to be taken into account. Normally, the maximum frequency seen in applications employing IGBTs as switching devices is limited to around 20 kHz [102]. However, as was also pointed out in Subsection 4.3.2.2, due to the soft switching conditions present in the VSC of the VARC-CB, higher frequencies than what normally encountered in IGBT applications may be used. The switch type employed, IGBT, hence allowed for a maximum f_{sw} of at least 20 kHz. However, it was observed that using very high switching frequencies easily compromised the design constraint related to the RRITIV and the VI's dv/dt capability (Equation (4.40)). In particular, choosing an f_{sw} value exceeding around 20 kHz made it difficult obtaining a breaker design not violating any component limitations. A switching frequency of 10 kHz was chosen, as this made an adequate breaker design possible, and as this is the frequency used in all available literature on the VARC-CB concept.

5.8.2 DC Link

C_{DC} and V_{DC} were the parameter values to decide for the DC link of the VSC. It is evident from the equations summarizing the design strategies in Subsection 4.3.5 that both C_{DC} and V_{DC} show interdependence with several other of the breaker parameters, such as Z_{LC}, f_{LC}, Q, and K. For simplicity, it was decided to make qualified choices of the C_{DC} and V_{DC} values, and then adjust other parameter values, in particular Z_{LC}, to ensure all the derived design constraints being satisfied.

The values of C_{DC} and V_{DC} were both selected based on the parameter values of the VARC-CB module prototype presented in [69]. The value of the DC link capacitance was chosen to be similar to the one given in the paper, $C_{\text{DC}} = 3.75$ mF. The V_{DC} value was selected to obtain a V_{DC}–V_{clamp}–ratio in the same range as the one in the paper, which is 1.6 kV / 40 kV = 0.04. A value of 400 V was chosen, giving V_{DC} / $V_{\text{clamp}} \approx 0.03$.

5.8.3 Charging Circuit

As seen in Figure 5.4, the charging circuit of the DC link capacitor was realized in Simulink by means of a *DC Voltage Source* block and a *Switch* block. The constant output voltage of the voltage source was set to V_{DC}. The closed resistance of the *Switch* was set to R_{CH}, providing the charging resistance when in its closed state. A charging resistance value of 1 Ω was used, resulting in a charging time constant of $\tau_{\text{CH}} = R_{\text{CH}}C_{\text{DC}} = 3.75$ ms. The control of S_{CH} is provided by a step block, which keeps the switch in the closed position until right before the fault inception at t_0, where the switch is opened. This is to prevent the charging circuit from interfering with the interruption process of the breaker. As previously mentioned, t_0 was set to 100 ms in the simulations, which ensured C_{DC} being fully charged when opening S_{CH} (as this happens after approximately $5\tau_{\text{CH}} = 18.75$ ms).

5.8.4 Passive Resonant Circuit

The parameter values to be specified for the passive resonant circuit were L_p, C_p, and R_p. The stray resistance R_p was, for simplicity, set equal to the one used for the VARC-CB prototype in [69], giving $R_p = 0.05\ \Omega$. To specify the values of L_p and C_p it was sufficient to set a value for Z_{LC}. As f_{LC} was already selected, the values of Z_{LC} and f_{LC} would uniquely determine the L_p and C_p values through Equations (3.1) and (3.3).

To decide the Z_{LC} value, it was necessary to take several design constraints into account. First, it had to be ensured that its value did not violate the limitation given in Equation (4.20). This equation required it to be smaller than 6.7 Ω, in order to prevent the MOV clamping voltage being reached before the designated time instant.

Second, Equation (4.14) had to be considered, to ensure that the maximum achievable oscillating current would exceed a safety margin times $I_{i,\text{max}}$. The safety margin K was chosen to 1.1, as suggested in [59], resulting in the desirable maximum value for $\hat{i}_{\text{VSC}}$ being at least 2.2 kA. By using the v_{DC} and $\hat{i}_{\text{VSC}}$ dynamics in Equations (4.12) and (4.13), it was found that Z_{LC} had to be equal to or below 5.3 Ω for $\hat{i}_{\text{VSC,max}}$ to exceed 2.2 kA.

Third, it was important to ensure that the constraint imposed by the VI's di/dt capability in Equation (4.34) was not violated. By plotting the left- and right-hand sides of this equation for different Z_{LC} values, 0.19 Ω resulted as the minimum required Z_{LC} value.

Fourth, the limitations imposed by dv/dt capability of the VI had to be accounted for: Equations (4.40) and (4.41) had to be satisfied. It was found that Equation (4.41) did not impose any tighter restrictions on the value of Z_{LC} than those mentioned in the previous paragraphs. In fact, a Z_{LC} value exceeding several thousands of ohms had to be chosen to obtain a C_p value violating (4.41). Equation (4.40), on the other hand, was more challenging to satisfy. It was found that a higher Z_{LC} value resulted in a lower WCS RRITIV value, and to obtain a WCS RRITIV value below 10 kV/μs, the value of Z_{LC} had to exceed 0.29 Ω. With a maximum restriction on Z_{LC} of 5.3 Ω, it was however not possible to obtain a WCS RRITIV value below 5 kV/μs. Consequently, a VI with high dv/dt capability had to be assumed in order to obtain an acceptable Z_{LC} value.

Finally, it was, as mentioned in Subsection 4.3.3, desirable to choose Z_{LC} as high as possible, to limit the current pulse amplitude at a potential reignition.

The value of Z_{LC} was chosen to 4.85 Ω, giving L_p = 77.2 μH and C_p = 3.28 μF. This resulted in a WCS MOV voltage prior to t_4 of 11.3 kV, calculated by Equation (4.19), which is well below the clamping voltage of 15 kV. The calculated value of $\hat{i}_{\text{VSC,max}}$ was 2.29 kA, exceeding the minimum of 2.2 kA. The left-hand side of Equation (4.34) was calculated to 75.1 A/μs, while the value of the right-hand side was 650.2 A/μs, hence satisfying the di/dt criterion. The C_p value of 3.28 μF is also well above the minimum of 2 nF required by Equation (4.41).

Z_{LC} = 4.85 gave f_s = 255 kHz and ITIV_{WCS} = −12 kV, resulting in a WCS RRITIV value of 6.95 kV/μs. A dv/dt capability of at least 7 kV/μs thus had to be assumed.

From the two previous paragraphs it is clear that Z_{LC} = 4.85 Ω gives an adequate breaker design, however with a possibility of a risk of high RRITIV values. If the dv/dt capability of the VI can be as high as 10 kV/μs indicated by [99], the calculated WCS RRITIV value represents no challenge to the VI. However, if the dv/dt capability is in the range of 5 kV/μs, as stated in [101], the RRITIV in a worst-case scenario may exceed what the VI can handle.

It was found that it was possible to obtain a WCS RRITIV value lower than 5 kV/μs if decreasing either f_{LC}, V_{DC}, or both. However, decreasing these parameter values made it difficult to obtain a design satisfying the $\hat{i}_{\text{VSC,max}}$ requirement in Equation (4.14). More specifically, it was difficult to obtain sufficient initial energy in the DC link of the VSC without increasing C_{DC} significantly. The values of f_{LC} = 10 kHz and V_{DC} = 400 V were therefore kept, hence assuming a VI with high dv/dt capability is obtainable.

5.8.5 Switch Positions

The switch positions of the VSC were implemented using *N-Channel IGBT* blocks connected in anti-parallel with *Diode* blocks. To specify the parameter values of these blocks, it was necessary to find datasheets of physical components having sufficient ratings.

As discussed in Subsection 4.3.2.2, the switch positions of the VSC must have maximum blocking voltage capabilities exceeding V_{DC}. They must also be able to carry a maximum current of $I_{i,\text{max}}$ for a short amount of time. With $V_{\text{DC}} = 0.4$ kV and $I_{i,\text{max}} = 2$ kA, a 1.2 kV/1.2 kA IGBT module was considered adequate. With a voltage rating of 1.2 kV, a safety factor of $1.2/0.4 = 3$ is obtained. This provides some margin for overvoltages, e.g. caused by stray inductances which in a physical application will be present in the VSC. With a continuous current capability of 1.2 kA, the IGBT module typically has a maximum pulse current rating of 2.4 kA. It will thus be able to handle the maximum possible VSC current peak of 2 kA. The 1.2 kV/1.2 kA module SKM1200MLI12TE4 from SEMIKRON was selected, and the values for IGBT1 and Diode1 from its datasheet [103] were used to specify the values of the *N-Channel IGBT* and *Diode* Simscape blocks.

The *N-Channel IGBT* block provides two main modeling options, *Full I-V and capacitance characteristics* and *Simplified I-V characteristics and event-based timing*, with the former being significantly more detailed than the latter [104]. To obtain the most accurate modeling, the first option was chosen. Using this option requires the user to fill in several parameter values, among them six values in the *Advanced* tab of the block. These six parameters are to be used for fine-tuning the I-V characteristics of the modeled device. To be able to utilize these parameters effectively, the example file and script provided by MathWorks® in [105] was used, which lets the user generate I_C versus V_{CE} curves for an *N-channel IGBT* block. The parameter values in the *Advanced* tab were tuned until the obtained I_C-V_{CE} plot was similar to the one found in the IGBT datasheet. The I_C-V_{CE} curves from the datasheet can be found in Figure B.1 in Appendix B, where the whole black line $\left(T_j = 25^\circ\right)$ shows the curve used as a reference when fine-tuning. The resulting values of the *Advanced* tab are included in Figure B.2 in Appendix B.

5.8.6 VSC Control

Each IGBT of the VSC is controlled by means of a separate *Gate Driver* block, as seen in Figure 5.4. This block gives an abstracted representation of an integrated circuit of a gate driver [106]. When the block input rises above its logic 1 level or below its logic 0 level, a transition of the block output from/to its off-state gate-source voltage to/from its on-state gate-source voltage is initiated. The off-state and on-state voltages were set to −15 V and +15 V, respectively. The dynamics of the state transitions are decided by the driver parameterization chosen. The block provides two parameterization options: *Output*

impedance and *Rise and fall times*. The latter option was selected, making it necessary to specify values for rise time, fall time, and load capacitance. These parameter values were adjusted through simulations, until adequate gate and switch behavior was observed.

Since the switching scheme of the VSC involves (S_1, S_2) and (S_3, S_4) being treated as switch pairs, the input signals provided to *Gate driver 1* and *Gate driver 2* are similar (G), and the input signals provided to *Gate driver 3* and *Gate driver 4* are similar (G_{inv}). Furthermore, the two input signals, G and G_{inv}, are complementary.

The circuitry implemented to generate and control G and G_{inv} is displayed in Figure 5.5. The circuitry consists of three main subcircuits: an i_{VI} zero-crossing detector (green), a gate signal generator (yellow), and a signal selector (blue).

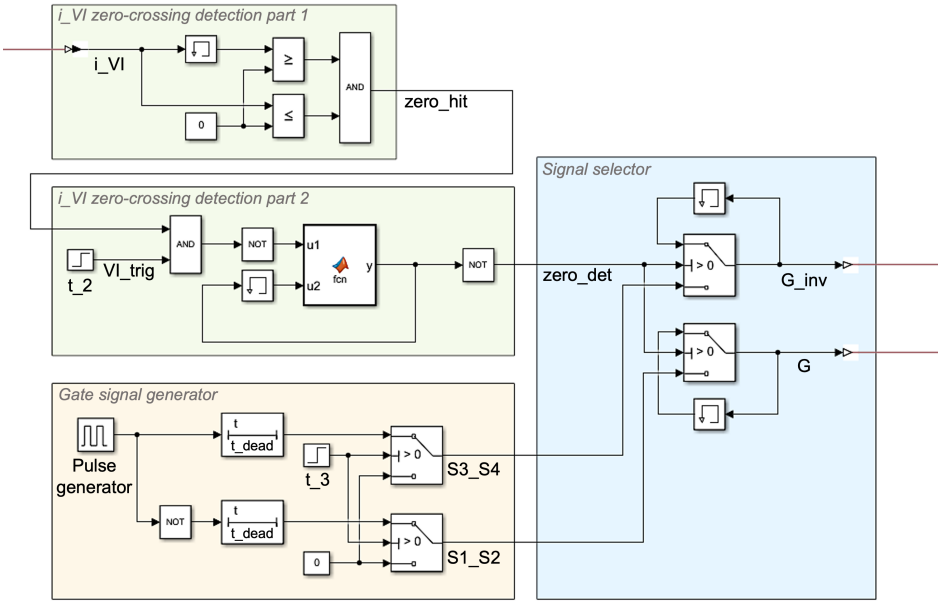


Figure 5.5: Circuitry for generation and control of the gate signals provided to the VSC switches.

Before i_{VI} reaches zero, the signals G and G_{inv} equal the output from the gate signal generator, S_1_S_2 and S_3_S_4, respectively. Before the VSC triggering at t_3, both S_1_S_2 and S_3_S_4 equal zero. Consequently, all four gate drivers of the VSC outputs -15 V, resulting in the IGBTs being in their off-state. At t_3 the step block causes S_1_S_2 and S_3_S_4 to become equal to the signals coming from the *Pulse Generator* block. The *Pulse Generator* block outputs a square wave with amplitude one, a frequency of f_{LC}, and a pulse width of 50%. As the gate signals of the two switch pairs are to be complementary, a *NOT* operator is connected in series with the *Pulse Generator* block in the S_1_S_2 path. A small delay, t_{dead}, is implemented to provide some dead time between the complementary switch signals, in order to prevent bridge shoot-through. In this short time interval, the VSC current will flow through the anti-parallel diodes of the IGBTs which are turning off.

When the VI current crosses zero at t_4, the signal *zero_det* changes from 0 to 1, causing G and G_{inv} to become equal to the output from the two *Memory* blocks of the signal selector. As the *Memory* blocks holds and delays their input by one time step, G and G_{inv} become constant at their t_4-values. Consequently, at t_4, the VSC stops switching, and from t_4 and onwards, the switches are kept in the switching state they were in at t_4.

The change in *zero_det* at t_4 is controlled by the i_{VI} zero-crossing detection circuitry displayed on green background in Figure 5.5. Part 1 of this circuitry takes a measurement of i_{VI} as input. Its output, *zero_hit*, is 1 when i_{VI} hits zero, and 0 otherwise. *zero_hit* is, together with VI_{trig} taken as input to the *AND* block of part 2 of the detection circuitry. At t_2 the value of VI_{trig} steps from 0 to 1. Consequently, at a zero-crossing of i_{VI} occurring *after* the VI triggering at t_2, the output of the *AND* block becomes 1. At the very first zero-crossing occurrence, i.e. at t_4, the blocks following the *AND* block ensure that the value of *zero_det* changes from 0 to 1, and is permanently kept at 1 from this point on.

The triggering of the VSC happens at t_3. As discussed in Subsection 4.3.4.1, the VSC triggering must be delayed with respect to the initial VI contact separation at t_2, in order to ensure sufficient opening time for the VI before the zero-crossing in i_{VI} is generated. For this to be ensured in all possible current interruption scenarios, the delay, $t_{\text{VSC,delay}}$, should be designed according to Equation (4.24). This resulted in $t_{\text{VSC,delay}} \geq 0.67$ ms, and the value of t_3 was set to be $t_2 + 0.67$ ms in the model.

5.8.7 Parameterization Overview

Table 5.4 summarizes the preceding section, by presenting an overview of the selected and designed values of the current injection branch related parameters.

Table 5.4: Parameter values related to the current injection branch.

f_{LC} [kHz]	C_{DC} [mF]	V_{DC} [V]	R_{CH} [Ω]	Z_{LC} [Ω]	L_p [μH]	C_p [μF]	R_p [Ω]	K [-]	$t_{\text{VSC,delay}}$ [ms]
10	3.75	400	1	4.85	77.2	3.28	0.05	1.1	0.67

5.9 Modeling and Parameterization of the Current-Limiting Inductor

The current-limiting inductor was modeled using an *Inductor* block from the passive component library in Simscape. The value of L_{lim} was determined by adjusting the inductance of the block until a $\hat{I}_{\text{line}}$ value of $I_{i,\text{max}}$ = 2 kA was obtained during a terminal fault simulation. This resulted in L_{lim} = 44.5 mH, which complies with design Equation (4.30).

Chapter 6

Simulation Results and Discussion

This chapter presents results from simulations performed with the model described in the previous chapter, and the findings are discussed. The aims of the simulations are to provide visualizations underpinning the described operating principles and characteristics of the VARC-CB module, to validate the proposed design strategies and simulation model, and to investigate possible improvements in the breaker design and modeling.

Three main simulation cases are defined to provide visualizations and validation. Case 1 simulates an interruption of a terminal fault, and is included to validate the breaking capability of the VARC-CB module when maximum fault current occurs. Case 2 simulates an interruption of $I_{\text{nom}} = I_{i,\text{min}} = 1$ kA, and verifies the VARC-CB modules ability to interrupt load currents. Case 3 simulates an interruption of reverse fault current, and is used to prove that the breaker module is capable of operating bidirectionally. Relevant waveforms from the three cases are included in Sections 6.1, 6.2, and 6.3, respectively. The simulation results are examined in light of the analysis of the VARC-CB module presented in the three previous chapters, with a particular focus on evaluating the robustness of the performed analysis, the design strategies derived, and the simulation model developed.

Section 6.4 provides the discussion part of the chapter. The simulation results from the three main cases are compared in Subsection 6.4.1, with interesting differences being pointed out and discussed. Subsection 6.4.2 points out a weakness in the analytical investigation performed, clearly shown by comparing simulation results with estimates obtained using equations derived in Chapter 4. Two possible improvements in the design and modeling of the VARC-CB module are proposed in Subsections 6.4.3 and 6.4.4. The first subsection presents the possibility of implementing an auxiliary passive resonant circuit in the breaker topology in order to ensure favorable interruption conditions for the VI in all interruption cases. The second subsection discusses the possible gains of the VSC triggering instant being adjustable, instead of having it fixed as suggested in Subsection 4.3.4.1. Finally, in Subsection 6.4.5, modeling aspects related to the voltage stresses on the VI are discussed. In particular, the impact of the system modeling on the obtained RRITIV values is examined, and possible shortcomings of the considered model are highlighted.

6.1 Case 1: Interrupting a Terminal Fault

Figure 6.1 displays the course of i_{line}, i_{VSC}, and i_{MOV} resulting from a simulation of a terminal SC fault, which gives the highest value of $\hat{I}_{\text{line}}$. The fault inception is at $t = 0$.

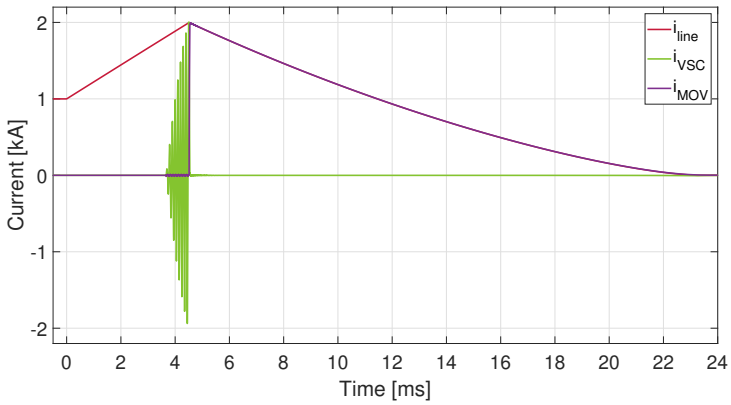


Figure 6.1: Line, VSC, and MOV currents during a terminal fault.

The line current begins to rise from the nominal value of 1 kA at the fault inception, and rises until reaching $\hat{I}_{\text{line}}$ = 1997 A at t = 4.51 ms, at which the fault is neutralized. $\hat{I}_{\text{line}}$ is kept just below $I_{i,\text{max}}$ = 2 kA, which was the aim when designing L_{lim}.

As the trip order is received by the VARC-CB after t_{rel} = 2 ms, the fault is neutralized in 2.51 ms. This is in accordance with the first point of the numbered list in Subsection 2.2.2, indicating that a DCCB operating in an MVDC grid must be able to neutralize a fault within few milliseconds from the trip instant. At t = 23.3 ms, the line current has successfully been forced down to zero. The total operation time, from the triggering signal was received by the VI from the relay until i_{line} = 0, is thus t_{tot} = 23.3–2 = 21.3 ms.

The waveforms in Figure 6.1 coincide well with the ones used to illustrate the basic, idealized operating principles of the VARC-CB module in Figure 3.3. A main difference, however, is the time scale; as previously pointed out, the proportions in Figure 3.3 are not to scale. In particular, the ratio between the time intervals t_2–t_5 and t_5–t_6 is significantly smaller in Figure 6.1 than what is indicated in Figure 3.3. Another difference is the course of i_{line} and i_{MOV} after t_5. As seen in Figure 6.1, the decrease in these currents is not completely linear; the rate of the decrease slows time with time. This is caused by the decrease in v_{MOV} occurring during this time interval, which is due to i_{MOV} being forced towards zero (ref. the MOV V-I characteristics in Figure 2.6b).

It should also be noted that the transient responses mentioned in Subsection 3.2.9 cannot be seen in Figure 6.1, nor in the other simulation results to be presented. In Subsection 3.2.9, it was stated that at the zero of the line current, transient, resonant responses in i_{line}, i_{VSC}, and v_{MOV} will be initiated. These responses can be observed in the simulation and experimental results of the VARC-CB module presented in [69]. However, as the RCB is opened exactly at the zero-crossing of the line current in the Simulink simulations, the galvanic isolation provided by the RCB prevents the transient responses from occurring.

Figure 6.2 includes details of i_{line}, i_{VSC}, and v_{VI} from a time instant slightly before the fault inception, until a time instant slightly after the VSC has been activated (remark the different scales of the vertical axes). At t = 3 ms, corresponding to the sum of the relay time and the VI actuation delay, there is a step in the VI voltage from 0 to 20 V. This indicates the initial contact separation in the VI and the arc inception, at which the VI voltage increases from its steady state of around zero to the voltage of the burning arc of V_{arc} = 20 V. The triggering of the VSC is, as discussed in Subsection 4.3.4.1, delayed with respect to the initial VI contact separation, and occurs at t = 3.67 ms. This is in accordance with the selected $t_{\text{VSC,delay}}$ value, which is 0.67 ms.

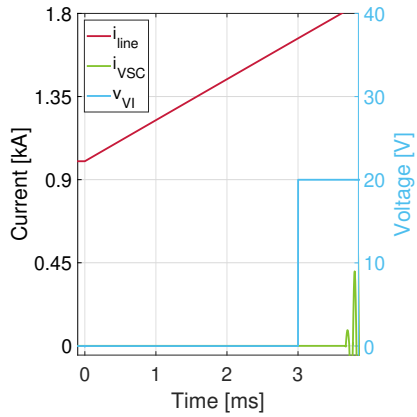


Figure 6.2: Line current, VSC current, and VI voltage during a terminal fault.

The left plot in Figure 6.3 displays details of i_{line}, i_{VSC}, and v_{VSC} from a time instant slightly before the VSC is activated, until a time instant slightly after the line current has commutated from the current injection branch into the energy absorption branch. The right plot in Figure 6.3 shows the details of i_{line} and i_{VI} during the same time interval. These waveforms also coincide well with the ones in Figure 3.3, with the exception of v_{VSC}, as the decrease in $|v_{\text{VSC}}|$ during the VSC operation was not accounted for in the idealized waveform in Figure 3.3.

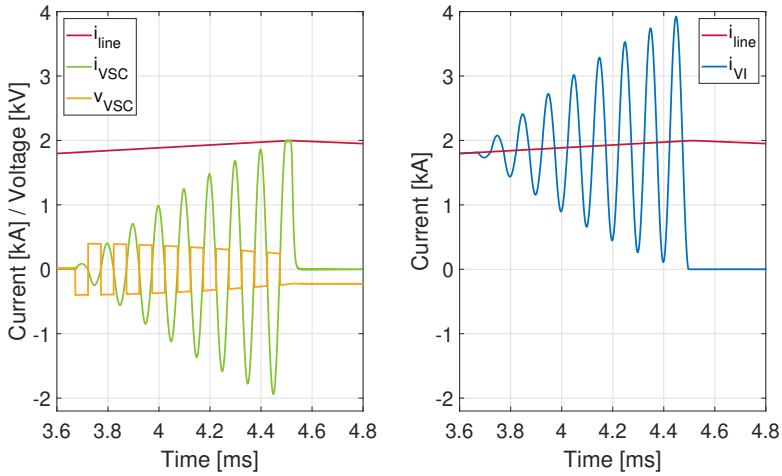


Figure 6.3: Terminal fault. Left: Line current, VSC current, and VSC voltage. Right: Line and VI currents.

After its activation at t = 3.67 ms, the VSC starts performing switching operations. This results in oscillations of increasing amplitude in i_{VSC} and in i_{VI}, as observed in Figure 6.3. The operations are, as expected, in synchronism with the current oscillations, which is seen by i_{VSC} and v_{VSC} being in phase. The VSC performs in total N = 17 switching operations before the magnitude of i_{VSC} reaches the level of i_{line}, causing i_{Vi} to cross zero.

The zero-crossing of i_{VI} occurs at t = 4.50, which is 1.50 ms after the initial contact separation in the VI. Consequently, the VI is provided 1.50 ms for opening its contacts, which is more than the opening time considered in the design, t_{open} = 1 ms. The VI is thus fully open when i_{VI} reaches zero, which facilitates successful current interruption in the VI. The interruption conditions for the VI are also favorable in terms of the di/dt at the zero-crossing. The i_{VI} slope at t = 4.50 ms is measured to 16.7 A/μs, which is well below the 650 A/μs considered for the di/dt capability of the VI.

Favorable dv/dt conditions are also observed for the VI in the simulation results. The value of the ITIV is measured to −1.24 kV, and the RRITIV is 0.92 kV/μs. The positive RRTIV is measured to 0.62 kV/μs. Both dv/dt values are well below the defined capability of the VI, and both the ITIV and the RRITIV values are significantly lower than the WCS values of −12 kV and 6.95 kV, respectively, which were calculated in Subsection 5.8.4.

Plots of the v_{VI} waveform are included in Figure 6.4. The left plot includes v_{VI} together with i_{VI} in a time interval reaching from an instant slightly before i_{VI} crosses zero, until a time instant slightly after v_{VI} has peaked. The right plot displays a zoom of the time interval around the zero-crossing of i_{VI}, to show the details the v_{VI} waveform directly after the current zero. v_{MOV} is also included in the plot.

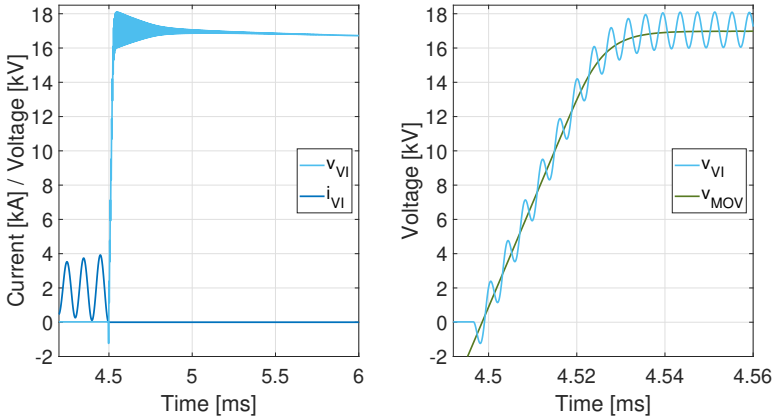


Figure 6.4: Terminal fault. Left: VI voltage and current. Right: VI and MOV voltages.

Figure 6.4 depicts what was explained and discussed in the second paragraph of Subsection 4.3.4.3: the course of v_{VI} is a superposition of v_{MOV} and a transient, oscillatory response, similar to how the TRV of an ACCB in an AC system is a superposition of the power frequency system voltage and a fast transient response.

A consequence of the transient oscillations v_{VI}, is that the maximum voltage experienced by the VI exceeds the maximum MOV voltage. The peak of v_{VI} in Figure 6.4 is

measured to $\hat{V}_{\mathrm{VI}}$ = 18.1 kV, whereas the v_{MOV} peak is 17.0 kV. It is, however, reasonable to assume that the damping of the transients in a real application would be higher than that seen in the figure, giving a lower v_{VI} peak value. As no frequency-dependence is included in the simulation model, the increase in effective resistance at high frequencies is not accounted for. Due to the skin effect, the effective resistance of e.g. R_p will, at the high frequencies of the v_{VI} oscillations, be higher than the constant value used in the simulations [107]. Resultantly, the high-frequency v_{VI} oscillations will, in reality, be more damped than what is observed in the simulation results.

The right plot in Figure 6.4 shows that the transient v_{VI} response has one dominating frequency. This is as expected from the discussion on the RRITIV in Subsection 4.3.4.3, where it was pointed out that a terminal fault short-circuits C_{x2} and the passive DC line components, preventing them from affecting the transient v_{VI} response. As a result, the frequency of the loop formed by C_{x1} and the VARC-CB module will dominate, which, by Equation (4.35), is calculated to f_s = 255 kHz. This agrees well with the dominating frequency in Figure 6.4, which is measured to around 254–256 kHz.

The measured ITIV magnitude, on the other hand, is quite much lower than what can be calculated using Equation (4.36) presented in Subsection 4.3.4.3. This equation gives $|\mathrm{ITIV}|$ = 2.38 kV, whereas the measured magnitude is 1.24 kV. This difference is due to the increase in v_{MOV} between the instant of VI current zero and the instant where the ITIV occurs, which was not accounted for when deriving Equation (4.36). Taking this into consideration will give an equation providing a more accurate estimation of the ITIV. At the same time, as the overestimate in Equation (4.36) was further used in the derivation of the RRITIV design criterion in Equation (4.40), some safety margin was automatically incorporated. The RRITIV design criterion can thus be considered conservative, but at the same time ensuring a reliable design in terms of favorable dv/dt conditions for the VI.

The left plot in Figure 6.5 displays i_{MOV} and v_{MOV} in the time interval 2–30 ms. The right plot shows the energy absorbed by the MOV in the same time interval.

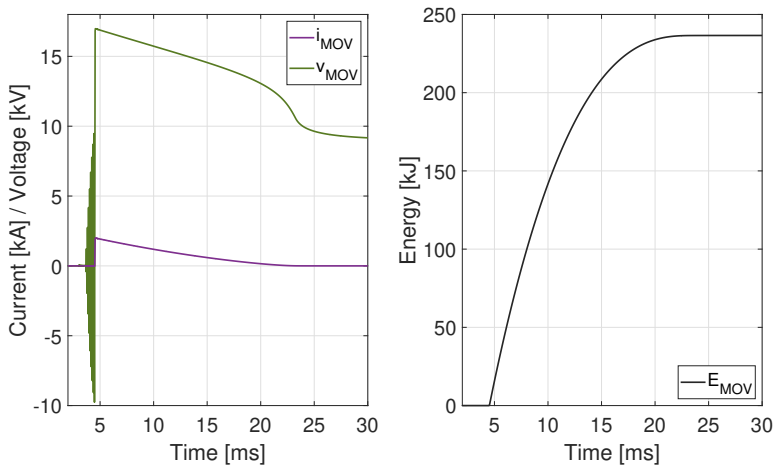


Figure 6.5: Terminal fault. Left: MOV current and voltage. Right: Energy absorption of the MOV.

The MOV voltage is, as expected, oscillating with increasing amplitude when the VSC operates, and the maximum amplitude reached by these oscillations is kept below V_{clamp}, as desired. The value of the maximum amplitude, which occurs at the very last negative peak of v_{MOV}, is measured to 9.8 kV, which is significantly lower than V_{clamp} = 15 kV. As a result, the leakage current through the MOV during the VSC operation is very low, as was the aim leading to the derivation of the design criterion in Equation (4.20) in Subsection 4.3.3. The leakage current is hard to observe in Figure 6.5, however some very small oscillations around zero can be seen in i_{MOV} in Figure 6.1.

When the VSC operation finishes at t = 4.50, the v_{MOV} oscillations cease, and the MOV voltage rises almost linearly, due to the charging of C_p. The line current commutates into the energy absorption branch when v_{MOV} reaches V_{clamp}, seen by the step in i_{MOV} in the left plot. v_{MOV} keeps rising until reaching a maximum value measured to $\hat{V}_{\text{MOV}}$ = 17.0 kV, corresponding to $V_{\text{clamp}} + R_{\text{MOV}} I_{i,\text{max}}$. The MOV module then clamps the voltage at a level higher than the MVDC voltage source, forcing the line current, hence also the MOV current, to zero. As seen in the figure, the MOV voltage decreases after its peak has been reached, which is in accordance with the V-I characteristics of the MOV module.

The right plot in Figure 6.5 shows the energy absorbed by the MOV module, which is calculated by means of Equation (2.4). The accumulated energy absorption is measured to be E_{MOV} = 237 kJ. This is in the same range as, but quite much less than the 600 kJ considered when developing a suitable MOV module in Section 5.5. The developed MOV module constituted by 24 MOVs is thus overrated, and optimally, the number of MOVs could have been chosen lower. This would, however, not have had a large impact on the behavior of the energy absorption branch in the simulations, hence the overrating does not impair the validity of the simulation results.

Table 6.1 summarizes some key values from the terminal fault simulation. Some of the parameter notations have not been previously explained or used. t_2–t_4 is the time available for VI contact separation (ref. Table 3.1), $[di_{\text{VI}}/dt]_{t_4}$ is the i_{VI} slope at its zero-crossing (t_4), RRTIV is short for the positive RRTIV, and $\hat{V}_{\text{MOV},t<t_4}$ is the maximum magnitude reached by v_{MOV} during the switching operation of the VSC ($t < t_4$). All values are absolute values.

Table 6.1: Key parameter values from case 1: Interrupting a terminal fault.

$\hat{I}_{\text{line}}$ [A]	1997	t_2–t_4 [ms]	1.50	RRITIV [kV/μs]	0.92	$\hat{V}_{\text{MOV},t<t_4}$ [kV]	9.8
t_{tot} [ms]	21.3	$\left[\frac{di_{\text{VI}}}{dt}\right]_{t_4}$ [A/μs]	16.7	RRTIV [kV/μs]	0.62	$\hat{V}_{\text{MOV}}$ [kV]	17.0
N [-]	17	ITIV [kV]	1.24	$\hat{V}_{\text{VI}}$ [kV]	18.1	E_{MOV} [kJ]	237

6.2 Case 2: Interrupting Nominal Load Current

The simulation of interruption of $I_{i,\text{min}} = I_{\text{nom}} = 1$ kA was performed using the same timing aspects as shown in Figure 6.2, except that no fault occurs at $t = 0$. The resulting i_{line}, i_{VSC}, and i_{MOV} waveforms are shown in Figure 6.6. The breaker is, as seen, able to interrupt nominal load current successfully. The total operation time is measured to 8.9 ms.

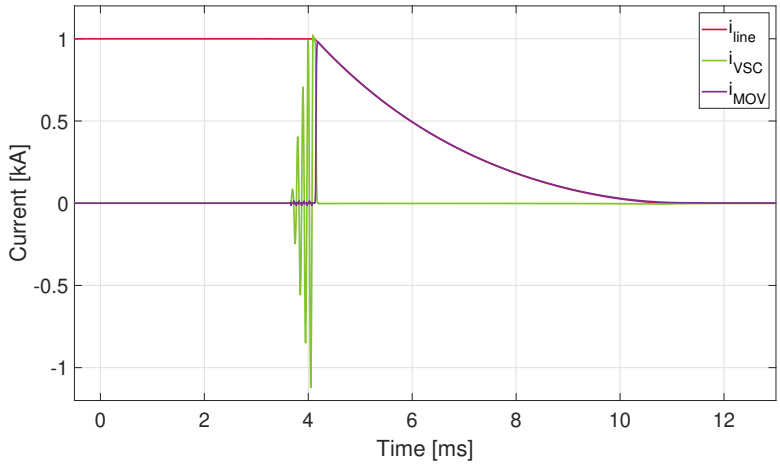


Figure 6.6: Line, VSC, and MOV currents during interruption of nominal load current.

Figure 6.7 is an equivalent to Figure 6.3 presented for case 1. In total 9 switching operations are, as seen, performed before $i_{\text{VI}} = 0$ is obtained.

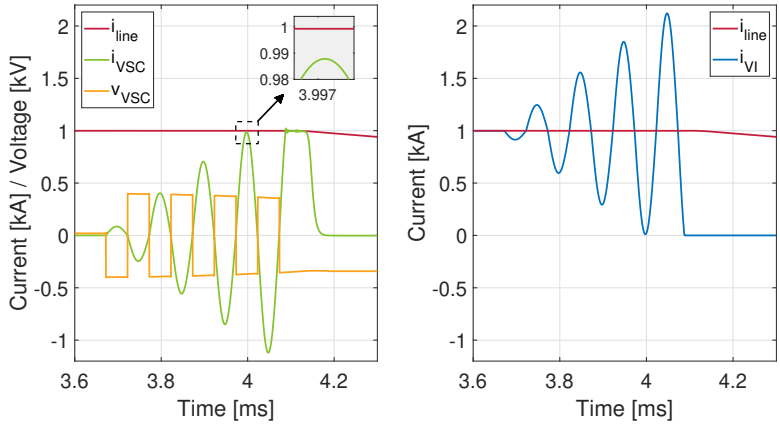


Figure 6.7: Nominal load current interruption. Left: Line current, VSC current, and VSC voltage. Right: Line and VI currents.

As discussed in Subsection 4.3.4.1 and indicated by Equation (4.24), the VSC triggering instant must be designed based on the interruption of I_{min}, in order to always ensure sufficient time for VI contact separation. This is because the VSC operation time is at its shortest when the VARC-CB interrupts I_{min}. In Figure 6.7, the zero-crossing of i_{VI} occurs at t = 4.09 ms, which is 1.09 ms after the initial contact separation in the VI. Consequently, the VI is provided 1.09 ms for opening its contacts, which is more than t_{open} = 1 ms. As the VI is provided sufficient opening time in this I_{min} interruption case, the VI will have enough time to fully open in all other interruption cases as well. This was the aim when using the criterion in Equation (4.24) in the design process.

Figure 6.8 is an equivalent to Figure 6.4 for case 1. The magnitude of di_{VI}/dt at the VI current zero is measured to 48.2 A/μs, which is well below the di/dt capability of the VI. The magnitudes of the ITIV, the RRITIV, and the positive RRTIV are measured to 5.81 kV, 4.1 kV/μs, and 0.24 kV/μs, respectively. The dv/dt capability of the VI is thus not violated. The peak value reached by v_{VI} is measured to 15.5 kV.

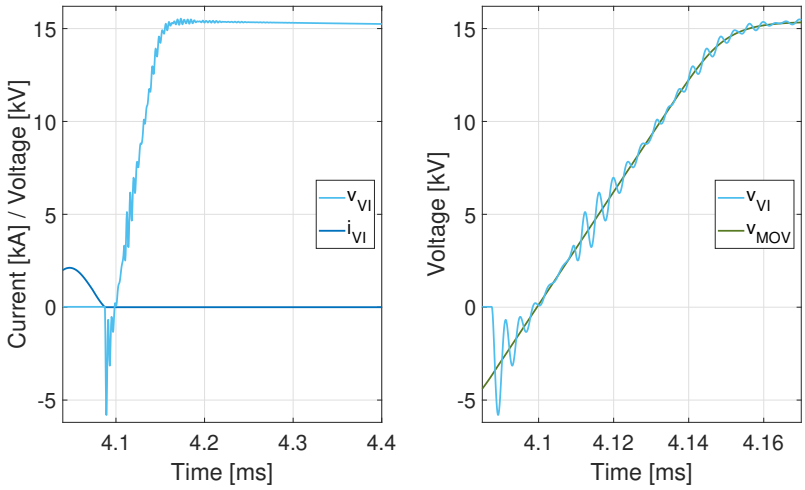


Figure 6.8: Nominal load current interruption. Left: VI voltage and current. Right: VI and MOV voltages.

In contrast to in case 1, C_{x2} and the passive DC line components are now not short-circuited, hence they impact the transient response in v_{VI}. Their presence results in the oscillatory, transient response being a superposition of multiple different frequencies, as seen in Figure 6.8, which was explained and discussed in the second paragraph of Subsection 4.3.4.3. The oscillations are quite quickly damped out, which is mainly due to the line resistance now being present, i.e. not short-circuited. However, similar to case 1, it is reasonable to assume that the damping would have been even greater, if the frequency-dependence of resistances was included in the modeling.

Plots for case 2 equivalent to Figure 6.5 for case 1 are not included, but the measured values of $\hat{V}_{\text{MOV},t<t_4}$, $\hat{V}_{\text{MOV}}$, and E_{MOV} are all included in Table 6.2. This table summarizes some key values measured in case 2, the same values as for case 1 in Table 6.1. All values are absolute values.

Table 6.2: Key parameter values from case 2: Interrupting nominal load current.

$\hat{I}_{\text{line}}$ [A]	1000	t_2–t_4 [ms]	1.09	RRITIV [kV/μs]	4.1	$\hat{V}_{\text{MOV},t<t_4}$ [kV]	6.1
t_{tot} [ms]	8.9	$\left[\frac{di_{\text{VI}}}{dt}\right]_{t_4}$ [A/μs]	48.2	RRTIV [kV/μs]	0.24	$\hat{V}_{\text{MOV}}$ [kV]	15.4
N [-]	9	ITIV [kV]	5.81	$\hat{V}_{\text{VI}}$ [kV]	15.5	E_{MOV} [kJ]	31.5

6.3 Case 3: Interrupting Reverse Fault Current

The simulation of interruption of reverse fault current was performed by changing polarity of the two voltage sources present in the simulation model, i.e. the MVDC power source and the controlled voltage source in the VI model. A simulation of a terminal fault was run, for being able to compare the results directly with the ones for case 1. Similar timing aspects as shown in Figure 6.2 were used. The resulting i_{line}, i_{VSC}, and i_{MOV} waveforms are shown in Figure 6.9. The breaker is, as seen, capable of interrupting a reverse terminal fault successfully. The behavior is very similar to that seen for the forward terminal fault case in Figure 6.1 (just upside down). This underlines the bidirectional nature of the breaker topology. The total operation time is measured to 21.4 ms.

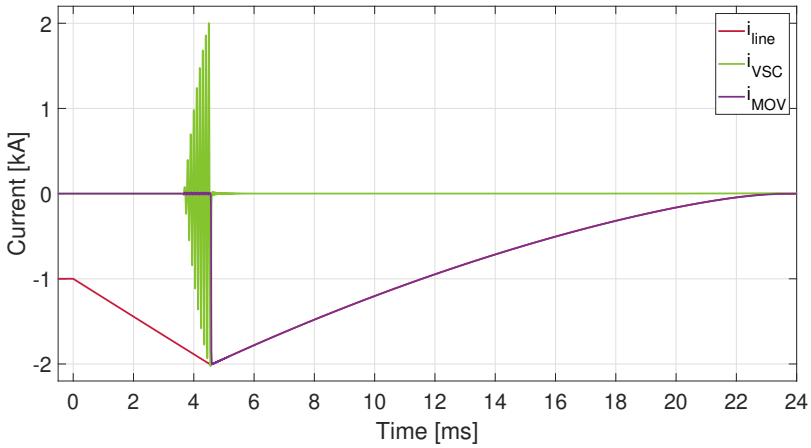


Figure 6.9: Line, VSC, and MOV currents during a terminal fault with reverse fault current.

Figure 6.10 is an equivalent to Figure 6.3 for case 1. 18 switching operations are, as seen, needed before $i_{\mathrm{VI}} = 0$ is obtained. $i_{\mathrm{VI}} = 0$ occurs at $t = 4.55$ ms. The VI is thus provided 1.55 ms for opening its contacts, which is more than $t_{\mathrm{open}} = 1$ ms, as desired.

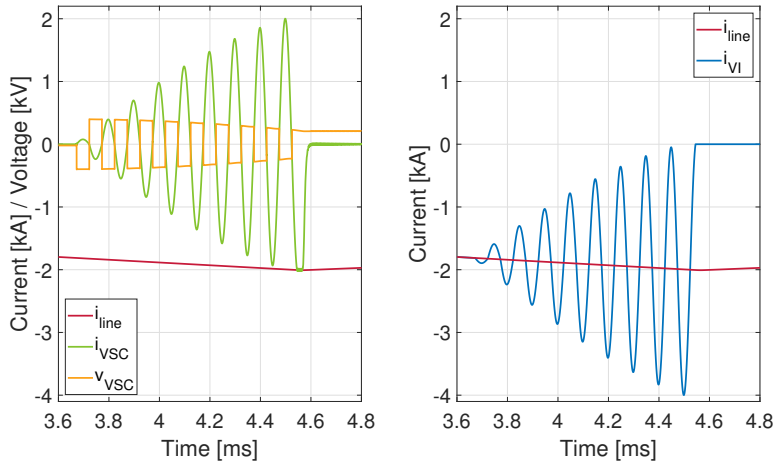


Figure 6.10: Terminal fault with reverse fault current. Left: Line current, VSC current, and VSC voltage. Right: Line and VI currents.

Figure 6.11 is an equivalent to Figure 6.4 for case 1. The interruption conditions of the VI are within the VI's di/dt- and dv/dt limits, with $[di_{\mathrm{VI}}/dt]_{t_4} = 33.5$ A/μs, ITIV = 3.60 kV, RRITIV = 2.3 kV/μs, and RRTIV = 0.61 kV/μs. The peak magnitude reached by v_{VI} is measured to 19.2 kV.

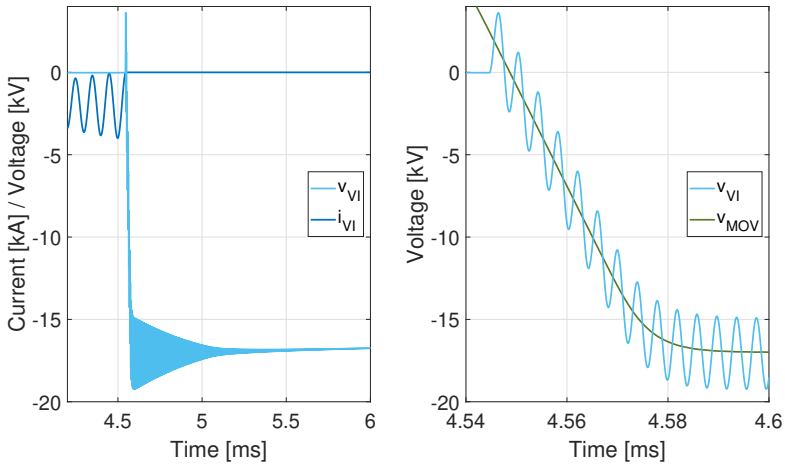


Figure 6.11: Terminal fault with reverse fault current. Left: VI voltage and current. Right: VI and MOV voltages.

Since a terminal SC fault is simulated, one frequency dominates the transient, oscillatory response in v_{VI} in Figure 6.11, just as in case 1. This frequency is measured to ca. 255 kHz, which corresponds to the one calculated by means of Equation (4.35).

Plots equivalent to Figure 6.5 for case 1 are not included for case 3, but the measured values of $\hat{V}_{\text{MOV},t<t_4}$, $\hat{V}_{\text{MOV}}$, and E_{MOV} are all included in Table 6.3. This table summarizes some key values for simulation case 3, the same values as for case 1 in Table 6.1 and case 2 in Table 6.2. All values are absolute values.

Table 6.3: Key parameter values from case 3: Interrupting reverse fault current.

$\hat{I}_{\text{line}}$ [A]	2008	t_2–t_4 [ms]	1.55	RRITIV [kV/μs]	2.3	$\hat{V}_{\text{MOV},t<t_4}$ [kV]	10.0
t_{tot} [ms]	21.4	$\left[\frac{di_{\text{VI}}}{dt}\right]_{t_4}$ [A/μs]	33.5	RRTIV [kV/μs]	0.61	$\hat{V}_{\text{MOV}}$ [kV]	17.0
N [-]	18	ITIV [kV]	3.60	$\hat{V}_{\text{VI}}$ [kV]	19.2	E_{MOV} [kJ]	239

6.4 Discussion

The simulation results presented so far have demonstrated that the simulation model developed behaves as expected, with a breaker performance in accordance with the developed design strategies. In this section, the simulation results from the three cases are compared and discussed in more detail, highlighting and explaining noteworthy differences between some key parameter values. Furthermore, some particularities of design Equations (4.12)–(4.13) are discussed. In addition, two possible improvements in the MVDC VARC-CB design are proposed. Finally, some comments are made regarding the chosen system modeling with respect to the validity of the obtained RRITIV values and of the presented RRITIV analysis.

6.4.1 Comparison of Results from the Three Simulation Cases

Some noticeable differences can be observed between the values for case 2 in Table 6.2 on the one hand, and the values for cases 1 and 3 in Tables 6.1 and 6.3, respectively, on the other. The number of switching operations required in case 2, N, is half the number needed in the other two cases. This is expected, as the current interrupted in case 2 is half of that interrupted in cases 1 and 3. Due to fewer switching operations being performed in case 2, a lower C_p voltage amplitude is accumulated during the VSC operation. This explains the considerably lower $\hat{V}_{\text{MOV},t<t_4}$ value in case 2. t_{tot} and E_{MOV} are also significantly smaller in the second case. The smaller E_{MOV} value is caused by the lower current level being interrupted (ref. Equation (2.3)). As the MOV module dissipates a lower amount of energy, the MOV operation is faster. Also the VSC operation is more rapid in case 2, due to the lower current level to be interrupted. The faster VSC and MOV operations are what give the faster overall operation time in case 2.

Furthermore, both $\hat{V}_{\text{MOV}}$ and $\hat{V}_{\text{VI}}$ attain notably lower values in case 2 than in the other two cases. In cases 1 and 3, $\hat{V}_{\text{MOV}}$ is measured to 17.0 kV, which corresponds to V_{clamp} + $R_{\text{MOV}} I_{i,\text{max}}$. In case 2, on the other hand, the $\hat{V}_{\text{MOV}}$ value is 15.4 kV. First, this is caused by the clamping voltage of the designed MOV module being 15 kV at 2 kA, hence the voltage at $I_{i,\text{min}}$ = 1 kA will be slightly lower. Second, the maximum current flowing through the MOV module in case 2 is around 1 kA, giving a voltage contribution from R_{MOV} of 1 kV, which is lower than the 2 kV obtained in cases 1 and 3. Due to the lower maximum MOV voltage, and also due to the higher damping of the v_{VI} oscillations, the peak value reached by v_{VI} is also lower in case 2.

Some noteworthy differences can also be observed between the values of case 1 and of case 2, and between the values of case 1 and of case 3. Subsection 6.4.1.1 highlights and discusses the former, while Subsection 6.4.1.2 goes into details on the latter.

6.4.1.1 VI Interruption Conditions in Case 1 and in Case 2

An interesting observation in Figure 6.7, is that the interruption of $I_{i,\text{min}}$ in case 2 corresponds to the worst-case scenario presented in Figure 4.2, which was used several times when deriving design strategies in Chapter 4. In this scenario, the positive peak resulting from the third to last VSC switching operation is very close to, but does not reach the level of the line current. This is displayed in the small gray box in the left plot in Figure 6.7. This can also be seen in the right plot, by the last negative peak of i_{VI} almost reaching zero. However, as i_{VI} does not hit zero, two additional switching operations are needed before the current interruption in the VI can occur.

As discussed when deriving design equations in Chapter 4, the scenario in Figure 4.2 is a worst-case situation for the i_{VI} slope at current zero, and for the ITIV and its rising rate. All these values also depend on the line current being interrupted, however for a certain interruption current value, the situation in Figure 4.2 is the worst-case.

The slope of i_{VI} at its zero-crossing is measured to 48.2 A/μs in case 2. This value is significantly lower than the VI's di/dt capability, but is almost three times higher than the 16.7 A/μs obtained in case 1. The main reason thereof, is the difference in the interruption instant during the last i_{VSC} pulse, indicated by θ_i in Figure 4.2. In case 1, the last i_{VSC} pulse is very close to its peak when i_{VI} = 0 is obtained. As a result, θ_i is close to 90°, giving a low di/dt value according to Equation (4.27). In case 2, on the other hand, θ_i is significantly lower, due to the case being similar to that in Figure 4.2. More specifically, θ_i is measured to 53° in case 2, and to 84° in case 1. This is the main reason behind the steeper slope of i_{VI} at its zero-crossing in case 2.

The ITIV magnitude is measured to 5.81 kV in case 2, which is significantly higher than the 1.24 kV obtained in case 1. Similar to the i_{VI} slope, this is caused by the difference in θ_i between the two cases. A lower θ_i gives a higher v_{C_p} magnitude at the moment of VI current interruption, hence a higher ITIV magnitude (ref. Equation (4.36)).

Also the RRITIV magnitude is considerably higher in case 2. RRITIV is measured to 4.1 kV/μs in case 2, which is almost five times higher than the 0.92 kV/μs measured in case 1. Consequently, even though the total capacitance and resistance present to limit the RRITIV is at minimum in case 1 (terminal fault), the ITIV attains a steeper slope in case 2. This is due to the larger ITIV magnitude, resulting from the lower θ_i.

6.4.1.2 Number of Switching Operations in Case 1 and in Case 3

One thing to notice when comparing the results from case 1 and case 3, is the difference in the total number of switching operations required before i_{VSC} reaches the level of the line current. In both cases, a terminal fault is simulated, resulting in equal line current rising rates in the two situations. However, one additional switching operation is required in case 3 (the reverse case) compared to case 1 (the forward case).

The reason for this difference can be explained by considering Figure 6.12. The figure includes the line and VSC currents obtained in the two simulation cases, the forward (fwd) and the reverse (rev). As seen, the two VSC currents follow each other until the first point where their magnitudes reach the line current level. This happens at $t = 4.50$ ms, which is during a positive i_{VSC} pulse, hence the VI current in the forward case is interrupted. However, as a negative i_{VSC} pulse is needed for being able to obtain $i_{\text{VSC}}(\text{rev}) = i_{\text{line}}(\text{rev})$, the VI current in the reverse case is not interrupted at this time instant. The required negative pulse is generated after one additional switching operation, resulting in the VI current interruption occurring at $t = 4.55$ ms, which is half a period of the oscillating current later than in the forward case.

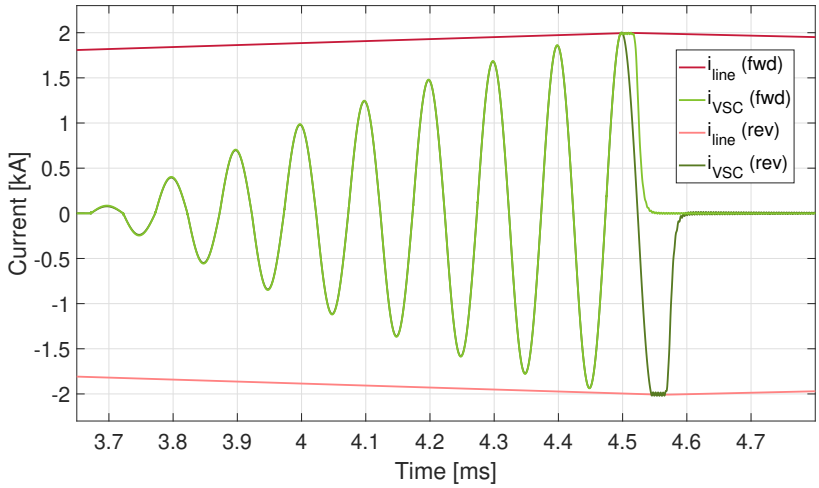


Figure 6.12: Line currents and VSC currents from case 1 (fwd) and case 3 (rev).

Due to the delayed VI interruption in case 3, some quantitative differences from the simulation results of case 1 can be observed. First, the value of $\hat{I}_{\text{line}}$ is somewhat higher than in case 1. $\hat{I}_{\text{line}}$ is 2008 A in case 3, hence slightly exceeding $I_{i,\text{max}} = 2$ kA, whereas the measured value in case 1 is 1997 A. Second, the total operation time increases from 21.3 ms in case 1 to 21.4 ms in case 3, the MOV energy absorption increases from 237 kJ to 239 kJ, and the maximum MOV voltage magnitude prior to the VI current zero increases from 9.8 kV to 10.0 kV. Third, the interruption conditions for the VI are less favorable in case 3, with an i_{VI} slope of 33.5 A/μs at current zero, and an ITIV of 3.60 kV with rising rate 2.3 kV/μs. These values are all higher than the corresponding magnitudes from case

1, which are 16.7 A/μs, 1.24 kV, and 0.92 kV/μs, respectively. Also the maximum v_{VI} peak magnitude increases from case 1 to the case 3, from 18.1 kV to 19.2 kV.

With the exception of $\hat{I}_{\text{line}}$, none of the values measured in case 3 violate any limitations of the breaker, and they are all in accordance with the derived design constraints. $\hat{I}_{\text{line}}$, on the other hand, slightly exceeds $I_{i,\text{max}}$. This can be critical, if the $I_{i,\text{max}}$ value is an absolute upper limit for the allowable grid current. If this is the case, the difference in VI interruption time instant between the forward and the reverse situations must be taken into account in the design process of the breaker. This can be done for example by designing the value of L_{lim} according to the terminal fault, either the forward or the reverse, giving the highest $\hat{I}_{\text{line}}$ value.

The quantitative differences between the forward and the reverse situations are due to the IGBT switching scheme being identical in the two cases, and can be eliminated, if making the IGBT gate signals in the two cases opposite to each other. In both cases, (S_3, S_4) is the first switch pair to be turned on at the moment of VSC triggering, causing the positive first i_{VSC} pulse seen in Figure 6.12. However, if (S_1, S_2) instead is the first pair turning on in the reverse case, a negative first pulse results, and $i_{\text{VSC}}(\text{rev})$ will become a mirror of $i_{\text{VSC}}(\text{fwd})$. This behavior is shown in Figure 6.13, where it is seen that the VI interruption instant now is the same in the two cases. Consequently, there are no quantitative differences between the simulation results (except the sign of the measured values).

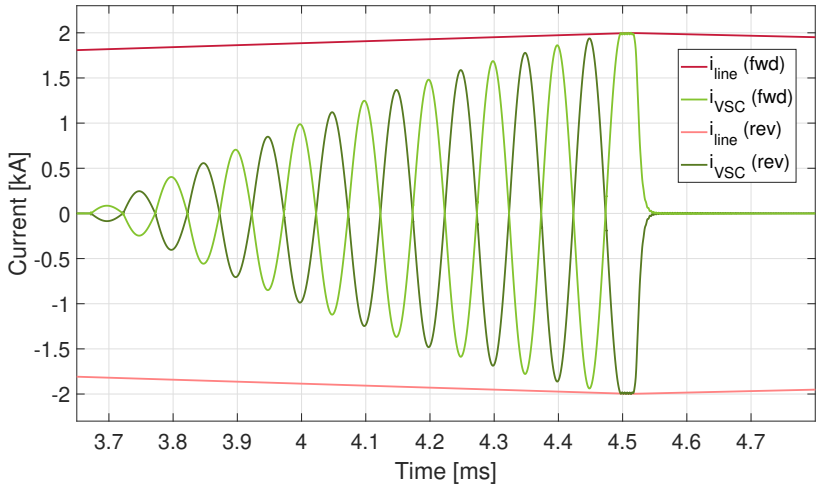


Figure 6.13: Line currents and VSC currents from case 1 (fwd) and case 3 (rev), with the case 3 simulation now using opposite gate signals compared to case 1.

In a real application, the slight change in switching scheme between forward and reverse current interruption cases can be implemented through sensing and logic circuitry, selecting the first switch pair to be turned on based on sensing of the current direction through the breaker. In this way, there will be no qualitative nor quantitative differences between a forward current interruption case and the corresponding reverse case.

6.4.2 Estimated vs. Simulated v_{DC} and i_{VSC} Dynamics

As a part of developing design strategies for the VARC-CB module in Chapter 4, Equations (4.12)–(4.13) describing the dynamics of v_{DC} and i_{VSC} were derived in Subsection 4.3.2.3. By using these, the trajectories of v_{DC} and $\hat{i}_{\mathrm{VSC}}$ can be predicted. In particular, the equations were used in the parameterization process in Chapter 5, to ensure that the designed breaker module would be capable of achieving a maximum oscillating current amplitude of at least $K \cdot I_{i,\max} = 2.2$ kA. Figure 6.14 shows a comparison of the v_{DC} and $\hat{i}_{\mathrm{VSC}}$ trajectories predicted by means of Equations (4.12)–(4.13), and the actual curves obtained by simulations. The simulated curves were obtained by running a simulation with a line current too high for the breaker to interrupt.

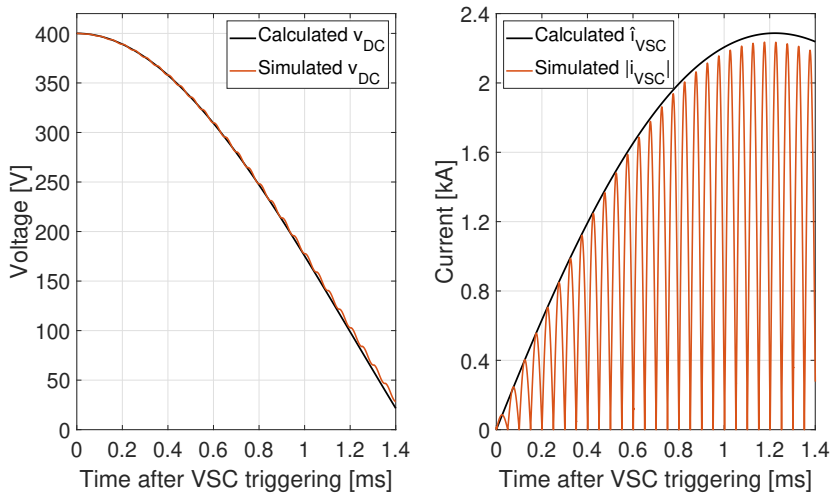


Figure 6.14: Left: Calculated and simulated trajectories for v_{DC}. Right: Calculated trajectory for $\hat{i}_{\mathrm{VSC}}$, and simulated waveform of $|i_{\mathrm{VSC}}|$.

The calculated trajectory of v_{DC} agrees very well with the one obtained from the simulation, as seen in the left plot in Figure 6.14. Both curves start from 400 V, which indicates C_{DC} being fully charged to V_{DC} before the VSC begins to operate. Due to the energy transfer from C_{DC} during the VSC operation, v_{DC} decreases with time. The simulated decrease follows the calculated trajectory, however with a slight oscillatory behavior. This is caused by the oscillations in the VSC current, which were not accounted for when using the VSC current envelope to derive Equation (4.12). Overall, however, it can be concluded that the predicted v_{DC} trajectory models the actual behavior of v_{DC} with high accuracy, hence validating the derivation of the v_{DC} dynamics performed in Subsection 4.3.2.3.

The calculated trajectory of the positive $\hat{i}_{\mathrm{VSC}}$ envelope also coincides well with the simulation results, however a slight deviation is seen in the right plot in Figure 6.14. As time passes, the envelope deviates slightly from the measured peaks of i_{VSC}, with the envelope giving an overestimate of the peak values. A reason thereof, may be that not all loss contributions were accounted for when deriving the loss term of $\hat{i}_{\mathrm{VSC}}$ in Equation

(4.9). The Q-factor used to derive this equation only includes the loss contribution from R_p. Other losses in the i_{VSC} loop, such as the conduction losses in S_1–S_4 and the energy losses in the VI arc, were neglected. The loss term, which retards the growth in $\hat{i}_{\text{VSC}}$, is thus, in reality, greater than what the predicted trajectory in Figure 6.14 indicates. It is evident that the R_p loss contribution is the one dominating, as the predicted and simulated values fit relatively well, however it is reasonable to assume that the fit can be improved if also the other loss contributions are taken into account.

A consequence of neglecting the mentioned loss contributions when deriving the $\hat{i}_{\text{VSC}}$ dynamics, is that the actual maximum achievable oscillating current amplitude is somewhat lower than the one estimated by Equations (4.12)–(4.13). The peak value reached by the estimated $\hat{i}_{\text{VSC}}$ trajectory in Figure 6.14 is 2287 A. The maximum value reached by the simulated waveform, however, is 2239 A. This is higher than $K \cdot I_{i,\text{max}}$, as desired, but it is 2.1% lower than the predicted value. This is a shortcoming of Equations (4.12)–(4.13) which should be paid attention to in the design process, to make sure that the breaker module actually is able to reach the desirable maximum oscillating current amplitude. This can be ensured, for example, by using a higher K-value. It can, of course, also be ensured by developing more accurate equations, however this would require a more detailed analysis and estimation of the loss mechanisms retarding the $\hat{i}_{\text{VSC}}$ growth.

6.4.3 Possible Improvement: Auxiliary Passive Resonant Circuit

From the comparison of case 1 and case 2 in Subsection 6.4.1.1, it is clear that interrupting $I_{i,\text{min}}$ with the designed VARC-CB module is less favorable for the VI in terms of di/dt and dv/dt conditions, compared to when interrupting $I_{i,\text{max}}$. This is mainly due to the difference in θ_i between the two cases, which again is a result of the dependence of θ_i on the line current to be interrupted, together with the chosen parameter value of the current injection branch. Consequently, for a certain breaker design, different interruption current levels result in different interruption conditions for the VI, and interrupting a low current can be less favorable for the VI in terms of di/dt and dv/dt than interrupting a high one.

In Deliverable D6.4 of the EU-funded PROMOTioN project [81], which discusses the design of an MCB with active current injection, the authors propose implementing two separate passive resonant circuits to always ensure favorable VI conditions at $i_{\text{VI}} = 0$. They suggest that the main passive resonant circuit is dedicated to interrupt fault currents, and is designed thereafter. The other circuit, the auxiliary circuit, is used to interrupt nominal load current, and is designed specifically to provide favorable VI conditions during this interruption. The results presented indicate that the use of separate LC circuits, each specifically designed for certain interruption currents, provides better VI interruption conditions overall compared to using one single LC circuit for all interruption current levels.

As the VARC-CB and the MCB with active current injection have quite similar basic operating principles, the same approach may be suitable for the VARC-CB. When running simulations with the developed VARC-CB design and model, it is observed that no matter the location of the SC fault along the DC line, $\hat{I}_{\text{line}}$ reaches approximately 2 kA, and the VI interruption always occurs during the same i_{VSC} pulse, the 17$^{\text{th}}$. The worst VI interruption conditions during an forward SC fault in the system under consideration are obtained when simulating a fault at the load terminals. This leads to the VI interruption furthest from the

17^{th} i_{VSC} peak, hence the lowest θ_i. The resulting values for the i_{VI} slope at VI current zero and the RRITIV are 25.1 A/μs and 1.8 kV/μs, respectively. However, even for this worst SC case, the di/dt and the dv/dt conditions are well within the capabilities of the VI. This indicates that the chosen VARC-CB module design, with a passive resonant circuit of Z_{LC} = 4.85 Ω, is well-suited for providing safe VI interruption conditions during every possible SC fault case. This LC circuit can thus be used as the main one, if implementing the suggested approach from [81].

The same LC circuit design does not violate the VI capabilities when $I_{i,\text{min}} = I_{\text{nom}}$ is interrupted, but a quite high RRITIV is observed, as pointed out in Subsection 6.4.1.1. By adjusting Z_{LC} slightly, however, keeping all other parameter values the same, it is observed that more favorable dv/dt conditions easily can be obtained for case 2. To exemplify, reducing Z_{LC} to 4.7 Ω results in an RRITIV of 0.93 kV/μs, which is significantly lower than the 4.1 kV/μs obtained when using the original design with Z_{LC} = 4.85 Ω. The i_{VI} slope at VI current zero is also reduced, from 48.2 A/μs with the original Z_{LC} value, to 12.2 A/μs with the adjusted value. Relevant current and voltage waveforms from the case 2 simulation with adjusted Z_{LC} value can be found in Figure D.1 in Appendix D.

Based on the above results and discussion, it thus seems plausible that the approach suggested in [81] with benefit also can be implemented for the VARC-CB concept: if using one LC circuit designed for interrupting currents in the SC fault current range, and one designed for interrupting nominal load current, safe and favorable interruption conditions for the VI are always ensured. It should be noted, however, that this requires two extra passive components, one inductor and one capacitor, when compared to the original design.

It should also be mentioned that a fault current range resulting from only bolted SC faults has been considered in this discussion. In all the above-mentioned fault simulations, an SC fault with negligible fault resistance has been assumed. However, if also including higher-impedance faults, the fault current range will be larger. In this case, it does not make sense to separate between one LC circuit used for faults and one used for nominal current, if the aim is to ensure favorable VI conditions. To illustrate, the results from simulating a mid-point SC fault with R_f = 6.2 Ω using the original LC circuit is included in Figure 6.15 and Figure 6.16. Due to the high fault resistance, the peak reached by the line current is only 1.5 kA, and the VI interruption occurs during the 13^{th} pulse of i_{VSC}. This is a worst-case scenario in terms of VI interruption conditions, just as case 2: the peak of the second to last positive pulse is very close to reaching i_{line}, but does not, as seen in the small gray box in Figure 6.15. The resulting values for the i_{VI} slope at VI current zero and the RRITIV are 50.8 A/μs and 4.3 kV/μs, respectively. It can therefore be concluded that the approach using two LC circuit is beneficial only if the breaker is to be designed for two separate, limited interruption current ranges.

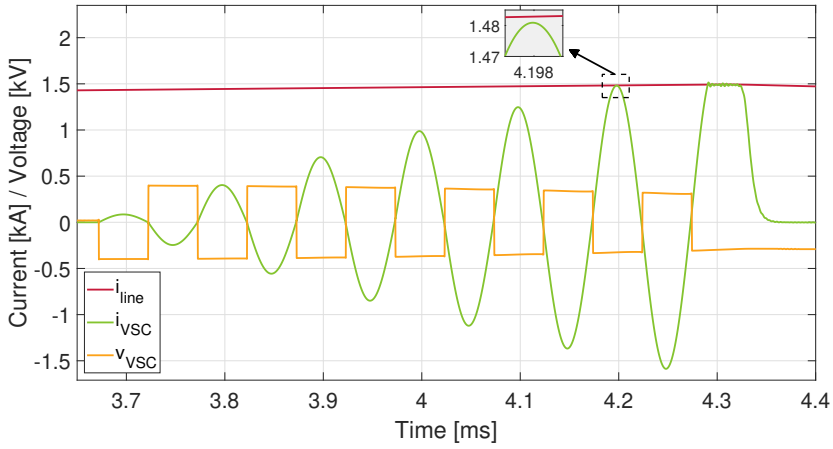


Figure 6.15: Line current, VSC current, and VSC voltage during mid-point fault with fault impedance 6.2 Ω.

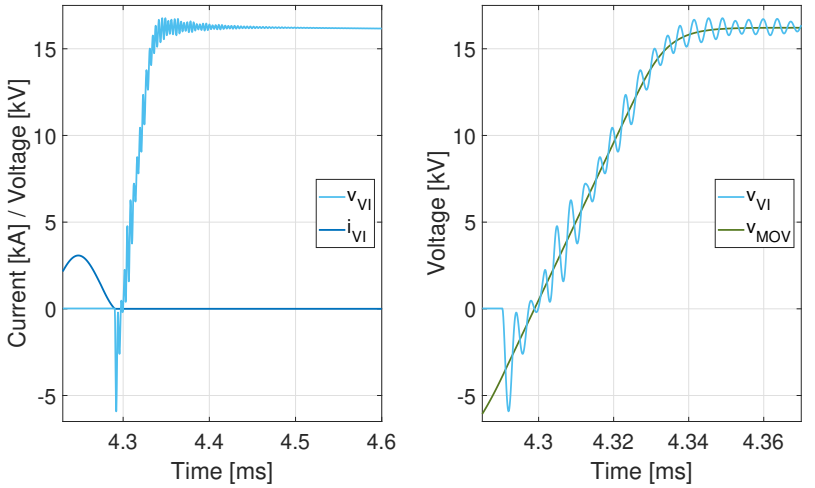


Figure 6.16: Mid-point fault with fault impedance 6.2 Ω. Left: VI voltage and VI current. Right: VI and MOV voltages.

6.4.4 Possible Improvement: Adjustment of VSC Triggering Instant

When accounting for the VI opening time in Subsection 4.3.4.1, a suggestion of using a fixed delay between the initial VI contact separation and the VSC triggering was made. Equation (4.24) was proposed as the design criterion for this delay, which was derived based on the shortest possible operation time of the VSC, which occurs when interrupting $I_{i,\text{min}}$. Using this equation for designing the delay ensures that sufficient time is provided for the VI opening, regardless the current level being interrupted. In addition, as the delay is fixed and constant, it gives a simple implementation. This section, however, investigates the possible gains by adjusting the delay according to the interruption situation, i.e. re-calculating the VSC triggering instant at every breaker operation. This requires implementing sophisticated methods and circuitry, which may increase the breaker cost and complexity, but if the gain is high, the implementation might be justifiable.

6.4.4.1 Minimizing $t_{\text{VSC,delay}}$

In an ideal case, the instant where the VSC generates a current zero-crossing in the VI is also the instant at which the VI achieves the required contact gap, as this will minimize the total operation time of the breaker. Since this involves the sum of t_{VSC} and $t_{\text{VSC,delay}}$ being exactly equal to t_{open}, the value of $t_{\text{VSC,delay}}$ must be adjusted according to the required VSC operation time in the interruption situation under consideration. More specifically, this involves the value of $t_{\text{VSC,delay}}$ always being minimized.

To illustrate how this can be done and the possible gains, case 1 will be explored as an example case. In the results from case 1 presented in Section 6.1, the time available for the VI opening is 1.50 ms. As the VI under consideration only needs 1 ms for its opening, it is clear that there is room for reducing $t_{\text{VSC,delay}}$ in this case. By using the right-hand side of Equation (4.23), with $I_{i,\text{min}}$ replaced by $I_{i,\text{max}}$, an estimation of 0.63 ms is obtained for the VSC operation time when $I_{i,\text{max}}$ is interrupted. This is, however, an underestimate, which was considered in Subsection 4.3.4.1 in order to incorporate some safety margin into the design of $t_{\text{VSC,delay}}$. A more accurate estimation can be obtained by considering the prospective $\hat{i}_{\text{VSC}}$ trajectory resulting from Equations (4.12)–(4.13), which is displayed by the black curve in the right plot in Figure 6.14. The $\hat{i}_{\text{VSC}}$ trajectory hits 2 kA after 0.805 ms, meaning that the actual VSC operation time will be around 0.805 ms in case 1. It should therefore be possible to activate the VSC at an instant $t_{\text{VSC,delay}}$ = 1−0.805 = 0.195 ms after the initial contact separation of the VI, and still provide 1 ms for the VI opening. This is a reduction of 0.48 ms compared to the $t_{\text{VSC,delay}}$ value used for providing the simulation results in Section 6.1.

Simulating a terminal fault with $t_{\text{VSC,delay}}$ = 0.195 ms results in some clear improvements in the breaker performance compared to what is presented in Section 6.1. First, it is possible to reduce the value of L_{lim} by 4.8 mH, corresponding to an 11% reduction, still obtaining a $\hat{I}_{\text{line}}$ value just below $I_{i,\text{max}}$. Second, the total operation time is reduced by 12%, from 21.3 to 18.8 ms. Third, the energy absorbed by the MOV decreases from 237 to 212 kJ, giving a reduction of 11%.

In the simulation with the reduced $t_{\text{VSC,delay}}$ value, the VI current zero occurs at t = 4.02 ms, hence providing 1.02 ms for the contact separation in the VI. This shows that $t_{\text{VSC,delay}}$ has been minimized, but still satisfies the requirement of t_{open} = 1 ms. However,

it should be pointed out that the safety margin in this case is small. A small measurement error, for example in the detection of the initial VI contact separation, or in the estimation of the line current trajectory, may then result in $i_{\mathrm{VI}} = 0$ being generated before the VI has reached sufficient voltage withstand capability. To incorporate some more safety margin, the underestimate of the VSC operation time obtained from the right-hand side of Equation (4.23) can be used instead of the more accurate one based on Equations (4.12)–(4.13). This will, however, reduce the improvements obtained, as $t_{\mathrm{VSC,delay}}$ is increased.

6.4.4.2 Ensuring Favorable VI Interruption Conditions

The aim of adjusting the VSC triggering instant in the previous subsection was to minimize $t_{\mathrm{VSC,delay}}$. The objective presented here, on the other hand, is to obtain favorable interruption conditions for the VI. More specifically, the aim is to adjust the triggering of the VSC in order to control θ_i. It should be noted that this is only possible in fault interruption cases, not in constant load current interruption cases, as θ_i will be the same irrespective of the $t_{\mathrm{VSC,delay}}$ value when interrupting constant currents.

As indicated by the right plot in Figure 6.14, a relatively accurate estimation of the envelope of i_{VSC} can be obtained. Since the envelope and the resonant frequency will be constant for a certain set of parameter values, it is possible to estimate the values of the i_{VSC} peaks, and the time instants at which they occur. This is shown for the original breaker design in Figure 6.17. The black curve is similar to the one in the right plot of Figure 6.14, i.e. the i_{VSC} envelope calculated by means of Equations (4.12)–(4.13). By using the resonant frequency, $f_{\mathrm{LC}} = 10$ kHz, the points at which the estimated i_{VSC} reaches its positive (green) and negative (blue) peaks have been marked. The figure also includes the i_{VSC} waveform from Figure 6.14, to show how well the peaks can be predicted.

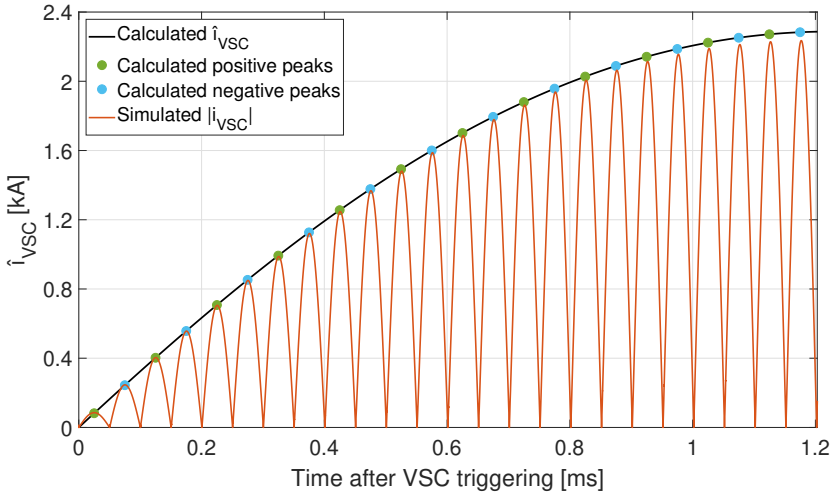


Figure 6.17: Black: Calculated trajectory for $\hat{i}_{\mathrm{VSC}}$. Dots: Estimated peaks of i_{VSC}. Orange: Simulated $|i_{\mathrm{VSC}}|$ waveform.

Under the assumption of a relatively linear increase in the line current during a fault, the line current trajectory can also be estimated quite accurately, if its value and slope are measured. By combining the estimated line current trajectory with the estimated i_{VSC} peak values and instants w.r.t. the VSC triggering, it should be possible to calculate a value for $t_{\text{VSC,delay}}$ which ensures that i_{VSC} and i_{line} intersects very close to a i_{VSC} peak, i.e. which ensures a θ_i close to 90°.

By using such a method, the situation displayed in the gray box in the Figure 6.15 can be avoided. As seen in the figure, a VI current zero is very close to being generated at the 6$^{\text{th}}$ positive peak of i_{VSC}, but as the peak value is just short of the line current level at this point, two additional switching operations are needed before $i_{\text{VI}} = 0$ is generated. However, if the VSC had been triggered at a slightly earlier time instant, the level of i_{line} during the 6$^{\text{th}}$ positive i_{VSC} pulse would had been lower, resulting in $i_{\text{VI}} = 0$ occurring at, or at least very close to, the the peak of i_{VSC} during this pulse. More specifically, by decreasing $t_{\text{VSC,delay}}$ by only 14.4 μs compared to the value used when obtaining the results in Figure 6.15, the results presented in Figure 6.18 and Figure 6.19 are obtained. Here, the VI interruption occurs during the 6$^{\text{th}}$ positive pulse of i_{VSC}, and it happens so close to the i_{VSC} peak, that almost no ITIV is generated. The measured ITIV value is around 60 V, and the RRITIV is 0.13 kV/μs. The i_{VI} slope at the zero-crossing is also negligibly small, with a value of 3.2 A/μs. The resulting interruption conditions for the VI in terms of di/dt and dv/dt are, as seen, very favorable.

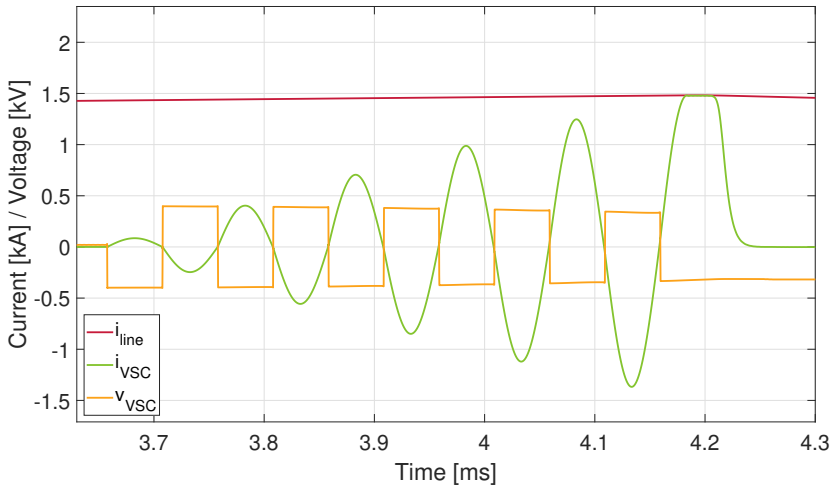


Figure 6.18: Results from simulation with adjusted $t_{\text{VSC,delay}}$, simulating a mid-point fault with fault impedance 6.2 Ω: Line current, VSC current, and VSC voltage.

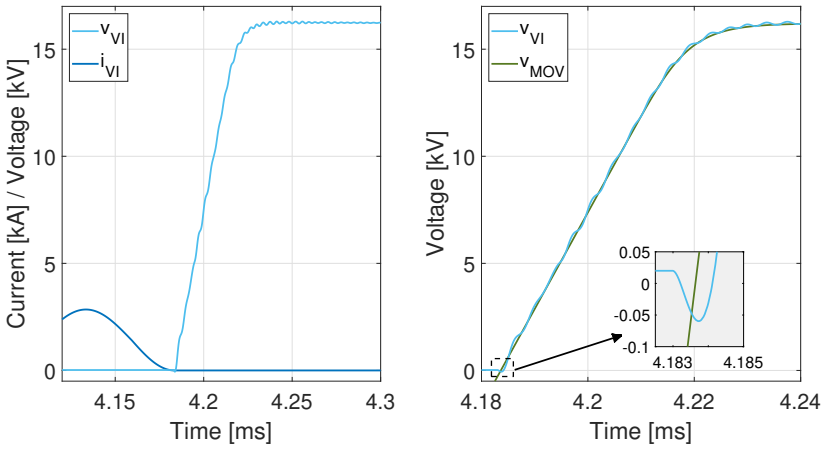


Figure 6.19: Results from simulation with adjusted $t_{\text{VSC,delay}}$, simulating a mid-point fault with fault impedance $6.2\ \Omega$. Left: VI voltage and VI current. Right: VI and MOV voltages.

The possibility of controlling the di/dt- and dv/dt conditions for the VI at its interruption through adjustments of $t_{\text{VSC,delay}}$ opens up new possibilities in the design and parameterization process of the VARC-CB module. As θ_i can be controlled, the constraints imposed by the limited di/dt- and dv/dt capabilities of the VI on the VARC-CB design are loosened. Consequently, it is easier to obtain a VARC-CB parameter design not violating any component limitations. This is especially true for the dv/dt considerations. The design criterion in Equation 4.34, resulting from the restricted di/dt capability of the VI, did not impose strict limitations on the VARC-CB parameterization. The constraints imposed by the restricted dv/dt capability of the VI through Equation (4.40), on the other hand, were more challenging. In particular, the restricted dv/dt capability was a limiting factor in the choice of switching frequency, as discussed in Subsection 5.8.1. In addition, a VI with high dv/dt capability had to be assumed in Subsection 5.8.4 in order to find a Z_{LC} value not violating any design constraints. By using the suggested method of $t_{\text{VSC,delay}}$ adjustment, however, these restrictions are loosened up, giving a wider range of possible values for the parameterization of the VARC-CB design.

As a concluding remark, it should be noted that the details around the actual implementation of a method like the one described have not been examined. More work is therefore required in order to decide whether the method is feasible, and how to realize the method in a real-life application must be investigated.

6.4.5 System Modeling and RRITIV Considerations

The limited dv/dt capability of the VI has been pointed out as a challenging restriction in the VARC-CB module design and parameterization. In particular, the RRITIV can, as seen in the simulation results presented in this chapter, become high, and care must be taken to obtain a breaker design which ensures a safe RRITIV in all interruption cases. It is, however, important to note that the TIV and the RRITIV values are highly affected by

the system configuration surrounding the VARC-CB module, as highlighted in Subsection 4.3.4.3. Just as for the TRV of ACCBs in AC systems, various network configurations will give large variations of the course of the TIV of the VARC-CB. It is therefore essential to discuss the the chosen system modeling, and its influence on the RRITIV results obtained.

As already pointed out in Section 6.1, no frequency-dependence was included in the simulation model. According to the previously mentioned IEEE Standard C37.011, detailed modeling of the connected line/cable and the circuit components nearest an ACCB is important, in order to obtain TRV calculations of adequate accuracy [39]. In particular, circuit constants at the TRV frequencies should be supplied for all the components present in the system in which an ACCB is connected. This means that for all the components in the MVDC system where the VARC-CB module is located, and for the components within the breaker module, the effective inductances, capacitances, and resistances at the frequencies of the TIV are needed, in order to determine the TIV accurately. In addition, the line/cable should be represented by a frequency-dependent, distributed parameter model, which preferably should include the complete conductor geometry [39]. In the simulation model used for simulating the VARC-CB module, these mentioned aspects were not accounted for. A constant-parameter model was used, and the DC line was modeled using a lumped-parameter pi-model. As mentioned in Subsection 5.3.3, a high number of pi-line segments was used in order to approach the more accurate distributed modeling. Nevertheless, the model was not frequency-dependent. Neglecting the frequency-dependence of the line and other circuit components typically leads to conservative results [39], indicating that it is reasonable to assume that the RRITIV values measured in the performed simulations are higher than what would have been the case in a real-life system. Obtaining more accurate results thus require more detailed, frequency-dependent modeling of the line and the circuit components in the test system.

In the proposed test system in Figure 4.1, the two capacitors C_{x1} and C_{x2} were included to represent the stray capacitance of equipment in the near vicinity of the VARC-CB module. A qualified choice of their capacitance values were made based on the values given in Annex B of the IEEE Standard C37.011, resulting in C_{x1} = C_{x2} = 5 nF. It is, however, observed that small changes in these values result in quite significant changes in the simulated RRITIV. To exemplify, when increasing both capacitance values to 10 nF, which still is reasonable according to the IEEE standard, the RRITIV obtained in case 2 is reduced from 4.1 kV/μs to 3.0 kV/μs. Simulating with C_{x1} = C_{x2} = 2 nF results in an increase to 6.4 kV/μs for the same case. These results indicate that a more detailed investigation of the stray capacitance surrounding the VARC-CB module should be performed, in order to obtain realistic and accurate RRITIV simulation values.

It is not only the values of C_{x1} and C_{x2} which are of importance for the RRITIV, but also their location in the simulation model. According to the IEEE Standard C37.011, the total equivalent stray capacitance of all equipment connected to each side of an ACCB can be modelled as two lumped capacitors, one on each side of the breaker. This was implemented in the simulated model, with C_{x1} placed on the source side, and C_{x2} placed on the load side of the VARC-CB module. The location of C_{x1} with respect to L_{lim}, can, however, be discussed.

Where C_{x1} should be located in the simulation model, depends on how L_{lim} is connected to the rest of the VARC-CB module [39]. If L_{lim} is installed immediately in series with the CB, it may be reasonable to separate C_{x1} into two, one on each side of L_{lim}. In this case, the one to the right of L_{lim} models the sum of the inherent stray capacitances of L_{lim} and of the cable connecting L_{lim} and the CB, while the one to the left models the total stray capacitance of the equipment connected on the source side of L_{lim}. If this is the case, the capacitance between L_{lim} and the rest of the VARC-CB module will typically be low, due to the low inherent capacitance of L_{lim}, and possibly low capacitance of the cable connecting L_{lim} and the CB module. This will result in the transient TIV oscillations containing very high frequencies [39], giving high RRITIV values. To exemplify, simulating case 2 with $0.8C_{x1}$ placed on the left side, and $0.2C_{x1}$ placed on the right side of L_{lim}, gives an RRITIV of 9.2 kV/μs. This is more than twice the 4.1 kV/μs obtained when having all capacitance of C_{x1} on the right side of L_{lim}. It is therefore clear that the chosen location of C_{x1} in the simulation model highly impacts the obtained RRITIV values.

The previous paragraphs suggest that the validity of the RRITIV simulation results presented can be questioned, and in order to obtain more accurate RRITIV values, a more comprehensive and realistic system modeling is needed. This indicates that also the RRITIV analysis presented in Subsection 4.3.4.3 should be revised. In particular, revised RRITIV-related design constraints should be derived, as these highly depend on the network configuration under consideration. More work on examining factors influencing the RRITIV conditions of the VI is thus needed, both for developing more accurate design constraints, and for obtaining more realistic simulation results.

As a concluding comment, it should be highlighted that although the location and values chosen for C_{x1} and C_{x2} may not be fully precise, it was of high importance to have them included in the analytical investigation and the simulation model of the VARC-CB. Removing them from the considered system results in the RRITIV being essentially determined by the stray capacitance of the VI. As this capacitance is very low, very high-frequency TIV oscillations results, giving large RRITIV values. When simulating case 2 without C_{x1} and C_{x2} in the system, one frequency is dominating the transient, oscillatory response in the TIV. The measured value of this frequency is 2.56 MHz, which corresponds to the frequency calculated by Equation (4.35) with C_{x1} removed, and with R_p replaced by the sum $R_p + R_s$. The resulting RRITIV is 41.7 kV/μs, which greatly exceeds the dv/dt capability of the VI. The voltage stress applied to the VI in this case is, however, unrealistically high. The VARC-CB will never be a stand-alone component in the network in which it is connected: other circuit components will be present in the network, having stray capacitances which contribute to a reduction of the dv/dt experienced by the VI. This underlines the importance of including the impact from C_{x1} and C_{x2} in the mathematical and Simulink modeling of the VARC-CB module. More generally, it emphasizes the importance of including stray capacitances in test circuits used for studying ACCB-based DCCBs, especially if the interruption conditions of, and the stresses on the ACCB are of interest in the study.

Chapter 7

Conclusion and Further Work

7.1 Conclusion

DC circuit breakers (DCCBs) are a key enabling technology for medium-voltage DC (MVDC) power grids, and the voltage source converter (VSC) assisted resonant current circuit breaker (VARC-CB) is a particularly interesting and promising breaker concept. This thesis has examined the MVDC VARC-CB in detail.

The MVDC VARC-CB has been analytically investigated, taking design principles and limitations into account. Based on this analysis, a complete set of design strategies to be used when designing the parameters of the breaker module has been developed. Some of the main findings and conclusions from this process are summarized in the list below.

- The opening time of the vacuum interrupter (VI) dictates the design of the delay between the initial VI contact separation and the VSC triggering instant, $t_{\text{VSC,delay}}$. The delay should be set based on the minimum possible VSC operation time (interrupting $I_{i,\text{min}}$) to ensure sufficient time for VI opening in all interruption cases.
- The limited di/dt capability of the VI results in two design constraints. First, it gives a minimum requirement for the current-limiting inductance L_{lim}. Second, it imposes a constraint involving f_{LC}, V_{DC}, Z_{LC}, and $I_{i,\text{max}}$ which is caused by the correlation between the parameter values of the current injection branch, the current to be interrupted, the interruption instant, and the VI current slope at current zero.
- The limited dv/dt capability of the VI imposes constraints on the VARC-CB module design. For accurately determining the VI voltage after VI current zero – namely, the transient interruption voltage (TIV) – numerical calculations with a detailed system representation is required. However, through a simplified analysis, two main design constraints can be derived:
  - The rising rate of the initial TIV (RRITIV) must be lower than the rising rate of the VI's capability curve. The resulting constraint involves Z_{LC}, R_p, V_{DC}, $I_{i,\text{max}}$, the stray capacitance of the VI, and stray capacitance of other equipment in the vicinity of the VARC-CB module, all of which impacts the RRITIV.

  - The positive TIV rising rate (RRTIV) should not exceed the VI's dv/dt capability, and puts a minimum requirement on the C_p value.

- The value of the current-limiting inductance must ensure that the maximum allowable fault current, $I_{i,\text{max}}$, is not exceeded.
- The design of the DC link capacitor, with its capacitance C_{DC} and precharged voltage V_{DC}, has to ensure an initial energy in the DC link sufficient to excite the oscillating current amplitude to a level exceeding $I_{i,\text{max}}$. The maximum achievable oscillating current amplitude is also influenced by the values of f_{LC}, Z_{LC}, and R_p.
- The switching frequency of the VSC equals the resonance frequency of the passive resonant circuit. It should be high to minimize L_p and C_p, however not higher than what the VSC switches can handle.
- The characteristic impedance of the passive LC circuit, Z_{LC}, must be lower than an upper limit imposed by the metal-oxide varistor (MOV). The purpose of this constraint is to prevent the MOV clamping voltage from being reached during VSC operation. Still, Z_{LC} should be as high as possible to limit the current pulse amplitude at a potential reignition of the VI arc.

A Simulink® simulation model of the VARC-CB employed in a simplified MVDC grid has been developed and parameterized. Readily available components from the Simscape Electrical™ toolbox were used to model the grid and the VARC-CB module's subcomponents. It was, however, necessary to build a separate VI model, as no Simscape component modeling vacuum arc behavior exists. To parameterize the overall simulation model, the developed VARC-CB design principles were applied, together with data found in literature and in datasheets of relevant physical devices.

A 10 kV/1 kA MVDC grid was assumed, with a range of interruption currents of $[I_{i,\text{min}}, I_{i,\text{max}}]$ = [1 kA, 2 kA]. Some of the key parameter values of the breaker module were designed as f_{LC} = 10 kHz, Z_{LC} = 4.85 Ω, C_{DC} = 3.75 mF, V_{DC} = 400 V, V_{clamp} = 15 kV, L_{lim} = 44.5 mH, and $t_{\text{VSC,delay}}$ = 0.67 ms.

In the parameterization process, it proved difficult to find a set of parameter values giving a low worst-case RRITIV value without violating any of the derived design constraints. It was therefore necessary to assume a VI with high dv/dt capability (minimum 7 kV/μs) in order to obtain an adequate breaker design.

Validation simulations have been performed, and results from three main cases have been presented. In case 1 a terminal fault was simulated. The results proved that the VARC-CB module was able to interrupt the maximum fault current it was designed for, $I_{i,\text{max}}$ = 2 kA. The fault current was neutralized within 2.51 ms, which is in accordance with requirements found for MVDC DCCBs in literature. The total operation time was measured to 21.3 ms. Case 2 verified the breaker performance during nominal load current interruption, $I_{i,\text{nom}} = I_{i,\text{min}}$ = 1 kA. The time available for VI opening was shown to be sufficient, hence validating the design of $t_{\text{VSC,delay}}$. In case 3 a terminal fault with reverse current was simulated, and the results verified that the breaker behavior is the same irrespective of the direction of the current to be interrupted.

It was observed that case 2 yielded considerably less favorable di/dt- and dv/dt conditions for the VI than case 1. In case 1, the i_{VI} slope at its zero-crossing and the RRITIV

were 16.7 A/μs and 0.92 kV/μs, respectively. In case 2, the corresponding values were 48.2 A/μs and 4.1 kV/μs. These values are within the VI's capabilities, but are significantly higher than in case 1. This is mainly caused by $i_{\text{VI}} = 0$ being generated further from an i_{VSC} peak in case 2 (lower θ_i) compared to case 1. This made it evident that different current levels result in different di/dt- and dv/dt conditions for the VI, and a lower interruption current may result in more challenging conditions than a higher one.

From comparing cases 1 and 3, it became apparent that employing a fixed VSC switching scheme results in quantitative differences between a forward current interruption case and its corresponding reverse case. A noteworthy observation was that this resulted in $\hat{I}_{\text{line}}$ slightly exceeding $I_{i,\text{max}}$ in case 3. This suggests that the value of L_{lim} should be designed according to the terminal fault, either the forward or the reverse, giving the highest $\hat{I}_{\text{line}}$ value. As an alternative, the quantitative differences can be eliminated by making the gate signals of the VSC switches in forward and reverse cases opposite to each other.

Except for $\hat{I}_{\text{line}}$ slightly exceeding $I_{i,\text{max}}$ in case 3, none of the values measured in the three cases violated any system or component limitations. Overall, the results from the cases validate that the developed simulation model behaves as expected, with a satisfactory breaker performance in accordance with the derived design constraints and equations.

However, by comparing the i_{VSC} dynamics obtained in simulations and those estimated by equations developed, a weakness of the performed i_{VSC} analysis was noted: when deriving an expression for the i_{VSC} dynamics, only the most dominating loss contribution in the i_{VSC} loop was considered. As a result, the developed equations overestimate the maximum oscillating current amplitude that is achievable by a certain breaker design. For the developed VARC-CB design, this involved an overestimate of 2.1%. When utilizing the derived equations (Equations (4.12)–(4.13)), it must therefore be made sure that the VSC is able to excite an oscillating current of sufficient maximum amplitude.

Two possible improvements in the MVDC VARC-CB design have been suggested. The first is to implement two separate LC circuits, each specifically designed for certain interruption current values. This can provide more favorable VI interruption conditions compared to using one single LC circuit for all interruption current levels. The approach is, however, only beneficial if the VARC-CB module is to be designed for two separate, limited ranges of interruption current values. For the modeled VARC-CB, it was found that using $Z_{LC} = 4.85\ \Omega$ when interrupting bolted SC faults and $Z_{LC} = 4.7\ \Omega$ when interrupting nominal load current (case 2) gave very favorable VI interruption conditions overall.

The second suggested improvement is to adjust the VSC triggering instant according to the interruption case, rather than keeping it fixed. One possibility is to adjust the triggering based on an estimation of the VSC operation time, and always minimize the value of $t_{\text{VSC,delay}}$. This will ensure that no additional time, beyond the time needed for the VI opening, is required for the VSC operation. In this way, the total operation time of the breaker is always minimized. Another possibility is to estimate the prospective line current together with the peak values and peak instants of i_{VSC}, and on this basis select a $t_{\text{VSC,delay}}$ value ensuring a θ_i close to 90°. By controlling θ_i in this way, the constraints imposed on the VARC-CB design by the limited di/dt- and dv/dt capabilities of the VI are loosened, enabling a wider range of possible parameter values.

7.2 Further Work

Several recommendations for further work can be made. One is stated in the very last subsection of the previous chapter, 6.4.5. Here it was emphasized that more work is required for examining factors influencing the interruption conditions of the VI, in particular the ones related to the RRITIV. In the DC system considered, capacitors were included to represent the stray capacitance of equipment in the vicinity of the VARC-CB module. This was a necessity in order to obtain RRITIV values in a realistic range. However, the chosen location and capacitance value of the capacitors, both of which have essential impact on the RRITIV, may not be fully precise. Furthermore, no frequency-dependence was included in the model, which is essential to consider for obtaining TIV waveforms and RRITIV values with adequate accuracy. These considerations indicate that a more comprehensive analysis and modeling of the system is needed in order to obtain more accurate design constraints and simulation results related to the dv/dt conditions at VI interruption.

A second recommendation for further work is to investigate the MVDC VARC-CB performance through lab work to verify the proposed design strategies experimentally. A third is to simulate the VARC-CB in a multi-terminal grid, to examine how it operates in a realistic DC grid application. The protection coordination when using multiple VARC-CBs in the multi-terminal grid should also be studied. A fourth is to investigate how to upscale the proposed MVDC design strategies to HVDC applications. Finally, different power semiconductor devices should be evaluated for the switch positions of the VSC in the VARC-CB module. In particular, the possibilities of using wide-bandgap (WBG) devices for improving breaker performance should be investigated.

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Appendix A

MOV Model Parameterization

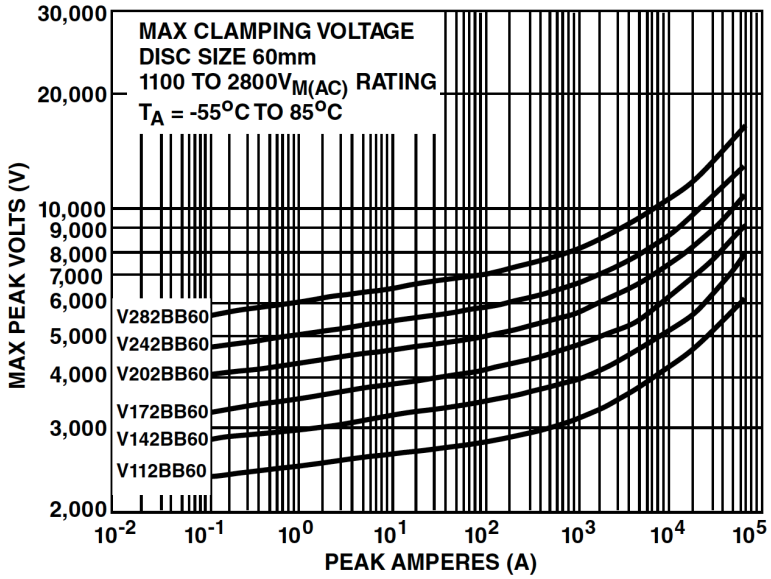

Figure A.1: V-I characteristics of the BB series MOVs from Littelfuse, from [89].

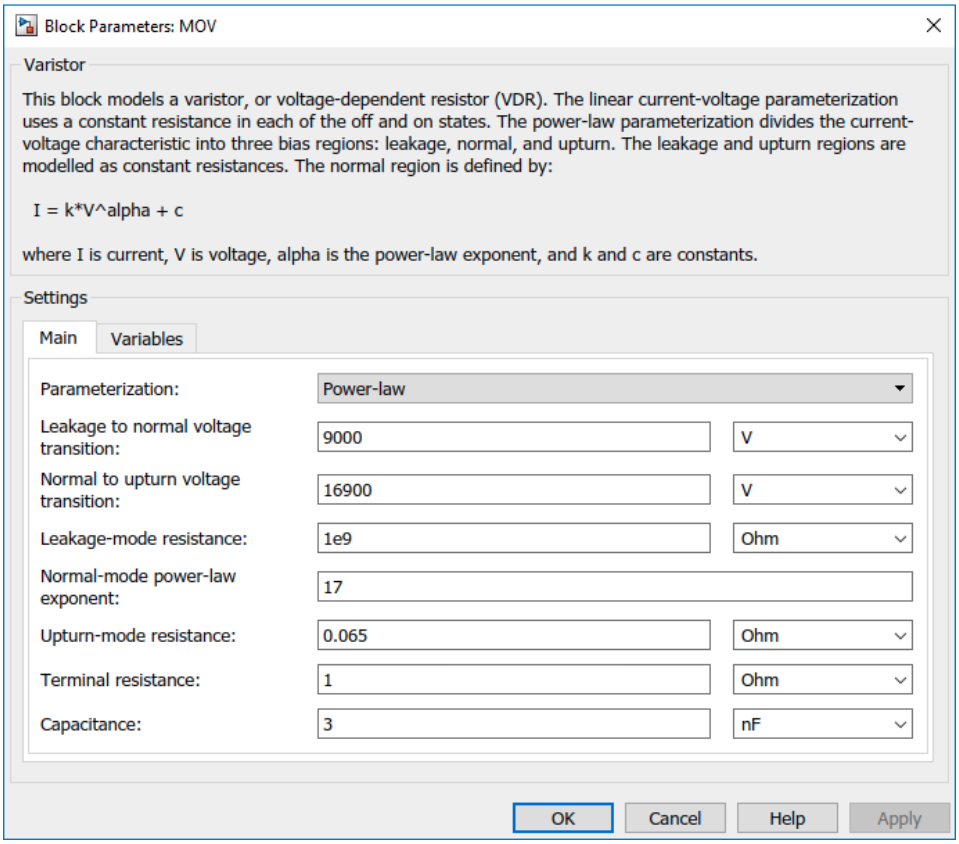

Figure A.2: Parameterization of the *Varistor* block representing the developed MOV module.

Appendix B

IGBT Model Parameterization

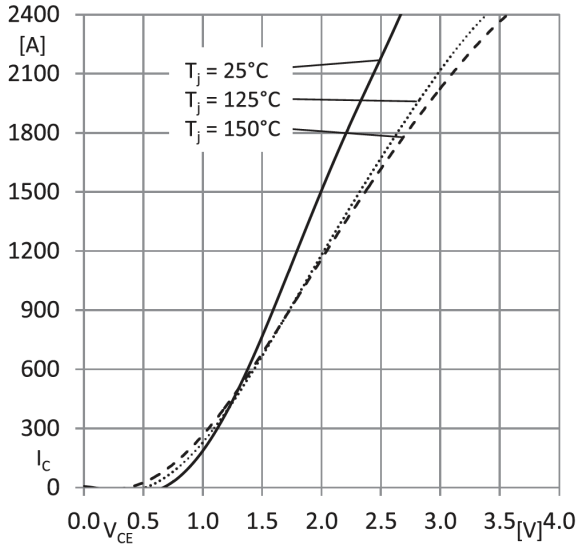

Figure B.1: SEMIKRON SKM1200MLI12TE4 IGBT1 output characteristics $I_C = f(V_{CS})$, V_{GE} = 15 V, from [103].

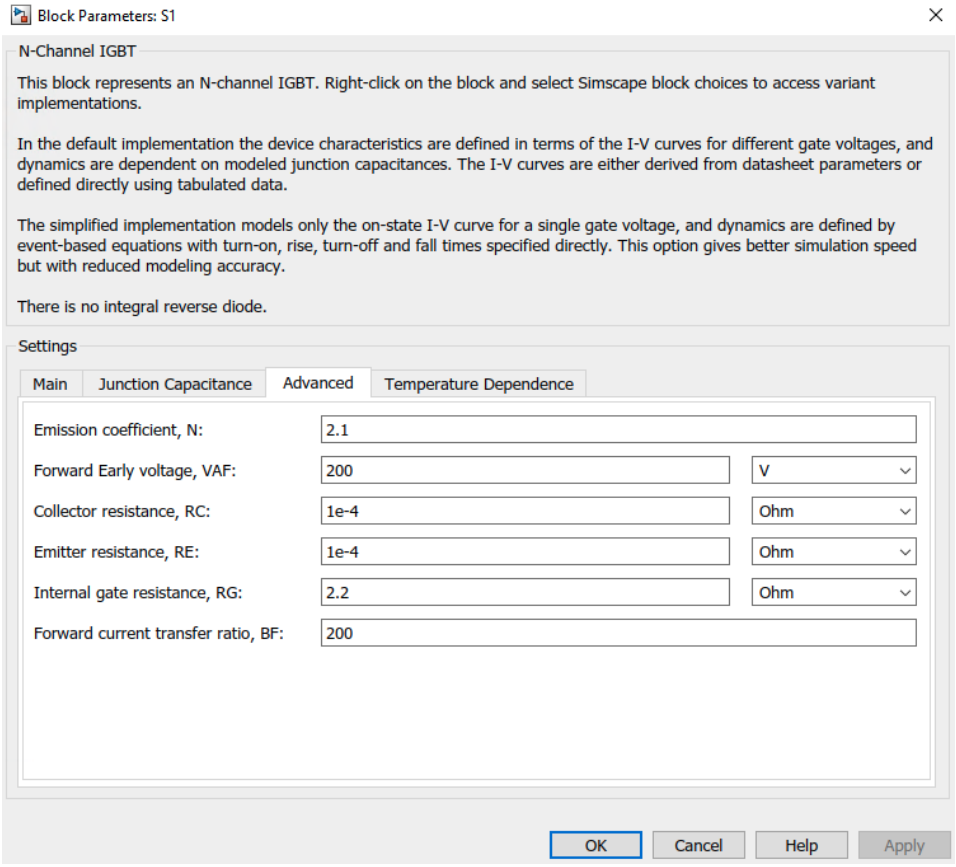

Figure B.2: Parameterization of the *N-Channel IGBT* blocks representing the IGBTs of the VSC.

Appendix C

Final Model Parameterization

Table C.1: Final parameterization of the simulation model.

Parameter	Description	Value	Unit
V_{nom}	Nominal grid voltage	10	kV
I_{nom}	Nominal grid current	1	kA
R_L	Nominal load resistance	10.4	Ω
$I_{i,\text{min}}$	Minimum interruption current	1	kA
$I_{i,\text{max}}$	Maximum interruption current	2	kA
r_{line}	DC line resistance per length	0.089	mΩ/m
l_{line}	DC line inductance per length	0.347	μH/m
c_{line}	DC line capacitance per length	0.307	nF/m
g_{line}	DC line conductance per length	5	μS/m
d_{line}	DC line length	1000	m
-	Number of series-connected pi-line segments	100	-
C_{x1}	Source side stray capacitance	5	nF
C_{x2}	Load side stray capacitance	5	nF
R_f	SC fault resistance	0.1	Ω
V_{clamp}	Clamping voltage of MOV module	15	kV
R_{MOV}	Terminal resistance of MOV module	1	Ω
C_{MOV}	Capacitance of MOV module	3	nF
L_{MOV}	Stray inductance of MOV module	30	nH
R_{low}	Closed resistance of VI	35	$\mu\Omega$

R_{high}	Open resistance of VI	1	TΩ
V_{arc}	Arc voltage of VI	20	V
R_s	Stray resistance of VI	50	Ω
L_s	Stray inductance of VI	50	nH
C_s	Stray capacitance of VI	50	pF
$(di/dt)_{\text{cap}}$	di/dt capability of VI	650	A/μs
$(dv/dt)_{\text{cap}}$	dv/dt capability of VI	5–10	kV/μs
-	Closed resistance of RCB	1	mΩ
-	Open conductance of RCB	1	μS
f_{LC}	Switching/resonance frequency	10	kHz
C_{DC}	DC link capacitance	3.75	mF
V_{DC}	Precharged DC link voltage	400	V
R_{CH}	Charging resistance of DC link	1	Ω
τ_{CH}	Charging time constant of DC link	3.75	ms
R_p	Resistance modeling losses in lead resistance and in passive components of current injection branch	0.05	Ω
L_p	Oscillation inductance	77.2	μH
C_p	Oscillation capacitance	3.28	μF
Z_{LC}	Characteristic impedance of passive resonant circuit	4.85	Ω
K	Safety margin related to maximum achievable oscillating current amplitude	1.1	-
L_{lim}	Current-limiting inductance	44.5	mH
t_{rel}	Relay time	2	ms
t_{act}	VI actuation delay	1	ms
t_{open}	VI opening time	1	ms
$t_{\text{VSC,delay}}$	Delay of VSC triggering w.r.t. initial VI contact separation	0.67	ms
t_0	Fault inception instant (NB: The simulation results are presented with t_0 = 0)	100	ms
t_1	Trip signal from relay received by VI	102	ms
t_2	Initial contact separation in VI	103	ms
t_3	VSC triggering	103.67	ms

Appendix D

Auxiliary Passive Resonant Circuit

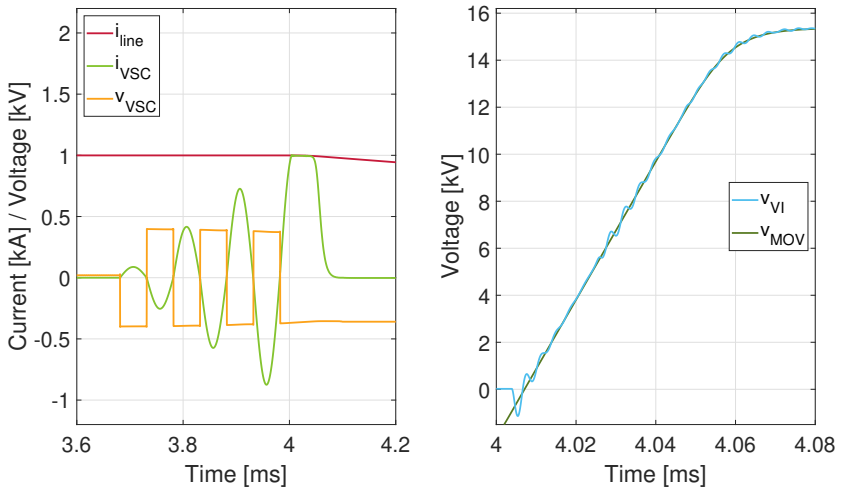

Figure D.1: Simulating case 2 with the proposed auxiliary LC circuit of Z_{LC} = 4.7 Ω. Left: Line current, VSC current, and VSC voltage. Right: VI and MOV voltages.

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Design Considerations and Modeling of a VSC Assisted Resonant Current DC Circuit Breaker for MVDC Applications

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