Master's thesis

NTNU
Norwegian University of Science and Technology
Faculty of Information Technology and Electrical Engineering
Department of Electric Power Engineering

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Introduction of Silicon Carbide in High-Power Converters Using a Hybrid Si-SiC Switch

Master's thesis in Energy and Environmental Engineering
Supervisor: Dimosthenis Peftitsis
June 2020

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SIEMENS

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Preface

This master thesis is the culmination of my five years at the Norwegian University for Science and Technology, and has been written in collaboration with Siemens AS. The entire thesis builds on the experiences I've accumulated through my years at NTNU, as well as the passion I've developed for electrical engineering since I chose the specialization at the end of my second year. Even though the studies have at times proved challenging, I've managed to get through it thanks to rigorous work and a strong support system consisting of of friends and family. I can't thank them enough.

The thesis itself builds on the specialization project "Introduction of Silicon Carbide in High-Power Converters - A Literature Review", meaning that almost entire year has been dedicated to researching this topic. The topic I ended up choosing for my thesis ended up being a big challenge, which was something I relished in. Nonetheless, there were times were I would not have been able to complete my thesis if it was not for the very helpful guidance I received throughout the year. Especially my supervisor, Dimosthenis Peftitsis, deserves praise, as he was always available, and his feedback was consistently constructive. I would also be remiss if I did not extend a thanks to my co-supervisor Jonas Sjolte of Siemens Trondheim, for the opportunity afforded to me when I was offered a summer internship at Siemens, as well as being offered this thesis subject. It was an invaluable experience. Finally, I must thank Andreas Giannakis, who ended up helping me greatly when I was experiencing difficulties with my simulations, even though he wasn't originally my co-supervisor.

Given the extraordinary circumstances that occurred this semester with the covid-19 pandemic, writing the thesis has proven to be challenging in more ways than one. It is therefore essential that I give my parents a special mention for letting me move home during the pandemic, which provided me with much needed stability in a stressful time. I must also mention my sisters, who have always been an important source of motivation, even if they might not know it.

I hope you enjoy your reading.

Lars-Kristian Njåstad
Trondheim, June 2019

Abstract

This master thesis has investigated the use of wide bandgap (WBG) semiconductors in high-powered converters. In comparison to the traditionally used semiconductors, like silicon (Si), WBG semiconductors like silicon carbide (SiC) enable the production of devices with larger breakdown voltages, lower conduction losses, and faster switching. All of these attributes are desirable for use in high-powered converters, but because of the immaturity of SiC technology there are cost and reliability issues. These deficiencies makes full SiC integration a nonviable solution for the industrial market. Therefore, novel solutions, like the hybrid Si-SiC switch (HyS) needs to be employed.

The HyS consists of a parallel connection of a Si IGBT and SiC MOSFET. The Si IGBT takes care of the steady-state conduction, enabling the use of a low-powered SiC MOSFET as an auxiliary switch in order to handle the hard switching actions of the converter. By using this configuration, the desirable features of SiC can be integrated into high-powered converters for a reasonable cost. Namely, increasing the switching speed of the converter is desirable as it would lead to a decrease in the size of passive components like inductors and capacitors, decreasing the bulk of the system. Therefore, it was deemed necessary to investigate the use of the HyS solution in a high-powered converter in order to establish if, and potentially by how much, the use of the HyS would increase the maximum achievable switching frequency, $f_{sw,max}$, of the given converter. Furthermore, the most pertinent practical challenges for realizing the HyS solution needed to be identified so that proper mitigation techniques could be put into place.

In order to verify the use of the HyS solution, the electrical and thermal performance of the HyS was assessed using simulations. Using the Simscape library in Simulink, the dynamic electrical performance of the HyS and its constituent components was assessed. From these simulations, several approximations of the dynamic behaviour of the HyS that would be used during the thermal simulations were established. Then, steady-state analysis of the thermal performance of the HyS was conducted using PLECS. During these simulations, a parametric sweep was conducted in order to assess how different operating conditions affected the $f_{sw,max}$ of a converter using the HyS solution.

These simulations uncovered that by using the HyS solution instead of a solo IGBT in a high-powered converter, $f_{sw,max}$ could be increased significantly. However, this was dependent on several factors, like minimizing the stray inductance in the HyS module, optimizing the current rating of the SiC MOSFETs, and maximizing the cooling efficiency of the system. Therefore, this thesis proposes a design process for an HyS custom module in order to combat the most pressing of these practical challenges.

Sammendrag

Denne masteroppgaven har undersøkt bruken av halvleder komponenter med høy båndbredde (WBG) i høyeffektsomformere. Sammenlignet med tradisjonelle halvledere, som for eksempel silisium (Si), så har WBG halvledere som for eksempel silisiumkarbid egenskaper som gjør det mulig å produsere komponenter med høyere blokkespenning, lavere ledetap, og raskere svitsjing. Alle disse egenskapene er ønskelige når det skal produseres høyeffektsomformere, men fordi SiC-teknologi fremdeles ikke har modnet enda så er det problemer med både kostnader og pålitelighet. Disse manglene betyr at fullstendig SiC integrasjon i det industrielle markedet fremdeles ikke er gjennomførbart. Derfor kreves nytenkende løsninger, som for eksempel hybrid Si-SiC svitsjen (HyS).

HyS består av en parallellkobling mellom en Si IGBT og en SiC MOSFET. Si IGBT'en tar hånd om steady-state strømoverføring, noe som gjør det mulig å bruke en laveffekt SiC MOSFET som en hjelpesvitsj som tar hånd om svitsjingen i omformeren. Ved å sette sammen de to svitsjene på denne måten blir det mulig å utnytte seg av de ønskelige egenskapene til en SiC MOSFET i en høyeffektsomformer for en fornuftig kostnad. Det er spesielt interesse for å øke svitsjehastigheten til omformeren siden det vil gjøre det mulig å redusere størrelsen på passive komponenter, som for eksempel spoler og kondensatorer, som vil bidra til å minimere massen til systemet. Av den grunn ble det sett på som nødvendig å undersøke hvordan HyS svitsjen opererte i en høyeffektsomformer. På den måten kunne det fastslås om bruk av HyS-løsningen kunne bidra til å øke den maksimalt oppnåelige svitsjefrekvensen, $f_{sw,max}$, for en gitt omformer, og eventuelt hvor mye $f_{sw,max}$ kunne økes med. Videre, så ble det sett på som viktig å identifisere de største utfordringene som måtte løses for å kunne realisere HyS-løsningen.

For å kunne verifisere HyS-løsningen så ble både de elektriske og termiske egenskapene av HyS-svitsjen evaluert ved hjelp av simuleringer. De dynamiske elektriske egenskapene til HyS'en ble kartlagt ved å bruke Simscape-biblioteket i Simulink. Disse simuleringene gjorde det mulig å sette sammen en rekke approksimasjoner av oppførselen til HyS'en som deretter skulle brukes i simuleringene av de termiske egenskapene til HyS-løsningen. De termiske egenskapene ble evaluert ved å bruke steady-state-analyseverktøyet til PLECS. Gjennom en rekke tester av forskjellige parametere hos HyS'en, ble forholdet til disse parameterne med $f_{sw,max}$ kartlagt.

Fra simuleringene i denne oppgaven ble det kommet frem til at ved å erstatte en solo IGBT-løsning i en høyeffektsomformer med HyS-løsningen, kunne en øke $f_{sw,max}$ markant. Dette var derimot avhengig av en rekke faktorer, som å minimere parasittisk induktans i HyS-modulen, optimere strømrating forholdet til SiC MOSFET'ene, og maksimere kjøleeffektivitet. Av den grunn foreslår denne oppgaven en designprosess for en HyS-modul som tar hensyn til alle disse utfordringene på en måte som maksimerer $f_{sw,max}$.

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Chapter 1

Introduction

1.1 Background and Hypothesis

Since the industrial revolution, the world's energy demands have skyrocketed. In tandem with this development, climate gas emissions have increased to unacceptable levels. This has led to a global climate crisis, with temperatures increasing, weather becoming more extreme, and the world's ecosystems in peril. Still, the world's energy demands are ever increasing, with developing countries becoming more and more industrialized with every passing year. In order to keep up with these energy demands, while at the same time managing the ongoing climate crisis, it essential to replace fossil fuel with clean, renewable energy as the primary energy source of the world. However, introducing renewable energy sources in a way that does not compromise the power grids' ability to reliably provide electricity requires the further development of technology used to both generate and store electrical energy. This technology should allow for renewable energy systems to be efficient, robust, and properly integrated into the preexisting energy infrastructure of the world.

One of the most important technologies for efficiently integrating renewable energy systems into the power grid is power electronics. Power electronics uses semiconductor technology to control and convert electrical energy in order to transfer the necessary power levels to and from various components in a system. Common power electronics devices are for example the HVDC converter used in transmission networks, which allows for the conversion of high-voltage DC power to high-voltage AC power and vice versa, and motor drives, which uses power electronic switches in order to control the speed and torque of an electrical motor. Since the advent of semiconductor technology, silicon (Si) has been the dominating material. Given the maturity of Si technology, it is both reliable and simple to manufacture. However, the technology has been pushed to its theoretical limit, and with increasing power demands, a paradigm shift is needed in order to keep up with the requirements of the ever developing power grid.

The most promising avenue for developing solutions which are compatible with the needs of future power systems, is to replace Si with a wide bandgap (WBG) semi conductor. Using a WBG instead of Si allows for the development of power electronic devices with several advantageous properties, including larger power densities, higher breakdown voltages, and lower power losses. These technologies have already been employed in many low-power converters, but for high-powered systems like for example motor drives, the WBG technology has still not taken hold. Nevertheless, high-powered applications are expected to move towards WBG technology, with silicon carbide (SiC) being the WBG semiconductor of choice. However, before this can be realized, some obstacles still needs to be overcome.

In contrast to Si technology, SiC technology is still immature. This leads to high costs and reliability issues, making a complete replacement of Si with SiC a nonviable solution for the industrial market. As a consequence, while the technology is still maturing, novel solutions needs to be employed in order to take advantage of the properties of SiC without being prohibitively expensive. One such solution will be the focus of this project: The hybrid Si-SiC power switch. The hybrid switch is a parallel connection of a Si IGBT, the dominant power transistor in current state-of-the-art high-power converters, and a SiC MOSFET. In this arrangement, the SiC MOSFET is only used as an auxiliary switch, while the IGBT takes care of steady-state current conduction. This allows for the use of a low-powered SiC MOSFET, significantly reducing the cost of the system compared to a full SiC MOSFET solution. Using the hybrid switch arrangement helps mitigating the biggest weakness of the silicon IGBT, switching losses, since the hard switching actions will done by the SiC MOSFET. This should allow for an increase in switching frequency in comparison to a full IGBT solution, which in turn would allow for the reduction in the size of passive components. Reducing the size of passive components is desirable, as it leads to a decrease in the cost and bulk of a system. However, it is uncertain if this arrangement will work in a high-power application, which leads to the research question of the thesis:

Research Question: Does the hybrid switch actually function in a high-power converter? If it does, by how much can the switching frequency be increased in order to reduce the bulk of passive components? What are the major practical challenges for realizing the hybrid switch in a functioning converter?

Given previous research on the subject conducted in the specialization project [1], the following hypothesis is presented:

Hypothesis: The introduction of the hybrid switch will remarkably increase the switching frequency of the converter, but with an important caveat: It will not be viable if it is put together by off-the-shelf-components, meaning a custom module design is required.

1.2 Objectives and Limitation of Scope

The main objectives of this master thesis is presented below:

- Present the SiC MOSFET, and illustrate how replacing Si with SiC changes the

properties of the device.

- Present the most pertinent challenges introduced by replacing Si with SiC.
- Present the hybrid switch concept, how it works, why it is useful, and the bottlenecks for realizing the concept.
- Design accurate models for the power transistors used in the hybrid switch; the IGBT and the SiC MOSFET.
- Through the use of simulations, investigate the behaviour of the hybrid switch in order to obtain an optimal switching pattern.
- Investigate how stray inductance affects the dynamic behaviour of the hybrid switch.
- Evaluate the performance of the hybrid switch using electrical and thermal simulations, and determine if, and potentially by how much, the maximum switching frequency of a given system can be increased by using the hybrid switch configuration.
- Identify potential challenges or bottlenecks for realizing the hybrid switch in a real converter.
- Present a proposal for how to design a high-power converter using the hybrid switch solution in a way that takes practical design challenges into account.

The scope of the thesis is limited to achieving these objectives through the use of simulations only, meaning no practical tests in a laboratory environment will be conducted. These simulations will be limited to analyzing electrical and thermal performance, meaning other issues like electromagnetic interference (EMI) and system reliability will not be studied in this thesis. The thesis also does not provide any detailed explanation, nor analysis, of the requirements of a gate driver for the hybrid switch, focusing only on the hybrid switch module itself. Furthermore, the practical feasibility of the different design techniques used in the thesis will not be analysed, and only how implementing such techniques affects the performance of the HyS will be discussed.

1.3 Report Outline

This thesis consists of 6 chapters, which together will cover all of the objectives, the research question, and test the hypothesis. This introduction is the first part of the thesis, having covered the background, hypothesis, objectives and the report outline.

Chapter 2 will present established theory that will be necessary in order to properly understand the ins and outs of the hybrid switch concept, as well as to justify why hybrid switches should be designed. Furthermore, the theory established in Chapter 2 will inform the methods used in the thesis, and will be used when analyzing the key findings of the thesis. The chapter is divided into three section; the first will be used to explain the SiC MOSFET, the second will go into detail of some of the major challenges tied to using SiC technology, and the final section will contain an in-depth explanation of how the HyS works.

Chapter 3 will present the methods used when modelling the hybrid switch in a way that is conducive to replication of the thesis. The method will be divided into three sections. The first section explains how the models for the two power transistors were designed. The second section explains how the electrical simulations were conducted, while the final section explains how the simulations of the thermal simulations were conducted.

Chapter 4 presents all of the results of the thesis, while Chapter 5 analyzes the results. Chapter 5 will consist of three sections, the first of which examines the viability of the power transistor models. The second and final sections will be analyzing the results from the electrical and thermal simulations, respectively. These sections will both the structured in the same way, with the first part of the sections being dedicated to analyzing the findings of the thesis in terms of how they compare to previously established theory, and use this to explain the significance of the results. The second part of the sections will critically examine both the method and results in order to uncover any limitations or sources of errors in the thesis, and discuss their consequences for the findings.

Finally, Chapter 6 will conclude the thesis. Starting by shortly summarizing the finding, and then concretely answering the research question presented in Chapter 1. This answer will then be compared to the hypothesis of the thesis in order to establish if the hypothesis was true or not. The final part of Chapter 6 will present a proposal for further work with the subject matter of the thesis.

Chapter 2

Theory

Note that the following chapter is an abridged version of the associated specialization project, "Introduction of Silicon Carbide in High-Power Converters - A Literature Review" [1].

This chapter will cover the theory surrounding three aspects of the hybrid Si-SiC switch: How replacing Si with SiC leads to a MOSFET with superior characteristics and why it would be desirable to use this MOSFET in mid- to high-voltage switching applications, the challenges related to using SiC, and how the Si-SiC hybrid functions and which aspects are the most pertinent bottlenecks for realizing the concept in high-power converters.

2.1 The SiC MOSFET

The SiC MOSFET is simply put a MOSFET which is manufactured using silicon carbide (SiC) instead of Si. Given that the electrical and material properties of SiC is vastly different than that of Si, as seen in Figure 2.1, this makes it possible to manufacture a MOSFET with some desirable features which are not possible to achieve using Si. This section will explain how using SiC is beneficial by contrasting the conduction and switching losses of the Si MOSFET with those of the SiC MOSFET. The section will also compare the SiC MOSFET with the State-of-the-Art switches used in mid- to high-voltage applications, the Si IGBT.

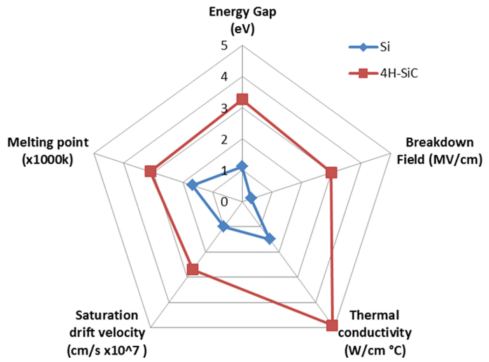


Figure 2.1: Comparison of select material properties between SiC and Si [2]

2.1.1 Conduction Losses

The defining characteristic of SiC is the fact that it is a WBG semiconductor. This means that the bandgap of SiC, or the energy required to transmit an electron from the valence band to the conduction band, is higher than compared to a conventional semiconductor like Si. This comes with a slew of advantages, the most notable being the increased breakdown field. As can be seen from Figure 2.1, the breakdown field of SiC is an order of magnitude larger than it is for Si. This means that it is possible to create devices with larger breakdown voltages and higher doping concentrations, which makes it possible to manufacture devices with thinner drift regions. Increasing the thickness of the drift region in a semiconductor die is the main way to increase the voltage blocking level of said device, but increased thickness comes with the downside of increased ON-resistance, $R_{ds(ON)}$, which leads to a larger fraction of the power through the semiconductor being dissipated as heat during conduction. Therefore, it follows that by using SiC, which enables the production of thinner dice, the conduction losses will be lowered for the same blocking voltages [2–4].

The improvement in specific ON-resistance, $R'_{ds(ON)}$, is illustrated by Figure 2.2. The figure shows that not only is the ON-resistance of the SiC MOSFET significantly smaller than for its Si counterpart, but the lower conduction losses also makes SiC MOSFETs with large voltage blocking levels viable. This allows for the use of MOSFETs instead of IGBTs in certain applications where the voltage levels would otherwise be too large for the traditional Si MOSFETs. Why this is desirable will be elaborated upon later in the section.

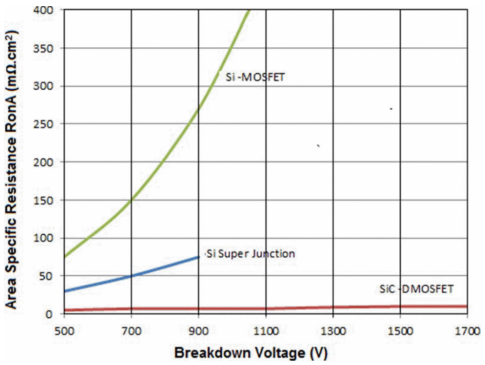
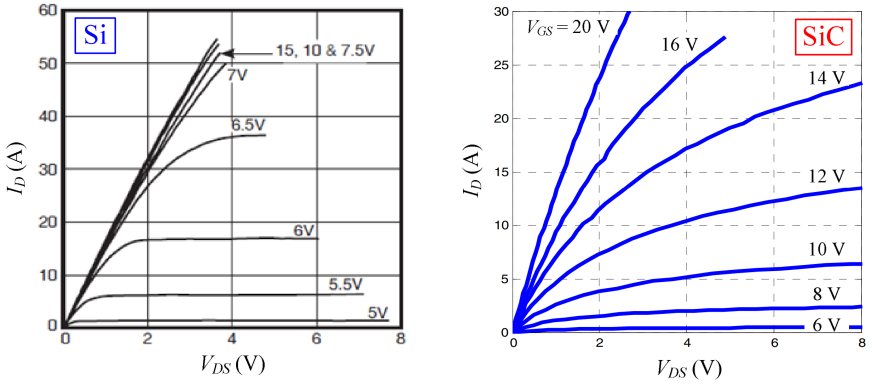


Figure 2.2: $R'_{ds(ON)}$ as a function of the breakdown voltage of SiC MOSFETs compared to Si MOSFETs [4]

Finally, there are a couple of differences in the behaviour of the ON-resistance of SiC MOSFETs in comparison to Si MOSFETs. The first difference is how the ON-resistance behaves in relation to gate voltage, V_{gs}. Figure 2.3 shows the IV-characteristics of a Si MOSFET and a SiC MOSFET for different gate voltages. The steeper the curve, the lower the ON-resistance is. As is clearly illustrated by the figure, the SiC MOSFET requires a larger gate voltage to reach optimal ON-resistance. This difference is caused by the lower transconductance of the SiC MOSFET, and means that the SiC MOSFET must be driven with a gate voltage of 20 V [2, 5]. This is important to keep in mind when designing driver circuits for SiC MOSFETs.



(a) Si **(b)** SiC

Figure 2.3: Comparison between the output characteristics for different gate voltage levels for a Si MOSFET and a SiC MOSFET [5]

The other difference is how the ON-resistance of the SiC MOSFET behaves at elevated temperatures. As with the Si MOSFET, the SiC MOSFET's ON-resistance has a positive

temperature coefficient. However, the ON-resistance of the SiC MOSFET increases significantly slower than the Si MOSFET's ON-resistance, as can be seen in Figure 2.4. The reason for this is because of how the channel resistance of the SiC MOSFET behaves in relation to temperature. The channel resistance is one of the main contributors to the total ON-resistance, along with for example the drift region resistance that was discussed earlier. In contrast to the channel resistance of the Si MOSFET, the channel resistance of the SiC MOSFET has a negative temperature coefficient, which partly counteracts the increase of ON-resistance as temperature rises. This is illustrated by the stapled line in Figure 2.4, since the channel resistance is dominating at a gate voltage of 16 V [4–6].

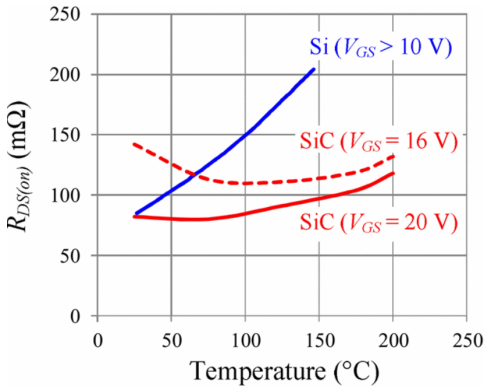


Figure 2.4: Selected Si- and SiC MOSFET's ON-resitance as a function of temperature [5]

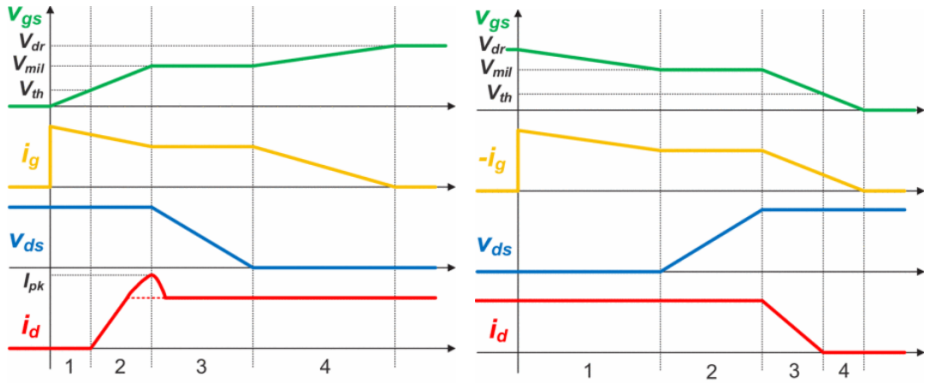
2.1.2 Switching Losses

Switching losses is one of the most important parameters for assessing the performance of a semiconductor device. In a power electronic switch, like a MOSFET or an IGBT, the switching losses in a hard switching converter are the consequence of a current-voltage overlap which occurs during turn-ON and turn-OFF. Accordingly, switching losses are divided into turn-ON losses and turn-OFF losses. Turn-ON losses, E_{ON}, can be calculated using (2.1), where t_{ov} is how long there is a current-voltage overlap, i_d is the instantaneous current, and v_{ds} is the instantaneous voltage. For the turn-ON operation, t_{ov} is defined as the sum of current rise time and voltage fall time. Turn-OFF losses are calculated in the same manner, but with t_{ov} defined as the sum of current fall time and voltage rise time [7, 8].

$$E_{ON} = \int_0^{t_{ov}} i_d v_{ds} dt \tag{2.1}$$

Figure 2.5 shows the ideal waveforms of a MOSFET during turn-ON and turn-OFF. The current-voltage overlap area can clearly be seen in area 2 and 3 during turn-ON, and area 3 and 4 during turn-OFF. As should be apparent when viewing the waveforms, the current-voltage overlap area of a MOSFET can be approximated as a triangle, which leads to (2.2).

Note that upper case denotes peak values of the respective variables, and that the subscripts r and f stands for rise and fall respectively.



(a) Turn-ON **(b)** Turn-OFF

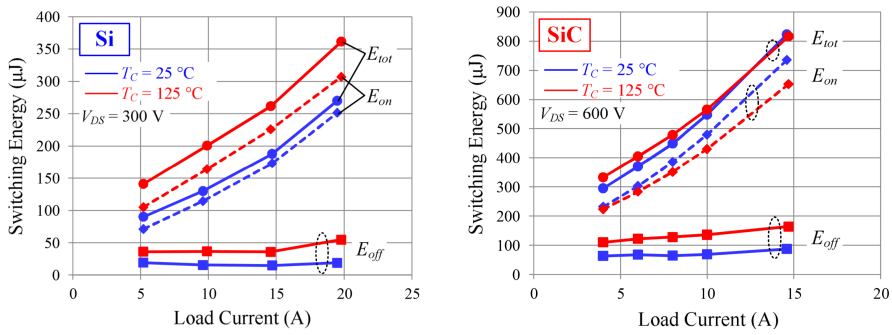
Figure 2.5: Theoretical switching waveforms of a MOSFET [8].

$$E_{ON} = \frac{1}{2} I_d V_{ds} (t_{ri} + t_{fv}) \tag{2.2a}$$

$$E_{OFF} = \frac{1}{2} I_d V_{ds} (t_{rv} + t_{fi}) \tag{2.2b}$$

These equations clearly shows that the switching losses are proportional to the rise and fall times of a MOSFET. As such, they imply that faster switching also leads to lower switching losses. Figure 2.1 shows that the saturation drift velocity of SiC is around three times higher than the case for Si. Since saturation drift velocity is directly related to the maximum switching frequency of a device, this shows that by using SiC instead of Si, the maximum switching frequency of a device can be increased. Consequently, the switching losses of a SiC device will be lower than that of a comparable Si device [4, 9]. Furthermore, because of the low ON-resistance of SiC devices, die areas can be reduced in comparison to Si devices. This leads to smaller gate capacitances and gate charges, which will lead to further switching loss reduction in SiC devices at high switching frequencies by reducing current oscillations [3].

An important difference between the switching characteristics of the SiC MOSFET and its Si counterpart is how the switching losses change with rising temperatures. As can be seen in Figure 2.6, in contrast to the Si MOSFET, the total switching losses of the SiC MOSFET are remarkably stable when increasing the temperature. This is because of the slight positive temperature coefficient of the SiC MOSFET's transconductance. As a consequence, the turn-ON losses of the SiC MOSFET actually decreases slightly with rising temperature. This decrease partly cancels out the increase in turn-OFF losses, leading to the stable nature of the total switching losses.



(a) Si **(b)** SiC

Figure 2.6: Switching losses for a Si MOSFET and a SiC MOSFET as a function of temperature [5].

There are several benefits to decreasing switching losses. The most obvious advantage is increased efficiency for a given switching frequency. Another benefit is that the switching frequency can be increased for the same amount of losses. Increasing the switching frequency will in some cases be preferred to making a more efficient system, since it allows for the reduction in the size of passive components like inductors, capacitors, and transformers. This allows for the production of a less bulky system, which is desirable in weight sensitive systems used in for example the transport industry. As an example, one of the more important parts of a power electronic circuit is the LC filter, which is necessary to reduce the harmonics which are transferred to the load. Harmonics can only carry reactive power, meaning that introducing harmonics to a load will lead to losses. This is filtered by using a low-pass LC filter, whose frequency response is shown in Figure 2.7. The cut-off frequency shown in the figure is a measure of which frequencies are filtered out by the filter, and it is determined by (2.3), where L is the inductance in Henries, and C is capacitance in Farads.

$$f_c = \frac{1}{2\pi\sqrt{LC}} \tag{2.3}$$

In a power electronics circuit, it is desirable to filter out the switching frequency used in the circuit. The lower the switching frequency, the larger the product LC needs to be. Since inductance is directly related to the weight of the filter inductor, a low switching frequency leads to a large inductor and a bulky system [7]. Therefore, as noted above, increasing the switching frequency used in the system can lead to a less bulky system. Accordingly, replacing a Si MOSFET with a SiC MOSFET will enable manufacturers to create less bulky systems.

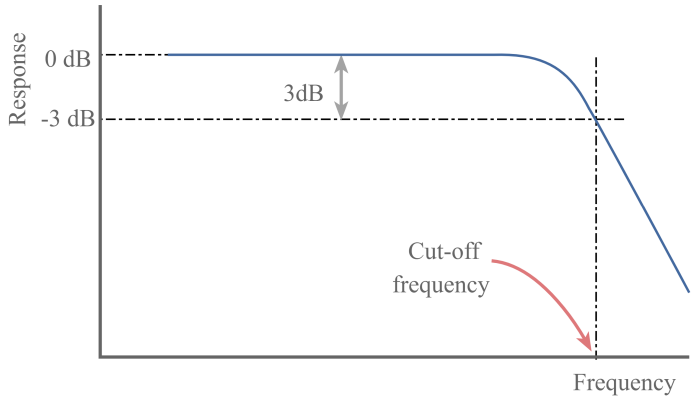


Figure 2.7: The frequency response of a low-pass LC filter [10]

2.1.3 Comparison to the IGBT

To illustrate why the SiC MOSFET might be preferred to the IGBT in some mid- to high-voltage applications, the two devices will be compared to each other.

The IGBT is the dominating device in mid- to high-voltage applications. It combines the features of a BJT and a MOSFET, being a voltage controlled bipolar device. A bipolar device, also known as a majority carrier device, is a semiconductor device that uses both holes and electrons to carry charge. In contrast, the MOSFET is a unipolar device, also known as a majority carrier device, which uses only one of either holes or electrons to carry charge. The bipolar nature of the IGBT is the main difference between it and the MOSFET, seeing as it drastically affects both conduction and switching characterisitcs [7].

In Figure 2.8, the IV-characteristics of an IGBT and a SiC MOSFET with the same voltage and current ratings are compared to each other. The most immediate difference between the two devices' characteristics is the constant voltage drop that is present across the IGBT. This means that at lower current levels, the conduction losses of the SiC MOSFET will be lower than that of the IGBT. However, the IGBT curve is clearly steeper than the SiC MOSFET curve, indicating that the conduction losses of the IGBT will be lower than the SiC MOSFET's when approaching rated current [11, 12]. The shape of the IGBT's IV-curves is a direct result of its bipolar nature, since the IGBT uses a concept known as conductivity modulation in order to decrease conduction losses. Conductivity modulation is facilitated by the injection of excess minority carriers, either electrons or holes depending on which is in the minority. This causes the electrons and holes which are present in the device to diffuse into the drift layer of the IGBT, which leads to higher conductivity than the ohmic characteristic of the device would suggest [7]. As a final note, where the IV-curves in Figure 2.8 intersect shows at which current level the IGBT conducts more efficiently than the SiC MOSFET. An important detail is the fact that at higher temperatures, this intersect point is at a lower current. This implies that the IGBT's conduction losses increases slower

than the conduction losses of the SiC MOSFET for rising temperatures.

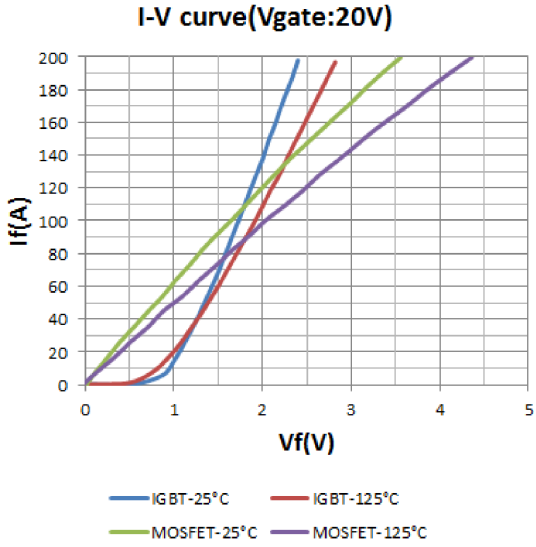


Figure 2.8: I-V characteristics of the Si IGBT and SiC MOSFET [11]

An example of the switching waveforms of an IGBT is shown in Figure 2.9. Like the MOSFET, the switching losses of the IGBT during hard switching operation is dominated by the current-voltage overlap area, and can be calculated in the same manner as with (2.1). The main difference between the IGBT waveform, and the MOSFET waveform shown in Figure 2.5, is the tailing current which can be seen during the IGBT turn-OFF. This is the consequence of using conductivity modulation, as the injected minority carriers needs to be completely removed to turn the IGBT off. The depletion of these carriers is a relatively time consuming process, thus the long current tail [7]. Consequently, the current-voltage overlap area during turn-OFF is increased, and the switching losses increases accordingly. This is corroborated by Figure 2.10, which shows that not only is the turn-OFF losses of the IGBT much larger than what is the case for the SiC MOSFET, but the turn-ON losses are larger as well. Accordingly, it can be concluded that the switching speed of the IGBT is slower than that of the SiC MOSFET, which can be attributed to the fact that the IGBT still uses Si. Si has a lower saturated drift velocity than SiC, leading to the lower switching speed. Finally, it is worth noting from Figure 2.10 that the IGBT's switching losses are more sensitive to elevated temperatures than the SiC MOSFET.

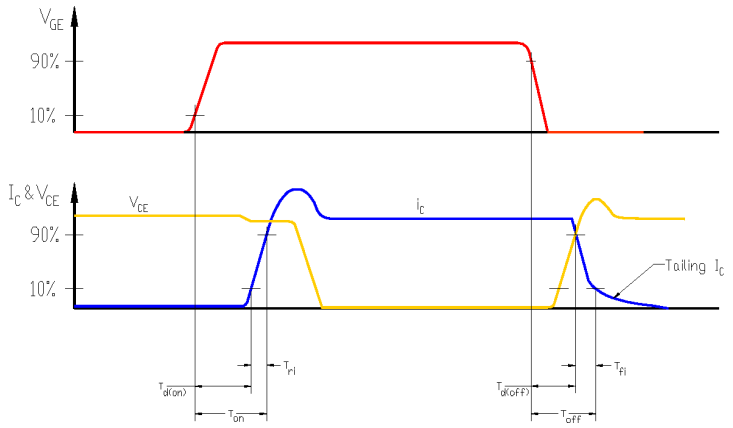
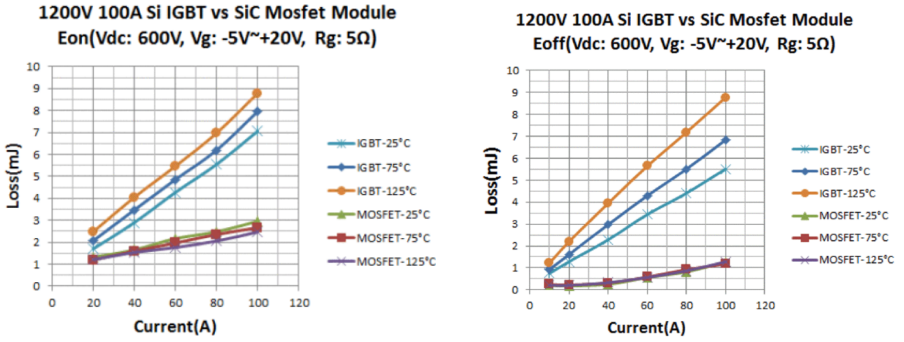


Figure 2.9: Theoretical switching waveforms of an IGBT [13]



(a) Turn-ON losses

(b) Turn-OFF losses

Figure 2.10: Turn-ON and Turn-OFF losses of the Si IGBT and SiC MOSFET as a function of load current [11]

In short, it will be desirable to replace the IGBT with a SiC MOSFET in applications where a higher switching frequency is desirable, while in applications where lower switching frequencies are acceptable the IGBT will be preferred because of its superior conduction properties.

2.2 Challenges with SiC

By using SiC instead of Si, some additional challenges are introduced to power electronic module design. These challenges can generally be attributed to one of four major differences between SiC and Si chips:

- Reduced die size as a result of lower specific ON-resistance.

- Can withstand higher temperatures as a result of the larger bandgap and the higher thermal conductivity.
- Faster switching as a result of higher saturated drift velocity.
- Stronger electric fields as a result of the higher bandgap energy.

More or less all of the challenges that originates from the above differences can be mitigated by using novel packaging solutions. A cross section of a package can be seen in Figure 2.11. As can be seen in the figure, a typical package consists of a heat sink, a baseplate, substrate, the semiconductor die, and the case. The die is anchored to the substrate using a die attachment material, and is electrically connected to the module terminals using traces in the substrate, and wirebonds at the top of the die. Finally, the case is filled with an encapsulation material to prevent contamination and vibration [14]. The challenges related to high-temperature operation and stronger electrical fields can both be solved by using different materials than what is typically used in off-the-shelf Si packages. This is elaborated upon in [15] and [16]. The two other differences between Si and SiC introduce more complex challenges, and therefore requires the use of novel packaging techniques.

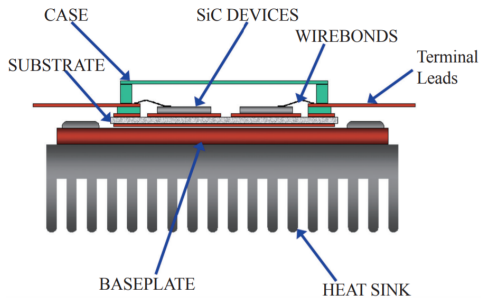


Figure 2.11: Cross-section of a traditional package structure [14]

2.2.1 Increasing Cooling Efficiency

As a direct consequence of the lower ON-resistance of SiC chips, the dice are thinner than what is the norm for Si dice. This means that a SiC chip will experience larger power- and current densities, leading to increased stress on the die, which might compromise its integrity [15]. Furthermore, because of immature production processes and the inability to manufacture large SiC wafers without defects, it is currently not possible to produce SiC chips with a chip area that allows for current ratings higher than around 100 A [17, 18]. These two issues in combination means that SiC dice are prone to a large amount of stress during full load operation. Additionally, the oxide layer of a SiC MOSFET is both thinner and experiences a larger amount of electrical stress than the oxide layer in a Si MOSFET. As a result, the oxide layer of a SiC MOSFET is quite sensitive, and is prone to cracking. This issue is exacerbated by elevated temperatures, which in turn means that current SiC MOSFETs are only able to withstand a maximum junction temperature of around 150-175

°C, far below the maximum potentail of the SiC material [17, 19, 20].

To maintain the reliability of a SiC MOSFET, it is therefore essential to enable efficient heat spreading and cooling of the device. In order to describe the thermal circuits of the SiC MOSFET, the Cauer thermal model will be used. In this model, every thermal layer is described as a branch with a thermal resistance and a thermal capacitance, as seen in the example shown in Figure 2.12. The thermal resistance is a measure of how the thermal layer resists a heat flow, and uses the unit K/W. Thermal capacitance, or heat capacity, describes how much heat can be stored in the layer per unit of temperature, and uses the unit J/K [7]. Using this model as a starting point, it is especially desirable to reduce the total thermal resistance of the thermal layers in order to make heat spreading more efficient. The high thermal conductivity of SiC in comparison to Si, as seen in Figure 2.1, is helpful, but there are other means which will further decrease the total thermal resistance.

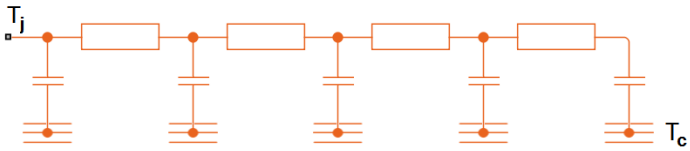


Figure 2.12: Cauer network describing thermal layers between semiconductor junction to base plate [21]

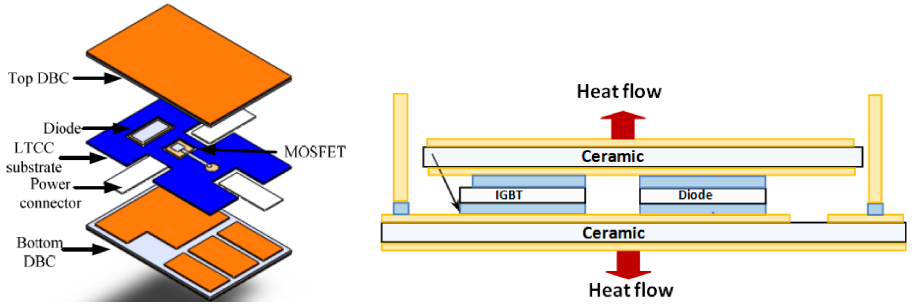
One way to decrease the thermal resistance, is to use a die attachment material with higher thermal conductivity. In (2.4), an approximation of the thermal resistance of a SiC chip with die attachment is shown.

$$R_{th} \approx \frac{d}{\lambda \cdot (L + d \cdot \tan(\alpha))^2} \tag{2.4}$$

L in this equation is the length of the chip edge of a square die, while d the thickness of a attachment material, λ is the conductivity of said material, and α is its thermal spreading angle. As is illustrated by the equation, the thermal conductivity of the die attachment material is inversely proportional to thermal resistance. Therefore, further emphasis on the choice of die attachment material and how it is applied will lead to more efficient heat spreading [15].

The most impactful method to decrease the total thermal resistance of the thermal network is to enhance how the system is cooled. In [22], two enhanced cooling methods are proposed: Direct liquid cooling and double sided cooling. Direct liquid cooling enables cooling through convection, which allows for the elimination of the conductive layer between the baseplate and the heat sink, which will reduce thermal resistance from heat sink to ambient significantly. Furthermore, convection cooling allows for a more stable heat exchange, reducing temperature variation in the SiC die, which is beneficial to the integrity of the device. Double sided cooling, as the name suggest, works by cooling the module from both bottom side and top side, instead of just the bottom as is done traditionally.

The concept is illustrated in Figure 2.13, which shows both the components required and a cross section of the setup. Using double sided cooling can increase cooling efficiency by up to 50 %, and this can be further improved by combining it with direct liquid cooling. However, it is only possible to employ double sided cooling by eliminating the use of wirebonds and replacing them with a flat substitute, for example by employing planar interconnection techniques.



(a) Component overview **(b)** Cross section

Figure 2.13: Double sided cooling setup showing both (a) component overview and (b) cross section [22]

A final issue introduced by the reduced die size comes from the aforementioned low current ratings. As a result of the low current ratings, several chips will need to be paralleled in order to reach desired power levels. This will have an adverse effect on heat spreading. Hence, an optimized distance between chips needs to be developed in order to have sufficient heat spreading while maintaining minimum distance between chips [15].

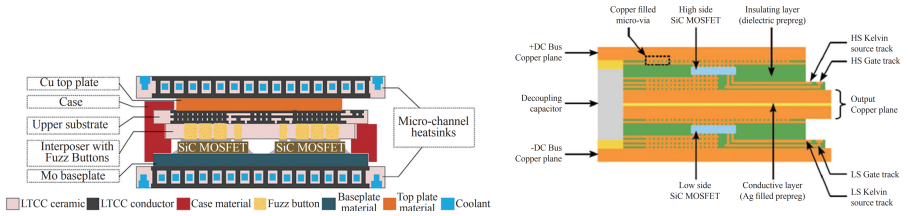
2.2.2 Mitigation of Parasitics

As was remarked in subsection 2.1.2, replacing Si with SiC enables the production of power devices with a higher maximum switching frequency. Although this is a desirable feature, it does bring along some challenges, since increasing the $\frac{di}{dt}$ and $\frac{dv}{dt}$ while keeping parasitic inductances and capacitances unchanged will lead to increased voltage overshoot, parasitic turn-ON in half-bridge modules, and ringing. In a typical semiconductor power module, there are three parasitic inductances of note: Commutation loop stray inductance, L_σ, gate loop inductance, L_G, and their mutual inductance, $M_{\sigma-G}$. These parasitics can prove to be a significant detriment to the performance of a SiC power module. The overvoltages induced by the parasitics might end up exceeding breakdown voltage levels if the stray inductance levels are not reduced from their typical magnitude in an off-the-shelf package [15].

The main way to reduce L_σ and L_G is to minimize the current loop in the module and in the gate driver, respectively.The gate driver loop can be reduced by using module integration, where associated components which are usually placed outside of the power module are put inside the package. One of these components is the gate driver, and placing the

gate driver within the power module will help to reduce the distance between the gate driver and the power device, which in turn will reduce L_G. Other components that can be integrated into the package are for example the decoupling capacitor, sensors, EMI filters, and thermal management systems [14].

In order to reduce L_σ, advanced packaging structures must be used. The commonly used structure in off-the-shelf packages is the wirebond structure, also known as a 2D structure. However, these structures leads to large amounts of stray inductance (>15 nH), making them incompatible with the high switching speed of the SiC. Therefore, solutions like the ones shown in Figure 2.14 needs to be used. The wireless structure eliminates the use of wirebonds, and instead employs planar interconnection techniques using an additional substrate. The additional substrate is placed directly on top of the chips, and copper traces on the substrate are used for routing and interconnection purposes. This allows for a vertical current flow between the two substrate planes, which can lead to a 30 % decrease in stray inductance by decreasing the interconnect paths. This structure is also better for cooling purposes, since it reduces the thermal resistance of the module, and allows for double sided cooling, as mentioned in subsection 2.2.1. The Chip-on-Chip solution, shown in Figure 2.14b, places chips directly atop of one another in order to further reduce the stray inductance of the module. This structure has been shown to reduce the stray inductance of a half-bridge module to as little as 0.25 nH, which is a reduction of two orders of magnitude in comparison to the current off-the-shelf packaging structures. The only way to reduce the stray inductance further is to use wafer-level packaging, which increases the complexity level of the packaging considerably [14, 15].

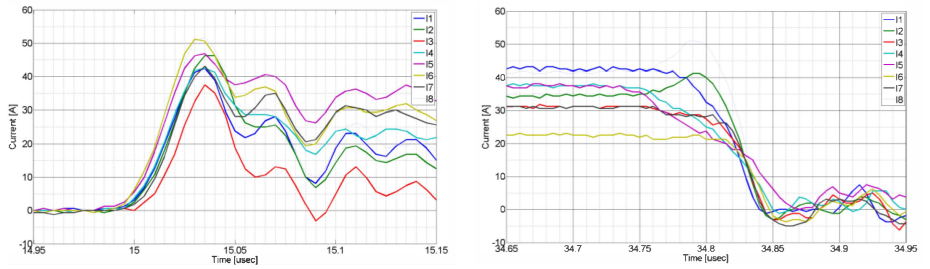


(a) Wireless **(b)** Chip-on-Chip

Figure 2.14: Example of different structures used to minimize stray induction [14]

An important issue related to the fast switching speed of SiC MOSFETs is how it relates to paralleling several chips. The reason for paralleling devices is generally to increase the current rating of the power module, and as such, it is imperative to keep the current level in all the paralleled devices balanced. In this way, no single die will be overloaded. Yet, parasitics between the paralleled chips can lead to current imbalance, and demands symmetrical layouts of the paralleled devices to mitigate the issue. But, with increased switching speed the tolerance for asymmetry is lower, making it more challenging to produce a module that is able to maintain current balance between its constituent components [14, 23]. Figure 2.15 shows an example of how asymmetric inductance distribution might affect the current sharing during switching instances. The set-up from the example consisted of 10 168 A rated SiC MOSFET half-bridge modules in parallel, where each module

consisted of 5 SiC MOSFETs in parallel per phase leg, for a total of 50 SiC MOSFETs per phase leg. A steady-state analysis of a single phase leg in a step down converter using a switching speed of 20 kHz showed that even without a perfectly uniform current distribution, the largest deviation from the average temperature of 38.73 °C was 1.5 °C, or 3.87 % [23]



(a) Turn-ON **(b)** Turn-OFF

Figure 2.15: Current distribution in 10 parallel SiC MOSFET modules during switching [23]

It is also worth noting that the Miller capacitance, the parasitic capacitance between the drain and gate of the SiC MOSFET, might lead to an accidental turn-ON in a half-bridge configuration or similar. If the charge in the capacitor leads to the voltage across the Miller capacitance exceeding the threshold voltage of the device in question, an accidental turn-ON will occur. The charge rate of the capacitor is the same as the current supplied to the capacitor, and this current is determined by the capacitor equation (2.5). The larger the $\frac{dv}{dt}$, the faster the capacitor is charged, and the more likely it is for an accidental turn-ON to occur [15].

$$i = C\frac{dv}{dt} \tag{2.5}$$

If this proves to be a problem, it can be mitigated using a Miller clamp, as seen in Figure 2.16. This allows the current to bypass the gate resistor by turning on the transistor CL during turn-OFF, significantly reducing the voltage drop across the gate. As a result, it becomes unlikely for a parasitic turn-ON to occur [24].

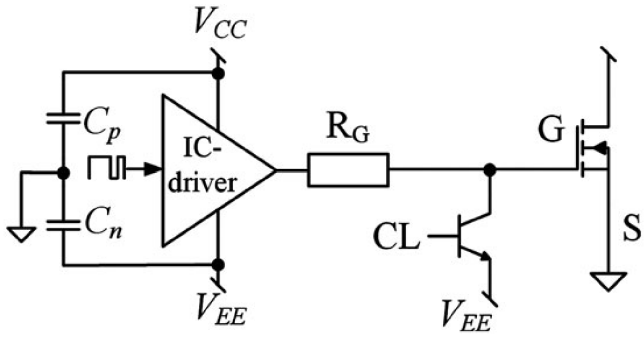


Figure 2.16: Gate driver using Miller clamp [24]

2.3 The Si-SiC Hybrid switch

The Si-SiC hybrid switch, hereafter referred to as the HyS, is a parallel connection of a Si IGBT and a SiC MOSFET, as can be seen in Figure 2.17. The aim of the HyS is to take advantage of the benefits provided by the SiC MOSFET while still keeping the cost of the system down. This is done by using the SiC as an auxiliary switch, which helps the IGBT during switching instances. As a result, the current rating of the SiC does not to match the current rating of the system it is used in, since the IGBT handles the steady-state conduction. This allows the HyS to provide switching loss mitigation while at the same time keeping the conduction capabilities of the IGBT and keeping costs at an acceptable level.

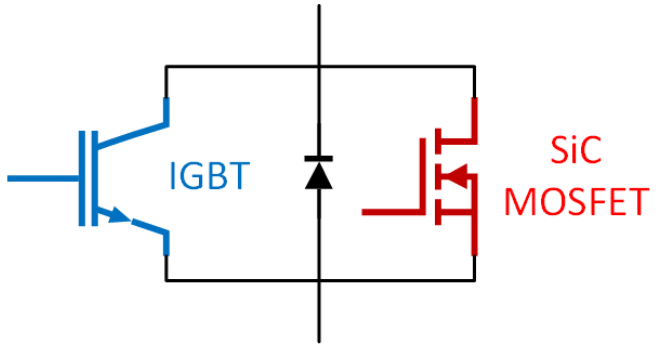


Figure 2.17: Circuit of hybrid switch

2.3.1 Conduction enhancement

By combining the IGBT and the SiC MOSFET using a parallel connection, not only is the favourable IGBT conduction profile maintained, it is also enhanced. One of the drawbacks of the IGBT is, as mentioned in subsection 2.1.3, the constant voltage drop across the device. As a consequence, the IGBT conducts current more efficiently at heavy-load

conditions than it does in light-load conditions. By paralleling the IGBT with the SiC MOSFET, this issue is subdued, as the SiC MOSFET will carry the majority of the current during ligh-load conditions. In this context, light-load conditions is defined as the load-level in which the SiC MOSFET carriers the majority of the current, while heavy-load conditions are defined as the load-level in which the IGBT carriers the majority of the current. This can be expressed using (2.6), where I'_{load} stands for the load current at the instance when the current through the IGBT and SiC MOSFET is equal, and I_{sp} is referred to as the sweet-point current, which is the current level through the SiC MOSFET when the voltage drop across the MOSFET is the same as the total voltage drop across the IGBT [25–28].

$$I_{sp} \approx \frac{V_{ce(sat)}}{R_{ds(ON)}} \tag{2.6a}$$

$$I'_{load} = I_{MOSFET} + I_{IGBT} = 2I_{sp} \tag{2.6b}$$

$$\text{light-load condition: } I_{load} < 2I_{sp} \tag{2.6c}$$

$$\text{heavy-load condition: } I_{load} > 2I_{sp} \tag{2.6d}$$

The sweet point current can also be defined as the point at which the two superimposed IV-characteristics of the IGBT and the SiC MOSFET intersect. This is illustrated by Figure 2.18, which also demonstrates how the sweet point current becomes lower as temperature rises [28]. This aligns with what was stated in subsection 2.1.3, since the conduction characteristic of the IGBT is less affected by temperature than the SiC MOSFET .

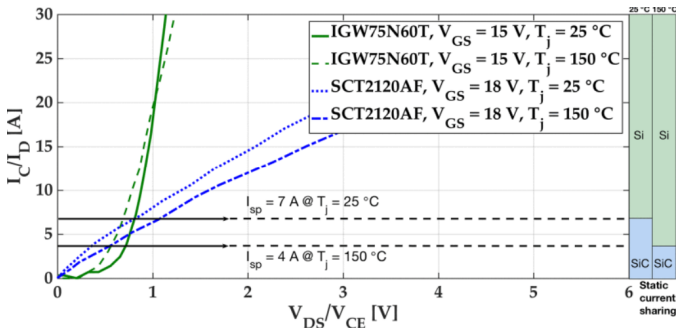


Figure 2.18: IV-Characteristics showing sweet point current for different temperatures [28].

Finally, the IV-characteristic of the HyS can be seen in Figure 2.19. This shows that the HyS reduces losses at almost every current level as a result of the conduction enhancement provided by the SiC MOSFET.

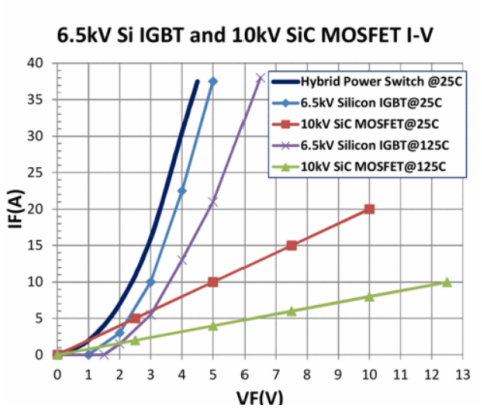


Figure 2.19: IV-characteristic of the HyS in comparison to its constituent components [25]

2.3.2 Switching strategies

In order to take advantage of the SiC MOSFETs superior switching capabilities, one of several gate control options can be used. The most common of these options are shown in Figure 2.20. As the figure makes clear, the main switching strategy is to delay the switching actions in a way that enables the IGBT to switch at approximately zero voltage switching (ZVS) conditions [25, 27, 28]. This will reduce the switching losses of the IGBT substantially, and since the SiC MOSFETs switching losses are much smaller than the IGBT, as demonstrated by Figure 2.10, the total switching losses of the HyS will be considerably lower than that of the IGBT.

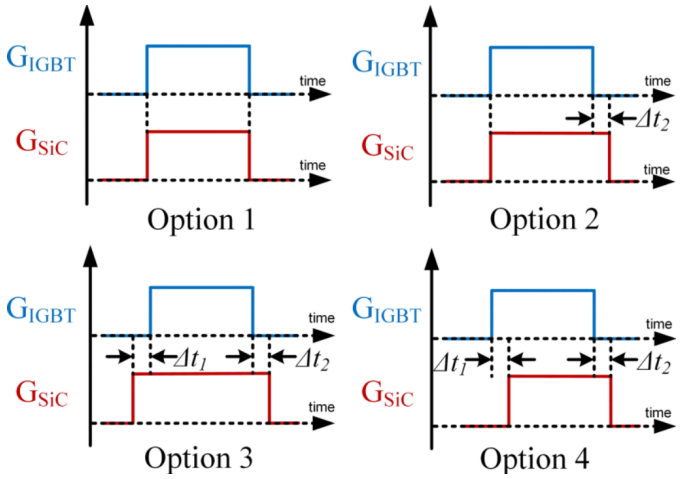


Figure 2.20: The gate control options for the hybrid switch [28]

The switching pattern that reduces switching losses the most is Option 3, where the SiC

MOSFET turns on before the IGBT, and then turns off after. In this way, the IGBT experiences near ZVS during both turn-ON and turn-OFF. In Figure 2.21, a timing diagram for this switching strategy is shown. This diagram demonstrates how to choose the length of the switching delays in order to simulate ZVS conditions for the IGBT. For the turn-ON delay, referred to as t_1, the duration of the delay should be slightly longer than the turn-ON time of the SiC MOSFET. Specifically, it is important that the voltage level of the HyS has had time to reach zero before the IGBT is turned on.

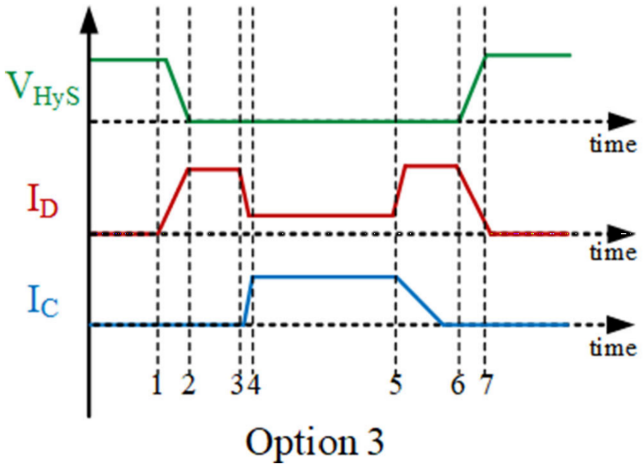


Figure 2.21: Timing diagram for gate control option 3 [28]

When choosing the turn-OFF delay, hereafter referred to as t_2, there are more variables that needs to be considered. Because of the tailing current during IGBT turn-OFF, the turn-OFF losses of an IGBT are substantial. This serves as one of the main motivations for using the HyS. Ideally, the entire current tail would be under ZVS conditions in order to completely eliminate the switching losses originating from it. However, since the SiC MOSFET has a lower current rating than the IGBT and the current tail lasts for a relatively long time, this would put the SiC MOSFET chip under a large amount of stress and could at worst compromise the integrity of the die. Furthermore, the length of the delay will adversely affect the maximum achievable switching frequency, $f_{sw,max}$, of the HyS. These factors means that when choosing the length of t_2, there will be a trade-off between switching losses, SiC MOSFET die integrity, and $f_{sw,max}$. Figure 2.22 shows the relationship between the HyS switching losses, and the length of t_2. The figure shows that at a certain point, depending on the length of the current tail, there will be diminishing returns from increasing the delay. This inflection point is a natural choice for t_2, and the length of said delay can be adjusted accordingly if there are issues related to thermal development or switching speed [28].

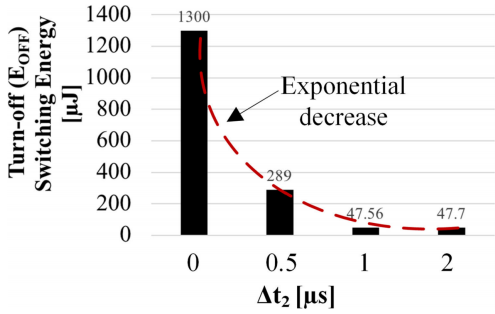


Figure 2.22: Turn-OFF losses as a function of turn-OFF delay time [28]

In [28], the improvement in switching performance has been quantified. The study used an IGBT with a voltage rating of 600 V and a current rating of 75 A, while the SiC MOSFET had a voltage rating of 650 A and a current rating of 29 A. Using $t_1 = 1$ µs and $t_2 = 1$ µs, the maximum possible switching frequency of a dc-dc converter using the HyS was determined relative to the maximum switching frequency of a dc-dc converter using only an IGBT. This means that the maximum switching frequency when using the HyS will be the switching frequency which results in the same losses as the dc-dc converter experiences when using the solo IGBT solution with a given switching frequency, in this case 20 kHz. The results can be seen in Figure 2.23. As the figure shows, the switching frequency of the converter can be notably increased by switching from the IGBT to the HyS. It is also worth noting that the maximum switching frequency decreases when the load current increases. This is presumably a consequence of the conduction loss that occurs in the SiC MOSFET during turn-ON and turn-OFF delays, since this loss would increase exponentially with the load current, and is larger than the conduction loss would have been if the IGBT was used.

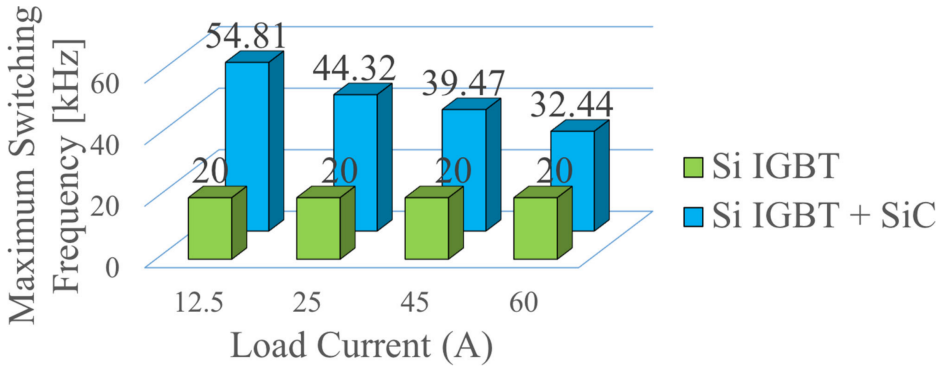


Figure 2.23: Maximum switching frequency of a dc-dc converter using the HyS, relative to a dc-dc converter using only an IGBT [28]

2.3.3 Thermal Considerations

One of the major design challenges tied to the HyS, is the previously mentioned trade-off between switching losses and the integrity of the SiC die. In Figure 2.24, the power profile of a SiC MOSFET used in a HyS configuration is shown. Notice the current level through the SiC die during the switching instances. During the turn-ON delay, t_1, and the turn-OFF delay, t_2, large current transients are conducted through the SiC MOSFET die. This leads to a pulsed power dissipation at these intervals, and in the worst case the power dissipation may be large enough for the SiC MOSFET's junction temperature to exceed its recommended maximum value. By exceeding this upper bound, the SiC MOSFET might degrade, and its reliability for use in the long term will be compromised. This problem is a direct consequence of using a SiC MOSFET with a lower current rating than the IGBT, which is a necessity for cost reasons. As such, a new optimization problem is introduced: Keeping the ratio, c_i, from (2.7) as low as permissible while still keeping the junction temperature of the SiC MOSFET at acceptable levels [28, 29].

$$c_i = \frac{I_{N,MOSFET}}{I_{N,IGBT}} \tag{2.7}$$

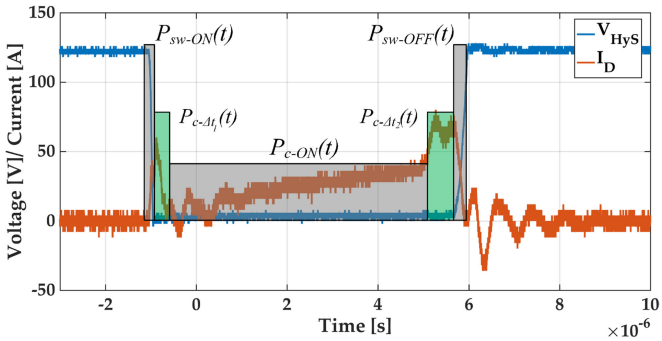


Figure 2.24: Power profile of SiC MOSFET using gate control option 3 [28]

In [27, 28], an optimization algorithm for this problem is introduced. The algorithm is shown in Figure 2.25. In short, a set of HyS configurations, starting with HyS-1, with descending c_i is prepared. The power profile is then extracted, and run through a thermal simulation using a Cauer model. If the junction temperature of the SiC MOSFET exceeds its maximum value when using the nth HyS set, the iterative process is terminated, and the c_i is finalized using the (n-1)th HyS set.

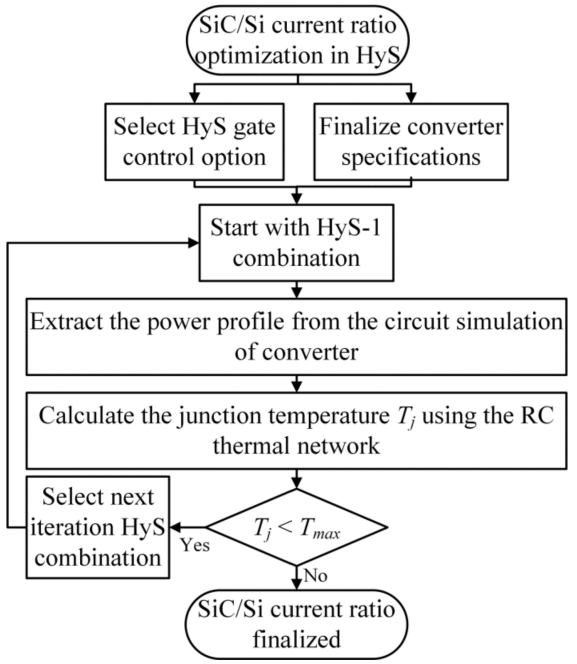
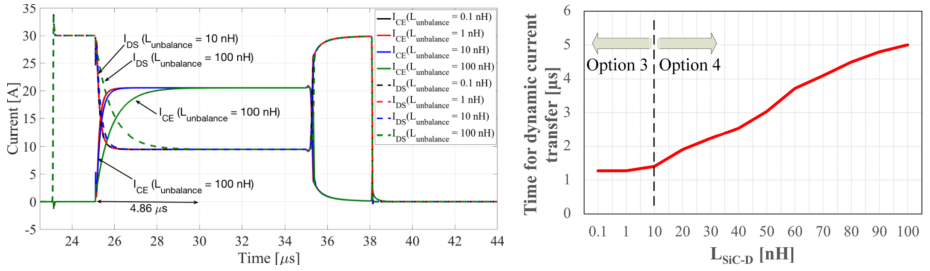


Figure 2.25: Current ratio optimization algorithm [28]

An added complication to the thermal management of the HyS is the detrimental effect of parasitic interconnect inductance. These are the stray inductances that form as a result of the interconnections between the IGBT and the SiC MOSFET. As shown by Figure 2.26, increased stray inductance imbalance between the two devices leads to an increase in the time it takes for the current to commutate between the SiC MOSFET and the IGBT when the IGBT is turned on. This leads to further stress on the SiC MOSFET die, which in turn will limit the potential of the HyS in terms of increasing switching frequency. In order to maintain the integrity of the SiC MOSFET die, it is therefore essential to limit these inductances. This can be done using the techniques shown in subsection 2.2.2. However, if this does not suffice, an alternative can be to change from gate control option 3 to option 4, as seen in Figure 2.20. This will help maintain the integrity of the SiC MOSFET die in exchange for increased switching losses during turn-ON. Figure 2.26b proposes that the change in strategy should occur when the inductance imbalance exceeds 10 nH, which implies that using option 3 is nonviable if using discrete components or off-the-shelf packaging units. Finally, it is worth pointing out that these issues are aggravated when paralleling multiple SiC MOSFET dice in order to increase current rating. Mainly, if there is an inductance imbalance between the SiC MOSFETs, this will lead to imbalanced current sharing. As a consequence, some SiC MOSFET dice will be stressed more than necessary. This translates to an increased requirement for a symmetrical lay-out of the paralleled SiC MOSFETs, as assymetry leads to inductance imbalance [28, 30].



(a) Current curves illustrating effect of stray inductance **(b)** Commutation time as a function of $L_{SiC,D}$

Figure 2.26: The effect of parasitic interconnect inductance between IGBT and SiC MOSFET [28]

As a final note, the thermal management of the HyS can be greatly enhanced by choosing an appropriate control strategy. For example, while it is common to control a converter using semiconductor switches with the goal being to maximize efficiency, which for the HyS is described by (2.8), this can lead to excessive temperature development in the SiC MOSFET since the temperature of the die is not taken into account.

$$\eta(t_1, t_2) = \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{loss,switch}}(t_1, t_2) + P_{\text{loss,others}}} \tag{2.8}$$

Therefore, [29] proposed the thermal balance control mode. When using this control strategy, the goal is to achieve the same temperature in the IGBT and SiC MOSFET. In simple terms, this strategy aims to use the IGBT as a heat sink for the MOSFET, so that the thermal development in the HyS will be optimally distributed. This can be easily achieved by taking advantage of the relation shown in (2.9), where $R_{th,jc,MOSFET}$ and $R_{th,jc,IGBT}$ is the thermal resistance from junction to case for the SiC MOSFET and the IGBT respectively. Simply, by keeping the ratio of power losses at this constant level, the temperature in the IGBT and the SiC MOSFET will be kept equal. The derivation of the relation is elaborated upon in [29].

$$\frac{P_{loss,IGBT}}{P_{loss,MOSFET}} = \frac{R_{th,jc,MOSFET}}{R_{th,jc,IGB)}} \tag{2.9}$$

Chapter 3

Modelling of the HyS

In order to properly assess the capabilities of the hybrid switch arrangement, a half-bridge circuit using the HyS will be simulated in PLECS. PLECS is a specialized simulation software for power electronic systems, which takes both electrical and thermal performance into account. However, before it is possible to conduct those simulations, several intermediary steps needs to be taken. First of all, PLECS uses idealized switching waveforms in its analysis, meaning that dynamic behaviour can not be analyzed using PLECS. This necessitates the use of several approximations based on data obtained from non-ideal models in order to ensure the viability of the results obtained from the PLECS simulations. Therefore, accurate, non-ideal models of the IGBT and SiC MOSFET are needed. These models will then be used to determine how the IGBT and SiC MOSFET interacts in the HyS configuration, which in turn will help inform how these interactions can be approximated in PLECS.

In this chapter, the different methods used in order to obtain the results shown in chapter 4 will be detailed step by step in a way that is conducive to replication of the entire process. The chapter is divided into three sections, the first covering the the power transistor modelling, the second covering the simulations of the HyS using the non-ideal power transistor models, and the final section will cover the electrical and thermal analysis of a half-bridge circuit containing the HyS in PLECS.

The foundation for every model and circuit used in this thesis is a high-power, three-phase AC/DC converter that Siemens uses between its battery bank and motor drives. The converter uses IGBTs as switches, and it is these IGBTs which have been envisioned to be replaced by the HyS. For simplicity's sake, the ratings of the IGBT and its anti-parallel diode will remain unchanged, and the only difference will be connecting the auxiliary SiC MOSFETs in parallel to the preexisting IGBTs. The specifications of the converter are as follows:

- DC-link voltage: $V_{DC} = 1000$ V

- Output voltage: $V_{out} \in [-1000, 1000]$ V
- Load current: $I_{load} \in [-2000, 2000]$ A
- Switching frequency: $f_{sw} \in [2, 3]$ kHz

3.1 Power Transistor Modelling

The first step of the thesis was to create accurate models for both the IGBT and the SiC MOSFET. The goal when designing these models was to provide an accurate simulation of particularly these three aspects:

- **The IV-characteristic of both transistors.** This is necessary, as it is important to obtain an accurate assessment of the current sharing between the IGBT and SiC MOSFETs. Specifically, it is important to know how much of the current is conducted through the SiC MOSFETs for a given load current.
- **The current tail of the IGBT.** In order to properly gauge how long t_2 needs to be, the current tail needs to be properly modelled. This is important because of the trade-offs involved when choosing the turn-OFF delay, as mentioned in subsection 2.3.2.
- **The switching losses of the SiC MOSFET.** Since the SiC MOSFET takes care of the hard switching actions, it is important that the switching losses and switching waveforms are properly modelled. Will be especially helpful when investigating how much stray inductance affects switching losses.

Notably, the turn-ON losses of the IGBT are completely absent in this list (turn-OFF losses are tied to the current tail). This is because the HyS used gate control option 3, shown in Figure 2.20. Using this option means that the turn-ON losses are almost completely eliminated. Because of this, accurately modelling the turn-ON losses of the IGBT was deemed of secondary importance compared to the other aspects that were outlined above. It is worth noting, however, that there is a benefit of accurately modelling the IGBT turn-ON loss, since the choice of t_1 is dependent on the voltage fall time of the IGBT. The reason this was not considered as important as the current tail, is that the voltage fall is mostly dependent on the SiC MOSFETs, since they are responsible for the hard switching actions. Therefore, t_1 is not directly dependent on the turn-ON waveforms of the IGBT, unlike how the length of t_2 is directly correlated with the length of the IGBT's turn-OFF waveforms.

In order to create an accurate model of the respective power transistors, they needed to be based on real components. The IGBT used by Siemens in their converter is the *FZ3600R17HP4_B2* by Infineon [31]. This is an IGBT module with three IGBT chips in parallel with one anti-parallel diode for each chip, and has a voltage rating of $V_N = 1700$ V and a current rating of $I_N = 3600$ A. However, because the datasheet of the *FZ3600R17HP4_B2* lacks important information, specifically the capacitance curves which are needed in order to accurately model the switching waveforms, it will not be used as the foundation of the IGBT model. Instead, the *5SNA 3600E170300* from ABB [32] will be used because of its almost identical nature to the *FZ3600R17HP4_B2*, while its datasheet,

seen in section A.2, contained the necessary information to create an accurate model. For the SiC MOSFET, the priority when choosing the component was a large current rating, since the system outlined above needs to be able to conduct large amounts of current. Therefore, the *C2M0045170P* from Wolfspeed [33] will be used as the foundation for the SiC MOSFET model. It has the largest current rating, at 72 A, of any SiC MOSFET in the 1700 V voltage class, while also having a datasheet, seen in section A.1, containing all the necessary information to create an accurate model. The most important parameters of the two components are compiled in Table 3.1.

Parameter	5SNA 3600E170300	C2M0045170P
V_N	1700 V	1700 V
I_N	3600 A	72 A
$R_{DS(on)}$	-	45 mΩ
$V_{CE(sat)}$	2.5 V	-
$T_{J,max}$	175	150

Table 3.1: Selected parameters of the chosen power transistors

It was decided to use the Simscape toolbox in Simulink to model the power transistors. This toolbox allows for the modelling of non-ideal semiconductor components using only information found in their datasheet, which sacrifices some accuracy for accessibility. Because of the simplicity of modelling power transistors in Simscape, using it was seen as an acceptable compromise to using more sophisticated software.

To model the IGBT the ”N-Channel IGBT” block [34] from the Simscape library was used. Using this block, the IGBT can be described by two different modeling variants: Full I-V and capacitance characteristics variant, which is suitable for simulating detailed switching characteristics, and the Simplified I-V characteristics and event-based timing variant, which is suitable when approximate dynamic characteristics are sufficient (see [34] for an elaboration of these two model types). The modelling variant that was used in this thesis is the full I-V and capacitance characteristics variant. Furthermore, this variant provides two ways to model the IGBT; either as an equivalent circuit of a PNP BJT and a N-channel MOSFET, as seen in Figure 3.1, or by using a look-up table. This thesis used the equivalent circuit method, as it was believed that it would provide the highest model fidelity.

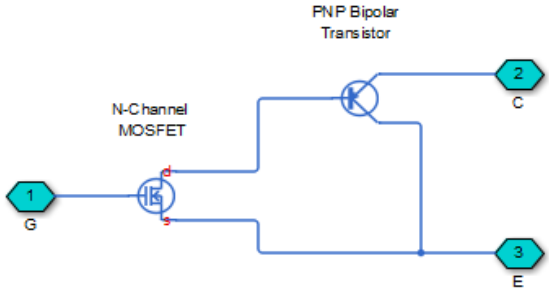


Figure 3.1: Equivalent circuit of the "N-Channel IGBT" block in Simscape [34]

To model the SiC MOSFET the "N-Channel MOSFET" block [35] from the Simscape library was used. This block can describe the MOSFET using either a threshold-based model, which is a basic model representing the MOSFET using the Shichman and Hodges equations, or a surface-potential-based model, which uses a simplified version of the world-standard PSP model (see [35] for an elaboration on these two model types). Even though the surface-potential-based model gives the highest model fidelity, it was not used because the model required information only possible to obtain if a physical die of the SiC MOSFET was available. This was not the case for this thesis, and therefore the threshold-based model had to be used.

Next, the process of refining the conduction- and switching characteristics of the IGBT and SiC MOSFET model will be described in detail.

3.1.1 Conduction Characteristics

As was briefly stated in the opening of this section, the goal when designing the conduction characteristics of the IGBT and the SiC MOSFET was to ensure that the current sharing between the two transistors when used in a HyS configuration would be representative of a realized module. Since the IV-characteristics of the two transistors are different, as seen in Figure 2.8, there will not be a uniform current sharing, and the ratio of current through the devices will change depending on the load current level. Therefore, the current sharing between the devices can not be predicted using simple ohmic calculations, and this necessitates the use of simulations. By ensuring that the current sharing was correctly modelled, it would also make sure that the SiC MOSFET received the correct load during steady-state conduction, which was important for the thermal analysis that was conducted in PLECS later.

IGBT

The IV-characteristics of the IGBT were defined using the "Fundamental non-linear equations" option, which is the option that uses the equivalent circuit description. Furthermore, temperature dependence was added to the model, and is described using the "Specify Ices and Vces(sat) at second measurement temperature" option. The parameters that were used

to form the shape of the IV-curves, and their chosen values, can be seen in subsection B.1.1. What each and every parameter means, and their effect on the behaviour of the IGBT model is elaborated upon in [34]. In short, the parameters that needed to be input to the "N-Channel IGBT" block can be divided into two categories: Parameters that can be extracted from the IGBT datasheet, which covers the parameters from the "Main" tab, seen in Table B.1, and some of the parameters from the "Temperature dependence" tab, seen in Table B.4, and parameters that were used to fine tune the shape of the IGBT IV-curves, which covers the parameters from the "Advanced" tab, seen in Table B.3 and the "XTI" and "BEX" parameters from the "Temperature dependence" tab. The parameters that were extracted from the datasheet in general used the value denoted as "typical" if multiple values where presented for the same parameter, and if only the "max" and "minimum" values were available, then the average of these extremes was used instead.

After extracting the necessary parameters from the IGBT's datasheet, the IV-curves of the IGBT needed to be fine-tuned so that conduction could be simulated as accurately as possibe. This was done using the "IGBT Characteristics" circuit [36] in Simscape, which allows for the generation of IV-curves for different values of gate-emitter voltages. The circuit can be seen in Figure B.1 from subsection B.1.1, and the script used to generate the curves can be seen in subsection C.1.1. In order to ensure the accuracy of the IV-curves of the IGBT aligned with the actual IV-curves of the device, voltage and current vectors were extracted from the IV-curves in the datasheet, see Fig. 1 on page 5 of the IGBT datasheet. In total, three pairs of vectors were extracted, one pair for the IV-curve at 25 °C, one for 125 °C, and one for 150 °C. The curves generated from the "IGBT Characteristics" circuit was then compared to the points formed from these vector pairs. If the generated curves did not match up with the vector points in a satisfactory manner, the parameters from the "Advanced" and "Temperature dependence" tabs where adjusted accordingly. The parameters from the "Advanced" tab were used to obtain the correct shape of the curve, while the "Temperature dependence" parameters were adjusted in order to obtain the correct relationship between the IV-characteristics and temperature. Since the only gate-emitter voltage that was used in this thesis was $V_{ge} = 15$ V, that was the only gate-emitter voltage level which the IV-curves were optimally modelled for. The finalized IV-characteristic of the IGBT model can be seen in Figure 4.1.

SiC MOSFET

The modelling of the conduction characteristics of the SiC MOSFET was very similar to how it was performed with the IGBT. The characteristics were defined using the "Specify from datasheet" option, and temperature dependence was described using the "Model temperature dependence option". The parameters which were used to shape the IV-curves of the SiC MOSFET can be seen in subsection B.1.1. The meaning of the different parameters is explained in [35]. The IV-curves of the SiC MOSFET model were verified in a similar way to the IGBT model: Using the "MOSFET Characteristics" circuit [37] in Simscape, and comparing the curves it generates with vector pairs extracted from the SiC MOSFETs datasheet. The circuit can be seen in Figure B.2 and the script used to generate the curves is shown in subsection C.1.1.

The parameters used to form IV-curves was the "Main" parameters, seen in Table B.5, and

the ”Temperature dependence” parameters, seen in Table B.7. The parameters from the ”Ohmic Resistance” and the ”Body Diode” tabs were kept at their default values, since they should not affect the simulations in any meaningful way. Notably, the MOSFFET model does not use any parameters similar to the ones in the ”Advanced” tab of the IGBT model. Therefore, in order to fine tune the shape of the MOSFET IV-curves, the parameters extracted from the SiC MOSFET datasheet were adjusted (within the min-max interval shown in the datasheet) in order to obtain a satisfactory IV-curve. Then the temperature dependency was modelled in the exact same way as with the IGBT. The finalized IV-characteristics of the SiC MOSFET model can be seen in Figure 4.2.

3.1.2 Switching characteristics

In order to properly assess the switching performance of the power transistor models, a double-pulse test (DPT) circuit was made in Simscape. In a DPT, the switching energy of a power transistor can be measured by sending a double-pulse signal at the gate of the device in question, which will cause the device to turn off when the first pulse is finished, and then turn on when the second pulse initiates. The circuit can be seen in Figure B.4. It was based on the circuit in shown Figure 29b on page 8 of the SiC MOSFET's datasheet. The circuit contained a voltage source supplying the circuit, and a free-wheeling diode in parallel with a load inductor. There is also a gate-driver block, which depending on the supplied control signal, supplies the desired gate voltage at turn-ON and turn-OFF. The gate driver block is also where the turn-ON and turn-OFF gate resistors are chosen. Finally, all of the current and voltage signals generated by this circuit is sent to the device under test (D.U.T.). There is also a stray inductance at the drain/collector, which was used depending on the stray inductance levels stated in the datasheet.

To achieve the desired current value through the D.U.T., the inductor equation, seen in (3.1), was used.

$$v = L\frac{di}{dt} \tag{3.1a}$$

$$\implies \Delta I = \frac{V\Delta t}{L} \tag{3.1b}$$

As the equation implies, if the voltage and inductance levels are kept constant, the current level can then be determined by changing the duration of the conduction period. This period is determined using the control signal. The control signal is constructed by summing two separate pulse signals, as illustrated by Figure 3.2. The length of *T2* will then determine the current level during the turn-OFF instance, and if *T3* is kept sufficiently short, the current level during the turn-ON instance will be approximately the same. In this way, it was possible to control at what current level the switching instances would be performed. This was essential when comparing the switching energy of the models to the values shown in the respective datasheets, since conducting the DPT at the same current and voltage levels as what was done in the datasheets would serve as a satisfactory comparative basis.

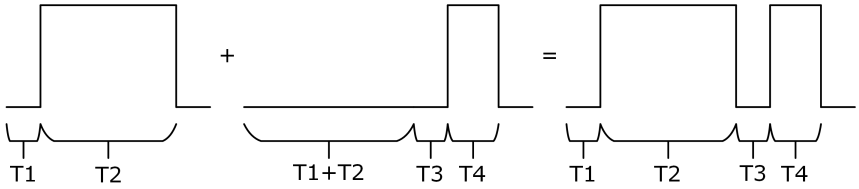


Figure 3.2: The construction of the double pulse signal

Figure B.3 shows the main system of the DPT model, in which the parameters for the test is chosen, the D.U.T. is chosen, and the necessary scopes for both waveforms and switching losses are available. The system worked by connecting the drain, source, and gate (or the equivalent) of the D.U.T. to their corresponding ports on the DPT circuit subsystem. The parameters were then chosen by entering the necessary data into the mask that was put on the DPT subsystem. The parameters in the mask, and their corresponding variables, can be seen in Table 3.2. Finally, the the voltage and current through the D.U.T. was extracted, and used to calculate the switching losses by continuously using (2.1), but where t_{ov} was replaced by the simulation time of the DPT model.

Before the running the DPT simulations, the switching behaviour of the two models needed to be modelled. Both the IGBT and the MOSFET block uses a similar charge model to describe their switching behaviour, and these models are described in [34] and [35] respectively. Both the IGBT and the MOSFET model used the "Specify tabulated input, reverse transfer and output capacitance" option in the "Junction Capacitance" tab, as this allowed for the most accurate description of the devices' capacitances. This option allows for the input of three capacitance vectors: C_{iss}; the input capacitance, C_{rss}; the reverse transfer capacitance, and C_{oss}; the output capacitance, which were mapped to a corresponding drain-source/collector-source voltage vector. These capacitances determined the switching speed of the IGBT and MOSFET models, and by mapping different capacitance values to different voltage levels, a more comprehensive picture of the dynamic behaviour of the power transistors was formed. The capacitance and voltage vectors needed for the model were extracted using Figure 17 and 18 on page 5 of the SiC MOSFET datasheet, and Fig. 9 on page 7 of the IGBT datasheet. The resulting capacitance vectors for the IGBT model can be seen in Table B.2, and the vectors for the SiC MOSFET model can be seen in Table B.6. One notable difference between the charge models of the IGBT and MOSFET, is that the IGBT model contains an extra parameter, referred to as "Total forward transit time". This is the parameter that was used to model the current tail of the IGBT. The value of this parameter could only be determined after conducting the DPT simulations, and therefore it will be discussed later in the subsection.

When the junction capacitance vectors were finalized, the DPT simulations could be conducted. The values of the parameters used in the DPT can be seen in Table 3.2. Most of the parameter values were based on the information provided by the two devices' datasheets. In that way, the DPT conducted by the manufacturers of the components could be replicated as accurately as possible. However, the inductance value used for the load inductor in the IGBT test was arbitrarily chosen, as was the length of $T1$ and $T4$, since these do not

affect the results of the DPT, while $T2$ and $T3$ was chosen in accordance with what was stated previously in the section. It is worth noting that when simulating the DPT of the SiC MOSFET model, an almost instantaneous current jump of 12 A occurs. This means that the actual length of $T2$ in the SiC MOSFET case is reduced to 3.325 µs in order to account for this current jump. Finally, the choice of the free-wheeling diode is also important in order to accurately compare the models to the actual components. The diode used for the SiC MOSFET test is the same as the one shown in the datasheet, the *C3D25170H* [38]. For the IGBT diode, however, the datasheet does not specify the exact diode model used in the test. It was therefore assumed that the diode that was used was the *5SLA 3600E170300* [32], as it is the only ABB diode module with the exact same ratings as the *5SNA 3600E170300* IGBT module. Both of these diode models were made using the "Diode" block [39] from the Simscape library. In both instances, the exponential model was used, and was parameterized using two IV-curve points extracted from the datasheets of the respective diode components. Neither a breakdown model, nor a capacitance model was used, since it was decided that only the conduction characteristics of the diode models would play a role in the results of the DPT simulations.

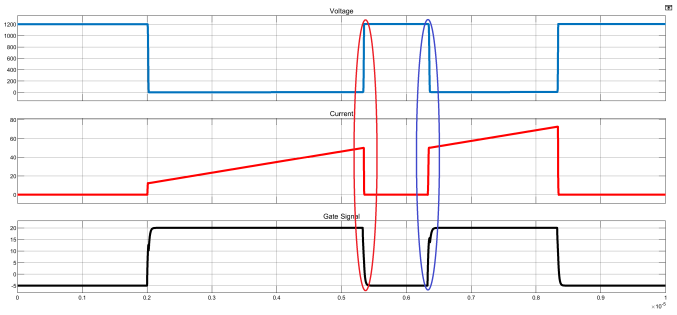
Parameters	**Variable**	**IGBT**	**SiC MOSFET**
Input Voltage [V]	V_dc	900	1200
Turn-ON Gate Resistor [Ω]	RG_ON	0.6	1.3+2.5
Turn-OFF Gate Resistor [Ω]	RG_OFF	0.6	2.5
ON-state gate voltage [V]	Vg_ON	15	20
OFF-state gate voltage [V]	Vg_OFF	-15	-5
Inductor value [µH]	L	50	105
Start, pulse 1 [µs]	T1	2	2
Length of pulse 1 [µs]	T2	200	4.375
Time between pulse 1 and 2 [µs]	T3	20	1
Length of pulse 2 [µs]	T4	20	2

Table 3.2: Parameters of double-pulse test

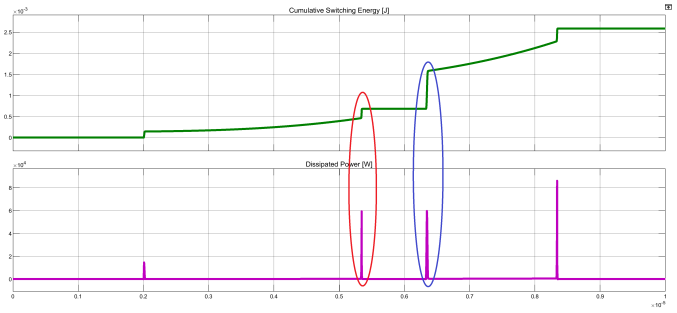
When the DPT simulations where conducted, they were conducted for several different temperature to allow for a comprehensive comparison with the datasheet values. For the IGBT model the simulation was run for 25 °C, 125 °C, and 150 °C, while for the SiC MOSFET model the simulation was run for 25 °C and 150 °C. For each of these simulations the switching waveform curves and the switching loss curves were recorded. An example of these curves can be seen in Figure 3.3. The blue curve shows the voltage across the D.U.T., the red curve shows the current through the D.U.T., the black curve shows the gate voltage supplied to the D.U.T., the green curve shows the D.U.T.'s cumulative switching losses, and the purple curve shows the D.U.T.'s instantaneous switching losses. The switching losses were then measured using the cursor option in the Simulink scope, where the instantaneous switching loss curve was used to help line up the cursors as accurately as possible by indicating when the switching event had started and ended. The resulting switching losses of the SiC MOSFET compared to datasheet values can be seen in Fig-

ure 4.7, and the finalized switching waveforms of the SiC MOSFET model can be seen in Figure 4.6.

For the IGBT, however, the current tail still needed to be modelled. This was done by first measuring the current fall time of the IGBT model by measuring the time it takes for the IGBT's current to fall from 90 % of its peak value of 3600 A, to 10 % of its peak value, as is shown by Figure 2.9. This was done for 25 °C, 125 °C, and 150 °C, and the results can be seen in Figure 4.4. The fall time data was gathered to discern if the fall time of the IGBT was comparable to the fall times shown in the datasheet in order to determine if the length of the current tail of the IGBT model would be too long or too short in comparison to the current tail of the actual component. This was necessitated by the fact that figures of the actual waveforms of the IGBT was unavailable, meaning that the length of the current tail of the IGBT model had to be estimated based on switching losses. In order to determine the size of the "Total forward transit time", the switching losses of the IGBT model at 150 °C were calculated, and then the transit time was adjusted accordingly until the turn-OFF energy of the IGBT model matched the turn-OFF energy in the datasheet for the same temperature. In the end, the length of the "Total forward transit time" ended up being 4.25 ns, as seen in Table B.2. The switching energy of the finalized IGBT model can be seen in Figure 4.5, and the finalized switching waveforms of the IGBT model can be seen in Figure 4.3.



(a) Switching waveforms



(b) Switching Losses

Figure 3.3: Example MOSFET model's switching waveforms and switching loss curve. The red oval denotes turn-OFF, while the blue oval denotes turn-ON

3.2 Electrical Simulations

The next step of the thesis was to put together the finalized models of the IGBT and SiC MOSFET in an HyS configuration. The goal of this part was to determine how the IGBT and SiC MOSFET interacted with one another, especially during switching instances. All of the findings from this part were used in order to make the simulations using PLECS as accurate as possible, and the following three aspects were of particular interest, since they would have a large impact on the thermal performance of the system:

- Determine how current is shared between the power transistors.
- Determine the optimal duration of t_2.
- Determine the consequences of stray inductance on the performance of the Hys.

The section is divided into two subsections. The first subsections will investigate the behaviour of the HyS without stray inductance, while the second subsections introduces stray inductance into the mix. In both subsections, the obtained results will be used to calculate approximations of the behaviour of the HyS that will enable that behaviour to be emulated in PLECS.

3.2.1 Without stray inductance

As when testing the individual power transistor models, a DPT circuit was used in order to test the HyS. The HyS DPT circuit was more or less the same as the DPT circuit used for the individual transistors, and can be seen in Figure B.5 to Figure B.8 in subsection B.1.2. As the figures shows, there were a couple of differences, however. First, since the HyS consists of two switching cells; the IGBT and the SiC MOSFET switching cell, switching losses were calculated for the individual switching cells, in a similar manner to what was shown in Figure 3.3, and then summed together retroactively. Using this approach allows for the study of how each constituent component of the HyS behaved for a given set of operating conditions, instead of treating the entire HyS as a black box. Furthermore, the introduction of the HyS required the addition of two new subsystems: The HyS subsystem, and the SiC MOSFET cell subsystem. The former contained the HyS, with all of its constituent components, its gate drivers, and the necessary measurement sensors. The latter was a subsystem within the HyS subsystem, and contained a parallel connection of up to 20 SiC MOSFET models, which was necessary in order to reach an acceptable current rating. In the Simscape model, each SiC MOSFET block had its own gate driver block. Although this is not something that would be feasible in an actual module, this approach was used in order to ensure that the correct gate resistance was present for every SiC MOSFET, and to ensure that the total gate resistance would be automatically adjusted when adding or removing MOSFETs from the cell. This would not be the case when using a single gate driver, since the gate resistance in this driver would have to be the equivalent gate resistance of all of the MOSFETs in order to achieve the same switching speed. Thus, it would have been necessary to manually recalculate the gate resistance every time the number of MOSFETs in parallel was changed. In short, one gate driver per SiC MOSFET model was used because it streamlined the process of adding or removing

further MOSFETs, which was necessary for assessing the behaviour of the steady-state conduction of the HyS.

Before the simulations of the HyS could begin, the turn-ON and turn-OFF delays needed to be incorporated into the control signals. This was done using two parameters in the timing tab of the gate driver block: In the IGBT gate driver, the "Propagation delay (logic $0 \rightarrow$ logic 1)" parameter was used to introduce the turn-ON delay, while the "Propagation delay (logic $1 \rightarrow$ logic 0)" option was used in the SiC MOSFET gate driver blocks to introduce the turn-OFF delay. These parameters works by delaying the gate driver signal by the specified amount after the control signal changes from 0 to 1 or from 1 to 0, for turn-ON and turn-OFF respectively. In this way, the control signal that was used in the previous DPT circuit could be recycled with only one minor alteration: t_2 needed to be subtracted from T2 in order to achieve the desired current level during turn-OFF. With the switching delays incorporated, the simulations could begin. Because of the large amount of parameters that needed to be adjusted in the HyS subsystem, a mask was designed for this system in addition to the mask that was designed for the DPT circuit subsystem. The parameters of the DPT mask and their final values can be seen in Table 3.3, while the parameters of the HyS mask and their final values can be seen in Table 3.4.

The first part of the HyS DPT simulations was to determine the current sharing between the IGBT and the SiC MOSFET cell for a certain load current. The load current was chosen as 2000 A, since that is the maximum load current used in Siemens' converter. The temperature level used for this test was 150 °C, since it was hypothesized that the temperature of the power transistors would be quite high as a result of the large current levels and high switching frequencies used in the thermal simulations. Thus, determining the current sharing at high-temperature would allow for the most realistic assessment when conducting the thermal simulations. After establishing the initial conditions, the DPT simulation was started, and when the IGBT turn-OFF occurred the simulation was stopped, since this is the moment the current would have reached the desired level. The current through the entire SiC MOSFET cell was then measured, and this result was then used to determine the ratio between the current through the IGBT and the current through the SiC MOSFET cell for the given load current. This was then repeated while changing the number of MOSFETs in the SiC MOSFET cell, where the first test used 20, then the following tests used 15, 10, and 5, respectively. The results of these tests can be seen in Figure 4.8, which indicates that the relationship between the current through the SiC MOSFET cell and the number of MOSFETs in the cell is linear for a given load current level.

The second part of the HyS DPT simulations was to determine the duration of t_1 and t_2. Determining the duration of t_1 was simply done by measuring the time it took for the voltage to fall from peak to zero. This took approximately 80 ns, which lead to the choice seen in Table 3.3 and Table 3.4. Next, t_2 needed to be determined. However, as can be seen in Figure 3.4, an accidental turn-ON of the IGBT occured during the SiC MOSFET turn-ON, and this issue needed to be resolved before an optimal length of t_2 could be chosen. It was suspected that the accidental turn-OFF was the result of a voltage drop across the drain-gate capacitance, also known as the Miller capacitance, of the IGBT. As a result of the IGBT's high current rating, its gate capacitances are relatively large, and this

combined with the large $\frac{dv}{dt}$ enabled by the SiC MOSFETs would make the IGBT prone to accidental turn-ONs, as described in subsection 2.2.2. Consequently, it was attempted to emulate a Miller clamp, as shown in Figure 2.16, by significantly reducing the turn-OFF gate resistance of the IGBT. By reducing this resistance to 0.05 Ω, the accidental turn-OFF was eliminated. Nevertheless, there was still a small current pulse through the IGBT during SiC MOSFET turn-OFF, but this was not characterized as an accidental turn-ON since there was no current tail and no major losses occurred as a result of its presence.

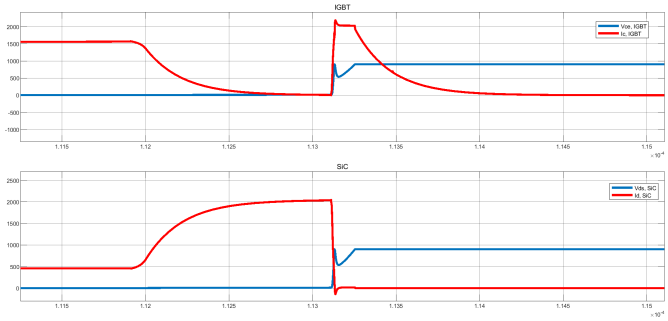
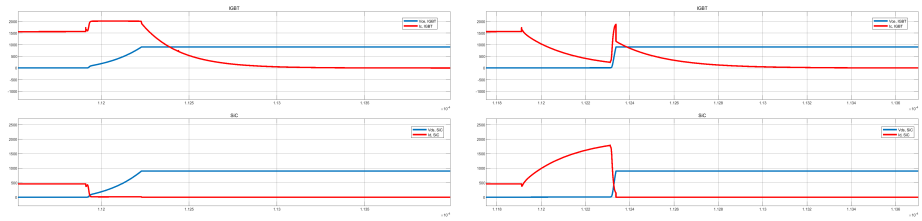


Figure 3.4: Accidental IGBT turn-ON during SiC MOSFET turn-OFF.

With the accidental turn-ON problem resolved, the duration of t_2 could finally be determined. In order to establish an unambiguous selection criterion for t_2, it was decided that the duration of t_2 would be the same as the inflection point mentioned in subsection 2.3.2, i.e. the point where increasing t_2 no longer leads to a decrease in the total turn-OFF energy. The process to determine this inflection point involved simulating a DPT for the HyS with a given duration to t_2. The switching losses from the DPT were then recorded, a new duration to t_2 was chosen, and the steps were repeated. This was done until it was certain that the total switching energy no longer decreased, and the inflection point could be determined with certainty. In Figure 3.5, the effect of increasing t_2 is illustrated. When conducting the tests, the initial DPT used $t_2 = 0$ µs, and then increased t_2 by an increment of 0.4 µs for each iteration. This was done until 2.4 µs had been reached, since it was at this point it was decided that the inflection point had been identified with certainty. The results of the tests can be seen in Figure 4.9.



(a) $t_1 = 0$ µs **(b)** $t_1 = 0.4$ µs

Figure 3.5: Example showing the difference between two turn-OFF delay lenghts

Parameter	Variable	Value
Input voltage [V]	Vdc	900
Inductor value [µH]	L	50
Start, pulse 1 [µs]	T1	2
Length of pulse 1 [µs]	T2	111.1111
Time between pulse 1 and 2 [µs]	T3	10
Length of pulse 2 [µs]	T4	20
Turn-ON delay [µs]	t1	1.2
Turn-OFF delay [µs]	t2	0.1

Table 3.3: Every parameter and their final values in the DPT circuit mask of the HyS DPT model

Parameter	Variable	Value
ON-state gate resistor, SiC [Ω]	RG_ON_SiC	1.3+2.5
OFF-state gate resistor, SiC [Ω]	RG_OFF_SiC	1.3+2.5
ON-state gate voltage, SiC [V]	Vg_ON_SiC	20
OFF-state gate voltage, SiC [V]	Vg_OFF_SiC	-5
ON-state gate resistor, IGBT [Ω]	RG_ON_IGBT	0.6
OFF-state gate resistor, IGBT [Ω]	RG_OFF_IGBT	0.05
ON-state gate voltage, IGBT [V]	Vg_ON_IGBT	15
OFF-state gate voltage, IGBT [V]	Vg_OFF_IGBT	-15
Turn-ON delay [µs]	t1	1.2
Turn-OFF delay [µs]	t2	0.1
Device temperature [°C]	T_HyS	150

Table 3.4: Every parameter and their final values in the HyS mask of the HyS DPT model

3.2.2 With stray inductance

The final part of simulating in Simscape was to introduce the stray inductances to the circuit. These inductances were initially introduced to the circuit in the manner that is shown in Figure 3.6. In addition, an inductance was placed between the gate driver and the gate of every transistor in the model. However, when trying to simulate the circuit after adding the inductances the model would not converge, and the simulation was always cancelled exactly at the start of the first pulse. It was identified that it was specifically a problem related to the IGBT, and if an inductance was not placed in series with the IGBT, the model would converge. It was suspected that the reason for this was tied to how the IGBT was modelled. As mentioned in section 3.1, the IGBT was modelled as an equivalent circuit of a MOSFET and a BJT. In [40], the model of the PNP BJT is described, and it explains that two current controlled current sources is used in the modelling, one source at the collector and one at the emitter. Moreover, as is explained in [41], if a current source is connected in series with an inductor, it results in Index-2 differential algebraic equations (DAEs). These DAEs slow down the simulation significantly, and might prevent a model

from converging. A possible solution to this problem was to introduce a small parasitc resistance to the inductor, but this did not help resolve the convergence issues. In the end, after much trial and error with no solution, it was decided that the only way to solve the problem was to replace the IGBT model with an ideal IGBT. This was deemed acceptable since the switching losses of the IGBT would be close to negligible anyway, and it was the behaviour of the SiC MOSFET that was of interest. Specifically, the objective was to determine by how much the switching losses of the SiC MOSFET increased, as well as how much longer the current commutation from the SiC MOSFET cell to the IGBT during IGBT turn-ON would take when adding the stray inductance.

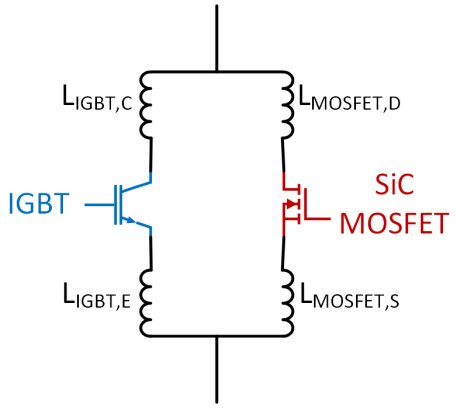


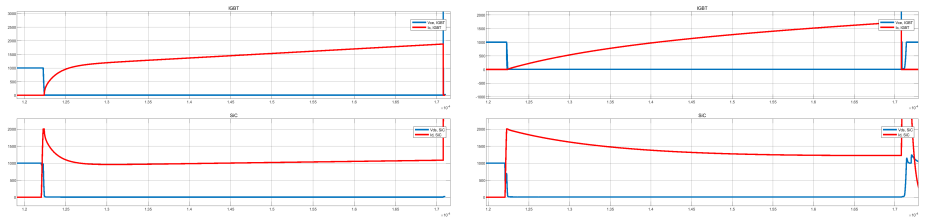
Figure 3.6: Interconnect inductance in the HyS

Unfortunately, even with this change, there were still some convergence issues present. At first, these issues were lessened slightly by removing the stray inductances from the emitter and source, respectively. This allowed the simulation to continue past the point it was cancelled previously, which made it possible to observe large oscillations with an extremely high frequency in the voltage and current waveforms of both the IGBT and the SiC MOSFETs during turn-OFF. However, the simulation was cancelled once again due to convergence issues before being able to complete the turn-OFF action. It was suspected that the high frequency of the oscillations caused numerical issues in the model, and that the oscillations were the result of an RLC circuit forming between the collector/drain, and the gate of the respective power transistors. Consequently, the oscillations could be dampened by increasing the R component in the RLC circuit, which in this case was the gate resistance of the switches. By increasing the gate resistor from their original level, shown in Table 3.4, to about 300 Ω, the circuit finally converged. The final circuit used when simulating the DPT of the HyS with stray inductance included can be seen in Figure B.9 and Figure B.10.

Although it was finally possible to complete a full simulation of the DPT with stray inductance, this came at a price of large switching losses for the SiC MOSFETs. These losses were in the range of 70 mJ per MOSFET when using 20 in parallel, with almost 50 mJ originating from the turn-OFF action, which lead to a total switching loss of ap-

proximately 1400 mJ when using a voltage level of 1000 V and a current level of 2000 A. However, the change in gate resistance was not the only reason for this increase, as using the large gate resistances without stray inductance present only lead to a switching loss of approximately 25 mJ per MOSFET, with only 5 mJ originating from turn-OFF. This shows that introducing stray inductance more than doubles the switching losses of the MOSFET model, and increases the turn-OFF energy by an entire order of magnitude. Even more peculiar, when increasing the stray inductance from 10 nH to 50 nH, the switching losses only increased by a couple of mJ, which implies that it is only the presence of stray inductance that leads to this significant increase, more or less independent of the actual amount of inductance that is introduced. This was considered unrealistic, both because of the odd behaviour of the model, and because these losses are more or less the same as the losses when using a solo IGBT at the same conditions. It was therefore concluded that it would not be possible to accurately calculate the switching losses of the SiC MOSFET whit stray inductance present in the model when using Simscape. Consequently, this objective had to be dropped. Even though the inability to extract the switching losses for the SiC MOSFET as a function of stray inductance was nonoptimal, it could be partly rectified by using the the PLECS models provided by the manufacturers of the IGBT and SiC MOSFET components. This will be elaborated upon in the next section

Even with the poor representation of the switching losses of the SiC MOSFET, the DPT simulations were still able to investigate the relationship between stray inductance and the commutation time during turn-ON. Since the current commutation between the SiC MOSFET cell and the IGBT is a passive process, the size of the gate resistors would not affect it. In order to measure the commutation time, T4 was increased to 50 µs to ensure that the entire commutation interval was included in the simulation. The stray inductance level was then chosen, were $L_\sigma = L_{IGBT,C} + L_{MOSFET,D}$, and the simulation of the DPT was started. Examples of the resulting waveforms can be seen in Figure 3.7. An important note about the stray inductances is that the commutation loop stray inductance was always spread evenly between the collector and drain stray inductances, meaning that there was no inductance imbalance. This was done because no difference in the current waveforms was observed if there was an inductance imbalance, as long as the sum of the inductances stayed at the same level.



(a) $L_\sigma = 10$ nH **(b)** $L_\sigma = 100$ nH

Figure 3.7: Example showing the difference between the current commutation time when changing the level of stray inductance

In order to measure the commutation time, the SiC MOSFET current was used. The

length of the commutation time, T_d, was then defined to be from the current peak of 2 kA, to 90 % of the total current change, ΔI, had occurred. The power loss resulting from the commutation interval was then approximated as a triangle, as seen on the left side of Figure 3.8. In the figure, the red stapled line signifies the actual current waveform of the SiC MOSFET. As can be seen, the triangle slightly overestimates the area under the curve. But by measuring the length of T_d in the way described above, this overestimation could be corrected slightly. A problem that occurred during these simulations was that using the ideal IGBT meant that the current sharing was no longer accurately modelled. As a consequence, ΔI did not equal 1540 A, as it would have if using the IGBT model. In order to correct for this, assuming that the triangle approximation was accurate, triangle similarity was used, as seen in (3.2). In this equation, T_d' is the corrected length of the commutation time, and $\Delta I'$ is equal to 1540 A. In short, T_d' represents what the measured commutation time would have been if the current sharing was correctly modelled.

$$T_d' = \frac{T_d}{\Delta I}\Delta I' \tag{3.2}$$

In order to introduce this commutation time into PLECS, where it would be important for the thermal simulations, it was modelled as an extra delay to the IGBT turn-ON. Since the switching waveforms used in PLECS are ideal, the current waveform during this delay would take the shape of a rectangle. In order to correct for the difference in the waveforms between Simscape and PLECS, the area of the triangle which was formed by T_d' and $\Delta I'$ was converted to a rectangle, as shown by the right side of Figure 3.8. Using this final conversion, the commutation time was measured and converted for $L_\sigma = 10$ nH, 30 nH, 50 nH, and 100 nH. The results can be seen in Figure 4.12, which indicates that the relationship between commutation time and commutation loop stray inductance is linear.

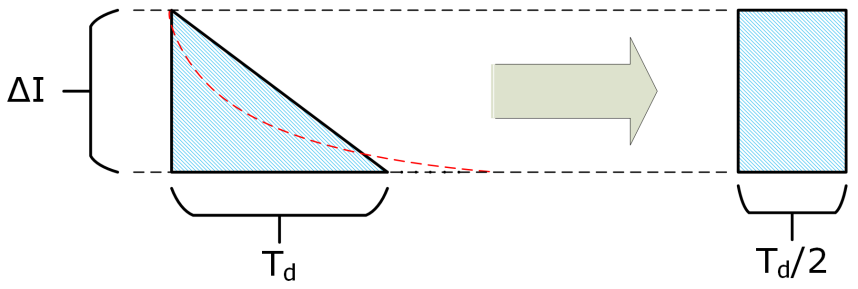


Figure 3.8: Approximation of the commutation time in a way that is compatible with PLECS

3.3 Thermal Simulations

With the Simscape simulations complete, the only remaining part of the thesis were the PLECS simulations. The goal of the PLECS simulations were to:

- Evaluate the HyS's performance in a converter setting to better emulate the conditions the HyS would experience in the three-phase converter used by Siemens.
- Determine by how much the maximum switching frequency of the converter can be increased by replacing a solo IGBT with the HyS, assuming the losses stay the same.
- Determine if the heat development in the SiC MOSFET will limit the maximum achievable switching frequency of the HyS for a given set of conditions.

In order to achieve the first goal, a half-bridge circuit with purely resistive load was built in PLECS. The completed circuit can be seen in Figure B.11 to Figure B.14. The most important part to note about the circuit is that it not only contains the electrical circuit for the half-bridge module, it also contains a thermal circuit. This circuit was necessary in order to determine the thermal performance of the HyS, and it was built using a Cauer network, as is described in subsection 2.2.1. The most important component to a thermal circuit in PLECS is the "Heat Sink" block, which according to its description "(...)absorbs the thermal losses dissipated by the components within its boundaries. At the same time, a heat sink defines an isotherm environment and propagates its temperature to the components it encloses" [42]. The only parameter of the heat sink is its thermal capacitance, which can be calculated using (3.3), where m is the mass of the heat sink, and c_p is the specific heat capacity of the heat sink.

$$C_{th} = mc_p \tag{3.3}$$

Siemens uses an 18 kg heat sink made out of aluminium, which has a $c_p = 921$ J/kgK [43]. Using (3.3), this gives a thermal capacitance of $C_{th} = 16580$ J/K. The heat sink was then connected to two thermal resistances, and a constant temperature with a thermal reference. The constant temperature represented the ambient temperature, and was be set to 298 K, or 25 °C, which was also the temperature which would be used as the initial temperature for all of the components in the circuit. The two thermal resistances represented the thermal resistance from the half-bridge module to the heat sink, $R_{th,ch}$, and the thermal resistance from the heat sink to ambient, $R_{th,ha}$, respectively. The potential values used for $R_{th,ch}$ was provided by Siemens, and can be seen in Table 3.5. These values all assume that the chips of the components in the half-bridge circuit are encapsulated within the same module, but the equivalent thermal resistance from cases to the heat sink was also calculated for when discrete components were used. This was calculated using the thermal resistance from case to ambient provided in the IGBT and SiC MOSFETs datasheets, assuming all of the thermal resistances were in parallel, and that there were 20 SiC MOSFETs in the SiC MOSFET switching cells. The value used for $R_{th,ha}$ was chosen based on the datasheet of the *SV-C215A-RG42080L32* [44], a heat sink designed for high-powered converters which employs forced air cooling. The heaviest version of this heat sink, sitting at 16.53 kg, has a thermal resistance of 0.0173 K/W. This was deemed as an acceptable approximation of the 18 kg heat sink used by Siemens, and therefore the thermal resistance from heat sink to ambient was chosen as $R_{th,ha} = 0.0173$ K/W.

Attach Material [-]	**$R_{th,ch}$ [K/kW]**
Pasta	6.3
Graphite	7
TIM	2.65
Discrete components	8.96

Table 3.5: The thermal resistance of different attach materials used by Siemens

As should be noticeable, the thermal resistance from junction to case was not included in the thermal circuit. This is because these resistances are included in the component models which are provided by the manufacturers. The PLECS model for the IGBT was retrieved from [32], while Wolfspeed provides PLECS models for all of their products at [45]. These models do not only contain the junction thermal resistances of the components, they also contain detailed look-up tables for turn-ON and turn-OFF losses, and conduction losses. Using these tables allows PLECS to calculate the losses for the components as a function of current, voltage and temperature, and the heat flow resulting from the dissipated power will then flow through the thermal network. Accordingly, using these models in conjunction with the half-bridge model allowed for the fulfilment of the final two goal of the PLECS simulations.

However, before the simulations could begin, some final details were ironed out. First of all, the switching waveforms of the HyS needed to be designed. Specifically, the turn-ON and turn-OFF delays, t_1 and t_2 had to be implemented. This was done using the "Pulse Delay" block on the SiC MOSFET gate signal, which delayed the entire SiC signal by $t_2 = 1.2$ µs. Then, the "Turn-ON Delay" block was used on the IGBT gate signal, which delayed the IGBT turn-ON by $t_1 + t_2 + T_L$. This resulted in the current waveforms seen in Figure 3.9.

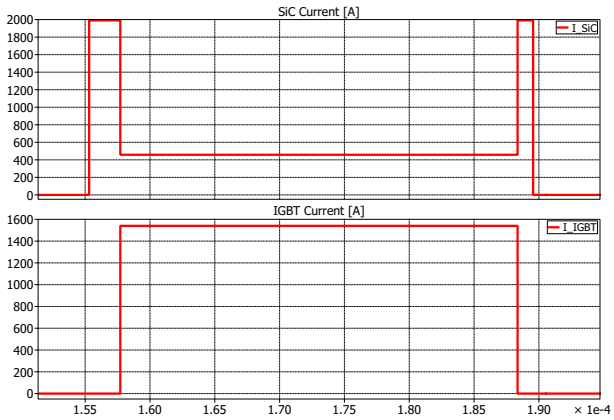


Figure 3.9: Current waveforms of the HyS components in PLECS

Next, the commutation delay needed to be properly modelled. The adjusted commutation time was denoted as T_L in the turn-ON delay, and it was found that the commutation time depends on the following variables: The load current, I_{Load}, the total commutation loop stray inductance, L_σ, and the number of SiC MOSFETs in parallel, N. An important assumption for these dependencies was the assumption that T_L is proportional to ΔI, as showcased by the triangle approximation used in Figure 3.8. This meant that if the load current was decreased, so would ΔI, and therefore T_L. Furthermore, since it was shown in Figure 4.8 that the relationship between the steady-state current through the SiC MOSFET cell and the number of SiC MOSFETs in parallel is linear, and that ΔI is the difference between load current and the steady-state current through the SiC MOSFET cell, it could be assumed that T_L is dependent on N. Finally, T_L was shown to be linearly proportional with L_σ by Figure 4.12. All of these dependencies were used together with triangle similarity to construct the equation shown in (3.4). This equation dynamically adjusts the commutation time according to the conditions used during the simulation. It was implemented into the PLECS model using the initialization script shown in subsection C.2.1.

$$T_L(I_{Load}, L_\sigma, N) = \left(\frac{T_D(L_\sigma)}{1540}\right) \cdot \left(I_{Load} - 460 \cdot \frac{20}{N}\right) \tag{3.4a}$$

$$T_D(L_\sigma) = T'_d/2 = 0.2377 \cdot L_\sigma - 0.0746 \tag{3.4b}$$

Finally, before starting the simulations, it was discovered that there was a mistake in the PLECS model for the *C2M0045170P* SiC MOSFET. In the Cauer network of the model, describing its junctions' thermal network, the final junction had thermal resistance value of 104 K/W. When cross-referencing this value with both the datasheet of the *C2M0045170P*, and with the PLECS model of the related SiC MOSFET, the *C2M0045170D*, it became

clear that the thermal resistance was three orders of magnitude too large. Accordingly, the thermal resistance was corrected to 0.104 K/W. With all of these issues taken care of, the PLECS simulations could begin.

The goal with the PLECS simulations as a whole is to map out the behaviour of the HyS for different operating conditions, and to compare it to using a solo IGBT solution. Therefore, the switching and conduction losses of the IGBT were measured for different load currents, with a switching frequency of $f_{sw} = 3$ kHz, and with a duty cycle of $D = 0.5$, where duty cycle was defined as $D = \frac{V_{out,avg}}{V_{in,DC}}$. The losses were extracted from the IGBT using a "Probe" block on the upper IGBT, and the conduction losses were ran through a "Periodic Average" block, while the switching losses were ran through a "Periodic Impulse Average" block. Using these blocks in conjunction with the PLECS steady-state analysis tool, which is explained in [46], allows for a consistent and accurate way to measure the losses of the IGBT, and eventually the HyS. The resulting losses were then recorded using the "Scope" block, and mapped to its corresponding load current. The load current interval used during these tests were $I_{Load} \in [250, 2000]$ A, using steps of 250 A between each test. An example of the measurement of the losses in the HyS is shown in Figure 3.10.

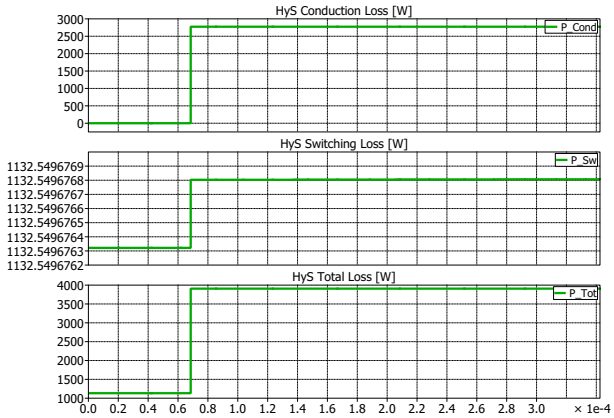


Figure 3.10: Example of power loss measurement in PLECS

With the losses from the IGBT recorded, these could be used as a comparative basis for the HyS tests. In order to calculate the losses of the HyS, the "Probe" block was used on a single SiC MOSFET in the upper SiC MOSFET cell, and then calculated using the same blocks as the case with the IGBT losses. The MOSFET losses were then multiplied by the number of MOSFETs in parallel, since the losses in PLECS are uniformly distributed amongst the MOSFETs, and summed with the IGBT losses. Furthermore, the junction temperature of the IGBT and the chosen MOSFET was also probed, and scoped together with the temperature of the heat sink and the heat flow through the thermal network. All of these parameters could then be used to determine by how much $f_{sw,max}$ of the converter could be increased if the solo IGBT was replaced by the HyS solution. It was therefore

decided to conduct a parametric sweep of the following parameters:

- **Load current.** $I_{Load} \in [250, 2000]$ A in steps of 250 A. Default value of $I_{Load} = 2000$ A.
- **Stray Inductance.** $L_\sigma \in [10, 100]$ nH in steps of 10 nH. Default value of $L_\sigma = 10$ nH.
- **Number of MOSFETs in parallel.** $N \in [10, 20]$ in steps of two MOSFETs. Default value of $N = 20$ MOSFETs in parallel.
- **Duty Cycle.** $D \in [0.2, 0.8]$ in steps of 0.1. Default value of $D = 0.5$.

For each parameter, the sweep was conducted as follows: The default value of each parameter was locked in, and the value of the swept parameter was varied within the given interval, with the pre-defined steps between each test. Each singular test consisted of choosing an arbitrary value for the switching frequency, then the junction temperature of the SiC MOSFET was measured, as showed in Figure 3.11. Assuming a 10 $\%$ safety margin, if the junction temperature exceeded 135 °C, the switching frequency would be decreased until the junction temperature was exactly 135 °C, or vice versa. The total losses of the HyS were then measured, and compared with the losses of the solo IGBT solution for the same load current. If the losses of the HyS solution were lower than the losses of the solo IGBT solution, the test was finished, and the switching frequency was recorded. If the HyS losses exceeded the corresponding solo IGBT losses, the switching frequency was decreased until the HyS losses were equal to the solo IGBT losses. The test was then finished, and the switching frequency was recorded. The values of several other parameters were also recorded alongside the switching frequency, like the transistors' junction temperatures, the switching losses of the HyS for the given test point, and the current distribution between the IGBT and the SiC MOSFET cell. As the testing procedure should make clear, the switching frequency of the HyS could be limited by either the junction temperature of the SiC MOSFET, or by the losses of the HyS, and which of these factors that limited the switching frequency was also recorded for each test. It is worth noting however, that the duty cycle sweep did not compare switching losses with the IGBT, since the results were incomparable. This was not a problem, because, as the results makes clear, the HyS was limited by junction temperature long before it was limited by losses at a load current of 2000 A. The results from the parametric sweep can be seen in Figure 4.13. A loss comparison between the solo IGBT solution and the HyS running at maximum allowable switching frequency for the given load points was also put together, and the results can be seen in Figure 4.14. During the parameter sweep, the current distribution when changing the load current was also recorded, and can be seen in Figure 4.15.

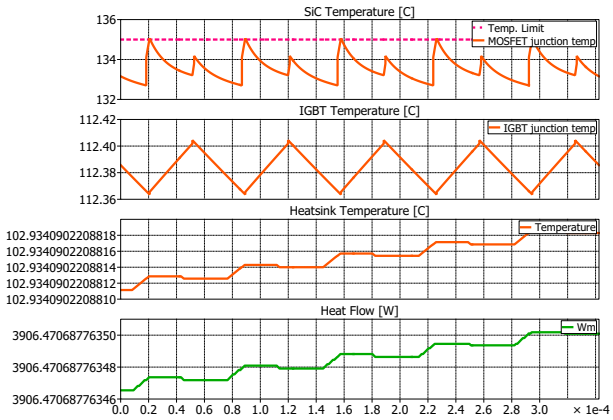


Figure 3.11: Example of temperature measurement in PLECS

The maximum switching frequency of the HyS was also determined when using different values of the thermal resistances $R_{th,ch}$ and $R_{th,ha}$ in order to determine the importance of the choice of attach material and cooling method. The default value of these resistances were $R_{th,ch} = 2.65$ K/kW, when using TIM as the attach material, and $R_{th,ha} = 0.0173$ K/W, when using forced air cooling. When testing $R_{th,ch}$, the thermal resistance value of the different attach materials shown in Table 3.5 were used. When testing $R_{th,ha}$, two additional cooling methods were approximated. First, by replacing forced air cooling with double-sided cooling, which was approximated as half of the default value for $R_{th,ha}$. Then, by replacing forced air cooling with passive cooling, which was approximated as double the default value of $R_{th,ha}$. The result of these tests can be seen in Figure 4.16.

Chapter 4

Results

This chapter contains all of the most important results from the thesis. All of these results will be presented in charts using either graphs or diagrams, making the results easily digestible and the relationship between variables simple to discern using only a cursory glance. The detailed tables containing all of the raw data from all of the tests can be found in Appendix D, in the appendices. The structure of the chapter will follow the chronology of the modelling method. First, the results related to designing the IGBT and SiC MOSFET models are presented, then the results of the electrical simulations of the HyS is shown. Finally, all of the final results from the thermal simulations of the HyS in a half-bridge configuration is presented. As a note, all of the figures shown in the sections which covers the Simscape simulations were extracted from simulations at a temperature of 150 °C, unless otherwise specified, in order to maintain consistency between figures.

4.1 Power Transistor Modelling

This section will show the resulting conduction and switching characteristics of the final models for the power transistors. First, the IV-characteristics of the two power transistor models in comparison to the IV-characteristics shown in the datasheet will be presented. Thereafter, the switching performance of the two models will be shown.

4.1.1 Conduction characteristics

In Figure 4.1 and Figure 4.2, the conduction characteristics of the IGBT model and the SiC MOSFET model, respectively, are presented. The figures contain the IV-curves from the models, compared with IV-points extracted from the datasheets of the respective components

IGBT

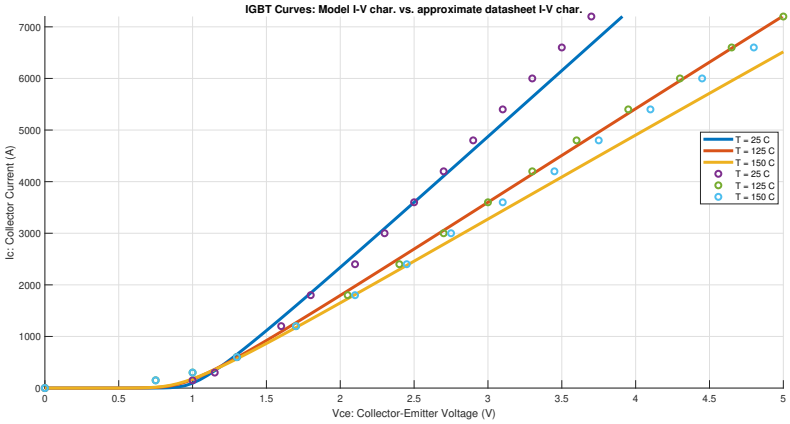


Figure 4.1: The finalized IV-characteristics of the IGBT model in comparison to IV-curves from the datasheet

SiC MOSFET

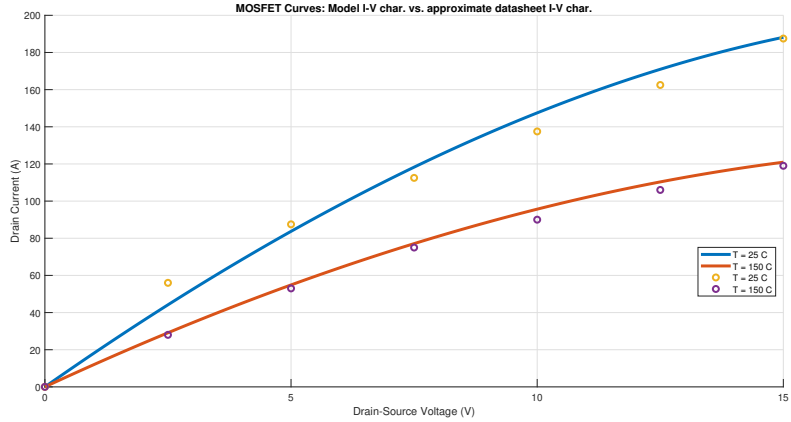


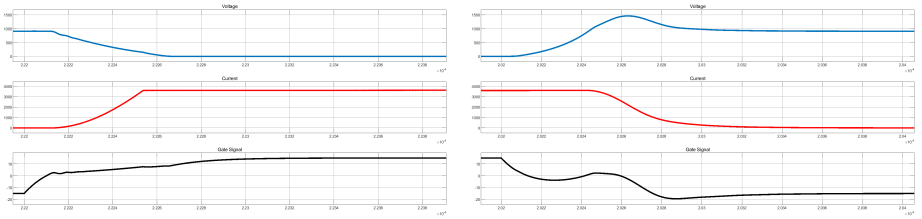
Figure 4.2: The finalized IV-characteristics of the SiC MOSFET model in comparison to IV-curves from the datasheet

4.1.2 Switching characteristics

The switching characteristics of the power transistor models are presented below. Both the switching waveforms, and the switching energy of the models will be presented, as well as the current fall times of the IGBT model.

IGBT

The turn-ON and turn-OFF waveforms of the IGBT model can be seen in Figure 4.3. The blue curve is the voltage waveform, the red curve is the current waveform, and the black curve is the gate voltage waveform.



(a) Turn-ON **(b)** Turn-OFF

Figure 4.3: IGBT model's switching waveforms during turn-ON and turn-OFF

The current fall time of the IGBT model, in comparison to the datasheet values, for different temperatures can be seen in Figure 4.4. The blue bars denotes the measurements done when using the IGBT model, while the orange bar denotes the datasheet values. The data used to compile the chart can be seen in Table D.2.

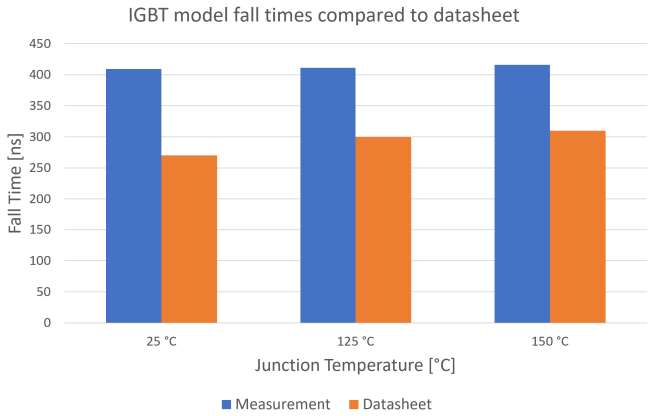


Figure 4.4: Current fall time of the IGBT model in comparison to the datasheet values at different temperatures

The switching losses of the IGBT model, in comparison to the datasheet values, for different temperatures can be seen in Figure 4.5. The blue bars denotes measurements, while the orange bars denotes datasheet values. The data used to compile the chart can be seen in Table D.1.

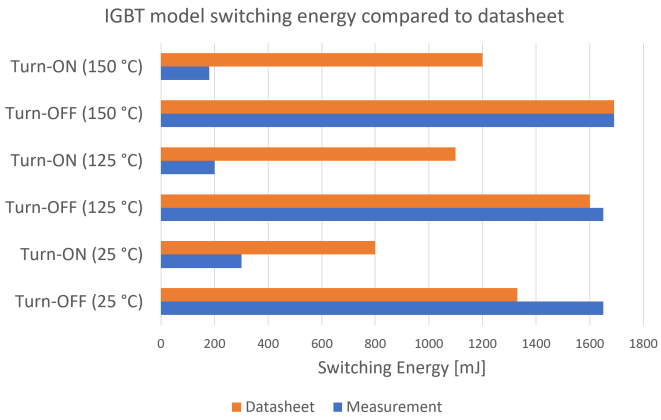
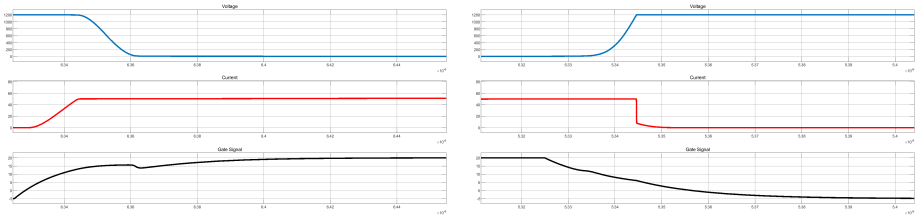


Figure 4.5: Switching Losses of the IGBT model in comparison to datasheet values at different temperatures

SiC MOSFET

The turn-ON and turn-OFF waveforms of the SiC MOSFET model can be seen in Figure 4.6. The blue curve is the voltage waveform, the red curve is the current waveform, and the black curve is the gate voltage waveform.



(a) Turn-ON **(b)** Turn-OFF

Figure 4.6: SiC MOSFET model's switching waveforms during turn-ON and turn-OFF

The switching losses of the SiC MOSFET model, in comparison to the datasheet values, for different temperatures can be seen in Figure 4.7. The blue bars denotes measurements, while the orange bars denotes datasheet values. The data used to compile the chart can be seen in Table D.3.

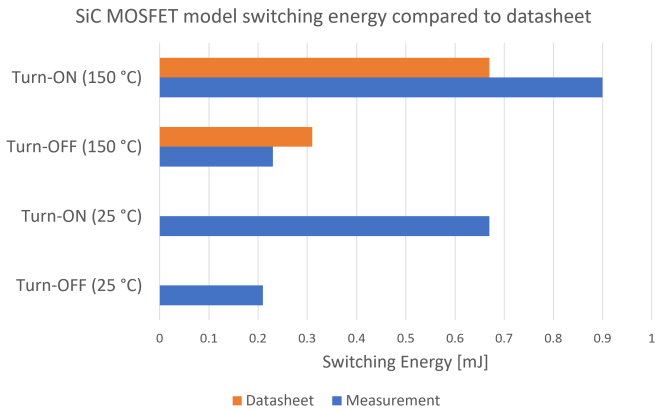


Figure 4.7: Switching Losses of the SiC MOSFET model in comparison to datasheet values at different temperatures

4.2 Results from Electrical Simulations

This section contains the results extracted from the Simscape simulations of the HyS DPT. First, it will present the results from the simulations without stray inductance present, and afterwards the results from the simulations with stray inductance is shown.

4.2.1 No Inductance

The relationship between current sharing and number of MOSFETs in parallel in the SiC MOSFET cell is shown in Figure 4.8. The data used to compile the chart can be seen in Table D.4. The red points denotes measurements, while the blue line is the linear trend-line of said measurements. As is shown by the figure and the R^2-value, the relationship between number of SiC MOSFETs in parallel and the steady-state current through the SiC MOSFET cell can be assumed to be linear.

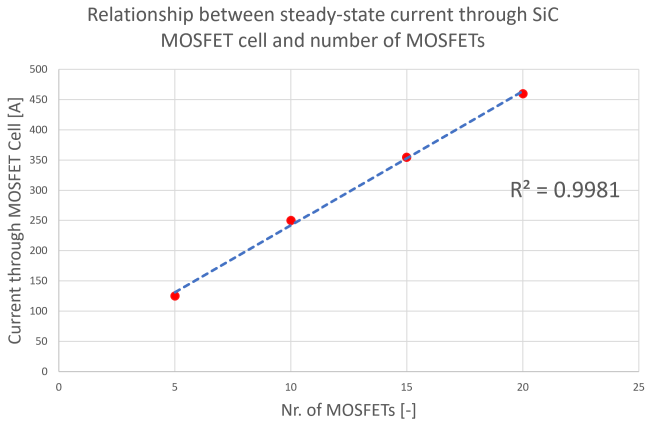


Figure 4.8: Relationship between current through SiC MOSFET cell and nr. of MOSFETs in the cell for a load current of 2 kA

The relationship between switching energy and the turn-OFF delay, t_2, can be seen in Figure 4.9. The cyan portion of the bar denotes IGBT loss, while the red portion of the bar denotes SiC MOSFET loss, and the black dotted line shows the total losses of the HyS. The data used to compile the chart can be seen in Table D.5. Based on the data presented in the figure, it was determined that $t_2 = 1.2$ µs was the optimal turn-OFF delay.

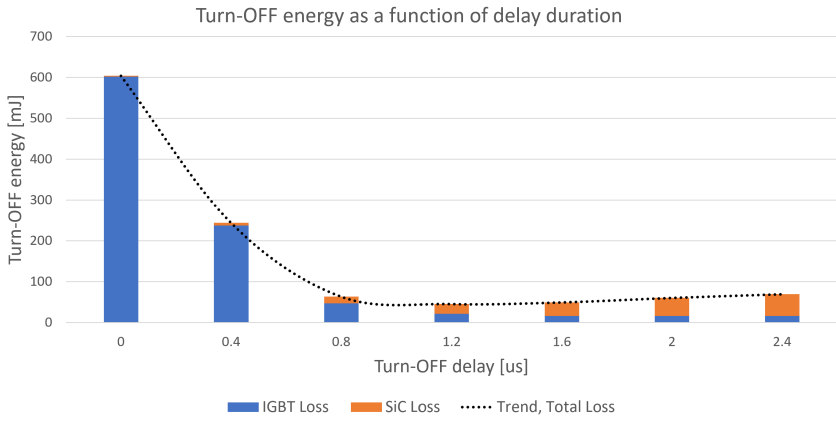
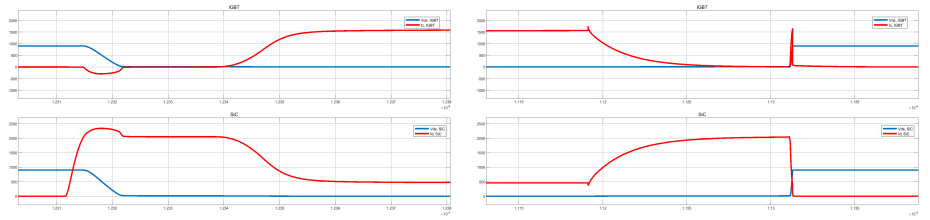


Figure 4.9: Relationship between switching energy and t_2

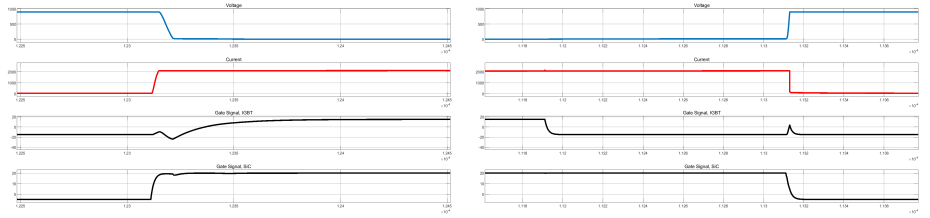
The switching waveforms of the constituent components of the HyS can be seen in Figure 4.10. The upper diagrams show the IGBT waveforms, while the lower diagrams show the SiC MOSFET waveforms. Like before, blue corresponds to a voltage waveform, while red corresponds to a current waveform.



(a) Turn-ON **(b)** Turn-OFF

Figure 4.10: The switching waveforms of the constituent components of the HyS

The aggregated waveforms of the HyS itself can be seen in Figure 4.11. The blue curve shows the voltage waveform and the red curve shows the current waveform, while the upper black curve shows the gate voltage of the IGBT, and the lower black curve shows the gate voltage of the SiC MOSFET.



(a) Turn-ON **(b)** Turn-OFF

Figure 4.11: HyS model's switching waveforms during turn-ON and turn-OFF

4.2.2 With Inductance

The commutation time as a function of commutation loop stray inductance can be seen in Figure 4.12. The red points denotes measurements, while the blue stapled line is the linear trendline of said measurements. Note that the commutation times in the figure is converted to the values that were used in the PLECS simulation, i.e. $T_d'/2$ is on the y-axis. The data used to compile the chart can be seen in Table D.6. A linear regression of the results was performed, and as can be seen from the R^2-value being approximately equal to 1, the relationship between commutation time and commutation loop stray inductance is linear. The relationship can be described using (4.1), where the units of $T_d'/2$ and L_σ is µs and nH, respectively.

$$T_d'/2 = 0.2377 L_\sigma - 0.0746 \tag{4.1}$$

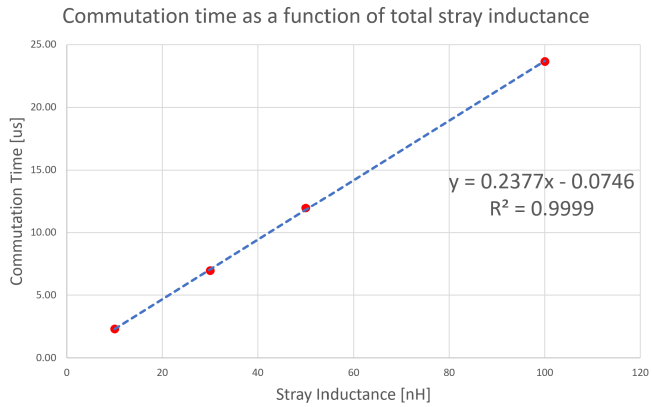


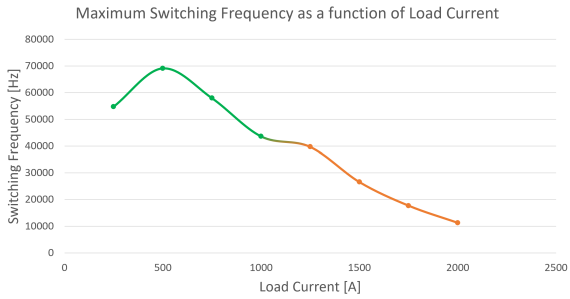
Figure 4.12: Commutation time as a function of stray inductance. Includes the linear trend line of the measurement points, its R^2-value, and the equation that describes the line

4.3 Results from Thermal Simulations

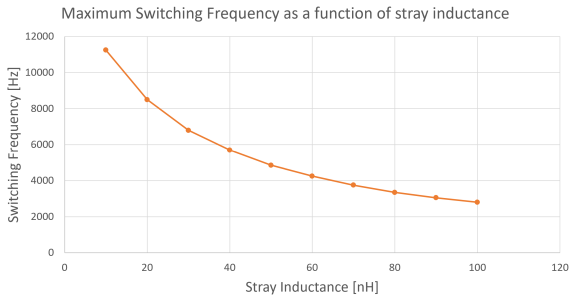
This section contains all of the results from the thermal simulations performed in PLECS.

Parametric sweep - Maximum switching frequency

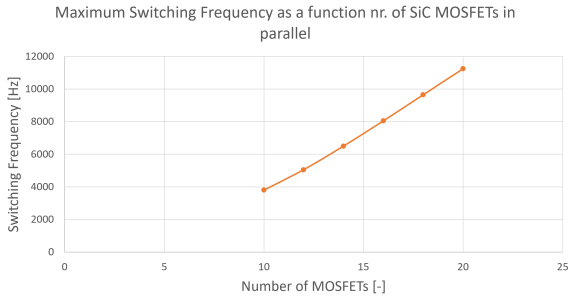
The relationship between the maximum achievable switching frequency of the half-bridge converter and the respective swept variables is shown in Figure 4.13. The colour of the line and markers indicates if the HyS was limited by junction temperature or power losses: If the line/marker is green, it was limited by power losses, while if the line/marker is orange, it was limited by the SiC MOSFET's junction temperature. The data used to compile the charts can be seen in Table D.8 to Table D.11. The power loss limit is based of an IGBT in a half-bridge circuit with a switching frequency of 4 kHz, and the power losses of said IGBT for different load currents can be seen in Table D.7.



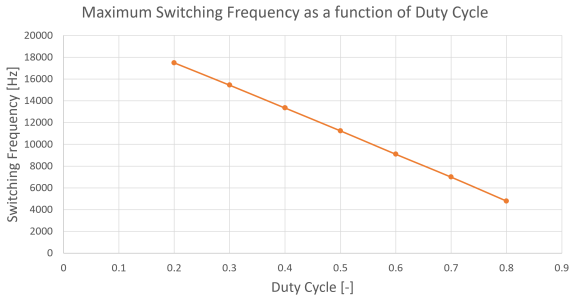
(a) Load current sweep



(b) Stray inductance sweep



(c) Paralleled MOSFETs sweep



(d) Duty cycle sweep

Figure 4.13: Results of the parametric sweep of the HyS in PLECS

Power loss comparison

A loss comparison between the solo IGBT solution and the HyS solution for different load currents can be seen in Figure 4.14. The gold portion of the bars denotes HyS switching loss, the blue portion denotes HyS conduction loss, the purple portion denotes solo IGBT switching loss, and the red portion denotes solo IGBT conduction loss. The data used to compile the chart can be found in Table D.8. Note that the switching frequency of the solo IGBT solution is 4 kHz, while the switching frequency of the HyS is the maximum allowable as given by the parametric sweep. Both solutions used a duty cycle of $D = 0.5$, and the HyS had a stray inductance of $L_\sigma = 10$ nH and used 20 SiC MOSFETs in parallel.

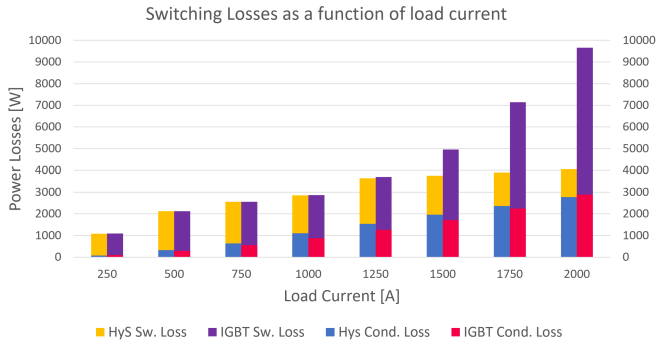


Figure 4.14: Power loss comparison between the solo IGBT solution and the HyS solution

Current distribution

The change in current distribution as a function of load current can be seen in Figure 4.15. The red portion of the bars denotes current through the SiC MOSFET cell, while the cyan portion of the bars denotes current through the IGBT. The data used to compile the charts can be seen in Table D.8.

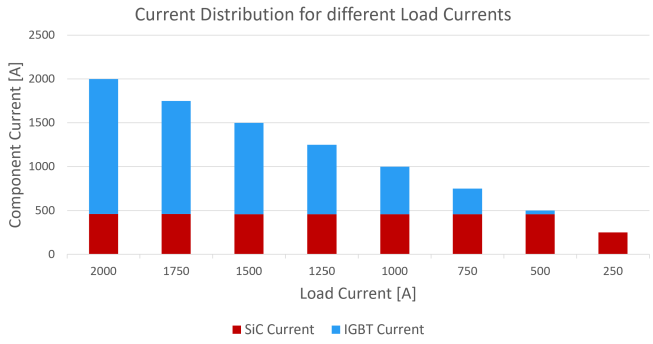
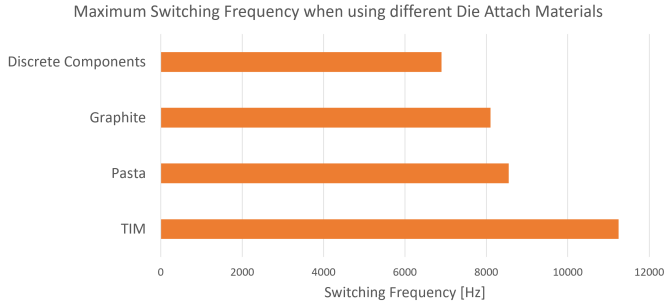


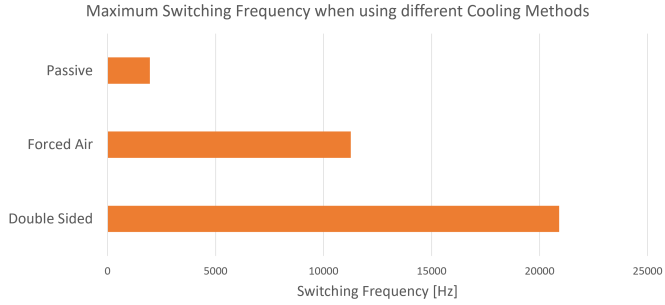
Figure 4.15: Change in current distribution with decreasing load current

Varying thermal resistance

The results from the tests where the thermal resistances in the PLECS model, $R_{th,ch}$ and $R_{th,ha}$, were varied can be seen in Figure 4.16. Figure 4.16a shows the maximum achievable switching frequency when using the different attach materials presented in Table 3.5, while Figure 4.16b shows the maximum achievable switching frequency for the different cooling method approximations presented in section 3.3. The orange colour of the bars indicate that the HyS was limited by junction temperature for all of the measurements. The data used to compile the charts can be seen in Table D.12 and Table D.13. In both the attach material and the cooling method test, the HyS operated using the default parameter values presented in section 3.3.



(a) Different attach materials



(b) Different cooling methods

Figure 4.16: Results from varying the thermal resistances in the thermal network of the PLECS model

Chapter 5

Analysis and Discussion

This chapter will serve as a platform to discuss, analyze, and reflect on the results presented in chapter 4. The discussion will surround the main research question presented in section 1.1: Is the HyS compatible with a high-power converter? How much can introducing the HyS increase $f_{sw,max}$ of a given converter? And what are the practical challenges for implementing the HyS in an actual converter? As can be seen from the key findings in section 4.3, shown in Figure 4.13, the results indicate that the HyS not only works in a high-power converter, it also enables an increase in switching frequency. The implications and validity of this finding, as well as the other findings in chapter 4, will be elaborated upon in the subsequent sections of this chapter.

The chapter will consist of three sections. The first section will review the viability of the power transistor models in order to establish a foundation for the analysis in the ensuing sections of the chapter. The second and final section will analyze the electrical and thermal simulations, respectively. Both sections will follow the same general structure: First, results will be analyzed, based in theory. Afterwards, the limitations of the results and the sources of error present in the method will be identified, and their consequences for the findings in the thesis will be deliberated upon.

5.1 Viability of the Power Transistor Models

This section will analyse the viability of the two power transistor models created in the thesis. What is accurately modelled, and what can be improved, is identified and dissected, and proposals on how the models could have been improved will also be discussed. Establishing the strengths and the limitations of the transistor models will serve as a foundation for further analysis of the electrical and thermal simulations of the HyS, and it is therefore imperative that these are properly identified in order to maintain the integrity of the discussion. In order to asses the quality of the models, their conduction and switching

characteristics will be compared to both established theory and the datasheets of the components that the models are based on.

5.1.1 Conduction characteristics

First of all, the conduction characteristics of the two models will need to be scrutinized. The IV-characteristics of the IGBT and SiC MOSFET models in comparison to their datasheet values are seen in Figure 4.1 and Figure 4.2, respectively. In general, a point on the IV-plane will indicate the magnitude of conduction losses by implying the ON-resistance for the given point. High current and low voltage (towards the upper left of the plane) indicates a low ON-resistance, and therefore low conduction losses. The opposite is true for high voltage, low current (lower right of the plane). This correlation is helpful when comparing the model IV-curves to the corresponding datasheet values, as it will indicate whether the model under- or overestimates the conduction losses of the component. If the model's IV-curve is above the corresponding point from the datasheet, the conduction losses are underestimated, and vice versa.

Taking a look at the IGBT IV-curves, it is apparent that the three curves all align reasonably with their corresponding datasheet values. All of the three curves also follow the same pattern, being that they underestimate conduction losses for current levels below rated level (3600 A), and overestimate at currents above rated level. At worst, the effective resistance is overestimated by around 5 $\%$ for 3.5 V. But this is not considered a large issue, since this current level is not used in the electrical simulations. The most important current level to model accurately, is the current around 2000 A, since that is the current level that would be used during the switching actions when testing the HyS. Luckily, all three curves follow the current point nearest 2000 A closely, with the largest deviation coming from the 25 °C line. It is worth noting that the conduction losses are all slightly underestimated at this current level, which is not ideal given that it might overestimate the capabilities of the IGBT. Nonetheless, these deviation from the datasheet values are considered small enough for the conduction model of the IGBT to be deemed acceptable.

The IV-characteristic of the SiC MOSFET model tells a similar story to the that of the IGBT. Both IV-curves roughly follows the datasheet values, with some minor deviations. For the SiC MOSFET model, it was important that the current interval from 0 A to 100 A was modelled accurately, since the SiC MOSFET in the HyS simulations conducted current within this range. Within this range, there is a quite noticeable overestimation of the ON-resistance for the 25 °C curve. At a voltage level of 2.5 V, the ON-resistance is overestimated by 20 $\%$, which is nonoptimal. This deviation is lessened for increasing current levels within the interval of importance, and seems to be almost gone at 100 A. In contrast, the deviations for the 150 °C curve are minuscule, and the conduction profile of the SiC MOSFET model at this temperature is considered to be quite accurate.

In order to assess the consequences of what has been discussed above, it is important to consider what the electrical simulations of the HyS explored in terms of conduction characteristics. As was mentioned in the opening of section 3.1, the most important part of modelling the conduction characteristics accurately was to determine how the current was shared between the IGBT and the MOSFET. Since calculations of conduction losses

are not needed in the electrical simulations, the absolute over- and/or underestimation of the conduction loss is not of categorical importance. Rather, it is imperative that the relationship between the conduction profiles of the IGBT and the SiC MOSFET is accurate for the relevant current intervals. Furthermore, since the current sharing was assessed at 150 °C, the large deviation of the 25 °C curve becomes irrelevant. As can be seen from Figure 4.1 and Figure 4.2, the IGBT curve at 150 °C follows the datasheet values very closely at 2000 A, while the SiC MOSFET curve at 150 °C slightly underestimates the conduction losses. As a consequence, the SiC MOSFET will conduct slightly more current in the electrical simulations than it should, but this deviation is considered within acceptable margins of errors. All in all, the conduction characteristics of the IGBT and SiC MOSFET models are considered to be satisfactorily accurate in order to fulfil their intended purpose in the electrical simulations.

5.1.2 Switching characteristics

The switching characteristics of the models will also be examined. Starting with the IGBT model, its switching waveforms can be seen in Figure 4.3. When comparing these waveforms with what was presented in Figure 2.9 in subsection 2.1.3, it is apparent that the waveforms are, for the most part, pretty similar. The turn-ON waveform of the model does not have any current overshoot, but the rest of the turn-ON waveforms exhibits expected behaviour. While the lack of an overshoot means that the turn-ON losses might be slightly underestimated, this is not of any consequence for the electrical simulations. As was mentioned in subsection 3.1.2, modelling of the turn-ON is not very important, since the switching losses during turn-ON will be negligible, and the length of the turn-ON delay is more dependent on the SiC MOSFET, than the IGBT.

For the turn-OFF waveforms, it can again be observed that the shape of the waveform falls within what was expected. There is a voltage overshoot, and most importantly, a noticeable current tail. There is some discrepancy with the gate voltage, as there is a slight increase during the current fall, and this seems to be caused by the voltage overshoot. This might cause a slowdown for the current fall, which Figure 4.4 seems to suggest is exactly what happens. As the figure shows, the model fall time is approximately 33 % longer than the value from the datasheet. The most notable consequence of this disparity is that it could lead to inaccuracies when modelling the length of the current tail. As was mentioned in subsection 3.1.2, the length of the current tail was determined using the switching losses from the IGBT datasheet as a guide. With the current fall time of the IGBT model being longer than that of the actual component, this implies that a larger portion of the switching losses in the model would occur before the current tail. Accordingly, when determining the length of the current tail using the ”Total forward transit time” parameter, the duration of the current tail would be underestimated. This is not ideal, given that one of the main objectives of the IGBT modelling, and the electrical simulations in general, is tied to the length of the IGBT current tail. Because of this inaccuracy, the optimal length of the turn-OFF delay will be different between the IGBT model, and the component it is based on.

The final part of the switching characteristics of the IGBT model that will be examined is the switching energies in comparison to what is in the datasheet. In Figure 4.5, the turn-ON

and turn-OFF switching energy of the IGBT model is compared with the corresponding values in the datasheet. The figure reveals some important aspects of the IGBT model. Namely, that the turn-ON energy is severely underestimated, and the turn-OFF energy matches quite well, especially at higher temperatures. In the case of the turn-ON energy, this obvious inaccuracy could have been quite problematic, but because of the unimportance of the IGBT turn-ON losses for the HyS's performance, this issue can be more or less completely ignored. When it comes to the turn-OFF energy, the almost perfect match that occurs during turn-OFF at 150 °C is a direct consequence of how the current tail was modelled. Since the length of the current tail was determined by matching the switching energy of the model with the datasheet at 150 °C, this would always be the result. What is more notable, however, is how temperature affects the switching energy of the model. Because, while the turn-OFF energy presented in the datasheet decreases as the temperature decreases, the turn-OFF losses are almost unchanged. This same trend was also present in the current fall time of the model as seen in Figure 4.4, and is a direct consequence of how the charge model of the "N-Channel IGBT" block in Simscape works. As is stated in [34], the charge model of the IGBT is independent of temperature, meaning that the switching dynamics of the IGBT model is mostly independent of temperature as well. Any changes in the dynamic characteristics of the IGBT model that occurs due to a change in temperature is the result of indirect effects stemming from the conduction profile of the IGBT, which is temperature dependent. An example of such an indirect effect can be observed at the turn-ON energy of the IGBT model, which actually more than doubles with a decrease in temperature, which is the complete opposite of what would have been expected given what was presented in Figure 2.10 in subsection 2.1.3. This limitation in the charge model of the IGBT actually serves as one of the justifications for optimizing the turn-OFF energy for 150 °C, since it was considered preferable for the IGBT model to overestimate the current tail, than to underestimate it. If the current tail length had been determined using the 25 °C turn-OFF energy in conjunction with the fact that it already has been underestimated as the result of the current fall time discrepancy, this would have lead to an unacceptable error when considering the objectives of the thesis. Furthermore, as has already been established, it is expected that the HyS would operate at high junction temperatures in the thermal simulations, and therefore modelling the current tail based of the 150 °C losses would better align with what was expected of the thermal simulations.

Next, the switching characteristics of the SiC MOSFET model will be assessed. The switching waveforms can be seen in Figure 4.6. When comparing these to the theoretical waveforms presented in Figure 2.5, it is clear that they look more or less as expected, with the only deviation being the lack of a current overshoot in the SiC MOSFET model waveforms. Similarly to the case with the IGBT, the lack of this overshoot might lead to a slight underestimation of the turn-ON losses. However, when examining the turn-OFF waveforms of the SiC MOSFET, it becomes clear that the SiC MOSFET model is not perfect. Because while the voltage waveforms behaves more or less like expected, there are some very severe differences with the current waveform. Specifically, the current fall time is almost immediate, being only a fraction of a nanosecond. This will of course lead to an underestimation of the turn-OFF energy, since one of the terms in t_{ov}, t_{fi}, is essentially zero, and according to (2.2) this has a direct impact on turn-OFF energy. It is suspected that the reason for this behaviour stems from how the SiC MOSFET was modelled. As was

explained in section 3.1, the SiC MOSFET was modelled using a threshold-based model. As is explained in [35], the threshold-based model has a noticeable weakness during the transition across the threshold voltage, which means the model can have trouble capturing accurate switching actions. Furthermore, it lacks a term for velocity saturation, which means that there is no inherent limit to the switching speed of the model. These two flaws in conjunction is then believed to be the cause of the inaccurate turn-OFF waveform. The obvious fix to this problem would be to use the surface-potential-based model instead, but as was explained in section 3.1, this was not possible in this thesis. Therefore, the deficiencies and limitations of the threshold-based models are a necessary evil in order to complete the thesis.

While the obvious consequence of the poor turn-OFF modelling is the underestimation of the SiC MOSFET's turn-OFF energy, there is also another consequence which is pertinent to the thesis: How inductance will interact with the current. Since an inductor acts as a limiter to the $\frac{di}{dt}$ of a system, introducing stray inductances to the MOSFET might lead to a completely different current waveform. A consequence of this is that it will become impossible to judge how stray inductance actually affects the switching performance of the SiC MOSFET. This was touched upon in subsection 3.2.2, where it was noted that merely introducing stray inductance into the system caused the switching losses to more than double, independent on how large the inductance value was. Given the current waveform of the SiC MOSFET model, it is reasonable to believe that this large increase in switching energy is caused by the current fall rate during turn-OFF being limited by the parasitic inductor. This hypothesis is corroborated by the fact that it was specifically the turn-OFF energy that was increased when introducing the stray inductance. Therefore, it seems that one of the major consequences of using a threshold-based model for the SiC MOSFET component is the fact that the relationship between switching energy and stray inductance level is not possible to assess in a realistic manner, making it impossible to include this effect in the thermal simulations.

Finally, the switching losses of the SiC MOSFET model can be discussed. The switching losses of the model is compared to the values from the datasheet in Figure 4.7. The first aspect to note is that there is a noticeable difference in the switching energies of the model and the actual component. However, since the threshold-based model does not contain any parameters that allows for fine-tuning of switching waveforms, this is not totally unexpected. Luckily, the difference between the total switching energy is not very large, with only a slight overestimation being present, since the turn-ON energy is overestimated, while the turn-OFF energy is underestimated. While the underestimation of turn-OFF energy is expected because of the waveform presented previously, it is a bit surprising that the turn-ON energy is overestimated, even though no current overshoot is present. Most likely, this is caused by the inaccuracies present during the transition across the threshold voltage, making the model a bit slower than the actual component.

The second aspect of Figure 4.7 to consider, is that the datasheet of the SiC MOSFET component only shows the switching energies for a single temperature, 150 °C. This is not ideal, since it does not allow for a proper comparison of how the model and the components behaves for different temperatures. Nonetheless, the switching energy of the SiC MOSFET model was still measured, since it can be compared to theory. As is clear to see,

the turn-ON losses increases with temperature, which is the opposite to what was stated in subsection 2.1.2. However, a discrepancy like this was not completely unexpected, since there was no way to model the MOSFET's charge model's temperature dependency, like the case was for the IGBT [35]. As a consequence, the MOSFET's charge model exhibits the same behaviour as the IGBT's; any change to switching energy as a result of temperature change is the result of indirect effects caused by the temperature dependent conduction characteristics of the model. In contrast, the turn-OFF does change in accordance with established theory, but this is more of a coincidence than a result of the temperature dependency of the turn-OFF instance being correctly modelled.

In total, the discrepancy between what is shown in the datasheet and what is produced by the model in terms of switching losses is considered within acceptable limits, and the model would have served its purpose. However, because of the poor modelling of the turn-OFF current waveform, the switching losses of the SiC MOSFET model ended up not being used in the thermal simulations. Accordingly, any deviation in switching characteristics between the model and the datasheet ended up not mattering to the results of the thesis. The consequences of not being able to include an approximation of how stray inductance affects the switching losses in the thermal simulations will be discussed in a later section.

5.2 Analysis of Electrical Simulations

In this section, the results from the electrical simulations conducted in Simscape, seen in section 4.2, will be analyzed and discussed. At first, all of the results will be compared to theory in order to establish if the findings are expected or unexpected. Dependent on how the results compares to expectations, their significance to research question of the thesis will then be elaborated upon. After the analysis of the results, a critical review of the method will be conducted in order to ascertain the limitations and sources of error of the results. The consequences of these errors will then be assessed in order to determine if they will have a detrimental effect to the conclusions drawn in regards to the research question.

5.2.1 Results compared to theory

The different results from section 4.2 will be assessed in the same order that was outlined in the section. Accordingly, the first results that will be analyzed are the results from the electrical simulations without stray inductance present. Of the findings in these simulations, the result presented in Figure 4.8 will be assessed first. This figure shows quite clearly that the steady-state current through the SiC MOSFET cell and the number of SiC MOSFETs in parallel in the cell is linear. This is corroborated by the fact that the R^2-value is close to one, which means that the measurements only slightly deviates from the projected linear line. This result is completely expected, since adding or removing MOSFETs in the switching cell in practice amounts to decreasing or increasing the equivalent resistance in the cell, respectively. Given that it is assumed that all of the SiC MOSFETs have the same ON-resistance, the equivalent resistance in the SiC MOSFET cell can be

described by (5.1), where $R_{ds(ON)}$ describes the ON-resistance of a single SiC MOSFET and N describes the number of SiC MOSFETs in parallel.

$$R_{eq,MOSFET} = \frac{R_{ds(ON)}}{N} \tag{5.1}$$

As the equation clearly shows, the equivalent resistance is inverse proportional to the number of SiC MOSFETs in parallel, and since current is inverse proportional to resistance according to Ohm's law, it follows that the current is linearly proportional to the number of SiC MOSFETs in parallel, just like what was observed in the electrical simulations. Although this result in and of itself is not groundbreaking, it was still important to verify the relationship between the current and the number of SiC MOSFETs in order to make use of the linearity in the approximations that were necessary for the thermal simulations in PLECS. Furthermore, the results also showed how the current was shared between the IGBT and the SiC MOSFET switching cell for the given load current. This was one of the goals of the electrical simulations, as outlined in section 3.2, since it was necessary to determine the current sharing in order to ensure the correct load through the SiC MOSFETs during the thermal simulations. Therefore, the results from Figure 4.8 was the first step towards answering the research question of the thesis.

In Figure 4.9, the turn-OFF energy of the HyS as a function of the turn-OFF delay, t_2, is illustrated. This relationship was used in order to optimize t_2, which was one of the main goals of the electrical simulations. As can be seen from the figure, increasing t_2 from 0 to 0.4 µs more than halves the turn-OFF energy, and increasing t_2 by a further 0.4 µS produces the same effect, before the effect of increasing t_2 experiences diminishing returns. This behaviour is very similar to the behaviour showcased in Figure 2.22, in subsection 2.3.2, and the behaviour is therefore expected. The reason for the diminishing returns can be explained by the shape of the IGBT turn-OFF current waveform. Since this current contains a current tail, the majority turn-OFF energy of the IGBT is concentrated at the beginning of the switching instance. Assuming that the length of the current tail is defined as the time it takes for the IGBT current to descend from 10 % of the peak current to zero, it can be seen from the IGBT waveform in Figure 4.3b that it might take the current the same amount of time to descend from peak to 10 %, as it takes the current to descend from 10 % to zero. Accordingly, increasing t_2 past the time it takes to reach 10 % of peak current will lead to diminishing returns since a much smaller portion of the current will be left from that point onwards. This point was referred to as the inflection point in subsection 2.3.2, and it was used in order to choose the optimal length of t_2. By using the selection criterion defined in subsection 3.2.2, the turn-OFF delay of the IGBT was determined to be $t_2 = 1.2$ µs.

Something to note is that Figure 4.9 shows that increasing t_2 past the inflection point does not only lead to the total turn-OFF energy plateauing, but it actually increases it. This behaviour can also be observed in Figure 2.22 to a lesser degree, and might seem counter-intuitive. However, since Figure 4.9 breaks down the HyS turn-OFF energy in IGBT and SiC MOSFET turn-OFF energy, it is possible to observe that the reason for the increase in HyS turn-OFF energy when t_2 increases past the inflection point is because of increased turn-OFF energy at the SiC MOSFET cell. By closely inspecting the turn-OFF waveforms

of the HyS components shown in Figure 4.3b, it can be observed that the moment the IGBT turns off a small voltage of around 10 to 12 V can be measured across SiC MOSFET cell, as seen in a zoomed in view of the IGBT turn-OFF instance shown in Figure 5.1. This voltage forms an additional current-voltage overlap, which will lead to a power loss in accordance with (2.1). In this additional current-voltage overlap, the current-voltage overlap time, t_{ov}, can be substituted for t_2, which plainly illustrates why an increase in t_2 leads to an increase in SiC MOSFET turn-OFF energy. This increase due to the SiC MOSFET illustrates the importance of a holistic approach when designing the HyS, since the optimal choice of t_2 was only possible when considering all of the constituent components of the HyS. Since the main goal of the turn-OFF delay is to decrease the IGBT switching loss, it would be easy to only measure the IGBT turn-OFF energy, and optimize t_2 with only that in mind, but that approach could have lead to an nonoptimal choice of t_2 when viewed from a system perspective. In short, it is essential to consider both the IGBT and the SiC MOSFETs in every choice related to the HyS's design, even if it seems like the choice should not have any influence on one of the components.

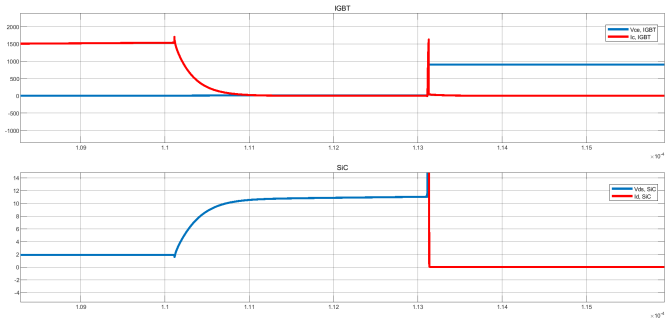


Figure 5.1: Zoomed in view during IGBT turn-OFF that shows voltage across the SiC MOSFET cell

The finalized waveforms of the constituent components of the HyS can be seen in Figure 4.10. The waveforms are for the most part the same as expected, i.e. they are almost the same as the waveforms from Figure 4.3 and Figure 4.6. However, there are some notable discrepancies. First of all, during the turn-ON instance, shown in Figure 4.10a, there is an overshoot present in the SiC MOSFET current. At the same time, there is a reverse current through the IGBT, and the sum of these currents cancel each other out. This implies that the currents are connected to one another, and it is believed to be a consequence of how Simscape handles electrical references. As was mentioned in subsection 3.2.1, the HyS model contains several gate drivers. Normally, this would not have any notable side effects, because the gate drivers would be electrically isolated from one another. However, this is not possible in Simscape, since every electrical reference added to the system will be connected to the same ground, which leads to the gate drivers being coupled. This allows for current to flow from one gate driver to the other, which is believed to be the cause of the overshoot and reverse current which can be observed in the waveforms of the IGBT and SiC MOSFET. The same phenomenon can also be observed in Figure 4.10b, but the cur-

rent is much smaller, and can be considered negligible. Furthermore, there is an additional current spike in the IGBT current when the SiC MOSFET turns off. This is not believed to be an accidental turn-ON, like was discussed in subsection 3.2.1, because of the lack of a current tail, but rather another consequence of the failure to completely decouple the gate drivers in the system. It is not known exactly why it happens, but it is believed that the gate drivers using the same ground is at the very least a factor that enables the behaviour. The suspicion that these issues are related to the coupling of the gate drivers is corroborated by the gate voltage waveforms of the two devices shown in Figure 4.11, which shows that the gate voltage of the IGBT is strongly affected by both the turn-ON and turn-OFF of the SiC MOSFET. In any way, these discrepancies won't have any consequences for the results in the thermal modelling because of the problems related to stray inductance.

Finally, the results from the electrical simulations with stray inductance present are to be analyzed. The result from these simulations are presented in Figure 4.12. As expected, the results show that increasing the stray inductance leads to an increase in the time it takes for the current to commutate from the SiC MOSFET cell to the IGBT after the IGBT is turned on. This aligns with what is shown in Figure 2.26. Furthermore, by emplying linear regression, it was found that the relationship between the commutation time and the total stray inductance was linear for the interval from 10 to 100 nH. This also seems to be in alignment with what is shown in Figure 2.26b, but there is an important difference. The results presented by [28] uses stray inductance imbalance as their variable, while this thesis uses total inductance as the variable. This thesis will argue that the approach using total impedance is the correct one. This claim is based on the fact that the slow down in commutation delay will be caused by the $\frac{L}{R}$-time constant. For the HyS, the current will commutate from the SiC MOSFET to the IGBT through the drain and collector inductances. Therefore, the inductance component of the $\frac{L}{R}$-time constant will be the sum of the drain and collector stray inductances. A simplified circuit showing the current commutation can be seen in Figure 5.2. Assuming that the simplification of the commutation path holds, it does not matter how the inductance is distributed between the IGBT and the SiC MOSFET cell when it comes to the current commutation time, since the current needs to flow through both of the inductances anyway. This conclusion is supported by the what was stated in subsection 3.2.2; that as long as the total stray inductance stayed the same, no discernible difference could be found between waveforms when changing how the stray inductance was distributed between the IGBT and SiC MOSFET. In any case, the results from the stray inductance tests are important to the thesis, as they were used during the thermal simulations in order to asses how stray inductance affects the thermal performance of the SiC MOSFETs.

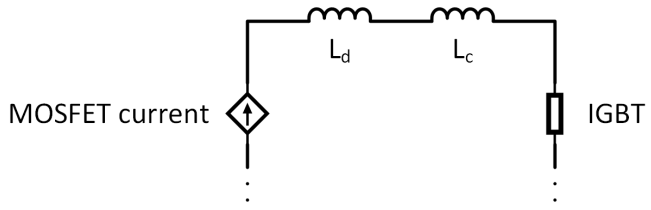


Figure 5.2: Equivalent circuit during current commutation from SiC MOSFET cell to IGBT

5.2.2 Limitations and sources of error

The most important limitations and sources of errors of the electrical simulations will be discussed in this subsection. First of all, it is worth pointing out that every result from these simulations will contain some margin of error due to the measurement methods used. Since every measurement during these simulations were done using the cursors built into the Simulink scopes, and these cursors need to be placed manually, the cursors will give rise to a certain amount of inaccuracy. While this inaccuracy can be somehow mitigated by using unambiguous measurement criteria and the like, it will never be completely eliminated. What is important to consider is how these inaccuracies might affect the ability to answer the research question. Given that one of the key elements used to answer the research question is using thermal analysis, the need for accuracy is not as high because of the slow dynamics involved. It is therefore believed that any kind of inaccuracy originating from the measurement method used during the electrical simulations will have a negligible effect on the thermal simulations, and therefore not prove to be a hindrance to answering the research question.

Any other error source present in the electrical simulations before stray inductance is introduced will have originated from the modelling of the power transistors. As was argued in subsection 5.1.1, the modelling of the conduction profiles of the power transistors is considered to be quite accurate, and any inaccuracy originating from the conduction profiles of the power transistor models is believed to have a negligible effect on the thermal simulations. However, as was noted in subsection 5.1.2, because of longer current fall time of the IGBT model in comparison to the actual component, the current tail of the IGBT model will be underestimated. As a consequence, the choice of t_2 will be different for the IGBT model in comparison to what would be optimal for the actual component. Depending on how large the difference is, this might have a non-negligible effect on the thermal simulations. It is therefore important to establish if t_2 will be under- or overestimated as a consequence of the current fall time discrepancy. Though it might seem natural that an underestimation of the current tail would lead to an underestimation of t_2, this is not necessarily the case. On the contrary, it is believed that t_2 has actually been overestimated. This belief stems from the fact that the majority of switching losses is concentrated during the current fall time interval, which has been corroborated by both Figure 2.22 and Figure 4.9. Therefore, it is believed that the inflection point would occur earlier with the actual component than with the IGBT model. Given how the selection criterion was defined in subsection 3.2.1, this means that t_2 has been overestimated in the electrical simulations. As a consequence, the SiC MOSFETs in the thermal simulations will experience larger conduction losses than necessary, which in turn will lead to a higher junction temperature, thus underestimating $f_{sw,max}$ of the HyS. Nonetheless, neither the electrical simulations nor the thermal simulations will be able to concretely quantify this effect because of the limitations of PLECS. The magnitude of the effect can, however, be inferred from how changing the commutation delay affects the switching frequency of the HyS.

Before discussing the different issues that arose from introducing the stray inductance to the circuit, it is worth mentioning that the selection criterion for t_2 is somewhat inflexible, and therefore might not be able to capture the nuances of the trade-off mentioned in subsection 2.3.2. Specifically, optimizing t_2 for the thermal integrity of the SiC MOSFET

dice is completely absent from the selection criterion. Although this deficiency might lead to a nonoptimal choice of t_2, it was decided that the compromise was worth it in order to achieve a selection criterion which was as unambiguous as possible.

The most consequential single complication encountered during the thesis work, was the convergence issues that arose when introducing stray inductance to the electrical simulations. As was explained in subsection 3.2.2, these issues ultimately lead to the use of an ideal IGBT model and large gate resistors. This inevitably had some notable consequences. Most importantly, the scope of the thesis was slightly limited, as it was no longer possible to accurately assess how the stray inductance influenced the switching energy of the HyS. This also means that the effect stray inductance has on switching losses was excluded from the thermal simulations, which means that the performance of the HyS was slightly overestimated in relation to the amount of stray inductance in the circuit.

Using an ideal IGBT model also introduces an additional error source to the electrical simulations, since the conduction profile of the ideal IGBT was unable to accurately model the conduction profile of the IGBT component. This had two notable consequences, the first of which was already mentioned in subsection 3.2.2: Because the current sharing was no longer accurate, the measured commutation time had to be corrected using (3.2). Given that this correction only holds if the assumption that the relationship between current change, ΔI, and commutation time, T_d, is linear, using the correction will introduce an error to the commutation time. While it is believed that the triangle approximation used in Figure 3.8 is the best possible approximation for the commutation time given the limitation present in PLECS, using this approximation in conjunction with the correction for the current sharing will increase this margin of error. In order to properly quantify the margin of error, a rudimentary analysis of the error originating from the triangle approximation was performed. In this analysis, the calculated area for the rectangle approximations used in PLECS were compared to the the measured area of the commutation current. The measurements were done using the ”Integrator” block in Simulink, and the area was measured using the cursors in the Simulink scope. The waveforms that were input to the scope were the commutation current and its integral, which is the equivalent of the area under the commutation current curve, and they can be seen in Figure 5.3. This was done for 10 nH, 30 nH, 50 nH, and 100 nH in order to make the error analysis as comprehensive as possible.

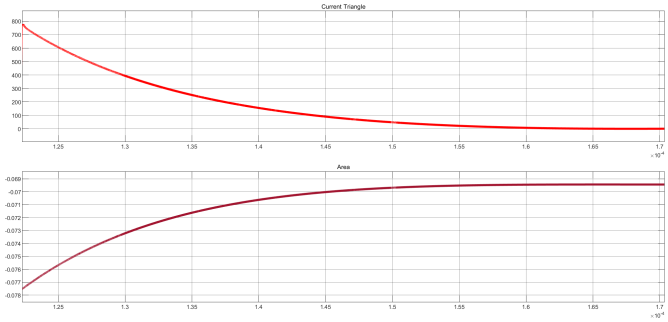


Figure 5.3: The waveforms used to measure the area of the commutation current. The upper curve is the commutation current, while the lower curve is the integral of the commutation current.

With all of the measurements completed, the error could be calculated using (5.2), where e_A denotes the error.

$$e_A = \frac{Approximation - Measurement}{Measurement} \tag{5.2}$$

Furthermore, this error could be used to calculate the error in conduction loss calculations which would occur in PLECS. By using the relationship between current and conduction loss, shown in (5.3), the conduction loss error, e_{Pcond}, could be estimated using (5.4).

$$P_{cond} = I^2 R_{ds(ON)} \tag{5.3}$$

$$P_{cond} \propto I^2 \implies e_{Pcond} = e_A^2 \tag{5.4}$$

The results from the error analysis can be seen in Table 5.1.

Stray Inductance [nH]	Calculated [As]	Measured [As]	Error [%]	Conduction Loss Error [%]
10	1.617E-03	1.21E-03	34.10	79.82
30	4.249E-03	3.56E-03	19.38	42.51
50	6.429E-03	5.41E-03	18.95	41.49
100	9.226E-03	8.08E-03	14.16	30.32

Table 5.1: Results from the error analysis of the current commutation approximations

First of all, the results shows that the conduction loss during the current commutation will be overestimated in PLECS. This was expected, and is illustrated by Figure 3.8, which

shows that the triangle approximation's area will always exceed the area of the current commutation to a certain degree. However, it is worth pointing out that the overestimation is rather large, which leads to an almost doubling of the conduction loss during current commutation for $L_\sigma = 10$ nH. Because of the size of the overestimation, this undoubtedly had an effect on the performance of the HyS during the thermal simulations, and it is reasonable to believe that it leads to an underestimation of the HyS's performance. Even when taking into account that the effect stray inductance has on switching losses are excluded from the thermal analysis, the HyS's performance is still probably underestimated for a stray inductance of $L_\sigma = 10$ nH. On the other hand, when the stray inductance increases, the error decreases. This can be explained by examining Figure 3.7, where it can be seen that the current commutation area approaches the shape of a triangle as the stray inductance increases. Taking this into account, it becomes harder to assess if the performance of the HyS is under or overestimated when stray inductance increases, since an increase in stray inductance will lead to larger voltage overshoots, which in turn leads to larger switching losses. At the very least, it can be assumed that the thermal simulations will go from underestimating the performance of the HyS, to overestimating it as the stray inductance increases. Nevertheless, at which level of stray inductance the transition from under- to overestimation occurs, and if it even happens within the interval used during this analysis, is impossible to predict using the tools available for the thesis.

Finally, there is another error source that occurs as a result from using an ideal IGBT instead of the IGBT model. Since the length of the commutation time is decided by the $\frac{L}{R}$-time constant, not using an IGBT model with an accurate conduction characteristic will result in the commutation time being inaccurate. When using the ideal IGBT model, more current was flowing through the SiC MOSFET cell than what would have been the case if the IGBT model had been used, which necessitated the use of triangle similarity in order to correct for the discrepancy. This implies that the effective resistance of the ideal IGBT is an overestimation of the effective resistance of the IGBT model. Consequently, the commutation time will be underestimated. It is difficult to predict by how much the commutation time has been underestimated, but given that it seems like the effective resistance of the ideal IGBT is about double of what would have been the case if an accurate conduction model was used, it is definitely underestimated by a non-negligible amount. However, it is important to note that this underestimation will not spoil the results from the commutation tests, since the general trend which was uncovered will not be affected by the underestimation. In short, the initial value of the commutation time is underestimated, but the trend shown in Figure 4.12 still holds.

All of these sources of error put together makes it challenging to ascertain if the approximations that will be used to model the HyS in the thermal simulations accurately describes the components that are used. Since some sources of error leads to underestimation, and other leads to overestimation, it is also difficult to gauge if the thermal simulations will over- or underestimate the performance of the HyS. Consequently, how accurately the thesis can assess how well this specific combination of components works as a HyS in a high-power converter is, to a certain extent, limited. Therefore, caution is advised when trying to design the HyS based solely on the findings of this thesis. However, even though the thesis might not necessarily be able to give a definitive answer to exactly how an HyS con-

sisting of a *5SNA 3600E170300* IGBT in parallel with certain number of *C2M0045170P* will perform for the given specifications, it will be able to answer how the different parameters of the HyS will affect its performance, and by how much. And this data will be very valuable when trying to realize the HyS concept in a high-powered converter, since it builds a foundation which will indicate what kind of behaviour should be expected by the HyS for different operating conditions. This can then be used to interpret which parameters should be minimized or maximized when realizing the HyS in order to optimize its performance.

5.3 Analysis of Thermal Simulations

In this section, the results from the thermal analysis, found in section 4.3, will be discussed and analyzed. Like with section 5.2, the section will be divided into two subsections. The first subsection will analyze the results, compare them with theory, and discuss the significance of the results in relation to the research question. This subsection will also examine the accuracy of the hypothesis of the thesis, and if anything deviates from it, why there is a deviation will be discussed. In the second subsection, the method and approximations used during the thermal simulations will be critically examined in order to ascertain the limitations and sources of error of the results. The consequences of these errors will then be assessed in order to determine if they will have a detrimental effect to the conclusions drawn in regards to the research question.

5.3.1 Results compared to theory

The results from the thermal simulations represents the key findings of the thesis. Specifically, the results from the parametric sweep shown in Figure 4.13 is significant in order to properly address the research question. First of all, the results from the figure immediately confirms the first part of the research question: The HyS does function in a high-power converter. This also aligns with the first part of the hypothesis, which stated that the HyS was expected to work in a high-powered converter. With this finding established, the second part of the research question can be tackled. By how much can the maximum achievable switching frequency, $f_{sw,max}$, be increased by using the HyS? In order to properly answer this, the trends and patterns in each of the four charts will first be assessed separately, in order to establish how each parameter affects the performance of the HyS. Subsequently, the overall significance the results has for the optimal design of a HyS will be discussed, which will culminate in a proposal for how to design a high-powered system which will use the HyS solution.

First, the significance of the load current level will be assessed. As can be seen in Figure 4.13a, the higher the load current is, the lower the maximum achievable switching frequency. This was expected, as the same trend was found by [28], seen in Figure 2.23, and is caused by the power transients experienced by the SiC MOSFETs during the switching instances. However, there are some important differences, the first of them being the voltage ratings, as the voltage rating used in this thesis, 1700 V, was significantly larger than the one used by [28], 600 V. In general, a high-voltage IGBT has significantly larger

switching losses than a medium-voltage IGBT, and the consequence of this is reflected in the results. If the results when using a current level of 60 A from the study in [28] is compared to the results when using a current level of 2000 A from this thesis, a solid comparative basis is formed since the relationship between the load current and the SiC MOSFET(s) current rating will be approximately the same for both cases. In Figure 2.23, for the chosen load current of 60 A, the switching frequency has been increased with 62 %, while for the results in this thesis, the switching frequency at the chosen current level of 2000 A has been increased by 275 %. The cause of the difference in switching frequency increase is believed to be the consequence of the different voltage levels, since the 1700 V IGBT would have much larger switching loss reduction when introducing the SiC MOSFETs than the 600 V IGBT.

Another difference between the thesis and the study in [28] is the large difference in power levels. The most notable consequence of this was the fact that while the low-powered case studied by [28] was consistently limited by power losses, the high-powered case studied in this thesis was limited by junction temperature at the highest load-current levels. Again, this finding was expected, given that the power transients through the SiC MOSFET would become exponentially larger with the significant increase in load current. This can also be seen from Figure 4.14, where the losses of the solo IGBT solution and the HyS solution are compared. The figure shows that with increased load current, a larger portion of the HyS losses are conduction losses. In fact, the conduction losses of the HyS solution are larger than the conduction losses of the solo IGBT solution for the same current level. This might seem like it contradicts the fact that the HyS leads to a conduction enhancement, as stated in subsection 2.3.1, but that is not the case. In actuality, the reason for the large conduction losses are because of the power transients. Since these occur during every switching instance, that means that the conduction losses of the HyS are not only dependent on the load current level, but also on the switching frequency of the converter. As a result, increasing the switching frequency of the converter during large load currents leads to an exponential increase in stress at the SiC MOSFETs. Furthermore, as was discussed in subsection 2.2.1, the SiC MOSFET dice that are currently available on the market do not have large current ratings, and the dice themselves are also quite small. Consequently, the thermal resistance of the SiC MOSFET dice will be relatively large, even when accounting for using several MOSFETs in parallel, meaning that the consequences of the increased power transients will be exacerbated. All of these factors combined then explains why $f_{sw,max}$ is limited by junction temperature for large load current levels.

It is worth noting that the transition from being limited by junction temperature to being limited by power loss occurs at a load current between 1000 A and 1250 A. This seems like it is not a coincidence if the total current rating of the SiC MOSFET cell is considered. The datasheet of the *C2M0045170P* states that at a temperature level of 150 °C, the current rating of a single die is 50 A, while it is 72 A for 25 °C. Given that the SiC MOSFET switching cell consists of 20 dice in parallel, the total current rating of the switching cell is somewhere between 1000 A and 1440 A, coinciding with the transition to the power loss limitation. At the moment of this transition, it is observed that the rate of change of $f_{sw,max}$ slows considerably, before it increases again. This behaviour is presumably

a direct consequence of the limitation criterion changing from power losses to junction temperature It is also observed that the rate of change of $f_{sw,max}$ slows down as the load current decreases after the limitation transition, and the maximum switching frequency even decreases when the load current is decreased from 500 A to 250 A. It is believed that this occurs as a result of the current distribution changing, with a larger fraction of the current being conducted through the SiC MOSFET cell, as is shown by Figure 4.15. As the load current decreases, the conduction characteristics of the HyS approaches that of the SiC MOSFETs, until the entire current is conducted through the SiC MOSFETs at a current level of 250 A. The consequence of this can be seen in Figure 4.14, as the switching losses becomes a more and more dominating factor of the total losses of the HyS as the load current decreases. At a load current of 250 A the switching losses dominate completely, which coincides with $f_{sw,max}$ decreasing. This behaviour is corroborated by established theory, and as can be seen in Figure 2.18, it happens because of the transition from a heavy-load condition, where the IGBT's conduction characteristics are favourable, to a light-load condition, where the SiC MOSFETs' conduction characteristics are favourable. In fact, by using Figure 4.15, it is simple to identify the sweet point current of the HyS as 460 A. Using (2.6), it can be shown that the transition from the heavy-load condition to the light-load condition occurs at a load current of 920 A, which again roughly coincides with the transition from $f_{sw,max}$ being limited by junction temperature to being limited by power loss. All of this implies that transitioning to heavy-load conditions will lead to large amounts of stress on the SiC MOSFETs. Thus it is important to identify the sweet point current of the HyS before attempting to build a custom module so that this transition can be predicted. If the behaviour of the HyS is predictable for different load levels it will help with identifying which thermal mitigation techniques should be used, and when to use them in order to obtain optimal performance. This will be elaborated upon later in the subsection.

Next, the impact of stray inductance will be assessed. From Figure 4.13b it can be seen that an increase in stray inductance quickly leads to a decrease in $f_{sw,max}$, as was expected based on the theory presented in subsection 2.3.3. Since all of the stray inductance tests were conducted using a load current of 2000 A, the switching frequency is consistently limited by junction temperature, and this will be the case for the remaining results as well. In any case, since the main effect of increased stray inductance on the performance of the HyS is slowing down the current commutation between the SiC MOSFET cell and the IGBT, the conduction losses will be increased by increasing the stray inductance. As was discussed above this will lead to a sharp decrease in $f_{sw,max}$, since the thermal development in the SiC MOSFETs will be increased significantly. By increasing stray inductance from 10 nH to 50 nH, $f_{sw,max}$ is more than halved. This is important, because 50 nH is a typical stray inductance level in an off-the-shelf IGBT module, as exemplified by the stray inductance level of the *5SNA 3600E170300* component. Furthermore, because of the large amount of SiC MOSFETs in parallel required to achieve the necessary current rating, it is within reason to expect that the stray inductance level of the HyS, if an off-the-shelf package was used, would be even higher than 50 nH. Not only will the large amount of SiC MOSFETs increase the size of the current loop, but the number of interconnects would increase substantially. Both of these factors will lead to an increase in stray inductance, as stated in subsection 2.2.2. As seen from the results, as the stray inductance approaches 100

nH, which is not unheard given what was mentioned above, $f_{sw,max}$ of the HyS solution will actually drop below the switching frequency of the solo IGBT solution. Consequently, it is apparent that using off-the-shelf packaging will lead to unacceptable performance for the HyS, and the use of the novel packaging and parasitic mitigation techniques discussed in subsection 2.2.2 will be a necessity if the potential of the HyS is to be fully exploited. This finding is in alignment with what was stated in the hypothesis; that the HyS can not be optimally utilized if it is put together using only off-the-shelf components.

Continuing with assessing the findings of the thermal simulations, how the number of SiC MOSFETs in parallel affects $f_{sw,max}$ will be examined next. As seen in Figure 4.13c, increasing the number of SiC MOSFETs in parallel does increase $f_{sw,max}$ of the HyS. Again, this is expected, as increasing the number of SiC MOSFETs means that the current will be distributed among the MOSFETs, decreasing the thermal stress experienced by the MOSFET dice. The most notable aspect of this relationship is the fact that it is seemingly linear, making it easy to predict how much $f_{sw,max}$ will increase when adding SiC MOSFETs, or vice versa. This trait is helpful when trying to realize the HyS concept, as predictability is conducive to the ability of making informed decisions. In terms of selecting the amount of SiC MOSFETs in parallel, this decision revolves around a question of cost and bulk. The limit on how many SiC MOSFETs can be used in parallel is mostly tied to cost, and by increasing the maximum switching frequency, the size of passive components can be decreased, as seen in (2.3). This will obviously lead to cheaper passive filters, and the choice of how many SiC MOSFETs are used can be taken purely from a cost reduction perspective, i.e. choosing the number of SiC MOSFETs that gives the optimal relationship between MOSFET cost and passive component cost. Then there is the secondary aspect involved; that the decrease in the size of passive components will lead to a less bulky system. Depending on what application the HyS will be used for, there might be a desire to increase cost in order to insure a system which reduces bulk to a minimum. This is especially relevant for e.g. the transport sector, among others. Thus the choice of number of SiC MOSFETs in parallel boils down to a combination of cost optimization, and how much a user is willing to pay for reduced bulk.

The final parameter of the parametric sweep was the duty cycle of the converter. Figure 4.13d shows that increasing the duty cycle leads to a lower $f_{sw,max}$. This happens because of an increased duty cycle leads to the switch in question being on for a longer fraction of the switching period. This has ramifications specifically for the SiC MOSFETs of the HyS. Because, while neither the switching losses nor the conduction losses of the HyS increases with an increase in duty cycle, the thermal development in the SiC MOSFET dice does. With the HyS being in the ON-state for a larger fraction of the switching period, the SiC MOSFETs are afforded less time to ”rest”, i.e. the SiC MOSFETs has to conduct current for a longer time during each switching cycle, which increases thermal development. The consequence of increased duty cycle leading to decreased $f_{sw,max}$ is that the passive components has to be designed in accordance with the maximum duty cycle that will be used for the application in question. Luckily, the relationship between $f_{sw,max}$ and duty cycle is also linear, at the very least within the interval in question. This means that it should be simple to take the duty cycle into account when designing a system containing a HyS solution. In general, in order to take the duty cycle into account when

designing an application using the HyS, the maximum duty cycle which is intended for use in the application should be identified. Then, the passive components used for the application should be dimensioned for $f_{sw,max}$ which is attainable using this duty cycle level.

While the results from Figure 4.13 are incredibly important, these parameters are not the only factors that play a role in the performance of the HyS. Since most of the time the HyS's $f_{sw,max}$ was limited by junction temperature, it is clear that using as effective cooling as possible will have a beneficial effect on the performance of the HyS. Figure 4.16 shows the effect of modifying the thermal resistances in the thermal network of the HyS. Figure 4.16a shows the effect of changing the attach material. While the difference between the best and the worst option is not remarkable, it is still worth using the best attach material possible since it is a simple way to slightly boost the performance of the HyS. In contrast, changing the cooling method of the module can have a drastic effect on performance. As shown in Figure 4.16b, decreasing the equivalent thermal resistance from heat sink to ambient by 50 $\%$ enables a $f_{sw,max} \approx 21$ kHz, or an increase of 85.8 $\%$. This is significant, since this decrease in thermal resistance corresponds to using double sided cooling, as discussed in subsection 2.2.1, meaning that such a drastic reduction is within the realm of possibility. What is more, using double sided cooling in conjunction with direct liquid cooling should make it possible to reduce the thermal resistance even further. Since more efficient cooling has such a profound effect on $f_{sw,max}$, optimizing cooling capabilities should be one of the foremost priorities when designing a system which uses the HyS solution.

Proposal for design process

A comprehensive parametric sweep of a an HyS like what has been conducted in this thesis is something that has not been done in literature before, especially for the large current levels that have been used. Therefore, this thesis provides a solid foundation for how to proceed when designing a high-power system using the HyS solution. A proposal for the design process of a high-powered system using the HyS with the goal of achieving maximum $f_{sw,max}$ will therefore be presented next. The proposal will focus on optimizing $f_{sw,max}$, but if minimizing power losses is prioritized instead, then the switching frequency should be adjusted accordingly within the switching frequency interval between $f_{sw,max}$ and the switching frequency used for the solo IGBT solution the HyS is replacing.

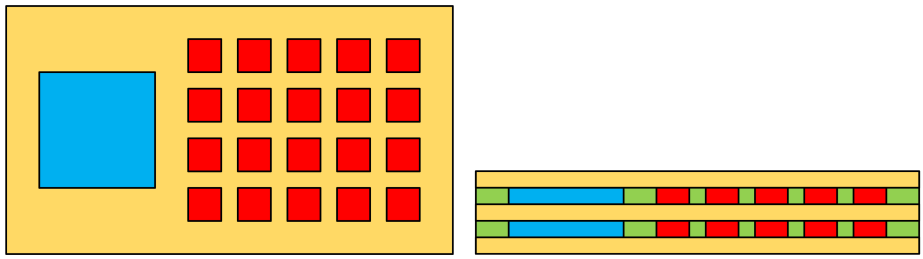
First of all, it is essential to have a complete overview of the system that the HyS will be used in. Not only are the specifications necessary, but the maximum duty cycle is also important to determine. As was shown by the duty cycle analysis, this is necessary in order to properly dimension the passive components of the system. Furthermore, if it is suspected that the duty cycle will exceed 0.8 for prolonged periods, it might not be a system that is suited for the HyS because of the thermal limitations of the solution. With the profile of the system established, the HyS itself needs to be designed. This entails determining how many SiC MOSFETs are needed, which can be determined by for example using the current optimization algorithm shown in Figure 2.25, and the delay timings t_1 and t_2 also needs to be determined. However, if optimal performance of the

HyS is desired, these delay timings should be dynamically varied, which will be discussed later. It is also worth noting that the IGBT used in the system should not be overrated, since this would lead to a nonoptimal conduction profile, leading to unnecessary stress on the SiC MOSFET chips during steady-state conduction. Additionally, the cooling system of the application needs to be established before the current ratio optimization, since the optimization is dependent on cooling efficiency. As discussed previously, it is desirable to maximize cooling efficiency in order to maximize $f_{sw,max}$. This is done by using double sided cooling. With double sided cooling in place, direct liquid cooling, or another technique that offers equal or better cooling efficiency should be used in order to optimize performance. Moreover, increasing the efficiency of cooling has a secondary effect, as it allows for the use of lighter heat sink since the heat will be dissipated to ambient faster. As a result, both the cost and the bulk of the system can be decreased, which is desirable when designing a system which is intended for use in industrial applications.

Next, it is essential that these devices are in the same package in order to minimize the stray inductance of the system. If the stray inductance is too large, the HyS will not reach the desired performance, as mentioned in the stray inductance discussion. In addition, it is important that the layout of the module is symmetrical, so that the current can be distributed as uniformly as possible. Since the SiC MOSFETs are sensitive to thermal development, uneven current distribution can quickly lead to degradation for individual chips, which will eventually lead to complete thermal breakdown for the SiC MOSFET cell. The importance of symmetry also necessitates the use of a powerful gate driver, which needs to be able to turn on and off the MOSFETs at more or less the exact same time, with a current of around 100 A going through each chip. Designing this gate driver is outside the scope of this thesis, but it still essential for the performance of the HyS. The gate drivers for the HyS should also use Miller clamps in order to avoid the accidental turn-ON problem encountered in subsection 3.2.1. Furthermore, the custom module should be designed in a way that allows for double sided cooling, using planar interconnection techniques as discussed in subsection 2.2.2.

In Figure 5.4, a proposal for the layout of an HyS custom half-bridge module containing 20 SiC MOSFETs in parallel is presented. As seen in Figure 5.4a, the SiC MOSFETs are placed perfectly symmetrical, and the different chips, both the IGBT and the SiC MOSFETs, are placed as close each other as is allowed by the thermal development in the module. This allows for stray inductance minimization, as well as optimal heat flow. The distance between chips presents another optimization problem, which needs to be solved through the use of thermal simulations. The proposed module also uses a type of CoC structure to further minimize the stray inductance in the module, as shown by the cross section in Figure 5.4b. Using this structure, the drain of the first switching position with the low side HyS is connected to the lower substrate plane, while the source of the low side HyS is connected to the middle substrate plane. Similarly, the drain of the second switching position with the high side HyS is connected to the middle substrate plane, while the source of the high side HyS is connected to the upper substrate plane. The current flows vertically from the drain through the first switching position, upwards to the middle substrate plane which functions as the output, and finally to ground through the second switching position. Interconnection between chips on the same substrate plane is done

using planar interconnection techniques, for example copper traces. This is a combination of the wireless and CoC structures shown in Figure 2.14, and is conducive to both stray inductance mitigation and to using double sided cooling.



(a) Layout **(b)** Cross section

Figure 5.4: Proposed layout for HyS custom module. Blue denotes IGBT, while red denotes SiC MOSFET

Lastly, after having established the design of the custom module and the cooling system, the choice of a control strategy that enables the HyS to reach peak performance should be considered. In order to fully capitalize on the characteristics of the HyS, different control strategies should be employed for light-load conditions and heavy-load conditions. Since light-load conditions does not lead to problematic thermal development, the control strategy should focus on optimizing the efficiency of the system in accordance with (2.8), since that will lead to lower losses, and therefore a higher maximum switching frequency. In contrast, during heavy-load conditions the thermal balance control mode proposed by [29] should be used. This strategy balances the temperature in the IGBT and SiC MOSFET cell using (2.9), and in theory that means that some of the heat in the SiC MOSFET cell could be sunk into the IGBT. By examining Table D.8 to Table D.13, it becomes apparent that a temperature difference between the SiC MOSFETs and IGBT is often present, and if this difference was evened out, the switching frequency could have been increased even further. The simplest way to implement this adaptive control strategy would be to allow the control system to dynamically change t_1 and t_2, since the switching and conduction losses of both the SiC MOSFET and the IGBT are dependent on these variables. Thus, by dynamically changing the delay durations, the performance of the HyS can be optimized in accordance with the conditions experienced by the system in question.

5.3.2 Limitations and sources of error

The limitations and sources of errors of the thermal simulations will be discussed in this subsection. Like with the electrical simulations, some small margin of error needs to be expected solely because of the measurement methods used. However, since thermal dynamics are much slower than electrical dynamics, this error source plays an even smaller role than the case in the electrical simulations. The difference of a couple degrees Celsius is not the difference between a working system and a system in complete failure, and since thermal development happens slowly, a large error is needed in order to increase or

decrease the temperature in a manner that is non-negligible. Thus, the error source related to measurement methods is considered to be of little to no importance, even if there is a compounding effect with the measurement errors from the electrical simulations.

The most important aspect to discuss with the thermal simulations, are the limitations of the PLECS software itself. As was mentioned in chapter 3, PLECS uses only idealized waveforms during simulations. While this greatly enhances simulation speed, it also makes it impossible to model some of the behaviours of the HyS that would have an effect on its performance. As a result, a number of approximations were used in order to emulate these behaviours. The most notable of these approximations was the calculation of the commutation time, seen in (3.4). This approximation was based off the triangle approximation discussed in subsection 5.2.2, and thus the error analysis in Table 5.1 also applies to this approximation. However, as was established in the previous analysis, even though the commutation time has been overestimated, it is impossible to precisely quantify by how much the switching losses have been over or underestimated due to the different sources of errors present in the electrical simulations. Conversely, the other two approximations used in the commutation time approximation, the inductance approximation and the number of MOSFETs approximation, can be confidently assumed as accurate given that Figure 4.12 and Figure 4.8 demonstrated linear relationships for the two approximations. In any way, every inaccuracy tied to the commutation time approximation is related to inaccuracies during the electrical simulations, which have already been analyzed.

Another error source that originates from the PLECS limitations is that the current waveform is square. In a realized application this would not be the case, since the load would be inductive to some degree. An inductive load results in a triangular waveform, and not in a square waveform. It was attempted to recreate this triangular waveform in PLECS, but that required the use of capacitors in parallel with a voltage source, creating dependent variables that PLECS was unable to solve in a manner conducive to thermal simulations since the simulation was slowed down considerably. As a consequence, using square waveforms for the current was deemed as an acceptable compromise between accuracy and speed. By using square current waveforms, the conduction losses would be either over- or underestimated depending on the duty cycle of the converter. With a duty cycle of $D = 0.5$, the ON-time and OFF-time of the switching period would be exactly the same, which means that the area of the square waveform and the triangular waveform would also be the same, therefore no over- or underestimation. However, if the duty cycle was below 0.5, the OFF-time would exceed the ON-time, and the area of the triangle would exceed the area of the square, leading to an underestimation of the conduction loss. Conversely, using a duty cycle exceeding 0.5 would lead to the ON-time being larger than the OFF-time, and the area of the square would exceed the area of the triangle, leading to an overestimation of the conduction loss. Since the default value of the duty cycle was chosen to be $D = 0.5$, the choice of using square waveform had more or less no effect on the results of the simulations. Only during the the duty cycle sweep would the shape of the waveform had an effect. However, since the duty cycle sweep interval did not include the extreme ends of the duty cycle, it is not believed that these inaccuracies would have mattered much, leading to a slightly too high $f_{sw,max}$ for the results where $D < 0.5$, and vice versa.

Continuing with sources of errors originating from PLECS's limitations, the current dis-

tribution between the SiC MOSFET cell and the IGBT would change depending on the respective devices' junction temperature. From subsection 2.1.3, it was established that with higher temperature, the conduction characteristics of the IGBT would become more and more favourable in relation to the conduction characteristics of the SiC MOSFET, and in Figure 2.18 it is shown that this results in the sweet point current decreasing with temperature. This behaviour is not possible to capture using PLECS, since the current distribution during steady-state conduction is entirely dependent on the relationship between the ohmic values of the devices in question, and these values are not temperature dependent. As a result of this limitation, it was decided to determine the current sharing between the switching cells based on simulations done with a device temperature of 150 °C. As explained in subsection 3.2.1, this was done because it was suspected that the junction temperature of the devices would be quite high in most of the thermal simulations. This suspicion was proven to be true, but as the results in Table D.8 to Table D.13 shows, the temperature is at times quite a bit lower for the IGBT. In theory, this means that the sweet point current has been underestimated, leading to an underestimation of the steady-state conduction losses for the SiC MOSFET. Therefore, this error source would result in an overestimation of $f_{sw,max}$ in cases where the IGBT junction temperature is significantly lower than 150 °C. It is challenging to quantify the exact overestimation, but it is unlikely that the results would have been affected to such a degree that the conclusions from subsection 5.3.1 would be changed in any appreciable manner.

The final error source that will be discussed in this analysis, is the fact that the current has been assumed uniformly distributed throughout the SiC MOSFET cell. This assumption was present during both the electrical and thermal simulations, but the consequences of it not holding is more severe for the thermal simulations than for the electrical ones. As was briefly mentioned in subsection 5.3.1, if current is unevenly distributed, this can quickly lead to a thermal breakdown in the SiC MOSFET cell. This can be mitigated by a symmetrical module layout, since a symmetrical layout is conducive to a symmetrical stray inductance distribution within the SiC MOSFET cell. For the HyS in a high-powered converter, this is especially challenging. Not only does the large current level mean that current imbalances has severe consequences, but the large amount of SiC MOSFET in parallel makes it even more challenging to uniformly distribute the current. Furthermore, as was mentioned in subsection 2.2.2, the faster the switching frequency, the lower the tolerance for asymmetry. Seeing as the switching frequency of the HyS for 2 kA load current is approximately 11 kHz with 20 SiC MOSFETs in parallel, as seen in Figure 4.13a, it becomes clear that designing a ultra symmetrical layout for the HyS custom module will be important, and presents one of the major practical challenges for realizing the HyS concept in a high-powered converter. In Figure 2.15, the results of a study by [23] which examined this exact problem can be seen. The study found that using 10 paralleled modules with a total of 50 SiC MOSFETs with a switching frequency of 20 kHz only lead to a small difference in temperature between the different MOSFET cells, which indicates that it is definitely possible to design a custom module with the necessary symmetry. However, there is an important difference between the MOSFETs from the study in [23], and the one in the HyS switching cell: The current level. Because while the maximum current through a MOSFET module in [23] is around 50 A, which is less than a third of the current rating of the modules in question, the SiC MOSFETs in the HyS conducts 100 A, which is double

the current rating of the MOSFET if the junction temperature approaches maximum. This difference implies that the SiC MOSFETs in the HyS will be more sensitive to asymmetry than the ones from [23], further emphasizing the challenge present when designing the custom HyS module.

All of the sources of error that has been discussed in this subsection in conjunction with the sources of error from the electrical simulations underscores the assessment from subsection 5.2.2; that the tools used in this thesis might not be be suitable for determining the performance of a specific HyS design. Because while the combination of PLECS and Simscape was excellent for determining the general behavioural patterns of the HyS, the accuracy in simulating a specific design is not ideal. Accordingly, it might be preferable to use a more sophisticated simulation software when looking to realize a specific HyS design. The design process described in subsection 5.3.1 is still viable, and could be used as a manual for designing a HyS for use in a high-power converter. In the parts of the design process where simulations are necessary in order to realize the HyS, for example when using the current ratio optimization algorithm from Figure 2.25, other simulation software than the Simscape/PLECS combination should be used. Since the general behavioural patterns of the HyS have already been determined in this thesis, and have been accounted for in the proposed design process, there will not be a need for parametric sweeps and similar time consuming simulation processes, meaning that simulation speed can be lowered in favour for increased fidelity. For example, SPICE software could be used for electrical simulations instead of Simscape, while finite element method (FEM) simulations could be used for thermal simulations instead of PLECS. Using these software would allow for the elimination of some of the more egregious sources of errors present when using the Simscape/PLECS combination, like for example the problems related to stray inductance.

Chapter 6

Conclusion and Further Work

6.1 Conclusion

This master thesis has investigated the general behavioural patterns of the Si-SiC hybrid switch concept in order to ascertain if the configuration would be viable in a high-power converter. The research question of the thesis asked if HyS could actually function in such a converter, and if it did, by how much the maximum switching frequency, $f_{sw,max}$, could be increased. Furthermore, it was stated that the major practical challenges for realizing the HyS solution should be identified. Through the use of electrical and thermal simulations, using Simscape and PLECS respectively, a parametric sweep was performed in order to establish the relationship between selected parameters and $f_{sw,max}$ of the HyS.

The parametric sweep first of all revealed that the HyS solution is indeed viable in a high-powered converter, given that it enabled a 275 $\%$ increase in switching frequency for the maximum load level of 2 kA. This aligns with what was stated in the hypothesis, were it was stated that the HyS should significantly increase the switching frequency of a the converter. However, this large increase only holds for a low total stray inductance of $L_\sigma = 10$ nH. If the stray inductance is increased, $f_{sw,max}$ will fall rapidly. This puts the cost effectiveness of the HyS into question, since the justification for using the expensive SiC MOSFETs is to decrease the size of the passive components in the system by increasing the switching frequency. If this increase is unsubstantial, the reduction in cost related to the decrease in passive component size might not offset the increased costs related to the SiC MOSFETs, making the HyS solution economically nonviable. As a consequence, it becomes essential to limit the total stray inductance of the HyS to 10 nH or below. This is not possible using the packaging solution which are currently commercially available, and thus a custom module design is required. Again, this is in alignment with the hypothesis.

As the conclusion above demonstrates, the hypothesis of the thesis has been shown to be

true based on the results from the electrical and thermal simulations. Given that the results showed that a custom module is necessary, the major challenges for realizing a custom HyS module was identified. At the forefront of the custom module design challenges is parasitic inductance mitigation, since novel module design is required in order to reduce stray inductance to the levels necessary for the required HyS performance. This includes the use of planar interconnection techniques replacing the commonly used wirebonds. In addition, the low current ratings of commercially available SiC MOSFETs forces the use of several SiC MOSFET chips in parallel to reach the desired current rating. In a parallel connected configuration, it is essential to achieve as close to uniformly distributed current as possible in order to avoid thermal breakdown. Therefore, the tolerance for inductance imbalance between the parallel connected SiC MOSFETs becomes lower with increased switching frequency, since inductance imbalances leads imbalanced current distribution. This necessitates the use of extremely symmetrical module layouts in order to uniformly distribute the stray inductance of the module. It also requires the use of a powerful gate driver, since all of the SiC MOSFETs needs to turn on and off at the same time, at current levels more than double that of the SiC MOSFET chips' current rating. Furthermore, the thermal management of the HyS is an important challenge, since the thesis found that $f_{sw,max}$ of the HyS was limited by the SiC MOSFETs' junction temperature at heavy-load conditions. This means that there is a potential for increased switching frequency if more efficient cooling is employed. Again, this requires the use of novel techniques, such as double sided cooling, which is only possible if wirebonds are eliminated, and direct liquid cooling which significantly reduces the thermal resistance between the heat sink and ambient. It is also possible to employ control strategies designed to optimize the thermal performance of the HyS. In short, the major challenges for realizing the HyS concept amounts to:

- Parasitic inductance mitigation using planar interconnection techniques.
- Designing a symmetrical module layout to avoid uneven current distribution.
- Designing a gate driver that is able to perform the switching actions in a satisfactory manner at the required current level.
- Optimize the cooling efficiency of the system using for example double sided cooling.

6.2 Further Work

While this thesis has established the general behavioural patterns of the HyS in a high-powered converter, as well as identified the major design challenges for realizing the concept, it does have limitations related to realizing a specific design. Furthermore, the thesis has not been able to investigate the feasibility of the various novel techniques which have been presented as possible solutions for these design challenges. Therefore, further work should focus on verifying if the design process proposed in subsection 5.3.1 will be able to create a viable HyS design.

Following the proposed design process should enable the production of an actual custom

HyS module, and the effectiveness of the parasitic inductance mitigation techniques, the various cooling techniques, and the proposed adaptive control strategy can all be verified. Another important aspect that can be tested is how problematic the large amount of SiC MOSFETs in parallel will be for the HyS performance. If the requirement for a symmetrical layout turns out to be too strict, it should be considered if it would be preferable to wait for higher rated SiC MOSFETs to become available before attempting to use the HyS solution in a high-power converter. The requirements of the gate drivers needed to operate the HyS should also be investigated, and it should be established if using commercially available gate drivers will enable the HyS to perform satisfactorily or if a custom design is needed for the gate driver as well. Finally, by designing a custom module based on the design process presented in this thesis, it could also be possible to test for how impactful the various sources of errors discussed in subsection 5.2.2 and subsection 5.3.2 will be for the performance of the HyS.

To sum up, further work should attempt to build a HyS module using the design process in this thesis, and focus on answering the following:

- Are the parasitic inductance mitigation techniques proposed in this thesis able to reduce the stray inductance to a level that is conducive to optimal HyS performance?
- By how much can the cooling efficiency be increased by using double sided cooling in tandem with a novel cooling technique like direct liquid cooling, and how does this increase in cooling efficiency affect HyS performance?
- To what degree will using the proposed adaptive control strategy increase the performance of the HyS?
- Is it possible to design an HyS layout with the symmetry required to achieve uniform current distribution with the SiC MOSFETs that are currently available on the market?
- Are custom gate drivers needed in order to operate the HyS satisfactorily, or is the use of commercially available, off-the-shelf gate driver units an acceptable solution?

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Appendices

Appendix A

Datasheets

A.1 C2M0045170P

In the following pages, the datasheet for the Wolfspeed SiC MOSFET, *C2M0045170P*, has been attached. This datasheet was retrieved from [33].

CREE

C2M0045170P

Silicon Carbide Power MOSFET
C2M™ MOSFET Technology

N-Channel Enhancement Mode

V_{DS}	1700 V
$I_{D\ @\ 25^{\circ}C}$	72 A
$R_{DS(on)}$	45 mΩ

Features

- Optimized package with separate driver source pin
- 8mm of creepage distance between drain and source
- High Blocking Voltage with Low On-Resistance
- High Speed Switching with Low Capacitances
- Easy to Parallel and Simple to Drive
- Halogen Free, RoHS Compliant

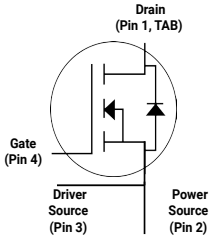
Benefits

- Reduce switching losses and minimize gate ringing
- Higher system efficiency
- Reduce cooling requirements
- Increase power density
- Increase system switching frequency

Applications

- 1500V Solar Inverters
- Switch Mode Power Supplies
- High Voltage DC/DC converters
- Pulsed Power Applications

Package



Part Number	Package	Marking
C2M0045170P	TO-247-4 Plus	C2M0045170P

Maximum Ratings (T_C = 25 ˚C unless otherwise specified)

Symbol	Parameter	Value	Unit	Test Conditions	Note
V_{DSmax}	Drain - Source Voltage	1700	V	V_{GS} = 0 V, I_D = 100 µA	
V_{GSmax}	Gate - Source Voltage (dynamic)	-10/+25	V	AC (f >1 Hz)	Note: 1
V_{GSop}	Gate - Source Voltage (Static)	-5/+20	V	Static	Note: 2
I_D	Continuous Drain Current	72	A	V_{GS} =20 V, T_C = 25˚C	Fig. 19
		48		V_{GS} =20 V, T_C = 100˚C	
$I_{D(pulse)}$	Pulsed Drain Current	160	A	Pulse width t_P limited by T_{jmax}	Fig. 22
P_D	Power Dissipation	520	W	T_C=25˚C, T_J = 150 ˚C	Fig. 20
T_J , T_{stg}	Operating Junction and Storage Temperature	-40 to +150	˚C		
T_L	Solder Temperature	260	˚C	1.6mm (0.063") from case for 10s	

Note (1): When using MOSFET Body Diode V_{GSmax} = -5V/+25V
Note (2): MOSFET can also safely operate at 0/+20V

Electrical Characteristics (T_C = 25˚C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	1700			V	V_{GS} = 0 V, I_D = 100 µA	
$V_{GS(th)}$	Gate Threshold Voltage	2.0	2.6	4	V	V_{DS} = V_{GS}, I_D = 18mA	Fig. 11
			1.8		V	V_{DS} = V_{GS}, I_D = 18mA, T_J = 150 °C	
I_{DSS}	Zero Gate Voltage Drain Current		2	100	µA	V_{DS} = 1700 V, V_{GS} = 0 V	
I_{GSS}	Gate-Source Leakage Current			600	nA	V_{GS} = 20 V, V_{DS} = 0 V	
$R_{DS(on)}$	Drain-Source On-State Resistance		45	59	mΩ	V_{GS} = 20 V, I_D = 50 A	Fig. 4,5,6
			90			V_{GS} = 20 V, I_D = 50 A, T_J = 150 °C	
g_{fs}	Transconductance		21.7		S	V_{DS}= 20 V, I_{DS}= 50 A	Fig. 7
			24.4			V_{DS}= 20 V, I_{DS}= 50 A, T_J = 150 °C	
C_{iss}	Input Capacitance		3672		pF	V_{GS} = 0 V V_{DS} = 1000 V f = 1 MHz V_{AC} = 25 mV	Fig. 17,18
C_{oss}	Output Capacitance		171				
C_{rss}	Reverse Transfer Capacitance		6.7				
E_{oss}	C_{oss} Stored Energy		105		µJ		Fig 16
E_{ON}	Turn-On Switching Energy (SiC Diode FWD)		0.67		mJ	V_{DS} = 1200 V, V_{GS} = -5/20 V, I_D = 50A, $R_{G(ext)}$ = 2.5Ω, L= 105 µH, T_J = 150 °C, using SiC Diode as FWD	Fig. 26, 29b
E_{OFF}	Turn Off Switching Energy (SiC Diode FWD)		0.31				
E_{ON}	Turn-On Switching Energy (Body Diode FWD)		2.8		mJ	V_{DS} = 1200 V, V_{GS} = -5/20 V, I_D = 50A, $R_{G(ext)}$ = 2.5Ω, L= 105 µH, T_J = 150 °C, using MOSFET as FWD	Fig. 26, 29a
E_{OFF}	Turn Off Switching Energy (Body Diode FWD)		0.35				
$t_{d(on)}$	Turn-On Delay Time		35		ns	V_{DD} = 1200 V, V_{GS} = -5/20 V I_D = 50 A, $R_{G(ext)}$ = 2.5 Ω, Timing relative to V_{DS} Inductive load	Fig. 27, 29
t_r	Rise Time		13				
$t_{d(off)}$	Turn-Off Delay Time		46				
t_f	Fall Time		10				
$R_{G(int)}$	Internal Gate Resistance		1.3		Ω	f = 1 MHz, V_{AC} = 25 mV	
Q_{gs}	Gate to Source Charge		44		nC	V_{DS} = 1200 V, V_{GS} = -5/20 V I_D = 50 A Per IEC60747-8-4 pg 21	Fig. 12
Q_{gd}	Gate to Drain Charge		57				
Q_g	Total Gate Charge		188				

Reverse Diode Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Diode Forward Voltage	4.1		V	V_{GS} = - 5 V, I_{SD} = 25 A	Fig. 8, 9, 10 Note 1
		3.6		V	V_{GS} = - 5 V, I_{SD} = 25 A, T_J = 150 °C	
I_S	Continuous Diode Forward Current		72	A	T_C= 25 °C, V_{GS} = - 5 V	Note 1
t_{rr}	Reverse Recovery Time	44		ns	V_{GS} = - 5 V, I_{SD} = 50 A , V_R = 1200 V dif/dt = 3000 A/µs	Note 1
Q_{rr}	Reverse Recovery Charge	2		µC		
I_{rrm}	Peak Reverse Recovery Current	60		A		

Note (1): When using SiC Body Diode the maximum recommended V_{GS} = -5V

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
$R_{\theta JC}$	Thermal Resistance from Junction to Case	0.22	0.24	°C/W		Fig. 21
$R_{\theta JC}$	Thermal Resistance from Junction to Ambient		40			

Typical Performance

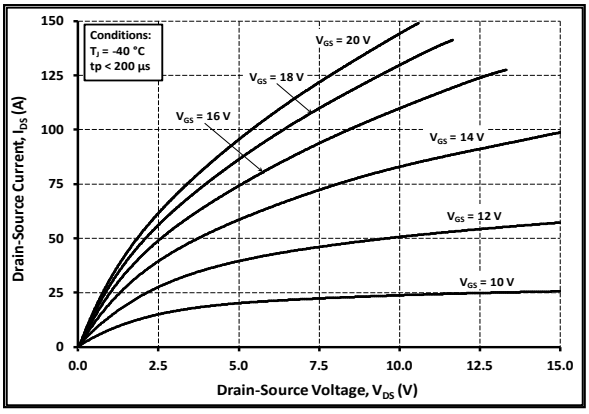


Figure 1. Output Characteristics T_J = -40 °C

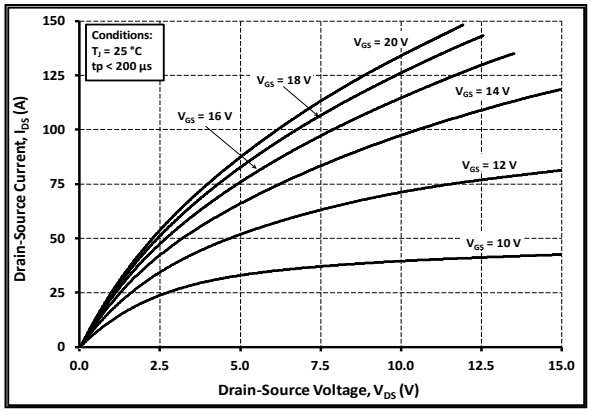


Figure 2. Output Characteristics T_J = 25 °C

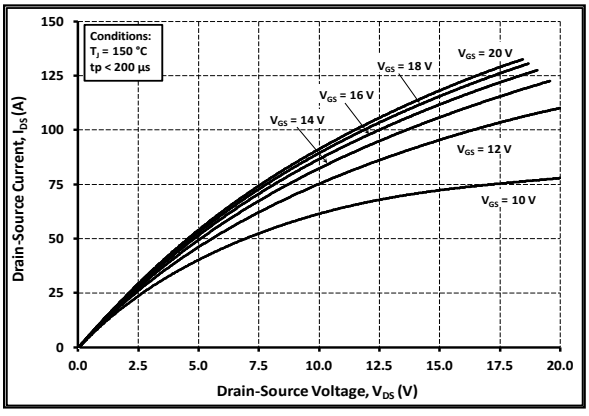


Figure 3. Output Characteristics T_J = 150 °C

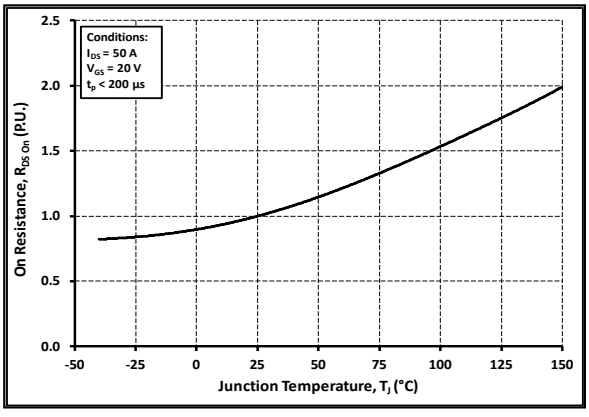


Figure 4. Normalized On-Resistance vs. Temperature

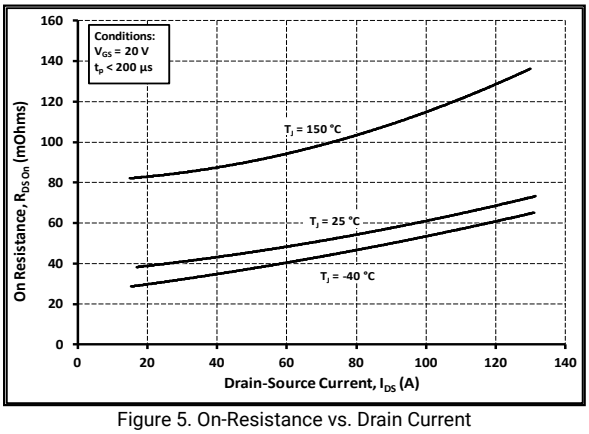


Figure 5. On-Resistance vs. Drain Current
For Various Temperatures

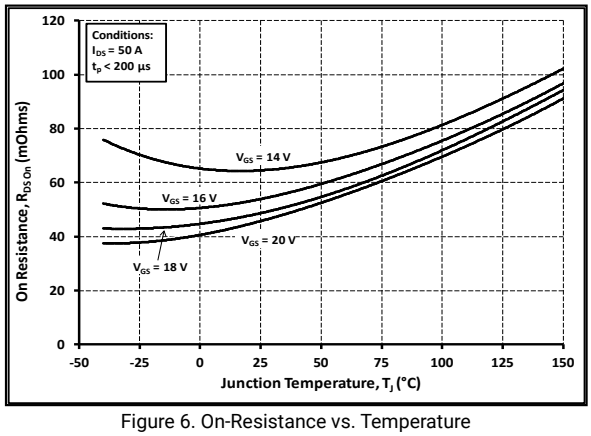


Figure 6. On-Resistance vs. Temperature
For Various Gate Voltage

Typical Performance

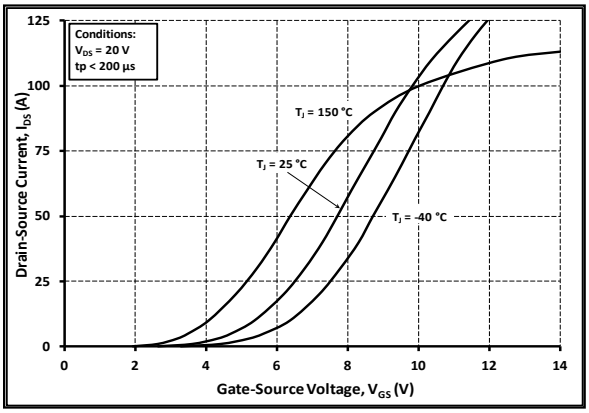


Figure 7. Transfer Characteristic For Various Junction Temperatures

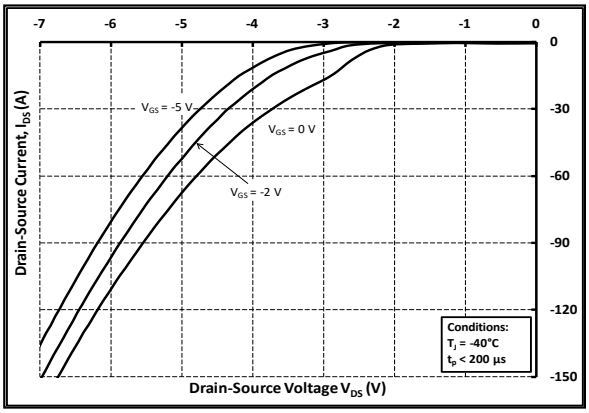


Figure 8. Body Diode Characteristic at -40 °C

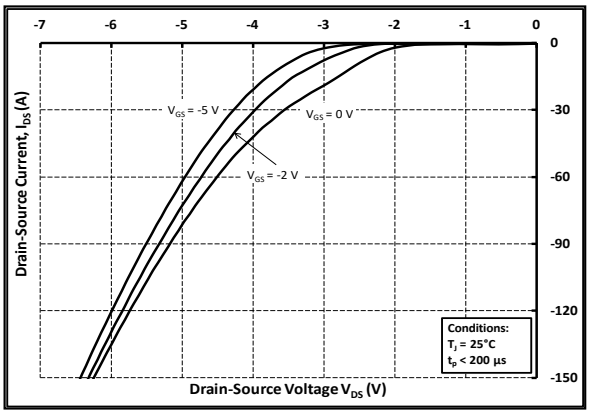


Figure 9. Body Diode Characteristic at 25 °C

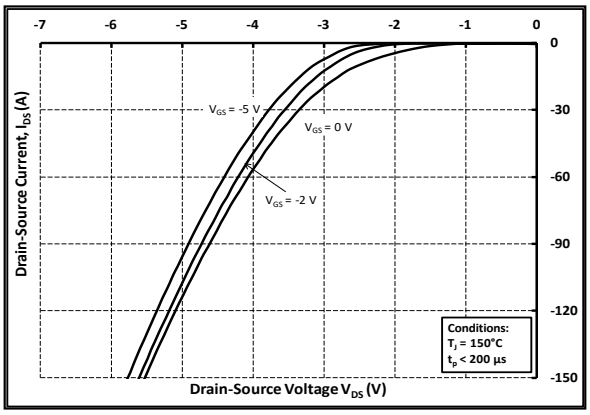


Figure 10. Body Diode Characteristic at 150 °C

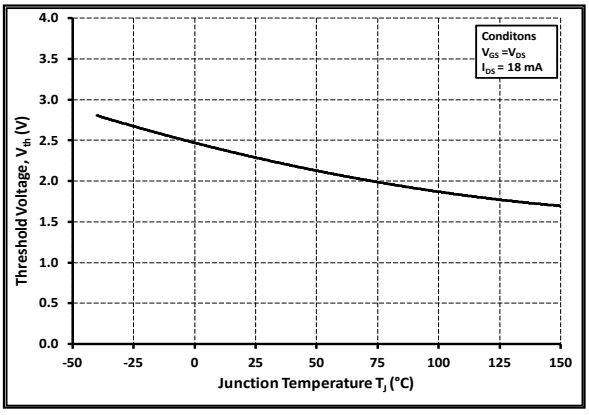


Figure 11. Threshold Voltage vs. Temperature

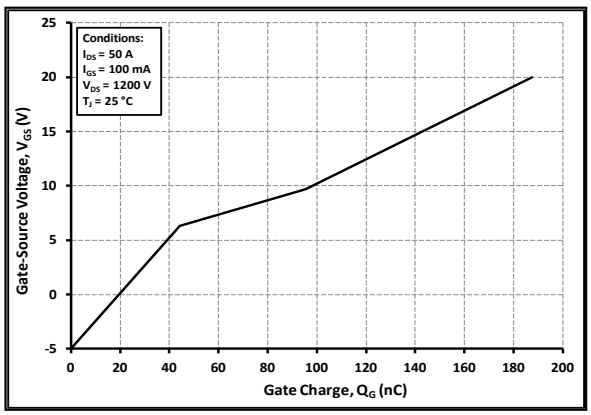


Figure 12. Gate Charge Characteristic

Typical Performance

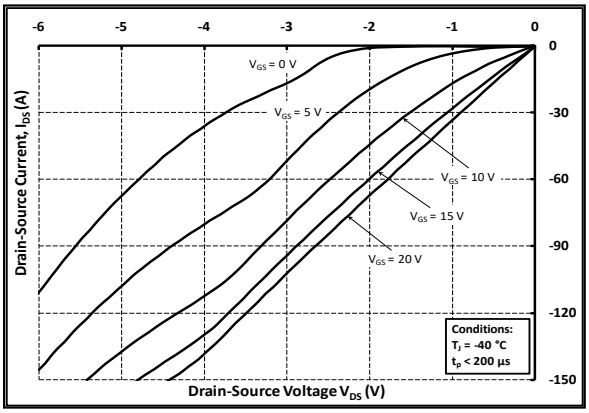


Figure 13. 3rd Quadrant Characteristic at -40 °C

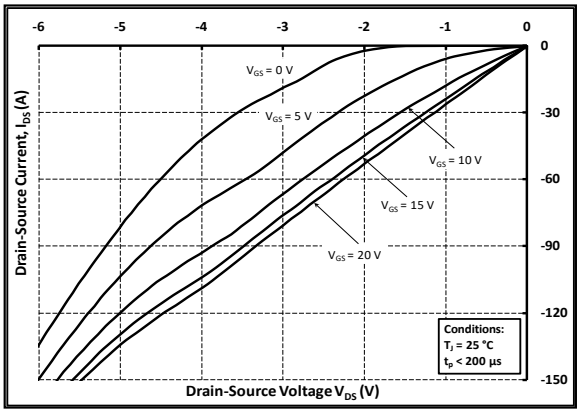


Figure 14. 3rd Quadrant Characteristic at 25 °C

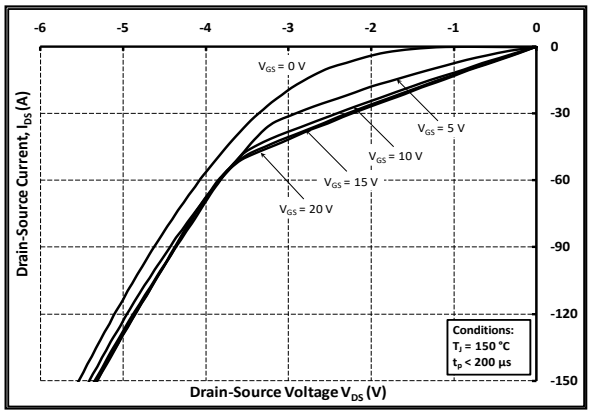


Figure 15. 3rd Quadrant Characteristic at 150 °C

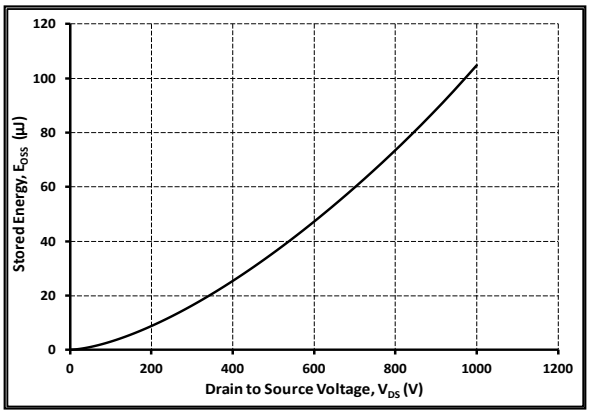


Figure 16. Output Capacitor Stored Energy

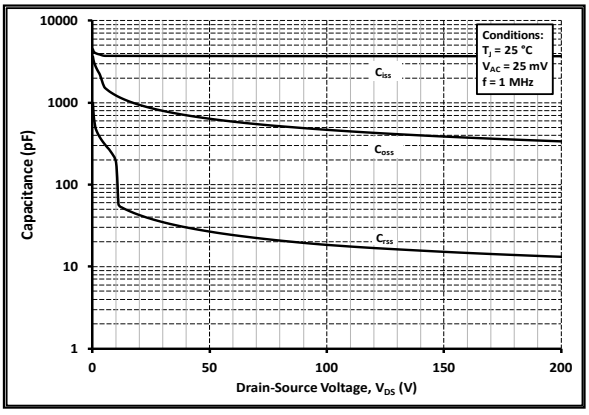


Figure 17. Capacitances vs. Drain-Source Voltage (0-200 V)

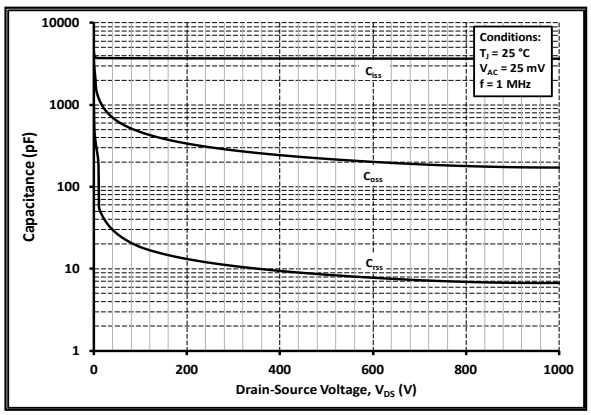


Figure 18. Capacitances vs. Drain-Source Voltage (0-1000 V)

Typical Performance

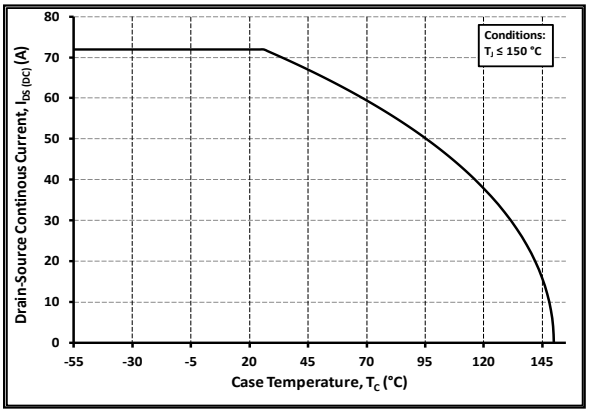


Figure 19. Continuous Drain Current Derating vs. Case Temperature

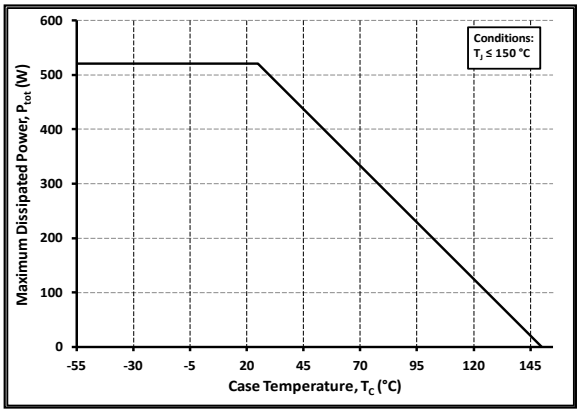


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

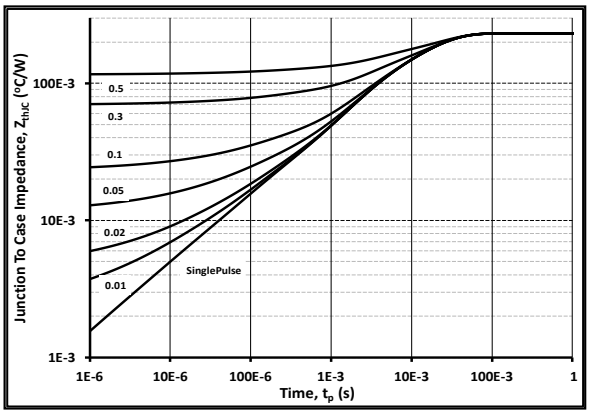


Figure 21. Transient Thermal Impedance (Junction - Case)

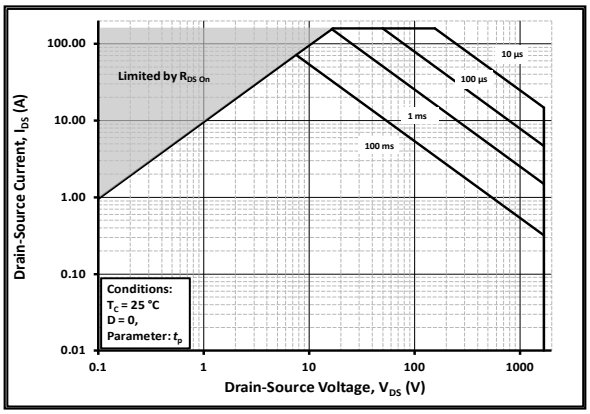


Figure 22. Safe Operating Area

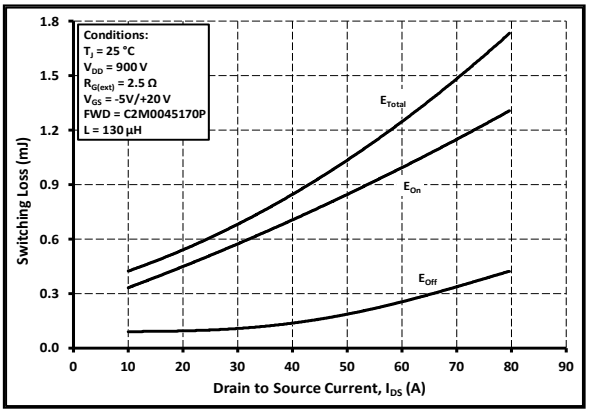


Figure 23. Clamped Inductive Switching Energy vs. Drain Current (V_{DD} = 900V)

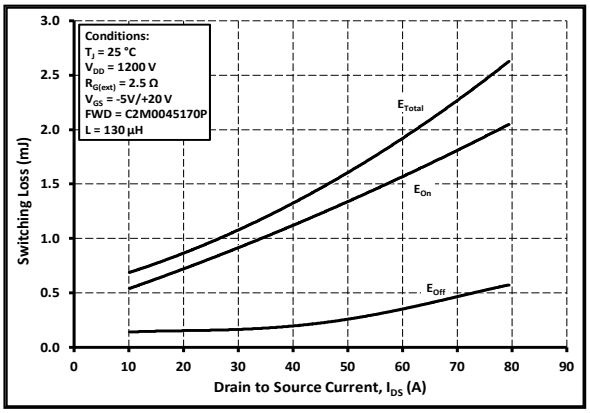


Figure 24. Clamped Inductive Switching Energy vs. Drain Current (V_{DD} = 1200V)

Typical Performance

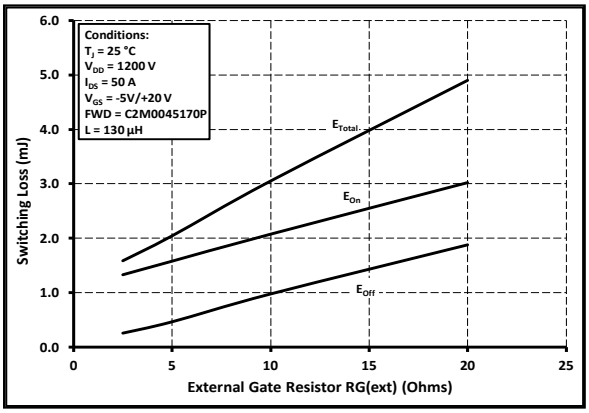


Figure 25. Clamped Inductive Switching Energy vs. $R_{G(ext)}$

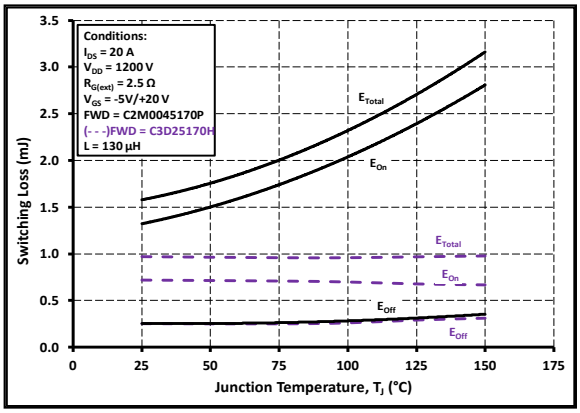


Figure 26. Clamped Inductive Switching Energy vs. Temperature

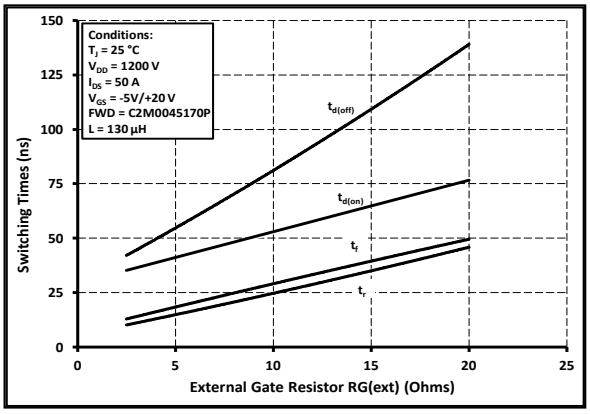


Figure 27. Switching Times vs. $R_{G(ext)}$

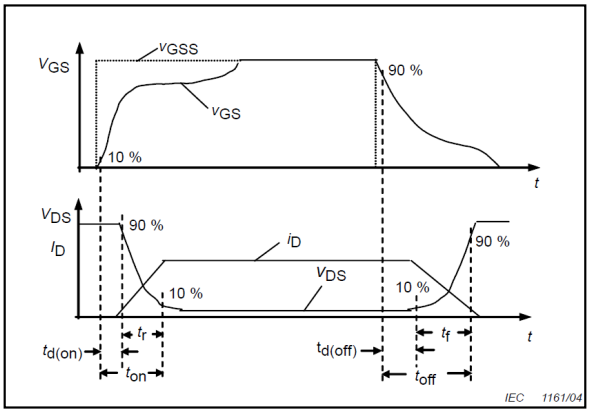


Figure 28. Switching Times Definition

Test Circuit Schematic

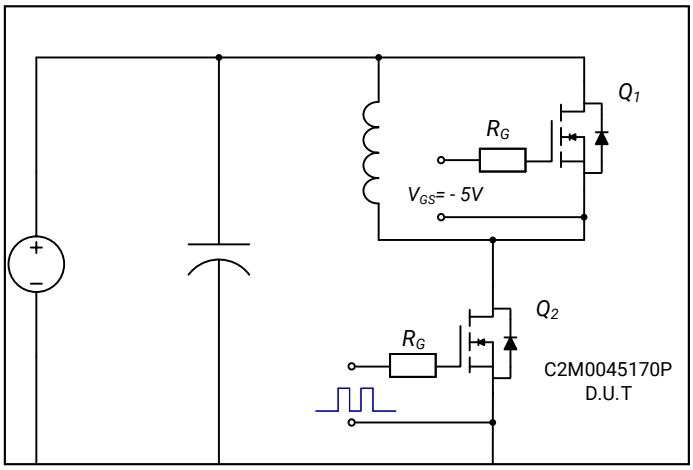


Figure 29a. Clamped Inductive Switching Test Circuit using
MOSFET intristic body diode

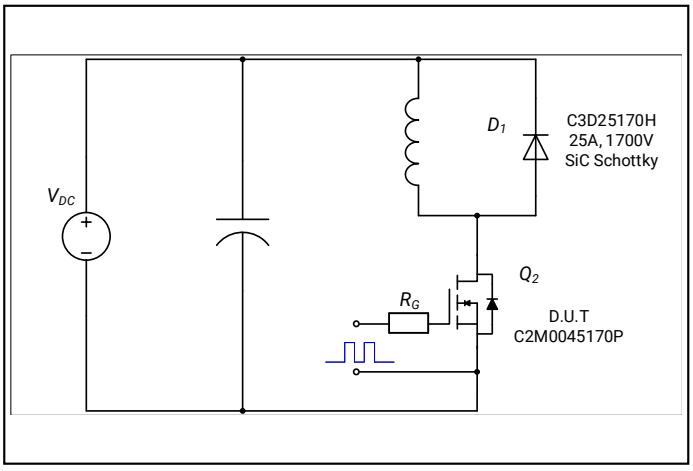
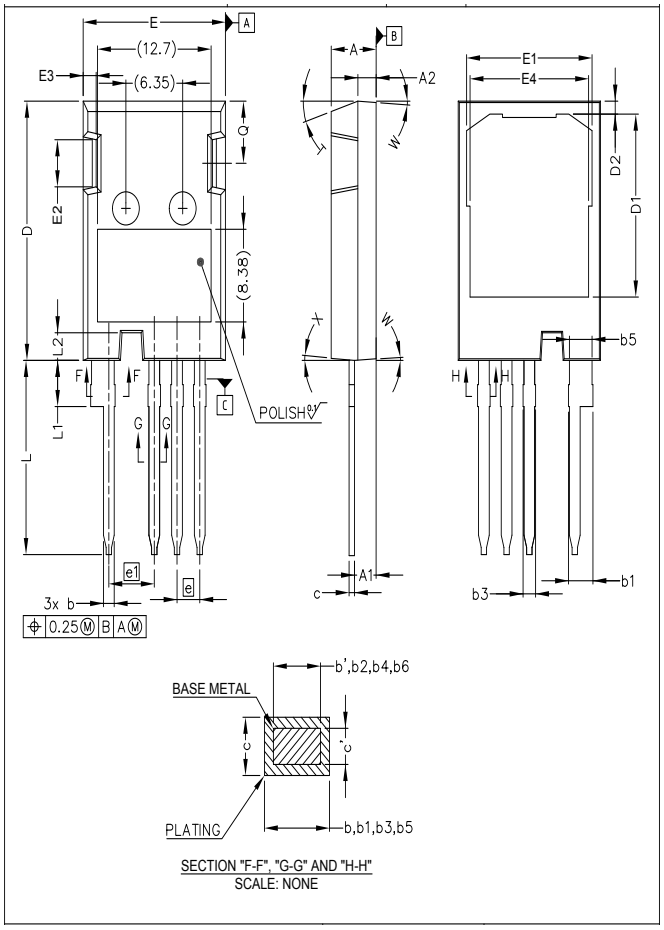


Figure 29b. Clamped Inductive Switching Test Circuit using
SiC Schottky diode

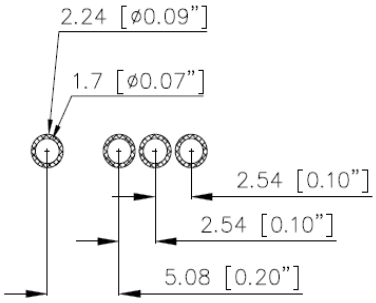
Package Dimensions

Package TO-247-4L Plus



SYM	MILLIMETERS	
	MIN	MAX
A	4.83	5.21
A1	2.29	2.54
A2	1.91	2.16
b'	1.07	1.28
b	1.07	1.33
b1	2.39	2.94
b2	2.39	2.84
b3	1.07	1.60
b4	1.07	1.50
b5	2.39	2.69
b6	2.39	2.64
c'	0.55	0.65
c	0.55	0.68
D	23.30	23.60
D1	16.25	17.65
D2	0.95	1.25
E	15.75	16.13
E1	13.10	14.15
E2	3.68	5.10
E3	1.00	1.90
E4	12.38	13.43
e	2.54 BSC	
e1	5.08 BSC	
N	4	
L	17.31	17.82
L1	3.97	4.37
L2	2.35	2.65
Q	5.49	6.00
T	17.5° REF.	
W	3.5 ° REF.	
X	4° REF.	

Recommended Solder Pad Layout



Notes

- **RoHS Compliance**
  The levels of RoHS restricted materials in this product are below the maximum concentration values (also referred to as the threshold limits) permitted for such substances, or are used in an exempted application, in accordance with EU Directive 2011/65/EC (RoHS2), as implemented January 2, 2013. RoHS Declarations for this product can be obtained from your Cree representative or from the Product Documentation sections of www.cree.com.

- **REACh Compliance**
  REACh substances of high concern (SVHCs) information is available for this product. Since the European Chemical Agency (ECHA) has published notice of their intent to frequently revise the SVHC listing for the foreseeable future,please contact a Cree representative to insure you get the most up-to-date REACh SVHC Declaration. REACh banned substance information (REACh Article 67) is also available upon request.

- This product has not been designed or tested for use in, and is not intended for use in, applications implanted into the human body nor in applications in which failure of the product could lead to death, personal injury or property damage, including but not limited to equipment used in the operation of nuclear facilities, life-support machines, cardiac defibrillators or similar emergency medical equipment, aircraft navigation or communication or control systems, air traffic control systems.

Related Links

- **C2M PSPICE Models: http://wolfspeed.com/power/tools-and-support**
- **SiC MOSFET Isolated Gate Driver reference design: http://wolfspeed.com/power/tools-and-support**
- **SiC MOSFET Evaluation Board: http://wolfspeed.com/power/tools-and-support**

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Fax: +1.919.313.5451
www.cree.com/power

A.2 5SNA 3600E170300

In the following pages, the datasheet for the ABB IGBT, *5SNA 3600E170300*, has been attached. This datasheet was retrieved from [32].

Data Sheet, Doc. No. 5SYA 1414-06 02-2014

5SNA 3600E170300
HiPak IGBT Module

V_{CE} = 1700 V
I_C = 3600 A

Ultra low-loss, rugged SPT+ chip-set
Smooth switching SPT+ chip-set for good EMC
AlSiC base-plate for high power cycling capability
AlN substrate for low thermal resistance
Improved high reliability package

Maximum rated values [1)]

Parameter	Symbol	Conditions	min	max	Unit
Collector-emitter voltage	V_{CES}	V_{GE} = 0 V, $T_{vj} \geq 25$ °C		1700	V
DC collector current	I_C	T_C = 70 °C, T_{vj} = 150 °C		3600	A
Peak collector current	I_{CM}	t_p = 1 ms		7200	A
Gate-emitter voltage	V_{GES}		-20	20	V
Total power dissipation	P_{tot}	T_C = 25 °C, T_{vj} = 150 °C		17800	W
DC forward current	I_F			3600	A
Peak forward current	I_{FRM}	t_p = 1 ms		7200	A
Surge current	I_{FSM}	V_R = 0 V, T_{vj} = 150 °C, t_p = 10 ms, half-sinewave		18000	A
IGBT short circuit SOA	t_{psc}	V_{CC} = 1200 V, $V_{CEM\ CHIP} \leq$ 1700 V $V_{GE} \leq$ 15 V, $T_{vj} \leq$ 150 °C		10	µs
Isolation voltage	V_{isol}	1 min, f = 50 Hz		4000	V
Junction temperature	T_{vj}			175	°C
Junction operating temperature	$T_{vj(op)}$		-50	150	°C
Case temperature	T_C		-50	150	°C
Storage temperature	T_{stg}		-50	125	°C
Mounting torques [2)]	M_s	Base-heatsink, M6 screws	4	6	Nm
	M_{t1}	Main terminals, M8 screws	8	10	
	M_{t2}	Auxiliary terminals, M4 screws	2	3	

[1)] Maximum rated values indicate limits beyond which damage to the device may occur per IEC 60747
[2)] For detailed mounting instructions refer to ABB Document No. 5SYA 2039

IGBT characteristic values [3]

Parameter	Symbol	Conditions		min	typ	max	Unit
Collector (-emitter) breakdown voltage	$V_{(BR)CES}$	V_{GE} = 0 V, I_C = 10 mA, T_{vj} = 25 °C		1700			V
Collector-emitter [4] saturation voltage	$V_{CE\ sat}$	I_C = 3600 A, V_{GE} = 15 V	T_{vj} = 25 °C	2.2	2.5	2.8	V
			T_{vj} = 125 °C	2.7	3.0	3.3	V
			T_{vj} = 150 °C		3.1		V
Collector cut-off current	I_{CES}	V_{CE} = 1700 V, V_{GE} = 0 V	T_{vj} = 25 °C		0.04	1	mA
			T_{vj} = 125 °C		30	60	mA
			T_{vj} = 150 °C		170		mA
Gate leakage current	I_{GES}	V_{CE} = 0 V, V_{GE} = ± 20 V, T_{vj} = 125 °C		-500		500	nA
Gate-emitter threshold voltage	$V_{GE(TO)}$	I_C = 240 mA, V_{CE} = V_{GE}, T_{vj} = 25 °C		5.3		7.3	V
Gate charge	Q_{ge}	I_C = 3600 A, V_{CE} = 900 V, V_{GE} = -15 V ..15 V			21		µC
Input capacitance	C_{ies}	V_{CE} = 25 V, V_{GE} = 0 V, f = 1 MHz, T_{vj} = 25 °C			239		nF
Output capacitance	C_{oes}				20.9		nF
Reverse transfer capacitance	C_{res}				9.24		nF
Turn-on delay time	$t_{d(on)}$	V_{CC} = 900 V, I_C = 3600 A, R_G = 0.6 Ω, C_{GE} = 0 nF, V_{GE} = ±15 V, L_σ = 50 nH, inductive load	T_{vj} = 25 °C		480		ns
			T_{vj} = 125 °C		510		ns
			T_{vj} = 150 °C		520		ns
Rise time	t_r		T_{vj} = 25 °C		290		ns
			T_{vj} = 125 °C		310		ns
			T_{vj} = 150 °C		315		ns
Turn-off delay time	$t_{d(off)}$	V_{CC} = 900 V, I_C = 3600 A, R_G = 0.6 Ω, C_{GE} = 0 nF, V_{GE} = ±15 V, L_σ = 50 nH, inductive load	T_{vj} = 25 °C		1160		ns
			T_{vj} = 125 °C		1260		ns
			T_{vj} = 150 °C		1290		ns
Fall time	t_f		T_{vj} = 25 °C		270		ns
			T_{vj} = 125 °C		300		ns
			T_{vj} = 150 °C		310		ns
Turn-on switching energy	E_{on}	V_{CC} = 900 V, I_C = 3600 A, R_G = 0.6 Ω, C_{GE} = 0 nF, V_{GE} = ±15 V, L_σ = 50 nH, inductive load	T_{vj} = 25 °C		800		mJ
			T_{vj} = 125 °C		1100		mJ
			T_{vj} = 150 °C		1200		mJ
Turn-off switching energy	E_{off}	V_{CC} = 900 V, I_C = 3600 A, R_G = 0.6 Ω, C_{GE} = 0 nF, V_{GE} = ±15 V, L_σ = 50 nH, inductive load	Tvj = 25 °C		1330		mJ
			Tvj = 125 °C		1600		mJ
			T_{vj} = 150 °C		1690		mJ
Short circuit current	I_{SC}	t_{psc} ≤ 10 µs, V_{GE} = 15 V, V_{CC} = 1200 V, $V_{CEM\ CHIP}$ ≤ 1700 V	Tvj = 150 °C		10000		A

[3] Characteristic values according to IEC 60747 - 9
[4] Collector-emitter saturation voltage is given at chip level

Diode characteristic values [5]

Parameter	Symbol	Conditions		min	typ	max	Unit
Forward voltage [6]	V_F	I_F = 3600 A	T_{vj} = 25 °C		1.85	2.2	V
			T_{vj} = 125 °C		1.95	2.3	V
			T_{vj} = 150 °C		1.9		V
Reverse recovery current	I_{rr}	V_{CC} = 900 V, I_F = 3600 A, V_{GE} = ±15 V, R_G = 0.6 Ω, C_{GE} = 0 nF, di/dt = 11.5 kA/µs L_σ = 50 nH, inductive load	T_{vj} = 25 °C		2030		A
			T_{vj} = 125 °C		2340		A
			T_{vj} = 150 °C		2500		A
Recovered charge	Q_{rr}		T_{vj} = 25 °C		1000		µC
			T_{vj} = 125 °C		1560		µC
			T_{vj} = 150 °C		1820		µC
Reverse recovery time	t_{rr}		T_{vj} = 25 °C		900		ns
			T_{vj} = 125 °C		1230		ns
			T_{vj} = 150 °C		1320		ns
Reverse recovery energy	E_{rec}		T_{vj} = 25 °C		710		mJ
			T_{vj} = 125 °C		1080		mJ
			T_{vj} = 150 °C		1260		mJ

[5] Characteristic values according to IEC 60747 - 2
[6] Forward voltage is given at chip level

Package properties [7]

Parameter	Symbol	Conditions	min	typ	max	Unit
IGBT thermal resistance junction to case	$R_{th(j-c)IGBT}$				0.007	K/W
Diode thermal resistance junction to case	$R_{th(j-c)DIODE}$				0.012	K/W
IGBT thermal resistance [2] case to heatsink	$R_{th(c-s)IGBT}$	IGBT per switch, λ grease = 1W/m x K		0.009		K/W
Diode thermal resistance [2] case to heatsink	$R_{th(c-s)DIODE}$	Diode per switch, λ grease = 1W/m x K		0.018		K/W
Comparative tracking index	CTI		600			
Module stray inductance	$L_{\sigma CE}$			8		nH
Resistance, terminal-chip	$R_{CC'+EE'}$	T_C = 25 °C		0.055		mΩ
		T_C = 125 °C		0.075		
		T_C = 150 °C		0.080		

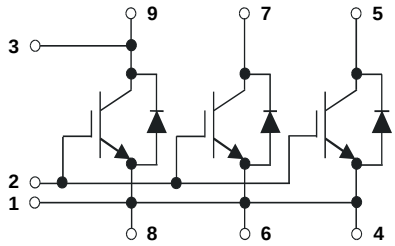
[2] For detailed mounting instructions refer to ABB Document No. 5SYA 2039

Mechanical properties [7]

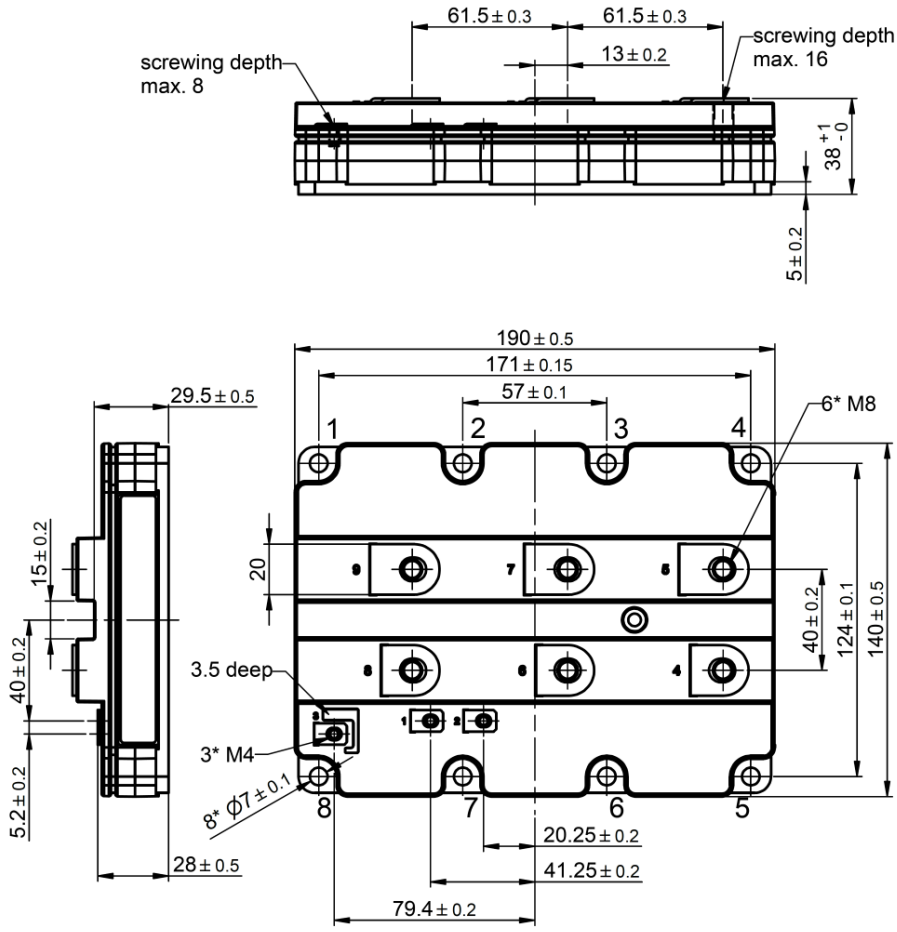
Parameter	Symbol	Conditions		min	typ	max	Unit
Dimensions	L x W x H	Typical		190 x 140 x 38			mm
Clearance distance in air	d_a	according to IEC 60664-1 and EN 50124-1	Term. to base:	23			mm
			Term. to term:	19			
Surface creepage distance	d_s	according to IEC 60664-1 and EN 50124-1	Term. to base:	28.2			mm
			Term. to term:	28.2			
Mass	m				1210		g

[7] Package and mechanical properties according to IEC 60747 - 15

Electrical configuration



Outline drawing [2)]



Note: all dimensions are shown in millimeters
[2)] For detailed mounting instructions refer to ABB Document No. 5SYA 2039

This is an electrostatic sensitive device, please observe the international standard IEC 60747-1, chap. IX.
This product has been designed and qualified for Industrial Level.

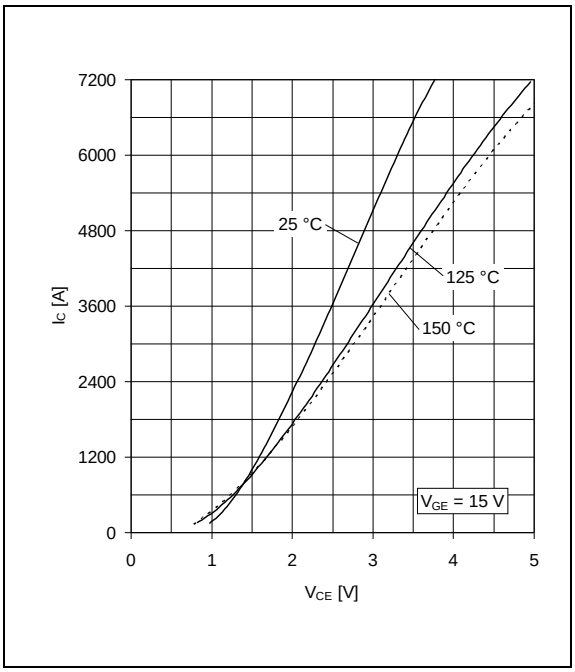


Fig. 1 Typical on-state characteristics, chip level

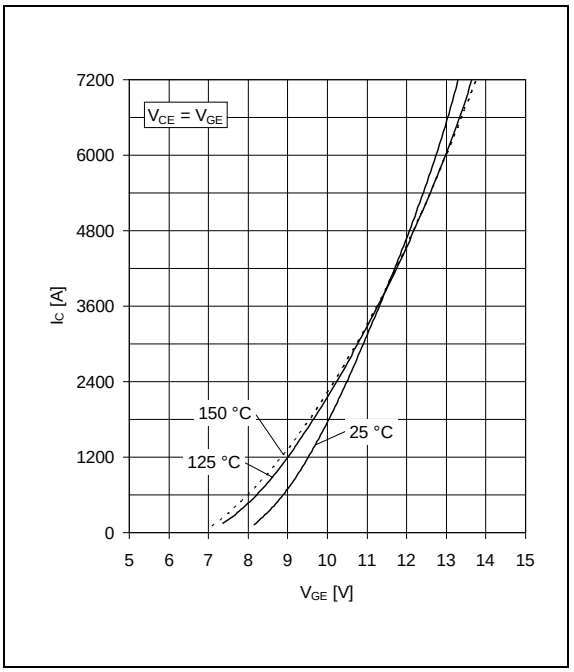


Fig. 2 Typical transfer characteristics, chip level

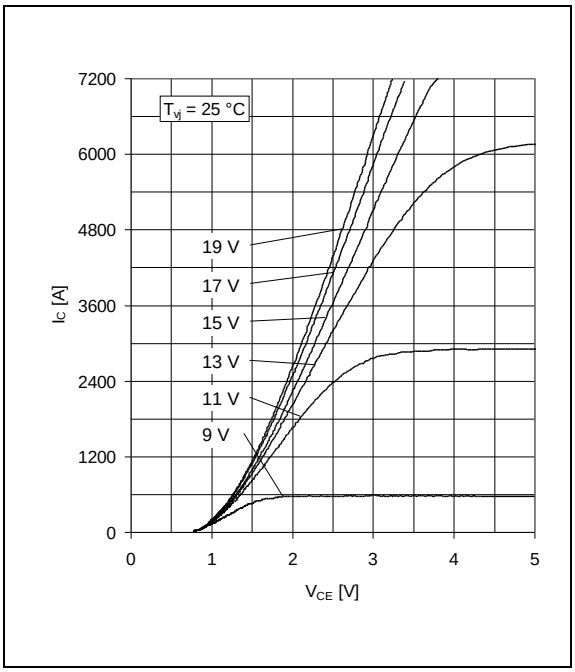


Fig. 3 Typical output characteristics, chip level

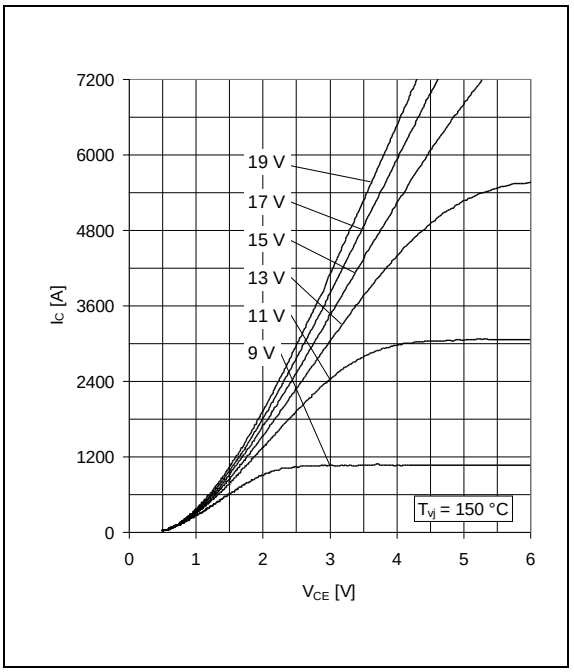


Fig. 4 Typical output characteristics, chip level

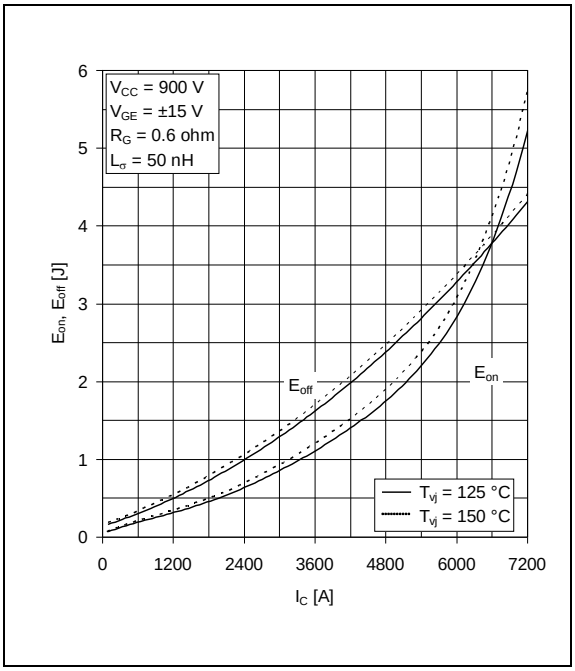


Fig. 5 Typical switching energies per pulse vs. collector current

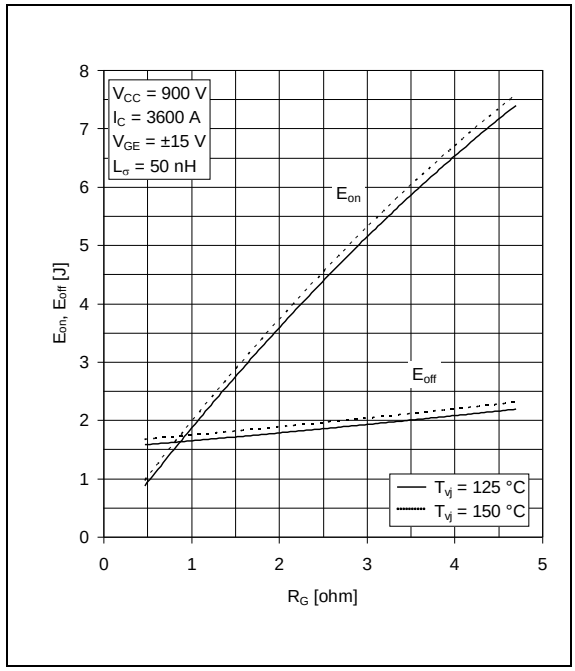


Fig. 6 Typical switching energies per pulse vs. gate resistor

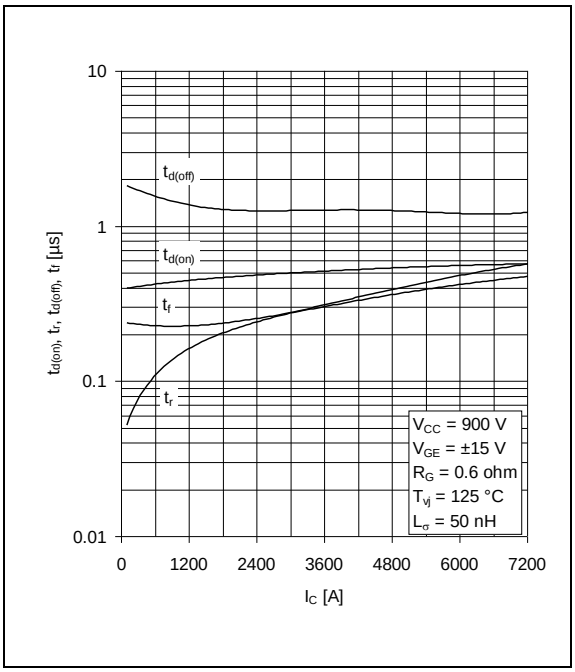


Fig. 7 Typical switching times vs. collector current

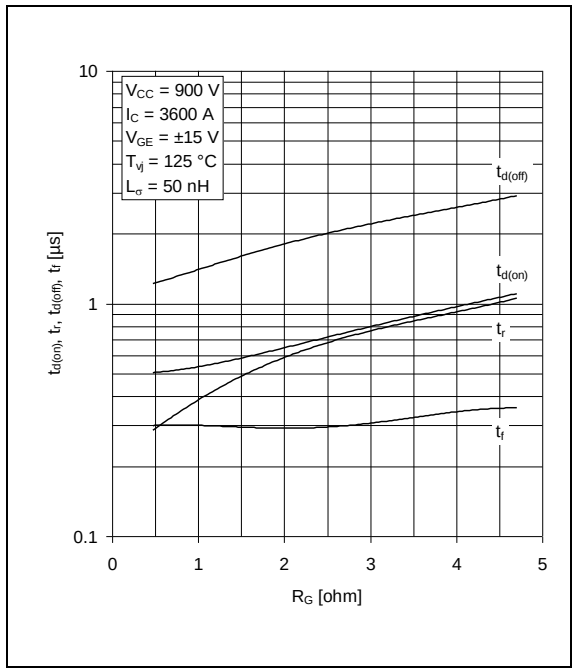


Fig. 8 Typical switching times vs. gate resistor

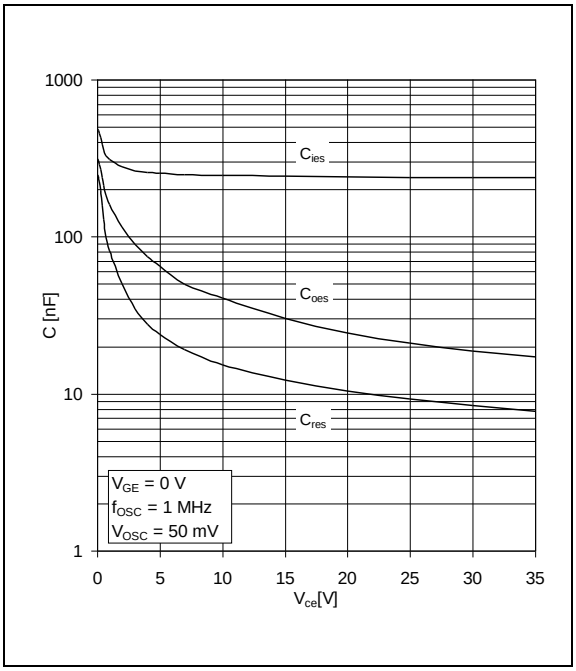


Fig. 9 Typical capacitances vs. collector-emitter voltage

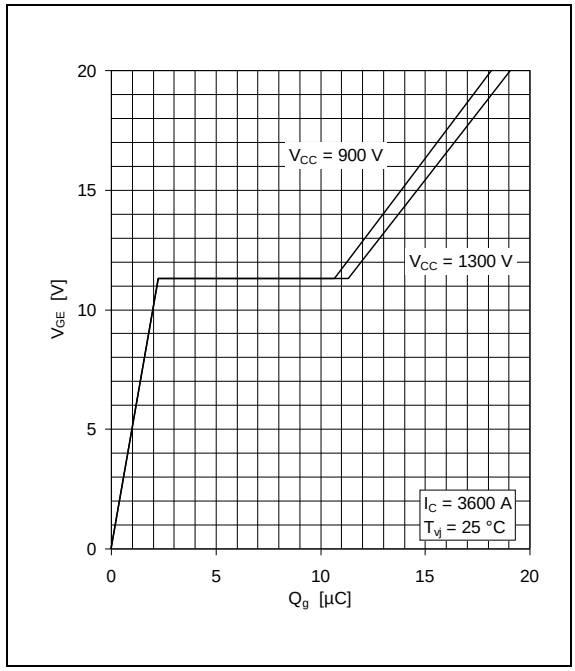


Fig. 10 Typical gate charge characteristics

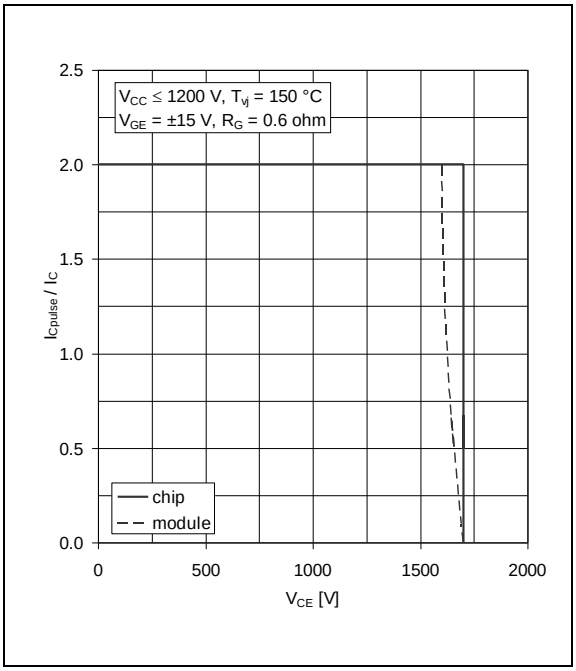


Fig. 11 Turn-off safe operating area (RBSOA)

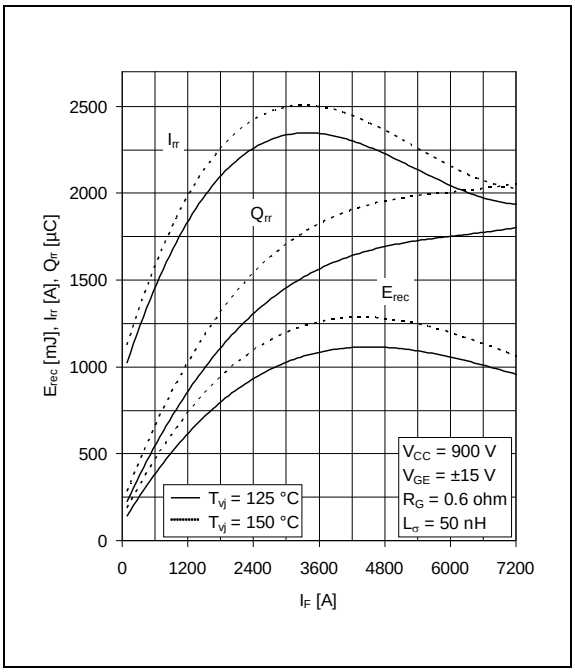


Fig. 12 Typical reverse recovery characteristics vs. forward current

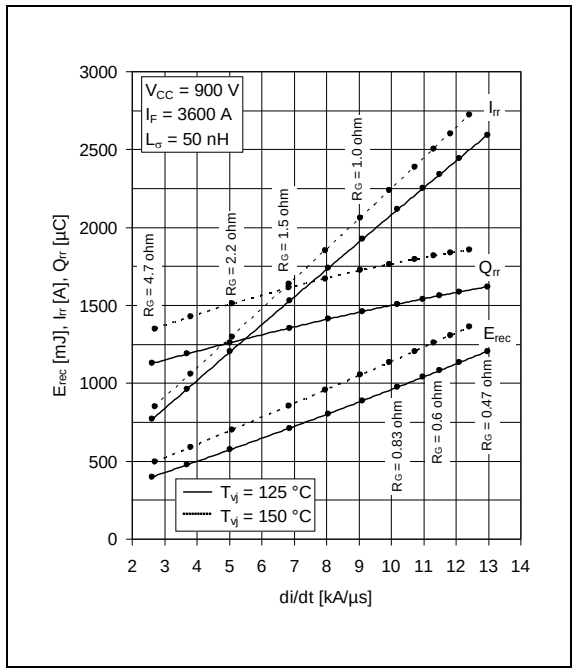


Fig. 13 Typical reverse recovery characteristics vs. di/dt

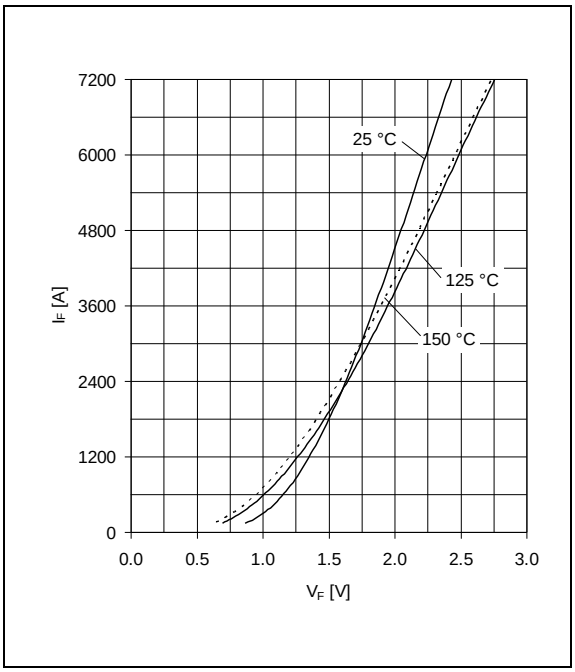


Fig. 14 Typicial diode forward characteristics chip level

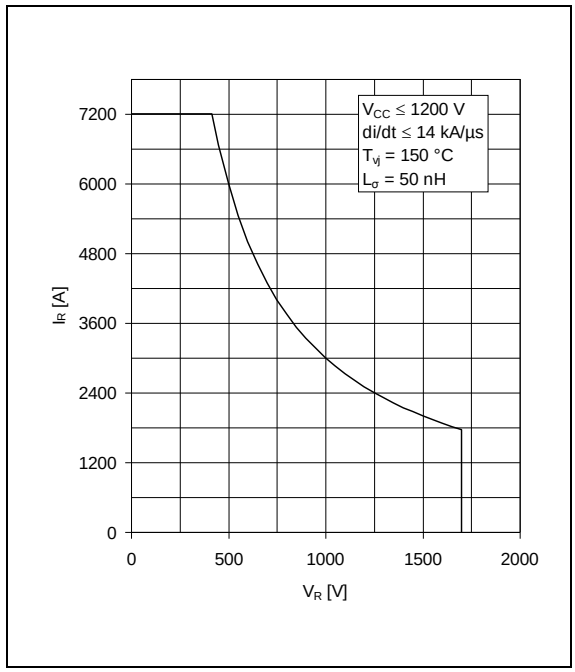
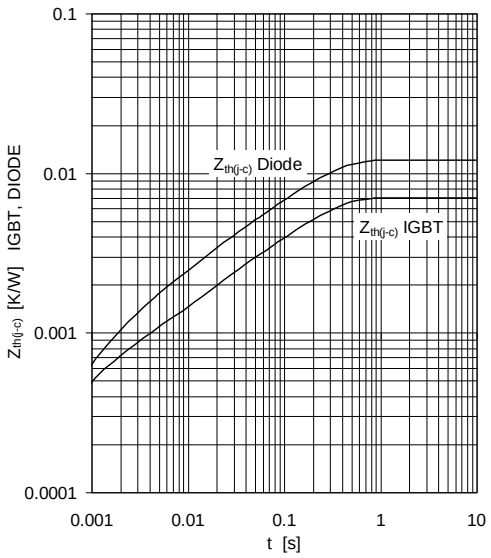


Fig. 15 Safe operating area diode (SOA)



Analytical function for transient thermal impedance:

$$Z_{th\,(j\text{-}c)}(t) = \sum_{i=1}^{n} R_i\,(1 - e^{-t/\tau_i})$$

	i	1	2	3	4	5
IGBT	Ri(K/kW)	5.059	1.201	0.495	0.246	
	τi(ms)	202.9	20.3	2.01	0.52	
DIODE	Ri(K/kW)	8.432	1.928	0.866	0.839	
	τi(ms)	210	29.6	7.01	1.49	

Fig. 16 Thermal impedance vs. time

5SNA 3600E170300 | Doc. No. 5SYA 1414-06 02-2014

Related documents:

5SYA 2042 Failure rates of HiPak modules due to cosmic rays
5SYA 2043 Load – cycle capability of HiPaks
5SYA 2045 Thermal runaway during blocking
5SYA 2053 Applying IGBT
5SYA 2058 Surge currents for IGBT diodes
5SYA 2093 Thermal design of IGBT modules
5SYA 2098 Paralleling of IGBT modules
5SZK 9111 Specification of environmental class for HiPak Storage
5SZK 9112 Specification of environmental class for HiPak Transportation
5SZK 9113 Specification of environmental class for HiPak Operation (Industry)
5SZK 9120 Specification of environmental class for HiPak

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Appendix B

Simulation models

B.1 Simscape Models

B.1.1 Transistor models

IGBT model parameters

Parameter	Value
Zero gate voltage collector current, Ices:	0.04 mA
Voltage at which Ices is defined:	1700 V
Gate-emitter threshold voltage, Vge(th):	6.7 V
Collector-emitter saturation voltage, Vce(sat):	2.5 V
Collector current at which Vce(sat) is defined:	3600 A
Gate-emitter voltage at which Vce(sat) is defined:	15 V
Measurement temperature:	25 °C

Table B.1: Main parameters of IGBT model

Parameter	Value
Input capacitance, Cies:	[490, 300, 280, 270, 260, 250, 245, 240, 240, 240] nF
Reverse transfer capacitance, Cres:	[240, 80, 50, 24, 16, 13, 11, 9.25, 8.5, 7.9] nF
Output capacitance, Coes:	[310, 160, 120, 65, 40, 30, 25, 22, 19, 18] nF
Corresponding collector-emitter voltages:	[0, 1, 2, 5, 10, 15, 20, 25, 30, 35] V
Total forward transit time:	4.25 ns

Table B.2: Junction capacitance parameters of IGBT model

Parameter	Value
Emission coefficient, N:	1.8
Forward Early voltage, VAF:	200 V
Collector resistance, RC:	0.0003 Ω
Emitter resistance, RE:	0.0000001 Ω
Internal gate resistance, RG:	0.001 Ω
Forward current transfer ratio, BF:	50

Table B.3: Advanced parameters of IGBT model

Parameter	Value
Zero gate voltage collector current, Ices, at second measurement temperature	30 mA
Collector-emitter saturation voltage, Vce(sat), at second measurement temperature:	3 V
Second measurement temperature:	125 °C
Saturation current temperature exponent, XTI:	3
Mobility temperature exponent, BEX:	-5
Internal gate resistance temperature coefficient:	0 1/K

Table B.4: Temperature dependence parameters of IGBT model

SiC MOSFET model parameters

Parameter	Value
Drain-source on resistance, R_DS(on):	0.057 Ω
Drain current, Ids, for R_DS(on):	50 A
Gate-source voltage, Vgs, for R_DS(on):	20 V
Gate-source threshold voltage, Vth:	2.3 V
Channel modulation, L:	0 1/V
Measurement temperature:	25 °C

Table B.5: Main parameters of SiC MOSFET model

Parameter	Value
Input capacitance, Ciss:	[4200, 3900, 3900,..., 3900] pF
Reverse transfer capacitance, Crss:	[1000, 350, 200, 60, 28, 19, 16, 14, 9.5, 8, 7, 6.9] pF
Output capacitance, Coss:	[3750, 1500, 1300, 950, 650, 475, 400, 325, 250, 200, 190, 180] pF
Corresponding drain-source voltages:	[0, 5, 10, 20, 50, 100, 150, 200, 400, 600, 800, 1000] V
Gate-source voltage, Vgs, for tabulated capacitances:	0 V

Table B.6: Junction capacitance parameters of SiC MOSFET model

Parameter	Value
Drain-source on resistance, R_DS(on), at second measurement temperature:	0.09 Ω
Second measurement temperature:	150 °C
Mobility temperature exponent, BEX:	-1.5
Body diode reverse saturation current temperature exponent:	3

Table B.7: Temperature dependence parameters of SiC MOSFET model

IGBT IV-characteristic verification circuit

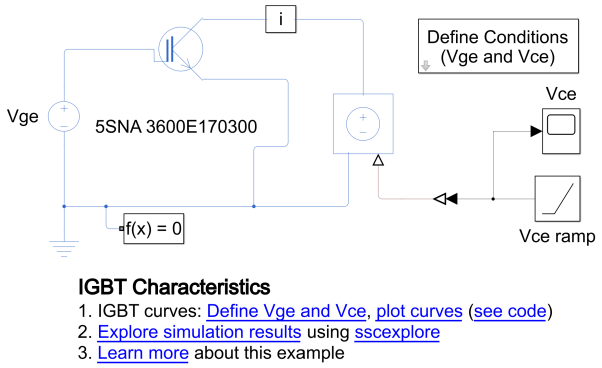

Figure B.1: Simulation circuit used to verify the IV-curves of the IGBT

SiC MOSFET IV-characteristic verification circuit

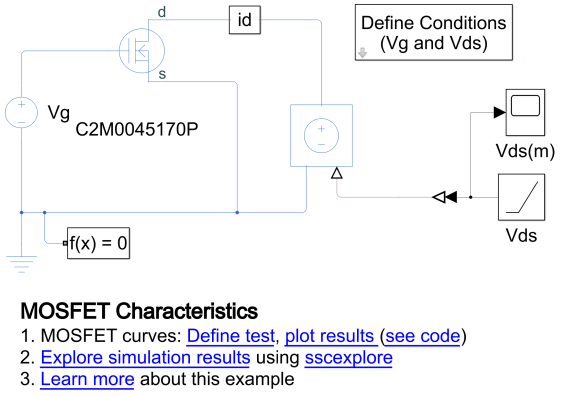

Figure B.2: Simulation circuit used to verify the IV-curves of the SiC MOSFET

Double-pulse test circuit

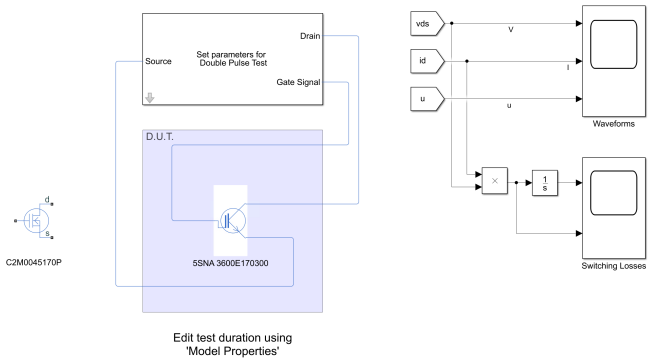

Figure B.3: Double-pulse test model in Simscape

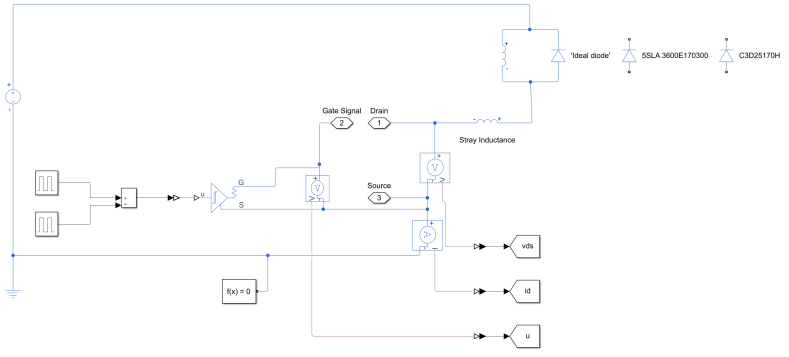

Figure B.4: Double-pulse test circuit subsystem

B.1.2 HyS Simscape models

HyS double-pulse test circuit

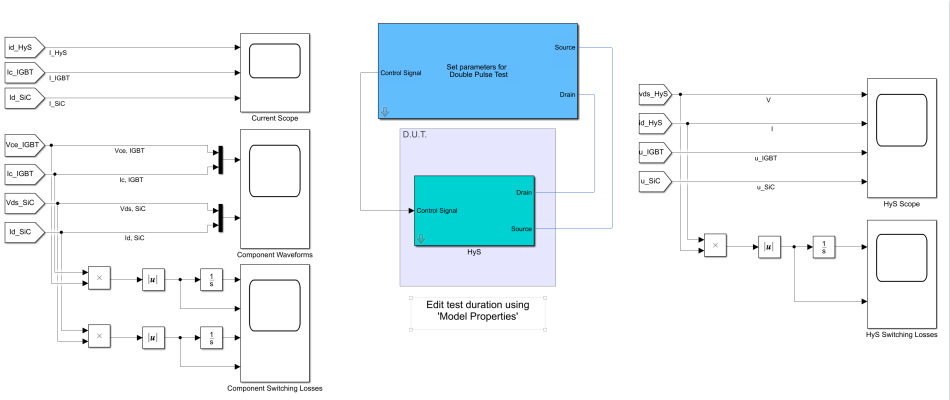

Figure B.5: HyS double-pulse test main system

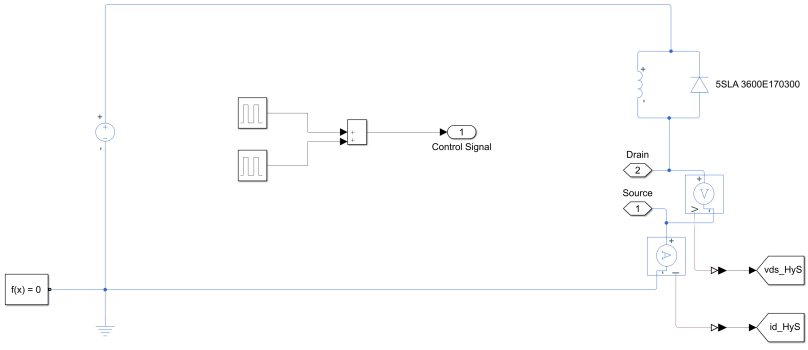

Figure B.6: HyS double-pulse test circuit subsystem

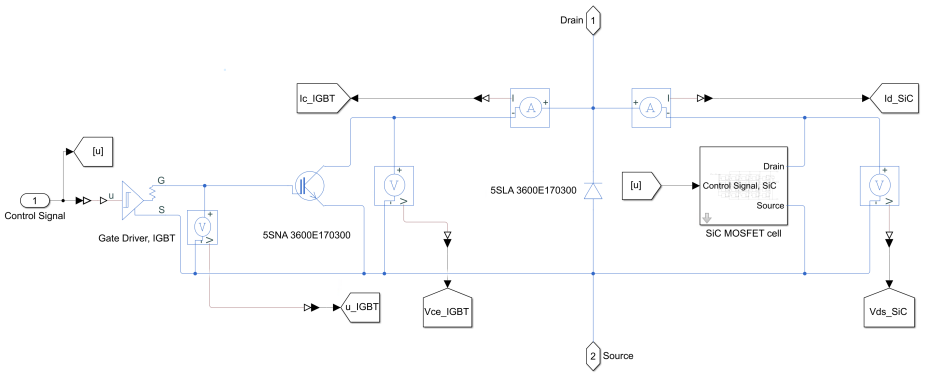

Figure B.7: HyS double-pulse test HyS subsystem

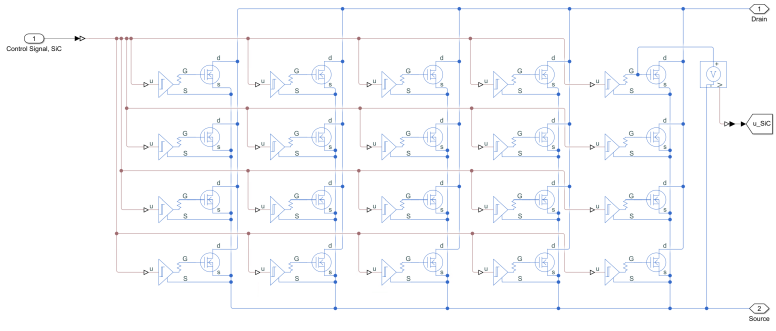

Figure B.8: HyS double-pulse test MOSFET cell system

HyS DPT circuit with inductance

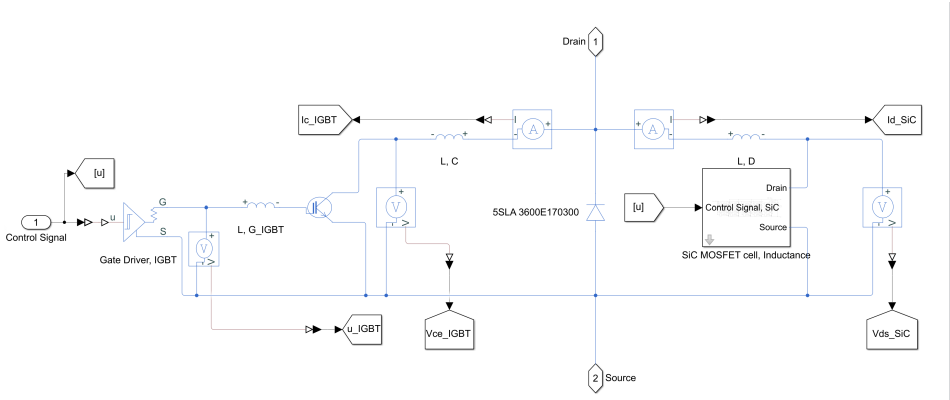

Figure B.9: HyS DPT with inductance HyS subsystem

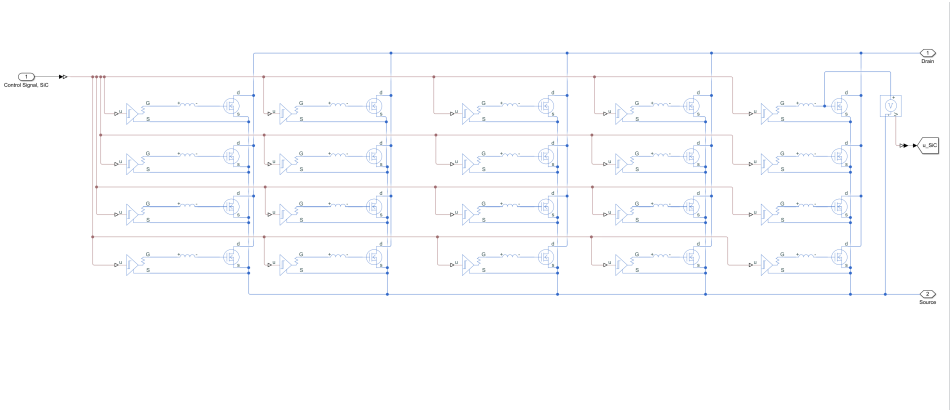

Figure B.10: HyS DPT with inductance MOSFET cell system

B.2 PLECS Models

PLECS half-bridge circuit

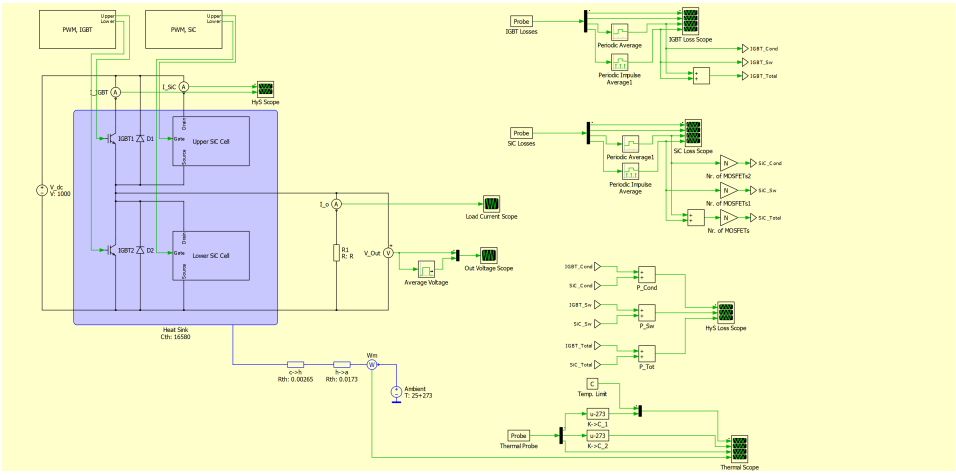

Figure B.11: Main system of PLECS half-bridge model

PLECS SiC MOSFET cell subsystem

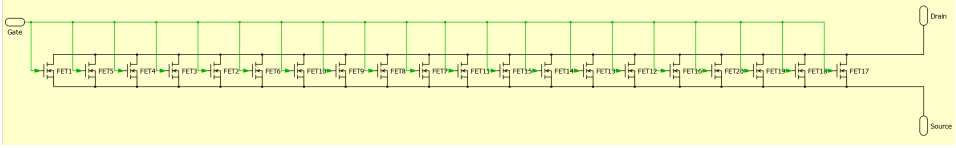

Figure B.12: MOSFET subsystem of PLECS half-bridge model

PLECS IGBT PWM subsystem

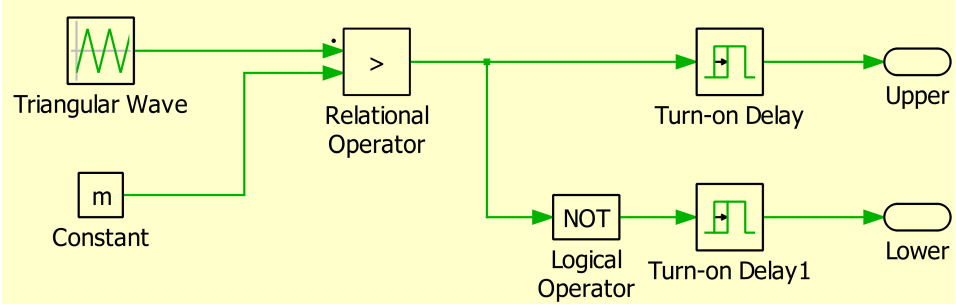

Figure B.13: IGBT PWM subsystem of PLECS half-bridge model

PLECS SiC MOSFET PWM subsystem

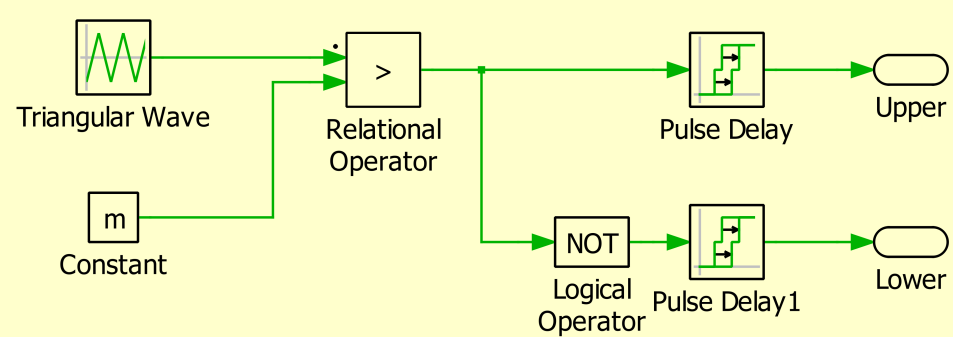

Figure B.14: SiC MOSFET PWM subsystem of PLECS half-bridge model

Appendix C

Scripts

C.1 MATLAB

C.1.1 Transistor Models

IGBT IV-characteristic verification

```
% Code to plot simulation results from ee_igbt
%% Plot Description:
%
% The plot below shows the collector current vs collector-emitter voltage
% characteristics for a range of gate-emitter voltages.

% Copyright 2008-2018 The MathWorks, Inc.

%% Model initialization(This is an alteration to the original script)

N = 1.8;
VAF = 200;
RC = 0.0003;
RE = 0.0000001;
RG = 0.0875;
BF = 50;

%% Plots
ModelName = 'IGBT_model_verification';
ParameterBlk = [ModelName '/Parameters'];
```

```
Vge_vec = str2num(get_param(ParameterBlk,'Vge_vec'));
Vce_min = str2double(get_param(ParameterBlk,'Vce_min'));
Vce_max = str2double(get_param(ParameterBlk,'Vce_max'));
Ic_max  = str2double(get_param(ParameterBlk,'Ic_max'));
Ic_approx = [0, 150, 300,  600, 1200, 1800, 2400, 3000,
    3600, 4200,...
     4800, 5400, 6000, 6600, 7200]; %Alteration from
         original script
%Voltage vectors, all alterations from original script
Vce_approx25 = [0, 1, 1.15, 1.3, 1.6, 1.8, 2.1, 2.3, 2.5,
    2.7, 2.9,...
     3.1, 3.3, 3.5, 3.7];
Vce_approx125 = [0, 0.75, 1, 1.3, 1.7, 2.05, 2.4, 2.7, 3,
    3.3, 3.6,...
     3.95, 4.3, 4.65, 5];
Vce_approx150 = [0, 0.75, 1, 1.3, 1.7, 2.1, 2.45, 2.75,
    3.1, 3.45, 3.75,...
     4.1, 4.45, 4.8, 5.15];

if Vce_max <= Vce_min
     pm_error('physmod:ee:library:InconsistentMaskParameters
         ',...
          'Maximum collector-emitter voltage',...
          'Minimum collector-emitter voltage')
end
t_sim = 1;
clear legend_info Ic_mat Vce_vec
for i=1:length(Vge_vec)
     Vge = Vge_vec(i);
     legend_info{i} = ['Vge = ',num2str(Vge)];
     sim(ModelName,t_sim)
     Ic_mat(:,i) = Ic.signals.values;
     Vce_vec = Vce.signals.values;
end

if ~exist('h1_ee_igbt', 'var') || ...
          ~isgraphics(h1_ee_igbt, 'figure')
     h1_ee_igbt = figure('Name', 'ee_igbt');
end
figure(h1_ee_igbt)
clf(h1_ee_igbt)

hold on %Alteration from original script
plot(Vce_vec,Ic_mat','LineWidth',1);
```

```
plot(Vce_approx25, Ic_approx, 'x'); %Alteration from
    original script
plot(Vce_approx125, Ic_approx, 'x'); %Alteration from
    original script
plot(Vce_approx150, Ic_approx, 'x'); %Alteration from
    original script
axis([Vce_min Vce_max 0 Ic_max])
xlabel('Vce: Collector-Emitter Voltage (V)')
ylabel('Ic: Collector Current (A)')
title('IGBT Curves: Model I-V char. vs. approximate
    datasheet I-V char.');
grid on
legend(legend_info);

% Reset default values
Vge = 10;
Vce_min = 0;
Vce_max = 5;
```

SiC MOSFET IV-characteristic verification

```
% Code to plot simulation results from ee_mosfet
%% Plot Description:
%
% The plot below shows drain current vs. drain-source
    voltage for a range
% of gate voltages.

% Copyright 2008-2018 The MathWorks, Inc.

ModelName = get_param(gcb,'Parent');
ParameterBlk = [ModelName '/Parameters'];
Vg_vec = str2num(get_param(ParameterBlk,'Vg_vec'));
Vds_min = str2num(get_param(ParameterBlk,'Vds_min'));
Vds_max = str2num(get_param(ParameterBlk,'Vds_max'));
Vds_approx = [0, 2.5, 5, 7.5, 10, 12.5, 15]; %Alteration
    from original
%script
% Current vectors, all alterations from original script
Id_approx25 = [0 56 87.5 112.5 137.5, 162.5, 187.5];
Id_approx150 = [0, 28, 53, 75, 90, 106, 119];
if Vds_max <= Vds_min
    pm_error('physmod:ee:library:InconsistentMaskParameters
        ',...
        'Maximum drain-source voltage','Minimum drain-
            source voltage')
```

```
end
t_sim = 1;
clear legend_info Id_mat Vds_vec
for i=1:length(Vg_vec)
    Vg = Vg_vec(i);
    legend_info{i} = ['Vg = ',num2str(Vg)]; %#ok<SAGROW>
    sim(ModelName,t_sim)
    Id_mat(:,i) = Id.signals.values; %#ok<SAGROW>
    Vds_vec = Vds.signals.values;
end

% Reuse figure if it exists, else create new figure
if ~exist('h1_ee_mosfet', 'var') || ...
        ~isgraphics(h1_ee_mosfet, 'figure')
    h1_ee_mosfet = figure('Name', 'ee_mosfet');
end
figure(h1_ee_mosfet)
clf(h1_ee_mosfet)

hold on %Alteration from original script
plot(Vds_vec,Id_mat','LineWidth',1)
plot(Vds_approx, Id_approx25, 'x') %Alteration from
    original script
plot(Vds_approx, Id_approx150, 'x') %Alteration from
    original script
axis([Vds_min Vds_max 0 200])
xlabel('Drain-Source Voltage (V)')
ylabel('Drain Current (A)')
legend(legend_info);
title('MOSFET Curves: Model I-V char. vs. approximate
    datasheet I-V char.')
grid on
% Reset default values
Vg = 5;
Vds_min = 0;
Vds_max = 4;
```

C.2 PLECS

C.2.1 Initialization script

```
%% Inputs
fsw=11250; %Switching frequency
I_Load=2000; %Load current
m=0; %Modulation index, determines duty cycle
N=20; %Nr. of MOSFETs
```

```
6  L=10; %Total stray inductance
7  %% Calculations
8  R=1000/I_Load; %Load resistance
9  T_d=0.2377*L-0.0746; %Commutation time as a function of
       stray inductance
10 T_L=(T_d/(1540))*(I_Load-(460*20/N)); %Adjusted commutation
       time
11 if T_L<0
12         T_L=0;
13 end
```

Appendix D

Raw Data

D.1 Transistor Models

IGBT switching energy

IGBT Switching Energy [mJ]	Turn-OFF (25 °C)	Turn-ON (25 °C)	Turn-OFF (125 °C)	Turn-ON (125 °C)	Turn-OFF (150 °C)	Turn-ON (150 °C)
Measurement	1650	300	1650	200	1690	180
Datasheet	1330	800	1600	1100	1690	1200

Table D.1: IGBT model switching energy compared to datasheet

IGBT fall times

IGBT Fall Times [ns]	25 °C	125 °C	150 °C
Measurement	409	411	416
Datasheet	270	300	310

Table D.2: IGBT model current fall times compared to datasheet

SiC MOSFET switching energy

SiC MOSFET Switching Energy [mJ]	Turn-OFF (25 °C)	Turn-ON (25 °C)	Turn-OFF (150 °C)	Turn-ON (150 °C)
Measurement	0.21	0.67	0.23	0.9
Datasheet	-	-	0.31	0.67

Table D.3: SiC MOSFET model switching energy compared to datasheet

D.2 HyS Simscape Model

D.2.1 Without stray inductance

MOSFET-Current relation

Nr. of MOSFETs [-]	Current [A]
20	460
15	355
10	250
5	125

Table D.4: Relationship between nr. of MOSFETs in parallel, and current conducted through SiC MOSFET cell

Turn-OFF delay optimization

t_1 [µs]	IGBT Loss [mJ]	SiC Loss [mJ]	Total Loss [mJ]
0	602	1.7	603.7
0.4	237	6.5	243.5
0.8	47	16	63
1.2	21	24	45
1.6	16	33	49
2	16	44	60
2.4	16	53	69

Table D.5: Turn-OFF energy of the HyS as a function of t_1

D.2.2 With stray inductance

Inductance delay

Inductance [nH]	ΔI [A]	T$_d$ [µs]	T'$_d$/2 [µs]
10	1040	3.11	2.30
30	970	8.76	6.95
50	910	14.13	11.96
100	775	23.81	23.66

Table D.6: Approximated commutation time for use in PLECS as a function of total stray inductance

D.3 HyS PLECS Model

IGBT only sweep

Load Current [A]	IGBT Cond. Loss [W]	IGBT Sw. Loss [W]	IGBT Total Loss [W]
2000	2889	6767	9656
1750	2251	4894	7145
1500	1712	3242	4954
1250	1265	2431	3696
1000	874	1987	2861
750	554	2001	2555
500	297	1829	2126
250	98	989	1087

Table D.7: IGBT losses as a function of load current

HyS - Load current sweep

Load Current [A]	Max. Sw. Freq. [Hz]	SiC Junction Temp [Hz]	IGBT Junction Temp [C]	Hys Cond. Loss [W]	HyS Sw. Loss [W]	HyS Total Loss [W]	SiC Current [A]	IGBT Current [A]	Current ratio [-]
2000	11250	135	119	3083	976	4059	460	1540	3.35
1750	17650	135	112	2583	1315	3898	460	1290	2.80
1500	26550	135	106	2091	1667	3758	459	1041	2.27
1250	39700	135	102	1602	2040	3642	459	791	1.72
1000	43600	112	84	1074	1785	2859	459	541	1.18
750	57950	105	77	721	1833	2554	459	291	0.63
500	69100	93	67	472	1654	2126	458	42	0.09
250	54750	60	57	134	952	1086	250	0	0.00

Table D.8: HyS parameters as a function of load current

HyS - Stray inductance sweep

Stray Inductance [nH]	Max. Sw. Freq. [Hz]	SiC Junction Temp [C]	IGBT Junction Temp [C]	Hys Cond. Loss [W]	HyS Sw. Loss [W]	HyS Total Loss [W]
10	11250	135	119	3083	976	4059
20	8500	135	117	3275	738	4013
30	6800	135	116	3386	590	3976
40	5700	135	116	3467	494	3961
50	4850	135	115	3511	421	3932
60	4250	135	115	3553	369	3922
70	3750	135	114	3574	325	3899
80	3350	135	114	3589	290	3879
90	3050	135	114	3611	264	3875
100	2800	135	114	3630	243	3873

Table D.9: HyS parameters as a function of stray inductance

HyS - Number of MOSFETs sweep

Nr. of MOSFETs [-]	Max. Sw. Freq. [Hz]	SiC Junction Temp [C]	IGBT Junction Temp [C]	Hys Cond. Loss [W]	HyS Sw. Loss [W]	HyS Total Loss [W]	SiC Current [A]	IGBT Current [A]	Current ratio [-]
20	11250	135	119	3083	976	4059	460	1540	3.35
18	9650	135	118	3147	852	3999	414	1586	3.83
16	8050	135	117	3201	724	3925	368	1632	4.43
14	6500	135	117	3252	599	3851	323	1677	5.19
12	5050	135	116	3269	478	3747	277	1723	6.22
10	3800	135	114	3262	373	3635	231	1769	7.66

Table D.10: HyS parameters as a function of number of SiC MOSFETs in parallel

HyS - Duty cycle sweep

Duty Cycle [-]	Max. Sw. Freq. [Hz]	SiC Junction Temp [C]	IGBT Junction Temp [C]	Hys Cond. Loss [W]	HyS Sw. Loss [W]	HyS Total Loss [W]
0.8	4800	135	136	4086	416	4502
0.7	7000	135	130	3752	607	4359
0.6	9100	135	124	3413	790	4203
0.5	11250	135	119	3083	976	4059
0.4	13350	135	113	2754	1159	3913
0.3	15450	135	107	2429	1341	3770
0.2	17500	135	102	2105	1519	3624

Table D.11: HyS parameters as a function of duty cycle

HyS - Die attach material

Die Attach Material [-]	Th. Resistance [K/kW]	Max. Sw. Freq. [Hz]	SiC Junction Temp [C]	IGBT Junction Temp [C]	Hys Cond. Loss [W]	HyS Sw. Loss [W]	HyS Total Loss [W]
TIM	2.65	11250	135	119	3083	976	4059
Pasta	6.3	8550	135	124	2909	742	3651
Graphite	7	8100	135	125	2880	703	3583
Discrete Components	8.96	6900	135	127	2803	599	3402

Table D.12: HyS parameters when using different die attach materials

HyS - Cooling Method

Cooling Method [-]	Th. Resistance [p.u]	Max. Sw. Freq. [Hz]	SiC Junction Temp [C]	IGBT Junction Temp [C]	Hys Cond. Loss [W]	HyS Sw. Loss [W]	HyS Total Loss [W]
Double Sided	0.5	20900	135	99	3709	1815	5524
Forced Air	1	11250	135	119	3083	976	4059
Passive	2	1950	135	137	2485	169	2654

Table D.13: HyS parameters when using different cooling methods

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