Master's thesis

NTNU
Norwegian University of Science and Technology
Faculty of Information Technology and Electrical Engineering
Department of Electric Power Engineering

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PSCAD Simulation of Distance Protection Performance in a Grid with Inverter Interfaced Generation

Master's thesis in Master of Energy and Environmental Engineering
Supervisor: Hans Kristian Høidalen
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Abstract

In this thesis, the performance of distance protection in a grid with inverter interfaced generation has been studied through PSCAD simulations. Statnett expects problems related to their distance protection relays close to the Fosen Wind project, where several wind farms will be finalized in 2020. At which point distance protection problems should be expected due to the increasing share of inverter interfaced generation, serves as the main problem of the thesis.

The developed PSCAD model consists of a transmission line with 3.6 MVA inverters connected to the left side, and a grid equivalent connected to the right side. Distance protection relays have been installed on both ends of the line to analyze how their performance is influenced by the inverters. Balanced three-phase to ground short circuits located on the center of the line have been used for the protection studies.

Simulation set 1 showed that a single inverter connected to the line caused unsatisfactory tripping for the inverter side relay.

Simulation set 2 showed that ten inverters connected to the line caused unsatisfactory tripping for the inverter side relay, however there was a slight performance improvement compared to Simulation set 1.

Simulation set 3 showed that when inverter generation was compared with synchronous generation, higher inverter generation shares caused reduced inverter side relay performances. For fault resistances of 1 Ω or less, the inverter side relay was able to trip satisfactorily for inverter generation shares of 50% or less.

Simulation set 4 showed that the ratio of the short circuit current contributions from the two sides of the line had a negative influence on the relay installed on the side with the lowest contribution. The influenced relay was able to trip satisfactorily for fault resistances of 0.1 Ω or less, with up to roughly 70 times larger short circuit current contribution from the other side.

The distance protection relay located on the grid side of the line did not experience any problems during any of the simulations.

However, due to the model assumptions and weaknesses, the obtained results cannot be used to give any general statements regarding the performance of distance protection in a grid with inverter interfaced generation. More research is needed to be able to give accurate statements related to which problems should be expected and under which circumstances they will occur.

Sammendrag

I denne oppgaven har ytelsen til distansevern i et kraftnett med vekselretter-tilkobede produksjonskilder blitt studert gjennom simuleringer i PSCAD. Statnett forventer at problemer for distansevern vil oppstå i nærheten av vindprosjektet Fosen Vind, hvor fleretalls vindparker blir ferdigstilt i 2020. Problemstillingen i oppgaven går ut på å finne et svar på når det dukker opp problemer for distansevernet, som følge av en stadig økende andel av vekselretter-tilkoblede produksjonskilder.

PSCAD modellen består av en transmisjonslinje med vekselrettere på 3,6 MVA tilkoblet venstre ende, og en nett-ekvivalent tilkoblet høyre ende. Distansevern har blitt installert i begge endene av linjen for å analysere hvordan ytelsen deres blir påvirket av vekselrettere. Symmetriske tre-fase-til-jord-feil midt på linjen har blitt brukt som utgangspunkt for studien.

Simuleringssett 1 viste at når én enkel vekselretter var tilkoblet linjen medførte det uakseptabel håndtering av feilen for reléet på vekselretter-siden.

Simuleringssett 2 viste at når ti vekselrettere var tilkoblet linjen medførte det uakseptabel håndtering av feilen for reléet på vekselretter-siden, men med en liten forbedring i ytelsen sammenliknet med Simuleringssett 1.

Simuleringssett 3 viste at når produksjon fra vekselrettere ble sammenliknet med produksjon fra synkronmaskiner medførte en høyere andel vekselretter-produksjon en redusert ytelse for reléet på vekselretter-siden. For feilmotstander på 1 Ω eller mindre klarte reléet på vekselretter-siden å håndtere feilen korrekt for en vekselretter-andel på 50% eller lavere.

Simuleringssett 4 viste at forholdet mellom kortslutnings-strømbidraget fra de to endene av linjen hadde en negativ påvirkning på reléet installert på siden med lavest bidrag. Reléet klarte å håndtere feilen korrekt for feilmotstander på 0.1 Ω eller mindre, med opp mot 70 ganger høyere bidrag fra den andre siden.

Distansevernet på nett-siden av linjen opplevde ingen problemer under noen av simuleringene.

På grunn av antakelsene og svakhetene i modellen kan resultatene ikke bli brukt til å gi noen generelle uttalelser om ytelsen til distansevern i et kraftnett med produksjon fra vekselrettere. Mer forskning er nødvendig for å kunne gi nøyaktige uttalelser om hvilke problemer som kan forventes, og under hvilke omstendigheter de vil inntreffe.

Preface

This master thesis finalizes my work at NTNU's master program Energy and Environmental Engineering with specialization in Electric Energy Technology and Smart Grids. I have always had a great interest for the electric power systems as it is critical for our society. It has been interesting to follow the progress of renewable energy technologies the recent years, which has lead to new important research topics. How to deal with the challenges emerging from the shift towards new renewable energy technologies has been my main motivation for choosing this topic for my master thesis.

I would like to give a big thanks to my supervisor Pr. Hans Kristian Høidalen for the continuous support and guidance I have received along the way. It has been rewarding to join the ProDig cooperation project and for getting the opportunity to present my work for all the participants. This has been very motivating as I have received positive response, and it has helped me to better understand the importance of my work.

The cooperation with Statnett throughout this project has been very valuable. Magnus Kolgrov, leader of protection in Statnett, has proposed the main research question of the thesis and provided great material to work with. Jorun Irene Marvik, relay planner in Statnett and co-supervisor, has offered continuous assistance and provided key parameters for the PSCAD model. I am very thankful for the help I have received, which has been essential for the progress of the thesis.

I would like to thank PhD candidate Maciej Grebla for great assistance with the development of the inverter model. Sharing of the inverter model developed in Simulink has been very helpful and has speeded up the model development significantly. I am also very thankful for Pr. Mohammad Amin's sharing of knowledge regarding inverter design.

Additionally, the conversations I have had with scientists at Sintef have been very helpful, and I would like to thank Jon Are Wold Suul, Kjell Ljøkelsøy and Salvatore D'Arco for sharing their knowledge.

At last, I would like to thank family and friends for the great support throughout the project.

It has been most rewarding to work with this master thesis, and I hope it will prove useful.

June 2020
Nicolay Anker Kavli

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Abbreviations

AC	Alternating Current
DC	Direct Current
DER	Distributed Energy Resources
DSOGI	Dual Second-Order Generalized Integrator
EMTDC	Electromagnetic Transient Program Including DC
FLL	Frequency Locked Loop
FRT	Fault Ride Through
IGBT	Insulated-Gate Bipolar Transistor
LC	Inductance-Capacitance filter
LCL	Inductance-Capacitance-Inductance filter
L-G	Single-phase to ground short circuit
L-L	Two-phase short circuit
L-L-G	Two-phase to ground short circuit
L-L-L	Three-phase short circuit
L-L-L-G	Three-phase to ground short circuit
PCC	Point of Common Coupling Bus for the Inverters
PSCAD	Power System Computer Aided Design
PV	Photovoltaics
PI	Proportional Integral
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
RMS	Root Mean Square
SRF	Synchronous Reference Frame
T4WT	Type 4 Wind Turbine utilizing a full-scale converter

1 Introduction

1.1 Background and Motivation

The share of renewable energy generation, grid-connected via inverters, is increasing rapidly [1] [2]. Technologies like wind and solar power utilize inverters for connection to the AC grid, changing the properties of the grid which has earlier been dominated by synchronous generation. One of the problems associated with the transition from synchronous generation to inverter interfaced generation, is the influence on grid protection [1] [3] [4]. This is critical as protection technologies which has proven to be effective in the past, may not operate reliably any longer. The emerging protection issues should be investigated thoroughly to maintain secure protection of the power grid.

Distance protection is commonly used today for main and backup protection of transmission lines [1] [3] [4]. The performance of this technology is expected to suffer from the increasing share of inverter interfaced generation. Multiple papers [5] [6] [7] have already pointed out concerns for such relays when used together with inverter interfaced generation, as the short circuit current contribution from inverters is strictly limited and unpredictable. For instance, this will influence the distance protection's ability to accurately measure the fault impedance which is essential for correct relay operation. Thus, it is expected that areas with a high share of inverter interfaced generation may experience relay malfunctioning, which is highly undesirable.

The ongoing Fosen Wind project in Norway is a practical example of where protection issues may arise. In this area, 278 inverter interfaced wind turbines (type 4) with a total capacity of 1 GW, are expected to cause challenges for the distance protection relays close by [8] [9]. Statnett, which is responsible for the main transmission grid in Norway, has requested the need for studies investigating the severity of the situation. Statnett's main motivation for this is based on a recently published ENTSO-E report stating that distance protection is the main protection technology expected to suffer the most from a high penetration of wind and solar power [4]. Problems related to fault impedance measurements and faulty phase selection are expected to arise. This summarizes the main motivation for the execution of the study.

A more precise definition of the problem given by Statnett is: "Are there indicators one can point to for determining when distance protection relays will start experiencing performance issues due to the increasing share of inverter interfaced generation?". A suggestion from Statnett was to look into the share of inverter interfaced generation, and if this could be used as an accurate indicator for answering the problem.

1.2 Approach

From the very beginning, based on discussions with Statnett and supervisor, it was agreed to develop a model in the EMTDC-based simulation program called PSCAD. PSCAD was chosen for performing the simulations as it was considered to be the most reliable program for handling power electronics. The model had to include a wind turbine model, a representative grid, and distance protection relays.

It was chosen to focus solely on type 4 wind turbines, connected to the grid via full-scale back-to-back frequency converters. The main reason for this choice was that all of the wind turbines at Fosen are type 4 wind turbines. The ENTSO-E report covers both type 3 (doubly-fed induction generators) and type 4 wind turbines as both of these contain power electronics. However, as type 4 wind turbines have gained an increasing market share the recent years and is now dominating the current market [10], it was considered reasonable to limit the scope to this technology.

As there is a lot of complexity associated with a complete wind turbine model, it would be beneficial to develop a simplified model for the simulations. Type 4 wind turbines are grid-connected via inverters, meaning that the current fed to the grid is solely determined by the inverter and its DC voltage. Thus, for grid side studies like in this thesis, it was decided to make a simplified model of the wind turbine with a DC sourced inverter [5] [6] [7].

For the grid, Statnett provided grid parameters such that the grid was relatively comparable to the grid at Fosen.

The distance protection relays were modelled, based on PSCAD's own cookbook for protection studies [11].

1.3 Scope

The aim of this thesis is to obtain useful simulation results about the impact of inverter interfaced generation on distance protection performance in a radial grid topology. Due to model limitations, only balanced three-phase to ground faults have been covered, yet for various fault resistances ranging from 0.1 mΩ to 10 Ω. The fault location has been set to the center of line. The results will primarily cover the accuracy of the fault impedance measured by the inverter side relay, and the corresponding tripping times for zone 1.

Simulation set 1 covers the influence of one single inverter connected to the line.

Simulation set 2 covers the influence of ten inverters connected to the line.

Simulation set 3 covers the influence of a varying inverter generation share of total generation.

Simulation set 4 covers the influence of different short circuit current contributions from the two sides of the line.

Additionally, this thesis will explain most details of the developed model and the approach for obtaining it. The aim is to make it easy to recreate the model, both for verification and improvement reasons. Thus, further work will be easier to conduct.

2 Theory

2.1 Grid short circuits

Short circuit faults in the power grid are short circuits between the lines and/or ground. Short circuits are undesirable and should be dealt with as quickly as possible to prevent damage to grid components. In three-phase power systems, short circuit faults are categorized into the following types [12]:

- Single-phase to ground (L-G) short circuit
- Two-phase (L-L) short circuit
- Two-phase to ground (L-L-G) short circuit
- Three-phase (L-L-L) short circuit
- Three-phase to ground (L-L-L-G) short circuit

L-L-L and L-L-L-G faults are considered balanced faults as all of the phases are influenced in the same way. During a perfectly balanced fault the voltages and currents are phase-displaced by 120° from each other and have identical magnitude. In such a balanced system, only positive sequence components exist. The other fault types are considered unbalanced, as the individual phases are influenced differently. During unbalanced faults there will be negative and/or zero sequence components in addition to the positive sequence components. The zero sequence components will depend on the system earthing [12]. Symmetrical components (positive, negative and zero sequence components) are explained in the upcoming section.

According to Statnett, single-phase to ground faults are the most common fault type for grids with transmission lines. Balanced faults are less common, and have lower fault resistances.

2.2 Symmetrical components

Under normal steady-state operation of a three-phase system, the system is assumed to be symmetrical (balanced) [13]. In a symmetrical three-phase system, the electrical signals have the same magnitude, and are phase-shifted 120 degrees from each other. During such conditions, the calculation of voltages, currents, load flow and loads is simplified significantly with per-phase analysis [14].

However, when abnormal operating conditions are present, such as asymmetrical grid faults, more complex calculation methods will have to be adapted.

During asymmetric conditions, it is required that all phases (which may have completely different behaviour) are described independently from each other. The "Symmetrical components model" allows for asymmetric systems to be described with symmetrical components, which simplifies asymmetrical system calculation considerably. The symmetrical components are displayed in Figure 1. It has been proven that any asymmetrical signal can be represented by a combination of the positive, negative and zero sequence components. This means that a three-phase signal with arbitrary magnitudes and phases may be represented by a set of symmetrical components.

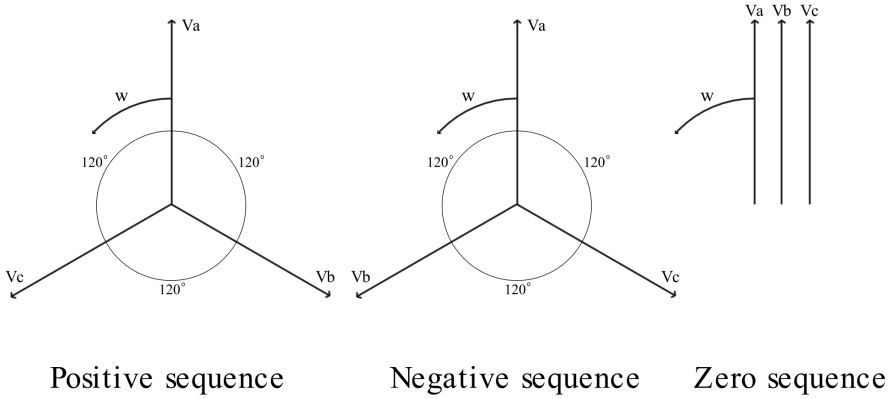


Figure 1: The three symmetrical components; positive, negative and zero sequence components [14].

The positive sequence component rotates counter-clockwise with phase sequence abc. The angular speed of which the vectors rotate is the fundamental angular frequency of the power system $\omega = 2\pi f$ during normal operation. Each of the three vectors it consists of have the same magnitude and are phase displaced by 120 degrees from each other. [15]

The negative sequence component does also rotate counter-clockwise, but as phase b and c have switched positions, the resulting phase sequence will be acb. The angular speed is the same in magnitude, but with the opposite polarity. Similarly to the positive sequence, the three vectors have the same magnitude and are phase displaced by 120 degrees from each other. Alternatively, one can say that the negative sequence component rotates clockwise (without switching phase b and c).

The zero sequence component differs from the other two as all of the vectors have the same phase (they are phase displayed by 0 degrees from each other). Still, the magnitudes of the vectors are equal, and the angular speed is the same

as for the other symmetrical components.

To better illustrate how an asymmetrical set of signals can be represented by a combination of the three sequence components mentioned above, Figure 2 visualizes the superposition of the vectors.

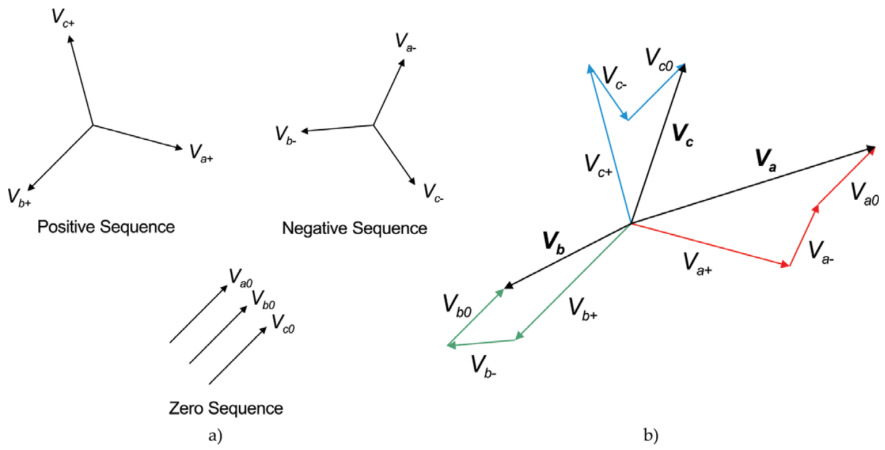


Figure 2: Visualization of how the symmetrical components a) can be combined to express an asymmetrical set of signals b) V_a, V_b and V_c [16].

The set of equations for describing an asymmetrical three-phase signal with symmetrical components are shown in equation (1) - (10) below [14].

$$V_a = V_a^+ + V_a^- + V_a^0 \tag{1}$$

$$V_b = V_b^+ + V_b^- + V_b^0 \tag{2}$$

$$V_c = V_c^+ + V_c^- + V_c^0 \tag{3}$$

$$V_a^+ = V^+\sqrt{2}sin(\omega t + \phi^+) \tag{4}$$

$$V_b^+ = V^+\sqrt{2}sin(\omega t + \phi^+ - \frac{2\pi}{3}) \tag{5}$$

$$V_c^+ = V^+\sqrt{2}sin(\omega t + \phi^+ + \frac{2\pi}{3}) \tag{6}$$

$$V_a^- = V^-\sqrt{2}sin(\omega t + \phi^-) \tag{7}$$

$$V_b^- = V^- \sqrt{2} sin(\omega t + \phi^- + \frac{2\pi}{3}) \tag{8}$$

$$V_c^- = V^- \sqrt{2} sin(\omega t + \phi^- - \frac{2\pi}{3}) \tag{9}$$

$$V_a^0 = V_b^0 = V_c^0 = V^0 \sqrt{2} sin(\omega t + \phi^0) \tag{10}$$

For a phasor representation in matrix form, the same set of equations can be represented as in equation (11).

$$\begin{bmatrix} Va \\ Vb \\ Vc \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ a^2 & a & 1 \\ a & a^2 & 1 \end{bmatrix} \begin{bmatrix} V^+ \\ V^- \\ V^0 \end{bmatrix} \tag{11}$$

2.2.1 The use of symmetrical components in power systems

Symmetrical components may be used for any three-phase system and can be used for describing both voltages and currents of a power system. Since the voltages and currents during normal steady-state operation are symmetrical, the utilization of symmetrical components is linked with abnormal conditions [15]. A practical example of when symmetrical components are used is during grid faults.

Short circuits in the power grid are in most cases asymmetrical single phase to ground faults [17]. For instance, when a short circuit occurs between a single phase and ground, that phase will have a much lower impedance to ground, causing the current to increase and the voltage to drop.

To better decouple the different sequence components from each other, it makes sense to define positive sequence impedances, negative sequence impedances and zero sequence impedances in the power system, each of them related to the voltage/current ratio for that specific sequence [13]. As positive and negative sequence currents sum up to zero in the neutral point (there is no return current), the impedances for these two sequences are the same for static components such as lines, cables and transformers. Note that for rotating machines, inverters and other non-static components the impedance can differ between them. In contrast, the zero sequence impedance is related to the impedance of the return path, as the currents of the three phases do not sum up to zero. The flow of zero sequence component current depends on whether the fault is connected to ground, yet also the system earthing (transformer earthing) [13].

Even though some older inverter designs may rely solely on positive sequence, inverters may have implemented control logic for handling asymmetrical conditions [4] [18]. In such cases the sequence components will have to be extracted

from the main three-phase signal. Newer inverters have the ability to detect and control both positive sequence and negative sequence components, and they may even support the grid with asymmetrical current if this is desired. Inverters supporting negative sequence control have a much more comprehensive control systems, and techniques for efficient extraction is desired.

2.3 Distance Protection

2.3.1 Fundamentals of Distance Protection

The distance protection is a commonly used protection technology for main short circuit protection of transmission lines, but does also work as backup protection [12] [19]. During a grid fault, the distance protection relay is responsible for the detection of the fault, and tripping of the corresponding circuit breaker to disconnect the faulted line from the rest of the grid. Preferably, the disconnected part of the grid should be as close to the fault as possible to minimize grid capacity loss and letting the current take an alternative route from the generation to the loads. In other words, only the faulted line should be disconnected from the grid.

A transmission line typically has two distance protection relays, one relay installed at each end of the line, facing towards each other. To locate the fault, the distance protection estimates the fault impedance Z from the relay to ground by measuring the voltages and currents of the line. A voltage transformer and a current transformer are used for the measurements. The fault impedance is calculated $Z = \frac{V}{I}$, and the corresponding reactance will be proportional to the distance from the relay to the fault, allowing for estimation of the fault location. In such a way, distance protection relays are able to provide selectivity, even without any communication between the relays. The idea is that the estimated distance is precise enough such that only the closest relays trip their breakers, and only the faulted line is disconnected from the grid [19].

In general, during normal grid operation, the grid voltage is high, at rated voltage, and the current is low, at up to rated current. During a short circuit, the local voltage will drop and the current will increase. The estimated fault impedance by the distance protection will in other words be high during normal operation, and low during faults. In this way, the relay can distinguish faulted cases from normal operation. The relay will decide to send a tripping signal if the estimated fault impedance Z is detected within a predefined area in the impedance plane, indicating that a fault has occurred. These dedicated areas in the impedance plane are referred to as zones [19].

A zone in the impedance plane of the relay, determines the borders of which impedances the relay should interpret as faults, and when the relay should respond. To provide selectivity and ensure that the closest relays trip first, the

closest relays should respond before the others. This implies that each relay should possess multiple zones, with different time delays. For instance, zone 1 of a relay corresponds to 80-90% of the line the relay is protecting, and has no added time delay. This means that the relay should respond as quickly as possible to faults on that line. Zone 2 for the same relay will reach further, and with an added intentional time delay. An impedance diagram with multiple zones is shown in Figure 3. As the resistance and the reactance per unit length of the transmission line is known, the impedance from the relay to any location on the line is also known. In the impedance diagram, this can be visually observed as the angle ϕ, which corresponds to the reactance/resistance ratio of the line and is close to 85° for overhead transmission lines. The line impedance is used associate the estimated fault impedance Z with the distance to the fault. During a short circuit, the impedance from the faulted lines to ground is mostly resistive. Thus, the reactance of the estimated fault impedance by the relay is directly proportional with the distance to the fault. Consequently, the height of the zone in the impedance diagram (the reactance) can be set to the desired value, such that only the closest faults (in forward direction) will appear within zone 1 of the relay, and faults further away will appear in the higher level zones with intentional time delays [19].

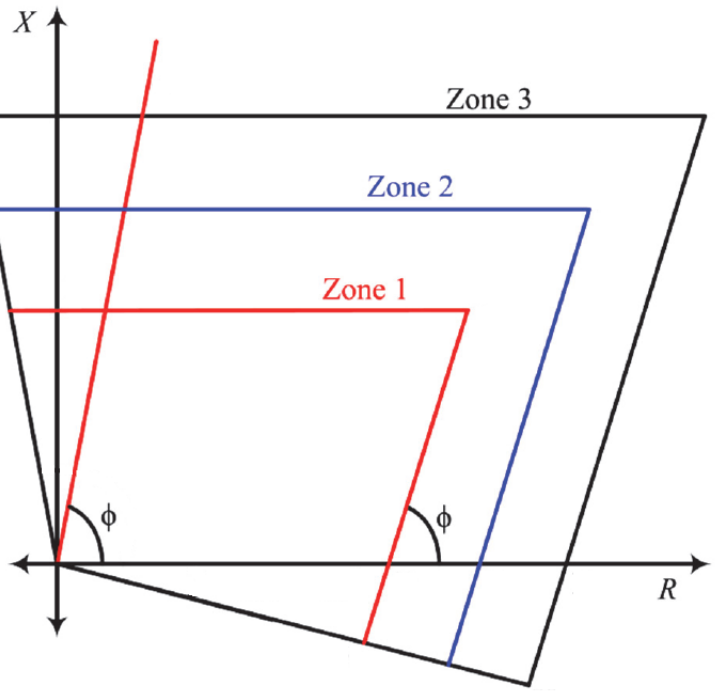


Figure 3: Distance protection impedance diagram with multiple zones [20].

When the reach of the zones are to be set, one must take measurement inaccuracies into account. As the estimated impedance by the relay may differ from the actual impedance, the reach of zone 1 has to be less than 100% of the line. This is to ensure that faults beyond the main protected line are not causing the neighboring relays to trip too early due to measurement inaccuracies. This can be explained with Figure 4. Thus, zone 1 is normally chosen to be 85% of the line for numerical distance protection [19].

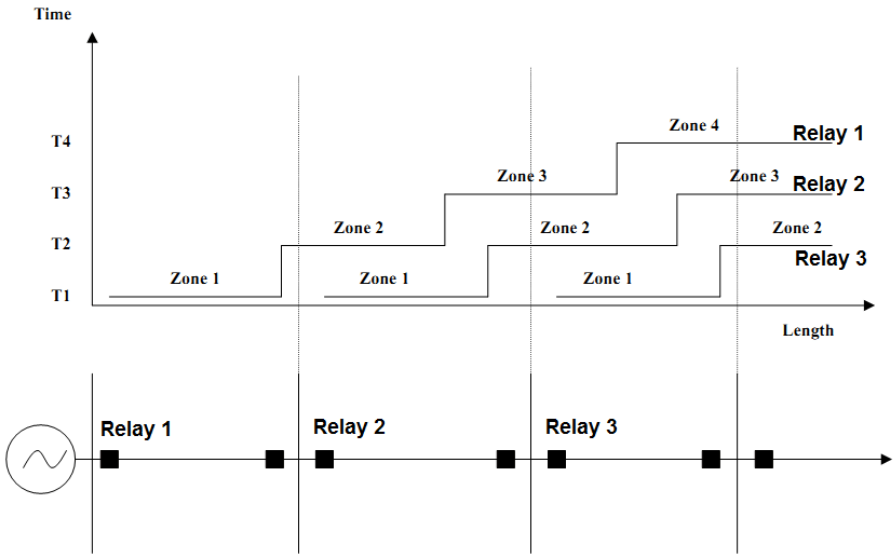


Figure 4: General zone reaching for distance protection. Each zone has a corresponding time delay [21].

2.3.2 Fault loops

In a three-phase system, there can be different types of faults, which may influence the phases differently. To be able to determine which phases are faulted, the relays typically use six fault loops to capture all the fault types [19]. The six fault loops are L1-G, L2-G, L3-G, L1-L2, L2-L3 and L3-L1.

The voltage and current transformers measure the voltages and currents of each loop, and if at least one loop is indicating a fault, the relay will send a tripping signal to the breaker. Distance protection relays can be classified into two groups; multiple-system-relays and single-system-relays. Multiple-system-relays are preferable, but are mostly used for higher voltage transmission lines above 132kV, due to the higher cost [12]. Single-system-relays are cheaper, and are commonly used for the 66kV and 132kV grids in Norway [12]. For multiple-system relays, three of the fault loops will be measured by Line-Ground systems,

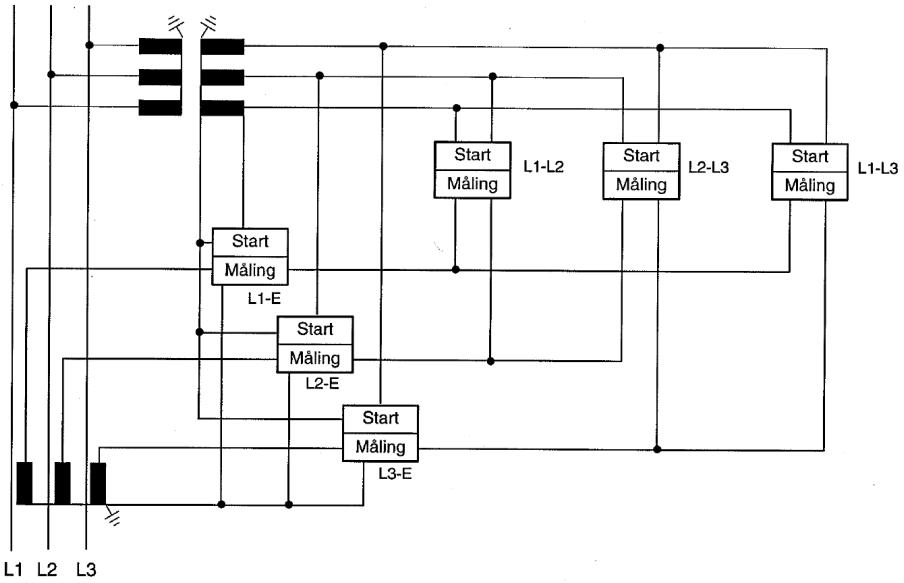


Figure 5: The six fault loops measured by a multiple-system distance protection relay. [12]

and three will be measured by Line-Line systems, like in Figure 5. For single-system relays a fault loop must be chosen for the measurement, like in Figure 6. The estimated fault impedances by the relays for each loop is given below from equation (12) to (17) [19].

$$Z_{L1-E} = \frac{U_{L1}}{I_{L1} - k_E \cdot I_E} \tag{12}$$

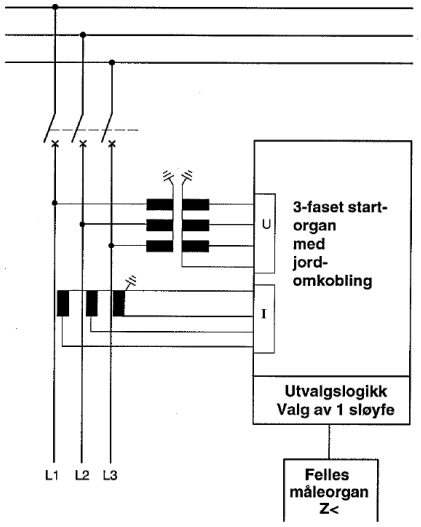
$$Z_{L2-E} = \frac{U_{L2}}{I_{L2} - k_E \cdot I_E} \tag{13}$$

$$Z_{L3-E} = \frac{U_{L3}}{I_{L3} - k_E \cdot I_E} \tag{14}$$

$$Z_{L1-L2} = \frac{U_{L1} - U_{L2}}{I_{L1} - I_{L2}} \tag{15}$$

$$Z_{L2-L3} = \frac{U_{L2} - U_{L3}}{I_{L2} - I_{L3}} \tag{16}$$

$$Z_{L3-L1} = \frac{U_{L3} - U_{L1}}{I_{L3} - I_{L1}} \tag{17}$$



Startkriterium	Utvalgt sløyfe
L1, E	L1-E
L2, E	L2-E
L3, E	L3-E
L1, L2	L1-L2
L2, L3	L2-L3
L1, L3	L3-L1
L1, L2, E	L2-E
L2, L3, E	L3-E
L1, L3, E	L3-E
L1, L2, L3	L2-L3
L1, L2, L3, E	L3-E

Figure 6: The six fault loops measured by a single-system distance protection relay. [12]

The line to ground measurements have to be corrected with the zero sequence compensation factor k_E, as the zero sequence current is influencing the measurement. The zero sequence compensation factor k_E and the earth current I_E are given in equation (18) and (19) [19]. Z_0 and Z_1 indicates the zero sequence and positive sequence impedance of the line, respectively.

$$k_E = \frac{Z_0 - Z_1}{Z_1} \tag{18}$$

$$I_E = -\frac{1}{3}(I_{L1} + I_{L2} + I_{L3}) \tag{19}$$

2.3.3 Impact of different short circuit current contributions

Consider a single transmission line with distance protection relays in both ends (see Figure 7). As the relays are measuring the voltages and currents locally, the current contribution from the other end is not taken into consideration [6]. For higher fault resistances, relays with lower short circuit current contribution from their side may experience a significant loss in the impedance measurement accuracy.

The measured fault impedance by Relay 1 is expressed below in equation (20).

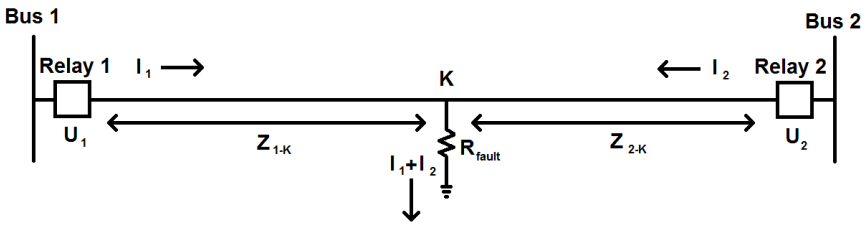


Figure 7: Representation of a faulted transmission line with distance protection relays at both ends. The fault location is denoted K, and the the fault resistance of the short circuit is R_{fault}. Z_{1-K} and Z_{2-K} are the the line impedances from each of the buses to the fault location K. The figure is based on [6].

$$Z_{Relay\_1} = \frac{\dot{U}_1}{\dot{I}_1} = \frac{\dot{I}_1 Z_{1-K} + (\dot{I}_1 + \dot{I}_2) R_{fault}}{\dot{I}_1} = Z_{1-K} + Z_{ad} \tag{20}$$

Z_{Relay_1} and Z_{Relay_2} are the actual fault impedances measured by the relays. The impedances Z_{1-K} and Z_{2-K} are the line impedances from each of the buses to the fault location K. R_{fault} is the fault resistance. The currents from each of the sides are denoted $\dot{I}_1$ and $\dot{I}_2$. $\dot{U}_1$ and $\dot{I}_1$ are the phase voltages and phase currents with zero-sequence compensation for Line-Ground measuring units, and line voltages and line currents for Line-Line measuring units.

Referring to equation (20), the measured impedance consists of two components, the line impedance to the fault Z_{1-K}, and an additional impedance Z_{ad}. The additional impedance is influenced by the current from the other side, yet this current is not measured by Relay 1. To better illustrate the problem, a single phase to ground loop is looked into for a three-phase fault. The fault impedances measured by the relays are shown in equation (21) and (22).

$$Z_{Relay\_2} = Z_{2-K} + (1 + \frac{\dot{I}_1}{\dot{I}_2}) R_{fault} \tag{21}$$

$$Z_{Relay\_1} = Z_{1-K} + (1 + \frac{\dot{I}_2}{\dot{I}_1}) R_{fault} \tag{22}$$

Given the assumption that the short circuit current contribution from Bus 2 is much higher than from Bus 1, the fault impedance measured by Relay 1 Z_{Relay_1} will be influenced by the high current ratio $\frac{\dot{I}_2}{\dot{I}_1}$. This may lead to a

significant measurement error, especially for large fault resistances R_{fault}. Depending on the phase of $\frac{\dot{I}_2}{\dot{I}_1}$, the additional impedance Z_{ad} may appear inductive or capacitive, causing the reactance of Z_{Relay_1} to differ from the reactive part of the line impedance Z_{1-K}, which is what the zone-reaching of distance protection relays are based on. This may cause the unwanted behaviours like underreaching and overreaching, as explained in the next section. For more severe cases, the estimated fault impedance may be appear very far away from actual fault impedance and never appear in any of the zones of the relay [6].

2.3.4 Underreaching and overreaching

Due to the influencing factors affecting the measurement accuracy of distance protection relays, the estimated fault impedance (Z_{Relay_1}) may be larger or smaller than the actual fault impedance ($Z_{1-K} + R_{fault}$) [6]. This may cause the impedance to appear in the wrong zone or in none of the zones. Two terms are used to describe this behaviour; underreaching and overreaching.

A relay is underreaching when the fault impedance is measured to be higher than the actual impedance. This may cause faults to appear in zones higher than it should, resulting in longer time delays before fault clearing.

In contrast, a relay is overreaching when the fault impedance is measured to be lower than the actual impedance, which may cause the relay to treat the faults as if they were in zones lower than they should. This may cause unnecessary tripping of more transmission lines than required, which will disconnect a larger part from the power grid.

2.3.5 Current and voltage transformers

The voltage and current transformers used by distance protection relays should be able to give precise measurements, with a defined minimum accuracy and transient behaviour [19].

Protection voltage transformers usually have a maximum error of 3% or 6%, and transform the primary system voltage to the secondary rated voltage of about 100 V [19]. Inductive voltage transformers are preferred over capacitive voltage transformers due to their high accuracy, even during voltage collapses down to 1% of rated voltage.

Protection current transformers usually have a maximum error of 5% or 10% depending on the classification, and has a transformation ratio of $\frac{600A}{1A}$ or $\frac{600A}{5A}$ [19].

2.3.6 Pilot distance protection

Conventional distance protection does not possess any communication between the relays. The selectivity is solely determined by the zones of the relays and the locally measured fault impedance. Pilot distance protection improves the classic distance protection by introducing communication cables between neighboring relays [19]. The communication will allow for faster tripping of both ends of the faulted line when the fault location is close to one of the relays. Without pilot protection, faults beyond the reach of zone 1, but still on that line, will appear in zone 2 of the relay installed in the other end, causing delayed tripping. Pilot protection improves the tripping time of the distant relay by letting the closest relay send a tripping signal (indicating that the fault has appeared within zone 1 of the relay) and thereby override the decision making of the other relay.

Thus, pilot distance protection effectively has a zone 1 reach of 100% of the main line. For higher level zones, the operation is similar to classic distance protection. Note that faults very close to the relays may still cause problems as it is challenging to determine whether the fault is in forward direction or backward direction when the voltage drops significantly. Multiple common pilot protection schemes exist; DUTT, POTT, DCUB and DCB [22], yet they will not be covered here.

2.4 Per Unit values

In power systems it is common to express voltages, currents, power etc. in per unit [23]. Per unit (pu) representation is convenient to deal with, as it is dimensionless and is easily comparable to rated conditions.

To express system quantities in pu, the base values have to be defined. Two main base values are specified, and the other base values are derived. For three phase systems the relation between the different base values for the system is shown in equation (23) to (25).

$$I_{base} = \frac{S_{base}}{\sqrt{3}V_{base}} = 1pu \tag{23}$$

$$Z_{base} = \frac{V_{base}}{\sqrt{3}I_{base}} = \frac{V_{base}^2}{S_{base}} = 1pu \tag{24}$$

$$Y_{base} = \frac{1}{Z_{base}} = 1pu \tag{25}$$

After the base values are defined, the system quantities are divided by their corresponding base value to obtain the pu value (26).

$$X_{pu} = \frac{X}{X_{base}} \tag{26}$$

In general, S_{base} is the three-phase rated apparent power, and V_{base} is the line-to-line RMS voltage.

2.5 Control systems

Control systems are used in a wide variety of fields, for different purposes. Two common types of controllers are the Proportional (P) and Proportional Integral (PI) controllers [24].

The P-controller will take the error (between the reference signal and the measured signal), and apply a correction which scales with the error. Thus, the higher the error, the stronger the effect of the correction. The transfer function $h(s)$ of a P-controller in the s-plane is shown in equation (27) [24]. $u(s)$ is the controller output (correction), and $e(s)$ is the controller input (error). K_p is a the proportional constant chosen by the designer.

$$h(s) = \frac{u(s)}{e(s)} = K_p \tag{27}$$

The PI-controller will possess a proportional controller in addition to an integral controller. The integrator adds up the error over time, and applies a correction based on this. By introducing an integrator, the stationary error can be eliminated, which is preferred. The transfer function of a PI-controller in the s-plane is shown in equation (28) [24]. Here, $T_i = \frac{K_p}{K_i}$, where K_i is the integral constant, and T_i is the integral time constant.

$$h(s) = \frac{u(s)}{e(s)} = K_p + \frac{K_i}{s} = K_p(1 + \frac{1}{T_i s}) \tag{28}$$

2.6 Inverters

2.6.1 Fundamentals of inverters

In general, the term "converter" can be used to describe any transformation between DC and AC voltage [25]. More precisely, the subcategories of the con-

verter can be classified into rectifiers and inverters. Rectifiers transform AC voltage into DC voltage and inverters transform DC voltage into AC voltage. Back-to-back frequency converters can be used for AC-DC-AC converters, consisting of both a rectifier and an inverter. The inverter converting DC into AC will be the focus in this section.

Power inverters are used to describe inverters with higher power ratings, and are used to connect DC sources like PV plants, batteries and HVDC links to the AC power grid. Additionally, newer types of wind turbines are grid-connected via inverters. The inverter has become increasingly more important in the power system during the recent years due to the transition towards renewable energy resources like solar and wind power[25].

The most common inverter implementation is DC to AC transformation via pulse width modulation (PWM) [25]. The concept of PWM is about outputting a DC signal with variable duty cycles and smoothing it to best represent an AC signal. There are several different variations of inverter designs, yet the basics remain the same. A two-level three phase inverter is shown in Figure 8. The DC voltage U_{DC}, is supplying the six switches (IGBT's) to output three-phase AC current, which finally is filtered through a low-pass filter to reduce the high-frequent distortion [25] [26].

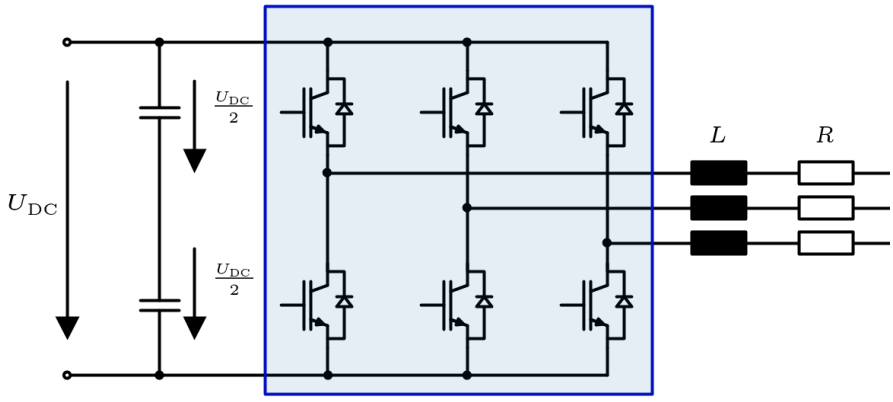


Figure 8: A three-phase two-level inverter. [27]

The switching signals controlling the switches are given by the PWM signals. When the PWM signal is high, the switch will be closed, allowing current to flow. Vice versa, the switch is open when the PWM signal is low. The PWM signal is composed from a high frequent triangle signal (carrier signal) combined with the desired AC voltage reference signal. This is shown in Figure 9. The blue reference signal is compared to the red carrier signal to determine

the switch state. When the reference signal is higher than the triangle pulse, the PWM signal is set to high, indicating that the switch should be closed.

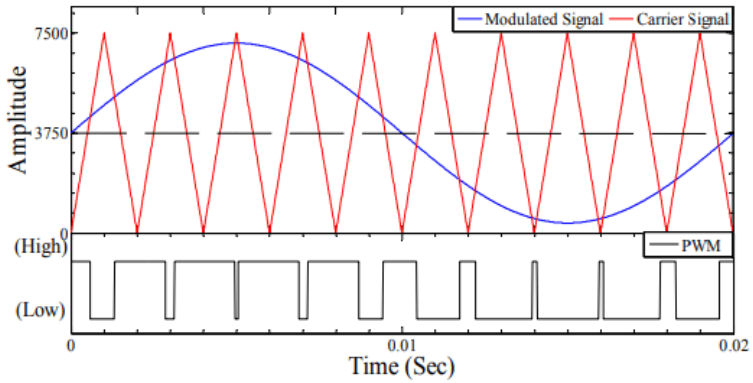


Figure 9: Basic pulse width modulation signal generation. When the sinusoidal reference signal is higher than the triangle pulse, the PWM signal will be set to high. [28].

The output signal is not very sinusoidal at this point, but filters are installed to improve this. Inductances and capacitances are used to create a low pass filter (normally LC or LCL filter) which will smoothen the signal. Depending on the filter, the voltage ripple can be so low that the voltage will be close to sinusoidal. Typical inverter output with filters is shown in Figure 10.

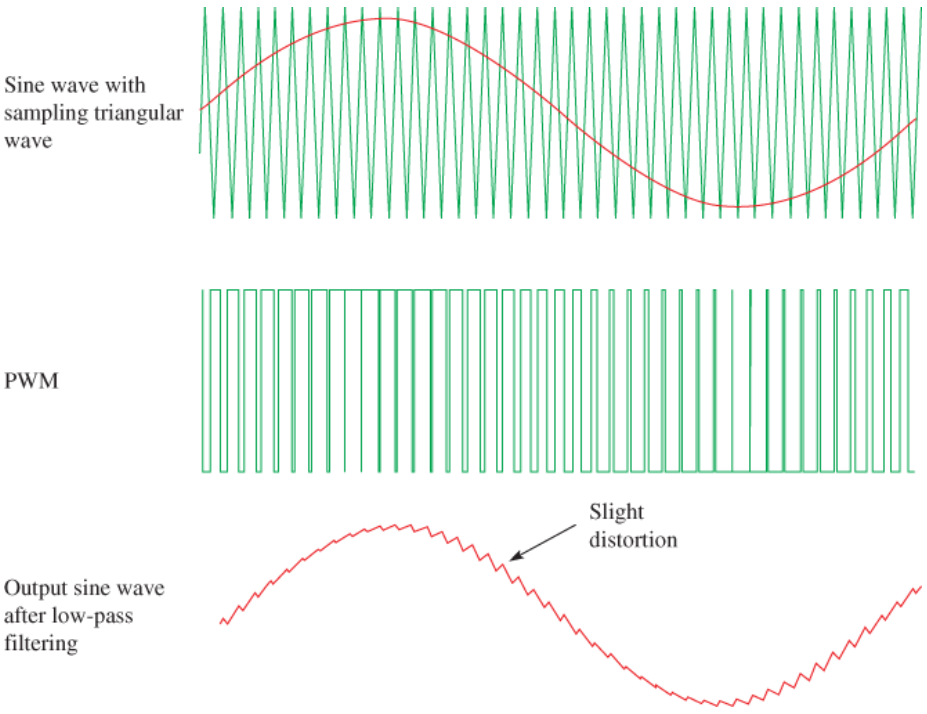


Figure 10: PWM and typical inverter output after filtering. [29]

2.6.2 Control systems

Inverters contain a control system responsible for controlling the current, voltage, active power and/or reactive power of the inverter. There are multiple options for inverter control. In general, one can classify inverters into three categories; grid-forming, grid-feeding and grid-supporting inverters [30]. The choice of the inverter control depends on the practical use.

Grid-forming inverters are rare as they do not automatically synchronize to the grid, but set the voltage and frequency references themselves. They simply output a given voltage at a given frequency, and act as independent sources. The typical control system of a Grid-forming inverter is shown in Figure 11.

Grid-feeding inverters synchronize to the grid automatically, and are ideal for connection to most grids. These inverters have given references for the active and reactive power (P* and Q*), and are suitable for constant power supply to the grid. For instance, a PV plant may be set to output 0.9 pu of nominal power as active power, and the remaining power as reactive power. Several Grid-feeding inverters may operate in parallel without problems as they all synchronize to the same phase and frequency. The typical control system for a Grid-feeding inverter is shown in Figure 12.

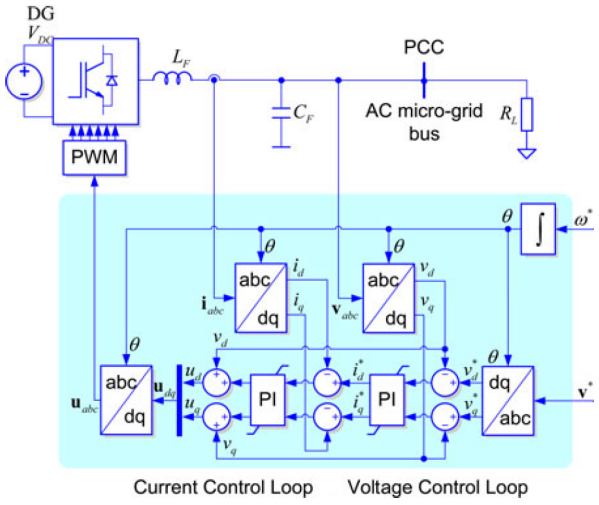


Figure 11: Typical control system of a Grid-forming inverter [30].

Grid-supporting inverters will also synchronize to the grid. These inverters have given references for the voltage and frequency (V* and f*), and support the grid in such a way that these references are met [30]. Grid-supporting inverters possess droop control which will adjust the active power generation based on the frequency, and the reactive power based on the voltage. The typical control system of a Grid-supporting inverter is shown in Figure 13. Such inverters are becoming increasingly more important as inverter interfaced generation is starting to play a larger role in the power system. Therefore, stricter requirements must be given to inverters, as they will have to be responsible for the grid stability [1] [3] [30].

When designing the control system of an inverter, a reference frame has to be chosen. A decomposition into a two-axis reference frame reduces the complexity of the control system and is preferable. Two main two-axis reference frames are used in today's inverter control systems; the stationary reference frame ($\alpha\beta$) and the synchronous reference frame (dq) [31] [25]. There are advantages and drawbacks of both methods, yet the dq reference frame tends to be the most common choice [30].

The $\alpha\beta$ reference frame represents a standard complex plane, with a real axis α and an imaginary axis β, orthogonal to each other. Sinusoidally rotating signals will consequently rotate counter-clockwise with respect to the axes [25]. The axes are shown in Figure 14.

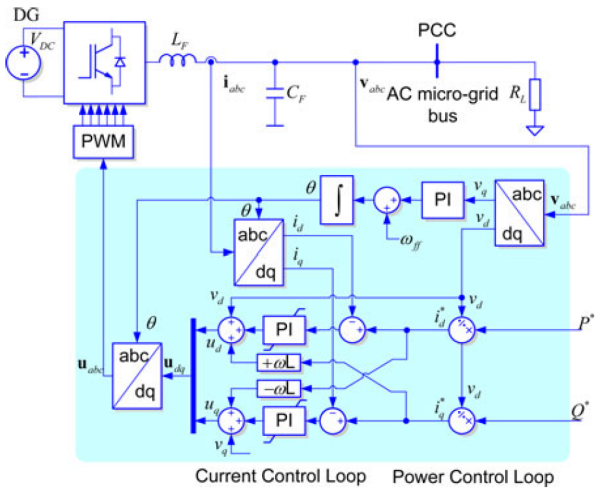


Figure 12: Typical control system of Grid-feeding inverters operating as current sources [30].

The dq reference frame also consists of two orthogonal axes d and q, but the axes themselves are rotating counter-clockwise with the angular velocity ω. Sinusoidal signals will rotate counter-clockwise together with the axes, resulting in constant d and q values (for steady-state operation) [25]. The axes are shown in Figure 14.

All of the control systems mentioned above (Figure 11, 12 and 13), have been implemented by using the synchronous reference frame dq. This reference frame is easier to work with, but contains weaknesses for unbalanced and distorted abc signals. Yet, there are methods for improving the dq reference frame performance during such conditions [33] [18]. For instance, it is possible to have two dedicated control systems for both positive and negative sequence components.

Power inverters connected to the power grid will have to synchronize themselves to the phase and frequency of the grid such that they operate in-phase with the grid. Two common methods for synchronization to the grid are called Phase Locked Loop (PLL) and frequency-locked-loop (FLL) [33] [18] [30] [34]. These synchronization methods are implemented in the control system together with the rest of the inverter control system.

In the dq reference frame, the Phase Locked Loop (PLL) is the standard implementation. The q-component of the voltage V_q is passed through a PI controller and added to the reference angular frequency of the grid ω^*, to obtain an estimate for the actual angular velocity ω'. This is further integrated

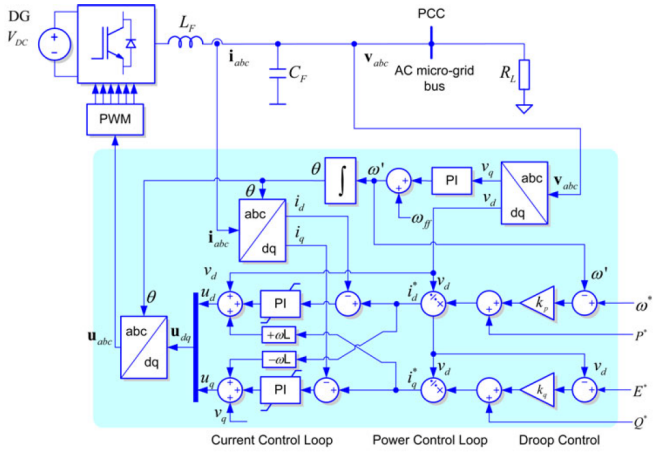


Figure 13: Typical control system of Grid-supporting inverters operating as current sources [30].

to obtain the phase angle estimate θ' [30], see Figure 15.

In contrast, in the $\alpha\beta$ reference frame, the frequency-locked-loop is the preferred implementation. An implementation that has proven to be effective is as shown in Figure 16. DSOGI stands for Dual Second-Order Generalized Integrator. As the figure shows, the implementation is more comprehensive than the PLL of the dq reference frame. The advantage though, is that this synchronization algorithm is less sensitive to phase-angle jumps [30].

2.6.2.1 Explanation of the Grid-feeding inverter control

The control system of a Grid-feeding power inverter (Figure 12) will be explained in greater detail here, based on [30].

The three-phase current $\boldsymbol{i}_{abc}$ and voltage $\boldsymbol{v}_{abc}$ out of the inverter are continuously being measured and sent to the control system as input parameters. Both of these signals are transformed from the abc reference frame to the dq reference frame via Park transformation. This transformation requires the phase angle θ, as the d and q axes are rotating counter-clockwise at $\omega = \frac{d}{dt}\theta$ radians per second. As the frequency of the grid may differ from 50 Hz, the mismatch has to be taken into consideration for proper grid synchronization. So the estimated angle θ from the PLL, θ', will be given as an input to the Park ($abc- > dq$) and Inverse Park ($dq- > abc$) transformation blocks.

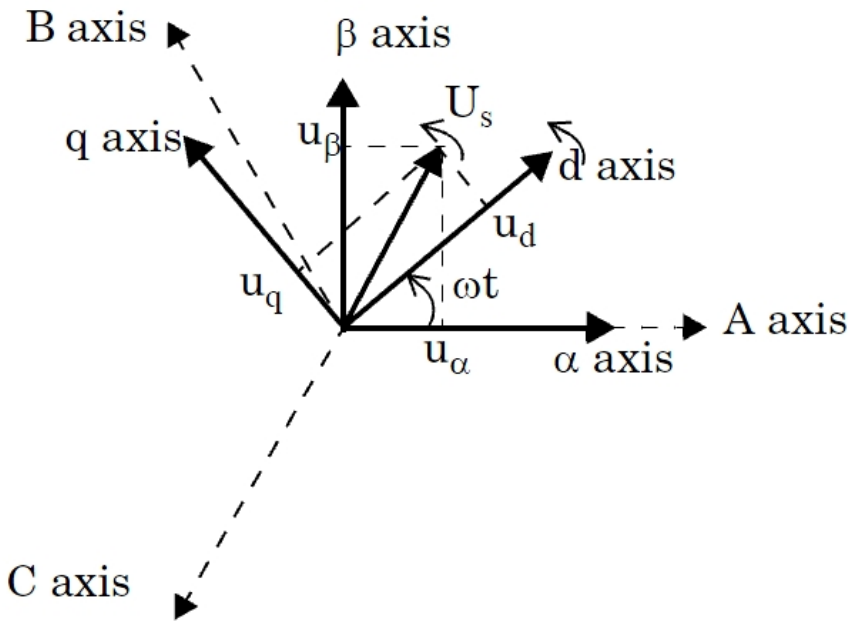


Figure 14: The abc-, $\alpha\beta$-, and dq-reference frames. The d and q axes rotate counter-clockwise with angular frequency ω, yet the other axes are fixed [32].

The references for the active and reactive power P^* and Q^*, will set the desired inverter output and are chosen by the user. Like in Figure 12, for a current controlled system, P^* and Q^* are divided by the output voltage v_d to further set the current references i_d^* and i_q^*. In this model, there are no current limits, but this may be implemented here. The current references are further compared to the measured current output i_d and i_q of the inverter to obtain the current error. Both errors enter a PI controller for controlling the inverter output with respect to the given errors. Lastly, the PI controller outputs are added to the measured voltages v_d and v_q to set the voltage reference signal $\boldsymbol{u}_{dq}$, which after a transformation back to $\boldsymbol{u}_{abc}$ enters the PWM block. The ωL blocks are optional, but improves the accuracy of the reference voltage by taking the voltage drop across the inductors (from the filter L_F) into account.

The pulse width modulation in the PWM block is straight forward. The voltage reference signal $\boldsymbol{u}_{abc}$ is compared to a high frequent triangle carrier signal to determine the switching signals entering the gate terminal of the inverter switches. The DC voltage source V_{DC} will feed the inverter, and with a properly defined low-pass filter (L_F and C_F) the output current will be close to sinusoidal and deliver the active power P^* and Q^* to the grid.

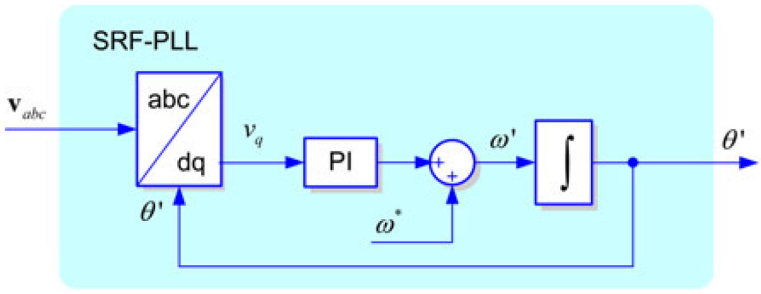


Figure 15: Synchronous Reference Frame (SRF) Phase Locked Loop (PLL) [30].

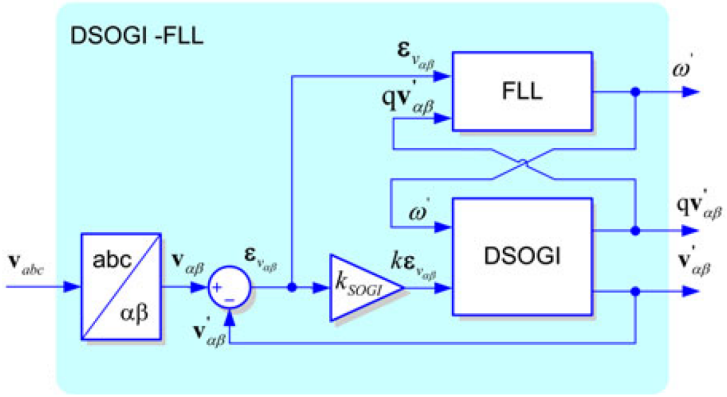


Figure 16: Dual Second-Order Generalized Integrator (DSOGI) Frequency Locked Loop (FLL) [30].

The constants of the PI controllers K_p and T_i (alternatively K_i) should be set according to control system theory to obtain a fast and stable regulation. Multiple methods for setting these constants are possible to use, yet it is also possible by trial and error [24].

2.6.3 Semiconductor switches

Semiconductor switches form the main building blocks of power-electronic converters [25]. Some examples of switches are IGBTs, MOSFETs and GTOs. IGBTs (Insulated Gate Bipolar Transistors) are used for a broad spectrum of applications in electric power systems, and has evolved significantly the last decades. The main advantages with IGBT switches are that they have a large bipolar current-carrying capability and that they are versatile [35]. The switch-

ing frequency of IGBTs however, is inferior to e.g the MOSFETs.

2.6.4 Filter design for inverters

Inverters will need filters at their terminal to smoothen the output signal. Based on [26], a procedure for parameter selection of an LCL-filter is proposed below. Adding of resistances in the capacitance branches are also suggested.

The first inductance L_1 will be set based on the DC voltage V_{DC}, the maximum allowed peak-to-peak current ripple $\Delta i_{max,p-p}$, and the PWM switching frequency f_{sw}. $\Delta i_{max,p-p}$ is suggested to be set to $0.1\sqrt{2}I_{base}$. L_1 should be chosen like in (29).

$$L_1 = \frac{V_{DC}}{8\Delta i_{max,p-p} f_{sw}} \tag{29}$$

The capacitance (to ground) will be set based on C_{base}, like in equation (30).

$$C = 0.05 C_{base} \tag{30}$$

The second inductance will be set based on the attenuation factor k_a, the first inductance L_1, the capacitance C, and the angular switching frequency $\omega_{sw} = 2\pi f_{sw}$. The ratio $x = \frac{L_2}{L_1}$ can be solved for in equation (31). The attenuation factor k_a is suggested to be 0.2. At last, L_2 can be found from equation (32).

$$k_a = \frac{1}{|1 + x(1 - L_1 C \omega_{sw}^2)|} \tag{31}$$

$$L_2 = x L_1 \tag{32}$$

To avoid resonance problems, the resonance frequency f_{res} should lie within a given interval, given by equation (33) and (34).

$$f_{res} = \frac{1}{2\pi}\sqrt{\frac{L_1 + L_2}{L_1 L_2 C}} \tag{33}$$

$$10 f_{base} \leq f_{res} \leq 0.5 f_{sw} \tag{34}$$

To suppress resonance frequency oscillations, a damping resistor should be installed in the capacitive branch as well. The damping resistor will be set based on the angular resonance frequency $\omega_{res} = 2\pi f_{res}$ and the capacitance C, according to equation (35).

$$R = \frac{1}{3\omega_{res}C} \tag{35}$$

2.7 Wind turbines

2.7.1 Wind turbine classification types

Wind turbines are categorized into five different classes listed below, describing their build and how they are connected to the grid [36]. Today, type 4 wind turbines are dominating the wind power market, surpassing the type 3 turbines [37] [10].

- Type 1 wind turbine: squirrel-cage induction generator.
- Type 2 wind turbine: wound rotor induction generator with a variable resistor to control rotor speed.
- Type 3 wind turbine: doubly-fed induction generator where the rotor is connected to the power grid via a full-scale back-to-back frequency converter, and the stator is directly connected.
- Type 4 wind turbine: synchronous or asynchronous generator, connected to the grid via a full-scale back-to-back frequency converter.
- Type 5 wind turbine: mechanical torque converter and a synchronous generator, directly connected to the grid.

2.7.2 Type 4 wind turbines

Type 4 wind turbines (T4WTs) connect to the grid via full-scale back-to-back frequency converters which are designed for the full rated power of the wind turbines. The general design is shown in Figure 17. The frequency converter consists of a rectifier (AC to DC), a DC link, and an inverter (DC to AC). This

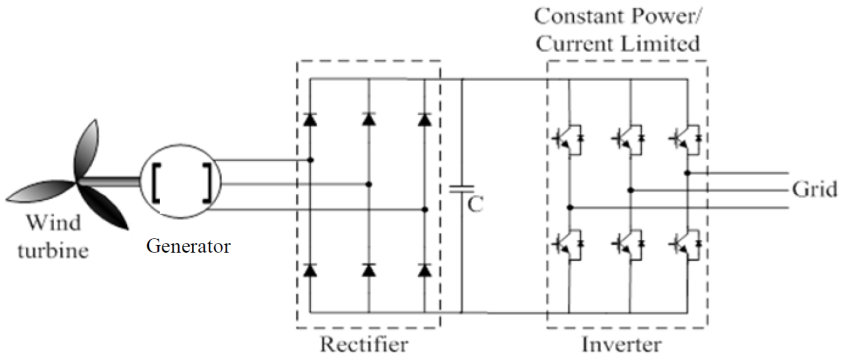


Figure 17: Type 4 Wind Turbine model [36].

allows turbine to rotate at variable speeds without the need of a gearbox [36].

Modelling of a complete wind turbine is comprehensive. However, for grid side studies T4WTs can be simplified to a DC-sourced inverter as the inverter determines the current fed to the grid. All of the complexity behind the DC-link is therefore avoided completely, and only a DC source and the inverter remain. This approach is supported by [6] [5] and [7], and is a reasonable modelling approach for protection studies.

2.8 Grid codes

The majority of this section, is copied directly from earlier project work [38].

National grid codes are technical specifications and requirements set for grid connected units to ensure safe operation of the power grid [1] [3] [39] [4]. Along with the renewable energy transition, the power system is going through rapid changes, and the grid codes have to adapt accordingly. Nowadays, the increasing share of distributed energy resources (DERs), including wind and solar power, plays a large role for determining further specified requirements. Fault Ride Through behaviour for DERs like inverter interfaced generation is becoming increasingly more important to consider, as DERs contribute to a larger share of the electricity generation. Therefore, it is necessary that DERs remain connected to the grid during faults to contribute to voltage and frequency stability along with conventional generation. Requirements can be related to active and reactive power control, but also positive and negative sequence control.

In Norway, Statnett approves units which are to be connected to transmission grids and higher voltage distribution grids [40]. The minimum technical requirements for connected units are specified in the national guideline FIKS,

provided by Statnett [41]. Currently, FIKS does not provide detailed requirements for wind turbines and other inverter interfaced generation units. Due to the lack of specified requirements, the inverter response during fault may vary between manufacturers [42], making it hard to predict.

A general protection requirement for the 420 kV grid in Norway set by FIKS is that short circuits on overhead lines should cause tripping of the line within 0.1 seconds after fault initiation [41].

3 Method

This chapter will describe the approach for the development of the PSCAD model and the reasoning for most of the model choices. The aim is to share the development process and most model parameters, such that the model can be reconstructed and improved for further work. In addition, by sharing the model parameters the thesis seeks to increase the utility of the simulation results as it will be easier to perform model comparisons.

First, the complete model overview with component description is presented.

Secondly, the development and justification of the model is presented.

Lastly, the main model assumptions are summarized.

3.1 Model overview and component description

The complete model, developed in PSCAD, is shown in Figure 18.

Each component used in the model is labelled in Figure 19 and 20, and their corresponding description is presented in Table 1, 2, 3 and 4. Further details of the subsystems such as the inverter control and the relay algorithms are presented in the next subsections.

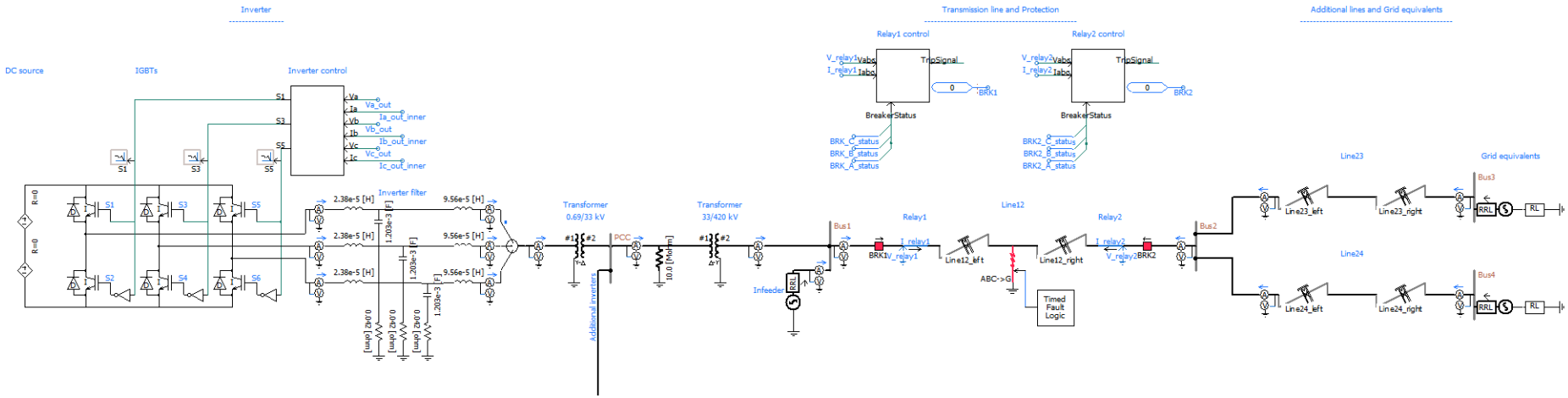


Figure 18: Complete model overview

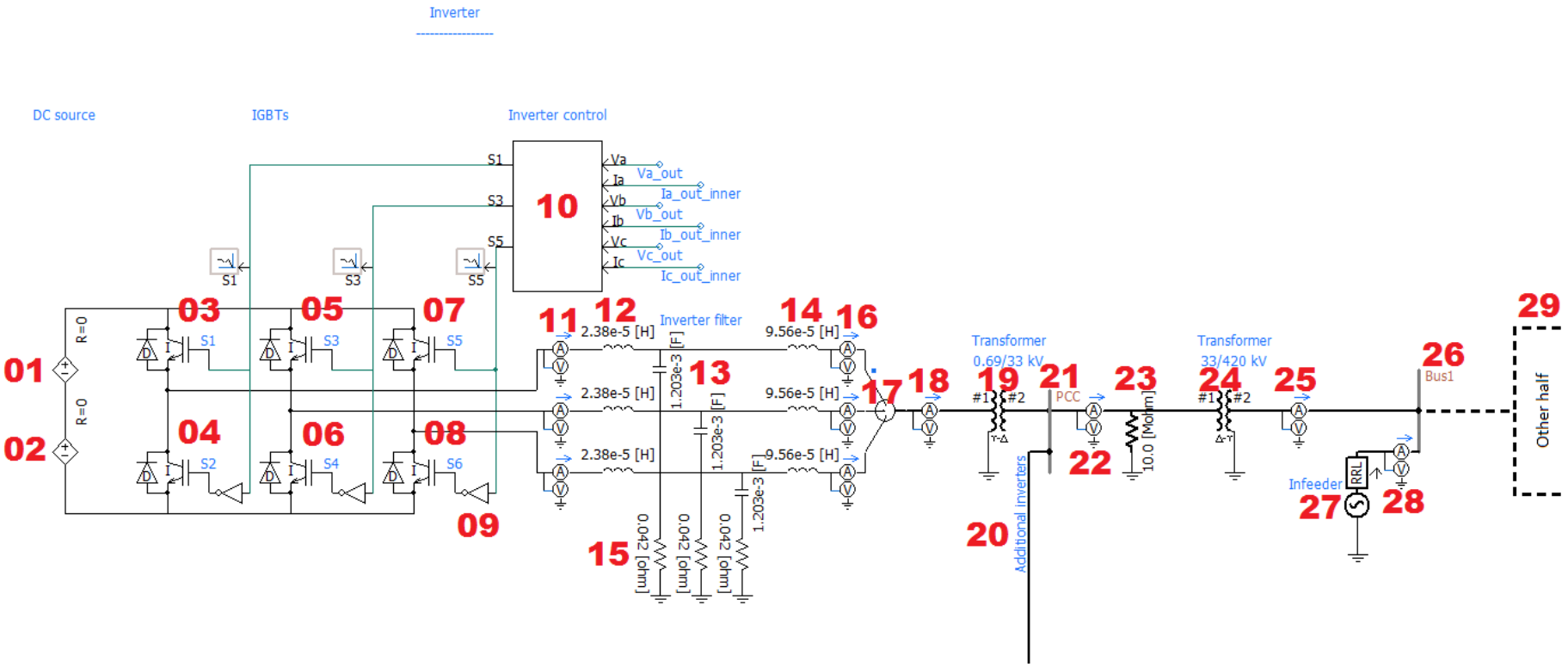


Figure 19: Left half of the model. The red IDs correspond to the component description in Table 1 and 2.

Table 1: Description of the model components, referred to Figure 19

ID	Component	Description
01, 02	Ideal DC voltage sources	The ideal voltage sources supplying the inverter. The DC source is split into two sources with half of DC link voltage to be able to access to the half potential node if desired. The total DC voltage was set to 1380 V.
03, 04, 05, 06, 07, 08	IGBT switches	The Insulated-Gate Bipolar Transistor switches of the inverter. The IGBT's are closed for gate signals equal to 1, and open for gate signals equal to 0. Backwards-facing diodes are installed in parallel to the IGBT's to deal with reverse voltage drops. No snubber circuit was enabled.
09	Logic inverter	A logic inverter (NOT) which converts 0's to 1's, and 1's to 0's.
10	The inverter control system	The inverter control system controlling the gate signals of the IGBT's such that the inverter feeds the desired current into the grid. The control system block imports the voltage and current measurements from the output terminals, and exports the gate signals for IGBT 1, 3 and 5. The gate signals for IGBT 2, 4 and 6 are obtained by inverting the signals.
11	Inner measurements	Measurements of variables with subscript _out_inner, e.g. Ia_out_inner. The inverter control system imports the currents measured here.
12	Left filter inductances	Inductances for the low-pass filter. The inductances were set to 23.80 μH.
13	Filter capacitances	Capacitances for the low-pass filter. The capacitances were set to 1.203 mF.
14	Right filter inductances	Inductances for the low-pass filter. The inductances were set to 95.60 μH.
15	Filter resistances	The resistances in series with the capacitances to reduce the amplitude of the resonance frequency of the LCL filter of 1050 Hz. The resistances were set to 42.00 mΩ.
16	Outer measurements	Measurements of variables with subscript _out, e.g. Va_out. The inverter control system imports the voltages measured here.
17	Three-phase merger	Three-phase view to single line view converter.
18	690V measurements	Measurements for variables with subscript _690V, e.g P_690V and Q_690V.

Table 2: Description of the model components, referred to Figure 19

ID	Component	Description
19	0.69/33 kV step-up transformer	A 4 MVA step-up star-delta transformer with a primary side voltage rating of 690 V, and a secondary side voltage rating of 33 kV. The leakage reactance is 0.1 pu, and copper losses are 0.01 pu. The star neutral point is grounded, and the secondary side leads the primary side by 30 degrees.
20	Additional inverters	If more than one single inverter should be connected to PCC, they are connected here.
21	PCC	The Point of Common Coupling Bus, where the inverters are connected.
22	33 kV measurements	Measurements for variables with subscript _33kV, e.g P_33kV and Q_33kV.
23	10 MΩ resistor	A three-phase resistor of 10 MΩ added only to avoid PSCAD warnings due to the floating node.
24	33/420 kV transformer	A 4 MVA step-up star-delta transformer with a primary side voltage rating of 33 kV, and a secondary side voltage rating of 420 kV. The leakage reactance is 0.1 pu, and copper losses are 0.01 pu. The star neutral point is grounded, and the primary side leads the secondary side by 30 degrees.
25	Inverter measurements at 420 kV	Measurements for variables with subscript _inverter.
26	Bus 1	Main bus number 1. The inverters are connected indirectly via transformers, and the infeeder is connected directly to this bus.
27	Infeeder	This voltage source is referred to as the Infeeder and is representing synchronous generation. Its positive sequence source impedance is referred to as $\|Z_{infeeder}\|$, with an angle of 86.06 degrees. The terminal voltage is set to 420 kV with a phase angle of 0 degrees. The zero sequence impedance is set identical to the positive sequence impedance. Otherwise, the parameters are similar to the sources described in Table 10
28	Infeeder measurements	Measurements for variables with subscript _infeeder.
29	Other half	The other half of the model, presented in Figure 20.

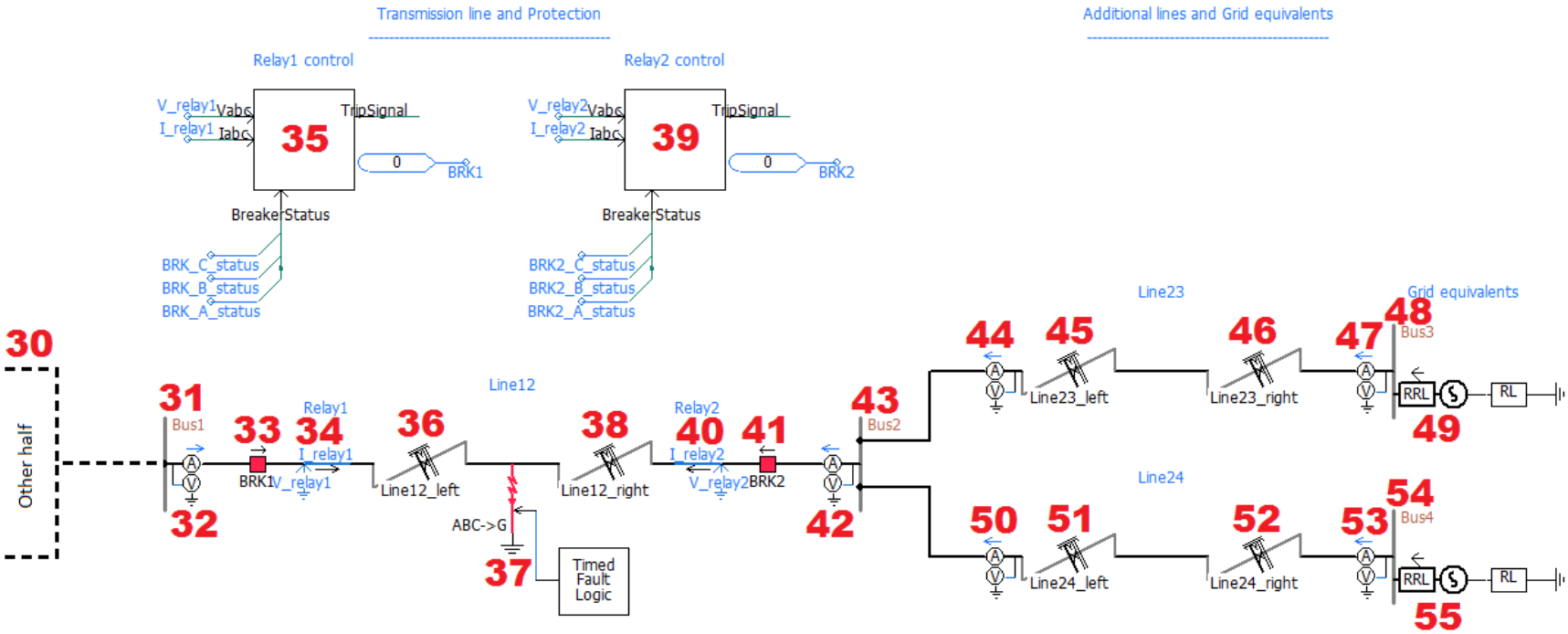


Figure 20: Right half of the model. The red IDs correspond to the component description in Table 3 and 4.

Table 3: Description of the model components, referred to Figure 20

ID	Component	Description
30	Other half	The other half of the model, presented in Figure 19.
31	Bus 1	Main bus number 1. The inverters are connected indirectly via transformers, and the infeeder is connected directly to this bus.
32	Line 12 Bus 1 measurements	Measurements for variables with subscript _line12_bus1 and _bus1, e.g I_line12_bus1 and V_bus1.
33	Breaker 1	Breaker for Relay 1. The breaker is set not to trip, regardless of the tripping signal from the relay.
34	Relay 1	Relay 1 is located here. The voltages and currents are sent to the relay control.
35	Relay 1 control	The relay control algorithm of Relay 1, responsible for detecting faulted conditions based on the voltage and current inputs.
36	Line 12 left	Left share of Line 12. The line is split in two to be able to access the fault location. The line parameters are presented later in this section.
37	Short circuit fault	The three-phase to ground short circuit is located here, with a variable fault resistance R_{fault}.
38	Line 12 right	Right share of Line 12. The line is split in two to be able to access the fault location. The line parameters are presented later in this section.
39	Relay 2 control	The relay control algorithm of Relay 2, responsible for detecting faulted conditions based on the voltage and current inputs.
40	Relay 2	Relay 2 is located here. The voltages and currents are sent to the relay control.
41	Breaker 2	Breaker for Relay 2. The breaker is set not to trip, regardless of the tripping signal from the relay.
42	Line 12 Bus 2 measurements	Measurements for variables with subscript _line12_bus2 and _bus2, e.g I_line12_bus2 and V_bus2.

Table 4: Description of the model components, referred to Figure 20

ID	Component	Description
43	Bus 2	Bus 2. This bus may be referred to as the grid side of Line 12.
44	Line 23 Bus 2 measurements	Measurements for variables with subscript _line23_bus2 and _bus2, e.g I_line23_bus2 and V_bus2.
45	Line 23 left	Left share of Line 23. The line is split in two to be able to access the fault location. The line parameters are presented later in this section.
46	Line 23 right	Right share of Line 23. The line is split in two to be able to access the fault location. The line parameters are presented later in this section.
47	Line 23 Bus 3 measurements	Measurements for variables with subscript _line23_bus3 and _bus3, e.g I_line23_bus3 and V_bus3.
48	Bus 3	Main bus number 3. Short circuit equivalent source 1 for the main grid is connected to this bus.
49	Short circuit grid equivalent 1	Short circuit equivalent source for the grid at the end of Line 23. The parameters are presented in Table 10.
50	Line 24 Bus 2 measurements	Measurements for variables with subscript _line24_bus2 and _bus2, e.g I_line24_bus2 and V_bus2.
51	Line 24 left	Left share of Line 24. The line is split in two to be able to access the fault location. The line parameters are presented later in this section.
52	Line 24 right	Right share of Line 24. The line is split in two to be able to access the fault location. The line parameters are presented later in this section.
53	Line 24 Bus 4 measurements	Measurements for variables with subscript _line24_bus4 and _bus4, e.g I_line24_bus4 and V_bus4.
54	Bus 4	Bus 4. Short circuit equivalent source 2 for the main grid is connected to this bus.
55	Short circuit grid equivalent 2	Short circuit equivalent source for the grid at the end of Line 24. The parameters are presented in Table 10.

3.1.1 Inverter control system

The inverter control system is shown in Figure 21. The components used in the control system are labelled in in Figure 22 and 23 and they are described in Table 5, 6 and 7.

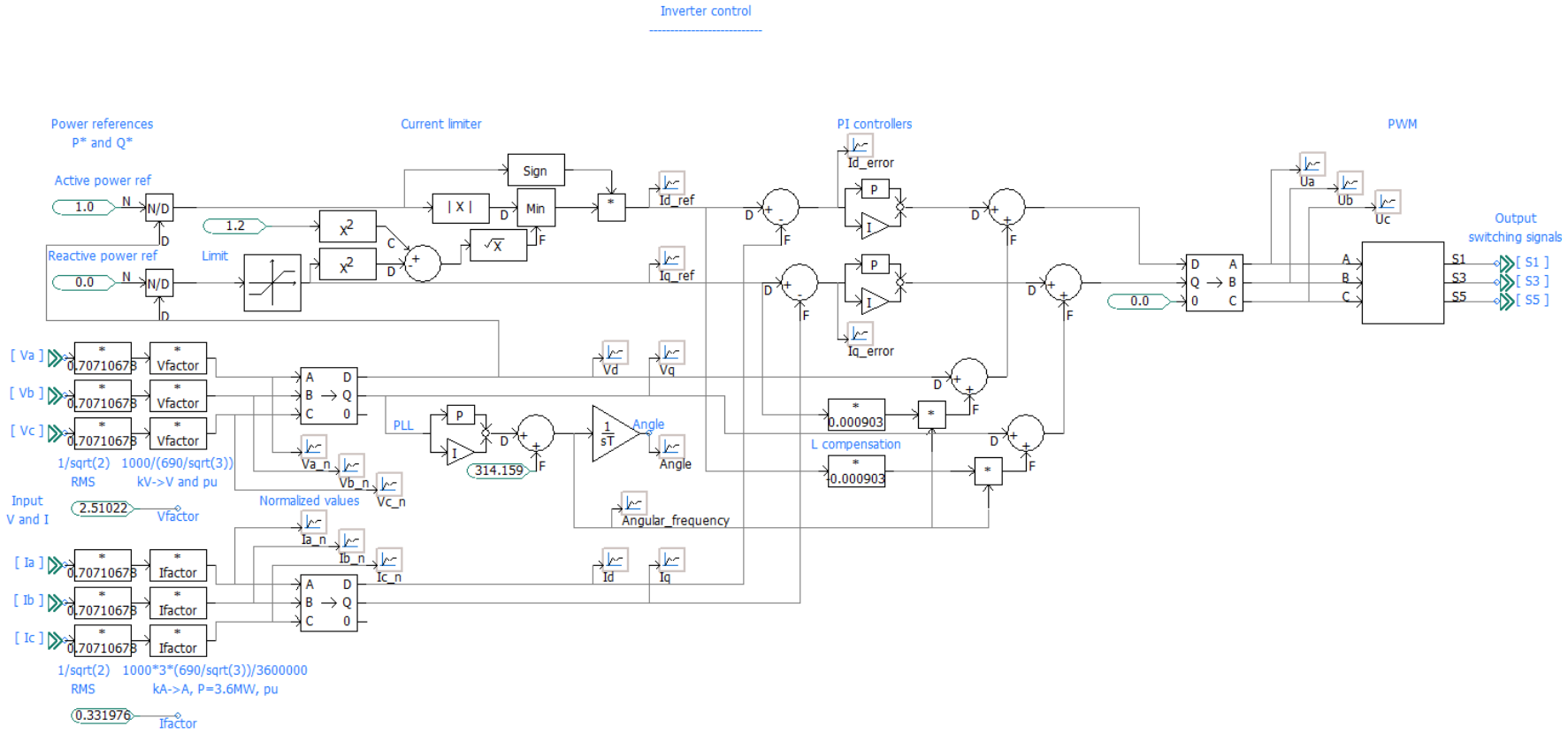


Figure 21: The inverter control system. Voltages and currents are imported, and switching signals are exported.

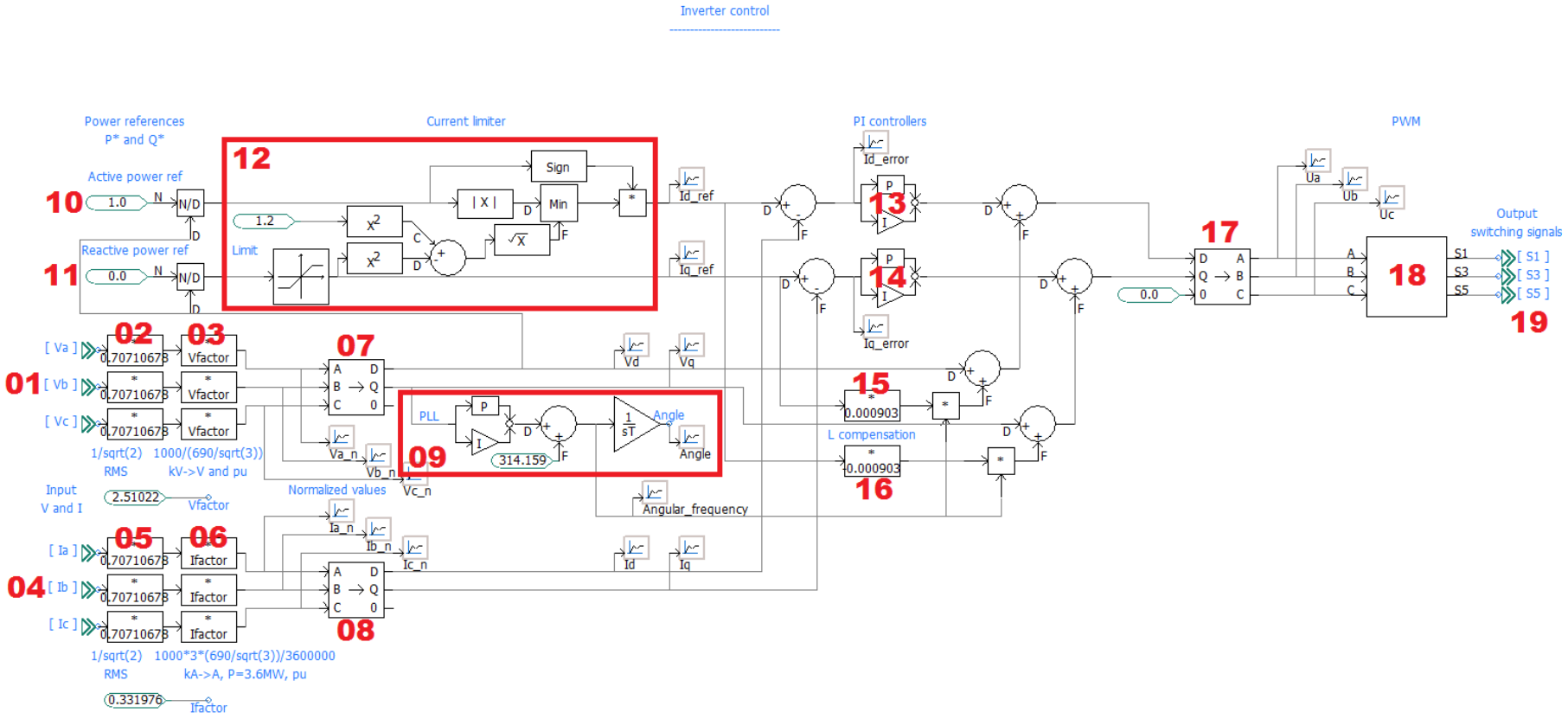


Figure 22: The inverter control system. The red IDs correspond to the component description in Table 5 and 6.

Table 5: Description of the components in the inverter control system, referred to Figure 22. The remaining components are described in Table 6.

ID	Component	Description
01	Voltage input	The imported three-phase phase voltages at the inverter terminals (outer measurements); Va_out, Vb_out and Vc_out.
02, 05	RMS Gain	The voltages and currents are scaled by $\frac{1}{\sqrt{2}}$, such that V_d and I_d have correct magnitude after the DQ0-transformation.
03	Voltage PU Gain Block	The voltages are converted to per unit by multiplying by $\frac{1}{V_{BASE,L-N}} = \frac{\sqrt{3}}{690V}$. Here, $V_{BASE,L-L} = 690V$, so $V_{BASE,L-N} = \frac{690}{\sqrt{3}}V$. Additionally, the voltages are multiplied by $1000V/kV$, as the voltage measurements are imported in kV. Now, V_d will be 1 for nominal voltages.
04	Current input	The imported three-phase currents at the inverter terminals (in front of the filter); Ia_out_inner, Ib_out_inner and Ic_out_inner.
06	Current PU Gain Block	The currents are converted to per unit by multiplying by $\frac{1}{I_{BASE,1-\phi}} = \frac{690V}{\sqrt{3}} \cdot \frac{3}{3600000VA}$, where $V_{BASE,L-N} = \frac{690V}{\sqrt{3}}$, and $S_{BASE,1-\phi} = \frac{3600000VA}{3}$. Additionally, the currents are multiplied by 1000 A/kA, as the current measurements are imported in kA. Now, I_d will be 1 for nominal currents.
07, 08, 17	DQ0 Transformation Block	Park transformation block converting the *abc* reference frame to the *dq*0 reference frame, or vice versa. This block is premade in PSCAD. The block imports the angle estimate "Angle" from the PLL, which is required for performing the transformation.
09	PLL	The Phase Locked Loop responsible for grid synchronization. It consists of a PI controller taking V_q as input, addition of the base angular frequency $2\pi 50\frac{rad}{s}$, and a pure integrator, generating the estimate for the "Angle". K_P and T_I of the PI controller are set to 10^{-8} and 10^{8}, respectively, for reasons discussed in the upcoming "Model development and justification" section.

Table 6: Description of the components in the inverter control system, referred to Figure 22. The remaining components are described in Table 5.

ID	Component	Description
10	Active Power Reference	The user-set active power reference of the Grid-feeding inverter, in per unit.
11	Reactive Power Reference	The user-set reactive power reference of the Grid-feeding inverter, in per unit.
12	Current limiter	The current limiter of the inverter, limiting $i_{q,ref}$ to 1.2 pu and the length of the vector sum of $i_{d,ref}$ and $i_{q,ref}$ to 1.2 pu. The reactive power has the highest priority to help increase the voltage during faults.
13, 14	Current controllers	The PI controllers for regulating the errors of the currents i_d and i_q. The proportional gain K_P is set to 1, and the integral time constant T_I is set to 0.02 s. The upper and lower output limits are set to 1 and -1, respectively.
15, 16	Inductance voltage drop compensation blocks	These blocks multiply the currents with the combined inductance impedance $\omega(L_1 + L_2) = \omega \cdot 0.9030 \cdot 10^{-3}$ pu and generate the voltage drops across the filter inductances. Note that the bottom block has negative polarity.
18	PWM block	This block generates the Pulse Width Modulation signals for the inverter switches, and is described in Figure 23 and Table 7.
19	Switching signals	The exported switching signals for each phase, controlling the IGBTs.

Table 7: Description of the Pulse Width Modulation in the inverter control system, referred to Figure 23.

ID	Component	Description
01	U references	The imported voltage references for each phase.
02	Modulation factor	Optional modulation factor if desired. Here only 1.
03	Carrier signal	The 8000 Hz triangle-shaped carrier signal with an amplitude of 1, used for the PWM.
04, 05, 06	Comparators	Comparators for generating the PWM signals (1 or 0) by determining which of the two input signals is the highest.
07	Switching signals	The generated switching signals, exported to the IGBTs.

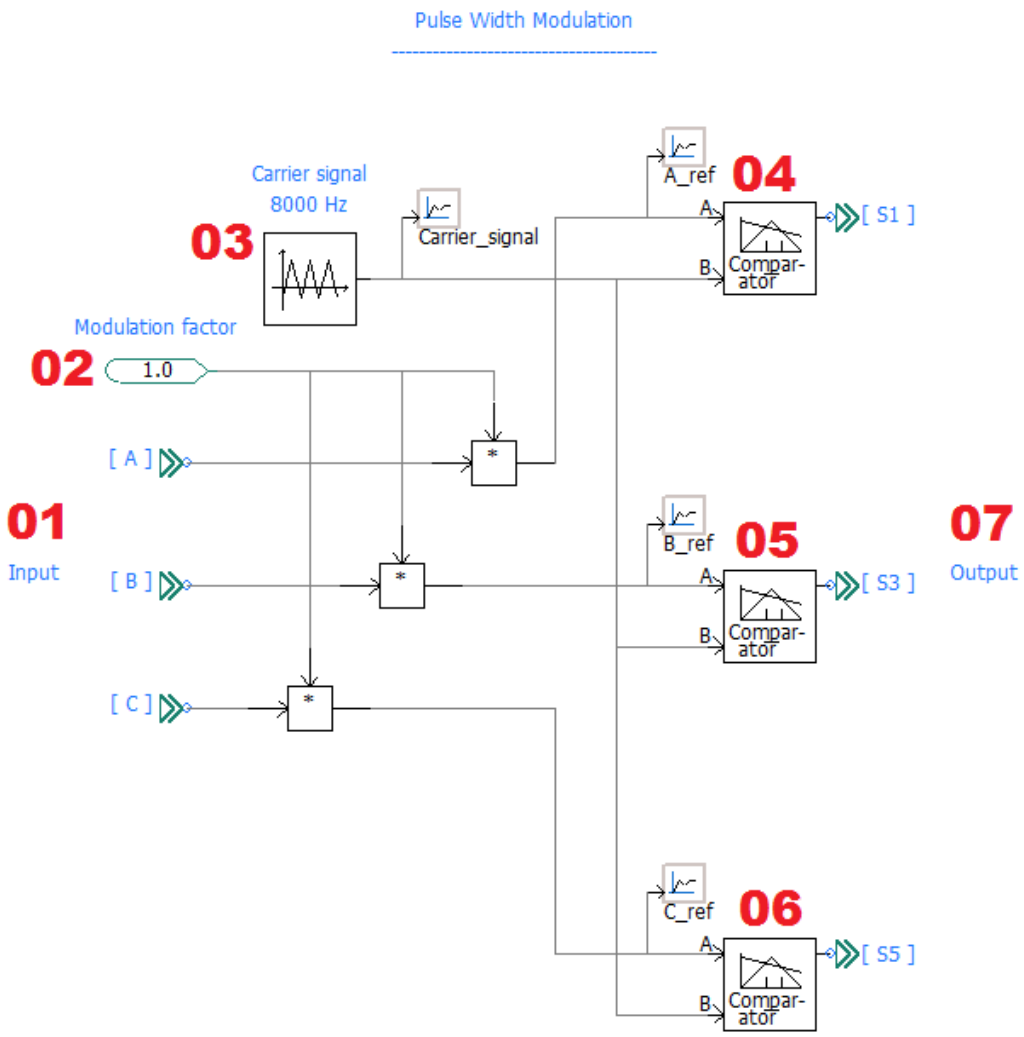


Figure 23: The implemented Pulse Width Modulation in the inverter control system. The red IDs correspond to the component description in Table 7.

3.1.2 Relay algorithm for distance protection

The relay algorithm used for the distance protection is shown in Figure 24. The components used in the relay algorithm are labelled in Figure 25 and are described in Table 8.

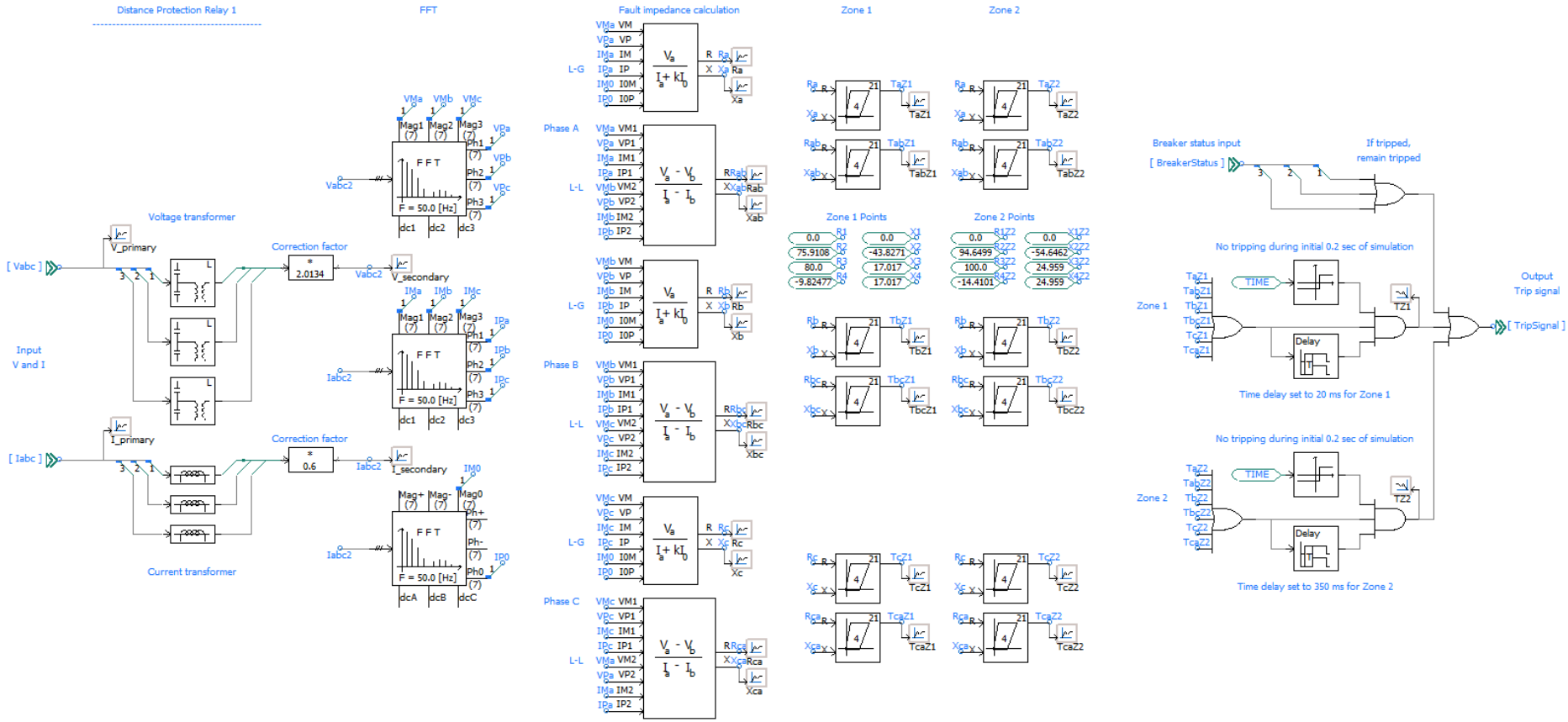


Figure 24: The relay control algorithm for the distance protection.

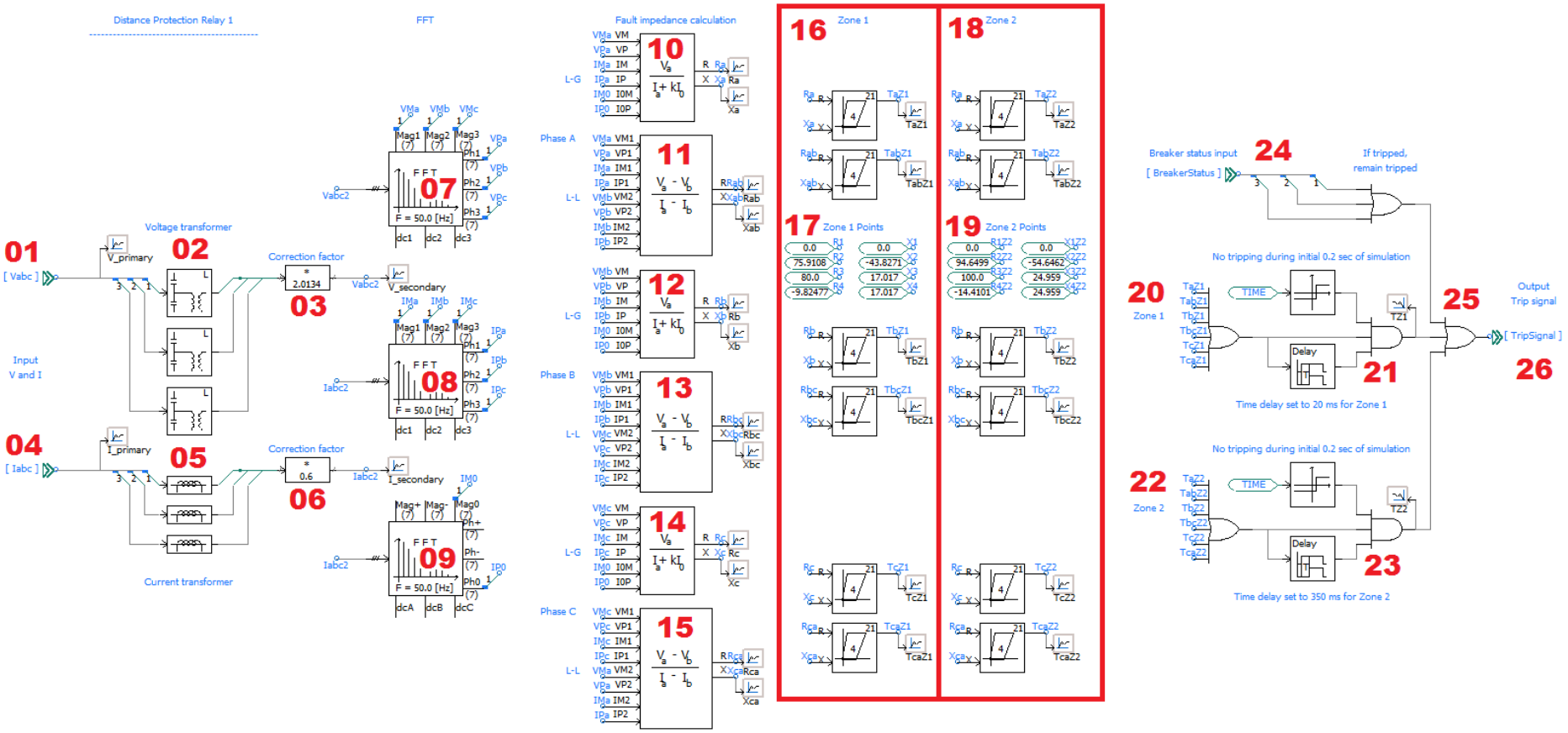


Figure 25: The relay control algorithm for the distance protection. The red IDs correspond to the component description in Table ??.

Table 8: Description of the relay control algorithm for the distance protection, referred to Figure 25.

ID	Component	Description
01	Voltage inputs	The imported phase voltages.
02	VT	The voltage transformer, emulating the influence of non-ideal measurements. The parameters are PSCAD standard parameters, but with capacitor 1 changed to 2841 pF. Note that the input is in kV, and the output is in V.
03	Voltage correction factor	A correction factor of 2.013 $\frac{kV}{V}$ to scale the voltage signal back to its original value.
04	Current inputs	The imported currents.
05	CT	The current transformer, emulating the influence of non-ideal measurements. The parameters are PSCAD standard parameters, but with the primary and secondary turns changed to 1 and 600, respectively. Note that the input is in kA, and the output is in A.
06	Current correction factor	A correction factor of 0.6 $\frac{kA}{A}$ to scale the current signal back to the same value before entering the CT.
07, 08, 09	FFT analysis	Fast Fourier Transform analysis blocks extracting the desired voltage and current magnitudes and phases for the fault impedance measurements.
10, 12, 14	L-G relays	The Line to Ground systems for each of the three phases, giving Z_a, Z_b and Z_c.
11, 13, 15	L-L relays	The Line to Line systems for each of the three phases, giving Z_{ab}, Z_{bc} and Z_{ca}.
16	Zone 1 detection	Separate zone 1 detection for each of the fault loops.
17	Zone 1 border	The coordinates for the four points, determining the border of zone 1.
18	Zone 2 detection	Separate zone 2 detection for each of the fault loops.
19	Zone 2 border	The coordinates for the four points, determining the border of zone 2.
20	Zone 1 OR	If any of the fault loops detect a fault, it is considered as a zone 1 fault.
21	Zone 1 delay	A zone 1 fault has to be detected consecutively for 20 ms for the fault to trigger tripping.
22	Zone 2 OR	If any of the fault loops detect a fault, it is considered as a zone 2 fault.
23	Zone 2 delay	A zone 2 fault has to be detected consecutively for 350 ms for the fault to trigger tripping.
24	Remain tripped	If the breaker at any point is tripped, the breaker will remain tripped.
25	General OR	If a zone 1 or zone 2 tripping signal is received, or if already tripped, then trip.
26	Trip signal	The trip signal exported to the breaker. The breaker is set to not trip regardless of the tripping signal.

3.1.3 Grid model

The parameters used for the transmission lines and the short circuit grid equivalents are presented here. Note that the base values used to achieve the per unit values of the transmission line parameters are different than the system base values.

Line 12	R [pu/m]	X [pu/m]	B [pu/m]
Positive seq.	1.294E-07	1.925E-06	6.032E-07
Zero seq.	1.160E-06	4.330E-06	4.460E-07
Line 23			
Positive seq.	1.298E-07	1.929E-06	5.967E-07
Zero seq.	1.470E-06	4.830E-06	3.900E-07
Line 24			
Positive seq.	1.298E-07	1.929E-06	5.967E-07
Zero seq.	1.470E-06	4.830E-06	3.900E-07

Table 9: Line parameters for Line 12, Line 23 and Line 24. $S_{base} = 1$ GVA and $V_{base} = 400$ kV are used for the per unit conversion. R, X and B correspond to the resistance, the inductive reactance and the capacitive susceptance, respectively. The line lengths are not provided due to sharing restrictions.

Short circuit equivalent 1	Bus 3
Source control	Fixed
Voltage input time constant	0.06 s
Terminal voltage	420 kV
Terminal phase angle	0°
Frequency	50 Hz
Positive seq. impedance magnitude	25.76 Ω
Positive seq. impedance angle	86.06°
Zero seq. impedance magnitude	20.82 Ω
Zero seq. impedance angle	82.79°
Short circuit equivalent 2	Bus 4
Source control	Fixed
Voltage input time constant	0.06 s
Terminal voltage	420 kV
Terminal phase angle	0°
Frequency	50 Hz
Positive seq. impedance magnitude	35.20 Ω
Positive seq. impedance angle	85.52°
Zero seq. impedance magnitude	15.85 Ω
Zero seq. impedance angle	11.62°

Table 10: Parameters used for the short circuit grid equivalents connected to Bus 3 and Bus 4.

3.2 Model development and justification

Most model choices are justified in this section.

Initially, it was decided to develop an inverter equivalent for the type 4 wind turbines at Fosen. This approach was chosen as the inverter is the grid-connected component effectively determining the grid feeding, and to avoid most of the complexity of the wind turbine. For grid-side studies such as protection studies, it was considered acceptable to go for the inverter model. [5], [6] and [7] have also developed inverter models as a representation of wind generation. Since the majority of the wind turbines at Fosen have a rating of 3.6 MVA, it was decided to develop a 3.6 MVA inverter.

The inverter rated voltage was chosen to be 690 V [43]. Based on grid data received from Statnett, 33 kV was chosen for the Point of Common Coupling voltage, and 420 kV was chosen for the high voltage transmission grid. All the voltages are RMS line-to-line voltages. The grid frequency was set to 50 Hz as this is the base frequency of the Norwegian grid.

It was decided to go for a Grid-feeding inverter model. It will synchronize

to the grid in contrast to a Grid-forming inverter, and is less comprehensive to develop than a Grid-supporting inverter [30].

The Grid-feeding inverter model has been developed based on [30]. The synchronously rotating frame dq0, has been chosen for the control system as this reference frame is broadly used, and is suggested by [30]. The control system has been modified to per unit for convenience.

Based on experience from model testing, it was observed that the Phase Locked Loop had major difficulties during severe voltage drops with heavily distorted voltages, causing the PLL to malfunction. As most of the simulations would have heavily distorted voltages on the inverter terminal, it was decided to manipulate the PLL implementation. The PI controller of the PLL was purposefully set to regulate extremely slowly ($K_P = 10^{-8}$ and $T_I = 10^8$ s), effectively making the estimated angular frequency and the phase angle of the PLL constant (The angle is increasing linearly). Thus, the phase angle had to be adjusted manually, to ensure proper grid synchronization. The initial output of the integrator (the constant phase angle) was chosen such that V_q was regulated to zero. This had to be ensured for every simulation, as model changes influenced which phase angle had to be chosen. A major drawback with this implementation of the PLL, is potential phase jumps during the simulation. In this case the, the PLL will lose grid synchronization, effectively changing the power factor of the inverter.

As [30] did not include a current limiter for the inverter, it had to be figured out how to implement such a current limiter. The current limiter has been developed without the use of any references, yet it was supported by professors and has been verified to work properly in the "Verification of the model" chapter. It was decided to limit the inverter current to 1.2 pu, based on [36], [42] and [44]. The reference for $|I_q|$ is limited to 1.2 pu. Then, the reference for $|I_d|$ is limited such that the length of the vector sum of $|I_q|$ and $|I_d|$ never exceeds 1.2 pu. Basic orthogonal vector summation theory was used to obtain this. As $|I_q|$ sets the upper limit for $|I_d|$, $|I_q|$ will have the highest priority. This choice was made as reactive power is preferred during voltage drops to help boost the grid voltage [1].

The PI controllers controlling the errors of I_d and I_q have been tuned based on experience from testing. The reasoning for the tuning is presented in the "Verification of the model" chapter. The proportional gain K_P was set to 1, and the integral time constant T_I was set to 0.02 s.

The suggested inductance voltage drop compensation in [30] was developed for inverters with LC filters. As this model uses an LCL filter, it was decided to use the sum of the inductances L_1 and L_2 for the inductance compensation block in the control system, even though this may not be accurate.

The carrier signal frequency for the Pulse Width Modulation was set to 8 kHz. Frequencies higher than 8 kHz were observed to cause carrier signal inaccuracies due to the restriction of the simulation solution time step of 5 μs. Thus, 8 kHz was chosen. This frequency should probably have been verified to be suitable for the IGBTs, however this was not done.

The DC voltage source was split into two sources, to be able to access the half potential node if desired. Each of the DC sources was set to 690 V, effectively generating a voltage of 1380 V. Theoretically, the DC voltage should be at least $\sqrt{2}V_{L-L,base} = \sqrt{2} \cdot 690V = 975.8V$, yet to be able to deliver the desired power output, it is common to use DC voltages higher than this value. 1380 V was chosen based on experience from testing.

The inverter model was chosen to be ideal, with no resistances added to the DC voltage sources, nor the terminals. This choice was made to keep the model simpler.

The inverter filter has been designed based on [26], with $\Delta i_{max,p-p}$ set to $0.2\sqrt{2}I_{base}$. The proposed filter was an LCL filter, with damping resistors added to the capacitive branches to reduce oscillations close to the resonance frequency.

The 0.69/33 kV step-up transformer was chosen to be a standard PSCAD star-delta transformer of 4 MVA with positive sequence reactance of 0.1 pu. The rating of 4 MVA was chosen to add a 10% security margin to the inverter rating of 3.6 MVA. Copper losses of 0.01 pu were chosen based on recommendations from Statnett.

The 33/420 kV transformer was chosen to be a standard PSCAD delta-star transformer of 200 MVA, with positive sequence reactance of 0.1 pu. The choices of 200 MVA as the rating for this transformer and copper losses of 0.01 pu were based on data provided by Statnett.

All the transmission lines have been modelled with the Bergeron model. The line lengths and the distributed line data for the positive and zero sequence parameters have been provided by Statnett to make the grid relatively comparable to the 420 kV grid at Fosen. The line lengths have not been provided in this thesis due to sharing restrictions, however, it can be stated that they are shorter than 100 km each.

The data for the short circuit grid equivalent sources located at Bus 3 and Bus 4, have been provided by Statnett to make the grid comparable to the grid at Fosen, with proper grid stiffness. The sources have a terminal voltage of 420 kV with a phase angle of 0 degrees. The positive and zero sequence impedances of the sources have been set based on the data provided by Statnett.

To be able to compare the influence of inverter interfaced generation with

synchronous generation, a source was developed to assemble synchronous generation. This source is referred to as the Infeeder. The source was set to have a terminal voltage of 420 kV with a phase angle of zero degrees, similar to the grid equivalents on Bus 3 and 4. In other words, angle shifts due to loading of transmission lines were not taken into consideration. However, as the transmission lines were very lightly loaded, this may have been reasonable. The Infeeder source impedance angle was set to 86.06 degrees, similar to the Grid equivalent at Bus 3. The infeeder source impedance magnitude has been set to different values throughout the simulations depending on the scenario. During Simulation set 3, the infeeder resembles synchronous generation. The infeeder source impedance magnitude has been chosen in such a way that the short circuit current of the infeeder is equivalent to a number of synchronous generators of the same rating as the inverter. A theoretical 3.6 MVA 690V synchronous generator will have a rated current of $\frac{3.6MVA}{3}\frac{\sqrt{3}}{690V} = 3012A$. Based on the assumption that synchronous generators have a short circuit current of approximately 6 pu [45], the short circuit current of the generator would be $6 \cdot 3012A = 18.07kA$. As the infeeder has a rated voltage of 420 kV in the model, the current will be a factor of $\frac{690V}{420kV} = 1.643 \cdot 10^{-3}$ smaller after ideal transformation from 690 V to 420 kV. Thus, the 3.6 MVA 690 V synchronous generator short circuit current would be $18.07kA \cdot 1.643 \cdot 10^{-3} = 29.69A$. So if the infeeder short circuit current is 29.69 A, it will resemble a 3.6 MVA 690V synchronous generator. Based on PSCAD testing, it was observed that the infeeder source impedance magnitude had to be set to 11560 Ω to generate a short circuit current (for a L-L-L-G fault with $R_{fault} = 0$) of 29.69 A (stationary value). If the infeeder had to represent several synchronous generators, the impedance was changed accordingly. This approximation of synchronous generation contains major simplifications, and is not expected to be an accurate way of modelling the short circuit current contribution of a synchronous generator.

The only short circuit type used for the protection studies in this thesis is a symmetrical three-phase to ground short circuit (L-L-L-G). The reason for this is due to the limitations of the inverter model. The inverter model was observed to not able to handle asymmetrical faults, as the control system was not developed for this. Thus, it was decided to look solely into L-L-L-G faults.

The distance protection model has been developed based on the PSCADs own "Cookbook for protection studies" [11]. The manual provides a step-by-step guide on how to develop the relay algorithm for basic distance protection. It has been decided to go for the classic distance protection algorithm without any advanced added features, to keep the model simple and general.

Voltage and current transformers have been added to the relays to replicate non-ideal measurements. Standard PSCAD VTs and CTs were used, with minor changes. [19] was used to ensure that the primary and secondary side voltages and currents of the VT and CT were properly chosen. Correction factors were

introduced after the VTs and CTs to scale the voltages and currents back to the original value for correct interpretation of the magnitudes.

The phase to ground relays require a value for the zero sequence compensation factor. The zero sequence compensation factor has been set based on the positive and zero sequence impedances of line 12, provided by Statnett.

It was decided to use a quadrilateral zone border for zone 1 and zone 2, as this is common for numerical distance protection. The four impedance points defining the the corners of the zone 1 borders of Relay 1, have been set based on the following reasoning:

- Point 1 [0 + j0 Ω] The origin. Forward fault coverage only.
- Point 2 [75.91 -j43.83 Ω] 30° from the real axis.
- Point 3 [80 + j17.02 Ω] 17.02 Ω is 85% of the reactance of line 12, setting the zone 1 reach to 85%. 80 Ω for the resistive reach was chosen as it was relatively similar to [5]. The slope of the zone border from point 2 to point 3 is identical to the X/R ratio of Line 12.
- Point 4 [-9.825 + j17.02] 30° from the imaginary axis.

The four impedance points defining the the corners of the zone 2 borders of Relay 1, have been set based on the following reasoning:

- Point 1 [0 + j0 Ω] The origin. Forward fault coverage only.
- Point 2 [94.65 -j54.65 Ω] 30° from the real axis.
- Point 3 [100 + j24.96 Ω] 24.96 Ω is 100% of the reactance of line 12 plus 20% of the reactance of line 23. 100 Ω for the resistive reach was chosen as it was relatively similar to [5]. The slope of the zone border from point 2 to point 3 is identical to the X/R ratio of Line 12.
- Point 4 [-14.41 + j24.96] 30° from the imaginary axis.

The zone 1 time delay was chosen to be 20 ms, based on [19]. The zone 2 time delay was chosen to be 350 ms, also based on [19].

The breakers in the model were set to never trip, regardless of the tripping signals from the relays. This was done to be able to study the whole faulted period.

The simulation solution time step in PSCAD was set to 5 μs, as this was a compromise of accuracy and simulation time. This time step was able to handle the 8 kHz carrier signal of the PWM in the inverter.

3.3 Summarized model assumptions

The main model assumptions are listed here.

- An ideal DC sourced Grid-feeding inverter is comparable to a type 4 wind turbine.
- The DC source feeding the inverter is ideal and constantly at rated voltage.
- The inverter current is limited to 1.2 pu.
- The short circuit current contribution of synchronous generation can be simplified to a voltage source.
- The short circuit current contribution of a synchronous generator is 6 pu.
- The short circuit is a symmetrical three-phase to ground fault.
- The short circuit impedance (resistance) is purely resistive.
- The fault location is on the center of the line.
- The distance protection algorithm implemented in this model is representative for classic distance protection.
- There is no phase angle shift from one side of the model to the other. The phase angle of the connected sources are set identical as if they were connected to the same node.

4 Verification of the model

To ensure that the model works as intended, this chapter is provided to verify the main parts of the model. The inverter model, which has been developed from scratch, needs verification before it is used for obtaining results. Additionally, the distance protection model should be verified as well, even though PSCAD's own recipe for developing distance protection has been used as a guideline.

This chapter contains simulation results from the different parts of the model that needs verification, in addition to a minor ongoing discussion. In this chapter, the infeeder source impedance is set low to ensure sinusoidal voltage on bus 1 during the voltage drop when the fault is initiated on Line 12. The current contribution from bus 1 will also be similar in magnitude as from bus 2, which is optimal for accurate distance protection operation. The reason for the choice of ideal conditions during the verification of the model is to verify that the model operates as intended, at least under such conditions.

4.1 Verification of the inverter model

The Grid-feeding inverter model has been tested through numerous simulations. The most critical data has been collected to visualize the different parts of the inverter control system. The results are presented below. More data is displayed for the first simulation, called Verification 1, including simulation results for most of the inverter control variables.

4.1.1 Verification 1 - Detailed

This simulation provides the most details about the variables of the inverter and its control system. The parameters were set like shown in Table 11. The results from the simulation are displayed in Figure 26 to 29.

Table 11: Standard system parameters used for Verification 1.

Parameter	Value	Description
P*	1 pu	Active power reference set to deliver 1 pu active power.
Q*	0 pu	Reactive power reference set to deliver 0 pu reactive power.
I_{lim}	1.2 pu	Current output limit of the inverter set to 1.2 pu.
K_P	1	Proportional gain of PI controllers set to 1.
T_I	0.02 s	Integral time constant of PI controllers set to 0.02 s.
$\|Z_{infeeder}\|$	25.76 Ω	The magnitude of the infeeder source impedance set to 25.76 Ω, identical to the positive sequence impedance of the grid equivalent on bus 3. This is to make sure the grid is strong enough to keep a sinusoidal waveform during the fault. This impedance will be significantly higher during the main simulations.
R_{fault}	0.01 Ω	Fault resistance of the L-L-L-G fault on line 12 set to 0.01 Ω.
x_{fault}	50%	Fault location on line 12 set to 50% of the line length, from bus 1.
t_{fault}	0.5 s	Fault initiation time set to 0.5 seconds. The fault duration is set to last for the rest of the simulation.
Tripping	No	Protection relays are set to not trip their breakers, regardless of fault detection.

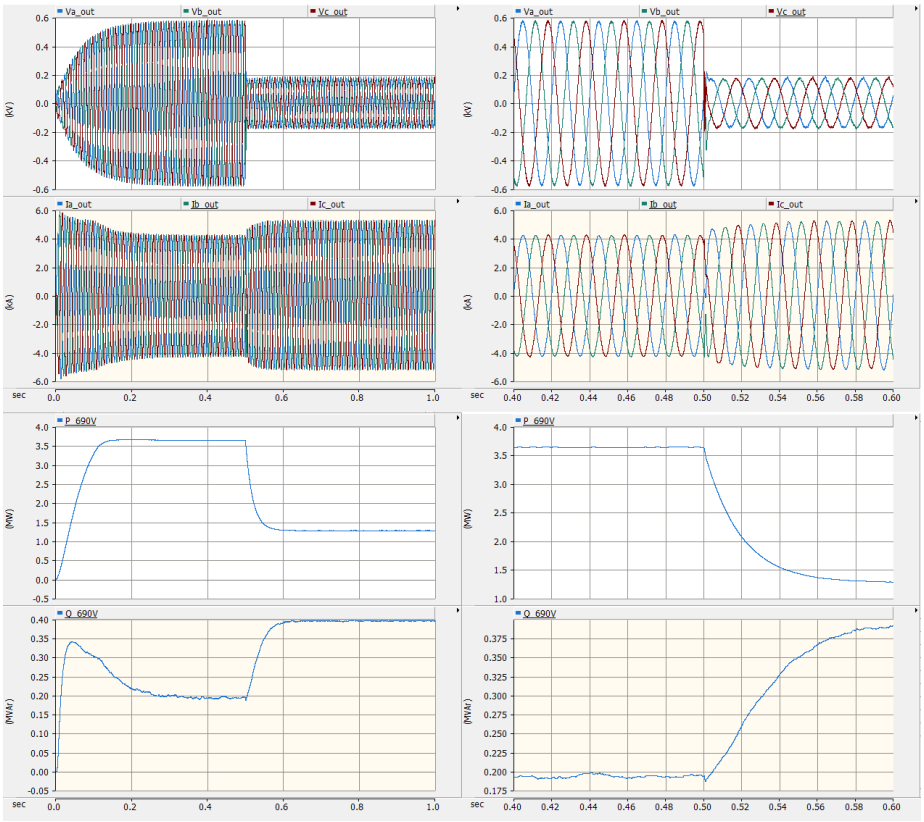


Figure 26: The voltage, current, active and reactive power supplied by the inverter at the 690V terminal right in front of the 0.69/33kV step-up transformer. The peak phase voltage and the peak phase current right before fault initiation were 570 V and 4.22 kA, respectively. The active and reactive power were 3.64 MW and 0.193 MVAr respectively. After the fault, the peak phase current converges to 5.25 kA.

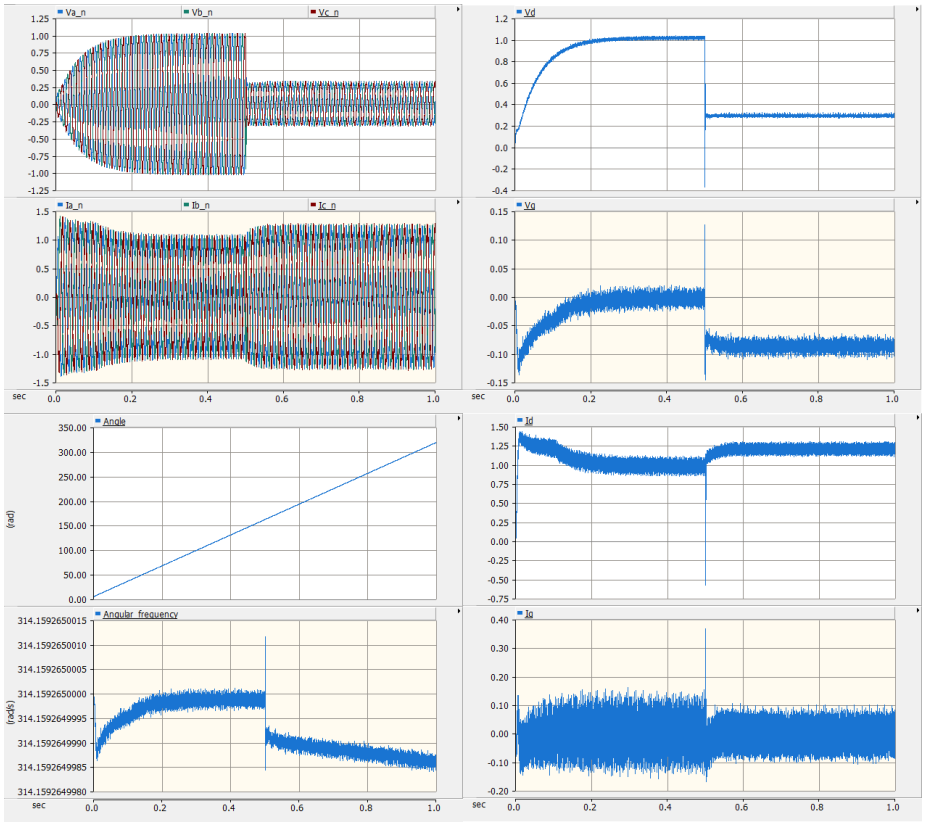


Figure 27: Inverter control: The normalized voltages and currents, the DQ0-transformed voltages and currents, and the PLL angle and angular frequency.

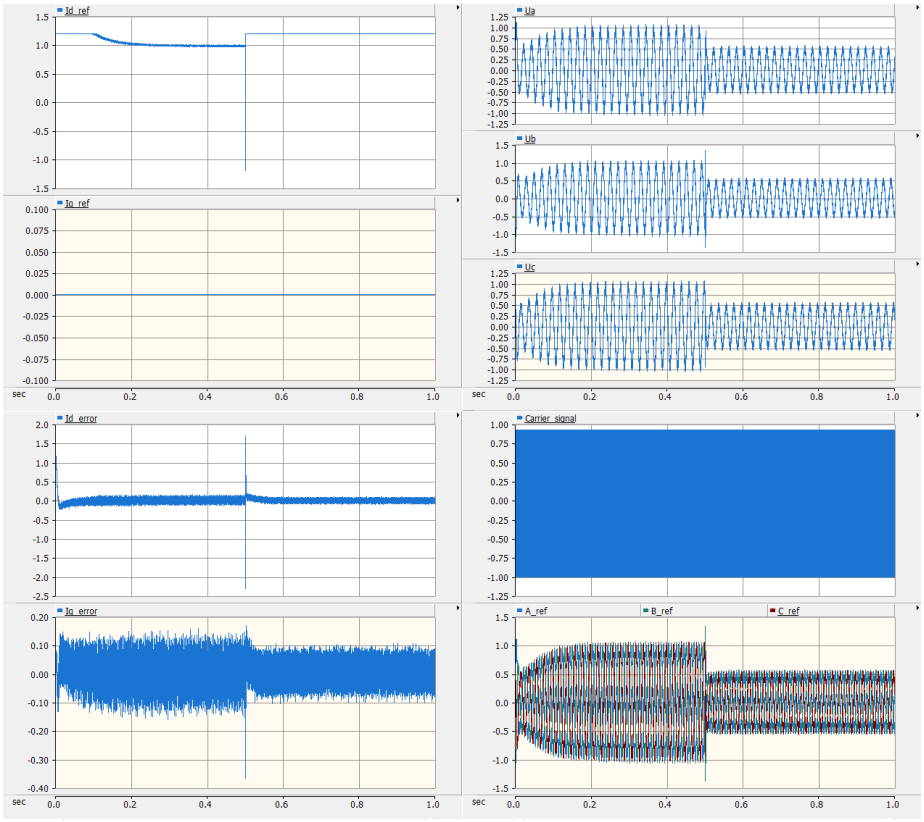


Figure 28: Inverter control: The references $I_{d,ref}$ and $I_{q,ref}$ and the corresponding errors, the PWM reference signals and the carrier signal. Note that the carrier signal seems to have a positive peak lower than 1. This is due to the plotting time step of 20 μs, in contrast to the solution time step of 5 μs. The carrier signal is therefore closer to 1 than displayed here.

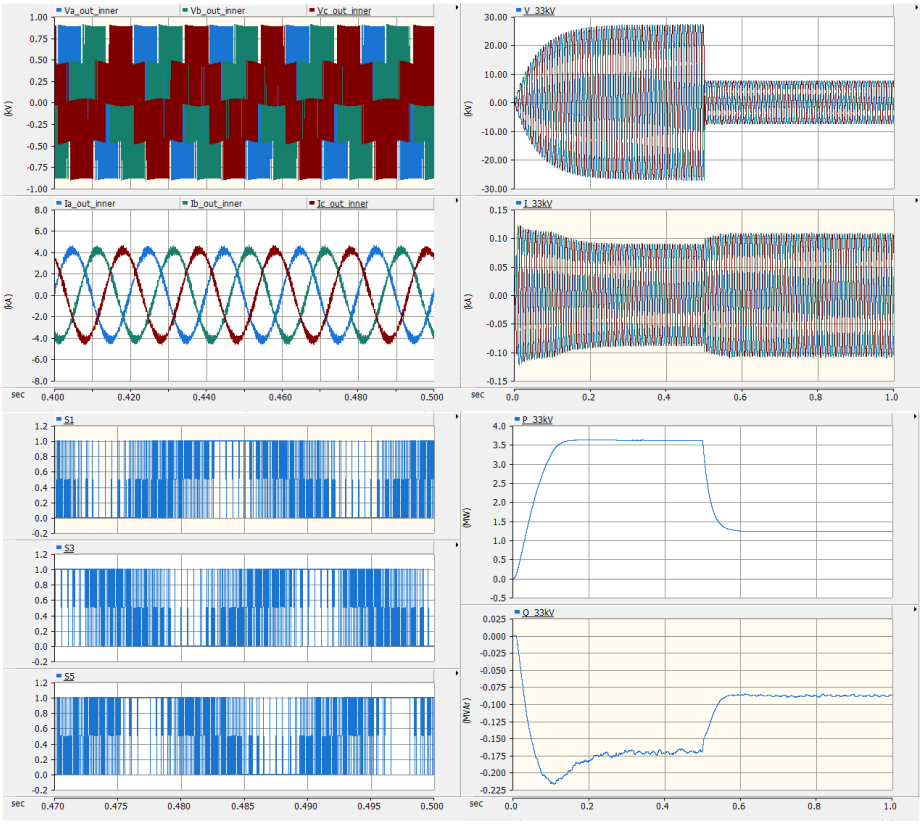


Figure 29: The inner voltages and currents (before filtering), the IGBT switching signals and the 33kV terminal outputs.

4.1.2 Influence of PI controller tuning

The PI controllers for the inner current control will have an impact on the inverter current response, and the tuning of the proportional gain K_P and the integral time constant T_I will have to be set correctly. In Figure 30, the inverter current is shown for different values of K_P and T_I. The model parameters are identical to Verification 1, see Table 11. During sinusoidal inverter terminal voltages, no major differences are observed between the different controller tunings. Nonetheless, a proportional gain of around 1 seems to give the most stable current output.

It is important to make sure that the PI controller tuning is suitable for distorted voltages on the inverter terminals as well, as most of the later simulations will have distorted voltages as a cause of significant voltage drops on Bus 1 and PCC, but also due to the transient response of the transmission line. Figure 31 shows the tests results from a scenario with different model parameters, resulting in a more distorted voltage, such that the inverter control is barely able to generate a sinusoidal current output. All parameters are identical to Verification 1, except $|Z_{infeeder}| = 2576\Omega$ and $R_{fault} = 5\Omega$. Due to the much higher source impedance, even with a higher fault resistance Bus 1 will experience a larger voltage drop, creating difficulties for the inverter control. Based on the results in Figure 31, and some additional simulations, it was decided to let the PI controller tuning be set to $K_P = 1$ and $T_I = 0.02$. This tuning will be used for all further simulations.

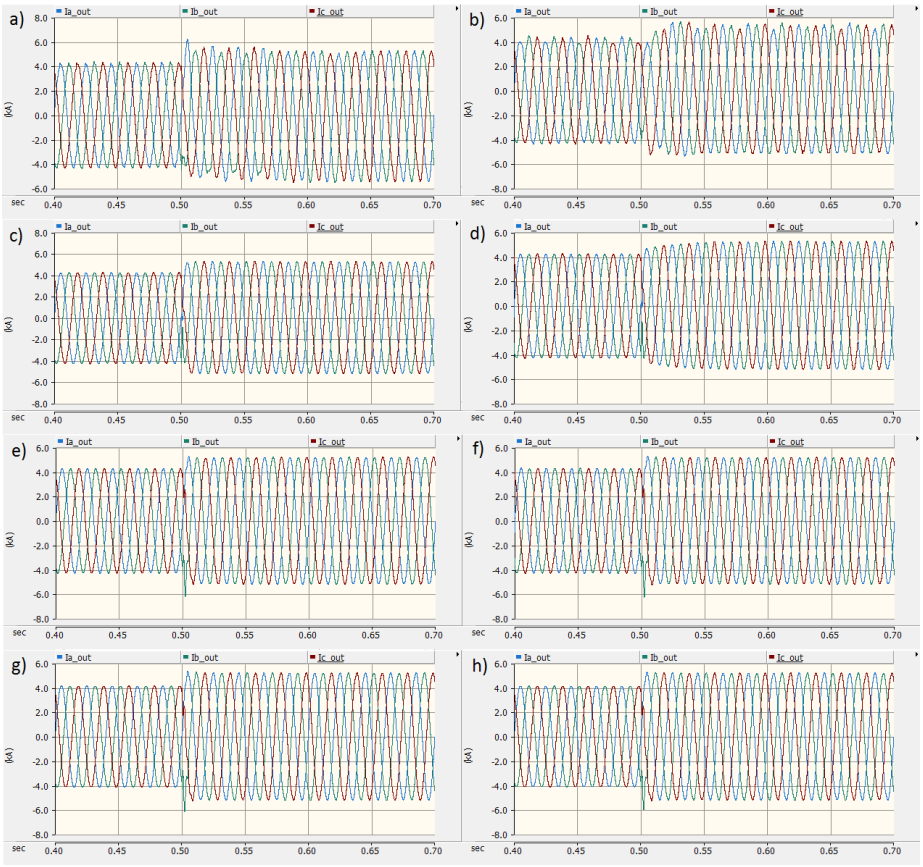


Figure 30: The current output of the inverter for different values of K_P and T_I during stable terminal voltage after fault initiation. The PI controllers are limited to [-1, 1] in all cases.

a) $K_P = 0.1$, $T_I = 0.002$
b) $K_P = 0.1$, $T_I = 0.02$
c) $K_P = 1$, $T_I = 0.002$
d) $K_P = 1$, $T_I = 0.02$
e) $K_P = 10$, $T_I = 0.002$
f) $K_P = 10$, $T_I = 0.02$
g) $K_P = 100$, $T_I = 0.002$
h) $K_P = 100$, $T_I = 0.02$

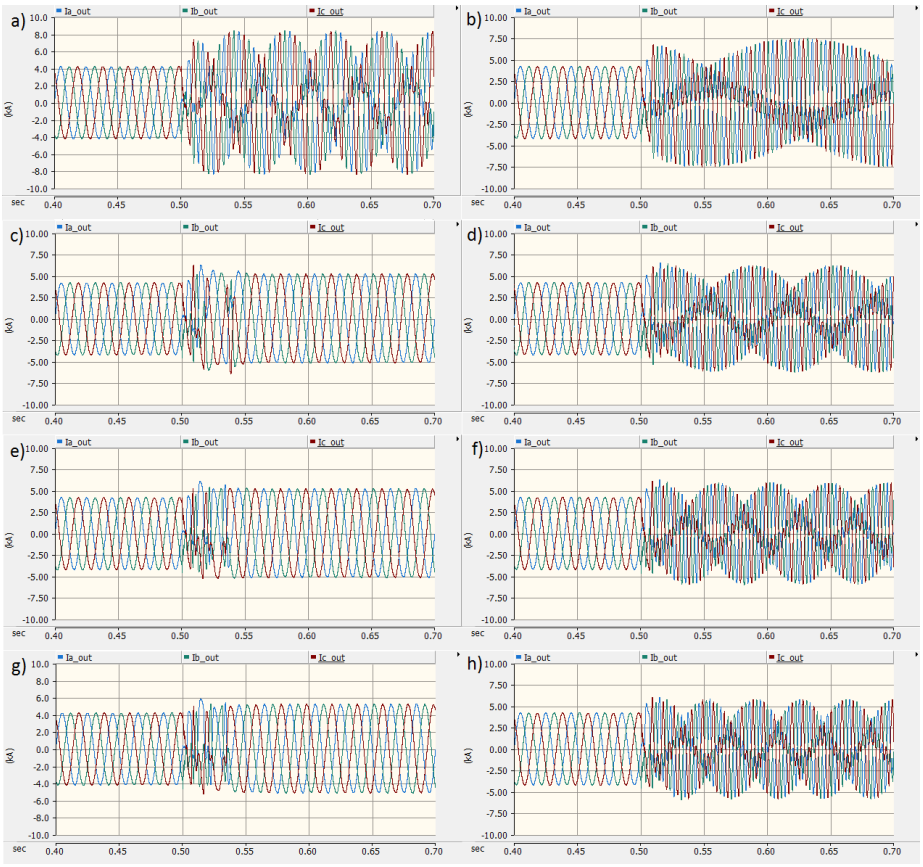


Figure 31: The current output of the inverter for different values of K_P and T_I during critical voltage stability at the inverter terminal after fault initiation. The PI controllers are limited to [-1, 1] in all cases.

a) $K_P = 1$, $T_I = 0.002$
b) $K_P = 2$, $T_I = 0.002$
c) $K_P = 1$, $T_I = 0.005$
d) $K_P = 2$, $T_I = 0.005$
e) $K_P = 1$, $T_I = 0.01$
f) $K_P = 2$, $T_I = 0.01$
g) $K_P = 1$, $T_I = 0.02$
h) $K_P = 2$, $T_I = 0.02$

4.1.3 Further verification of the power output

The inverter should be able to deliver power accurately at different power factors. Figure 32 and 33 shows the power output of the inverter for different active and reactive power references at the 33kV level (PCC). The inverter rating is 3.6 MVA.

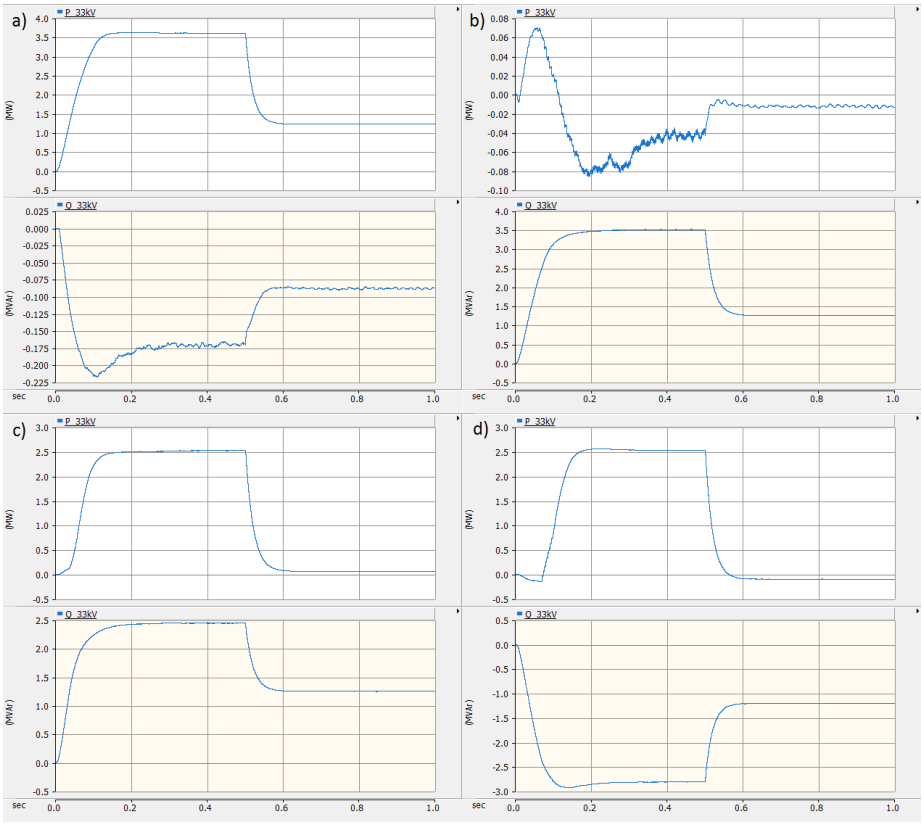


Figure 32: The power output of the inverter after step-up to 33kV. The active and reactive power references are given below.
a) P* = 1 pu = 3.6 MW, Q* = 0 pu = 0 MVAr
b) P* = 0 pu = 0 MW, Q* = 1 pu = 3.6 MVAr
c) P* = 0.707 pu = 2.55 MW, Q* = 0.707 pu = 2.55 MVAr
d) P* = 0.707 pu = 2.55 MW, Q* = -0.707 pu = -2.55 MVAr

The simulations from Figure 32 and 33 show that the power references are met, with acceptable accuracy. The reactive power output is generally lower than the reference, which is explained by the leakage reactance of the step-up transformer. Even though deviations occur, the accuracy is acceptable for this type of study.

From the same set of simulations, it was observed that the current output after fault initiation was distorted (not purely sinusoidal) for power factors different than 1. Thus, to generate the smoothest current during the fault, the inverter power factor would have to be set to 1; P*=1 pu and Q*=0 pu. Further simulations should therefore be executed with these power references, as this inverter model is more predictable under such circumstances. Ideally, the inverter should have produced the same sinusoidal current for other power factors as well, which highlights one of the drawbacks of this inverter model.

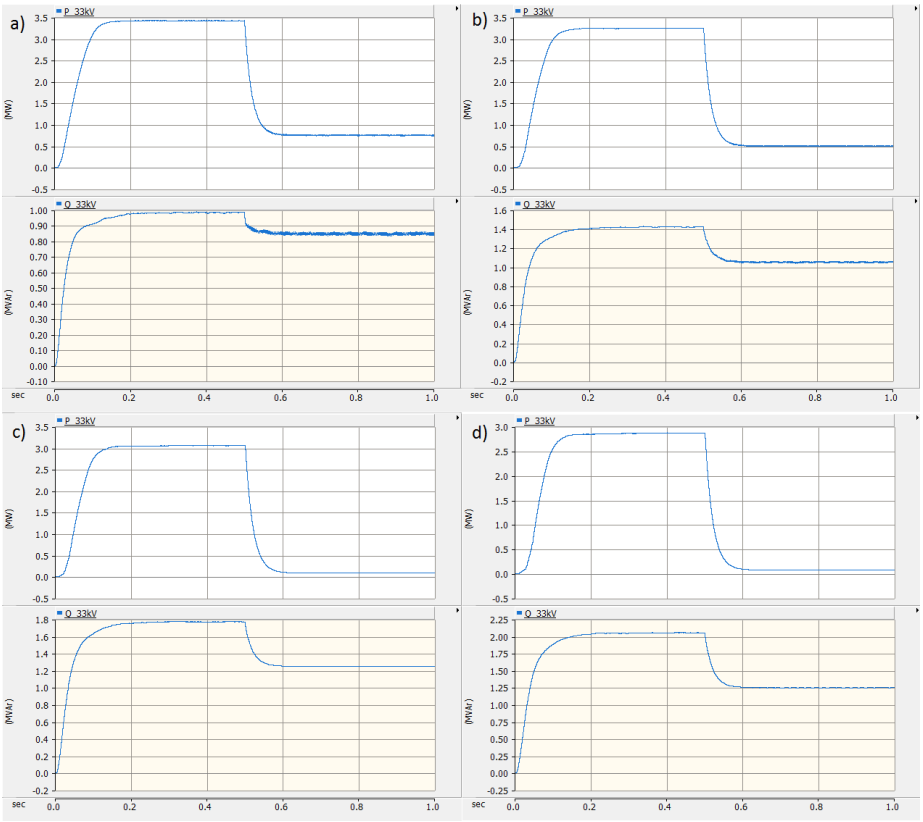


Figure 33: The power output of the inverter after step-up to 33kV. The active and reactive power references are given below.
a) P* = 0.95 pu = 3.42 MW, Q* = 0.312 pu = 1.12 MVAr
b) P* = 0.9 pu = 3.24 MW, Q* = 0.436 pu = 1.57 MVAr
c) P* = 0.85 pu = 3.06 MW, Q* = 0.527 pu = 1.90 MVAr
d) P* = 0.8 pu = 2.88 MW, Q* = 0.6 pu = 2.16 MVAr

4.1.4 Current limiter

The current limiter has been developed without the use of any references. Thus, it will have to be verified here.

In Figure 34, the current limit has been set to different values, and the corresponding current output is displayed. The model parameters are identical to those in Verification 1, see Table 11.

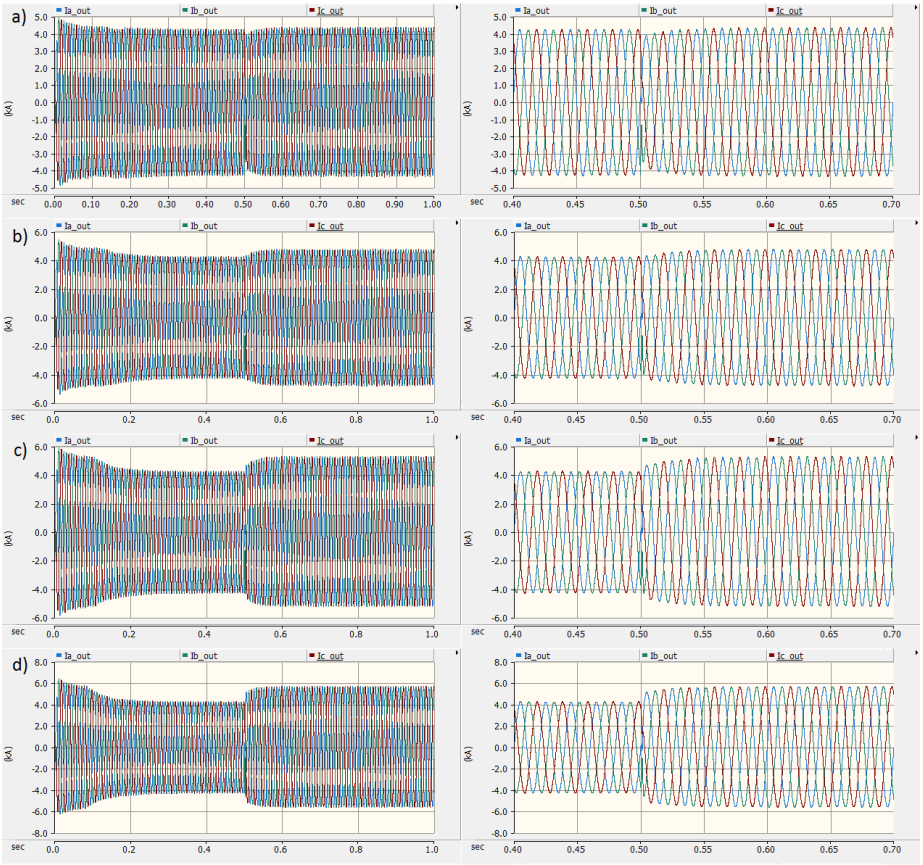


Figure 34: The current output of the inverter for different current limits. Below, the references of the currents are compared to the measured stationary current after the fault. Ahead of the fault, all currents were about 4.24 A peak.

a) I_{lim}= 1 pu = 4.26 A peak — Measured: 4.33 A peak
b) I_{lim}= 1.1 pu = 4.69 A peak — Measured: 4.73 A peak
c) I_{lim}= 1.2 pu = 5.11 A peak — Measured: 5.25 A peak
d) I_{lim}= 1.3 pu = 5.54 A peak — Measured: 5.65 A peak

The current limiter seems to work as designated based on the results presented in Figure 34. The current is limited to the given current limit, with some deviation. Based on earlier simulations, this current limiter was observed to not function correctly under unbalanced faults, as the control system is confused during such circumstances.

4.2 Verification of the Distance Protection Relay

The distance protection relay algorithm has been developed based on PSCAD's cookbook for protection studies. The algorithm is simple, and correlates to classic numerical distance protection. The implemented distance protection algorithm should be verified to accurately measure the fault impedance during a short circuit. The model parameters are identical to those in Verification 1.

First, Relay 1 is looked into in detail, and then both relays are examined for different fault resistances and locations.

4.2.1 Detailed examination of Relay 1

For the same model parameters as in Verification 1, Relay 1 is examined in detail. As $|Z_{infeeder}|= 25.76\ \Omega$, the current from both ends of line 12 should be similar in magnitude during the fault. This is shown in Figure 35. Problems related to fault impedance measurement from distance protection relays are not expected when the short circuit current contribution from the two sides are similar and stable. Thus, this setup can be used to verify the accuracy of the impedance measurement and the tripping times for ideal conditions.

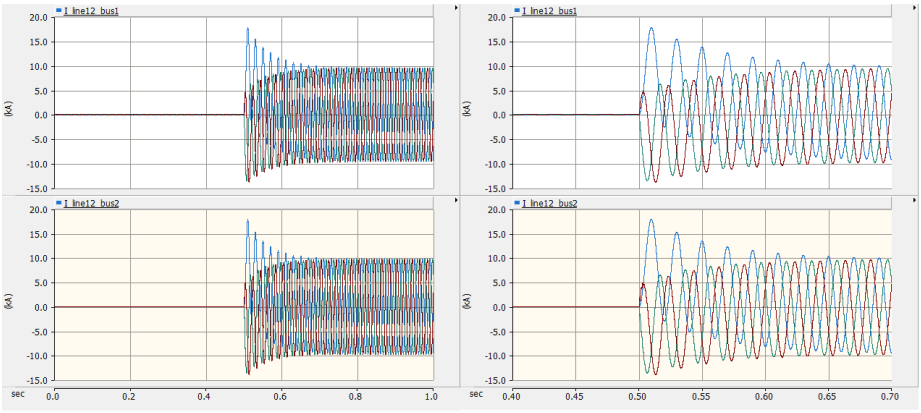


Figure 35: The current flowing into line 12 from bus 1 and bus 2.

In PSCAD, voltage and current transformers take digital signals as inputs,

not electrical signals. Thus, the voltage and current inputs of the relays are measured by ideal voltmeters and ammeters before they pass through the VT and CT blocks which emulates the influence of these transformers. The VTs and CTs have been scaled properly, and the output is passed through a gain block such that the output equals the input (for balanced nominal conditions). The signals before entering the VTs and CTs are indicated as the primary signals, see Figure 36. After transformation and the gain compensation, the signals are referred to as the secondary signals. These secondary signals are used for fault impedance calculation.

The fault impedance are measured independently by the six fault loops A-G, B-G, C-G, A-B, B-C and C-A. Notation-wise, Ra and Xa are the resistance and reactance measured by the A-G phase to ground component of the relay. Rab and Xab are the resistance and reactance measured by the A-B phase to phase impedance component of the relay. Similar notation is used for the other fault loops.

The impedance diagram of Relay 1 is shown in Figure 37.

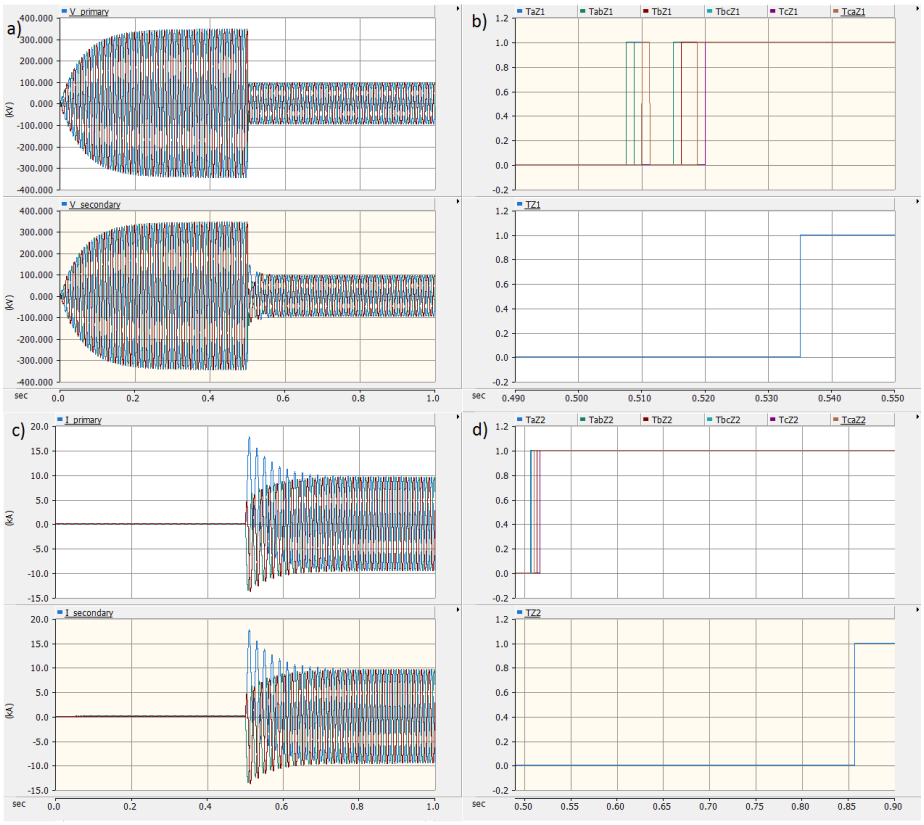


Figure 36: The phase voltages and currents before and after passing through the voltage and current transformers, in addition to the zone 1 and zone 2 fault detection and their corresponding tripping times.
a) Phase voltages of the primary side of the voltage transformer, and phase voltages of the secondary side including compensation.
b) Fault detection of the different fault loops for zone 1, and the relay tripping time set to trip after 20 ms of consecutive fault detection for any of the fault loops.
c) Currents of the primary side of the current transformer, and the currents of the secondary side including compensation.
d) Fault detection of the different fault loops for zone 2, and the relay tripping time set to trip after 350 ms of consecutive fault detection of any for the fault loops.

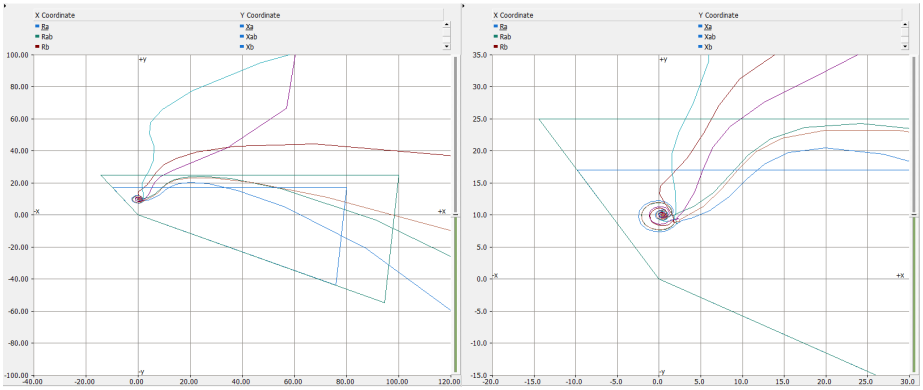


Figure 37: Impedance diagram of Relay 1 with plotting of the measured fault impedances of the six fault loops. The x-axis is the resistance in ohms, and the y-axis is the reactance in ohms. The quadrilateral zone borders of zone 1 and zone 2 are plotted as well. Ra and Xa converged to 0.4447 Ω and 10.03 Ω, respectively. In comparison, the exact positive sequence impedance of 50% of the line is 0.6728 + j10.01 Ω.

4.2.2 Different fault resistances

In Figure 38, the impedance diagram is displayed for four different fault resistances. It can be observed that the reactance measurements are accurate, yet the resistance measurements have deviations. Theoretically, according to [6] the resistance measurement should be accurate for lower values of R_{fault}. For higher values of R_{fault} and when the short circuit contribution from both sides is similar, the relay will experience a doubling of R_{fault}. This can be observed for c) and d) in Figure 38, where R_{fault} is dominating the line resistance.

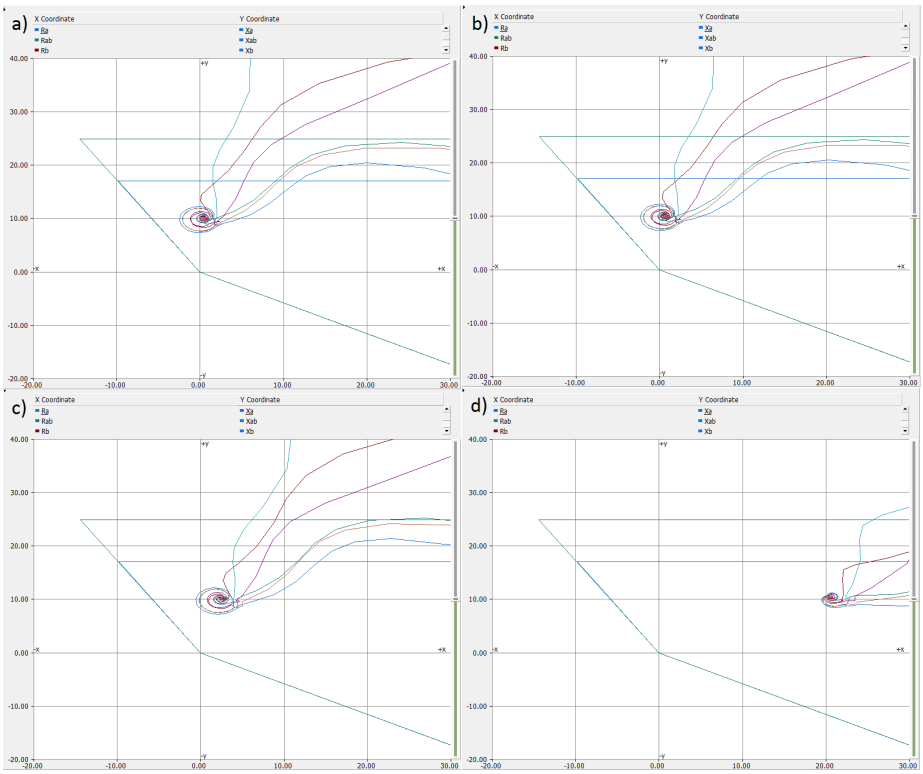


Figure 38: Impedance diagram of Relay 1 for different values of the fault resistance R_{fault}, with fault location at 50% of Line 12. For comparison, the positive sequence line impedance for 50% of line 12 is 0.6728 + j10.01 Ω.

a) $R_{fault} = 0.01\ \Omega$: $Z_a = 0.4447 + j10.03\ \Omega$.
b) $R_{fault} = 0.1\ \Omega$: $Z_a = 0.6262 + j10.03\ \Omega$.
c) $R_{fault} = 1\ \Omega$: $Z_a = 2.443 + j10.08\ \Omega$.
d) $R_{fault} = 10\ \Omega$: $Z_a = 20.61 + j10.43\ \Omega$.

4.2.3 Different fault locations

The fault has been set to different locations to verify if the relay is able to place the fault in the correct zone. The results are displayed in Figure 39. In all of the four test scenarios, Relay 1 tripped correctly, with zone 1 tripping for a) and b) and zone 2 tripping for c) and d). Even though scenario d) lead to correct tripping here, one can observe that the measured fault impedance was very close to the border of zone 2. A fault located at 15% of line 23 may therefore cause incorrect tripping. When a fault occurs on neighboring lines, like in d), relays may experience problems caused by feeding from other lines (line 24 in this case). However, for faults on line 12, problems related to this is not expected for Relay 1 and Relay 2.

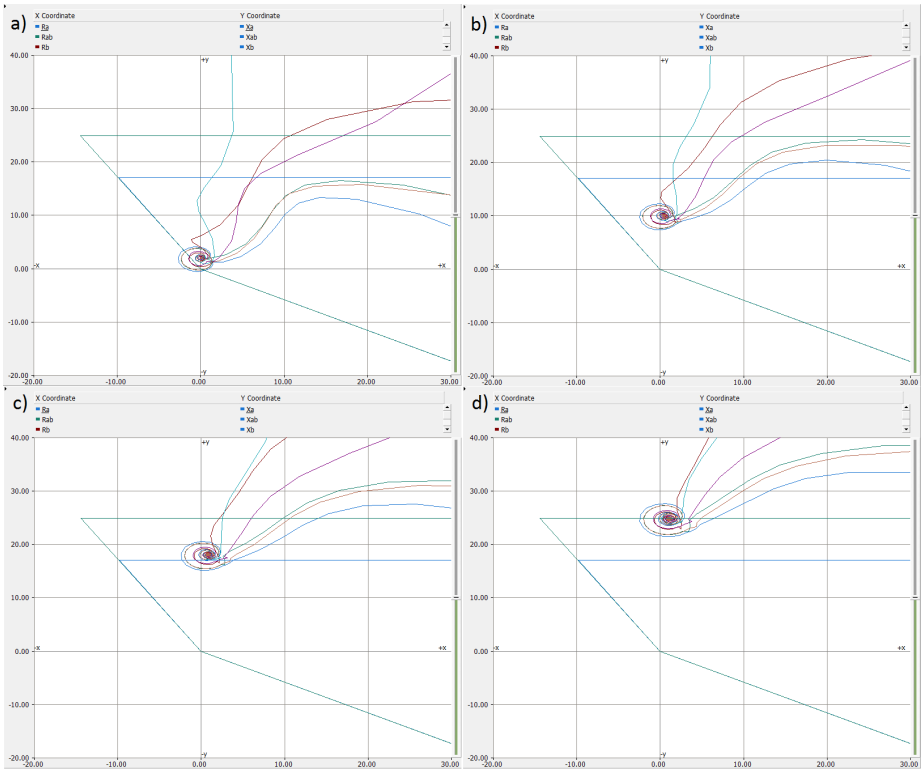


Figure 39: Impedance diagram of Relay 1 for different fault locations, with fault resistance R_{fault} equal to 0.01 Ω. Zone 1 is set to 85% of Line 12, and zone 2 is set to 100% of Line 12 plus 20% of Line 23.

a) At 10% of Line 12: $Z_a = 0.1015 + j2.005\ \Omega$.
b) At 50% of Line 12: $Z_a = 0.4447 + j10.03\ \Omega$.
c) At 90% of Line 12: $Z_a = 0.7912 + j18.07\ \Omega$.
d) At 10% of Line 23: $Z_a = 1.075 + j24.82\ \Omega$.

5 Results

This chapter presents the main simulation results, primarily being the tripping times of the inverter side relay (Relay 1). Additional simulation results are presented in Appendix A, B, C and D for Simulation set 1, 2, 3 and 4, respectively.

For Simulation set 1, the infeeder is completely disconnected from Bus 1, and one single inverter is connected to PCC. For Simulation set 2, the infeeder remains disconnected, and ten inverters are connected to PCC. For Simulation set 3, the infeeder is connected to Bus 1, and the share of inverter generation is varied from 0% to 100%. For Simulation set 4, only the infeeder is connected to Bus 1 (no inverters are connected to PCC), and the impact of different short circuit current contributions from the two ends of line 12 was investigated. The main model parameter set is given in Table 12.

Table 12: Model parameter set 1.

Parameter	Value	Description
P*	1 pu	Active power reference set to deliver 1 pu active power.
Q*	0 pu	Reactive power reference set to deliver 0 pu reactive power.
I_{lim}	1.2 pu	Current output limit of the inverter set to 1.2 pu.
K_P	1	Proportional gain of PI controllers set to 1.
T_I	0.02 s	Integral time constant of PI controllers set to 0.02 s.
$\|Z_{infeeder}\|$	-	The infeeder is physically disconnected from Bus 1.
Fault type	L-L-L-G	The fault type is a symmetrical three-phase to ground fault.
R_{fault}	-	The fault resistance of the fault on Line 12 will vary.
x_{fault}	50%	Fault location on Line 12 set to 50% of the line length, from bus 1.
t_{fault}	0.5 s	Fault initiation time set to 0.5 seconds. The fault duration is set to last for the rest of the simulation.
T_{zone_1}	20 ms	Time delay for zone 1 set to 20 ms to avoid unwanted tripping. Zone 1 fault detection consecutively for 20 ms will cause tripping.
Tripping	No	Protection relays are set to not trip their breakers, regardless of fault detection.

5.1 Simulation set 1 - Generation from one single inverter

Initially, the infeeder was completely disconnected from Bus 1 making the inverter the only power generating source connected to Bus 1 (via PCC). The model parameters are set as in Table 12.

The Relay 1 zone 1 trip times are summarized in Table 13.

Relay 2, located on the grid side, did not experience any problems.

For visualization, the Relay 1 fault impedance diagrams for different fault resistances, varying from 0.0001 Ω to 10 Ω, are shown in Figure 40. The fault impedance diagrams for both relays for a fault resistance of 0.0001 Ω are displayed in Figure 41.

Additional results, such as the inverter output, the short circuit current contribution from both sides of the line, and trip times, are presented in Appendix A.

Table 13: Relay 1 zone 1 trip times for one single inverter connected to PCC, for different values of R_{fault}. The trip time is the duration from fault inception until the relay sends the trip signal. The selected model parameters are given in Table 12.
Green = tripped within 0.1 s after fault initiation.
Yellow = tripped within 0.5 s after fault initiation.
Red = did not trip within 0.5 s after fault initiation

R_{fault} [Ω]	0.0001	0.001	0.01	0.1	1	10
t_{trip} [s]	0.3137	0.2462	-	-	-	-

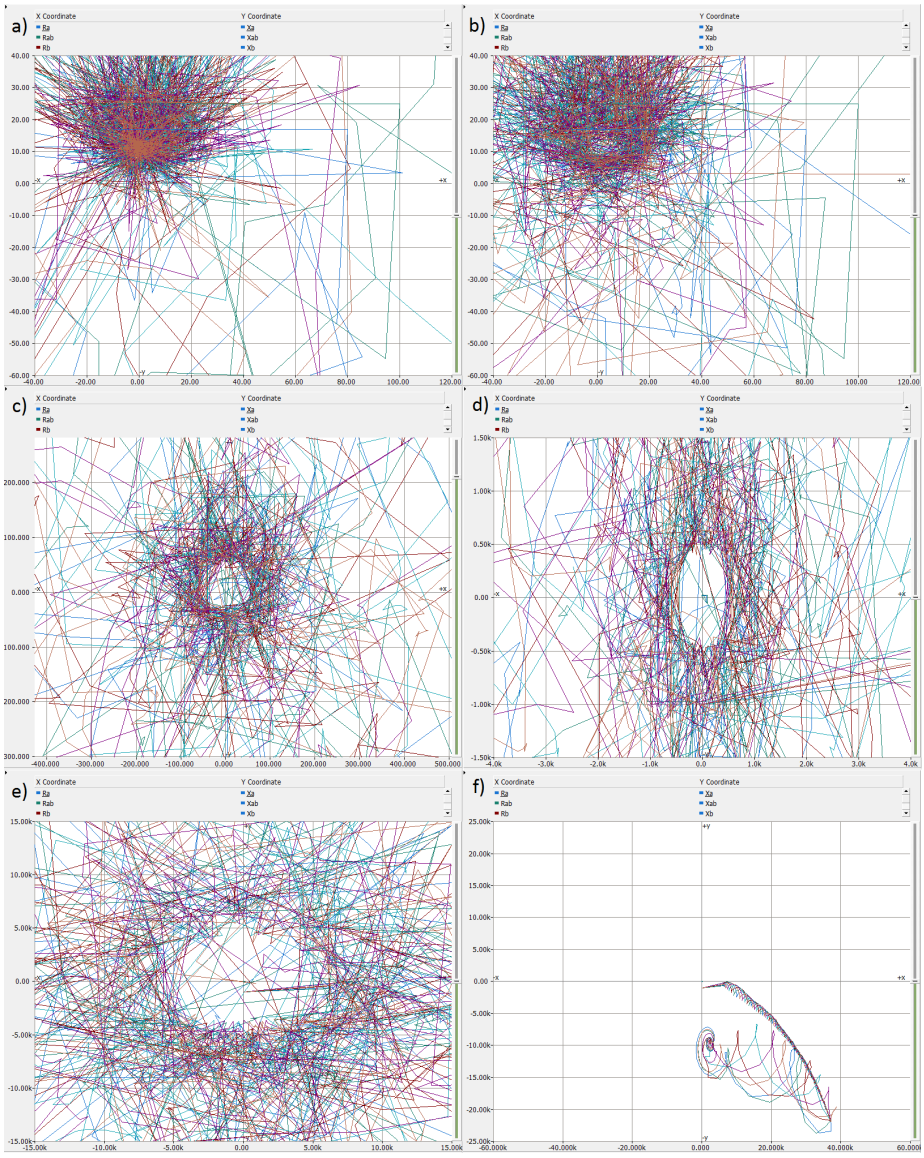


Figure 40: The fault impedances of the six fault loops measured by Relay 1 for one single inverter connected to PCC. The selected model parameters are given in Table 12, and the fault resistances R_{fault} are given below. Note that the scaling of the axes may differ. The measured fault impedance for the fault loop A-G is given when convergence is obtained.

a) $R_{fault} = 0.0001\ \Omega$, b) $R_{fault} = 0.001\ \Omega$
c) $R_{fault} = 0.01\ \Omega$ d) $R_{fault} = 0.1\ \Omega$
e) $R_{fault} = 1\ \Omega$ f) $R_{fault} = 10\ \Omega$; Z_a = 2381 - j9456 Ω

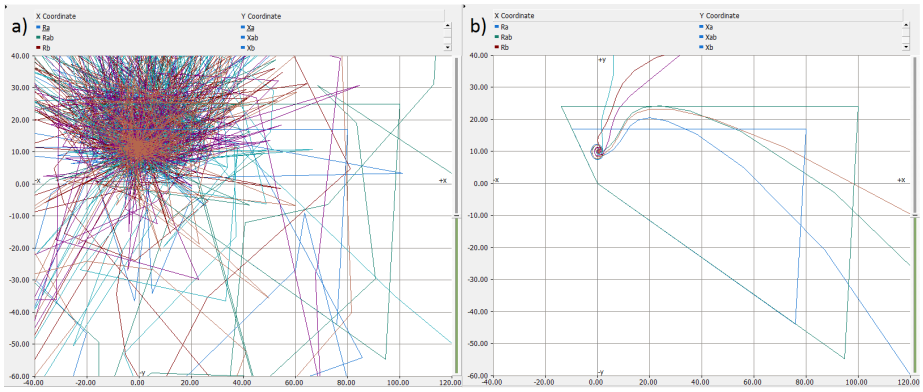


Figure 41: The fault impedances of the six fault loops measured by Relay 1 (left) and Relay 2 (right; $Z_a = 0.4242 + \text{j}10.03\ \Omega$). The selected model parameters are given in Table 12, and the fault resistance R_{fault} is set to 0.0001 Ω.

5.2 Simulation set 2 - Generation from ten inverters

To observe the impact of installing multiple inverters, it was decided to run the same set of simulations, but with ten inverters connected to PCC. The model parameters are set as in Table 12.

The Relay 1 zone 1 trip times are summarized in Table 14.

Relay 2, located on the grid side, did not experience any problems.

For visualization, the impedance diagrams of Relay 1 are shown in Figure 42.

Additional simulation results have been presented in Appendix B.

Table 14: Relay 1 zone 1 trip times for 10 inverters connected to PCC, for different values of R_{fault}. The trip time is the duration from fault inception until the relay sends the trip signal. The selected model parameters are given in Table 12.
Green = tripped within 0.1 s after fault initiation.
Yellow = tripped within 0.5 s after fault initiation.
Red = did not trip within 0.5 s after fault initiation

R_{fault} [Ω]	0.0001	0.001	0.01	0.1	1	10
t_{trip} [s]	0.2400	0.2487	0.4900	-	-	-

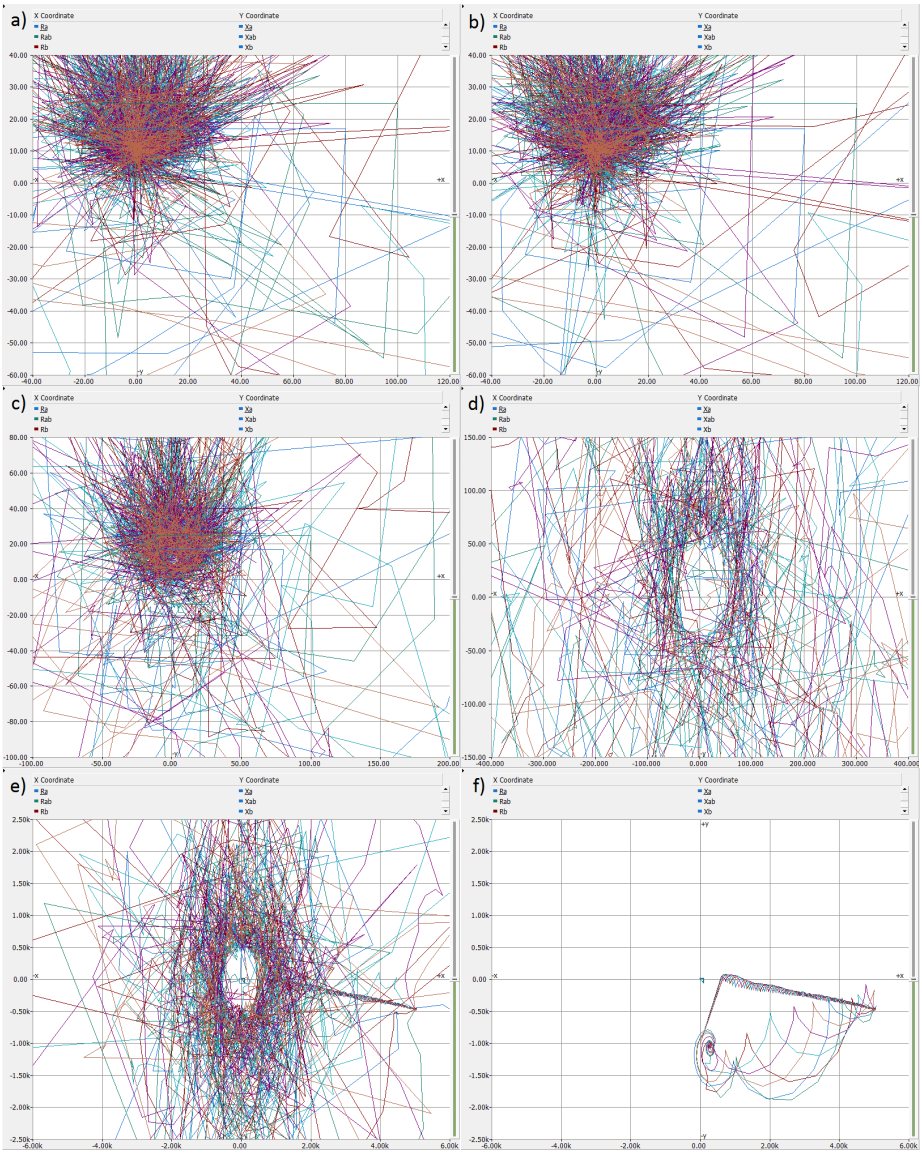


Figure 42: The fault impedances of the six fault loops measured by Relay 1 for one single inverter connected to PCC. The selected model parameters are given in Table 12, and the fault resistances R_{fault} are given below. Note that the scaling of the axes differ. The measured fault impedance for the fault loop A-G is given when convergence is obtained.

a) $R_{fault} = 0.0001\ \Omega$,
b) $R_{fault} = 0.001\ \Omega$
c) $R_{fault} = 0.01\ \Omega$
d) $R_{fault} = 0.1\ \Omega$
e) $R_{fault} = 1\ \Omega$
f) $R_{fault} = 10\ \Omega$; Z_a = 280.0 - j1029 Ω

5.3 Simulation set 3 - Share of inverter generation

The infeeder is now connected to Bus 1, representing synchronous generation. The source impedance of the infeeder is chosen such that the short circuit current contribution of the infeeder is comparable to a given number of 3.6 MVA 690 V synchronous generators.

The total rated power (of both the inverters and the infeeder equivalent) is held constant at 36 MVA. The share of inverter interfaced generation can be adjusted by selecting how many inverters are connected to PCC, and by adjusting the infeeder source impedance. The inverter generation is increased by steps of 10% (3.6 MVA) from 0% (0 MVA) to 100% (36 MVA), and the infeeder source impedance is chosen accordingly to obtain a total rating of 36 MVA. The different scenarios are listed in Table 15.

Table 15: Overview of the number of 3.6 MVA 690V inverters connected to PCC, and the corresponding value for $|Z_{infeeder}|$ resulting in an equivalent short circuit current contribution for a number of 3.6 MVA 690V synchronous generators. The total rating of inverter and synchronous generation is held constant at 36 MVA.

Inverter %	Inverters	Synchronous generator %	Equivalent synchronous generators	$\|Z_{infeeder}\|$ [Ω]
0%	0	100%	10	1156
10%	1	90%	9	1284.4
20%	2	80%	8	1445.0
30%	3	70%	7	1651.4
40%	4	60%	6	1926.7
50%	5	50%	5	2312.0
60%	6	40%	4	2890.0
70%	7	30%	3	3853.3
80%	8	20%	2	5780.0
90%	9	10%	1	11560
100%	10	0%	0	-

The zone 1 trip times for Relay 1 are summarized in Table 16.

Relay 2, located on the grid side, did not experience any problems.

The fault impedance diagrams and the trip times are presented in Appendix C.

Table 16: Relay 1 zone 1 trip times in seconds for different shares of inverter generation, for different values of R_{fault}. The trip time is the duration from fault inception until the relay sends the trip signal. The selected model parameters are given in Table 12.
Green = tripped within 0.1 s after fault initiation.
Yellow = tripped within 0.5 s after fault initiation.
Red = did not trip within 0.5 s after fault initiation

R_{fault} [Ω] Inverter %	0.0001	0.001	0.01	0.1	1	10
0%	0.0837	0.0837	0.0837	0.0650	0.0662	-
10%	0.0900	0.0837	0.0837	0.0650	0.0662	-
20%	0.0912	0.0912	0.0912	0.0650	0.0675	-
30%	0.0925	0.0925	0.0925	0.0825	0.0687	-
40%	0.0937	0.0937	0.0925	0.0825	0.0937	-
50%	0.0937	0.0937	0.0937	0.0937	0.0950	-
60%	0.0937	0.0937	0.0937	0.0950	-	-
70%	0.1137	0.1137	0.1100	0.0950	-	-
80%	0.1537	0.1537	0.1250	0.0950	-	-
90%	0.1537	0.1562	0.1525	0.1250	-	-
100%	0.2400	0.2487	0.4900	-	-	-

5.4 Simulation set 4 - Influence of different short circuit current contributions

This simulation set has been carried out to examine the influence of different short circuit current contributions from the ends of the transmission line. All inverters have been disconnected from PCC, and the infeeder is the only source connected to Bus 1. The infeeder source impedance $|Z_{infeeder}|$ has been varied with factors of ten, resulting in different short circuit currents flowing from the two line ends.

The zone 1 trip times for Relay 1 is summarized in Table 17.

Relay 2, located on the other side (grid side), did not experience any problems.

The fault impedance diagrams, trip times, and the currents entering both ends of line 12, are presented in Appendix D.

Table 17: Relay 1 zone 1 trip times in seconds for different values of $|Z_{infeeder}|$ and R_{fault}. The trip time is the duration from fault inception until the relay sends the trip signal. The selected model parameters are given in Table 12, except for $|Z_{infeeder}|$, and no inverters were connected to PCC.
Green = tripped within 0.1 s after fault initiation.
Yellow = tripped within 0.5 s after fault initiation.
Red = did not trip within 0.5 s after fault initiation

$\|Z_{infeeder}\|$	R_{fault} [Ω] I_{Bus2}/I_{Bus1}	0.0001	0.001	0.01	0.1	1	10
25.76 Ω	1.02	0.0350	0.0350	0.0350	0.0350	0.0362	0.0362
257.6 Ω	7.58	0.0375	0.0375	0.0375	0.0375	0.0375	-
2576 Ω	73.4	0.0937	0.0937	0.0937	0.0937	0.1062	-
25760 Ω	732	0.1537	0.1537	0.1537	0.1587	-	-

6 Discussion

This chapter covers discussion of the model assumptions and weaknesses, the results, and additional topics of interest.

6.1 Discussion of model assumptions and weaknesses

Type 4 Wind Turbines (T4WTs) are obviously more comprehensive than the simplification in this model. The power being generated by a wind turbine depends on the wind speed, which is normally way below the rated wind speed of about 12 m/s, at which the turbine starts generating rated power [46] [47]. This may lead to a lower short circuit current contribution than the model shows. There will also be uncertainties associated with the DC voltage at the DC link between the rectifier and the inverter. How this voltage will drop during short circuits for different wind speeds would be interesting to study as it is expected to influence the output current of the inverter. Thus, an inverter being supplied by an ideal constant DC source is probably not a very accurate approximation of a T4WT. At least, the model it is representative for scenarios where the DC link voltage would have remained constant at rated voltage.

The inverter developed in this model is a Grid-feeding inverter with given references for the active and reactive power P* and Q*. In other words, this inverter tries to deliver the power references to the grid, regardless of the grid voltage and frequency. Thus, it is not the optimal way of controlling the inverter. Earlier, distributed generation was frequently disconnected to the grid during faults, and it was not critical that fault handling was integrated. However, now as inverter interfaced generation starts to reach noteworthy shares of the total generation, these sources will also have to contribute to grid stability. Thus, Fault Ride Through (FRT) requirements have lately become more important for wind turbines, and the turbines should then possess grid supporting control [1] [3]. A Grid-supporting inverter is more optimized for this than a Grid-feeding inverter, and its droop control will deliver active and reactive power based on the voltage and frequency errors.

During the main simulation sets, the Grid-feeding inverter references for P* and Q* were set to 1 pu and 0 pu, respectively, resulting in a power factor of 1. This was due to the observations made in the "Verification of the model" chapter, where these references provided the most stable inverter outputs. A power factor of 1 may not be the most commonly used power factor, as it may be beneficial to also generate or consume some reactive power, depending on the system. Still, this is expected to have little impact on the results. The model should be improved to also generate a sinusoidal output current for power factors different than 1.

Referring to simulation set 1 and 2 (and Appendix A and B), the short circuit current contribution from inverters is generally hard to predict. Multiple reports that have analyzed the inverter current, point to the fact that the current is highly unpredictable during the initial transient state just after the fault initiation [4] [36] [42]. The "transient state", which depending on the reports [4], [36] and [42] could last from half a cycle (10 ms) up to three-cycles ore more (60 ms), is hard to determine from the results of this thesis since the current and voltage signals generally never reach the sinusoidal stationary state (see Figure 44 and 47). Instead oscillations around 100-200 Hz remain throughout the rest of the simulation. This contradicts [4], which states that after the initial 60 ms, the current would be predictable. From the same figures, one can observe that the current drops to much lower values than 1 pu (some peak exceptions) during the initial 60 ms after the fault inception. It must be emphasized that this current behaviour was unexpected, and that peaks up to 2-3 pu, similar to the findings in [36], [42] and [44], were expected. On the contrary, for the simulations with a fault resistance of 10 Ω, the signal remained sinusoidal and reached the stationary state after approximately 60 ms (see Figure 45 and 48). These simulations resulting in a non-distorted short circuit current can be linked with the simulations with a converging fault impedance. Actually, the general tendency for the simulations with a fault resistance R_{fault} of 10 Ω, is a converging fault impedance measured by Relay 1 (regardless of whether the fault impedances caused tripping or not). The reasoning for this seems to be linked to the inverter control system and the severity of the voltage drop. Most likely, the inverter control is very sensitive to distorted voltages, such that it behaves unpredictably during such circumstances. During severe voltage drops (due to low fault resistances), the voltage reference signal will be hard to detect and the transient response of the transmission line seems to dominate the inverter terminal voltage, confusing the inverter control. For less severe voltage drops (e.g with $R_{fault} = 10\ \Omega$), the inverter terminal voltage remains sinusoidal, helping the inverter to behave as intended. It is hard to justify whether the short circuit current contribution of the inverter model in this thesis is representative to state-of-the-art inverters. Most likely, the continuous unpredictable output current during the simulations with R_{fault} ranging from 0.1 mΩ to 1 Ω is not a good comparison to the output current of state-of-the-art inverters.

The fact that only balanced three-phase to ground (L-L-L-G) short circuits were studied in this thesis narrows the scope significantly. Three-phase faults are very rare, according to Statnett and [17], and their fault resistance is low. This means that the scenarios with the higher fault resistances (e.g $R_{fault} = 1$ Ω and $R_{fault} = 10\ \Omega$) may not be representing actual practical phenomenons. Additionally, the obtained results are less valuable, as most grid short circuits are unbalanced [17]. Nonetheless, the same general tendencies may also apply for unbalanced faults as for balanced faults, but this will have to be studied.

A purely resistive short circuit may be reasonable to assume, and is supported by [6] and [5] in similar short circuit studies.

The fault location on Line 12 is expected to have major impact on the relay tripping times. As the fault location in this thesis only covers faults located on the center of the line, the relay fault detection and tripping time results will be close to a "Best case" scenario. This is due to the large margins for error within zone 1. For instance, the fault impedance can appear to have a reactance error of up to 70% and may still appear in zone 1 with a reach of 85% of line 1. This will influence the results significantly, as many of the scenarios cause a non-converging fault impedance. A fault close to the border of zone 1 would probably cause a higher tripping delay or no tripping at all. This leads us to the impact of the time delays for the zones as well. According to [19] the time delay for zone 1 was set to 20 ms, to avoid unwanted tripping (due to potential zone crossings). In the way the distance protection algorithm is implemented [11], a zone 1 fault has to be detected consecutively for 20 ms to cause tripping. This may not be a very clever way to implement the distance protection algorithm as faults can be detected regularly for a long time, but as long as there is no fault detection at any instance before the 20 ms has passed, the timer is reset and no tripping signal is sent. This is even more critical for zone 2, with a delay of 350 ms. Even though this is PSCADs own suggested implementation of classic distance protection, it may contain weaknesses and an improvement of the algorithm should be considered. Note that the time delay is less of a problem when the fault impedances actually converge.

The distance protection algorithm implemented in this model is very basic and does not contain advanced features improving the performance of the relay. Most numerical distance protections today should possess features like improved direction determination (e.g cross-polarisation), options for tripping of faulted phases only, and improved logic to handle e.g. parallel lines and intermediate infeeds [19]. The distance protection in this model is developed in its most basic form, which may distinguish its performance from more advanced relays. Note that zone 1 and 2 are the only zones included in the model. Further reaching, but also backwards reaching zones should be implemented for a complete relay.

The assumption of being able to represent the short circuit current contribution of a synchronous generator with a source equivalent (in Simulation set 3) is bold. The use of a complete synchronous generator model would have been more accurate as the machine response depends on numerous influencing factors. Additionally, the assumption that synchronous generators generate a short circuit current of 6 pu is weak and should be interpreted as a rough approximation only. Despite the approximations, the obtained results are still representative for the given fault current contributions of the infeeder for the different values of $|Z_{infeeder}|$, regardless of whether the theoretical comparison to synchronous generation is accurate or not.

Another influence of not having real synchronous generators in the model is the lack of system inertia. A grid with synchronous generation will in reality

possess inertia preventing sudden changes in the grid frequency.

The phase angles of the sources at the different buses (Bus 1 (the infeeder), Bus 3 and Bus 4) in the model have been set to the same value. This simplification should be avoided, as it may cause additional power flow between the buses. A way to avoid this would have been to only set one single source to a fixed phase angle, and the other sources to adjust themselves to that master source. Due to the added complexity of adapting grid synchronization to the sources, it was decided to go for a simplification of setting their phase angle to the same value. It is important to be aware of the phase angle shifts between the two ends of a transmission line, due to line loading [48]. The angle shift is proportional to the active power loading of the line, such that higher loaded lines have a greater phase angle shift between its ends. In the model, the loading of the lines in the model is low due to the maximum generation rating of only 36 MVA connected to Bus 1. Hopefully this has reduced the influence of identical phase angles on the buses. During the initial model verification, it was checked whether additional power flow was flowing between the buses (e.g. between Bus 3 and 4), but power flow was observed between them. However, it was observed that the transmission lines themselves generated a considerable amount of reactive power which had to flow out of the model through the grid sources at Bus 3 and 4 (and sometimes Bus 1). For low line loadings, transmission lines will generate reactive power [49], in contrast to higher line loadings when the lines will consume reactive power. The reactive power generation is causing a higher current flow through the lines before fault initiation. It is assumed that this phenomenon is not influencing the results by a large amount, as the line loadings during faulted conditions are very different. This may have to be researched though.

It is important to emphasize that the PLL implementation in the inverter control has been modified, such that it no longer functions as a traditional phase locked loop. The reason for this choice was based on observations from testing, showing that the PLL had major difficulties to operate as intended during severe voltage drops on the inverter terminals. Due to the distorted non-sinusoidal voltage during the faulted period, the PLL was confused and the estimation of the frequency and the phase angle went chaotic. Thus, it was decided to make the PI controller of the PLL infinitely slow ($K_P = 10^{-8}$ and $T_I = 10^8$ s) such that the angular frequency estimation was kept constant. The phase angle would therefore have to be set manually to ensure proper grid synchronization. This is a cumbersome way of obtaining grid synchronization, and ideally the PLL should be able to handle the voltage distortions such that this shortcut is avoided. With the phase angle held constant, the inverter may lose synchronization with the grid if potential phase jumps occur, for instance during the fault initiation. Also if there is a change in the grid frequency, this solution cannot be used. However, during the simulations performed in this thesis, the frequency and phase angle of the grid sources was kept constant, and it was considered acceptable to do this modification.

Line models were only included on the the 420 kV voltage level. In reality there should be line models for the 33 kV grid, and the ignored 132 kV grid between the 33 kV and 420 kV. This choice may also have influenced the results to some extent, yet no major differences are expected. Additionally, the grid topology in this model is radial and simple. To cover a greater variety of grid topologies, meshed grids and parallel lines should be studied as well.

The fact that the maximum rating of the total generation connected to Bus 1 never exceeded 36 MVA is a large contributing factor associated with the results obtained from this model. The original aim was to develop an equivalent to one of the wind farms at Fosen, and study distance protection with the short circuit current contribution from a complete wind farm connected to Bus 1. This would have been more comparable to the situation at Fosen, and the results would have been more valuable. Since the short circuit current contribution increases with the number of wind turbines, the simulation results (from Simulation set 2 and 3) are closely linked with the total generation rating of 36 MVA. In other words, the results presented with inverter % of total generation in Simulation set 3 are not general, but tied to the generation rating of 36 MVA. For instance, if a total rating of 200 MVA would have been connected to Bus 1, the simulation results would have been expected to turn out differently, most likely to the distance protection's favor. It should be noted that PSCAD Educational has a limitation of 200 electrical nodes, limiting the number of inverters allowed in the model to about 14. PSCAD Professional would be needed to increase the number of inverters, yet the simulation duration increases rapidly with more inverters. Thus, it would be better to develop a single wind farm equivalent model to obtain higher power ratings.

6.2 Discussion of the Results

6.2.1 Simulation set 1

With only one single inverter supplying Bus 1, the Relay 1 fault detection was not satisfactory. The Relay failed to trip for all fault resistances larger than or equal to 0.01 Ω, and the tripping of the lowest fault resistances were delayed significantly. None of the tripping times were within the requirement of 0.1 s, given by Statnett's specifications in FIKS [41]. The fact that Relay 1 would experience difficulties, but not Relay 2, was expected based on the reasoning in [6].

The relay tripping was the most successful for lower values of the fault resistance. This was expected, as for higher fault resistances, the more severe the fault impedance error measured by the relay on the inverter side of the line [6].

The measured fault impedance by Relay 1 did only converge for the fault resistance of 10 Ω. This result is most likely linked to the less severe voltage drop

such that the inverter control avoided heavy distortion and generated a sinusoidal current output (Figure 45). Note that even though the fault impedance converged, the relay did not detect the fault. The reason for the very high negative reactance value, even though the fault resistance was purely resistive may be due to different phase angles of the short circuit currents, making the resistance appear reactive [6]. The In all the other cases, the fault impedances did not converge, and the patterns are hard to explain.

An summarized tendency based on the results from Simulation set 1 is that fault detection by the inverter side relay (Relay 1) is harder for higher fault resistances.

6.2.2 Simulation set 2

Similarly, for the case with ten inverters supplying Bus 1, the Relay 1 tripping times is still not satisfactory. The results are relatively similar compared to Simulation set 1, yet the main difference is that Relay 1 was able to trip for the fault resistance of 0.01 Ω this time. Thus, relay performance seems to have increased slightly, which was expected as they provide a higher short circuit current contribution. Still, all of the tripping times are above the requirement of 0.1 s given by Statnett.

6.2.3 Simulation set 3

With the infeeder connected, and the share of inverter generation being varied, the Relay 1 tripping times were satisfactory for some of the scenarios. The relay had acceptable tripping times for all scenarios with a fault resistance R_{fault} of 1 Ω or less, and an inverter share of 50% or less. For inverter shares of 70% or above, almost all the scenarios lead to undesirable tripping times or no tripping at all. Additionally, one can observe that the likeliness of no tripping increases with both the fault resistance and the inverter % share. There is also a clear tendency that the tripping times increase with the inverter % share. Based on these results, it is expected that distance protection relays will suffer in performance from increasing fault resistances and inverter shares.

The reason for the lowest tripping times for fault resistances R_{fault} of 0.1 and 1 Ω may be due to a lower voltage drop, causing a more stable and sinusoidal voltage waveform, making it easier for the relay to estimate the fault impedance.

It is expected that the obtained results depended heavily on the total constant power rating of 36 MVA, the fault location set to the center of the line, and the inverter control. Thus, it is not possible to give a general answer to the original problem; "Are there indicators one can point to for determining when distance protection relays will start experiencing performance issues due to the

increasing share of inverter interfaced generation?". More research is needed to be able to give accurate answers.

6.2.4 Simulation set 4

When all the inverters were disconnected, and the influence of the ratio of the short circuit current contributions from the two ends of the line was studied, the Relay 1 fault detection was again only satisfactory for some of the scenarios.

The relay had harder times tripping satisfactorily for higher fault resistances, and lower fault current contributions from the relay side. This was expected, based on the distance protection theory discussed in [6]. The tripping times increased with a lower fault current contribution, yet remained relatively constant for the different fault resistances. Likeliness of no tripping at all increases with both the fault resistance and the current ratio.

The relay was able to trip satisfactorily for fault resistances R_{fault} of 0.1 Ω or less, with up to 73.4 times higher short circuit current contribution from the other side. This number cannot be used directly as the steps between the current ratios are too large.

The results show that relay malfunction is not directly linked to the inverters, as long as the short circuit current contributions from the two ends of the line are very different in magnitude.

6.2.5 General conclusion from simulations

The simulations show tendencies for the inverter side relay to suffer from reduced performance for higher fault resistances and higher inverter shares. However, due to the assumptions and weaknesses of the model, the obtained results cannot be used to give any general statement regarding the performance of distance protection in a grid with inverter interfaced generation.

6.3 Discussion of additional topics of interest

Some important topics which have not been covered by the simulations of this thesis, yet is critical to study as well, will be discussed briefly in this section.

6.3.1 Pilot distance protection

Despite Statnett's request of studying classic distance protection in this thesis, their distance protections are improved with pilot protection communication.

This is expected to significantly improve the distance protection's ability to operate successfully in a grid with inverter interfaced generation. As pilot distance protections provide a communication cable between the two relays on each of the line ends, a tripping signal can be sent to the inverter side relay from the grid side relay when e.g. a zone 1 fault is detected by the grid side relay. Based on the assumption that only the short circuit current contributions from the two sides are the contributing factor to distance protection malfunctioning (Simulation set 4), it can be deduced that inverter interfaced generation may only pose difficulties for one of the two relays protecting a line. Thus, if one of the relays detects a zone 1 fault without problems, pilot distance protection will make the other relay trip as well. Pilot distance protection is therefore believed to perform much better than classic distance protection.

However, pilot distance protection is not expected to free of problems. If a fault appears on the line, but in zone 2 of the grid side relay, the tripping of the inverter side relay will be delayed to the zone 2 delay (350 ms), given that the inverter side relay is not able detect faults, even though the fault was within zone 1 of that relay. In other words, this results in delayed tripping times. Additionally, faults very close to the relays may cause directional problems, potentially making the relay mistreat forward facing faults with backward facing faults, and vice versa. Under such circumstances, a backward facing fault may be treated as a forward facing fault, making the fault appear in zone 1 (e.g for the grid side relay) also causing tripping for the inverter side relay even though the relay should not have tripped. This leads to too early tripping of neighboring relays, such that more than the faulted line is disconnected during the fault. Note that this argumentation has not gone into details, and that solutions for such problems may already have been implemented in the relay algorithms. Direction determination will be discussed in greater detail in the upcoming paragraph.

6.3.2 Direction determination - polarisation

More advanced distance protections may have added features such as improved direction determination to better deal with faults located very close to the relays.

Self-polarisation is inherent in basic distance protection and relies on the polarity of the fault loop voltage, or the measured fault impedance [19]. A pre-requisite for this is an inductive fault impedance, which poses problems for series compensated lines. Self-polarisation is also weak for faults so close to the relay when the fault loop voltage is close to zero. The dead zone voltage for conventional relays are in the area of 0.1 V [19], which means that faults resulting in a fault loop voltage of less than 0.1 V cause insecure directional decision. Thus, it is desirable to have some form of improved direction determination for the relays.

Cross-polarisation is an improved direction determination method which utilizes healthy phases. Since most short circuits only impact one or two of the phases, it is possible to use the voltages of the healthy phases [19]. Relays with cross-polarisation will use the short circuit current of the faulted phase, and the voltage of a healthy phase to determine the direction of the fault.

It is also possible to utilize memorized voltages in addition for improving the direction determination for three-phase faults. Numerical relays have the advantage to be able to store measurements for as long as desired, for the use of determining the fault direction. The high directional sensitivity of 0.1 V required previously to minimize the dead zone, is not necessary for numerical relays because a voltage memory is always available [19]. Thus, for numerical relays, direction determination problems are not expected. Bear in mind that this reasoning is not directly evaluating the influence of inverter interfaced generation.

6.3.3 Subsequent tripping

The reasoning in this paragraph is solely based on own thoughts.

Assuming that the short circuit current contribution ratio based on the currents from the two line ends is the main contributing factor to reduced distance protection performance, it would have been interesting to study the impact of breaker tripping in the model. Considering a single line with distance protection relays on both line ends, if at least one of the two relays trips its breaker, it may improve the fault detection for the other relay. Based on the results from Simulation set 4, it was observed that a higher short circuit current contribution from the right side lead to reduced relay performance on the left side relay. However, if the right side relay (which is expected to trip successfully due to the higher short circuit current contribution from that side) trips its breaker, there will no longer be any current contribution from that side. This may improve the estimated fault impedance location of the left side relay significantly since all the fault current now comes from the left side. In other words, the impact of higher fault resistances may be less severe, and even the side with the lowest short circuit current contribution may accurately estimate the fault impedance, as long as the neighboring relay on the opposite side trips successfully. This reasoning is obviously assuming stable sinusoidal electrical signals, not causing any additional complications.

6.3.4 The ENTSO-E report

Statnett's request for the study was based on an ENTSO-E report published in April 2019 [4]. The main conclusion from the report was that distance protection relays could suffer the greatest from a high penetration of inverter interfaced

generation. The main problems addressed were related to the impedance measurement and the faulty phase selection.

The impedance measurements been covered in this thesis, visualized in the impedance diagrams presented in the "Results" chapter and the appendices. However, the problems related to faulty phase selection has not been covered due to the limitations of the inverter model. The ENTSO-E report states that errors in faulty phase selection could be expected for relays based on superimposed quantities, however, it depends on the negative sequence strategy of the inverter and the distance protection algorithm. Such problems related to unbalanced faults and analysis of symmetrical components will have to be studied in future work.

7 Conclusion

In this thesis, the performance of distance protection in a grid with inverter interfaced generation has been studied through simulations in PSCAD. The work has been conducted in cooperation with Statnett, who has requested the need for research on this topic based on a recently published ENTSO-E report. The Fosen Wind project in Norway is the practical example of where protection issues are expected due to the large penetration of wind power. The main problem has been defined as "Are there indicators one can point to for determining when distance protection relays will start experiencing performance issues due to the increasing share of inverter interfaced generation?".

The PSCAD model has been developed from scratch and consists of a Grid-feeding inverter model (representing a 3.6 MVA type 4 wind turbine), a grid, and distance protection relays. Essentially, the model is a transmission line with inverters connected to the left end (Bus 1 / Inverter side) and a grid equivalent connected to the right end (Bus 2 / Grid side), with distance protections installed on both ends of the line. The model development has been described in detail and most of the system parameters have been provided. A verification of the model has been included as well.

Four sets of simulations have been executed with a balanced three-phase to ground fault located on the center of the line. The fault resistance has been varied, ranging from 0.1 mΩ to 10 Ω. The main focus has been to obtain results for the inverter side relay's impedance diagrams and tripping times.

Simulation set 1 showed that a single inverter connected to Bus 1 caused unsatisfactory tripping for the inverter side relay. The performance was generally worse for higher fault resistances, causing no tripping at all.

Simulation set 2 showed that ten inverters connected to Bus 1 also caused unsatisfactory tripping for the inverter side relay. However, the relay performance was slightly improved compared to Simulation set 1. Again, the relay performance was worse for higher fault resistances.

Simulation set 3 showed that the share of inverter interfaced generation (opposed to synchronous generation) connected to Bus 1 influences the inverter side relay performance. The relay was able to trip satisfactorily (within 0.1 s) for inverter shares of 50% or less, for fault resistances of 1 Ω or less. With few exceptions, there were no satisfactory trippings for inverter shares of 70% or more. The relay performance was reduced for increasing inverter shares of the total generation and increasing fault resistances. The instances which caused no tripping at all, were linked to a combination of higher inverter shares and higher fault resistances, yet the fault resistance had the greatest impact.

Simulation set 4 showed that the ratio of the short circuit current contributions from each side of the line influenced the relay performance. The relay located on the side with the lowest short circuit current contribution suffered more the greater the short circuit current contribution from the other side. For similar short circuit current contributions from the two sides, both relays were able to trip correctly and fast. For higher short circuit current contributions from Bus 2, the relay located at Bus 1 suffered from reduced performance, especially for higher fault resistances. Still, the relay was able to trip satisfactorily for fault resistances of 0.1 Ω or less, when the short circuit current contribution from the other side was up to roughly 70 times greater.

The distance protection relay located on the grid side of the line did not experience any problems during any of the simulations.

However, due to the model assumptions and weaknesses, the obtained results cannot be used to give any general statement regarding the performance of distance protection in a grid with inverter interfaced generation. Thus, the main problem cannot be answered. More research is needed to be able to give accurate statements related to which problems should be expected and under which circumstances they will occur. The model should be developed further, with an improved inverter model and distance protection algorithm, such that unbalanced faults can be studied as well.

8 Further work

An improved inverter model is necessary for further studies. It should be aimed to develop an inverter model with a Grid-supporting capability, such that the short circuit current is more comparable to future oriented inverters with grid code requirements for Fault Ride Through operation. Thus, grid code requirements will have to be studied in greater detail, and the inverter control should be developed such that these requirements are met during faults. Additionally, the inverter should be able to handle unbalanced conditions such that the inverter operates reliably also under such circumstances. For instance, the inverter control system should be able to extract the positive and negative sequence components from the voltage and current signals, and include separate control for both of these components. In such a way, the inverter should be able to control its current output to a much greater extent during unbalanced conditions, such that also unbalanced faults can be studied. Note that positive and negative sequence extraction may introduce time delays worsening the dynamic response of the inverter control. Most likely, the Phase Locked Loop of the inverter control will also perform better with separation of positive and negative sequence components, and the shortcut in this thesis should be avoided.

The distance protection algorithm developed in this thesis is very basic, and should be improved to better compare to modern numerical distance protection relays. Added features such as cross-polarisation, memorized voltages and currents, and superimposed quantities should be considered to improve the performance of the relay. Additionally, pilot distance protection relays should be studied as well since Statnett is using such relays today and they are expected to improve the situation significantly. The selected parameters of the voltage and current transformers (VTs and CTs) should be chosen more carefully, such that they have a more similar behaviour to the actual transformers being used today. The zones of the relay can be justified better, especially the resistive reach, and additional zones can be added to support fault detection in backward direction and further in forward direction.

Further studies should cover a greater variety of fault types and fault locations. The influence of unbalanced short circuits should be studied, demanding in-depth analysis of positive, negative and zero sequence components in the system. This is again closely linked with the inverter control and the distance protection algorithm. For instance, the ENTSO-E report stated that inverters with the strategy of negative sequence suppression could affect distance protection relays relying on the phase angle between the negative and zero sequence components. Different fault types may lead to different protection issues, and therefore should all fault types be studied before coming to a conclusion. The fault location should also be varied throughout the tests. The fault location plays an important role in the zone determination of the relays as their estimated fault impedances may be inaccurate. Thus, faults closer to the border

between two zones (e.g zone 1 and zone 2) may more frequently be misinterpreted to appear in the wrong zone. Additionally, the direction determination of the relays should be tested by locating faults very close to the relays. Note that this can be hard to verify in a simulation program as measurement inaccuracies may be hard to emulate. This is another reason to dive deeper into the parameters of the voltage and current transformers.

The influence of different grid topologies should also be examined, as more meshed-like grids and parallel lines may cause problems not observed. In contrast to the model in this thesis, line data for the lower voltage lines should also be included to make the model more comparable to the real grid. It would also be relevant to look into the influence of lower voltage levels which may have different system earthing. For example, the medium voltage level may be physically disconnected to earth due to the delta-connected side of the transformers, changing the behaviour of the zero sequence component. The choice of correct transformer parameters should also be ensured.

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Appendices

Appendix A

Additional results for Simulation set 1 are presented here. The results include the trip times for Relay 1, and additional simulation results for fault resistances R_{fault} of 0.0001 Ω and 10 Ω.

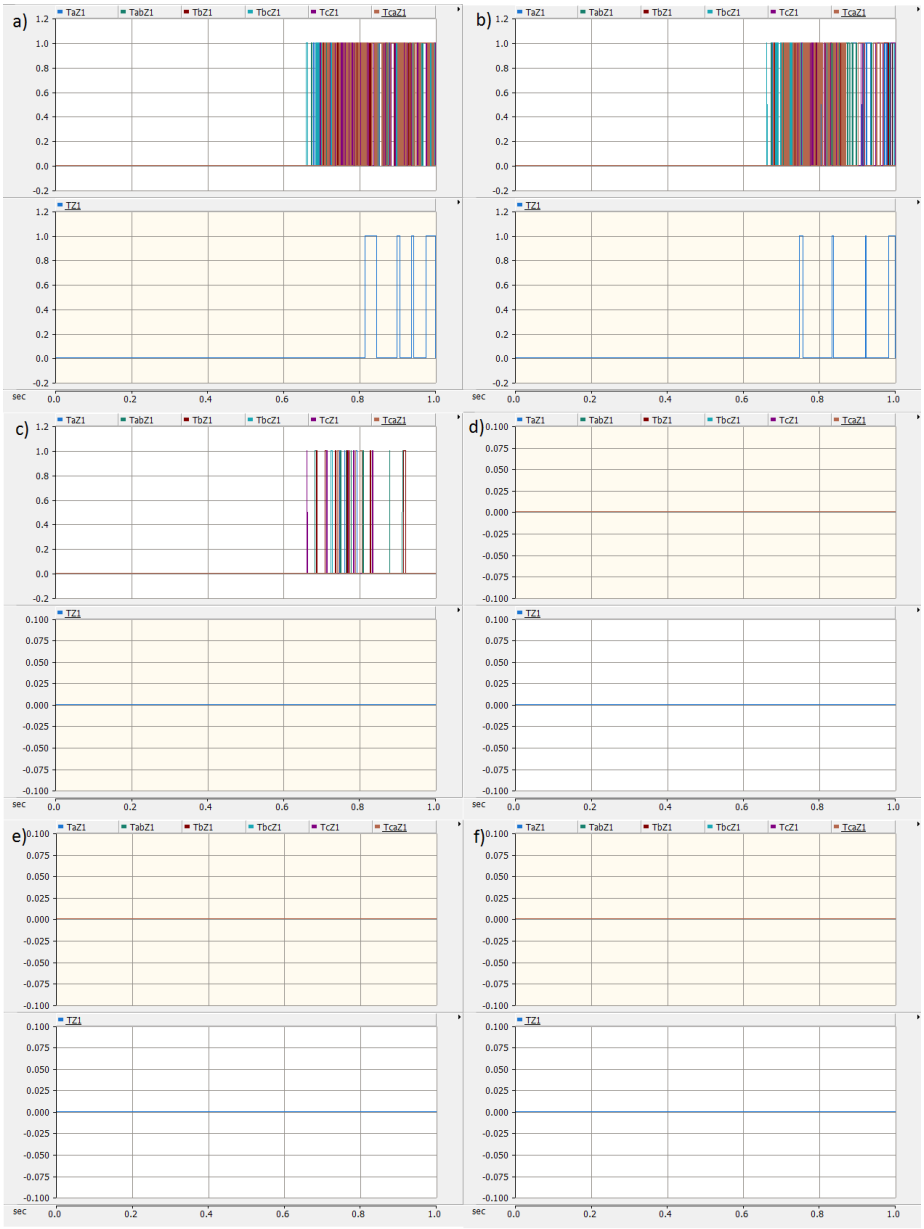

Figure 43: Relay 1 zone 1 fault detection and tripping for one single inverter connected to PCC, for different values of R_{fault}. The Infeeder is disconnected from Bus 1. The selected model parameters are given in Table 12. The trip times t_{trip} includes the 0.5 s before fault initiation.

a) $R_{fault} = 0.0001\ \Omega$ $t_{trip} = 0.8137$ s
b) $R_{fault} = 0.001\ \Omega$ $t_{trip} = 0.7462$ s
c) $R_{fault} = 0.01\ \Omega$ $t_{trip} =$ -
d) $R_{fault} = 0.1\ \Omega$ $t_{trip} =$ -
e) $R_{fault} = 1\ \Omega$ $t_{trip} =$ -
f) $R_{fault} = 10\ \Omega$ $t_{trip} =$ -

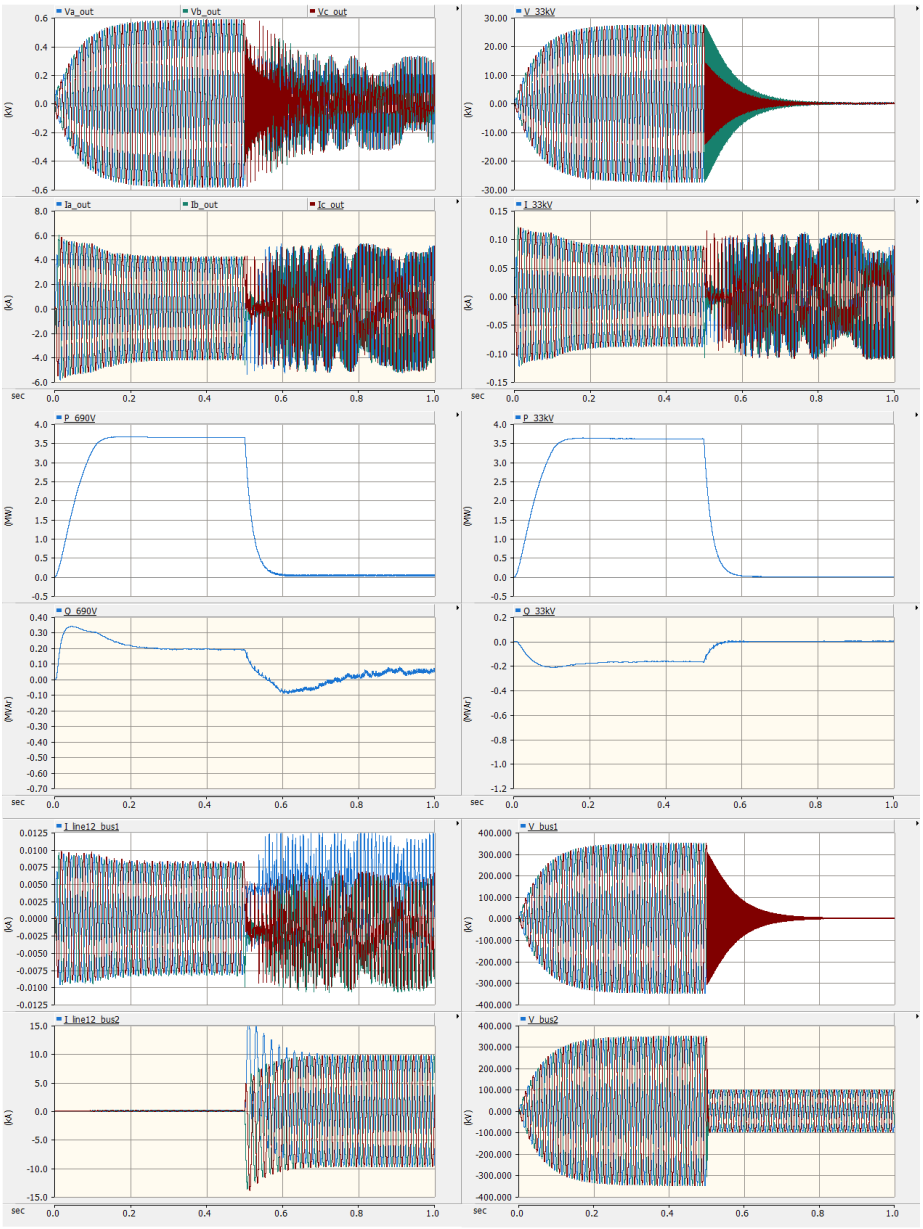

Figure 44: The inverter output at the 690V and 33 kV terminal, and the currents and voltages related to Line 12. The fault resistance R_{fault} is 0.0001 Ω.

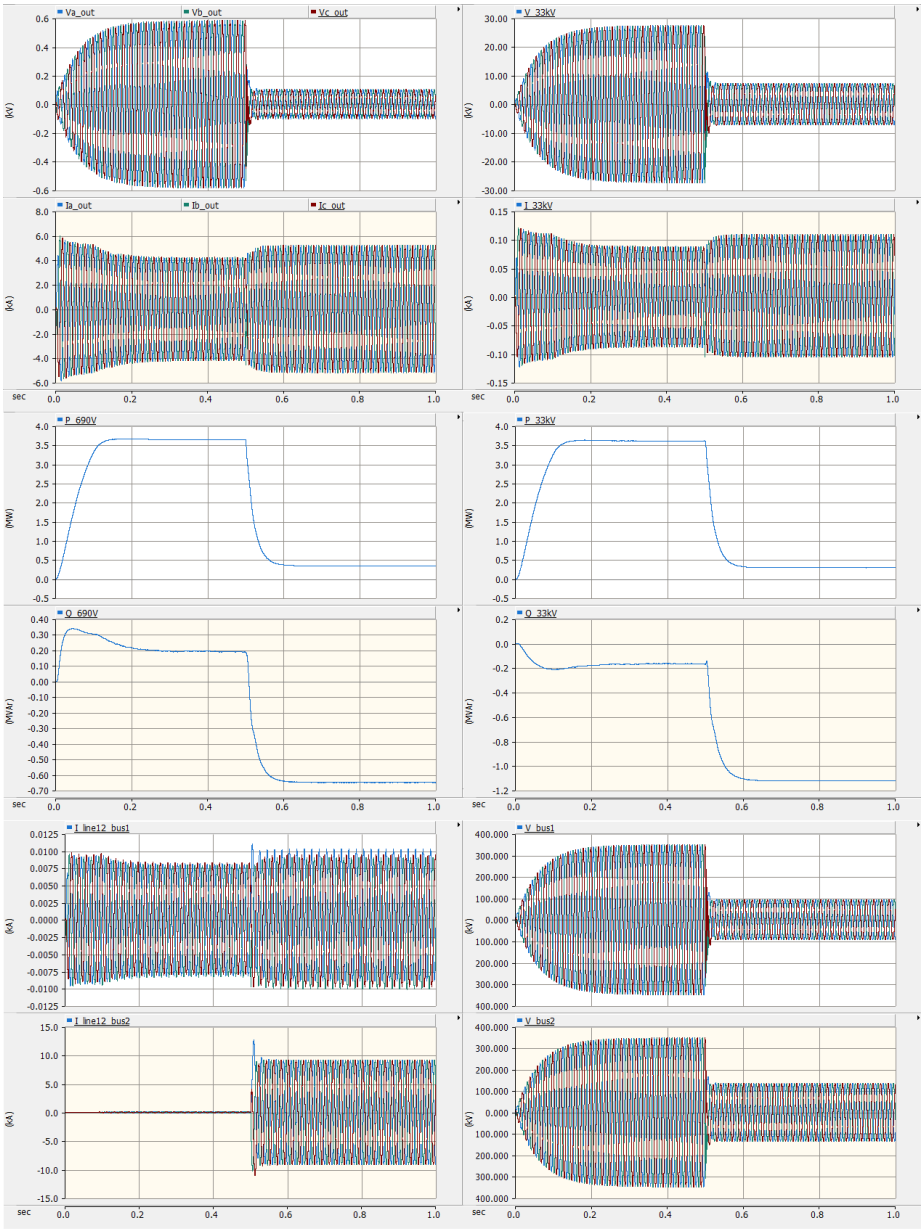

Figure 45: The inverter output at the 690V and 33 kV terminal, and the currents and voltages related to Line 12. The fault resistance R_{fault} is 10 Ω.

Appendix B

Additional results for Simulation set 2 are presented here. The results include the trip times for Relay 1, and additional simulation results for fault resistances R_{fault} of 0.0001 Ω and 10 Ω.

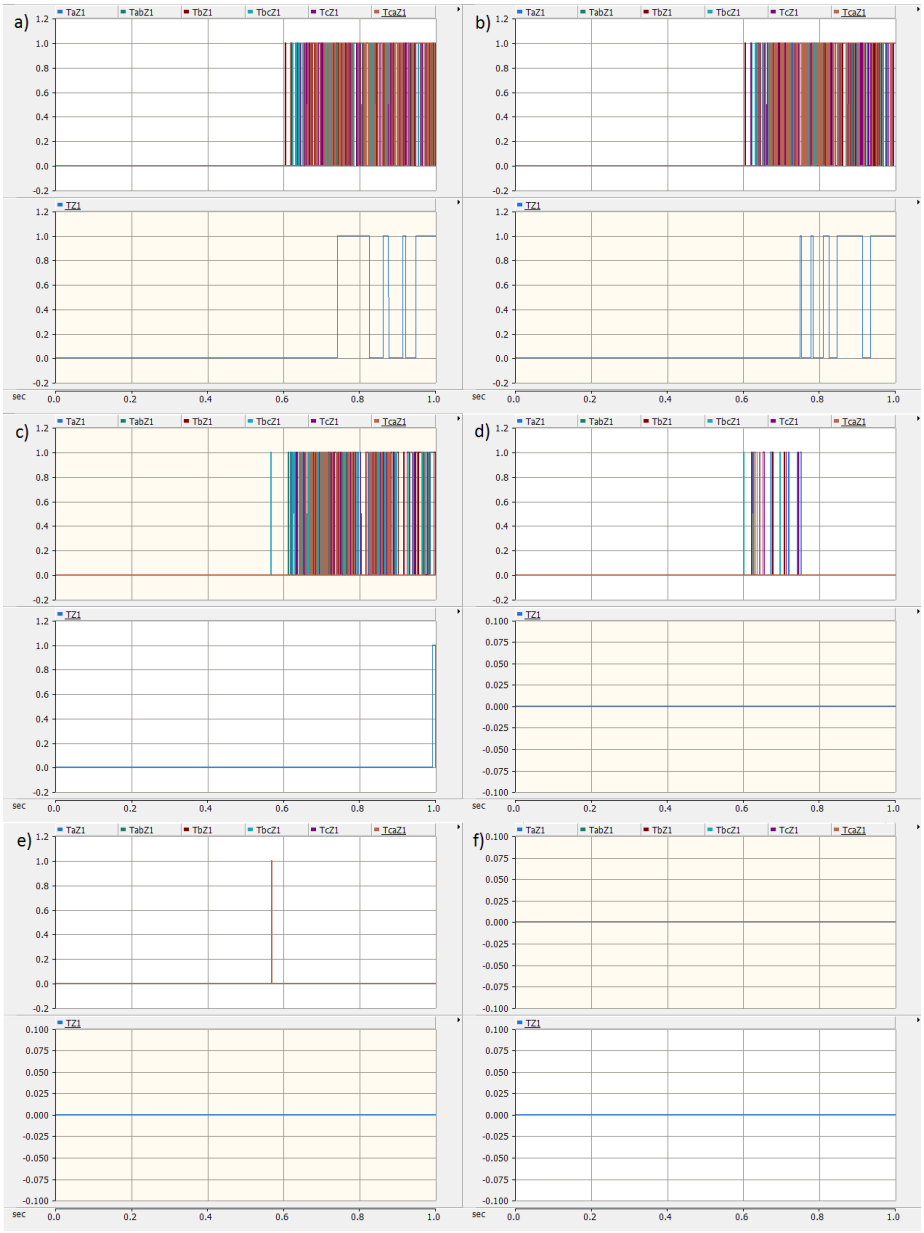

Figure 46: Relay 1 zone 1 fault detection and tripping for 10 inverters connected to PCC, for different values of R_{fault}. The Infeeder is disconnected from Bus 1. The selected model parameters are given in Table 12. The trip times t_{trip} includes the 0.5 s before fault initiation.

a) $R_{fault} = 0.0001\ \Omega$ $t_{trip} = 0.7400$ s
b) $R_{fault} = 0.001\ \Omega$ $t_{trip} = 0.7487$ s
c) $R_{fault} = 0.01\ \Omega$ $t_{trip} = 0.9900$ s
d) $R_{fault} = 0.1\ \Omega$ $t_{trip} =$ -
e) $R_{fault} = 1\ \Omega$ $t_{trip} =$ -
f) $R_{fault} = 10\ \Omega$ $t_{trip} =$ -

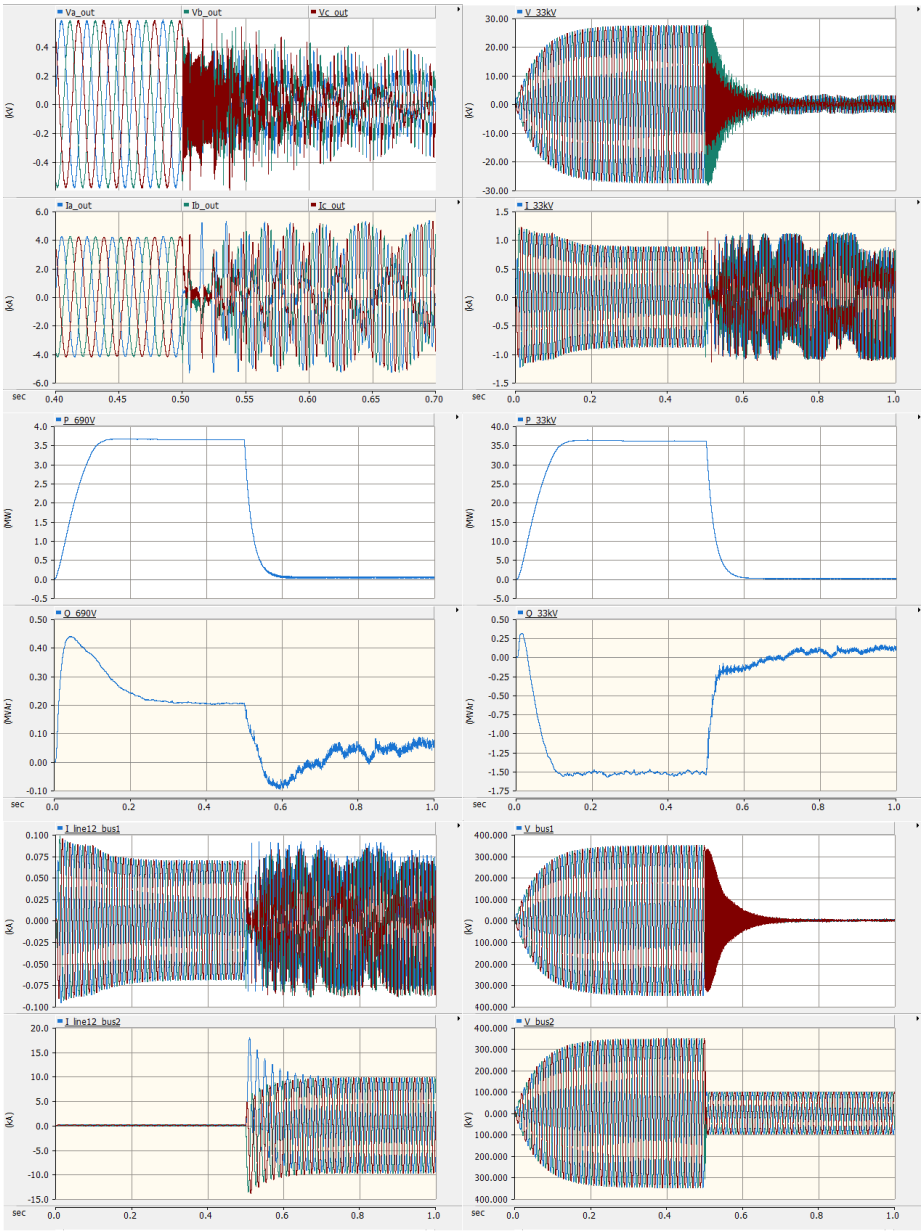

Figure 47: The inverter output at the 690V and 33 kV terminal, and the currents and voltages related to Line 12. The fault resistance R_{fault} is 0.0001 Ω.

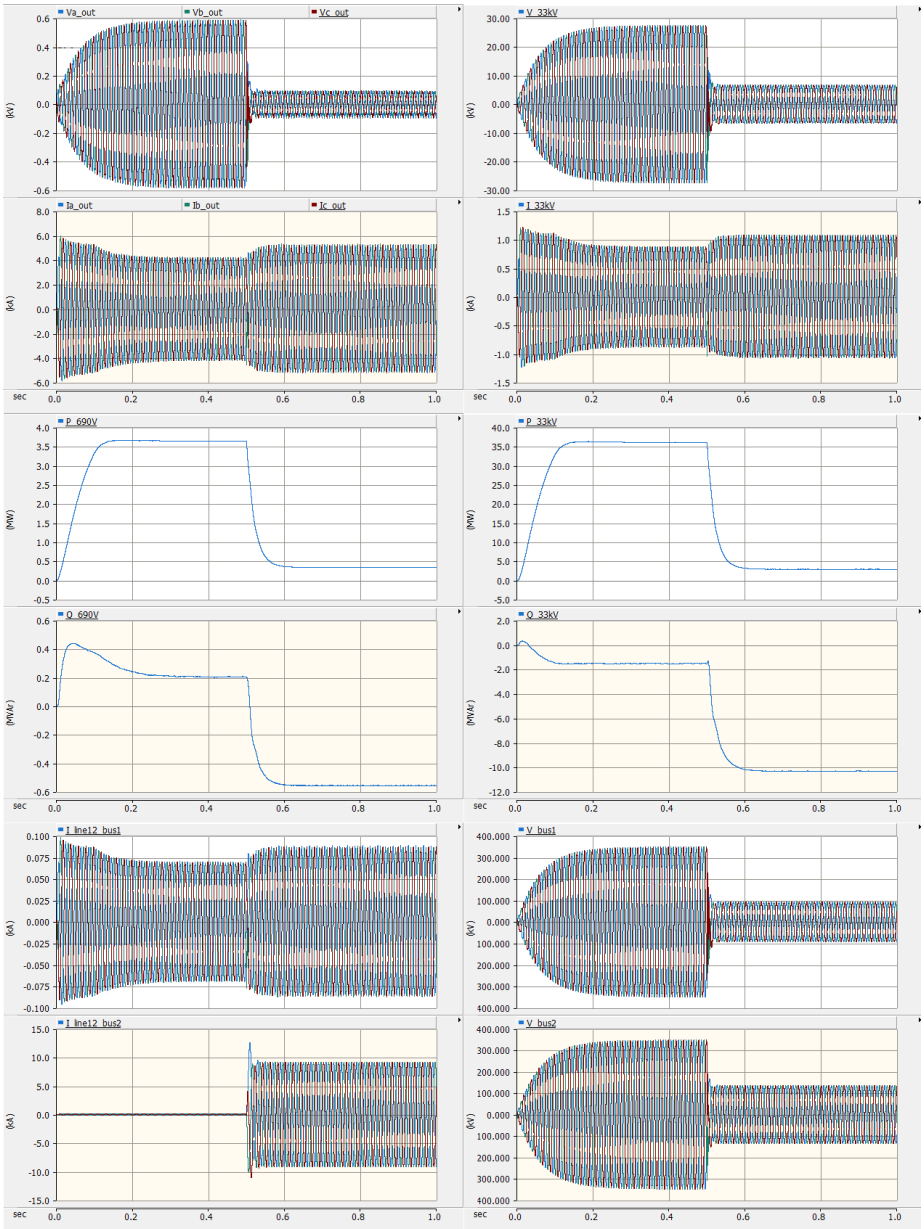

Figure 48: The inverter output at the 690V and 33 kV terminal, and the currents and voltages related to Line 12. The fault resistance R_{fault} is 10 Ω.

Appendix C

Additional results for simulation set 3 are presented here, including the fault impedance diagrams and the trip times. The diagrams for 100% inverter generation is identical to those presented in Simulation set 2 and Appendix B.

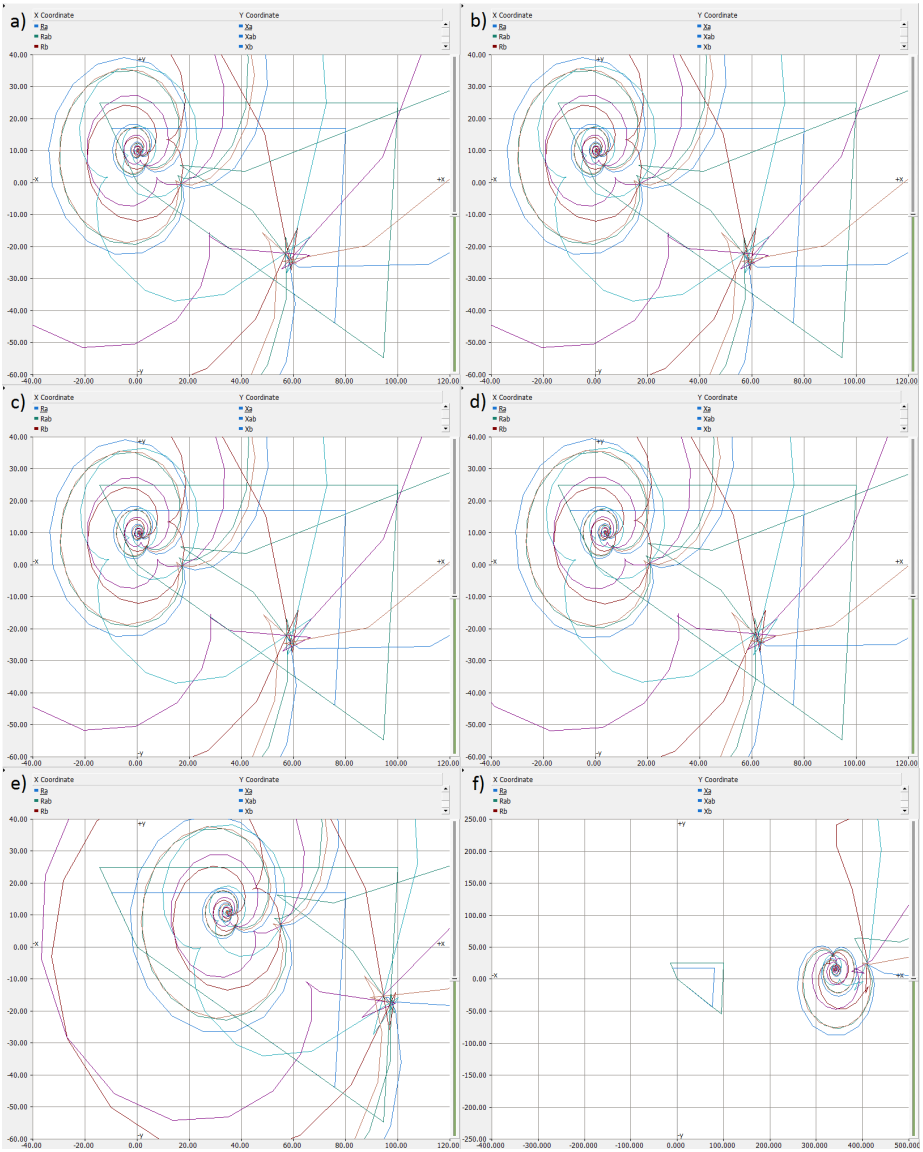

Figure 49: Relay 1 impedance diagrams for 0% inverter generation, for different values of R_{fault}. $|Z_{infeeder}|$ is set to 1156 Ω, generating a short circuit current contribution equivalent to 10 synchronous machines of 3.6 MVA at 690V. The selected model parameters are given in Table 12, except for $|Z_{infeeder}|$, and that 0 inverters were connected to PCC.

a) $R_{fault} = 0.0001\ \Omega$ $Z_a = 0.4242 + \text{j}10.03\ \Omega$
b) $R_{fault} = 0.001\ \Omega$ $Z_a = 0.4583 + \text{j}10.03\ \Omega$
c) $R_{fault} = 0.01\ \Omega$ $Z_a = 0.7659 + \text{j}10.04\ \Omega$
d) $R_{fault} = 0.1\ \Omega$ $Z_a = 3.841 + \text{j}10.12\ \Omega$
e) $R_{fault} = 1\ \Omega$ $Z_a = 34.60 + \text{j}10.89\ \Omega$
f) $R_{fault} = 10\ \Omega$ $Z_a = 342.2 + \text{j}15.90\ \Omega$

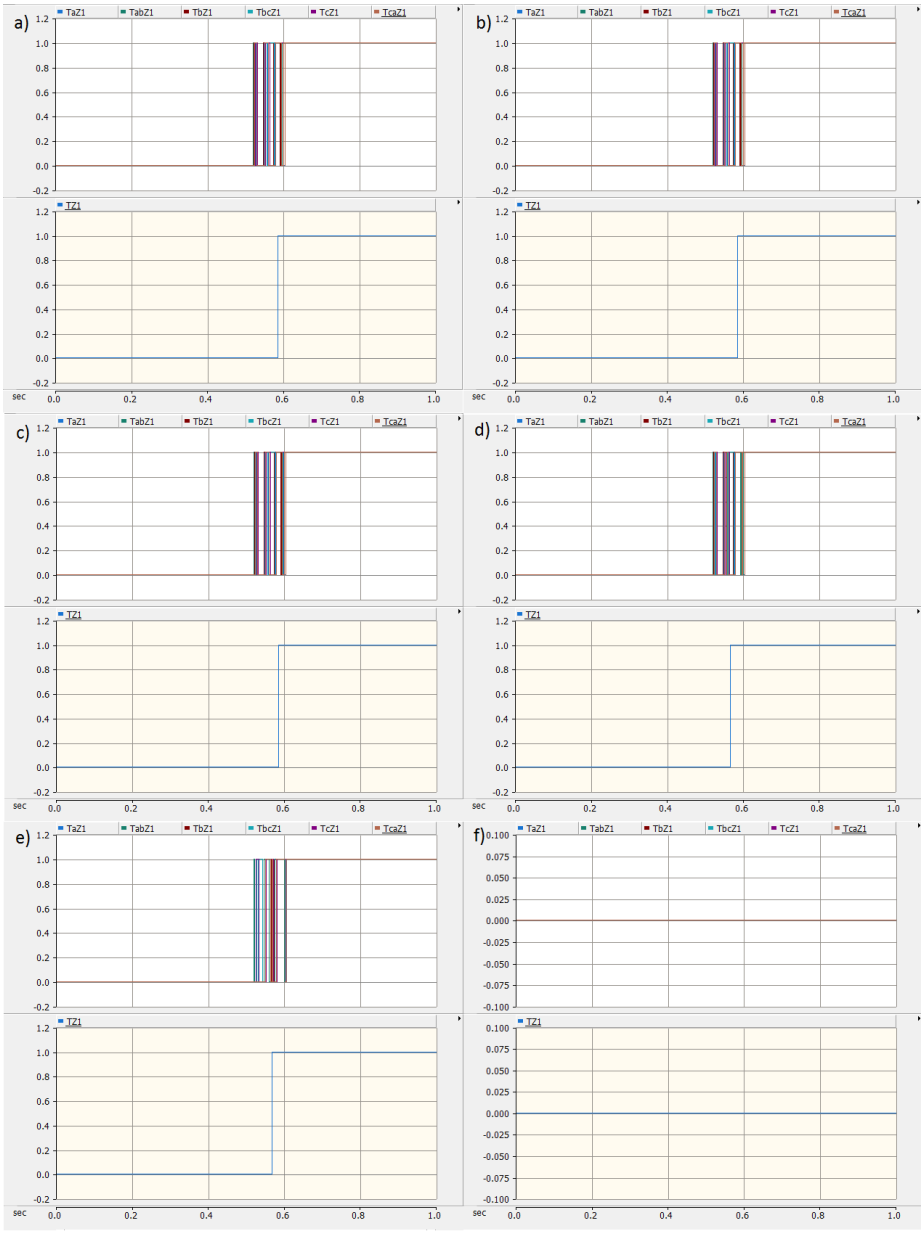

Figure 50: Relay 1 zone 1 fault detection and tripping for 0% inverter generation, for different values of R_{fault}. $|Z_{infeeder}|$ is set to 1156 Ω, generating a short circuit current contribution equivalent to 10 synchronous machines of 3.6 MVA at 690V. The selected model parameters are given in Table 12, except for $|Z_{infeeder}|$, and that 0 inverters were connected to PCC. The trip times t_{trip} includes the 0.5 s before fault initiation.

a) $R_{fault} = 0.0001\ \Omega$ $t_{trip} = 0.5837$ s
b) $R_{fault} = 0.001\ \Omega$ $t_{trip} = 0.5837$ s
c) $R_{fault} = 0.01\ \Omega$ $t_{trip} = 0.5837$ s
d) $R_{fault} = 0.1\ \Omega$ $t_{trip} = 0.5650$ s
e) $R_{fault} = 1\ \Omega$ $t_{trip} = 0.5662$ s
f) $R_{fault} = 10\ \Omega$ $t_{trip} =$ -

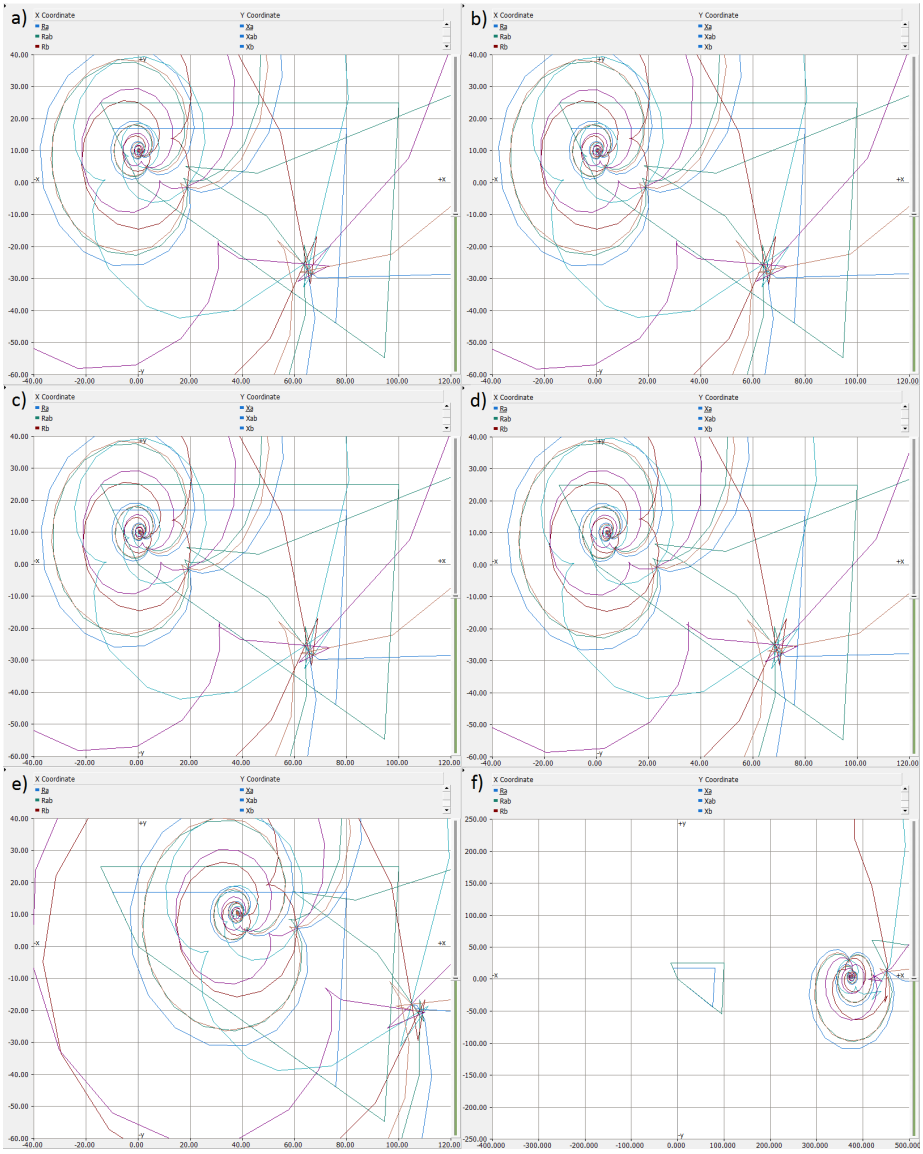

Figure 51: Relay 1 impedance diagrams for 10% inverter generation, for different values of R_{fault}. $|Z_{infeeder}|$ is set to 1284.4 Ω, generating a short circuit current contribution equivalent to 9 synchronous machines of 3.6 MVA at 690V. The selected model parameters are given in Table 12, except for $|Z_{infeeder}|$. 1 inverter was connected to PCC.

a) $R_{fault} = 0.0001\ \Omega$ $Z_a = 0.4185 + \text{j}10.03\ \Omega$
b) $R_{fault} = 0.001\ \Omega$ $Z_a = 0.4474 + \text{j}10.01\ \Omega$
c) $R_{fault} = 0.01\ \Omega$ $Z_a = 0.7891 + \text{j}10.03\ \Omega$
d) $R_{fault} = 0.1\ \Omega$ $Z_a = 4.219 + \text{j}10.11\ \Omega$
e) $R_{fault} = 1\ \Omega$ $Z_a = 38.21 + \text{j}10.52\ \Omega$
f) $R_{fault} = 10\ \Omega$ $Z_a = 375.4 + \text{j}4.616\ \Omega$

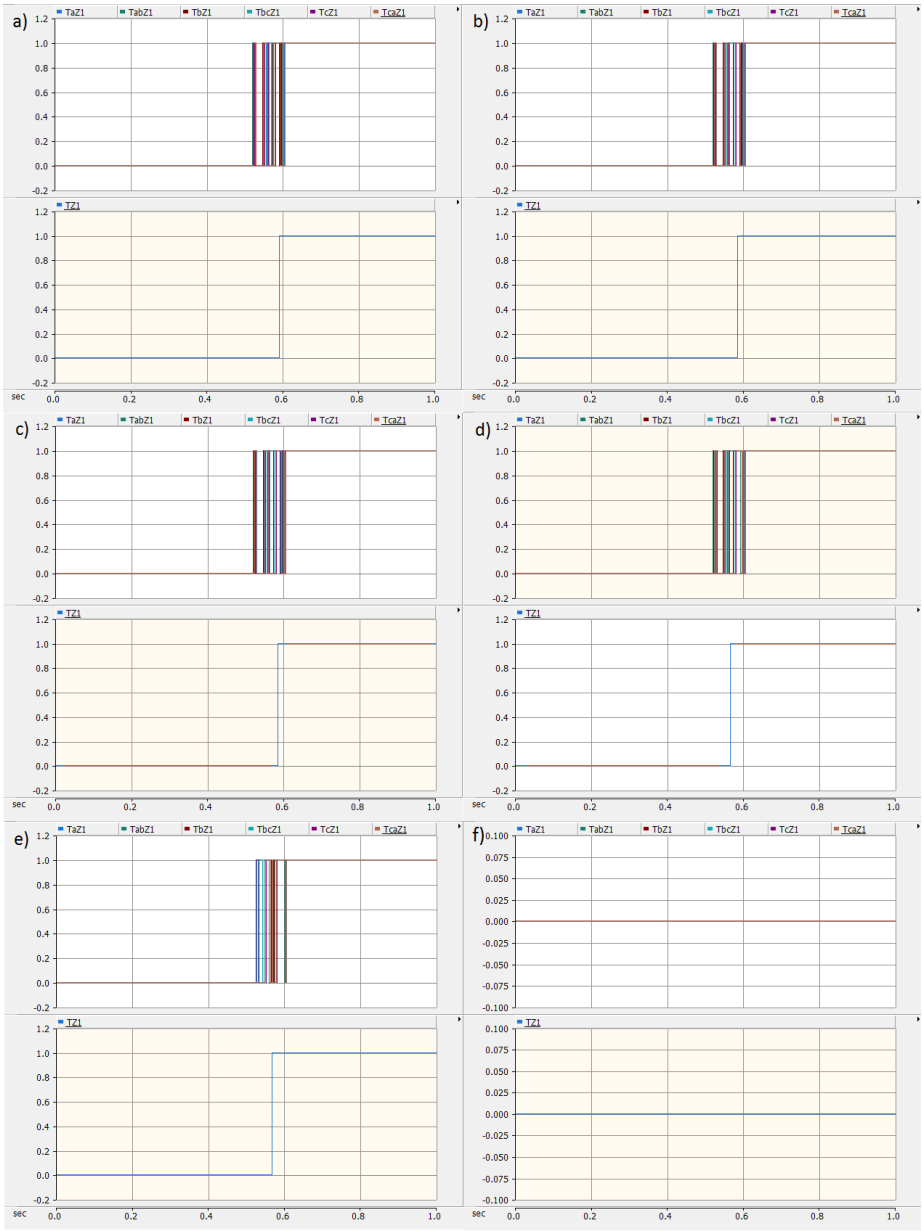

Figure 52: Relay 1 zone 1 fault detection and tripping for 10% inverter generation, for different values of R_{fault}. $|Z_{infeeder}|$ is set to 1284.4 Ω, generating a short circuit current contribution equivalent to 9 synchronous machines of 3.6 MVA at 690V. The selected model parameters are given in Table 12, except for $|Z_{infeeder}|$. 1 inverter was connected to PCC. The trip times t_{trip} includes the 0.5 s before fault initiation.

a) $R_{fault} = 0.0001\ \Omega$ $t_{trip} = 0.5900$ s
b) $R_{fault} = 0.001\ \Omega$ $t_{trip} = 0.5837$ s
c) $R_{fault} = 0.01\ \Omega$ $t_{trip} = 0.5837$ s
d) $R_{fault} = 0.1\ \Omega$ $t_{trip} = 0.5650$ s
e) $R_{fault} = 1\ \Omega$ $t_{trip} = 0.5662$ s
f) $R_{fault} = 10\ \Omega$ $t_{trip} =$ -

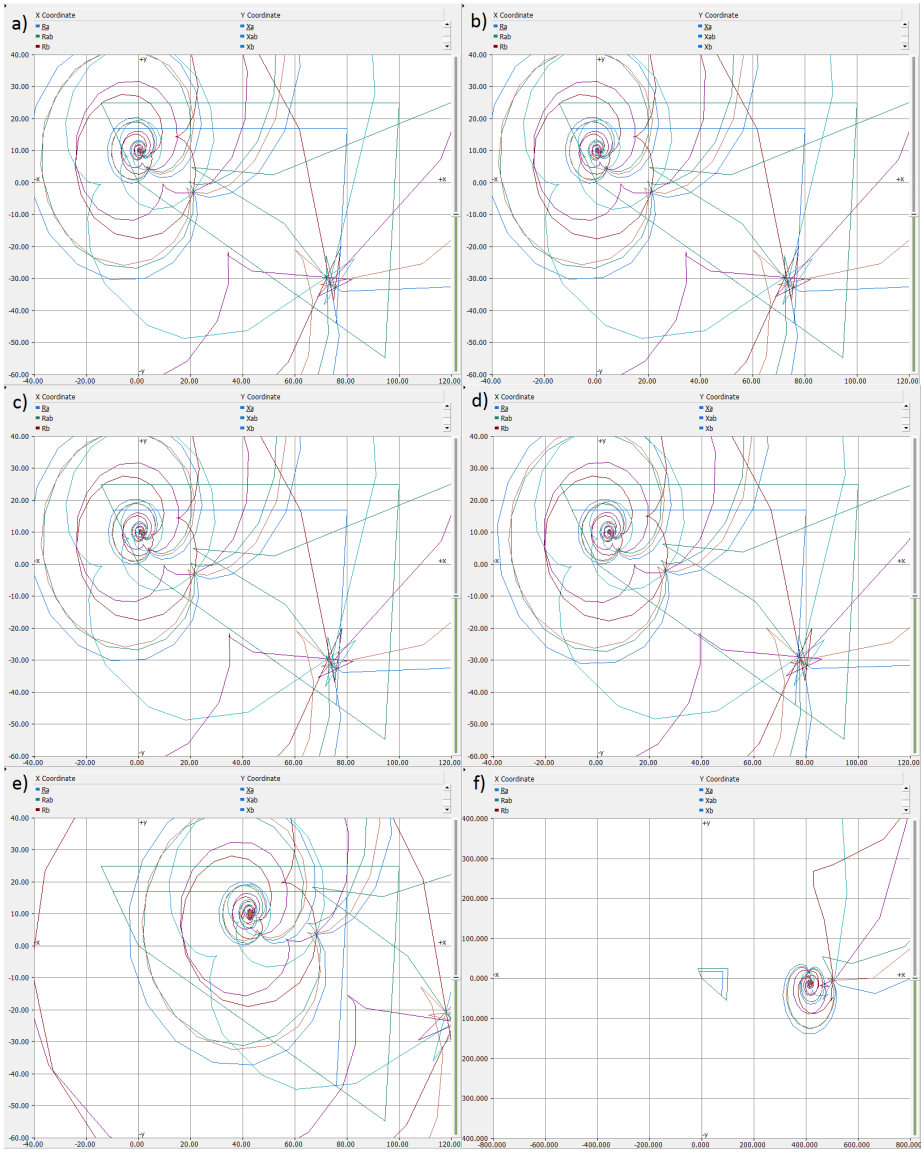

Figure 53: Relay 1 impedance diagrams for 20% inverter generation, for different values of R_{fault}. $|Z_{infeeder}|$ is set to 1445 Ω, generating a short circuit current contribution equivalent to 8 synchronous machines of 3.6 MVA at 690V. The selected model parameters are given in Table 12, except for $|Z_{infeeder}|$, and that 2 inverters were connected to PCC.

a) $R_{fault} = 0.0001\ \Omega$ $Z_a = 0.4186 + j10.03\ \Omega$
b) $R_{fault} = 0.001\ \Omega$ $Z_a = 0.4667 + j10.03\ \Omega$
c) $R_{fault} = 0.01\ \Omega$ $Z_a = 0.8433 + j10.03\ \Omega$
d) $R_{fault} = 0.1\ \Omega$ $Z_a = 4.626 + j10.10\ \Omega$
e) $R_{fault} = 1\ \Omega$ $Z_a = 42.14 + j9.564\ \Omega$
f) $R_{fault} = 10\ \Omega$ $Z_a = 414.8 - j12.16\ \Omega$

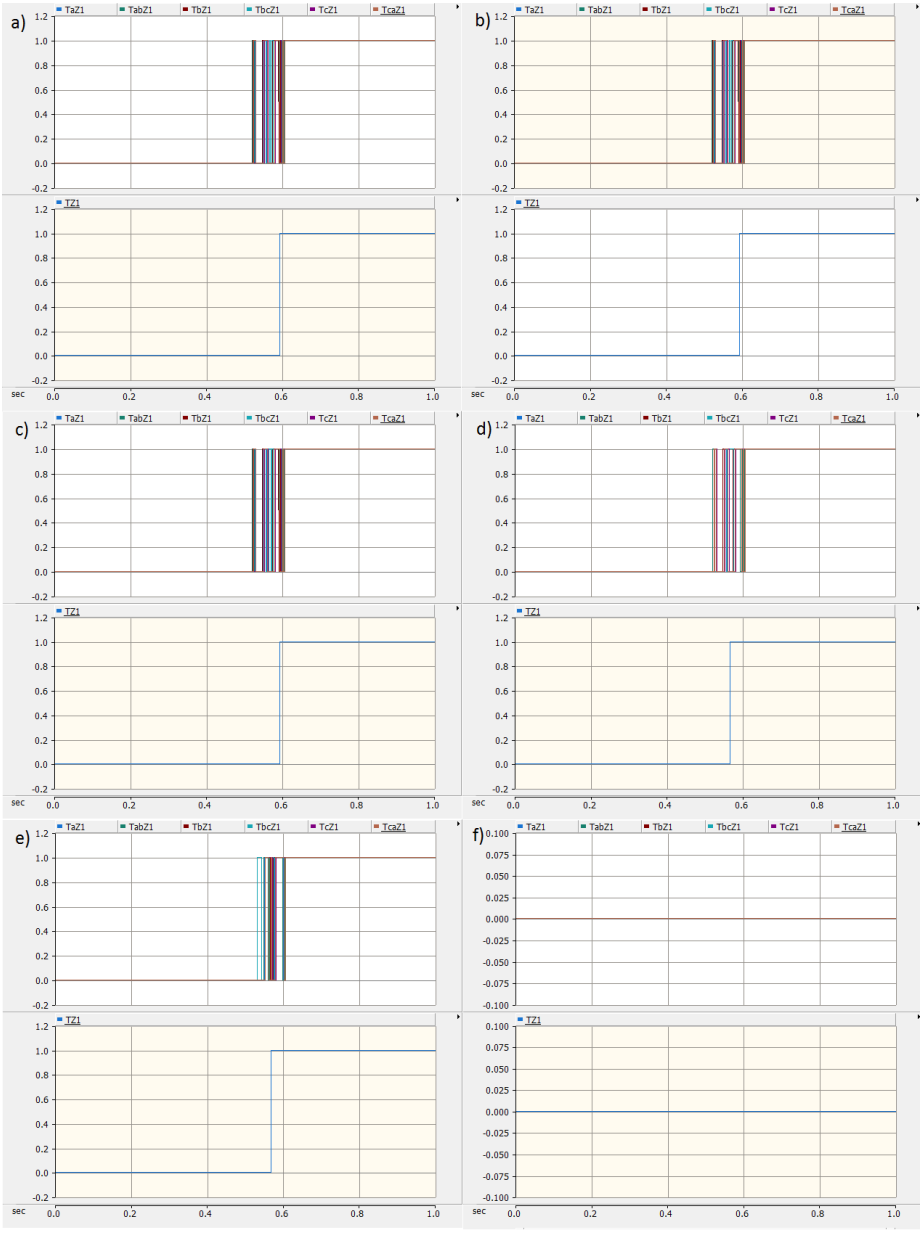

Figure 54: Relay 1 zone 1 fault detection and tripping for 20% inverter generation, for different values of R_{fault}. $|Z_{infeeder}|$ is set to 1445 Ω, generating a short circuit current contribution equivalent to 8 synchronous machines of 3.6 MVA at 690V. The selected model parameters are given in Table 12, except for $|Z_{infeeder}|$, and that 2 inverters were connected to PCC. The trip times t_{trip} includes the 0.5 s before fault initiation.

a) $R_{fault} = 0.0001\ \Omega$ $t_{trip} = 0.5912$ s
b) $R_{fault} = 0.001\ \Omega$ $t_{trip} = 0.5912$ s
c) $R_{fault} = 0.01\ \Omega$ $t_{trip} = 0.5912$ s
d) $R_{fault} = 0.1\ \Omega$ $t_{trip} = 0.5650$ s
e) $R_{fault} = 1\ \Omega$ $t_{trip} = 0.5675$ s
f) $R_{fault} = 10\ \Omega$ $t_{trip} =$ -

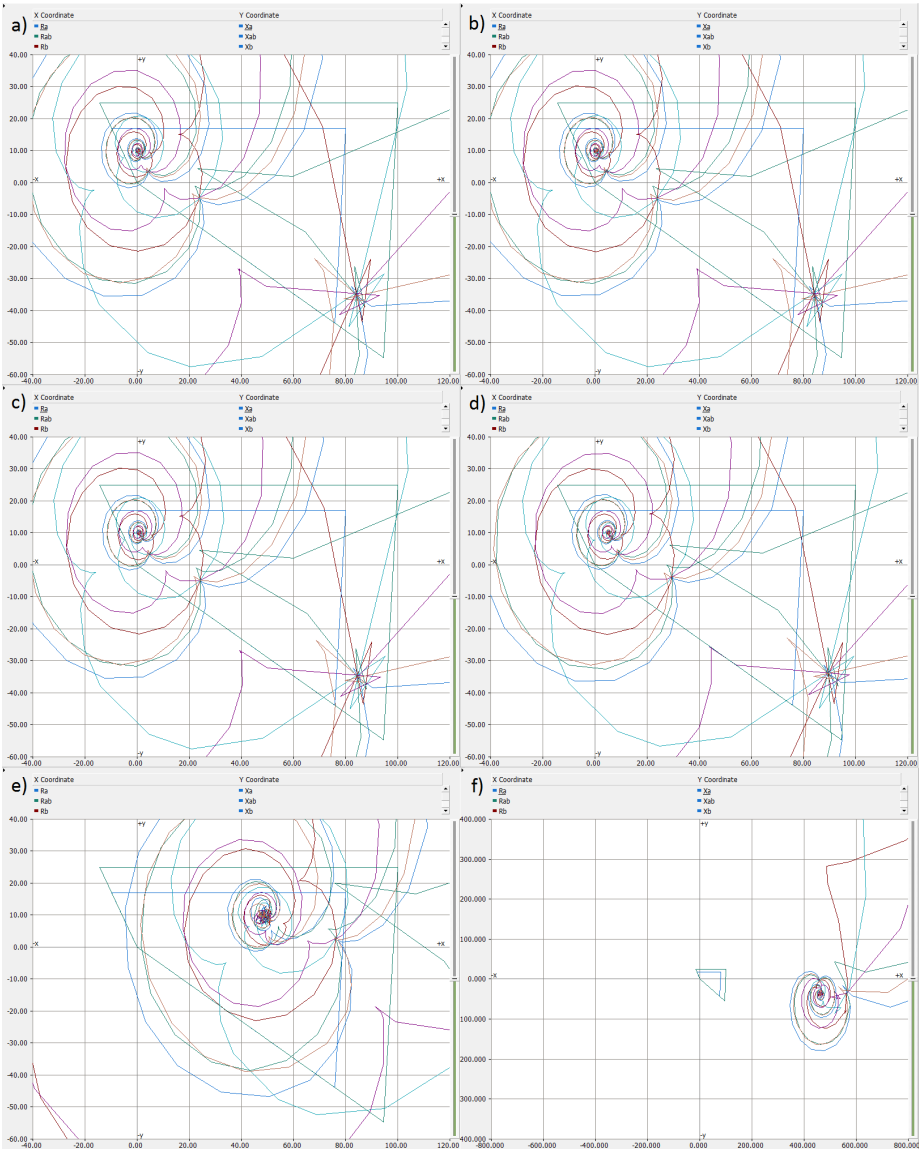

Figure 55: Relay 1 impedance diagrams for 30% inverter generation, for different values of R_{fault}. $|Z_{infeeder}|$ is set to 1651.4 Ω, generating a short circuit current contribution equivalent to 7 synchronous machines of 3.6 MVA at 690V. The selected model parameters are given in Table 12, except for $|Z_{infeeder}|$, and that 3 inverters were connected to PCC.

a) $R_{fault} = 0.0001\ \Omega$ $Z_a = 0.4174 + j10.03\ \Omega$
b) $R_{fault} = 0.001\ \Omega$ $Z_a = 0.4320 + j10.01\ \Omega$
c) $R_{fault} = 0.01\ \Omega$ $Z_a = 0.8826 + j10.03\ \Omega$
d) $R_{fault} = 0.1\ \Omega$ $Z_a = 5.248 + j10.07\ \Omega$
e) $R_{fault} = 1\ \Omega$ $Z_a = 48.80 + j11.03\ \Omega$
f) $R_{fault} = 10\ \Omega$ $Z_a = 462.4 - j37.56\ \Omega$

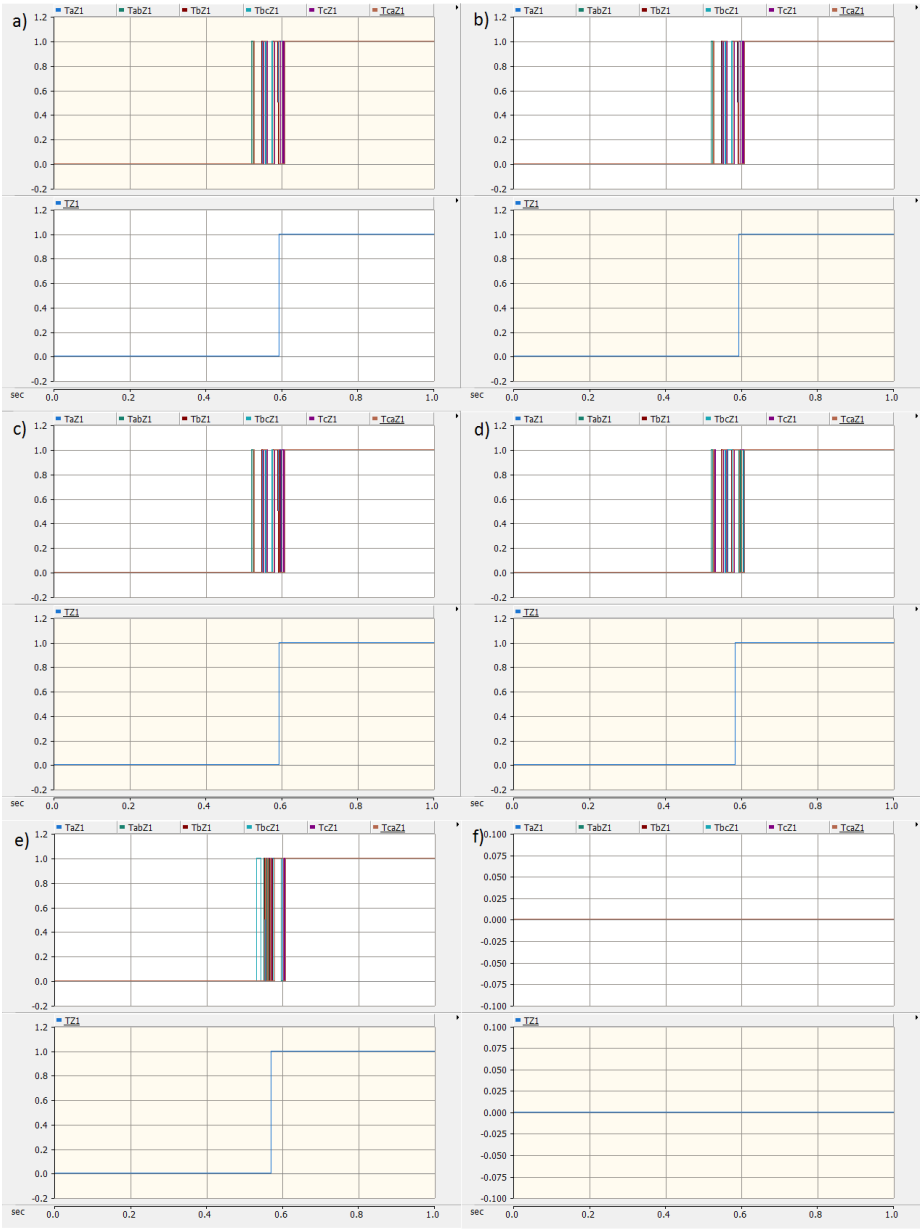

Figure 56: Relay 1 zone 1 fault detection and tripping for 30% inverter generation, for different values of R_{fault}. $|Z_{infeeder}|$ is set to 1651.4 Ω, generating a short circuit current contribution equivalent to 7 synchronous machines of 3.6 MVA at 690V. The selected model parameters are given in Table 12, except for $|Z_{infeeder}|$, and that 3 inverters were connected to PCC. The trip times t_{trip} includes the 0.5 s before fault initiation.

a) $R_{fault} = 0.0001\ \Omega$ $t_{trip} = 0.5925$ s
b) $R_{fault} = 0.001\ \Omega$ $t_{trip} = 0.5925$ s
c) $R_{fault} = 0.01\ \Omega$ $t_{trip} = 0.5925$ s
d) $R_{fault} = 0.1\ \Omega$ $t_{trip} = 0.5825$ s
e) $R_{fault} = 1\ \Omega$ $t_{trip} = 0.5687$ s
f) $R_{fault} = 10\ \Omega$ $t_{trip} =$ -

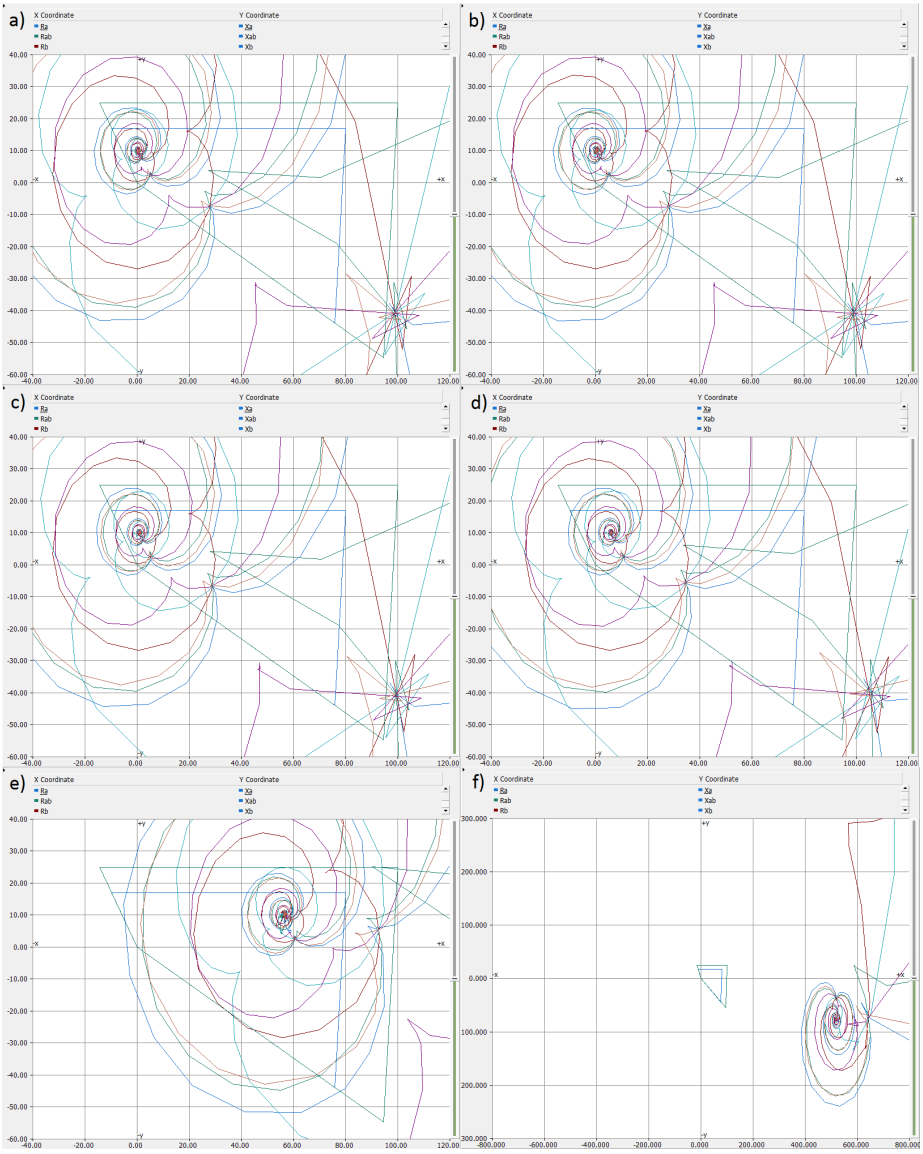

Figure 57: Relay 1 impedance diagrams for 40% inverter generation, for different values of R_{fault}. $|Z_{infeeder}|$ is set to 1926.7 Ω, generating a short circuit current contribution equivalent to 6 synchronous machines of 3.6 MVA at 690V. The selected model parameters are given in Table 12, except for $|Z_{infeeder}|$, and that 4 inverters were connected to PCC.

a) $R_{fault} = 0.0001\ \Omega$ $Z_a = 0.4507 + j10.04\ \Omega$
b) $R_{fault} = 0.001\ \Omega$ $Z_a = 0.4673 + j10.03\ \Omega$
c) $R_{fault} = 0.01\ \Omega$ $Z_a = 0.8978 + j10.00\ \Omega$
d) $R_{fault} = 0.1\ \Omega$ $Z_a = 6.097 + j10.20\ \Omega$
e) $R_{fault} = 1\ \Omega$ $Z_a = 56.62 + j10.24\ \Omega$
f) $R_{fault} = 10\ \Omega$ $Z_a = 519.0 - j76.53\ \Omega$

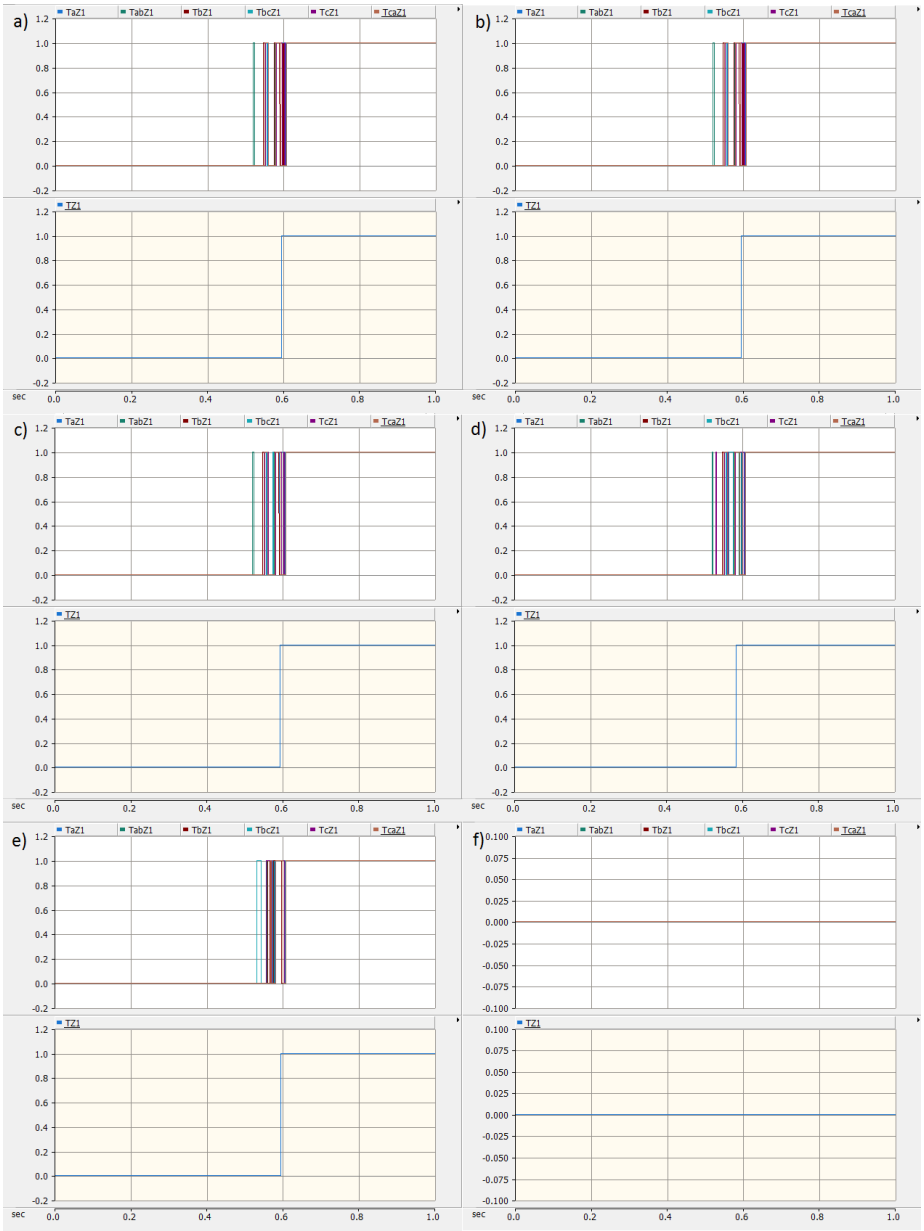

Figure 58: Relay 1 zone 1 fault detection and tripping for 40% inverter generation, for different values of R_{fault}. $|Z_{infeeder}|$ is set to 1926.7 Ω, generating a short circuit current contribution equivalent to 6 synchronous machines of 3.6 MVA at 690V. The selected model parameters are given in Table 12, except for $|Z_{infeeder}|$, and that 4 inverters were connected to PCC. The trip times t_{trip} includes the 0.5 s before fault initiation.

a) $R_{fault} = 0.0001\ \Omega$ $t_{trip} = 0.5937$ s
b) $R_{fault} = 0.001\ \Omega$ $t_{trip} = 0.5937$ s
c) $R_{fault} = 0.01\ \Omega$ $t_{trip} = 0.5925$ s
d) $R_{fault} = 0.1\ \Omega$ $t_{trip} = 0.5825$ s
e) $R_{fault} = 1\ \Omega$ $t_{trip} = 0.5937$ s
f) $R_{fault} = 10\ \Omega$ $t_{trip} =$ -

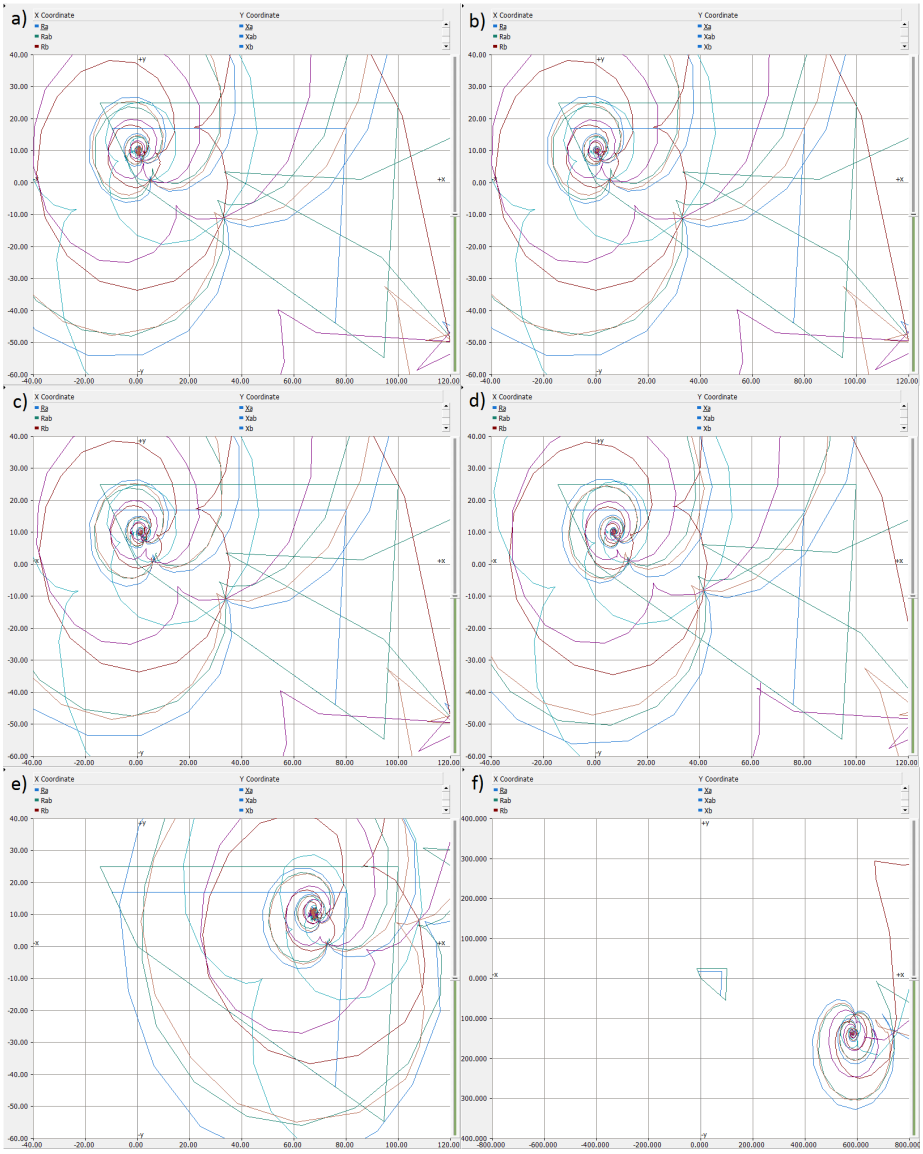

Figure 59: Relay 1 impedance diagrams for 50% inverter generation, for different values of R_{fault}. $|Z_{infeeder}|$ is set to 2312 Ω, generating a short circuit current contribution equivalent to 5 synchronous machines of 3.6 MVA at 690V. The selected model parameters are given in Table 12, except for $|Z_{infeeder}|$, and that 5 inverters were connected to PCC.

a) $R_{fault} = 0.0001\ \Omega$ $Z_a = 0.4531 + \text{j}10.03\ \Omega$
b) $R_{fault} = 0.001\ \Omega$ $Z_a = 0.3763 + \text{j}10.04\ \Omega$
c) $R_{fault} = 0.01\ \Omega$ $Z_a = 0.8930 + \text{j}9.993\ \Omega$
d) $R_{fault} = 0.1\ \Omega$ $Z_a = 6.964 + \text{j}10.02\ \Omega$
e) $R_{fault} = 1\ \Omega$ $Z_a = 67.90 + \text{j}10.73\ \Omega$
f) $R_{fault} = 10\ \Omega$ $Z_a = 584.2$ - j137.5 Ω

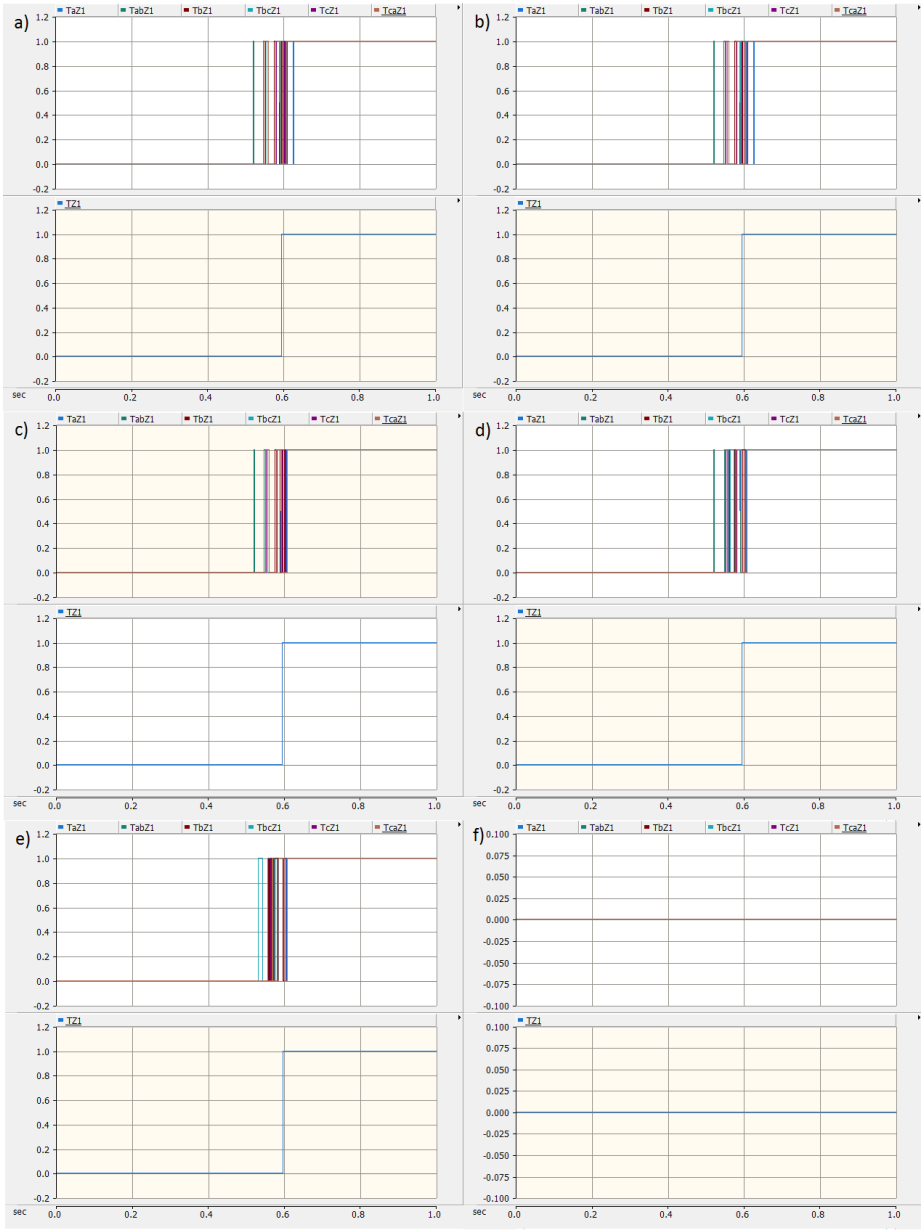

Figure 60: Relay 1 zone 1 fault detection and tripping for 50% inverter generation, for different values of R_{fault}. $|Z_{infeeder}|$ is set to 2312 Ω, generating a short circuit current contribution equivalent to 5 synchronous machines of 3.6 MVA at 690V. The selected model parameters are given in Table 12, except for $|Z_{infeeder}|$, and that 5 inverters were connected to PCC. The trip times t_{trip} includes the 0.5 s before fault initiation.

a) $R_{fault} = 0.0001\ \Omega$ $t_{trip} = 0.5937$ s
b) $R_{fault} = 0.001\ \Omega$ $t_{trip} = 0.5937$ s
c) $R_{fault} = 0.01\ \Omega$ $t_{trip} = 0.5937$ s
d) $R_{fault} = 0.1\ \Omega$ $t_{trip} = 0.5937$ s
e) $R_{fault} = 1\ \Omega$ $t_{trip} = 0.5950$ s
f) $R_{fault} = 10\ \Omega$ $t_{trip} =$ -

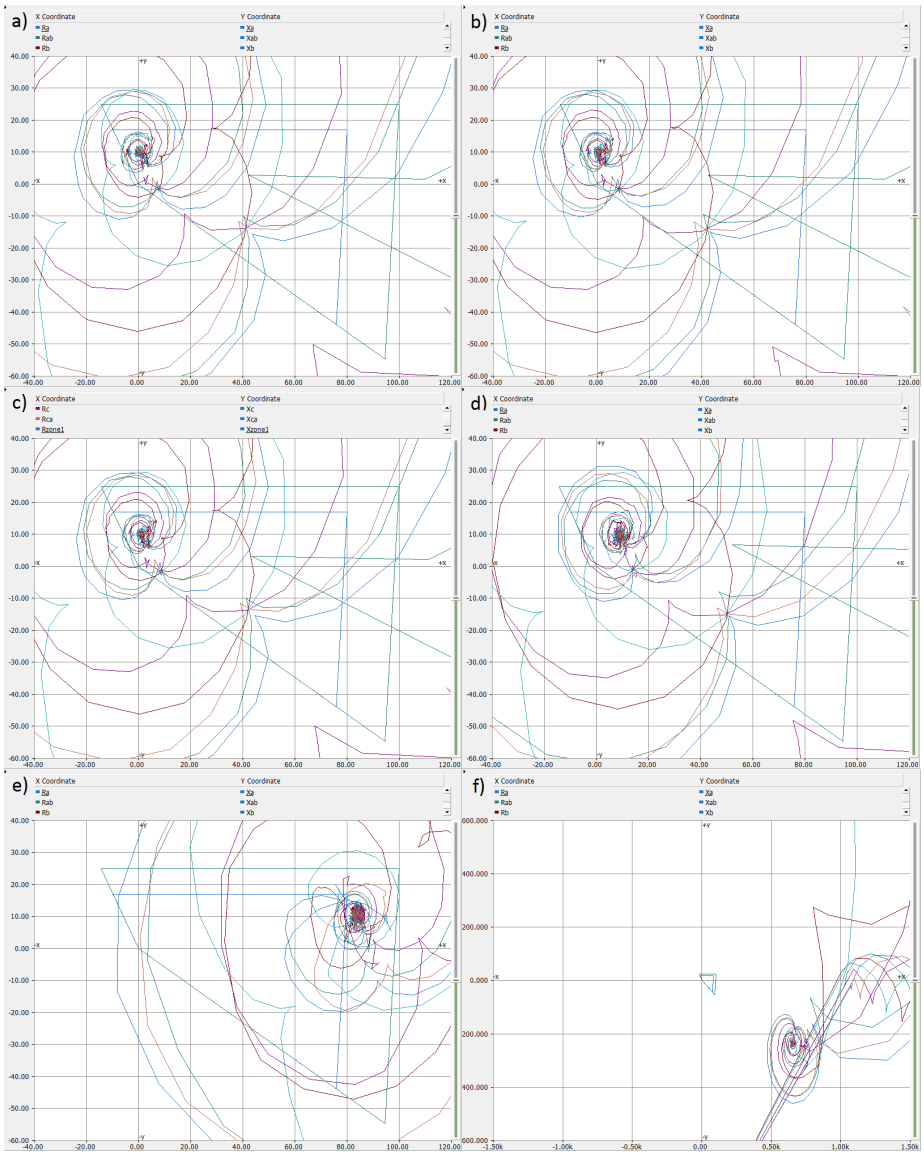

Figure 61: Relay 1 impedance diagrams for 60% inverter generation, for different values of R_{fault}. $|Z_{infeeder}|$ is set to 2890 Ω, generating a short circuit current contribution equivalent to 4 synchronous machines of 3.6 MVA at 690V. The selected model parameters are given in Table 12, except for $|Z_{infeeder}|$, and that 6 inverters were connected to PCC.

a) $R_{fault} = 0.0001\ \Omega$ $Z_a = 0.5123 + \text{j}10.05\ \Omega$
b) $R_{fault} = 0.001\ \Omega$ $Z_a = 0.3989 + \text{j}9.988\ \Omega$
c) $R_{fault} = 0.01\ \Omega$ $Z_a = 1.182 + \text{j}10.07\ \Omega$
d) $R_{fault} = 0.1\ \Omega$ $Z_a = 8.766 + \text{j}10.16\ \Omega$
e) $R_{fault} = 1\ \Omega$ $Z_a = 82.92 + \text{j}7.350\ \Omega$
f) $R_{fault} = 10\ \Omega$ $Z_a = 654.5 - \text{j}235.3\ \Omega$

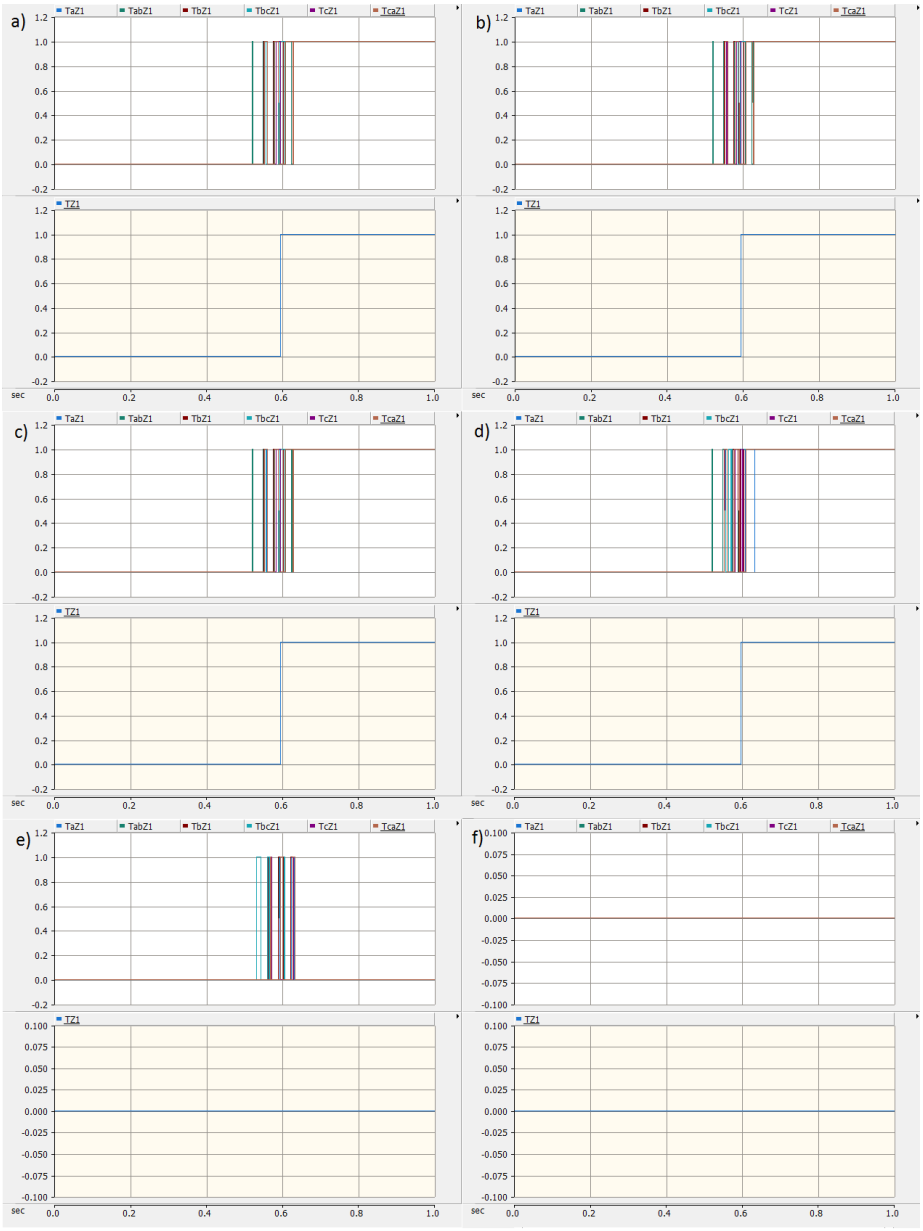

Figure 62: Relay 1 zone 1 fault detection and tripping for 60% inverter generation, for different values of R_{fault}. $|Z_{infeeder}|$ is set to 2890 Ω, generating a short circuit current contribution equivalent to 4 synchronous machines of 3.6 MVA at 690V. The selected model parameters are given in Table 12, except for $|Z_{infeeder}|$, and that 6 inverters were connected to PCC. The trip times t_{trip} includes the 0.5 s before fault initiation.

a) $R_{fault} = 0.0001\ \Omega$ $t_{trip} = 0.5937$ s
b) $R_{fault} = 0.001\ \Omega$ $t_{trip} = 0.5937$ s
c) $R_{fault} = 0.01\ \Omega$ $t_{trip} = 0.5937$ s
d) $R_{fault} = 0.1\ \Omega$ $t_{trip} = 0.5950$ s
e) $R_{fault} = 1\ \Omega$ $t_{trip} =$ -
f) $R_{fault} = 10\ \Omega$ $t_{trip} =$ -

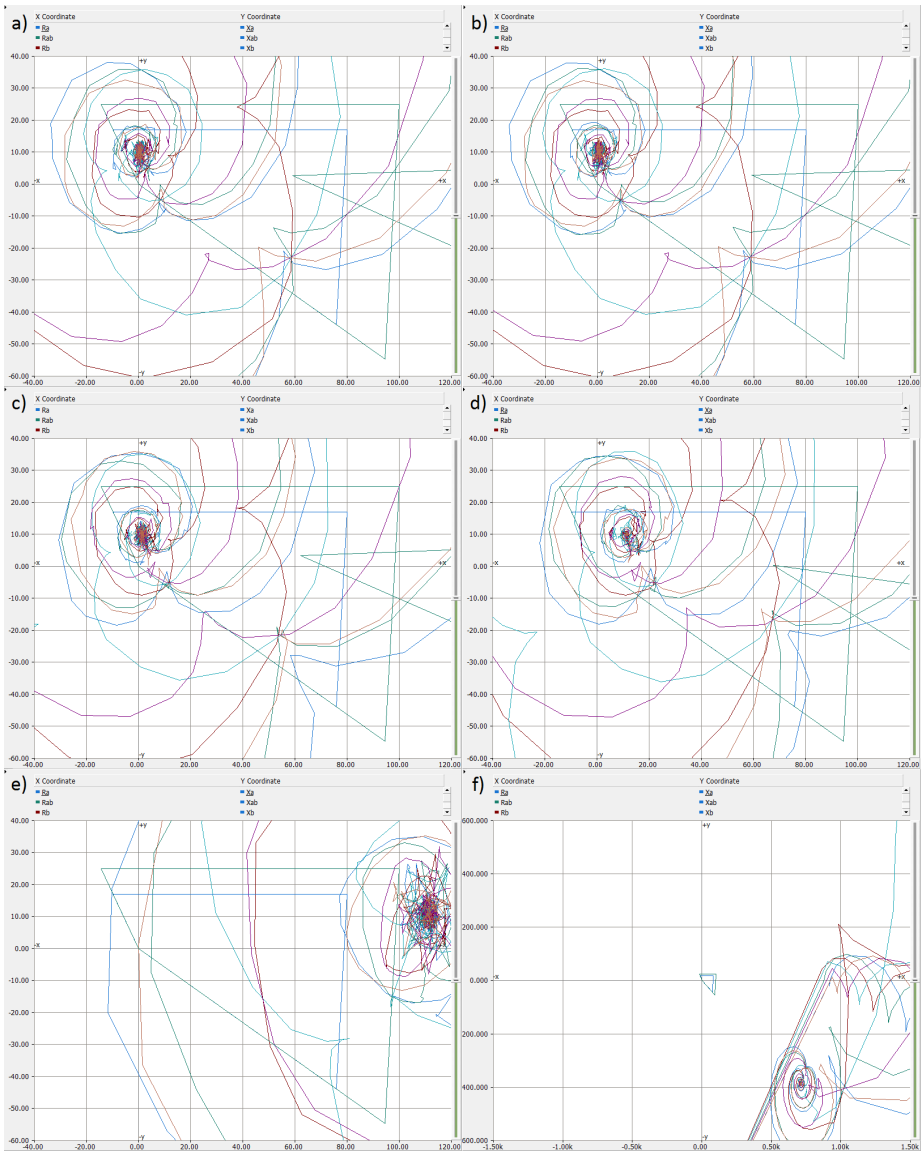

Figure 63: Relay 1 impedance diagrams for 70% inverter generation, for different values of R_{fault}. $|Z_{infeeder}|$ is set to 3853.3 Ω, generating a short circuit current contribution equivalent to 3 synchronous machines of 3.6 MVA at 690V. The selected model parameters are given in Table 12, except for $|Z_{infeeder}|$, and that 7 inverters were connected to PCC.

a) $R_{fault} = 0.0001\ \Omega$ $Z_a = 0.7085 + j10.06\ \Omega$
b) $R_{fault} = 0.001\ \Omega$ $Z_a = 0.5426 + j10.04\ \Omega$
c) $R_{fault} = 0.01\ \Omega$ $Z_a = 1.571 + j10.00\ \Omega$
d) $R_{fault} = 0.1\ \Omega$ $Z_a = 11.50 + j10.24\ \Omega$
e) $R_{fault} = 1\ \Omega$ $Z_a = 114.6 + j9.343\ \Omega$
f) $R_{fault} = 10\ \Omega$ $Z_a = 712.4 - j387.6\ \Omega$

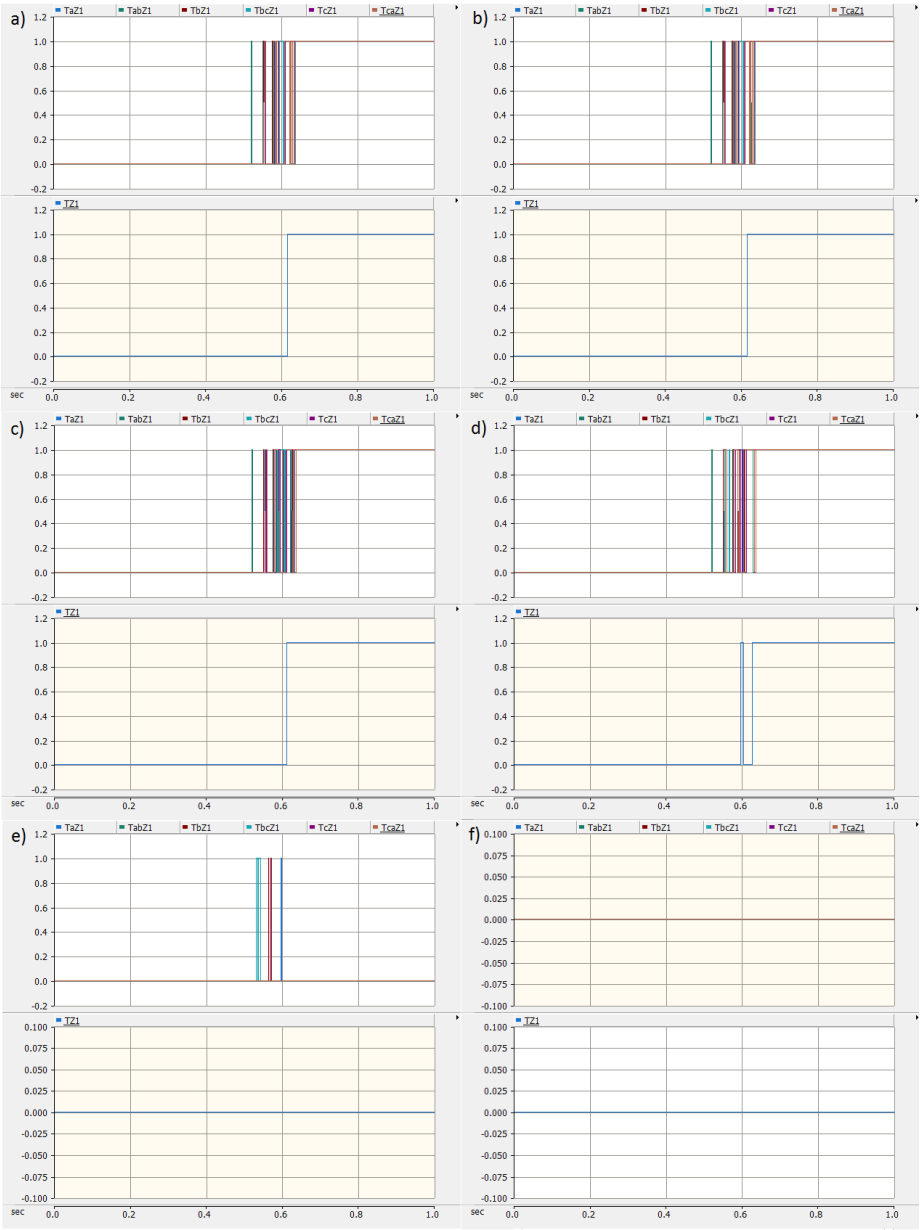

Figure 64: Relay 1 zone 1 fault detection and tripping for 70% inverter generation, for different values of R_{fault}. $|Z_{infeeder}|$ is set to 3853.3 Ω, generating a short circuit current contribution equivalent to 3 synchronous machines of 3.6 MVA at 690V. The selected model parameters are given in Table 12, except for $|Z_{infeeder}|$, and that 7 inverters were connected to PCC. The trip times t_{trip} includes the 0.5 s before fault initiation.

a) $R_{fault} = 0.0001\ \Omega$ $t_{trip} = 0.6137$ s
b) $R_{fault} = 0.001\ \Omega$ $t_{trip} = 0.6137$ s
c) $R_{fault} = 0.01\ \Omega$ $t_{trip} = 0.6100$ s
d) $R_{fault} = 0.1\ \Omega$ $t_{trip} = 0.5950$ s
e) $R_{fault} = 1\ \Omega$ $t_{trip} =$ -
f) $R_{fault} = 10\ \Omega$ $t_{trip} =$ -

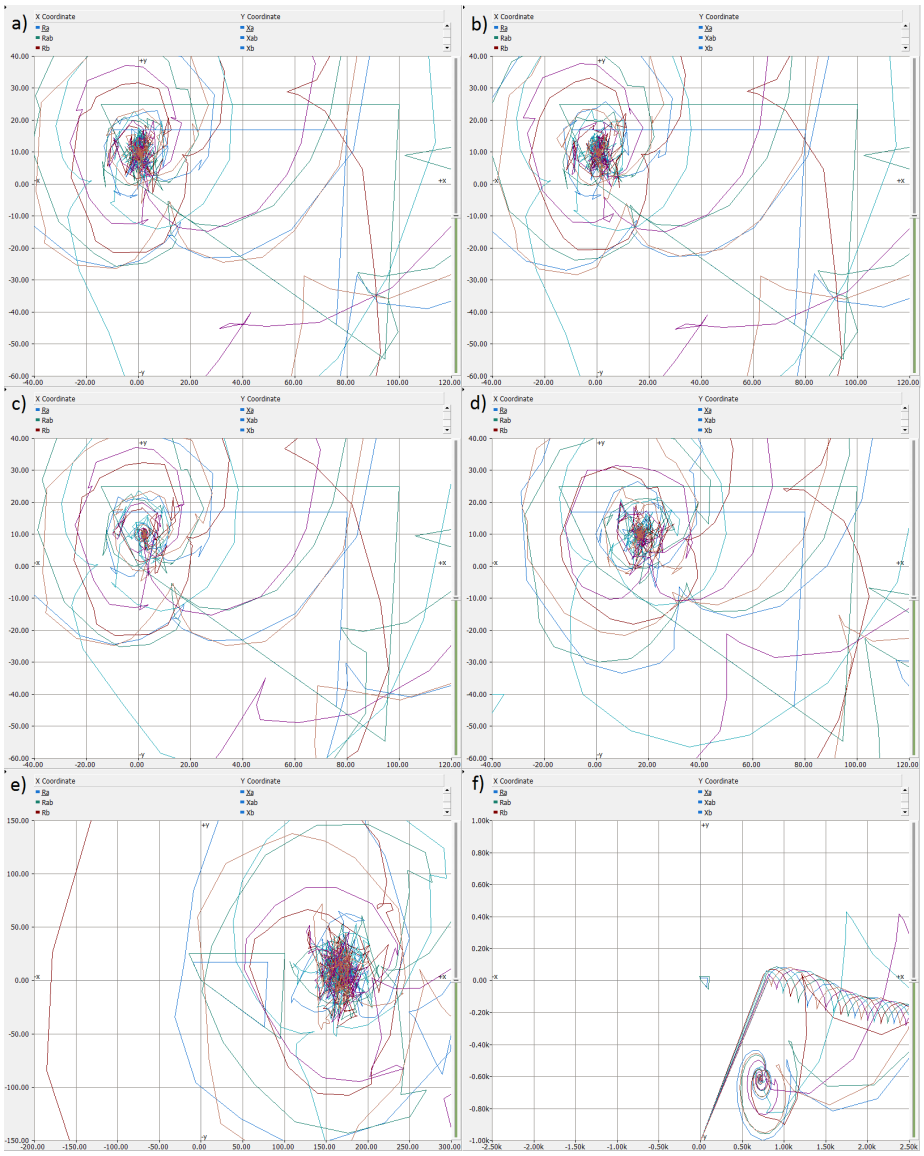

Figure 65: Relay 1 impedance diagrams for 80% inverter generation, for different values of R_{fault}. $|Z_{infeeder}|$ is set to 5780 Ω, generating a short circuit current contribution equivalent to 2 synchronous machines of 3.6 MVA at 690V. The selected model parameters are given in Table 12, except for $|Z_{infeeder}|$, and that 8 inverters were connected to PCC.

a) $R_{fault} = 0.0001\ \Omega$ $Z_a = 0.7085 + \text{j}10.06\ \Omega$
b) $R_{fault} = 0.001\ \Omega$ $Z_a = 0.5426 + \text{j}10.04\ \Omega$
c) $R_{fault} = 0.01\ \Omega$ $Z_a = 1.571 + \text{j}10.00\ \Omega$
d) $R_{fault} = 0.1\ \Omega$ $Z_a = 11.50 + \text{j}10.24\ \Omega$
e) $R_{fault} = 1\ \Omega$ $Z_a = 114.6 + \text{j}9.343\ \Omega$
f) $R_{fault} = 10\ \Omega$ $Z_a = 712.4 - \text{j}387.6\ \Omega$

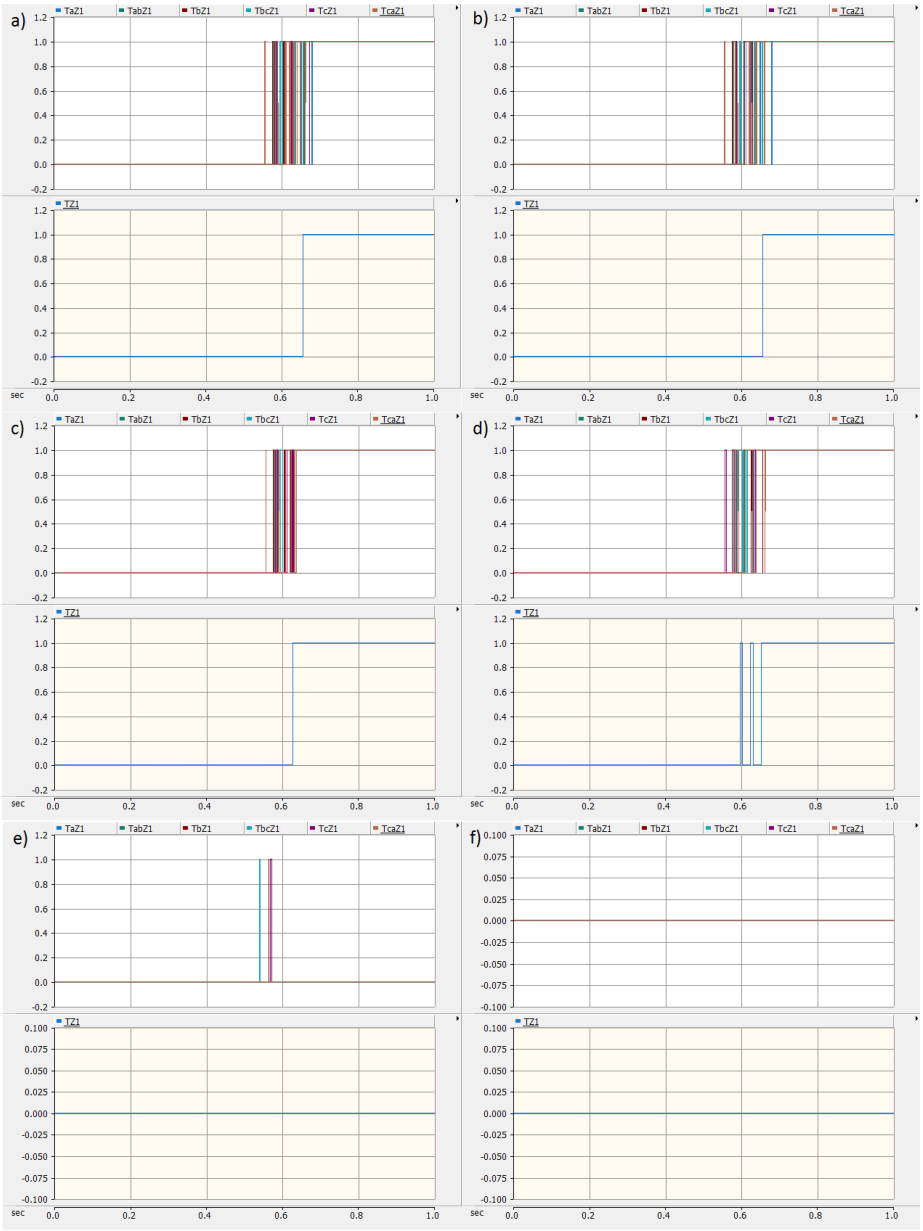

Figure 66: Relay 1 zone 1 fault detection and tripping for 80% inverter generation, for different values of R_{fault}. $|Z_{infeeder}|$ is set to 5780 Ω, generating a short circuit current contribution equivalent to 2 synchronous machines of 3.6 MVA at 690V. The selected model parameters are given in Table 12, except for $|Z_{infeeder}|$, and that 8 inverters were connected to PCC. The trip times t_{trip} includes the 0.5 s before fault initiation.

a) $R_{fault} = 0.0001\ \Omega$ $t_{trip} = 0.6537$ s
b) $R_{fault} = 0.001\ \Omega$ $t_{trip} = 0.6537$ s
c) $R_{fault} = 0.01\ \Omega$ $t_{trip} = 0.6250$ s
d) $R_{fault} = 0.1\ \Omega$ $t_{trip} = 0.5950$ s
e) $R_{fault} = 1\ \Omega$ $t_{trip} =$ -
f) $R_{fault} = 10\ \Omega$ $t_{trip} =$ -

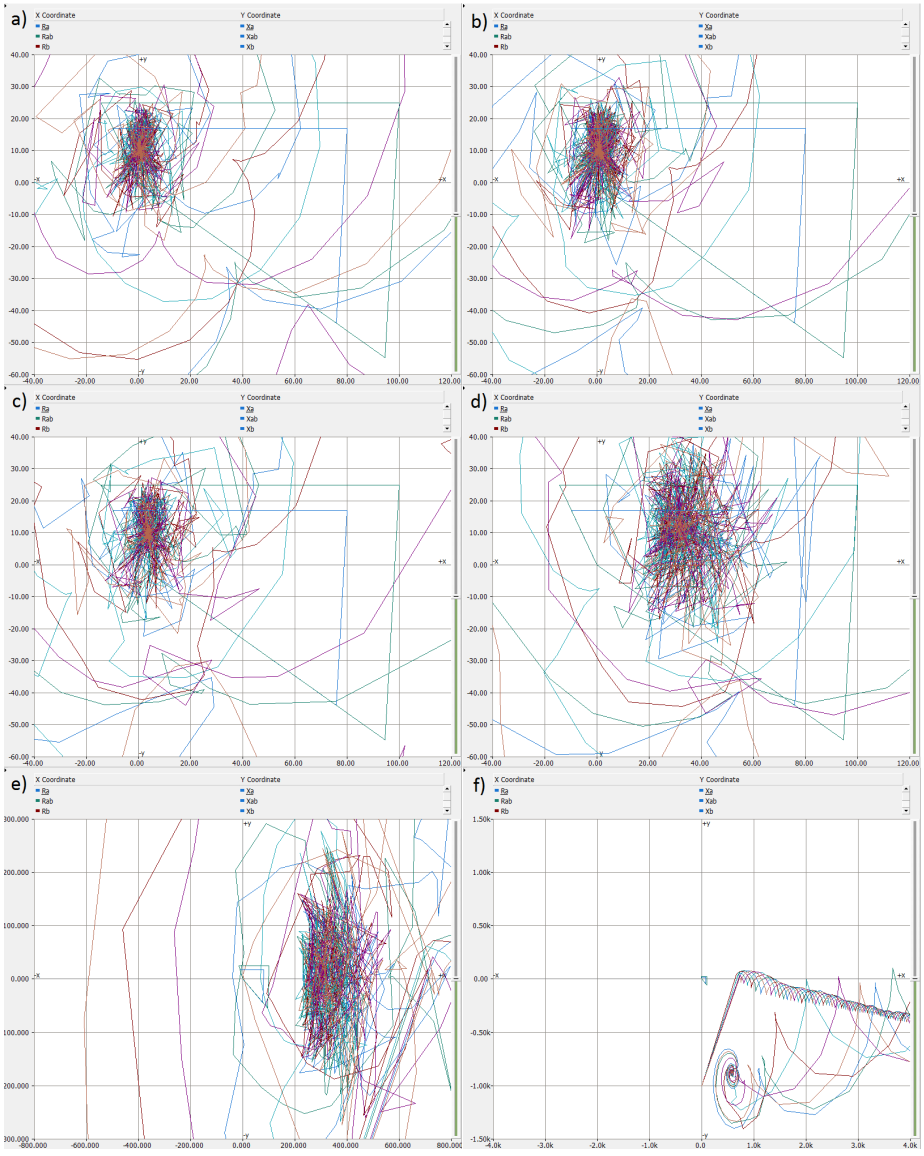

Figure 67: Relay 1 impedance diagrams for 90% inverter generation, for different values of R_{fault}. $|Z_{infeeder}|$ is set to 11560 Ω, generating a short circuit current contribution equivalent to 1 synchronous machine of 3.6 MVA at 690V. The selected model parameters are given in Table 12, except for $|Z_{infeeder}|$, and that 9 inverters were connected to PCC.

a) $R_{fault} = 0.0001\ \Omega$ Z_a = -
b) $R_{fault} = 0.001\ \Omega$ Z_a = -
c) $R_{fault} = 0.01\ \Omega$ Z_a = -
d) $R_{fault} = 0.1\ \Omega$ Z_a = -
e) $R_{fault} = 1\ \Omega$ Z_a = -
f) $R_{fault} = 10\ \Omega$ Z_a = 574.4 - j875.2 Ω

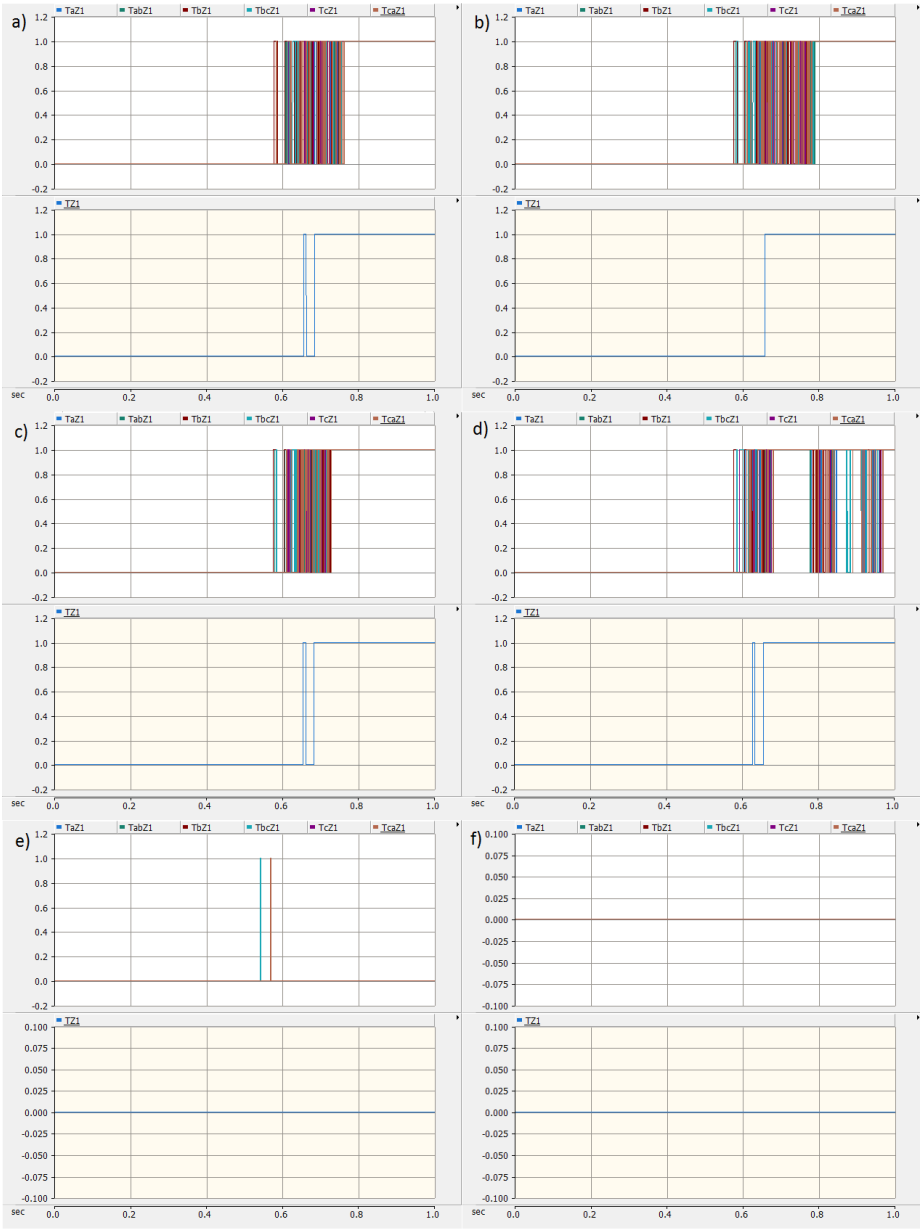

Figure 68: Relay 1 zone 1 fault detection and tripping for 90% inverter generation, for different values of R_{fault}. $|Z_{infeeder}|$ is set to 11560 Ω, generating a short circuit current contribution equivalent to 1 synchronous machines of 3.6 MVA at 690V. The selected model parameters are given in Table 12, except for $|Z_{infeeder}|$, and that 9 inverters were connected to PCC. The trip times t_{trip} includes the 0.5 s before fault initiation.

a) $R_{fault} = 0.0001\ \Omega$ $t_{trip} = 0.6537$ s
b) $R_{fault} = 0.001\ \Omega$ $t_{trip} = 0.6562$ s
c) $R_{fault} = 0.01\ \Omega$ $t_{trip} = 0.6525$ s
d) $R_{fault} = 0.1\ \Omega$ $t_{trip} = 0.6250$ s
e) $R_{fault} = 1\ \Omega$ $t_{trip} =$ -
f) $R_{fault} = 10\ \Omega$ $t_{trip} =$ -

Appendix D

Additional results for simulation set 4 are presented here, including the fault impedance diagrams, the trip times, and the short circuit current contributions from both ends of Line 12.

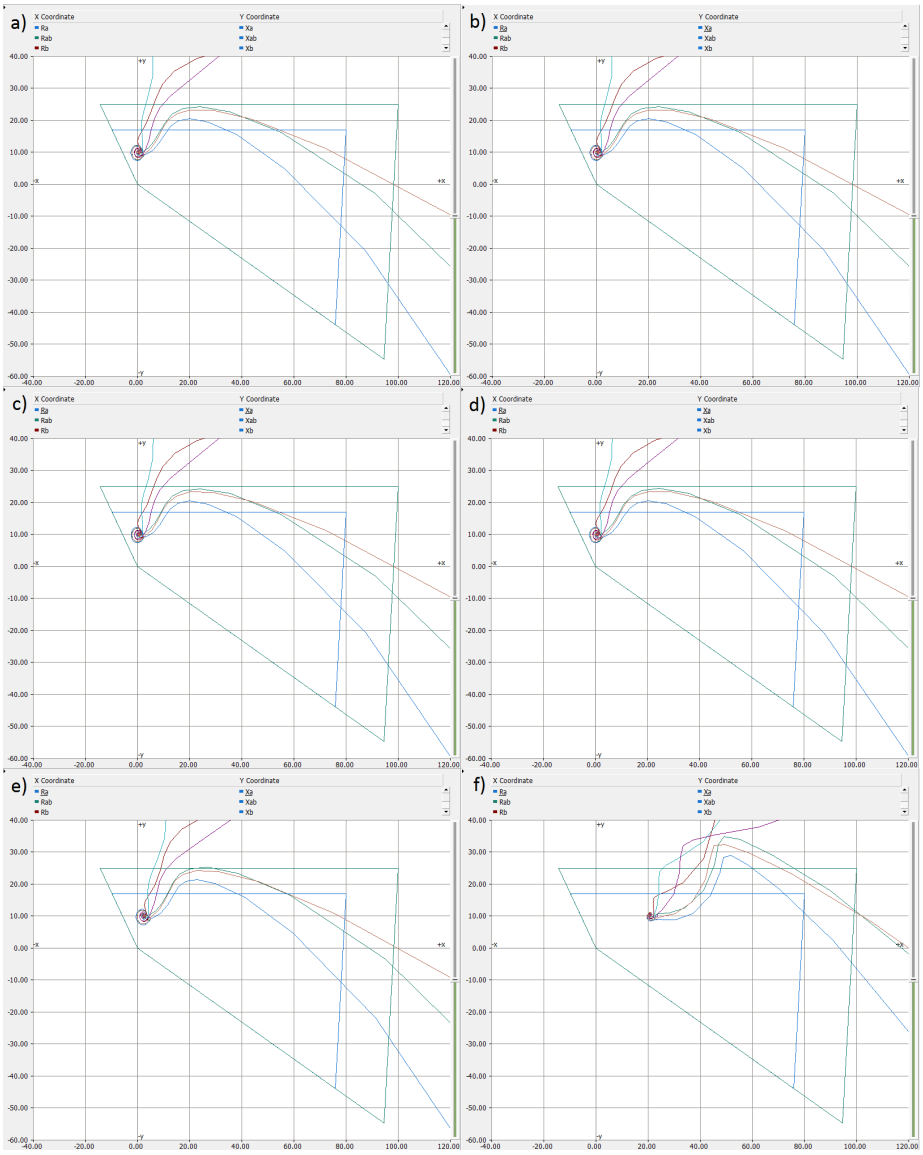

Figure 69: Relay 1 impedance diagrams for infeeder generation only and $|Z_{infeeder}|$ set to 25.76 Ω, for different values of R_{fault}. The selected model parameters are given in Table 12, except for $|Z_{infeeder}|$, and that no inverters were connected to PCC.

a) $R_{fault} = 0.0001\ \Omega$ $Z_a = 0.4246 + \text{j}10.03\ \Omega$
b) $R_{fault} = 0.001\ \Omega$ $Z_a = 0.4266 + 10.03\ \Omega$
c) $R_{fault} = 0.01\ \Omega$ $Z_a = 0.4447 + 10.03\ \Omega$
d) $R_{fault} = 0.1\ \Omega$ $Z_a = 0.6262 + 10.03\ \Omega$
e) $R_{fault} = 1\ \Omega$ $Z_a = 2.443 + 10.08\ \Omega$
f) $R_{fault} = 10\ \Omega$ $Z_a = 20.62 + 10.44\ \Omega$

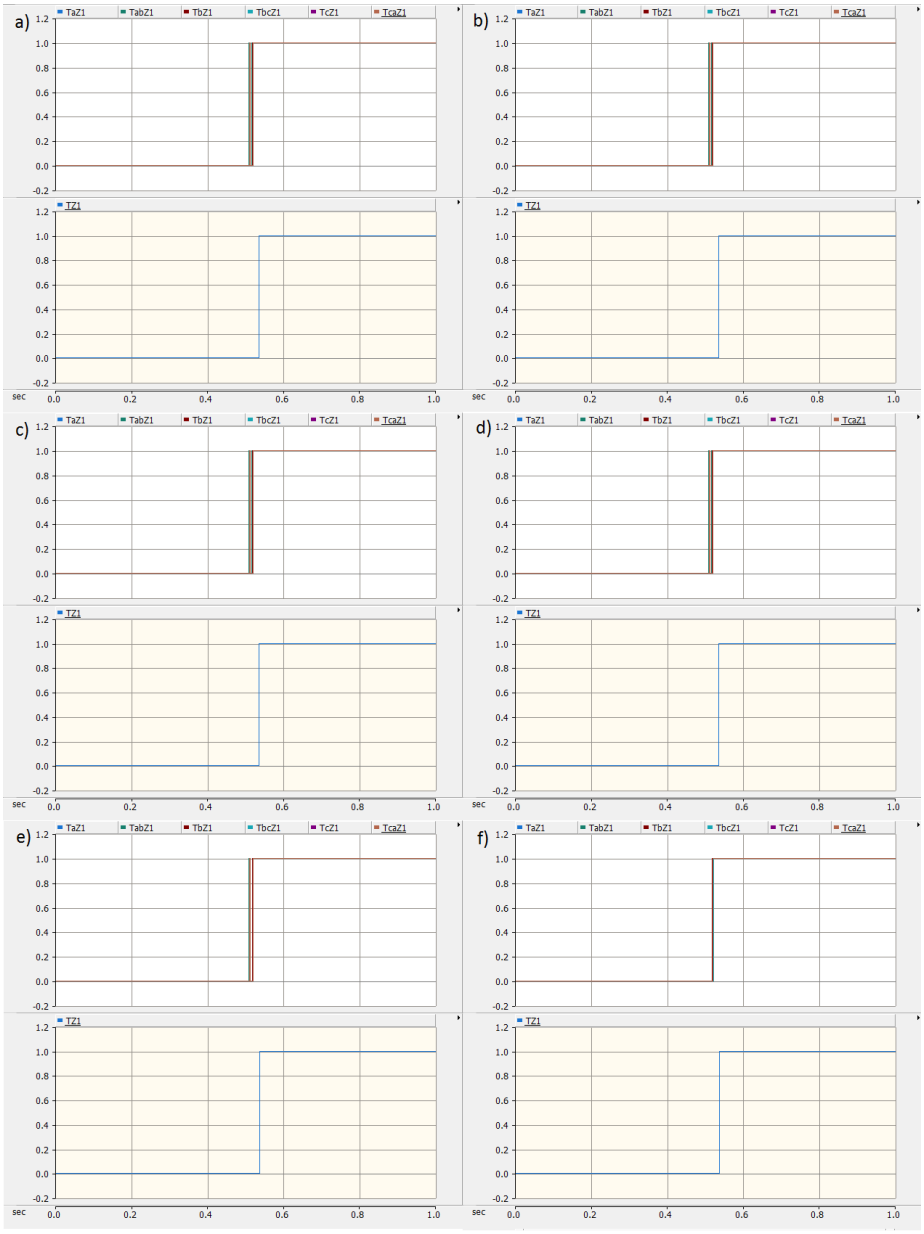

Figure 70: Relay 1 trip times for infeeder generation only and $|Z_{infeeder}|$ set to 25.76 Ω, for different values of R_{fault}. The selected model parameters are given in Table 12, except for $|Z_{infeeder}|$, and that no inverters were connected to PCC. The trip times t_{trip} includes the 0.5 s before fault initiation.

a) $R_{fault} = 0.0001\ \Omega$ $t_{trip} = 0.535$ s
b) $R_{fault} = 0.001\ \Omega$ $t_{trip} = 0.535$ s
c) $R_{fault} = 0.01\ \Omega$ $t_{trip} = 0.535$ s
d) $R_{fault} = 0.1\ \Omega$ $t_{trip} = 0.535$ s
e) $R_{fault} = 1\ \Omega$ $t_{trip} = 0.5362$ s
f) $R_{fault} = 10\ \Omega$ $t_{trip} = 0.5362$ s

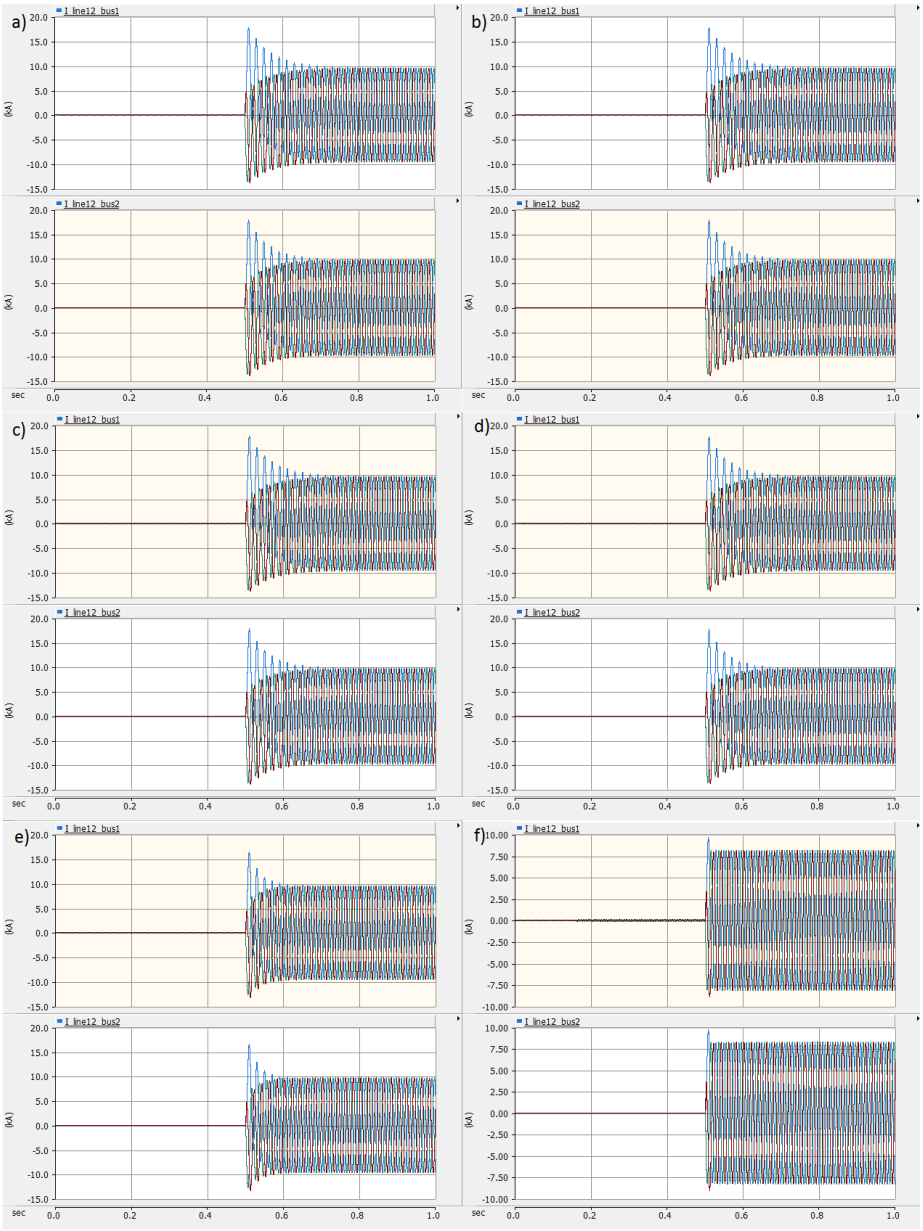

Figure 71: Current contributions for infeeder generation only and $|Z_{infeeder}|$ set to 25.76 Ω, for different values of R_{fault}. The selected model parameters are given in Table 12, except for $|Z_{infeeder}|$, and that no inverters were connected to PCC. During the faulted period, $\frac{I\_line12\_bus2}{I\_line12\_bus1} \approx 1.02$.

a) $R_{fault} = 0.0001\ \Omega$ b) $R_{fault} = 0.001\ \Omega$

c) $R_{fault} = 0.01\ \Omega$ d) $R_{fault} = 0.1\ \Omega$

e) $R_{fault} = 1\ \Omega$ f) $R_{fault} = 10\ \Omega$

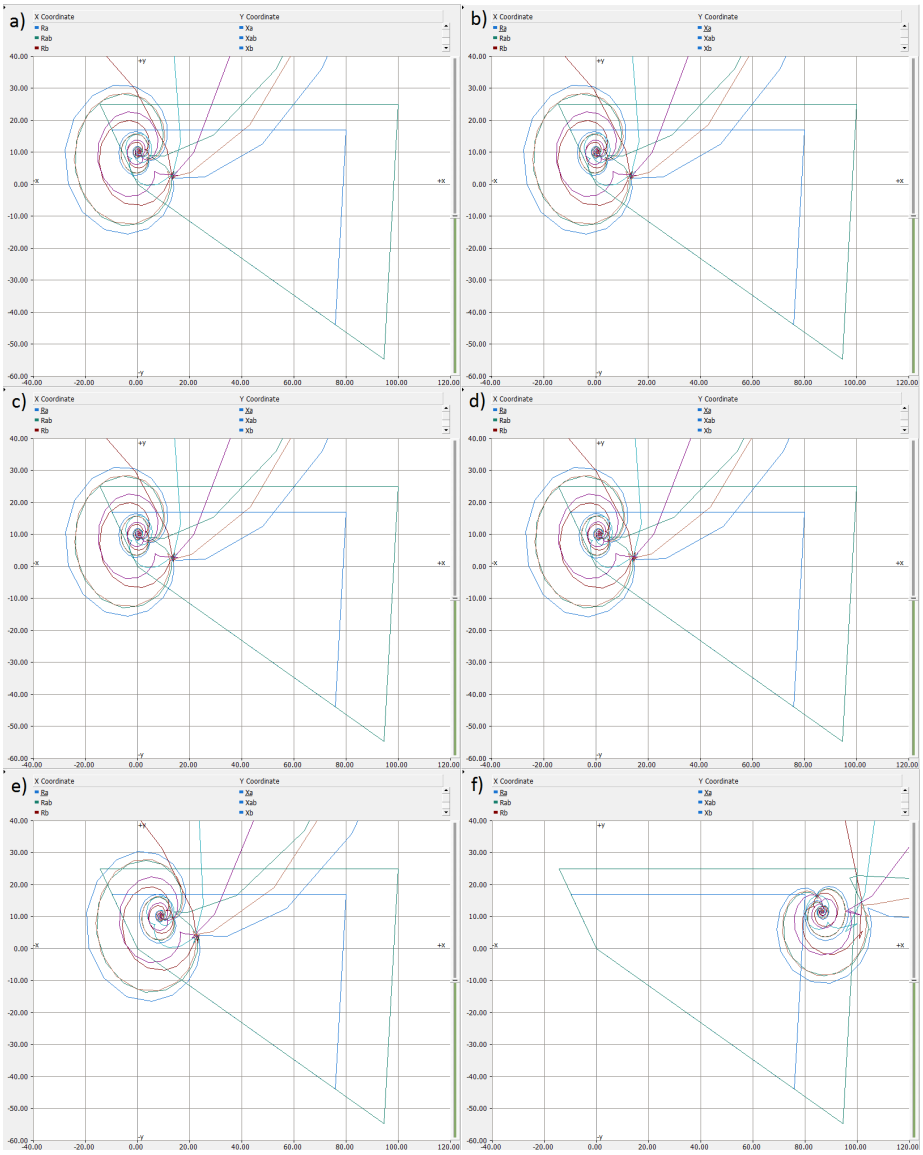

Figure 72: Relay 1 impedance diagrams for infeeder generation only and $|Z_{infeeder}|$ set to 257.6 Ω, for different values of R_{fault}. The selected model parameters are given in Table 12, except for $|Z_{infeeder}|$, and that no inverters were connected to PCC.

a) $R_{fault} = 0.0001\ \Omega$ $Z_a = 0.4242 + \text{j}10.03\ \Omega$
b) $R_{fault} = 0.001\ \Omega$ $Z_a = 0.4328 + \text{j}10.03\ \Omega$
c) $R_{fault} = 0.01\ \Omega$ $Z_a = 0.5103 + \text{j}10.03\ \Omega$
d) $R_{fault} = 0.1\ \Omega$ $Z_a = 1.285 + \text{j}10.05\ \Omega$
e) $R_{fault} = 1\ \Omega$ $Z_a = 9.038 + \text{j}10.25\ \Omega$
f) $R_{fault} = 10\ \Omega$ $Z_a = 86.58 + \text{j}11.75\ \Omega$

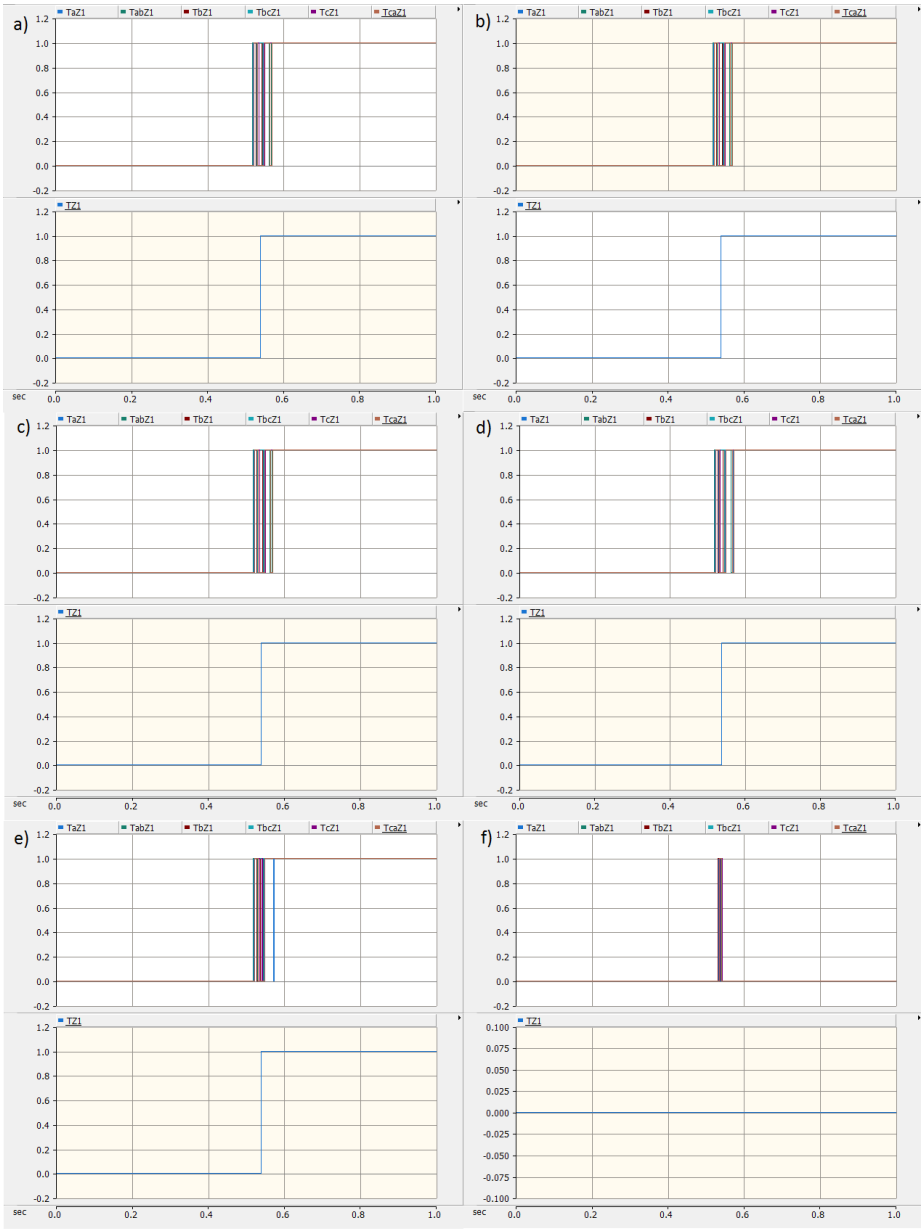

Figure 73: Relay 1 trip times for infeeder generation only and $|Z_{infeeder}|$ set to 257.6 Ω, for different values of R_{fault}. The selected model parameters are given in Table 12, except for $|Z_{infeeder}|$, and that no inverters were connected to PCC. The trip times t_{trip} includes the 0.5 s before fault initiation.

a) $R_{fault} = 0.0001\ \Omega$ $t_{trip} = 0.5375$ s
b) $R_{fault} = 0.001\ \Omega$ $t_{trip} = 0.5375$ s
c) $R_{fault} = 0.01\ \Omega$ $t_{trip} = 0.5375$ s
d) $R_{fault} = 0.1\ \Omega$ $t_{trip} = 0.5375$ s
e) $R_{fault} = 1\ \Omega$ $t_{trip} = 0.5375$ s
f) $R_{fault} = 10\ \Omega$ $t_{trip} =$ -

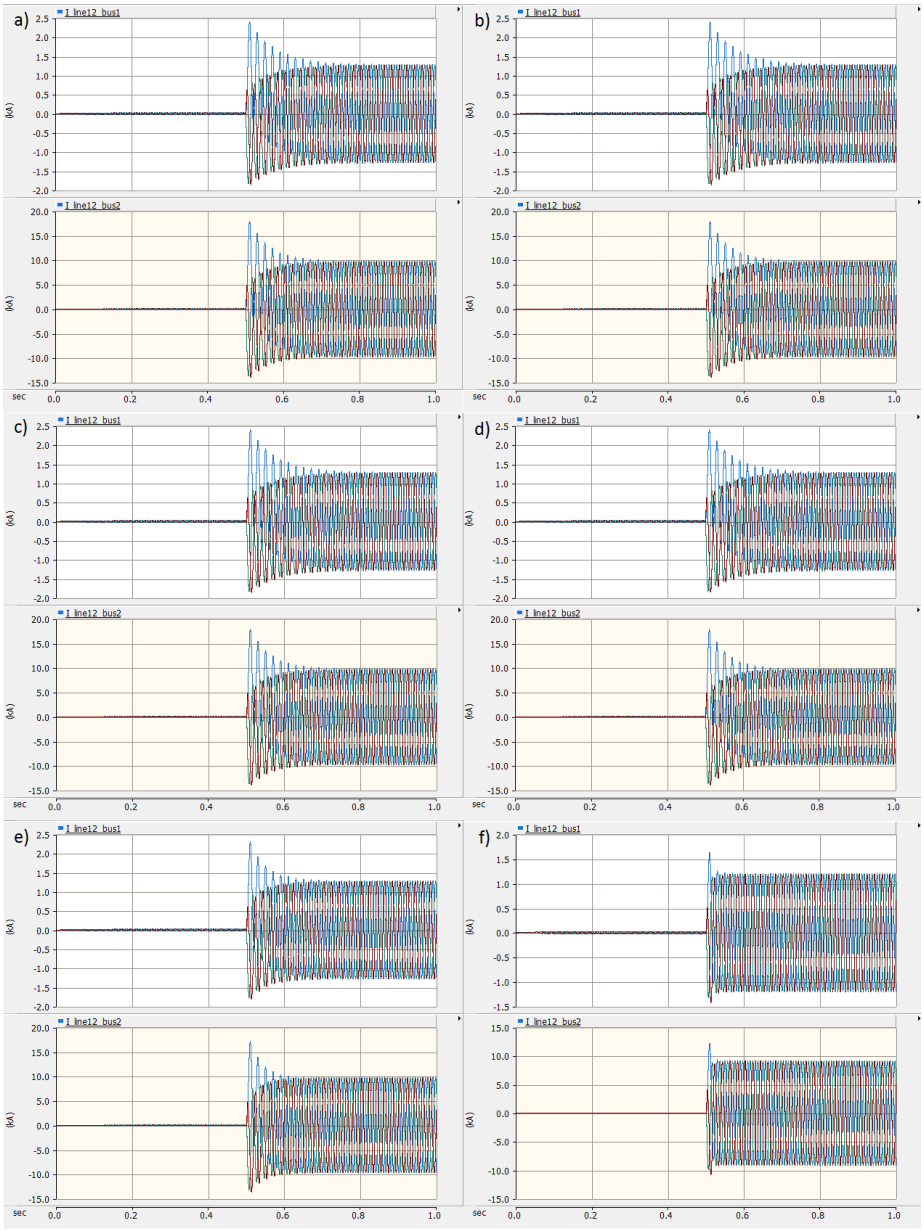

Figure 74: Current contributions for infeeder generation only and $|Z_{infeeder}|$ set to 257.6 Ω, for different values of R_{fault}. The selected model parameters are given in Table 12, except for $|Z_{infeeder}|$, and that no inverters were connected to PCC. During the faulted period, $\frac{I\_line12\_bus2}{I\_line12\_bus1} \approx 7.58$.

a) $R_{fault} = 0.0001\ \Omega$ b) $R_{fault} = 0.001\ \Omega$

c) $R_{fault} = 0.01\ \Omega$ d) $R_{fault} = 0.1\ \Omega$

e) $R_{fault} = 1\ \Omega$ f) $R_{fault} = 10\ \Omega$

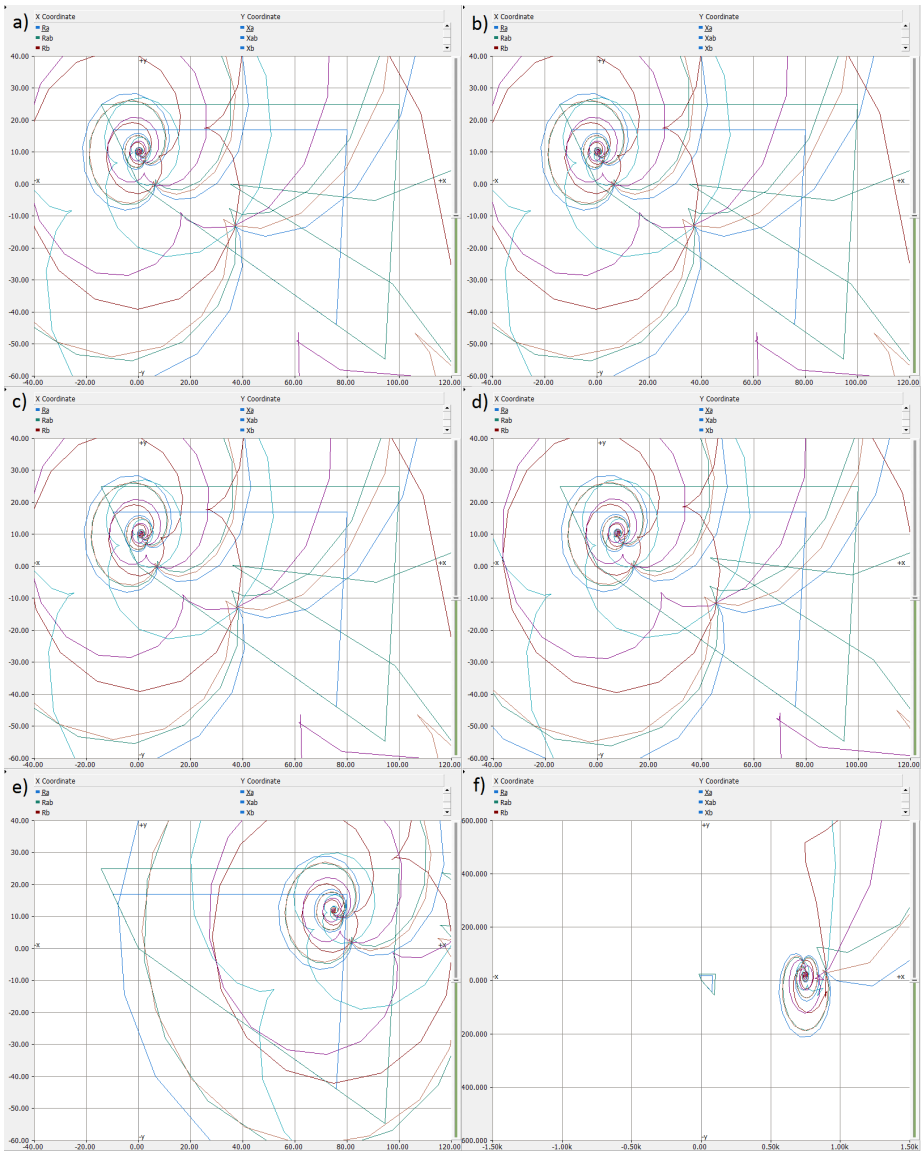

Figure 75: Relay 1 impedance diagrams for infeeder generation only and $|Z_{infeeder}|$ set to 2576 Ω, for different values of R_{fault}. The selected model parameters are given in Table 12, except for $|Z_{infeeder}|$, and that no inverters were connected to PCC.

a) $R_{fault} = 0.0001\ \Omega$ $Z_a = 0.4242 + \text{j}10.03\ \Omega$
b) $R_{fault} = 0.001\ \Omega$ $Z_a = 0.4988 + \text{j}10.03\ \Omega$
c) $R_{fault} = 0.01\ \Omega$ $Z_a = 1.17 + \text{j}10.05\ \Omega$
d) $R_{fault} = 0.1\ \Omega$ $Z_a = 7.881 + \text{j}10.22\ \Omega$
e) $R_{fault} = 1\ \Omega$ $Z_a = 74.99 + \text{j}11.87\ \Omega$
f) $R_{fault} = 10\ \Omega$ $Z_a = 746.2 + \text{j}19.44\ \Omega$

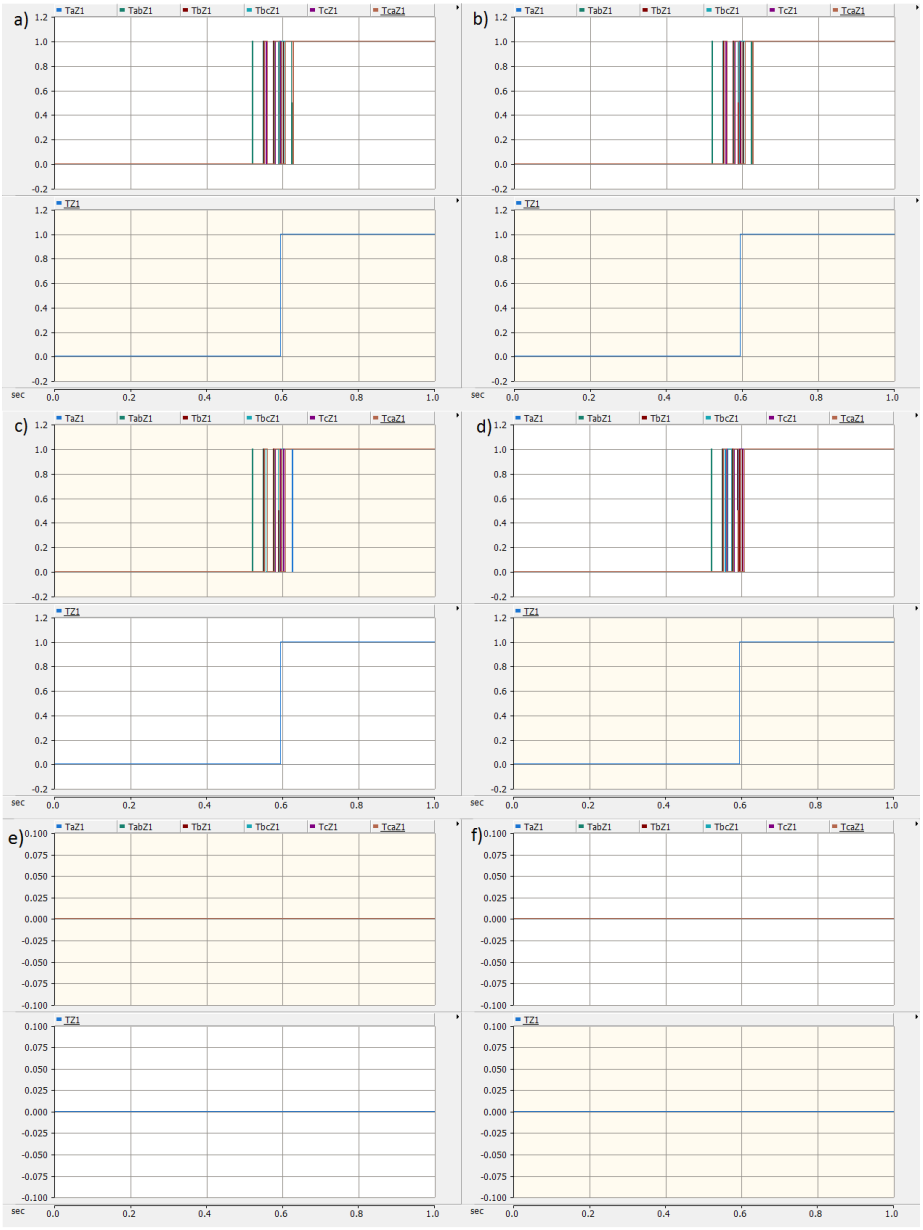

Figure 76: Relay 1 trip times for infeeder generation only and $|Z_{infeeder}|$ set to 2576 Ω, for different values of R_{fault}. The selected model parameters are given in Table 12, except for $|Z_{infeeder}|$, and that no inverters were connected to PCC. The trip times t_{trip} includes the 0.5 s before fault initiation.

a) $R_{fault} = 0.0001\ \Omega$ $t_{trip} = 0.5937$ s
b) $R_{fault} = 0.001\ \Omega$ $t_{trip} = 0.5937$ s
c) $R_{fault} = 0.01\ \Omega$ $t_{trip} = 0.5937$ s
d) $R_{fault} = 0.1\ \Omega$ $t_{trip} = 0.5937$ s
e) $R_{fault} = 1\ \Omega$ $t_{trip} = 0.6062$ s
f) $R_{fault} = 10\ \Omega$ $t_{trip} =$ -

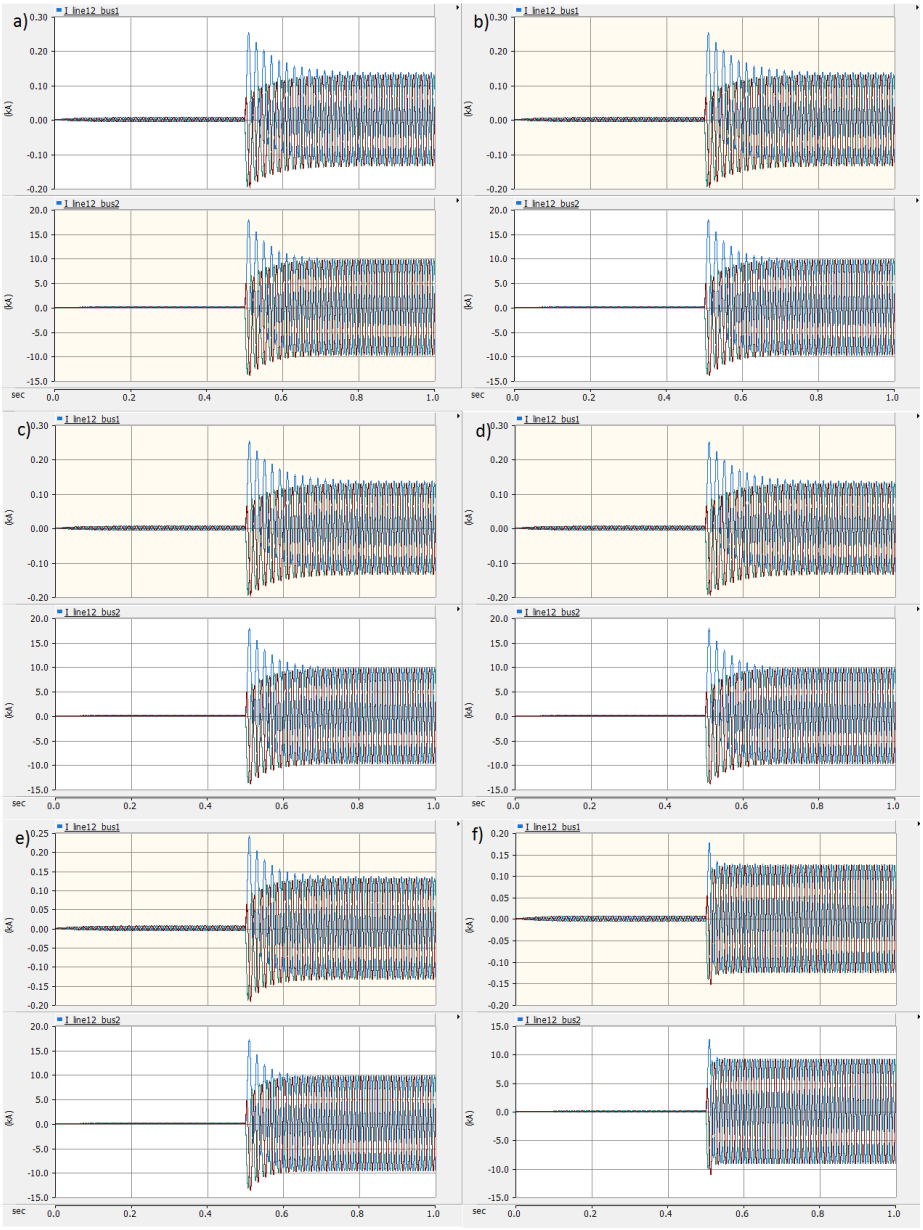

Figure 77: Current contributions for infeeder generation only and $|Z_{infeeder}|$ set to 2576 Ω, for different values of R_{fault}. The selected model parameters are given in Table 12, except for $|Z_{infeeder}|$, and that no inverters were connected to PCC. During the faulted period, $\frac{I\_line12\_bus2}{I\_line12\_bus1} \approx 73.4$.

a) $R_{fault} = 0.0001\ \Omega$
b) $R_{fault} = 0.001\ \Omega$
c) $R_{fault} = 0.01\ \Omega$
d) $R_{fault} = 0.1\ \Omega$
e) $R_{fault} = 1\ \Omega$
f) $R_{fault} = 10\ \Omega$

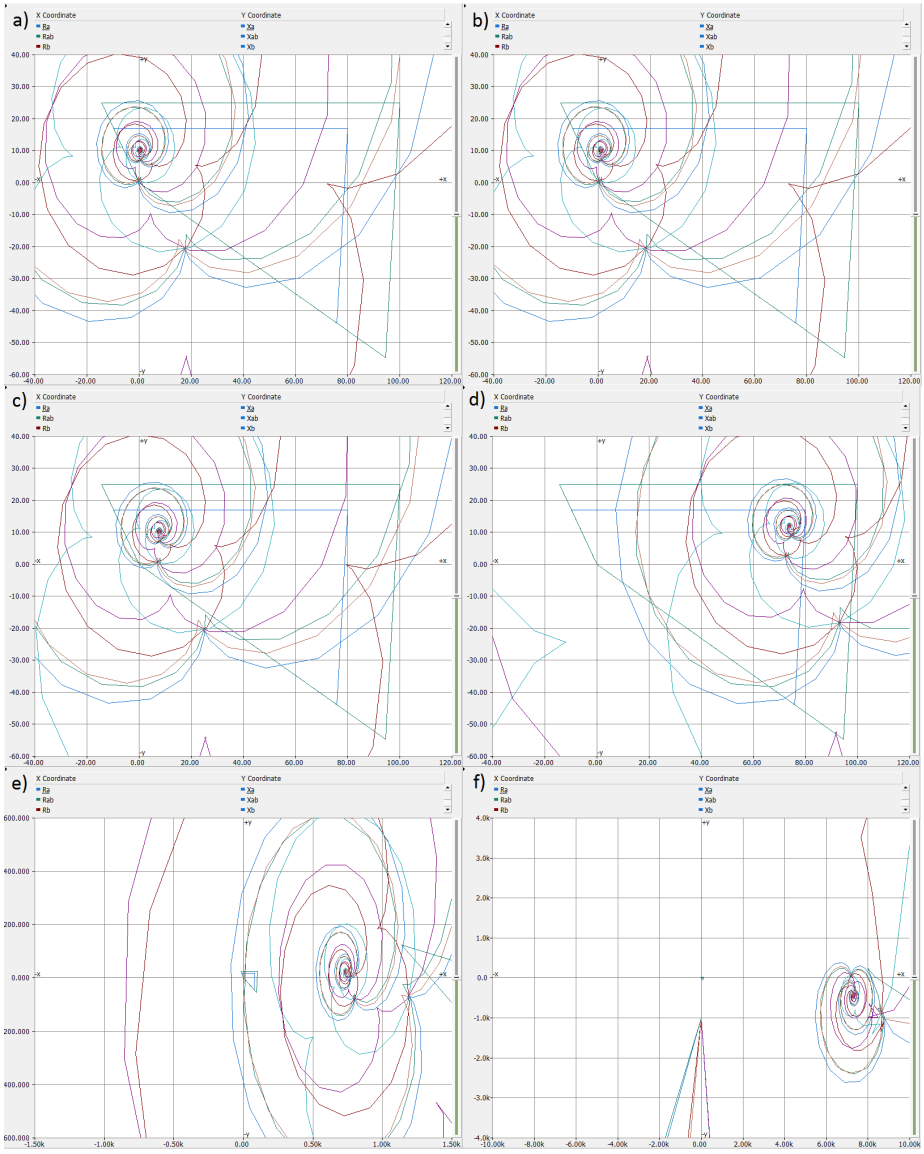

Figure 78: Relay 1 impedance diagrams for infeeder generation only and $|Z_{infeeder}|$ set to 25760 Ω, for different values of R_{fault}. The selected model parameters are given in Table 12, except for $|Z_{infeeder}|$, and that no inverters were connected to PCC.

a) $R_{fault} = 0.0001\ \Omega$ $Z_a = 0.4247 + \text{j}10.03\ \Omega$
b) $R_{fault} = 0.001\ \Omega$ $Z_a = 1.159 + \text{j}10.05\ \Omega$
c) $R_{fault} = 0.01\ \Omega$ $Z_a = 7.766 + \text{j}10.22\ \Omega$
d) $R_{fault} = 0.1\ \Omega$ $Z_a = 73.84 + \text{j}11.87\ \Omega$
e) $R_{fault} = 1\ \Omega$ $Z_a = 734.7 + \text{j}22.7\ \Omega$
f) $R_{fault} = 10\ \Omega$ $Z_a = 7302 - \text{j}442.6\ \Omega$

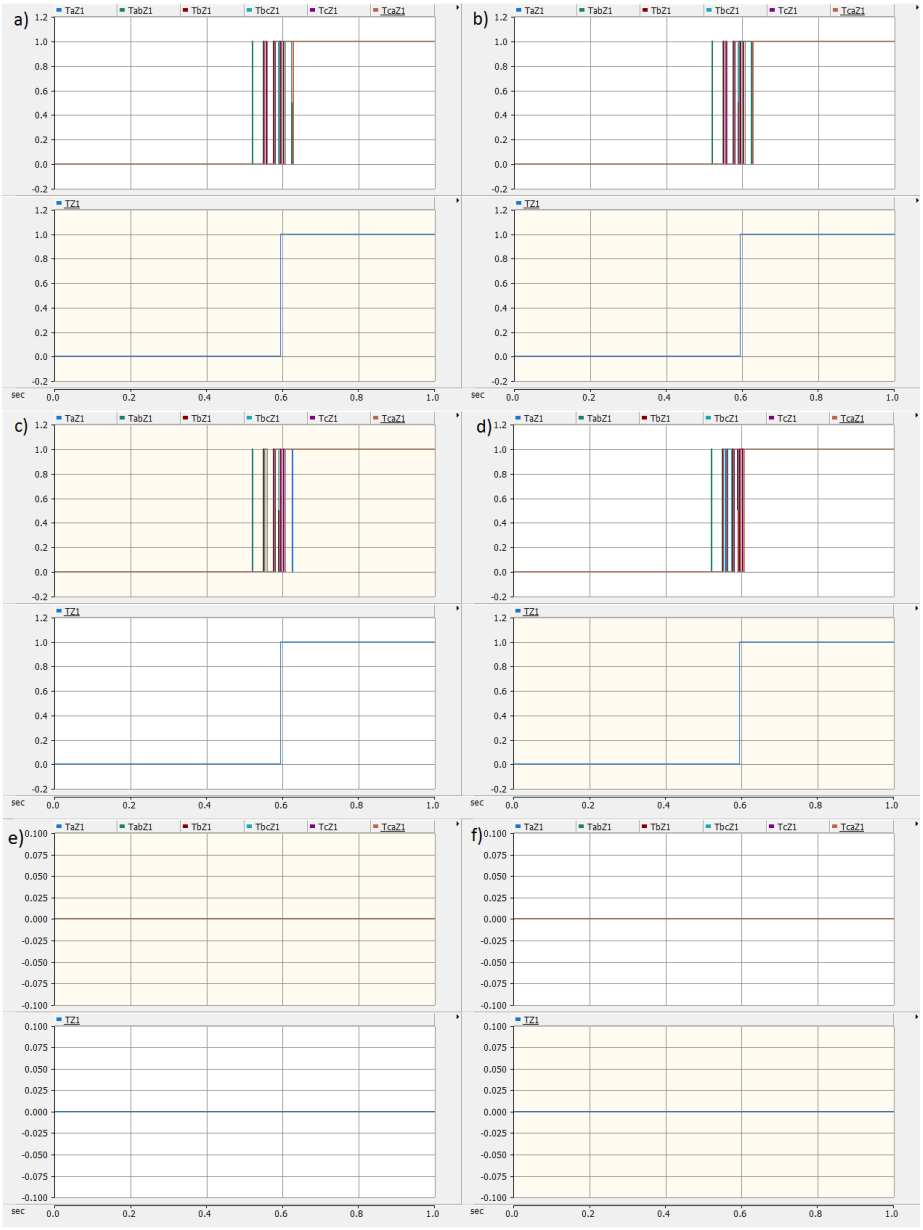

Figure 79: Relay 1 trip times for infeeder generation only and $|Z_{infeeder}|$ set to 25760 Ω, for different values of R_{fault}. The selected model parameters are given in Table 12, except for $|Z_{infeeder}|$, and that no inverters were connected to PCC. The trip times t_{trip} includes the 0.5 s before fault initiation.

a) $R_{fault} = 0.0001\ \Omega$ $t_{trip} = 0.6537$ s
b) $R_{fault} = 0.001\ \Omega$ $t_{trip} = 0.6537$ s
c) $R_{fault} = 0.01\ \Omega$ $t_{trip} = 0.6537$ s
d) $R_{fault} = 0.1\ \Omega$ $t_{trip} = 0.6587$ s
e) $R_{fault} = 1\ \Omega$ $t_{trip} =$ -
f) $R_{fault} = 10\ \Omega$ $t_{trip} =$ -

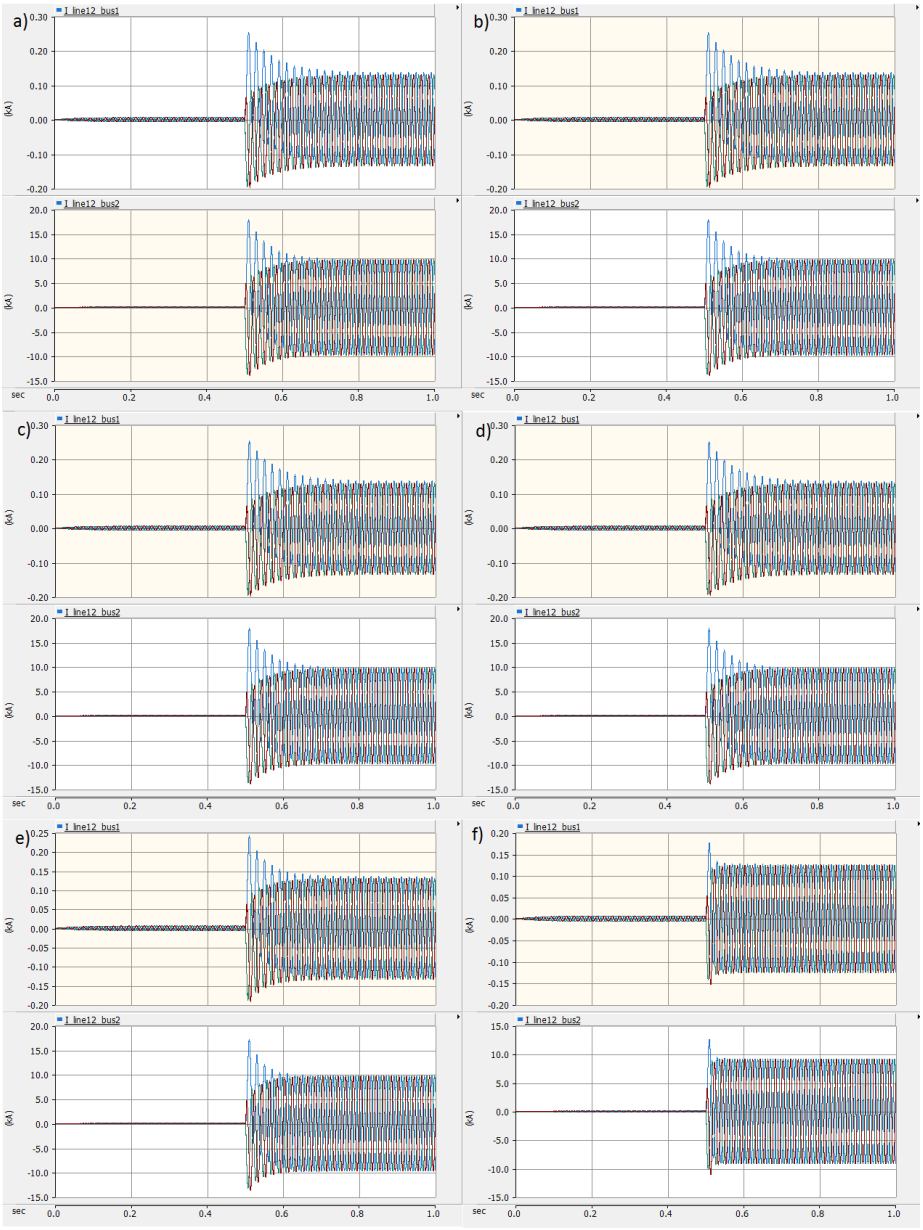

Figure 80: Current contributions for infeeder generation only and $|Z_{infeeder}|$ set to 25760 Ω, for different values of R_{fault}. The selected model parameters are given in Table 12, except for $|Z_{infeeder}|$, and that no inverters were connected to PCC. During the faulted period, $\frac{I\_line12\_bus2}{I\_line12\_bus1} \approx 732$.

a) $R_{fault} = 0.0001\ \Omega$
b) $R_{fault} = 0.001\ \Omega$
c) $R_{fault} = 0.01\ \Omega$
d) $R_{fault} = 0.1\ \Omega$
e) $R_{fault} = 1\ \Omega$
f) $R_{fault} = 10\ \Omega$

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PSCAD Simulation of Distance Protection Performance in a Grid with Inverter Interfaced Generation

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Science and Technology