Master's thesis

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Faculty of Information Technology and Electrical Engineering
Department of Electronic Systems

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Ultra-low power accurate temperature sensor for IoT

Master's thesis in Electronic Systems Design

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Summary

The analog front-end of a proposed BJT-based temperature sensor has been designed. The design has been analysed using Monte-Carlo simulations with mismatch over all process corners. The design was implemented in a 90nm generic process design kit. The analog front-end achieves ultra-low power consumption with a current consumption of 2.3 µA at a temperature of 27 °C and can operate over the military temperature range of -55 °C - 125 °C. It uses a voltage supply of 2 V.
An adaptive self-biasing operational amplifier was implemented in the bandgap reference circuit to ensure sufficiently high DC loop-gain. It operates on an ultra-low current consumption of 631 nA. To reduce errors due to mismatch and process spread two correction techniques have been employed, that is chopping of the input signals of the operational amplifier and dynamic element matching of the current sources in the bipolar core.
The residual temperature reading error at the output of the analog front-end is large and results in significant errors. This is because no compensation technique was implemented in the analog front-end to compensate for process spread of the BJTs and should be implemented digitally. The temperature reading errors due to offset and mismatch in the current sources have been reduced to around 0.03 °C at a temperature of 27 °C. The noise in the circuit was analysed without the dynamic effects of the DEM because of its simple implementation and results in an equivalent temperature error of around 0.12 °C, which indicates the resolution that is achievable. The settling time of the circuit is in the range of 110 µs.

Acknowledgement

I would like to thank my supervisor Professor Snorre Aunet at NTNU for agreeing to supervise this project and helping me with words and deeds.
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Also I would like to thank my family for making it possible for me to pursue a master's degree in Norway and always supporting me on my way.

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List of Abbreviations

Abbreviation	Definition
ADC	Analog-to-digital converter
AC	Alternating current
BJT	Bipolar junction transistor
CTAT	Complementary to absolute temperature
CMOS	Complementary metal-oxide-semiconductor
DC	Direct current
DEM	Dynamic Element Matching
FoM	Figure of merit
GBW	Gain-bandwidth product
LAN	Local area network
MOSFET	Metal-oxide-semiconductor field-effect transistor
MC	Monte-Carlo
Op amp	Operational amplifier
NMOS	n-channel MOSFET
PMOS	p-channel MOSFET
PTAT	Proportional to absolute temperature
REF	Reference
SAR-ADC	Successive-approximation ADC
Std dev	Standard deviation
TC	Temperature coefficient
$\Delta\Sigma$-ADC	Sigma-delta ADC

List of Symbols

Symbol	Definition	Unit
A	Constant, equal to 600 K	K
A_v	Voltage gain	V/V
A_{Vt0}	Process dependent parameter	Vμm
A_K	Process dependent parameter	%μ
B	Constant, equal to -273 K	K
C_D	Depletion layer capacitance	F
C_{ox}	Gate-oxide capacitance	F
D_{out}	Temperature reading at the output of the sensor	°C
g_m	Transconductance	S
I_D	Drain current	A
I_S	Saturation current	A
I_C	Collector current	A
I_E	Emitter current	A
I_B	Base current	A
k	Boltzmann constant	J/K
k_f	Flicker noise constant	
L	Gate length of a MOSFET	m
p	Current density ratio	
q	Electron charge	C
R_B	Base resistance of a BJT	Ω
R_E	Emitter resistance of a BJT	Ω
R_b	Bias resistor	Ω
r_{ds}	Drain-source resistance	Ω
T	Absolute temperature	K
V_{BE}	Base-emitter voltage	V
V_{PTAT}	Proportional to absolute temperature dependent voltage	V
V_{REF}	Reference voltage	V
V_{GS}	Gate-source voltage	V
V_{th}	Threshold voltage	V
V_{DD}	Supply voltage	V
V_t	Thermal voltage	V
V_{g0}	Silicon bandgap voltage	V
V_{os}	Offset voltage	V
V_{ov}	Overdrive voltage	V
W	Gate width of a MOSFET	m
α	Scaling factor	
α_{TCR}	Temperature coefficient	1/K
α_F	Common-base current-gain	

β_F	Forward current-gain of BJT	
μ	Electron mobility	$cm^2/(Vs)$
μ	ADC output	
ΔV_{BE}	Difference voltage of V_{BE2} and V_{BE1}	V
σ	Standard deviation	

Chapter 1

Introduction

Temperature sensors are used in many measurement, instrumentation and control systems, and even in households they are employed in various places. Examples of where temperature sensors are used are coffee machines, computers, heating systems or cars ([1], p. 1). This makes the temperature to the most-often measured environmental quantity, which leads to a large market. Therefore, it makes sense to integrate temperature sensors on chip with a readout circuitry that provides a digital output to reduce manufacturing costs to a minimum. Such temperature sensors are called *smart temperature sensor*. These sensors are able to directly communicate with computers in a standardised digital format. Nowadays, the digital output is almost mandatory in modern systems ([1], p. 2). Low-power radio systems have become more and more important in recent years which is why wireless temperature sensing has become very attractive for a many applications. Examples are in automotive, building automation or healthcare ([2], p. 1.).
Wireless sensors can be implemented as spatially distributed nodes in a wireless sensor network, which were introduced in the 2000s. Physical or environmental quantities can be measured and monitored by smart sensors, and due to the integrated analog-to-digital converter (ADC) a digital output is generated that is sent to a control unit via the wireless network. This control unit can either be centralised or distributed and receives the data for further processing. ([2], p. 2)
A smart temperature sensor is depicted in figure 1.1, it consists of an analog front-end which includes a temperature sensing circuit and a bias circuit. Additionally, an ADC is present that converts the temperature reading from voltages or currents to a digital format which is then communicated to another system through a digital interface. This digital interface can be, for example, I^2C for a wired sensor, or wireless local area network (LAN) for a wireless sensor ([1], p. 4), [3].
There are different techniques of designing temperature sensors that exploit the temperature dependency of the device characteristics. The output of the temperature sensing circuit is usually a temperature-dependent analog signal, such as a voltage, current, period or frequency ([1], p. 3). Which is indicated as temperature-dependent voltage V_{PTAT} in figure 1.1. PTAT stands for proportional to absolute temperature which means it has a

linear and positive increase with rising temperature. However, to implement a smart temperature sensor a second analog signal is required to produce a digital representation of the temperature. In this case, it is a reference voltage V_{REF} to which V_{PTAT} is compared. This kind of measurement is called a ratiometric measurement ([1], p. 3).
The scope of this thesis is to design the analog front-end of a bipolar junction transistor (BJT) based temperature sensor with ultra-low power consumption. The temperature sensor is to be implemented on-chip for wireless operation, hence the ultra-low power consumption.
The thesis is organised as follows, chapter 2 will describe different sensing methods used in smart temperature sensors and gives a brief overview of achieved performances. Chapter 3 describes the theory of the temperature sensing method using BJTs and their non-idealities. In chapter 4, different correction and compensation techniques are presented to improve the performance. The design of the analog front-end of the chosen temperature sensor is explained in chapter 5. Chapter 6 deals with the simulations that are conducted in the simulation program Cadence Virtuoso to verify the design. The final result will then be analysed using Monte-Carlo (MC) simulations. The last chapter 7 will conclude the thesis and will give an outlook for future work.

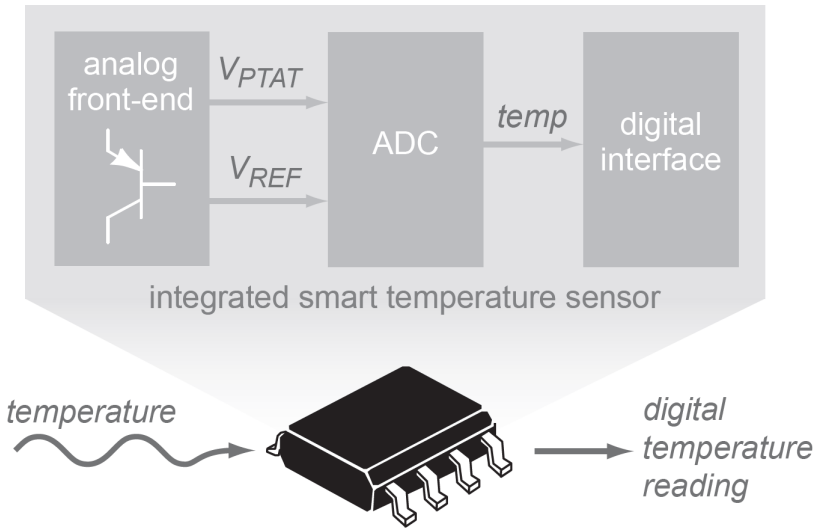


Figure 1.1: Block diagram of a smart temperature sensor. It shows the different parts included on the chip ([1], p. 3).

1.1 Pre-Study

This master's thesis is based on the findings of a pre-study that was conducted as a part of the two years master's programme at NTNU, Trondheim, at the Department of Electronic Systems [4]. During the pre-study a literature review was conducted with the aim of finding and comparing reported sensor architectures to obtain an architecture that fulfils the requirements. These requirements were set beforehand and are listed here [4]:

- Ultra-low power consumption
- Sampling speed of 1 to 100 samples per second
- One temperature calibration after manufacturing
- Temperature range from -40 °C to +100 °C
- Absolute accuracy within 0.5 °C from 0 °C to 65 °C
- Resolution of 0.25 °C from 0 °C to 65 °C
- Implemented on-chip in 0.18 µm CMOS technology.

A total of 20 articles, comprising different types and architectures of temperature sensors, were compared based on two figure of merits (FoM) and their overall performance. Table 1.1 was extracted from [4] and shows the performance parameters of the two sensors (BJT-sensor [5] and MOS-sensor [6]) that were deemed to be the most promising. At the bottom of the table the two FoMs are compared. The lower the value, the better the performance. It can be seen that the MOS-sensor ([6]) has lower FoM-values than the BJT-sensor ([5]). However, as is described in [4], the BJT-based sensor shows an overall good performance which fulfils all the requirements. The comparatively high power consumption can be reduced by decreasing the resolution and/or the accuracy, as well as the conversion time. One very important aspect is the calibration of the sensor. The MOSFET-based sensor is calibrated with a more expensive 2-point calibration, whereas the BJT-sensor only uses a fast 1-point voltage calibration. The combination of these characteristics is the reason why the BJT-sensor was deemed more promising. The architecture of the BJT sensor is described in chapter 2.3.

Table 1.1: Parameter list of the chosen temperature sensors. Excerpt from [4].

Parameters	**2** [5]	**17** [6]
Sensor type	BJT	MOSFET
CMOS Technology	0.16 µm	65 nm
Chip Area	0.08 mm^2	0.013 mm^2
Power	5.1 µW	640 pW
Supply Voltage	1.5 V - 2 V	1.2 V (V_{DDH}) 0.5 V (V_{DDL})
Temp. Range	-55 °C - +125 °C	-20 °C - +100 °C
Inaccuracy	±0.15 °C	-2.7 °C / +1.8 °C
Resolution	0.02 °C	0.25 °C
Calibration	voltage 1-point	2-point
Conv. Time	5.2 ms	34.3 ms
Energy/Conv.	27 nJ	0.022 nJ
Resolution-FoM	0.0108 nJK^2	0.001375nJK^2
Project-FoM	0.0009 nJK	0.00020625 nJK
Voltage Sensitivity	0.5 °C / V	

Chapter 2

Literature Review

2.1 Introduction

In section 2.2 a brief overview of different temperature sensing methods that are used in state-of-the-art sensors is given, as well as a brief description of their functionality and the achieved results of state-of-the-art chips. Afterwards, a short outline of the functionality of the chosen temperature sensor is presented in section 2.3.

2.2 Temperature Sensing Methods

2.2.1 Resistor-based Sensors

Temperature sensors based on resistors are widely used. Most of the CMOS-compatible resistors have a high temperature-coefficient which is desirable because the temperature is measured based on the resistance variations. Typical temperature coefficients of resistors in CMOS are between 0.1 %/°C and 0.4 %/°C, depending on the resistor type, according to [2]. This means that the resistance value can change about 72 % over a temperature range of -55 °C to 125 °C. Resistor-based sensors can function on very low voltages which is then limited by the minimum supply voltage of the readout circuit.
However, the drawback is that resistors suffer from strong processing spread. In typical CMOS-processes these resistance spreads can be as high as 15 % or 20 %. In addition, the temperature coefficients are also affected by processing spread and higher order non-linearities. That is why this type of temperature sensor can be rather costly since it needs multiple temperature calibrations. ([2], p. 8-9)
Temperature sensors based on resistors are reported to have temperature ranges of -40 °C to +180 °C and achieve inaccuracies of ± 0.15 °C (for a standard deviation of 3σ) over a temperature range of -55 °C to +85 °C, after trimming the sensor at three temperatures according to [2]. Another sensor is reported to achieve an inaccuracy of ± 1 °C over a range of -45 °C to +125 °C ([2], p. 9).

2.2.2 Thermal Diffusivity Sensors

According to [2], the thermal diffusivity of silicon is well defined and exhibits a highly temperature dependent characteristic. It is a rate at which the heat diffuses through a silicon substrate which can be used to design temperature sensors. The thermal diffusivity D can be approximated by $D \propto 1/T^{1.8}$.
The working principle is shown in figure 2.1. It uses a heater to generate heat pulses which are sensed by a relative temperature sensor, a thermopile, which is placed at a known distance from the heater. The received heat pulses are converted into a small voltage signal. Current pulses with a constant frequency are sent through the substrate while dissipating power into the substrate. This results in temperature fluctuations which also propagate through the substrate and are then sensed by the thermopile. The delay between the pulses of the heater and the sensed temperature fluctuations is related to D. [3]

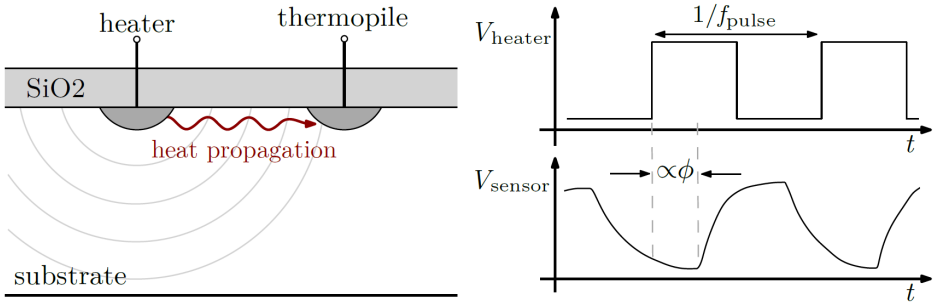


Figure 2.1: Operating principle of a thermal diffusivity based sensor ([7], p. 15).

However, such a temperature sensor is not suited for low-power operation because of the energy required for the heat pulses. Yet, it is possible to design sensors with decent accuracies without trimming. Sensors with accuracies of ±0.2 °C and ±0.5 °C (3σ) over a temperature range from -55 °C to +125 °C are reported. Therefore, this type of sensor can be a solution in applications where uncalibrated accuracy is important, while the power consumption is of second interest. ([2], p. 9-10)

2.2.3 MOSFET-based Sensors

MOSFETs are well defined and optimised in CMOS processes and therefore it is of benefit to use MOSFETs as temperature sensing elements [3]. In addition, when MOS transistors are biased in sub-threshold region their power consumption is very low. When a MOSFET is operated in the sub-threshold region its drain current I_D and the gate-source voltage V_{GS} are temperature-dependent exponentially related which is a similar relation as exhibited by the bipolar junction transistor. Equation 2.1 shows the exponential relationship of I_D and V_{GS} ([2], p. 10).

$$I_D \propto \frac{W}{L} exp\left[\frac{q}{mkT} \cdot (V_{GS} - V_T)\right] \tag{2.1}$$

In this equation, k is the Boltzmann's constant, T the absolute temperature, q the electron charge, W and L are the width and the length respectively and m the body effect coefficient, which is computed as $m = 1 + C_D/C_{OX}$. Here, C_D is the depletion-layer and C_{OX} is the gate-oxide capacitance.
It is possible that the MOSFET replaces the BJT as sensing element. Though, the MOS transistor performance is dependent on the processing spread of two parameters which results in greater inaccuracies. The parameters that are suffering from processing spread are the threshold voltage V_T and the oxide capacitance C_{OX}. Nevertheless, the MOSFET offers the possibility of low supply voltage operation, due to the fact that it is biased in sub-threshold region as mentioned above. Therefore, the gate-source voltage is significantly lower as in saturation region and can be controlled by sizing W or L ([2], p. 11).

Another method of measuring the temperature is the propagation delay of a CMOS inverter chain or the frequency of a ring oscillator. The operating principle is shown in figure 2.2. It uses a counter to measure the propagation delay where the delay T_P in an inverter consisting of PMOS and NMOS transistors can be written as follows ([2], p. 11), [3]:

$$T_P = \frac{\left(\frac{L}{W}\right) \cdot C_L}{\mu C_{OX}(V_{DD} - V_{th})} \cdot ln\left[\frac{3V_{DD} - 4V_{th}}{V_{DD}}\right]. \tag{2.2}$$

The mobility μ and the threshold voltage V_{th} are temperature dependent. Due to processing spread it is usually necessary to perform a two-point calibration, and in addition it suffers from very high power supply sensitivity, which can be in the range of 10 °C/V ([2], p. 11). A temperature range from -20 °C to +100 °C are reported with inaccuracies of several degrees [8].

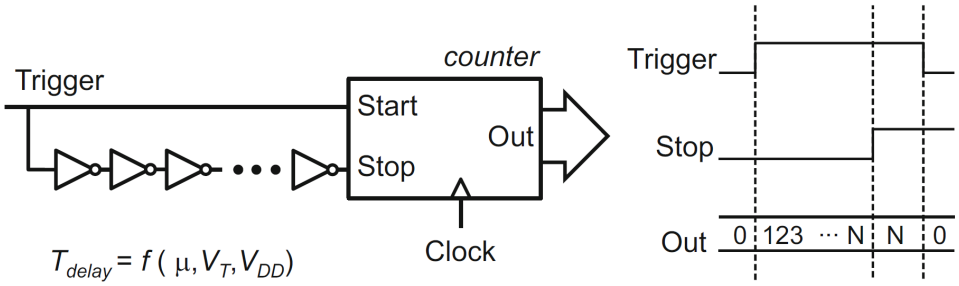


Figure 2.2: Block diagram of the alternative temperature measurement, based on MOSFET inverter delay ([2], p. 11).

2.2.4 BJT-based Sensors

The sensor type that is used in this thesis (the process of choosing this architecture was explained in section 1.1) is based on the bipolar junction transistor and its temperature characteristics. These characteristics exploit two voltages, which is the thermal voltage $V_t = kT/q$ (where k is the Boltzmann constant, T is the absolute temperature and q is the electron charge) and the silicon bandgap voltage V_{g0}, for a ratiometric measurement. Figure 2.3 shows that it is possible to use the thermal voltage to generate a voltage V_{PTAT} that is proportional to absolute temperature (PTAT) while the bandgap voltage is used to generate the temperature-independent reference voltage V_{REF} ([1], p. 4).

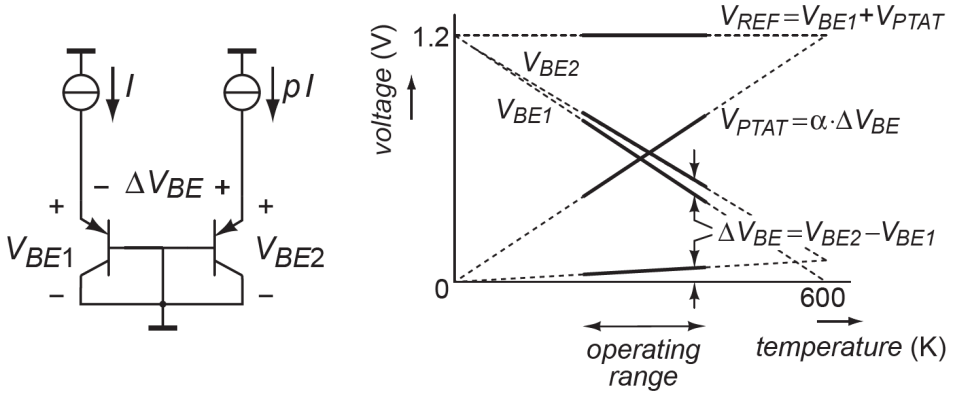


Figure 2.3: Operation principle of a BJT-based CMOS smart temperature sensor. a) Two diode-connected transistors are biased at a well-defined current density ratio 1:p; b) the in that way generated base-emitter voltages are generating the voltage V_{PTAT} and V_{REF} for the ratiometric measurement ([1], p. 4).

The two diode-connected transistors are biased at a precise current density ratio p. This results in two base-emitter voltages V_{BE1} and V_{BE2} that are complementary to absolute temperature (CTAT) in nature. The difference between these two base-emitter voltages generates the PTAT voltage ΔV_{BE}. Since this voltage is rather small it has to be amplified to be useful, which is then the voltage $V_{PTAT} = \alpha \cdot \Delta V_{BE}$ [[1], p. 4), [3].
As can also be seen from figure 2.3 b) is that the reference voltage V_{REF} is based on the absolute base-emitter voltage of a BJT. If the base-emitter voltage is extrapolated to T = 0 K it equals the silicon bandgap voltage V_{g0} of around 1.2 V. From there, it decreases by about 2 mV/K (equation 2.5) which is why the amplified difference voltage is added to the base-emitter voltage. The reference voltage is approximately temperature-independent ([1], p.5).
The scaling factor α can be calculated by taking the equation for V_{REF}:

$$V_{REF} = V_{BE} + \alpha \cdot \Delta V_{BE}, \tag{2.3}$$

and solving it such that the temperature coefficient of V_{REF} is zero ([2], p. 23):

$$S^T_{V_{BE}} = \left| \frac{\partial V_{BE}}{\partial T} \right| \approx 2mV/°C = \alpha \cdot \frac{k}{q} \cdot ln(p). \tag{2.4}$$

Thus, the scaling factor is found to be approximately:

$$\alpha \approx \frac{S^T_{V_{BE}}}{\frac{k}{q} ln(p)}. \tag{2.5}$$

The bipolar transistors that are used for the temperature sensing core are vertical bipolar junction transistors. Vertical PNP BJTs are less prone to processing spread and packaging stress but they are, however, less flexible in terms of implementation. This is due to the collector being inside the P-substrate, and therefore, not directly accessible which is shown in figure 2.4.
The typical forward current gain β_F of a vertical PNP transistor is in the range of 3 to 4, which is rather small compared to the forward current gain of vertical NPN transistors ($\beta_F \approx 24$) ([2], p. 7). This results in a relatively large base current and this in turn in lower sensitivity to non-ideal higher order components in the saturation current I_S of the BJT.
The overall well-defined temperature dependency of V_{BE} and ΔV_{BE} makes the BJT-based temperature sensor attractive for industrial use. According to [2], temperature sensors with a one-point trim and accuracies of $\pm$0.5 °C (3σ) over a temperature range of -50 °C to +120 °C, and $\pm$0.1 °C (3σ) from -55 °C to +125 °C are reported. An additional advantage is that the temperature dependent voltages and the reference voltage are generated from the same circuit which greatly simplifies the implementation ([2], p. 8).

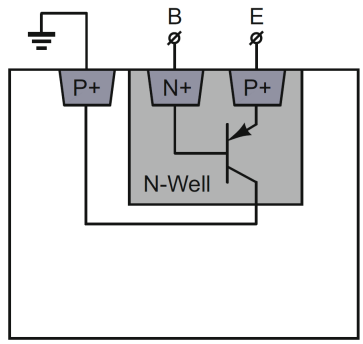


Figure 2.4: Cross section of a vertical PNP transistor in a standard CMOS process ([2], p. 7).

The generic readout of BJT-based sensors scales the generated ΔV_{BE} voltage, as was already mentioned in equation 2.3 and shown in figure 2.3. This can be seen in figure 2.5 where the reference voltage and the PTAT voltage are applied to an ADC. The ADC output μ is then scaled to generate the according digital temperature reading D_{out}. The ratio μ can be calculated as follows ([2], p. 23)

$$\mu = \frac{\alpha \cdot \Delta V_{BE}}{V_{BE} + \alpha \cdot \Delta V_{BE}} = \frac{V_{PTAT}}{V_{REF}}. \tag{2.6}$$

This ratio is PTAT and varies between 0 and 1 over a temperature range of 600 K. The digital output D_{out} can be expressed as

$$D_{out} = A \cdot \mu + B, \tag{2.7}$$

where A = 600 K and B = -273 K ([2], p. 23).

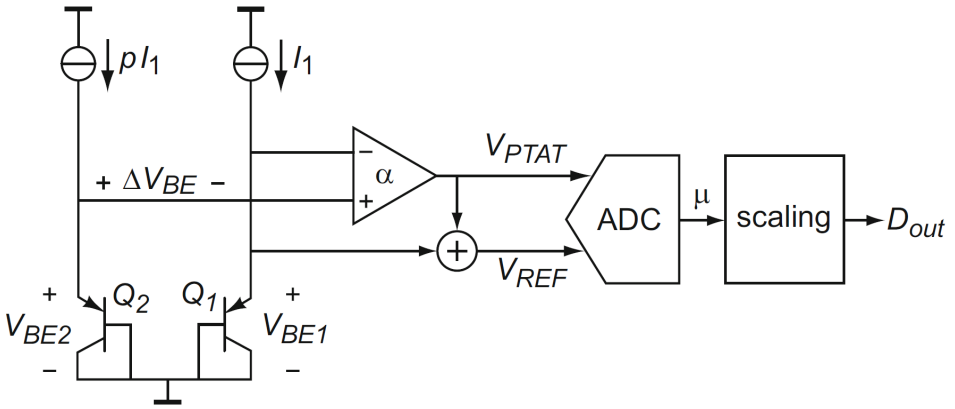


Figure 2.5: Bias core and generic readout circuit of BJT-based bandgap temperature sensors ([2], p. 24).

2.3 Chosen Temperature Sensor

The chosen temperature sensor ([5]) is, as stated in 1.1, based on BJTs and the bandgap reference architecture described in 2.2.4 and shown in figure 2.3. However, instead of generating the reference voltage $V_{REF} = V_{BE1} + \alpha \cdot \Delta V_{BE}$ it is sufficient to use the ratio $X = V_{BE1} / \Delta V_{BE}$ which contains all necessary information. A block diagram is shown in figure 2.6.

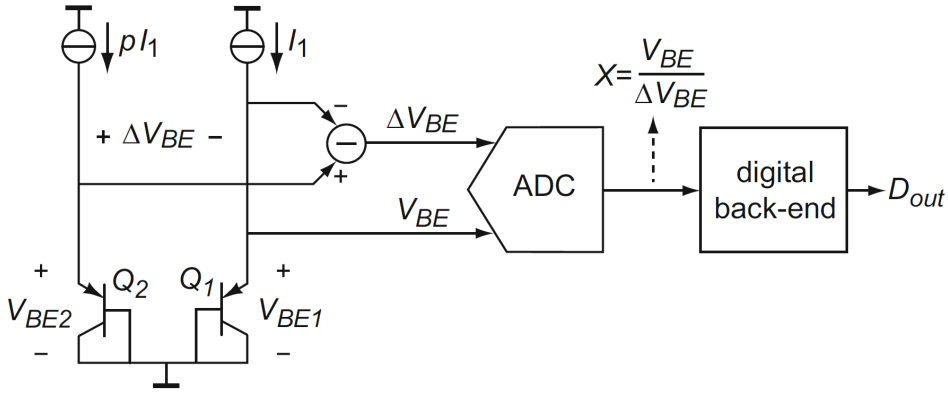


Figure 2.6: Circuit diagram of the proposed sensor. It consists of the bias circuit (not shown), the sensing circuit, the ADC and the digital backend and uses the ratio X to determine the temperature ([2], p. 39.).

The ratio $X = V_{BE1} / \Delta V_{BE}$ is a non-linear, monotonic function of the temperature for a current density ratio p = 5 (shown in figure 2.7). This temperature dependency can be linearised to:

$$\mu = \frac{\alpha}{\alpha + X}, \tag{2.8}$$

and then implemented in the digital backend.
Next to the analog front-end with the biasing and sensing circuits, a 2nd-order Zoom-ADC is existent. It consists of a coarse 5-bit SAR-ADC and a fine 10-bit $\Delta\Sigma$-ADC. The Zoom-ADC firstly finds the coarse temperature range which lies between the integers n and n+1. During the coarse conversion phase a clocked comparator compares the base-emitter voltage V_{BE} to integer multiples of ΔV_{BE}. Five steps are executed in which the SAR-ADC adjusts the scaling factor until the integer n is found. Afterwards, the fine conversion zooms into this range and finds the fraction part of the temperature value. A block diagram of the Zoom-ADC is shown in figure 2.8. Every cycle of the fine conversion requires an integration. The voltages V_{BE} and ΔV_{BE} are sampled during the same clock cycle and integrated the next cycle. Thus, the conversion time can be reduced by half, which in turn improves the energy efficiency.

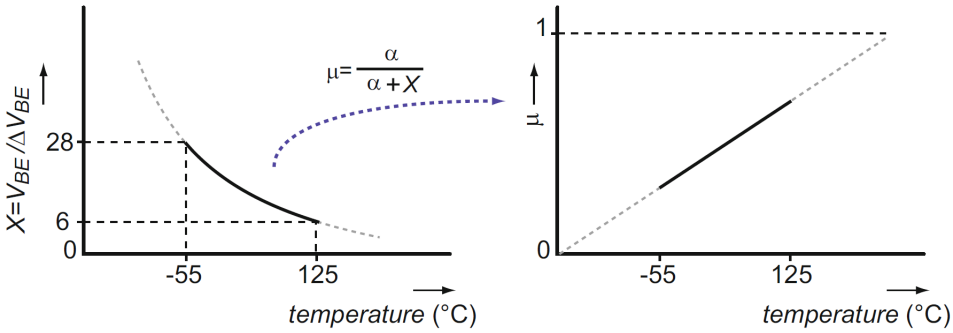


Figure 2.7: Non-linear, monotonic function of X and the linearised function μ as a function of the temperature ([2], p. 40).

The zoom-in phase reduces the complexity of the ADC and the power consumption because it reduces the resolution requirements on the ΔΣ-ADC. In addition, a second order Zoom-ADC is employed instead of a first order ADC which was done in previous works. This approach shows significant improvements in speed and energy conversion.

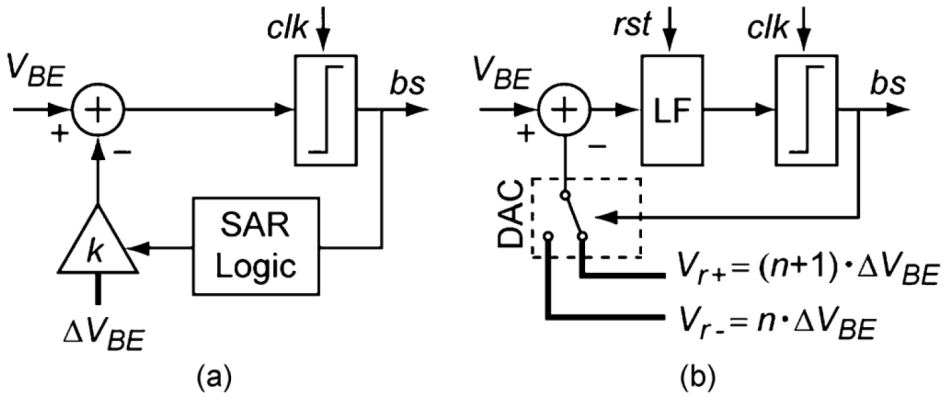


Figure 2.8: Block diagram of the Zoom-ADC during a) coarse and b) fine conversion [5].

Chapter 3

The Parasitic Vertical PNP BJT

3.1 Introduction

Chapter 3 describes the physics and characteristics of bipolar junction transistors. First, a categorisation of random and systematic errors is given in section 3.2. Afterwards in section 3.3, the ideal characteristics of the BJT are described. Hereinafter, the non-idealities of the I-V-Characteristics are explained in section 3.4 which are causing inaccuracies in the currents and voltages. In addition to the non-idealities, processing spreads and temperature dependencies are adding to errors in the temperature reading at the output of the sensor. In the end, the noise model of the BJT and MOSFET will be briefly explained (section 3.7).

In the literature it is common to use the same sign conventions for PNP as for NPN transistors, also indicated in figure 3.1. This means, the base-emitter voltage of the PNP transistor is called V_{BE} and difference voltage ΔV_{BE} instead of the technically correct terms V_{EB} and ΔV_{EB}. Therefore, V_{BE} should be read as $|V_{BE}|$ or V_{EB}.

3.2 Error Definition

The error sources in a temperature sensor can be distinguished in different categories, systematic errors, random errors and process errors ([1], p. 55, [9], p. 96).
Systematic errors are predictable and the same for each sensor. It is possible to correct them by design. An example for a systematic error is the curvature of the V_{BE} voltage ([1], p. 55).
Random errors on the other hand are unpredictable and vary from sensor to sensor but they are zero on average. These errors are statistical in nature and are present in each sensor. An example is the mismatch of two transistors that were fabricated under the same nominal conditions ([1], p. 55, [9], p. 96).
Process errors result from the manufacturing process which conditions can never be kept precisely the same (temperature, concentration levels, oxide thickness, etc.). Therefore,

the nominal properties of a circuit differ from sample to sample ([9], p. 96).

3.3 Ideal I-V-Characteristics

The collector current, and therefore the collector current base-emitter voltage relation of a bipolar junction transistor can be written as ([1], p. 16)

$$I_C = I_S \cdot exp\left(\frac{qV_{BE}}{kT}\right). \tag{3.1}$$

The saturation current I_S is given by ([1], p. 16)

$$I_S = \frac{qA_E n_i^2 \overline{D_p}}{W_B N_d} = \frac{kTA_E n_i^2 \overline{\mu_p}}{G_B}, \tag{3.2}$$

where q is the elementary charge of an electron, A_E is the emitter area, n_i is the intrinsic carrier concentration, D_p is the average diffusion constant of holes in the base, W_B is the base width and N_d is the donor concentration. The product $W_B N_d$ indicates the number of impurities per unit area of the base, and is also called Gummel number G_B. The effective hole diffusion constant $\overline{D_p}$ can be expressed as

$$\overline{D_p} = \frac{kT}{q} \cdot \overline{\mu_p}. \tag{3.3}$$

The variable $\overline{\mu_p}$ is the effective hole mobility, T is the absolute temperature and k the Boltzmann constant.
By rearranging equation 3.1, it is thus possible to express the ideal base-emitter voltage as follows

$$V_{BE} = \frac{kT}{q} \cdot ln\left(\frac{I_C}{I_S}\right). \tag{3.4}$$

3.4 Non-Idealities of the I-V-Characteristics

In practice, non-ideal currents have to be taken into account that affect the accuracy of the difference voltage $\Delta V_{BE} = V_{BE2} - V_{BE1}$.
Generation of carriers in the base-collector junction and diffusion of minority electrons in the collector result in leakage currents. Therefore, the PNP transistors are used in a diode-connected configuration (figure 3.1), where the base-collector voltage is set to zero, which reduces the leakage current to negligible levels ([2], p. 20, [1], p. 17).
To account for these differences in the hole concentration the collector current is thus ([1], p. 17)

$$I_C = I_S \cdot exp\left(\frac{qV_{BE}}{kT} - 1\right). \tag{3.5}$$

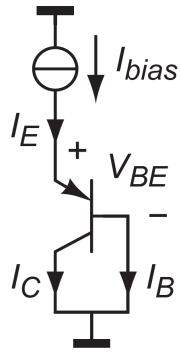


Figure 3.1: Diode-connected PNP transistor and the indicated base-emitter voltage drop V_{BE} ([1], p. 19).

This results in a better approximation of the base-emitter voltage V_{BE}

$$V_{BE} = \frac{kT}{q} \cdot ln\left(\frac{I_C + I_S}{I_S}\right). \tag{3.6}$$

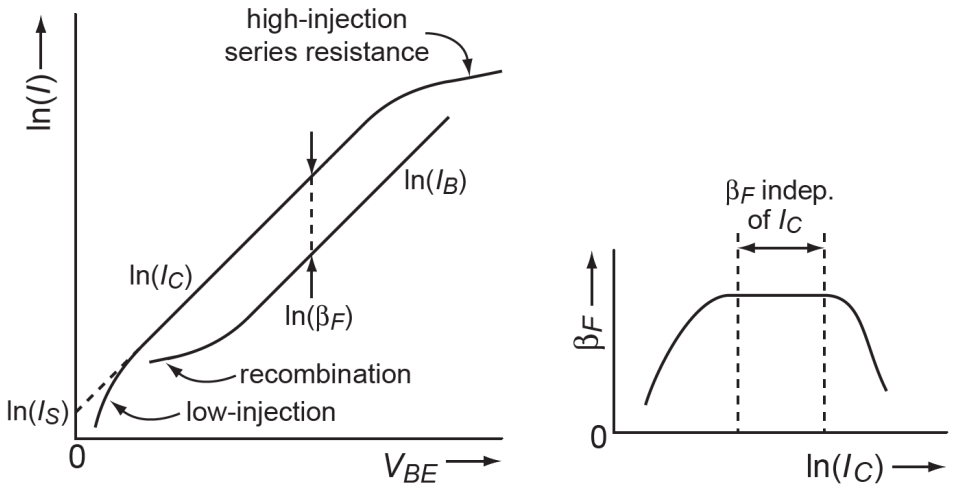
Accordingly, the difference voltage ΔV_{BE} is calculated as follows, by taking the base-emitter voltages of the two PNP transistors in the sensing circuit (compare figure 2.3)

$$\begin{aligned} \Delta V_{BE} = V_{BE2} - V_{BE2} &= \frac{kT}{q} \cdot ln\left(\frac{p \cdot I_C + I_S}{I_S}\right) - \frac{kT}{q} \cdot ln\left(\frac{I_C + I_S}{I_S}\right) \\ &= \frac{kT}{q} \cdot ln\left(\frac{p \cdot I_C + I_S}{I_S} \cdot \frac{I_S}{I_C + I_S}\right) = \frac{kT}{q} \cdot ln\left(\frac{p \cdot I_C + I_S}{I_C + I_S}\right) \end{aligned} \tag{3.7}$$

The term kT/q is the thermal voltage V_t which equals around 26 mV at room temperature. Even though the voltage seems to have a positive temperature coefficient, it is actually negative due to the strong temperature dependency of I_S ([2], p. 21). This will be explained in the sections 3.5 and 3.6.
As long as the collector current I_C is significantly larger than the saturation current I_S it is possible to say that

$$\Delta V_{BE} = \frac{kT}{q} \cdot ln(p). \tag{3.8}$$

This indicates that the collector current should be chosen as high as possible. However, it cannot be chosen arbitrarily high. Self-heating and a considerable voltage drop across series resistances are results of a current that is too high. According to ([1], p. 17), the second reason is that the transistor would enter the high-injection region. In this region the concentration of the minority carrier is low in comparison to the majority carrier concentration. That means that the logarithm of the collector current $\ln(I_C)$ becomes proportional to $qV_{BE}/(2kT)$. Figure 3.2 shows this effect and the plotted collector current and current-gain.



(a) (b)

Figure 3.2: a) The collector current I_C and the base current I_B are shown as a function of the base-emitter voltage V_{BE}; b) the corresponding forward current-gain β_F versus the collector current ([1], p. 18).

Another non-ideality is that the transistor is biased via its emitter node instead of the collector node which makes it necessary to take the base current into account when determining the base-emitter voltage. Diode-connected substrate PNP transistors have their base grounded to make sure that the base-collector voltage is zero. That, however, means that the resulting collector current is smaller than the emitter current ([1], p. 18).

$$I_C = I_E - I_B = \alpha_F \cdot I_E = \frac{\beta_F}{1+\beta_F} \cdot I_E \tag{3.9}$$

α_F is the common-base current-gain, and β_F is the common-emitter current-gain, which is equal to I_C/I_B. The common-base current-gain α_F is an indicator for how much of the emitter current flows to the collector. It is ideally one.

3.4.1 Series Resistance

The voltages of the BJT are differing because of resistances in the BJT. The base-emitter voltage is a sum of the intrinsic base-emitter voltage $V_{B'E'}$ and the voltages across the base and emitter resistances, R_B and R_E, respectively ([1], p. 36).

$$\begin{aligned} V_{BE} &= V_{B'E'} + I_E R_E + I_B R_B \\ V_{BE} &= V_{B'E'} + I_E \left(R_E + \frac{R_B}{\beta_F + 1} \right) \end{aligned} \tag{3.10}$$

Combining the base and emitter resistances into a single resistance R_S in series with the emitter, the base-emitter voltage can be written as follows ([1], p. 36)

$$V_{BE} = \frac{kT}{q} ln\left(\frac{I_{bias}}{I_S}\right) + I_{bias} R_S, \tag{3.11}$$

where $I_{bias} = I_E$ and the finite current-gain is ignored. This series resistance affects the difference voltage ΔV_{BE}, too

$$\Delta V_{BE} = \frac{kT}{q} \cdot ln\left(p\right) + I_{bias}\left(p-1\right) R_S. \tag{3.12}$$

For currents in the range of a few µA or lower, the resulting voltage drop is small enough to be neglected in comparison to V_{BE}. But for ΔV_{BE} it can be significant.

3.4.2 Early Effects

There are two Early effects in the BJT that affect the base-emitter voltage V_{BE}, the forward and reverse Early effect.
A voltage drop across the base resistance R_B and the collector resistance R_C results in a non-zero base-collector voltage which in the end affects the effective base width W_B of the transistor. Thus, it causes the collector current of a BJT to depend on the base-collector voltage. Typically, this forward Early voltage is quite large (according to [1] around 100 V) which is why this effect is usually negligible ([1], p.38).
The reverse Early effect also has an impact on the base width which changes the collector current I_C. It introduces a multiplicative error in the base-emitter voltage V_{BE}. However, if the temperature sensor uses a ratiometric measurement which is common for smart temperature sensors, then the multiplicative error cancels due to division of the base-emitter voltages ([1], p. 39).

3.5 Temperature Dependencies

3.5.1 Saturation Current

The base-emitter voltage V_{BE} is affected by the temperature dependency of the saturation current I_S. The saturation current has several temperature dependencies as following equation shows

$$I_S = \frac{kTAn_i^2(T)\overline{\mu_p}(T)}{G_B(T)}. \tag{3.13}$$

As can be seen, the intrinsic carrier concentration n_i, the effective hole mobility $\overline{\mu_p}$ and the Gummel number G_B are temperature dependent in different ways. Therefore, the saturation current can be written as ([2], p. 20, [1], p. 21)

$$I_S(T) = CT^{\eta} exp\left(-\frac{qV_{g0}}{kT}\right), \tag{3.14}$$

where C is a constant, η = 4 - n, and V_{g0} is the extrapolated bandgap voltage at 0 K. Inserting 3.14 into 3.1 results in

$$I_C(T) = CT^{\eta} exp\left(\frac{q(V_{BE}(T) - V_{g0})}{kT}\right). \tag{3.15}$$

Rearranging this expression yields:

$$V_{BE}(T) = V_{g0} + \frac{kT}{q} \cdot ln\left(\frac{I_C(T)}{CT^{\eta}}\right). \tag{3.16}$$

In figure 3.3 which is taken from [1], the curvature of the base-emitter voltage is figuratively depicted. The variable V_{BE0} is the extrapolated bandgap voltage without curvature at T = 0 K, V_{g0} is the extrapolated bandgap voltage with curvature at T = 0 K and $V_{BE}(T_r)$ is the base-emitter voltage at a reference temperature of T = 300 K.

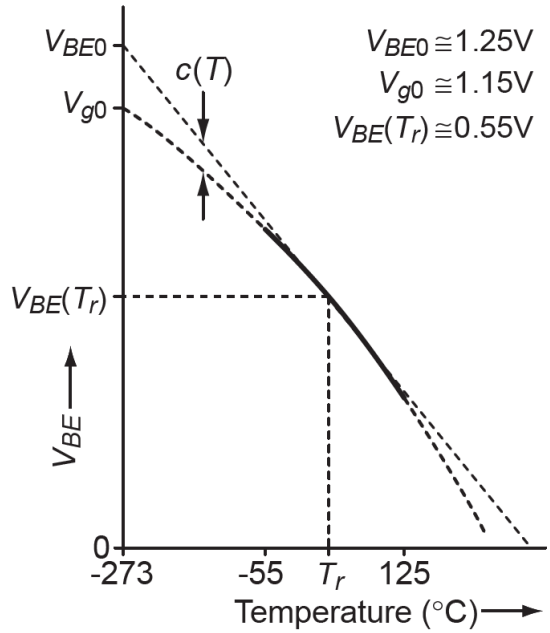


Figure 3.3: The temperature dependency of the base-emitter voltage V_{BE} ([1], p. 23).

In [1] it is described that the curvature for a collector current that exhibits PTAT behaviour can be calculated as follows

$$c(T) = \frac{k}{q} \cdot (\eta - m)\left(T - T_r - T \cdot ln\left(\frac{T}{T_r}\right)\right). \tag{3.17}$$

Figure 3.4 shows different curvatures for different values of (η - m). In the Spectre model of the 90nm process kit used for this work, the variables V_{g0} and η are called EG and XTI, respectively. The bandgap voltage EG = 1.11 V, and XTI = 3. Therefore, the curve for (η -

m) = 2 (for m = 1, because the collector current I_C is proportional to T^1) is valid. However, this should be understood as a rough estimate.

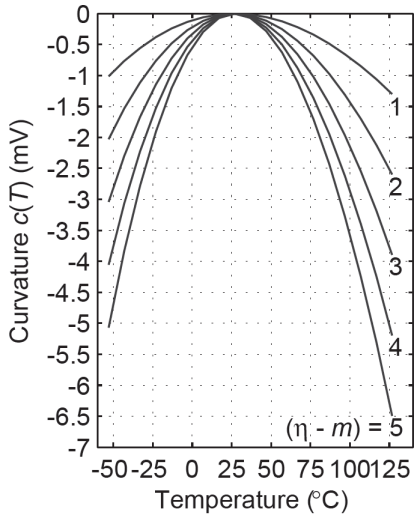


Figure 3.4: Curvature of V_{BE} for different values of (η - m) ([1], p. 23).

3.5.2 Current Gain

The common-base current (equation 3.9) is temperature dependent and can vary significantly which has to be taken into account when the temperature dependency of V_{BE} is derived. Taking equation 3.9 and adding the temperature dependence of β_F

$$\alpha_F(T) = \frac{\beta_F(T)}{1 + \beta_F(T)}, \tag{3.18}$$

where β_F can be written as

$$\beta_F(T) = \beta_{F0} \left(\frac{T}{Tr} \right)^{X_{TB}}. \tag{3.19}$$

The term β_{F0} is the nominal current-gain, T_r is a reference temperature and X_{TB} is a temperature exponent found by fitting the equation to measured data ([1], p. 24).

This temperature dependency of $I_C(T) = \alpha_F(T)I_E(T)$ results in an additional term in $V_{BE}(T)$

$$\begin{aligned} V_{BE}(T) &= V_{BE}(T)|_{\alpha_F=constant} + \frac{kT}{q} \cdot ln\left(\frac{\alpha_F(T)}{\alpha_F(T_r)}\right) \\ &= V_{BE}(T)|_{\alpha_F=constant} + \frac{kT}{q} \cdot ln\left(\frac{(1+\beta_{F0})\left(\frac{T}{T_r}\right)^{X_{TB}}}{1+\beta_{F0}\left(\frac{T}{T_r}\right)^{X_{TB}}}\right). \end{aligned} \tag{3.20}$$

With the aid of compensation techniques it is possible to reduce the additional term in V_{BE} to negligible levels ([1], p. 24).

3.5.3 Bias Resistor

The bias resistor in the biasing circuit affects the collector current, too. The collector current is dependent on the temperature dependency of the bias voltage and the bias resistor. The collector current can therefore be written as

$$I_C(T) = \frac{V_{bias}(T_r)}{R_{bias}(T)}\left(\frac{T}{T_r}\right)^m, \tag{3.21}$$

where the bias voltage V_{bias} is assumed to be proportional to a power of T ([1], p. 42). This temperature dependency of the bias resistor results in an additional term in $V_{BE}(T)$ ([1], p. 42):

$$\begin{aligned} V_{BE}(T) = {} & V_{BE}(T)|_{R_{bias}=constant} \\ & - \frac{kT}{q} ln(1 + \alpha_{TCR1}(T - T_r) + \alpha_{TCR2}(T - T_r)^2). \end{aligned} \tag{3.22}$$

The variables α_{TCR1} and α_{TCR2} are the first- and second-order temperature coefficients. The contribution of the second-order coefficient is usually small enough to be ignored. The first-order coefficient on the other hand can have a quite significant effect on the base-emitter voltage and its curvature. This effect can have both, negative and positive effects on the curvature. For negative values of α_{TCR1} the curvature of V_{BE} is reduced. However, for positive values the curvature is increased ([1], p. 43).

3.6 Processing Spread

3.6.1 Preface

Every chip is subject to processing spread which affects the performance of the devices. The temperature under which the manufacturing steps are done can vary, or the concentration of elements that is introduced differs from chip to chip ([9], p. 98). Even though it is attempted to minimise the variations during the fabrication there will always be some spread, and this spread can be significant. In [9] it is stated that device parameter variations

can occur that are equal to, for example, a change of 100 mV in the threshold voltage V_{th0}. This section describes the processing spread of the saturation current and current gain and its effect on the base-emitter voltage V_{BE}.

3.6.2 Saturation current

The saturation current I_S is not only dependent on temperature variations but is also subject to processing spread. This becomes clear when equation 3.2 is examined, which is repeated here

$$I_S = \frac{kTAn_i^2\overline{\mu_p}}{W_B N_p}. \tag{3.23}$$

The base doping N_d depends on tolerances in the manufacturing process. An n-well forms the base region and its spread can be estimated by using the n-well sheet resistance which can vary up to 50 %, according to ([1], p. 29). Such variations would result in similar changes in I_S and variations in V_{BE} up to $\pm$13 mV. Usually however, the spread is much smaller.
The base width W_B differs from the ideal value because of lithographic errors and variations in the depth of diffusions. Spreads in the area can result in changes of V_{BE} of up to $\pm$0.25 mV. The base width is determined by the difference in the depth between the base and the emitter diffusions. It is typically small to optimise the current gain ([1], p. 30).
The intrinsic carrier concentration n_i and $\overline{\mu_p}$ are both subject to variations due to mechanical stress ([1], p. 30). The mechanical stress will not be further investigated in this thesis.

The spread of the base-emitter voltage V_{BE} due to the spread in the saturation current I_S can therefore be expressed as follows ([1], p. 29)

$$\begin{aligned} V_{BE} &= \frac{kT}{q} \cdot ln\left(\frac{I_C}{I_S + \Delta I_S}\right) \\ &= \frac{kT}{q} \cdot ln\left(\frac{I_C}{I_S}\right) - \frac{kT}{q} \cdot ln\left(1 + \frac{I_S}{\Delta I_S}\right) \\ &\approx V_{BE}|_{\Delta I_S = 0} - \frac{kT}{q}\frac{\Delta I_S}{I_S}, \end{aligned} \tag{3.24}$$

where the approximation ln(1 + x) = x for $x \ll 1$ is used. For the used process kit gpdk090 this V_{BE} spread results in a change of up to $\pm$10 mV over the temperature range of -50 °C to 125 °C. This is shown in figure 3.5. The dotted line indicates the normal base-emitter voltage without process spread. The two black lines indicate the process spread for the worst cases which are retrieved by using corner simulations.
As was already stated, these process variations persist and are random which is why they cannot be controlled by the circuit designer. It is necessary to expect at least a few mV of V_{BE} spread. This will result in significant errors in the temperature accuracy of the sensor which have to be trimmed. The sensitivity analysis is done in chapter 5.6.

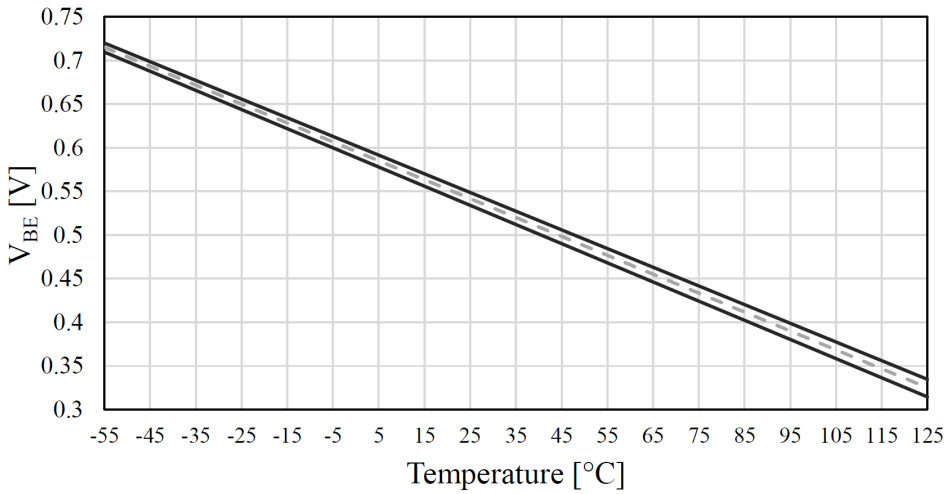


Figure 3.5: Spread of V_{BE} due to processing spread of the saturation current I_S for a PNP BJT in gpdk090nm.

3.6.3 Current Gain

The common-base current gain α_F (see 3.4) is also subject to processing spread which results in spread of V_{BE}. This can written as ([1], p. 31)

$$\begin{aligned} V_{BE} &= \frac{kT}{q} \cdot ln\left(\frac{(\alpha_F + \Delta\alpha_F)I_E}{I_S}\right) \\ &= \frac{kT}{q} \cdot ln\left(\frac{\alpha_F I_E}{I_S}\right) + \frac{kT}{q} \cdot ln\left(1 + \frac{\Delta\alpha_F}{\alpha_F}\right) \\ &\approx V_{BE}|_{\Delta\alpha_F=0} + \frac{kT}{q}\frac{\Delta\alpha_F}{\alpha_F} \end{aligned} \tag{3.25}$$

This shows that the spread in the current gain α_F affects V_{BE} similarly as the saturation current I_S. If the current gain was independent of the temperature, it would result in a PTAT spread in V_{BE} that could be trimmed out. However, $\Delta\alpha_F$ / α_F is likely dependent on the temperature because of the spread in different base-current components. Thus, the resulting spread is not PTAT and cannot be fully removed by trimming ([1], p. 32).

3.6.4 Bias Resistor

Due to processing spread the nominal value and the temperature dependency of the resistor will vary. The spread in V_{BE} due to the bias resistor adds directly to the spread as a result of the spread in the saturation current. The base-emitter voltage can be written as ([1], p. 43)

$$\begin{aligned} V_{BE} &= V_{BE}(T)|_{R_{bias}=constant} - \frac{kT}{q} ln\left(\frac{R_{bias}+\Delta R_{bias}}{R_{bias}}\right) \\ &= V_{BE}(T)|_{R_{bias}=constant} - \frac{kT}{q}\frac{\Delta R_{bias}}{R_{bias}}. \end{aligned} \tag{3.26}$$

The resistor value R_{bias} can be determined by taking the sheet resistance R_{sh} and the resistor's length and width:

$$R_{bias} = R_{sh}\frac{L}{W}. \tag{3.27}$$

It is possible to decrease the spread of the length and width ratio to negligible levels by making W several times larger than the minimum width ([1], p. 43). This means that the spread of the bias resistor is only dependent of the sheet resistance which is subject to spread in the doping and thickness of the resistive layer and other parameters ([1], p. 43). If the spread $\Delta R_{bias}/R_{bias}$ is temperature independent it would be PTAT. Such a spread can be trimmed out based on a temperature calibration. However, in practice the temperature coefficients of resistors depend on the doping level and other parameters. Therefore, it is not possible to say that the bias resistor spread is PTAT. To be able to trim out the effects of the spread it is necessary to measure the absolute value of the resistor and determine the temperature coefficients. ([1], p. 45)

3.7 Noise-Model

3.7.1 Types of Noise

There are various noise sources in electronic circuits. The three most important noise sources are *thermal noise, flicker noise* and *shot noise*.
The *thermal noise* is related to the random motion of electrons in a conductor. It has a white spectral density and is directly proportional to the absolute temperature. This type of noise occurs in all resistors and semiconductors. Thermal noise is always existent above the absolute zero temperature also when there is no current present. It is therefore unaffected by the bias conditions of the system. This noise imposes fundamental limits on the dynamic range achievable in electronic circuits. ([9], [10], [11])
Flicker noise is existent in every active device. However, contrary to the thermal noise, it only occurs if a dc current is flowing. This kind of noise arises because some carriers are trapped in the semiconductor for some time period and then released. It can be modelled with a dependency of 1/f, where f is the frequency. This shows that the flicker noise is most significant at low frequencies. ([9], [10], [11])
Shot noise occurs in pn-junctions and appears because a dc current is not continuous or smooth but rather a consequence of pulses induced by the flow of individual carriers. Therefore, it is dependent on the dc bias current and is typically larger than thermal noise. It can also be modelled as a white noise source. ([9], [11])

3.7.2 Noise in BJTs

The noise of bipolar transistors is a result of shot noise in the collector and the base currents, flicker noise of the base current and thermal noise of the base resistance. All noise sources are independent of each other and can therefore be summed. The mean-square values of the different noise sources are usually combined in two equivalent noise sources at the base of the BJT, see figure 3.6. The input voltage noise $V_i(f)$ is given by ([9], p. 380)

$$\frac{V_i^2(f)}{\Delta f} = 4kT\left(r_b + \frac{1}{2g_m}\right), \tag{3.28}$$

where Δf is the bandwidth, k is the Boltzmann constant, T the absolute temperature, r_b is the base resistance and the g_m term is due to the shot noise in the collector current referred back to the input. The second source is the equivalent input current noise, I_i ([9], p. 380)

$$\frac{I_i^2(f)}{\Delta f} = 2q\left(I_B + \frac{k_f I_B}{f} + \frac{I_C}{|\beta(f)|^2}\right), \tag{3.29}$$

where q is the electron charge, the term $2qI_B$ is the base current shot noise, the $k_f I_B/f$ term is the flicker noise (k_f is a process dependent parameter), and the $I_C/|\beta(f)|^2$ term is the input-referred collector current shot noise which is often ignored.
Typically, the noise in a BJT is dominated by thermal noise due to the series base resistance and shot noise in the base-current junction.

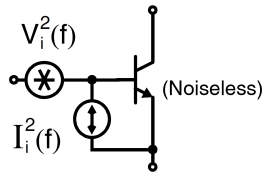


Figure 3.6: Noise sources of a BJT ([9], p.379).

3.7.3 Noise in MOSFETs

The noise in MOSFETs is typically dominated by flicker and thermal noise and is modelled as a noise-voltage source at the gate of the MOSFET and noise-current source from drain to source, which can be seen in figure 3.7.
The voltage source at the gate models the flicker noise as follows ([9], p. 380)

$$\frac{V_g^2(f)}{\Delta f} = \frac{k_f}{WLC_{ox}f}, \tag{3.30}$$

where k_f is again the process dependent parameter, W is the width, L the length and C_{ox} the oxide capacitance of the transistor. The 1/f-noise in MOSFETs typically dominates at low frequencies and is therefore very important. As equation 3.30 indicates larger devices

have lower flicker noise, and in addition, the flicker noise in PMOS devices is lower than in their counterparts, the NMOS.
The thermal noise is due to the resistive channel of the MOSFET in the active region and can be modelled as ([9], p. 381)

$$\frac{I_d^2(f)}{\Delta f} = 4kT\gamma g_m, \tag{3.31}$$

where γ is the white noise parameter and equal to 2/3 for long-channel devices. For short gate-length devices much higher values are possible.

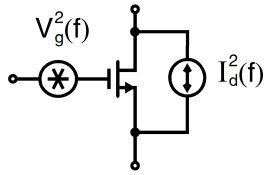


Figure 3.7: Noise sources of a MOSFET ([9], p. 379).

Chapter 4

Compensation and Correction Techniques

4.1 Introduction

Chapter 4 gives insight into advanced circuit techniques to reduce errors introduced by random and systematic errors that were discussed in chapter 3. Different techniques are mentioned and explained that address different errors in the system to reduce them to acceptable levels.

4.2 Compensation for Finite Current Gain

In chapter 3.5.2 it was explained that the error of the current gain affects the base-emitter voltage V_{BE} of the PNP transistor. The collector current I_C of a BJT depends on the forward current gain β_F and therefore it might be obvious to control the collector current in some way instead of the emitter current. However, since the collector node of substrate PNP transistors is grounded this could only be done indirectly ([1], p. 92).
Therefore, an alternative is employed to reduce the error due to finite current gain. A resistor is added to the base of the PNP transistor Q_{BL} (see figure 5.2) with the higher current in the bias circuit. Due to the feedback loop the input voltage of the op amp is zero, and thus ([1], p. 93)

$$V_{BE,QBL} + I_{bias} R_b = m I_{bias} \frac{1}{1+\beta_F} \frac{R_b}{m} + V_{BE,QBR}. \tag{4.1}$$

Solving this equation for I_{bias} results in

$$I_{bias} = \frac{1+\beta_F}{\beta_F} \frac{V_{BE,QBR} - V_{BE,QBL}}{R_b} = \frac{1+\beta_F}{\beta_F} \frac{\Delta V_{BE}}{R_b}. \tag{4.2}$$

Applying this current to the emitter of the BJT results in a base-emitter voltage of

$$V_{BE} = \frac{kT}{q} ln \left(\frac{I_b}{I_S} \frac{\beta_F}{\beta_F + 1} \right) = \frac{kT}{q} ln \left(\frac{\Delta V_{BE}}{R_b I_S} \right). \tag{4.3}$$

Now the base-emitter voltage is independent of β_F. In practice, the base resistance of Q_{BL} has to be taken into account because it adds to the resistor R_b/m ([1], p. 94)

4.3 Chopping

The offset at the input of the op amp is a significant source of inaccuracy in the system. CMOS amplifiers usually exhibit offset voltages in the mV range which is caused by transistor mismatch in the input pair of the differential amplifier. This mismatch can be reduced by using larger transistors but to achieve offset levels in the µV range it is necessary to employ offset cancellation techniques, such as chopping. The chopping technique is a dynamic process that is able to not only remove the offset of the amplifier but also 1/f-noise, as well as offset drift ([1], p. 175).
The principle of this technique is shown in figures 4.1 and 4.2. The input signal V_{in} is passed through a switch (see figure 4.3), which can be implemented as a transmission gate, that changes the polarity of the inputs of the differential amplifier. This switch is driven by a clock signal φ_{ch}. Because of the periodically switched polarity of the inputs the signal V_{in} is modulated by a square wave. This modulated signal is then passed through the differential amplifier with the offset V_{os}. At the output of the amplifier the input signal is found at the harmonics of φ_{ch} and the amplified offset voltage is found at DC. A second chopping demodulates the amplified signal back to DC and modulates the offset to the harmonics of φ_{ch}. The harmonics are then filtered out by a low-pass filter which leaves the amplified input signal without the offset ([1], p. 176).

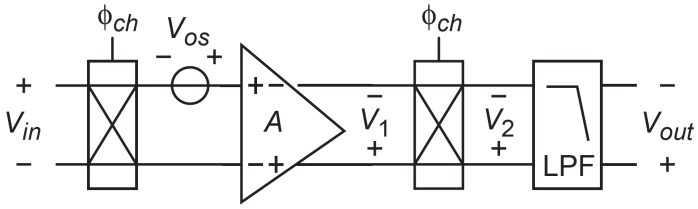


Figure 4.1: A chopper amplifier. Containing two chopper switches, the amplifier and a low-pass filter ([1], p.177).

The duty cycle of the chopping switch control signal needs to be exactly 50 % to average out the offset voltage.
The residual offset of chopper amplifiers is due to charge injection and clock feed-through in the chopper switches which results in voltage spikes. If these voltage spikes are at the input or output of the amplifier they will be demodulated by the second chopper which appears as an average DC offset. This offset is typically in the range of a few tens of µV.

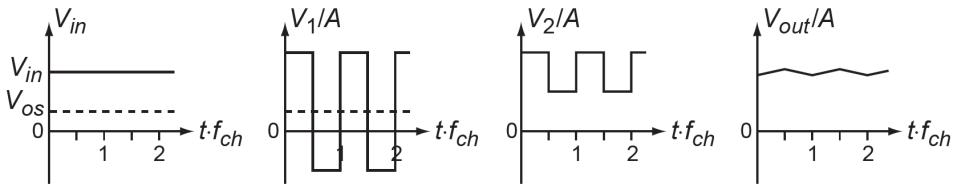


Figure 4.2: The voltages V_{in}, V_{os}, V_1, V_2 and V_{out} as function of time ([1], p.177).

([1], p. 179)
The residual offset can be reduced by reducing the switching frequency f_{ch} of the chopping switches. This results in less voltage spikes. However, this is limited by the corner frequency of the flicker noise because if the frequency f_{ch} is lower than the corner frequency of the flicker noise it will not be entirely averaged out.

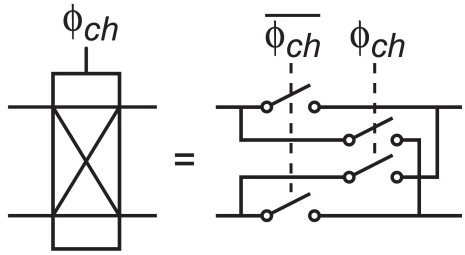


Figure 4.3: The chopper switch. Taken from ([1], p.177).

4.4 Dynamic Element Matching

Dynamic element matching is a technique to reduce errors due to mismatch. If, for example, six current sources are used to generate a bias current ratio of 1:5, where each current source generates the unit current then the voltage ΔV_{BE} will have six possible values. This is due to the mismatch between the current sources. It is possible to average out the error of the mismatch which results in an error of almost zero. Figure 4.4 shows a possible implementation of dynamic element matching for current sources. It shows that each current can be directed to the bipolar transistors Q_1 or Q_2. If current I_n, (where $1 \leq n \leq p+1$) flows through Q_1 and the remaining currents through Q_2 then the generated difference voltage ΔV_{BE} is equal to ([1], p. 60)

$$\Delta V_{BE,n} = \frac{kT}{q} \cdot ln\left(\frac{\sum_{i \neq n} I_i}{I_n}\right) = \frac{kT}{q} \cdot ln(p + \Delta p_n). \tag{4.4}$$

The mismatch between the currents I_n and the average of the remaining currents is Δp_n / p.

The average of the p + 1 possible difference voltages ΔV_{BE} can be computed as follows ([1], p. 60)

$$\Delta V_{BE,avg} = \frac{1}{p+1} \sum_{n=1}^{p+1} \Delta V_{BE,n}. \tag{4.5}$$

According to [1] this technique cancels the first-order errors but a second-order error is still existent. The second-order error can be expressed as

$$|\Delta V_{BE,avg} - \Delta V_{BE|\Delta p=0}| < \frac{1}{2} \frac{kT}{q} \left(\frac{\Delta p}{p} \right)^2, \tag{4.6}$$

where $\Delta p / p$ is the worst-case mismatch between the currents. Dynamic element matching can be easily implemented and reduces errors to levels of a few μV in ΔV_{BE}.
The same procedure can be employed to reduce mismatch errors in the bipolar transistors. However, if only two transistors are used with the same emitter area then it is possible to completely eliminate the mismatch error between the transistors without any additional switches in series. It is enough if the circuit from figure 4.4 is used. This is due to the fact that the difference voltage ΔV_{BE} is the difference between two ΔV_{BE} voltages that are generated by the same current I_n flowing through Q_1 first and then Q_2. The resulting ΔV_{BE} can be written as ([1], p. 62)

$$\Delta V_{BEA,n} - \Delta V_{BEB,n} = 2 \cdot \frac{kT}{q} ln(p + \Delta p_n). \tag{4.7}$$

The error is then removed by averaging the p + 1 difference voltages as is done in equation 4.5. It takes 2(p + 1) steps to run through the entire DEM process which results in an overall average that is free from first-order mismatch errors.

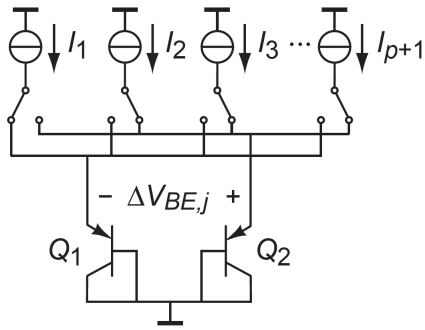


Figure 4.4: Principle of dynamic element matching for current sources to generate an accurate ΔV_{BE} ([1], p. 61).

4.5 Curvature Correction

In section 3.5 it was described that the base-emitter voltage is experiencing a curvature due to the temperature dependency of the collector current, see equations 3.16 and 3.17. There are many ways to correct the curvature of the base-emitter voltage, therefore, only a small selection is presented here.
One way of reducing the curvature of V_{BE} is to use a bias current that is dependent of the temperature since the saturation current I_S is the reason of the curvature in the first place. The bias current is proportional to T^m, as can be seen in equation 3.17 which leads to the curvature in V_{BE} to be proportional to (η - m). If the bias current is also dependent on the temperature, for example, as a PTAT/R current then the bias current is proportional to T^1, with m = 1. The outcome is a smaller curvature of the base-emitter voltage ([1], p. 81).
It is possible to make the bias current proportional to m $\approx \eta$. This would cancel the majority of the curvature. However, this technique is hard to implement in standard CMOS processes.
In addition, the temperature dependency of the bias current is also dependent of the temperature dependency of the bias resistor R_{bias}. Resistors that exhibit a negative first-order temperature coefficient (TC) reduce the curvature whereas a positive TC increases the curvature. Very high TCs are needed to cancel the second-order curvature, however, resistors in standard CMOS processes usually do not have such high TCs ([1], p. 82).
Another option to reduce the curvature is to use a temperature dependent gain α that is applied to ΔV_{BE}. Often times the value of α depends on the ratio of two resistors. The two resistors can be chosen such that they exhibit two different TCs. One resistor with a low TC and another one with a high TC. That makes it possible to achieve a temperature dependency of α that reduces the curvature of V_{BE}. ([1], p. 82)

4.6 Trimming

Processing spread can result in considerable errors in the base-emitter voltage V_{BE}. To account for these errors trimming techniques can be used to reduce them. To be able to trim a temperature sensor the temperature error has to be determined. This is done through calibration of the sensor at one or sometimes more than one calibration temperatures. It is possible to reduce the temperature error at the calibration temperature to zero ([1], p. 69).
The errors in V_{BE} are due to processing spread and mechanical stress. The processing spread induces an error that is PTAT which is why this error can be reduced by adding a PTAT voltage to V_{BE} which results in ([1], p.69)

$$V_{BE,trim} = V_{BE} + \gamma \frac{kT}{q}, \tag{4.8}$$

where the PTAT voltage is a multiple of the thermal voltage. The coefficient γ is obtained from the calibration that has to be done beforehand. The calibration data consists of the output reading D_{out} and the actual temperature. Using these two parameters it is possible to calculate an ideal ADC output μ_{ideal} and the actual ADC output μ. By computing the error in the base-emitter voltage V_{BE} a relation between the actual and the ideal ADC output can be established which then leads to the coefficient γ. ([1], p. 71)

One way of introducing a PTAT correction to V_{BE} is to add a programmable PTAT voltage to V_{BE} which can be a difference in ΔV_{BE} which is scaled by a factor γ_V. Figure 4.5 shows how this can be implemented. The PNP transistor is biased at a PTAT/R current. An additional resistor R_{trim} is added in series with the emitter of the transistor. R_{trim} is made of the same material as the bias resistor R_{bias}. This results in a PTAT voltage across the resistor which can be described as follows ([1], p. 71)

$$V_{BE,trim} = V_{BE} + \gamma_V \cdot \Delta V_{BE,bias} = V_{BE} + \gamma_V \cdot \frac{kT}{q} ln(p). \tag{4.9}$$

The coefficient $\gamma_V = R_{trim} / R_{bias}$ and p is the current density ratio. Adjusting the size of R_{trim} changes the magnitude of the PTAT voltage which can be achieved by dividing R_{trim} in N discrete unit elements and using a multiplexer.

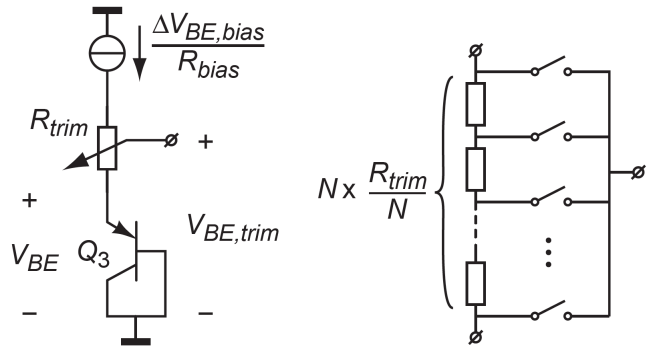


Figure 4.5: Voltage domain trimming. A programmable resistor is implemented in series with the emitter of the PNP transistor. The resistor R_{trim} can be implemented by N unit elements ([1], p. 71).

A second method of trimming is the current-domain trimming where the emitter-current density is adjusted. This is shown in figure 4.6. The bias current I_{bias} is changed by factor γ_I and/or by changing the emitter area A_E by a factor γ_A.

$$V_{BE,trim} = V_{BE} + \frac{kT}{q} ln\left(\frac{\gamma_I}{\gamma_A}\right) \tag{4.10}$$

However, the PTAT voltage that is added to the base-emitter voltage is a logarithmic function which has to be taken into account when determining the coefficients. It is possible to compose the emitter area A_E of several transistors in parallel. Using switches in series with the emitter it is possible to switch the transistors on and off. This however leads to an additional voltage drop across the switches that is added to the base-emitter voltage, therefore, large switches would be needed to reduce this effect. An alternative is to compose the bias current of a number of current sources where the switches are in series with the high impedance of the current source. This means that their on-resistance can be large and small switches can be used ([1], p. 72).
Modulated trimming is a method that uses less chip area if high resolution trimming is a requirement. This process uses a digital modulator to switch the bias current of a PNP transistor between two values, I_{bias1} and I_{bias2}. These two values correspond to the extreme

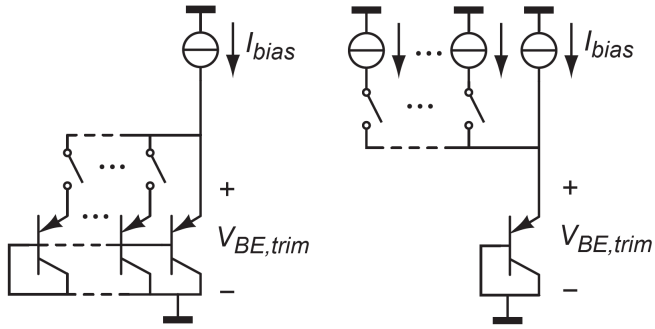


Figure 4.6: Current-domain trimming. On the left side, the programmable emitter area is shown; on the right hand side is the programmable bias current shown ([1], p. 72).

values of the trimming range. The modulator uses an input γ_M which is in the range of $0 \leq \gamma_M \leq 1$ to generate an output that is in the end passed through a low-pass filter which results in the average voltage ([1], p. 73)

$$V_{BE,trim} = (1-\gamma_M)V_{BE1} + \gamma_M V_{BE2} = V_{BE1} + \gamma_M \cdot ln\left(\frac{I_{bias1}}{I_{bias2}}\right). \tag{4.11}$$

In case it is crucial to keep the analog circuitry simple the effect of errors in V_{BE} can be reduced or cancelled by means of a digital correction. This digital correction, however, needs a significant amount of chip area but might also be implemented off-chip on a microcontroller. But the trimming parameter has to be known to be implemented in the microcontroller. If the effect of a PTAT error in V_{BE} on the ADC's output μ is known then the output can be written as

$$\mu = \frac{\alpha \cdot \Delta V_{BE}}{V_{BE,ideal} + \varepsilon\dfrac{kT}{q} + \alpha \cdot \Delta V_{BE}}, \tag{4.12}$$

and the ideal output is

$$\mu_{ideal} = \frac{\alpha \cdot \Delta V_{BE}}{V_{BE,ideal} + \alpha \cdot \Delta V_{BE}}. \tag{4.13}$$

The difference between the reciprocal outputs is a temperature independent variable γ_D and equal to

$$\gamma_D = \frac{\varepsilon\dfrac{kT}{q}}{\alpha \cdot \Delta V_{BE}}, \tag{4.14}$$

which leads to the ideal output μ_{ideal}

$$\mu_{ideal} = \frac{\mu}{1-\gamma_D\mu}. \tag{4.15}$$

In the end, the digital temperature reading at the output of the system (see equation 2.7) should be expressed as

$$D_{out} = A \cdot \frac{\mu}{1 - \gamma_D \mu} + B, \tag{4.16}$$

where A and B are the already mentioned constants in chapter 2.2.4.

Chapter 5

Design of the Temperature Sensor

5.1 Introduction

Chapter 5 describes the design of the analog front-end. It starts by setting specifications that serve as design guideline in section 5.2. Afterwards, in section 5.3 the structure of the analog front-end is analysed. Hereinafter, a budget for the system is established by setting up equations for the sensitivity of the temperature reading at the output to errors in the analog front-end, section 5.4. This includes a detailed evaluation of each error which is done in section 5.6. Then the analog front-end design is explained, which deals with the device dimensioning of the different circuit parts, such as the current-mirror or the op-amp. In the end in section 5.7.8, the initial design is tested and altered to achieve a better performance.

5.2 Design Specifications

In chapter 1.1 the requirements for the temperature sensor and the process of finding a suitable one were presented. The design specifications for the design of the analog front-end are based on the available performance data of the proposed temperature sensor in [5]. Table 5.1 shows the performance that is aimed for and should be understood as design guideline. The sensor should be implemented on-chip in 0.18 µm CMOS technology. However, only a generic process design kit for 90 nm is available which will be used instead of a 180 nm process design kit.
The entire proposed temperature sensor draws a current of 3.4 µA with a conversion time of 5.3 ms, where the entire front-end draws only 2.1 µA. Since only the analog part is being designed in this thesis the goal is to achieve such a low current for the analog front-end. The conversion time is 5.3 ms which means part of the conversion time goes to the settling of the signals in the analog part of the system. As an assumption, 1 ms will be put aside for the settling. Leaving a comfortable margin means that the settling of the signals should be done in 500 µs. The chip area is as an initial budget also chosen to be the same as the

one of the proposed sensor, which uses 0.08 mm^2.
The accuracy of the analog front-end is just a guideline for the design process. Since it depends also on the digital part of the sensor, where error corrections are performed to reduce errors of the analog front-end.

Table 5.1: Design specifications of the analog front-end.

Parameter	Specification
Temp. range	-55 °C - 125 °C
Supply voltage	2 V
I_{bias}	90 nA
Current consumpt. op amp	630 nA
Total current consumpt.	2.1 µA
Accuracy	0.5 °C
Resolution	0.1 °C
Settling time	500 µs
Area	0.08 mm^2

5.3 The Analog Front-End

The proposed temperature sensor in [5] consists of the analog front-end and a digital part that consists of the ADC and the digital-backend. This is shown in figure 5.1.

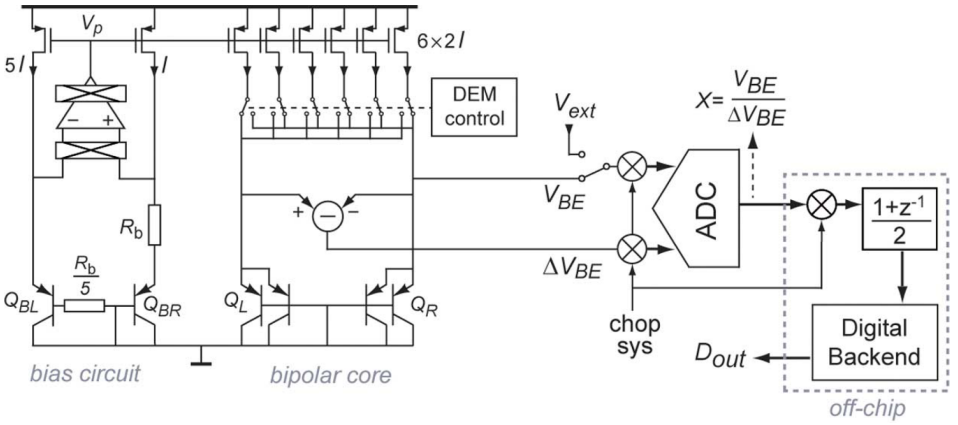


Figure 5.1: Overview of the entire system of the proposed temeperature sensor [5].

Due to the limited amount of time for this thesis only the analog front-end will be designed, and therefore, the ADC and the digital back-end are not further explained.
The analog front-end (shown again in figure 5.2) consists of the bias circuit and the bipolar core. The bias circuit generates the two PTAT voltages V_{BE1} and V_{BE2} and the CTAT voltage ΔV_{BE} (see figure 2.3). The resulting current I_b is PTAT in nature and used to bias

the PNP transistors of the bipolar core, where the base-emitter and difference voltages, V_{BE} and ΔV_{BE} respectively, are applied to the inputs of the succeeding ADC.

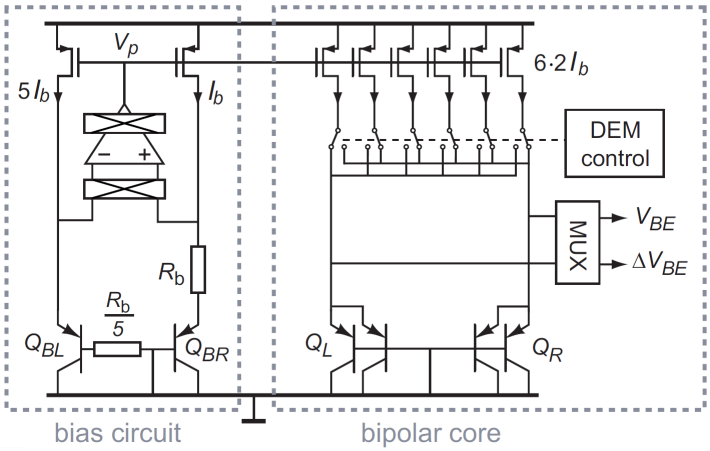


Figure 5.2: Overview of the analog front-end ([2], p. 61).

The bias circuit is a common way of setting up a bandgap reference circuit and to generate a PTAT current. The two PNP transistors in the bias circuit have equal emitter areas which is why a higher current density ratio is used to achieve the two base-emitter voltages V_{BE1} and V_{BE2}. The op amp in the positive feedback loop forces ΔV_{BE} across the resistor R_b which has an accurate PTAT current I_b as consequence. The resistor $R_b/5$ is implemented to compensate for spread in the forward current-gain β_F, see chapter 4.2.
The positive feedback loop of the op amp in open-loop configuration would respond to negative/positive differential input voltages with an ever-increasing/decreasing output current. In the bias circuit the op amp is configured in a negative feedback loop. This is due to the PMOS current mirror at the output of the op amp which inverts the signal resulting in a stabilised circuit. For proper operation, a start-up circuit is needed for the bias circuit because it has two stable operating points. The first stable point is a so-called "degenerate" bias point where all the transistors carry zero current even though the supply voltage is turned on. The feedback loop is able to support a zero current state in both branches. The second stable point is the bias point. The start-up circuit will be explained later in section 5.7.6.
The inputs and the output of the op amp are chopped to reduce the input offset voltage, as described in chapter 4.3.
The op amp is using an adaptive self-biasing layout which is shown in figure 5.3. Its input stage consists of a common differential input stage (M_5:M_6) with NMOS loads (M_1:M_2). The small-signal differential gain can be obtained by using the half-circuit analysis approach of the differential stage which results in ([10], p. 123)

$$A_{v1} = -g_{m5} \cdot \left(\frac{1}{g_{m1}} || r_{ds5} || r_{ds1} \right), \tag{5.1}$$

Where $g_{m1,2}$ is the transconductance of the transistors and r_{ds} the source-drain impedance.

Since the NMOS loads are diode-connected and typically it is assumed that $r_{ds} >> g_m$ the voltage gain can be approximated as

$$A_{v1} \approx -\frac{g_{m5}}{g_{m1}} = -\frac{g_{m6}}{g_{m2}}. \tag{5.2}$$

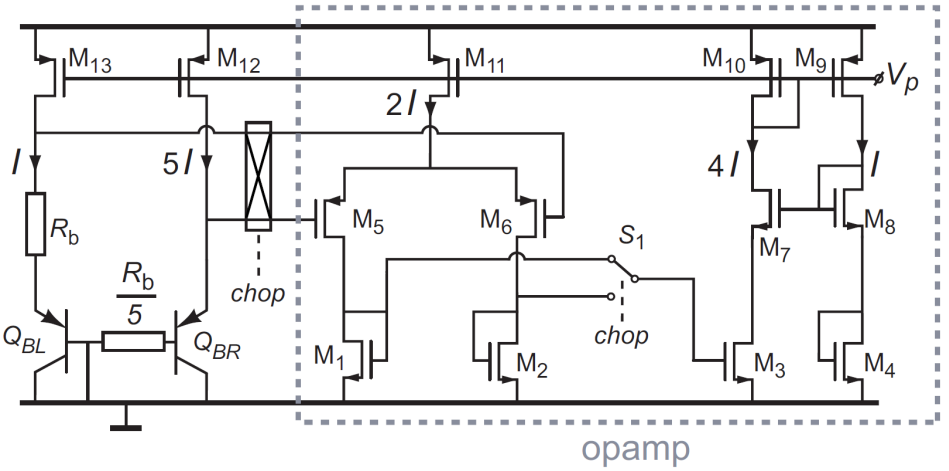


Figure 5.3: Proposed circuit of the adaptive self-biasing operational amplifier. Taken from ([2], p. 63).

The second stage of the op amp consists of the transistor M_3 that converts the voltage output of the first stage into a current which is fed back to the differential pair via the current mirror M_{10}:M_{11}. The transistor M_7 forms a voltage follower with the diode-connected transistor M_8. The branch consisting of M_4:M_8:M_9 is therefore a replica circuit to make sure that the drain-source voltage of M_3 is equal to $M_{1,2}$. This is due to the fact that the diode-connected transistor M_4 has the same drain current and the same size as $M_{1,2}$ resulting in the same drain-source voltage V_{ds}. M_7 and M_8 are assumed to be equal apart from their width to length ratio. The gate voltage of M_7 and M_8 is the same which results in the same source voltage, and thus the same drain-source voltage for M_3 as that of $M_{1,2}$.
The branch consisting of M_3:M_7:M_{10} can be analysed as a cascode stage with active PMOS load. The voltage gain can be written as

$$A_{v2} = -G_m \cdot R_{out}, \tag{5.3}$$

where G_m is the overall transconductance of the branch. The overall transconductance G_m can be approximated as $G_m = g_{m3}$ ([10], p. 86). The ouput resistance of the circuit can be found to be

$$R_{out} = ([1 + (g_{m7} r_{ds7})] r_{ds3} + r_{ds7}) \;||\; r_{10}, \tag{5.4}$$

where the first part is derived from a common-source stage (M_7) with a degeneration resistor equal to r_{ds3} in parallel with the output impedance of M_{10}. The PMOS M_{10} is

diode-connected which allows to approximate the output impedance as $r_{10} = 1/g_{m10}$. Using equation 5.3 and inserting G_m and R_{out} results in

$$\begin{aligned} A_{v2} &= -g_{m3} \cdot (([1 + (g_{m7} r_{ds7})] r_{ds3} + r_{ds7}) \;||\; r_{10}) \\ A_{v2} &= -g_{m3} \cdot (([1 + (g_{m7} r_{ds7})] r_{ds3} + r_{ds7}) \;||\; \frac{1}{g_{m10}}), \end{aligned} \tag{5.5}$$

where it can be assumed that $g_{m7}r_{ds7} \gg 1$ and $g_{m7}r_{ds7}r_{ds3} \gg r_{ds7}$. This results in

$$\begin{aligned} A_{v2} &= -g_{m3} \cdot (g_{m7} r_{ds7} r_{ds3} \;||\; \frac{1}{g_{m10}}) \\ A_{v2} &\approx -\frac{g_{m3}}{g_{m10}}. \end{aligned} \tag{5.6}$$

The replica branch consisting of M_4:M_8:M_9 is found to have no significant influence on the gain of the amplifier as it is just there to ensure the independence of the current from mismatch between the drain-source voltages of $M_{1,2}$ and M_3. Therefore, the total voltage gain of the amplifier can be approximated as

$$A_{v,tot} \approx A_{v1} \cdot A_{v2} = \frac{g_{m5}}{g_{m1}} \cdot \frac{g_{m3}}{g_{m10}}. \tag{5.7}$$

The main loop of the bias circuit consists of the transistor M_{13}, the bias resistor R_b, the BJT Q_{BL} and the positive input of the op amp. The loop-gain A_{loop} can be expressed as

$$A_{loop} = A_{v,M13} \cdot A_{v,opamp}, \tag{5.8}$$

where $A_{v,M13}$ is the gain of the common-source stage M_{13} and $A_{v,opamp}$ the total op amp gain (equation 5.7). Noticing that the transconductance $g_{m3} = 4g_{m1}$ and $g_{m10} = 4g_{m13}$ means that the transconductances cancel each other. Inserting the two gain expression yields the final loop-gain A_{loop}

$$\begin{aligned} A_{loop} &= -g_{m13} \cdot R_{out} \cdot \frac{g_{m5}}{g_{m1}} \cdot \frac{g_{m3}}{g_{m10}} \\ A_{loop} &= -g_{m13} \cdot R_{out} \cdot \frac{g_{m5}}{g_{m1}} \cdot \frac{4g_{m1}}{4g_{m13}} \\ A_{loop} &= -g_{m5} \cdot R_{out} \\ A_{loop} &= -g_{m5} \cdot (r_{ds13} || (R_b + \frac{1}{g_{mQBL}}) \\ A_{loop} &\approx -g_{m5} \cdot (R_b + \frac{1}{g_{mQBL}}) \end{aligned} \tag{5.9}$$

5.4 Sensitivity Analysis

As explained in Chapter 2.2.4 the final digital output of a BJT-based temperature sensor can be written as [1]

$$D_{out} = A \cdot \mu + B. \tag{5.10}$$

Where A $\approx$ 600 K, B $\approx$ -273 K and

$$\mu = \frac{V_{PTAT}}{V_{REF}} = \frac{\alpha \cdot \Delta V_{BE}}{V_{BE} + \alpha \cdot \Delta V_{BE}}. \tag{5.11}$$

As can be seen from these equations, the output D_{out} depends on the three variables V_{BE}, ΔV_{BE} and α. Therefore, the temperature error at the output can be calculated using these values which results in the sensitivity equations 5.12, 5.13 and 5.14. These equations indicate how much the output D_{out} reacts to changes of the aforementioned variables.
The sensitivity equations are calculated by using the equations 5.10 and 5.11 and by differentiating D_{out} to V_{BE}, ΔV_{BE} and α. The sensitivity equations are therefore ([1], p. 55)

$$\begin{aligned} S_{V_{BE}}^{D_{out}}(T) &= \frac{\partial D_{out}}{\partial V_{BE}} = \frac{\partial (A \cdot \frac{\alpha \cdot \Delta V_{BE}}{V_{BE} + \alpha \cdot \Delta V_{BE}} + B)}{\partial V_{BE}} \\ &= -\frac{A \cdot \alpha \cdot \Delta V_{BE}}{V_{REF}^2} = -\frac{A \cdot \mu}{V_{REF}} = -\frac{T}{V_{REF}}, \end{aligned} \tag{5.12}$$

$$\begin{aligned} S_{\Delta V_{BE}}^{D_{out}}(T) &= \frac{\partial D_{out}}{\partial \Delta V_{BE}} = \frac{\partial (A \cdot \frac{\alpha \cdot \Delta V_{BE}}{V_{BE} + \alpha \cdot \Delta V_{BE}} + B)}{\partial \Delta V_{BE}} = \frac{A \cdot \alpha \cdot V_{BE}}{V_{REF}^2} \\ &= \frac{A \cdot \alpha \cdot (V_{REF} - \alpha \cdot \Delta V_{BE})}{V_{REF}^2} = \frac{A \cdot \alpha \cdot (1 - \frac{\alpha \cdot \Delta V_{BE}}{V_{REF}})}{V_{REF}^2} \\ &= \frac{A - T}{V_{REF}} \cdot \alpha, \end{aligned} \tag{5.13}$$

$$\begin{aligned} S_{\alpha}^{D_{out}}(T) &= \frac{\partial D_{out}}{\partial \alpha} = \frac{\partial (A \cdot \frac{\alpha \cdot \Delta V_{BE}}{V_{BE} + \alpha \cdot \Delta V_{BE}} + B)}{\partial \alpha} \\ &= \frac{A \cdot \Delta V_{BE} \cdot V_{BE}}{V_{REF}^2} = \frac{A \cdot V_{BE} \cdot \mu}{\alpha \cdot V_{REF}} = \frac{T \cdot V_{BE}}{\alpha \cdot V_{REF}} \\ &= \frac{T}{\alpha} \cdot \frac{V_{REF} - \alpha \cdot \Delta V_{BE}}{V_{REF}} = \frac{T}{\alpha} \cdot \left(1 - \frac{T}{A}\right). \end{aligned} \tag{5.14}$$

The approximation $\mu \approx$ T/A was used to simplify the equations which originates in

$$\mu = \frac{D_{out} - B}{A} \approx \frac{D_{out} - 273°C}{A} = \frac{T_{out}}{A} \approx \frac{T}{A}. \tag{5.15}$$

From these equations it can be seen that the sensitivities in V_{BE} and ΔV_{BE} are PTAT and CTAT, respectively. Figure 5.4 shows the sensitivities over a temperature range from -55 °C to +125 °C. In this graph the sensitivity $S_{\Delta V_{BE}}^{D_{out}}(T)$ is divided by α, that is the sensitivity to errors in $\alpha \cdot \Delta V_{BE}$. It clearly shows the already mentioned PTAT and CTAT characteristics. The worst-case for a 1 mV error in V_{BE} is at 125 °C with an error of 0.32 °C, whereas the worst-case error of 0.33 °C in ΔV_{BE} is at -55 °C for a 1 mV error. For α the worst-case error of 1.5 °C is at room temperature for an error of 1 % in α ([1], p. 56).

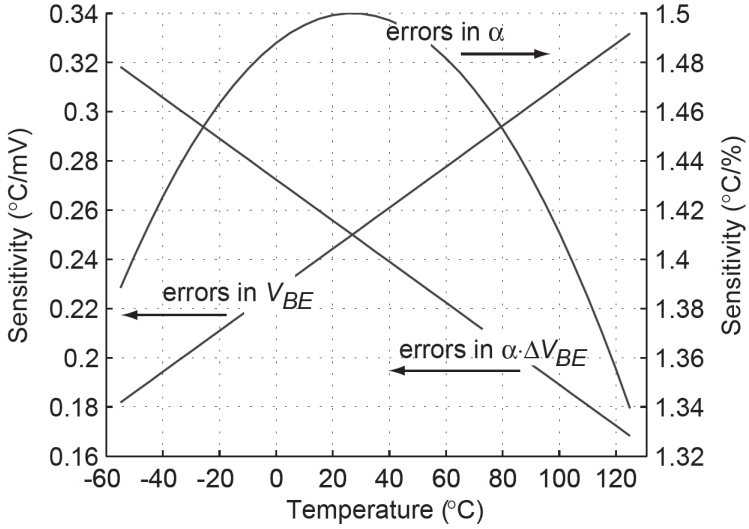
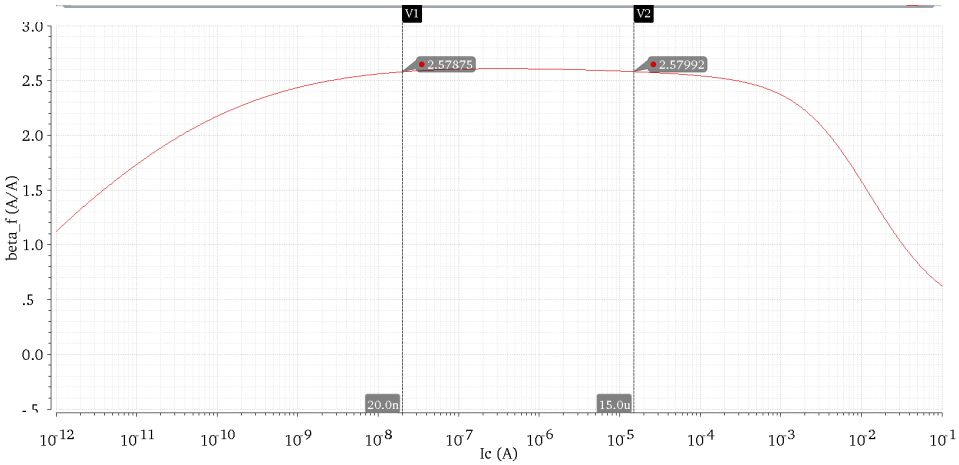


Figure 5.4: Sensitivities of the digital output D_{out} to errors in V_{BE}, $\alpha \cdot \Delta V_{BE}$ and relative errors in α ([1], p. 56.)

5.5 Determination of the Bias Current

In chapter 3.4 it was explained that the bias current of the PNP transistors cannot be chosen arbitrarily high (see figure 3.2). To determine the current range that results in an almost constant forward current-gain β_F, a diode-connected PNP transistor (figure 3.1) of the used process kit was biased with an emitter current that was swept from 1 pA up to 100 mA.
The resulting β_F versus the collector current I_C is shown in figure 5.5. It can be seen that the current-gain stays almost constant for a current range between 20 nA up to 15 µA. Therefore, it is possible to choose a bias current for the PNP transistors of $I_{bias} = I_C = 90$ nA ($5I_{bias} = 450$ nA) which results in a $\beta_F \approx 2.6$.



orward current-gain β_F versus the collector current I_C.Forward current-gain β_F versus the collector current I_C.

Figure 5.5: F

5.6 Error Budgeting

The voltages V_{BE} and ΔV_{BE} show various non-idealities, as was explained in chapter 3.4. The total error at the output of the temperature sensor will be the accumulation of all errors in the analog front-end as well as the readout circuit. This means that a fraction of the total error has to be allocated to each error source that exists in the circuitry. This is done by using the sensitivity analysis equations and calculating the maximum error in V_{BE}, ΔV_{BE} and α based on a given error contribution ΔT at the output of the sensor system.
For the budgeting of this sensor an error contribution of $\Delta T = 0.1$ °C was chosen for each error source. Since the scaling factor α is not implemented in the analog front-end but in the digital part, there will be no error budget for it.
In the end, the budget will be presented in table 5.2 and serves as design guideline in addition to the design specifications in table 5.1.

5.6.1 I_S and R_{bias} Errors

Errors, such as processing spread, temperature dependencies or other non-idealities, in the saturation current I_S and the biasing resistor R_{bias} affect the base-emitter voltage V_{BE}, as described in chapter 3.5 and 3.6. It is either possible to calculate the combined error of both (I_S and R_{bias}) or the individual error in V_{BE} of the saturation current and the bias resistor by using the maximum relative errors due to processing spread.
The combined error can be written as ([1], p. 57)

$$V_{BE} - V_{BE,ideal} = \delta(V_{BE}) = \frac{kT}{q} \cdot ln\left(1 + \varepsilon\right), \tag{5.16}$$

$$\delta(V_{BE}) \approx \frac{kT}{q} \cdot \varepsilon, \tag{5.17}$$

where $\delta(V_{BE})$ is the absolute error in V_{BE} and ε is the relative error in the saturation current I_S and/or the bias resistor R_b.
To be able to calculate the temperature reading error at the output of the sensor the sensitivity equation 5.12 has to be multiplied with the error in V_{BE} ([1], p. 57).

$$\varepsilon = \Delta T = S_{V_{BE}}^{D_{out}}(T) \cdot \delta(V_{BE}) \tag{5.18}$$

If an error contribution of $\Delta T = 0.1\ °C$ is to be achieved at the output then the combined relative error ε in I_S and R_b has to be smaller than

$$\varepsilon(D_{out}) < \left(\frac{\Delta T \cdot V_{REF} \cdot q}{T^2 \cdot k}\right) = 0.871\ \%. \tag{5.19}$$

The individual error of the resistance process spread is (based on equation 3.26)

$$V_{BE} - V_{BE,ideal} = \delta(V_{BE,\Delta R_b}) = \frac{kT}{q} \cdot ln\left(1 + \frac{\Delta R_b}{R_b}\right). \tag{5.20}$$

The maximum error in V_{BE} due to the resistor spread can be calculated at the top of the temperature range ($T \approx 400\ K$) as follows

$$\delta(V_{BE,\Delta R_b}) = \frac{1.38 \cdot 10^{-23}\ \frac{J}{K} \cdot 400\ K}{1.602 \cdot 10^{-19}\ C} \cdot ln\left(1 \pm 15\ \%\right) = \begin{pmatrix} +4.82\ mV \\ -5.6\ mV \end{pmatrix}. \tag{5.21}$$

From equation 5.21 it can be seen that the worst-case error of the resistor spread at the top of the temperature range results in several mV error in V_{BE}. By using equation 5.12 and 5.21 the temperature error at the output of the sensor can be calculated as

$$\varepsilon(D_{out}) = S_{V_{BE}}^{D_{out}}(T) \cdot \delta(V_{BE,\Delta R_b}) = -\frac{T}{V_{REF}} \cdot \begin{pmatrix} +4.82\ mV \\ -5.6\ mV \end{pmatrix} = \begin{pmatrix} -1.61\ °C \\ +1.87\ °C \end{pmatrix} \tag{5.22}$$

In addition, the spread of the saturation current I_S adds to the error of the bias resistor. Based on corner simulations of a diode-connected PNP transistor it was found that the

voltage V_{BE} varies around ± 10 mV for the used process kit (see chapter 3.6). The resulting error in V_{BE} is then

$$\varepsilon(D_{out}) = S_{V_{BE}}^{D_{out}}(T) \cdot \delta(V_{BE,\Delta I_S}) = -\frac{T}{V_{REF}} \cdot \pm 10\ mV = \pm 3.33\ ^\circ C. \tag{5.23}$$

The individual errors of I_S and R_b show that these errors are very large in the worst case. An error contribution of ε = 0.874 % is therefore not likely to be achieved without trimming the PTAT errors in V_{BE}.

5.6.2 Mismatch Errors

Two PNP transistors with the same emitter-area are operated at a specific current-density ratio p to generate an accurate PTAT voltage ΔV_{BE}. Therefore, the ideal difference voltage ΔV_{BE} is ([1], p.58)

$$\Delta V_{BE} = \frac{kT}{q} \cdot ln(p). \tag{5.24}$$

Mismatch between the current sources that generate the current density ratio p affects ΔV_{BE} as follows ([1], p. 59)

$$\Delta V_{BE} = \frac{kT}{q} ln(p + \Delta p) = \frac{kT}{q} \cdot \left[ln(p) + ln\left(1 + \frac{\Delta p}{p}\right)\right]. \tag{5.25}$$

The absolute error $\delta(\Delta V_{BE})$ can then be written as

$$\delta(\Delta V_{BE}) = \frac{kT}{q} \cdot ln\left(1 + \frac{\Delta p}{p}\right). \tag{5.26}$$

$$\delta(\Delta V_{BE}) \approx \frac{kT}{q} \cdot \frac{\Delta p}{p}. \tag{5.27}$$

As was done before, the sensitivity of the sensor output D_{out} to changes in ΔV_{BE} is multiplied by the absolute error to calculate the temperature error at the output. This means that equation 5.13 and 5.27 are used as follows

$$\epsilon(D_{out}) = S_{\Delta V_{BE}}^{D_{out}}(T) \cdot \delta(\Delta V_{BE}) = \frac{A - T}{V_{REF}} \cdot \alpha \cdot \frac{kT}{q} \cdot \frac{\Delta p}{p}. \tag{5.28}$$

This equation has its maximum around the middle of the temperature range (T $\approx$ 300 K) because the sensitivity 5.13 is CTAT whereas the error 5.27 is PTAT. The scaling factor α can be determined by using equation 2.5 which results in α = 14.43.
The equation 5.28 can be rearranged to calculate the maximum relative error to achieve a temperature error contribution of ΔT = 0.1 °C

$$\frac{\Delta p}{p} < \frac{\Delta T \cdot V_{REF} \cdot q}{(A - T) \cdot \alpha \cdot k \cdot T} = \frac{0.1\ ^\circ C \cdot 1.2\ V \cdot q}{(600\ K - 300\ K) \cdot 14.43 \cdot k \cdot 300\ K} = 0.107\ \%. \tag{5.29}$$

To achieve such a low temperature error contribution due to mismatch in the current sources of the bipolar core, dynamic element matching (DEM) is needed.

5.6.3 Bias Circuit Errors

The bias circuit proposed by Souri, Chae and Makinwa ([5]) uses a common approach for the analog front-end. It consists of the bias circuit with an op amp in a feedback loop to ensure that the difference voltage ΔV_{BE} is generated across the bias resistor R_b ([5], [1], p. 66). The circuit will have inherent errors that will affect the generated V_{BE} voltage such that it will deviate from its ideal value. The most important errors are ([1], p. 67)

- offset V_{OS} (= $\delta(\Delta V_{BE})$) of the op amp,
- inaccuracy $\frac{\Delta p}{p}$ in the current mirror,
- finite open-loop gain A_{OL}.

The offset of the op amp adds directly to ΔV_{BE} which results in an error in V_{BE}. Therefore, the voltage V_{BE} can be written as ([1], p. 67)

$$\begin{aligned} V_{BE} &= \frac{kT}{q} \cdot ln\left(\frac{\Delta V_{BE} + \delta(\Delta V_{BE})}{R_b \cdot I_S}\right) \\ &= \frac{kT}{q} \cdot \left[ln\left(\frac{\Delta V_{BE}}{R_b \cdot I_S}\right) + ln\left(1 + \frac{\delta(\Delta V_{BE})}{\Delta V_{BE}}\right)\right]. \end{aligned} \tag{5.30}$$

The error in V_{BE} is then, using the simplification of $ln(1+x) = x$ for $\delta(\Delta V_{BE}) << \Delta V_{BE}$

$$\delta(V_{BE}) \approx \frac{kT}{q} \cdot \frac{\delta(\Delta V_{BE)}}{\Delta V_{BE}} = \frac{kT}{q} \cdot \frac{\delta(\Delta V_{BE)}}{\frac{kT}{q} \cdot ln(p)} = \frac{\delta(\Delta V_{BE})}{ln(p)}. \tag{5.31}$$

To determine the maximum offset $\delta(\Delta V_{BE})$ for a given error contribution equations 5.12 and 5.31 are used.

$$\delta(D_{out}) = S_{V_{BE}}^{D_{out}}(T) \cdot \delta(V_{BE}) = -\frac{T}{V_{REF}} \cdot \frac{\delta(\Delta V_{BE})}{ln(p)} \tag{5.32}$$

Rearranging equation 5.32 the maximum error in ΔV_{BE} can be found as follows

$$\delta(\Delta V_{BE}) < \frac{\delta(D_{out}) \cdot V_{REF} \cdot ln(p)}{T}. \tag{5.33}$$

Setting $\delta(D_{out})$ = 0.1 °C, V_{REF} = 1.2 V, p = 5 and the temperature T $\approx$ 400 K to get the smallest error then

$$\delta(\Delta V_{BE}) < \pm 483\ \mu V. \tag{5.34}$$

This offset might be possibly achievable by precision layout but to reduce the offset chopping can be used.

The inaccuracy in the current-mirror ratio adds also directly to ΔV_{BE}. This means that ΔV_{BE} can be written as ([1], p.67)

$$\Delta V_{BE} = \frac{kT}{q} \cdot ln(p + \Delta p) \approx \frac{kT}{q} \cdot ln(p) + \frac{kT}{q} \cdot \frac{\Delta p}{p}, \tag{5.35}$$

$$\delta(\Delta V_{BE}) = \frac{kT}{q} \cdot \frac{\Delta p}{p}. \tag{5.36}$$

ΔV_{BE} is affecting V_{BE} in the same way as the offset voltage. Therefore, it is possible to use equation 5.32 and insert equation 5.36 ([1], p.67).

$$\delta(D_{out}) = S_{V_{BE}}^{D_{out}}(T) \cdot \delta(V_{BE}) = -\frac{T}{V_{REF}} \cdot \frac{\delta(\Delta V_{BE})}{ln(p)} \tag{5.37}$$

Again, rearranging the equation leads to the following:

$$\frac{\Delta p}{p} < \frac{\delta(D_{out}) \cdot ln(p) \cdot V_{REF} \cdot q}{k \cdot T^2}. \tag{5.38}$$

The same values are used as they were used for equation 5.34 which results in a maximum inaccuracy for the current-mirror ratio:

$$\frac{\Delta p}{p} < \pm 1.4\ \% \tag{5.39}$$

This or even tighter requirements, for example an error contribution of ΔT = 0.01 °C, lead to the fact that DEM is needed, as was already said earlier.

According to [1] and [10], the needed open-loop gain can be computed to be

$$A_{OL} > \frac{V_{DD} - V_{GS}}{V_{os}} = \frac{2\ V - 0.6\ V}{483\ \mu V} \approx 3000 \approx 69\ dB. \tag{5.40}$$

The gate-source voltage V_{GS} is set to 600 mV because the overdrive voltage for the current mirror will be set to 200 mV, this will be explained later.

5.6.4 Noise Budget

The overall noise in the system to achieve a temperature error of ΔT = 0.1 °C can be computed as follows, using the sensitivity equations 5.12 and 5.13

$$\varepsilon(D_{out}) = \Delta T = S_{V_{BE}}^{D_{out}} \cdot v_{n,V_{BE}}, \tag{5.41}$$

and

$$\varepsilon(D_{out}) = \Delta T = S_{\Delta V_{BE}}^{D_{out}} \cdot v_{n,\Delta V_{BE}}. \tag{5.42}$$

Rearranging both equations 5.41 and 5.42 yields the maximum noise voltage for V_{BE} and ΔV_{BE}

$$v_{n,V_{BE}} < \frac{\varepsilon(D_{out})}{S_{V_{BE}}^{D_{out}}} = \frac{\pm 0.1\ °C \cdot 1.2\ V}{400\ K} = 300\ \mu V, \tag{5.43}$$

and for ΔV_{BE}

$$v_{n,\Delta V_{BE}} < \frac{\varepsilon(D_{out})}{S_{\Delta V_{BE}}^{D_{out}}} = \frac{\pm 0.1\ °C \cdot 1.2\ V}{(600\ K - 300\ K) \cdot 14.43} = 27.73\ \mu V. \tag{5.44}$$

In chapter 3.7, the theory of noise in BJTs and MOSFETs was described. The resolution of the circuit is mostly limited by the noise present in the voltages V_{BE} and ΔV_{BE}. This noise is partly due to thermal noise and shot noise in the diode-connected PNP transistors base resistance and collector current ([2], p. 27). Therefore, the noise can be written as

$$\begin{aligned} v_{n,V_{BE}}^2 &= \frac{i_{n,c}^2}{g_m^2} + 4kTR_BB_n = 2qI_CB_n\left(\frac{kT}{qI_C}\right)^2 + 4kTR_BB_n \\ &= \frac{2kT}{g_m}B_n + 4kTR_BB_n. \end{aligned} \tag{5.45}$$

According to [2] the 1/f-noise can be neglected because it is relatively small in BJTs. In addition, the noise due to the base resistance is also negligible because small bias currents are used (in the range of µA or smaller) which results in the $1/g_m$-related noise being the dominating noise in the base-emitter voltage V_{BE}. In [2] it is also assumed that the noise in the bias current is dominated by shot noise and adds to the overall noise in base-emitter voltage. Therefore, the V_{BE} voltage can be written as

$$v_{n,V_{BE}}^2 = \frac{2kT}{g_m}B_n + \frac{2qI_{bias}}{g_m^2}B_n = \frac{4kT}{g_m}B_n. \tag{5.46}$$

The difference voltage ΔV_{BE} is a combination of two V_{BE} voltages. This means that the noise present in ΔV_{BE} is the sum of the noise of two PNP transistors ([2], p. 27).

$$v_{n,\Delta V_{BE}}^2 = v_{n,V_{BE1}}^2 + v_{n,V_{BE2}}^2 = \frac{4kT}{g_m}B_n \cdot \left(1 + \frac{1}{p}\right) \tag{5.47}$$

The succeeding ΔΣ-ADC integrates the voltages V_{BE} and ΔV_{BE}, and thus also the noise present in these voltages, during a period T_{conv} which is the conversion time. The integration is equivalent to filtering the noise with a sinc filter with a noise bandwidth $B_n = 1/(2 \cdot T_{conv})$. According to [2] the integrated noise voltages can be written as

$$v_{n,V_{BE}} = \sqrt{\frac{2kT}{g_m} \cdot \frac{1}{T_{conv}}}, \tag{5.48}$$

$$v_{n,\Delta V_{BE}} = \sqrt{\frac{2kT}{g_m} \cdot \frac{1}{T_{conv}} \cdot \left(1 + \frac{1}{p}\right)}. \tag{5.49}$$

Taking equations 5.48 and 5.49 and multiply them with the sensitivity equations 5.12 and 5.13, respectively, results in the noise at the output of the sensor.

$$\sigma_{T,V_{BE}} = S^{D_{out}}_{V_{BE}}(T) \cdot v_{n,V_{BE}} = -\frac{T}{V_{REF}} \cdot \sqrt{\frac{2kT}{g_m} \cdot \frac{1}{T_{conv}}} \tag{5.50}$$

$$\sigma_{T,\Delta V_{BE}} = S^{D_{out}}_{\Delta V_{BE}}(T) \cdot v_{n,\Delta V_{BE}} = \frac{A-T}{V_{REF}} \cdot \alpha \cdot \sqrt{\frac{2kT}{g_m} \cdot \frac{1}{T_{conv}} \cdot \left(1+\frac{1}{p}\right)}. \tag{5.51}$$

Based on the simulated forward-current gain β_F versus the collector current I_C a current is chosen to bias the BJTs (see chapter 3.4). If a current I_C = 450 nA ($5I_{bias}$) is chosen then the noise contribution can be calculated. The transconductance of the BJT can be computed as shown in equation 5.52. For $\sigma_{T,\Delta V_{BE}}$ the transconductance of the BJT with the lower bias current is used.

$$g_m = \frac{qI_C}{kT} \tag{5.52}$$

Taking the equations 5.50 and 5.51 and filling in all the parameters with tightest temperature requirements and a conversion time of T_{conv} = 5 ms leads to the following

$$\sigma_{T,V_{BE}} = -\frac{400\ K}{1.2\ V} \cdot \sqrt{\frac{2k \cdot 400\ K}{13.06\ \mu\frac{A}{V}} \cdot \frac{1}{5\ ms}} \approx 0.137\ mK, \tag{5.53}$$

$$\begin{aligned}\sigma_{T,\Delta V_{BE}} &= \frac{600\ K - 300\ K}{1.2\ V} 2 \cdot 14.43^2 \cdot \sqrt{\frac{2k \cdot 300\ K}{17.41\ \mu\frac{A}{V}} \cdot \frac{1}{5\ ms} \cdot \left(1+\frac{1}{5}\right)} \\ &\approx 2.73\ mK.\end{aligned} \tag{5.54}$$

The results show that first of all the noise in the difference voltage ΔV_{BE} is much larger than the noise in V_{BE} and that the output-referred noise of the BJTs is negligible. Usually, the readout circuitry and the quantization noise are the dominating noise sources ([1], p. 165).

5.6.5 Budget Summary

The previous sections were setting the budget for the analog front-end that should be met to fulfil the requirements set in section 5.2. Table 5.2 lists the budget for the circuit which also serves as design guideline.

Table 5.2: Design specifications of the analog front-end.

Parameter	Budget
I_S and R_{bias} errors	< 0.87 %
Input offset voltage	$\pm$ 483 µV
Current density ratio bias circuit	< 1.4 %
Current density ratio bipolar core	< 0.107 %
A_{OL}	$>$ 69 dB
Noise V_{BE}	$<$ 300 µV
Noise ΔV_{BE}	$<$ 27.73 µV

5.7 Analog Front-End Design

5.7.1 Introduction

After the budgeting of the system is done the sizing of the transistors is the next step. The sizing of the transistors is more or less an estimate. Thus, it might include several iterations combined with simulation to achieve the final device dimensions.
First, the sizing of the bias resistor will be explained and then the current mirror of the bias circuit will be sized. Afterwards, the design of the op amp will be explained. Thereafter, the design of the chopper and the DEM, as well as the start-up circuit will be explained. In the end, the test of the design and changes are briefly described.

5.7.2 PNP Transistors and Bias Resistor

The PNP transistors that are used in the proposed design of [5] have an emitter area of 5 µm x 5 µm. The same PNP transistors are available in the 90 nm process kit and are therefore used.
The bias resistor will be made out of p-poly resistors without silicide to achieve high sheet resistances. In section 5.5 the bias current was determined at which the forward current gain of the PNP transistors is almost constant. The value was set to I_{bias} = 90 nA. Thus, the value of the bias resistor can be calculated using the equation 4.2 by rearranging it

$$
\begin{aligned}
R_b &= \frac{\Delta V_{BE}}{I_{bias}} \cdot \frac{\beta+1}{\beta} \\
R_b &= \frac{\frac{kT}{q} \cdot ln(p)}{I_{bias}} \cdot \frac{\beta+1}{\beta} \\
R_{bias} &= \frac{\frac{k \cdot 300\ K}{q} ln(5)}{90 \cdot 10^{-9}\ A} \cdot \frac{2.6+1}{2.6} = 639880\ \Omega \approx 640\ k\Omega.
\end{aligned}
\tag{5.55}
$$

The final value was set to

$$R_{bias} = 643\ k\Omega, \tag{5.56}$$

to adjust the bias current to be closer to 90 nA. As can be seen, the bias resistor is quite large this will result in large structures on the chip. However, if ultra-low power consumption is crucial then this trade-off is necessary.

5.7.3 Current Mirror

The bias current of the bias circuit is set by the bias resistor to I_{bias} = 90 nA. The MOSFETs are supposed to work in saturation region, therefore the drain-source voltage V_{ds} needs to be larger than the overdrive voltage V_{ov}. In addition, the gate-source voltage V_{SG} (positive polarity for PMOS) needs to be larger than the threshold voltage V_{tp}. Further, the transistors are supposed to be biased in strong inversion. Therefore, an overdrive voltage of V_{ov} = 130 mV is chosen.
Using square-law models for estimation it is possible to calculate a ratio of the dimensions of the transistor ([9], p. 41)

$$V_{ov} = V_{SG} - |V_{tp}| = \sqrt{\frac{2I_{bias}}{\mu_p C_{ox} W/L}}, \tag{5.57}$$

where $\mu_p C_{ox}$ is the product of the carrier mobility and the oxide capacitance. Rearranging the equation leads to the ratio of the width and length W/L

$$\frac{W}{L} = \frac{2I_{bias}}{V_{ov}^2 \cdot \mu_p C_{ox}}. \tag{5.58}$$

The value of $\mu_p C_{ox}$ was found using the simulator and biasing a PMOS transistor at bias point with V_{ov} = 130 mV and a W/L-ratio of 5 µm / 5 µm. The value *betaeff* in Cadence is defined as

$$betaeff = \mu_p C_{ox} \cdot \frac{W}{L}. \tag{5.59}$$

To make sure that it only depends on $\mu_p C_{ox}$ the W/L-ratio was set to 1 with a length L larger than 1 µm because the transistors are likely to have a long gate due to the small current.

It was found to be

$$betaeff = 122.14\ \mu\frac{A}{V^2}. \tag{5.60}$$

Inserting 5.60, V_{ov} = 130 mV and the bias current I_{bias} into equation 5.58 yields

$$\frac{W}{L} = \frac{2 \cdot 90 \cdot 10^{-9}\ A}{0.13^2\ V^2 \cdot 122.14\ \mu A/V^2} = 0.0872. \tag{5.61}$$

Through simulation it was found that the ratio is closer to

$$\frac{W}{L} = 0.1081. \tag{5.62}$$

In equation 5.39 the maximum mismatch for the current mirror was calculated and found to be $\Delta p / p = 1.4\ \%$. This mismatch requirement is used to determine the necessary area WL of the transistors. It is possible to calculate matching of MOS transistors using the following equation to define the mismatch in the threshold voltage [12]

$$\sigma^2(V_{t0}) = \frac{A_{Vt0}^2}{WL} + S_{Vt0}^2 D^2, \tag{5.63}$$

where σ^2 is the standard deviation of the threshold voltage V_{t0}, $A_{Vt0}{}^2$ is a process dependent constant, WL the area, $S_{Vt0}{}^2$ a process dependent constant and D^2 the distance between two devices. If the devices are closely spaced the right part of the equation is negligible. The same can be written for the betaeff from equation 5.60, which will be called K [12]

$$\frac{\sigma^2(K)}{K^2} = \frac{A_K^2}{WL} + S_K^2 D^2. \tag{5.64}$$

The process constants $A_{Vt0}{}^2$ and $A_K{}^2$ are not available for the 90 nm gpdk used for this thesis. Therefore, values of a 180 nm process were used instead to get an initial estimate. The constant for threshold voltage is assumed to be $A_{Vt0}{}^2$ = 20 $mV^2\mu m^2$, and for the K parameter for PMOS $A_K{}^2$ = 0.5711 $\%^2\mu m^2$.
Using both standard deviation equations 5.63 and 5.64, it is possible to calculate the relative error in I_D for two transistors with the same V_{GS} [13]

$$\begin{aligned}\left(\frac{\sigma(\Delta I_D)}{I_D}\right)^2 &= \left(\frac{g_m}{I_D}\right)^2 \cdot \sigma^2(\Delta V_t) + \frac{\sigma^2(\Delta K)}{K^2} \\ &= \frac{1}{WL} \cdot \left[A_{Vt0}^2 \left(\frac{g_m}{I_D}\right)^2 + A_K^2\right].\end{aligned} \tag{5.65}$$

Rearranging the equation yields

$$WL = \frac{1}{\left(\frac{\sigma(\Delta I_D)}{I_D}\right)^2} \cdot \left[A_{Vt0}^2 \left(\frac{g_m}{I_D}\right)^2 + A_K^2\right]. \tag{5.66}$$

Inserting all parameters where

$$\left(\frac{\sigma(\Delta I_D)}{I_D}\right)^2 = \left(\frac{\Delta p}{p}\right)^2 = (0.014)^2, \tag{5.67}$$

and

$$g_m = \frac{2I_D}{V_{ov}}, \tag{5.68}$$

yields the area WL of the PMOS current mirror devices:

$$WL = 24.318\ \mu m^2. \tag{5.69}$$

To make sure that 99.7 % (3σ) of the devices are matching the area has to be tripled which results in

$$WL = 72.954\ \mu m^2. \tag{5.70}$$

With the ratio W/L $\approx$ 0.11 and the area WL = 72.954 μm^2 the initial dimensions of the current mirror devices are calculated to be

$$\begin{aligned} L &= 26\ \mu m \\ W &= 2.8\ \mu m. \end{aligned} \tag{5.71}$$

These device dimensions are used as unit size for the current mirror devices. Table 5.3 shows the sizes for the initial design of the two current mirror devices. The width of M_{13} is multiplied by 5 to achieve the right current ratio. In Cadence, this is implemented by using the multiplier function of the device which puts 5 devices in parallel. For the final device sizes it was decided to use the maximum length of one device and adjust the width accordingly to leave some margin.

Table 5.3: Aspect ratios of the current mirror devices M_{12} and M_{13}.

Device	Width [µm]	Length [µm]
M_{12}	3.2	30
M_{13}	$5 \cdot 3.2$	30

5.7.4 Operational Amplifier

The gain expression of the operational amplifier was already mentioned in section 5.3. The sizing of the devices is based on the gain expression but also on the overall requirements, especially the current consumption. Therefore, as shown in figure 5.3, the input differential pair is biased with I_d = 90 nA which is why M_{11} is twice the size of M_{13}. The same applies to M_{10} and M_9.
The differential input pair was sized in such a way that the overdrive voltage V_{ov} equals 100 mV. This means that the transistors are biased in saturation region and barely in strong inversion. This way the transconductance g_m of the transistors is still quite high and the

transistor behaves according to the square-law model, which makes matching easier. However, matching is not as important for the input pair as for the current mirror because chopping is used (see chapter 4.3).
Since the matching is not too important due to chopping it was decided to aim for an offset voltage of the input pair in the range of 1 mV. Using the mismatch equation for differential input pairs according to [9]

$$\sigma^2(V_{os}) = \frac{1}{WL} \cdot \left[A_{Vt0}^2 + \left(\frac{I_D}{g_m} \right)^2 A_K^2 \right]. \tag{5.72}$$

The values for the all parameters are the same as were used for equation 5.65. Setting the offset voltage for a variance of 3σ to 1 mV yields an area of

$$WL = 24.46\ \mu m^2. \tag{5.73}$$

This results in a width and a length of W = 1.9 µm and L = 12.77 µm. The initial dimensions are chosen slightly larger to leave some margin and can be found in table 5.4.
The NMOS loads of the differential pair are also sized to be in saturation region and strong inversion. An overdrive voltage of 130 mV, the same as for the current mirror, was chosen. As was done for the PMOS transistors, the value of $\mu_n C_{ox}$ was found by simulating an NMOS transistor in saturation with the overdrive voltage of 130 mV and an aspect ratio of W/L = 5 µm / 5 µm. It was found to be

$$betaeff = 211.87\ \mu \frac{A}{V^2}. \tag{5.74}$$

Using equation 5.58 an estimate of the aspect ratio is found

$$\frac{W}{L} = \frac{2 \cdot 90 \cdot 10^{-9}\ A}{0.13^2\ V^2 \cdot 211.87\ \mu A/V^2} = 0.05027. \tag{5.75}$$

By using the simulator and iterating the more accurate aspect ratio was found to be

$$\frac{W}{L} = 0.05769. \tag{5.76}$$

The NMOS devices of the op amp are biased with the same drain current I_D, which means that the gate-source voltage of the devices varies. To achieve high matching of the NMOS devices in the op amp the maximum length for a single device was chosen. This is limited by Cadence to L = 30 µm. Accordingly, the width can be calculated with equation 5.76. The width and length result in an area of WL = 51.921 μm^2.
The variance of the gate-source voltage can be calculated as follows ([14], p. 102.)

$$\begin{aligned} \sigma^2(V_{GS}) &= \left(\frac{I_D}{g_m} \right)^2 \cdot \frac{\sigma^2(\Delta K)}{K^2} + \sigma^2(\Delta V_t) \\ &= \frac{1}{WL} \cdot \left[A_{Vt0}^2 \left(\frac{I_D}{g_m} \right)^2 + A_K^2 \right] \end{aligned} \tag{5.77}$$

Inserting the area WL = 51.921 μm^2, the process constants $A_{Vt0}{}^2$ = 20 $mV^2\mu m^2$ and $A_K{}^2$ = (0.865 $\%\mu m)^2$, as well as the bias current I_D = 90 nA and g_m as in equation 5.68, in the above equation yields a variance of

$$\begin{aligned} \sigma^2(V_{GS}) &= 1.43\ \mu V^2 \\ \sigma(V_{GS}) &= 1.2\ mV. \end{aligned} \tag{5.78}$$

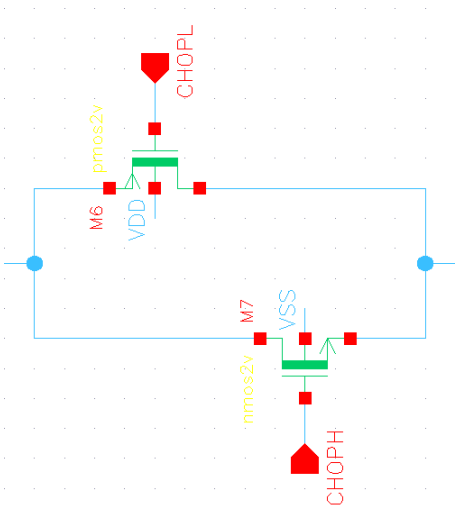
The initial values that were chosen for the devices of the operational amplifier are listed in table 5.4. Again, the multiplication means that there are n devices in parallel.

Table 5.4: Aspect ratios of the operational amplifier devices.

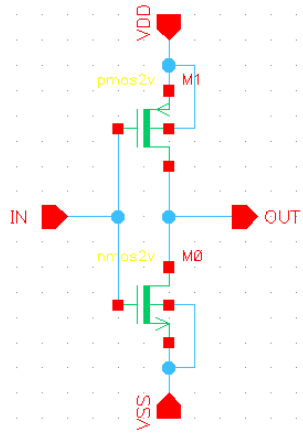
Device	Width [μm]	Length [μm]
M_1	1.75	30
M_2	1.75	30
M_3	$4 \cdot 1.75$	30
M_4	1.75	30
M_5	2	13
M_6	2	13
M_7	$4 \cdot 1.75$	30
M_8	1.75	30
M_9	3.2	30
M_{10}	$4 \cdot 3.2$	30
M_{11}	$2 \cdot 3.2$	30

5.7.5 Chopping Circuit

The chopping of the amplifier was designed as explained in chapter 4.3. The switches are designed as transmission gates (figure 5.6a) made out of one PMOS and one NMOS transistor for each switch. This is done because PMOS transistors can pass higher voltages better and NMOS transistors lower voltages which ensures that signals in a range from close to ground to supply voltage can be passed. Signals between the supply rail and ground are passed the worst because the on resistance r_{on} of the transistors is the highest. However, these switches are only passing a very small current which is due to dynamic effects of charging gate-source capacitances. The charge stored on the parasitic capacitances is the reason for voltage spikes during the switching [15]. To keep the parasitics low and since the speed of the transmission gates does not have to be very high, the switches are designed with minimum size of W = 150 nm and L = 280 nm.



(a) Transmission gate in Cadence.



(b) Inverter in Cadence.

Figure 5.6: Transmission gate and inverter in Cadence

The clock signal for the chopping switches has to be also inverted which requires an inverter circuit, which can be seen in figure 5.6b. The clock inverter circuit consists of three inverters and one transmission gate. This setup is due to the fact that one inverter has an inherent delay for passing voltages. To account for this delay an always on transmission gate is included in the inverting branch. The non-inverting branch consists of two inverters. The circuit schematic can be seen in B.6. All transistors are minimum sized. Table 5.5 lists the device dimensions.

Table 5.5: Aspect ratios of the switch devices.

Device	Width [µm]	Length [µm]
PMOS	0.15	0.28
NMOS	0.15	0.28

5.7.6 Start-up Circuit

A bandgap reference circuit has two stable bias points. The bias point the circuit is designed for and a so-called ”degenerate” bias point ([10], p. 512). The degenerate bias point occurs when there is no current flowing through the branches of the bias circuit. To get the circuit out of the zero-current state it is necessary to force some current into one branch so that the op amp in feedback configuration starts to regulate the voltage difference at its inputs. This leads to the start up of the circuit until it is settled at the bias point it is designed for.
The start-up circuit for this bias circuit can be seen in figure 5.7. It consists of three transistors and a start-up resistance. The transistor M_{16} is always on even though there is no current flowing. It acts as cascode transistor for M_{14}. If there is no current flowing

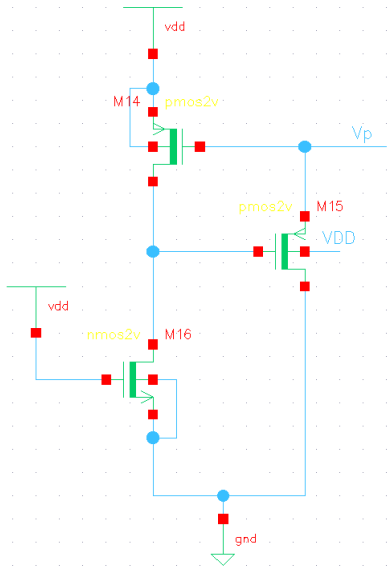


Figure 5.7: Start-up circuit in Cadence.

through M_{14} then no current is flowing through M16 either which pulls down the voltage at the gate of M_{15}. M_{15} is connected to the node V_p which is the output of the op amp and the gate voltage of the PMOS current mirrors. Once the voltage V_p is pulled down by M_{15} the current mirrors start conducting which forces a current to flow. When the current that is flowing through transistor M_{16} is increasing the voltage at the gate of M_{15} will rise which turns it off. Therefore, the start-up circuit is not connected to the bias circuit anymore. However, this circuit draws steady-current which is limited by the start-up resistance. Since the steady-current should be as small as possible this variant of the start-up circuit relies on a very large resistance in the range of megaohms (MΩ).
The transistor M_{14} is a current mirror, and therefore sized as the other current mirrors, as described in 5.7.3. Transistor M_{15} should be sized such that the current flowing through it is as small as possible which leads to long and narrow transistor. Its size was chosen with minimum width W = 150 nm and a length of L = 20 µm. The size of transistor M_{16} was also chosen to be a long and narrow transistor as well, and therefore it has the same size, W = 150 nm and L = 20 µm. The sizes are summarised in table 5.6. The start-up resistance is 50 MΩ. Because of the size of the resistance it was decided to use an ideal resistor.

Table 5.6: Aspect ratios of the start-up circuit devices.

Device	Width [µm]	Length [µm]
M_{14}	3.2	30
M_{15}	0.15	20
M_{16}	0.15	20

5.7.7 Dynamic Element Matching

The dynamic element matching consists of switches and a controller which periodically switches the current mirrors in the bipolar core. However, only the switches are implemented in this thesis. To generate the control signals of the switches, voltage sources are used that generate pulses for the switches. The switches are using the same transmission gates as the chopping switches (see 5.6a). The dimensions are listed in table 5.5. The frequency of the switching was chosen to be six times faster as the chopping, so that one complete cycle of the DEM is done in one cycle of chopping.

5.7.8 Test of Initial Design

This section describes how the iterative approach to improve the design was carried out by testing the initial design described in this chapter and by using simulations which are briefly described next chapter (see 6.2). Table 5.7 shows the final device dimensions. Even though the circuit shows the expected behaviour in terms of bias currents and voltages, as well as sufficiently high gain and stability over the corners for DC operating point analyses, it did not fulfil all the requirements of section 5.6. The Monte-Carlo simulations showed that the sensors input offset voltage showed a variance of 3σ higher than the requirement (see chapter 5.6.5). The current density ratio showed also high variations, as well as the gain. In Cadence, it is possible to see which device contributes to mismatch between devices. For example, it was shown that the current mirror devices M_{12} and M_{13} have a large effect on the variation of the input offset voltage. Therefore, in an iterative way, the design was simulated and improved by checking which device affects which parameter the most and which devices mismatch can be reduced.
The current mirror devices M_{12} and M_{13} showed great influence on the input offset voltage. This means that their matching needs to be improved. In chapter 5.7.3, the equation 5.65 for the matching of current mirrors was used, it is not surprising that the mismatch is not quite as expected. This is due to the fact that the process parameters A_{Vt0} and A_K that were used are not for this process design kit. Thus, to increase the matching of the devices which is mostly dependent of the threshold voltage, the area of the transistors was increased and at the same time the overdrive voltage was increased to lower the effect on the input offset voltage. Therefore, the new overdrive voltage for all current mirrors is set to 200 mV and the area is increased from 96 μm^2 to around 150 μm^2. This results in a new width and length for all PMOS current-mirror devices. The values can be found in table 5.7.
In addition, it was tried to lower the input offset voltage and to improve the current density ratio of the bipolar core by increasing the area of the NMOS devices in the op amp. However, increasing the area increases the capacitances which slows down the circuit. Nevertheless, since temperature usually does not change very rapidly it is acceptable to have low speeds. Therefore, all NMOS devices were changed to larger areas while keeping the overdrive voltage the same. It was found after running MC-simulations that the current density ratio and the offset voltage improved, however, for temperatures at the end of the range the current density ratio got significantly worse. This led to the decision to keep the NMOS devices as before. The device dimensions are shown in table 5.7.
The differential input pair greatly affects the input offset voltage, however, since chopping

is used these two transistors are kept the same.
All of the current mirror devices are exceeding the length limit for a single device which is set to L = 30 µm. Therefore, it was necessary to ”cascode” two devices. When two devices are biased with the same gate voltage they behave like one transistor with the length of both devices summed up. This is called a ”poor man’s” cascode ([10], p. 88).

Table 5.7: Final aspect ratios of all devices.

Device	Width [µm]	Length [µm]
Current Mirror		
M_{12}	2.77	55
M_{13}	$5 \cdot 2.77$	55
Operational Amplifier		
M_1	1.75	30
M_2	1.75	30
M_3	$4 \cdot 1.75$	30
M_4	1.75	30
M_5	2	13
M_6	2	13
M_7	$4 \cdot 1.75$	30
M_8	1.75	30
M_9	2.77	55
M_{10}	$4 \cdot 2.77$	55
M_{11}	$2 \cdot 2.77$	55
Bipolar Core		
M_{17}	$2 \cdot 2.77$	55
M_{18}	$2 \cdot 2.77$	55
M_{19}	$2 \cdot 2.77$	55
M_{20}	$2 \cdot 2.77$	55
M_{21}	$2 \cdot 2.77$	55
M_{22}	$2 \cdot 2.77$	55
Start-Up Circuit		
M_{14}	$2 \cdot 2.77$	55
M_{15}	0.15	20
M_{16}	0.15	20
Switching Devices		
PMOS	0.15	0.28
NMOS	0.15	0.28

Chapter 6

Simulation

6.1 Introduction

Chapter 6 presents the simulation of the circuit, and afterwards the results. It starts by explaining the different analyses that were conducted in section 6.2. Afterwards, the performance of the analog front-end is presented in section 6.3.

6.2 Simulations

To test the circuit a variety of simulations are available in Cadence Virtuoso but only a few are conducted to check the correct operation. A very brief overview of the simulations that were used is given
The DC operating point analysis checks the bias point of the circuit, where it is possible to check all the assumptions made about the circuit, such as bias currents, voltages, resistances or capacitances.
The AC analysis is used to test the circuit to see how it reacts to a small signal stimulus around the DC operating point, which includes, for example, the frequency response of the circuit, as well as the bandwidth and amplification. Similarly, the stability analysis can be used to check the frequency response of the system and whether it is stable or not.
The transient analysis computes the transient response of the circuit over a specified time interval.
The noise analysis analyses the noise contribution of every device and computes the total output referred noise.
Monte-Carlo (MC) simulations are used to simulate the random effects of processing spreads and to receive an overview of statistical variations of the devices parameters and how mismatch of the devices affect the performance.
Corner simulations are used to test the circuit for extreme cases in terms of device parameters, such as thinner gate oxide or lower threshold voltage. These extreme cases can occur due to process variations. There are four corners and the nominal ”corner”, shown

in figure 6.1. These corners are named FF, SS, FS, SF and NN, where the first of the letters stands for the NMOS and the second letter for the PMOS. They describe the speed of the MOS-devices. Therefore, the FF-corner includes fast NMOS and fast PMOS devices and so on ([10], p. 709). All of the mentioned simulations are also conducted over all corners.

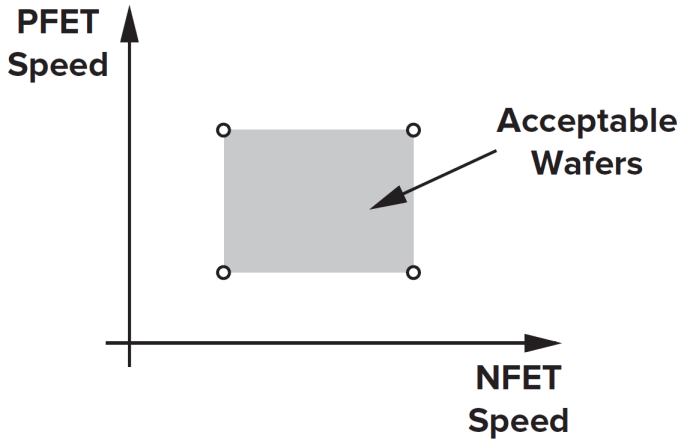


Figure 6.1: Process corners and speed of NMOS and PMOS devices ([10], p. 709).

6.3 Achieved Performance

6.3.1 Performance of the Analog Front-end

After several iterations on the design were performed the final version will be presented here with the help of simulation results. The sensor will be analysed such that an overview of the analog front-end performance for the nominal case is given at the three temperatures T = -55 °C, 27 °C and 125 °C including the variance σ of each parameter.
First, the analog front-end uses an area of around 0.06 mm^2 which meets the set requirement. Second, the current consumption of the the analog front-end, the bias circuit and the bipolar core are presented in table 6.1. The bias current achieves the desired current of I_{bias} = 90 nA at the nominal temperature of T = 27 °C and voltage supply of V_{DD} = 2 V.

The designed analog front-end achieves a comparable low current as bias current and total op amp current as the proposed temperature sensor. The total analog front-end current consumption is similar to the stated 2.1 µA of [5], too. The start-up circuit was excluded from the analysis because it draws a steady-current while the sensor is sampling the temperature. Due to the limited time available this simple solution was chosen instead of implementing a start-up circuit that draws no steady-current. It has to be stated that the results presented in table 6.1 were retrieved from a DC operating point analysis and do not consider processing spread or mismatch.

Table 6.1: Area and current consumption of the analog front-end.

Parameter			
Area		0.06 mm^2	
Supply voltage		2 V	
	T = -55 °C	T = 27 °C	T = 125 °C
I_{bias}	66.25 nA	90.29 nA	118.36 nA
Op amp total	462.88 nA	631.09 nA	813.8 nA
bias circuit	860.39 µA	1.173 µA	1.512 µA
bipolar core	795.05 nA	1.084 µA	1.397 µA
total (w/o start-up)	1.655 µA	2.256 µA	2.909 µA

Table 6.2 shows the MC simulation results of the generated bias current I_{bias} and the base-emitter voltage V_{BE}, as well as the difference voltage ΔV_{BE}. The deviation over 3σ of the bias current I_{bias} is quite large. According to the MC simulation this spread in the bias current can be referred to the saturation current spread in the BJTs. However, the current density ratio p is much smaller, which is important for achieving accurate voltages. This will be described further down based on table 6.4.
The base-emitter voltage V_{BE} shows that it is in the expected range based on simulation of a diode-connected BJT (refer to figure 3.5). Similarly the difference voltage ΔV_{BE} is close to the expected ideal value.

Table 6.2: Bias current and base-emitter voltage of the bias circuit.

Parameter	Min	Mean	Max	Std Dev (σ)
T = -55 °C				
I_{bias}	59.4 nA	66 nA	73.6 nA	2.6 nA
V_{BE}	707.8 mV	709.2 mV	711.3 mV	694 µV
ΔV_{BE}	39.5 mV	42.4 mV	46 mV	1.3 mV
T = 27 °C				
I_{bias}	82.1 nA	89.9 nA	99.6 nA	3.2 nA
V_{BE}	539.2 mV	541.1 mV	543.8 mV	885.5 µV
ΔV_{BE}	53.8 mV	57.7 mV	62.6 mV	1.8 mV
T = 125 °C				
I_{bias}	108.5 nA	117.9 nA	129.9 nA	4 nA
V_{BE}	331.8 mV	334.5 mV	337.9 mV	1.1 mV
ΔV_{BE}	70.6 mV	75.7 mV	82.1 mV	2.3 mV

Table 6.3 shows the simulation results of the bipolar core. The bias current of the bipolar core matches closely the bias current of the bias circuit. The base-emitter voltage matches the expected values, as well as the difference voltage ΔV_{BE} which is close to the expected values obtained from equation 3.8.
The standard deviation of the base-emitter voltages V_{BE} and the difference voltage ΔV_{BE} for both circuits stand out due to their large values. Those values are expected and can be explained to originate in the spread of the saturation current I_S and the bias resistor R_b

(chapter 3.4 and 5.6.1). According to the MC simulations the deviation in the bias circuit voltages stems almost exclusively from the saturation current of the two PNP BJTs. The same can be seen for the base-emitter voltages of the bipolar core. Since the difference voltage ΔV_{BE} is dependent of both base-emitter voltages (V_{BE1} and V_{BE2}, see equation 3.7) the error is much larger compared to V_{BE}. This deviation can be reduced to very small errors by using a trimming technique (chapter 4.6). However, the sensor proposed in [5] uses a single digital trim of α (equation 2.5) to compensate for PTAT errors in V_{BE}, therefore, no trimming was implemented in the analog front-end in this thesis.

Table 6.3: Bias current and base-emitter voltage of the bipolar core.

Parameter	Min	Mean	Max	Std Dev (σ)
T = -55 °C				
I_{bias}	118.7 nA	132.1 nA	147.1 nA	5.2 nA
V_{BE}	705.3 mV	707.6 mV	709.9 mV	818.9 µV
ΔV_{BE}	30.2 mV	31.9 mV	33.9 mV	837.6 µV
T = 27 °C				
I_{bias}	163.9 nA	179.9 nA	199.2 nA	6.5 nA
V_{BE}	536.3 mV	539 mV	542 mV	1.1 mV
ΔV_{BE}	41.3 mV	43.8 mV	46.6 mV	1.2 mV
T = 125 °C				
I_{bias}	216.8 nA	235.9 nA	259.9 nA	8.1 nA
V_{BE}	329.1 mV	332.6 mV	336.5 mV	1.5 mV
ΔV_{BE}	53.9 mV	57.2 mV	60.9 mV	1.5 mV

The current density ratio of both circuits is presented in table 6.4. The current ratio is very close to the ratio of p = 5, which was the aim. In chapter 5.6.2 the maximum mismatch in the current sources for the bipolar core and in chapter 5.6.3 the mismatch for the current sources in the bias circuit were computed. The mismatch in the bipolar core needs to be smaller than $\Delta p / p = 0.107$ %. In the bias circuit it should be smaller than $\Delta p / p = 1.4$ %. It can be seen that for a deviation of 3σ the bipolar core current density ratio at its worst for the the nominal process corner is at -55 °C, where it is around 0.054 %, and therefore, smaller than the requirement. Which was achieved due to the usage of DEM for the current sources (chapter 4.4). The bias circuit deviation at its worst is with 0.66 % smaller than the requirement, too.
The current ratio of the bias circuit is well distributed around the aim of p = 5, whereas the ratio for the bipolar core is slightly too high. This might originate in the switching due to the DEM, which was not well adjusted. The DEM results in large current spikes while switching, which might have the effect of increasing the current ratio because in MC simulations without the use of DEM the two current ratios were exactly the same. The DEM and the current spikes will be shown later.

Table 6.4: Current density ratios of the bias circuit and the bipolar core.

Parameter	Min	Mean	Max	Std Dev (σ)
T = -55 °C				
Current density ratio bias	4.974	4.999	5.022	0.22 %
Current density ratio bipolar	5.014	5.016	5.021	0.018 %
T = 27 °C				
Current density ratio bias	4.979	4.999	5.017	0.18 %
Current density ratio bipolar	5.015	5.016	5.019	0.013 %
T = 125 °C				
Current density ratio bias	4.982	4.999	5.015	0.16 %
Current density ratio bipolar	5.001	5.004	5.005	0.01 %

In table 6.5 the DC loop-gain, phase margin and gain-bandwidth product GBW are listed, and also the input offset voltage after chopping is applied. The mean of the DC loop-gain is somewhat lower as expected from the DC operating point analyses, where it was in the range of 66 dB for the nominal corner at 27 °C. It stands out that the standard deviation is very large for the loop-gain. A σ = 10 dB is a bad sign of some underlying problem, and therefore should be analysed thoroughly. According to the simulations different parameters are playing into the gain and its deviation. The variance contribution can be distributed to different components of the circuit, such as the current mirror devices of the op amp, or the differential input pair. Most of the variance contributions range from 1 % to 4 %, which is a sign that the matching in the circuit is fairly well. At 27 °C for the nominal corner, the NMOS-load transistor M_2 contributes by far the most to the variance with 21 %. Another large part goes to the bias resistor, which is around 17 %. Therefore, it suggests itself to improve the matching of the resistor by increasing its area, the same can be applied to the transistor M2. However, after several iterations on the design where the area of the bias resistor R_b was increased it was found that this measure did not improve the variance of the DC loop-gain. In addition, it seemed that the input offset voltage and the current density ratio were also negatively affected by this change. The NMOS-load was therefore subject for further possible improvements. Different approaches were tested on the design to achieve higher matching of the NMOS devices in the op amp. These approaches include the increase of area while keeping the overdrive voltage the same and increasing the aforementioned. The deviation in the DC loop-gain never significantly changed. The last test was conducted using ideal resistors for the bias resistor but even this did not change the problem. For this reason, it was decided that this problem has to be kept for future work (see chapter 7).
Apart from the DC loop-gain, table 6.5 shows that the phase margin of the loop is sufficiently high and that the system is stable with a 3σ = 1.4°. The gain-bandwidth product is not really high but as was mentioned before it is not really necessary since the temperature usually does not change very quickly. The settling time of the system will be shown further down.
The input offset voltage was decreased from $3\sigma \approx$ 2.1 mV to around 180 µV with chopping at 27 °C. To lower the input offset voltage even further a higher gain is necessary.

Table 6.5: DC loop gain, phase margin, gain-bandwidth product and input offset-voltage of the bias circuit.

Parameter	Min	Mean	Max	Std Dev (σ)
T = -55 °C				
DC loop gain	36 dB	52.2 dB	83.9 dB	8.8 dB
Phase margin	72.7°	74.4°	75.8 °	0.51°
GBW	5263.2 Hz	6379.5 Hz	8037.1 Hz	417.4 Hz
Offset w/ chopping	-497.4 µV	-9.3 µV	292.3 µV	112.4 µV
T = 27 °C				
DC loop gain	34.4 dB	52 dB	92.9 dB	9.7 dB
Phase margin	73.1°	74.7°	75.9°	0.47°
GBW	4969.8 Hz	5820.8 Hz	7113.1 Hz	326.8 Hz
Offset w/ chopping	-334.1 µV	-3 µV	177.1 µV	61.3 µV
T = 125 °C				
DC loop gain	33.8 dB	51.7 dB	100.3 dB	11.3 dB
Phase margin	73.1°	74.6°	76.1°	0.47°
GBW	4652.2 Hz	5380.4 Hz	6434.9 Hz	279.9 Hz
Offset w/ chopping	-188.8 µV	3.8 µV	125.5 µV	31 µV

6.3.2 Settling Time and Dynamic Effects

The settling time of V_p for the nominal case at 27 °C is depicted in figure 6.2. Once the supply voltage is turned on, the start-up circuit injects a current into the system. It clearly overshoots in the beginning when it starts but the voltage V_p settles without much ringing to its nominal value of V_p = 1.4 V in 110 µs. This is significantly below the requirement which was set to τ = 500 µs (compare table 5.2).

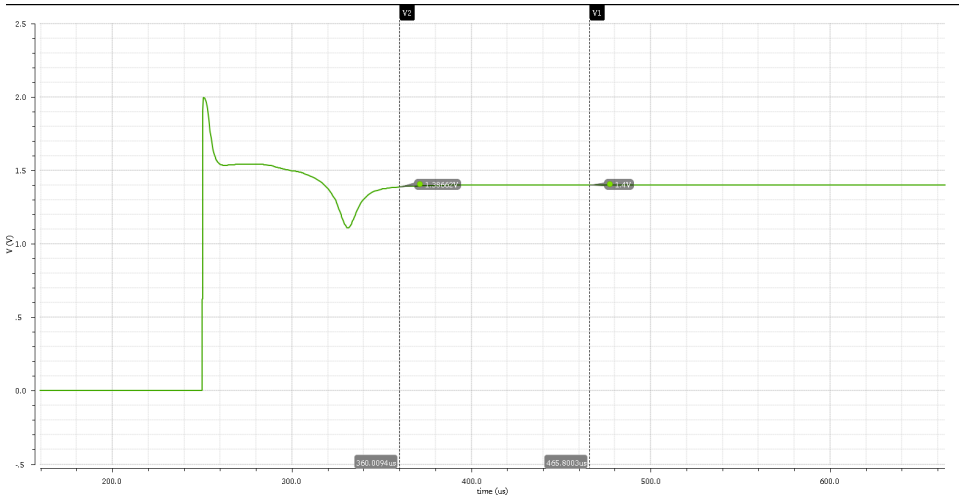


Figure 6.2: Settling of voltage V_p when the supply voltage is ramped from 0 V in 500 ns.

Due to the chopping and the DEM, dynamic effects arise that affect the voltages and the currents. The residual offset of the chopper amplifier is depending on clock feed-through and charge injection of the switches. The voltage spikes at the output of the chopper switch in front of the op amp are shown in figure 6.3. The voltages directly after the chopping show voltage spikes of around 30 mV. The voltage V_p at the output of the amplifier is almost not affected by these voltage spikes. Also the voltage V_{BE} shows only little variations in the range of a few micro volts due to the chopping, which is shown in figure 6.4.

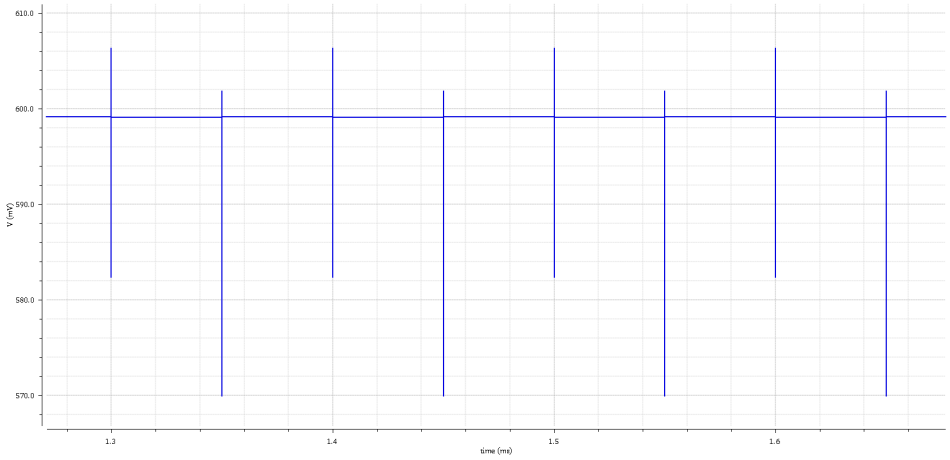


Figure 6.3: Voltage spikes due to switching of the chopper at the input of the differential pair.

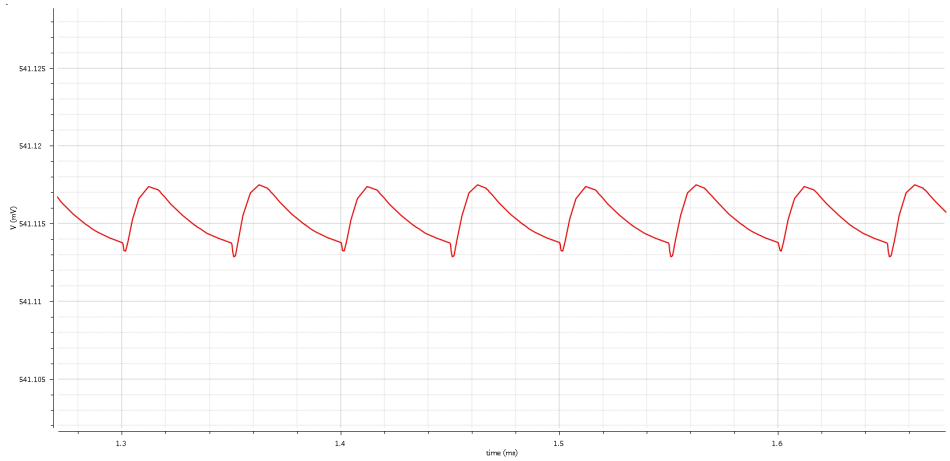


Figure 6.4: Effect of chopping on base-emitter voltage V_{BE1}.

Figure 6.5 shows the effect of the DEM. The DEM was not well adjusted to the system which is why it shows very large current spikes. These spikes are certainly unacceptable and need to be mitigated. This can be done by proper timing of the switches so that one

switch is fully open before another switch closes. In addition, the charge injection of the switches should be minimised. However, this is left for future work (see chapter 7).

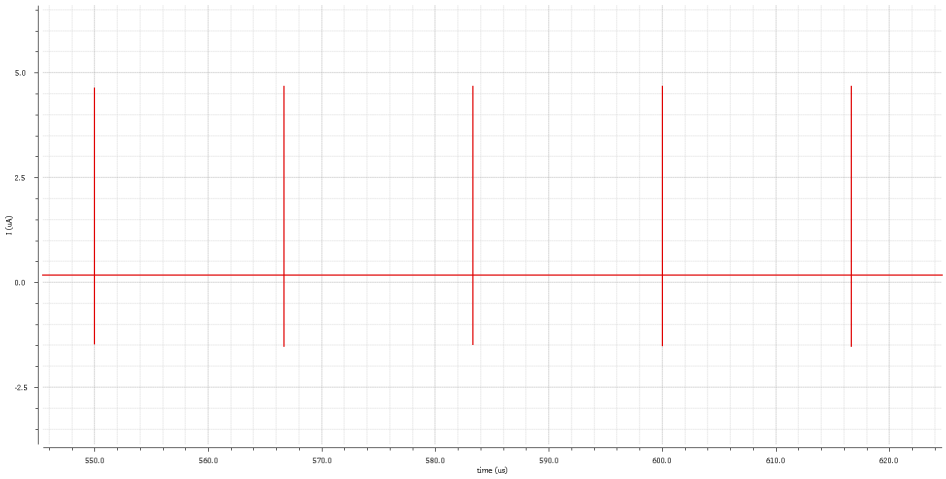


Figure 6.5: Current spikes due to DEM switching.

6.3.3 Noise

The total noise of the circuit was simulated for the outputs of the bipolar core. The noise bandwidth was set to 8 kHz, which is approximately equal to the bandwidth of the circuit. Table 6.6 presents the integrated noise for the V_{BE1}, V_{BE2} and the output noise in ΔV_{BE} which is a summation of the two base-emitter voltages. In chapter 5.6.4 a total noise limit was set to achieve a possible resolution of 0.1 °C. Using the sensitivity equations 5.12 and 5.13 the resulting error due to noise can be computed. The results are also shown in table 6.6. It has to be noted that the switching devices of the DEM were not included in the noise analysis. Due to the rather simple design of the switches and the large spikes it would result in high noise at the output.
The noise in the base-emitter voltages is far below the limit and results in negligible error contributions. The error in ΔV_{BE} can be calculated by summing the spectral densities of the base-emitter voltages ([2], p. 27). It is very close to the desired limit of 0.1 °C.
The highest noise contributors without the switching devices can be found to be thermal noise of the differential input pair of the op amp, as well as the NMOS load M_2. Adjusting the area of these transistors can help to reduce the flicker noise part. Also properly implementing the DEM and chopping switches can reduce the noise contribution by mitigating the flicker noise.

Table 6.6: Total noise at the output.

Noise	V	V^2	$\varepsilon(D_{out})$
T = -55 °C			
v_{VBE1}	20.85 µV	434.81 pV^2	0.0037 °C
v_{VBE2}	20.57 µV	423.09 pV^2	0.0037 °C
$v_{\Delta VBE}$	29.29 µV	857.9 pV^2	0.13 °C
T = 27 °C			
v_{VBE1}	22.84 µV	521.46 pV^2	0.0057 °C
v_{VBE2}	22.51 µV	506.63 pV^2	0.0056 °C
$v_{\Delta VBE}$	32.07 µV	1.028 nV^2	0.12 °C
T = 125 °C			
v_{VBE1}	24.91 µV	620.59 pV^2	0.0083 °C
v_{VBE2}	24.54 µV	602.06 pV^2	0.0081 °C
$v_{\Delta VBE}$	34.97 µV	1.022 nV^2	0.09 °C

6.3.4 Residual Temperature Error

The residual temperature error of the bias circuit and the bipolar core can be computed by using the sensitivity equations 5.12 and 5.13 and the results of the bipolar core presented in table 6.3. Since the proposed temperature sensor in [5] is using a digital approach by trimming the scaling factor α (see 2.5) to trim out the error in the base emitter voltages of the BJTs, the error in the base emitter voltage is therefore quite large. Nevertheless, the table 6.7 shows the 3σ residual errors and how they would affect the temperature reading at the output.

Table 6.7: Residual errors and the resulting temperature error $\varepsilon(D_{out})$.

	3σ signal deviation			3σ $\varepsilon(D_{out})$ deviation		
Error source	-55 °C	27 °C	125 °C	-55 °C	27 °C	125 °C
V_{BE}	2.457 mV	3.3 mV	4.5 mV	0.45 °C	0.6 °C	0.82 °C
ΔV_{BE}	2.512 mV	3.6 mV	4.5 mV	11.54 °C	12.98 °C	10.93 °C
current ratio p	0.054 %	0.039 %	0.03 %	0.047 °C	0.028 °C	0.039 °C

As can be seen, the error due to ΔV_{BE} extremely stands out. The base-emitter voltage is strongly dependent on the saturation current as was described before. Deviations of up to 4.5 mV are therefore expected. The difference voltage ΔV_{BE} is the result of V_{BE2} - V_{BE1} which is why it deviates that much as well. If the base-emitter voltage deviation can be reduced to microvolts by means of trimming, the deviation of ΔV_{BE} will significantly decrease, too. This is also in accordance with the MC simulation where it is shown that the variance contribution of both voltages stems almost entirely from the BJT's saturation current I_S.
The current density ratio of the bipolar core is lower than the requirements, and therefore fulfils the desired error contribution of 0.1 °C (see chapter 5.6.2).
The errors shown here include the errors of the bias circuit, as well. To show that the

desired results of the bias circuit are met, the error contributions are computed in table 6.8. Again, the base-emitter voltage shows large deviations, similar to the base-emitter voltage of the bipolar core and is therefore left out.

Table 6.8: Residual errors and the resulting temperature error $\varepsilon(D_{out})$ of the bias circuit.

	3σ signal deviation			3σ $\varepsilon(D_{out})$ deviation		
Error source	-55 °C	27 °C	125 °C	-55 °C	27 °C	125 °C
current ratio p	0.66 %	0.54 %	0.48 %	0.014 °C	0.022 °C	0.034 °C
Offset w/ chopping	337.2 µV	183.9 µV	93 µV	0.038 °C	0.029 °C	0.019 °C

The residual errors due to the current density ratio and the input offset voltage of the op amp are far below the set maximum limits.

6.3.5 Worst Case Analysis

Most of the circuit was tested over several hundred Monte Carlo simulations over each process corner. Table 6.9 shows the two worst cases of each parameter, for parameters that were tested with MC simulations it shows the 3σ range.

Table 6.9: Worst cases and their according process corner and temperature.

Parameter	Worst Case 1	Worst Case 2
Bias circuit		
I_{bias}	FS at 125 °C 3σ = 13.43 nA	FF at 125 °C 3σ = 13.05 nA
V_{BE}	SS at 125 °C 3σ = 3.58 mV	FS at 125 °C 3σ = 3.76 mV
ΔV_{BE}	SS at 125 °C 3σ = 7.96 mV	NN at 125 °C 3σ = 6.96 mV
Offset w/ chopping	FF at -55 °C 3σ = 565.2 µV	SS at 125 °C 3σ = 482.7 µV
current ratio p	SF at -55 °C 3σ = 0.71 %	FF at -55 °C 3σ = 0.71 %
DC loop-gain	FS at -55 °C 55 dB	SS at -55 °C 54.9 dB
Phase margin	SF at -55 °C 73.5°	NN at -55 °C 74.5°
Bipolar core		
I_{bias}	FS at 125 °C 3σ = 26.94 nA	FF at 125 °C 3σ = 26.16 nA
V_{BE}	SS at 125 °C 3σ = 4.62 mV	FS at 125 °C 3σ = 4.71 mV
ΔV_{BE}	FF at -55 °C 3σ = 4.62 mV	FS at 125 °C 3σ = 4.6 mV
current ratio p	FF at -55 °C 3σ = 0.24 %	FS at 125 °C 3σ = 0.15 %
Settling time	222 µs	188 µs
Noise V_{BE}	FS at 125 °C 26.4 µV	NN at 125 °C 24.9 µV
Noise ΔV_{BE}	FS at 125 °C 37.1 µV	NN at 125 °C 34.97 µV

The deviation in I_{bias} is not as important as the current density ratio p, however it was listed here to show its largest deviation. The current density ratio p needs to be as precise as possible to lower the temperature reading error. It can be seen that the current density ratio for the bias circuit fulfils the requirement of $\Delta p / p < 1.4$ %. However, for the bipolar core the two worst cases exceed the limit of $\Delta p / p < 0.107$ %. The variance contribution is distributed on many parts of the circuit which means that the matching is fairly well done. Higher matching might be achieved by a better designed DEM.
The input offset voltage of the op amp exceeds the aim of 483 µV in one case and barely

stays at the limit for the second case. This problem might be mitigated by precision layout of the differential input pair.
The settling time could not be analysed with MC simulations but the worst cases presented here, indicate that the margin to the required settling time is quite large.
The worst case noise in the base-emitter voltage V_{BE} is small enough to be neglected. The noise in ΔV_{BE} ranges between 0.1 °C and 0.15 °C and should therefore be reduced for the worst cases.
The worst gain achieved for DC operating point analysis was included. It shows that the gain is lower than the requirement. However, it might be sufficient to keep the input offset voltage low enough but this has to be verified after the problem of the large gain deviation was investigated. The phase margin is sufficiently high for every case with small standard deviations. The gain and phase margin for the nominal case and the two worst cases are shown in appendix A.

Chapter 7

Conclusion

The goal of this work was to design the analog front-end for a BJT-based temperature sensor. The temperature sensor was found while carrying out a literature review on state-of-the-art low-power sensors based on requirements stated in 1.1. The literature review was conducted as a pre-study to this Master's thesis at NTNU, Trondheim.
After presenting different design approaches of temperature sensors in CMOS process technology (chapter 2), the most important device physics of the bipolar junction transistor were explained in chapter 3. These include the ideal I-V-characteristics and the non-idealities, which are important for designing an accurate sensor. To mitigate errors due to processing spread and mismatch between the devices it is necessary to employ different techniques such as chopping or dynamic element matching.
In chapter 5, the specifications for the analog front-end are set based on the achievements of the proposed temperature sensor in [5]. After analysing the analog front-end and the operational amplifier, sensitivity equations were set up which are used to describe the sensitivity of the temperature reading D_{out} to errors in different parameters of the analog front-end. To complete the specifications for the analog front-end, those sensitivity equations were used to set up an error budget for the circuit (see table 5.2) that should be met in order to meet the specifications (see table 5.1). Afterwards, the sizing of the MOSFET devices is described which emphasises on the matching of the devices. After testing the initial design in Cadence Virtuoso using different simulation types, the design was adjusted to better meet the requirements.
Chapter 6 presents and discusses the results of the final design. The designed analog front-end achieves very similar current consumptions for the op amp, I_{opamp} = 631 nA, and the total analog front-end, I_{total} = 2.26 µA, as the proposed sensor, running on a voltage supply of V_{DD} = 2 V.
Two error and mismatch correction techniques are used to mitigate the input offset voltage of the op amp and the mismatch in the current sources of the bipolar core, which are chopping and DEM respectively. Due to the chopping of the op amp it was possible to reduce the offset voltage to $V_{os,3\sigma}$ = 184 µV, which results in a temperature error of
0.03 °C at 27 °C. The DEM manages to reduce the current density ratio error in the bipolar

core to around 0.054 % which equals a temperature reading error of around 0.03 °C. These values are well below the limit which was set beforehand. The base-emitter voltages and the difference voltage, however, show very large deviations. This is expected because no correction technique was used to account for processing spread in the saturation current of the BJTs. The proposed temperature sensor in [5] employs digital trimming of the saturation current of the BJTs which is why no analog correction technique was implemented. Reducing the deviation in the base-emitter voltages should therefore reduce the temperature reading errors to acceptable levels. The noise in the circuit was analysed without the switching devices of the DEM because the DEM was not properly set up due to limited time for this work. Without the DEM, the circuit achieves a noise level of around 32.1 µV in the difference voltage ΔV_{BE} of the bipolar core which results in a temperature reading error of around 0.12 °C. Thus, it does not completely fulfil the requirements set in the beginning.
The DC loop-gain of the bias circuit shows sufficiently high values for DC operating point analyses, however, when using MC simulations it shows extreme deviations of up to σ = 11 dB. This could mean that something in the circuit is designed too marginal which results in the large deviations. Analysing the MC simulation results show the variance contribution is distributed on numerous devices. Even though it was attempted to increase the matching and using ideal resistors for the bias resistor this problem could not be resolved.
The phase margin of the loop is in the range of 75°, indicating that the system is stable. In addition, the GBW is around 5.8 kHz. The settling time of the system after start-up was shown to be well below the required minimum of 500 µs with τ = 110 µs.
The bandgap reference circuit and the bipolar core designed in this work match the requirements of ultra-low power consumption for temperature sensors based on BJTs. Therefore, it is possible to use this work as starting point for usage in smart sensors for wireless sensor networks. However, since there are several aspects that are showing shortcomings, such as the gain deviation or the current spikes of the DEM, further work has to be put into this design to make it a reliable and promising ultra-low power analog front-end, that meets all requirements over all process corners and the entire temperature range.

Future Work

Due to the limited time of this work, several aspects could not be properly dealt with. Thus, a brief overview for possible future work is given here.
Most prominently, the problem of the DC loop-gain needs to be investigated and resolved to ensure proper functionality. To obtain proper temperature readings, it is necessary to mitigate the process spread in the BJTs by means of trimming to reduce the deviation of the base-emitter voltage to an acceptable level. The DEM needs to be properly implemented to mitigate large current spikes. This is also valid for the chopping, however, the dynamic effects of the chopping are less compared to the DEM. The circuit does not fulfil all requirements for all process corners over the entire temperature range, for example the current density ratio and the input offset voltage. A proper analysis of the noise with DEM should be conducted. The start-up circuit of the analog front-end should be replaced by a start-up circuit that draws almost zero current when the circuit is turned on.

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Appendices

Appendix A

Gain and Phase Margin

The following figures show the gain and the phase margin of the bias circuit for the nominal case at 27 °C and the two worst cases, SS at -55 °C and FS at -55 °C. The gain is depicted in red and the phase margin in blue.

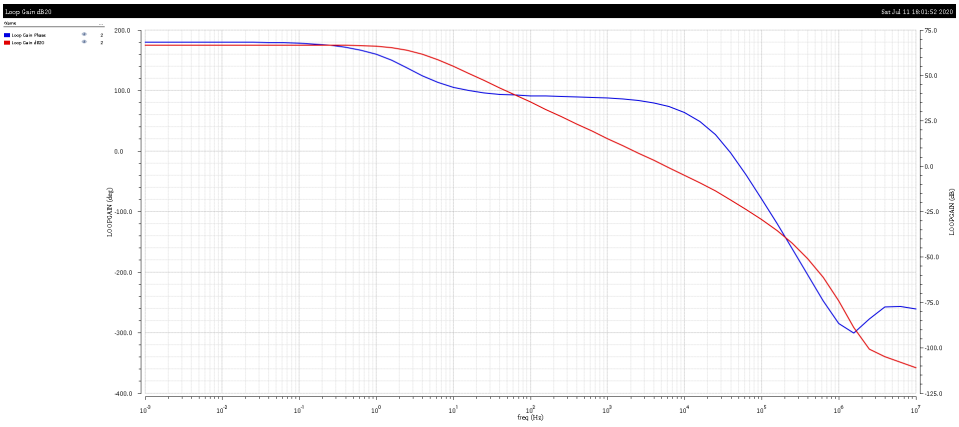


Figure A.1: Gain and phase margin for NN at 27 °C.

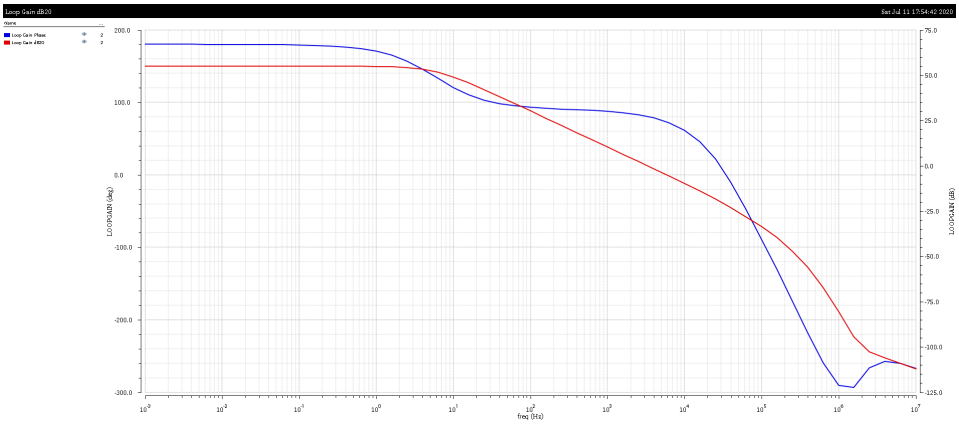


Figure A.2: Gain and phase margin for SS at -55 °C.

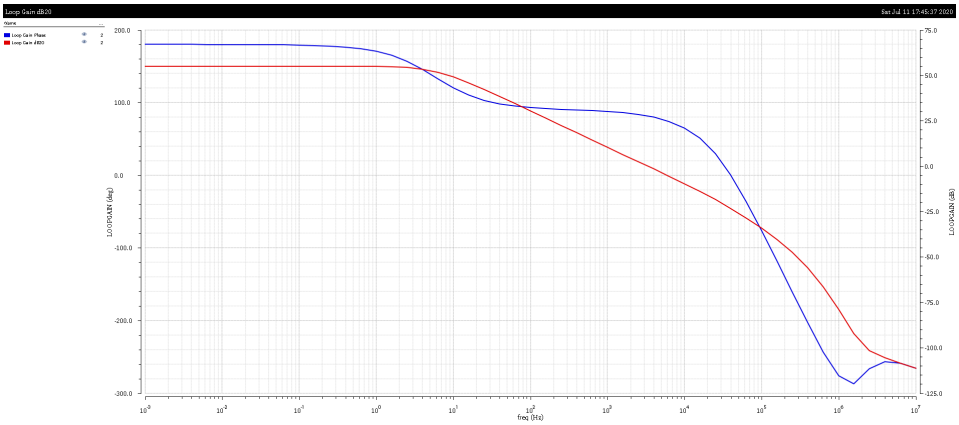


Figure A.3: Gain and phase margin for FS at -55 °C.

Appendix B

Circuit Schematics

The following pages contain all the schematics of the analog front-end. First, an overview of the entire analog front-end and the voltage sources for the testing are shown. Afterwards, each part is shown separately.

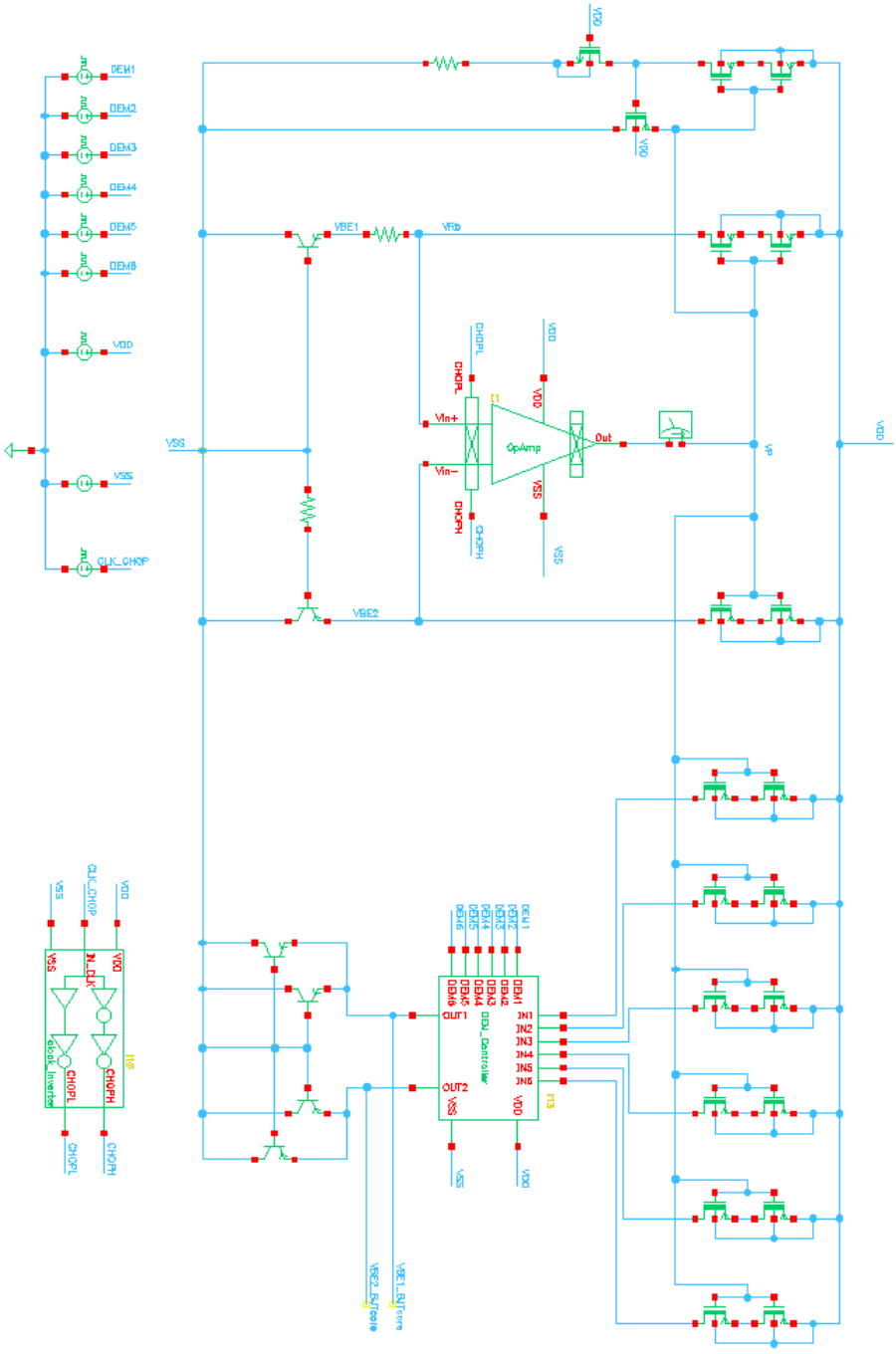


Figure B.1: Overview of the analog front-end schematic.

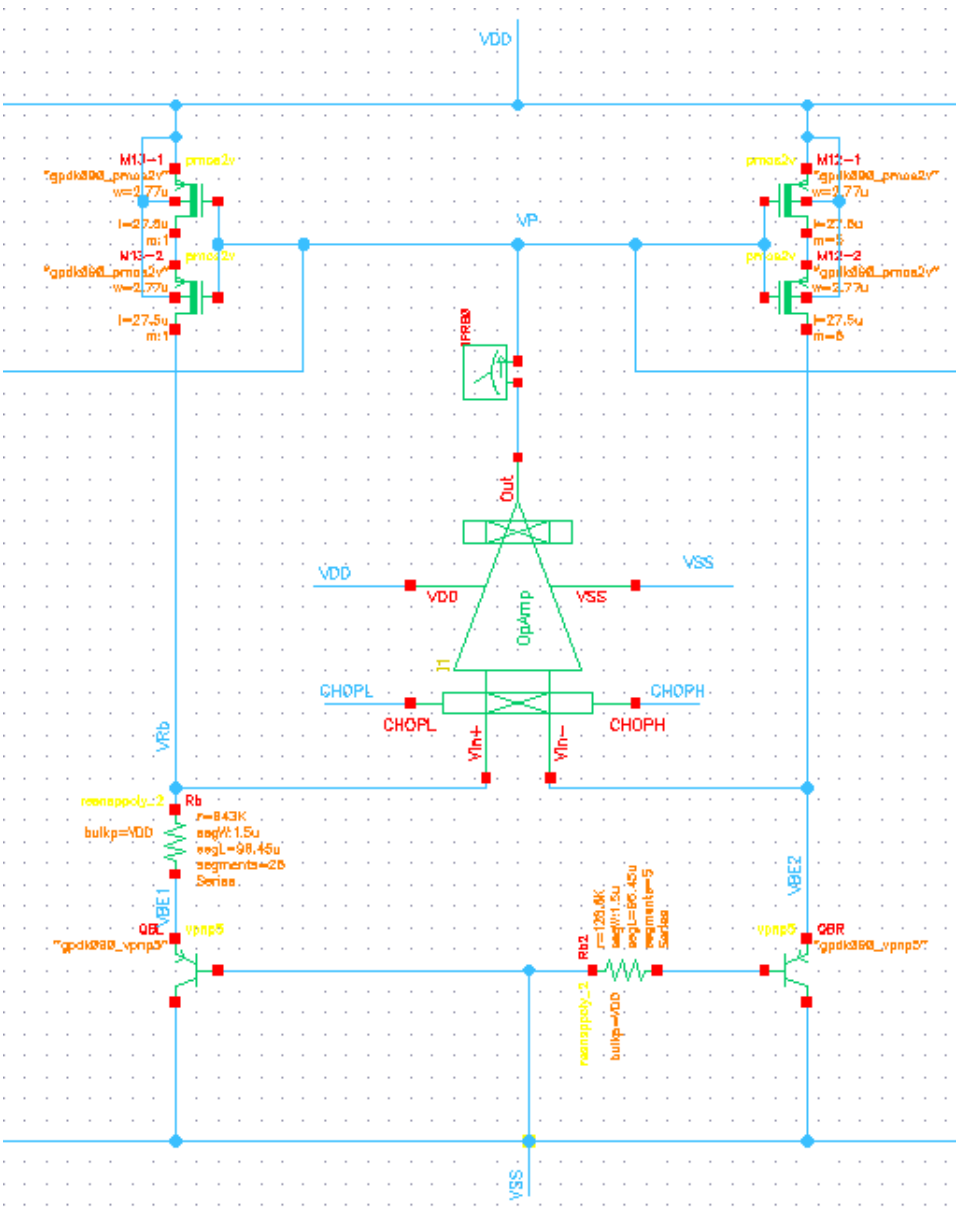


Figure B.2: Close-up of the bias circuit schematic.

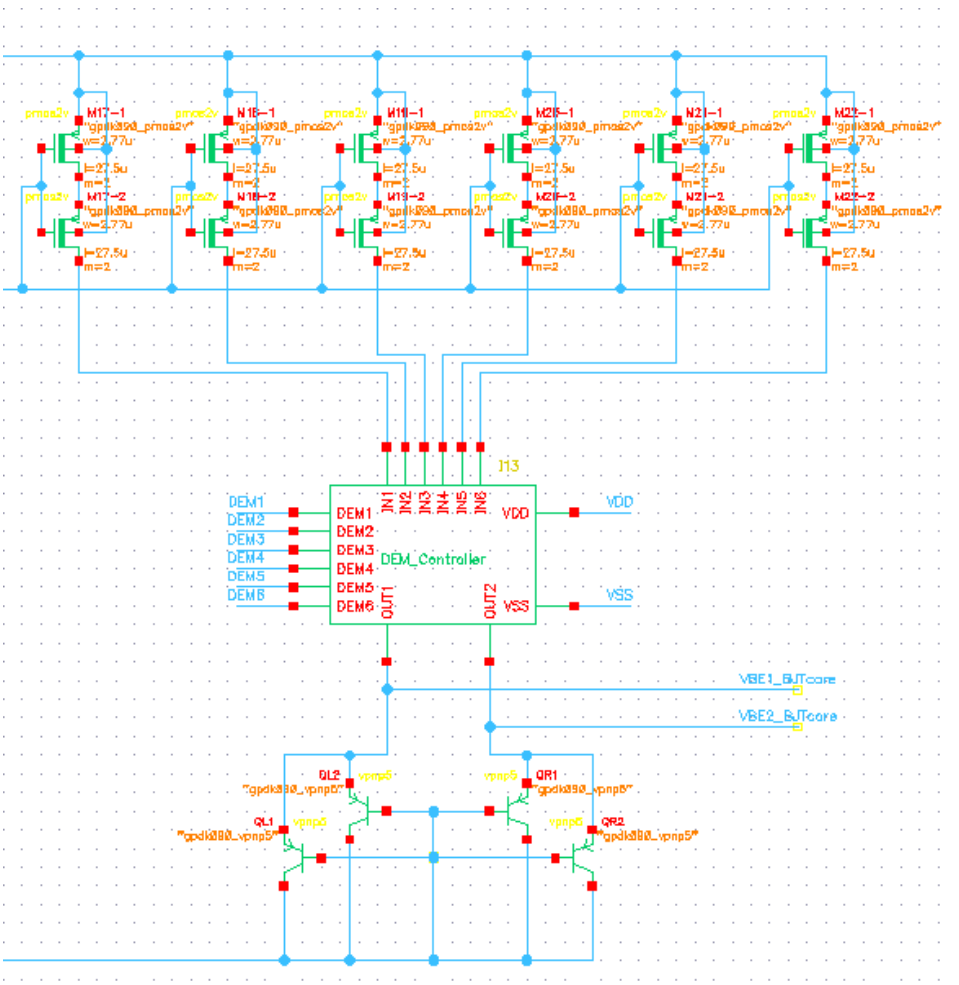


Figure B.3: Close-up of the bipolar core schematic.

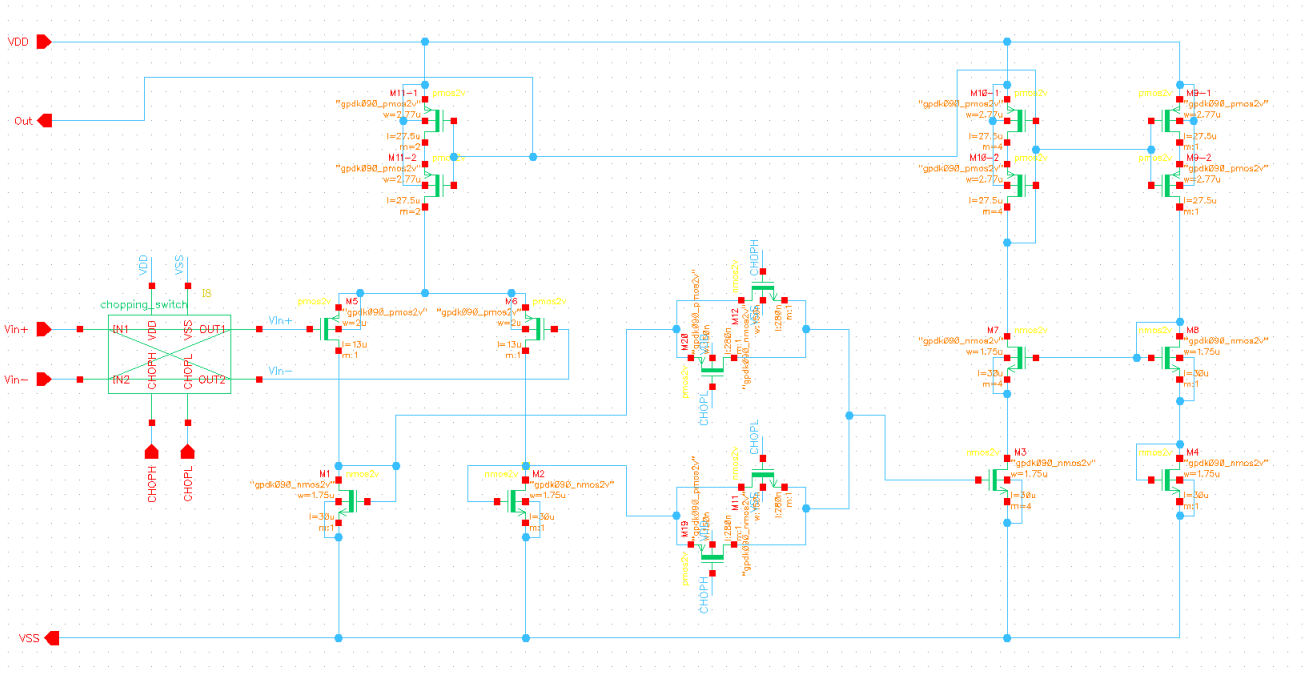


Figure B.4: Op amp schematic.

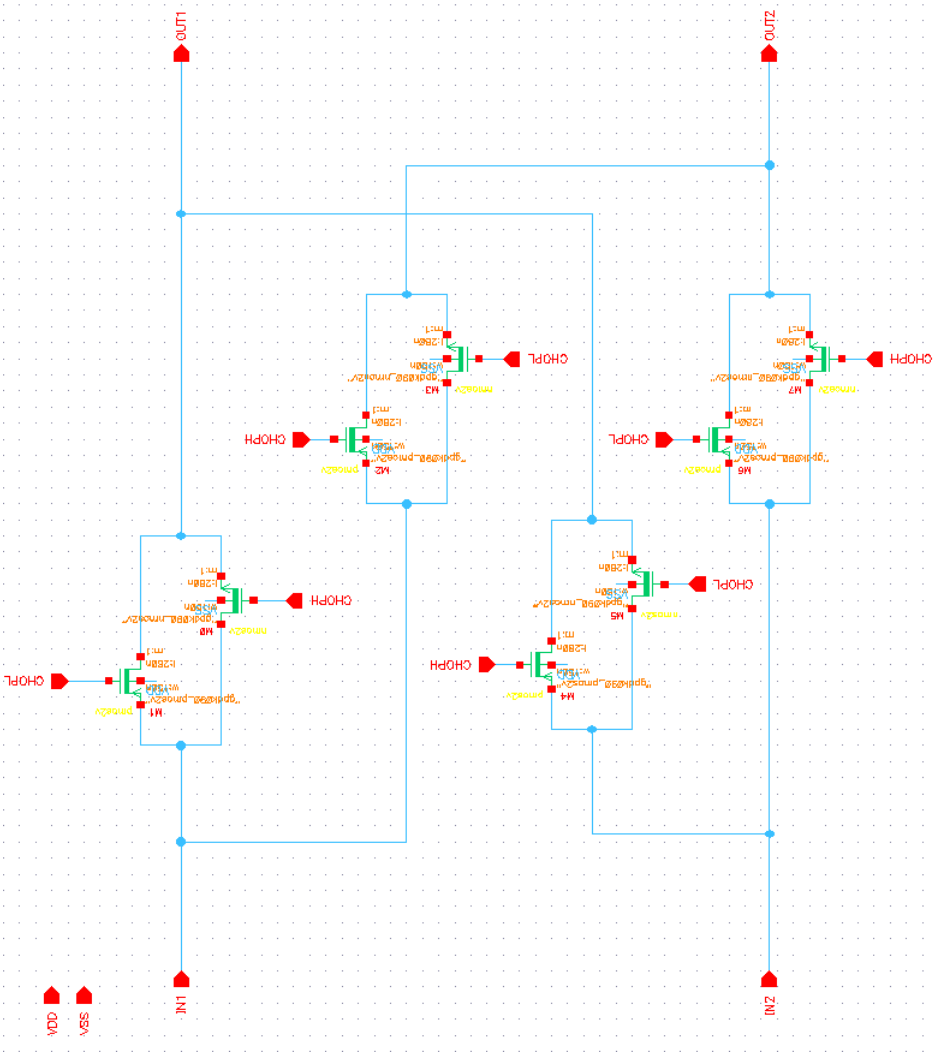


Figure B.5: Chopping switch schematic

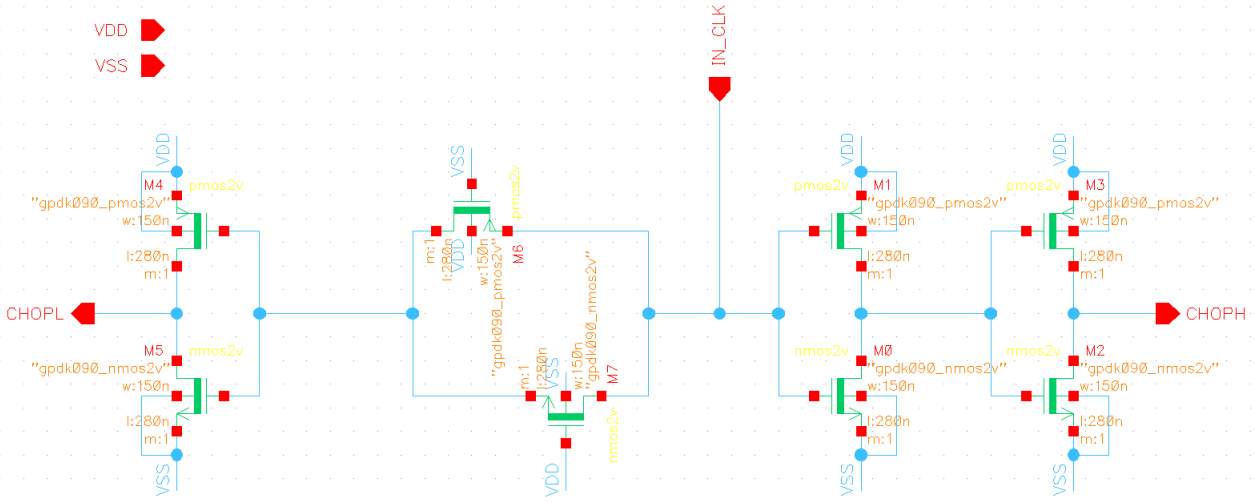


Figure B.6: Clock inverter schematic.

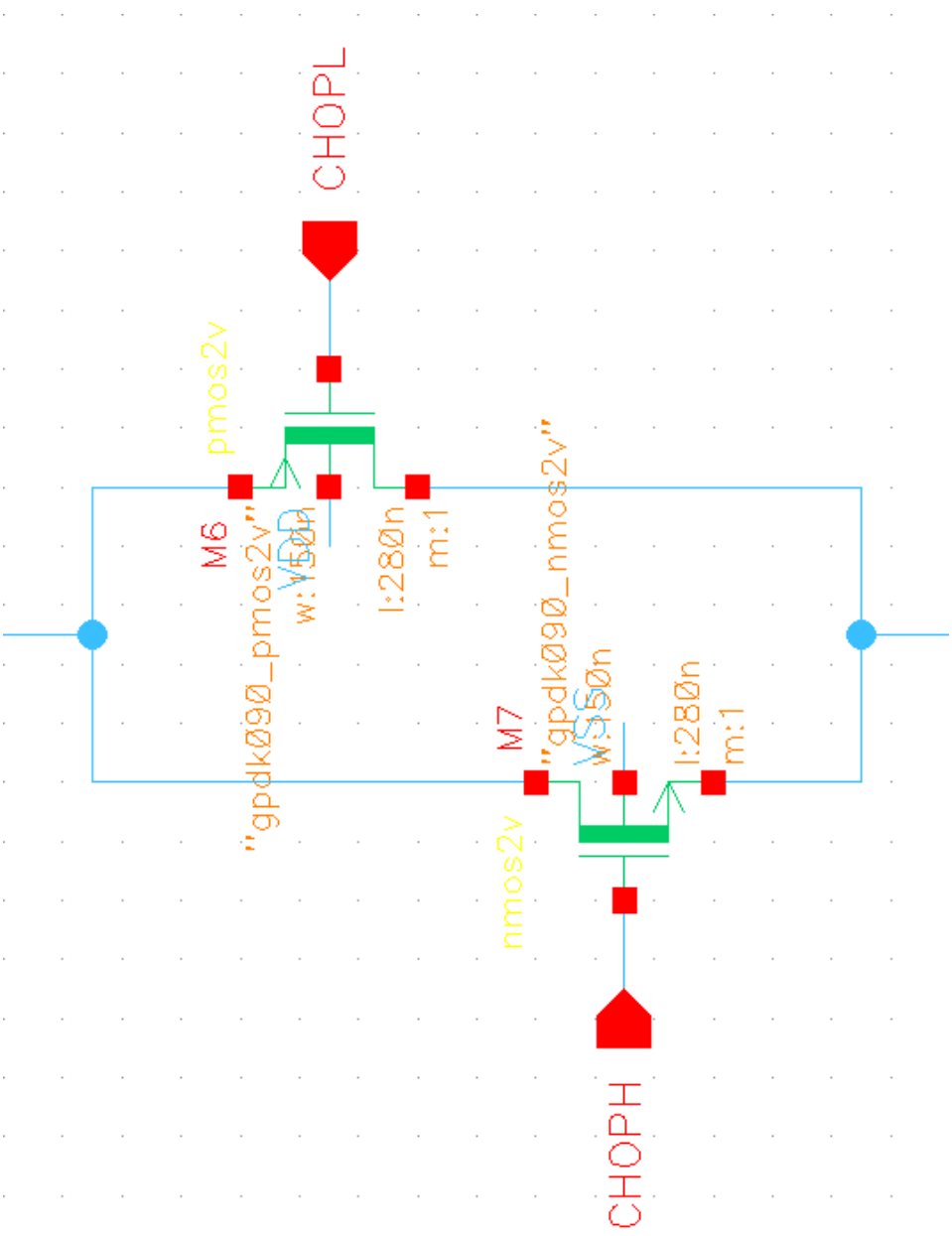


Figure B.7: Transmission gate schematic.

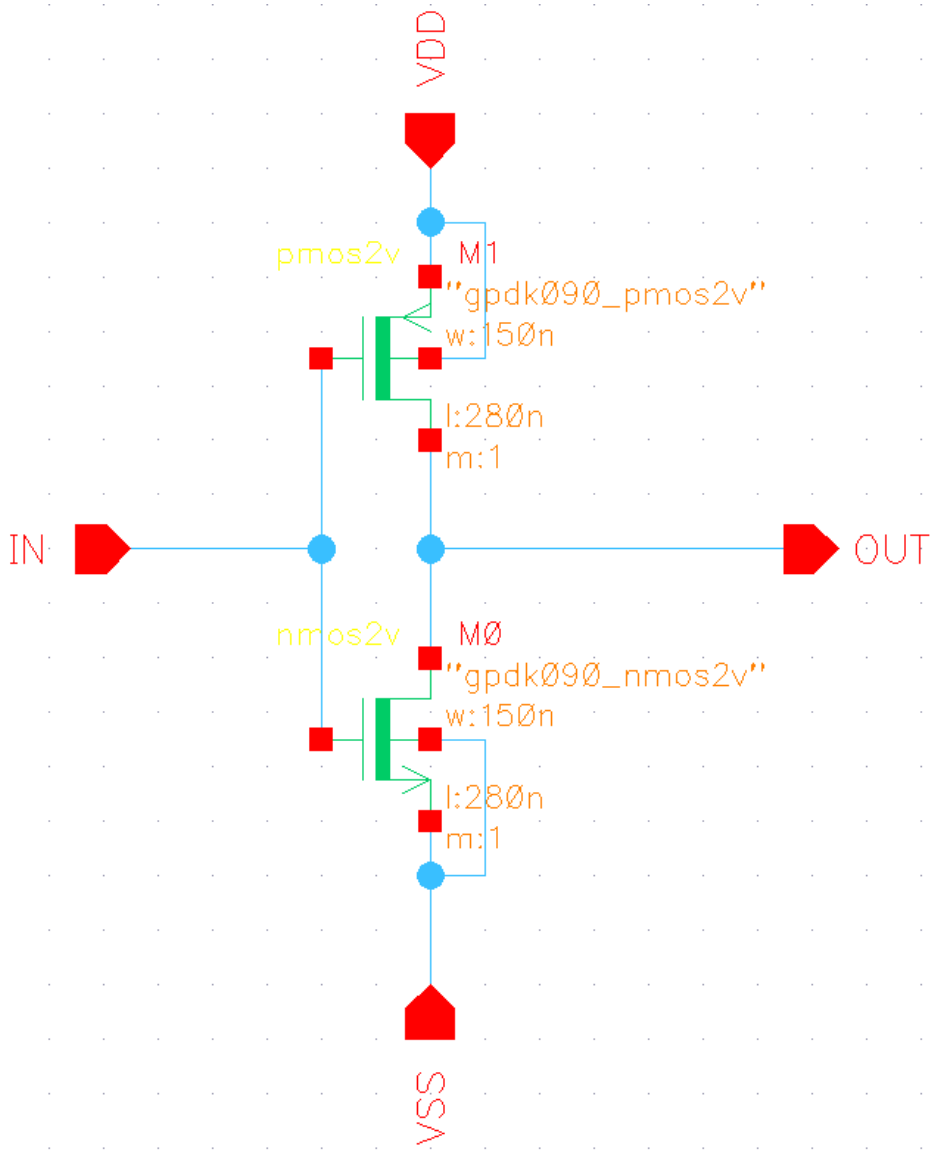


Figure B.8: Inverter schematic.

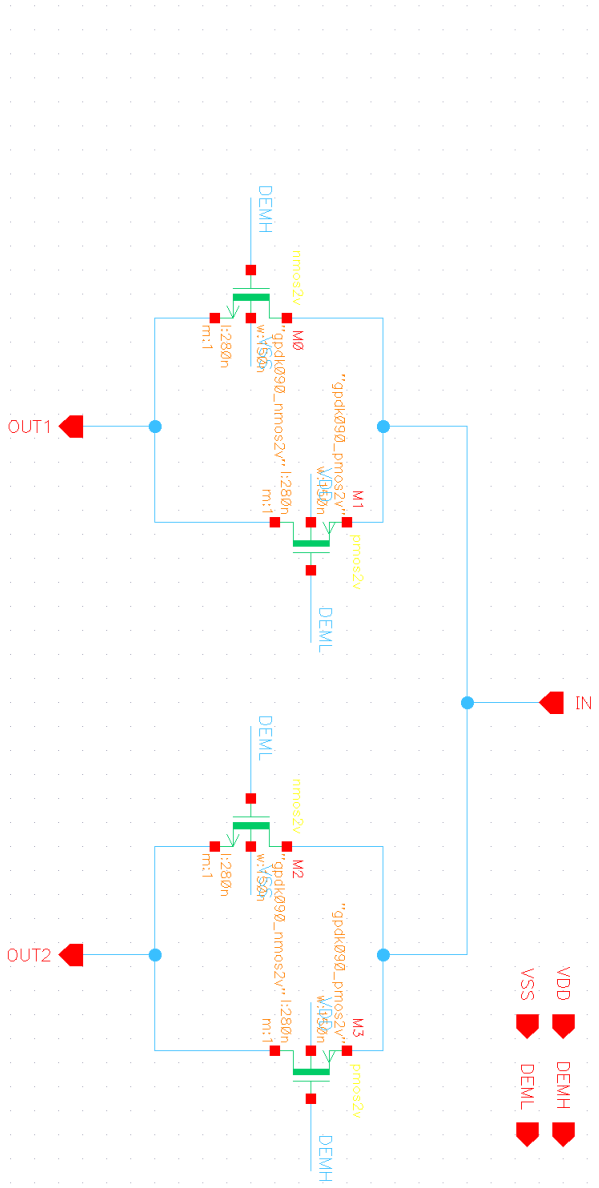
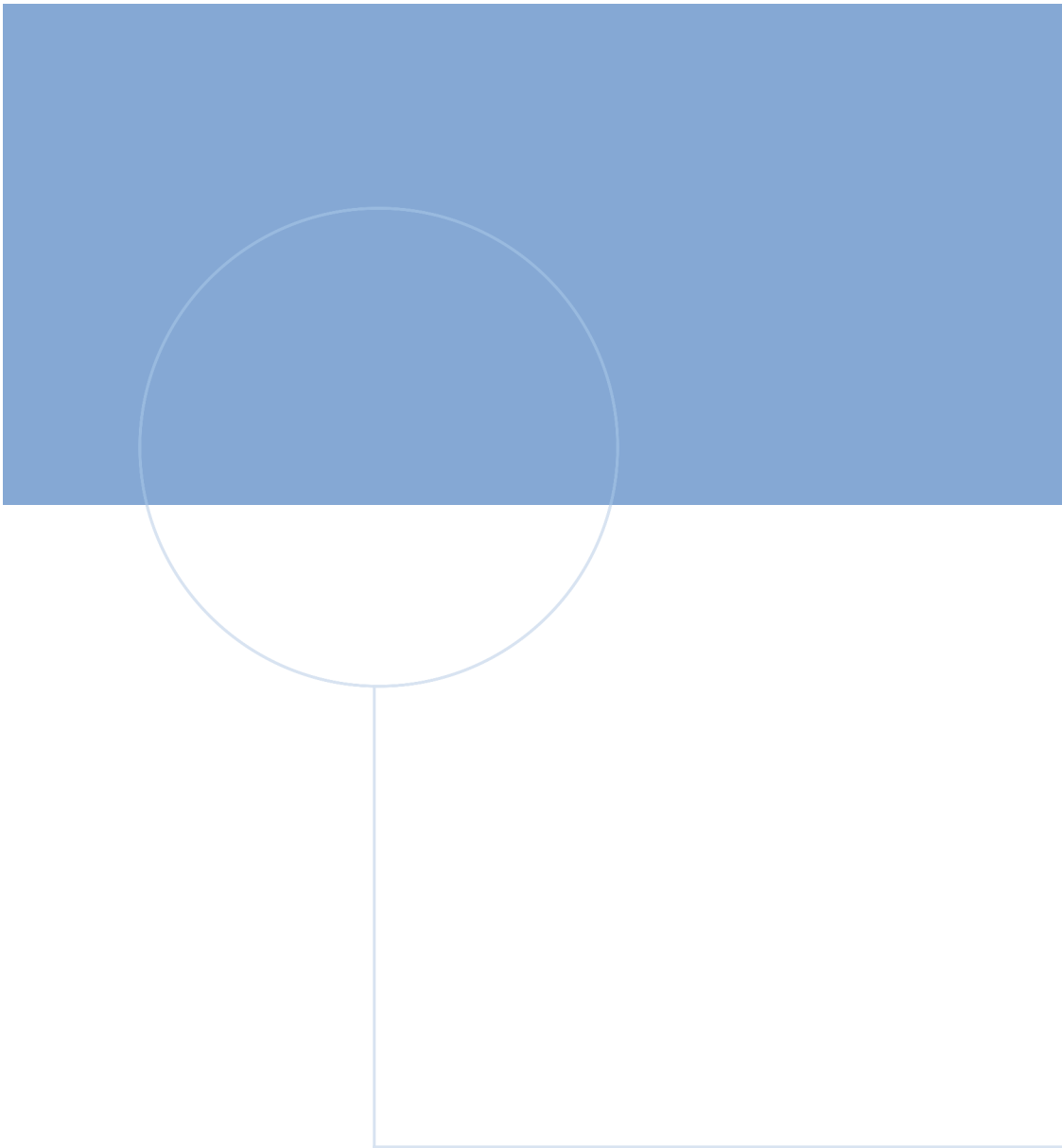


Figure B.9: DEM switch schematic.



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