Investigation of the Effect of Operating Conditions on Reliability of DC-link Capacitors in Microgrids

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***Abstract*—This paper considers a microgrid system where the impact of different non-ideal operating conditions on the reliability of the DC-link capacitor in three phase inverter systems is investigated. Rather than focusing on the lifetime of the capacitor, its failure rate is investigated and deemed a valuable indicator of the system's reliability. The thermal modeling of the capacitor is investigated as well is its importance in evaluating the failure rate of the capacitor. The study shows that unbalanced conditions has a particularly detrimental effect on the DC-link reliability. Nonlinear loads may have small effects as long as they do not adversely affect the power factor.**

I. Introduction

One of the main challenges of distribution grids is related to the significant amount of unbalanced and non-linear loads present in them [1]. The unbalanced and harmonically distorted currents drawn by these loads, lead to distorted voltages, particularly in the case of weak grids [2]. This might result in poor voltage quality, which can further lead to reduced lifetime of various system components, and in the worst case malfunction of loads connected in parallel with the system.

As a response to this issue, harmonic and unbalance compensation by distributed generators (DGs) have been deemed an attractive option for microgrids [2]. For DGs based on renewable energy sources, this is particularly attractive since these are rarely operated at full capacity. In recent years, several schemes for achieving power quality improvement using DGs have been proposed [2]–[7].

A common feature of many of the proposed schemes is to utilize resonant controllers and altered current and or voltage references for harmonic frequencies, in order to achieve the power quality improvement. Even though many of these schemes achieve the desired power quality improvement, the studies do not consider how the compensation affects the reliability of the underlying DG unit.

Reliability is the ability of an item to perform a required function under stated conditions for a stated period of time [8]. In terms of reliability, capacitors are among the most fragile components in power electronic systems [9]. In assessing the reliability of power electronic systems, it is thus important to include its effect on indicators used to assess reliability. DC-link capacitors are an integral part of power electronic systems and their failure will lead to failure of the power electronic system as a whole. In reliability studies, failure rate of a component can significantly affect the system-wide reliability [8], [10]. While some literature is available on evaluating the lifetime of DC-link capacitors depending on system conditions [11], [12], literature on evaluating their failure rate is scarce, especially under non-optimal operating conditions such as unbalances and harmonic distortion.

In this work, the capacitor's failure rate has been deemed an appropriate indicator to evaluate its effect on inverter and system reliability. The main contribution of this paper will thus be to develop a means of calculating the failure rate of the capacitor under unbalanced and non-linear conditions and evaluate the conditions impact on the failure rate of the capacitor. Electrolytic capacitors has been considered a bad choice due to its poor ripple current and lifetime characteristics. Only film capacitors will thus be considered even though the analysis can easily be extended to different kind of capacitors such as electrolytic capacitors. Although inverter control strategy is not the main focus of this paper, the inclusion of a proper harmonic compensation strategy was necessary to properly see the impact of the mentioned non-optimal operating conditions as well as to keep the grid voltage stable and clean. The results can thus also be interpreted as a trade-off for such control strategies.

The rest of this paper is organized as follows: Section II describes the study system and provides the details regarding the DG structure and control design. Section III explains the details of reliability of capacitors, while section IV analyses their thermal modelling. The results are provided in Section V, and these are further discussed in Section VI. Finally, Section VII concludes the paper.

II. System Description

In order to investigate the effect the harmonic compensation approach has on the reliability of the dc link capacitor, the system in Fig. 1 is used. The system represents a simplified lumped version of the CIGRE LV Benchmark System [13].

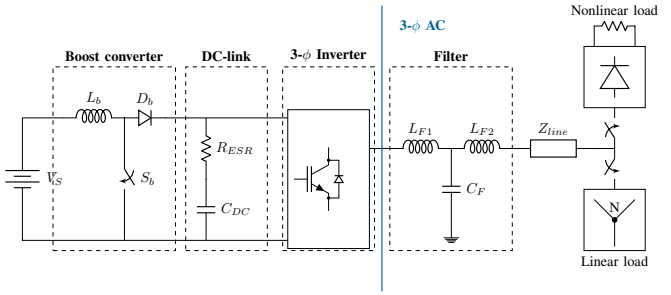

Fig. 1. Test system for considering the effect different loads have on the dc link capacitor of a grid-forming inverter.

Referring to the benchmark model, distributed generator (DG) 4 and loads 4 and 5 serve as the basis for the considered system. The DG is rated at $S_{max} = 25\,\text{kVA}$. It is modelled by an ideal voltage source feeding a boost converter, which provides the dc link voltage for a three-phase inverter. A boost converter is used to capture the dynamics of the DC-link more in detail compared to using a DC-link in parallel with a constant voltage source. At the same time, the boost converter is simple to model and is a representative DC/DC converter for interfacing PV sources. It can also represent the discharging mode of a half bridge bi-directional converter interfacing a battery energy storage.

A line impedance connects the DG unit and the load. The line impedance is modelled as being balanced in order to be able to more easily compare the balanced and unbalanced load cases. The R/X ratio of the line is set according to the benchmark model [13]. The nonlinear load considered is a 3-phase diode rectifier load.

A. Inverter Control

The DG is interfaced to the microgrid with a standard two-level, three phase inverter with an output LCL filter as shown in Fig. 1. The inverter is controlled in voltage control mode (VCM) using a hierarchical control structure, where the outermost loop is the conventional droop control which provides the voltage reference for the DG [14]. The voltage reference is tracked using a cascaded voltage and current control, where the outer loop controls the voltage across the capacitor C_F, and the inner loop controls the current flowing through L_{F1}. Both control loops were devised in the dq frame, and utilize PI controllers with appropriate decoupling terms [15].

The harmonic voltage reference is set to zero, in order to achieve a clean output voltage of the DG. To reduce the steady state error at negative sequence components and harmonic frequencies, the voltage controller contains a parallel resonance controller in addition to the mentioned PI controller. In particular, a resonance controller is applied for the negative sequence components, as well as the 5^{th}, 7^{th}, 11^{th} and 13^{th} harmonic components. In the dq frame, these components are shifted such that they end up at the 2^{nd}, 6^{th} and 12^{th} harmonics. The resulting voltage controller transfer function is thus given by:

$$C_v(s) = k_{pv} + \frac{k_{iv}}{s} + \sum_{h=2,6,12} \frac{2K_h\omega_c s}{s^2 + 2\omega_c s + (h\omega_1)^2}, \quad (1)$$

where k_{pv} and k_{pi} are the PI controller proportional and integral gains respectively, K_h is the resonance gain corresponding to the harmonic h, ω_c is the resonance controller width and ω_1 is the angular fundamental frequency.

B. Boost Converter Design and Control

A standard boost converter was utilized to regulate the dc link voltage. The boost converter passive elements were designed in order to guarantee continuous current mode in the inductor, as well as a ripple of the dc link voltage of less than 5%. The dc-link capacitor was chosen based on anticipated inverter RMS currents and capacitor current ripples [16]. Moreover, a commercially available device, Vishay MKP1848C DC-Link capacitor, was chosen [17].

TABLE I
SIMULATION PARAMETERS FOR THE SYSTEM UNDER STUDY

Name	Value	Description
Vs	500 V	Boost input voltage
V_{dc}	800 V	DC link voltage
V_{LL}	400 V	AC side line-line voltage
f_0	50 Hz	Nominal AC side frequency
$f_{sw,b}$	15 kHz	Boost switching frequency
$f_{sw,i}$	10 kHz	Inverter switching frequency
L_b	0.36765 mH	Boost inductor
R_{esr}	$3.5\,\text{m}\Omega$	Dc link capacitor resistance
C_{dc}	$100\,\mu\text{F}$	Dc link capacitance
L_{F1}	$500\,\mu\text{H}$	Inverter side LCL inductance
C_F	$50\,\mu\text{F}$	LCL capacitance
L_{F2}	$200\,\mu\text{H}$	Grid side LCL inductance
w_{z1}, w_{z2}	1.63k, 1.63k rad/s	Type three compensator zeros
w_{p1}, w_{p2}	2.85 M, 47.1k rad/s	Type three compensator poles
m	5e-5 rad/s/W	Droop controller active gain
n	1e-4 V/VAr	Droop controller reactive gain
T_f	0.1 s	Droop control low-pass filter
k_{pv}, k_{iv}	0.6702, 211 p.u.	Voltage PI controller gains
ω_c	1 rad/s	Resonance controller width
K_2, K_6, K_{12}	200, 200, 50 p.u.	Resonance controller gains
k_{pi}, k_{ii}	0.647, 1851 p.u.	Current PI controller gains

A single loop control scheme was utilized to directly control the output voltage. In order to achieve a reasonable phase margin and cross-over frequency, a type 3 compensator was utilized [18]. The control parameters were set to achieve a cross-over frequency of $1.56\,\text{kHz}$ and a phase margin of 45°. The crossover frequency was chosen in accordance with [19] to be reasonably above the LC resonance frequency, yet reasonably below the frequency of the right half plane zero of the boost converter.

A summary of the DG elements and main control parameters are given in Table I.

C. Case study configurations

The mentioned loads 4 and 5 are lumped and modelled as a single entity. Several different load scenarios are considered in order to determine the effect that both harmonic and unbalanced currents will have on the reliability of the dc link capacitor. A fair comparison between the different load cases is ensured by having the total apparent power and the power factor constant for all the considered cases. In particular, these are given by $S_{tot} = 22\,\text{kVA}$ and $pf = 0.85$, respectively.

An overview of the considered load cases is shown in Table II. Case 1 represents the case where the load is balanced, and serves as the base case for the study. Cases $2-4$ represent increasing amount of load unbalance, where case 2 represents a small unbalance, and Case 4 can be considered an extreme case. The case denoted "CIGRE" represents the load unbalance as it is in the benchmark model. Finally, cases $5-8$ represent an increasing penetration of non-linear loads. In these cases, the linear load is balanced, and adjusted through load flow calculations to achieve the desired apparent power and power factor given the non-linear load of the particular case.

TABLE II
DESCRIPTION OF THE CONSIDERED LOAD CASES

Case	Apparent power [kV A] for the phases abc	Non-linear load as percentage of active power
1	{7.33, 7.33, 7.33}	0
2	{8.25, 8.25, 5.5}	0
3	{5.5, 5.5, 11}	0
4	{1, 1, 22}	0
CIGRE	{4.8, 6.4, 10.8}	0
5	{7.33, 7.33, 7.33}	10
6	{7.33, 7.33, 7.33}	30
7	{7.33, 7.33, 7.33}	50
8	{7.33, 7.33, 7.33}	75

III. RELIABILITY OF FILM CAPACITORS

The reliability of a capacitor is reflected by its failure rate $\lambda(t)$. In time, given a set of operating conditions, it follows the characteristic "bathtub curve" illustrated in Fig. 2.

During the useful lifetime L of a component (usually given in hours at a specific rated voltage and temperature [20]), The failure rate is often simplified with a constant failure rate in time $\lambda(U,T)$.

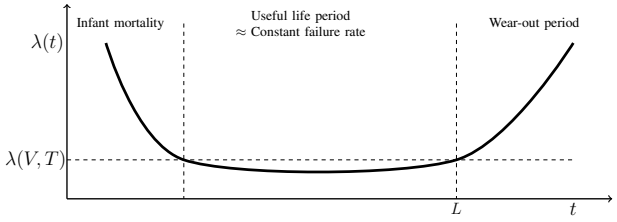

Fig. 2. Bathtub curve - Expected failure rate as a function of time.

Datasheets also states the failure rate given in failure in time (FIT) at half the rated voltage and $40°C$ [17]. This baseline failure rate will be denoted λ_0. In the general technical information sheets, voltage and temperature dependency of the failure rate is also found as multipliers for the different film capacitor types [20]. For Vishay MKP capacitors the failure rate multiplier, denoted as M, can be seen in Fig. 3. The real failure rate is thus given by $\lambda(V,T) = \lambda_0 M$.

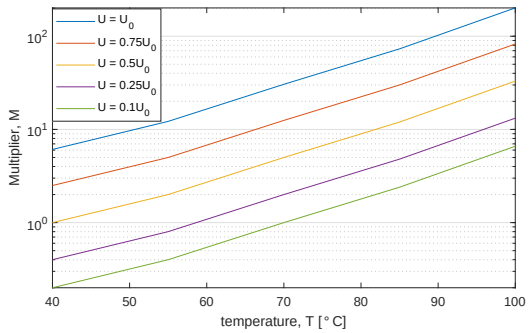

Fig. 3. Failure rate multiplier M as a function of temperature and voltage.

IV. THERMAL MODELING

The impedance and the equivalent series resistance (ESR) of film capacitors are frequency dependent [21]. Although RMS values for the capacitor current as well as a constant ESR have been used in literature, such usage yields inaccurate results [22].

Using Fourier analysis on the current through the capacitor, a frequency dependent power loss model can be constructed where the power loss in the capacitor is given by [23]:

$$P_{\mathrm{C,\,loss}} = \sum_{\mathrm{h}=1}^{N} I_{\mathrm{ch}}^2 R_{\mathrm{ESR}}(f_{\mathrm{h}}) \tag{2}$$

The thermal behaviour of the capacitor can be illustrated by a thermal network from the capacitor hot-spot to the ambient surroundings as seen in Fig. 4. The thermal resistance from hot-spot to case and from the case to the ambient surroundings is given by R_{hc}^{th} and R_{ca}^{th}, respectively. The thermal capacitance of hot-spot and the case is given by C_h^{th} and C_c^{th}, respectively [23]. T_a is the ambient temperature and P is the power loss of the capacitor.

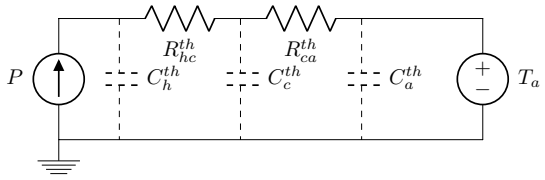

Fig. 4. Schematic diagram of the capacitor thermal circuit.

Transient thermal behaviour of a film capacitor mainly decides the time it takes for the capacitor to reach steady state temperature for a certain operating condition and will not be of importance to this study. When transient characteristics are not of interest, the steady state temperature can be given by the thermal circuit in Fig. 4 by neglecting the dashed parts. In this case, the steady state temperature of the capacitor hot-spot is given by:

$$T_h = T_a + (R_{hc}^{th} + R_{ca}^{th})P \tag{3}$$

Since the capacitor acts like an inductor beyond its resonance frequency, a fair assumption is that currents of frequencies higher than these will not pass through the capacitor and can thus be neglected in the calculation of power losses.

From the measurements seen in Fig. 5, the Assumption that the capacitance is constant will be a valid approximation for frequencies lower than the capacitor's resonance frequency. The current through the capacitor is thus given by:

$$I_C = \frac{U_C}{Z_C} = \frac{U_C}{R_{ESR} + \frac{1}{j\omega C}} \approx \frac{U_C}{\frac{1}{j\omega C}} \quad \Big| \Big(\frac{1}{j\omega C} \gg R_{ESR} \Big) \tag{4}$$

The effect of a frequency dependent ESR on the current will thus be considered negligible since the impedance will be dominated by the capacitance. This also becomes clear when measuring the frequency characteristics of the chosen capacitor as seen in Fig. 5.

A computationally effective, yet accurate way of calculating the steady state temperature of the capacitor would thus be as follows:

1) Simulate the system to obtain steady state current waveforms through the capacitor using a constant R_{ESR} given by the datasheet.
2) Analyse the current by means of fast Fourier transform (FFT) to obtain the frequency-magnitude spectrum of the capacitor current.
3) Calculate the power loss by means of 2.

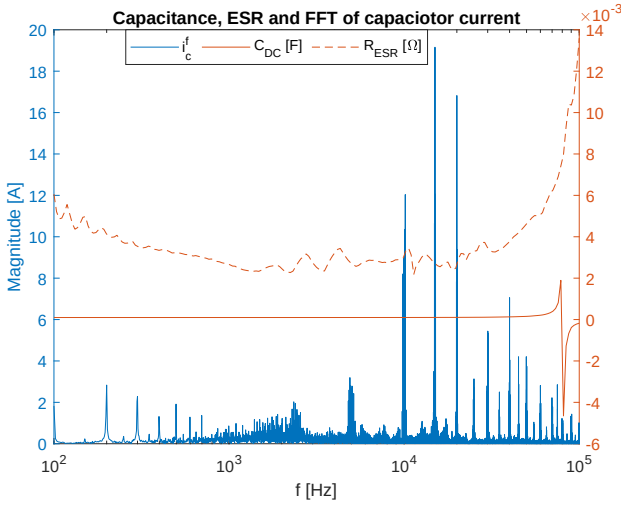

Fig. 5. i_c^f is the magnitude of the current through the capacitor at different frequencies obtained through FFT analysis of Case CIGRE in steady state. C_{DC} and R_{ESR} are the capacitance and resistance of the Vishay MKP1848C DC-Link capacitor [17] measured with an E4990A Impedance Analyzer.

V. Results

The different cases described in Section II were modelled in Simulink. Fig. 6 shows one cycle of the three phase currents i_a, i_b and i_c for all the cases. The apparent, active and reactive powers consumed by the load, S_{load}, P_{load} and Q_{load}, are also shown for 0.5 s of each case during the steady state operation. Also shown is the representation of real and reactive power losses in the line impedance S_{line}.

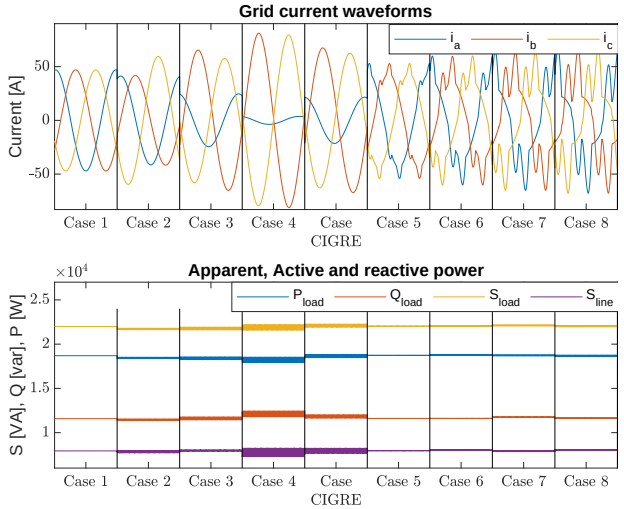

Fig. 6. Stable grid current characteristics for all phases and consumed active, reactive and apparent powers for load and line.

As described in Section II, a close to constant apparent power of 22 kVA and power factor of 0.85 is achieved.

In Fig. 7, the current through the capacitor i_C is seen for all cases for 0.5 s of steady state operation together with its calculated RMS current I_C^{RMS}. The power dissipated in the capacitor and the resulting temperature increase are presented for both ways of modeling the capacitor ESR discussed in Section IV.

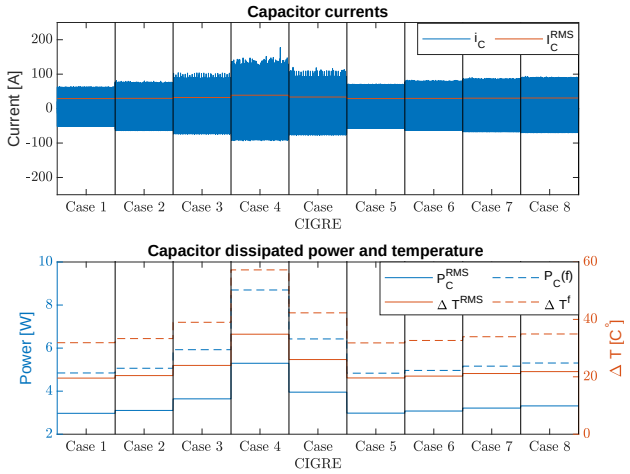

Fig. 7. Current and RMS current through the capacitor as well as dissipated power and temperature change in the capacitor.

P_C^{RMS} and ΔT^{RMS} represent the power loss and the resulting temperature increase resulting from a constant ESR modeling. P_C^f and ΔT^f use a frequency dependent ESR model according to equations (2) and (3) as well as the ESR frequency characteristics seen in Fig. 5. Using the temperature increase ΔT^{RMS} and ΔT^f and a DC-link voltage of 800 V, the failure rate multiplier $M(U,T)$ can be found by interpolation of the characteristics shown in Fig. 3. Together with the baseline failure rate λ_0 from the datasheet [17], failure rates for all cases for different ambient temperatures are found and shown in table III. λ^f uses a frequency dependent ESR while λ uses a constant ESR.

In table III, it can generally be seen that the the failure rate is very dependent on the operating conditions as well as the ambient temperature. Furthermore, it can be seen that the thermal modeling also plays an important role in accurately capturing the failure rate characteristics.

TABLE III
Failure rates of cases at different ambient temperatures.

Case	$T_a = 25°C$		$T_a = 37°C$		$T_a = 50°C$	
	λ^f	λ	λ^f	λ	λ^f	λ
1	0.089	0.042	0.172	0.074	0.368	0.158
2	0.0982	0.044	0.1949	0.080	0.399	0.167
3	0.137	0.052	0.285	0.103	0.667	0.221
4	0.385	0.096	0.922	0.189	rating breach	0.384
CIGRE	0.159	0.056	0.337	0.116	0.823	0.251
5	0.089	0.042	0.172	0.075	0.367	0.1647
6	0.094	0.044	0.184	0.079	0.380	0.165
7	0.102	0.045	0.204	0.085	0.425	0.178
8	0.109	0.047	0.219	0.089	0.471	0.188

VI. Discussion

From the presented results, it is obvious that non-optimal operating conditions have a large impact on the temperature and consequently the failure rate of the capacitor. Particularly the unbalanced cases have a significant impact on the failure rate of the capacitor.

In spite of the power factor being kept constant through all cases, a trend of increasing temperature and failure rates for the non-linear load cases is seen. The temperature increase could thus be a result of the distorted current waveforms alone and not a result of increased RMS grid current caused by a poor power factor in the non-linear load.

It is evident that unbalanced loads may play a significant role in lowering the reliability in DC-link capacitors. The same is true for the ambient temperature. Comparing the reference balanced case at an ambient temperature of $25°C$ and the CIGRE case at an ambient temperature of $37°C$, the failure rates are 0.089 and 0.337, respectively.

The modelling of the ESR is also a very important consideration. From table III, the frequency dependent ESR estimates much higher failure rates, which suggests that the frequency characteristics of the ESR should be modelled in reliability considerations of the capacitor.

The DC-DC converter topology used, as well as the switching frequency and strategy will affect the current through the capacitor. Although this study considers a boost converter, the shown trends are expected regardless of chosen topology and switching scheme. The magnitudes of these trends is however likely to differ depending on converter scheme.

The whole electric power system is a series connection of subsystems with their own characteristic failure rates. The increase in the failure rate of the capacitor will thus be reflected in the equivalent failure rate of the inverter. This could again have a detrimental effect on the reliability of the distribution system (in this case the microgrid) itself. These result will however need to be validated through experimental long term stress tests of the capacitor.

VII. Conclusion

This paper has considered the reliability of the dc-link capacitor of DGs in microgrids with different degrees of harmonic pollution and imbalance of loads. It has been found that the failure rate of the dc-link capacitors in DG units may play a vital role in the overall reliability of microgrid systems. This failure rate is heavily dependent on system operating conditions such as harmonic pollution or unbalanced loads. In modeling these conditions, the method used to evaluate the thermal characteristics of the capacitor is of great importance.

In three phase inverter systems, it has been pointed out that unbalanced conditions in particular has a detrimental effect on the reliability of the dc-link capacitor. Nonlinear loads may have small effects if they do not adversely affect the power factor.

The results and reasoning provided herein can be applicable to other types of capacitors and operating conditions as well. In such cases, modification of parameters and additional features (such as including the effect of ripple current degradation in electrolytic capacitors) should be appropriately modelled where applicable.

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