A Very Low SEF Neural Amplifier by Utilizing a High Swing Current-Reuse Amplifier

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***Abstract*—Although current-reuse amplifier has been widely used in biomedical applications because of their low input-referred thermal noise, they don't have high output swing and their gain is limited. In this article, a rail-to-rail current-reuse amplifier with a 92 dB open-loop gain is introduced while its power and noise increment is just 7%. The proposed structure is a two stage amplifier which doesn't need further compensation since all nodes are diode connected except for the output node. In order to show the merit of the proposed structure, the NEF, PEF and SEF of the proposed amplifier in a capacitively-coupled neural amplifier structure is compared to the state-of-the-art neural amplifiers. The amplifier is designed and simulated in a commercially available 0.18 µm CMOS technology. The midband gain of the neural amplifier is 40 dB in the bandwidth between 0.6 Hz and 5 kHz. The proposed structure consumes 1.07 µA current from a 1.2 V supply voltage. The NEF, PEF and SEF of proposed structure are 1.68, 3.4, 0.05, respectively. The total area consumption of the neural amplifier is 0.03 mm^2 without pads.**

***Index Terms*—High-swing amplifier, low SEF, current-reuse OTA, high gain, dynamic range**

I. Introduction

Although there have been many excellent works aimed at reducing power and noise in the past, their swing is too limited [1], [2]. That's why, they usually propose to use a second stage in order to boost the output swing [1]. The second stage is required not only to increase the output swing, but also it's required to boost the open-loop gain in order to minimize the gain error in close-loop application with high close-loop gain or instrumentation amplifiers [3].

There is a fundamental trade-off between power, noise, gain, area and swing of a system. Typically, the front-end amplifier defines the overall noise of a a sensor read-out system. Thus, a large proportion of power should be consumed in the first stage only to keep the noise below a certain target. Battery usually takes up a large area for biomedical implant applications to generate required power, in which area is one of the most stringent parameters. Besides, heat dissipation is another concern about the power consumption of implantable applications [4].

The trade-off between different factors shows the amplifier efficiency. Noise efficiency factor (NEF) was defined to correlate noise, bandwidth and current consumption of an amplifier firstly in [5]. In [3], power efficiency factor (PEF) was proposed to add the supply voltage to the NEF equation. Although NEF and PEF are widely used to show the merit of an amplifier, their output swing and the gain were another point which are not mentioned in NEF and PEF. Finally, the system efficieny factor (SEF) in [2] was proposed to combine PEF with output dynamic range which added the gain of the amplifier and output swing. Dynamic range, NEF, PEF and SEF can be calculated as below.

$$DR_{out} = 10\log\frac{V_{amp,max}^2}{2.G_{AFE}^2.V_{ni,rms}^2} \tag{1}$$

$$NEF = V_{ni,rms}\sqrt{\frac{2I_{tot}}{\pi U_T 4kTBW}} \tag{2}$$

$$PEF = NEF^2.V_{DD} \tag{3}$$

$$SEF = PEF/DR_{out} \tag{4}$$

where $V_{ni,rms}$ is the total equivalent input-referred noise in the amplifier's bandwidth, k is the Boltzmann constant, T is temperature in Kelvin, BW is the amplifier's -3 dB bandwidth, U_T refers to the thermal voltage, I_{tot} is the total current drawn from the power supply V_{DD}, $V_{amp,max}$ is the maximum swing at the amplifier output and G_{AFE} is the amplifier voltage gain.

To minimize the thermal noise of an amplifier, the classical way is to bias input transistors in weak inversion or even deep subthreshold region which lead to maximize g_m/I_D [6]. Besides, current-reuse structure which was first introduced in [7], has been widely used in biomedical application [8]–[10]. Although their NEF is theoretically 1.4 times better than conventional amplifiers since it double the overall g_m of an amplifier, their system efficiency factor is not much better.

In this article, first, a high swing current-reuse amplifier (HSCR) with low SEF is introduced. Although current-reuse suffer from low open-loop gain, the proposed structure can easily achieve higher gain which leads to less gain error in close-loop application. Second, to make the proposed structure suitable for a neural amplifier and compare its performance

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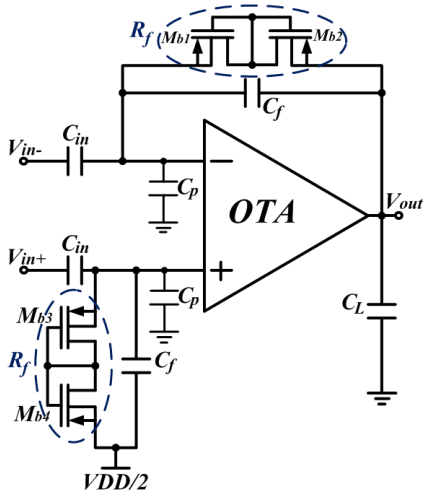

Fig. 1. The capacitively-coupled neural amplifier

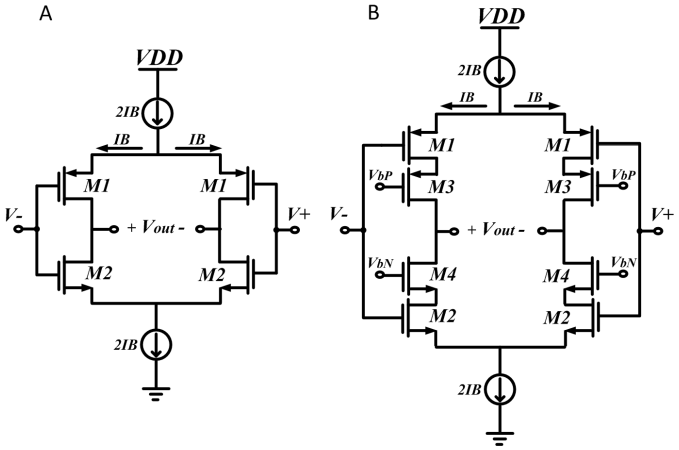

Fig. 2. A) a current-reuse amplifier B) a cascode current-reuse amplifier

with the state-of-the-art neural amplifiers, the amplifier is designed and simulated in an conventional structure as it's depicted in figure 1.

II. Current-reuse amplifier limitations

The structure of a simple current-reuse amplifier and cascode current-reuse amplifier are depicted in Fig. 2. If we assume the NMOS and PMOS transistors have same transconductance and output impedance, the total input-referred thermal noise and the gain of a simple current-reuse amplifier can be calculated as Eq. 5 and 6, respectively.

$$v_{ni}^2 = \frac{16}{3}\frac{kT}{g_{m1}+g_{m2}} = \frac{8}{3}\frac{kT}{g_{m1}} \tag{5}$$

$$A = (g_{m1}+g_{m2})(r_{o1} \parallel r_{o2}) = g_{m1}r_{o1} \tag{6}$$

In order to minimze the noise, input transistors should be biased in weack inversion or subthreshold region. According to EKV model which is valid for all regions, the estimated value of input transconductance of an amplifier is Eq. 7 [11]. Also,

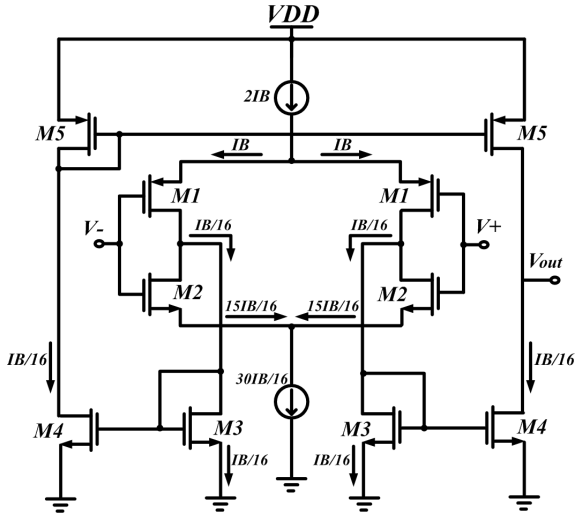

Fig. 3. The proposed high swing current reuse amplifier

the output impedance of a single transistor can be calculated accordin to Eq 8.

$$g_m = \frac{\kappa I_D}{U_T}\frac{2}{1+\sqrt{1+4IC}} \tag{7}$$

$$r_o = \frac{1}{\lambda I_D} \tag{8}$$

where κ is the subthreshold gate coupling coefficient, λ is channel-length modulation coefficient and IC is inversion coefficient. The IC is less than 0.1 when it operates in weack inversion or subtheshold region. Thus, the Eq. 6 will be modified as below.

$$A = \frac{\kappa I_{1,2}}{U_T}\cdot\frac{2}{1+\sqrt{1+4IC}}\cdot\frac{1}{\lambda I_{1,2}} \tag{9}$$

$$A = \frac{2\kappa}{\lambda U_T(1+\sqrt{1+4IC})} \tag{10}$$

According to Eq. 10, the gain of the amplifier will be limited by technology restriction since all parameters in this equation are technology dependent parameters and the circuit designer doesn't have much control on them. This should be mentioned, although the λ of a transistor varies also by the channel-length of a transistor, it is still limited to a specific value according to technology. Therefore, cascoding output transistor as it's depicted in Fig. 2 is required to boost the gain.

The problem of current-reuse amplifier is their limited output swing and their limited open-loop gain. Although this gain can be increased by cascoding transistor or other techniques, the total output swing peak-to-peak will be limited to $6V_{ds,sat}$ below V_{DD}.

III. Proposed HSCR Amplifier

The proposed HSCR amplifier is shown in Fig. 3. The proposed structure has not only low input-referred noise, but also it has high swing and the gain is flexible and tunable. The

TABLE I
THE DIMENSION AND OPERATING POINTS OF TRANSISTORS

Device	W/L (μm/ μm)	Operational region	g_m/I_d	I_d
M_1	100/3.5	Subthreshold	25	500 nA
M_2	80/6	Subthreshold	25	465 nA
M_3	0.5/20	Strong inversion	13	35 nA
M_4	0.5/20	Strong inversion	13	35 nA
M_5	1/20	Strong inversion	13	35 nA

gain of proposed HSCR amplifer can be approximated to Eq. 11.

$$A = (g_{m1} + g_{m2})(r_{o4} \parallel r_{o5}) \tag{11}$$

$$r_{o4,5} = \frac{1}{\lambda I_{out}} \quad \text{and} \quad I_{out} = I_{D1} - I_{D2} \tag{12}$$

Assume g_{m1} and g_{m2} are approximately equal (it acceptable as long as I_{out} is much smaller than I_{D1} and I_{D2}) and output impedance of M_4 and M_5 are equal. Then Eq. 11 and 12 can be simplified to 13. Accordingly, the gain of the proposed HSCR amplifier is theoretically I_{D1}/I_{out} times higher than current-reuse amplfiers. Noteworthy, the I_{D1}/I_{out} ratio cannot be increased dramatically. For very high ratio I_{D1}/I_{out}, Eq. 11 is not valid. In this design, the ratio of 1/16 has been chosen to prove at least 24 dB gain boosting.

$$A = g_{m1} r_{o4} = \frac{2\kappa}{\lambda U_T (1 + \sqrt{1 + 4IC})} \frac{I_{D1}}{I_{out}} \tag{13}$$

The noise of the proposed high swing current reuse amplifier is according to Eq. 16. Although this noise has three terms more than the noise of a current reuse which was mentioned in Eq. 5, these terms are negligible since $I_{3,4,5}$ are much smaller than $I_{1,2}$. Besides, input transistors are biased in subthreshold region whereas the rest are biased in strong inversion region. Therefore, the noise of the amplifier is expected to be approximately equal to current reuse amplifier.

$$v_{ni}^2 = \frac{16}{3} \frac{kT}{g_{in}} (1 + \frac{g_{m3}}{g_{in}} + \frac{g_{m4}}{g_{in}} + \frac{g_{m5}}{g_{in}}) \tag{14}$$

$$g_{in} = g_{m1} + g_{m2} \tag{15}$$

$$v_{ni}^2 = \frac{8}{3} \frac{kT}{g_{m1}} (1 + \frac{g_{m3}}{2g_{m1}} + \frac{g_{m4}}{2g_{m1}} + \frac{g_{m5}}{2g_{m1}}) \tag{16}$$

Finally, the output swing of the proposed HSCR amplifier is rail-to-rail. More accurately, the output swing is according to Eq.17. The transistor's dimension of proposed HSCR amplifier is reported in table I. The W and L of input transistors are chosen to be large enough to minimize the flicker noise.

$$V_{ds,sat} < V_{out} < V_{DD} - V_{ds,sat} \tag{17}$$

In order to have a better comparison, conventional current reuse amplifier, cascode current-reuse amplifier and HSCR amplifier, with same W and L, are designed and compared together in table II. It is noteworthy that a 1.2 V supply voltage is chosen for all circuits. Finally, to have a better comparison between their swing, $V_{ds,sat}$ is assumed 100 mV. The gain of the amplifier is better than it's expected in the equation.

TABLE II
PERFORMANCE COMPARISON OF THE AMPLIFIERS

Parameter	Current-reuse	Cascode Current-reuse	HSCR
Current (μA)	1	1	1.070
Gain (dB)	54	84	92
Noise (nV/ $\sqrt{\text{Hz}}$)	27	27	28
Swing (V)	0.8	0.6	1

Although the noise, power and swing are matched to the equations, the gain is better than it was expected. This is due to the higher V_{ds} on output transistors of HSCR amplifier in comparison with conventional current-reuse amplifier. The power and noise consumption are negligibly higher whereas output swing is much better for HSCR amplifier.

IV. SIMULATION RESULTS

The HSCR amplifier is used as a core amplifier in a capacitively-coupled neural amplifier structure as it was depicted in Fig. 1. The neural amplifier is designed and simulated in a commercially available 0.18 μm CMOS technology. Besides, the layout of the proposed structure is shown in Fig. 4. The ratio between C_{in} and C_f is set on 100. In order to consume less area and to achieve a good Monte Carlo simulation result, the value of C_{in} and C_f are chosen 10 pF and 100fF, respectively. In addition, to control the lower cut-off frequency, a high value resistor is required since C_f is 100 fF. Therefore, a pseudo-resistor is implemented. The input referred-noise of the neural amplifier is according to Eq. 18. The total input-referred noise in the bandwidth is 3 μV_{rms} in its bandwidth (0.6 Hz - 5 kHz). The noise and gain of the amplifier is shown in Fig. 5. The total Power consumption is 1.3 μW. In order to show the robustness of the amplifier, Monte Carlo simulation for process and mismatch variation is carried out for 400 runs. The CMRR according to the simulation is depicted in Fig. 6. Since the proposed amplifier has more than 90 dB gain, the mean value of the close-loop gain is 39.93 dB with just 0.016 dB standard deviation. The total harmonic distortion is -40 dB for 10 mV_{pp} input (1 V_{pp} output). At the end, the proposed neural amplifier with HSCR amplifier is compared to the state-of-the-art amplifiers in table III. Since the neural signals amplitudes can reach up to 5 mV and the gain of the amplifier determines the ADC's resolution, the comparison has been done between amplifiers which can amplify input signals up to 5 mV and have at least 40 dB gain. This should be regarded that the SR (slew rate) of proposed amplifier is 11 mV/μs with a 5-pF capacitive load.

$$v_{ni,amp}^2 = (\frac{C_{in} + C_f + C_p}{C_{in}})^2 v_{ni}^2 \tag{18}$$

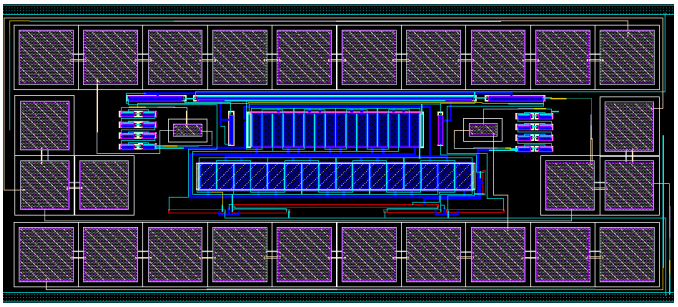

Fig. 4. The layout of the proposed neural amplifier (260 µm× 114 µm)

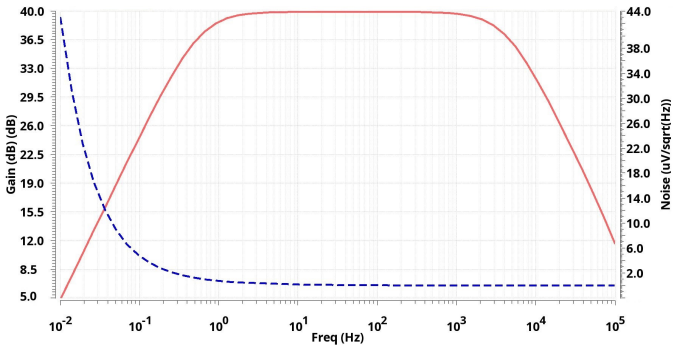

Fig. 5. The gain and noise of the proposed amplifier

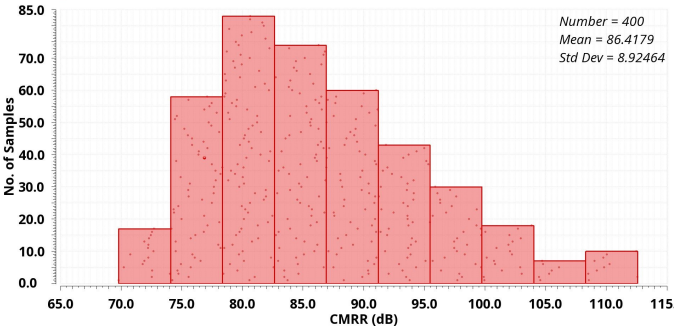

Fig. 6. The CMRR of the proposed neural amplifier for 400 runs

TABLE III
PERFORMANCE SUMMARY AND COMPARISON

Specs	[12]	[13]	[14]	[15]	This Work
Technology (nm)	500	600	180	180	180
Supply Voltage (V)	2.8	2.8	1.8	1.8	1.2
Power (µW)	7.56	2.4	1.5	4.07	1.28
Gain (dB)	40.85	39.4	40.17	39.75	39.93
Bandwidth (Hz)	45-5.32 k	0.36-1.3 k	8 m-1.68 k	0.3-4.4 k	0.6-5 k
Max. Signal (V_{pp}) @ THD 1%	7.3 m (input)	10 m (input)	5.9 m (input)	14.86 m (input) 1.38 (output)	10 m (input) 1 (output)
IR Noise (μV_{rms})	3.06	3.07	2.99	3.19	3
NEF	2.67	3.09	2.6	2.78	1.68
PEF	20	26.7	12.16	13.91	3.4
SEF	0.34	0.44	0.21	0.22	0.05
CMRR (dB)	66	66	70	76	>70
PSRR (dB)	75	70	-	77.6	>80
Area (mm^2)	0.16	0.13	-	0.058	0.03
Sim./Meas.	Meas.	Meas.	Sim.	Sim.	Sim.

V. Conclusion

The proposed structure is an improved version of current-reuse amplifier which has a rail-to-rail output swing. In addition, the gain of current-reuse amplifiers are limited and technology dependent that doesn't give flexibility to achieve higher than 80 dB gain with simple current reuse amplifier. With the proposed high swing current-reuse amplifier, 40 dB higher gain is easily achievable with higher swing and relatively same power and noise. This leads to the design of a low NEF and PEF capacitively-coupled neural amplifier with very low SEF.

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