A Power Efficient, High Gain and High Input Impedance Capacitively-coupled Neural Amplifier

Erwin H. T. Shad[1], Tania Moeinfard[2], Marta Molinas[3], Trond Ytterdal[4]

***Abstract*—In this article, a capacitively-coupled neural amplifier based on a new high gain low-noise amplifier is proposed. By utilizing a cross-coupled structure, the open-loop gain of the amplifier is boosted. This modification leads to higher closed-loop gain of the amplifier only with one-stage and reduces the gain error. Besides, the input impedance of the amplifier is boosted by a factor of 100 at 100 Hz using a power-efficient technique. A detail analysis to model the high frequency behaviour of input impedance boosting technique is carried out to show and formulate a limitation. The amplifier is designed and simulated in a commercially available 0.18 µm CMOS technology. The Bandwidth of the amplifier is from 0.5 to 10 kHz and the midband gain is 52 dB. The total input-referred noise is 3.26 μV_{rms} in the bandwidth. The noise and power efficiency factor of proposed amplifier is 1.4 and 1.7 , respectively. The superior performance of the amplifier is achieved by increasing the input capacitor value and exploiting noise efficient amplifier. Furthermore, to show the robustness of the proposed structure, a Monte Carlo simulation is carried out for process variation and mismatch. The mean value of the input impedance and CMRR are 10.5 GΩ and 90 dB, respectively. Finally, the total area consumption without pads is 0.03 mm^2.**

***Index Terms*—High input impedance, input impedance analysis, neural amplifier, low-power amplifier, low-noise amplifier**

I. Introduction

Neural amplifiers have widely been used in many applications such as brain computer interfaces (BCIs) and medical equipment [1], [2]. There are different parameters needed to be considered when designing a neural amplifier. For instance, input impedance of amplifiers plays a significant role in minimizing the signal attenuation [3]. The high gain of the amplifier relaxes the ADC requirements. Besides, power consumption and input-referred noise is another critical parameter in designing these applications as well as common-mode rejection ratio (CMRR) [4].

The cross-coupled effects on CMRR and gain are reported in [5]. Although the proposed technique boosted the CMRR of the amplifier, the final amplifier could not be designed with very low current because of the mismatch effect on cross-coupled pairs. Besides, half of the input transistors current is drawn by cross-coupled transistors which degrade the noise efficiency of the amplifier.

In order to minimize the close-loop gain error, the high open-loop gain is a requirement [6]. Current reuse is a conventional structure in biomedical application because of its low input-referred noise. However, its open-loop gain is limited as it is described in [7]. The open-loop gain is boosted in [8] but the output swing is very limited. This problem is alleviated in [7] by modifying the current reuse structure but its open-loop gain remains limited as it will be discussed.

Capacitively coupled neural amplifiers have widely been used because of their DC offset blocking and power efficiency [9]. However, their input-referred noise might be affected by input parasitic capacitor. The neural signals bandwidth is up to 10 kHz. Usually flicker noise is dominant in low frequency amplifiers. Flicker noise depends on transistor dimensions. In order to minimize the flicker noise, W and L of input transistors should be much larger than typical values. This leads to larger input parasitic capacitors which will increase the total input-referred noise. Besides, the input capacitor cannot be increased since it defines the input impedance.

In [10], they utilized positive feedback to boost the input impedance. Since the structure was based on single ended amplifiers, they were forced to use a buffer in the feedback loop to invert the signal and boost the input impedance. Another technique for differential amplifiers is proposed in [11] which requires a buffer in the feed-forward path. All these techniques come with additional power consumption. In [12], they proposed a power and area efficient technique to boost the input impedance for chopper amplifiers which is only effective for low frequencies.

In this article, a noise and area-efficient capacitively-coupled amplifier is proposed. Besides, by utilizing the properties of negative impedance generated by cross-coupled transistors, the open-loop gain of the main amplifier which was proposed in [7] is boosted. Furthermore, a detailed analysis on input impedance is carried out to model the high frequency behaviour of input impedance boosting technique. The other poles and zeros in the boosted input impedance are calculated as well, according to those equations. The noise efficiency is improved by increasing input capacitor and input transistors dimensions while the input impedance is kept sufficiently high by input impedance boosting technique.

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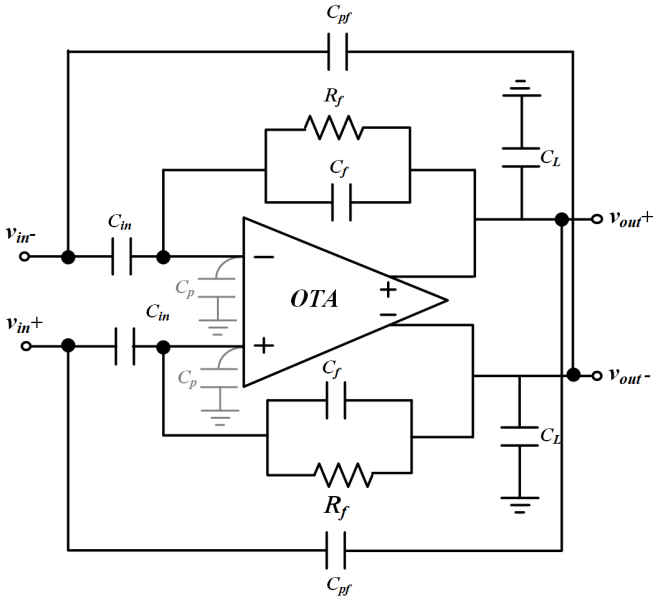

Fig. 1. A fully differential capacitively coupled neural amplifier with an input impedance boosting loop

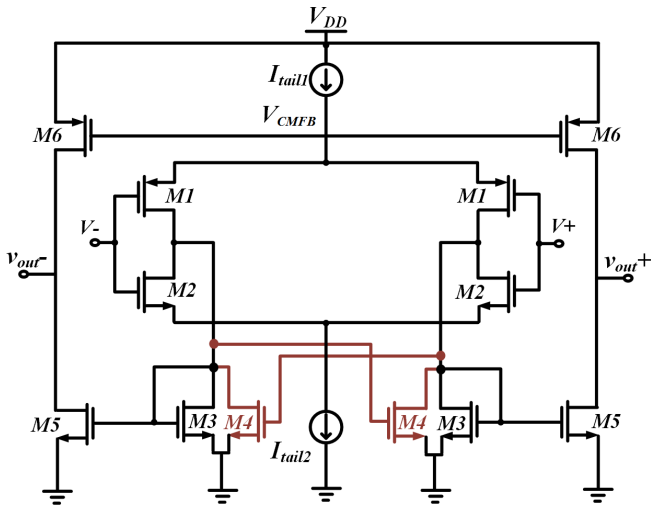

Fig. 2. Proposed high-gain low-noise amplifier by utilizing cross-coupled structure

II. System Overview

A fully differential capacitively-coupled amplifier for neural recording is depicted in the Fig. 1 where C_p is modeled as the parasitic capacitors of the input transistors. The total input-referred noise can be calculated according to Eq. 1, where v_{ni} is the input-referred noise of the main amplifier. C_f and R_f define the lower cut-off frequency. To achieve 0.5 Hz lower cut-off frequency, R_f is implemented by pseudo resistors. The midband gain of the close-loop neural amplifier is according to Eq. 2.

$$v_{ni,amp}^2 = (\frac{C_{in}+C_f+C_p}{C_{in}})^2 v_{ni}^2 \tag{1}$$

$$A_{CL} = \frac{C_{in}}{C_f} \tag{2}$$

III. Proposed Low-Noise and High Gain Amplifier

A. Noise Analysis

The proposed amplifier and its common-mode feedback are depicted in Fig. 2 and Fig. 3, respectively. The input-referred noise of the proposed amplifier can be calculated as Eq. 5. As far as the g_m of the input transistors is much larger than the other transistors, the total input-referred noise can be simplified to Eg. 6.

$$v_{ni}^2 = \frac{16}{3}\frac{kT}{g_{in}}(1+\frac{g_{m3}}{g_{in}}+\frac{g_{m4}}{g_{in}}+\frac{g_{m5}}{g_{in}}+\frac{g_{m6}}{g_{in}}) \tag{3}$$

$$g_{in} = g_{m1}+g_{m2} \tag{4}$$

$$v_{ni}^2 = \frac{8}{3}\frac{kT}{g_{m1}}(1+\frac{g_{m3}}{2g_{m1}}+\frac{g_{m4}}{2g_{m1}}+\frac{g_{m5}}{2g_{m1}}+\frac{g_{m6}}{2g_1}) \tag{5}$$

$$v_{ni}^2 \approx \frac{8}{3}\frac{kT}{g_{m1}} \tag{6}$$

B. Gain Analysis

Without M4, by decreasing the current of M3, M5 and M6 the gain increases as long as $1/g_{m3}$ is smaller than $r_{o1,2}$. But at specific point, it becomes comparable and the gain will be limited when the current consumption is limited. By adding M4, the output impedance at the drain of $M_{1,2}$ is according to Eq. 7. In order to minimize the noise, the current is mostly going through M1 and M2. Therefore, the output impedance of M1 and M2 is much lower than M3 and M4. By considering the same current for M3 and M4, Eq. 7 can be simplified as Eq. 8 and the gain will be as Eq. 9.

$$R_{D1,2} = (r_{o1} \parallel r_{o2} \parallel r_{o3} \parallel r_{o4} \parallel \frac{1}{g_{m3}} \parallel \frac{-1}{g_{m4}}) \tag{7}$$

$$R_{D1,2} \approx (r_{o1} \parallel r_{o2}) \tag{8}$$

$$A = (g_{m1}+g_{m2})R_{D1,2} \times g_{m5}(r_{o5} \parallel r_{o6}) \tag{9}$$

As long as the most of the current goes through M1 and M2 and they remain in subthreshold region, their g_m will be approximately equal. Therefore, the total open-loop gain can be approximated to Eq. 10.

$$A \approx g_{m1}g_{m5}r_{o1}r_{o5} \tag{10}$$

It is noteworthy that since the current in the output branch is much smaller than the rest, the output impedance is much larger than the other nodes. In addition, the largest capacitor is at the output node. Therefore, the output pole is dominant and the amplifier can be considered as a single-pole amplifier. The transistors dimensions and some other parameters are reported in table I.

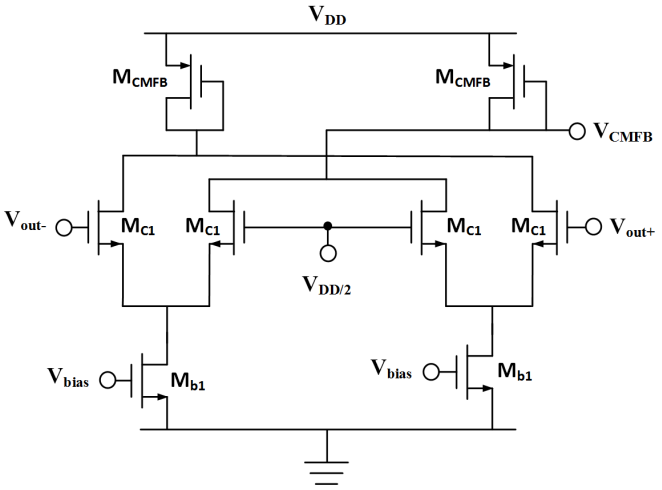

Fig. 3. The common-mode feedback used to set output voltage

TABLE I
THE DIMENSION AND OPERATING POINTS OF TRANSISTORS

Device	W/L (μm/ μm)	Operational region	g_m/I_d	I_d
M_1	150/3	Subthreshold	26	500 nA
M_2	120/9	Subthreshold	26	450 nA
M_3	0.5/20	Strong inversion	15	25 nA
M_4	0.5/20	Strong inversion	15	25 nA
M_5	3(0.5/20)	Strong inversion	15	75 nA
M_6	3(1/20)	Strong inversion	15	75 nA

IV. Input impedance boosting

In order to boost the input impedance, the area and power efficient positive feedback loop is used [12]. In order to calculate the input impedance, the structure in Fig. 4 is used. Usually the input nodes of amplifiers are considered to be virtual ground. Therefore, the input impedance will be according to the Eq. 11.

$$\frac{v_t}{i_t} = \frac{1}{sC_{in}} \frac{1 + sR_fC_f}{1 + s(R_fC_f - R_fC_{pf})} \tag{11}$$

$$\frac{v_t}{i_t} = \frac{1 + sR_fC_f}{sC_{in}} \tag{12}$$

This equation shows that the input impedance is inversely proportional to the input capacitor for frequencies less than $1/2\pi R_fC_f$. By considering the C_{pf} equal to C_f, a constant input impedance value is expected for frequencies higher than $1/2\pi R_fC_f$ as it's calculated in Eq. 12.

However, in reality input impedance starts to drop from a specific frequency. This fact cannot be extracted from the mentioned equations. In order to find the exact frequency where the input impedance start decreasing, the transfer function of the main amplifier should be considered. The open-loop gain of the amplifier is considered to have only one pole as it is shown in Eq. 13 and $Z_f(s)$ is the model of parallel resistor and capacitor in feedback loop. Therefore, it will be calculated as in Eq. 14.

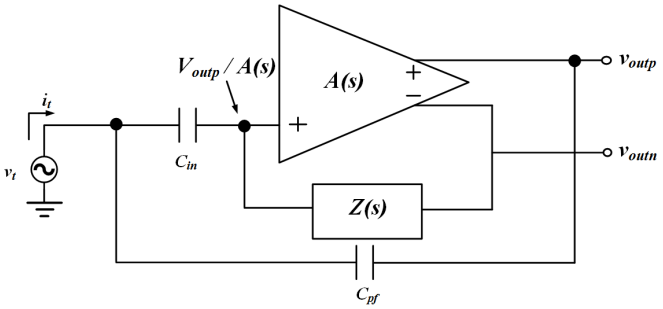

Fig. 4. Half circuit analysis for calculating input impedance

$$A(s) = \frac{A_0}{1 + \frac{s}{\omega_L}} \quad \text{and} \quad \omega_L = \frac{1}{R_LC_L} \tag{13}$$

$$Z_f(s) = R_f \parallel \frac{1}{sC_f} = \frac{R_f}{1 + sC_fR_f} \tag{14}$$

By two KCLs at the input node of the amplifier and at the input node of the test voltage source, Eq. 15 and 16 can be derived. Therefore, Eq. 17 can be derived by solving the last two equations. By adding the values of $Z_f(s)$ and A(s), and considering the open-loop gain much higher than 1 and C_{pf} equal to C_f, the input impedance can be approximated to Eq. 18.

$$(\frac{v_{outp}}{A(s)} - v_t)sC_{in} + \frac{\frac{v_{outp}}{A(s)} - v_{outn}}{Z_f} = 0 \tag{15}$$

$$(v_t - \frac{v_{outp}}{A(s)})sC_{in} + (v_t - v_{outp})sC_{pf} = i_t \tag{16}$$

$$Z_{in} = \frac{v_t}{i_t} \approx \frac{1}{sC_{in}} \frac{1 + A(s) + sC_{in}Z_f}{1 + A(s)(1 - sC_{pf}Z_f)} \tag{17}$$

$$Z_{in} \approx \frac{1}{sC_{in}} \frac{1 + sR_fC_f + s^2R_LC_LR_fC_f\frac{A_{CL}}{A_0}}{1 + s\frac{R_LC_L + R_fC_f}{A_0} + s^2\frac{R_LC_LR_fC_f}{A_0}} \tag{18}$$

In order to calculate the poles of the equation above, it is first assumed that the they are far from each other. The same situation is assumed for zeros. Zeros and poles are extracted and they are according to Eq. 19-23. The calculated poles and zeros shows that the first assumption was correct. ω_{z2} is at the higher cut-off frequency and as long as the open-loop gain is high ω_{p2} is out of interested bandwidth.

The Input impedance before and after boosting is depicted in Fig. 5. It is also shown in decibel in order to make it easier to see the boosting and cut-off frequency in boosted impedance. As it's shown, the input impedance is boosted in the whole bandwidth but the boosting factor decreases. The effect of higher cut-off frequency of amplifier is obvious in the input impedance. Therefore, the boosting factor in our simulation at 10 kHz drops to 3 while it's about 100 at 100 Hz.

$$\omega_{z1} \approx \frac{-1}{R_fC_f} \tag{19}$$

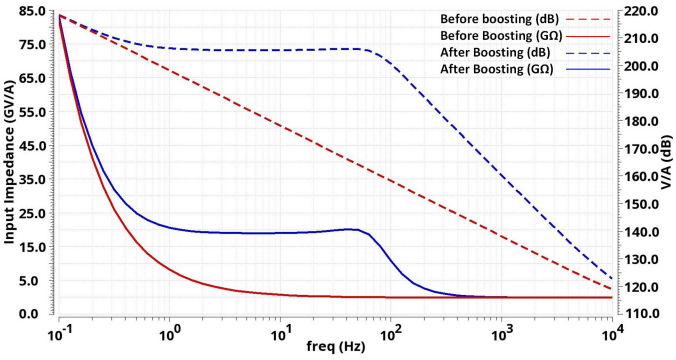

Fig. 5. The Input impedance before and after boosting versus frequency in order to compare the effect of an ideal negative capacitor and implemented negative capacitor

$$\omega_{z2} \approx \frac{-A_0}{A_{CL}} \frac{1}{R_L C_L} \tag{20}$$

$$\omega_{p1} = 0 \tag{21}$$

$$\omega_{p2} \approx \frac{-(R_L C_L + R_f C_f)}{R_L C_L R_f C_f} \tag{22}$$

$$\omega_{p3} \approx \frac{-A_0}{R_L C_L + R_f C_f} \tag{23}$$

V. Simulation Results

The layout of the proposed neural amplifier is shown in Fig. 6. Most of the area is occupied by input transistors and capacitors. The total area consumption is 0.03 mm^2. The closed-loop gain and input-referred noise of the amplifier are depicted in Fig. 7. The midband gain is 52 dB while the open-loop gain is 113 dB. Therefore, the gain error in Monte Carlo simulation was less than 3.5 mdB. The proposed amplifier open-loop gain can be enhanced more by decreasing the output current. The mean value of the CMRR in 500 runs for process and mismatch variation is 90 dB. The CMRR variation is depicted in Fig. 8.

The thermal noise of the proposed amplifier is just 27 nV/sqrtHz while the tail current is 1.2 µA. The total current consumption used in common-mode feedback amplifier is just 50 nA. After applying feedback to the amplifier, noise floor is increased slightly to 30 nV/sqrtHz. This result was expected according to Eq. 1. The negligible noise floor increment was achieved by opting input capacitor larger than normal values. C_{in} and C_f are 40 pF and 100 fF respectively. Due to the access to high density capacitor in the technology, the area consumption does not increase significantly.

The total input-referred noise in the bandwidth of EEG and Action potential (AP) signals are 0.9 μV_{rms} and 3.1 μV_{rms}, respectively. Thus, the NEF (noise efficiency factor) for EEG and AP signals are 3.9 and 1.4 respectively. The dominant noise in EEG bandwidth is usually flicker noise. This noise is decreased by increasing the size of input transistors. In order to

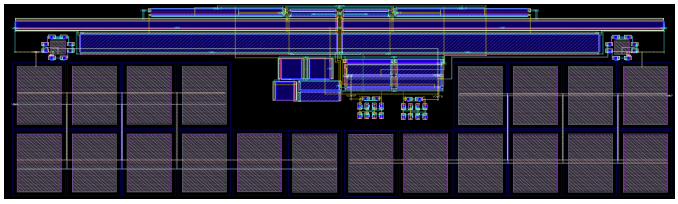

Fig. 6. Layout of the proposed amplifier without pads (100 µm x 309 µm), high density capacitors are exploited to minimize the area consumption

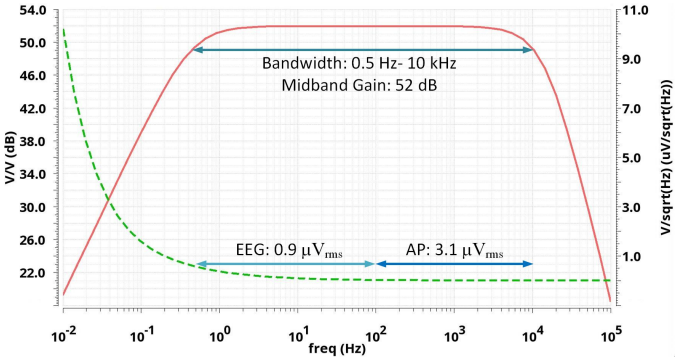

Fig. 7. Gain and noise of closed-loop amplifier

minimize the effect of parasitic capacitors, the input capacitors are considered 40 pF. Consequently, the input impedance drops in comparison with amplifiers with smaller capacitors. The input impedance is boosted by utilizing positive feedback loop. At 100 Hz, the input impedance is 10 GΩ. Under process and mismatch variation this value drops approximately to 8 GΩ as it is shown in Fig. 9 which is relatively high. This value proves to capture brain signal with negligible attenuation.

The proposed amplifier is compared with the state-of-the-art in table II. This structure achieved much better NEF [6] and PEF (power efficiency factor) [13] due to utilizing a new amplifier and power-efficient technique to boost the input impedance. The input impedance technique is the same as in [10]. Because of utilizing single input amplifier, they were obliged to exploit an inverter in feedback. Besides, they used back-end common-mode feedback to improve CMRR. Therefore, their NEF, PEF and area consumption is much higher. However, the proposed power efficient amplifier helped a lot to significantly reduce the NEF and PEF in our simulation.

Although the NEF of the proposed amplifier is relatively good in the bandwidth, it is a little high in the EEG bandwidth since the flicker noise is dominant in that bandwidth. By utilizing chopping technique after input capacitors, it is expected to achieve low NEF with the approximate same input impedance [4]. Besides, it can help to reduce the dimension of input transistors. Consequently, the parasitic capacitor will be minimized. It means that the total input-referred noise can be minimized. Finally, by considering the effect of second pole in the transfer function of boosted input impedance and some structural modifications, a high and constant input impedance can be achieved at the whole bandwidth in the future work.

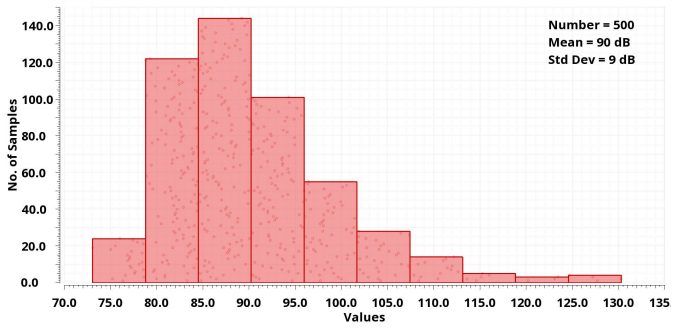

Fig. 8. CMRR at 50 Hz over process and mismatch variation

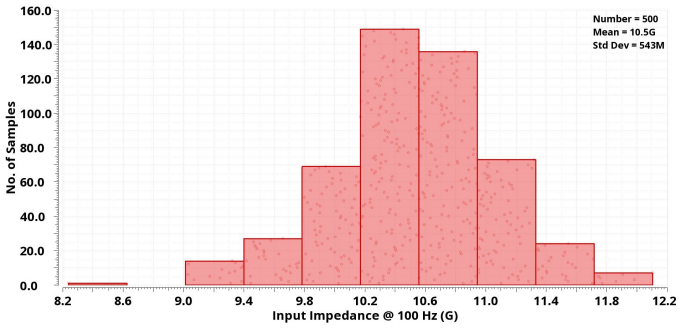

Fig. 9. Boosted input impedance for process and mismatch variation at 100 Hz

VI. Conclusion

In this article, a noise efficient amplifier based on combining cross-coupled amplifier and a high swing current reuse amplifier is proposed which has a high open-loop gain. The open-loop gain and thermal noise of the amplifier is 113 dB, 27 nV/sqrtHz respectively while it only consumes 1.2 µA from a 1.2 V voltage source. The NEF and PEF of the close-loop system are relatively low, because of the low NEF and PEF amplifier and high input capacitor value. Due to utilizing a power-efficient input impedance boosting technique, the proposed amplifier has about 10 GΩ and is suitable for high input impedance electrodes although it has high input capacitor. More importantly, the high frequency behaviour of the input impedance boosting technique is calculated. Through calculation and simulation, the second pole of the boosted input impedance is shown. This pole is dependent to lower cut-off frequency of the closed-loop amplifier and higher cut-off frequency of the open-loop amplifier. Therefore, the boosted input impedance is not flat and it decreases after a specific frequency. This frequency is lower than the higher cut-off frequency of the close-loop amplifier.

TABLE II
Comparison the proposed high input impedance amplifier with the state-of-the-art capacitively-coupled neural amplifiers

Specs	[14]	[11]	[10]	[15]	This Work
Technology (nm)	180	40	180	65	180
Supply Voltage (V)	1	1.2	1.8	1.2	1.2
Power (µW)	5.5	2.8	19.8	30	1.44
Gain (dB)	40-70	25.7	40	40	52
Bandwidth (Hz)	0.6-1k	1-5k	0.5-100	0.7-450	0.5-10.5 k
IR Noise (μV_{rms})	2.4	7.1	0.8	-	3.26
NEF	7	6.1	12.3	-	1.4
PEF	49	44.6	272	-	1.7
Input Impedance GΩ @ 100 Hz	6	1	0.05	0.3	10
Boosting Technique	Buffer	Aux-path	Positive feedback	Negative Cap.	Positive feedback
Area (mm^2)	-	0.069	6.5	-	0.03
Sim./Meas.	Sim.	Meas.	Meas.	Sim.	Sim.

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