Analog Integrated Circuits and Signal Processing
https://doi.org/10.1007/s10470-019-01577-w

A fully differential capacitively-coupled high CMRR low-power chopper amplifier for EEG dry electrodes

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Received: 14 June 2019 / Revised: 23 October 2019 / Accepted: 13 December 2019

Abstract
The use of dry electrodes is increasing rapidly. Since their impedance is high, there is a high impedance node at the connecting node between the electrode and amplifier. This leads to absorb powerline signal and high CMRR amplifiers are essential to eliminate this. In this article, we propose a low-power low-noise chopper-stabilized amplifier with high CMRR. In order to minimise the input-referred noise, an inverter-based differential amplifier is utilized. Meanwhile, a DC servo loop is designed to reject the DC offset of the electrode. Since all of the stages required a common-mode feedback, for each of the amplifiers a suitable circuit was used. Furthermore, a chopping spike filter is implemented at the final stage to attenuate the choppers' spike. Finally, to eliminate the offset effect from the mismatch and post-layout, a DC offset rejection technique is used. The designed circuit is simulated in a standard 180 nm CMOS technology. The designed chopper amplifier consumes just 1.1 μW at a 1.2 V supply. The mid-band gain is 40 dB while the bandwidth is from 0.5 to 200 Hz. The total input-referred noise is 1 μV_{rms} in its bandwidth. Thus the NEF and PEF of the designed circuit is 2.7 and 9.7, respectively. In order to analyse the performance of the proposed chopper amplifier against process and mismatch variation, Monte Carlo simulation is done. According to 200 Monte Carlo simulations, CMRR and PSRR are 124 dB with 6.9 dB standard deviation and 107 dB with 7.7 standard deviation, respectively. Ultimately, the total area consumption is 0.1 mm^2 without pads.

Keywords Chopper amplifier · EEG amplifier · Inverter-based amplifier · High CMRR · Low-power · Low-noise

1 Introduction

The importance of EEG signals is growing rapidly in the decades, owing to their high potential for use in the early diagnosis of ailments. They are not only used for clinical purposes such as epilepsy [1], Parkinson's disease [2], narcolepsy [3], depression [4] and motor impairment [5], but also in sports, entertainment and brain computer interfaces (BCI) [6–9].

Most of the clinical EEG signal monitoring systems use wet electrodes in order to improve the quality of the acquired signals. Wet electrodes need gel or saline solutions to decrease the skin to electrode impedance. When the EEG monitoring is required to be performed for a prolonged time, wet electrodes will lose their signal quality as the gel will dry out over time. Recently, considerable research efforts have been focused on dry electrodes which are more suitable for prolonged uses [10].

Although dry electrodes are more suitable for prolonged use than wet electrodes, they have a higher skin to electrode impedance and a lower signal to noise ratio. Because of their high skin to electrode impedance, the electrode will behave like an antenna and absorb the 50/60 Hz noise. In order to overcome this problem, a high CMRR biomedical amplifier could offer a solution due to the fact that the 50/60 Hz noise is like a common-mode signal in all of the electrodes. In this case, we are able to overcome some of the obstacles when moving towards dry electrodes, which

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Published online: 14 January 2020

are a promising solution for the future of a portable EEG signal acquisition device.

Thanks to recent developments in nano- and micro-electronics, these systems are more portable and non-invasive, which makes them suitable for outdoor monitoring. The portability and ease of use of EEG devices will have to rely on dry sensors that are capable of overcoming the high electrode impedance on skin. One way to compensate for this is the use of a high input impedance amplifier. The amplifier's input impedance $(Z_{in,amp})$ should be much greater than Z_1, which is depicted in Fig. 1 in order to have the lowest attenuation, and required $Z_{in,amp}$ could be calculated according to Eq. 1 where A_v is the gain of the chopper amplifier. The value of the skin to electrode and the electrode impedance of the state-of-the-art dry electrodes are depicted in Fig. 1, in their DC frequencies. It should be noted that all these impedances are dependent on the operating frequency. While Z_1 is high, and $Z_{in,amp}$ should be higher than Z_1 in order to have the minimum signal attenuation, the pointed node in Fig. 1 will have a very high impedance. One of the consequences of the high impedance node is its environmental noise. In this article, we have focused on a low-power and high CMRR amplifier in order to minimise the capacitive and inductive picked up noise to achieve a higher SNR in EEG systems.

$$V_{out} = A_v \left[\frac{Z_{in,amp}}{Z_{in,amp} + Z_1} \right] V_{brain} \tag{1}$$

Typical adult EEG signals have very low amplitudes (from 10 to 500 μV [11]) while the frequency of brain signals is in the bandwidth of 0.5 and 200 Hz [12]. In such a low frequency, the flicker noise will become a dominant noise contribution. Unfortunately, this noise value is comparable or even higher than the amplitudes of EEG signals [13, 14]. Consequently, conventional amplifiers cannot amplify them accurately. A number of techniques have been proposed to overcome these problems, such as Auto-Zeroing, chopping and bulk-driven techniques [15–17].

Chopping technique is one of the best approaches due to of their good trade-off between noise and power. In addition, it improves the CMRR of the designed circuit. Chopper amplifiers usually use a high switching frequency to minimise the flicker noise of a circuit. Consequently, their input impedance is lower than other techniques. Fortunately, auxiliary paths [18], positive feedback loops [19] and other techniques such as [20] have been proposed in order to increase this impedance. Therefore, the chopping techniques could be compatible even with dry electrodes which have high impedance.

In this article, a low-power low-noise chopper amplifier is designed. To this aim, different techniques are combined in order to achieve a chopper amplifier with improved performance. Some dry electrodes utilize an inherent buffer to decrease the impedance of the electrode, which is known as active electrodes [3, 21]. The chopping frequency of the designed amplifier is 20 kHz, is in the range of many comparable chopper amplifiers and proves that this input impedance is acceptable with suitable input impedance boosting techniques. An inverter-based amplifier is used in the first stage to minimise the total input-referred noise. In addition, the DC offset of dry and wet electrodes are considerably higher than the input signal which might saturate the outputs. To eliminate the amplification of the DC offset of an electrode, a DC servo loop was used, which acts as a high pass filter [10]. In order to eliminate the effect of the inherent offset which might cause a ripple in the output after fabrication, a parallel resistor and capacitor were used to block the inherent DC offset. The final designed amplifier has more than 112 dB CMRR, which is relatively high so that it can reject the high 50/60 Hz noise. Most noteworthy is the fact that the power line noise is not the only source of the common-mode signal in the electrodes. All common-mode interferences and artifacts can be converted to differential signals that can reduce the dynamic range of the amplifier. Therefore, a high CMRR biomedical amplifier is essential for the future of dry electrodes.

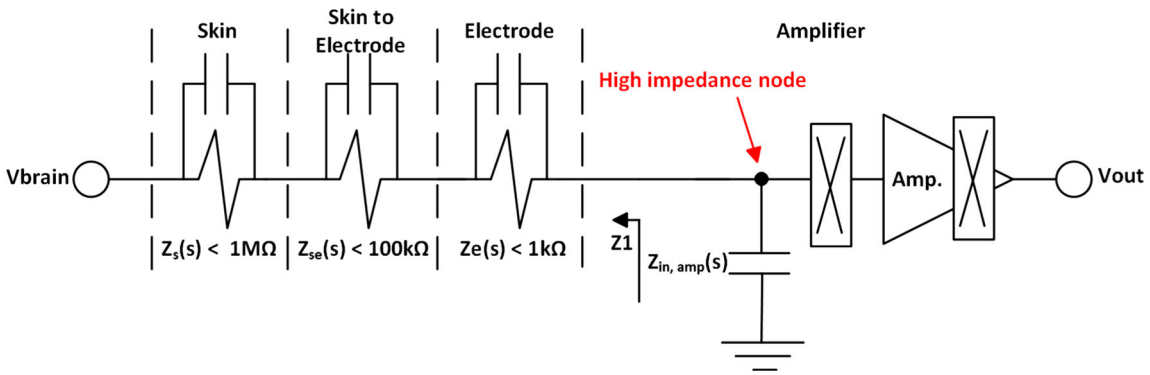

Fig. 1 The high impedance node and the nominal impedance values for dry electrodes

2 Architecture of the chopper amplifier

2.1 System overview

The schematics of the designed chopper amplifier are presented in Fig. 2. It has an up-modulator, shown with CH_{in} in the input, which operates with a 20 kHz switching frequency. A fully differential inverter-based amplifier is used as a pre-amplifier in the first stage to reduce the thermal noise, although it has a higher flicker noise which will be reduced significantly due to choppers. The up-modulated signal and unwanted noise will be amplified in this stage. Due to the use of choppers in the first stage, the input signal frequency is much higher than the noise corner frequency. Then, with the second modulator, the input signal will be sent back to the initial frequency and the flicker noise will be up-modulated [22]. The second amplifier with capacitive feedback will behave like a low-pass filter. The R_c is used to improve the phase margin of the two-stage amplifier. Regarding the chopping frequency and low-pass cut-off frequency, the low-pass filter separates the input and flicker noise. The DC servo loop function is described in [23]. In this article, we used a simple integrator consisting of a fully differential amplifier, a pseudo-resistor and a capacitor. The output swing of the amplifier in this stage determines the value of the tolerable electrode offset. That is the reason why a structure like [16] was used in order to reach the maximum output swing. While all of the amplifiers are fully differential, each has its own common-mode feedback. Furthermore, R_1 and C_1 were used to block the inherent offset of the G_{m1}. Due to the high value of R_1, it will block the DC signal, whereafter the AC signal will go through C_1 to the output.In this way the DC offset will be blocked while the AC signal goes through the capacitor. Finally, the ripple, due to the residual noise and chopping spikes after filtering, diminished with the chopping spike filter (CSF).

2.2 First stage amplifier

Because of the importance of the first stage in the total input-referred noise, the pre-amplifier is designed according to Fig. 3a. The total approximate input-referred noise of this structure is calculated as follows:

$$\overline{V_n^2} = \frac{8kTc}{g_{m_1} + g_{m_2}} + \frac{2K_n}{W_1 L_1 f C_{ox}} + \frac{2K_p}{W_2 L_2 f C_{ox}} \tag{2}$$

In the above equation c is approximately 2/3 though it varies slightly according to the biasing of the transistor, k is the Boltzmann constant and T is temperature in Kelvin. As can be seen, the total input-referred noise consists of two major contributions: the flicker and thermal noise. Although this structure has approximately doubled the input flicker noise, the thermal noise will be approximately halved. Fortunately, the effect of the flicker noise will be reduced by the size of the transistors. Furthermore, due to the use of a chopping technique, the flicker noise will be significantly reduced. Thus, the equation could be simplified in the following manner:

$$\overline{V_n^2} = \frac{8kTc}{g_{m_1} + g_{m_2}} \tag{3}$$

A fully differential structure needs a common-mode feedback in order to function properly. Therefore, the common-

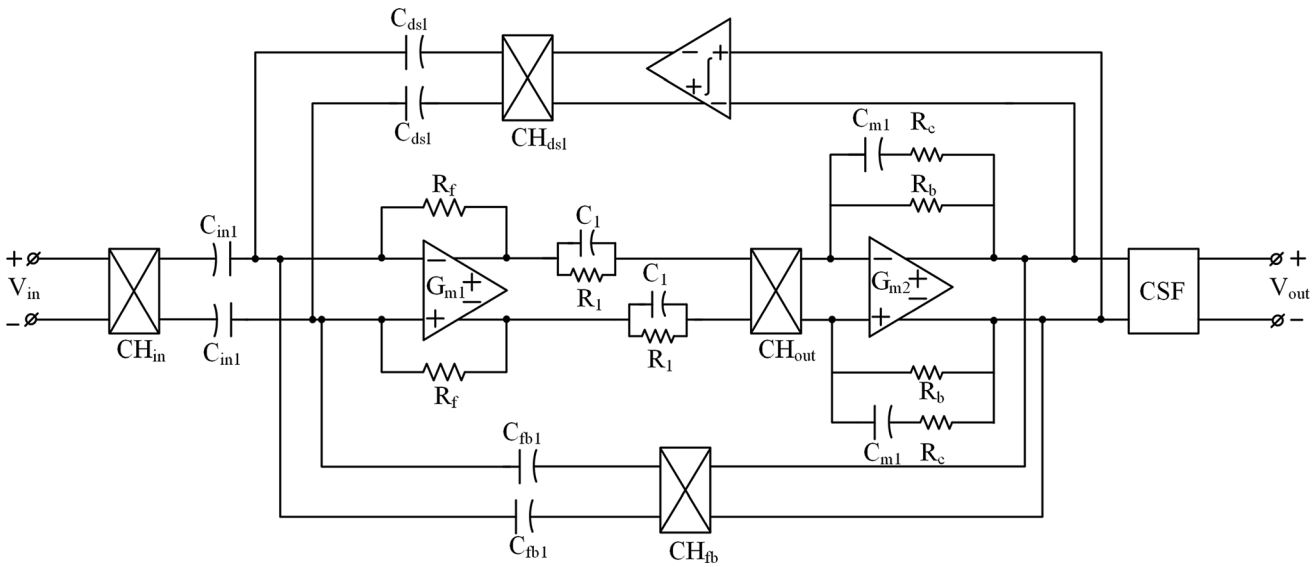

Fig. 2 Structure of designed chopper amplifier

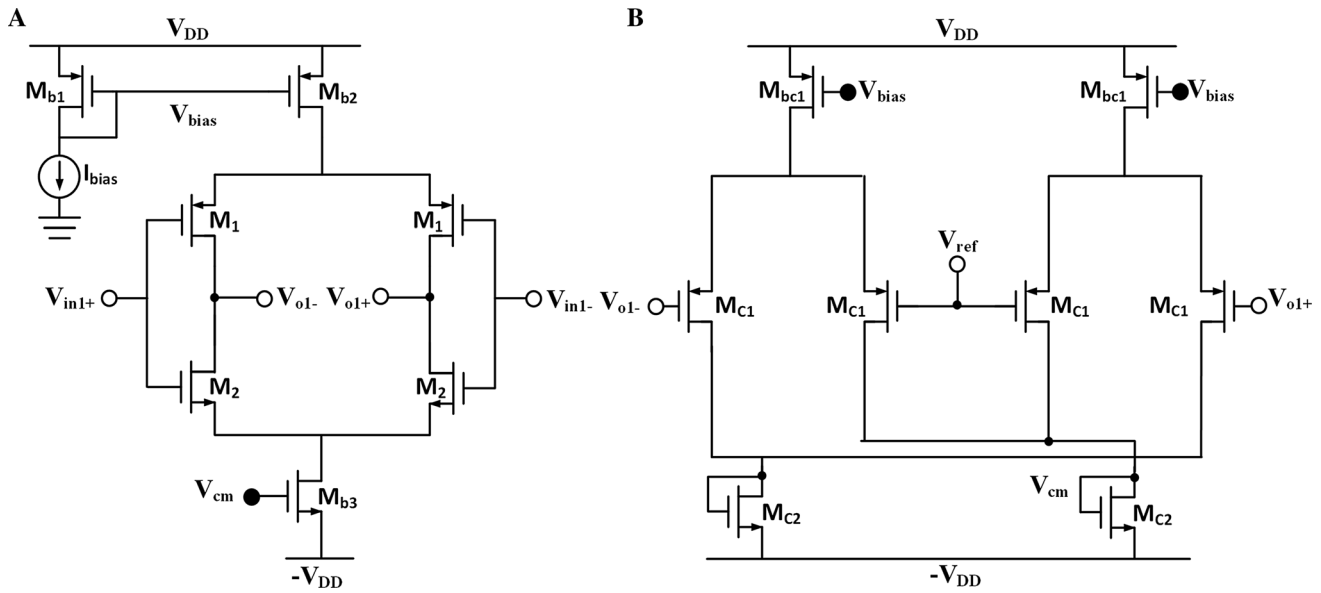

Fig. 3 (**a**) First stage current-resuse pre-amplifier; (**b**) common mode feedback

mode feedback (depicted in Fig. 3) is used. In addition, the R_f (which is depicted in Fig 2) was used to fix the DC of the input and output on common-voltage.

2.3 Active low-pass filter

Most of the observed EEG signals have a maximum frequency of 200 Hz. In order to have such a small cut-off frequency a very large RC is needed, which leads to an enormous area consumption. For implantable and wearable applications, area consumption is a limitation and challenge. To overcome this problem, an active filter was used in the second stage. This is a trade-off between the area and power consumption. The structure of the amplifier which is used in the active filter is shown in Fig. 4a. While the second amplifier gain is 40 dB, according to Miller's theorem, the effective capacitor in the input of the second amplifier will be 100 times larger than the physical value.

R_{cm} is needed to set the DC voltage at the output nodes, though if the value of R_{cm} is low, the differential gain of the amplifier would be limited according to Eq. 4. Since the value of r_o is considerably high due to the low current and large L, the implemented resistor should have a big value. That's why pseudo resistors were used instead of conventional passive resistors [13].

$$\frac{v_{out}}{v_{in}} = g_{m_3}[R_{cm} \parallel r_{o3} \parallel r_{o4}] \tag{4}$$

In addition, the value of R_c is 850k Ω and is implemented by the N-well resistor. It is calculated according to Eq. 5 to eliminate the right hand side zero and improve the phase margin of the two-stage amplifier. The output DC value is set by $-V_{DD} + V_{gs3,4}$.

$$R_c = 1/g_{m3} \tag{5}$$

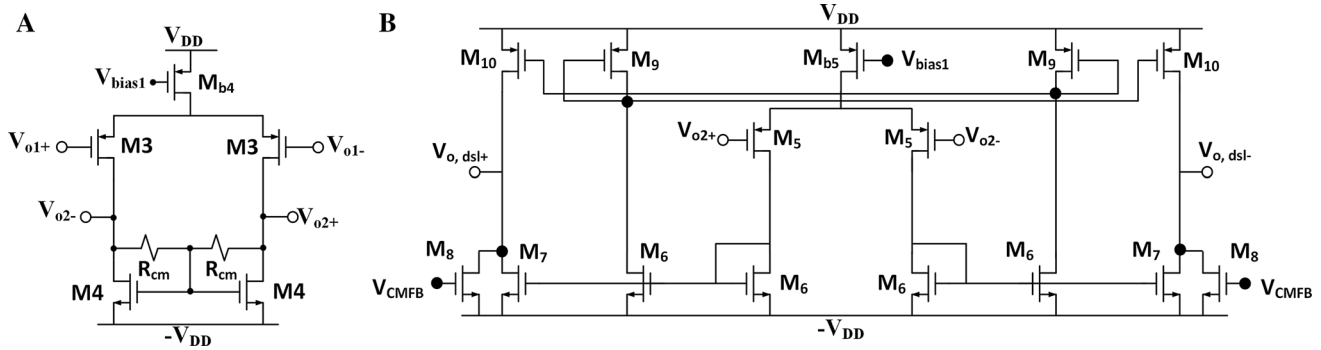

Fig. 4 (**a**) The amplifier which is used in the low-pass filter; (**b**) the DSL amplifier

2.4 DC servo loop (DSL)

The designed DSL consists of an integrator, a modulator and two capacitors to feed them back, as is shown in Fig. 2. The DSL is used when electrodes which have considerable offset voltage are used. This voltage is usually much higher than the amplitude of the input signal. In this case, in order to prevent output saturation, we have had to block the DC voltage. Although insulator electrodes do not have an offset due to their electrical properties, most of the dry and wet electrodes have large offsets, which indicated the DSL's significance. Therefore, with special feedback structure, a high pass filter was achieved and the DC input offset will be attenuated, while the input signal will be amplified as before. The designed integrator utilizes one amplifier, two capacitors and two resistors. The EEG bandwidth is from about 0.5 Hz and the low cut-off frequency is determined according to Eq. 6 [24]:

$$f_h = \frac{C_{dsl}}{C_{fb1}} f_{0dsl} \tag{6}$$

In the above equation f_h is the minimum required bandwidth, which in this design is 0.5 Hz and f_{0dsl} is the unity-gain frequency of the integrator in the DSL. This unity-gain frequency is determined by R and C inside the integrator. In order to obtain such a low f_h , we require a large RC. Since area consumption is one of the limitations, in the designed integrator a pseudo resistor, such as the low-pass filter, is used in the integrator structure in order to minimise the area consumption. As the maximum tolerable offset is calculated with Eq. 7, the designed amplifier should have the maximum output swing. Thus, the best choice is to utilize just two transistors at the output nodes, as is done in Fig. 4 [24].

$$V_{EO} = \frac{C_{dsl}}{C_{in1}} V_{out,max} \tag{7}$$

In the above equation V_{EO} is the maximum tolerable input offset voltage and $V_{out,max}$ is the maximum output swing of the integrator. The designed amplifier can tolerate ± 50mV offset. If the desired tolerable offset is higher, this amplifier can tolerate the higher offset at the cost of the higher input-referred noise. As the DSL output-referred noise is considerably high, it will increase input noise. In order to minimise the flicker noise of DSL, the input transistors have big W and L. Fortunately, in the designed amplifier, most of the contribution to the input-referred noise is still from the pre-amplifier. This means that the DSL has a negligible noise contribution in the entire system and the designed circuit can even tolerate the higher offset at the cost of a little noise increment.

The structure of the common-mode feedback which is used for the DSL amplifier is similar to what is used for the pre-amplifier at the first stage. Due to the use of common-mode feedback in all stages, the designed amplifier has a high CMRR.

2.5 Ripple reduction and chopping spike filter

There are different ripple reduction approaches proposed in the literature [25–27]. One of the sources of the output ripple is the inherent offset, especially the offset of the pre-amplifier. In this design, the power consumption was one of the most important parameters to maintain at a low level. That is why a structure similar to that used in [28] was used (as is shown in Fig. 2). In this case, a parallel capacitor and resistor are used to block the DC offset of the first stage amplifier, which is the dominant contribution of the total internal offset. These capacitors and resistors are represented by R_1 and C_1. The DC signal is blocked due to the large resistor while the AC signal goes through the capacitor. Accordingly, we need a large resistor which is implemented by a pseudo-resistor. The performance of this circuit is checked after the post-layout. It is noteworthy that the total ripple of the outputs without any ripple reduction technique implementation could be calculated by Eq. 8 [28].

$$V_{ripple,PP} \approx \frac{8V_{os} \times \omega_0 \times A_0}{\pi \times \omega_{chop}} \tag{8}$$

In this equation V_{os} is the offset of pre-amplifier, ω_0 and A_0 are closed-loop bandwidth and gain, respectively. These ripples are attenuated by utilizing the parallel RC. The absolute mean value of residual offset based on 200 Monte Carlo simulation is 23 μV with 19 μV standard deviation when the DSL is off. According to simulation, the absolute offset temperature coefficient is $270\,\mathrm{nV/C^\circ}$ when the temperature varies from -20° to 80°. Although chopping techniques reduce the flicker noise significantly, the choppers inject spikes into the input signals. In this case, these spikes should be suppressed by another circuit. Therefore, a chopping spike filter was used (as depicted in Fig. 5), which works with a chopping frequency twice as high as all of the chopper modulators in the circuit [29].

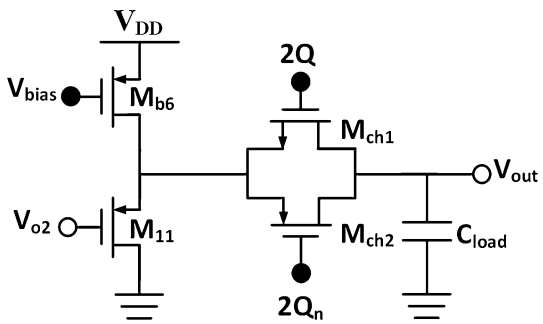

Fig. 5 Chopping spike filter with load capacitor

The load capacitor of the next stage, which is usually the input of an analog to digital converter, is modelled as a required capacitor. The schematic of the chopping spike filter is depicted in Fig. 5.

3 Post-layout simulation results and discussion

The proposed EEG amplifier is simulated in a 180 nm CMOS technology with one poly and six metals. All the transistor dimensions in each of the amplifiers are presented in Tables 1 and 2. It draws $0.9\,\mu A$ from a 1.2 V supply. It is noteworthy that the minimum and maximum supply voltages are − 0.6 V and + 0.6 V, respectively. In total it consumes $1.1\,\mu W$, which is half of the most state-of-the-art amplifiers with similar noise. The total area consumption is about $0.1\,\text{mm}^2$. The density of the available capacitor in this technology was $1\,fF/\mu m^2$ and according to Fig. 6, most of the area is occupied by the capacitors. This shows that the area consumption could be relatively reduced with technologies which have high-density capacitors. In the following, the values of different parameters of the chopper amplifier after the post-layout simulation will be discussed.

The gain, CMRR and PSRR are shown in Fig. 7. The blue line depicts the differential gain while the red line is the common-mode gain. The green and yellow lines depict the output gains according to the positive and negative supply voltage source, respectively. The chopper amplifier bandwidth is from 0.5 to 200 Hz when the mid-band gain is 40 dB. The 0.5 Hz high-pass frequency shows the DSL's performance. Due to good biasing and three common-mode feedbacks in each stage, the CMRR is more than 112 dB, which is considerably higher than most of the best structures reported in the literature. The PSRR is limited by the $PSRR^-$ though it is still 90 dB, which is adequately high. It is noteworthy that high CMRR applications are more essential than high PSRR applications, as many commercial and clinical EEG systems use an inherent battery to make them portable and wearable. In addition the CMRR and PSRR mean-value are 124 and 107 dB, respectively.

Table 1 Transistor size in the first and second stages

Tran.	W/L (μm/μm)	g_m/I_d	Tran.	W/L (μm/μm)	g_m/I_d
M_1	5(10/7)	24	M_{b1}	2.5/7	15.5
M_2	8/6	23	M_{b2}	2(2.5/7)	15.4
M_3	10(1/1)	24	M_{b3}	1/15	12.2
M_4	0.5/200	11	M_{b4}	2(2.5/7)	15.4

Table 2 Transistor size in the DSL and CSF stages

Tran.	W/L (μm/μm)	g_m/I_d	Tran.	W/L(μm/μm)	g_m/I_d
M_5	10(5/1)	30	M_{11}	2.2/1.8	23
M_6	10(2/2)	28.8	M_{b6}	1/17	15
M_7	10(4/2)	28.8			
M_8	10(4/2)	29	M_{ch1}	0.22/0.18	–
M_9	10(1.7/1)	29			
M_{10}	20(3/1)	28	M_{ch2}	0.48/0.18	–
M_{b5}	1/6	15			

Besides, CMRR and PSRR standard deviations are 6.9 and 7.7 dB, respectively

The integrated input-referred noise, from 0.5 to 200 Hz, is a mere $1\mu V_{rms}$. The total input-referred noise spectral density is depicted in Fig. 8. Most of the contribution is related to the thermal noise of the first stage which can be reduced at the cost of a higher power consumption. All input transistors are biased in the sub-threshold to achieve the highest g_m/I_d.

In the second stage, a resistor and capacitor were used in order to reach a phase margin of 60 degrees. In order to minimise the area consumption of the resistors, the N-well resistors were used. Fortunately, the phase margin has an acceptable variation even with 30% process variation in resistance value.

The total harmonic distortion for the 10 mV peak-peak input voltage is less than 10 %. Due to the chopping spike filter, the output spike is negligible for a 10 pF load. In Fig. 9, the output spikes are shown for a 1 pF load and without a load. The red line represents no load, while the yellow line represents a 1 pF load where the spikes are negligible.

The noise efficiency factor is a figure-of-merit to quantify the merit of a designed circuit. This could be calculated according to Eq. 9.

$$NEF = V_{ni,rms}\sqrt{\frac{2I_{tot}}{\pi U_T 4kTBW}} \tag{9}$$

In the above, $V_{ni,rms}$ is the total equivalent input-referred noise in the amplifier's bandwidth, BW is the amplifier's − 3 dB bandwidth, U_T refers to the thermal voltage and I_{tot} is the total current drawn from the power supplies. Accordingly, the NEF of the designed amplifier is 2.7 and PEF (defined as $NEF^2 V_{DD}$, where V_{DD} is the total supply voltage) is 9.2. In Table 3 the designed chopper amplifier is compared to the available state-of-the-art circuits. Finally, it should be noted that the range of CMRR is driven from 200 Monte Carlo simulations under both process and

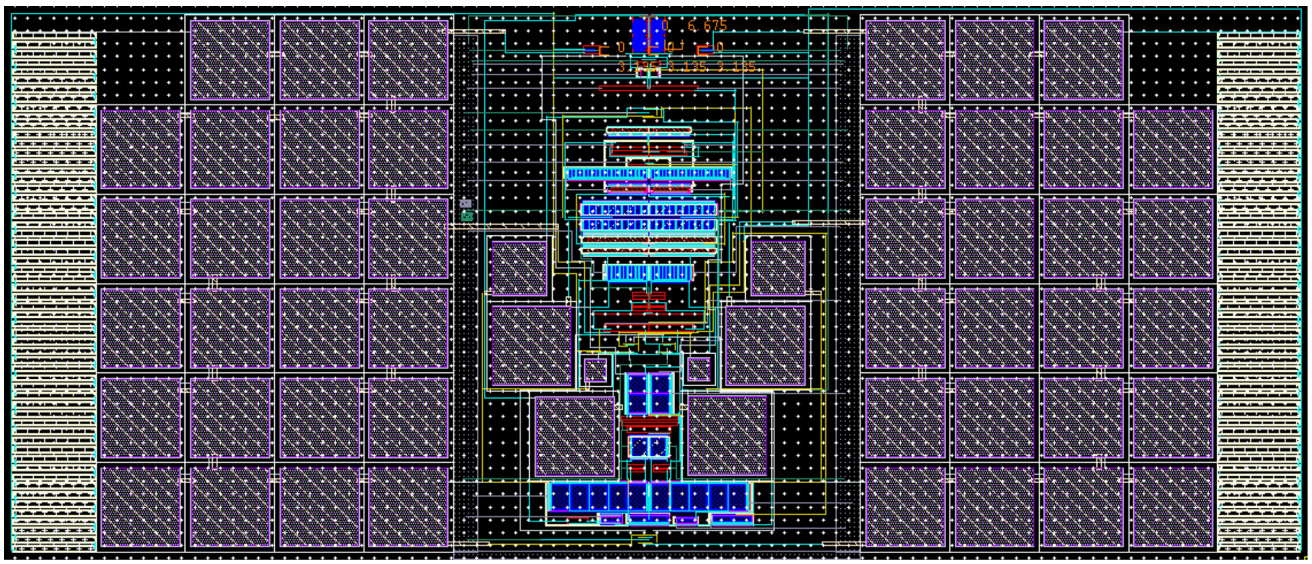

Fig. 6 The layout of the designed chopper amplifiers without pads

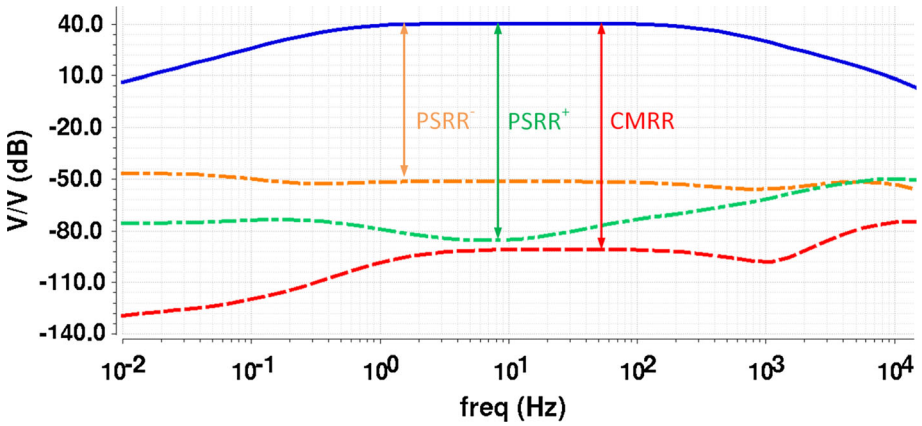

Fig. 7 The CMRR and $PSRR^{+}$ and $PSRR^{-}$

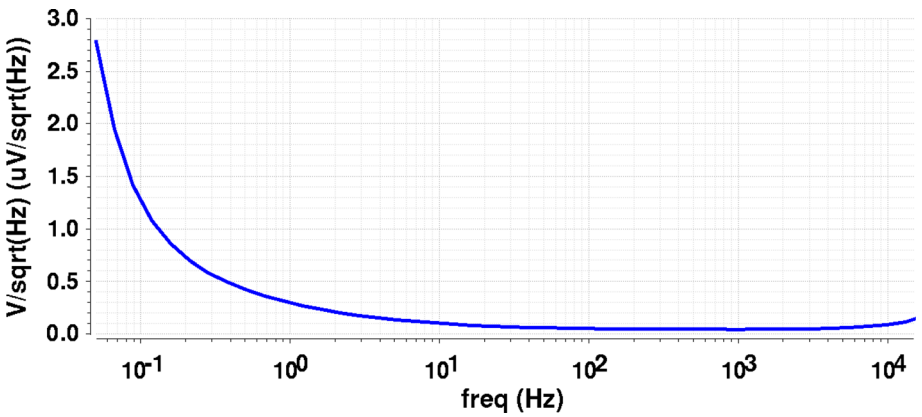

Fig. 8 The input-referred noise of the designed chopper amplifier

mismatch variations. Additionally, the PSRR variation was between 92 and 125 dB.

Although the proposed chopper amplifier addresses an important challenge due to the unwanted power line noise in EEG systems with dry electrodes, it's not still fully compatible with dry electrodes due to its low input impedance. Therefore, in our future work, the designed amplifier will be further enhanced with suitable input impedance boosting circuit. Furthermore, it will be fabricated and the

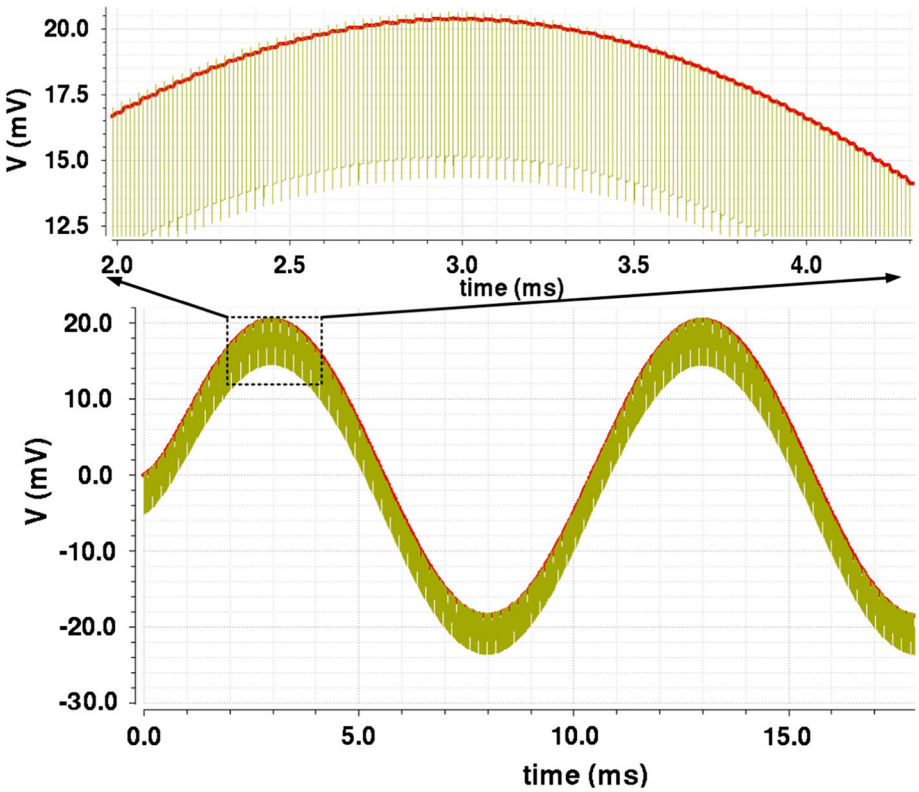

Fig. 9 Residual spikes with 1 pF load and without any load

Table 3 Performance summary and comparison with available state-of-the-art circuits

Parameters	[24]	[30]	[31]	[32]*	This work
Year	2011	2016	2017	2018	2019
Technology	65	180	130	180	180
Supply voltage	1	1.25	1.2	1	1.2
Power	1.8	2.1	3.5	3.8	1.1
Gain (dB)	40	34	40	40/60	40
CMRR (dB)	134	85	85	105	112–146
Noise ($nV_{rms}/\sqrt{Hz}$)	60	45	47	54	50
NEF	3.3	2.9	3.9	4.1	2.7
PEF	10.89	10.5	18	16.81	9.2
Area (mm^2)	0.2	0.23	0.3	–	0.1

*Simulation results without DSL

performance of the proposed amplifier will be tested with real EEG signals.

4 Conclusion

In this article, a low-power low-noise chopper amplifier was designed in order to reduce the powerline noise in EEG systems with dry electrodes. Due to good biasing, common-mode feedback and the use of chopping technique, the designed circuit has a relatively high CMRR which makes it more suitable for EEG dry electrodes. In order to consider inherent offset, Monte Carlo simulation for process and mismatch is done. The CMRR of the designed amplifier is more than 112 dB, which will prove to eliminate 50/60 Hz noise. The proposed chopper amplifier consumes relatively low power while resulting in low noise, due to combining inverter-based amplifiers at the first stage and the chopper. The chopper amplifier is specifically designed for EEG recording. The NEF and PEF are 2.7 and 9.2 respectively, which prove the merit of the designed circuit. The total area consumption is 0.1 mm^2 which makes it suitable for even an implantable circuit, especially when it consumes a mere 1.1 μW. The DSL was implemented in order to make a high-pass filter to prevent the output saturation due to the electrode offset. The total input-referred noise is 1 μV_{rms}, from a bandwidth of 0.5 to 200 Hz. In summary, the proposed chopper amplifier could be a good choice for amplifying EEG signals from wet and dry electrodes, as it has low noise, uses low power and high CMRR, and is able to block the electrode offset.

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