Master's thesis

NTNU
Norwegian University of Science and Technology
Faculty of Information Technology and Electrical Engineering
Department of Electronic Systems

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Microwave Characterization and Analysis of RF-components in 5G-systems

Master's thesis in Electronics System Design and Innovation
Supervisor: Morten Olavsbråten
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Summary

This thesis presents a characterization of the GaN GH25 HEMT process produced by the UMS foundry, in addition to a simulation of envelope tracking techniques on GaN and GaAs amplifiers. The GaN MMIC is measured using a manual probe station calibrated with a LRRM on-wafer technique. The measured results verifies the computer simulation models up to 30 GHz. The transistor models are most accurate in the range from 10 GHz to 22 GHz and show a conservative performance at lower frequencies.

The envelope tracking techniques made on a GaN LNA and a GaAs PA does not allow for a comparison based on the substrate materials. Simulations are made using a 4 MHz 16-QAM modulated signal. Both amplifiers show increases in PAE, but because the GaN amplifier is low noise optimized, envelope tracking this amplifier is of little interest. The GaAs amplifier however, shows great results with regards to gain, linearity and PAE. Different envelope tracking functions are explored, and the PET technique shows that drain voltage bandwidth is lower than 50 % at the equal performance or slight cost of PAE or linearity compared to conventional ET technique.

Sammendrag

Denne masteroppgaven presenterer en karakterisering av GaN GH25 HEMT prosessen produsert av UMS, i tillegg til en simulering av envelope tracking teknikker på GaN og GaAs forsterkere. GaN MMICen er målt ved hjelp av en manuell probestasjon kalibrert med en LRRM på-wafer teknikk. De målte resultatene verifiserer datamodellene opp til 30 GHz. Transistormodellene er mest nøyaktige i området fra 10 GHz til 22 GHz og viser en konservativ ytelse på lavere frekvenser.

Envelope tracking teknikkene gjort på en GaN LNA og en GaAs effektforsterker gir ikke rom for en sammenligning basert på substratmaterialene. Simuleringer er gjort ved bruk av et 4 MHz 16-QAM modulert signal. Begge forsterkerne viser forbedring i PAE, med en faktor på 2. Fordi GaN forsterkeren er lavstøyoptimert, har envelope tracking på denne forsterkeren lite hensikt. GaAs forsterkeren derimot, viser gode resultater med tanke på gain, linearitet og PAE. Forskjellige envelope tracking funksjoner er vist, og PET teknikken viser at spekteret til drainspenningen er mindre enn 50 % ved lik eller en liten kostand til PAE eller linearitet sammenlignet med konvensjonell ET-teknikk.

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CHAPTER 1

INTRODUCTION

1.1 Motivation

Modern communication systems have evolved at an increasing rate in the last decades in regards to data throughput and availability. To achieve the high datarates of these systems a great deal of challenges arise for the radio front end designer. Modern systems require large orders of linearity and great power back-off capability to meet the requirements of high throughput modulation schemes like orthogonal frequency division multiplexing (OFDM) combined with deep amplitude and phase modulation (QAM) used in LTE (4G) and 5G.

To achieve the necessary transmission throughput a compromise is done on the power amplifier efficiency. This leads to very inefficient base stations in cellular networks. One of the biggest contributors to the energy consumption is the base station power amplifier which needs great amounts of cooling hardware during operation due to its inefficiency.

A promising type of efficiency enhancement in power amplifiers is the envelope tracking technique. This master thesis explores the use of this technique on two power amplifier substrate technologies, GaN MMIC (Monolithic Microwave Integrated Circuit) and GaAs MMIC. A simplified diagram of an envelope tracking transmitter is shown in figure 1.1. This thesis also characterizes the produced GaN MMIC's properties and compares the results to a computer simulation model provided by the manufacturer.

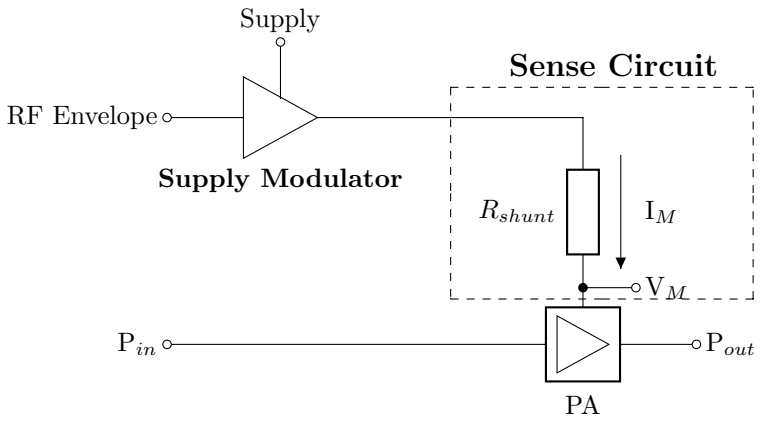


Figure 1.1: Simple diagram showing an envelope tracking power amplifier transmission system

1.2 Scope

This thesis describes the characterization of a GaN MMIC and the use of envelope tracking on two power amplifier technologies, GaN and GaAs. The GaN circuits presented are not designed by the author, but by previous students' thesises due to long manufacturer lead time. Because the original power amplifier that was meant to be used oscillates, a LNA (low noise amplifier) on the same chip will be used in its place. The GaAs amplifier is a commercially available MMIC used in the telecom industry [2]. The text is divided into several parts, the theoretical background provides the reader with an introduction to basic theory used in microwave design and measurements. Then the characterization and implementation of the envelope tracking technique is presented, before the resulting simulations are shown, discussed and concluded.

CHAPTER 2

THEORETICAL BACKGROUND

This chapter will give an introduction to the theory applied in this thesis.

2.1 Power Amplifier Process Technologies

As the development of semiconductor fabrication has accelerated with the growth of conventional silicon based technologies, the process technologies used in power amplifiers have also seen great improvement at an improved rate. The following sub-chapters will briefly explore some of these power amplifier technologies.

2.1.1 Heterojunction Bipolar Transistor

The heterojunction bipolar transistor (HBT) has the same operational characteristics as the bipolar junction transistor (BJT) but consists of two differing semiconductor materials in the emitter and base, thus the heterojunction name. The heterojunction gives the transistor separate bandgap energies in the emitter and base, allowing higher current gain compared to the BJT [9]. The high frequency performance can also be increased due to the heterojunction characteristic, so HBTs are suitably used in very fast switching, high power applications.

2.1.2 Metal Semiconductor Field Effect Transistor

The Metal Semiconductor Field Effect Transistor (MESFET) is similar to the MOSFET, but utilizes a Schottky metal gate rather than a dielectric oxide insulator found in the MOSFET. Due to the Schottky barrier, enhancement mode operation is more rarely used as this causes a current leak through the gate into the channel if the threshold voltage is not kept below the forward bias voltage of ≈ 0.7 V. In RF applications the increased mobility of charge carriers in the channel compared

to that of the MOSFET is essential, as this increases transconductance, maximum current and high frequency performance.

2.1.3 High Electron Mobility Transistor

The High Electron Mobility Transistor (HEMT) is a field-effect transistor using a heterojunction in the channel instead of a doped region as in the MESFET, yielding the similar boost in performance as the HBT over the BJT. HEMT-transistors have high gain, high frequency performance and excellent low noise characteristics. However, they share the same Schottky like operation in the gate with the MESFET so they are also most often used in depletion mode.

2.1.4 The GaN HEMT Transistor

The Gallium Nitride HEMT transistor uses GaN in the heterojunction. The AlGaN/GaN heterojunction is very sought after due to its very high band gap energies [8]. Compared to conventional HEMT technology using GaAs the bandgap energies gives the GaN transistor very high breakdown voltages, which in turn increases the power density in the device. Higher power density devices allows for smaller packages for a given output power in the transmitter.

2.1.5 UMS Foundry

The United Monolithic Semiconductors' (UMS) foundry provide several options in fabricating Microwave Monolithic Integrated Circuits, including GaN and GaAs HEMT, HBT and MESFET. Table 2.1 [4] shows some of these processes. The table shows some of the mentioned differences between GaN and GaAs HEMTs. Notice the power density, saturation current and breakdown voltage.

Table 2.1: UMS Foundry process technologies

	GH25 GaN	**PH25 Low Noise GaAs**	**PPH25 Power GaAs**	**PPH25X High Power GaAs**	**HB20M GaAs**	**HP07 GaAs**
Active device	HEMT	pHEMT	pHEMT	pHEMT	HBT	MESFET
Power Density	4.5 W/mm	250 mW/mm	700 mW/mm	900 mW/mm	2 W/mm	400 mW/mm
Gate / Emitter Length	0.25 um	0.25 um	0.25 um	0.25 um	2 um	0.7 um
Ids (gm max)	750 mA/mm	200 mA/mm	200 mA/mm	170 mA/mm	0.3 mA/mu2	300 mA/mm
Ids sat / Ic	1000 mA/mm	500 mA/mm	500 mA/mm	450 mA/mm		450 mA/mm
Vbds / Vbce	>100 V	>6 V	>12 V	>18 V	>14 V	>14 V
Cut off freq.	30 GHz	90 GHz	50 GHz	45 GHz	30 GHz	15 GHz
Vpinch	-3.4 V	-0.8 V	-0.9 V	-0.9 V	-	-4.0 V
Gm max / beta	300 mS/mm	560 mS/mm	450 mS/mm	400 mS/mm	60	110 mS/mm
Noise / Gain	1.8 dB / 11 dB @ 15 GHz	0.6 dB / 13 dB @ 10 GHz 2 dB / 8 dB @ 40 GHz	0.6 dB / 12 dB @ 10 GHz	-	-	-

This thesis uses the GH25 GaN process [5] from UMS. At a cost of 2500 $\frac{\$}{mm^2}$, 15 MMICs of 3 mm x 2 mm are produced on academic license.

2.2 S-Parameters

At high frequencies it becomes difficult to measure open and short circuit absolute voltages and currents, as these measurements may destabilise and destroy active circuits. The use of S-parameters solves these problems, by measuring small signal incident and reflected waves into matched sources and loads in terms of power. In general S-parameters support an arbitrary number of ports on a DUT, but for simplicity a typical S-parameter two-port is shown in figure 2.1.

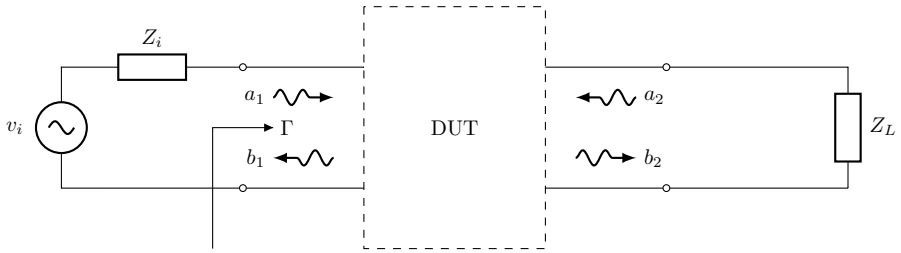


Figure 2.1: 2-Port S-Parameters

The S-parameter is defined as the ratio of reflected and incident wave

$$S_{ij} = \frac{b_i}{a_i} \tag{2.1}$$

where $a_k = \sqrt{V_k^+ I_k^+}$ and $b_k = \sqrt{V_k^- I_k^-}$. From these and (2.1) one can show that

$$\Gamma_s = \frac{Z_s - Z_0}{Z_s + Z_0} \tag{2.2}$$

and

$$\Gamma_l = \frac{Z_l - Z_0}{Z_l + Z_0} \tag{2.3}$$

where Z_0 is the characteristic impedance. Ultimately the input and output reflection coefficients become

$$\Gamma_{in} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \tag{2.4}$$

and

$$\Gamma_{out} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \tag{2.5}$$

2.3 Power Amplifier Metrics

2.3.1 Stability

Power amplifiers have to be unconditionally stable to suppress oscillations. Stability is unconditional if $|\Gamma_{in}| < 1$ and $|\Gamma_{out}| < 1$. Thus it is clear from (2.4) and (2.5) that the amplifiers' stability varies with Γ_s and Γ_l which are frequency dependent, leading to design restraints outside the RF bandwidth. To measure *how* stable an amplifier is, μ-factors are used where

$$\mu_{source} = \frac{1 - |S_{22}|^2}{|S_{11} - \Delta S_{22}^*| + |S_{12}S_{21}|} \tag{2.6}$$

and

$$\mu_{load} = \frac{1 - |S_{11}|^2}{|S_{22} - \Delta S_{11}^*| + |S_{12}S_{21}|} \tag{2.7}$$

where $\Delta = S_{11}S22 - S_{12}S_{21}$. If either μ_{source} or μ_{load} is > 1 the amplifier is unconditionally stable, and the greater they become the more stable it is.

2.3.2 Bias and Amplifier Classes

The bias point of a power amplifier sets the amplifiers mode of operation. Figure 2.2 shows 3 common linear amplifier classes, A, AB and B, and their current-voltage relationship. The increasing blue curves shows an increasing gate-source voltages, V_{GS}. In class A the operating point is set so that at no input drive power, the amplifier will draw $I_D = 0.5I_{DMax}$, and as the voltage of the input varies, the amplifier will conduct the complete input wave. So a class A amplifier has a conduction angle of $\sigma = 2\pi$. This means low efficiency and high linearity.

Conversely, the class B amplifier will not conduct any current at no input drive power. Because the amplifier will not conduct with lower gate voltages, the amplifier will clip the waveform, causing distortion and yielding a conduction angle of $\sigma = \pi$, effectively making a rectifier. And thus the class AB amplifier will be somewhere in between the A and B classes with $0 < I_D < 0.5I_{DMax}$ and $\pi < \sigma < 2\pi$.

An AB class amplifier is often chosen because it compromises between the higher efficiency of the class B amplifier and the linearity of the class A amplifier.

2.3.3 Power Output

An ideal amplifier's power output will have a similar characteristic to that of figure 2.3. The amplifier will work linearly with constant gain at lower input powers, but as it reaches a certain level, the output power will start to saturate and the gain will drop. The point where the output power deviates 1 dB from ideal operation is called the compression point.

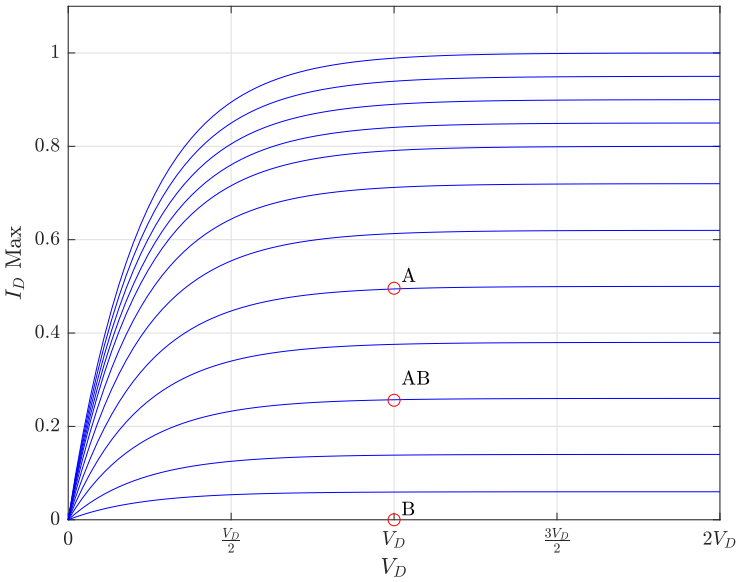


Figure 2.2: Bias operating points for an ideal amplifier

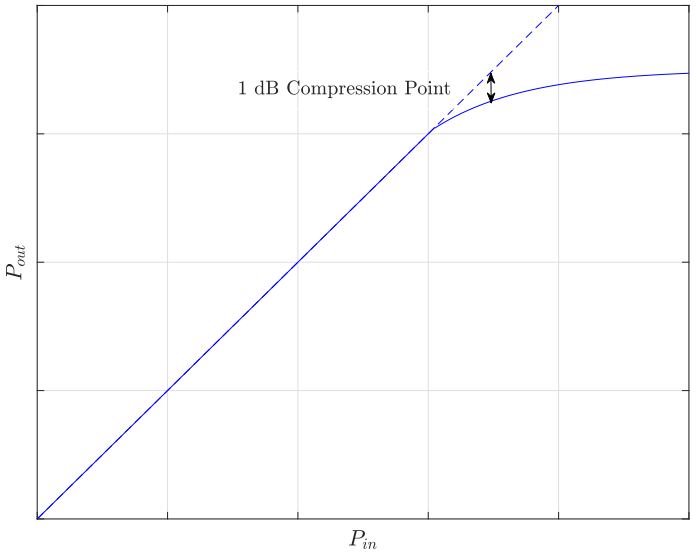


Figure 2.3: P_{out} vs P_{in} characteristic showing the 1 dB compression point

2.3.4 Gain

The field of RF-microwave design operates with three definitions of gain. These definitions are listed in (2.8), (2.9) and (2.10).

$$\text{Power Gain: } G = \frac{P_L}{P_{in}} \tag{2.8}$$

$$\text{Available Gain: } G_A = \frac{P_{avn}}{P_{avs}} \tag{2.9}$$

$$\text{Transducer Power Gain: } G_T = \frac{P_L}{P_{avs}} \tag{2.10}$$

Power gain is the ratio between the power that is dissipated in the load and the power being delivered to the 2-port. Available gain is the ratio between the power available from the 2-port and the power available from the source, while transducer gain is the ratio between power dissipated in the load and power avilable at the source. Transducer gain is a very useful metric because it takes the load and source mismatch into account.

2.3.5 Efficiency

There are multiple ways to define efficiency in a power amplifier. Drain efficiency describes the ability to convert DC power to RF power.

$$\eta = \frac{P_{out}}{P_{DC}} \tag{2.11}$$

Power added effiency also includes P_{in}, i.e. the gain, in the equation, resulting in a more accurate result in low gain amplifiers compared to (2.11).

$$\text{PAE} = \frac{P_{out} - P_{in}}{P_{DC}} \tag{2.12}$$

This relation shows that an amplifier will work most efficiently close to its compression point as shown in figure 2.3.

2.3.6 Linearity, Error Vector Magnitude

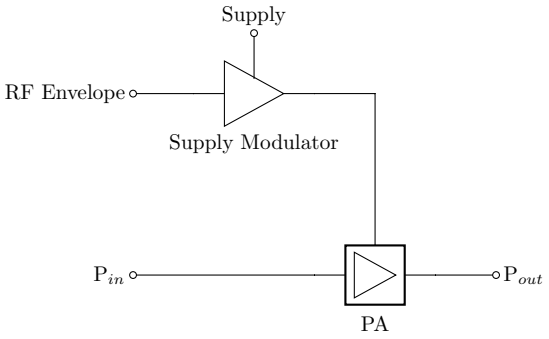
A common linearity measurement method in a modulated transceiver system is the error vector magnitude (EVM). Considering a received constellation of I and Q samples, the ratio of the received sample to the ideal sent sample is the error vector magnitude. Which mathematically can be described as

$$\text{EVM} = \sqrt{\frac{P_{error}}{P_{ref}}} \tag{2.13}$$

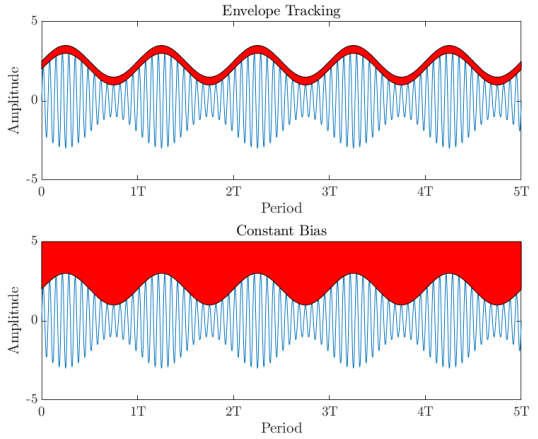
2.4 Efficiency and Linearity Enhancing Techniques

2.4.1 Envelope Tracking

The envelope tracking technique is a method to increase efficiency in a RF transmitter by dynamically varying the drain bias of the power transistor. This is done to keep the power amplifier in a region of compression, where it is the most efficient and at the same time minimizing the loss due to dissipated power. This principle is shown in figure 2.4.



(a) Envelope tracking block diagram



(b) Simplified waveforms showing the amount of dissipated power in the form of heat in the red areas

Figure 2.4: Envelope tracking principle shown by diagram and waveform

The supply modulator, or the tracking circuit, must have high bandwidth capabilities to be able to modulate the drain voltage correctly. The theoretical bandwidth of the envelope of a signal is infinite, however in practice the tracker must be able to reach several times the bandwidth of the signal itself, typically 4-5 times. A general envelope tracking polynomial function of n'th order could be

$$V_D = a_n V_{in,env}^n + a_{n-1} V_{in,env}^{n-1} + ... + a_0 \tag{2.14}$$

2.4.2 Power Envelope Tracking

Power Envelope Tracking (PET) is a new promising efficiency and linearity enhancing technique that builds upon classical envelope tracking. Power envelope tracking differentiates itself from conventional envelope tracking in that the drain voltage function is based on the *power* of the RF envelope, not the voltage. A first order power envelope tracking function would be

$$V_D = a_1 V_{in,env}^2 + a_0 \tag{2.15}$$

The advantage of PET is to significantly reduce the spectrum of the drain voltage by only using even ordered polynomials of the envelope power, at a small cost in performance. Further reading on the PET technique can be found in [7].

2.5 Calibration

Calibration is an important step in any small signal measurement setup in the radio frequency domain. For good results calibration is needed to remove systematic and drift errors in the setup. For conventional devices using coaxial interfaces calibration techniques like the SOLT (Short-Open-Load-Through) is popular. However, for DUTs not connecting to a coaxial interface a common calibration method is the LRRM (Line-Reflect-Reflect-Match) which can be used for on-wafer calibration with coplanar probes, used for example with MMICs. By performing calibration *on the wafer* itself, very high accuracy can be achieved. LRRM uses a reference calibration substrate with on-wafer features for the through (line), short (reflect) and load (match) cases. The open circuit (reflect) part is simply lifting the coplanar probes a set height off the waver. Keysight [3] offers a great application note for further diving into calibration of VNAs (Vector Network Analyzer).

CHAPTER 3

GAN MMIC COMPONENTS CHARACTERIZATION

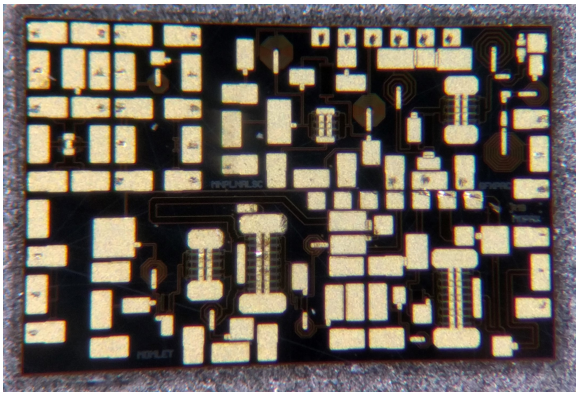


Figure 3.1: Photo of GaN MMIC through microscope lenses

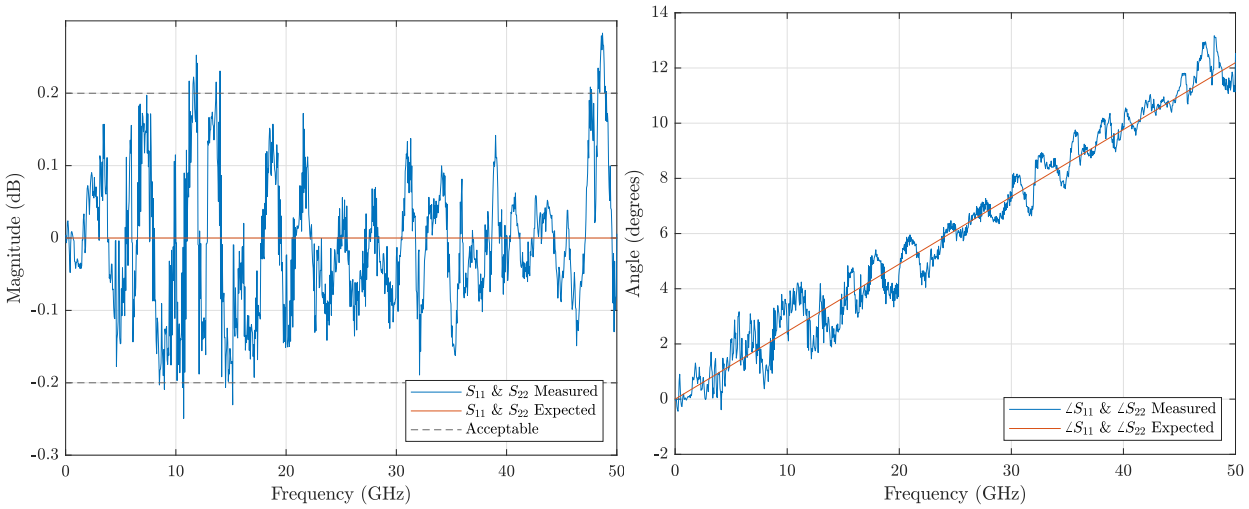
This chapter will present the characterization of the manufactured GaN MMIC and compare the measured results to the manufacturer's Advanced Design Suite (ADS) [1] model. A photo taken through the microscope lens of the 3 mm x 2 mm chip is shown in figure 3.1. The passive and active components relevant for this thesis is in the top left corner and the LNA is seen in the top middle section. The layout can also be seen in the appendix A.

3.1 Passive Structures

A characterization of the passive structures on the MMIC is a great way to verify circuit element functionality in the other larger structures and circuits on the chip. By having a verified circuit simulation model other elements affecting circuit performance can be found.

3.1.1 Verification of Calibration

The calibration method used is LRRM which gives on-wafer reference planes for the measurement probes. The software used in calibration and measuring small signal performance of the MMIC is WinCal XE [6] which contains model parameters for the LRRM calibration substrate and the probes used. By knowing these parameters the software can verify the quality of the calibration, which is essential feedback for the user. The verified calibration data is shown in figure 3.2.



(a) Magnitude **(b)** Phase

Figure 3.2: Passive calibration showing magnitude and phase difference from calibration to ideal model

3.1.2 Open Circuit

The open circuit and its physical implementation is shown figure 3.3.

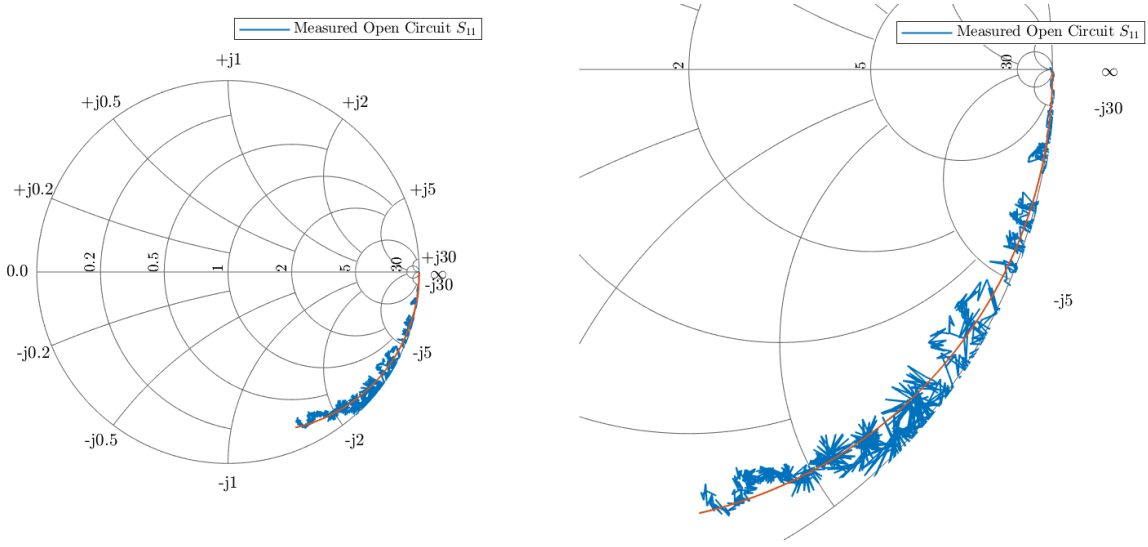
(a) Circuit equivalent **(b)** Physical implementation

Figure 3.3: Open circuit

The open circuit passive structure is essentially the probe points used on the MMIC. The physical implementation in figure 3.3 shows the coplanar structure of the probes using a GSG (Ground-Signal-Ground) configuration with purple circles indicating vias to the ground plane. The probe pads' parasitics can be seen as a plate capacitor, modelled by equation (3.1), in addition to a slight loss and inductance.

$$C = \frac{\epsilon_r \epsilon_0 A}{d} \tag{3.1}$$

By applying the values $\epsilon_r = 10.2$, $\epsilon_0 = 8.85 \cdot 10^{-12}$ F/m, $d = 100\mu m$ and $A = 100\mu m \cdot 200\mu m$. This gives a capacitance of $C = 18$ fF. The measured results are shown in figure 3.4.



(a) Open circuit smith chart **(b)** Open circuit smith chart enlarged

Figure 3.4: Open circuit measurement and simulation

By experimentation the actual best fit model for the parasitics is found in figure 3.5, showing that the plate capacitor parasitics assumption is quite good, being off by a factor of ≈ 2.

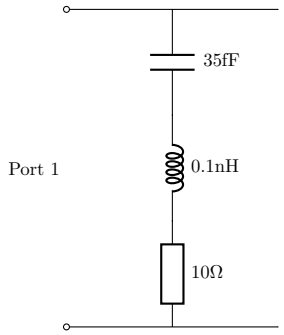
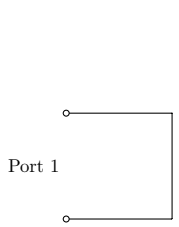


Figure 3.5: Open circuit pad parasitics

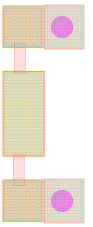
This open circuit probe point model will be used in the rest of the characterization.

3.1.3 Short Circuit

The short circuit and its physical implementation is shown in figure 3.6 and the measurements and simulation is shown in figure 3.7.

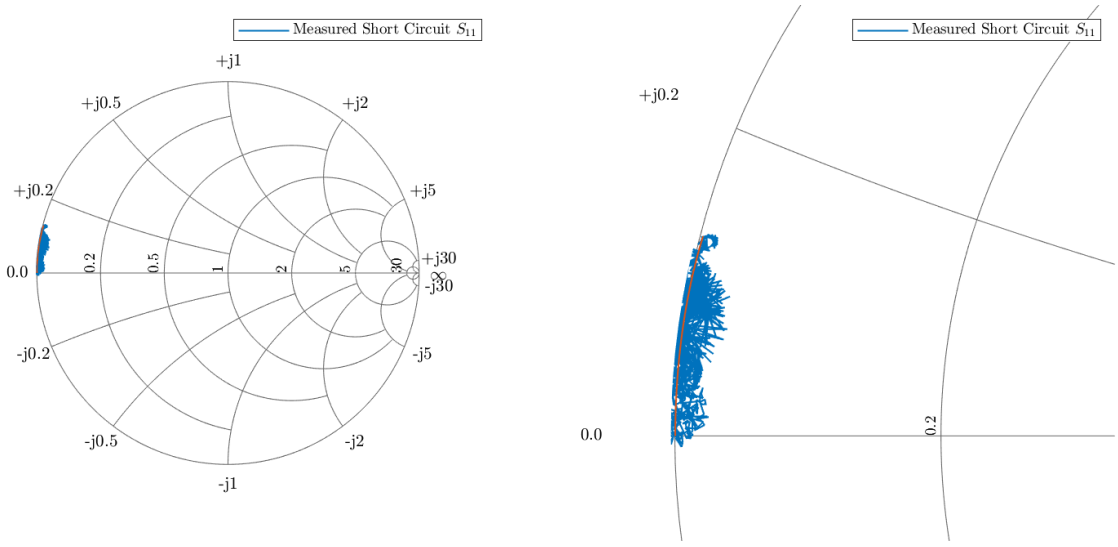


(a) Circuit equivalent



(b) Physical implementation

Figure 3.6: Short circuit



(a) Short circuit smith chart

(b) Short circuit smith chart enlarged

Figure 3.7: Short circuit measurement and simulation

The results show an inductive effect as expected from a short circuit and a good fit of the simulation to the measured data.

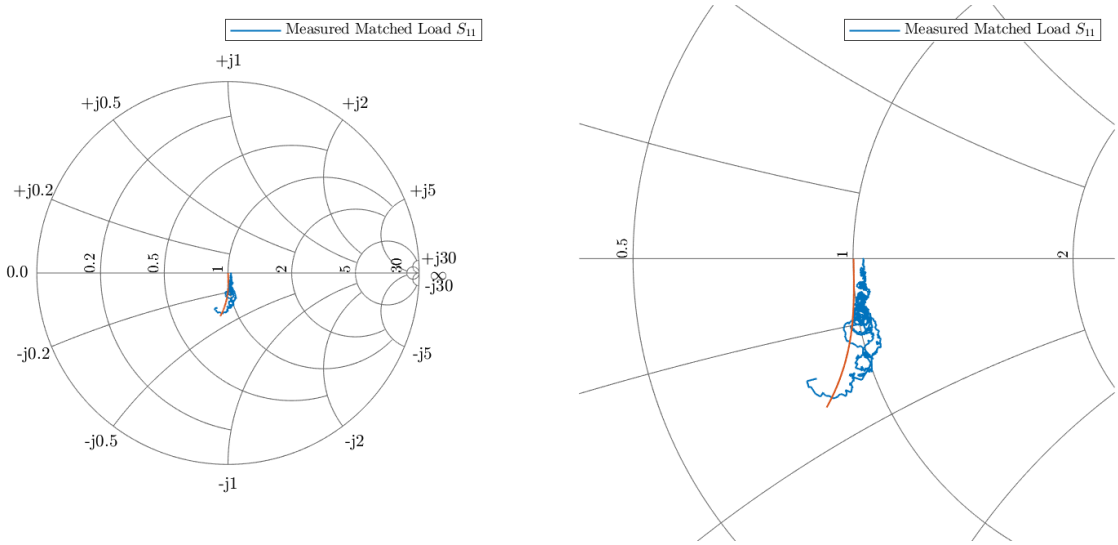
3.1.4 Matched Load

The matched load and its physical implementation is shown in figure 3.8 with its impedance equal to the characteristic impedance, Z_0. The physical implementation consists of two 100 Ω resistors connected in parallel to the two coplanar ground points.

(a) Circuit equivalent

(b) Physical implementation

Figure 3.8: Matched load



(a) Matched load smith chart

(b) Matched load smith chart enlarged

Figure 3.9: Matched load measurement and simulation

The simulated and measured results are shown in figure 3.9. The results show a quite good fit of the model to the measured data, with the measured low frequency normalized impedance at $z = 1.03$ yielding an actual impedance of $Z = z \cdot Z_0 = 51.5\Omega$.

One might expect that the circuit would show an inductive effect due to the physical length of the resistors, but the probe parasitics causes the equivalent circuit to become capacitive.

3.1.5 Capacitor

The capacitor and its physical implementation is shown in figure 3.10.

(a) Circuit equivalent

(b) Physical implementation

Figure 3.10: Series capacitor

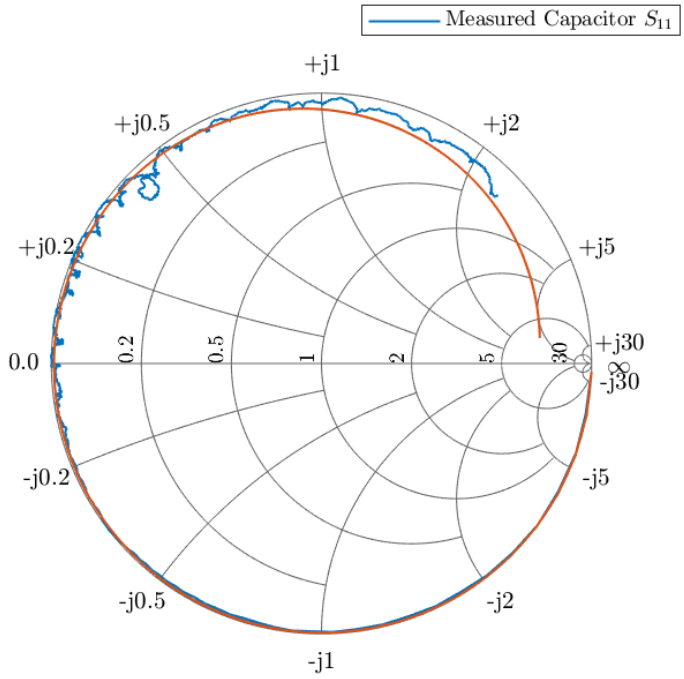
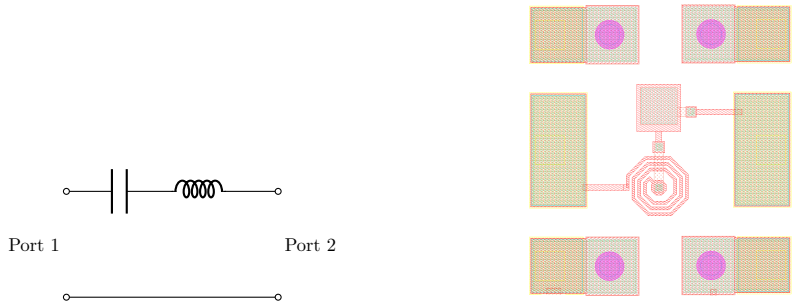


Figure 3.11: Capacitor measurement and simulation

The results of the measurements and the simulation is shown in figure 3.11. The results follow the expected trajectory around the Smith chart from an open circuit through a parallel resonance and into the inductive area. The measured capacitor crosses the real line, or hits the resonance, at 6 GHz to 6.5 GHz. A slight interval is used as the measurement has a curl at the crossing. The simulated data however, crosses clearly at 6 GHz. The lossy effect of the parasitic probe point seems to fit well as the frequency increases over the resonance.

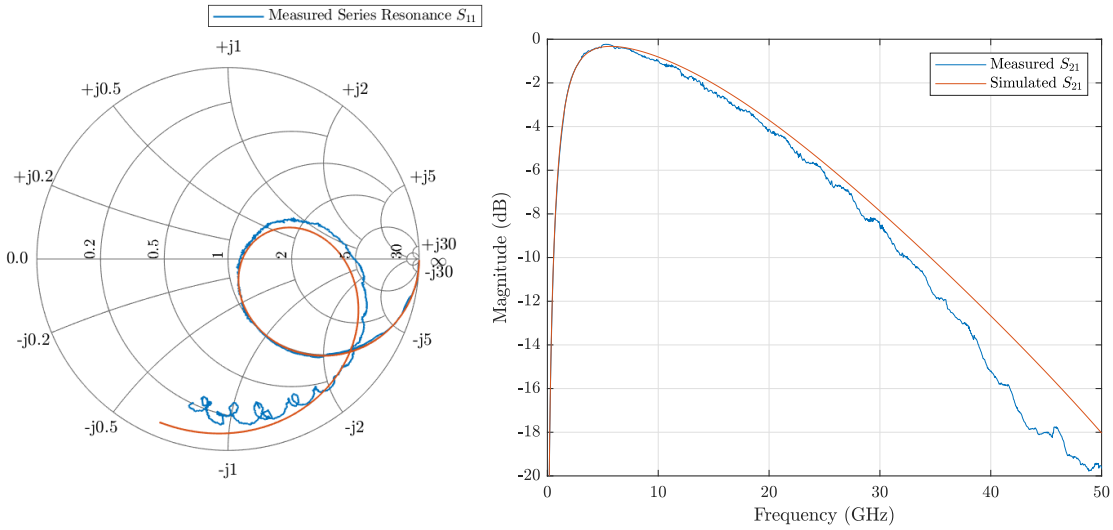
3.1.6 Series Resonance

The series resonance and its physical implementation is shown in figure 3.12 below.



(a) Circuit equivalent **(b)** Physical implementation

Figure 3.12: Series resonance



(a) Smith chart series resonance S_{11} **(b)** Magnitude series resonance S_{21}

Figure 3.13: Series resonance measurement and simulation

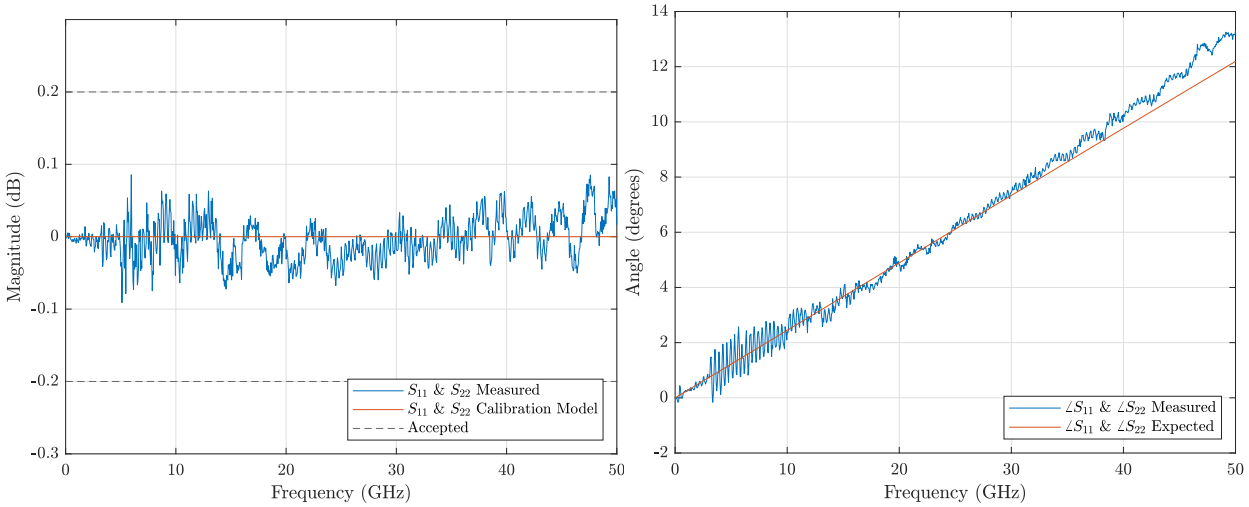
The results of the measured and simulated series resonance is shown in figure 3.13. As the plots show the simulated series resonance follows the measured resonance very good at least up to around 30 GHz. As a series resonance a perfect ideal circuit would have crossed through the center of the Smith chart. But as the magnitude plot shows, a slight loss is observed at the peak. The loss is due to the transmission lines into and out of the resonance circuit, in addition to other parasitics. From the magnitude plot it is seen that the loss is 0.3 dB, with a deviation between simulated and measured circuit in the magnitude of 0.05 dB.

3.2 Active Structure

The active structure of the GaN MMIC characterization circuits consist of a two finger transistor. To verify functionality of the larger systems on the die, only verifying passive structures' models are not enough. The following subsections will look into this transistor.

3.2.1 Verification of Calibration

Due to these measurements being made at a different time than the passives, a new calibration is necessary. The new calibration verification through Wincal XE is shown in figure 3.14 below. It is clear that this calibration is better than the one used during the passive characterization, both in terms of magnitude error and phase error.



(a) Magnitude

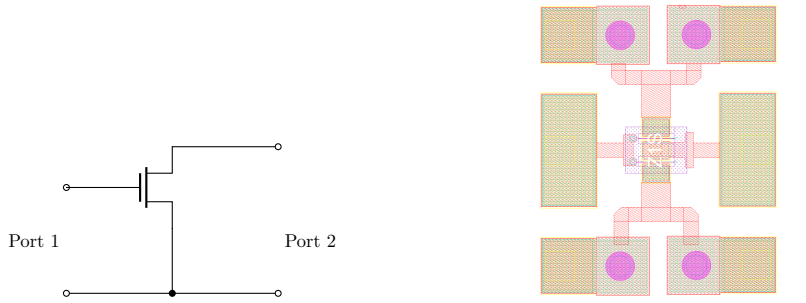
(b) Phase

Figure 3.14: Active calibration showing magnitude and phase difference from calibration to ideal model

3.2.2 The Two Finger Transistor

The transistor and its physical implementation is shown in figure 3.15. To function the transistor needs to be biased. This is achieved by applying bias externally to the network analyzer which internally sets DC levels on its ports. The same probe parasitics model is used in the simulation of the transistor, as in the passive structures.

The measured and simulated results of S_{21} through the transistor over a variety of bias points are shown in figure 3.16 below. The results show that the highest gain appears at a bias of 20 mA, meaning that the higher bias of 40 mA is too



(a) Circuit equivalent **(b)** Physical implementation

Figure 3.15: Transistor

high and leads to gain collapse. Notice that the simulated gain at 40 mA bias is lower than the simulated gain at 8 mA bias, even though the measured gain at 40 mA bias is higher than at 8 mA bias. This is probably due to the sensitivity at a too high bias, leading to erronous measurements of bias current with only one significant digit in the power supply during measurements. The simulated data can of course have higher number of significant digits. It is also seen that at lower frequencies the measured gain is higher than the simulated across all bias points. The crossing of the measured and simulated curves are in the interval 12 GHz to 21 GHz. As mentioned in the passive characterization the model used seems to differ significantly as the frequency crosses 30 GHz, this is also seen here.

3.2.3 Low Noise Amplifier

A small signal gain measurement of the LNA at its designed bias and drain voltage is shown in figure 3.17. The measured gain is at its peak at 2.35 GHz which is missed by 200 MHz to the designed simulated curve which has its peak at 2.15 GHz. The measured gain is close to the designed peak, a difference of only 0.2 dB. There is however a steep 5 dB gain drop between 2.5 and 3.5 GHz.

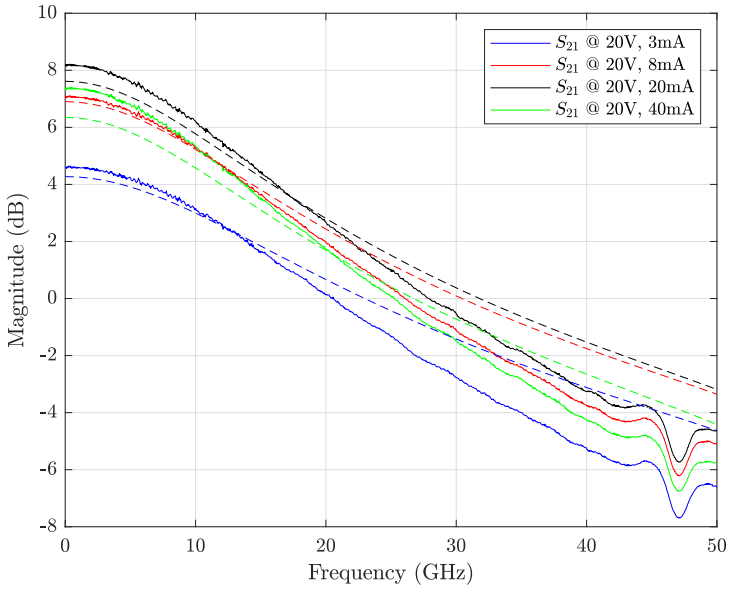
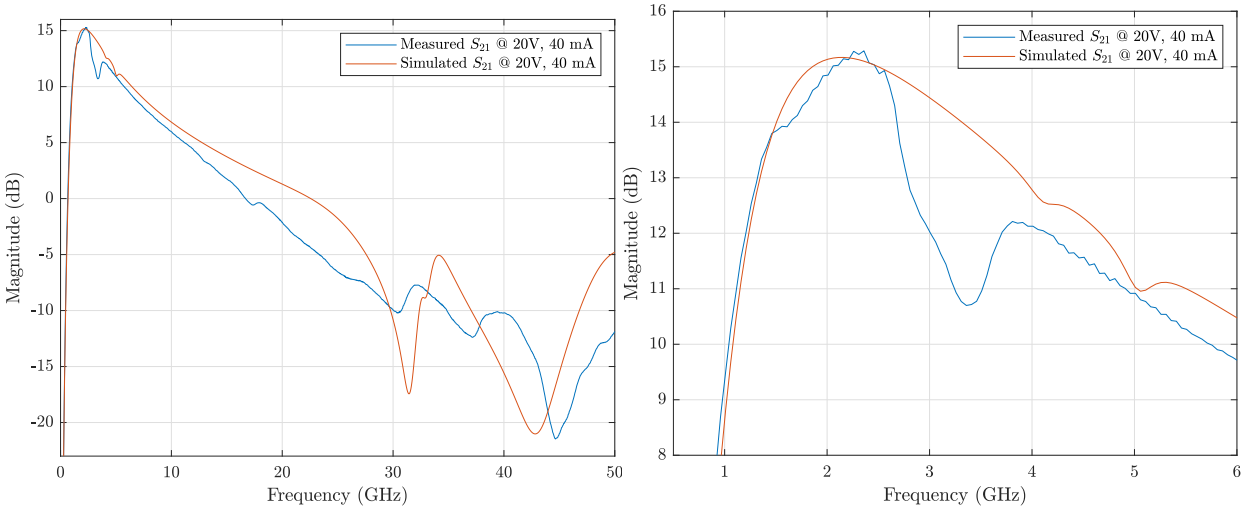


Figure 3.16: Single transistor small signal parameter swept over bias points, dotted lines are simulated



(a) Complete LNA gain

(b) Gain over designed bandwidth

Figure 3.17: Small signal gain of low noise amplifier

CHAPTER 4

ENVELOPE TRACKING IMPLEMENTATION

This chapter shows the method of obtaining the tracking functions needed for the drain voltage supply modulator in an envelope tracking transmission system.

4.1 Large Signal Measurement Setup

To find the correct tracking functions a power sweep is necessary over the amplifier's gate and drain voltages. By this method a three dimensional data set is obtained in which one can find optimal points for PAE and flat gain as a function of the gate and/or drain voltage. The large signal measurement setup is shown in figure 4.1. Given as both the GaN LNA and the GaAs amplifier has similar output power levels, the measurement setup is the same for both. All losses are measured and corrected at the respective operating frequencies of the amplifiers, 2.3 GHz for the GaN LNA and 5.5 GHz for the GaAs PA.

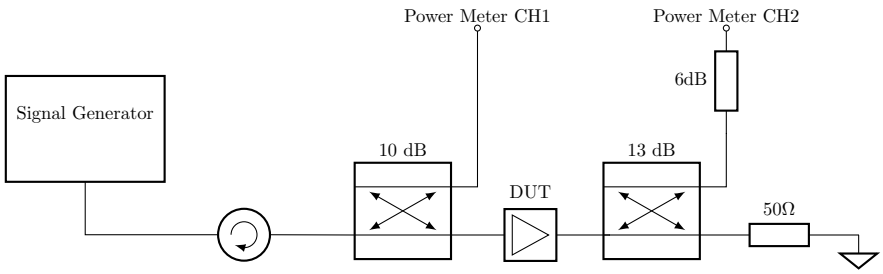
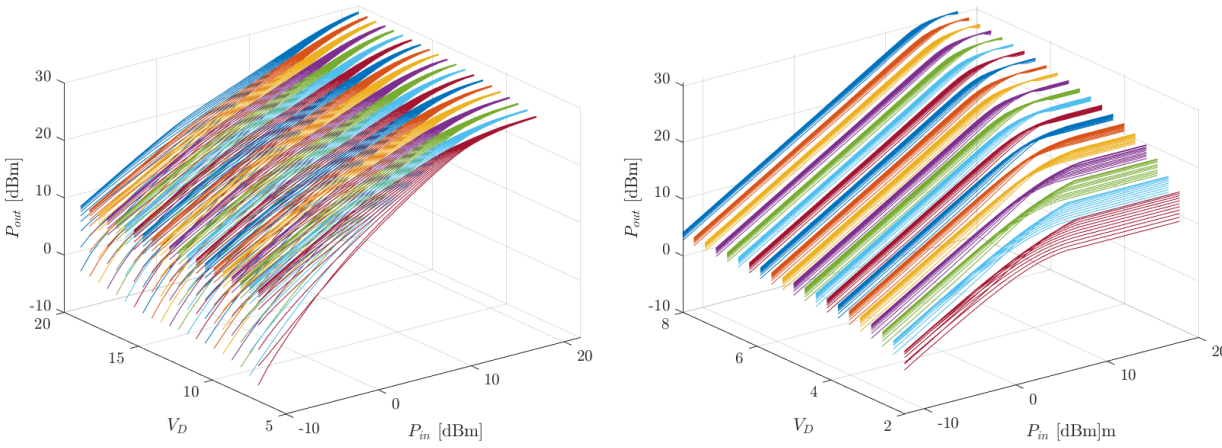


Figure 4.1: Large signal measurement setup



(a) GaN

(b) GaAs

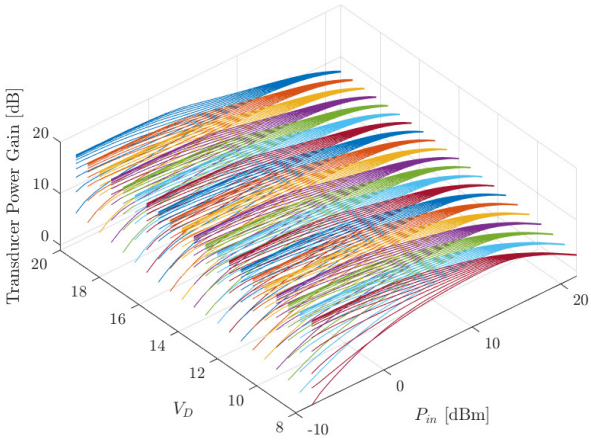
Figure 4.2: V_G, V_D, P_{in} sweep for P_{out}

4.2 Power Sweep

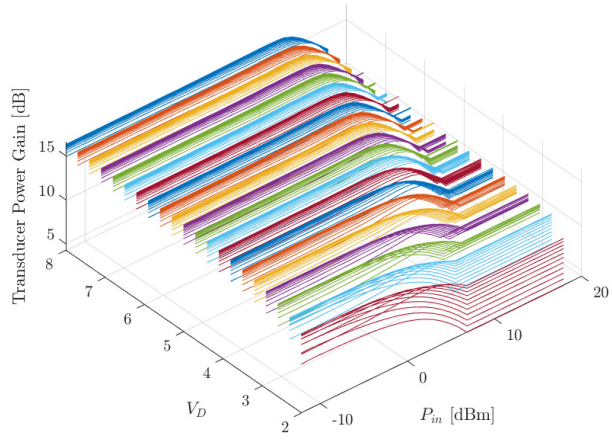
The power in/power out sweep is shown in figure 4.2. The same colored plots show different gate voltages. A characteristic easily seen is the gain drop for low bias in the GaN process. This leads to a lower output power when the GaN amplifier is not driven significantly. The gain is shown in figure 4.3. Notice the effect at lower input power levels.

The same effect of gain breakdown is seen in the GaAs amplifier as well, but is significantly smaller. The effect is almost negligable if one is not comparing the lowest drain voltage to the highest. The second effect seen in the gain is that the GaN amplifier seems to enter into compression at approximately the same input power. The GaAs amplifier gradually enters compression as the input power increases with drain voltage.

The resulting PAE for both amplifiers is shown in figure 4.4. Here the above mentioned compression differences affect the PAE. Notice the GaN PAE increases as the drain goes *down*. This effect is in contrast to the GaAs amplifier's PAE curves increasing with drain voltage and input power. The GaN amplifier's differing performance is naturally due to its low noise optimization, additionally leading to the lower over all maximum efficiency at 25 % to 30 % for single tones. This will of course affect the quality of comparison in envelope tracking between these two processes.

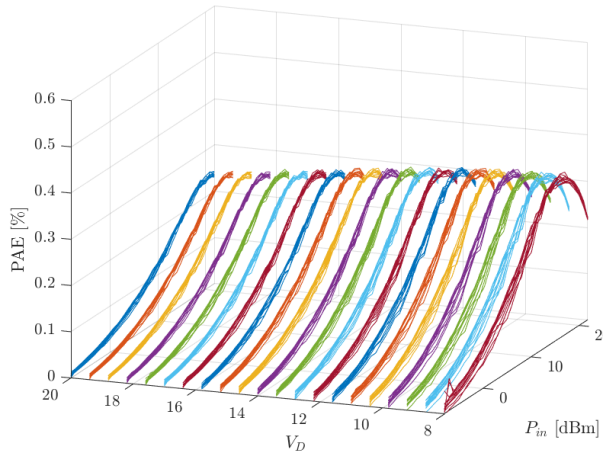


(a) GaN

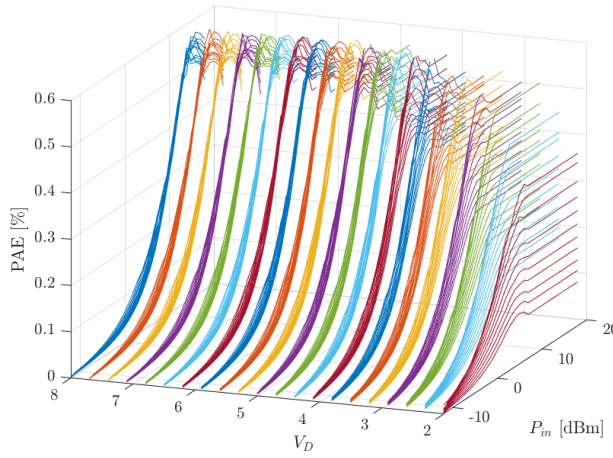


(b) GaAs

Figure 4.3: V_G, V_D, P_{in} sweep for gain



(a) GaN



(b) GaAs

Figure 4.4: V_G, V_D, P_{in} sweep for PAE

4.3 Envelope Tracking Trajectory Selection

From the measured sweep data from the previous section one can now look for points of maximized PAE and flat gain. For simplicity the gate bias is set constant, although it is possible to track both gate and drain voltages at the same time for some (possibly) increased performance. The GaN amplifier is set to a bias of 10 mA, slightly lower than original LNA designed bias of 20 mA. This equals quite deep class AB operation. This is to increase flat gain performance at lower input powers. The GaAs amplifier is set to a bias of 100 mA, also in class AB operation.

In this thesis four different tracking functions are explored for two cases of optimization. Those are:

- Max PAE conventional ET
- Max PAE PET
- Flat Gain conventional ET
- Flat Gain PET

The flat gain levels for the GaN and GaAs amplifiers are 10 dB and 15 dB respectively.

4.3.1 GaN Tracking Functions

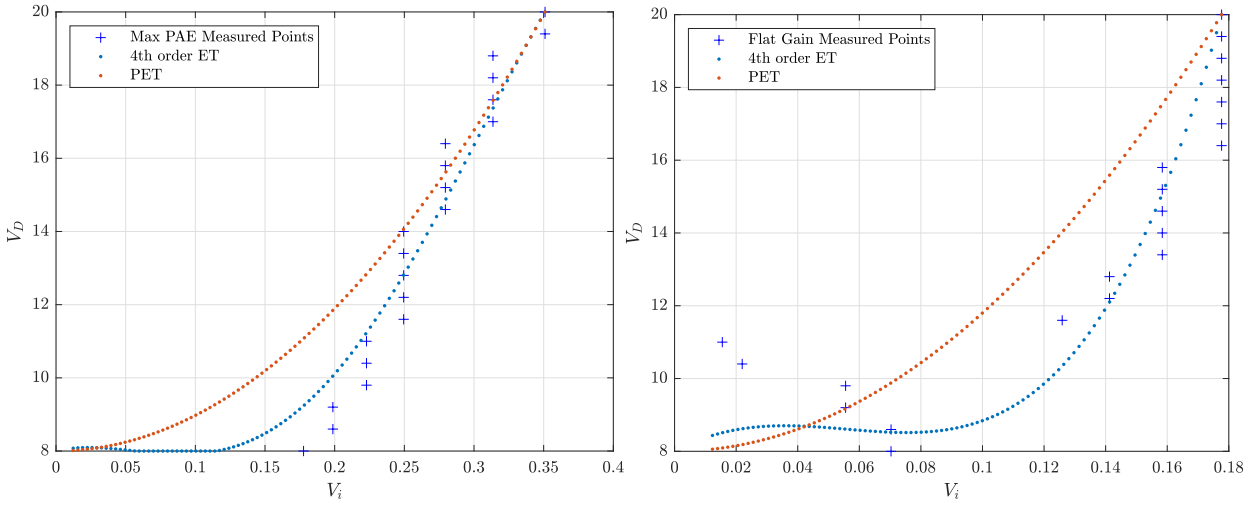
The GaN amplifier's tracking functions are shown in figure 4.5, with $V_i = \sqrt{P_i}$. The crosses shows the optimal points for maximum PAE and flat gain. Notice that in the flat gain figure, there are crosses above 10 V. This is simply due to the gain collapse at lower input powers. For a better fit of the most important points on higher input levels, those first crosses are ignored.

The conventional envelope tracking functions for max PAE and flat gain are both realized using a fourth order polynomial on the form

$$V_D = a_4 V_i^4 + a_3 V_i^3 + a_2 V_i^2 + a_1 V + a_0 \tag{4.1}$$

where the coefficients are found using simple curve fitting techniques in Matlab. The PET tracking functions are found accordingly to earlier described theory.

The 4th order ET polynomial will fit the optimized points best, but the PET is not that far off. Some slight clipping is seen in the max PAE function as a consequence, which the PET avoids.



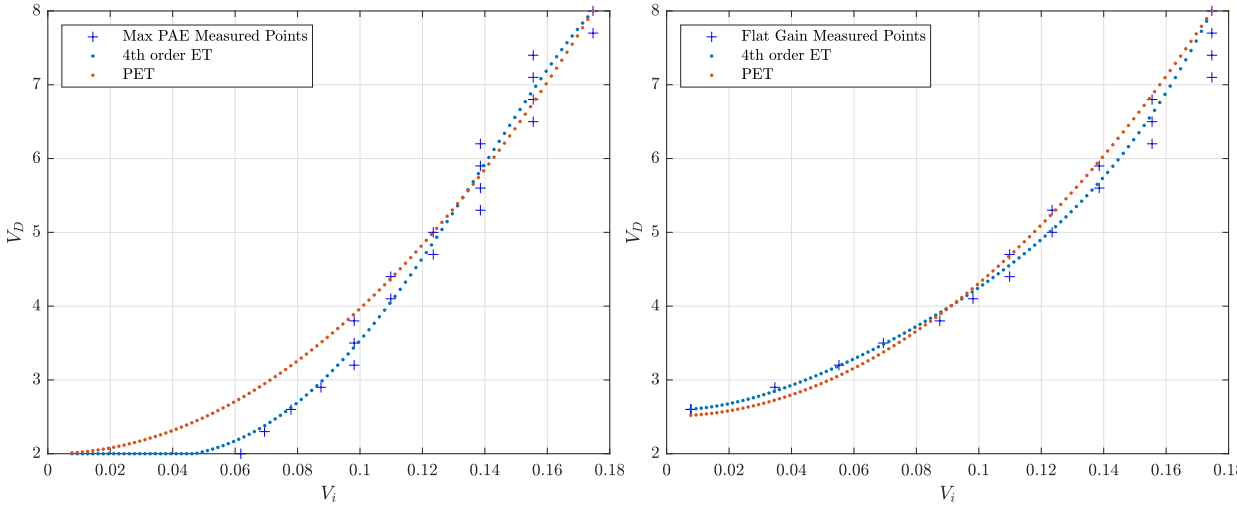
(a) Maximum PAE trajectories

(b) 10 dB flat gain trajectories

Figure 4.5: Interpolated tracking functions from measured data points

4.3.2 GaAs Tracking Functions

The GaAs tracking functions are found the same way as the GaN functions, with the same 4th order polynomial in equation (4.1). The tracking functions are seen in figure 4.6. The figure shows that the PET and ET functions are really close, with some slight clipping in the ET function.



(a) Maximum PAE trajectories

(b) 15 dB flat gain trajectories

Figure 4.6: Interpolated tracking functions from measured data points

CHAPTER 5

ENVELOPE TRACKING RESULTS

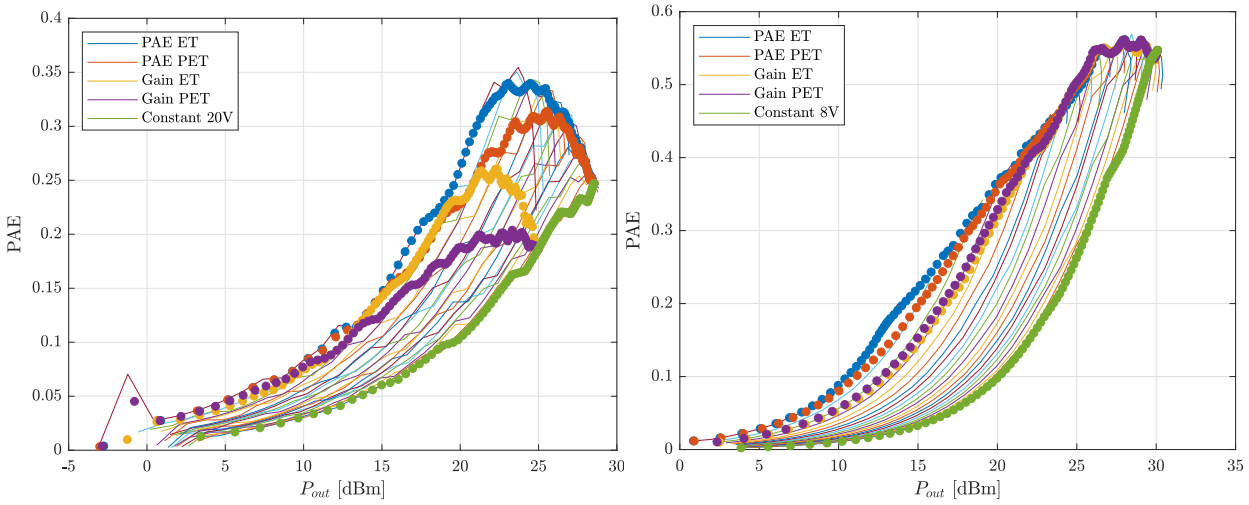
The results in this chapter are simulated from the tracking functions found in the previous chapter. A constant drain voltage level is also highligheted in the result to compare to a normal operating amplifier. The bold curves show how the functions "move" in the constant gate voltage dataset for a given output or input power.

5.1 PAE

The resulting power added efficiency for the different tracking functions is shown in figure 5.1. As seen in the figure the GaAs amplifier has quite similar PAE tracking performance for the different functions peaking at 55 % and sustaining this level 6-8 dB into back-off. However, the GaN LNA shows greater discrepencies in PAE curves. The PAE ET follows the optimal PAE points and performs the best, and is able to sustain a PAE just short of 30 % into a few dB back-off.

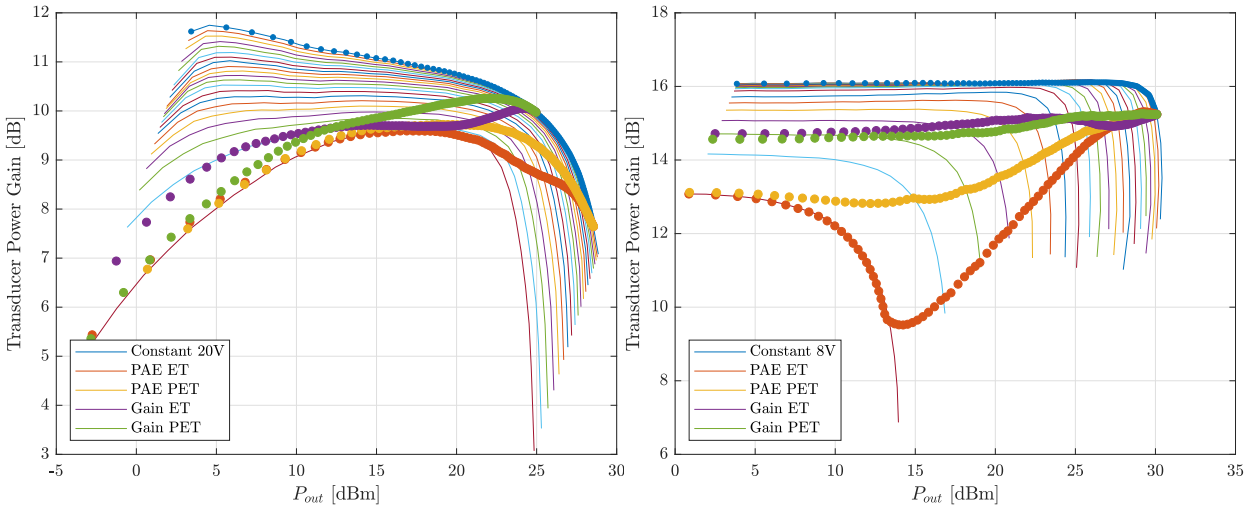
5.2 Gain

The resulting gain for the different tracking functions is shown in figure 5.2. In the GaN amplifier the tracking functions follows the gain breakdown at low output levels. The flat gain optimized tracking functions shows a somewhat poor performance, not being able to hold the 10 dB gain value in back-off. The GaAs amplifier however manages to hold a constant 15 dB flat gain in back-off. The Gain ET curve has a dip at approximately 27 dBm output power. The PAE PET curve shows very poor performance dropping from 15 dB to 10 dB as the output power is reduced.



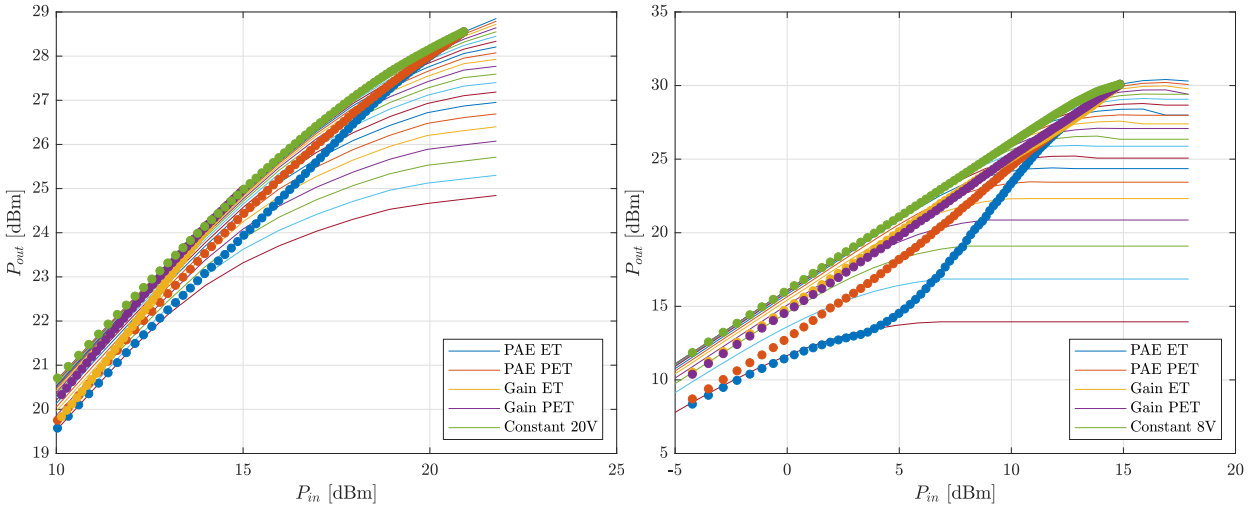
(a) GaN PAE **(b)** GaAs PAE

Figure 5.1: Resulting PAE from different tracking functions



(a) GaN Gain **(b)** GaAs Gain

Figure 5.2: Resulting gain from different tracking functions



(a) GaN P_{out} **(b)** GAs P_{out}

Figure 5.3: Resulting P_{out} from different tracking functions

5.3 Output Power

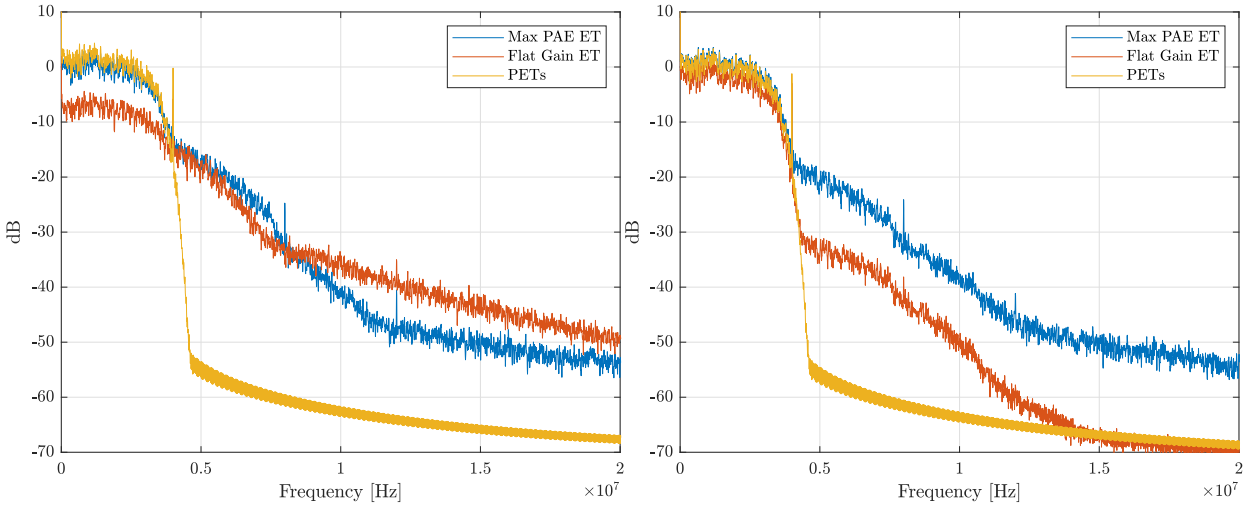
The resulting ouput power for the different tracking functions is shown in figure 5.3. The GaN LNA has quite similar output power trajectories across all tracking functions with the PAE ET curve suffering the most at lower input powers. The GaAs amplifier shows the same lagging performance of the PAE ET curve.

5.4 Drain Voltage Spectrum

The resulting drain voltage spectrum under a 4 MHz 16-QAM signal for the different tracking functions is shown in figure 5.4. The filter used is a raised cosine filter with a roll-off factor of $\alpha = 0.22$. These results shows the raw performance improvement of the PET technique over the ET, with a dramatically better drain voltage spectrum. A typical figure of merit for drain spectrum performance is the bandwidth at -40 dB. The results summarized in figure 5.1.

Table 5.1: Drain voltage spectrum -40 dB bandwidths

	Max PAE	Flat Gain ET	PETs
GaN	9 MHz	13 MHz	4.4 MHz
GaAs	10 MHz	8 MHz	4.4 MHz



(a) GaN Drain Spectrum

(b) GaAs Drain Spectrum

Figure 5.4: Resulting drain spectrum from different tracking functions

5.5 QAM Simulation

To test the performance of the found tracking functions, the same 4 MHz 16-QAM signal is applied. By using the trajectories found, simulated results in *average* P_{out}, PAE and gain, in addition to EVM is found for the GaN and GaAs amplifiers as shown in tables 5.2 and 5.3. Notice that since no phase data have been used, the EVM is only a result of AM-AM distortion.

Table 5.2: Results from GaN drain tracking simulations

	Po [dBm]	Gain [dB]	PAE [%]	EVM [%]
Max PAE	23	8.9	30	2.9
Max PAE PET	23.4	9.3	27.7	2.9
Flat Gain 10dB	18	10.1	11.3	0.5
Flat Gain 10dB PET	18.4	10.1	11.3	1.8
Constant 20V	24	9.8	17.6	4.6

Table 5.3: Results from GaAs drain tracking simulations

	Po [dBm]	Gain [dB]	PAE [%]	EVM [%]
Max PAE	21.7	13.7	42.9	12.5
Max PAE PET	22.5	14.4	44.5	5
Flat Gain 15dB	23.1	15	45.1	0.8
Flat Gain 15dB PET	23.2	15.1	45.8	1.4
Constant 8V	24.1	16	23.2	0.3

CHAPTER 6

DISCUSSION

6.1 GaN MMIC Characterization

The GaN MMIC characterization shows good results and verifies the given computer model as a good approximation to the circuit's measured performance. By verification of the calibration and producing a good model for an open circuit for probe parasitics the simulated data fits the measured circuit well. Even though the passive calibration seen in figure 3.2 shows slight deviances to ideal performance and is locally above accepted limits, the difference is so small that it doesn't affect the end result in a significant way.

The assumption of a parallel plate capacitance effect on probe parasitics is a good approximation. Missing by a factor ≈ 2 is good considering an estimate is not made for the coplanar probe's ground fingers, which would add some additional capacitance.

As seen in the physical implementation and layout of figure 3.10 and figure 3.12 the circuit structures input and outputs are not centered on the probe points. This causes slightly longer distances, but this will not have *major* impact on circuit performance. Consider a 10 GHz frequency giving a 3 cm wavelength. The distance errors are in the order of $\approx 30\mu m$. The length error is a thousandth of the wavelength. This ratio lowers at lower frequencies, but increases at higher frequencies. Since this is a *characterization* of a semiconductor process model accuracy is key, and every source of error must be considered.

It is shown in the resonance circuit in figure 3.13 and the two-finger transistor in figure 3.16 that the measurement results deviate significantly from the simulation as the frequency passes 30 GHz. It is clear that the probe parasitic model is

too simple as the frequency increases. This is seen as a "kink", or sharper turn of trajectory in the smith chart, which appears in measurement data of the open circuit in figure 3.4. The same kink is seen in the matched circuit in figure 3.9 as the simulated curve deviates from the measured. If a higher ordered probe parasitic model were made, greater accuracy at the highest frequencies would be made.

The transistor model UMS provides is at its most accurate between the frequencies 10 GHz to 22 GHz as seen in 3.16, which fits UMS' claim of process optimization up to 20 GHz. At lower frequencies the simulated gain is higher than the measured, leading to that the model is conservative at lower frequencies giving some extra design margin.

The significant gain drop of the LNA seen in figure 3.17 is probably not due to a component error in the process, as has been proved the component models provided are very good! The chance of this error being due to a layout fault seems probable. As circuit features are closely placed to minimize total area used, non-ideal coupling effects could become apparent. This is a hypothesis that could be explored by setting up an EM-simulation on the circuit.

6.2 Envelope Tracking

The envelope tracking simulation results shows a great contrast in performance between the two amplifiers. Due to the low noise optimized matching of the GaN amplifier, significantly lower efficiency levels are reached. Table 5.2 and table 5.3 shows that a 4 MHz 16-QAM modulated signal would reach an average PAE of 30 % with a PAE maximized ET tracking function, while the GaAs amplifier reaches 45.8 % on a flat gain optimized PET tracking function.

Because the GaN low noise amplifier is used as a conventional power amplifier driven into compression, the resulting distortion levels are very high. A LNA is never driven into compression because it significantly ruins the integrity of the amplified signal. The EVM is at 4.6 % for the LNA at constant drain voltage compared to 0.3 % for the GaAs amplifier at constant drain voltage. Across the different tracking functions the distortion naturally deviates. Notice for example the very non-linear gain of the GaAs PAE ET curve in figure 5.2 leading to poor EVM (12.5 %) for the modulated QAM-signal.

It is not possible to directly compare the processes on the basis of the envelope tracking simulations, but the differences in performance of ET and PET is easily seen in figure 5.4. The PET technique's strength is the reduction of the drain modulators bandwidth at equal performance or small costs in PAE and/or linearity. The drain voltage spectrum is dependent on the interpolated tracking functions from figure 4.5 and figure 4.6.

The GaN flat gain ET has 8 dB lower spectrum at low frequencies due to the

smaller dynamic range of the tracking function. At low input envelope levels the tracking function does not even reach the lowest point of 8V. The GaN PAE ET function shows clipping at 8V in the tracking function, this leads to increased tracking bandwidth, but still a smaller effect than the first and third order products in the GaN flat gain ET function. In the GaAs drain spectrum the flat gain ET is so close to the PET that it is nearly the same, here the clipping effect in the PAE ET curve is significant enough to cause an increased tracking bandwidth.

CHAPTER 7

CONCLUSION

7.1 GaN MMIC Characterization

This thesis shows that the UMS provided computer simulation model is verified up to 30 GHz. By finding a reasonable model for probe parasitics several passive and active components are measured and compared to the simulation model. The transistor models provided show an optimal gain similarity in the range from 10 GHz to 22 GHz and gives a conservative estimate of the real performance at lower frequencies.

A LNA circuit is measured and is found to have great difference in gain in its designed bandwidth. As the circuit models used is verified by the characterization, it is possible that the layout of the amplifier is the root cause. However, this cannot be concluded until a proper EM-simulation is made on the circuit.

7.2 Envelope Tracking

The envelope tracking results shows that there is significant performance gains of tracking an envelope by dynamically modulating the drain voltage of a GaAs amplifier. This is in contrast a GaN amplifier which is matched optimized for low noise operation. This makes it difficult to make an apples-to-apples comparison of the two process technologies in regards to the envelope tracking efficiency and linearity enhancing technique.

The envelope tracking simulation results shows that the PET technique is a great trade-off of PAE and linearity for drain modulator bandwidth, allowing easier physical implementation with regards to circuit requirements. This thesis shows

that power envelope tracking is a viable efficiency and linearity enhancing technique for use in advanced telecommunication systems.

7.3 Future Work

There are several possibilities to build on the work made in this thesis. For example an EM-simulation on the GaN LNA could be made to conclude on the hypothesis of layout issues on the MMIC. In addition only simulation are made on the different envelope tracking functions. A natural step forward would be to design circuitry that could provide envelope tracking functionality to the amplifiers described in this thesis. Lastly, adding phase information in the simulations would give an increased accuracy of the distortion levels of the amplifiers, adding AM-PM errors. The simulations could also add different modulation techniques in addition to 16-QAM, such as OFDM and LTE.

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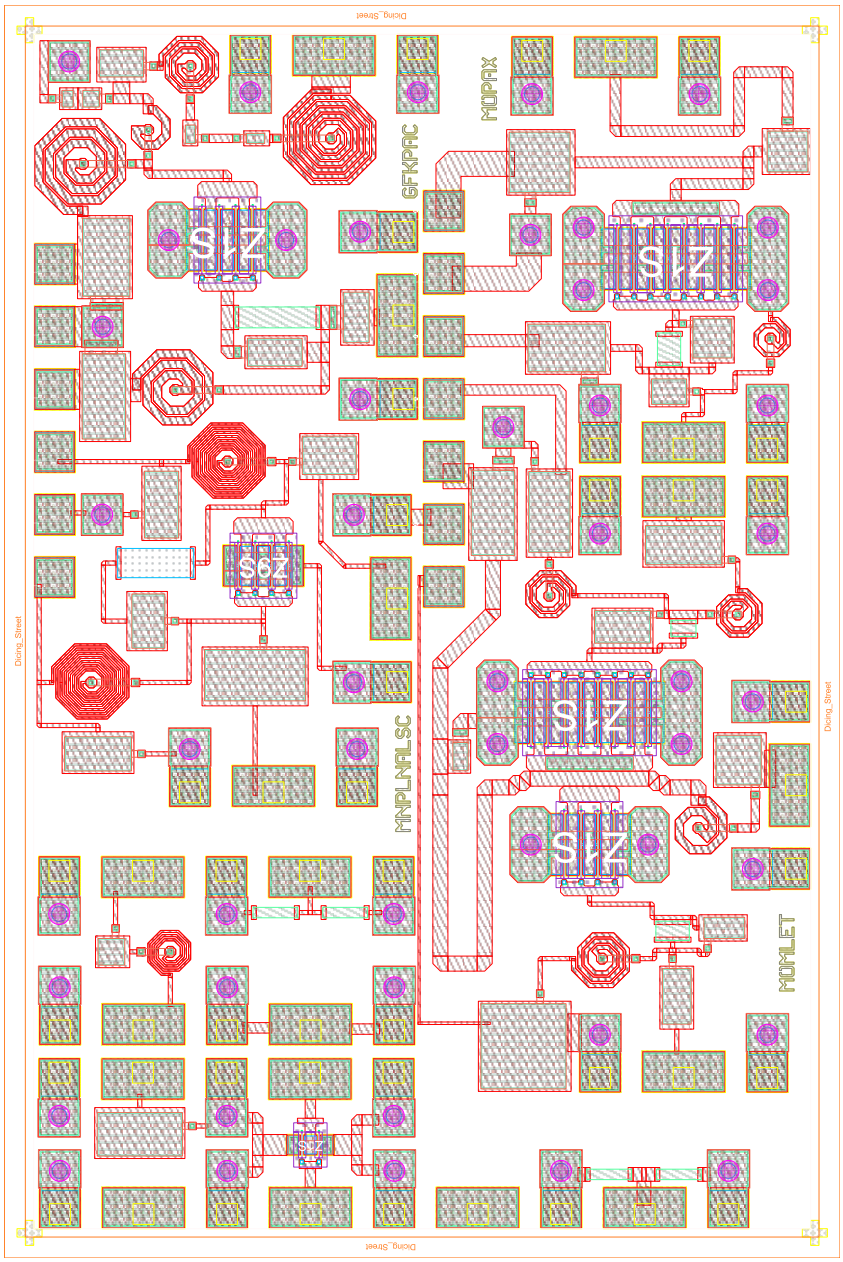
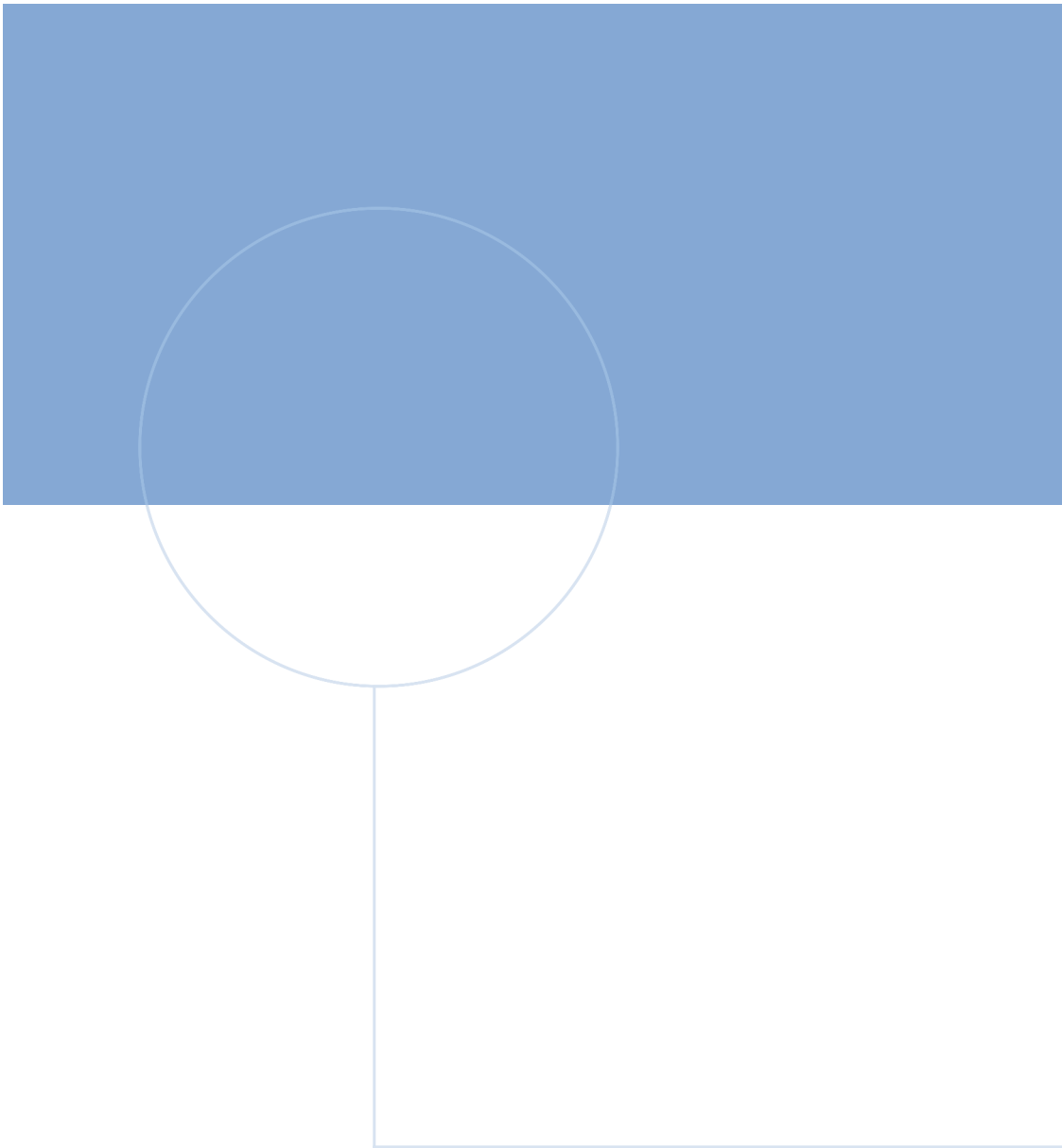
Appendix

Appendix A - GaN MMIC Layout





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