Carl Einar Hellenes

Construction of a Power Amplifier based on a newly developed Power Envelope Tracking (PET) of Gate and Drain

Master's thesis in MTELSYS
Supervisor: Olavsbråten, Morten
July 2019

Master's thesis

NTNU
Norwegian University of Science and Technology
Faculty of Information Technology and Electrical Engineering
Department of Electronic Systems

NTNU
Norwegian University of
Science and Technology

Carl Einar Hellenes

Construction of a Power Amplifier based on a newly developed Power Envelope Tracking (PET) of Gate and Drain

Master's thesis in MTELSYS
Supervisor: Olavsbråten, Morten
July 2019

Norwegian University of Science and Technology
Faculty of Information Technology and Electrical Engineering
Department of Electronic Systems

NTNU
Norwegian University of
Science and Technology

Dedicated to my Mother, Father and my brothers.
Thanks for always being there for me

Preface

This Master Thesis has been developed for the Department of Electronics Systems at NTNU with guidance from associate professor Morten Olavsbråten. The motivation behind this thesis was to design and produce an improved RF power amplifier. The amplifier is intended for the newly developed tracking technology Power Envelope Tracking (PET) of gate and drain. The amplifier uses the improved discrete gallium nitride high electron mobility transistor from Cree, called CG2H40010. Design and simulation is done with the software Advanced design systems (ADS) from Keysight.

Acknowledgment

I would like to thank my fellow students and classmates for many tough but good years together. It is the people around me that inspire me and push me to be better. I hope I can continue to be in such good company in my future endeavors. I would also like to thank my family and closest friends for supporting and helping me to push through, even when times have been though. And finally, I would like to thank my supervisor Associate Professor Morten Olavsbråten. You love to talk, and I love to listen. Thank you for all your valuable advice, knowledge and good talks along the way. I aspire to be as passionate about my work and learning as you.

Carl Einar Hellenes
Trondheim, July 2019

Summary

In this master's thesis a Radio Frequency Power Amplifier (RF PA) compatible with tracking technology has been designed and produced. The PA is designed as a class AB amplifier, with a bias current of 161 mA and a drain voltage V_d = 28 V. The PA has a center frequency at 2.2 GHz, with a bandwidth of 120 MHz. The highest small-signal gain in the bandwidth is about 17.3 dB with a 1 dB ripple. The maximum output power of the device is 41 dBm or 12.5 W, when the input power is 30.5 dBm. The Power Added Efficiency (PAE) of the device is 71.3% at max output power. The transducer power gain at the 1 dB compression point is close to 13 dB.

The PA has been measured with variable drain and gate bias. The data from these measurements have been used to create tracking functions for the tracking technologies Envelope Tracking (ET) and Power Envelope Tracking (PET). The tracking functions are made for constant gain and max PAE by controlling V_g and V_d. The constant gain achieved is about 10.5 dB transducer power gain. For max PAE, a higher efficiency is maintained over a bigger span of power compared to the PA without a tracker. The highest PAE achieved with tracking is 72.4%. The tracking functions are made in MATLAB. Physical tracking devices have not been tested with the PA. However, the tracking functions are assumed to be close to the behavior of the real thing.

During the design and prototyping process, it was discovered that the Microstrip Substrate (MSUB) model used for FR-4 was inaccurate. Therefore, a new MSUB was characterized. This led to modifications of the amplifier. For this reason, the final PA has not been properly measured for linearity (2-tone test) but is assumed to be close to simulations.

The amplifier was designed using the gallium nitride high electron mobility transistor CG2H40010 from Cree/Wolfspeed. The transistor is an improved version of the CGH40010F. The improvement claims have been validated with the results for PAE and small-signal gain achieved here.

Sammendrag

I denne masteroppgaven har en Radiofrekvens Effektforsterker (RF PA) kompatibel med tracking-teknologi blitt designet og produsert. PA'en er designet som en klasse AB forsterker, med bias strøm lik 161 mA og med drain-spenning V_d = 28 V. PA'en har senterfrekvens ved 2.2 GHz, med en båndbredde på 120 MHz. Det høyeste småsignal forsterkningen innen båndbredden er ca. 17.3 dB med mindre enn 1 dB rippel i båndet. Maksimal utgangseffekt til forsterkeren er 41 dBm eller 12.5 W, når inngangseffekten er 30.5 dBm. Effektiviteten (PAE) til forsterkeren er 71.3% ved maks utgangseffekt. Transducer-effektforsterkning ved 1 dB kompresjonspunktet er nesten 13 dB.

PA'en har blitt målt med variabel drain og gate biasering. Dataene fra disse målingene har blitt brukt til å lage tracking-funksjoner for trackings-teknologiene Envelope Tracking (ET) og Power Envelope Tracking (PET). Trackings-funksjonene er laget for både konstant forsterkning og maks PAE, ved å kontrollere V_g and V_d. Den konstante forsterkningen oppnådd er omtrent 10.5 dB. For maks PAE er et høyere effektivitetsnivå oppnådd over et større spenn av effekt i forhold til en PA uten tracker. Det høyeste PAE oppnådd med en tracker er 72.4%. Trackings-funksjonene er laget i MATLAB. Fysiske trackere har ikke blitt testet på PA'en. Men det er antatt at funksjonene oppfører seg tilnærmet likt som den virkelige trackeren vil.

I design og prototypeprosessen, ble det oppdaget at Microstrip-substratmodellen (MSUB) brukt for FR-4 var unøyaktig. Derfor ble MSUB karakterisert på nytt. Dette førte til modifikasjoner av forsterkeren. På grunn av dette, har ikke forsterkeren blitt testet ordentlig for linearitet (2-tone test), men det er antatt at resultatet er nærme simuleringene.

Forsterkeren ble designet med galliumnitrid-høyelektronmobilitets-transistor CG2H40010 fra Cree/Wolfspeed. Denne transistoren er en forbedret versjon av CGH40010F. Påstanden om forbedring fra produsenten har blitt validert, med resultatene for PAE og småsignal forsterkning oppnådd her.

Table of Contents

List of Tables

List of Figures

Abbreviations

Symbol	=	definition
ADS	=	Advanced Design System
APT	=	Average Power Tracking
DSP	=	Digital Signal Processing
ET	=	Envelope Tracking
FET	=	Field Effect Transistor
HEMT	=	High Electron Mobility Transistor
GaN	=	Gallium Nitride
IMD	=	Intermodulation Distortion
MAG	=	Maximum Available Gain
MSUB	=	Microstrip Substrate
NPA	=	New Power Amplifier
OFDM	=	Orthogonal Frequency Division Multiplexing
OPA	=	Original Power Amplifier
PA	=	Power Amplifier
PAE	=	Power Added Efficiency
PAPR	=	Peak-to-Average Power Ratio
PCB	=	Printed Circuit Board
PET	=	Power Envelope Tracking
RF	=	Radio Frequency
VNA	=	Vector Network Analyzer

Chapter 1

Introduction

With the development of 4G LTE and soon to be 5G, there is an ever-increasing need for devices that can deal with issues regarding wider bandwidth and complicated modulation schemes. LTE can give a data rate of around 100 Mbps and 5G is said to possibly be 1-10 Gbps or higher [16]. To get such high data rates, special modulation schemes must be used. In the case of LTE, we have what is called OFDM. OFDM has a very high peak-to-average power ratio (PAPR), which makes it very inefficient for the battery supply of a device. One way of dealing with this supply issue is to use efficiency techniques such as Envelope Tracking (ET), Envelope Elimination and restoration (Kahn), Chireix outphasing or make a Doherty amplifier. But recently a new technique was developed called Power Envelope Tracking (PET) [15]. The inventors of the technique is associate professor at NTNU, Morten Olavsbråten and his former Phd student Dragan Gecan. The technique is still in its infancy and there are many tests and measurements to be done. Testing of a physical PET is not performed here, but a power amplifier (PA) compatible with the PET and ET is designed and produced. The data from this however, is used to make tracking functions. Other PAs compatible with PET exists, these are implemented with a single GaN transistor from Cree of type CGH40010 [5]. The motivation behind designing a new PA is an improved transistor which could enhance the results. The updated version of this transistor is called CG2H40010 [6], which promise to deliver 2 dB extra small signal gain and about 5% more efficiency compared to CGH40010. The hope is that it will be more efficient while still giving as much, or more output power compared to previous PAs.

1.1 Structure of the thesis

The focus in this thesis is primarily on the construction of a class AB power amplifier capable of supporting a power envelope tracker. Necessary theory for understanding PAs and the design process is explained in **Chapter 2**. In this chapter envelope tracking is explained for a better understanding of efficiency techniques and to give a better overview and comparison of PET. PET is explained briefly as motivation behind the design. The specification for the PA is given in **Chapter 3**. In this thesis a PA, an improved PA and a tracker is designed. For this reason, the method and results are not presented by themselves as their own chapters. The design and results are presented over several chapters. **Chapter 4** goes through the design process and results of the PA. **Chapter 5** is about characterization of the PCB-substrate to improve the performance of the PA in Chapter 4. **Section 6** continues where Chapter 5 left off, and uses the new model for the PCB-substrate to design a new PA. Finally, in **Chapter 7**, tracking functions based on the PA in Chapter 6 is presented. Each of these chapters have a brief introduction in the beginning and a summary at the end. **Chapter 8** discusses the most important findings and proposes further work that can be done. The **Appendix** contain tracking tables but also a datasheet for the final PA.

Chapter 2

Theory

In this chapter important theory is presented that will help with understanding the consecutive chapters. The theory mainly covers power amplifiers, but also the tracking technologies Envelope Tracking (ET) and Power Envelope Tracking (PET). Not all theory is presented here, it is assumed the reader has some prior knowledge about s-parameters. Where the theory might be lacking, it can be supplemented by similar previous master thesis's [2][10], that commonly go through the same theory. Or can be studied in detail through books and articles in the reference section.

2.1 Power amplifiers

When designing a power amplifier for radio frequency (RF) applications it is important to consider the biasing network, stability and matching networks for both input and output. A system overview of a transistor PA is shown in Figure 2.1. Generally, there is a source input with characteristic impedance Z_s and an output load with an impedance of Z_l. A transistor biased with a certain gate and drain voltage is used as the amplifier with matching networks to both input and output. The matching networks decides the bandwidth, stability and gain for the amplifier.

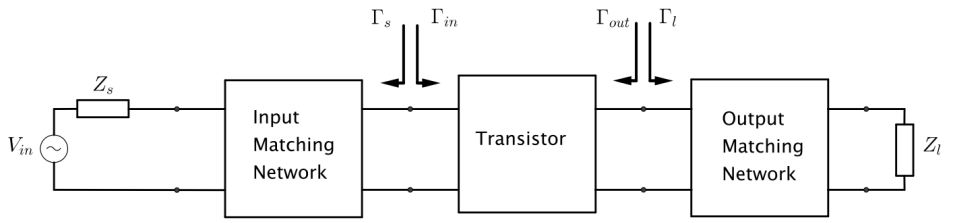


Figure 2.1: System overview of transistor power amplifier [2].

2.2 Biasing network

The input to the transistor is routed to the gate of the transistor, the output is routed to the drain of the transistor and the source of the transistor is grounded. To bias the transistors operating area, DC-sources are coupled to the input and output. When the bias network is implemented as shown in Figure 2.2, it is important to include RF-chokes. RF-chokes forces the RF signal to the output and stops leakage into the DC-sources. The DC-blocks are included to avoid DC leakage on the input and output. It is common to use capacitors and inductors to implement the DC-blocks and RF-chokes because of the high impedance at DC and RF, respectively.

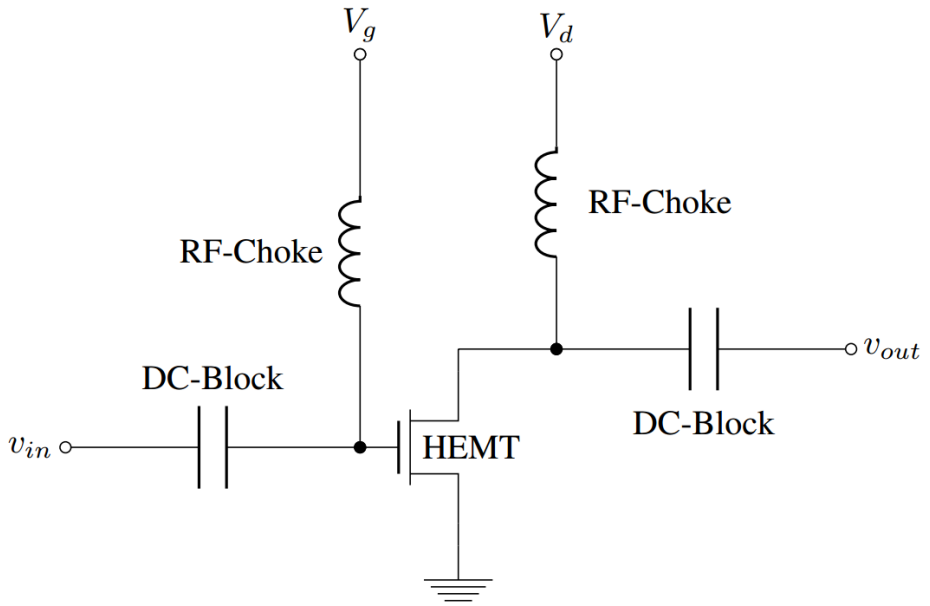


Figure 2.2: HEMT PA without matching networks [2].

2.3 Transistor operating point

The operating point for the transistor can be determined by its IV-curves. A sketch of these curves are plotted in Figure 2.3. The first bias point is set by determining the maximum drain current of the transistor. This also determines the maximum gate voltage and the knee voltage of the transistor. The second bias point is then limited by the knee voltage and the maximum drain voltage, because the transistor would leave the linear operating area or exceed the functional operating drain voltage. It would also be limited by the maximum drain current and cannot have a negative current. Assuming the transistor is linear, the second bias point would also be limited by the line from (V_{knee}, I_{max}) to $(V_{max}, 0)$.

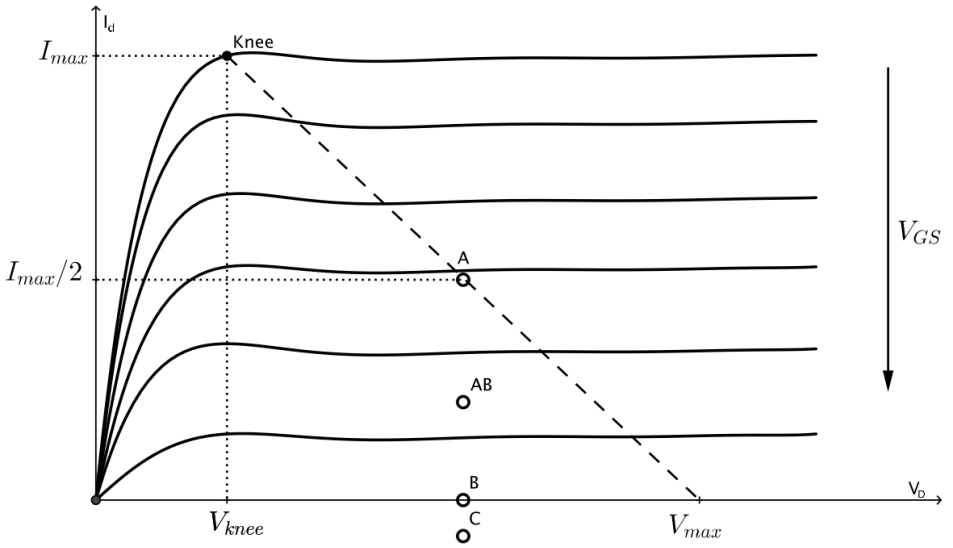
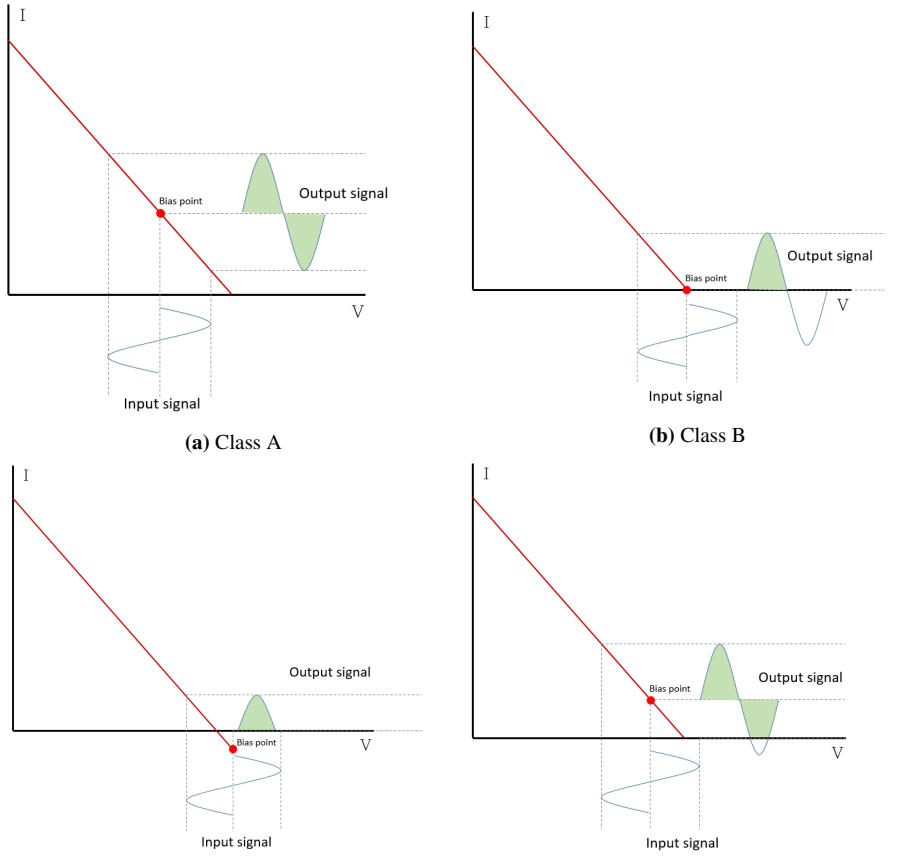


Figure 2.3: System overview of transistor power amplifier [2].

The characteristics of the amplifier would be described by the line from the point (V_{knee}, I_{max}) through the bias point. For a given bias point the amplifier can be associated with different classes of PA's. The classes in Figure 2.3 are given for a specified drain voltage bias.

2.4 Amplifier classes

The main operating characteristics of an amplifier are linearity, signal gain, efficiency and power output. For real PA's there is always a trade-off between these characteristics. To distinguish between the different types, they are assigned into different classes. One set of classes are the set of controlled conduction angle amplifiers; A, B, AB and C. These are defined by the length of the state of the amplifier in which it conducts over a portion of the output waveform. The difference in the length of the conductive state for each class is shown in the output signal in Figure 2.4. The same input signal is used in each class. As seen in the figure, the bias point decides how much of the output signal is distorted.



(a) Class A

(b) Class B

(c) Class C

(d) Class AB

Figure 2.4: Difference in the power amplifier classes [3].

Class A PA's conducts over the entire range of the duty cycle and offers good linearity, minimum distortion and maximum amplitude to the output. However, it is very inefficient with a theoretical efficiency of only 50%. Class B PA's only conducts for half of the range of the duty cycle, thus creating a large amount of distortion, but they have a far better efficiency than the class A PA with a theoretical efficiency of 78.5%. In addition the class B PA's uses two transistors compared to class A witch uses only one transistor. The class AB PA's combines the low distortion of class A and the efficiency of class B. For small power outputs, the class AB PA's acts like a class A amplifier and for large power outputs, it will act like a class B amplifier. From class B or AB it is possible to make what is called class F. Class F can deliver high output power and is highly efficient. Higher efficiency is achieved by using harmonic resonators in the output network to shape the output waveform into a square wave. This technique is called harmonic tuning.

2.5 Efficiency

Efficiency is a very important characteristic of a PA. If a PA has low efficiency, it will deplete its power supply faster, and may overheat. Efficiency is a measure of how well a device can transform one energy source into another. There are different measures of efficiency, but in this design the focus is on two of the most common ones; drain efficiency and power-added efficiency (PAE).

2.5.1 Drain efficiency

Drain efficiency is the ratio of output RF power to input DC power. Drain efficiency is used for a single FET device. It is a measure of how much DC-power is converted into RF-power. This measurement is widely used, but can be a bit misleading.

$$\eta_{drain} = \frac{P_{RFout}}{P_{DC}} = \frac{P_{RFout}}{V_{DC} \times I_{DC}} \tag{2.1}$$

As seen in equation (2.1), drain efficiency only takes the variables P_{RFout} for the output RF power and P_{DC} for the input DC power into account. The input RF power however, is not considered and this can be quite significant. Therefore drain efficiency should be seen in context and not by itself to determine the efficiency of the device.

2.5.2 Power added efficiency (PAE)

PAE is more reliable as a figure of merit for single devices. It is similar to drain efficiency, the difference is that PAE uses input RF power in its expression and is therefore more reliable than drain efficiency as a measurement for figure of merit. This is shown in equation (2.2).

$$\eta_{PAE} = \frac{P_{RFout} - P_{RFin}}{P_{DC}} = \frac{P_{RFout} - P_{RFin}}{V_{DC} \times I_{DC}} \tag{2.2}$$

Comparing the two equations (2.1) and (2.2) it is easy to see that when $P_{RFout} \gg P_{RFin}$ the two measurements are approximately the same, but PAE will always be lower than drain efficiency.
The relationship between the two measurements is shown in equation (2.3) where the PAE is represented by drain efficiency η_{drain} and gain G. Large gain such as 30 dB will give a difference of only 0.1% between the two, while low gain shows the weakness of using only drain efficiency as a figure of merit. For this reason PAE will be used when referring to efficiency in this design.

$$\eta_{PAE} = \eta_{drain} \frac{G-1}{G} \tag{2.3}$$

2.6 1 dB Compression point

The 1 dB compression point is an important metric used with amplifiers. The metric is important regarding the gain and output of the amplifier. The 1 dB compression point referrers to the point P_1 on the amplifier characteristics where the output power is 1 dB lower than an ideal (linear) amplifier. This is illustrated in Figure 2.5. Also seen in the figure is the 3rd order intercept point. This fictive point, P_3, is where the ideal curve meets the 3rd order intermodulation products.

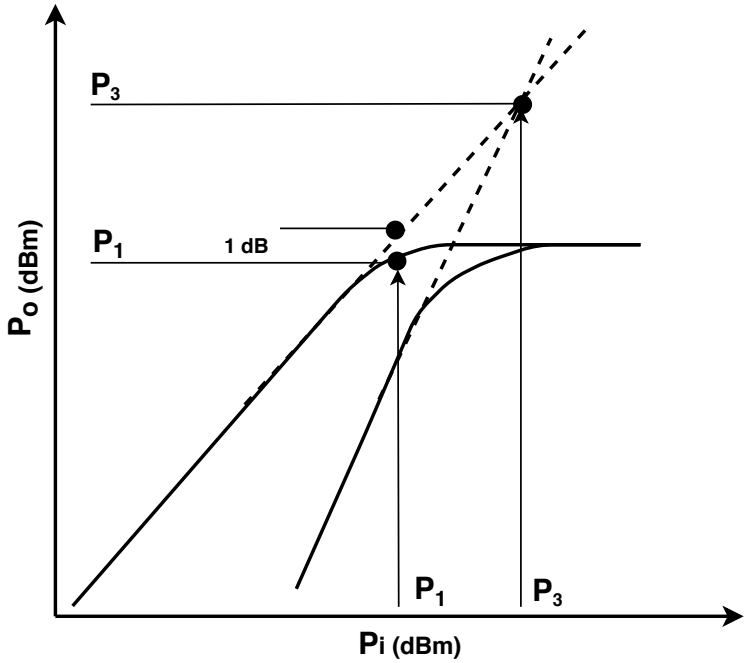


Figure 2.5: Amplifier characteristic showing 1 dB compression point and 3.rd order intercept point

2.7 Load-pull

Load-pull is a technique for measuring performance parameters of an RF device and seeing how these vary with changes in matching impedance. The goal is to find the optimum operating point for an impedance match, working with the Smith chart. Further, it provides insight into the complex impedance:

$Z = R = jX$ of the device under test (DUT) as well as the variations in its impedance as operating conditions (supply voltage, temperature, or frequency) also vary. (Schweber, 2018)

2.8 Envelope tracking

Envelope Tracking or ET for short, is a technique used with PAs to improve their efficiency [11]. The increase in efficiency helps reduce power dissipation in the PA leading to less heating and longer lasting battery time if the power supply is a battery. This technique was invented many decades ago and has not been used for a long time. It was made to tackle PAs efficiency problems with amplitude modulation. Its resurrection is due to improvements in RF-power devices, and especially areas such as digital signal processing (DSP), which has made the technique more viable. The technique is being utilized more and more and can be found in newer smartphones, base stations and other devices. A PA not using any efficiency techniques such as ET is most efficient when it is in compression. This kind of PA is a good choice for signals with no amplitude modulation. However, when signals do have amplitude modulation, it is important not to clip or distort the signal in order to avoid loss of information. The PA must therefore be more linear. Higher linearity can be achieved by operating the PA in back off and/or use techniques such as predistortion. Figure 2.6 illustrates this problem.

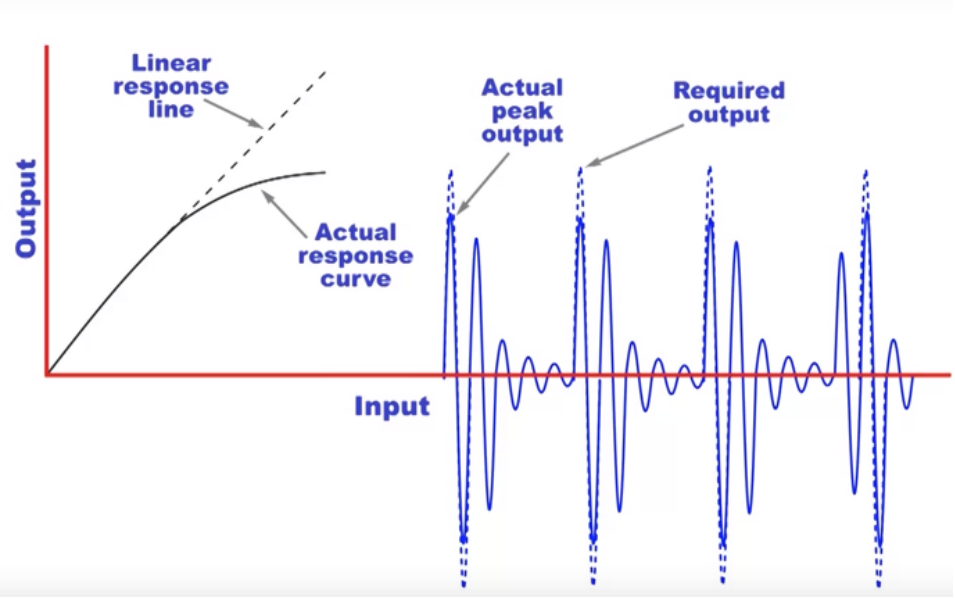


Figure 2.6: IV-curve for PA and amplitude modulated signal in compression [8].

Usage

ET is used when the modulation scheme has amplitude modulation where the peak-to-average power ratio (PAPR) is high. Development in mobile network technology in later years show an increase in PAPR making ET increasingly relevant. The increase from 3G to 4G(LTE) is shown in Figure 2.7. To accommodate the highest peaks the PA must be provided with the right amount of power. If too little power is provided the peaks outside the power level will be clipped and information will be lost. For the most basic systems the supply for the PA is at a constant level, and high enough to ensure the highest peaks in the signal stay intact. The efficiency problem stems from the times where there are no high peaks but rather valleys. When this happens, the extra power is dissipated as heat. PAPR is key to what efficiency level that can be achieved.

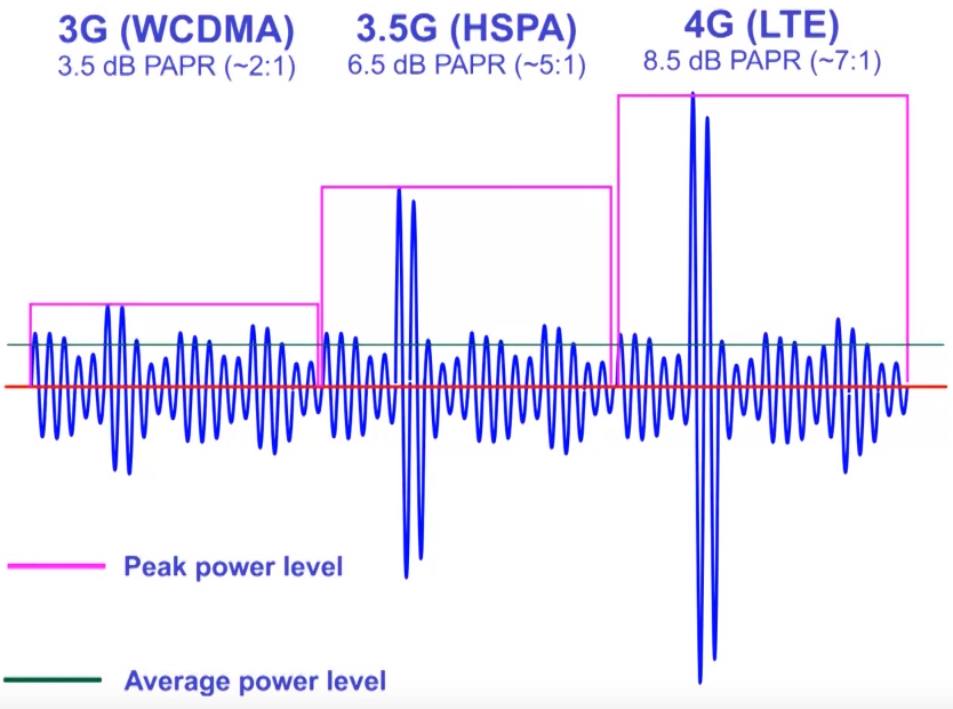


Figure 2.7: PAPR for 3G-4G/LTE [8].

How it works

In an ET amplifier [1] the voltage supply of the drain(collector) is modulated with the envelope of the input RF signal. This voltage on the drain "tracks" the envelope. To improve the efficiency of the amplifier, the envelope of the signal is used to reduce the drain voltage when the envelope is small. It is important that the amplifier gain is constant when this is done. Because of ET the amplifier operates near saturation for all envelope levels. An example of ET on a signal can be seen in Figure 2.8. The idea behind ET is simple, while the implementation is quite complicated and involves considerable amounts of DSP. Figure 2.9 shows a block diagram of the basic structure for an ET-PA [11].

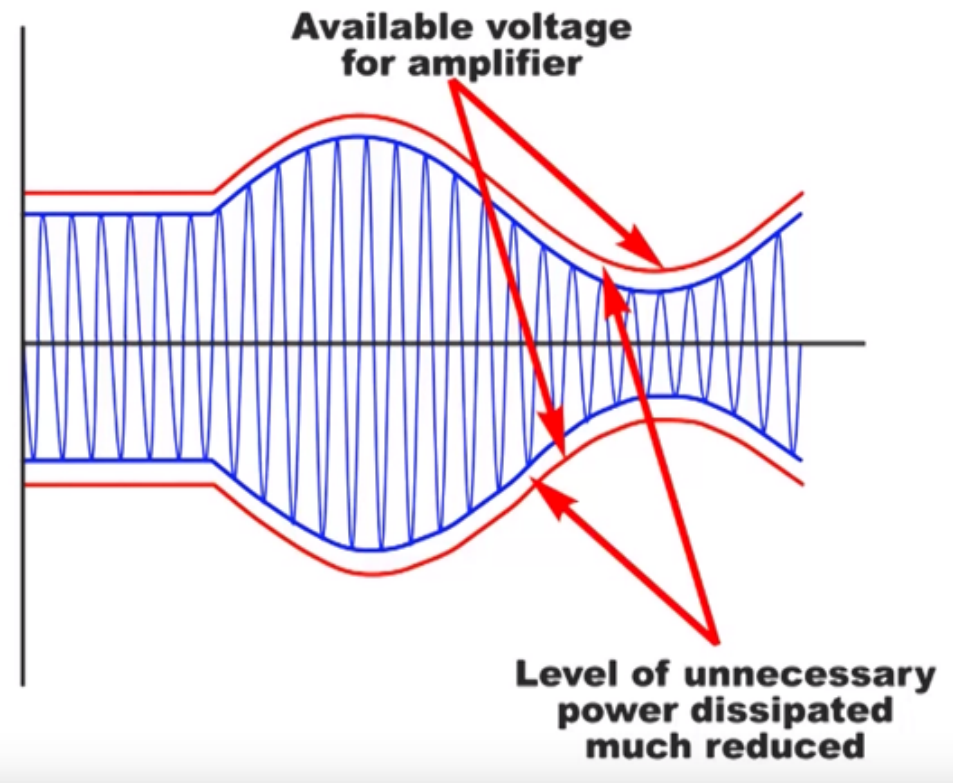


Figure 2.8: Envelope tracking on signal [8].

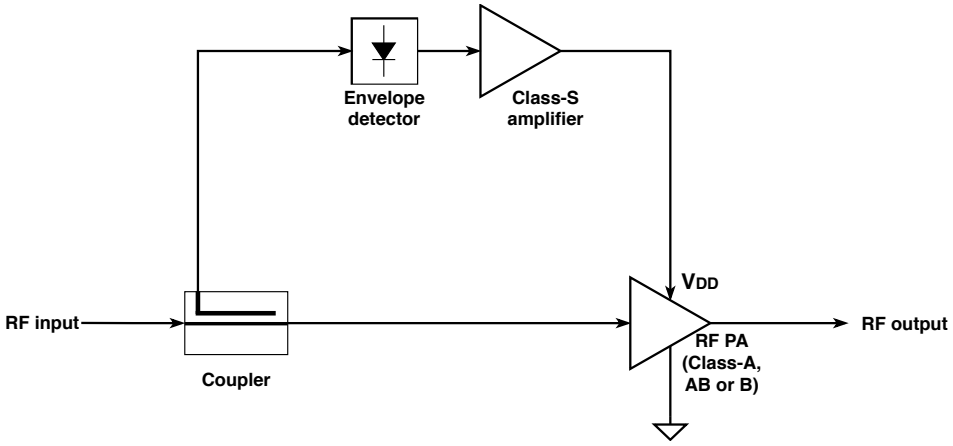


Figure 2.9: Schematic of an RF amplifier employing envelope tracking.

Comparison

Figure 2.10 gives a simple overview of the contrast with and without ET in terms of efficiency. Figure 2.10a is a PA with a constant supply voltage and no power control. The yellow line indicates the supply voltage while orange is unused power being dissipated as heat. Figure 2.10b is a PA using power control called average power tracking or APT. APT works by dividing the signal in time slots, for each slot the level of the supply voltage is adjusted to the highest peak in that slot. This technique can work well with lower PAPR and is much simpler and cheaper than ET. ET is more complicated but offer far better efficiency in comparison when PAPR is high as seen in Figure 2.10c.

Drawbacks

Although ET is very beneficial it also has some drawbacks, the major one is the required bandwidth of the drain (collector) supply. In theory the required bandwidth of the envelope approaches infinity for any standard modulation schemes [15]. But in practice ET requires about 4 to 8 times the bandwidth of the RF signal [9]. Newer systems demand larger bandwidths to accommodate more users and increase the data-rate, which means another technique may be required.

2.9 Power envelope tracking

Power envelope tracking or PET is a newly developed efficiency technique for PAs [15]. The technique is similar to ET, but is much simpler to implement, requires very little DSP and requires a much smaller bandwidth for its drain (collector) supply compared to ET. A drawback of the technique is that it is less efficient compared to ET.

While ET uses the envelope of its RF signal to modulate the voltage supply to the drain of the transistor, PET uses an approximate tracking function. The difference this makes in relation to the bandwidth is considerable and is mathematically explained in this excerpt from one of the papers on PET [15]:

Assume that the transmitted RF signal has a bandwidth, B_{RF}, with a corresponding baseband signal, $v_s(t)$, which is a complex modulated time varying signal with a baseband bandwidth, $W = W_{BB} = B_{RF}/2$, given in (1).

$$v_s(t) = v_I(t) + j \cdot v_Q(t) \rightarrow \underline{W = B_{RF}/2} \tag{1}$$

Shaping the drain voltage as a function of the envelope of the signal (2), results in a theoretic infinite bandwidth. This is an effect of the square root function.

$$v_{d,env}(t) \propto v_{s,env}(t) = |v_s(t)| = \sqrt{v_I^2(t) + v_Q^2(t)} \rightarrow \underline{W = \infty} \tag{2}$$

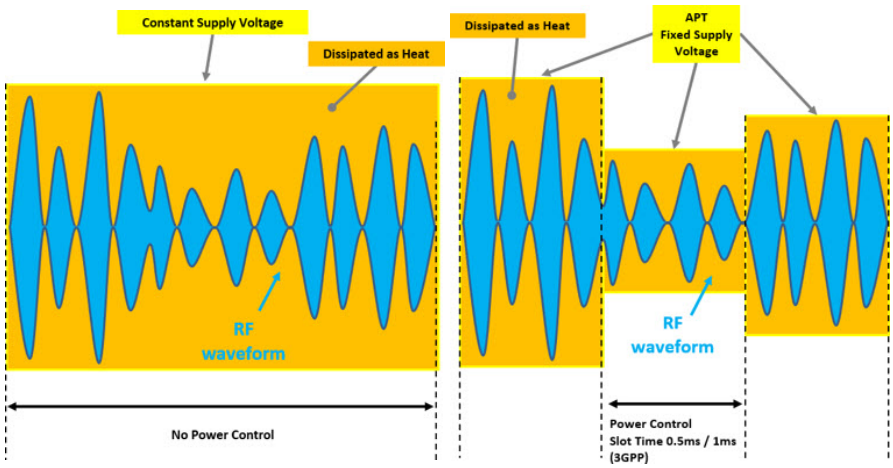
The bandwidth of a transmitted RF signal in a system is normally only $B_{RF} = 2W_{BB}$. This is the bandwidth of the transmitted RF power. Using this as a basis for the technique development, the drain voltage should be shaped after the power of the baseband signal instead of the envelope. The technique of the Power Envelope Tracking (PET) is shown in (3). This will have some consequences for the efficiency of the RF PA, as will be shown in the next sections.

$$\begin{aligned} p_{env}(t) = v_s(t) \cdot v_s^*(t) = v_{s,env}^2(t) \rightarrow \underline{W = B_{RF}} \\ \Rightarrow \underline{v_d(t) = a_0 + a_2 \cdot v_{s,env}^2(t) = a_0 + a_2 \cdot p_{env}(t)} \end{aligned} \tag{3}$$

(Olavsbråten and Gecan, 2017, p. 374)
While ET uses equation (2) from the paper with a theoretic bandwidth of infinity, PET uses an approximation based on the baseband instead and does not follow the envelope of the signal. Figure 2.11a shows the technique in action, it manages to hit all the peaks, which is most important, but does not go as low as ET for the valleys or lowest points in the signal. Therefore it is less efficient, but the bandwidth required is limited and well defined. Figure 2.11b shows how practical the technique can be in terms of limiting the bandwidth required.

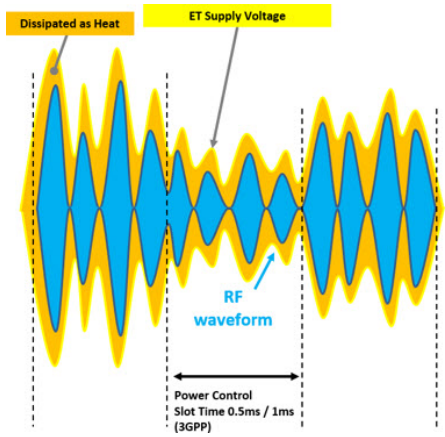
Mentioned in the paper is a way to increase efficiency further, this can be done by extending the PET to higher orders of power as seen in equation (4), this is called 2.order PET. With 2.order PET the tracking can better fit the signals envelope almost as good as ET, this leads to better efficiency and higher bandwidth requirement, but the bandwidth is still well defined and limited as seen in Figure 2.11. Newer technology has an increasing demand for more bandwidth to be able to transfer more data in shorter time. 5G could require RF-signal with GHz bands. For ET which needs about 4-8 times this for its envelope bandwidth, it does not seem feasible unless bandwidth limiting techniques are used in combination with it. PET on the other hand is more feasible based on these results.

$$\begin{aligned} v_d(t) = a_0 + a_2 \cdot v_{env}^2(t) + a_4 \cdot v_{env}^4(t) \rightarrow \underline{W = 2 \cdot B_{RF}} \\ \Rightarrow \underline{v_d(t) = a_0 + a_2 \cdot p_{env}(t) + a_4 \cdot p_{env}^2(t)} \end{aligned} \tag{4}$$



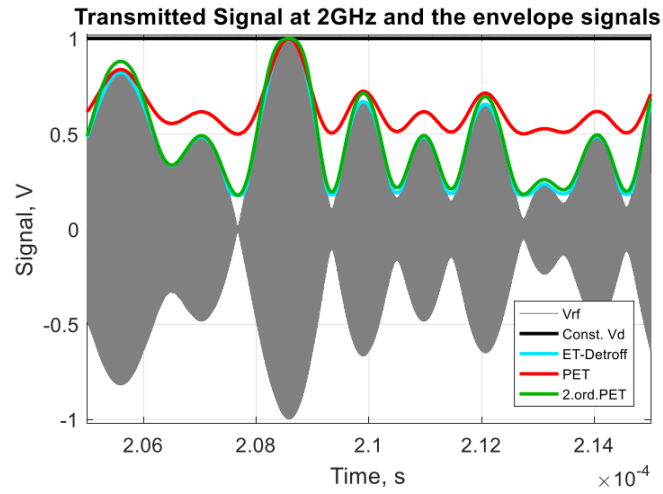
(a) PA with constant supply voltage

(b) PA using APT

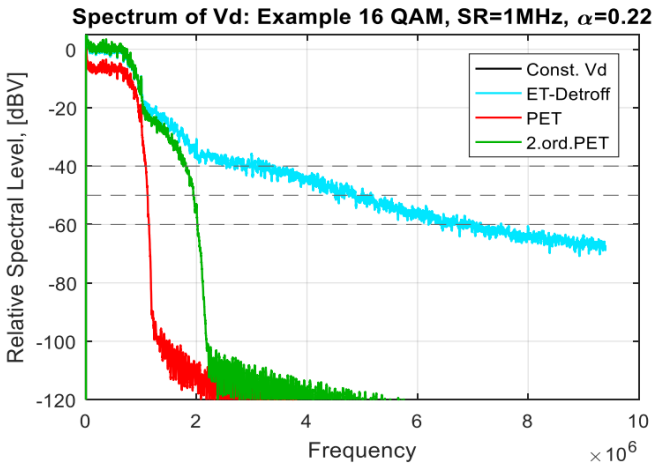


(c) PA using ET

Figure 2.10: Comparison of PA with a battery supply (left), PA with APT (right) and a PA with ET (bottom) [13].



(a)



(b)

Figure 2.11: Plots comparing ET, PET and 2.order PET using a 16QAM-signal [15]. An ideal lossless transistor (current source) is used as the RF PA in these plots.

Chapter 3

Design restrictions and specifications

3.1 Design restrictions

- The frequency of operation f_c is 2.2 GHz.
- The device must be biased with a drain voltage V_D of 28 V.
- The drain current I_D should be no less than 50 mA. This implies that gate voltages V_G below approximately -3.0 V cannot be used.
- Advanced design systems [12] (ADS) from Keysight is used for design and simulations.
- For the connection between the tracker and the PA there must be low resistance, low capacitance and low inductance [7].

3.2 Small-signal specifications

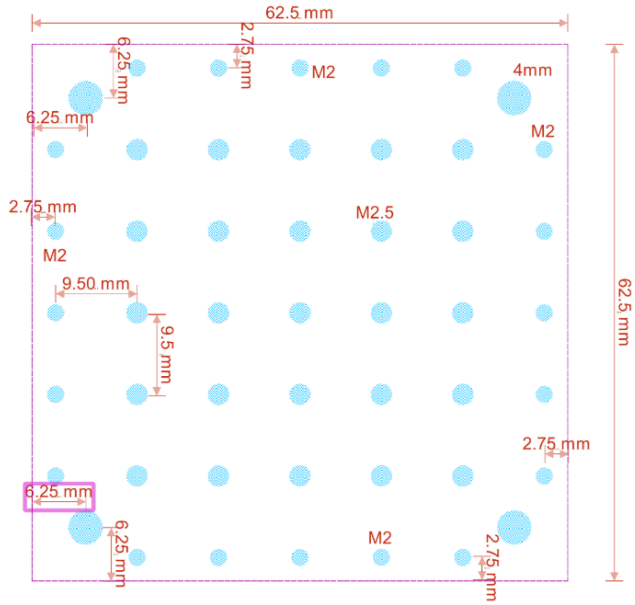
- The device must be unconditionally stable, e.g. the stability factor (μ) must be greater than unity for all frequencies.
- The small-signal bandwidth f_{bw} should be at least 400 MHz.
- The small-signal gain S_{21} should be at least 14 dB throughout the bandwidth 2.0 GHz to 2.40 GHz.
- The bandwidth should have no more than 1 dB ripple.

3.3 Large-signal specifications

- The device should produce an output power P_{out} of at least 40 dBm at single-tone input power P_{in} of 28 dBm.
- The power added efficiency η_{PAE} with a single-tone input power of 27 dBm should be as high as possible.
- For a two-tone peak output power of 38 dBm, the intermodulation distortion (IMD) should be as little as possible. The tone spacing should be 5 MHz for the two-tone test.

3.4 Layout restrictions

The layout has few specific restrictions when it comes to size. The most important thing is that it is larger than the heat sinks available, so that the SMA connectors can be soldered on. The heat sink used is an 62.5x62.5 mm aluminum plate. The layout of the heat sink and the SMA-connector used can be seen in Figure 3.1a and 3.1b. These connectors must be soldered on both sides of the PCB to be secured in place, therefore on the input and output side of the PCB, the edge of the PCB must be at least 5 mm longer than the heat sink on either side. If the layout is produced in China through pcbway.com, it should be no larger than 100x100 mm to keep production cost down.



(a) Outline for the heat sink [18].

(b) SMA connector [4].

3.5 Transistor technology

The transistor used in the project is a Gallium Nitride (GaN) high electron mobility transistor (HEMT) from *Cree*, the CG2H40010 [6]. It offers high efficiency, high gain and a general purpose, broadband solution to a variety of RF and microwave applications. The CG2H40010 is a powerful 10 W device, which, if matched properly, can deliver more than 17 W when operated in deep compression. CG2H40010 promises to give 2 dB higher small-signal gain and 5% higher PAE compared to its predecessor CGH40010 [5].

3.6 Microstrip substrate

The substrate used in the design is the standard FR-4, which is a composite material manufactured from fiberglass cloth embedded in flame resistant epoxy resin. The characteristics of FR-4 material used is summarized in table 3.1.

Height	ϵ_r	μ_r	Conductivity	Thickness	Loss Tangent
$1.6 * 10^{-3} m$	$4.4 {}^{F}/_{m}$	$1.0 {}^{H}/_{m}$	$5.96 * 10^{7} s$	$35 * 10^{-6} m$	0.02

Table 3.1: Substrate characteristics [17]

Chapter 4

Method and preliminary design

This chapter is divided into two main parts. First part explains the method for designing and producing an RF PA, it consists of section 4.1 through 4.6. The second part presents simulated and measured results of a PA using the design method presented in part one.

4.1 Bias point

The operating point of the transistor can also be referred to as its bias point. As described in section 2.3 and 2.4, it plays a major role in the amplifier's characteristics. Therefore, before any circuit design is done, it is important to choose an operating point for the transistor. The operating point is chosen based on what amplifier qualities is important for the specific design. To make the choice easier, the operating point can be determined by using amplifier classes. In this case the chosen amplifier class is a conduction angle type. This type of amplifier class is explained in section 2.4. Each class has their pros and cons. The classes to choose from is A, AB, B and C. In the specification in Chapter 3, the desired qualities listed are; high efficiency, high output power, high gain and good linearity. Among these the efficiency and output power is prioritized. Class A should not be chosen, because it is the least efficient. Class B and C are the most efficient, however the properties of the transistor combined with the specifications for the minimum drain current excludes class B and C. The transistor must therefore be biased as class AB. Class AB allows for better efficiency than class A, it has higher output power and is more linear than B and C. Additionally the efficiency can be increased with harmonic tuning. This requires enough nonlinearity so that harmonic components arise. For increased nonlinearity the amplifier can be biased in deep AB. The amplifier is then closer to a class B amplifier than class A.

The bias point of the transistor is chosen to be -2.7 V gate voltage and 28 V drain voltage, the latter being the default operating bias of the transistor. The maximum current is set to 1.49 A, being close to the maximum current (1.5 A) available from the transistor. This also sets the knee voltage to 4.0 V. The maximum drain-source voltage of the transistor is 120 V and maximum power dissipation is 14 W. These properties of the transistor is found in its datasheet [6]. As seen in Figure 4.1, this results in a transistor biased as a class AB. The transistor is operating close to the limit of its drain current and power dissipation. The bias or drain current for operation should be about 161 mA.

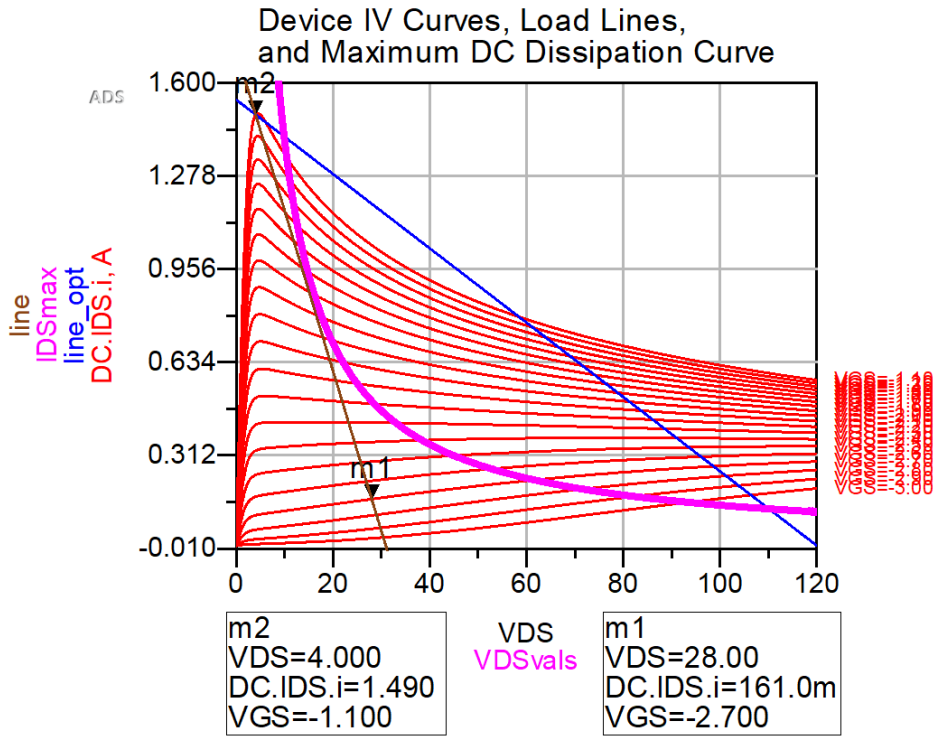


Figure 4.1: Bias point simulation with power dissipation limit (pink), operating area for ideal class A power amplifier (blue) and chosen bias point m1 (brown).

4.2 DC-bias network

The DC-bias network is similar to the RF-choke mentioned in section 2.2. It works as a high impedance network for the RF-signals and a low impedance network for DC-signals. This ensures that DC-bias can be applied to the transistor without the RF-signals leaking into the DC-sources. To achieve the desired characteristics of the DC-bias network, the reflection coefficient S_{11} of the port connected to the DC-source should see short circuit

for the fundamental, 2nd and 3rd harmonics. The reflection coefficient S_{22} of port 2 connected to the RF-network should see open circuit for the fundamental and 3rd harmonic, while the 2nd harmonic should be short circuited. This is achieved first with ideal lines and ideal components. The results achieved in simulation with microstrip and real components is shown in Figure 4.2 and Figure 4.3. For S_{21} and S_{12} there is attenuation for all higher frequencies. As seen in Figure 4.3, S_{21} and S_{12} are the same, for the fundamental frequency there is almost 41 dB attenuation and all frequencies above 900 MHz have at least 10 dB attenuation. For DC the attenuation is minimal, less than 0.1 dB.

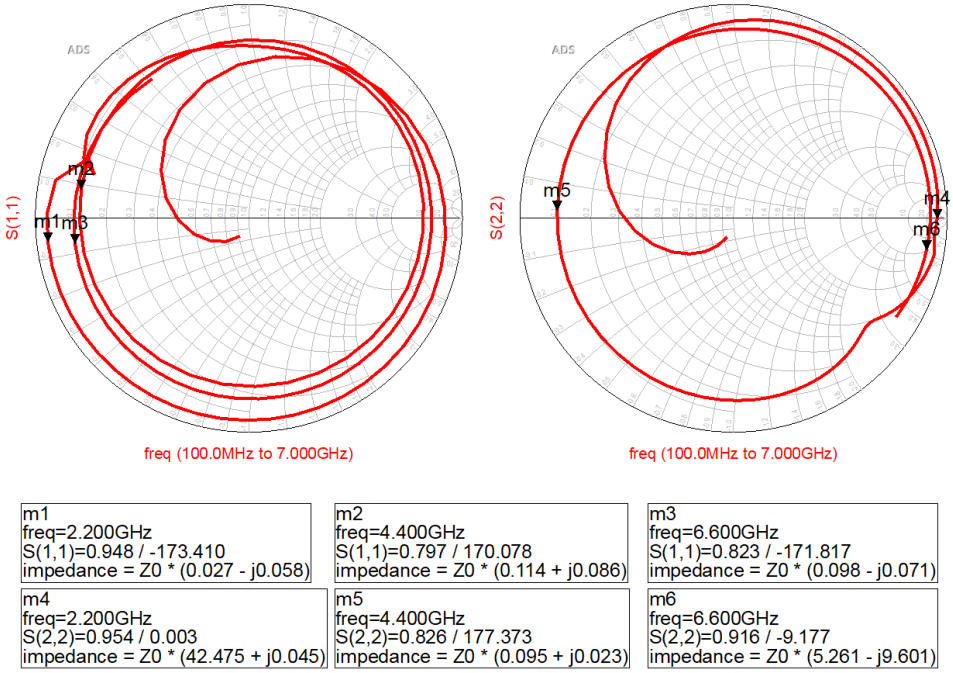


Figure 4.2: Simulations of the reflection coefficients S_{11} (left) and S_{22} (right) for the DC-bias network.

For ET and PET the power supply is not able to have a decoupling capacitor on the link to the power amplifier. Because of high bandwidth modulation required by the tracking supply, a decoupling capacitor cannot be used [7]. This places some requirements on the connection between the tracker supply and the PA. This is listed in the specifications; low resistance, low inductance and low capacitance. Low resistance is required to ensure that no voltage is developed across the link between the tracking supply and the PA. Low inductance is also important to avoid voltage to develop across inductive elements of any reactance. Lastly, too high capacitance in the connection will limit the tracking performance. The capacitance must therefore be kept as low as possible. This is why only two small capacitors are used in the DC bias network, their values are 3.9 pF and 5.6 pF. If no tracker is connected to the PA it will oscillate heavily. To prevent oscillations while measuring the PA by itself, it is necessary to add a 1μF capacitor in each bias network.

The design for the drain and gate bias network is nearly identical. The resulting topology for the DC bias is shown in Figure 4.4. A radial stub is used to increase the small-signal bandwidth.

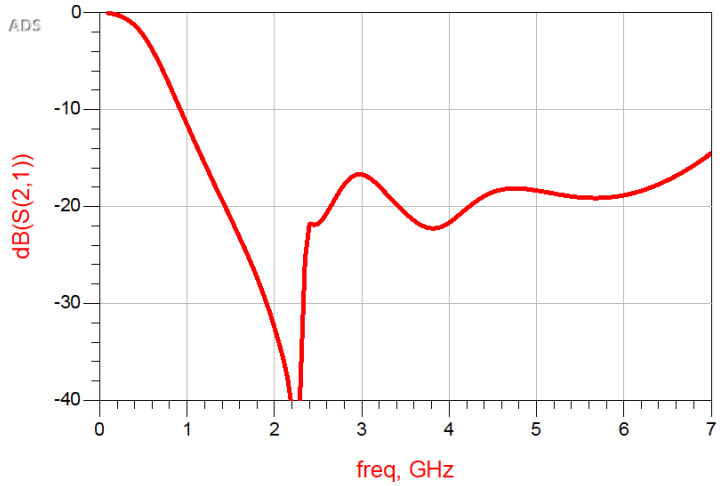


Figure 4.3: Simulations of the reflection coefficients S_{21} for the DC-bias network.

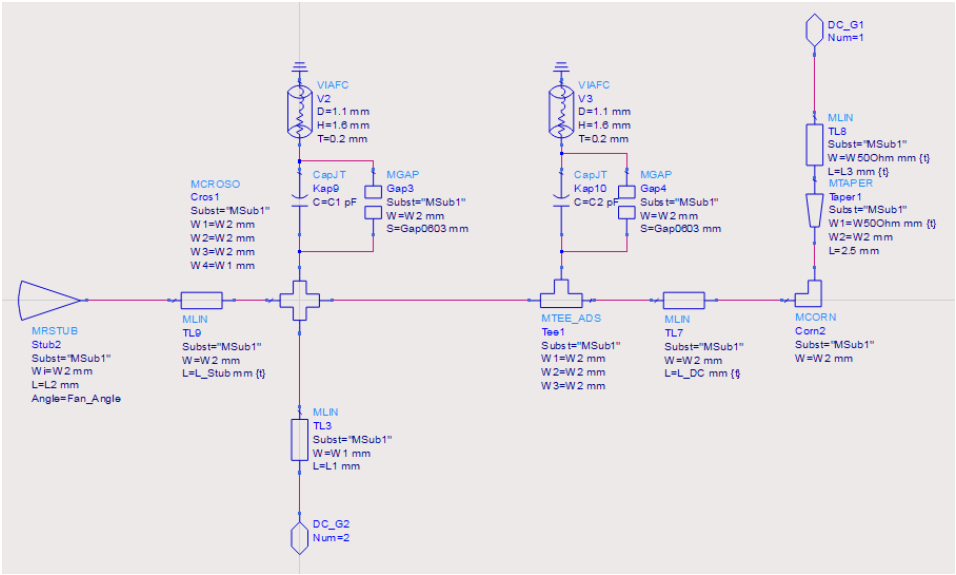


Figure 4.4: Schematic for the DC-bias network. DC_G1 is port 1 while DC_G2 is port 2.

4.3 Small-signal stability

With the transistor biased, the next step is to make the circuit stable. A common issue when designing PAs, is that they behave as oscillators rather than amplifiers. The oscillations happen due to instability in the circuit. A requirement of the PA is that it should be unconditionally stable. There are numerous formulas for determining the stability of the circuit. Possibly the most used are the K-factor and the μ-factor. In ADS, the stability is calculated using the K-factor and the μ-factor. The K-factor is only defined for two-port network and does not provide information of how stable the PA is. If the factor is larger than 1 the PA is guaranteed to be stable for that specified frequency. A K-factor above 1 for all frequencies will be unconditionally stable. The μ-factor on the other hand, does provide information on how stable the PA is. Larger values of μ means greater stability. If either μ_{source} or μ_{load} is larger than 1 for all frequencies, the PA will be unconditionally stable. Figure 4.5 shows the stability factors of the PA, they are all larger than 1 for all frequencies.

It is very important to have a margin of error when designing for stability. A good practice is to have either μ_{source} or μ_{load} above 1.1. The reason for this is that production of circuits does not have the same quality every time, there will always be some slight variation in the characteristics of the material and components. In the design μ_{load} is around 1.1 for all the tested frequencies. For 80 MHz and lower the factor is about 1 for both μ_{source} and μ_{load}.

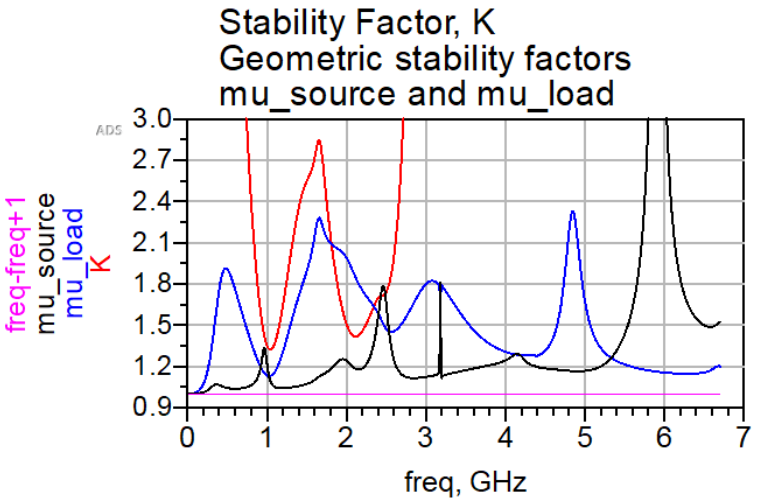


Figure 4.5: Stability simulations for the PA.

The bias network has a desired effect on the stability of the circuit and can be tuned to some extent for improved stability. However, the main parts used to achieve unconditional stability is seen in Figure 4.7, this is called the stability circuit. At the gate of the transistor a parallel resistor and capacitor is connected. The parallel RC has good effect for the stability of most frequencies. This however is not always enough. There can be instabil-

ity for the lower frequencies, which is the case for this design. To gain stability for the frequencies below 1 GHz, what is known as a pull-down resistor is used. The resistor is connected with the Gate Bias as seen in the figure.

The stability circuit not only influences stability, but also the maximum available gain (MAG). MAG is the gain it is possible to achieve when the PA is perfectly matched. For a more stable circuit, MAG can be sacrificed. To get more bandwidth, the matched gain can be sacrificed. Therefore, if a broad bandwidth with high gain is desired, the MAG should be as high as possible within that frequency range. Once the desired maximum available gain and stability is achieved, the component values of the stability circuit should not be changed.

4.4 Matching network

The matching network for the input and output of the power amplifier is essential when determining the desired frequency band, stability and gain. Usually there is a trade-off between these factors, where improving one may deteriorate the others. In order to match the input and output properly it is common to use smith charts and use the complex conjugate method. This gives a point in the smith chart representing either the input or output impedance. To get a match, one must simply make a way from the point to the center of the smith chart, using components and or transmission lines. A perfect match gives a very narrow bandwidth, but is a good starting point to do additional tuning to achieve desired results.

In this design however, a different approach is used. Instead of transmission lines or passive components, special components called load-pull and source-pull is used. Normally load-pull is done on a physical device, but in this design a ADS model has been made by Morten Olavsbråten. The ADS components are seen in Figure 4.6. These have tunable variables for the vector of the fundamental, 2nd and 3rd harmonics. With this, harmonic tuning is possible. Load-pull and source-pull is used for matching. The methods described up until now are the main modules of the PA design. Together as seen in Figure 4.7, they make up the full design. Source-pull functions as the input matching network, while load-pull is the output matching network. After proper tuning is performed, the load-pull and source-pull is switched with real matching networks.

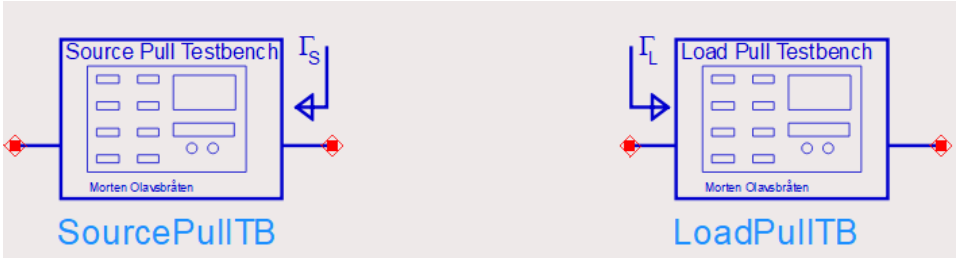


Figure 4.6: Source-pull and load-pull component in ADS, made by Morten Olavsbråten

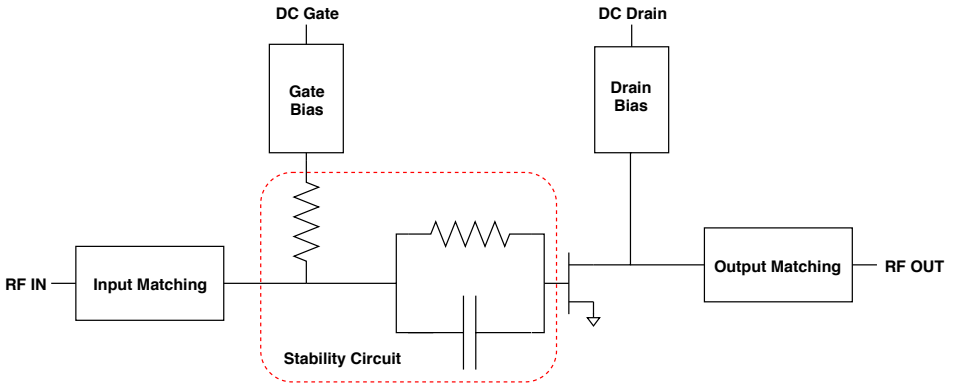


Figure 4.7: Main modules in the PA-design

The three vectors from load-pull can be plotted in a Smith chart as seen in Figure 4.8. A matching network can be synthesized using these points. The best results are achieved by making a topology that best matches the reflection coefficient of the load-pull. In this design, different topologies are tested and tuned using an optimize function in ADS. If S11 (teal colored) as seen in Figure 4.8 intersects or is close to the points, a network with similar reflection coefficient can be synthesized.

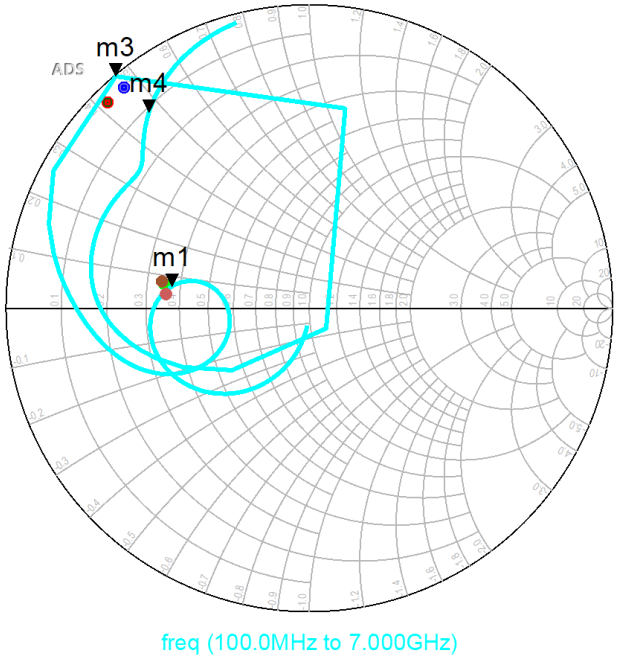


Figure 4.8: Load-pull results seen as colored points in the Smith chart. S_{11} for the synthesized network is represented by teal.

The load-pull component is switched with the synthesized network when it is done. The whole system is then optimized before performing the same process for source-pull. A synthesized network for the load-pull results from Figure 4.8 is seen in Figure 4.9. This uses a component called MSOP.

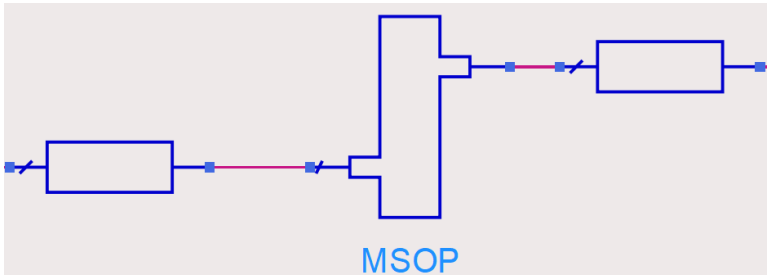


Figure 4.9: Synthesized network.

The input match has most influence on matching for small signal gain. While the output has most influence on the output power and efficiency. The final input and output network containing the synthesized networks is seen in Figure 4.10 and Figure 4.11. The transistor is connected between the two networks as seen in Figure 4.7. The synthesized network does most of the matching, but DC block capacitors and the surrounding transmission lines are also tuned for better matching.

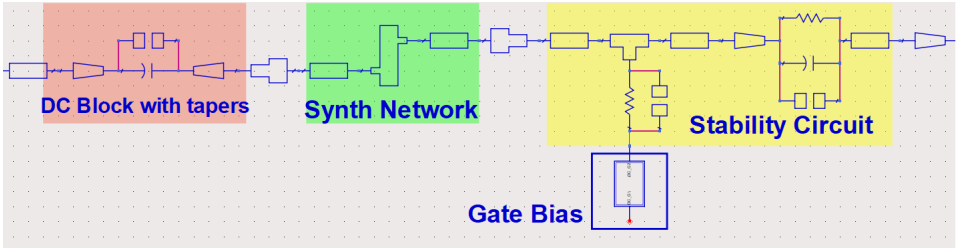


Figure 4.10: Input network

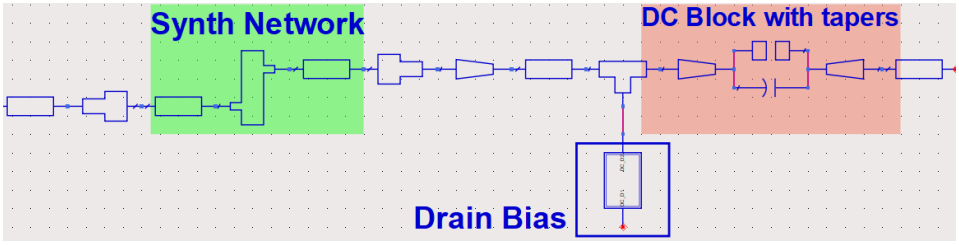


Figure 4.11: Output network

4.5 Layout

The layout is the final step of the design before it is sent to production. The layout for the PA is done in ADS. ADS automatically make a layout based on the schematic design. Other miscellaneous elements, such as holes for the heatsink are added manually. To prevent errors, the design in schematic is constantly changed to make sure layout is correct and meet the specifications. Final layout is seen in Figure 4.12. Gerber and drill files can then be exported and sent to production.

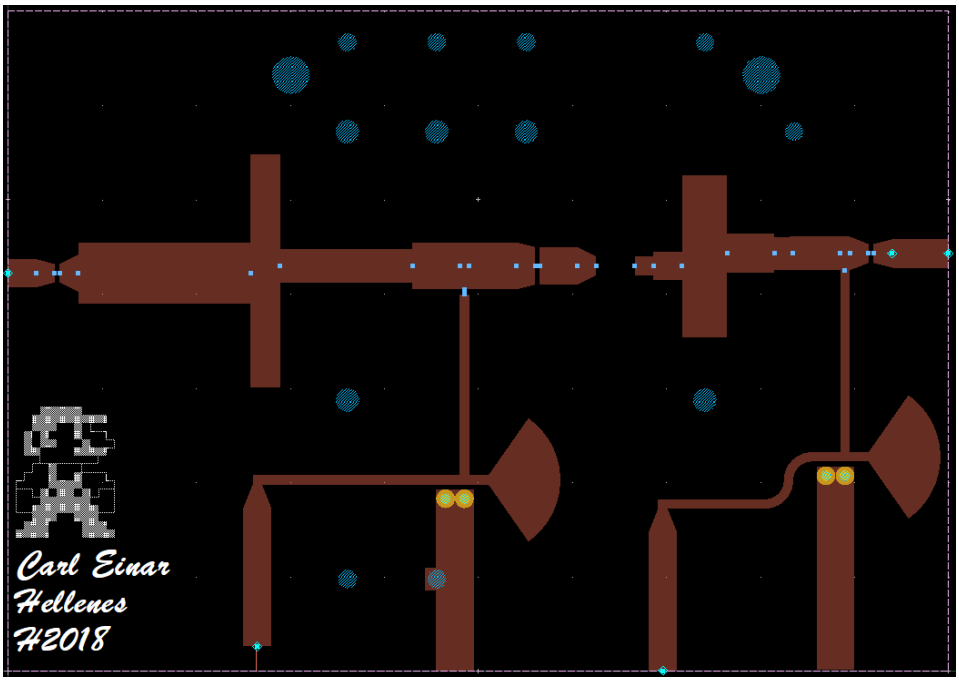


Figure 4.12: PA layout in ADS.

4.6 Production

To produce the designed circuit there are several options available. The PCB can be produced in-house if possible. However, this is not possible for everyone. To check other alternatives, the circuit is produced in China through a website called PCBWay.com. The production costs only $5 for 5 copies of the circuit, this is with the cheapest options. The final product from PCBWay is seen in Figure 4.13. The PCB also has a tinned layer over the copper to make soldering of components easier. The size of the original design is reduced to some extent. It is reduced to meet the requirement of maximum size of 100x100 mm, larger sizes increase cost drastically. No hole is drilled for the transistor, the reason for this is so that the circuit can be cut in two. This divides the circuit into an input and

output network, if something is wrong with one side it is easier to do troubleshooting. The finished PA mounted on a heat sink, is seen in Figure 4.14.

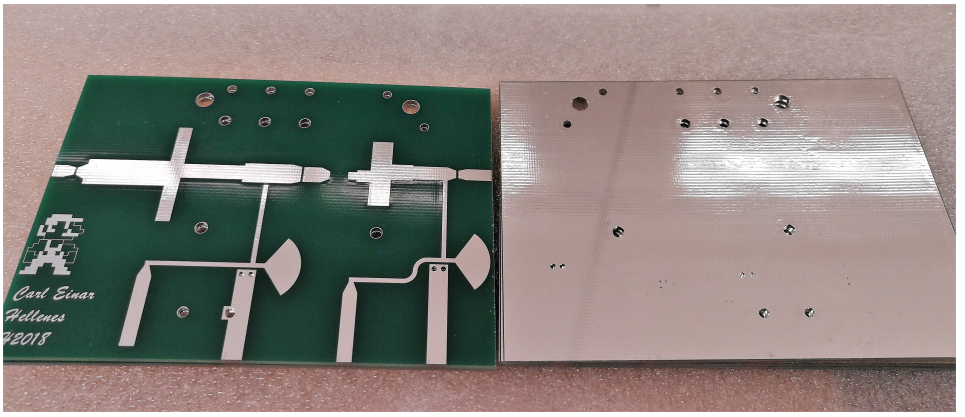


Figure 4.13: PCB produced in China through PCBWay.com.

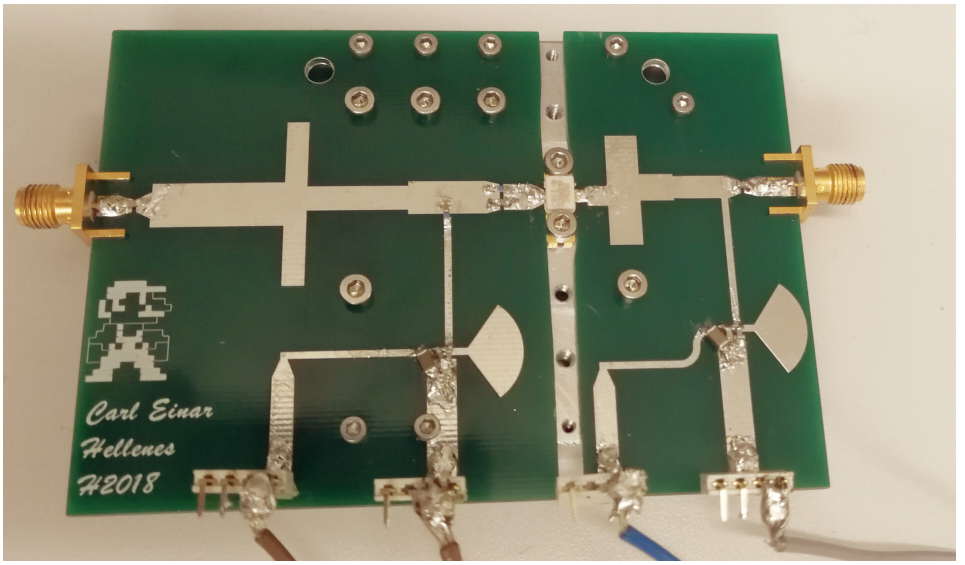


Figure 4.14: PA mounted on heat sink.

4.7 Small-signal analysis

Maximum available gain is the amount of gain the amplifier can supply when perfectly matched. As previously stated, perfect matching can be achieved with complex conjugate matching. This is done by using the values for the conjugate of the impedance given by ADS for Z_{Source} and Z_{Load} to match in the smith chart. This however will only give perfect matching for a small bandwidth of a few MHz or less, therefore some gain must be sacrificed to get a broader bandwidth. The desired small signal gain is achieved through source-pull matching on the input side. Load-pull matching on the output contributes as well, but to a lesser degree. The output however, must be fine-tuned in order to keep a high output power and high PAE, with the desired gain.

Simulation

Figure 4.15 is the simulated small-signal gain from ADS. The blue plot represents MAG, while the pink plot is S_{21}. The two plots are not perfectly matched at the center frequency of 2.2 GHz. Some mismatch is allowed in return for more bandwidth. A bandwidth of about 540 MHz with less than 1dB gain ripple is achieved in ADS. The bandwidth is in the interval from 1.93 GHz to 2.47 GHz. The highest gain in the bandwidth is around the 2 GHz point, where the gain is about 17.8 dB. There is also an unwanted peak outside the band at the 1GHz point, this also has a gain of 17.8 dB. The gain is lowest around the edges of the band, as well as in the middle of the bandwidth creating a little valley around 2.27GHz, where the gain is 17 dB. For the higher frequencies measured up to 7 GHz, the gain is lower than -7 dB.

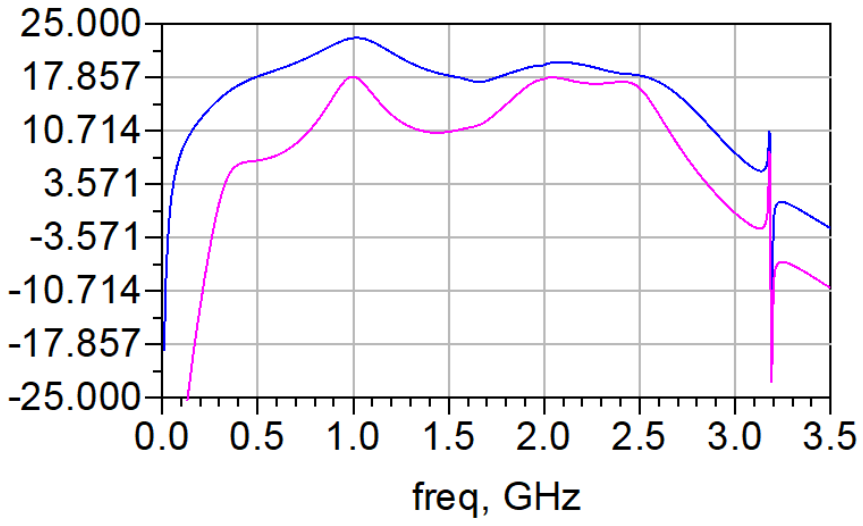


Figure 4.15: Results for small signal simulation, MAG in blue and S_{21} in pink

Lab setup

To measure the S-parameters of the PA, a VNA or Vector Network Analyzer from Rohde & Schwarz is used. The lab setup is quite simple. It requires two SMA cables, a power supply for the PA, as well as an attenuator. The attenuator is placed at the output of the PA to protect the VNA from high power levels. The setup is seen in Figure 4.16. The setup is calibrated using SOLT; Short-Open-Load-Through. For Rohde & Schwarz this is referred to as TOSM; Through-Open-Short-Match. The DUT in the figure stands for Device Under Test. In this case the device is a PA.

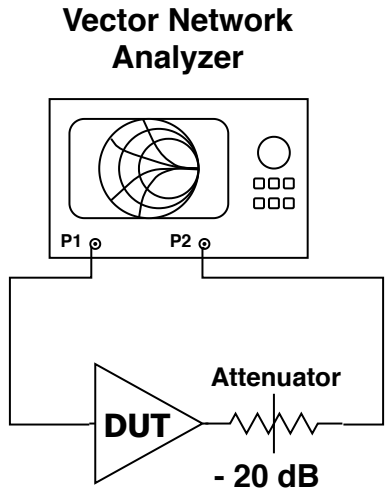


Figure 4.16: Lab setup for small-signal analysis

Measurements

The finished PA seem to behave very similar to the results when measuring. The measurements can be seen in Figure 4.17. The pink plot is the simulated S_{21}, while the teal, green and blue is the finished PA, measured on three separate occasions. The teal colored is the oldest measurement. Besides being shifted by about 50-60 MHz to the left, it is nearly identical to the simulated result. The peak at 1 GHz is lowered and is only at 12.6 dB. The gain around the bandwidth is still high, at some places higher than in simulation, about 18.2 dB. However, there is an unfortunate dip in the middle of the bandwidth at 2.30 GHz, the gain her is 15 dB. The measured bandwidth is from 2.00-2.26 GHz and 2.40-2.55 GHz. The dip could be caused by many things. Simulations with different values for the capacitors in the bias network and DC block can be used to affect the matching and the shape of the gain curve. Perhaps the cause of the dip is components with the wrong value that have been soldered on. Switching the values of the capacitors in simulations does give a dip, trying other capacitor values could remove the dip. Another explanation suggested, is that the two Johanson capacitors in the bias network cause a resonance with each other. Using only one Johanson capacitor could possibly solve the problem.

The blue plot is the second oldest measurement, measured 5 months apart from the first one with the same VNA. It is nearly identical to the first measurement except for fine details. The only major difference is that it is lowered by about 4 to 4.7 dB for most frequencies. The PA having a lowered performance of 4 dB after only 5 months is improbable. It is possible some settings on the VNA is different or the calibration is wrong, the reference might be lowered. Other known devices, however, seem accurate with the same calibration. It could be a fault in the bias network not providing the right bias. This seem more plausible since the whole plot is lowered and not limited to single areas. The newest measurement in green has its bias measured with a multimeter, this does not seem to be the problem either. All the measurements use averaging to reduce noise, the newest uses a higher resolution than previous measurements. This measurement is slow to stabilize at the correct gain, it matches the plot in blue but eventually stabilizes closer to the teal plot. The problem could therefore simply be that the measurement in blue is taken before it has stabilized at the right gain. The newest measurement is assumed to be correct. It has a bandwidth from 2.01-2.26 GHz and 2.39-2.55 GHz, where the highest gain is about 17 dB. The gain in the dip at 2.30 GHz is 13.8 dB. The peak at 1 GHz is now at 10.8 dB. The type of gain measured for the small-signal setup is available gain. For the large-signal measurement, transducer gain is measured. The input and output are assumed matched so that the $G_T = G_A$. If the load is not 50 Ω, then the transducer gain will be lowered. Therefore, the small-signal gain should not be lower than the measured transducer gain. This is another indicator that the blue plot is incorrect.

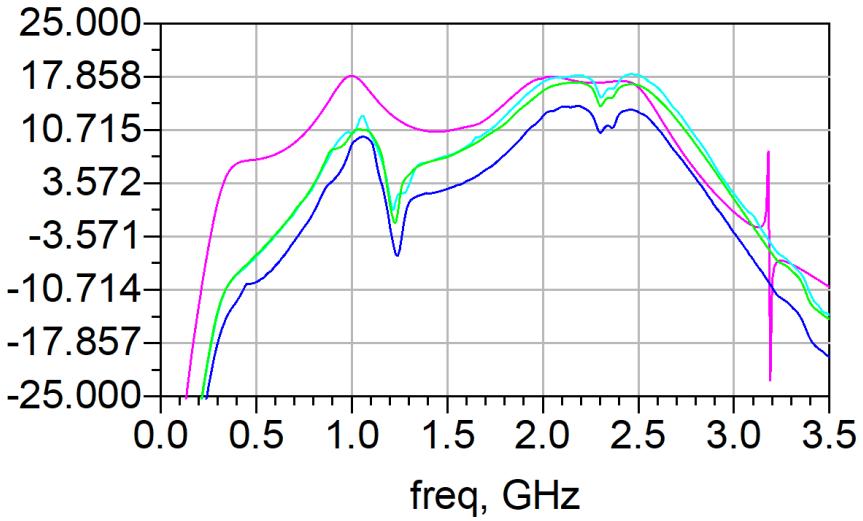


Figure 4.17: S_{21} measurements for physical PA (teal) and second measurement of PA (green) compared with S_{21} from simulation (pink)

4.8 Large-signal analysis

The 1-tone test is a test used to determine the relationship of the input and output power of a device when a single-tone is sent through the device. With the input, output and DC-power measured, it is possible to determine the efficiency of the device as well as its transducer power gain. The 2-tone test is similar and sends two spaced tones through the device. With two tones the phase of these can be measured, this is used to determine the linearity of the device.

Simulations

Simulation results are quite promising for the 1-tone test. Figure 4.18 shows the simulated result for the input versus output power. The highest output power achieved is 41 dBm at 31 dBm input power, this is in deep compression. The output power is over 40 dBm for 28 dBm input power and is therefore within the specification.

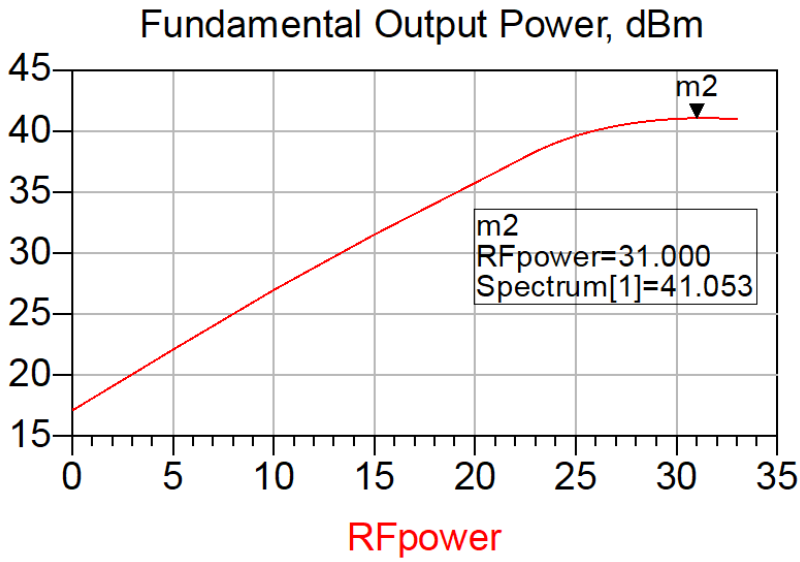


Figure 4.18: Input vs. Output power for 1-tone

The simulated PAE is shown in Figure 4.19. The PAE should be as high as possible to fulfill the specification. The maximum PAE achieved is 74% at 41 dBm output power. As seen in the figure, the efficiency is highest at max output power, if it is driven too hard the efficiency and output power will drop to some extent. This is visible as a little curl at the plots tail in Figure 4.19. The PAE is comparable to the theoretical max efficiency for a class AB which is 78.5%. This may be too good to be true, however this is not achieved with ideal components, but with microstrip and models for real components. If the models are accurate it should be possible to achieve similar results with the real PA.

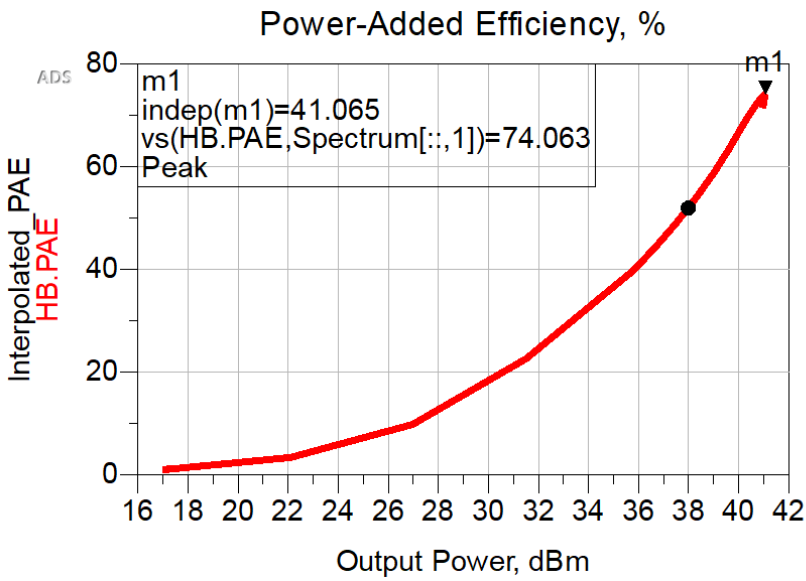


Figure 4.19: PAE for 1-tone

Figure 4.20 is a typical gain curve for a class AB amplifier. For output powers up to 27 dBm it acts as class A, then it gets a slight bend and act like class AB. For this reason, the 1 dB compression point is not where the gain is lowered by 1 dB, but 1 dB lower than the knee of the curve. According to Figure 4.20, this will be around 40 dBm output with gain of about 14 dB.

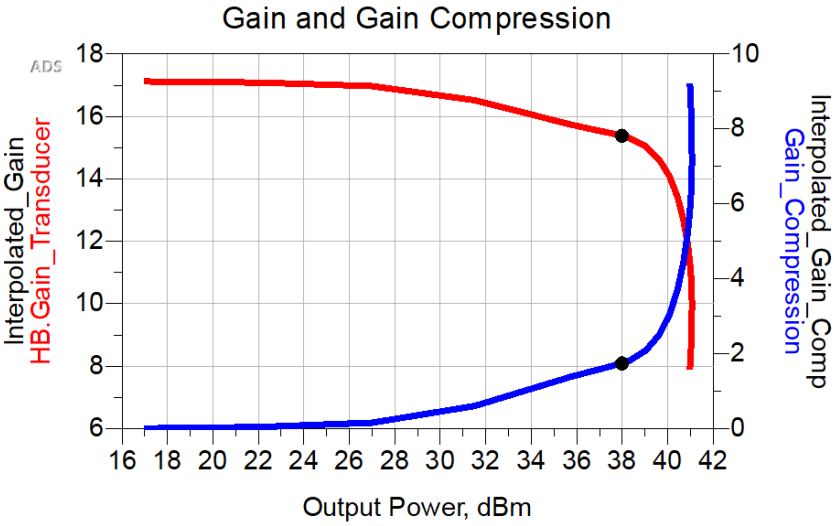


Figure 4.20: Transducer Power Gain for 1-tone

When performing a 2-tone test, the amplifiers nonlinearity will give rise to frequency components near the two tones. The power in these tones is called intermodulation distortion (IMD). The most typical way of measuring this is by measuring the biggest IMD component in comparison to the power in one of the test tones. For better linearity it is desired to have the third-order intermodulation distortion (IMD) as low as possible. Figure 4.21 shows simulated third-order IMD for the PA. The PA will have a 'sweet spot' from 30 to 36 dBm, where increased power has the same linearity. The two tones should also align as much as possible. In the figure there is a blue line and a red line, these are almost identical, the blue line is only vaguely visible.

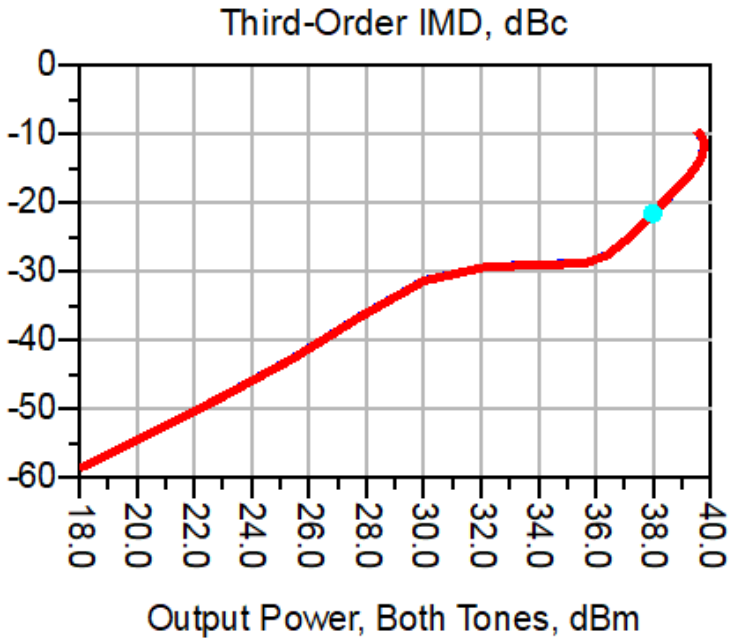


Figure 4.21: Third-order IMD for 2-tone

Lab setup

The lab setup [10] used for the 1 and 2-tone test is seen in Figure 4.22 the setup is more complicated than the one used for small-signal analysis. It consists of a vector signal generator, driver, circulator, couplers, attenuator, load and a spectrum analyzer. A similar setup will be explained in detail in Chapter 6.

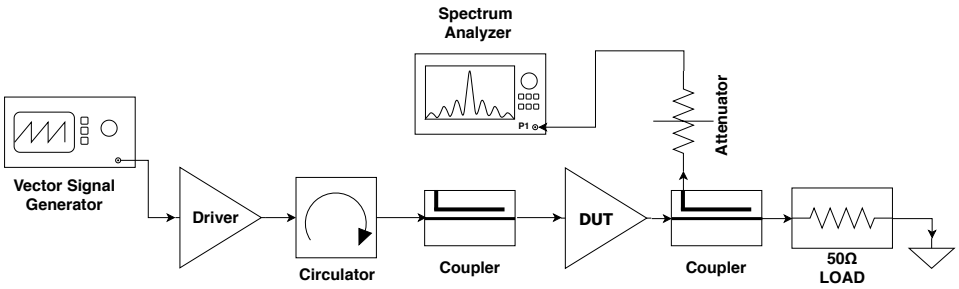


Figure 4.22: Labsetup for 1 and 2-tone test

Measurements

For the simulations of the 1-tone test the specifications are achieved. This is not true for actual measurements. Figure 4.23 shows the measured output power of the PA. The highest output power is about 39dBm at 30 dBm input power, this is 2 dB lower than simulated and below what is required in the specifications. Driving the PA further into compression only leads to lower output and is therefore not recommended. Extra input power will dissipate as heat. Since the output power is lower, PAE should also be considerably lowered since these are dependent on each other.

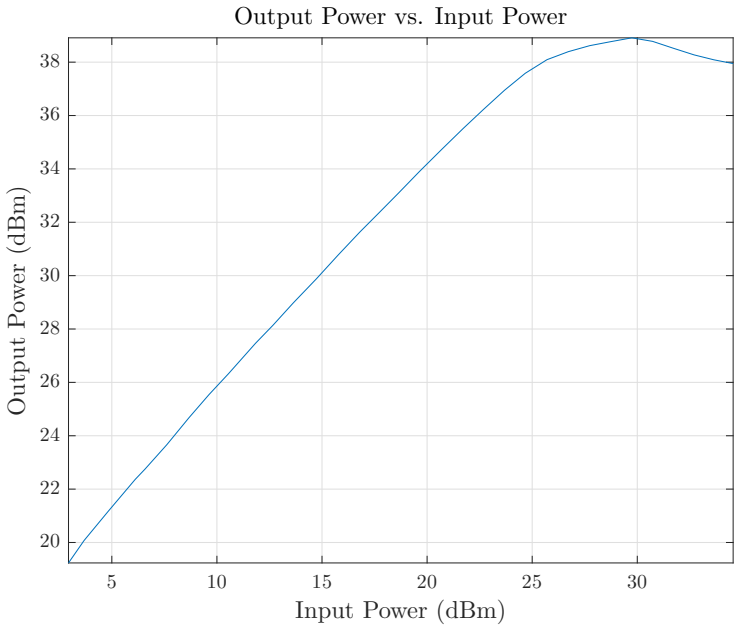


Figure 4.23: Output power result for 1-tone

The measured PAE is seen in Figure 4.24, as expected the PAE is much lower than simulated due to the decrease in output power. The highest PAE is about 57% at 28 dBm input power, this is 17% lower than simulated. Further in compression the PAE is lowered similarly to the output power. There is clearly some unaccounted loss in the PA causing lowered performance. A possible explanation could be that the PA is mismatched. Output power and efficiency is heavily influenced by the output network, it is therefore reasonable to believe that the problem lies there. The transducer power gain seen in Figure 4.25 be-

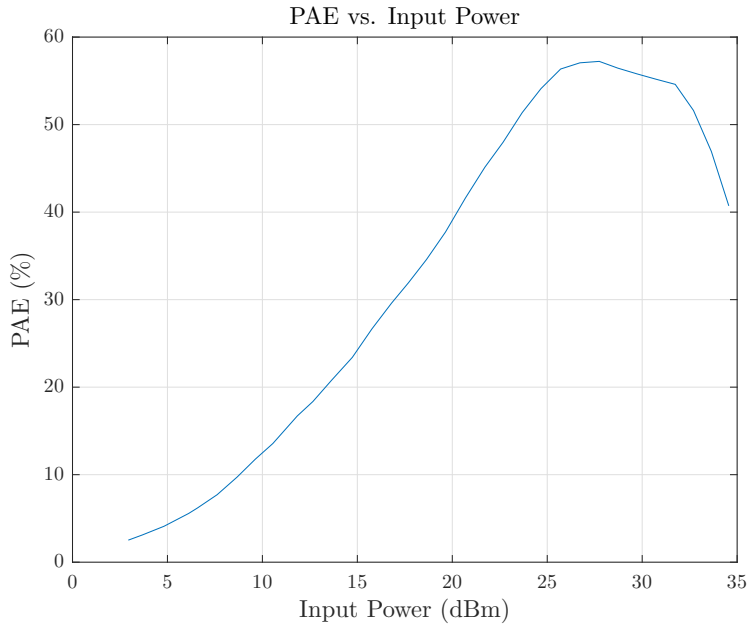


Figure 4.24: PAE results for 1-tone

haves as expected from a class AB. Around 23 dBm it changes from class A to class AB. The gain at the 1 dB compression point is about 12.5 dB with an output power of about 38.5 dBm.

Figure 4.26 shows the 2-tone output power and 3.order IMD versus input power. The two tones are mostly aligned. At saturation 28 dBm input the 3.order IMD is about 17.5 dBc. The curve still retains a 'sweet spot' although not as effective, from 26 to 35 dBm output or 12 to 23 dBm input power.

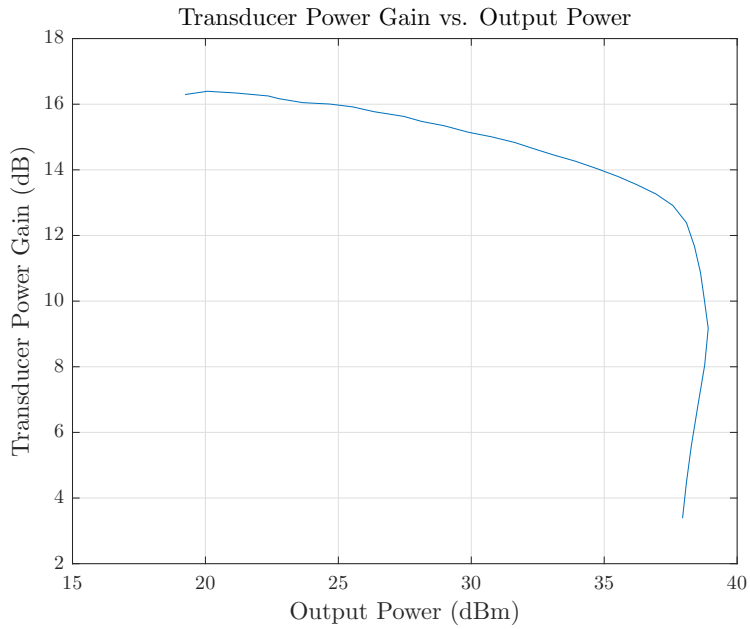


Figure 4.25: Results for 1-tone transducer power gain

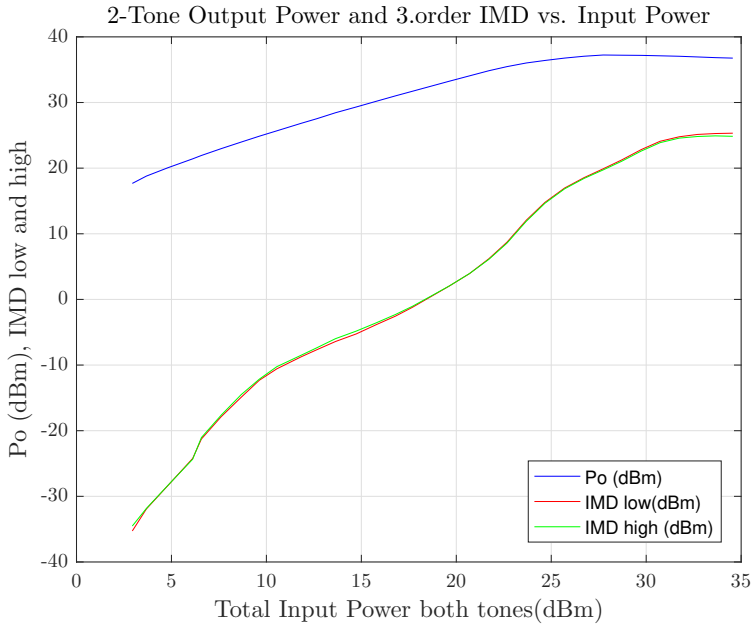


Figure 4.26: Results for 2-tone test

Some of the most important data from the 1-tone test is summarized in Table 4.1. While important data for the 2-tone test is summarized in Table 4.2.

ADS simulation	**Output power**	**PAE**	**Transducer power gain**
Single-tone performance at 28 dBm input power	40.7 dBm	71.9%	12.7 dB
Measurement	**Output power**	**PAE**	**Transducer power gain**
Single-tone performance at 28 dBm input power	38.7 dBm	57%	11 dB

Table 4.1: 1-tone test results referenced to the input power

ADS simulation	**Output power**	**Third Order IMD (low)**	**Third Order IMD (high**
Two-tone performance at 38 dBm output power	38 dBm	-21.5 dBc	-21.48 dBc
Measurement	**Output power**	**Third Order IMD (low)**	**Third Order IMD (high**
Single-tone performance at 38 dBm output power	37.2 dBm	-17.5 dBc	-17.5 dBc

Table 4.2: 2-tone test results referenced to the output power

4.9 Summary and discussion

In this chapter the design method for an RF PA have been presented. Using the design method, a PA was made. The PA performs well in simulations and fulfills all the specifications. The measured results on the other hand does not. Output power is 2dB lower while PAE is down 17%, there is also an unfortunate dip in the small-signal bandwidth. The fulfilled and unfulfilled specifications can be seen in Table 4.3.

Specifications	**ADS Simulation**	**Measurements**
Stability	Unconditionally stable	Stable
400 MHz bandwidth	540 MHz	260 MHz and 160 MHz
Small signal gain of 14 dB or more	17.8 dB	17 dB
Output of at least 40 dBm for 1-tone	41 dBm	39 dBm
PAE as high as possible for 1-tone	Max 74%	Max 57%
Output of at least 38 dBm for 2-tone	40 dBm	37.2 dBm

Table 4.3: Fulfilled and unfulfilled specifications

Lower results are to be expected when going from a simulation to reality, but with good models it should not be this severe. Therefore, the problem could be inaccurate models. Since the most affected aspect is the output power and efficiency, it is probable that there is a problem with the output network. The model for the PCB itself could be part of the problem. There could be differences between the PCB from China and the one produced in-house, characterizing the substrate to get a new model could be an option.

There are also smaller details that could have some influence on the performance. The PCB from China is slightly higher than the one produced at NTNU, about 1-1.5mm. For this reason, the transistor does not have proper contact with the heat sink and the

ground plane. The transistor is therefore screwed tight to the heat sink before soldering it on to the PCB. Because it is stuck to the heat sink the two metal flips of the transistor is bent upwards, which could add a little bit of transmission line around the transistor. Changing lengths around the transistor can be quite sensitive and affect the matching to some degree, whether this is the case remains to be tested. For better contact with the heat sink a thermal paste used for CPU's is added under the transistor, this does seem to give a better result. Dividing the PCB in two is good for troubleshooting but may cause some issues, the primary issue is that they are a bit unstable, they don't seem to have optimal contact. They do have screws to tighten them, but each piece is quite small and does not have enough screw holes, the PCB pieces are slightly bigger than the heat sink making them a bit unstable. Better contact here might improve things, this can be solved by drilling more holes, or using thermal paste between the back plate and the heat sink.

Chapter 5

Characterizing the PCB substrate

Chapter 4 discussed possible errors that can cause the low output power and efficiency of the PA. The most likely reason is believed to be with the substrate model MSUB and the output network. In this chapter a new PCB design is presented. This design is used to characterize the PCB substrate from China. With this a new model for MSUB can be created. This model can then be used when designing a new PA. Section 5.1 explains the motivation behind characterizing the PCB. Section 5.2 goes through the design and presents a device to measure the resulting PCB called a Jigg. In section 5.3 the focus is on calibration with a Jigg. Section 5.4 presents and discusses the measured results. In section 5.5 the new model for MSUB, is created based on the results in section 5.4. Finally in section 5.6 the work is summarized and briefly discussed.

5.1 Motivation

Producing PCBs are not always easy. Institutions such as universities or bigger electronic companies may have the equipment readily available, but for the average consumers or hobbyist the price of the equipment is too steep. Therefore, to get a custom PCB produced, a good option is ordering the PCB online. Companies such as PCBWay offers affordable PCBs of sizes up to 100x100 mm with two layers for only 5 USD. With this the customer gets a total of 5 PCB copies of their design. More options are available but are more expensive. The PCB for the first PA is produced in China, ordering is done through PCBWays website `pcbway.com`.

For this to be a viable option, it is important that the performance of the design, seen in simulations matches the actual PCB being produced, at least to a certain extent. Based on the results for this PA, the simulated and measured performance are significantly different. If this is generally the case, then future designs will not be able to achieve peak performance and will always differ significantly from their simulated performance. The reason for the difference is because the models used in ADS does not describe reality well enough. The models for the components might be off or the model for the PCB substrate itself could be off. The ADS-models for the components are provided by the manufacturer,

these have been thoroughly characterized and should be quite accurate. The components typically have a tolerance of $\pm 5\%$. However, tuning these in ADS, does not have enough effect on output power and efficiency to account for the reduced performance. What does have a great impact on the design however, is the relative permittivity ϵ_r and the loss factor $tand$ of the substrate. This is evident when tuning said variables for the Microstrip Substrate (MSUB) model in ADS.

The output power of an amplifier is highly dependent on the output matching network. It is therefore reason to believe that there is a problem with the output network of the PA. An inaccurate MSUB model could be the reason why. If the substrate model is incorrect, it could cause a mismatch in the output network causing a different output power than expected. This does seem like a plausible explanation for the lowered performance. To test this hypothesis, a new model for MSUB must be found. This is done through characterization of the substrate. Assuming this works, a new output network using the new model can be made and tested with the PA. If the new performance of the PA better matches simulations, then the hypothesis will be strengthened.

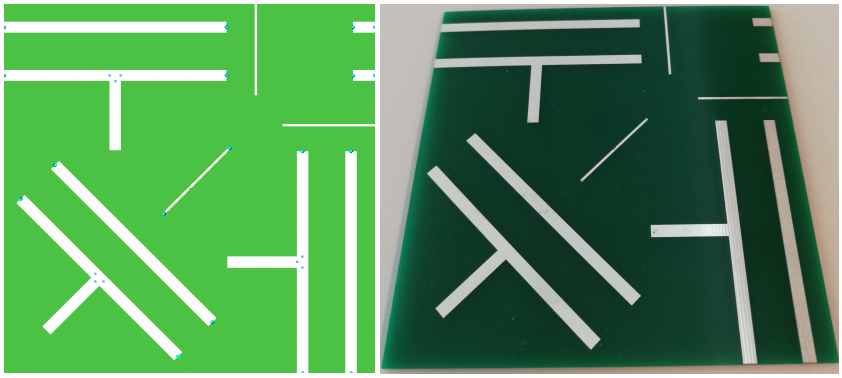
If the error is in the substrate model, then finding a new model is not only essential for this PA, but also every other future project using FR-4 and this manufacturer. Previous PCBs using the same FR-4 model, have had a significant reduction in output and efficiency. These have been made in-house. If the substrate from China and the one from NTNU is similar, it could potentially improve performance of future projects produced in-house as well. The new model will therefore be invaluable to students, professors and hobbyists alike. To determine the new model's validity, it would require it to be used in several projects, and get better results compared to what is achieved with the older model.

5.2 Design

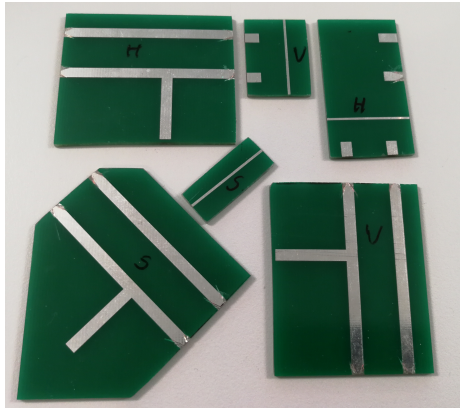
The design is produced from the same substrate as the PA and by the same manufacturer, its sole purpose is characterization of the substrate. The PCB is used to measure S-parameters for:

- 50 Ω line
- 50 Ω line with a $\frac{\lambda}{4}$ shunt line
- 100 Ω line
- Different orientations of these

The substrate is FR-4. FR-4 is a NEMA grade designation for glass-reinforced epoxy laminate material. FR-4 is a composite material composed of woven fiberglass cloth with an epoxy resin binder that is flame resistant. Because it is woven it is possible to see the direction of the weave in the PCB. The transmission lines are placed in three different orientations to determine if this influences the performance of the design. Three identical designs can be seen in Figure 5.1 with the orientations; horizontal, vertical and diagonal. In order to make the conditions of the substrate as similar as possible to the PA design, the PCB has a solder mask everywhere but the transmission lines, while the transmission lines and ground plane have a thin coating of tin.



(a) Layout for PCB **(b)** Manufactured FR-4 PCB



(c) Cut out PCB pieces

Figure 5.1: Design for characterization of PCB, produced in China through `www.pcbway.com`

Each section of the PCB is tested using the Jigg seen in Figure 5.2. The Jigg is used to test devices without soldering connectors to the device. It has clamps to hold PCBs, these are operated by the black levers seen in Figure 5.2. Adjustable screws allow PCBs of different sizes to fit. It can be adjusted in X and Y-direction. It has two pins to connect with the input and output of a device. To test each separate section of the PCB in Figure 5.1b, the PCB must be cut up as seen in Figure 5.1c. The biggest pieces are originally too long to fit in the Jigg. The maximum length between the PCB input and output can only be 50 mm. For this reason, the 50 Ω lines with a shunt line, are asymmetrical after cutting. Future design if any, must take this into account. The connection pin of the Jigg is no more than 1 mm in width. It is surrounded by a semicircle of space as seen in Figure 5.3, the area outside the circle is grounded. The 50 Ω lines must therefore be trimmed to fit within this area, otherwise the measurements will show a shortage to ground.

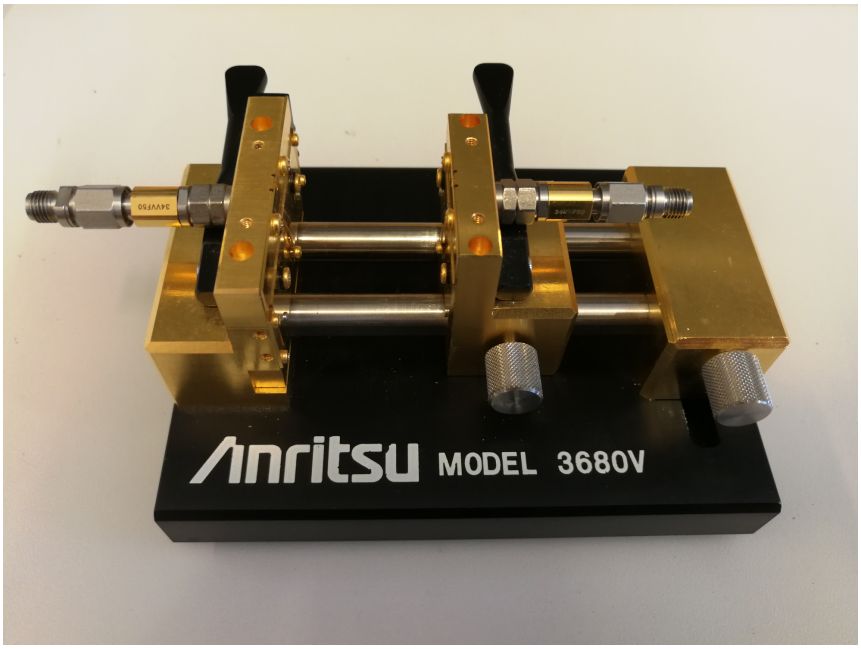


Figure 5.2: Overview of the Jigg

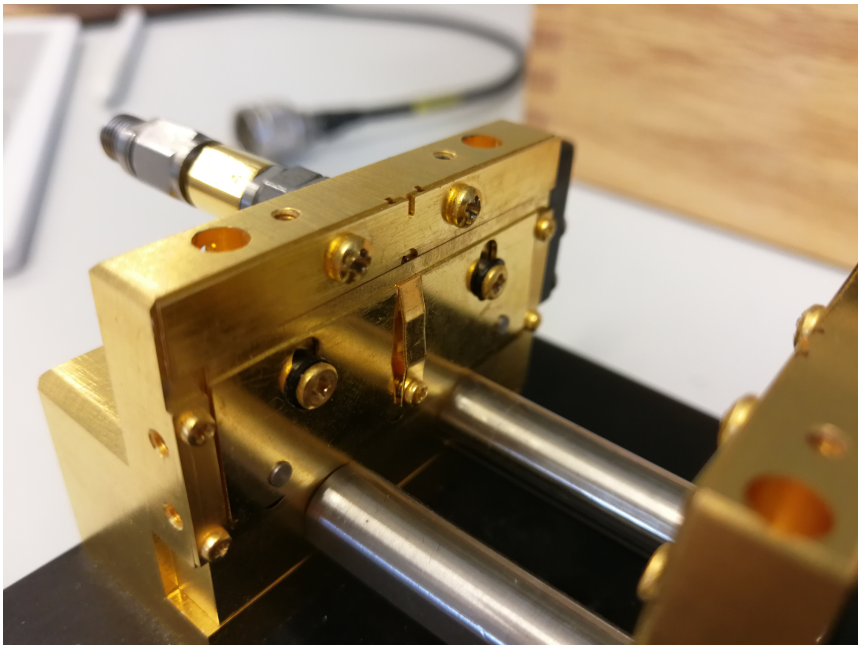


Figure 5.3: Input of Jigg

5.3 Calibration

For the measurement, a VNA is used. The setup is similar to Figure 4.16 where the DUT is in a Jigg. The calibration technique used is SOLT (TOSM for Rohde Schwarz equipment). When measuring PA prototypes, an attenuator is always attached to the output of the PA. PAs can be unstable and incur powerful oscillations, the attenuator is there to protect the VNA from high power. However, the devices tested during characterization are all passive, an attenuator is therefore not necessary.

When measuring the DUT, it is desirable to have the measurement referenced to the DUTs ports. This is normally done though calibration. Calibration removes the added length from the cables between the DUT and the VNA. With a Jigg however, as seen in Figure 5.2 an extra length is added to both sides of the DUT. The extra length adds a phase shift to the measurements. This is not calibrated away with the VNA alone but can easily be fixed in post simulation using ADS. The measured open and short circuit for the Jigg, can be seen in the Smith charts in Figure 5.4.

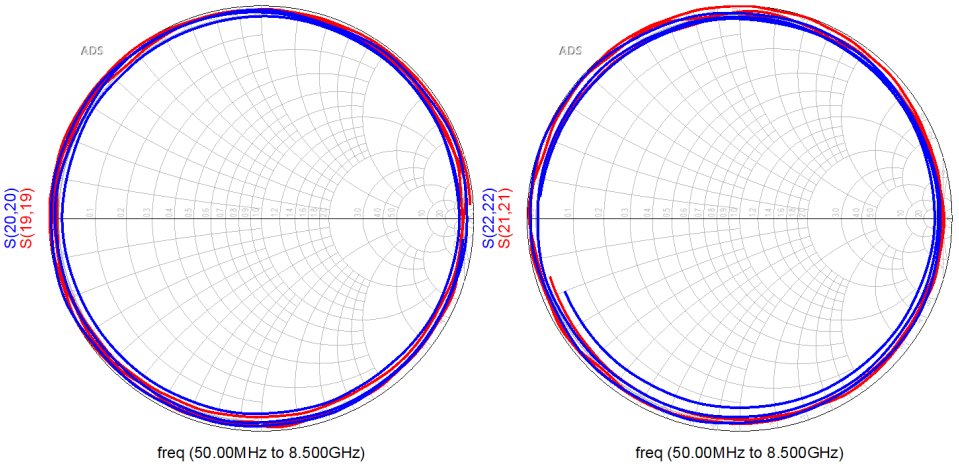


Figure 5.4: Jigg open and short before calibration

The added length is quite significant. By using ideal transmission lines with negative length on either sides of the DUT as seen in Figure 5.5 this problem is fixed. Figure 5.6 is the result after adding the ideal lines, the new calibrated open is seen on the left Smith Chart, while the calibrated short is seen on the right side. Any further measurements done with the Jigg can be represented in ADS with the same setup and same length.

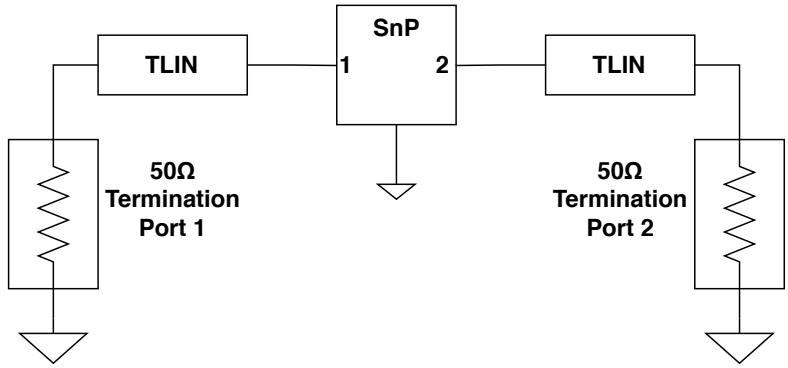


Figure 5.5: Jigg setup in ADS to fix calibration problem. SnP is the measured s-parameter of the DUT

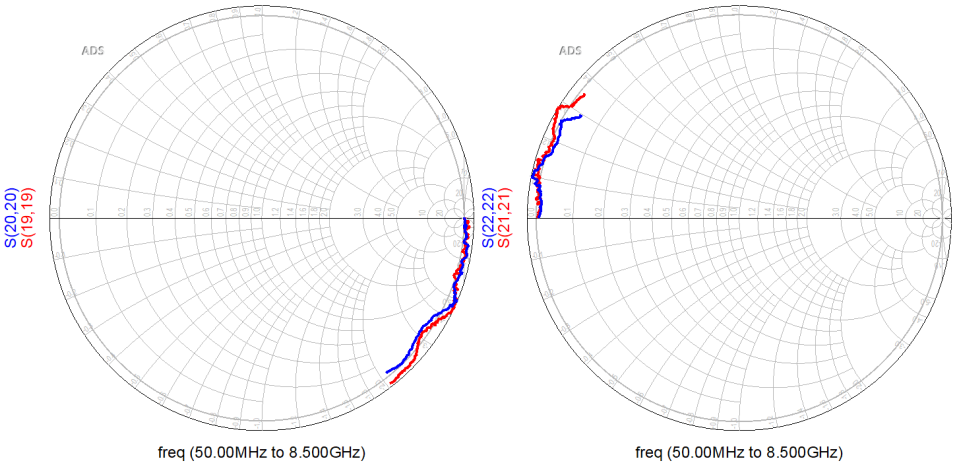


Figure 5.6: Jigg open and short after calibration in ADS

5.4 Results

In this section the three designs are tested for the three orientations; vertical, diagonal and horizontal. First for 50 Ω line, 50 Ω line with a $\frac{\lambda}{4}$ shunt and finally for a 100 Ω line. the three orientations of the same design is tested to see if placement on the weave of the glass fiber in the PCB has any affect on the results. Based on the results this does not seem to be the case. There is however parasitic effects in the Jigg connection.

50 Ω line

Figure 5.7 shows the measured S_{11} parameters. Figure 5.8 shows the measured S_{21} parameters.

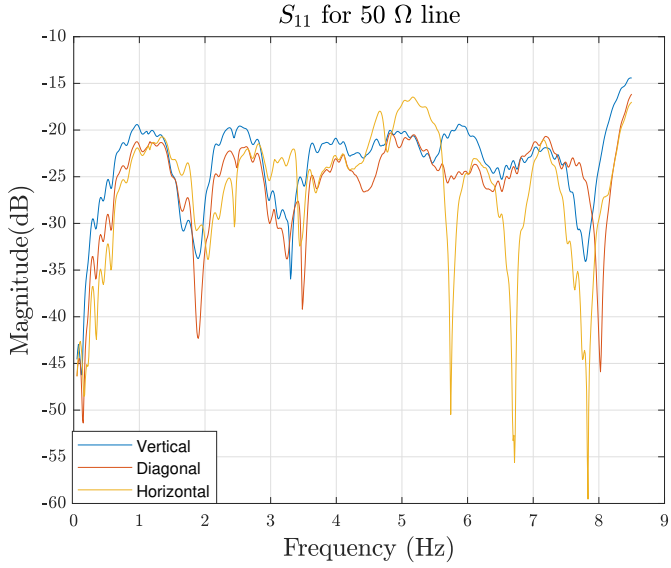


Figure 5.7: S_{11} parameter for 50 Ω transmission lines

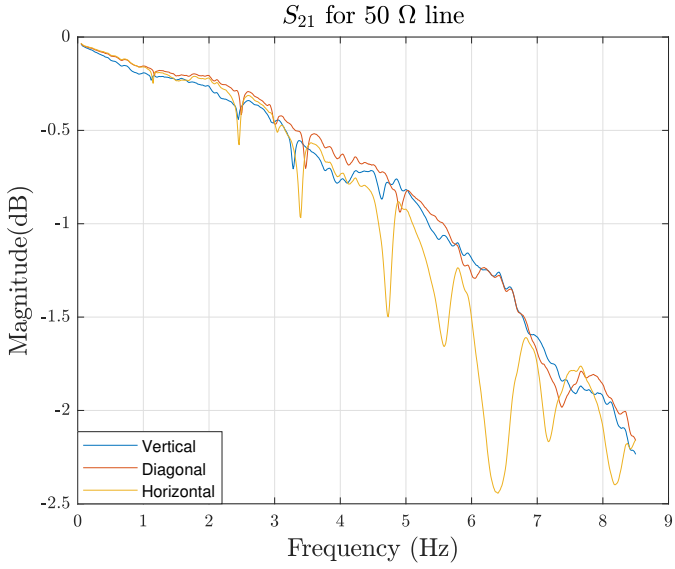


Figure 5.8: S_{21} parameter for 50 Ω transmission lines

All three orientations have similar shape, the vertical and diagonal pieces in particular are nearly identical. The horizontal piece is similar for the lower frequencies until around 4.5 GHz, from there it has increasingly stronger and more frequent resonances compared to the other two. It is worth noting the phase shift between the three orientations. It is only a slight shift, but still noticeable. The length of each piece is listed in Table 5.1. The length of the transmission lines are slightly different, which explains the phase shift. The larger resonances for the horizontal piece, is likely because of parasitic inductance and capacitance. The edge of the horizontal piece is not entirely straight. When the piece is in the Jigg, there will be some free space near the connector and PCB which can give rise to parasitic effects because of bad contact. Another reason for the discrepancy could be stress in the material itself, the horizontal piece was slightly bent when cut to fit the Jigg.

Transmission line	**Orientation**	**Length [mm]**
50 Ω	Vertical	50.0
50 Ω	Diagonal	49.2
50 Ω	Horizontal	48.6

Table 5.1: Length of each 50 Ω PCB-piece

50 Ω line with a $\frac{\lambda}{4}$ shunt line

The pieces for the 50 Ω line with a $\frac{\lambda}{4}$ shunt line are the same as in Table 5.1. The discrepancy seen in Figure 5.9 and Figure 5.10 is comparable to what is seen for the 50 Ω line. There is a slight phase shift and the horizontal piece stands out.

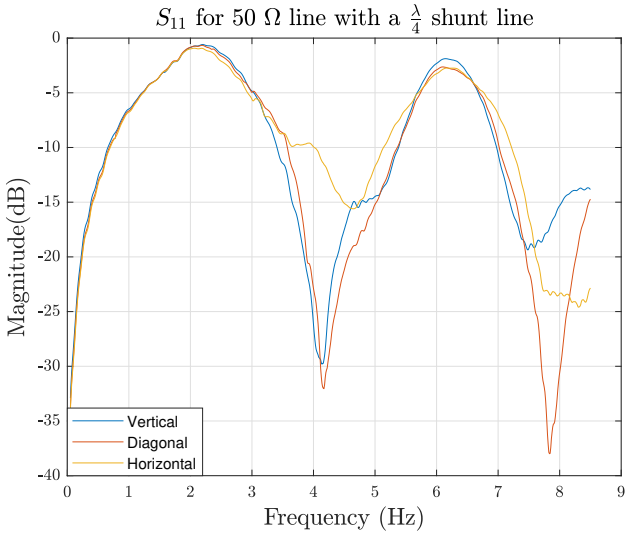


Figure 5.9: S_{11} parameter for 50 Ω line with a $\frac{\lambda}{4}$ shunt line

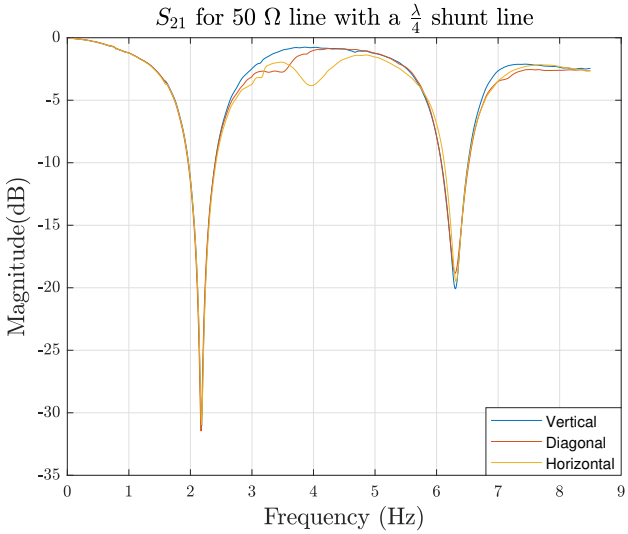


Figure 5.10: S_{21} parameter for 50 Ω line with a $\frac{\lambda}{4}$ shunt line

100 Ω line

Among the lines tested, the 100 Ω lines are the ones that are most similar for S_{11} as seen in Figure 5.11. Neither these are the same length, which gives a phase shift clearly seen near the resonances. The length of each piece is in Table 5.2. The horizontal is the shortest followed by diagonal and then vertical. The lines are about the same width as the pins in the Jigg. They are therefore not trimmed and should be the ones with the best contact and therefore least parasitic effects. The three lines are not perfectly similar as seen in Figure 5.12 likely because edges are not perfectly straight. However, using these results and the results from the 50 Ω lines as a basis for the characterization, it should be possible to reach a good enough approximation for the substrate.

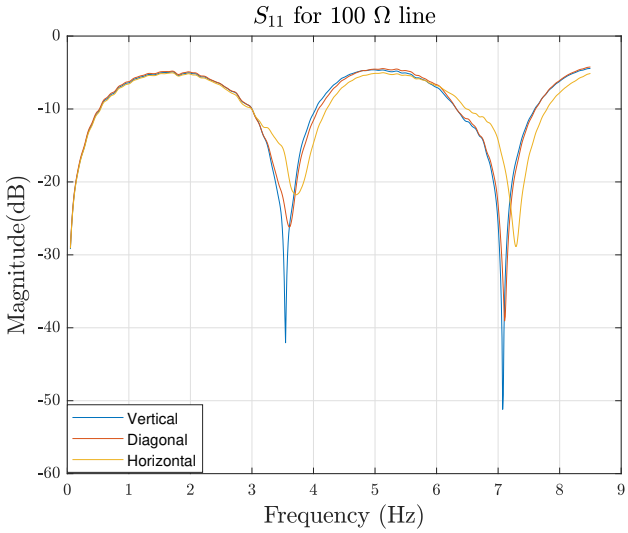


Figure 5.11: S_{11} parameter for 100 Ω transmission lines

Transmission line	Orientation	Length [mm]
100 Ω	Vertical	25.1
100 Ω	Diagonal	25.0
100 Ω	Horizontal	24.4

Table 5.2: Length of each 100 Ω PCB-piece

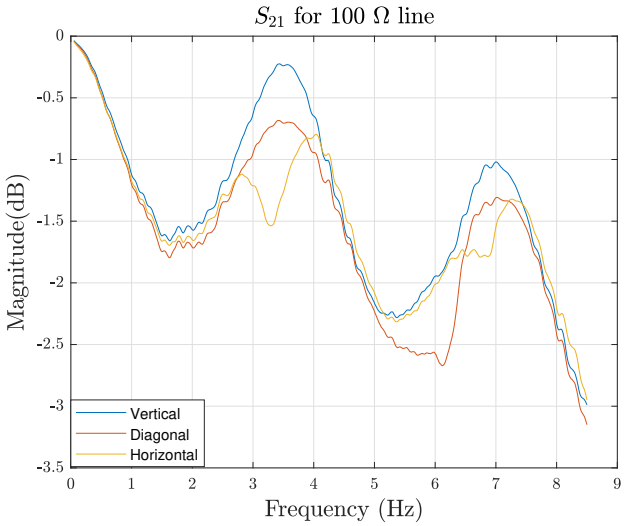


Figure 5.12: S_{21} parameter for 100 Ω transmission lines

5.5 Jigg parameters

When characterizing anything, a model is made to approximately behave the same way as the real thing would. The reason to use transmission lines by themselves, is because of simplicity. It is easier to model something simple, with as few variables as possible. For best accuracy, it is necessary to model the Jiggs behavior and the substrate, both is important. The characterization is based upon the results from the diagonal and vertical measurements. These are used because of the similarity in the measured results. The model for the Jigg is seen in Figure 5.13. The transmission lines on each side is used to compensate for the added length during calibration. The connection between the DUT and Jigg is a transition from coax-pin to microstrip and microstrip to coax-pin. This means a transition in modes, from TEM to QTEM and back. This effect is modeled with the capacitors and inductors on either side of the DUT. Different topologies have been tested, however this is the best one found so far. The capacitors are quite small, in the attofarad [aF] range. The Inductors are bigger and are in the picohenry [pH] range. The DUT in the middle is a microstrip line, but can later be switched with other devices. The microstrip line has a MSUB with variable permittivity ϵ_r and loss factor $tand$. Through optimization and manual tuning of these variables, a characteristic that fit the plots quite well is found. It is not perfect but seem to give a better approximation than with the old MSUB model. Figure 5.14 shows the measured S_{11} for a vertical 50 Ω line (blue). Both the red and green plots are identical microstrip lines, simulated with the same MSUB-model. The only difference is that the red plot uses the setup in Figure 5.13, while the green does not account for the transition effect and therefore does not have the capacitors or inductors in its model. A combination of optimizing with the results from 50 ohm and 100 ohm in vertical and diagonal direction, gives the new MSUB parameters in Table 5.3.

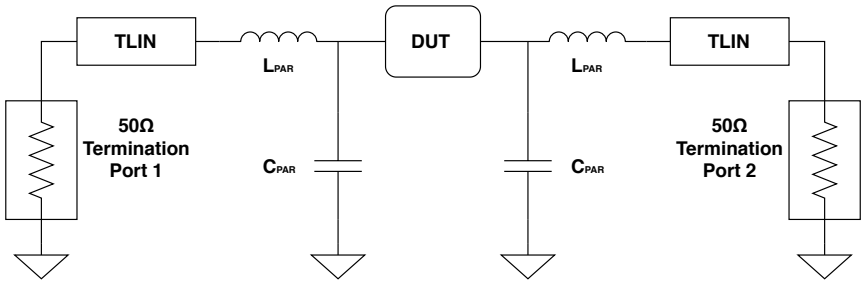


Figure 5.13: Jigg characterization model

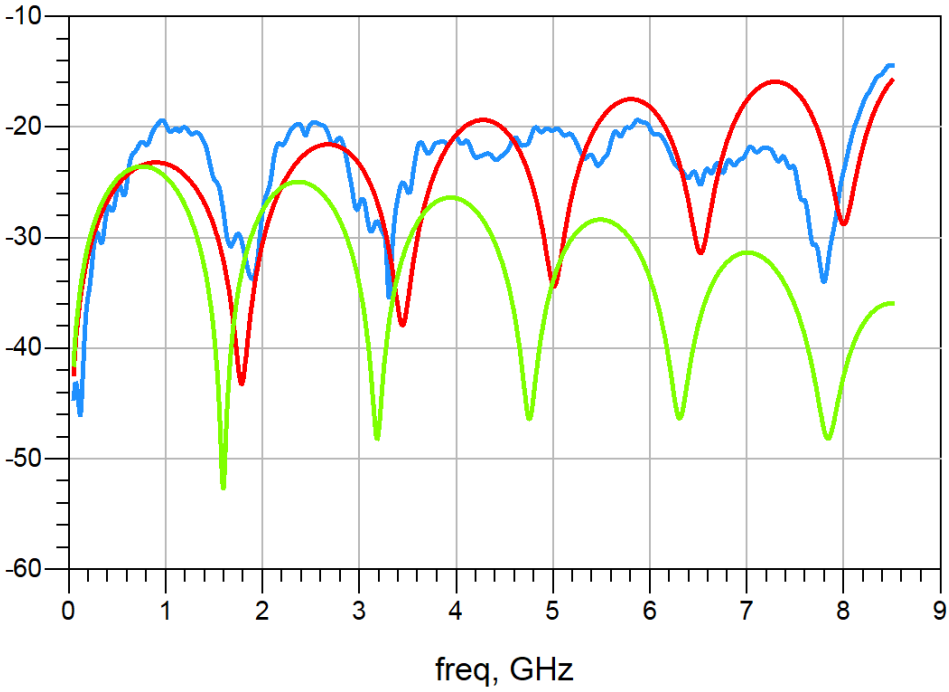


Figure 5.14: Measured S_{11} (blue), simulated microstrip with transition effects (red), simulated microstrip without transition effects (green). Red has increased reflection with frequency, the opposite is true for green

Height	ϵ_r	μ_r	Conductivity	Thickness	Loss Tangent
$1.52 * 10^{-3} m$	$4.7^{F}/_{m}$	$1.0^{H}/_{m}$	$5.96 * 10^{7} s$	$35 * 10^{-6} m$	0.025

Table 5.3: Substrate characteristics for new MSUB

MSUB comparison

To see the difference or similarity between the substrate made in China and the one made in-house, an identical output network is produced in-house. If the two is similar enough, the new model can be used for both, otherwise the new output network must be produced in China with the new MSUB. Figure 5.15 and Figure 5.16 show the S-parameters of the two. The measured output network produced in China is seen in red, the one produced at NTNU is seen in blue. Other than very small differences the two are identical. Previous measurement had a resonance at 3.4 GHz for the China-PCB, but in newer measurements this is suddenly gone, why that is, is unknown. The two PCBs are not entirely identical physically, the one from China has a layer of tin around its via holes, the transmission lines are also covered in tin. Since this is the only difference and the resonance is suddenly gone, it is assumed the model is valid for both substrates. The new substrate model is not much different from the old MSUB, but seem to match the result slightly better. The simulated output network with old and new MSUB can be seen in the figures as teal and pink, respectively.

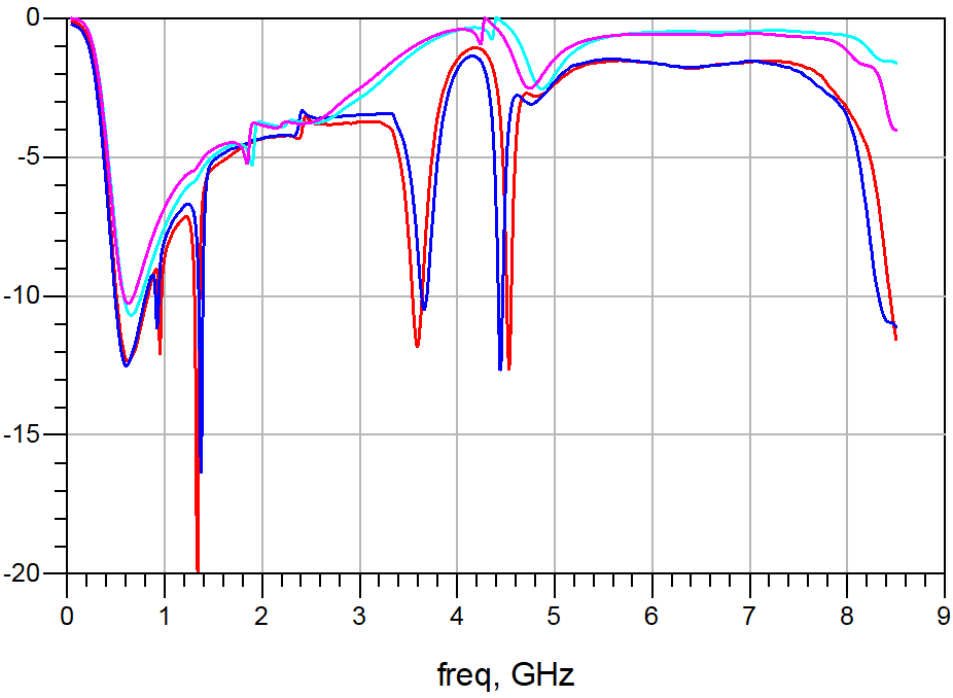


Figure 5.15: S_{11} results for output networks. China-PCB measurement (red), NTNU-PCB measurement (blue), simulated with old MSUB (teal), simulated with new MSUB(pink)

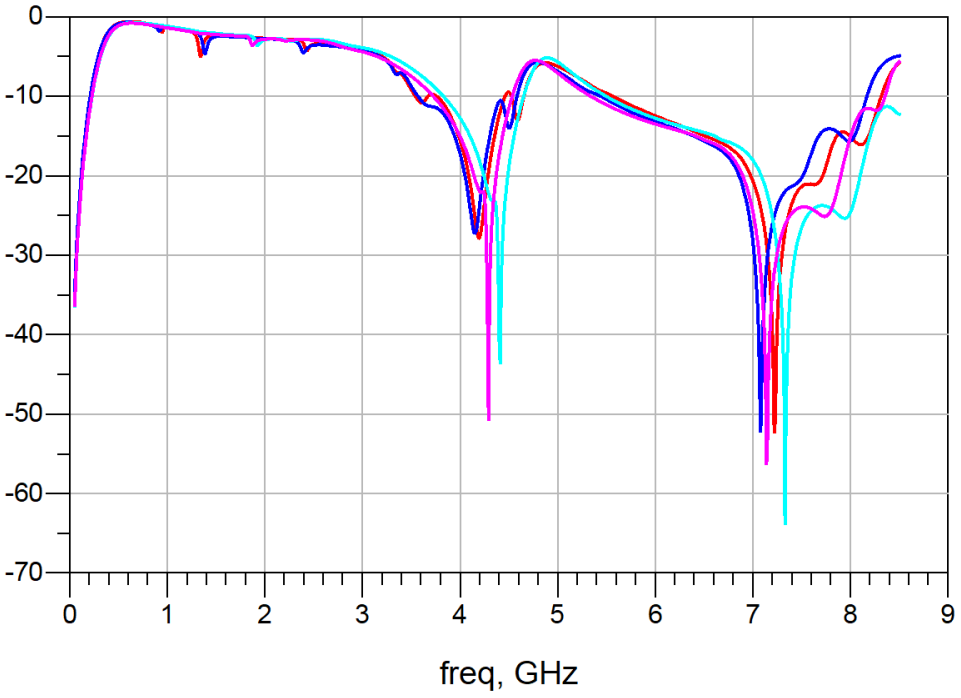


Figure 5.16: S_{21} results for output networks. China-PCB measurement (red), NTNU-PCB measurement (blue), simulated with old MSUB (teal), simulated with new MSUB(pink)

MSUB simulation

The new MSUB is tested with the original design in ADS. The hypothesis is that the simulations will better fit with the measured result. A comparison of the most important results is summarized in Table 5.4. The results are promising for the new MSUB and do fit the measured results better than the original.

ADS simulations	MSUB	Input power	Output Power	PAE	Transducer Gain
Single tone	Original	31 dBm	41.05 dBm	74.3%	9.6 dB
Single tone	New	31 dBm	40.58 dBm	65.9%	9.2 dB
Measured Results	**Substrate**	**Input power**	**Output Power**	**PAE**	**Transducer Gain**
Single tone	China	28 dBm	38.7 dBm	57%	10 dB

Table 5.4: Large signal results for different MSUB. The results are referenced to max output power achieved

5.6 Summary and discussion

In this chapter a design for characterizing the FR-4 substrate of a PA has been presented. The motivation behind this was to determine if an inaccurate substrate model was the reason for poor PA performance. Another reason was to compare a PCB produced in China to one produced in-house to see if they produce different results. To determine if certain placement on the PCB played a role in its behavior, three identical transmission line design were placed in three different orientations. The designs were cut into separate pieces and measured using a VNA and a device called a Jigg. Measurement, however, shows that placing the designs in horizontal, vertical and diagonal orientations on the PCB weave make little difference. Differences that did occur, are attributed to other factors such as shape of PCB-pieces and possible damage to certain pieces when they were cut. A model was made for the Jigg as well as the MSUB based on results from 50 Ω and 100 Ω transmission lines. The new MSUB-model has slightly higher permittivity and loss factor compared to the original. Simulations with the new MSUB-model does give lower performance for the PA, closer to what has been measured. Based on this, it is very plausible that the performance of the PA can be improved by redesigning the output network with the newly acquired MSUB. Two output networks were also tested and compared, one from China and one made in-house. Measurement show that they are nearly indistinguishable from one another. The new output network should therefore have the same performance regardless of it being produced in-house or in China. The results are only acquired from a small sample and may therefore not be applicable for all designs. If the new model does give better results for a newly designed PA, it should also be used with future projects to determine if it is more accurate than the original model.

Chapter 6

Final design and results

In this chapter the final design for the PA is discussed. This version uses the new model for MSUB characterized in chapter 5. In section 6.1 possible solutions for increasing output power and efficiency is discussed briefly. A final design is later presented with the most important results from simulations in ADS. In section 6.2 the measurements for the new PA is presented and discussed. This section also contains the lab setup for each type of measurements, small-signal and large-signal analysis. Finally measurements of the new design is compared with the previous design using the same lab setup.

6.1 Redesigning the output network

The final design is made using the new MSUB-model. The value of its parameters is presented in Table 5.3. Since the substrate produced in China and the one produced in-house only have slight differences, it is assumed that the model is valid for both. The new design is therefore produced in-house, to save time and money.

The performance of the old design has about 2.3 dB less output power compared to simulations. PAE is dependent on output power and is therefore lower than simulated. To increase these two aspects, the easiest and most effective way is to modify the output network.

The new design does not require much redesigning. By optimizing with the new MSUB, only small differences in transmission lines are changed for the output network. The original input network is reused as is, only the DC-block is changed for better matching. The capacitors in the bias networks are altered to improve dips in the small-signal bandwidth. It is believed that two Johanson capacitors in parallel cause a resonance inside the usable band. To explore this possibility, the Johanson capacitor values are changed.

6.2 Small-signal analysis

Lab setup

To measure the S-parameters of the PA a VNA from Rohde & Schwarz is used. The lab setup is the same as in Chapter 4 seen in Figure 4.16.

Results

Figure 6.1 shows S_{21} for the improved PA. With the new MSUB and new design, the simulated result in pink and the measured result in teal is nearly spot on. There is still a resonance in the band however. The resonance has been shifted down in frequency while the usable band is pushed into slightly higher frequencies. The gain is about 17.3 dB around the center frequency 2.2 GHz. There is a usable band of 120 MHz with 1 dB ripple around the center frequency i.e. 2.14 GHz to 2.26 GHz. However, there is a band from 2.15 GHz to 2.54 GHz, this has less than 1 dB ripple and the highest gain is 17.74 dB. With a center frequency at 2.345 GHz, this is a bandwidth of 390 MHz. There is also a top before the resonance, this has a gain of 18.26 dB. Around the 1 GHz frequency there is an unwanted peak. The peak has gain of 18.7 dB and a significant bandwidth. Compared to the original design, the measured result does match the simulated result much better, but so does the unwanted peak around 1 GHz. Since changing the bias capacitor values only shifted the resonance in the band, another approach could be attempted. To fix the problem, a possible solution could be to only use a single Johanson capacitor and not two. This has not been attempted but should be done in the future. If the resonance is removed, then the usable bandwidth around the center frequency of 2.2 GHz should be at least 400 MHz. This would fulfil the requirements specified in Chapter 3.

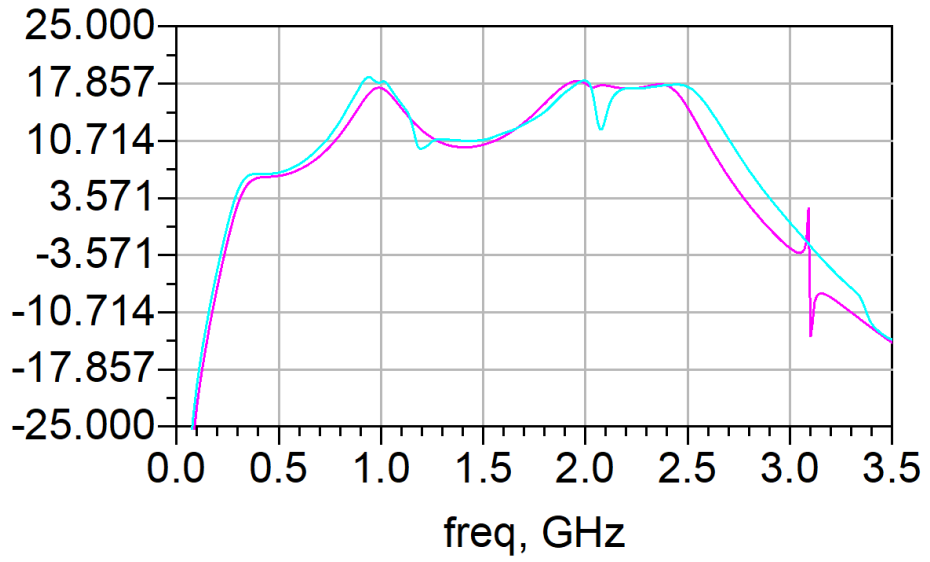


Figure 6.1: Simulated S_{21} (pink) and measured S_{21} (teal) for the new PA

6.3 Large-signal analysis

Once the design is optimized with the new MSUB, very similar results compared to the original PA is achieved. The ADS plots are therefore not presented here, similar plots are found in Chapter 4. The most important simulated and measured results for the one-tone test are found in Table 6.1. The table compares results from both PAs.

Lab setup

The lab setup used to measure the PA is seen in Figure 6.2. It consists of a vector signal generator, driver, circulator, couplers, attenuators, load and a power meter. A MATLAB script controls the vector signal generator as well as the power meter. All the measuring data aquired is stored via the MATLAB script. The **vector signal generator** produces

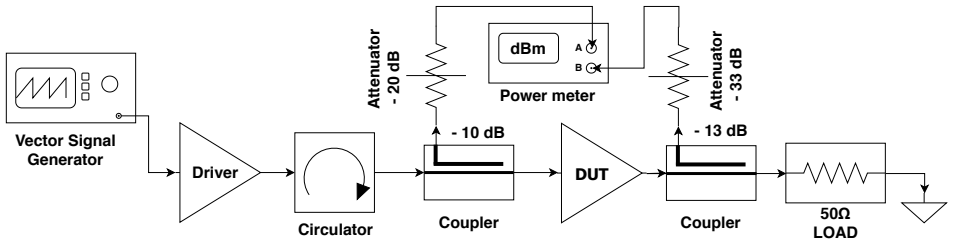


Figure 6.2: Lab setup for Large-signal analysis

the RF input signal for the DUT. The vector signal generator can generate a variety of complex signals such as QAM, QPSK, OFDM etc. In this setup a sinus wave with a set frequency is used. The frequency used, is the center frequency of the DUT. It is necessary to test the device for multiple power levels in order to characterize its PAE and output power. The generator therefore sweeps a given interval from low input power, until the DUT is in compression. However, the generator can only deliver a signal with a maximum of 20 dBm. The amount of input power is not sufficient to drive this particular DUT into compression, further amplification is therefore needed.

The **driver** is a type of broadband amplifier, it has good linearity and is used to amplify the RF input signal before it reaches the DUT. Between the driver and DUT, there is a device called a **circulator**. This device ensures any RF signal reflected from the DUT will not be reflected toward the driver but will dissipate in the circulator. The circulator acts like a diode, it is unidirectional. Without the circulator between the driver and the DUT, the reflected power from the DUT could affect the driver and make it less linear, potentially ruining the measurement data.

On either side of the DUT, **couplers** are placed. The couplers have multiple ports, one is usually terminated in 50 Ω. Two of the ports lets a signal pass through unobstructed, while a coupled attenuated version of this signal goes through the last port. The **power meter** measures the RF power before it enters the DUT. The measured signal is already attenuated, but the signal is still too powerful for the instrument to handle. To protect the instrument from high power, **attenuators** are added. The signal the power meter receives before and after the DUT is therefore much weaker than the actual signal.

Calibration

Because the signal reaching the power meter is heavily attenuated, it is necessary with a calibration of the setup. This will ensure the measured power is referenced to the input and output of the DUT. For this calibration it is only necessary to find a correction factor for the attenuation caused by the couplers and attenuators on each side of the DUT. Once this is found, the correction factor can be added to the script running the measurements. Small-signal analysis is performed on the couplers with their attenuators connected. The total attenuation at the specified center frequency, is used as a correction factor for the signal measured at the input and output of the DUT. By doing the calibration this way, the couplers only need to be measured once. What happens in the stages before the coupler is therefore not necessary for the calibration. For the lab setup in Figure 6.2 the input signal measured is attenuated by 31 dB before reaching the power meter, the input correction factor is therefore 31 dB. Similarly, for the output, the attenuation factor is about 47 dB at the center frequency, the output correction factor is therefore 47 dB. The attenuation is slightly different for other frequencies. Some added attenuation is also due to the connection between coupler and attenuator, these have extra transitions to comply with the sexes of the connectors.

Results

The results are for V_g=-2.68 V and V_d=28 V since this is what gives the drain current I_d, that the PA is designed for. The setup however, measures for an array of different V_g and V_d. This is done in order to create a tracking function later. Tracking functions are discussed in Chapter 7. The setup is also used with the original PA (OPA), to be able to compare the two PAs under the same conditions. The setup has only been tested for the 1-tone test so far. Since the 2-tone test is not performed for the new PA (NPA), it is assumed that the linear behavior is close to simulations. This however, should be measured in future work since simulated and measured results usually differ for the worse.

Output power vs input power

The result for the Pin vs Pout for the NPA can be seen in Figure 6.3. The output power has increased significantly. The output power at 30.5 dBm input power, is 41.05 dBm. The result for the Pin vs Pout for the OPA can be seen in Figure 6.4. Here the output power at 29 dBm input power, is only 38.1 dBm. The way the script for the setup is written, it will stop measuring if the transducer gain is in deep compression, this is to protect the transistor from overheating. The OPA therefore has very little gain on higher input and is not displayed. It could still have better output power, but likely very little. Based on this the max output power is about 3 dB higher for the NPA compared to the OPA. The PAE should also be considerably better since the output power is increased.

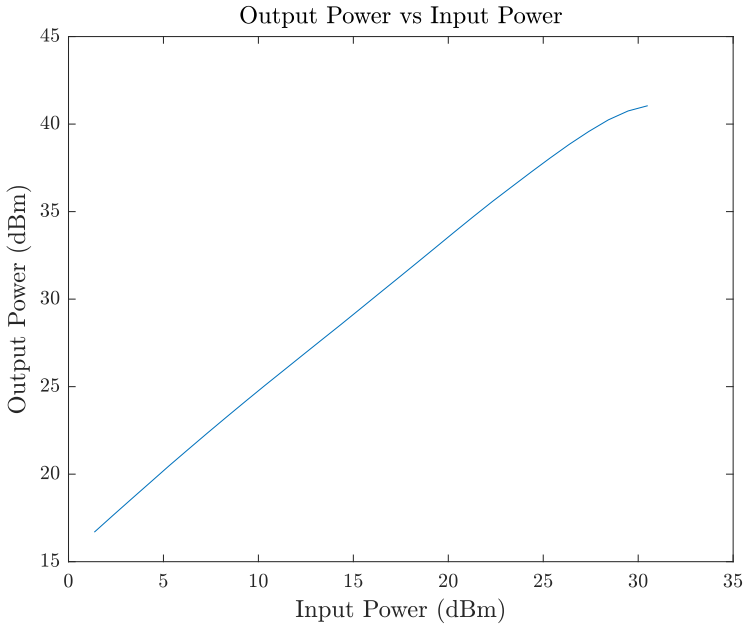


Figure 6.3: Measured output vs input power for the new PA

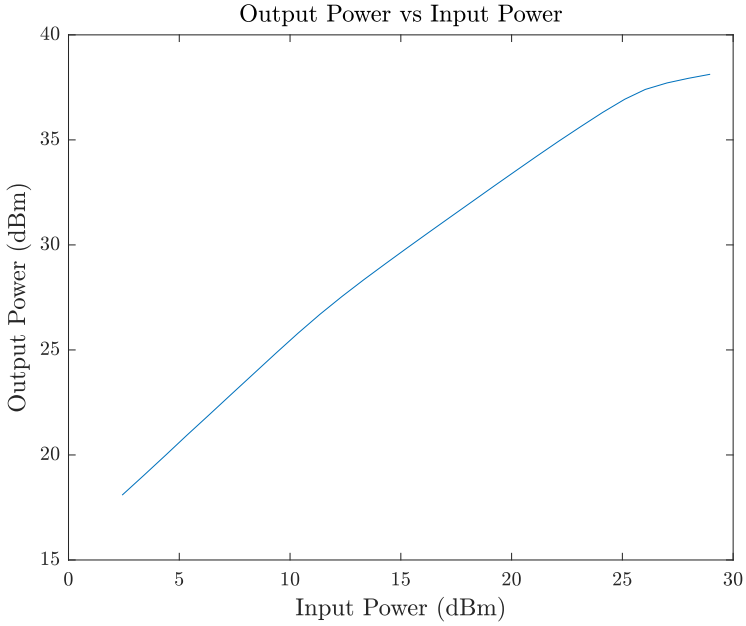


Figure 6.4: Measured output vs input power for the original PA

PAE

The results for the PAE of the NPA can be seen in Figure 6.5. The PAE has increased to 71.3%, at an input power of 30.5 dBm. The result is very promising, being only 3.6% from the simulated result. The results for the PAE of the OPA can be seen in Figure 6.6. The PA has a peak at 28 dBm input power with PAE of 49.8%, after this the PAE is decreasing. At the max input power, the PAE is 49.1%. If higher inputs are applied the PAE will decrease because of deep compression. Using another value for V_g only increases the PAE by 1%. Based on this the max PAE has increased by 21.5% for the NPA compared to the OPA. Besides certain capacitor values in the input network, the only thing changed in the NPA is the output network. Therefore, it is evident that the output network was the problem in the OPA. The output network was redesigned based on a new MSUB. Since the performance is greatly improved, the hypothesis that the original MSUB-model was wrong has been strengthened as well.

Transducer power gain

The results of the transducer power gain for the NPA can be seen in Figure 6.7. The result of the transducer power gain for the OPA can be seen in Figure 6.8. It is easier to see where the OPA acts like a class A PA and when it acts like class AB compared to the NPA. The NPA has a more gradual curve, the gain is also over higher levels of output power. The OPA has slightly higher gain compared to the NPA for lower output power. It seems to act as a class A for longer than the NPA, but once it switches to class AB at 27 dBm, the gain quickly drops. The two PAs are very similar in performance until they start going into compression. The OPA starts compressing earlier, at around 35 dBm and deep compression around 38 dBm, the gain drops by 3.8 dB and will drop even further with higher input. The same is true for the NPA only for higher output power. It starts compressing around 36.5 dBm and deep compression around 41 dBm. The drop in gain in this region is about 2.5 dB. The NPA can therefore sustain higher gain for higher output power compared to the OPA. From comparison of the 1 dB compression point based on a rough estimation of the plot, the OPA has 11.8 dB gain at 37 dBm. While the NPA has its 1 dB compression point around 38 dBm where the gain is 12.7 dB. With the modifications to the output network, the NPA has therefore improved large signal gain by roughly 1 dB at the 1 dB compression point. It also has higher gain for higher output powers.

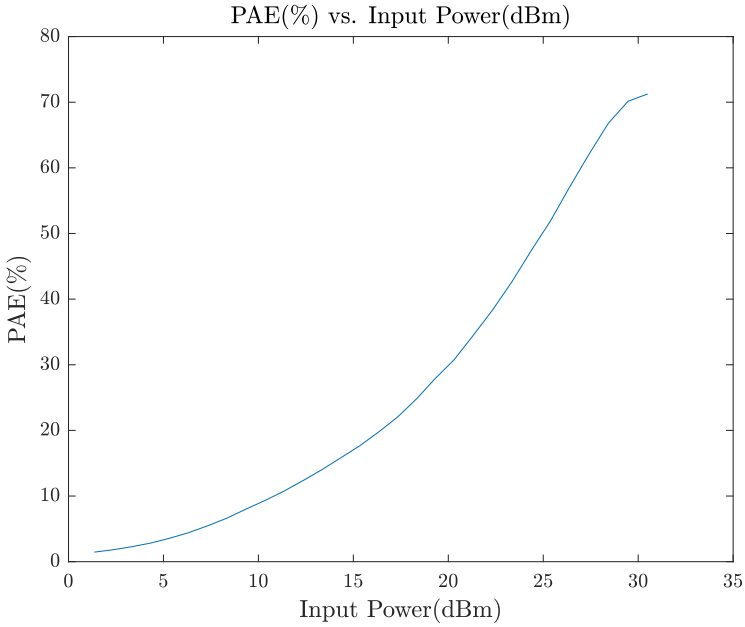


Figure 6.5: Measured PAE for the new PA

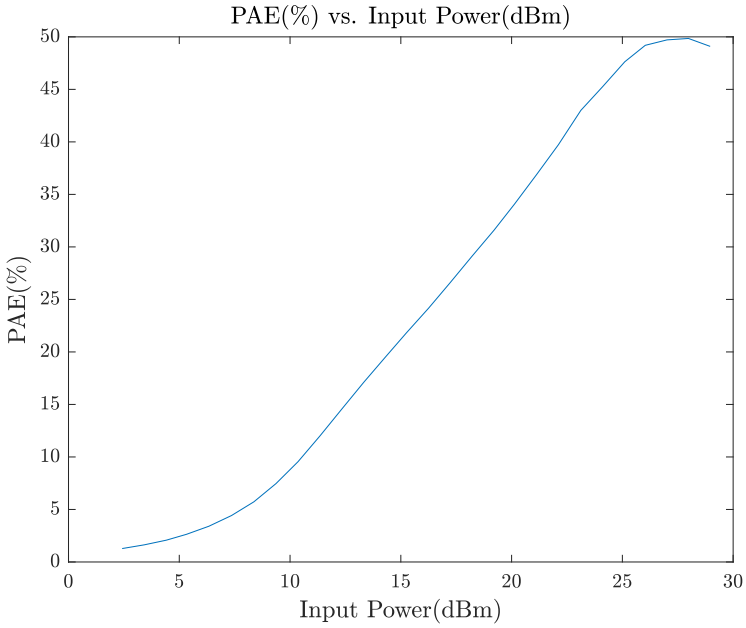


Figure 6.6: Measured PAE for the original PA

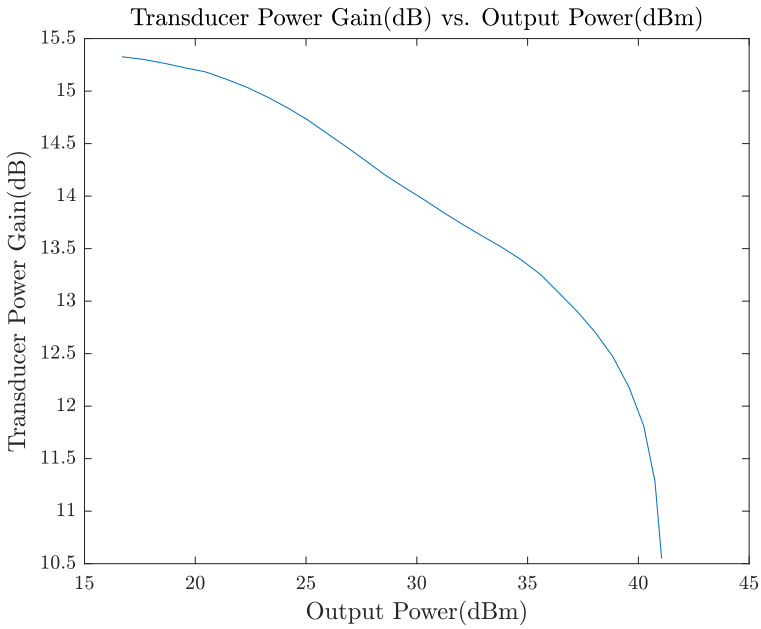


Figure 6.7: Measured transducer power gain for the new PA

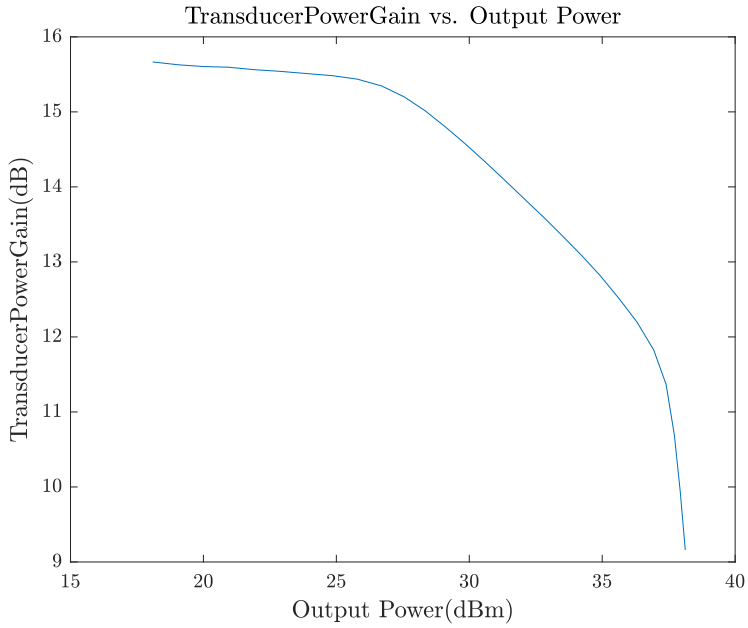


Figure 6.8: Measured transducer power gain for the original PA

6.4 Summary and discussion

In this chapter the results for the new PA have been presented and compared with the original PA using a new lab setup. By redesigning the output network with a new MSUB-model, the efficiency, output power and transducer gain is increased. Output power is increased by about 3 dB, while max PAE is increased by 21.5%. The transducer power gain is increased by about 1 dB at the compression point. A comparison of the simulated and measured results for the two PAs can be seen in Table 6.1. The values are referenced to the highest efficiency the PA has achieved. With the new MSUB the measured result is nearly spot on with the simulated results. The output power is higher than simulated, this is likely due to how the output power is measured. The power meter measures not only the fundamental, but also the power of the harmonics combined. Even if the power in the harmonics are low, it will contribute to the measured power. Only the linearity of the device is unclear since the 2-tone test has not been performed on it. This should be done in the future. Otherwise the behavior is assumed to be close to simulations. Changing the output network and the MSUB-model proved to be a good choice. The only undesirable property of the PA based on the results, is its bandwidth. The PA can still be used with a tracker and will be. However, increasing the bandwidth would be desirable. It has been proposed to remove one of the Johanson capacitors in the bias networks to remedy this. If this will work remains to be seen.

ADS simulations	**MSUB**	**Input power**	**Output Power**	**PAE**	**Transducer Gain**
Original PA	Original	31 dBm	41.05 dBm	74.3%	9.6 dB
Original PA	New	31 dBm	40.58 dBm	65.9%	9.2 dB
Improved PA	New	31 dBm	40.9 dBm	74.9%	9.8 dB
Measured Results	**MSUB**	**Input power**	**Output Power**	**PAE**	**Transducer Gain**
Original PA	Original	28 dBm	37.9 dBm	49.8%	9.9 dB
Improved PA	New	30.5 dBm	41.05 dBm	71.3%	10.5 dB

Table 6.1: 1-tone simulated and measured results with V_d=28 V and V_g=2.68 V referenced to max PAE

Chapter 7

Tracking

In this chapter the focus is on making tracking functions. The tracking functions are made using the data from the measurements done in Chapter 6. The tracking functions are not used on an actual tracker, they are only simulated in MATLAB. The tracking functions however, should be close to the real thing. Tracking functions for both ET and PET are presented. The work done here can be used for further work in the future.

The first section 7.1 covers how the MATLAB script used in the setup in Chapter 6 works. This explains necessary calibration as well as important considerations for the data used in the tracking. In section 7.2 and 7.3 tracking functions are explained and presented. Section 7.2 covers two cases of tracking functions for max PAE, one using drain tracking and one using both gate and drain tracking. Section 7.3 does the same only for constant gain tracking. In both cases ET and PET tracking functions are made. Finally, in section 7.4 the most important findings are summarized and discussed.

7.1 Understanding the data

The setup in Figure 6.2 is used to get the data for the tracking function. While Chapter 6 only presents data for a single V_d and V_g, the same setup measures the amplifiers behavior over a range of different V_d and V_g. The ranges are found in Table 7.1. With this it is possible to make functions for max PAE and constant gain. A physical tracker can vary the amplifiers V_d and V_g to achieve this.

Range calibration

The V_d range is based on the transistor's characteristics [6]. It is meant to operate at 28 V, for this reason it is chosen as the maximum voltage in the range. The value of V_d determines how much DC-power is available to be transformed into RF-power. For the tracking, it is therefore desirable to have a large range to choose from to see this effect, lower V_d will naturally give lower output power but may in turn make the PA more efficient at lower RF input power. It is therefore decided to have at least 20 different values for V_d.

The step size is decided to be 1 V and V_d goes as low as 6 V. Lower values for V_d will give very little amplification and will force the PA into compression very early.

To find the V_g range, the PA is connected to the setup without powering any other part of the setup. The setup acts as a passive load for the PAs input and output. V_d is set to the max i.e. 28 V, while V_g is varied to see at which voltages the gate open, and the drain current starts to flow. The transistor can handle a drain current up to 1.5 A. Here however, it is decided to keep the current to a maximum of about 500 mA. This is only an approximation and the current will differ when the whole setup is powered. The limit is set in order to protect the transistor from potential damage. The range for V_g starts where the gate opens, and the drain current is 25 mA and ends where the current is 500 mA. It is preferable to have at least 10 different values for V_g in order to have some flexibility when tracking. Starting from -3 V the step size is 0.08 V.

For the input power the most important limit is the max input. The max input is determined by which input level gives max output power for the PA, and what level the power meter can handle with the attached attenuators. For good resolution in the data it is preferable with at least 30 steps, this can be increased but will add extra time to an already time heavy measurement. Max output is reached at about 30 dBm input power, making the start of the range 1 dBm.

Variable	Range	Step size	Total steps
V_g	-3 V to -2.28 V	0.08 V	10
V_d	6 V to 28 V	1 V	23
Input power	1 to 30 dBm	1 dB	30

Table 7.1: Variables used with array as index for the measured data

Matlab script

The MATLAB script uses a struct-file to store the measured data. Struct in programming is quite useful, it allows the program to store different file types together in a structure. In this case they are stored as three multidimensional arrays. The setup only measures three things; input power, output power and drain current. Other variables, like the ones in Table 7.1 are already determined in the script.

The arrays have 10x23x30 data points, for accurate measurement pauses are added between every full power sweep for a single V_g and V_d. The pause allows the power supply to settle on a new V_g or V_d before going through a power sweep.

With the amount of measured data, it is important to have an understandable system, otherwise the data will be hard to work with. The three main arrays store the data for drain current I_d, the input power P_{in} and the output power P_{out}. The indexing of the arrays or position of each measured data is given by three variables in the following order: V_g, V_d and input power. With the same indexing, the measured data can easily be compared with each other. Figure 8.1 in Appendix A, shows visually how the data is stored.

Errors in the data

Not all data while measuring is accurate. Figure 7.1 is an example of faulty data appearing in the measurement. This seem to mostly happen to the gate voltages in position 8,9 and 10, i.e. V_g = [-2.44, -2.36, -2.28]. It is also more common for the lower drain voltages. This is when the gain is the lowest and it quickly goes into compression. The corrected data is seen in blue and is corrected manually. Spikes shown in Figure 7.2 are fixed by averaging the data around the spike. Other more exaggerated versions of Figure 7.1 also occur, these are corrected using the mean data values of gate voltages one step higher or lower. The data is then made smoother with built in smoothing functions in MATLAB. These data point will not be perfect, but without the spikes the tracking function will be more accurate. Output power seem to be most effective when correcting the data and is therefore used. When making the tracking functions these are avoided entirely, or use only the affected areas.

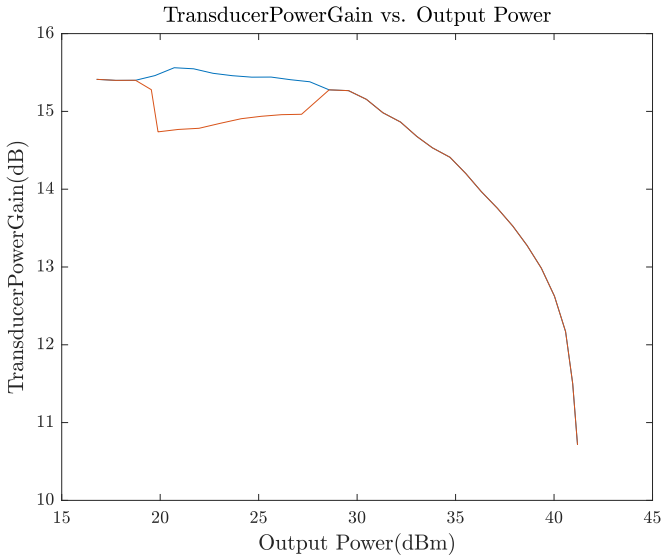


Figure 7.1: Error in data with correction

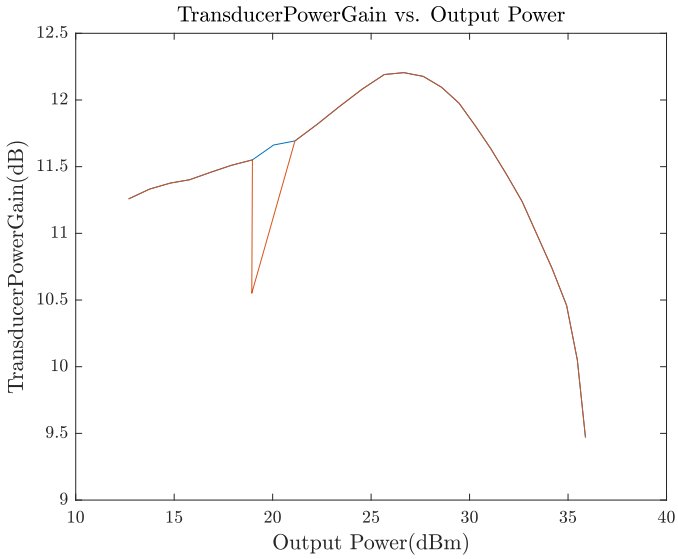


Figure 7.2: Error in data with correction

7.2 Max PAE

For the max PAE tracking function, the intention is to maximize efficiency for the whole power range. Using a constant V_d and constant V_g as in Chapter 6 is efficient for the highest input powers. For lower input powers however, the PA is supplied with more DC-power than is necessary for the same amplification. Efficiency can therefore be improved by varying these two parameters V_d and V_g, so that the PA is only supplied with what it needs and nothing more. Two cases will be presented here; tracking varying only drain and tracking varying both gate and drain.

Drain and gate tracking

When tracking for max PAE the approach is to find the maximum PAE point for each V_d curve. Ideally the lower values for V_d will have a curve with a peak at the lower input powers, as input power is increased the ascending V_d will have higher peaks and be shifted towards higher input power. This is illustrated in Figure 7.3. The tracker can then switch to the most efficient V_d as input power is increased. With max PAE chosen for each V_d with a corresponding input power, the points will form a new curve. The new curve can be approximated with polynomials. The tracking function will be the approximated polynomial. ET tracking functions are found by adding a higher order until the polynomial fits the chosen datapoints. PET on the other hand only uses even polynomials where the odd parts are not included, this is explained in section 2.9. The approximation is not perfect but manages to get quite good results while requiring less bandwidth.

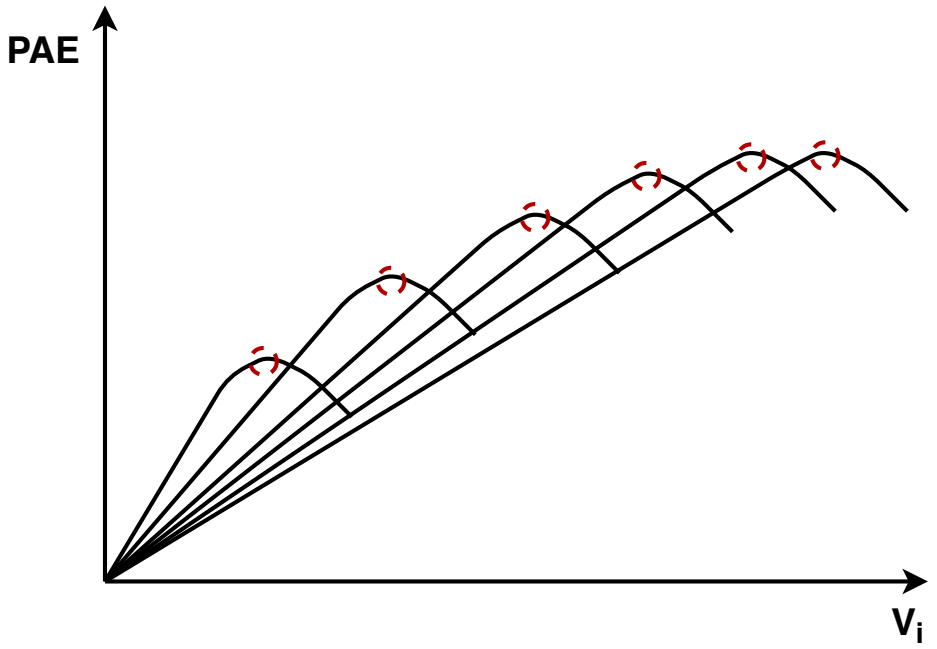


Figure 7.3: Illustrated procedure for finding datapoints for max PAE tracking

For the PA however, the situation is not ideal. As seen in Figure 7.4 the curves are tightly packed together, and the peaks are mostly concentrated at higher input power. The corresponding curve used for tracking is therefore limited to the upper power levels. Table 8.1 and Table 8.2 in Appendix C are the datapoints used for tracking. The resulting PAE and transducer gain for the two cases are seen in Figure 7.5. The PAE remains quite high for most V_d. While the gain is steadily decreasing as V_d decreases. There are only small improvements in efficiency when tracking with V_g, while the gain is lower than constant V_d for the most part. The data in the figures are normalized to V_i, where V_i is given by formula 7.1. P_{in} is input power, 50Ω is the assumed impedance at the input. V_i is used in order to get the correct polynomial order and relates to V_{env} described in section 2.9.

Since the improvement is minimal when using gate tracking, only a drain tracking function is approximated. The function is approximated for ET by making a polynomial of 9th order. Compared with PET the tracking is better but will require substantially more bandwidth. 1st order PET and 2nd order PET manages to approximate the function quite well while reducing the bandwidth needed. The efficiency will go down, how much however has not been checked. Based on previous articles on PET[15] [14] it should be worth the sacrifice in return for lower bandwidth requirements. The results are seen in Figure 7.6.

$$V_i = \sqrt{P_{in} * 50\Omega} \tag{7.1}$$

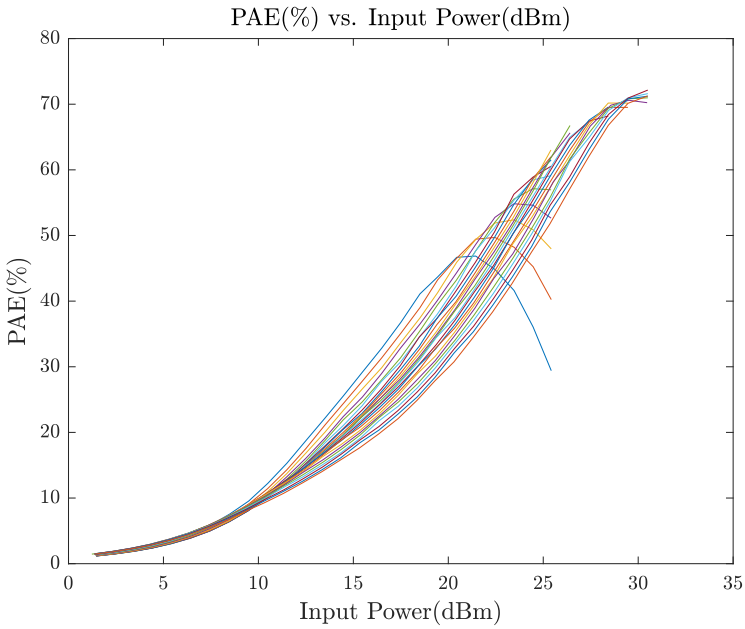


Figure 7.4: PAE for all V_d in the range

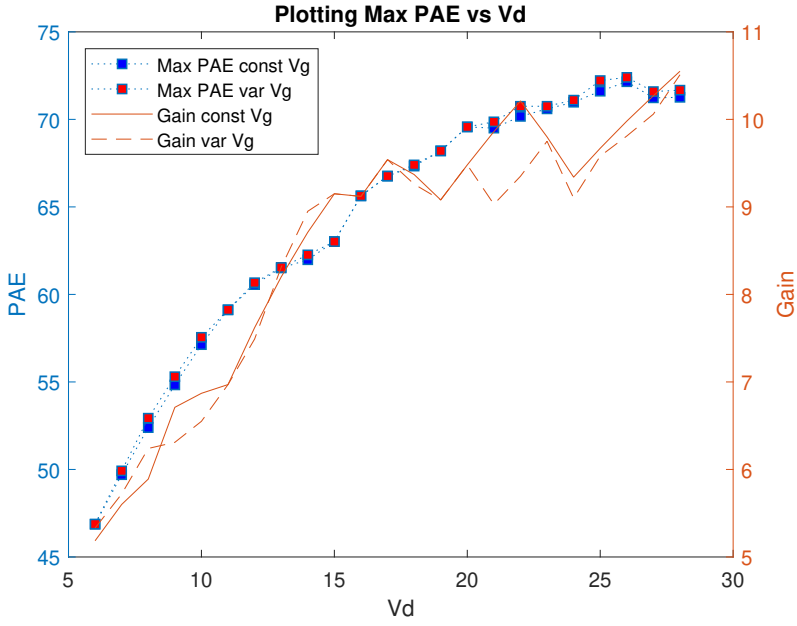


Figure 7.5: PAE and transducer gain versus V_d, with and without variable V_g

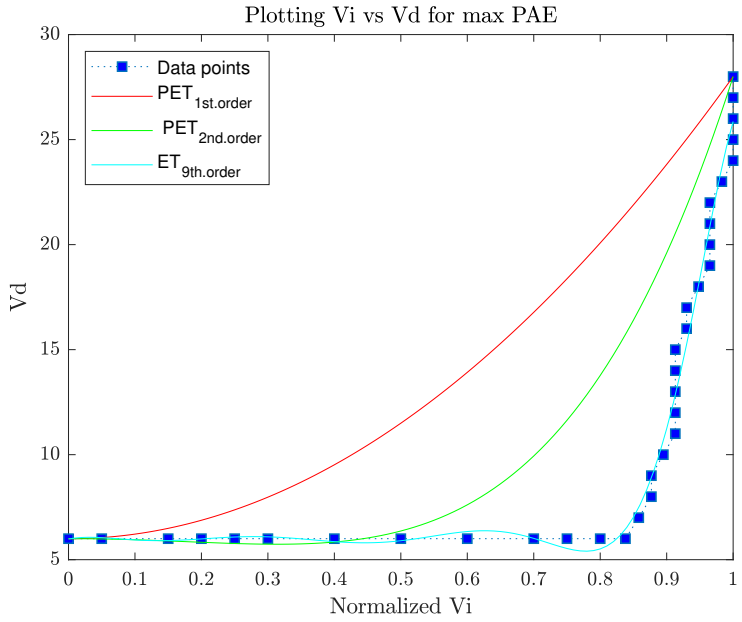


Figure 7.6: Tracking functions for max PAE

7.3 Constant gain

For the constant gain tracking function, the intention is to maintain the same gain for the whole power range. When tracking for constant gain the efficiency will decrease, just like gain went down for max PAE with decreasing V_d. In this section two cases will be presented.

Drain and gate tracking

When tracking for constant gain the transducer gain plot is used. A plot for multiple V_d is seen in Figure 7.7. When tracking with drain, the approach is to make a straight line through multiple V_d curves. When the input power changes, so will the V_d to keep the same constant gain. The reason to do gate tracking, is to increase efficiency while keeping the same constant gain. Gate tracking adds extra curves, increasing the freedom of choice. The basis for the straight line depends on what characteristics are desired. Higher gain will mean sacrificing output power. Here the focus is on max output power, therefore the curve for V_d = 28 V is used as the starting point for the line. The curve has the highest gain of the curves at max output. Figure 7.8 illustrate this scenario. The corresponding datapoints gathered from Figure 7.7 are found in Table 8.3 in Appendix C, the gathered datapoints for variable V_g are found in Table 8.4.

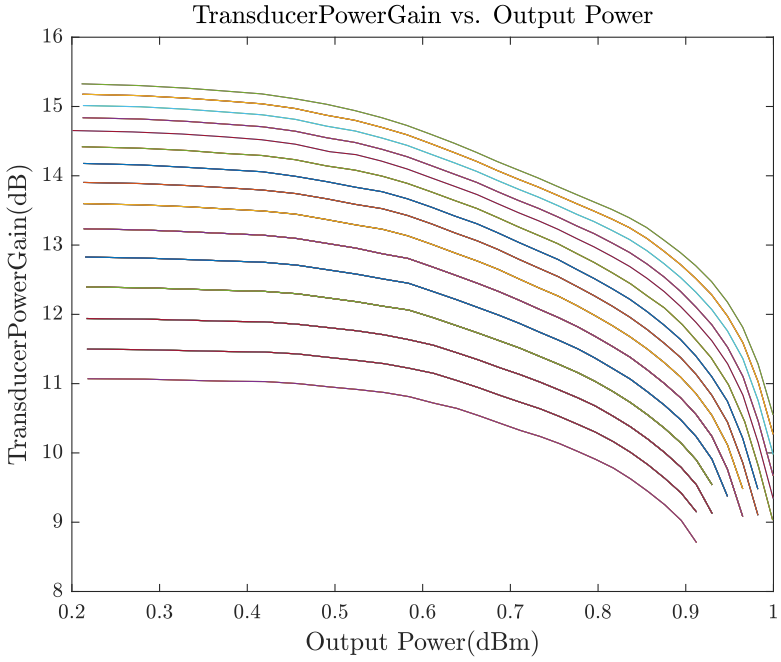


Figure 7.7: Transducer gain for the highest V_d in the range

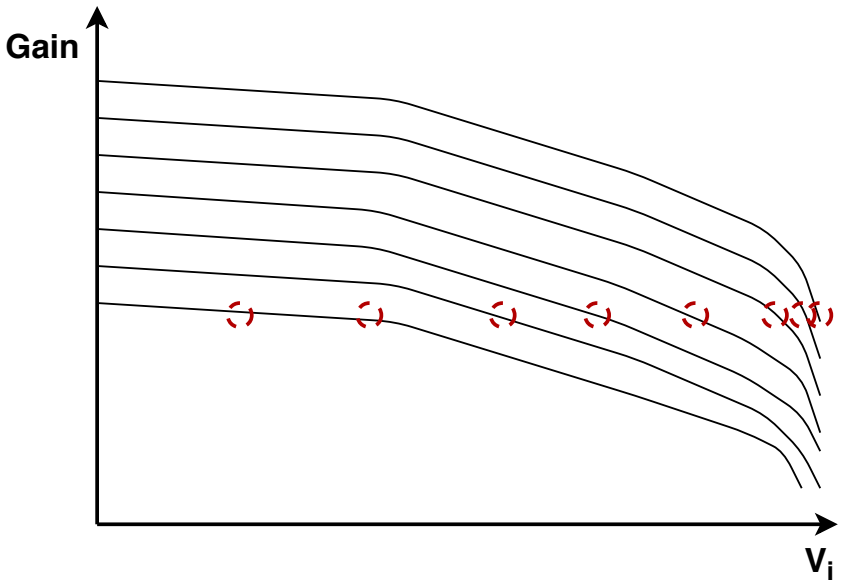


Figure 7.8: Illustrated procedure for finding datapoints for constant gain tracking

A stable gain around 10.5 dB is achieved with drain tracking alone. The corresponding PAE is also quite high for the upper levels of V_i. To increase efficiency further, gate tracking is used. A performance comparison for drain tracking and drain-gate tracking can be seen in Figure 7.9 and Figure 7.10. Only minor improvements in PAE are seen for the upper levels of V_i. By attempting to track for even lower V_d compared to the constant gain with variable gate, PAE is lowered. This can be seen as the dip in Figure 7.10 for variable V_g. From normalized V_i = 0.8 and down, varying gate does not give any improvement and drain tracking alone is enough.

Since the improvement is minimal when using gate tracking, only a drain tracking function is approximated. The function is approximated for ET by making a polynomial of 8th order. Compared with PET the tracking is better but will require substantially more bandwidth. 1st order PET and 2nd order PET manages to approximate the function quite well while reducing the bandwidth needed.

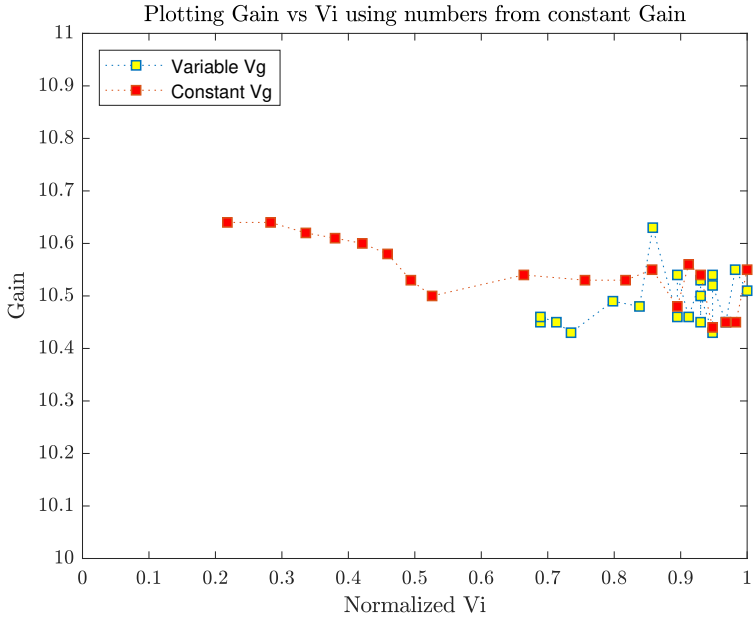


Figure 7.9: Datapoints for gain when tracking for constant gain

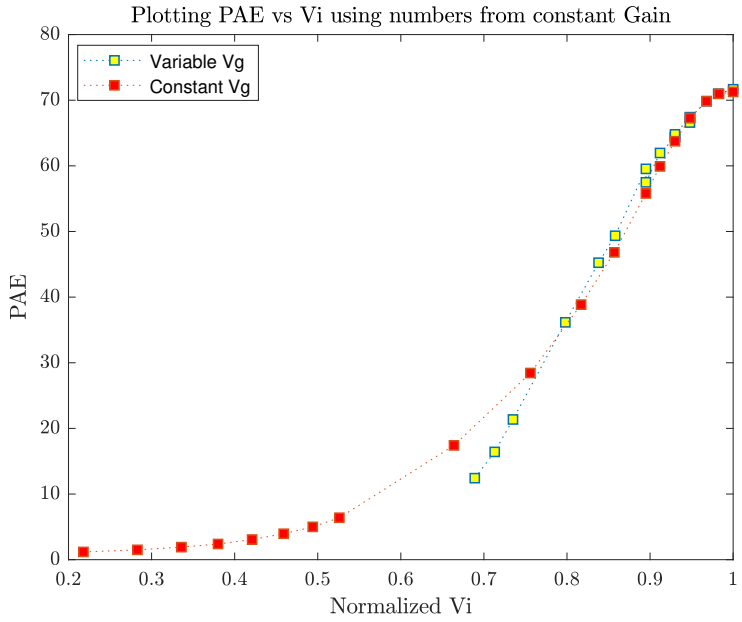


Figure 7.10: Datapoints for PAE when tracking for constant gain

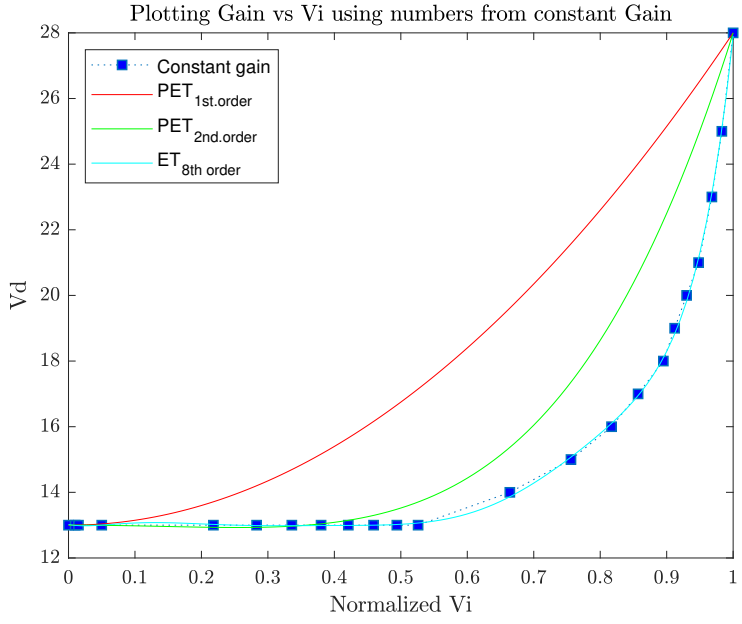


Figure 7.11: Tracking functions for constant gain

7.4 Summary and discussion

In this chapter the data used to make tracking functions have been presented. These have been used to make tracking functions for max PAE and constant gain. Both drain and gate tracking have been simulated with the measurement data, but there is little improvement from using gate tracking. Therefore, tracking functions are only made for drain tracking. Tracking functions are approximated with polynomials. While ET better approximate the data, it requires high order polynomials and will therefore also require large bandwidth. PET is simpler with poorer approximation, but in turn requires less bandwidth. Further work on this area should assess the PAE PET of 1st and 2nd order achieves with its simpler approximation for this PA, to better compare it with ET. The PA should also be tested with actual trackers to verify if the simulated results are accurate.

Chapter 8

Conclusion

The purpose of this thesis was to design and produce an RF PA compatible with tracking technology. Two PA designs were ultimately produced, the reason for this was because the first PA did not perform as expected. The large-signal results were much lower than expected. Therefore, a second design was made. Only the output network was necessary to redesign and was done so by first characterizing a new model for the microstrip substrate MSUB. With the new model the performance was greatly increased especially regarding PAE and output power. The measurements are very much like the simulations and for this reason the model might be applicable for future projects as well. Compared to previous projects using the old model, the performance has always been below simulations by a significant margin. With the new model, future designs might have an increase in output power and PAE performance. The model should therefore be used as much as possible in the future, to determine if it is more accurate than the original or if it only worked for this case.

The final PA fulfills most of the specifications but does have an issue with bandwidth. The small-signal bandwidth is about 540 MHz in simulations but is not achieved in real measurements. The bandwidth has a resonance or dip close to the center frequency 2.2 GHz. If this issue is fixed, then all the specifications will be fulfilled. The assumption is that the two Johanson capacitors create a resonance with each other because of proximity and being in parallel. To fix this changing the values of the capacitors in the bias could work or one of the capacitors could be removed.

The transistor used in this thesis promised to deliver about 18 dB for small-signal gain and about 70% for PAE. Small-signal gain is a bit lower but PAE is even better than promised at compression. The previous version in comparison, promises 16 dB small-signal gain and about 65% PAE. The results here, therefore validate the claim that the transistor has improved performance.

Although it has not been tested with actual trackers, the PA shows good tracking performance in simulations based on the measured results. By using PET the bandwidth required for tracking is less compared to ET, but will be slightly less efficient. Simulations showed that while drain tracking gave improved performance while tracking, gate tracking

was less effective. The next step with tracking, would be to test the tracking functions with real trackers.

Bibliography

[1] P. Asbeck and Z. Popovic. ET Comes of Age: Envelope Tracking for Higher-Efficiency Power Amplifiers. *IEEE Microwave Magazine*, 17(3):16–25, March 2016.

[2] A. Bognøy. 10W GaN effektforsterker med Envelope Tracking og optimalisert tilpasning. http://hdl.handle.net/11250/2371404, Jan 2015. [Accessed 28/12/2018].

[3] C.E, Hellenes, G. Karlsen. Design of a Power amplifier. https://ufile.io/zxqhu, 2018. [Accessed 14/08/2018].

[4] C. connectivity solutions. SMA 50 Ohm End Launch Jack Receptacle-Round Contact. https://belfuse.com/resources/Johnson/productinformation/pi-142-0701-801.pdf. [Accessed 02/01/2019].

[5] Cree. CGH40010 Rev. 4.0 Data Sheet. http://www.wolfspeed.com/downloads/dl/file/id/317/product/117/cgh40010.pdf, 2015. [Accessed 20/09/2018].

[6] Cree. CG2H40010 Rev. 1.1 Data Sheet. https://www.wolfspeed.com/downloads/dl/file/id/1051/product/242/cg2h40010.pdf, 2018. [Accessed 20/09/2018].

[7] ElectronicsNotes. Envelope Tracking Power Supply / DC Modulator. https://www.electronics-notes.com/articles/radio/rf-envelope-tracking/power-supply-dc-modulator.php. [Accessed 16/12/2018].

[8] ElectronicsNotes. RF Envelope Tracking Tutorial — Improving RF Power Amplifier Efficiency. https://www.youtube.com/watch?v=vSSY11Df2hk. [Accessed 14/08/2018].

[9] J. Jeong, D. Kimball, M. Kwak, C. Hsia, P. Draxler, and P. M. Asbeck. Wideband Envelope Tracking Power Amplifier with Reduced Bandwidth Power Supply Waveform. pages 1381 – 1384, 07 2009.

[10] G. Karlsen. Design of a Harmonically Tuned Two-Stage Broadband Power Amplifier in Discrete GaN Technology - A Harmonic Loadpull and Harmonic Termination Approach. https://ntnuopen.ntnu.no/ntnu-xmlui/handle/11250/2565883, 2018. [Accessed 14/04/2019].

[11] P. B. Kenington. *High Linearity RF Amplifier Design*. Artech House Publishers, 2000.

[12] Keysight. Agilent Technologies, Advanced Design System Software 2017.1.0. http://www.keysight.com/main/software.jspx?ckey=2212036&lc=eng&cc=NO&nid=-34346.1078495&id=2212036&pageMode=PV. [Accessed 14/08/2018].

[13] Leopedrini. What is Envelope Tracking? http://www.telecomhall.com/what-is-envelope-tracking.aspx, 2016. [Accessed 11/12/2018].

[14] M. Olavsbråten, D. Gecan. Efficiency enhancement and linearization of GaN PAs using reduced-bandwidth supply modulation. In *European Microwave Conference (EuMC)*, pages 456–459, Kuala Lumpur, Malaysia, 2017 47th.

[15] M. Olavsbråten and D. Gecan. Bandwidth Reduction for Supply Modulated RF PAs using Power Envelope Tracking. *IEEE Microwave and Wireless Components Letters*, 27(4):374–376, April 2017.

[16] K. S. How fast is 5G - 5G speeds and performance. https://5g.co.uk/guides/how-fast-is-5g/, 2018. [Accessed 03/01/2019].

[17] TTT4201. Semester Project. https://ntnu.blackboard.com/bbcswebdav/pid-455501-dt-content-rid-17308409_1/courses/194_TTT4201_1_2018_H_1/SemesterProject2018.pdf, 2018. [Accessed 08/10/2018].

[18] TTT4201. Semester Project. https://ntnu.blackboard.com/bbcswebdav/pid-455501-dt-content-rid-18050141_1/courses/194_TTT4201_1_2018_H_1/OutlineNew62.5x62.5.png, 2018. [Accessed 14/08/2018].

Appendix A:
Visual representation of structure in MATLAB

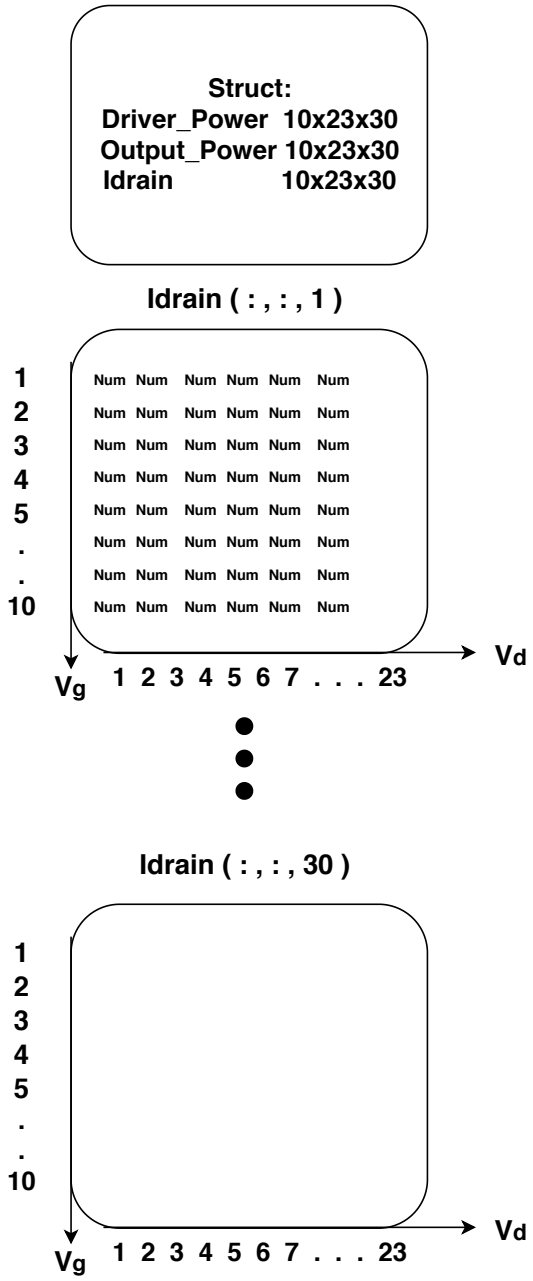


Figure 8.1: Visual representation of data stored in struct array

Appendix B:
Datasheet for the RF PA

RF PA 2019 v1.2

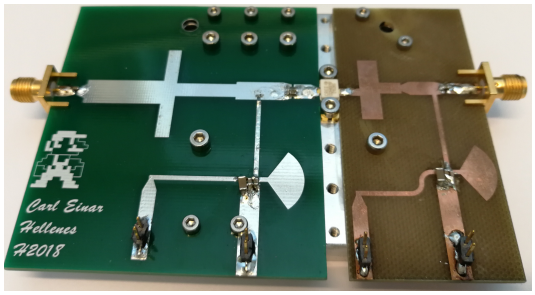


Figure 1: RF PA version 1.2

FEATURES

- Single RF-input signal up to 30.5 dBm
- Can provide a maximum RF output power of 41 dBm
- Measured power added efficiency (PAE) of 71% at maximum output power
- Bandwidth of 120 MHz with center frequency at 2.2 GHz
- Bandwidth of 390 MHz with center frequency at 2.345 GHz by sacrificing output power by 2 dB
- Measured small-signal gain of 17 dB

APPLICATIONS

- Compatible with tracking technology such as Envelope Tracking (ET) and Power Envelope Tracking (PET)
- Class AB amplifier, Linear amplifier suitable for OFDM, W-CDMA, EDGE, CDMA waveforms

Introduction

An RF PA or radio frequency power amplifier is a device used to amplify a radio signal. In this document a class AB, RF PA is presented. It is designed as part of a master thesis done for NTNU. The motivation behind the project is to test the usability of a newly developed tracking technology. Other PAs exist that can perform this task, however this PA utilizes an improved transistor from Cree, the 10 W GaN HEMT CG2H40010. The transistor has improved efficiency and output power from its predecessor CGH40010. The PA is designed using Advanced Design System (ADS) from Keysight. The final PCB is produced in China through PCBWay (`www.pcbway.com`)

Description

The PA is a 100x100 mm two-piece PCB attached to a heatsink with the transistor connecting the two pieces at the center. The PA is seen in Figure 1. The left side is called the input network. It consists of a matching network, stability circuit and bias network. The SMA connector is for RF input, first pin from the left is for gate voltage V_g, the second pin is ground. The PCB on the right is called the output network. It is similar, but does not contain a stability circuit. The pins starting from the left are for drain voltage V_d, the other for ground and the SMA connector is for RF output. How each part fit together, can be seen in Figure 2, these are the main elements of the PA.

Design process

The PA design process contains the following steps:

- Choosing an operating point for the transistor, also called biasing.
- Making a suitable bias network, this ensures correct operation for the PA as well as minimizing RF power leakage into the DC supply.
- Implementing a stability circuit. This ensures the PA does not oscillate while in operation.
- Matching network. Matching is done to achieve a certain gain over a certain bandwidth for a chosen center frequency. Here a trade-off is made, higher gain means less bandwidth and vice versa. The matching network also affects output power for the PA as well as efficiency.

Special considerations

Tracking technology like ET is used together with amplifiers to increase their efficiency. It does this by tracking the envelope of the RF input signal. The envelope is used to regulate the bias V_g and V_d so that the amplifier is only supplied with what it needs and nothing more. High capacitance in the tracker/bias network connection is undesired because it will limit the tracking performance. The bias network therefore only uses small capacitors. When the PA is used without a tracker, it must therefore have a capacitor of about 1 μF or it will oscillate.

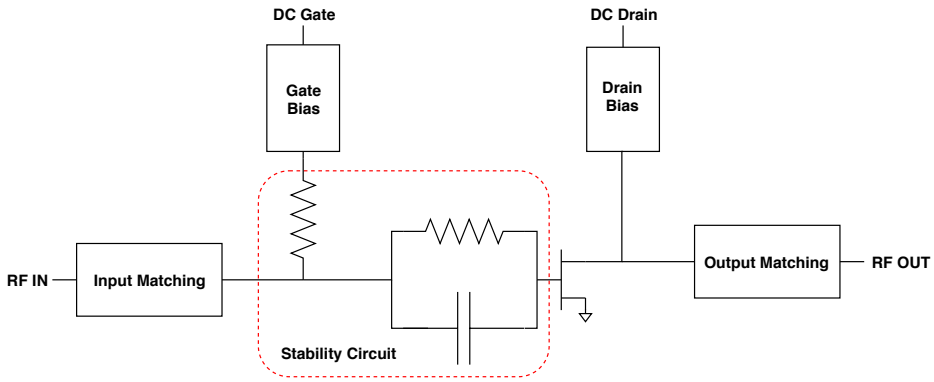


Figure 2: Main parts of the PA

Measurements and setup

The RF PA is a powerful device, Figure 3 shows the Power Added Efficiency or PAE. When the PA is in saturation the maximum efficiency it can achieve is 71%. For class AB the theoretical maximum is 78.5%. In saturation it can output 41 dBm. Any RF input above 30 dBm is not suggested because of the high compression rate. Most if not all extra power added will dissipate as heat.

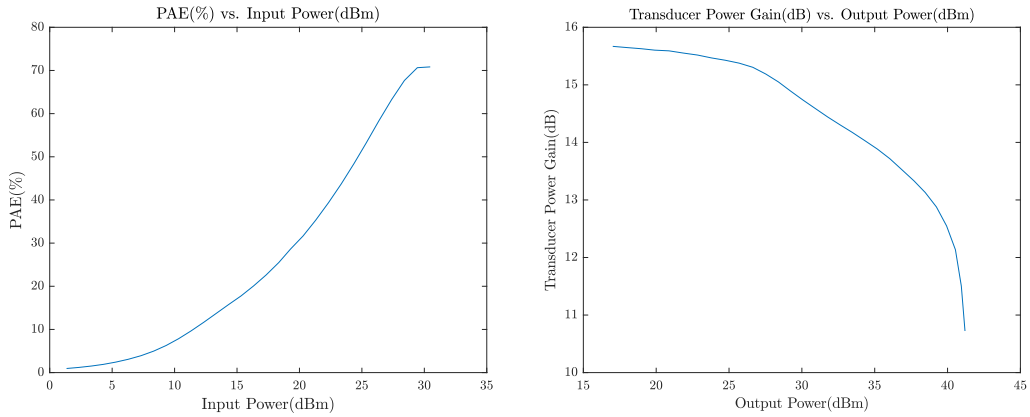


Figure 3: Gain and PAE measurements (V_g = -2.6V and V_d = 28V)

The lab setup used to measure the PA is seen in Figure 4. It uses a Vector Signal Generator to produce the RF input signal. The generator can only deliver a maximum signal of 20 dBm. Therefore, a broadband PA called a driver is used to amplify the signal before it is delivered to the RF PA, shown as DUT (device under test) in Figure 4. Couplers are used in order to measure the signal in the stages before and after the RF PA. The signals at the couplers are too powerful for a power meter to handle, therefore appropriate attenuators are chosen to attenuate the signal to acceptable levels. The instruments and measurements are controlled through MATLAB code.

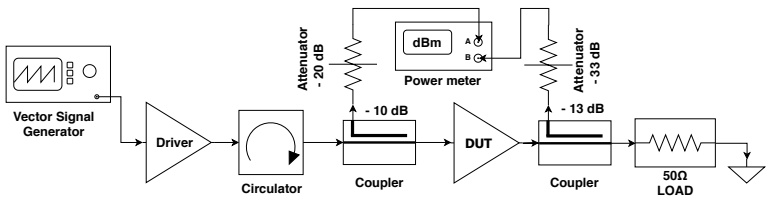


Figure 4: Setup used for measurements on the PA

Appendix C:
Tracking tables

Max PAE with varying V_d and constant V_g				
Vi	PAE [%]	Gain [dB]	V_d [V]	V_g [-V]
1	71.26	10.55	28	2.68
1	71.23	10.27	27	2.68
1	72.15	9.98	26	2.68
1	71.61	9.67	25	2.68
1	70.98	9.34	24	2.68
0.983	70.60	9.80	23	2.68
0.965	70.17	10.21	22	2.68
0.965	69.50	9.86	21	2.68
0.965	69.57	9.48	20	2.68
0.965	68.20	9.08	19	2.68
0.948	67.33	9.37	18	2.68
0.930	66.76	9.54	17	2.68
0.930	65.63	9.12	16	2.68
0.913	63.02	9.15	15	2.68
0.913	61.98	8.71	14	2.68
0.913	61.51	8.20	13	2.68
0.913	60.56	7.62	12	2.68
0.913	59.12	6,97	11	2.68
0.895	57.13	6.87	10	2.68
0.877	54.83	6.71	9	2.68
0.877	52.39	5.89	8	2.68
0.858	49.70	5.60	7	2.68
0.838	46.87	5.185	6	2.68

Table 8.1: Datapoints used to make tracking function for max PAE with a variable V_d and constant V_g

Max PAE with varying V_d and V_g				
Vi	PAE [%]	Gain [dB]	V_d [V]	V_g [-V]
1	71.67	10.51	28	2.76
1	71.59	10.06	27	3
1	72.40	9.81	26	2.92
1	72.22	9.58	25	2.84
1	71.10	9.10	24	3
0.982	70.75	9.75	23	2.76
0.983	70.75	9.35	22	2.84
0.982	69.86	9.03	21	2.76
0.965	69.57	9.48	20	2.68
0.965	68.20	9.08	19	2.68
0.948	67.40	9.26	18	2.76
0.930	66.76	9.54	17	2.68
0.930	65.63	9.12	16	2.68
0.912	63.02	9.15	15	2.68
0.913	62.26	8.95	14	2.52
0.913	61.54	8.31	13	2.60
0.912	60.67	7.49	12	2.76
0.912	59.12	6.97	11	2.68
0.895	57.55	6.55	10	2.84
0.877	55.30	6.31	9	2.84
0.858	52.93	6.24	8	2.76
0.858	49.92	5.72	7	2.60
0.838	46.88	5.33	6	2.60

Table 8.2: Datapoints used to make tracking function for max PAE with a variable V_d and V_g

Constant gain with varying V_d and constant V_g				
Vi	PAE [%]	Gain [dB]	V_d [V]	V_g [-V]
1	71.26	10.55	28	2.68
0.983	70.97	10.45	25	2.68
0.968	69.85	10.45	23	2.68
0.948	67.28	10.44	21	2.68
0.930	63.75	10.54	20	2.68
0.912	59.91	10.56	19	2.68
0.895	55.79	10.48	18	2.68
0.857	46.82	10.55	17	2.68
0.817	38.86	10.53	16	2.68
0.756	28.44	10.53	15	2.68
0.664	17.41	10.54	14	2.68
0.526	6.39	10.50	13	2.68
0.494	5.00	10.53	13	2.68
0.459	3.95	10.58	13	2.68
0.421	3.07	10.60	13	2.68
0.380	2.39	10.61	13	2.68
0.336	1.91	10.62	13	2.68
0.283	1.5	10.64	13	2.68
0.218	1.18	10.64	13	2.68

Table 8.3: Datapoints used to make tracking function for constant gain with a variable V_d and constant V_g

Constant gain with varying V_d and V_g				
Vi	PAE [%]	Gain [dB]	V_d [V]	V_g [dB]
1	71.67	10.51	28	2.76
0.982	70.99	10.55	25	2.52
0.968	69.85	10.45	23	2.68
0.948	67.31	10.52	21	2.60
0.948	66.60	10.54	20	2.36
0.948	67.42	10.43	20	2.44
0.930	64.80	10.50	19	2.52
0.930	64.44	10.45	18	2.36
0.930	64.31	10.53	18	2.28
0.912	61.96	10.46	17	2.44
0.895	57.49	10.54	17	2.52
0.895	59.54	10.46	16	2.44
0.858	49.35	10.63	15	2.44
0.838	45.24	10.48	14	2.44
0.798	36.16	10.49	13	2.44
0.735	21.36	10.43	12	2.44
0.713	16.42	10.45	12	2.44
0.689	12.42	10.46	12	2.44

Table 8.4: Datapoints used to make tracking function for constant gain with a variable V_d and V_g

Carl Einar Hellenes

Construction of a Power Amplifier based on a newly developed Power Envelope Tracking (PET) of Gate and Drain

NTNU
Norwegian University of
Science and Technology