Master's thesis

NTNU
Norwegian University of Science and Technology
Faculty of Information Technology and Electrical Engineering
Department of Electronic Systems

Kristoffer Krav Skjølseth

Design and Characterization of a 20 W Dual-Input Doherty Power Amplifier

Master's thesis in Electronic Systems Design
Supervisor: Associate Professor Morten Olavsbråten
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NTNU
Kunnskap for en bedre verden

Abstract

The high PAPR characteristic of signals used in modern wireless communication systems causes poor RFPA performance in terms of efficiency.

The Doherty power amplifier architecture (DPA) employs two amplifiers to implement load modulation in order to increase the poor back-off efficiency typically seen in conventional RFPA's. This thesis explores the benefits of dynamically controlling the relative phase between the input signals to the two amplifiers, as well as using adaptive auxiliary device biasing in order to improve the performance of DPA's.

A 20 W dual-input DPA prototype utilizing two GaN HEMT's as its main and auxiliary device is designed using ADS, with focus on maintaining the bandwidth in the low power and Doherty region.

The designed prototype is characterized in a fully automated measurement setup which utilizes scalar power measurements to approximate the relative phase between the two input signals in order to align them in phase. The prototype is characterized with both dynamic and fixed phase and bias.

With fixed phase and bias, the measured results show that the prototype delivers a peak output power of 44 dBm at a peak efficiency of 58 %. When the phase is allowed to vary dynamically as a function of input power, and the bias is kept fixed, the prototype delivers a peak output power of 43 dBm at a peak efficiency of 63 %.

The back-off efficiency is measured to be only 33 % due to not having used a sufficiently large auxiliary device bias sweep range in the measurement setup. However, with dynamic phase the efficiency in the Doherty region is around 10 % higher than in the case with fixed phase.

With both dynamic phase and dynamic bias, the prototype shows an extremely flat gain response, although at the expense of efficiency.

Sammendrag

Signaler som brukes i moderne systemer for trådløs kommunikasjon har typisk høy PAPR. Dette gjør at ytelsen til RF-effektforsterkerne som brukes er lav når det gjelder virkningsgrad.

Doherty-effektforsterkerarkitekturen benytter to forsterkere til å implementere lastmodulasjon for å øke den lave gjennomsnittsvirkningsgraden som vanligvis sees i konvensjonelle RF-effektforsterkere. Denne masteroppgaven utforsker fordelene ved dynamisk styring av den relative fasen mellom inngangssignalene til de to forsterkerne, samt bruk av adaptiv forspenning av transistoren i auxiliary-forsterkeren for å øke ytelsen til Doherty-effektforsterkeren ytterligere.

En 20 W DPA-prototype med to innganger – bestående av to forsterkere basert på to GaN HEMT – designes i ADS, med fokus på å opprettholde båndbredden i lav-effekt- og Doherty-regionen.

Prototypen karakteriseres i et helautomatisert måleoppsett som benytter skalare effektmålinger for å approksimere den relative fasen mellom de to inngangssignalene for å synkronisere de to signalene i fase. Prototypen karakteriseres med både dynamisk og fast fase og forspenning.

Med fast fase og forspenning viser de målte resultatene at prototypen leverer en maksimal utgangseffekt på 44 dBm med en maksimal virkningsgrad på 58 %. Når fasen tillates å variere dynamisk som funksjon av inngangseffekt, og forspenningen holdes fast, leverer prototypen en maksimal utgangseffekt på 43 dBm med en virkningsgrad på 63 %.

Gjennomsnittsvirkningsgraden måles til å være bare 33 %, grunnet et utilstrekkelig sveipeområde for forspenningen når målingene er gjort. Virkningsgraden i Doherty-regionen er imidlertid rundt 10 % høyere enn i tilfellet med fast fase.

Med både dynamisk fase og dynamisk forspenning viser prototypen en ekstremt flat gainrespons, men på bekostning av virkningsgrad.

Preface

This thesis is submitted in partial fulfillment of the requirements for the degree of Master of Science at the Department of Electronic Systems at the Norwegian University of Science and Technology (NTNU) in Trondheim, Norway. The work was carried out between January and July 2019.

I would like to express my sincere gratitude to my supervisor, Assiociate Professor Morten Olavsbråten at the Department of Electronic Systems. His commitment to his students and his never-ending support and encouragement has been invaluable during my time as a master's student.

Trondheim, July 2019
Kristoffer Krav Skjølseth

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Abbreviations

RF	=	Radio Frequency
GMSK	=	Gaussian Minimum Shift Keying
PAPR	=	Peak-to-Average Power Ratio
PA	=	Power Amplifier
DPA	=	Doherty Power Amplifier
ADS	=	Advanced Design System
ESR	=	Equivalent Series Resistance
ESL	=	Equivalent Series Inductance
PDF	=	Probability Density Function
GSM	=	Global System for Mobile Communications
OPBO	=	Output Power Back-Off
ET	=	Envelope Tracking
EER	=	Envelope Elimination and Restoration
GaN	=	Gallium nitride
HEMT	=	High-Electron-Mobility Transistor
SCPI	=	Standard Commands for Programmable Instruments
VNA	=	Vector Network Analyzer
DSP	=	Digital Signal Processor

Chapter 1

Introduction

The ever-increasing demand for higher data rates in wireless communication systems along with strict restrictions on allowable out-of-band emission presents several challenges to today's RF design engineers.

The introduction of 3G networks in 1998 marked the end of using relatively simple, constant envelope modulation schemes, like for example GMSK, used in the 2G standard. The speed and spectral efficiency requirements set by the 3G and following standards could no longer be met by only encoding information in the phases of the signals. The amplitudes also had to be made use of. The 4G LTE standard already requires data rates up to 100 Mbps [12], and with the introduction of 5G, this is expected to increase by as much as two orders of magnitude (10 Gbps) [12]. The need for information to also be encoded in the amplitude of the signals causes the signals to have high peak-to-average power ratio (PAPR).

1.1 Background

In wireless communication systems, the RF power amplifier (PA) in the transmitter is one of the most power-hungry components. This shortens the battery life of mobile devices, and creates a need for large cooling systems in base stations, which are also power-hungry and inefficient. Because of the high PAPR characteristic of modern signals, the PA's consume even more power than what they ideally have to. To avoid distorting the signal passing through a PA, the amplifying device, i.e. the transistor, must be able to amplify the peaks just as well as the average part of the input signal. However, modern, complex-modulated signals "spend" much more time on low to medium amplitude levels than on high amplitude levels, i.e. peaks. Consequently, the transistor spends much more time amplifying the average levels than the high levels, and this is a disadvantage.

For a transistor with a given bias point to operate optimally, i.e. at its highest efficiency,

the output voltage and current swings must be maximized – which they are only when the transistor is close to saturation. Here is where the problem is: as stated above, the transistor is not allowed to clip the output signal when the amplitude of the input signal is at high levels; which it is only for a fraction of the signal period, meaning the transistor is rarely close to saturation, consequently only operating at maximum efficiency only for a fraction of the time, resulting in very low average efficiency.

Increasing the average efficiency is one of the hardest challenges RFPA designers are facing when designing PA's for modern day communication systems.

1.2 Scope of Work

The objectives of the work described in this thesis is to design and characterize a power amplifier prototype operating at 3.4 GHz, employing a well-adopted efficiency enhancement technique, namely a Doherty power amplifier (DPA). The DPA is an amplifier architecture which employs two amplifiers to implement a technique called load modulation [18]. The designed prototype has two inputs, one for each amplifier, so that the phase difference between the two inputs can be dynamically controlled to reach higher levels of efficiency than what is typical for the most basic, conventional DPA architecture. An effort is also made to try to reach a greater bandwidth than what is typical for DPA's.

The design and simulations are done in Keysight's Advanced Design System (ADS), and the designed prototype is characterized in a measurement setup which uses MATLAB to fully automate the measurement procedure.

1.3 Outline of Report

Chapter 2 describes the theory needed to understand the concepts discussed in the introduction and throughout the rest of this thesis. Chapter 3 describes the DPA prototype design methodology, Chapter 4 covers the fully automated measurement setup in detail. Chapter 5 presents the measured performance of the prototype alongside the simulated performance, and in Chapter 6, the results are discussed and interpreted. Lastly, Chapter 7 concludes the work presented in this thesis.

Chapter 2

Theoretical Background

This chapter presents the basic theoretical concepts needed to understand the challenges a designer is faced with when designing circuits operating at RF and microwave frequencies. It also describes the downsides, in terms of efficiency, when using conventional RF power amplifiers (PA's). It describes the implications high PAPR has on the PA's, which will make it clear that the use of conventional amplifier architectures are not suited in modern applications where high efficiency is desired.

2.1 Transmission Line Theory

When using conventional circuit theory to describe an electrical circuit, it is assumed that the physical dimensions of the circuit are much smaller than the electrical wavelength. Unless physically very small integrated circuits are considered, this is never the case for microwave circuits.

The electrical wavelength of an RF signal can be expressed as

$$\lambda = \frac{v_p}{f} \tag{2.1}$$

The velocity of propagation is given as

$$v_p = \frac{c}{\sqrt{\epsilon_r}} \tag{2.2}$$

where c is the speed of light in vacuum, and the relative permittivity, ϵ_r, sometimes referred to as the dielectric constant of the medium, is the ratio

$$\epsilon_r = \frac{\epsilon}{\epsilon_0} \tag{2.3}$$

where ϵ is the absolute permittivity of the medium; a material property which affects the electrostatic force between two point charges in the material, and ϵ_0 is the permittivity of free space, which is approximately equal to $8.854 \cdot 10^{-12}$ F/m.

As an example, using equations 2.1 and 2.2, the wavelength of a signal with a frequency of 3 GHz in a medium with a relative permittivity of 3.0 is approximately equal to 30 mm.

Conventional analysis using discrete circuit elements described by lumped parameters assumes that currents flowing in the circuit elements do not vary spatially over the elements. Therefore, this kind of analysis will not produce reliable results when dealing with such short wavelengths. Transmission line theory, which describes distributed parameter networks, should instead be used.

A transmission line can be described by the following four parameters: resistance per unit length, **R**, inductance per unit length, **L**, conductance per unit length, **G**, and capacitance per unit length, **C**. Figure 2.1 shows a transmission line segment of length Δz.

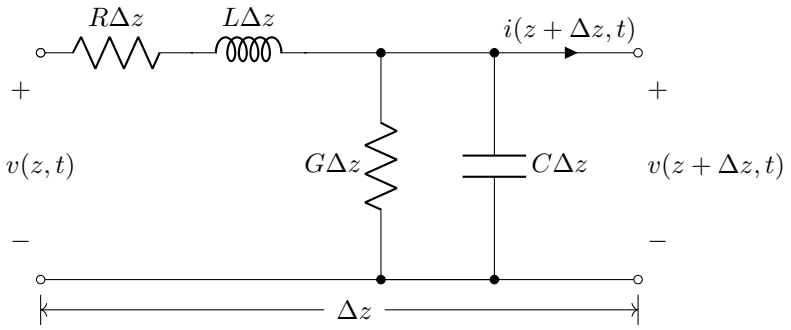


Figure 2.1: Equivalent circuit of two-conductor transmission line of length Δz.

In [4, pp. 437 - 439], Equations 2.4 and 2.5, known as the time-harmonic transmission line equations, are derived, which describe the voltage and current on a transmission line.

$$\frac{dV(z)}{dz} = -(R + j\omega L)I(z) \tag{2.4}$$

$$\frac{dI(z)}{dz} = -(G + j\omega C)V(z) \tag{2.5}$$

One of the most important parameters of a transmission line is its characteristic impedance, Z_0, which is the relationship

$$Z_0 = \frac{V(z)}{I(z)} = \sqrt{\frac{L}{C}} \tag{2.6}$$

The two most common types of transmission lines [4, pp. 427 - 428] are

Parallel-plate transmission line: consists of two parallel conducting plates separated by a dielectric material. An example of this type of transmission line is microstrip line (see 2.1.1).

Coaxial transmission line: consists of an inner conductor and a coaxial outer conducting sheath separated by a dielectric material. An example of this type of transmission line is the coaxial cables used to connect antennas to radio transmitters/receivers.

2.1.1 Microstrip Line

Microstrip line is a planar transmission line consisting of a conductor of width W printed on a thin, grounded dielectric substrate of thickness h and relative permittivity ϵ_r, as shown in Figure 2.2.

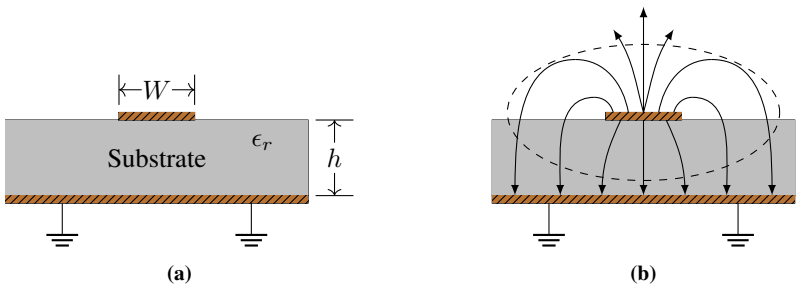


Figure 2.2: (a) Microstrip transmission line, (b) with electric and magnetic field lines shown.

Microstrip line has most of its electric field confined in the dielectric substrate between the strip conductor and the ground plane; however, a fraction of the field will be located in the air region above the substrate, and since the relative permittivity of the substrate and the relative permittivity of air is not the same, the velocity of propagation in the substrate does not equal the velocity of propagation in air. Nevertheless, since only a small fraction of the field is located in the air region, and the substrate is electrically very thin ($h << \lambda$), the combined velocity of propagation can be approximated by an expression where the relative permittivity is substituted by an effective permittivity, ϵ_{eff}:

$$v_p = \frac{c}{\sqrt{\epsilon_{eff}}} \tag{2.7}$$

An approximation of ϵ_{eff} is given in [3], which is also used to calculate the characteristic impedance, Z_0, of the microstrip line as follows:

For $\frac{W}{h} < 1$:

$$\epsilon_{eff} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} \left[\left(1 + 12 \left(\frac{h}{W} \right) \right)^{-1/2} + 0.04 \left(1 - \frac{W}{h} \right)^2 \right] \tag{2.8}$$

For $\frac{W}{h} \geq 1$:

$$\epsilon_{eff} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} \left(1 + 12 \left(\frac{h}{W} \right) \right)^{-1/2} \tag{2.9}$$

which further can be used to calculate the characteristic impedance of the microstrip line as

$$Z_0 = \begin{cases} \frac{60}{\sqrt{\epsilon_{eff}}} \ln \left(\frac{8h}{W} + \frac{W}{4h} \right), & \text{for } \frac{W}{h} < 1 \\ \frac{120\pi}{\sqrt{\epsilon_{eff}} \left(\frac{W}{h} + 1.393 + \frac{2}{3} \ln \left(\frac{W}{h} + 1.444 \right) \right)}, & \text{for } \frac{W}{h} \geq 1 \end{cases} \tag{2.10}$$

In Figure 2.3, the characteristic impedance of microstrip line is plotted as a function of conductor width, with $h = 1.5\,mm$ and $\epsilon_r = 3.4$.

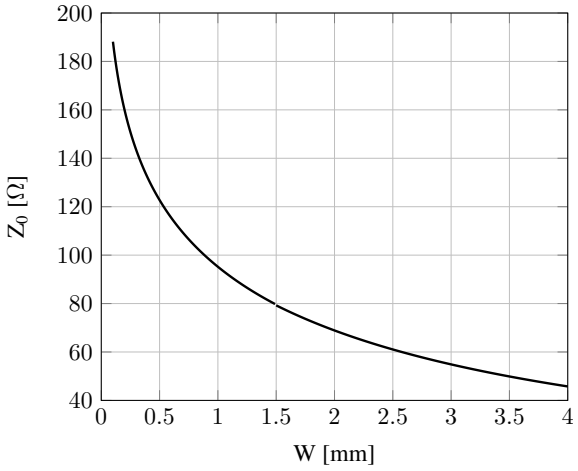


Figure 2.3: Microstrip characteristic impedance versus line width.

2.2 S-Parameters

The most common way to describe a high-frequency N-port network is by the network's scattering matrix [15, p. 178], shown below.

$$\begin{bmatrix} V_1^- \\ V_2^- \\ \vdots \\ V_N^- \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & \dots & S_{1N} \\ S_{21} & & & \vdots \\ S_{N1} & \dots & & S_{NN} \\ \vdots & & & \end{bmatrix} \begin{bmatrix} V_1^+ \\ V_2^+ \\ \vdots \\ V_N^+ \end{bmatrix}$$

V_n^+ is the amplitude of the voltage wave incident on port n, and V_n^- is the amplitude of the voltage wave reflected from port n.

The elements of the scattering matrix are called S-parameters, and they are defined as

$$S_{ij} = \left. \frac{V_i^-}{V_j^+} \right|_{V_k^+ = 0 \text{ for } k \neq j} \tag{2.11}$$

A two-port network, like a power amplifier, is described by the following scattering matrix:

$$\begin{bmatrix} V_1^- \\ V_2^- \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} V_1^+ \\ V_2^+ \end{bmatrix}$$

The input return loss of the two-port network is given by [1]

$$RL_{in} = -20 \log_{10} (|S_{11}|) \text{ [dB]} \tag{2.12}$$

and the output return loss by

$$RL_{out} = -20 \log_{10} (|S_{22}|) \text{ [dB]} \tag{2.13}$$

The small-signal gain magnitude is given by

$$|G| = |S_{21}| \text{ [dB]} \tag{2.14}$$

and the reverse gain as

$$G_{rev} = 20 \log_{10} (|S_{12}|) \text{ [dB]} \tag{2.15}$$

The input and output reflection coefficients, Γ_{in} and Γ_{out}, are equivalent to S_{11} and S_{22} respectively.

[1] Return loss is often given as the negative of this quantity.

2.3 The Quarter-wave Transformer

A quarter-wave transformer is nothing but a $\lambda/4$-long transmission line with characteristic impedance Z_0. However, it has a very useful property: the input impedance of a length of transmission line connected to an arbitrary load impedance, Z_L, is

$$Z_{in} = Z_0 \frac{Z_L + jZ_0 \tan \beta l}{Z_0 + jZ_L \tan \beta l} \tag{2.16}$$

where $\beta = 2\pi/\lambda$.

When $l = \lambda/4$, $\beta l = \pi/2$, and Equation 2.16 simplifies to

$$Z_{in} = \frac{Z_0^2}{Z_L} \tag{2.17}$$

which shows that such a transmission line has the effect of transforming the load impedance in an inverse manner. Quarter-wave transformers are therefore often used as matching elements to match different impedances.

Using quarter-wave transformers as matching elements, however, has an obvious disadvantage. Since a $\lambda/4$-long transmission line will only be $\lambda/4$ long for one frequency, the bandwidth of the quarter-wave transformer is limited.

A way to get around this, is by not only using a single quarter-wave transformer, but to connect several $\lambda/4$-long transmission lines with different characteristic impedances in series, in what is known as a multisection matching transformer. Different types of multisection matching transformers are described in detail by Pozar in [15, pp. 250-269].

2.4 Basic RF Power Amplifier Design Theory

Figure 2.4 shows a generic power amplifier circuit. This section will go through the basic theory behind every part of the circuit in the figure.

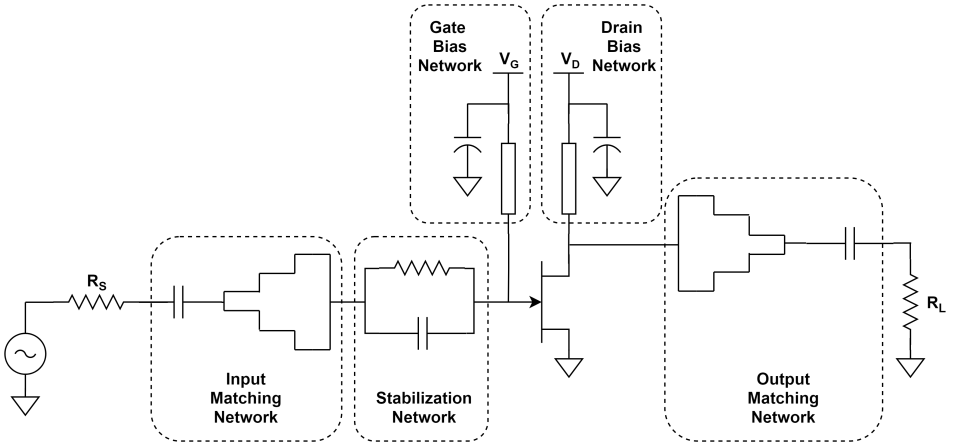


Figure 2.4: Generic power amplifier circuit.

2.4.1 Matching Networks

In a power amplifier, the main purpose of the matching networks at the input and output is to ensure maximum power transfer between the signal generator at the input and the input of the transistor (the gate), and between the output of the transistor (the drain), and the load.

Maximum power is delivered to any resistive load connected to any generator when the load resistance equals the source resistance of the generator, i.e., when the load resistance is *matched* to the source's output resistance. For complex valued impedances, the same applies, but the load impedance must now be the complex conjugate of the source's output impedance, so that the reactive parts "cancel out". This is known as a conjugate match.

2.4.2 Bias Networks

In order to connect the DC bias voltages to the device, a bias networks are needed. This usually consists of relatively large decoupling capacitors acting as a charge reservoir, with series impedances connecting the bias points to the active device, as shown in Figure 2.5.

The role of the bias networks are to prevent the RF signal from leaking out of the amplifier circuit and into the DC power supply, ideally by appearing as an open circuit to the signal, including all harmonics. This is to ensure stability and preservation of signal power. Quarter-wave transformers AC-coupled to ground in the DC connection end are often used

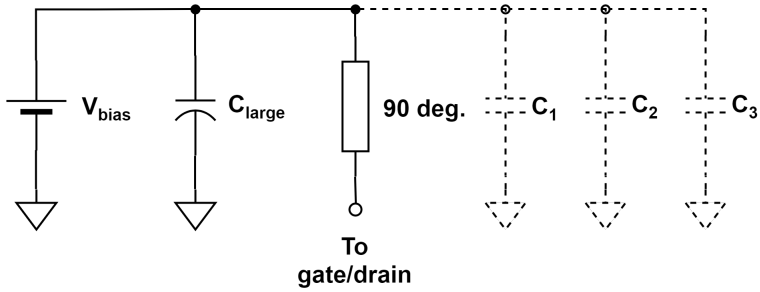


Figure 2.5: Bias network example.

to achieve this, which represents an open circuit to all odd-order harmonics. However, for even-order harmonics, a quarter-wave transformer represents a short circuit, so additional capacitors, smaller than the main reservoir capacitor, must be added between the DC connection point and ground to short circuit any part of the RF signal leaking through the quarter-wave transformer. Several capacitors of different sizes are usually used to make sure that all harmonics are shorted. The "stacking" of capacitors in parallel also reduces the net ESR (equivalent series resistance) and ESL (equivalent series inductance) of the capacitors.

Proper bias circuit design is crucial for an RF power amplifier to operate properly. The gate and drain bias voltages are often derived from the same supply, so if there is RF leakage at the drain (the output of the device), this can be coupled back to the gate (the input of the device) through the supply and lead to positive feedback, and consequently oscillations.

2.4.3 Stabilization Network

In addition to the bias networks, a dedicated stabilizaton network must often be employed to ensure stable amplifier operation. Cripps provides a detailed description of common RFPA stability issues, and how to tackle these using proper bias and stabilization network design in [8, pp. 337-357].

If either the input impedance (looking into the gate of the transistor) or the output impedance (looking into the drain of the transistor) has a negative real part, i.e., $|\Gamma_{in}| > 1$ or $|\Gamma_{out}| > 1$, oscillation is possible [15, pp. 564 - 570].

Any amplifier circuit is required to be unconditionally stable: a network is unconditionally stable if $|\Gamma_{in}| < 1$ and $|\Gamma_{out}| < 1$ for all passive source and load impedances.

The basic idea behind the stabilization network is that it adds the required positive resistance to cancel out the negative resistance causing the oscillations. Very often in RFPA circuits, oscillations occur at relatively low frequencies, i.e., a few hundred MHz. The capacitor shown in the stabilization network in Figure 2.4 makes the stabilization network frequency-selective, so that unecessary loss is not introduced at higher frequencies than what is needed.

A common test for unconditional stability is the μ-test:

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22}| - \Delta S_{11}^*| + |S_{12}S_{21}|} > 1$$

where

$$\Delta = S_{11}S_{22} - S_{12}S_{21}$$

2.5 Conduction Angle and Amplifier Classes

An amplifier's class of operation may be defined by its quiescent bias point, or by its conduction angle. The bias point of a device can be defined as the steady-state DC voltage or current at a specified terminal of an active device such as a transistor with no input signal applied [1]. The device output conduction angle, α, of an amplifier is defined as the fraction of the RF signal period where a non-zero current is flowing [6, p. 23]. Different quiescent bias points and different conduction angles, corresponding to different classes of operation, are illustrated in Figure 2.6a and Figure 2.6b, respectively. In Figure 2.7, waveforms of two different conduction angles are shown.

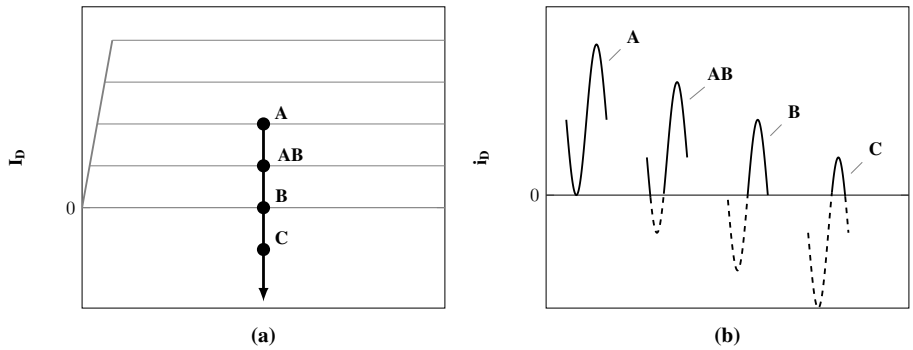


Figure 2.6: Amplifier class of operation based on (a) bias point, (b) conduction angle.

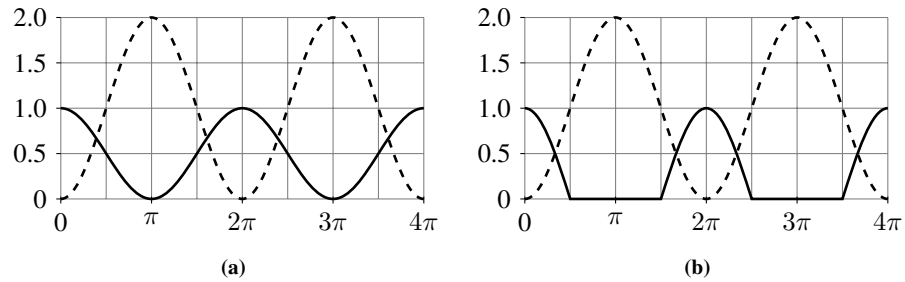


Figure 2.7: Conduction angle, voltage (dashed), current (solid), (a) $\alpha = 2\pi$, (b) $\alpha = \pi$.

In Figure 2.7a, the conduction angle is $\alpha = 2\pi$, and in Figure 2.7b, the conduction angle is $\alpha = \pi$, corresponding to class A and class B, respectively. A device operating in class AB has its bias point and conduction angle between that of class A and class B, and a device operating in class C has its bias point and conduction angle below that of class B. Different classes of operation and corresponding conduction angles are summarized in Table 2.1.

Table 2.1: Class of Operation and Conduction Angles

Class of Operation	Conduction Angle (α)
A	$\alpha = 2\pi$
AB	$\pi < \alpha < 2\pi$
B	$\alpha = \pi$
C	$0 \leq \alpha < \pi$

2.6 Efficiency of Conventional RF Power Amplifiers

The efficiency, η, of a power amplifier relates the RF fundamental output power to the DC supply power, by the relationship [8, pp. 41 - 45]

$$\eta = \frac{P_{RF}}{P_{DC}} \tag{2.18}$$

where P_{RF} is given by

$$P_{RF} = \frac{V_{DC}}{\sqrt{2}} \cdot \frac{I_{RF}}{\sqrt{2}} \tag{2.19}$$

V_{DC} is the RF output voltage amplitude, and I_{RF} is defined as

$$I_{RF} = \frac{I_{max}}{2\pi} \cdot \frac{\alpha - sin\,\alpha}{1 - cos(\alpha/2)} \tag{2.20}$$

Here, I_{max} is the output current amplitude, and α is the conduction angle. The DC supply power is

$$P_{DC} = V_{DC} \cdot I_{DC} \tag{2.21}$$

where I_{DC} is given by

$$I_{DC} = \frac{I_{max}}{2\pi} \cdot \frac{2 \cdot sin(\alpha/2) - \alpha \cdot cos(\alpha/2)}{1 - cos(\alpha/2)} \tag{2.22}$$

Another commonly used efficiency measure is power-added efficiency (PAE), which also takes into account the RF drive power required, and is defined as

$$PAE = \frac{P_{RF} - P_i}{P_{DC}} \tag{2.23}$$

where P_i is input RF drive power. Since input power is also considered, PAE is dependent on gain.

In Figure 2.8, efficiency is plotted as a function of conduction angle under ideal conditions: maximum linear current swing up to I_{max}, and maximum voltage swing of $2{\cdot}V_{DC}$. I_{max} and V_{DC} are both normalized to a value of 1.0.

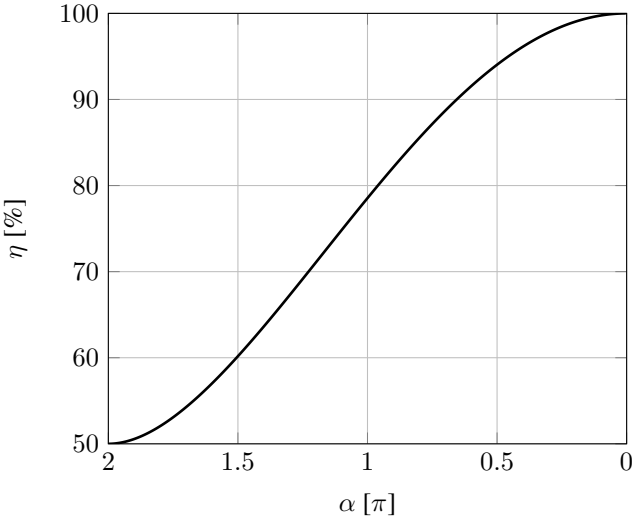


Figure 2.8: Efficiency as a function of conduction angle

From the figure, it can be seen that maximum efficiency is 50 % for class A, 78.5 % for class B, and 100 % for class C (when $\alpha = 0$ and no current flows).

2.7 High PAPR – Effects on Efficiency

The plot in Figure 2.8 shows *maximum* efficiency. As mentioned in section 1.1, a PA used to amplify non-constant envelope signals must be able to accommodate signal peaks just as well as the average part of the signal: to avoid clipping the signal peaks, the PA cannot be driven too hard, i.e., it is only allowed to run at maximum output power when the input signal is at a peak. In modern communication systems employing complex modulation schemes, the average input drive level is often much lower than the peak input drive level, meaning that the average efficiency, also sometimes referred to as back-off efficiency, which is a function of the input signal's probability density function (PDF), will be much lower than that shown in Figure 2.8.

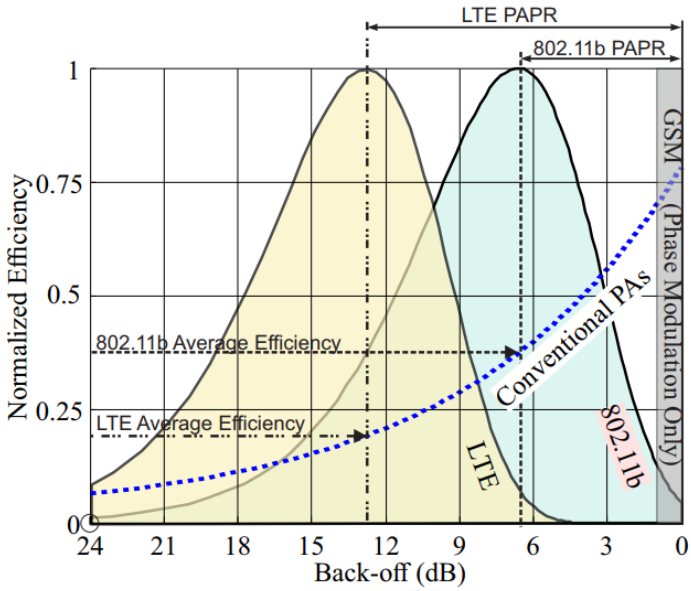


Figure 2.9: Efficiency as a function of OPBO. Figure from [18].

In Figure 2.9, efficiency as a function of output power back-off (OPBO), which is the amount of output power reduction with respect to the maximum, is shown for a conventional Class AB PA along with the probability density functions of three different modulated signals.

The figure shows that the average efficiency of a theoretical, ideal class AB PA used in 802.11b (WLAN) systems is only around 40 %, while in 4G LTE systems, it is even lower – shown at below 25 %. To the far right in the figure, the PDF of a GSM signal is shown to be constant. This is because GSM uses constant envelope signalling, meaning that the PA's can be driven hard at all times without the risk of distorting the signal because of peak clipping, consequently allowing for high-efficiency operation at all times.

2.8 Increasing the Back-off Efficiency

The root of the low back-off efficiency problem is that, in a sense, the transistor is not utilized to it's full potential. Figure 2.8 shows efficiency as a function of conduction angle under ideal conditions, as stated above. Ideal conditions here means that the current is allowed to swing up to I_{max}, which is the maximum value before it starts clipping, and the voltage is allowed to swing up to a value of $2 \cdot V_{DC}$. Only when the voltage and current swings are at their maximum, maximum efficiency can be achieved. These voltage and current swings are shown in Figure 2.10.

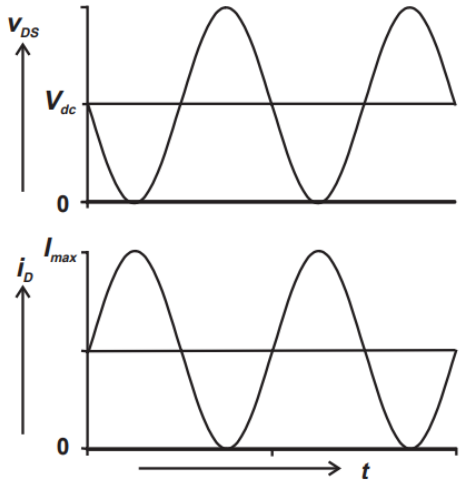


Figure 2.10: Maximum voltage and current swings. Figure from [8, p. 23].

The current amplitude is $I_{max}/2$, and the voltage amplitude is V_{dc}.

The current and voltage swings can be related by an optimal load resistance, R_{opt}, given by

$$R_{opt} = \frac{V_{dc}}{I_{max}/2} = 2 \cdot \frac{V_{dc}}{I_{max}} \tag{2.24}$$

This is also known as the load line resistor. Figure 2.11 shows the I-V curves of an idealized transistor together with the so-called load line. The slope of the load line is $1/R_{opt}$.

When output power is backed off, the load line decreases in length, i.e., point P1 in Figure 2.11 moves towards point P2 (which is fixed). This means that the current and voltage swings are no longer are maximized, consequently, maximum efficiency is no longer achieved. However, if point P1 could be fixed in the horizontal dimension, only being allowed to move vertically towards point P3, maximum swing could be ensured for a range of back-off levels, i.e., for a range of input drive levels. From the figure, there are two ways of achieving this: either by decreasing the angle θ as the output power is backed off, or by moving point P2 along the x-axis towards point P3. This is illustrated in Figure 2.12, and is known as load modulation and bias modulation, respectively.

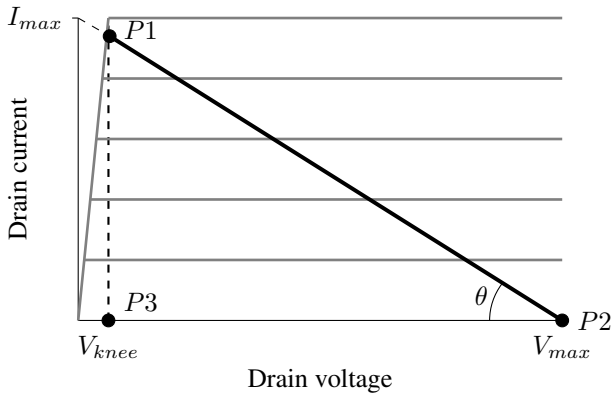


Figure 2.11: Idealized transistor I-V curves and load line.

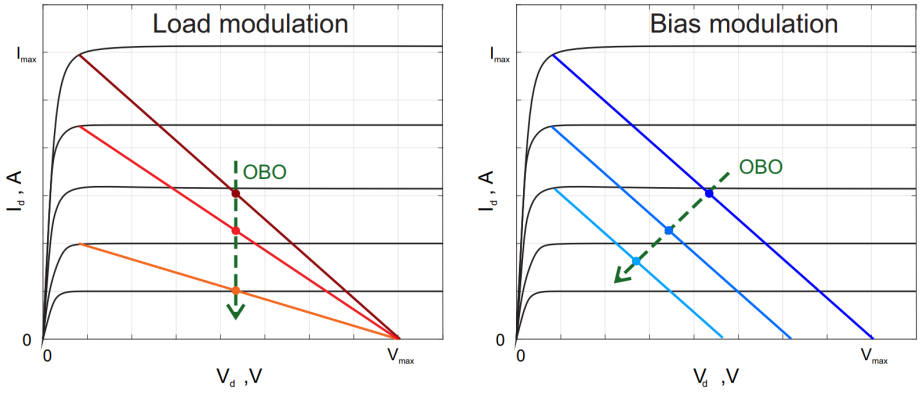


Figure 2.12: Load and bias modulation. Figure from [18].

Both of these techniques emerged many years ago. Load modulation, utilized in the Doherty power amplifier architecture proposed by William H. Doherty in 1936 [9], and bias modulation utilized in the envelope elimination and restoration (EER) technique proposed by Leonard R. Kahn in 1952 [13]. Both originally intended to increase the efficiency in high power, short wave broadcast stations, but later lost traction due to the transition to FM systems, which are constant envelope, thus eliminating the need for such techniques. They later gained interest again, when more and more systems started utilizing non-constant envelope modulation schemes.

There are several other techniques based on load modulation and bias modulation, e.g. outphasing [5, 17] and envelope tracking (ET) [2, 10], but these are not discussed in this thesis.

2.9 Active Load Modulation

This section presents a further analysis of what happens when the voltage amplitude of the RF input signal is reduced from that required to produce maximum RF swings at the output of the amplifier. The analysis is based on [8, pp. 43 - 46 and pp. 286 - 288].

The voltage and current waveforms used in the analysis are the ones shown in Figure 2.13. Notice the half-wave rectified current waveform, meaning that the amplifier producing these waveforms is operating in class B.

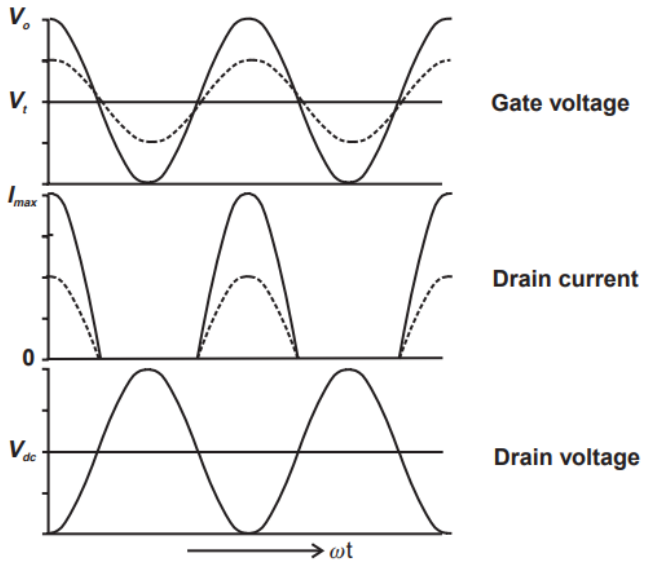


Figure 2.13: Waveforms for efficiency analysis, full drive (solid) and 6 dB back-off condition using a load resistor having twice the normal load line value (dotted). Figure from [8].

Since the fundamental component of the half-wave rectified current waveform is the same as in the non-rectified case, namely $I_{max}/2$, the load resistor is given by

$$R_{opt} = 2 \cdot \frac{V_{dc}}{I_{max}} \tag{2.25}$$

just as before. The RF output power is given by

$$P_{RF} = \frac{V_{dc} \cdot I_{max}}{4}$$

and the DC supply power is given by

$$P_{DC} = \frac{V_{dc} \cdot I_{max}}{\pi}$$

The efficiency is then

$$\eta = \frac{P_{RF}}{P_{DC}} = \frac{\pi}{4} \approx 78.5\,\%$$

just as shown in Figure 2.8.

As discussed in section 2.7, a reduction in input drive level, corresponding to a reduction in output current and voltage swing, will have severe effects on the efficiency of the amplifier. If the voltage amplitude of the input RF signal is reduced by a factor ρ from the ideal level which produces maximum output swing, the fundamental component of the RF current will be [8, pp. 287 - 288]

$$I_{RF} = \frac{I_{max}}{2\rho}$$

The output voltage swing will have an amplitude given by

$$V_{RF} = \frac{I_{max}}{2\rho} \cdot R_{opt} = \frac{V_{dc}}{\rho}$$

so the RF output power is now given by

$$P_{RF} = \frac{V_{dc} \cdot I_{max}}{4\rho^2} \tag{2.26}$$

and the DC supply power is

$$P_{DC} = \frac{V_{dc} \cdot I_{max}}{\rho\pi} \tag{2.27}$$

Hence, the efficiency is now

$$\eta = \frac{\pi}{4\rho} \tag{2.28}$$

This means that for example a 6 dB reduction in drive power results in a 6 db reduction in output power, but corresponds to a drop in efficiency from 78.5 % to 39.3 %. The reason for this is that the load value chosen (Equation 2.25) is not the optimal value in the 6 dB back-off case. However, if the load is allowed to change its value dynamically as

$$R_\rho = \frac{V_{dc}}{I_{max}} \cdot 2\rho \tag{2.29}$$

the load value would be $2 \cdot R_{opt}$ for the 6 dB back-off condition, which for that specific condition, is the optimal value. The efficiency would then be 78.5 % also for the back-off condition.

2.10 The Doherty Power Amplifier

Changing the load resistance dynamically as a function of input drive level is exactly what the Doherty power amplifier (DPA) does. The following explanation of how the DPA works is based on [6, pp. 438 - 441] and [8, pp. 290 - 298].

The DPA uses an active load-pull technique, where the resistance or reactance of an RF load is modified by applying current from a second, phase coherent source, see Figure 2.14.

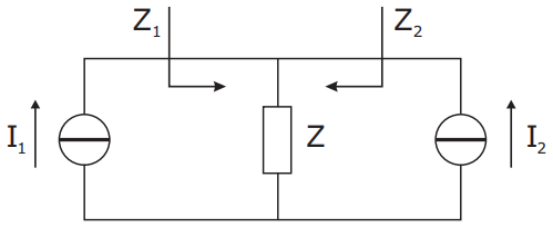


Figure 2.14: The active load principle. Figure from [6, p. 438].

The impedance presented to each of the two current sources in Figure 2.14 is given by

$$Z_1 = \frac{(I_1 + I_2) \cdot Z}{I_1} = Z\,(1 + \frac{I_2}{I_1}) \tag{2.30}$$

$$Z_2 = \frac{(I_1 + I_2) \cdot Z}{I_2} = Z\,(1 + \frac{I_1}{I_2}) \tag{2.31}$$

Thus, the load seen by one current source is controlled by the current contribution from the other source. To ensure proper load modulation, the resistance seen by the left generator must decrease as the current contribution from the right generator increases. To achieve this, Figure 2.14 must be modified to that of Figure 2.15, in which an impedance inverting network has been added. This causes the impedance seen by the left generator to decrease, instead of increase, as the current contribution from the right generator increases.

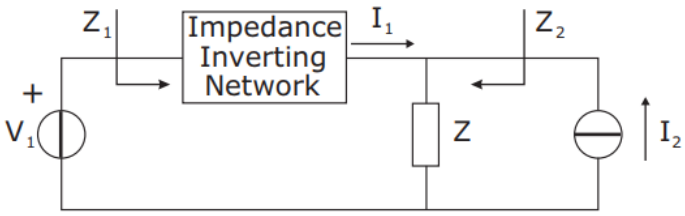


Figure 2.15: Active load scheme with impedance inverter. Figure from [6, p. 439].

Figure 2.16 shows the typical DPA configuration: the RF input signal is split between a main amplifier and an auxiliary amplifier. The quarter-wave transformer at the output of

the main amplifier is the impedance inverter mentioned above, and the quarter-wave long transmission line at the input of the auxiliary amplifier is there to compensate for the 90° phase shift introduced by the impedance inverter.

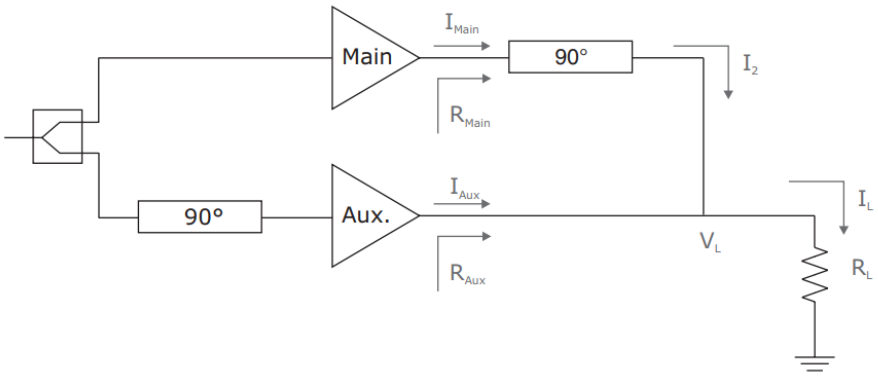


Figure 2.16: Typical Doherty configuration. Figure from [6, p. 436].

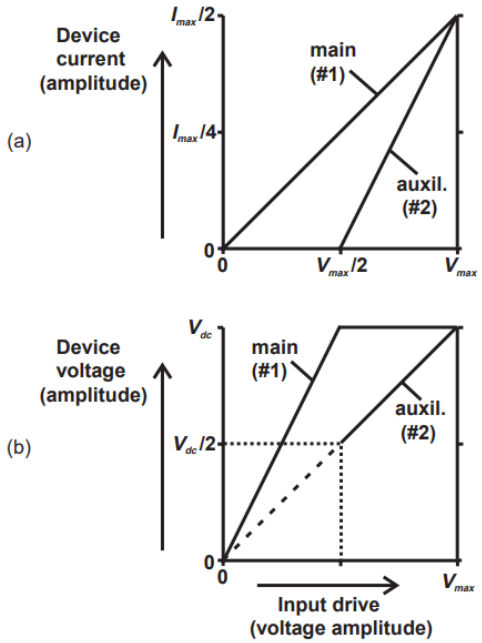


Figure 2.17: RF amplitude variations versus input drive. (a) Device currents, (b) Device voltages. Figure from [8, p. 296].

For a range of input drive levels up to a certain point, typically the point corresponding to 6 dB output power back-off (OPBO), only the main amplifier contributes with current to the load, and the auxiliary amplifier is said to be off. This is often referred to as the low power region. At 6 dB OPBO, the auxiliary amplifier turns on, and adds an additional current contribution through the load. From the 6 dB OPBO point, up to 0 dB OPBO, often referred to as the Doherty region, the main amplifier can be considered as the left generator, and the auxiliary amplifier as the right generator in Figure 2.15. In Figure 2.17, transistor currents and voltages are shown.

Figure 2.17a shows that only the main device contributes with current up until the input drive level reaches $V_{max}/2$, corresponding to an output current of $I_{max}/4$, which in turn corresponds to 6 dB OPBO, where the auxiliary device also starts conducting. Figure 2.17b shows that the main device voltage is held constant from the point where the auxiliary device starts conducting.

2.11 Efficiency of the Doherty Power Amplifier

The overall efficiency of the DPA as a function of input drive level is in [8, pp. 297 - 298] shown to be

$$\eta = \frac{\pi}{2} \cdot \frac{\left(\frac{v_{in}}{V_{max}}\right)^2}{3 \cdot \left(\frac{v_{in}}{V_{max}}\right) - 1} \tag{2.32}$$

where v_{in} is input drive level, and V_{max} is the input drive level corresponding to 0 dB OPBO.

It can be seen that Equation 2.32 equals $\pi/4$ for both $v_{in} = V_{max}$, corresponding to 0 dB OPBO, and for $v_{in} = V_{max}/2$, corresponding to 6 dB OPBO.

Figure 2.18 shows the theoretical efficiency curve of the DPA as a function of input power. The vertical line labelled “Break point” corresponds to 6 dB OPBO.

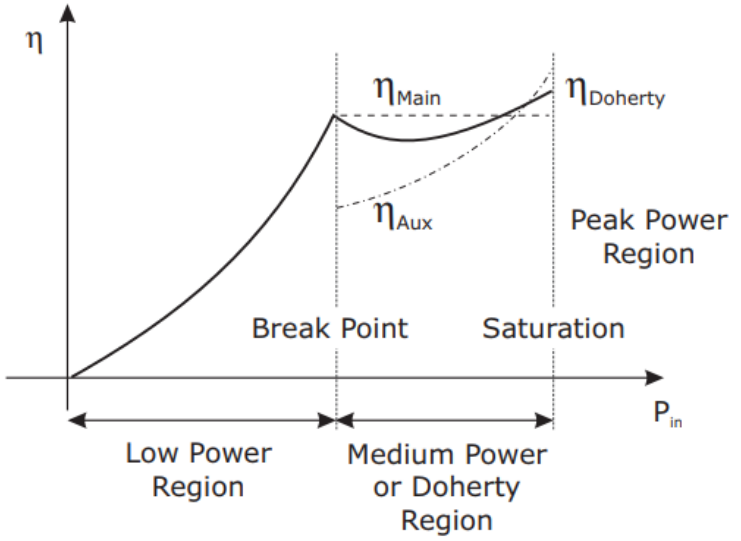


Figure 2.18: Theoretical efficiency of the DPA as a function of input power. Figure from [6, p. 437].

2.12 Bandwidth of the Doherty Power Amplifier

The major limitation of the DPA architecture is its narrow bandwidth. The bandwidth limitation is due to the quarter-wave transformer used as impedance inverter only being $\lambda/4$ long at the design frequency, as discussed in section 2.3.

The bandwidth, or efficiency bandwidth, of DPA's are typically defined as the range of frequencies over which the efficiency at 6 dB OPBO drops no more than 10 % below the maximum efficiency. At 0 dB OPBO, the bandwidth is unaffected by the quarter-wave transformer, since the effective main device load impedance will then equal the characteristic impedance of the quarter-wave transformer.

In [16], an efficiency analysis of the circuit in Figure 2.15 is done by showing the frequency depencence of the voltages and currents in the circuit, and then using these frequency-dependent voltages and currents in the equation

$$\eta = \frac{\pi}{4} \frac{Re\left(V_1(f) \cdot I_1^*(f)\right) + Re\left(V_L(f) \cdot I_2^*(f)\right)}{|V_{1,max}||I_1(f)| + |V_{2,max}||I_2(f)|} \tag{2.33}$$

Figure 2.19 shows that the fractional efficiency-bandwidth is 28 % at 6 dB OPBO. However, this is with ideal devices which act like perfect current sources.

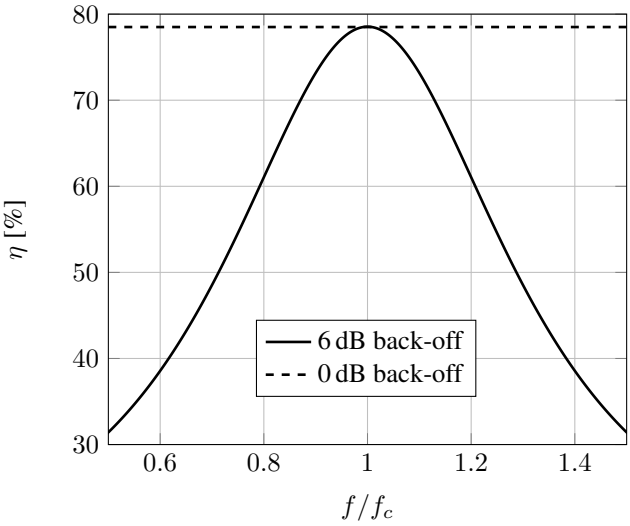


Figure 2.19: Efficiency vs. normalized frequency.

All real devices have parasitic output reactances due to capacitance between drain and source, bond wires and bond pads, which become very apparent at high frequencies. Designing fixed-load matching networks which resonate out these reactances is usually not particularly difficult, but designing matching networks which does this over a range of different load impedances (R_{opt} to $2{\cdot}R_{opt}$) is very challenging.

Because of this, conventional DPA implementations typically show efficiency bandwidths of only 5 to 10 % [16].

2.13 Variations of the Doherty Architecture

A great overview of different variations of the DPA architecture is given in the article "High-Efficiency Doherty Power Amplifiers: Historical Aspect and Modern Trends" [11]. One of which is the digitally driven, or digital DPA, where the amplifier has two inputs, one for the main amplifier and one for the auxiliary amplifier.

2.13.1 Digital Doherty Power Amplifier

A dual-input DPA allows for the input signal of each branch to be digitally preprocessed in terms of phase and power levels, and supplied separately to each input to optimize the overall performance of the DPA.

Chapter 3

Design methodology

This chapter presents the methodology used in the Doherty amplifier design process. As mentioned in Chapter 1, Keysight's Advanced Design System (ADS) is used for the circuit design and simulations.

3.1 Preliminary Design Considerations

In the theory presented so far, as well as in Doherty's original implementation [9], both the main and the auxiliary device are biased in class B. This approach gives rise to an obvious issue: if the main device is to be held in saturation in the Doherty region, the auxiliary device has to be turned on only when the main device reaches saturation, which will not happen if both devices have the same bias. If the auxiliary device is biased in class C, so that a higher drive level is required for it to turn on, this issue is resolved. However, if two identical devices are used, the class C biased device will not be able to deliver the required $I_{max}/2$ current swing. Two ways to get around this are by scaling up the auxiliary device, or by having unequal power splitting on the input of the amplifier. Cripps recommends a device scaling factor of 2.5 [8, p. 299].

To keep the design simple, however, identical devices are used in this thesis. Class AB bias for the main amplifier is also typically preferred over pure Class B, because of its increased linearity [6, p. 443].

Because of the reasons mentioned above, the AB/C-Doherty implementation is chosen in this thesis work.

The basis for the DPA prototype design is shown in Figure 3.1. As can be seen in the figure, it has two inputs, so that the auxiliary path phase delay can vary as a function of input drive level, much like in a digital Doherty. Furthermore, the figure shows that a $35\,\Omega$ quarterwave transformer is used to transform the $50\,\Omega$ load to $25\,\Omega$. This, in combination

with the $50\,\Omega$ quarterwave transformer connected between the two matching networks, will ensure that both amplifiers will see a $50\,\Omega$ load at 0 dB OPBO. At 6 dB OPBO, the $50\,\Omega$ quarterwave transformer will transform the $25\,\Omega$ to $100\,\Omega$ for the main amplifier, which in turn is matched/transformed to R_{opt} and $2 \cdot R_{opt}$ respectively, by the matching network connected to the output of the main device.

The following sections describe the methodology used to design the circuit in Figure 3.1.

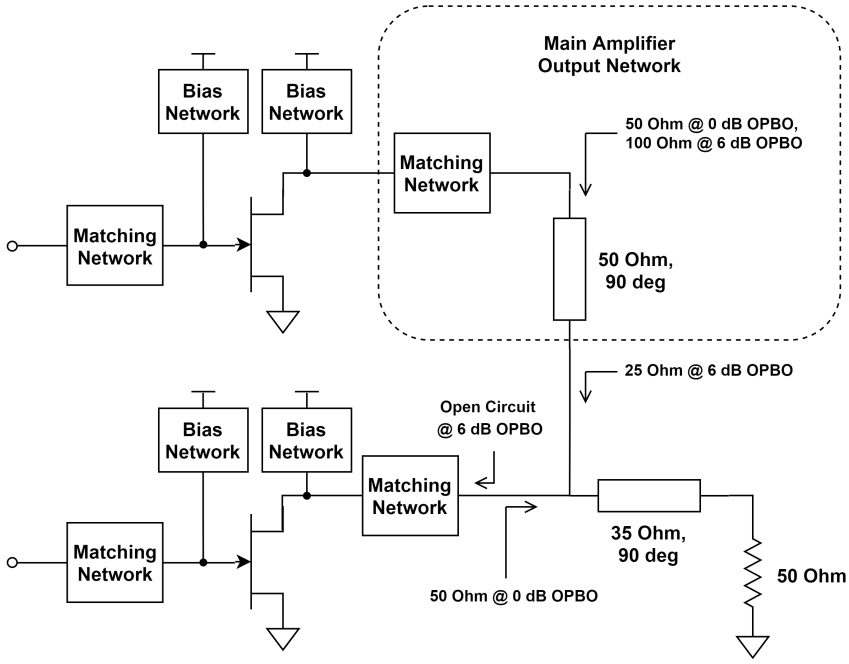


Figure 3.1: Doherty design basis.

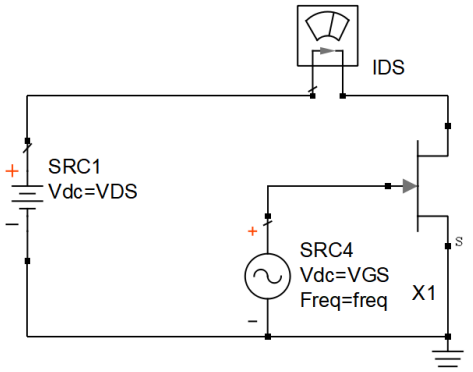
3.2 Transistors and Biasing

The main and auxiliary device utilized in the design is the Cree CG2H40010 10 W RF power GaN HEMT [7, (datasheet)], and both devices operate from a 28 V rail.

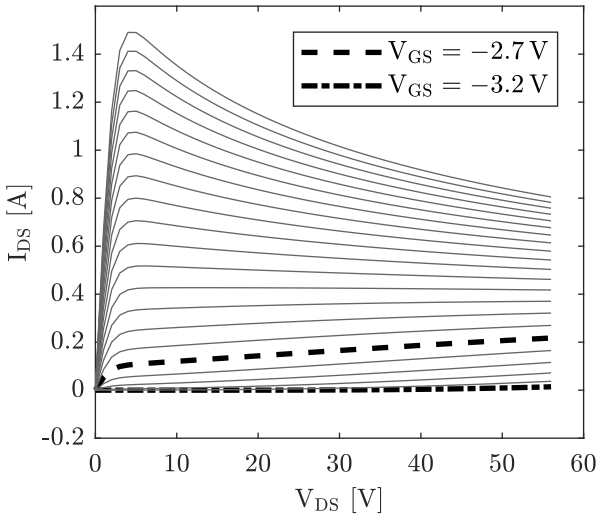
Proper biasing of the two devices is determined by doing a parametric sweep of V_{GS} and V_{DS} in the simulation setup shown in Figure 3.2a. V_{GS} is swept from -3.4 V to -1.1 V, and V_{DS} is swept from 0 to 56 V. This produces the I-V curves shown in Figure 3.2b.

The results show that at $V_{DS} = 28\,V$, a gate bias voltage $V_{GS} = -2.7\,V$ produces a drain bias current $I_{DS} = 161\,mA$, which results in a reasonable class AB bias condition.

Determining what will be a good class C bias condition is slightly more difficult, since there will be no quiescent current flow when the device is biased below threshold, but the results show that $V_{GS} = -3.2\,V$ results in a drain bias current $I_{DS} = 0$, which means that any $V_{GS} < -3.2\,V$ corresponds to a class C bias condition.



(a)



(b)

Figure 3.2: (a) I-V curve generation circuit, (b) Generated I-V curves.

3.3 Initial Matching Networks

The devices' input and output impedances must be matched to the source and load impedances for the reasons described in Chapter 2. Designing wide-band output matching networks is often challenging due to the fact that real transistors have parasitic output reactances which become very apparent at high frequencies. Most often the dominant part of this reactance is the capacitive part, and it is often enough to compensate for this part to achieve high bandwidth.

The basic idea behind the methodology used in the design of the matching networks is to first find the input and output impedances at the design frequency (3.4 GHz), using small-signal analysis (S-parameters), and then design an initial wide-band matching network which matches these impedances to $50\,\Omega$. After having designed the initial matching networks, large-signal analysis is used together with ADS' optimization functionality to optimize the matching networks for maximum output power and efficiency.

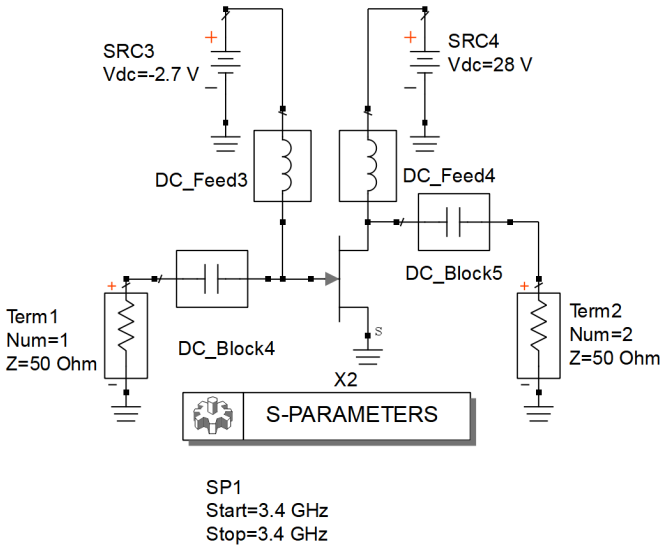
Small-signal analysis will not work for a class C biased device, since small signal excitation will not be enough for the device to conduct, but the initial matching network designed for the class AB biased device is also used as a starting point for ADS' optimizer when designing the final matching networks for the auxiliary device, although at the correct class C bias.

In reality, the input and output impedances will vary with frequency because of the parasitic reactances. This is not taken into account directly when using the S-parameters simulated at the design frequency to design the initial matching networks. Wide-band parasitic compensation is left to ADS' optimizer to achieve.

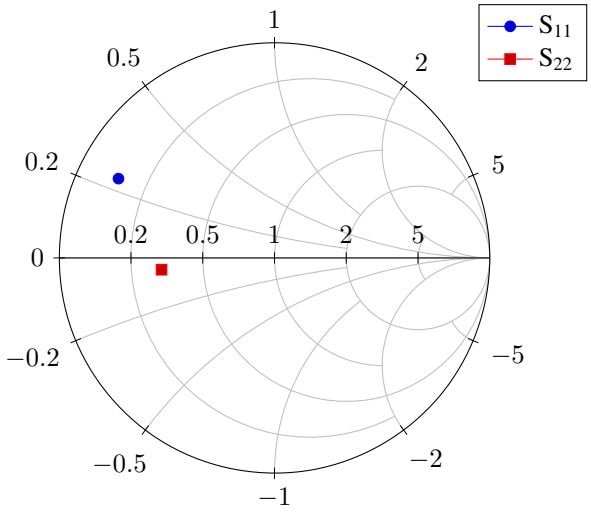
The input and output impedance of the Cree CG2H40010, biased at $V_{DS} = 28\,V$, and $V_{GS} = -2.7\,V$, is found using the simulation setup shown in Figure 3.3a. An S-parameter simulation is performed at the center frequency of 3.4 GHz, and the result is shown in Figure 3.3b.

As can be seen in Figure 3.3b, the input reflection coefficient, $\Gamma_{in} = S_{11}$, is equal to $0.812\angle 153\,°$, and the output reflection coefficient, $\Gamma_{out} = S_{22}$, is equal to $0.528\angle -174\,°$. This corresponds to an input impedance, Z_{in}, of $(5.45 + j11.85)\,\Omega$, and an output impedance, Z_{out}, of $(15.5 - j2.35)\,\Omega$, respectively. In Chapter 2 it was shown that the quarter-wave transformer typically used as impedance inverter in DPA output networks limits the bandwidth of typical DPA designs. To not impose any other "bandwidth bottlenecks" on the design these impedances must be matched to $50\,\Omega$ in a wide-band manner. The initial matching networks utilize multisection matching transformers to achieve this.

Some practical considerations regarding the physical sizes of microstrip transmission lines must be made when deciding how to design the matching networks. The substrate used in the design is RO4003C by Rogers Corporation, which has a relative permittivity, ϵ_r, of 3.4 and a thickness, h, of 0.06" = 1.524 mm. Using ADS' "LineCalc" tool, which uses the equations presented in section 2.1.1, it is found that a characteristic line impedance, Z_0, of $25\,\Omega$ corresponds to a line width, W, of 9.32 mm. This is initially considered the maximum allowable microstrip width.



(a)

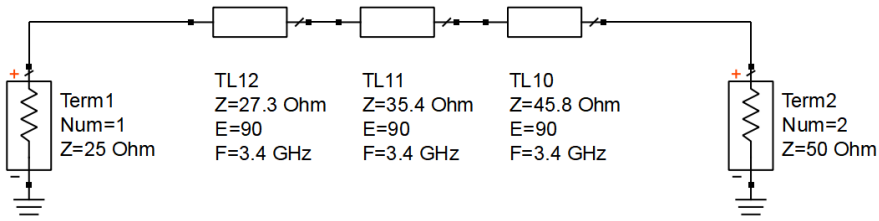


(b)

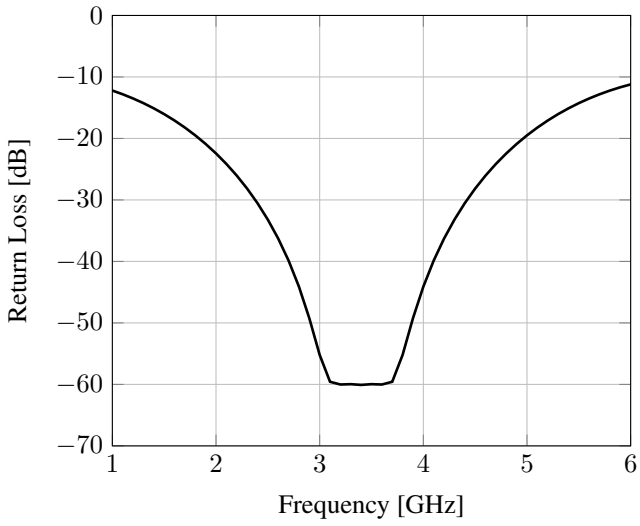
Figure 3.3: (a) S-parameters simulation setup, (b) S-parameters simulation result.

Since the first section of the matching transformer will have a characteristic impedance close to the load impedance, and the maximum allowable microstrip width corresponds to a characteristic impedance of $25\,\Omega$, the matching transformer is designed to match a load impedance of $25\,\Omega$ to a line impedance of $50\,\Omega$, as shown in Figure 3.4a.

Using three sections is considered to result in a satisfactory trade-off between bandwidth and physical size. The section impedances are calculated using Table 5.1 in [15, p. 254].



(a)



(b)

Figure 3.4: (a) 3-section matching transformer, (b) Return loss of the circuit in (a).

Figure 3.4b shows the return loss of the matching transformer.

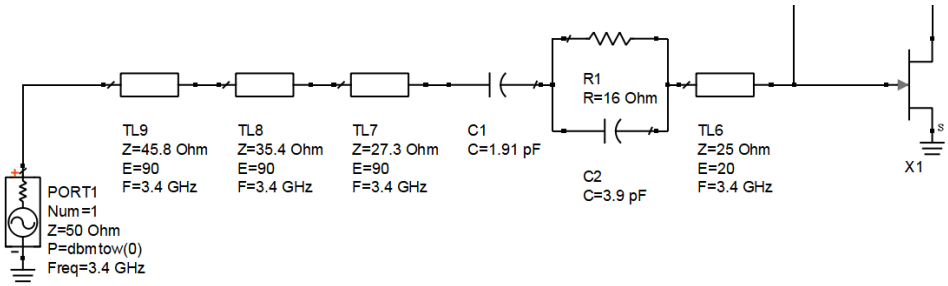
As described in section 2.3, a multisection transformer consists of several quarter-wave transformers, and a quarter-wave transformer can only be used to match a real load impedance. This means that the complex Z_{in} and Z_{out} must first be transformed to real impedances before the multisection transformers can be used.

Figure 3.5a and Figure 3.6a show the initial input and output matching networks. These are initially designed with ideal components and transmission line models which is later replaced by microstrip line models. In the input matching network, TL6, R1 and C1 transform the complex $(5.45 + j11.85)\,\Omega$ input impedance to a real impedance of $25\,\Omega$. The 3-section matching transformer comprised of TL7, TL8 and TL9 matches this impedance to $50\,\Omega$ in a wide-band manner. R1 also functions as a stabilization component, as described in section 2.4.3.

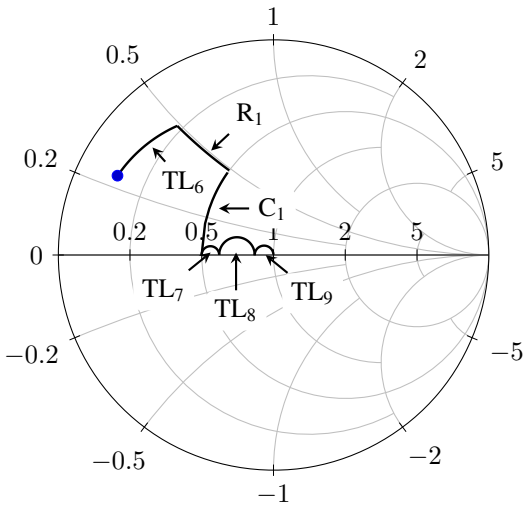
The addition of C2 makes the stabilization network frequency selective, such that loss is introduced for $f < 1/2\pi RC$.

Similarly, in the output matching network, the impedance transformation from $(15.5 - j2.35)\,\Omega$ to $25\,\Omega$ is performed by TL1 and TL2, and the same 3-section matching transformer used in the input matching network matches this impedance to $50\,\Omega$.

Figure 3.5b and Figure 3.6b show the impedance transformation performed by the matching networks.



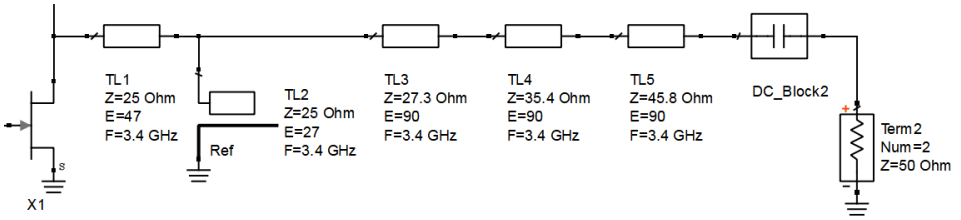
(a)



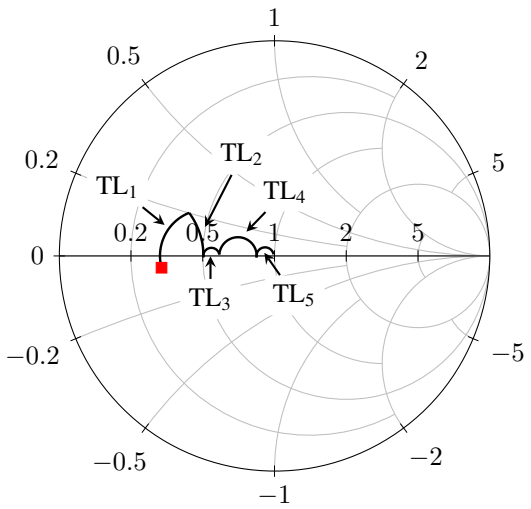
(b)

Figure 3.5: (a) Initial input matching network using ideal components, (b) impedance transforming properties of the components shown in (a).

After having designed the matching networks with initial component values found by using the Smith chart as shown above, more specific circuit performance goals are defined, and ADS' optimizer is employed to try to reach these goals.



(a)



(b)

Figure 3.6: (a) Initial output matching network using ideal components, (b) impedance transforming properties of the components shown in (a).

The goals set for the optimizer to achieve are S_{11} and $S_{22} < -25\,dB$ over a fractional bandwidth, $\Delta f/f_0$, of 50 %. The result of the optimization is shown in Figure 3.7.

Now that optimal ideal matching networks have been designed, the ideal transmission line models can be replaced by microstrip models. In addition to replacing the ideal lines, additional microstrip lines are added for practical reasons, i.e., solder pads for the capacitors and resistors etc.

To calculate the widths and lengths of the microstrip lines, “LineCalc” is used. In addition to calculating the the physical width corresponding to a specific characteristic impedance, “LineCalc” also calculates the physical length corresponding to a specific electrical length using Equation 2.7 and the relationships

$$\frac{v_p}{f} = \lambda$$
$$1 \cdot 360\,[^\circ] = 1 \cdot \lambda\,[m]$$

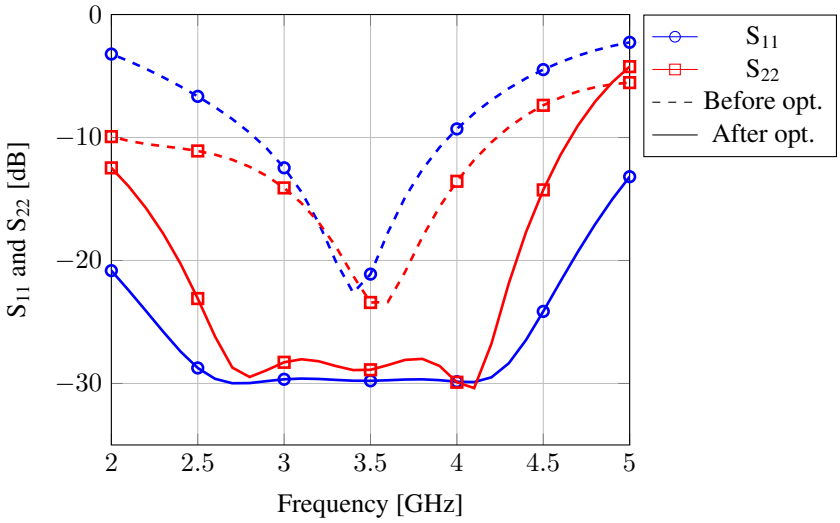


Figure 3.7: S_{11} and S_{22} with initial matching networks

The input network employing microstrip transmission line models, as well as more accurate lumped component models, is shown in Figure 3.8. A corresponding component replacement is done in the output network.

The widths and lengths of the microstrip lines and the component values of the capacitors and resistors are then made variables which the optimizer can change in order to try to reach the same goals as with the ideal input and output networks.

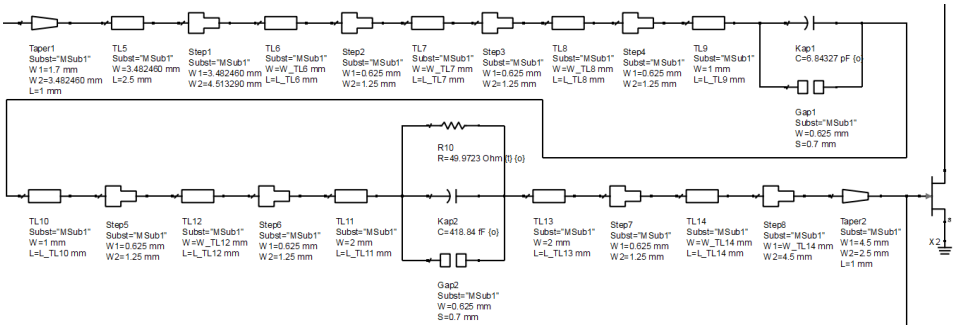


Figure 3.8: Input network using microstrip Models.

After satisfactory S-parameter results have been obtained using the optimizer in small-signal analysis, large-signal analysis can be performed, and the optimization goals modified to instead maximize gain and efficiency (described in sections 3.6 and 3.7).

3.4 Finding R_{opt}

To determine what is the optimal load for the transistor, the simulation setup shown in Figure 3.9 is used. The initial input matching network described above is connected at the input of the transistor, and an impedance tuner made by Associate Professor Morten Olavsbråten is connected to the output. The tuner allows for setting the magnitude and phase of the load reflection coefficient seen by up to three harmonics.

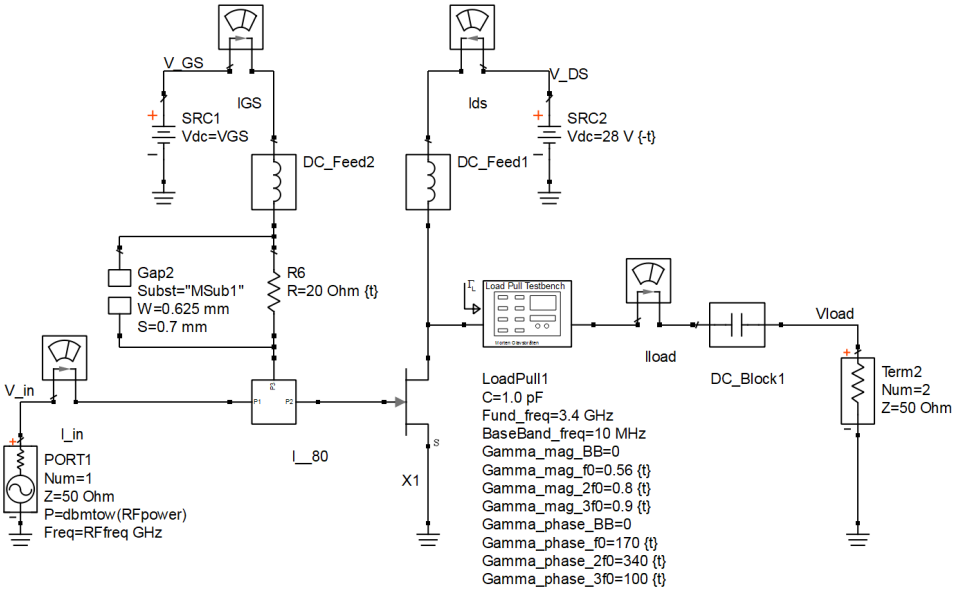


Figure 3.9: Simulation setup to determine R_{opt}.

With the ADS transistor model from Cree, the user has access to the current and voltage waveforms internal to the device, directly at the current generator plane. These waveforms are used to calculate the load reflection coefficient as

$$\Gamma_L = \frac{v_d/i_d - 50}{v_d/i_d + 50}$$

which is further used to identify under which loading conditions the transistor produces the maximum output power and efficiency.

The simulation results show that when presented with a load resulting in $\Gamma_L = 0.18\angle 180\,^\circ$, i.e., $35\,\Omega$, the transistor produces an output power of around 41.5 dBm at an efficiency of around 70 %, i.e., $R_{opt} = 35\,\Omega$ and $2{\cdot}R_{opt} = 70\,\Omega$.

3.5 Bias Networks

Replacing the ideal DC-Feed components with physically realizable bias networks will of course have an impact on the input and output impedance of the amplifier, so before advancing further in the design process, the bias networks must be implemented.

The design basis for the bias networks used in the DPA design is the circuit discussed in section 2.4.2 (Figure 2.5), shown in Figure 3.10, i.e., a quarterwave-long transmission line (TL20) connected between the gate/drain of the transistor (P2) and the DC connection point (P1), a large decoupling capacitor (C11) between this point and ground, together with additional, smaller capacitors (C12, C13 and C14).

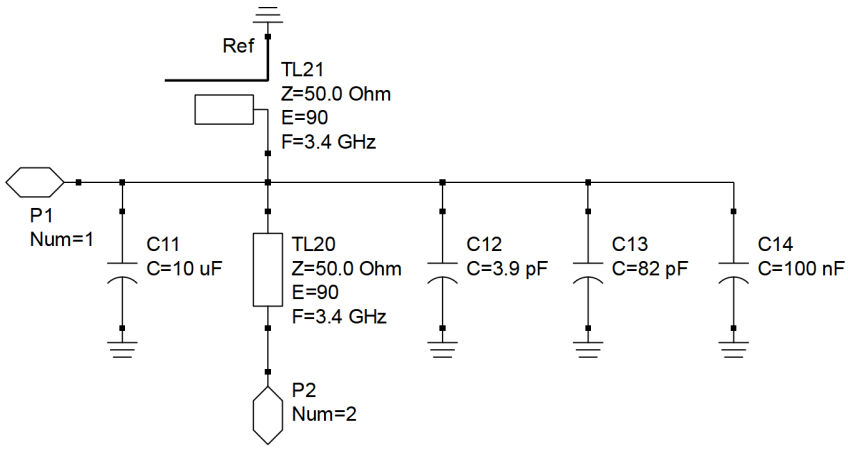


Figure 3.10: Ideal bias network.

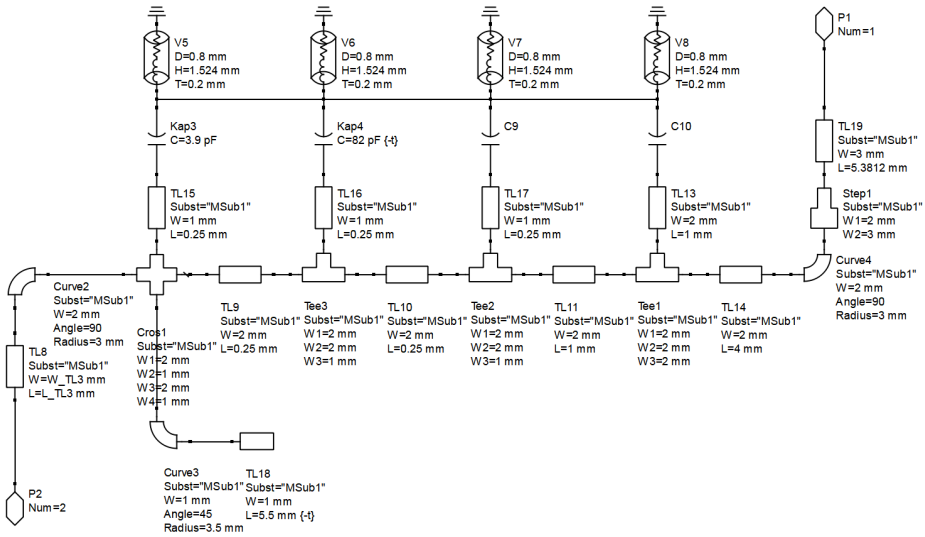
In addition to the circuit elements described in section 2.4.2, a second quarterwave-long transmission line (TL21), which is open-circuited in one end, is included to further ensure that the DC connection point is signal ground.

The network is initially designed using ideal transmission line and capacitor models (Figure 3.10) to verify that the circuit appears as an open circuit to the RF signal connected to P2 (for all odd order harmonics), which with ideal components, it does. The components are then replaced by microstrip and capacitor models which more accurately represent the physical components used in the design.

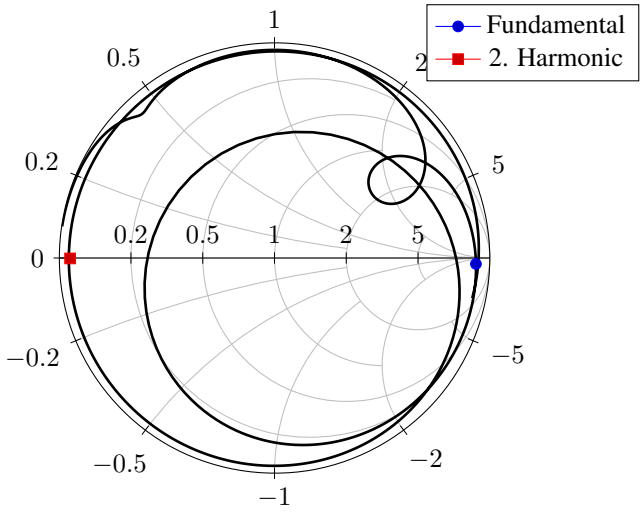
The final bias network design is shown in Figure 3.11a, and the impedance seen looking into port P2 is plotted as a function of frequency in Figure 3.11b. [1]

All capacitors used in the design are high quality ceramic Murata or Johanson Technology components in 1206 or 0603 packages.

[1] In the simulation producing this result, a $50\,\Omega$ resistor is connected to port P1. This is obviously not a very good approximation of the wires connected between the DC power supply, and the output impedance of the power sypply itself, but the simulation results are not noteworthy affected by changing this impedance.



(a)



(b)

Figure 3.11: Final bias network.

3.6 Main Amplifier Output Network

Since the $50\,\Omega$ quarterwave transformer shown in Figure 3.1 will limit the efficiency bandwidth of the amplifier (see section 2.12), ideally, the main amplifier output network should have impedance inverting properties incorporated into it, to eliminate the need for the quar-

terwave transformer. Furthermore, it should also compensate for the parasitic reactance at the output of the transistor in a wide-band manner.

Actually, from the signal's perspective, the series reactance in the bias network connected to the drain of the transistor (TL20 in Figure 3.10) will be connected in parallel with the output, effectively shunting the parasitic reactance at the output of the device. Making TL20 inductive ($< 90\,°$) is initially thought to be enough to resonate out the dominant (capacitive) part of the parasitic output reactance, but experiments with different TL20-line lengths do not produce satisfactory results.

With the output matching network designed in section 3.3 as a starting point, the optimizer is used in the simulation setup shown in Figure 3.12 to reach the goals listed in Table 3.1.[2]

The circuit inside the "main_match_output" block in Figure 3.12 is shown in Figure 3.13.

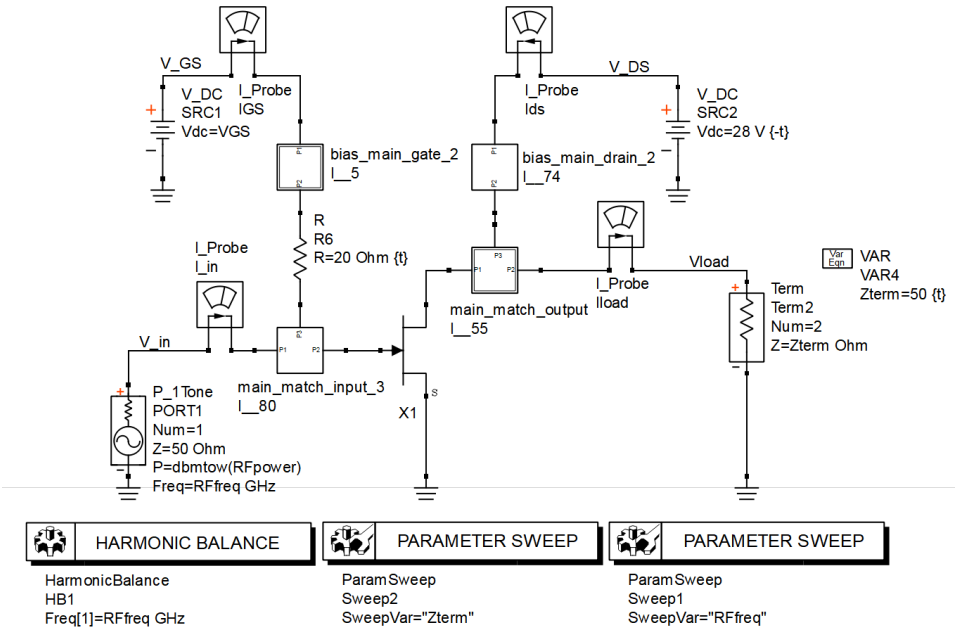


Figure 3.12: Simulation setup to Synthesize output network.

The simulation is done using a single frequency power source at the input of the input matching network, which generates two different power levels, the first at 23 dBm, and the second at 29 dBm, roughly corresponding to 6 dB OPBO and 0 dB OPBO respectively. At P_{in} = 23 dBm, R_L (Term2 in Figure 3.12) is set to 25 Ω, and the optimizer adjusts the parameters of the components in the output network to achieve an output power, P_{load}, between 34 and 35 dBm and an efficiency, η, above 70 % over a bandwidth of 800 MHz. At P_{in} = 29 dBm, R_L is set to 50 Ω, and the optimizer tries to achieve an output power between 40 and 41 dBm, at the same efficiency as for the first case, over the same bandwidth.

[2] In this simulation/optimization it is assumed that a linear increase in input power leads to a linear increase in output power, which of course is not the case when approaching saturation.

Table 3.1: Optimization goals set to achieve impedance matching, parasitic compensation and impedance inversion.

Parameter	Goal	Limits
P_{load}	$\in [40, 41]\, dBm$	$P_{in} = 29$, $R_{load} = 50$, $f \in [3.0, 3.8]\, GHz$
η	$> 70\,\%$	$P_{in} = 29$, $R_{load} = 50$, $f \in [3.0, 3.8]\, GHz$
$\lvert\Gamma_L\rvert$	$\in [0.17, 0.19]$	$P_{in} = 29$, $R_{load} = 50$, $f \in [3.0, 3.8]\, GHz$
$\angle\Gamma_L$	$\in [170, 190]\,^\circ$	$P_{in} = 29$, $R_{load} = 50$, $f \in [3.0, 3.8]\, GHz$
P_{load}	$\in [34, 35]\, dBm$	$P_{in} = 23$, $R_{load} = 25$, $f \in [3.0, 3.8]\, GHz$
η	$> 70\,\%$	$P_{in} = 23$, $R_{load} = 25$, $f \in [3.0, 3.8]\, GHz$
$\lvert\Gamma_L\rvert$	$\in [0.17, 0.19]$	$P_{in} = 23$, $R_{load} = 25$, $f \in [3.0, 3.8]\, GHz$
$\angle\Gamma_L$	$\in [-10, 10]\,^\circ$	$P_{in} = 23$, $R_{load} = 25$, $f \in [3.0, 3.8]\, GHz$

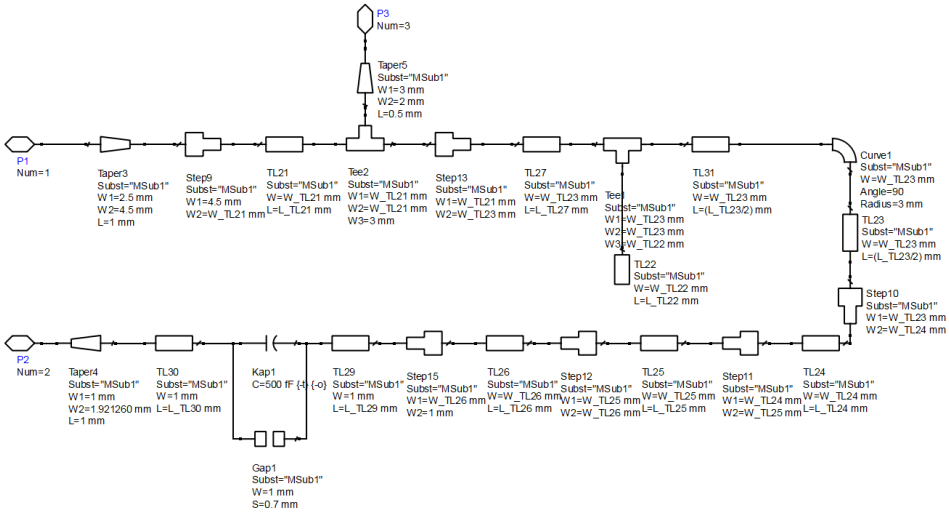


Figure 3.13

To, in a sense, "tell" the optimizer how to achieve these goals, additional goals for the load reflection coefficient, Γ_L are defined: the optimizer is told to try to achieve the goals regarding output power and efficiency when the two different power levels and corresponding loads, $25\,\Omega$ and $50\ \Omega$, are matched to $2{\cdot}R_{opt}$ and R_{opt}, respectively, effectively forcing it to also make the output network impedance inverting.

The optimization is an iterative process where the optimizer alternates between optimizing the components in the output network and the components in the input network.

In Figure 3.14, Γ_L is shown when R_L is swept between $25\,\Omega$ and $50\,\Omega$ after the optimization is complete. This clearly shows the impedance inverting properties of the output network.

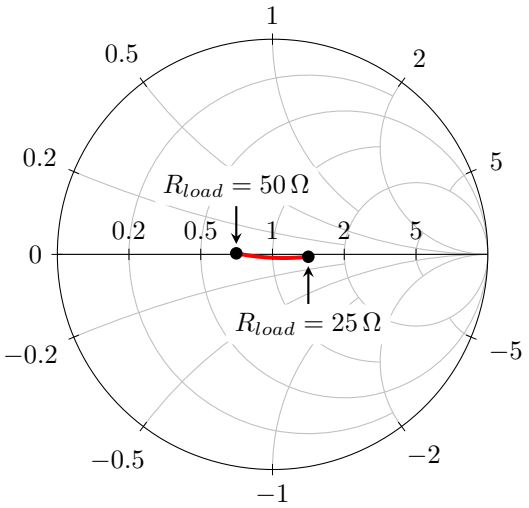


Figure 3.14

3.7 Auxiliary Amplifier Output Network

The auxiliary amplifier output network is, just as the main amplifier output network, designed using the initial output matching network described in section 3.3 as a starting point. The differences are that the transistor is now biased at $V_{GS} = -6\,V$, and the goals regarding Γ_L are changed so that the optimizer is no longer forced to make the network impedance inverting (which would reinstate the need for a quarterwave transformer).

Since the impedance seen by the auxiliary device will change from open circuit at 6 dB OPBO to R_{opt} at 0 dB OPBO, the new goals for Γ_L are set so that at 0 dB OPBO, the network should provide a wide-band match to $50\,\Omega$, by absorbing the parasitic reactance and transforming the $50\,\Omega$ to R_{opt}, i.e., $35\,\Omega$, just as with the main amplifier. At 3 dB OPBO, the goals for Γ_L are set so that the optimizer tries to match a relatively high impedance, i.e., between R_{opt} and a few kΩ – effectively open circuit relative to R_{opt} – to the $50\,\Omega$ load. After several iterations, it is found that around $200\,\Omega$ produces the best result.

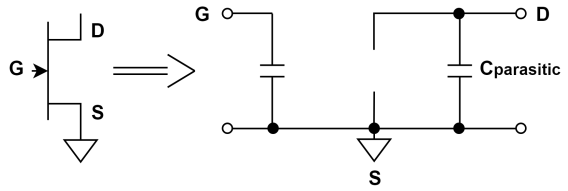


Figure 3.15: Simplified small-signal model of the transistor when it is not conducting.

A third goal is needed for the auxiliary amplifier optimization: consider the simplified

small-signal model of the transistor when it is not conducting, shown in Figure 3.15. Because of the parasitic reactance between the drain and source (ground) of the transistor (in the figure simplified to just $C_{parasitic}$), the output impedance of the transistor when it is not conducting will not appear as an open circuit, but rather as a capacitor connected to ground. For this reason, at 6 dB OPBO, goals are set to ensure that Γ_L is a real value, i.e., not reactive.

The auxiliary amplifier output network is shown in Figure 3.16, where P1 is connected to the drain of the transistor, the load is connected to P2, and the bias voltage is connected to P3.

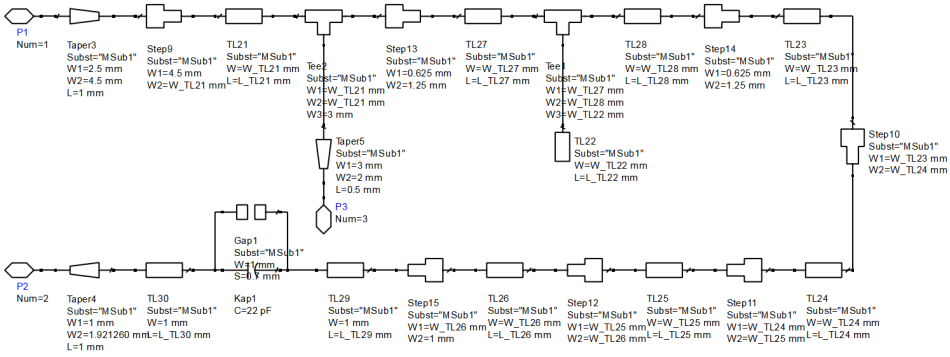


Figure 3.16: Auxiliary amplifier output network.

3.8 Connecting it All Together

Figure 3.17 shows how the outputs of the main and auxiliary amplifiers are connected. The drain of the main device is connected to P1, and the drain of the auxiliary device to P2. The drain bias voltages are connected to P4 and P5. The characteristic impedance of TL36 and TL37 is $2 \cdot R_{opt} = 70\,\Omega$, and their lenghts are adjusted manually to the values which result in the best amplifier performance.

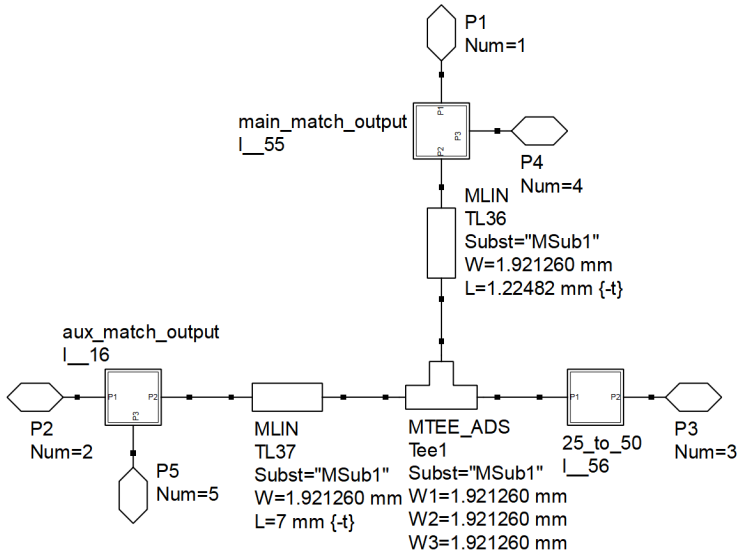


Figure 3.17: Connection of the amplifier outputs.

The amplifier is designed to drive a $25\,\Omega$ load at 6 dB OPBO, which must be matched to $50\,\Omega$. In Figure 3.1, this impedance transformation is done by a quarterwave transformer with a characteristic impedance of $35\,\Omega$. In the final design, a multisection transformer, like the one described in section 3.3, is used. This is shown in Figure 3.18.

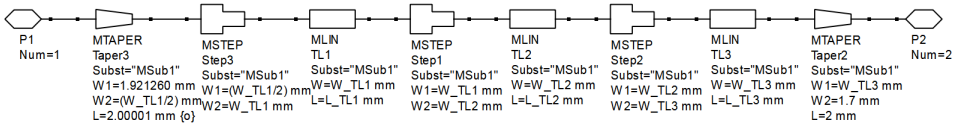


Figure 3.18: Output multisection transformer.

The layout of the finished Doherty power amplifier prototype is shown in Figure 3.19, where

1. Main amplifier input network
2. Main amplifier output network
3. Main device gate bias network
4. Main device drain bias network
5. Aux. amplifier input network
6. Aux. amplifier output network
7. Aux. device gate bias network
8. Aux. device drain bias network
9. Output matching transformer

In Figure 3.20, a picture of the finished, assembled prototype is shown.

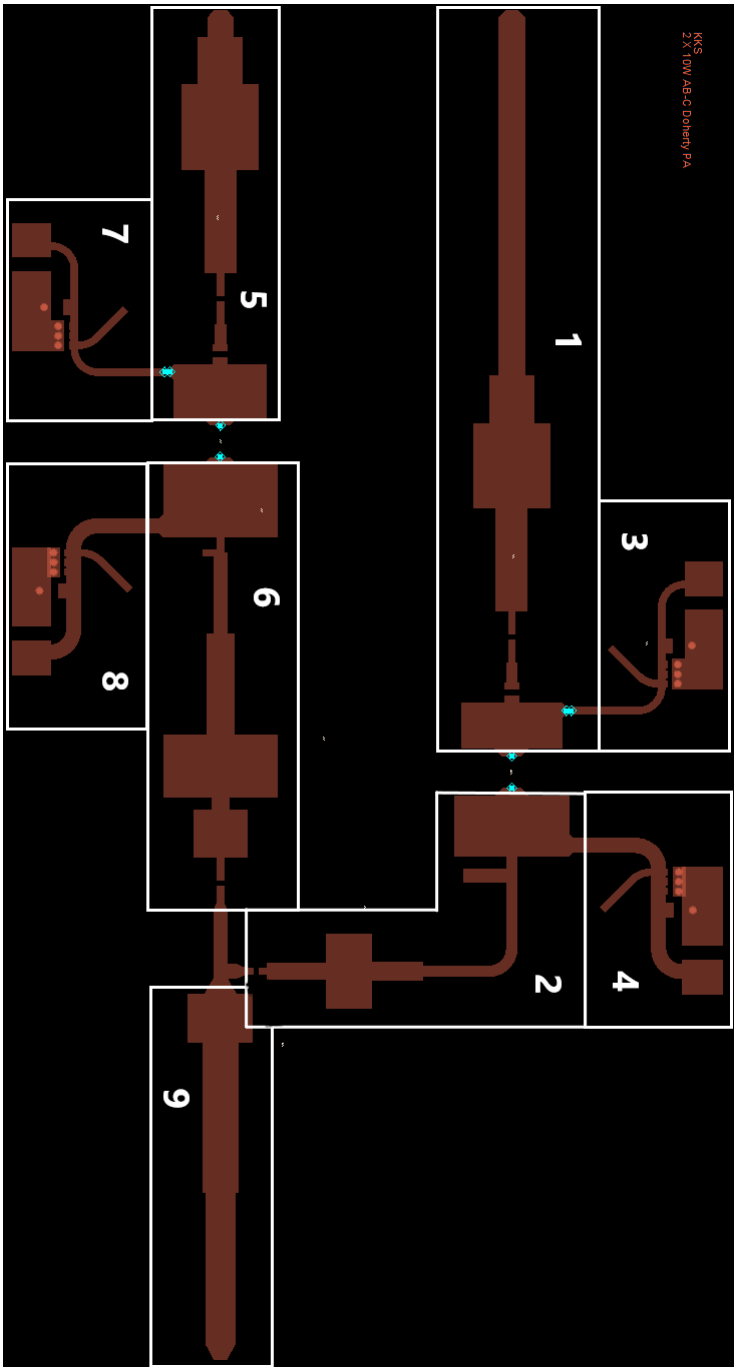


Figure 3.19: DPA prototype layout.

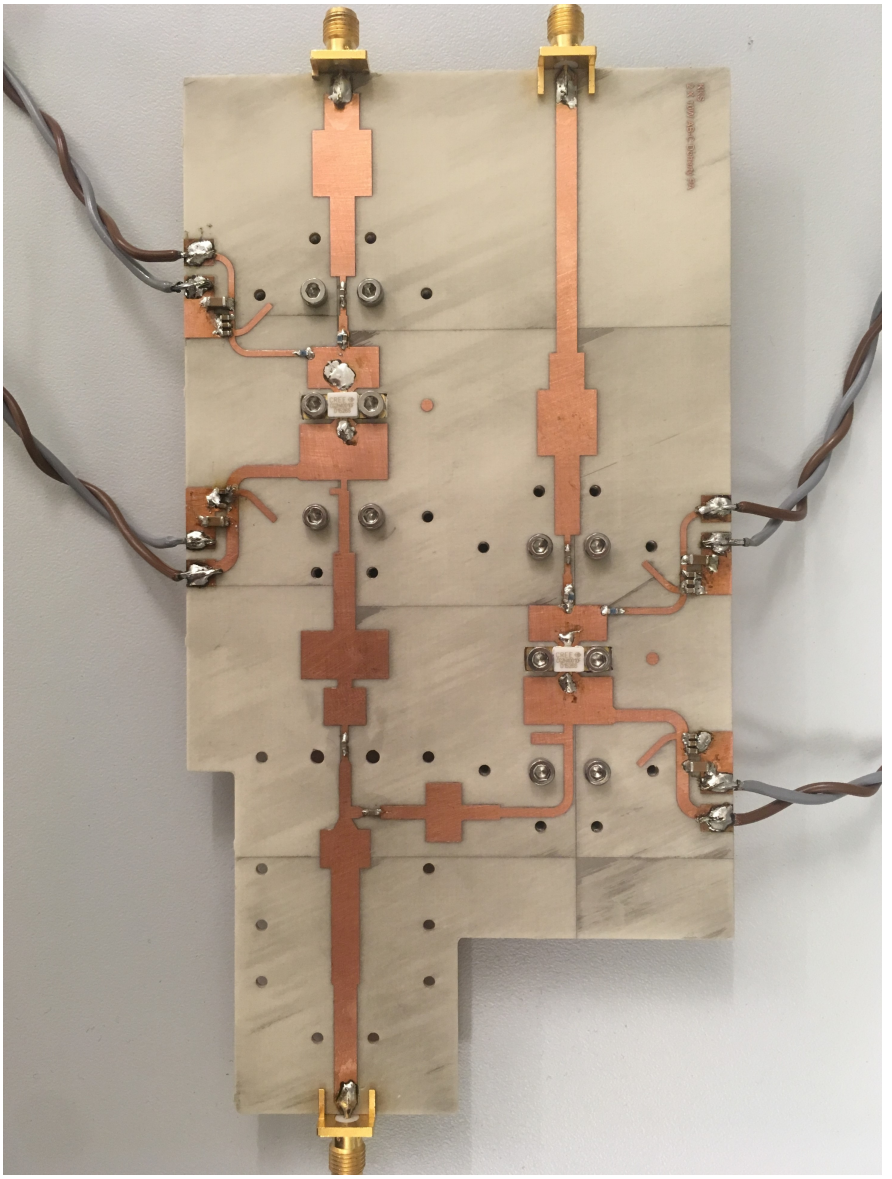


Figure 3.20: Assembled DPA prototype.

Chapter 4

Automated Measurement Setup

The characterization of the DPA prototype is done using a fully automated measurement setup employing two signal generators, three driver amplifiers, a spectrum analyzer, a power meter with accompanying power sensor and a total of eleven DC power supplies. All of the test and measurement instruments are controlled by a desktop computer running a MATLAB script which communicates with the instruments using Standard Commands for Programmable Instruments (SCPI). The setup is described in detail in the sections to follow.

4.1 General Measurement Considerations

All measurements are done using equipment available in the microwave research and development laboratory at the Department of electronic systems, imposing both degrees of freedom and restrictions on how the measurements must be made.

As described in section 3.2, the prototype DPA, utilizes a Cree/Wolfspeed CG2H40010 10 W RF Power GaN HEMT both as main and auxiliary device, biased in class AB and class C respectively. The prototype has one input for each amplifier so that the optimum phase delay in the auxiliary amplifier input path can be determined experimentally (for each specific input power level). This means that two separate signals, one for the main amplifier input and one for the auxiliary amplifier input, are needed. Two Rohde & Shwarz SGS100A SGMA RF Sources [19, (datasheet)] are used to generate these signals.

4.2 Phase Coherence and Phase Control

To be able to reliably control the relative phase between the two signals, it must be made sure that the signals are phase coherent; phase coherence meaning that they maintain a fixed phase relationship between them over time (fixed, although controllable/settable). In the back panel of each of the two signal generators there is a reference/local oscillator (LO) input connector and a reference/LO output connector. The SGS100A can be configured to accept an external LO or reference signal, and also to output its LO signal, or a 10 MHz or 1 GHz reference signal.

Phase coherence can be achieved in two different ways. The first alternative is having the two generators share a common reference signal, and the second is having them share a common LO signal. With a common reference signal, the long term phase stability will be poor due to several factors mentioned in the Rohde & Shwarz application note "GP108_1E" [21], with non-time-correlated phase noise and "weak" coupling being the main factors. A consequence of weak coupling is that a small phase drift in the reference signal leads to a large phase drift in the RF signal. The lower the reference frequency (compared to the RF frequency), the weaker the coupling. The second alternative, using a common LO, eliminates these problems, but when the LO is shared, there is no way of changing the relative phase between the two signals, so for the purpose of determining the optimum auxiliary path phase delay by sweeping the relative phase between the two DPA input signals, LO coupling is not a valid alternative. Despite the disadvantages mentioned above, reference coupling must be used to achieve both phase coherence and phase control. To minimize weak coupling issues, 1 GHz reference coupling is used (as opposed to 100 MHz).

To be able to directly identify which relative phase shift results in optimum operating conditions for the DPA, the two input signals must first be aligned in phase, i.e., be exactly on top of each other with respect to time, in order for the exact relative phase difference to be used during post-processing of the results. Moreover, initial experiments with the two generators reveal that at some given output power levels, the relative phase between their outputs does a seemingly random jump. This further calls for a phase alignment procedure.

4.2.1 Measuring the Relative Phase Between Two Signals

There are three common methods to measure the relative phase between two signals: by use of a vector network analyzer (VNA), a spectrum analyzer or an oscilloscope. In the lab, all three instruments are available, but the frequency of the signals to be measured (3 to 3.8 GHz) eliminates using the available oscilloscope (2.5 GHz, 20 GSa/s). In terms of phase measurement accuracy, the most precise instrument of the two remaining alternatives is the VNA. However, the needed configuration of the VNA along with its physical placement in the lab, makes using the spectrum analyzer the best alternative. Besides, the spectrum analyzer's accuracy is more than sufficient for the application.

A spectrum analyzer of course can only do scalar measurements, but can be used for relative phase measurements in the following way: the sum of two sinusoids of equal frequency, S_1 and S_2, can be expressed as

$$S_1 + S_2 = Asin(\omega t) + Bsin(\omega t + \varphi)$$

$$= f(\varphi) \cdot sin\left(\omega t + tan^{-1}\left[\frac{Bsin(\varphi)}{Bcos(\varphi) + A}\right]\right)$$

where

$$f(\varphi) = \sqrt{A^2 + B^2 + 2AB\,cos(\varphi)} = |S_1 + S_2| \tag{4.1}$$

The magnitude of the sum of the two sinusoids, $f(\varphi)$, is a function of the relative phase between them, φ, and will be at a maximum when $\varphi = 0$, and at a minimum when $\varphi = 180\,°$, due to total constructive and total destructive interference respectively. By exploiting this, scalar power magnitude measurements of the sum of the two signals coming from the two signal generators, made by a spectrum analyzer, can be used to determine the relative phase between them.

The way in which this is done in practice is shown in Figure 4.1: the two generators' output signals, S_1 and S_2, are summed in a power combiner, and the magnitude of this sum is measured by the spectrum analyzer.

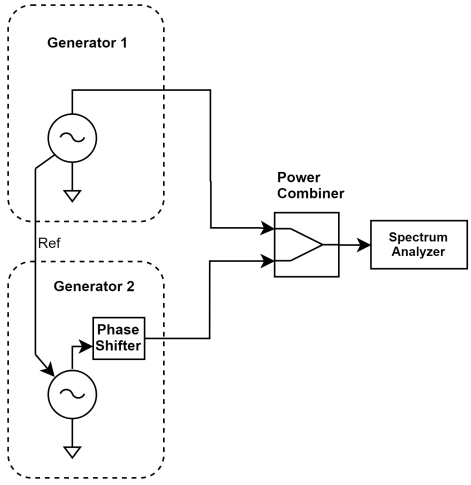


Figure 4.1: Phase Measurement.

When the generators are turned on, their output signals are phase coherent, but not aligned (generator 2 starts off with an arbitrary phase shift relative to generator 1). Using the SGS100A's built-in phase shifter in steps of 1 °, and measuring the power at the output of the combiner for each phase step, the plot shown in Figure 4.2 is produced. In the figure, the measured power levels have been mapped to the φ-axis by defining the minimum measured power level as the power level resulting from a phase shift of 180 °.

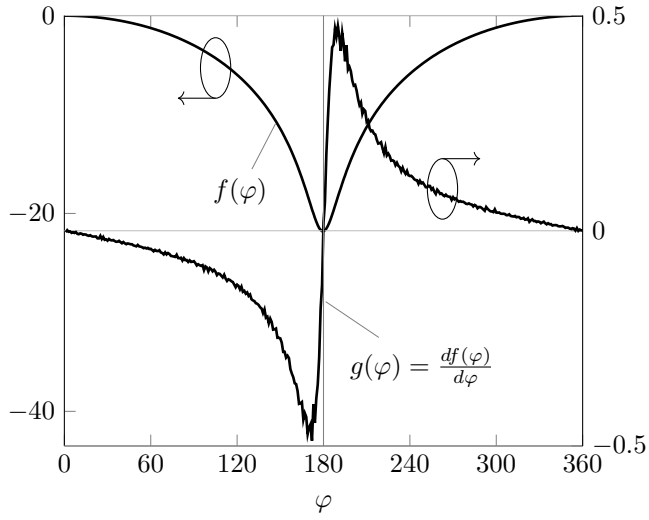


Figure 4.2: Measured magnitude of the sum of the two generators' output signals, $f(\varphi)$, along with its derivative, $g(\varphi)$, (in dBm, normalized) vs. relative phase.

4.2.2 Phase Alignment

The ability to control the relative phase between the two generators' output signals along with the ability to accurately measure it, allows for the two signals to be aligned in phase. In section 4.2 it is mentioned that the relative phase does a seemingly random jump when the generators' output power level is changed. This means that every time the output power level changes, the two signals must be realigned.

A very efficient way to do this would be to first measure the magnitude of the sum of the two signals for an initial output power level, say 0 dBm, and map them to specific phase shifts, exactly like in Figure 4.2, and then store these values in a look-up table. As an example, say the phase would need realigning at an output power level of 5 dBm: a measurement of the magnitude of the sum of the signals is made, and the value is compared to the values stored in the look-up table + 5 dB above the initial 0 dBm power level used to make the table. The value in the table, corresponding to a specific phase shift, closest to the measured value can then be used to determine the current phase shift. However, since $f(\varphi)$ is symmetric there are two equal values corresponding to two different phase shifts. Let us say the values in the table closest to the measured value corresponds to $\varphi = 150\,^\circ$ and $\varphi = 210\,^\circ$. The phase would then need a shift of either $-150\,^\circ$ ($150\,^\circ - 150\,^\circ = 0$) or $+150\,^\circ$ ($210\,^\circ + 150\,^\circ = 360\,^\circ$). Two new measurements are made, one at $\varphi = \varphi - 150\,^\circ$, and a second at $\varphi = \varphi + 150\,^\circ$. Whichever phase shift produces a measured value closest to the stored value which corresponds to a phase shift of 0 is the phase shift used to align the two signals.

However, although time-efficient, the method described above would be rather application-specific, and the accuracy of it would be suboptimal. A more general-purpose, more ac-

curate phase alignment algorithm is developed, and it works as shown by the flowchart in Figure 4.3. It is based on taking the derivative of the magnitude of the sum of the two signals, $g(\varphi)$, also shown in Figure 4.2. Obtaining the exact version of $g(\varphi)$ shown in Figure 4.2 would require that $f(\varphi)$ is known, meaning that a lot of time would have to be spent doing all the required measurements to obtain $f(\varphi)$. Because of this, a "low-resolution" version of $g(\varphi)$ is obtained as

$$g'(\varphi) = \frac{\Delta P}{\Delta \varphi} = \frac{P(\varphi + \varphi_{step}) - P(\varphi)}{\varphi_{step}} \tag{4.2}$$

where φ_{step} is initially set to 40 °. φ is then changed in steps of the initial 40 °, and $g'(\varphi)$ is calculated for each step until the sign of $g'(\varphi)$ changes. A change in the sign of $g'(\varphi)$ means that the axis of symmetry ($\varphi = 180\,°$) has been crossed. φ is then shifted the other way (back towards $\varphi = 180\,°$) in steps half that of the initial step size until the sign of $g'(\varphi)$ changes once again. This process is repeated until the step size is 0.1 °(which is the phase resolution of the internal phase shifter in the SGS100A), in theory meaning that $\varphi = 180\,°$ is found with an accuracy of $\pm 0.1\,°$. φ is then shifted by 180 °, aligning the two signals.

An initial phase step size of 40 ° divided by 2 enough times will of course not produce a final step size of 0.1 °. The division by 2 is just used for ease of explanation. The actual step sizes used are 40 °, -20 °, 10 °, -5 °, 2 °, -1 °, 0.5 °, -0.2 ° and 0.1 °.

The reason the algorithm is not written in such a way so that it finds $\varphi = 0$ directly, lies in the plot of $g(\varphi)$. Since the rate of change in $f(\varphi)$ is at its highest at $\varphi = 180\,°$, using $g(\varphi)$ to find $\varphi = 180\,°$ is a lot more reliable than using it to find $\varphi = 0$, especially when taking noise into consideration (notice the fuzziness of the plot of $g(\varphi)$).

The flowchart in Figure 4.3 shows that the two signals start off with an arbitrary relative phase shift $\varphi < 180\,°$. Before the algorithm is run, it is made sure that $\varphi < 180\,°$ by measuring the change in power over a change in φ of 1 °, and then shifting φ by 180 ° if the change in power is positive. This is to make sure that the algorithm always has the same starting conditions, so that the first φ_{step} can always be positive. Of course, if the initial φ is close to 0 or 360 °, the change in power over 1 ° would be very small, which could challenge the algorithm's ability to determine whether or not the current φ is above or below 180 °, but with several tests only providing successfull results, this is not considered to be of concern.

Figure 4.4 shows an example of how the algorithm functions: the initial φ is 135 °. φ is then changed in steps of 40 ° until the slope of the tangent between two power measurements changes, which happens after two steps (shown in green). Then φ is changed in steps of -20 ° until the slope changes once again, which happens after three steps (shown in blue). This process of halving and changing the sign of the step size continues until it converges towards $\varphi = 180\,°$. Steps up to and including -5 ° are shown in the figure.

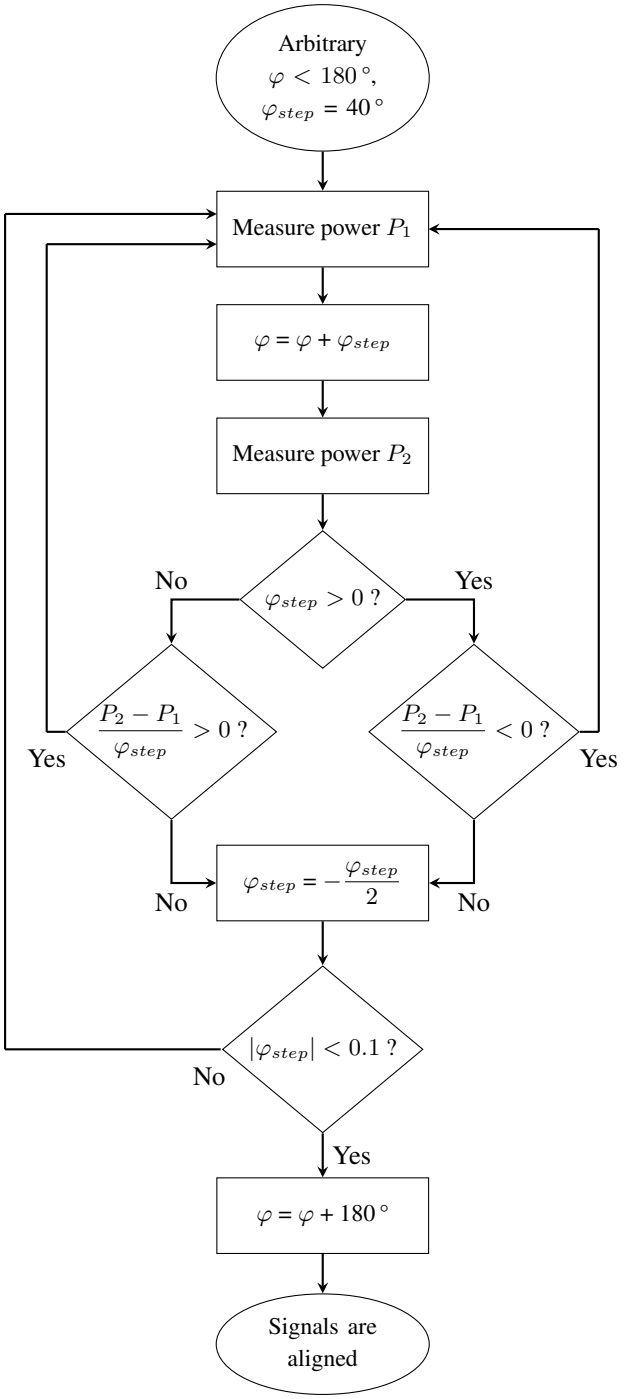


Figure 4.3: Phase determination algorithm.

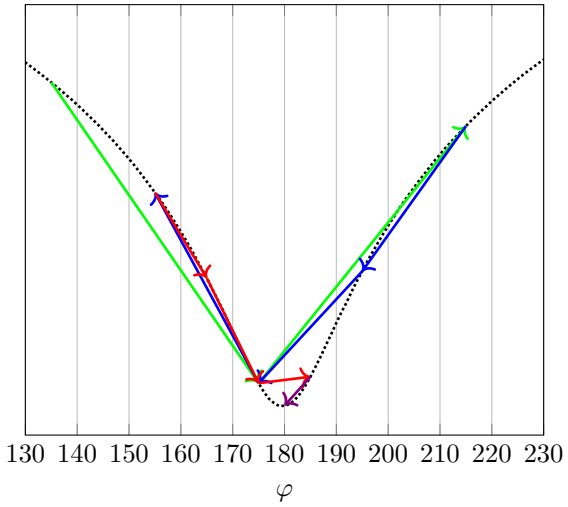


Figure 4.4: Phase alignment example.

The accuracy of the phase alignment algorithm is tested by using the algorithm to first find $\varphi = 180\,°$, then doing a phase sweep from $170\,°$ to $190\,°$. This is done 20 times with 20 different initial phase shifts, and the result is shown in Figure 4.5. The figure shows that the worst misses made by the algorithm are approximately $\pm 1\,°$.

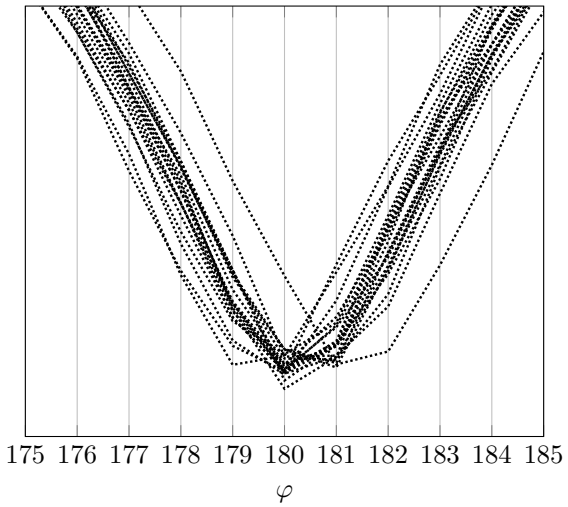


Figure 4.5: Phase alignment algorithm accuracy.

4.3 Preamplification and Isolation

The maximum output power of the two signal generators is, according to their datasheet, around 20 dBm. The simulations of the DPA show that the power levels required to drive it well into compression is well above 30 dBm, meaning that the two signals coming from the two generators must be amplified by more than 10 dB before being fed to the DPA in order to properly characterize it.

Moreover, one of the two generators displays an issue: when its output power level is set to anything above 5 dBm, its actual measured power level is around 30 dB lower than the set level, effectively limiting the upper limit of its power level range to 5 dBm. This means that in order to raise its power level to the same level as that of the other generator, an additional gain of at least 15 dB is needed in the path containing the faulty generator.

The driver amplifiers of course have their own characteristics which must be compensated for when performing the measurements of the DPA. For these characteristics to be accurately compensated for, they must be predictable, and for them to be predictable, the output of the driver amplifiers must be isolated from the inputs of the DPA, since any reflected signal from the DPA inputs, due to poor matching, may alter the driving conditions for the driver amplifiers.

This is done with RF circulators, shown in Figure 4.6. A circulator works in such a way so that it allows signal transmission from port 1 to port 2, from port 2 to port 3, and from port 3 to port 1. It does not, however, allow transmission from port 1 to port 3, from port 3 to port 2, or from port 2 to port 1. This non-reciprocal characteristic means it can be used to isolate the driver amplifier output connected to port 1 from any reflected signal from the DPA input connected on port 2. The reflected power will be dissipated in a $50\,\Omega$ termination resistor connected on port 3.

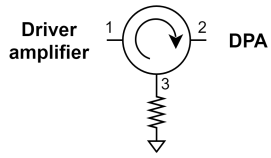


Figure 4.6: RF circulator.

The driver amplifiers and circulators are connected as shown in Figure 4.7.[1] Driver 1 is a two-stage, 0.5 - 5.0 GHz, 25 W amplifier designed by Associate Professor Morten Olavsbråten, which provides around 15 dB of gain. Driver 2 is a Mini Circuits ZHL-42 [14, (datasheet)], and Driver 3 is a 0.5 - 5.1 GHz 10 W amplifier, also designed by Associate Professor Morten Olavsbråten. Drivers 2 and 3 provide a combined gain of around 45 dB.

The figure also shows two attenuators connected between port 3 on the circulators and the $50\,\Omega$ terminations. This is just a precautionary measure in case a lot of power is reflected and needs to be dissipated in the $50\,\Omega$ terminations. Additionally, two directional

[1] In Figure 4.7, the circulators are designated as "isolators"; this is an error. An isolator functions in the same way as a circulator, but port 3 is terminated internally, making it a two-port device.

couplers, one in each path, used to couple a fraction of each of the two signals into a power combiner, is shown. This is used for the phase alignment described in section 4.2.2. The two 30 dB attenuators between the directional couplers and the power combiner is also just a precautionary measure to prevent damage to the power combiner, since a resistive power splitter is used as the combiner, and no maximum "reverse" power rating seems to exist in any documentation for this component.

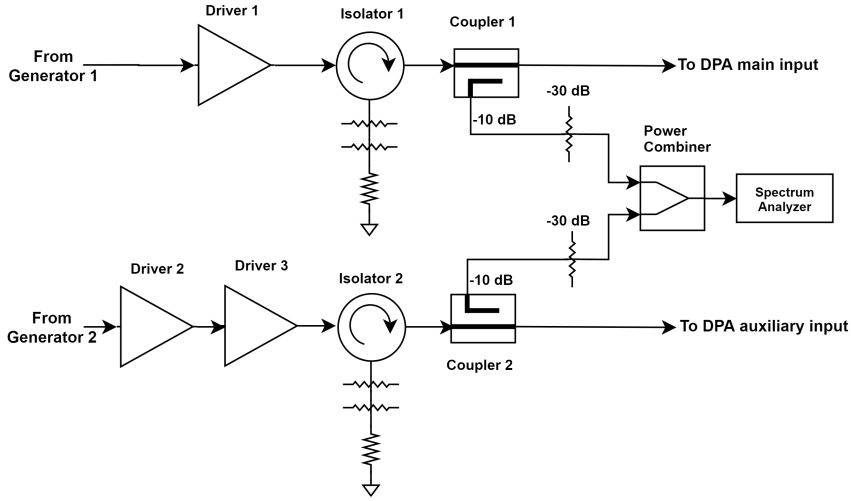


Figure 4.7: Driver amplifiers, circulators and phase measurements.

4.3.1 Linearization and Gain Correction

Driver 1 in Figure 4.7 has a P_{out}-P_{in} characteristic which is slightly nonlinear around 17 dBm. Moreover, both driver sections start compressing at output powers above 30 dBm, while the drive power needed to fully characterize the DPA is a few dB above 30 dBm.

The driver sections, Driver 1, and the combination of Driver 2 and 3, are linearized up to an output power of 34 dBm in the following way: the output power of Generator 1, P_{gen}, is adjusted until the power measured at the output of Coupler 1, $P_{out,\,driver} = P_{gen} + G_{driver}$, is 0 dBm. P_{gen} is then sweeped linearly from the power level resulting in $P_{out,\,driver} = 0$ dBm up to $P_{gen} = 34$ dBm, in steps of 1 dBm, and a power measurement at the output of Coupler 1 is made for each step. The difference between the linear increase in P_{gen} and the measured values is then used to linearize the gain of Driver 1. The section consisting of Driver 2 and 3 is linearized in the same way, using Generator 2 and measuring output power at Coupler 2.

When measuring the output power of the DPA vs. input power, the input power reference plane should be at the DPA's input connectors. This is easily achieved by compensating for the gain in the driver amplifiers and the losses in cables, circulators and couplers. Figure 4.8 shows the results of the linearization and compensation.

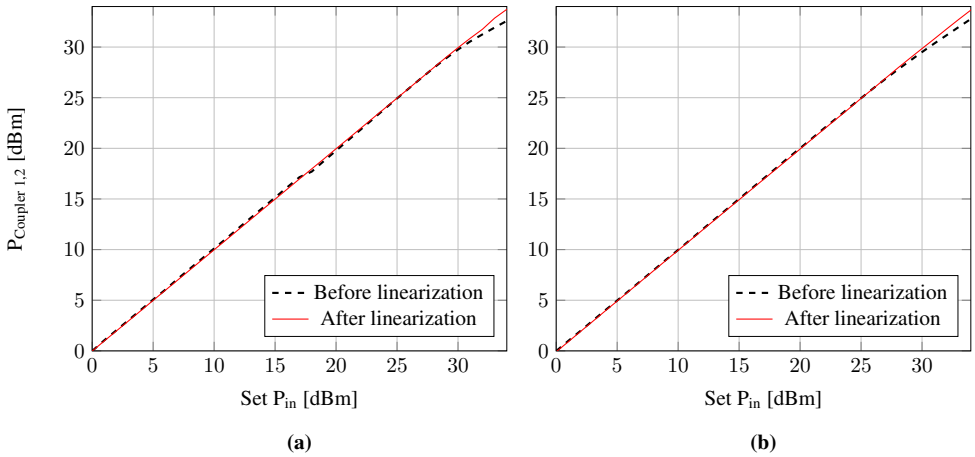


Figure 4.8: Power measured at output of (a) Coupler 1, (b) Coupler 2, vs. set P_{in}.

4.4 Transistor Biasing

The needed gate bias voltage set to achieve the wanted drain bias current in the CG2H40010 HEMT will often be different from what is found with simulations of the ADS model. In fact, the needed gate bias voltage will vary by a considerable amount from device to device. For the main device biased in class AB, this is not an issue. Since it is biased above threshold there will be a quiescent current flowing, and the gate bias voltage can be set to whichever value corresponds to the quiescent current resulting in the wanted class AB bias condition.

For the class C biased device however, finding the gate bias voltage corresponding to the same class C bias condition used in the simulations is not as straightforward. Since the device is biased below threshold, no quiescent current will flow. Because of this, to determine optimum DPA operating conditions, all measurements are done at several different auxiliary device gate bias voltages. Additionally, the measurement results are used to determine dynamic gate biasing functions in Chapter 5.

4.5 Output Power Measurements

Relatively high power levels are to be measured by a power meter when measuring the output power of the DPA. The power probe connected to the power meter is rated for power levels up to 20 dBm, and the expected DPA output power levels are as high as 43 dBm. To reduce this to a maximum of 20 dBm at the input of the power probe, a 13 dB directional coupler is used and a 20 dB attenuator is connected between the coupled port and the power probe, as shown in Figure 4.9. A 20 W 50 Ω termination connected via a relatively lossy cable to the output of the directional coupler dissipates the remaining

power. The lossy cable is included because the measurements are to be made around the maximum power rating of the termination.

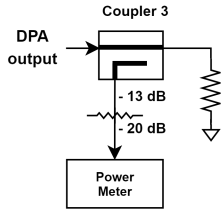


Figure 4.9: Measurement setup output network.

4.6 Complete Measurement Setup

The final measurement setup is the combination of everything described in this chapter, and is shown in Figure 4.11.[2] All instruments and equipment used in the setup is listed in Table 4.1.

In the final setup, a slight modification must be made to the phase alignment algorithm: the outputs of Couplers 2 and 3 are connected to the inputs of the DPA via cables that do not necessarily have the same phase responses, meaning that the last 180 ° phase shift done by the last process block in Figure 4.3 is not necessarily the phase shift which results in a phase shift of 0 at the inputs of the DPA. To correct for this, an initial phase alignment is done, with the original 180 ° phase shift. Then, a ± 20 ° sweep in steps of 1 ° is done, and a measurement of the combined power coming out of the two cables connected to the coupler outputs is made for each step, as shown in Figure 4.10. The initial 180 ° shift can then be adjusted to the value which shifts the minimum measured power level at the output of the second power combiner to 180 °.

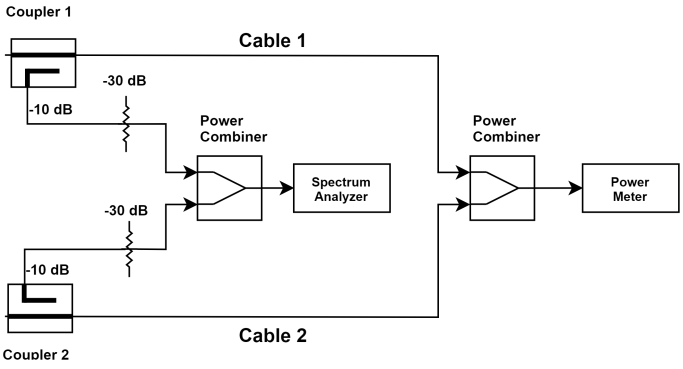


Figure 4.10: Setup for correcting the different phase response of different cables.

[2]The DC power supplies used to power the driver amplifiers are not shown in the figure.

To fully characterize the DPA, output power and main and auxiliary amplifier DC current consumption must be measured as functions of input power, relative phase between input signals and auxiliary amplifier gate bias voltage. To achieve this, all of the variables are swept in discrete steps, and power and current measurements are done for each step.

4.6.1 The MATLAB script

As mentioned in the introduction to this chapter, the DPA prototype characterization is done in a fully automated measurement setup using a MATLAB script communicating with the instruments via SCPI. The MATLAB script functions in the following way:

1. Establish connection with the instruments.
2. Initialize instruments (generator output frequency, spectrum analyzer center frequency, PSU current limiting etc.).
3. Turn on generators.
4. Set input power level, P_{in}.
5. Do phase alignment.
6. Set auxiliary device gate bias voltage, $V_{GS,aux}$.
7. Set relative phase between input signals, φ.
8. Measure output power, gate and drain DC current draw of both main and auxiliary amplifiers.

The sweep variables are all set using nested for-loops, where the first (outer) loop sets P_{in}, the second loop sets $V_{GS,aux}$, and the third and innermost loop sets φ. The innermost loop also contains the measurement functions which measure output power and DC current draw.

P_{in} is set in the outer loop since φ must be realigned for each new input power level, and having this done in the outer loop makes it so that the alignment algorithm is only run once for each power level, which saves time. $V_{GS,aux}$ is set in the second loop so that the settling time of the power supply when a new output voltage is set will not affect the measurements. The innermost loop sets a new φ every 250^{th} millisecond to allow for the power probe to settle between each measurement.

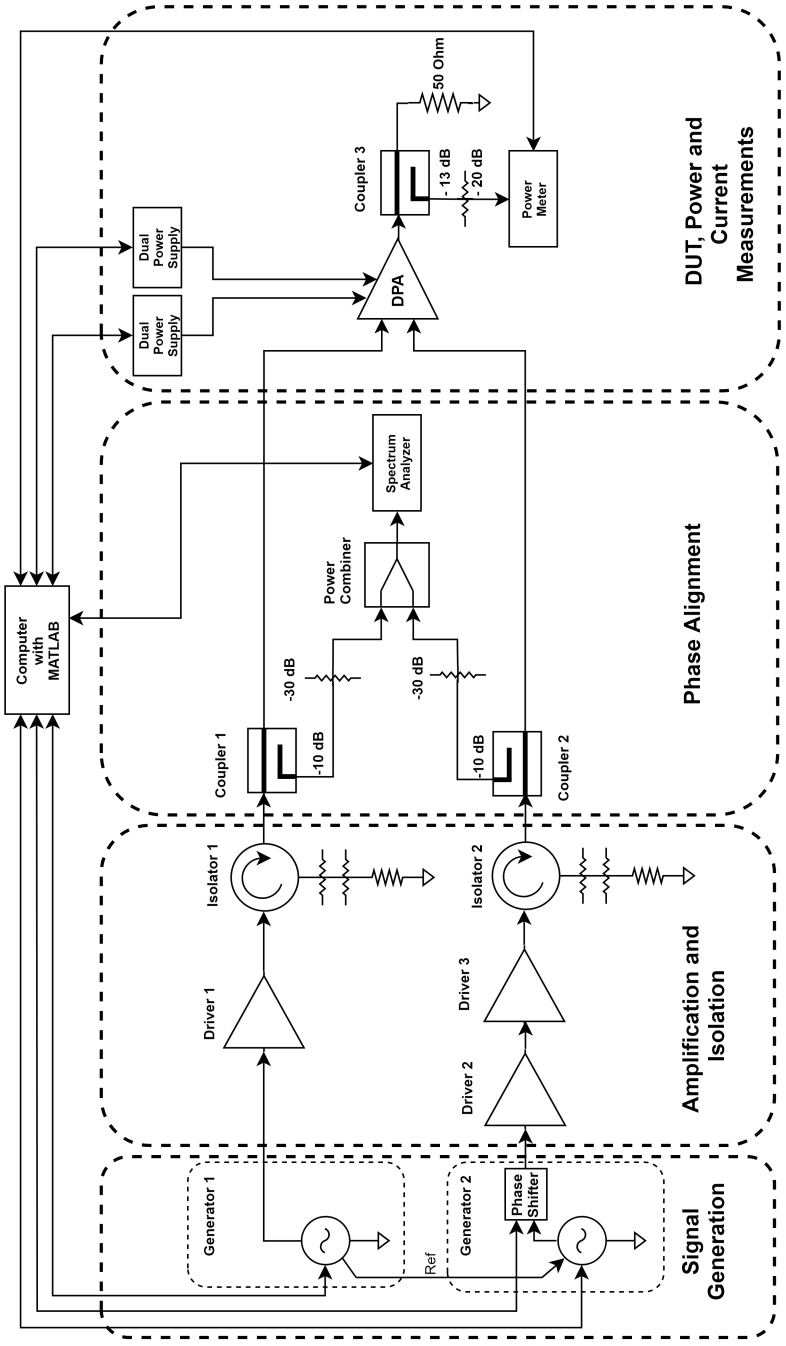


Figure 4.11: Complete Measurement setup.

Table 4.1: List of components used in the measurement setup.

Component	Manufacturer	Model
Generator 1	Rohde & Shwarz	SGS100A
Generator 2	Rohde & Shwarz	SGS100A
Driver 1	N/A	N/A
Driver 2	Mini-Circuits	ZHL-42
Driver 3	N/A	N/A
Circulator 1	Microwave Communications Laboratories, Inc.	CS-144-35
Circulator 2	Microwave Communications Laboratories, Inc.	CS-144-35
Coupler 1	Advanced Technical Materials, Inc.	C124H-10/RL
Coupler 2	Advanced Technical Materials, Inc.	C124H-10/RL
Power Combiner	Anritsu	K240C
Spectrum Analyzer	Rohde & Shwarz	FSQ40
Dual Power Supply	Aim-TTi	CPX200DP
Dual Power Supply	Aim-TTi	CPX200DP
Coupler 3	Narda	5292
Power Meter	Anritsu	ML2438A
Power Sensor	Anritsu	MA2474D

Chapter 5

Results

In this chapter, measurement results are presented and compared to simulation results. First, small-signal results are presented, which give good indications of the large-signal performance of the amplifier. Second, large-signal results obtained by measuring the performance of the DPA prototype using the setup described in Chapter 4 are presented.

All mentions of "gain" refers to transducer power gain, G_T [15], and all mentions of "efficiency" refers to drain efficiency, η, described in section 2.6.

5.1 Small-Signal Results

Measuring the S-parameters of the amplifier is done using a Rohde & Shwarz ZNB8 vector network analyzer (VNA) [20, (specifications)]. Since the VNA only has two ports, the two amplifiers comprising the complete DPA prototype is measured one at a time. Furthermore, the S-parameters of the auxiliary amplifier biased in class C can not be measured at the correct bias, since small-signal excitation will not be enough to drive the device. Because of this, the auxiliary device is set up with the same class AB bias as the main device when the measurements are performed.

The input and output impedance of an active device will vary with bias, so the auxiliary amplifier S-parameter results will not necessarily accurately represent the performance of this amplifier, but it is useful to compare the measured results with results obtained with simulations performed with the same class AB bias.

When the main amplifier measurements are performed, the auxiliary amplifier is biased at V_{GS} = -10 V to make sure the auxiliary device is properly turned off, and a $50\,\Omega$ termination is connected to its input. The same applies to the main amplifier when the auxiliary amplifier measurements are performed.

A 20 dB attenuator is connected between the DPA output and the VNA as a precautionary

measure to prevent that the full output power of the amplifier ends up at the VNA port connected to the DPA, should the DPA be unstable and oscillate. This causes the S_{22} measurements to be slightly non-accurate due to noise, since such small signal levels are measured.

5.1.1 Main Amplifier

The main amplifier S-parameter measurement results are shown together with the simulated results in Figure 5.1.

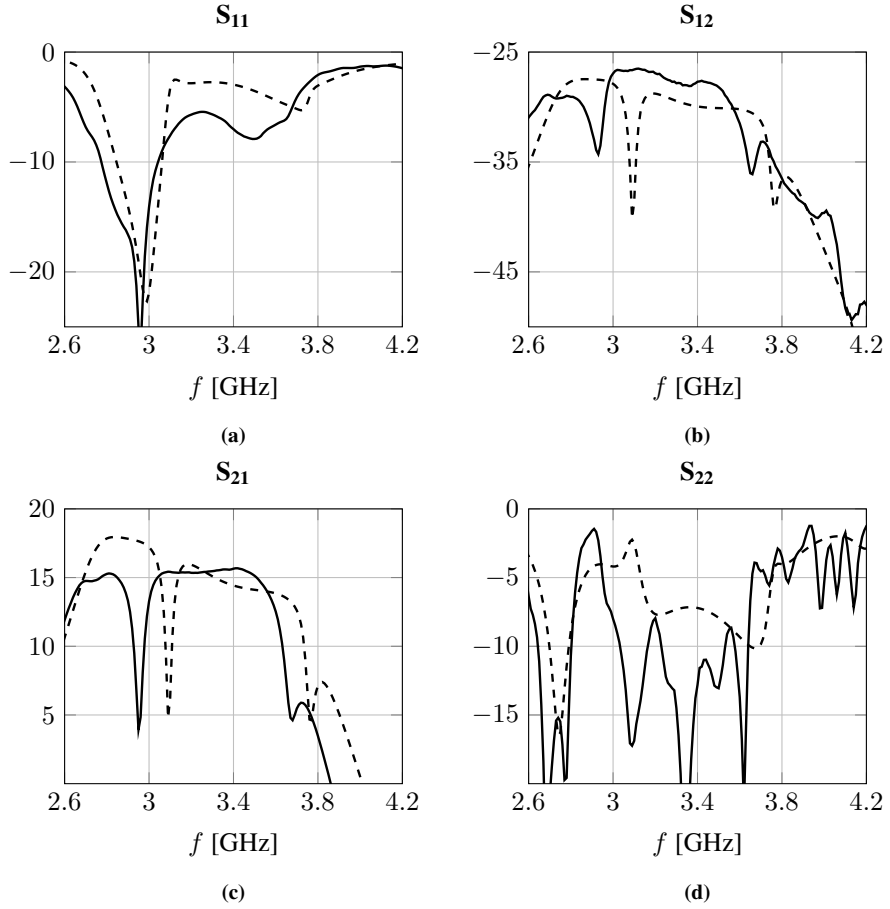


Figure 5.1: Measured (solid) and simulated (dashed) S-parameters of the main amplifier: (a) S_{11}, (b) S_{12}, (c) S_{21} and (d) S_{22} [dB].

The results displayed in the figure above show that the measurements are generally similar to the simulations, but a shift in center frequency can be observed. The plots of S_{11} and S_{22} show that the amplifier is better matched to $50\,\Omega$ than in the simulations. The plot of S_{21}

shows that the small-signal gain is around 15.5 dB, and the measured frequency response is flatter than in the simulations in the band of interest (when ignoring the center frequency shift).

5.1.2 Auxiliary Amplifier

Figure 5.2 shows the measured and simulated S-parameters of the auxiliary amplifier.

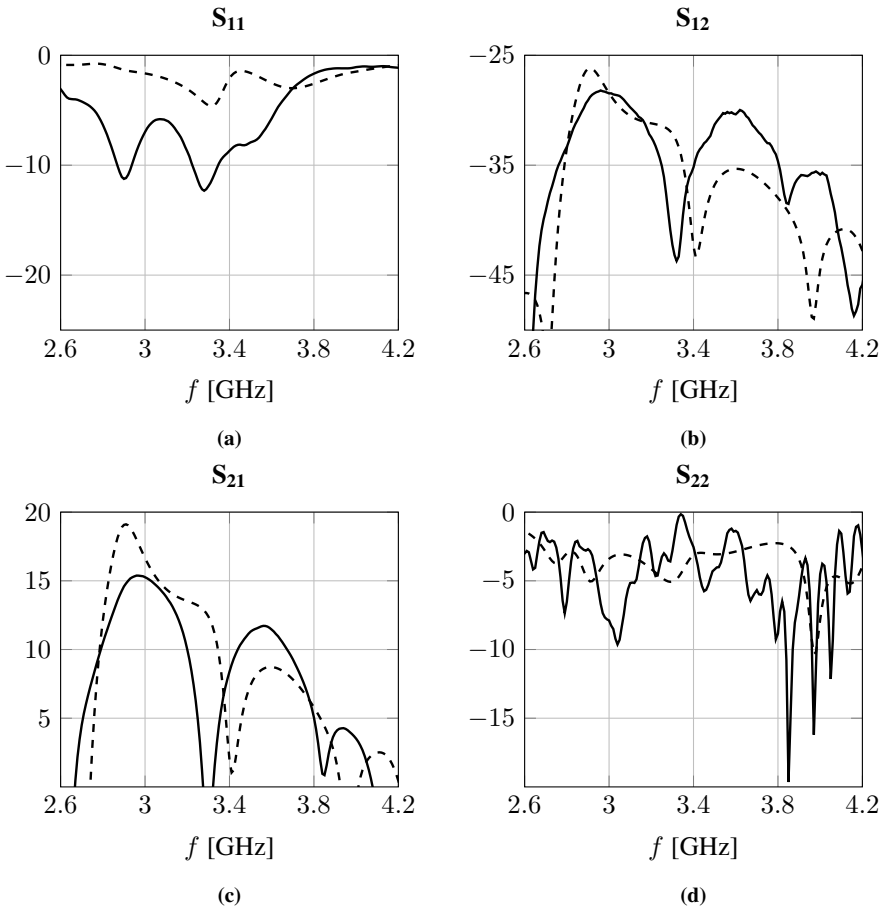


Figure 5.2: Measured (solid) and simulated (dashed) S-parameters of the auxiliary amplifier: (a) S_{11}, (b) S_{12}, (c) S_{21} and (d) S_{22} [dB].

The results display the same center frequency shift as with the main amplifier. In general, on the basis of these results, the performance of the auxiliary amplifier is not optimal. This is, however, partly due to the class AB bias needed to perform the measurements, and its performance at the correct class C bias is likely slightly better. The fact that the measured results are similar to the simulations further indicates this.

5.2 Large-Signal Results

The following results are obtained using the setup described in Chapter 4.

5.2.1 Fixed φ and V_{GS}

As described in Chapter 4, all large-signal measurements are performed with different auxiliary device gate bias voltages, V_{GS}, and relative phases between the input signals, φ. The design procedure presented in Chapter 3 however, is done aiming for the best performance using fixed V_{GS} and φ.

The following is a comparison of simulated and measured results with fixed V_{GS} and φ. The performance theoretically obtainable with dynamic V_{GS} and φ is presented in section 5.2.3.

Optimal Theoretical Performance

In terms of producing the most Doherty-like efficiency curve, the optimal configuration of the amplifier with fixed V_{GS} and φ is with $V_{GS} = -6\,V$, and $\varphi = 160\,°$. Furthermore, this is achieved when $P_{in,main}/P_{in,aux}$ = 1.5, i.e., with 50 % more power given to the input of the main amplifier than given to the input of the auxiliary amplifier.

However, due to time constraints, no measurements at different relative input power levels are performed, so the simulation results with $P_{in,main}/P_{in,aux}$ = 1.5 can not be compared to measurements. Nonetheless, the simulation results are presented in Figures 5.3 and 5.4 to show what the design is theoretically capable of.

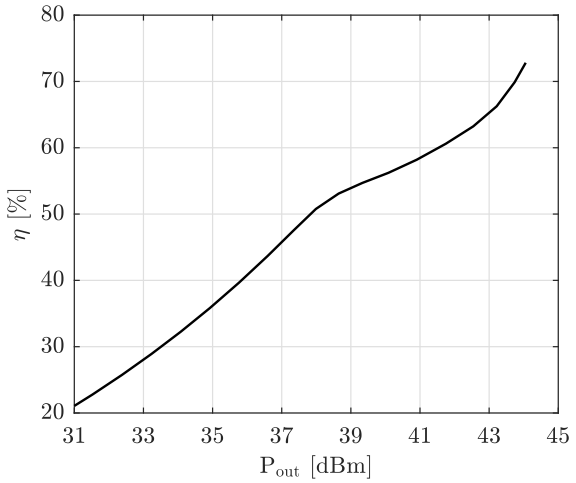


Figure 5.3: Simulated η vs. P_{out} ($V_{GS} = -6\,V$, $\varphi = 160\,°$, $P_{in,main}/P_{in,aux}$ = 1.5).

Figure 5.3 shows that, according to simulations when configured as described above, the drain efficiency is above 51 % at 6 dB OPBO (P_{out} = 38 dBm), and just short of 73 % at 0 dB OPBO (P_{out} = 44 dBm).

Figure 5.4 however, shows that at 6 dB OPBO the amplifier is already 3 dB deep into compression, and at 0 dB OPBO, the gain compression is over 5 dB. This is due to the power relationship between the two inputs. The gain characteristics of Doherty power amplifiers typically show an increase from the point where the auxiliary amplifier turns on, up to 0 dB OPBO. Since more power is given to the main amplifier than to the auxiliary amplifier, and the auxiliary device being identical to the main device but biased in class C, this is not the case for the designed prototype with this V_{GS} and φ configuration.

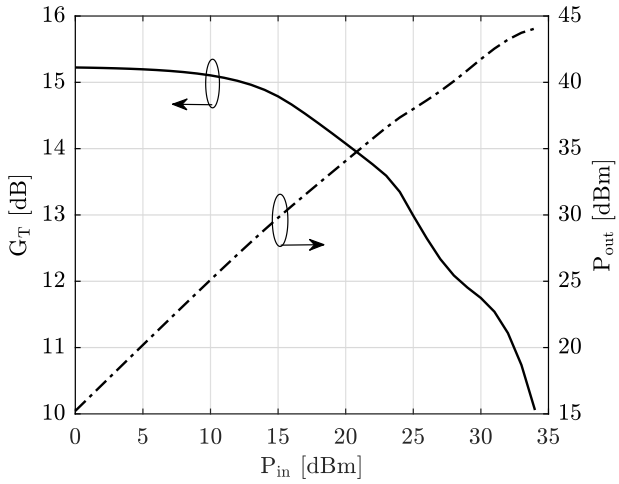


Figure 5.4: Simulated G_T (solid) and P_{out} (dashed) vs. P_{in} ($V_{GS} = -6\,V$, $\varphi = 160\,°$, $P_{in,main}/P_{in,aux}$ = 1.5).

Comparison of Simulations and Measurements ($P_{in,main}/P_{in,aux}$ = 1)

Simulated and measured results with the fixed V_{GS} and φ producing the most Doherty-like efficiency curve is shown in the following figures. The V_{GS} and φ set in the simulation is -6 V and 160 °, respectively, and the V_{GS} and φ set when performing the measurements is -6.5 V and 165 °, respectively.

Output Power

Figure 5.5 shows output power, P_{out} vs. input power, P_{in}.

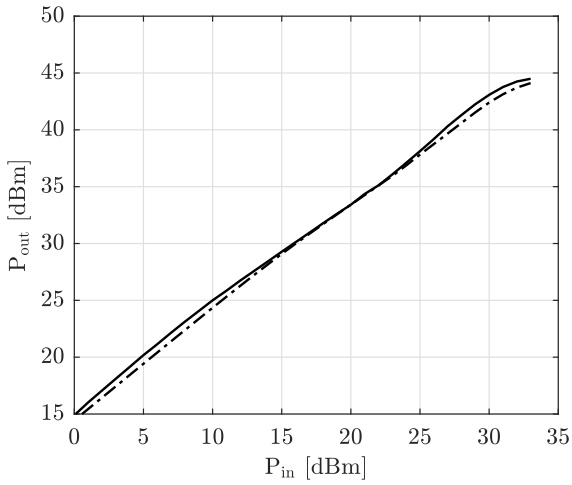


Figure 5.5: Simulated (dashed) and measured (solid) P_{out} vs. P_{in}.

It can be seen that the maximum measured P_{out} is 44.5 dBm. 0 dB OPBO is therefore defined as P_{out} = 44 dBm, which means that 6 dB OPBO is defined as P_{out} = 38 dBm.

Efficiency

The efficiency of the DPA prototype is shown in Figure 5.6.

The figure shows that the Doherty region starts at P_o = 35 dBm, instead of the intended 6 dB OPBO point (P_o = 38 dBm). This means that the main device is not allowed to go deep enough into compression before the auxiliary device turns on, which causes the efficiency to be around 10 % lower than in the simulations at output power levels above 35 dBm. The measured efficiency can be seen to be 33 % at the start of the Doherty region (9 dB OPBO), and 60 % at 0 dB OPBO.

Gain

The gain of the amplifier can be seen in Figure 5.7, which shows a peak at P_{out} = 20 dBm, before the main amplifier approaches saturation.

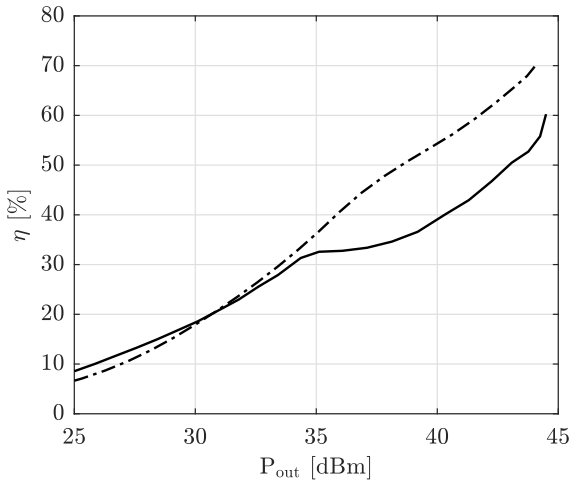


Figure 5.6: Simulated (dashed) and measured (solid) η vs. P_{out}.

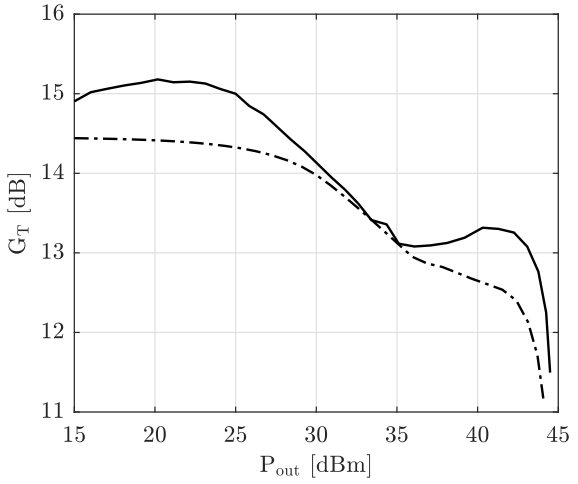


Figure 5.7: Simulated (dashed) and measured (solid) G_T vs. P_{out}.

The measured gain resembles a more typical Doherty gain curve than the simulated one, where it can be seen that there is a slight increase in gain after the auxiliary device turn-on point.

Bandwidth

Figure 5.9 shows measured and simulated gain vs. frequency.

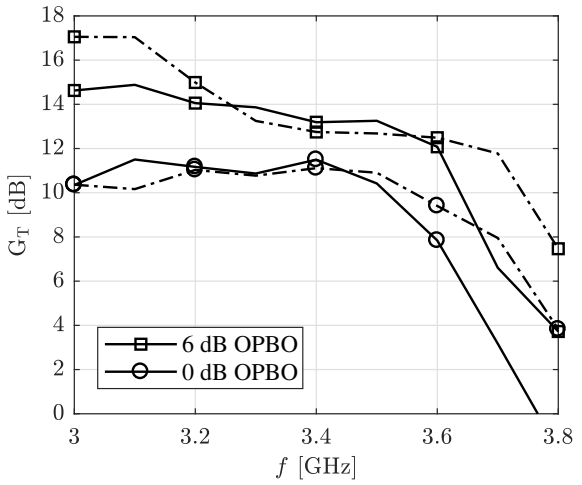


Figure 5.8: Simulated (dashed) and measured (solid) G_T vs. f.

The measured results are very similar to the simulations, apart from the center frequency shift also seen in the small-signal results.

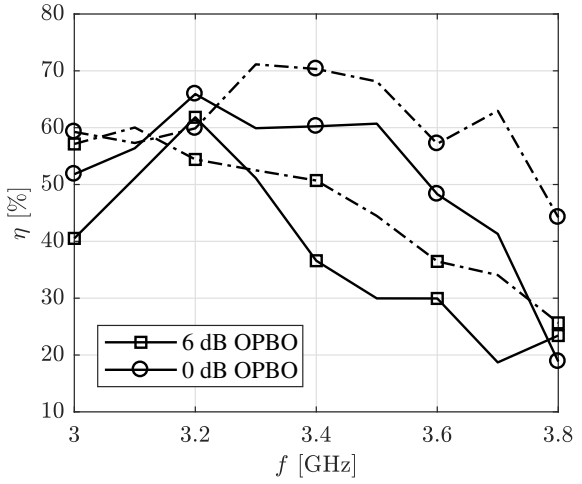


Figure 5.9: Simulated (dashed) and measured (solid) η vs. f.

The measured efficiency vs. frequency, shown in Figure 5.9, is also similar to the simulations, apart from the center frequency shift, as well as being around 10 % lower, which corresponds well with what is seen in Figure 5.6.

5.2.2 Dynamic φ, Fixed V_{GS}

The results presented in this section and in section 5.2.3 are obtained by post-processing large amounts of data obtained with the measurement setup described in Chapter 4. In the setup, V_{GS} is swept from -6.5 V to -3.5 V in steps of 0.1 V, and φ is swept from 120 ° to 200 ° in steps of 5 °.

If φ is allowed to change dynamically, the efficiency in the Doherty region can be improved. Figure 5.10 shows the maximum theoretically obtainable efficiency if φ is allowed to vary as a function of input power. This is superimposed onto plots of efficiency vs. input power for all values of φ. V_{GS} is kept fixed at -6.5 V.

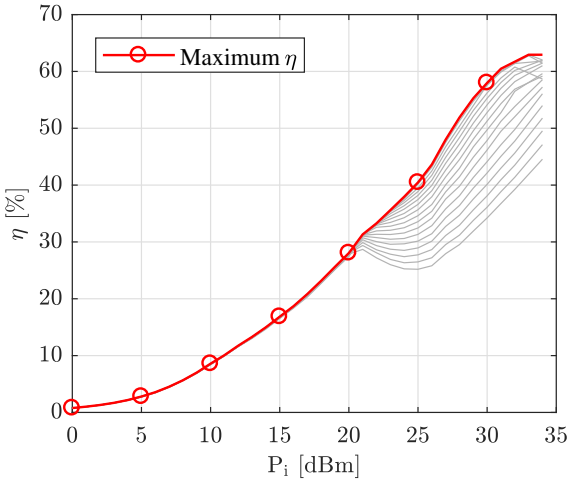


Figure 5.10: Maximum η vs. P_i, with dynamic φ.

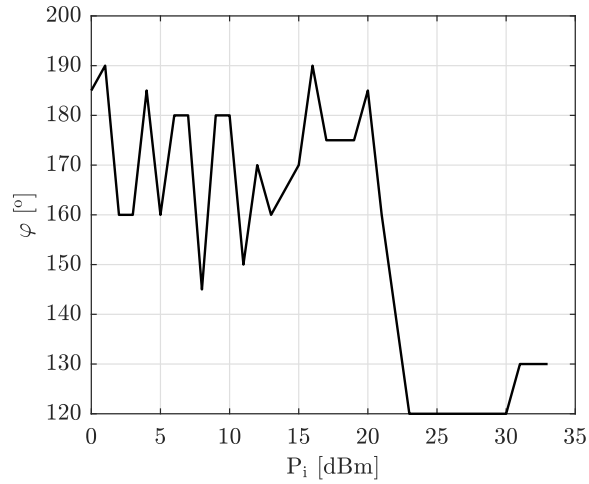


Figure 5.11: φ vs. P_i for maximum efficiency.

The needed variations in φ is shown in Figure 5.11, and efficiency vs. output power with φ following this function, is shown together with the efficiency with fixed φ in Figure 5.12. The figure shows that the efficiency with dynamic φ is between 6 and 8 % higher in the Doherty region than what it is with fixed φ.

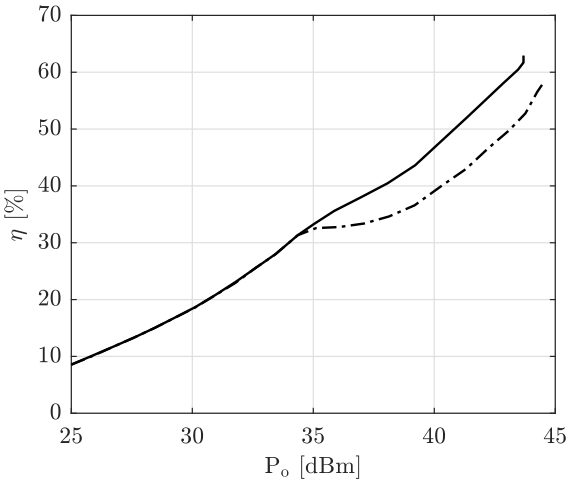


Figure 5.12: η vs. P_o with fixed (dashed) and dynamic (solid) φ.

The gain when using this φ-function, shown in Figure 5.13, stays the same as in the case with fixed φ in the low power region, but changes slightly in the Doherty and peak power

regions. It can be seen that the amplifier goes into compression a bit sooner than in the case with fixed φ.

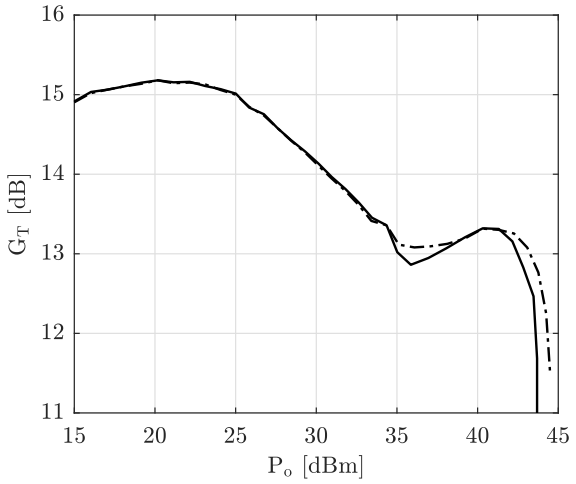


Figure 5.13: η vs. P_o with fixed (dashed) and dynamic (solid) φ.

5.2.3 Dynamic φ and V_{GS}

If V_{GS} is also allowed to vary dynamically, the gain curve can be improved in terms of flatness.

Figure 5.14 shows the maximum gain flatness theoretically achievable with varying φ and V_{GS}, just as described above for maximum efficiency, but here with a different dynamic phase function, and also with a dynamic bias function.

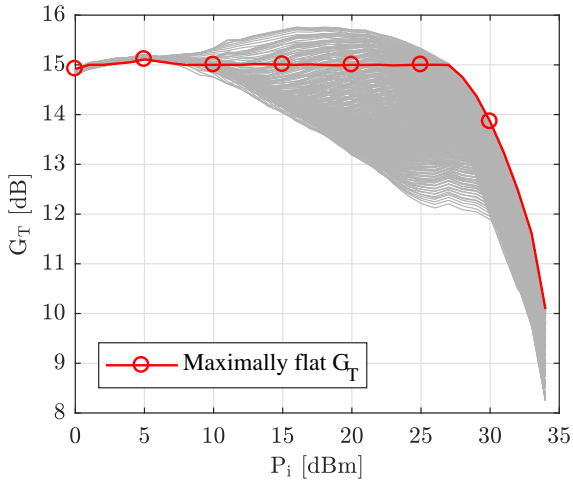


Figure 5.14: Maximally flat G_T vs. P_i, with dynamic φ and V_{GS}.

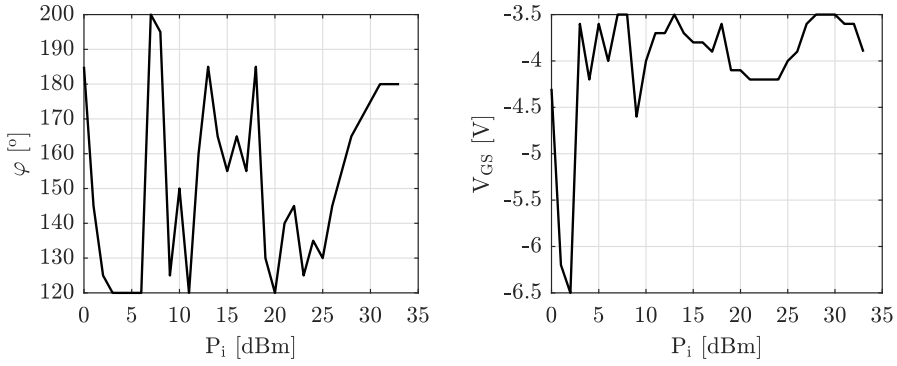


Figure 5.15: (a) φ and (b) V_{GS} vs. P_i for max. flat G_T.

The needed variations in φ and V_{GS} to achieve this, is shown in Figure 5.15. The gain and efficiency vs. output power with V_{GS} and φ following these functions, is shown in Figure 5.16.

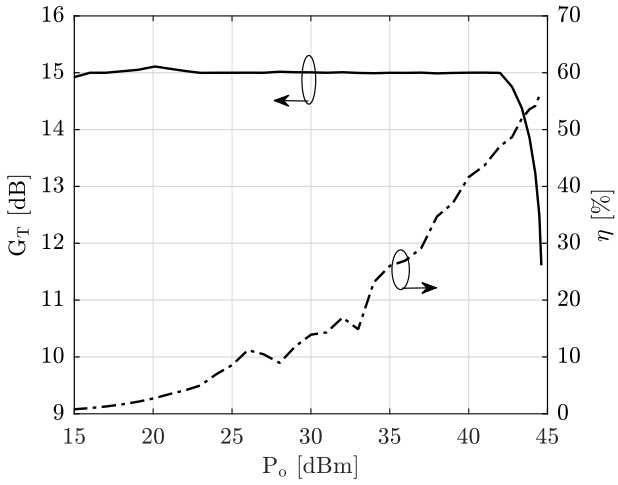
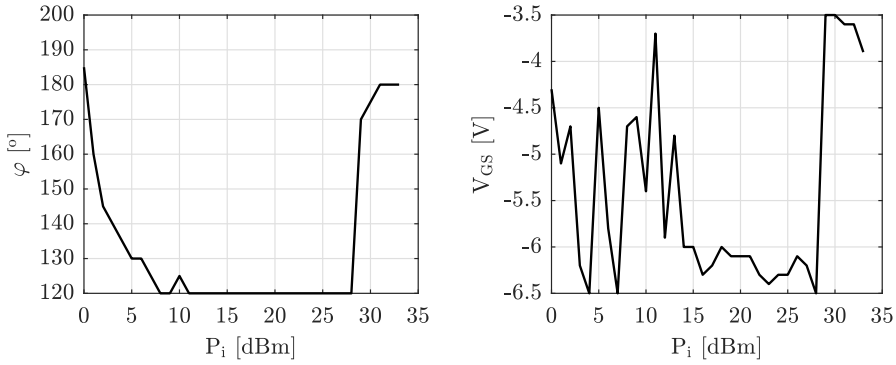


Figure 5.16: G_T (solid) and η (dashed) vs. P_{out}, with dynamic φ and V_{GS} for maximally flat G_T.

The figure shows that the gain curve is now almost entirely flat up to P_o = 42 dBm, where the amplifier starts going into compression. The efficiency is of course significantly lower when using these bias and phase functions. However, if gain variations of $\pm$ 0.5 dB is tolerated within the flat region, φ and V_{GS} can follow the functions shown in Figure 5.17, resulting in the efficiency shown in Figure 5.18.



(a) **(b)**

Figure 5.17: (a) φ and (b) V_{GS} vs. P_i for max. flat $G_T \pm 0.5$ dB.

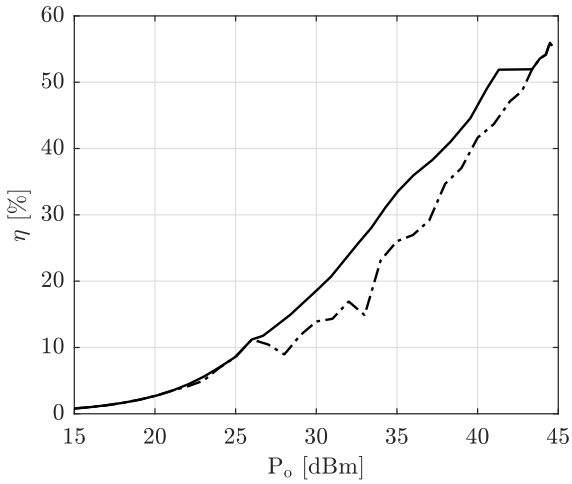


Figure 5.18: η vs. P_{out}, with dynamic φ and V_{GS} for maximally flat gain (dashed), and maximally flat gain $\pm$ 0.5 dB (solid).

The above figure shows that an efficiency-increase in the Doherty region of up to 10 % can be achived when $\pm$ 0.5 dB gain variation is allowed.

Chapter 6

Discussion

In this chapter, the results presented in Chapter 5 are discussed and interpreted, and the design methodology and measurement setup described in chapters 3 and 4 are discussed in light of these results.

6.1 Main Amplifier Performance

The main amplifier seem to function reasonably well on its own, based on the simulations and measurements (apart from the center frequency shift). The small-signal results show that the main amplifier has a fractional gain-bandwidth of around 16 %, and the large-signal results with fixed V_{GS} and φ indicate that the output network is impedance inverting.

6.2 Auxiliary Amplifier Performance

The auxiliary amplifier is more difficult to evaluate, since small-signal measurements at the correct class C bias can not be performed. However, large-signal simulation and measurement results indicate that the auxiliary amplifier's performance is suboptimal.

Figure 6.1 shows that the auxiliary amplifier DC drain current at 0 dB OPBO is around 700 mA at the center frequency, but only around 300 mA at 3.6 GHz, and 100 mA at 3.8 GHz. At 6 dB OPBO, where this current is supposed to be relatively low, it is around 60 mA at 3.4 GHz, but above 400 mA at 3.0 GHz. These results indicate that the output network is not doing a very good job of compensating the parasitic output reactance of the device.

Output and bias networks designed using a more systematic analysis of the parasitic output reactance of the device would probably benefit the performance of both the main and the

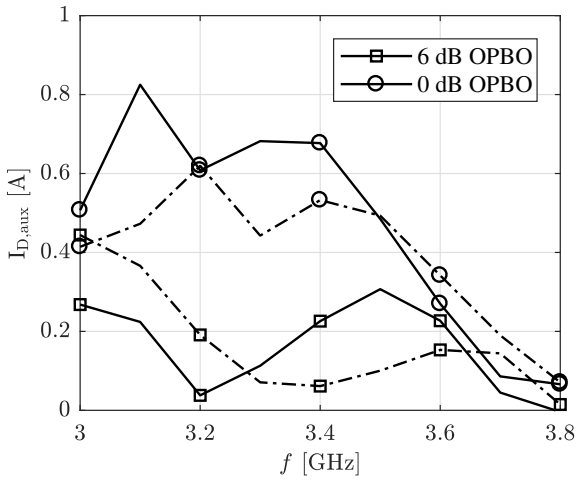


Figure 6.1: Measured (solid) and simulated (dashed) auxiliary amplifier DC drain current vs. frequency.

auxiliary amplifier, but especially the auxiliary, since it has to function over a larger range of load impedances (theoretically from open circuit to R_{opt}).

6.3 Doherty Amplifier Performance

6.3.1 Fixed φ and V_{GS}

The measured performance of the DPA protoype with fixed φ and V_{GS} is relatively similar to the simulations, apart from the gain being slightly higher, and the efficiency being considerably lower from the point where the auxiliary device turns on.

Figure 6.2a shows that the auxiliary device turn-on point is at around P_{out} = 35 dBm, meaning that the effective load seen by the main device starts changing sooner than it is supposed to. Consequently, the main amplifier does not reach saturation when it is supposed to, which causes the measured efficiency seen in Figure 5.6 to be rather low at output power levels above 35 dBm. The main amplifier DC drain current is shown in Figure 6.2b. The figure shows that it is slightly higher than in the simulations, but the measured output power is also slightly higher than in the simulations, so this does not affect the efficiency noteworthy.

The premature auxiliary device turn-on point indicates that the set V_{GS} (-6.5 V) is too high. Unfortunately this is the lowest V_{GS} used in the measurement setup. Had the measurements been performed with lower values of V_{GS}, the back-off efficiency would almost certainly be significantly better.

This of course also affects the efficiency-bandwidth, shown in Figure 5.9. At 0 dB OPBO,

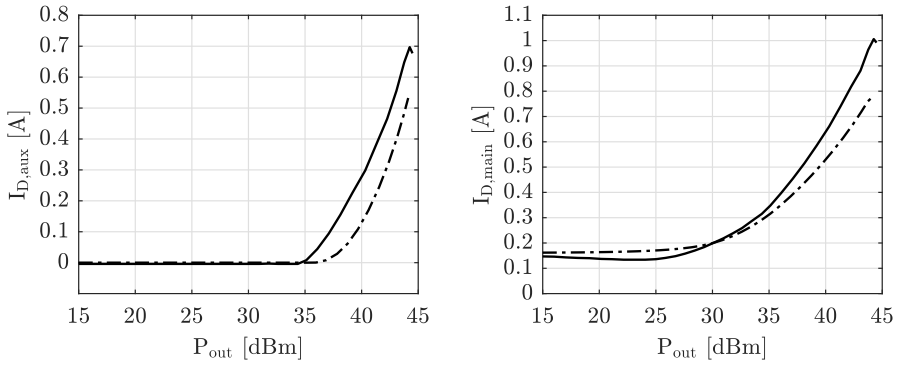


Figure 6.2: Simulated (dashed) and measured (solid) DC drain current vs. P_{out}. (a) Main amplifier, (b) auxiliary amplifier.

the measured efficiency-bandwidth is close to the simulated results, apart from the frequency shift and being around 10 % lower, because of the reasons mentioned above. At 6 dB OPBO, the measured result does not follow the same trend as the simulated result. This is because 6 dB OPBO does not correspond to the start of the Doherty region, but rather in the middle of the Doherty region. Unfortunately, no measurements with lower input power than 26 dBm (which corresponds to 6 dB OPBO) have been performed at frequencies other than 3.4 GHz, so the efficiency bandwidth at the OPBO-point corresponding to the start of the Doherty region is unknown.

6.3.2 Dynamic φ and V_{GS}

The theoretical performance with dynamic φ and V_{GS} is the highest performance possible to achieve with the DPA design in its current state. At least with the φ- and V_{GS}-ranges over which the measurements have been made. Again, better results would most likely be possible to obtain with lower V_{GS}.

The functions φ and V_{GS} would have to follow to achieve the presented results, however, are likely not entirely straightforward to implement in practice. Approximating them by higher order polynomials would most likely not produce satisfactory resluts, as the functions are rather "messy". The best solution would be to store their values in a power-indexed look-up table used by a digital signal processor (DSP).

6.4 Other Comments and Future Work

Stability

Something which is not discussed in Chapter 5 is the stability of the designed DPA prototype. This is because if for example the μ-factor is calculated using the measured S-parameters, the result would be a μ-factor < 1. The reason for this is the unreliable S_{22}-measurement which is noisy due to the 20 dB attenuator at the output of the amplifier needed when performing small-signal measurements. Small-signal simulations, however, show that the protoype is stable at all frequencies.

Linearity

A very important performance measure not discussed in this thesis is the linearity of power amplifiers. The focus in this thesis has been to explore the benefits of using an alternative approach to conventional Doherty PA design, not worrying about linearity concerns.

More thorough characterization

Since no measurements at lower input powers than 26 dBm have been performed at frequencies other than 3.4 GHz, the analysis of the efficiency-bandwidth is somewhat lacking. If more time had been spent on optimizing the automated measurement setup for time-efficiency, these measurements could have been made, and the needed data for a more thorough characterization of the DPA prototype could have been gathered.

Power measurements

All of the output power measurements are made by a power sensor and power meter. The bandwidth of the power sensor is from DC to 40 GHz, meaning that the power in any spurious tones resulting from nonlinearities are also measured. This introduces a small error in the output power measurements, meaning that the actual output power of the DPA prototype might be slightly lower than what has been measured. Because of this, the output signal should also have been analyzed with a spectrum analyzer.

Input power ratio

As well as being done with lower values of V_{GS}, the measurements should also had been done with different main amplifier / auxiliary amplifier input power ratios, $P_{in,main}/P_{in,aux}$. If this ratio had been allowed to be anything between 0 and 1, both devices could even have the same bias.

All of the subjects mentioned in this section are considered to be opportunities future work.

Chapter 7

Conclusion

This thesis has explored the benefits of using adaptive auxiliary amplifier input phase control and adaptive auxiliary device biasing to improve the performance of Doherty power amplifiers.

A dual-input DPA prototype utilizing two 10 W GaN HEMT's has been designed using ADS, with focus on increased bandwidth in the low power region compared to what is typically seen with DPA's. This is done by eliminating the quarterwave transformer typically used as impedance inverter in traditional DPA designs.

A fully automated measurement setup which utilizes a relatively complex phase alignment algorithm, has been developed to characterize the designed prototype.

The measured results indicate that there are obvious benefits to dynamically controlling the relative phase between the two inputs, and to using adaptive auxiliary device biasing. The measured results suggests that an efficiency increase in the Doherty region of up to 10 % can be achieved by dynamically controlling the phase between the two inputs, although at the expense of output power. By also controlling the biasing of the auxiliary device, an extremely flat gain response can be achieved, but then at the expense of efficiency.

The measurements have not been performed with sufficiently low auxiliary device gate bias voltages, so these benefits can not be completely confirmed with the currently existing measurement data.

The results also show that poor device output reactance compensation prevents the benefits of eliminating the quarterwave transformer impedance inverter from clearly showing.

Bibliography

[1] Farnell Element 14. *Q-point definition*. URL: https://uk.farnell.com/q-point-definition# (visited on 12/10/2018).

[2] P. Asbeck and Z. Popovic. "ET Comes of Age: Envelope Tracking for Higher-Efficiency Power Amplifiers". In: *Microwave Magazine, IEEE* 17.3 (2016), pp. 16–25. ISSN: 1527-3342.

[3] I.J. Bahl and D.K. Triveldi. *A Designer's Guide to Microstrip Line*. Microwaves, 1977.

[4] D. K. Cheng. *Field and Wave Electromagnetics*. 2. Edition. Pearson, 2014.

[5] H. Chireix. "High Power Outphasing Modulation". In: *Proceedings of the IRE* 23.11 (1935), pp. 1370–1392. ISSN: 0731-5996.

[6] P. Colantonio, F. Giannini, and E. Limiti. *High Efficiency RF and Microwave Solid State Power Amplifiers*. 2009.

[7] Cree. *CG2H40010*. 10 W, DC - 6 GHz, RF Power GaN HEMT datasheet. 2019. URL: https://www.wolfspeed.com/media/downloads/1051/CG2H40010.pdf.

[8] S. C. Cripps. *RF Rower Amplifiers for Wireless Communications*. 2. Edition. Artech House, 2006.

[9] W. H. Doherty. "A New High Efficiency Power Amplifier for Modulated Waves". In: *Proceedings of the IRE* 24.9 (1936), pp. 1163–1182. ISSN: 0731-5996.

[10] M.R. Duffy et al. "Bandwidth-reduced supply modulation of a high-efficiency X-band GaN MMIC PA for multiple wideband signals". In: *IEEE MTT-S International Microwave Symposium Digest* (2017), pp. 1850–1853. ISSN: 0149645X.

[11] Andrei Grebennikov and Senad Bulja. "High-Efficiency Doherty Power Amplifiers: Historical Aspect and Modern Trends". In: *Proceedings of the IEEE* 100.12 (2012), pp. 3190–3219. ISSN: 0018-9219.

[12] ITU. *IMT-2020 NETWORK HIGH LEVEL REQUIREMENTS, presentation*. ITU. URL: https://www.itu.int/en/ITU-T/Workshops-and-Seminars/standardization/20170402/Documents/S2_4.%5C%20Presentation%5C%5C_IMT%5C%202020%5C%20Requirements-how%5C%20developing%5C%20countries%5C%20can%5C%20cope.pdf.

[13] L. R Kahn. "Single-Sideband Transmission by Envelope Elimination and Restoration". In: *Proceedings of the IRE* 40.7 (1952), pp. 803–806. ISSN: 0096-8390.

[14] Mini-Circuits. *Coaxial Amplifier*. ZHL-42 datasheet. URL: https://ww2.minicircuits.com/pdfs/ZHL-42.pdf.

[15] D.M. Pozar. *Microwave engineering*. 4th ed. Wiley, 2012. ISBN: 9780470631553.

[16] J. H. Qureshi et al. "A wide-band 20W LMOS Doherty power amplifier". In: *2010 IEEE MTT-S International Microwave Symposium*. IEEE, 2010, pp. 1504–1507. ISBN: 9781424460564.

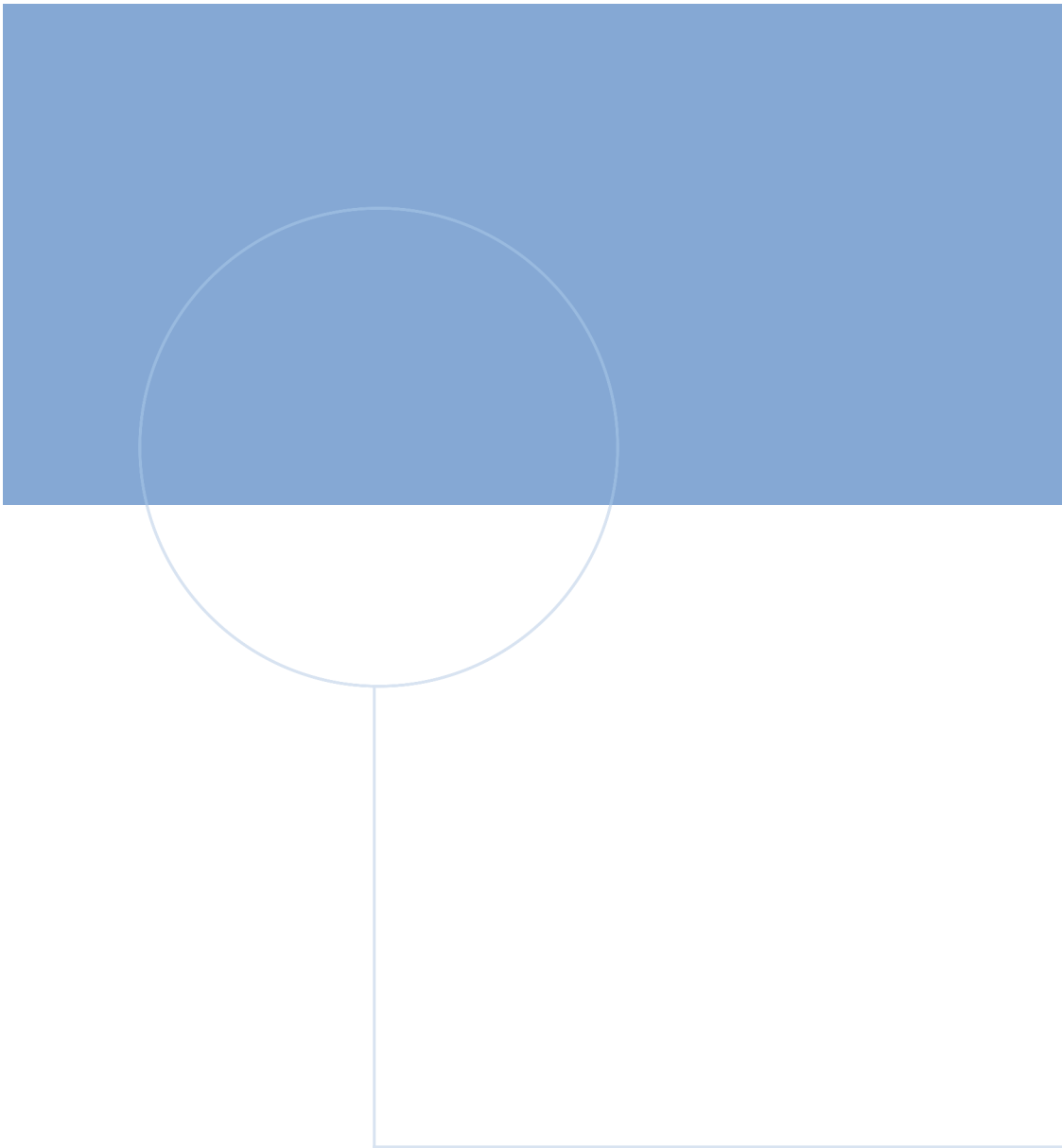
[17] F. Raab. "Efficiency of Outphasing RF Power-Amplifier Systems". In: *IEEE Transactions on Communications* 33.10 (1985), pp. 1094–1099. ISSN: 0090-6778.

[18] C. Ramella et al. "High Efficiency Power Amplifiers for Modern Mobile Communications: The Load-Modulation Approach". In: *Electronics* 6.4 (2017). ISSN: 2079-9292. DOI: 10.3390/electronics6040096. URL: http://www.mdpi.com/2079-9292/6/4/96.

[19] Rohde & Schwarz. *SGMA RF Source Specifications*. SGS100A datasheet. 2019. URL: https://scdn.rohde-schwarz.com/ur/pws/dl_downloads/dl_common_library/dl_brochures_and_datasheets/pdf_1/service_support_30/SGS100A_dat-sw_en_5214-5703-22_v0401_120dpi.pdf.

[20] Rohde & Shwarz. *ZNB8*. Vector Network Analyzer Specifications. 2017. URL: https://scdn.rohde-schwarz.com/ur/pws/dl_downloads/dl_common_library/dl_brochures_and_datasheets/pdf_1/service_support_30/ZNB_dat-sw_en_5214-5384-22_v0900_96dp.pdf.

[21] D. Tröster-Schmid and T. Bednorz. *Generating Multiple Phase Coherent Signals – Aligned in Phase and Time*. https://scdn.rohde-schwarz.com/ur/pws/dl_downloads/dl_application/application_notes/1gp108/1GP108_1E_Generating_Phase_Coherent_Signals.pdf. 2016.



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