Master's thesis

NTNU
Norwegian University of Science and Technology
Faculty of Information Technology and Electrical Engineering
Department of Electric Power Engineering

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Advanced gate drivers for next generation high power converters

Master's thesis in Energy and Environmental Engineering
Supervisor: Dimosthenis Peftitsis
June 2019

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Preface

This master thesis contains my final work as a master student at the Department of Electric Power Engineering at the Norwegian University of Science and Technology. The master thesis is written in collaboration with SINTEF Energy Research.

From I started my studies in August 2014, my passion for power engineering has grown. Especially within the field of power electronics I have found possibilities and challenges that motivates me. Therefore, power electronics have been my specialization field for the last two years of my studies. With the challenges we meet in the future in terms of greener energy systems and electrification, I am sure I have made the right decision.

The thesis builds on the specialization project that was delivered in December 2018 [1]. As it should be possible to read the master thesis without having read the specialization project, Chapter 2 and 3 that covers basic semiconductor theory and gate drivers have been re-used. However, both chapters have been modified to fit into the master thesis. In Chapter 2, some sections have been added or modified and figures have been redrawn to provide better explanations. In Chapter 3, the literature research have been updated to provide an even better overview of the state-of-the art than what was presented in the specialization project.

All the results that are presented in the master thesis are original. Even though some of the the presented figures show similar results as was presented in the specialization project, the laboratory work have been re-done, so that all results have been obtained with the same environmental conditions and thereby can be compared.

Through the work that is presented I have been given the opportunity to publish a paper and to submit an abstract. The paper have been presented at ECCE Asia 2019 in Busan, South Korea, May 27^{th} 2019. It can be found in Appendix A.1. The abstract is submitted to the ICSCRM 2019 conference which will be held in Kyoto, Japan, September 29^{th} to October 4^{th} 2019. The abstract submission can be found in Appendix A.2.

Trondheim, June 2019
Håvard Lefdal Hove

Acknowledgment

I started working with gate drivers for silicon carbide MOSFETs during a summer internship at SINTEF Energy research. I would therefore like to thank SINTEF Energy Research with my two supervisors Giuseppe Guidi and Kjell Ljøkelsøy for giving me the opportunity to work with this interesting topic. The two have always been available to provide help and support with understanding, writing and lab work.

From NTNU my supervisors have been Associate Professor Dimosthenis Peftitsis and PhD candidate Ole Christian Spro. Their support and guiding have been vital in my work with this master thesis. Dimosthenis have always been available for quick questions and meeting, and have encouraged me and helped me with paper writing and abstract submission. Ole Christian have been my day-to-day supervisor. He have always been available for questions and have spent numerous of hours helping me with understanding and guiding me in lab. A massive thanks goes to both Dimosthenis and Ole Christian.

I would also like to thank my parents and my two sisters for supporting me and beliving in me through my five years of studies. It was my parents that opened the door for studies within a technical field at NTNU. Finally, I would like to thank my girlfriend for the support and for being patient with me through hectic months of master writing.

Abstract

This master thesis investigates advanced gate driver topologies for new wide band-gap (WBG) semiconductor devices such as the silicon carbide (SiC) MOSFET. Compared to traditional semiconductor materials such as silicon (Si), WBG devices offer higher blocking voltages, lower on-state resistance, faster switching transients and operation under higher temperatures. This increases the requirement for the gate driver design as high precision and low parasitics are vital to be able to act on the fast switching transients.

Modeling and simulation is an important tool when designing power electronic converters employing WBG devices. Therefore, simulation models must provide accurate and reliable results and converge easily. However, the manufacturer of the SiC MOSFET that is used in this master thesis provides a non-continuous SPICE model for the device that often tends to run into convergence errors. Improvements are therefore suggested, and the reliability of the new model is verified through lab measurements on the actual device. The proposed model provides steady state simulation results that are as accurate as with the model provided by the manufacturer. Moreover, the simulation performance is improved and it converges easily.

A new gate driver topology that aims for delay time minimization, termed the multistage driver, is proposed and validated through laboratory work. The multistage driver is voltage controlled, which is more robust than timing based gate drivers for fast switching devices. By making the multistage driver adaptive based on load current and junction temperature, the best possible reduction in delay time can be obtained. Compared to a conventional gate driver (CGD), the adaptive multistage driver reduces the turn-on delay time by 72 % and turn-off delay time by 74 %. A control circuit that realizes the adaptive multistage driver based on load current measurements for turn-off is proposed and validated through laboratory work as well. With the control circuit, the turn-off delay time is reduced by 71 %.

By using a delay time minimization gate driver in a converter bridge leg, the requirements for dead time and minimum pulse width can be reduced. A motor drive application was simulated. When using the multistage driver compared to the CGD, the simulation results suggests that the linear modulation region can be increased by up to 3.8 %, and the current THD in the linear region reduced by up to 7.7 % when switching at 15 kHz.

Sammendrag

Denne masteroppgaven tar for seg avanserte driverkretser for halvleder komponenter med høy båndbredde (WBG) slik som de nye silisiumkarbid (SiC) MOSFETene. Sammenlignet med tradisjonelle halvleder materialer som silisium tilbyr WBG komponenter høyere blokkespenning, lavere ledemotstand, raskere svitsjetransienter og de kan opereres under høyere temperaturer. Dette øker kravene til driverkretsen side høy presisjon og lite parasittkomponenter er avgjørende for å kunne håndtere de raske svitsjetransientene.

Modellering og simulering er et viktig verktøy i design av kraftelektronikkomformere der WBG komponenter brukes. Simuleringsmodellene må derfor være presise, pålitelige og konvergere raskt. Produsenten av SiC MOSFETen som er brukt i denne masteroppgaven gir derimot en SPICE model som er ikke-kontinuerlig ofte gir konvergeringsproblemer i simuleringer. Forbedringer til denne modellen er derfor foreslått og troverdigheten til den nye modellen er verifisert gjennom labarbeid med en faktisk komponent. Resultatene viser at den foreslåtte modellen og den opprinnelige modellen fra produsenten er like presise for stasjonære forhold. Men, med den foreslåtte modellen er konvergeringsproblemene borte.

En ny driverkrets med formål om å minimere tidsforsinkelser er foreslått og verifisert gjennom labarbeid. Denne er referert til som en flertrinnsdriver. Flertrinnsdriveren er spenningskontrollert, noe som ansees som mer robust for raske svitsjetransienter enn tidsbaserte drivere. Den største reduksjonen i tidsforsinkelser oppnås når flertrinnsdriveren er gjort adaptiv basert på laststrøm og komponent temperatur. Sammenlignet med en konvensjonell driver (CGD) er den adaptive flertrinnsdriveren i stand til å kutte tidsforsinkelsen med 72 % ved påslag og 74 % ved avslag. En kontrollkrets som realiserer den adaptive flertrinnsdriveren ved avslag basert på laststrømsmåling er i tillegg foreslått og testet i lab. Med kontrollkretsen er tidsforsinkelsen kuttet med 71 %.

Ved å bruke en driverkrets som minimerer tidsforsinkelser i en omformerhalvbro kan kravene til dødtid og minimal pulsbredde reduseres. Et motordrifttilfelle ble simulert for å teste påvirkningen dette har. Sammenlignet med CGS viser simuleringsresultatene at ved å bruke flertrinnsdriveren så kan de lineære modulasjonsområdet økes med opptil 3.8 %, og strømmens THD i det lineære området reduseres med opptil 7.7 % når det svitsjes med en svitsjefrekvens på 15 kHz.

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Abbreviations

AGC	=	Active Gate Driver
CGD	=	Conventional Gate Driver
DTM	=	Delay Time Minimization
EMI	=	Electromagnetic Interference
FACTS	=	Flexible Alternating Current Transmission System
FPGA	=	Field Programmable Gate Array
GND	=	Ground
HV	=	High Voltage
HVDC	=	High Voltage Direct Current
IC	=	Integrated Circuit
IGBT	=	Insulated Gate Bipolar Transistor
MOSFET	=	Metal Oxide Semiconductor Field Effect Transistor
MPW	=	Minimum Pulse Width
OV	=	Over-voltage
PCB	=	Printed Circuit Board
PV	=	Photovoltaic
PWM	=	Pulse Width Modulation
SPICE	=	Simulation Program with Integrated Circuit Emphasis
VSI	=	Voltage Source Inverter
WBG	=	Wide Band-gap

Chapter 1

Introduction

1.1 Background and perspective

The worlds energy demand is increasing. According to UN, around one billion people lacks access to electricity [16]. Even though there are a lot of ongoing projects aiming to give more people access, it is still a long way to go. Through the Paris Agreement, almost every country have committed to cut their pollution of climate gasses [17]. Still, to cover the increasing energy demand by use of renewable energy sources is challenging and the CO_2 emissions have continued to increase [18].

Fulfilling the goals in the Paris Agreement depends on the technology development. Evolving the energy systems from fossil fuel to energy carriers such as electricity have been pointed out as important, especially when the electricity comes from renewable energy sources. Equipment that allows renewable energy sources to be introduced to the energy system in an efficient and cost effective way must be developed. In addition, clean technologies that can substitute traditional fossil fuel technologies such as vehicles and airplanes must be further developed. This includes electric vehicles and energy storage systems. The recent trends are positive as the installed renewable energy sources are increasing [19]. In 2017 25% of all electricity worldwide was produced by renewables [20]. However, to keep up with the Paris Agreement the expansion of renewable energy sources must increase. In that development, power electronics will play a key role.

Power electronic components are today used in many electric applications and the integration level is increasing [21]. Typical examples are converters for power supplies, rectifiers for data centers or in HVDC power systems, motor drives in electric vehicles or ships, FACTS in HV transmission systems, or converters for renewable energy integration [22]. The possibilities are many, but further improvement of costs, reliability and efficiency is needed.

In the recent years, a new family of devices within power electronics have been introduced to the market, known as wide band-gap (WBG) devices [5]. They offer higher breakdown voltage, lower on-state resistance, operation under higher temperatures and faster switching transients [23]. Their capabilities opens for new possibilities in power

electronic applications and designs. Currently, the two most promising WBG materials are galium nitride (GaN) and silicon carbide (SiC) [22]. The development show great potential, and the devices are suitable for many different applications [24, 25, 26]. However, since the component price is higher than for conventional semiconductor devices, the benefits of the new technology must be exploited with resulting benefit for the total system. One such benefit could be that the size of passive elements such as filters decrease with increasing switching frequency. Moreover, as the devices can operate under higher temperatures, the requirement for heatsink design can be lowered. This allows for converters with higher power density.

The gate driver is the circuitry that controls the turn-on and turn-off switching transient of semiconductor switching devices. To fully utilize the potential of WBG devices, such as the SiC MOSFET, proper gate drivers must be designed. For traditional semiconductor devices, all parts of the switching transient can be controlled separately by the gate driver. However, due to the increased switching speed of WBG devices, time delays and accuracy makes the control strategies challenging. New gate driver topologies that are able to control the fast switching transients of WBG are therefore vital to push the performance of the devices to the limit.

This master thesis continues the work that was done in the specialization project [1]. In the specialization project, a new gate driver topology was presented and evaluated through laboratory work and simulations. Results in terms of delay time as a function of load current was presented for turn-on and turn-off both from lab work and simulations. In the master thesis, the gate driver performance is further investigated in terms of junction temperature dependency, the SPICE simulation model that was used in the specialization project have been improved to avoid convergence errors, and the impact time delay minimization has on the output voltage and load current quality is investigated.

1.2 Objectives

In this master thesis the main objectives are to:

- Present the development of WBG devices and discuss the areas where they are useful.
- Present and discuss gate drivers in general and to give an overview of the state-of-the-art.
- Propose and discuss a new gate driver topology aiming for delay time minimization.
- Evaluate the performance of the new gate driver through laboratory work.
- Investigate and improve the non-continuous behaviour of the SiC MOSFET SPICE model that is provided by the manufacturer.
- Investigate the impact delay time minimization gate drivers have on the output voltage and line current quality.
- Propose functionality to realize adaptive gate driving based on load current measurements.

1.3 Report Outline

The thesis is divided into 8 chapters to cover the objectives. The first chapter is the introduction. Then, in Chapter 2, an overview of semiconductor basics are provided. The chapter presents the basics in semiconductor physics and uses it to describe the operation principle of the MOSFET including switching transients. In the last part of the chapter, WBG devices are presented and compared to traditional semiconductor materials.

Chapter 3 presents gate drivers. First, a conventional gate driver is presented as it makes the benchmark for the other gate driver topologies in this thesis. Then, state-of-the-art gate drivers from literature are presented and discussed. Finally, a new gate driver topology, termed the multistage driver, is proposed.

In Chapter 4, the SPICE model that is provided by the manufacturer for the chosen SiC MOSFET is investigated. The model tended to run into convergence errors in the specialization project. Therefore, the model structure is investigated and improvements are proposed. The work have resulted in an Abstract submission for the ICSCRM 2019 conference in Kyoto, Japan in September 2019 which can be found in Appendix A.2.

Chapter 5 and 6 presents the work and results that was done for the paper that was presented at ECCE Asia in Busan in May 2019. The paper is found in Appendix A.1. In Chapter 5, the experimental work is presented. Here, the multistage driver is evaluated both for load current and junction temperature dependency. In Chapter 6, the impact delay time minimization gate drivers have on the output voltage and line current quality is investigated through simulations.

In Chapter 7 the multistage driver is made adaptive based on load current measurements. The chapter presents a control circuit that takes in current measurements and provides a voltage reference to the existing PCB. The performance is evaluated through experimental work and compared to the conventional gate driver and the results from Chapter 5.

Finally, in Chapter 8, the conclusions from the master thesis is drawn. In addition, further work is suggested based on the findings in the thesis.

Chapter 2

Semiconductor device theory

Silicon (Si) technology is dominating as the most used semiconductor in power electronic components. However, as the components are reaching their performance limit, the industry is looking for new semiconductor materials. The goal is to make new components with the right characteristics to allow the ongoing development of power electronics in terms of efficiency, increasing switching frequency and higher temperature operation. The result is the introduction of the wide band-gap (WBG) semiconductors. In this chapter, the basics for understanding semiconductors are presented.

2.1 Basics

For a current to flow in a material, charge carriers must be available and free to flow when an electric field is applied. For good conductors, such as metals, the free carrier density (electrons) is high, which gives low resistance. The free carrier density in a metal is a material constant and cannot be changed. For semiconductors such as silicon on the other hand, the carrier density can be changed if impurities are introduced or high electric fields are applied. For impurities, either atoms with fewer or more valence electrons can be introduced to the semiconductor material. If an introduced atom have fewer valence electrons, it will absorb one of the free electrons from another semiconductor atom giving an apparent positive charge that is free to move. This is referred to as a hole, and the semiconductor is said to be p-doped as the majority carrier is a positive charge. If an atom with more valence electrons are introduced, the extra electrons will be free to move in the semiconductor. This gives a higher free electron density and the semiconductor is said to be n-doped [3].

When a p-doped and an n-doped layer is created in the same semiconductor crystal, a pn junction is formed. In the junction, majority carriers will diffuse to the other side. At equilibrium this creates ionized, immobile impurities on each side of the junction. The width of this area is referred to as the depletion layer. On the p-doped side of the junction, but within the depletion layer, there will then be a negative space charge. For the n-doped side it will be opposite with a positive space charge. The charges will create an electric

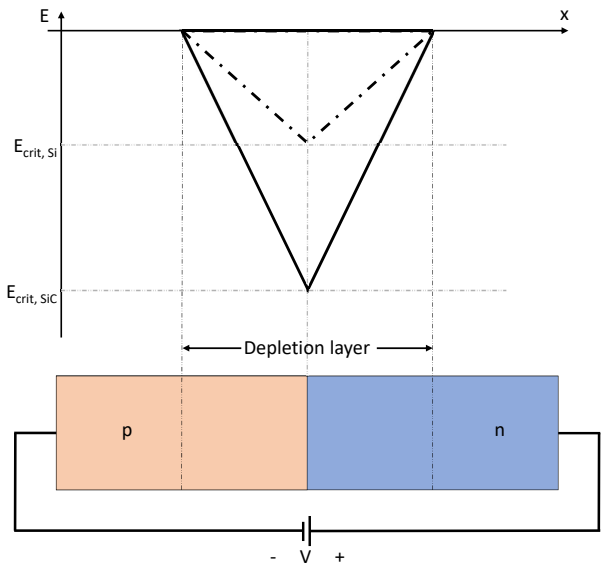


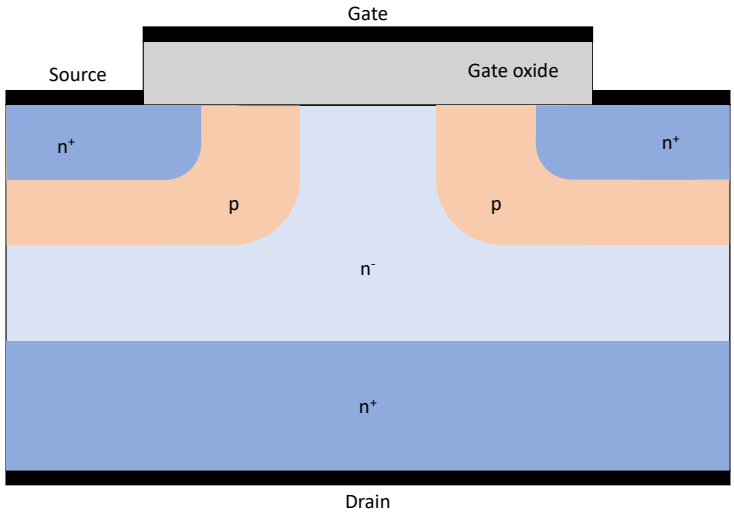
Figure 2.1: Pn junction and critical electrical field for Si and SiC.

field as shown in Figure (2.1). The slope of the electric field is proportional to the space charges in the depletion layer, which is depending on the doping level [3]. The space charges in the depletion layer is assumed to be evenly distributed in Figure (2.1), giving a linear electric field. The pn junction with the solid line must then have a higher doping level than the one with the dotted line. If the peak electric field is higher than the critical field of the semiconductor E_{crit}, the junction will start to conduct current in the reverse direction. This is termed reverse breakdown or avalanche breakdown and must be avoided as the high voltage and current leads to a large heat dissipation that can destroy the device if it is not reduced. Different semiconductors have different critical electric fields, for instance do silicon carbide (SiC) have a higher critical field than Si.

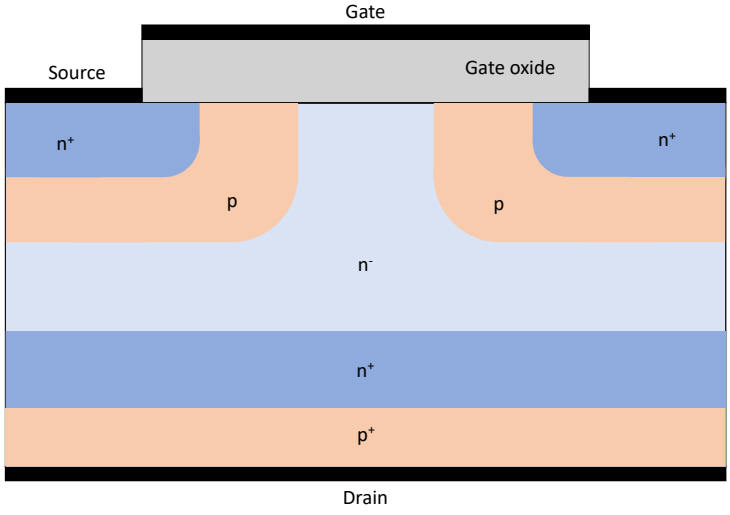
When a voltage is applied in the reverse bias direction of the pn junction (positive voltage on the n-doped side), more charge will diffuse over the junction. This will create a wider depletion layer which results in a higher peak electric field, as the slope of the electric field will have the same characteristic as before. The relationship between the applied voltage and the electric field in the semiconductor is given by Equation (2.1), where DL indicates the depletion layer.

$$V = -\int_{DL} E(x)dx \tag{2.1}$$

The breakdown voltage can be found by evaluating the expression when the peak electric field reaches the critical value. For two semiconductors with the same critical electric field, but with different doping level, the one with the highest doping level will have the lowest breakdown voltage. However, as previously mentioned, the one with the higher doping level will have a lower resistance.



(a) MOSFET



(b) IGBT

Figure 2.2: Semiconducture structures for MOSFET and IGBT.

Semiconductor structures for a n-type MOSFET and n-type IGBT are shown in Figure (2.2). The n-type refers to that it is the negative charged electrons that are the majority carriers and the positive holes that are minority carriers. In p-type devices it is opposite, the positive charged holes will be the majority carriers while the electrons act as the minority carriers. In principle, the semiconductor structure for n-type and p-type devices are opposite with n-doped layers becoming p-doped and the other way around. In practical

use, the n-type MOSFETs and IGBTs are turned on by a positive gate-source voltage, while the p-type will need a negative gate-source voltage to create the channel for the current to flow [3]. In addition, the p-type devices typically have a higher on-state resistance and switches slower as the holes have a lower mobility than the electrons. P-type devices therefore needs a larger area for the same current rating, which makes the devices larger in physical size [27].

In Figure (2.2), the n^- layer is referred to as drift region. The doping level and length of this region determines the breakdown voltage and on-state resistance of the device [3]. In the MOSFET, to allow higher breakdown voltages, the doping needs to be low and the drift region wide. This results in a high on-state resistance, and the performance is poor. To target the challenges, the IGBT was created. In principle, the only difference in the semiconductor structure is the p-doped layer at the bottom of the structure as shown in Figure (2.2). Due to this extra layer, the charges flow through the drift region both by drifting of electrons and diffusion of holes. The drift region is then said to be shorted and the on-state resistance becomes low [3].

2.2 Ideal switching characteristics

2.2.1 MOSFET capacitor model

To describe the ideal switching characteristics of unipolar devices, a MOSFET with its capacitor model will be used as shown in Figure (2.3). It is assumed that the gate is controlled by a conventional gate driver (CGD), which basically is a voltage source (driving voltage) with a resistor in series to the gate. The total gate-loop resistance used in explanations, R_G, includes the external gate resistance and the internal gate resistance of both the MOSFET and the buffer circuit. CGD and other gate driver topologies will be described in Chapter 3.

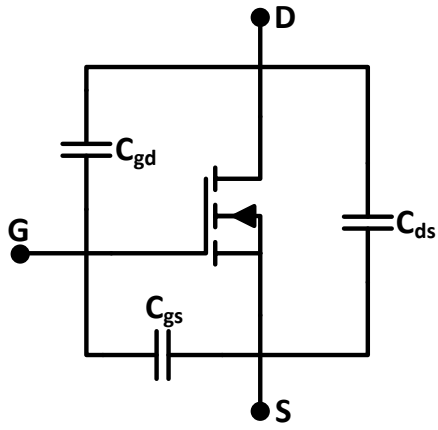


Figure 2.3: MOSFET capacitor model.

When using a CGD, the gate resistance and input capacitance, C_{iss}, of the MOSFET

creates a RC-circuit for the gate-source voltage. This RC-circuit determines the behaviours of the gate-source voltage. In datasheets, the capacitances are presented as given by Equation (2.2), as shown in Figure (2.4).

$$\begin{aligned} C_{iss} &= C_{gs} + C_{gd} \\ C_{oss} &= C_{ds} + C_{gd} \\ C_{rss} &= C_{gd} \end{aligned} \tag{2.2}$$

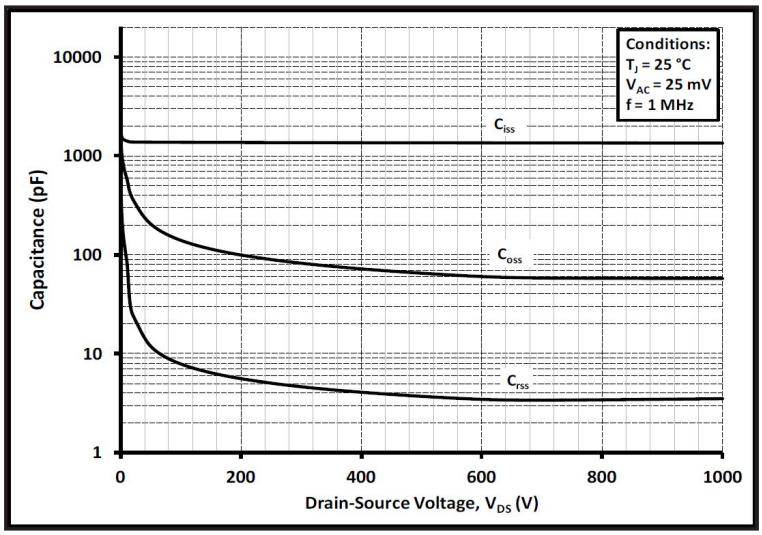


Figure 2.4: MOSFET capacitors as function of drain-source voltage. Taken from C3M0075120K datasheet [2].

One major challenge when modeling the switching transient is the non-linearity of the parasitic capacitors in the MOSFET. Especially $C_{gd} = C_{rss}$, the so-called Miller capacitor, which is highly depending on the drain-source voltage, as seen in Figure (2.4). A common way to model it is therefore with a constant high capacitance value for drain-source voltages up to the driving voltage and with a constant low capacitance value for higher drain-source voltages [3]. This is illustrated in Figure (2.5), where C_{gd1} is the low capacitor value and C_{gd2} is the high capacitor value.

To explain the switching characteristics, the setup in Figure (2.6) is used. In the setup, a current source provides a constant load current that will flow through an ideal diode, D, when the MOSFET is off. The total DC-link voltage, V_{DC}, will then be over the MOSFET.

2.2.2 Turn-on characteristics

For turn-on, it is first when the gate-source voltage reaches the threshold voltage (V_{th}), that the current starts to commutate through the MOSFET as shown in Figure (2.7). At this point, the electric field in the structure is large enough to provide an inversion layer

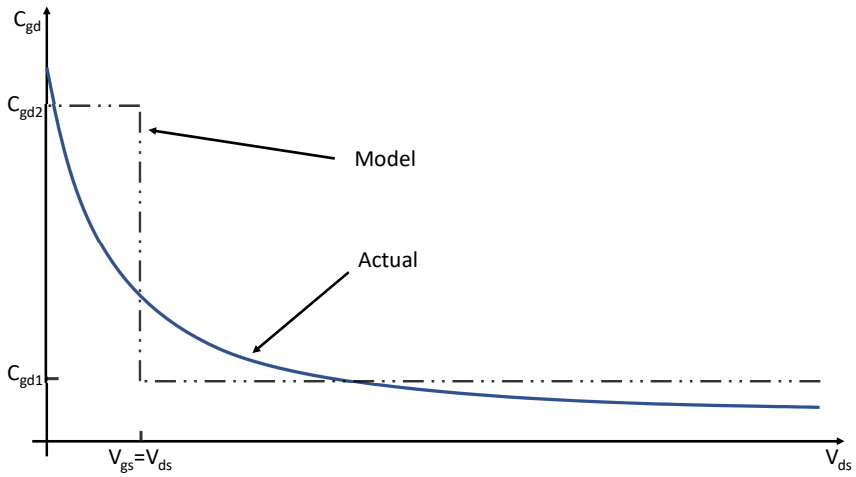


Figure 2.5: Miller capacitor model, recreated from [3].

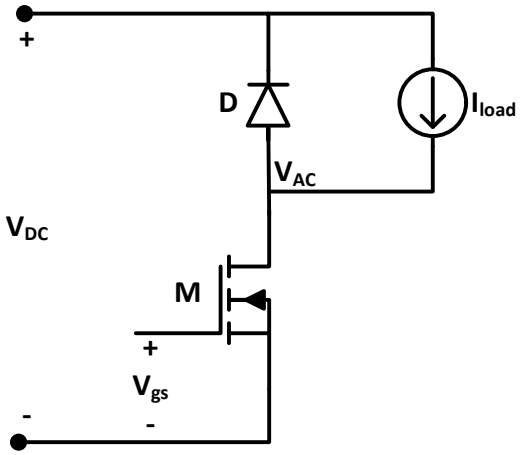


Figure 2.6: Setup used to describe the switching characteristics.

with free electrons, a ”channel”, for the current to flow past the p-layer in the MOSFET structure seen in Figure (2.2). The time it takes before the gate-source voltage reaches the threshold voltage is referred to as the turn-on delay time. When including the parasitic inductances in the circuit loop, the gate-source voltage and gate current will be given by Equation (2.3) and (2.4) as presented in [28]:

$$v_{gs} = \frac{V_{gg}}{L_{eq}C_{\text{iss}}s^2 + R_G C_{\text{iss}}s + 1} \tag{2.3}$$

$$i_g = C_{\text{iss}}sv_{gs} \tag{2.4}$$

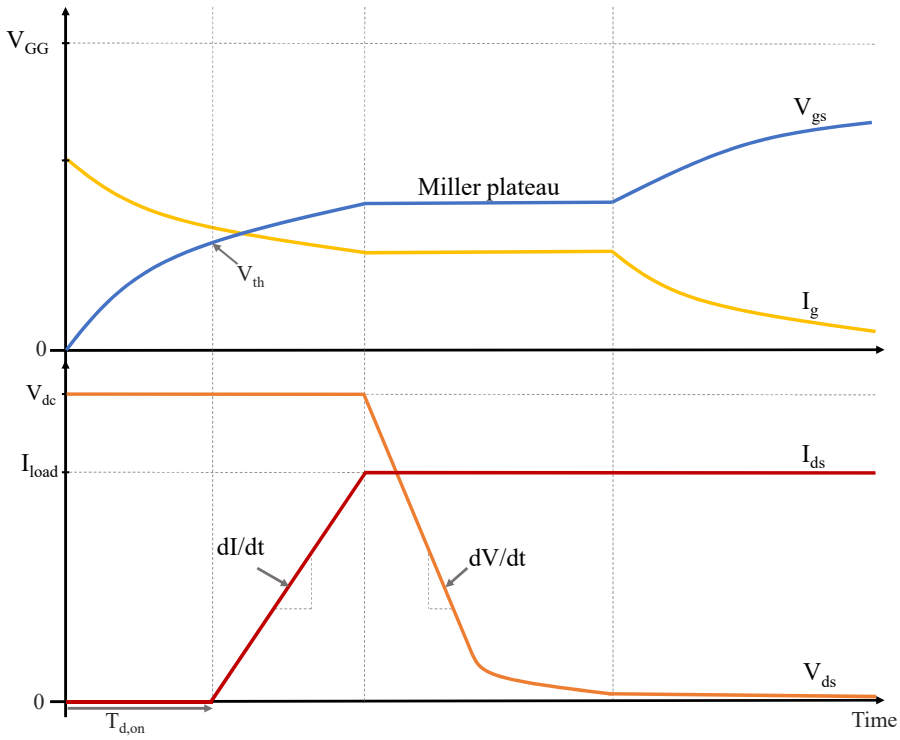


Figure 2.7: Ideal turn-on switching waveforms as presented in [3].

where V_{gg} is the driving voltage, R_G is the total gate-loop resistance, L_{eq} is the total inductance in the gate loop and s is the laplace operator. Before the voltage commutation starts, the drain-source voltage is high. Therefore, C_{iss} is modeled with a low value as previously explained. The gate-loop inductance is small and often neglected when drawing ideal switching trajectories like in Figure (2.7). This gives a pure exponential behaviour with no oscillations. The delay time is determined by the time constant created by the gate resistor and the input capacitor.

When the gate-source voltage reaches the threshold voltage, the current commutation, di/dt, starts. The relationship between the drain current, gate-source voltage and gate current is then given by the transconductance of the switching device, g_m, as shown in Equation (2.5).

$$\frac{\mathrm{d}i_d}{\mathrm{d}t} = g_m \cdot \frac{\mathrm{d}V_{gs}}{\mathrm{d}t} = g_m \cdot \frac{i_g}{C_{gs}} \tag{2.5}$$

The transconductance is not a constant; it is gate-source voltage and junction temperature dependent. Equation (2.5) will therefore be non-linear. Estimating the current commutation with other simpler equations is therefore preferred. For example, in [28] the current commutation is modeled as a function of gate-source voltage by Equation (2.6), where β is a constant and V_{th} the threshold voltage.

$$i_d = \beta \left[v_{gs}(t) - V_{th} \right]^2 \tag{2.6}$$

A linear relationship between drain current and gate-source voltage is also presented, for instance in [3]. Anyhow, both models show that if the gate-source voltage is changed fast, then the drain current will commutate fast as well which is in accordance with Equation (2.5). Hence, di/dt can be controlled by the gate-source voltage. The transfer curve for the SiC MOSFET used in experimental tests in Chapter 5 in this thesis is included in Figure (2.8).

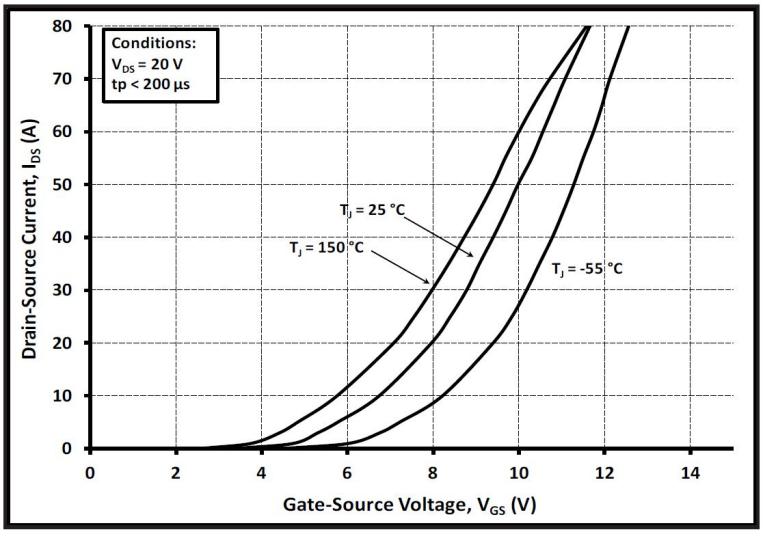


Figure 2.8: MOSFET transfer curve. Taken from C3M0075120K datasheet [2].

The drain current commutation will continue until the full load current is carried by the MOSFET. During the commutation, the MOSFET is in the active region and the current is said to be saturated. This means that drain current is not depending on the drain-source voltage, but rather on the gate-source voltage. This means that both drain current and drain-source voltage is non-zero, giving losses.

Once the full load current is carried by the MOSFET, the drain-source voltage will start to decrease. When the drain-source voltage decreases, the drain-gate voltage will decrease as well. This means that the gate-drain capacitor (C_{gd}) will be charged. In fact, almost all the gate current will charge this capacitor, and the gate-source voltage, v_{gs}, will therefore be temporary clamped at the current value. This is referred to as the Miller plateau, and is illustrated in Figure (2.7) by a constant gate-source voltage while the drain-source voltage is falling (V_{miller}). During the Miller plateau, the gate current can be assumed to be almost constant, given by Equation (2.7).

$$i_g = \frac{V_{gg} - V_{miller}}{R_G} \tag{2.7}$$

As the gate-source voltage is temporary clamped, the drain-gate voltage will drop at a

similar rate as the drain-source voltage. As the gate current flows through the gate-drain capacitor, the dv/dt will be given by Equation (2.8) which is presented both in [28] and [3].

$$\frac{dv_{dg}}{dt} = \frac{dv_{ds}}{dt} = -\frac{i_g}{C_{gd}} \tag{2.8}$$

When the MOSFET has reached the linear region, where the voltage drop can be given by the drain current and the on-state resistance, v_{gs} is no longer clamped. The MOSFET is then said to be turned on. However, the drive circuit continues to charge the input capacitors until $v_{gs} = V_{gg}$. This will increase the inversion layer and thereby reduce the on-state resistance slightly. This last part of the gate-source voltage slope will again be given by Equation (2.3), but now C_{iss} is modeled as a high value [3].

2.2.3 Turn-off characteristics

For turn-off, the characteristics are opposite of turn-on. The driving voltage is low (typically zero or negative), and the gate-source voltage starts to decrease. The turn-off process aims to close the channel to stop the current from flowing. Initially, the input capacitor of the MOSFET is discharging and the shape of the gate-source voltage will again be given by Equation (2.3). However, this time with a low driving voltage and a high initial gate-source voltage. Furthermore, as the drain-source voltage is low at this point, C_{iss} will be modeled as a high value giving a large time constant. As seen from Equation (2.4) and illustrated in Figure (2.9), the gate current will be negative as the derivative of the gate-source voltage is negative. This is also obvious as the MOSFET capacitors are discharging. The idealized turn-off waveforms are shown in Figure (2.9).

As the switching characteristics for turn-off are opposite from the turn-on process, the gate-source voltage will decrease until it meets the Miller plateau. The time it takes is referred to as the turn-off delay time. During the delay time, the on-state resistance will increase slightly due to a smaller inversion layer, and the drain-source voltage will increase slightly as well. However, it is first during the Miller plateau that the voltage commutates from low to high. As for turn-on, the gate current and voltage commutation slope will be given by Equation (2.7) and (2.8).

When the drain-source voltage commutation is finished, the drain current starts to decrease. As for turn-on, the behaviour will be given by the transfer curve of the MOSFET which could be modeled either linear or as a second order function [3], [28].

After the current commutation, the gate-source voltage will be back at the threshold voltage. The device is then turned off. The gate-source voltage will still decrease until it meets the driving voltage level.

2.2.4 Switching losses

One of the main concerns in power electronics design is switching losses. During turn-on, the MOSFET will be in the active region where the drain current increases while the drain-source voltage still is high. This means that for a short time period, both the drain current and drain-source voltage will be high, resulting in losses as illustrated in Figure (2.10). The area under the triangular curve for power dissipation represents the switching

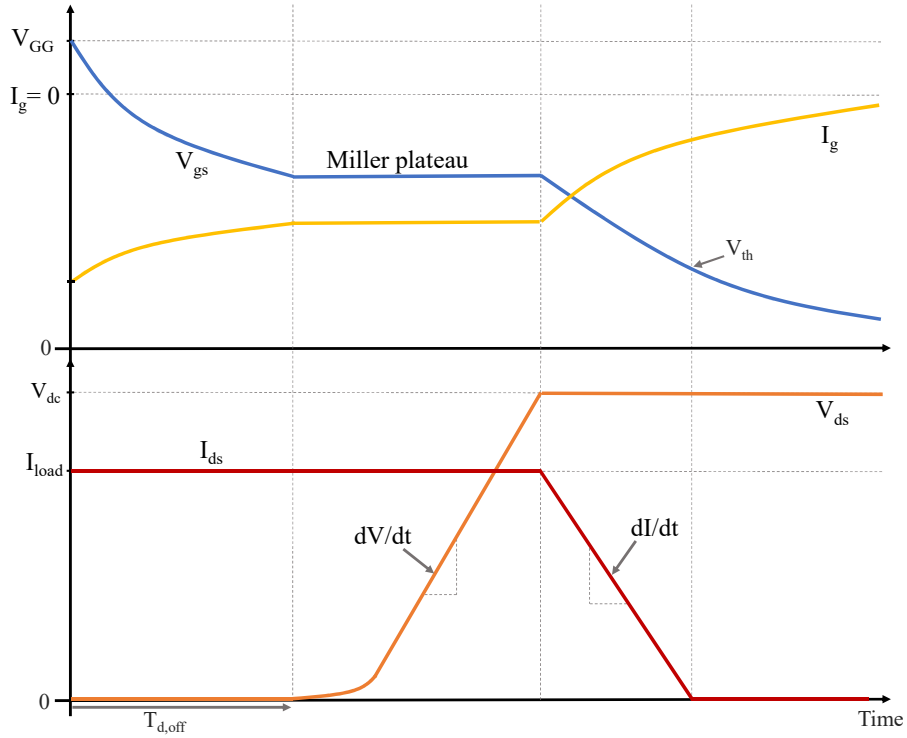


Figure 2.9: Ideal turn-off switching waveforms as presented in [3].

energy for turn-on. Characteristics for turn-off is similar. The total switching losses is the sum of the turn-on and turn-off energy multiplied with the switching frequency.

From Figure (2.10) it is seen that the peak of the power dissipation curve is given by the DC-link voltage and the load current. The total switching energy will still vary depending on the voltage and current commutation slopes, which can be controlled by the gate driver. If the gate resistor is chosen to be small, the time constants in the switching transients will be small as well. This gives fast commutation slopes and, hence, low switching losses. However, due to parasitics or equipment in the power loop, there could be restrictions on the maximum allowed dv/dt and di/dt. The MOSFET can therefore not be switched as fast as desired, but needs to be adjusted for the specific application.

2.3 Non-ideal switching characteristics

2.3.1 Ringing and overshoots

For explanation purposes, the inductances in the power loop and the gate loop was neglected when explaining the ideal switching characteristics. However, as seen from Equation (2.3), the equivalent gate loop inductance, L_{eq}, gives a second order response for the gate-source voltage. Similarly, the total power loop inductance will make an impact on

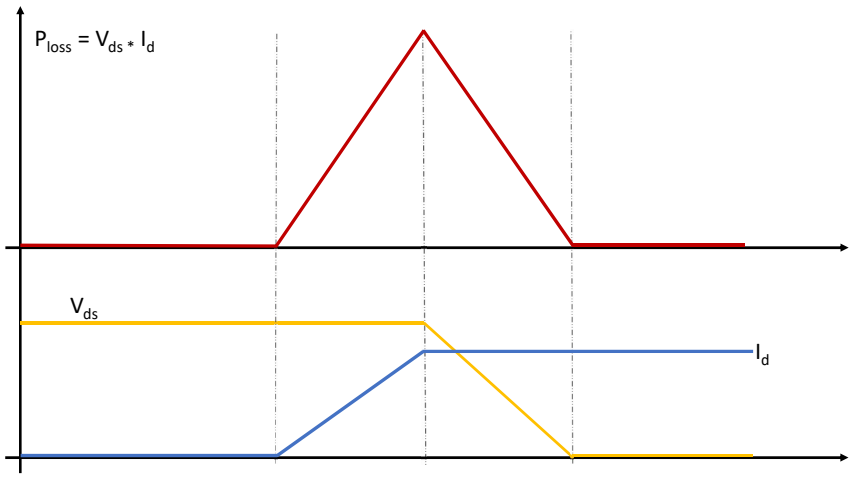


Figure 2.10: Switching losses in a MOSFET with an inductive load.

the switching transients. Moreover, most MOSFETs have a common loop inductance that couples the gate loop and the power loop. Thus, disturbances in the power loop can be visible in the gate loop.

The impact of the power loop inductance is largest at turn-off as it gives overshoots and ringings in the drain-source voltage [28]. The ratio between the power loop inductance and the common loop inductance determines the overshoot together with the voltage commutation slope [29]. The ringing frequency will be given by the power loop inductance and the parasitic capacitance in the circuit and the dampening controlled by the resistance in the loop. Minimizing the overshoot and ringings are usually a design goal in power electronics design.

At turn-on, the most obvious disturbances in a half-bridge is the reverse recovery of diodes. When a power diode is forward bias and conducts current, it stores a certain amount of charge. This amount of charge must be swept out of the diode again for it to become reverse bias and start to block current. This mechanism is visible as a current spike in the reverse current direction for the diode. The total amount of charge and the current commutation rate determines the magnitude of the spike which gives rise to ringings and potential over-voltages [3].

2.3.2 Current and temperature dependency

In the explanations so far nothing have been assumed regarding DC-link voltage, load current magnitude or device temperature. However, the switching characteristics depends on all these parameters. As seen from Equation (2.8), the voltage commutation rate is independent of the DC-link voltage. Hence, DC-link voltage mostly impacts the length of the Miller plateau and thereby the commutation time. However, for a given application, the DC-link voltage is usually constant. Therefore, its impact does not change dynamically during operation like for example the impact from load current magnitude and junction

temperature.

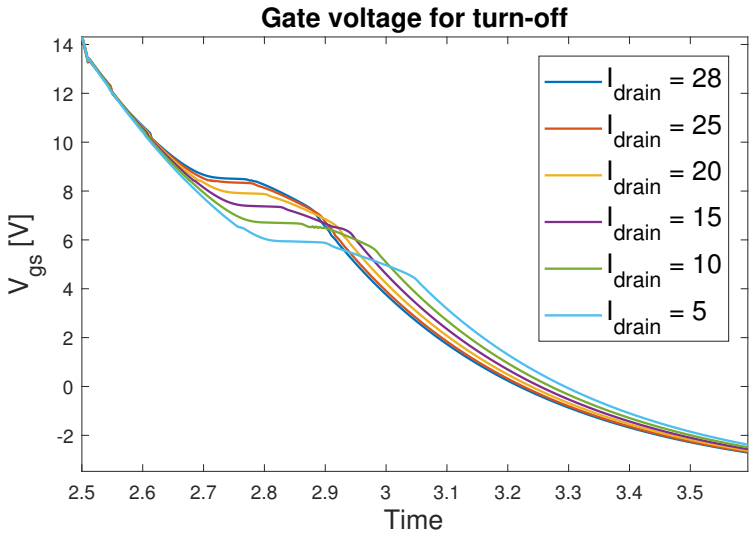


Figure 2.11: Gate-source voltage at turn-off for different load currents.

As the threshold voltage and input capacitors of the MOSFET is independent of load current, the turn-on delay time and gate-source voltage will not be influenced by the load current either. Moreover, as seen from Equation (2.5), the current commutation rate does not depend on the load current magnitude. This means that for a larger load currents, the commutation time will increase. During this increased commutation time, the gate-source voltage will rise to a higher voltage level before the current commutation is over and voltage commutation starts. Hence, the Miller plateau is load current dependent as illustrated in Figure (2.11).

The amount of free charges in a semiconductor increases with increased temperature [3]. With more free charges available, the electric field grows faster and gives a thicker inversion layer. This means that the threshold voltage of a MOSFET will depend on the junction temperature as the inversion layer grows faster for higher temperatures allowing the current to flow at a lower gate-source voltage. This relationship is shown in Figure (2.12) for the SiC MOSFET that will be tested in Chapter 5.

As discussed, for a higher junction temperature, the MOSFET will start to conduct the load current at a lower gate-source voltage. As the Miller plateau will be determined by the gate-source voltage level where all the load current is carried by the MOSFET, this means that for a given load current, the Miller plateau will be at a lower voltage level for a higher junction temperature. Hence, the Miller plateau is both load current and junction temperature dependent; it increases with increased load current, and is lowered by increasing junction temperature.

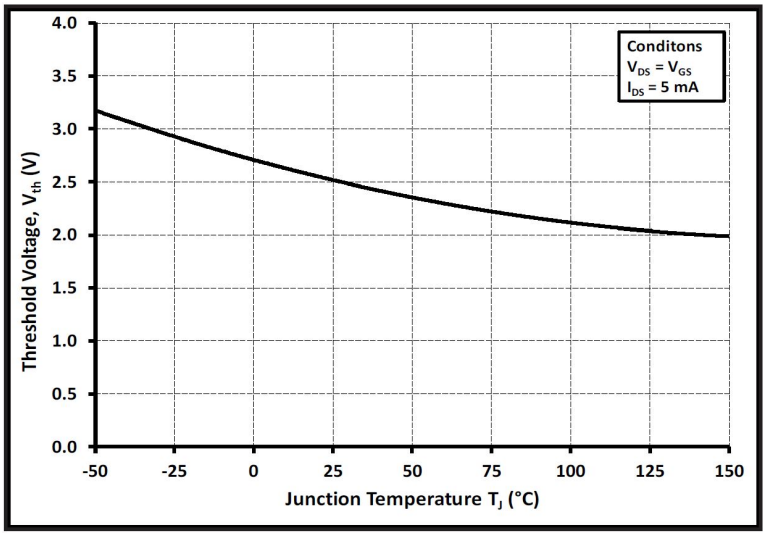


Figure 2.12: Threshold voltage for different junction temperatures. Taken from C3M0075120K datasheet [2].

2.3.3 Dead time

To avoid shoot through when switching a bridge leg such as the one shown in Figure (2.13), a dead time where both switches are turned off must be added as indicated in Figure (2.14). The dead time must be large enough so that the conducting switch is turned completely off before it is safe to turn on the complementary switch. In addition, a safety margin is usually added to ensure that the switch will not be turned back on due to the Miller effect when turning on the complementary switch. The minimum dead time that must be added is given by Equation (2.9) where $T_{dv/dt}$ and $T_{di/dt}$ is the voltage and current commutation times and T_{safe} is the added safety margin.

$$T_{dt} = T_{d,off} + T_{dv/dt} + T_{di/dt} + T_{safe} \tag{2.9}$$

Due to the Miller plateau's dependency on load current and junction temperature, $T_{d,off}$ and thus the dead time requirement will depend on the load current and junction temperature as well. Usually, the dead time is set based on the operating point with the largest dead time requirement. However, load current dependent dead time can be decreased by adaptive gate driving [30].

Due to the inductive behaviour of the load, the current must have an alternative path during the dead time. Therefore, during dead time, the load current will be freewheeling through the anti-parallel diode of either the upper or the lower switch. For a positive load current, it must conduct through the lower anti-parallel diode thus dragging the bridge leg midpoint down to the negative DC-link voltage. Likewise for a negative load current that must conduct through the upper anti-parallel diode thus dragging the bridge leg midpoint up to the positive DC-link voltage. This gives voltage pulses that are load current dependent as shown in Figure (2.14). Furthermore, if the body diode of the SiC MOSFET

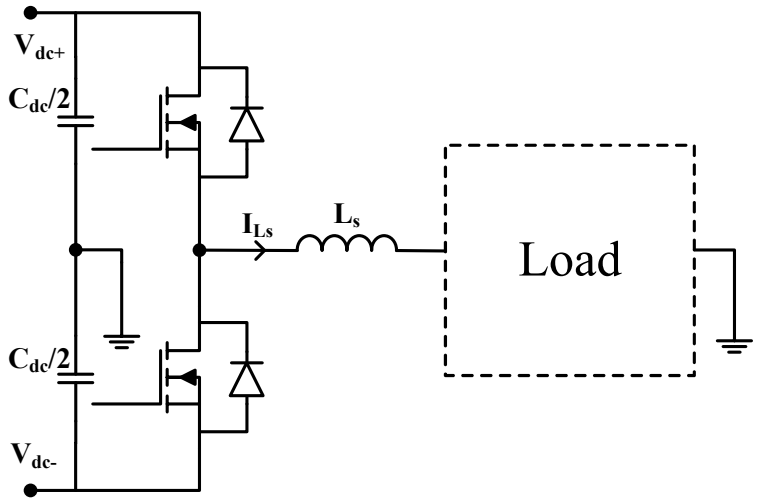


Figure 2.13: Schematic diagram of a half-bridge with a load connected.

is used as anti-parallel diode instead of an external Si power diode, the conduction losses during freewheeling are increased due to the higher forward voltage drop of WBG devices. Hence, minimizing dead time could increase the efficiency as well as the output voltage quality.

2.3.4 Miller effect

One of the reasons to add a safety margin to the dead time is to avoid parasitic turn-on due to the Miller effect. For a MOSFET, the parasitic capacitors will be located as was shown in Figure (2.3). During operation, these capacitors will act as very fast voltage dividers, and the changes in the drain-source voltage will be seen on the gate-source voltage as described by Equation (2.10) [31], where U_{gs} is the gate-source voltage and U_{ds} is the drain-source voltage.

$$U_{gs} = \frac{C_{gd}}{C_{gd} + C_{gs}} U_{ds} \tag{2.10}$$

Transient changes in the drain-source voltage such as large dv/dt during commutation of the complimentary switch, could potentially be visible on the gate-source voltage. If the gate-source voltage is not sufficiently low at the time, this could potentially turn the MOSFET on which will lead to a short circuit.

In power electronics design, due to the problems with parasitic turn-on, it is important that the parasitic capacitance between gate and drain is not to large. In addition, one should ensure that the gate-source voltage is sufficiently low when the voltage commutation starts. SiC MOSFETs typically have a lower threshold voltage than Si MOSFETs and are therefore often driven by a negative biased lower driving voltage to avoid parasitic turn-on [23]. Another solution that addresses the problem is to insert a capacitor

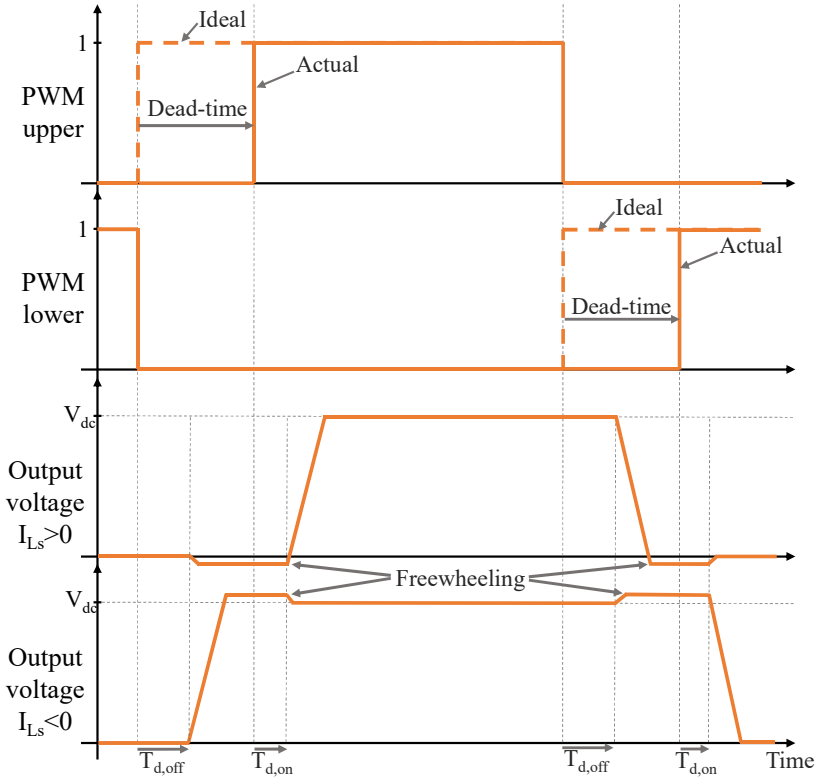


Figure 2.14: Theoretical waveforms showing the impact of dead time in a bridge leg. First presented in [4].

between gate and source. This increases the ratio between the gate-source capacitance and gate-drain capacitance as was described to be vital in [31]. However, this will slow down the switching transient and other solutions are therefore proposed. The Miller-clamp is highlighted as a good solution in particular [32].

2.4 WBG devices

2.4.1 Properties

The two most promising WBG semiconductor materials are silicon carbide (SiC) and gallium nitride (GaN). As all WBG materials, they benefit from the larger energy gap and a high critical electric field. Their material properties compared to silicon (Si) can be seen in Figure (2.15).

Both GaN and SiC have a high critical electric field compared to Si. In fact, it is 10 times higher than the critical field of Si for both GaN and SiC according to [23]. This allows the components to be made with a much thinner drift layer, higher doping, or a combination of the two and still provide the same voltage ratings.

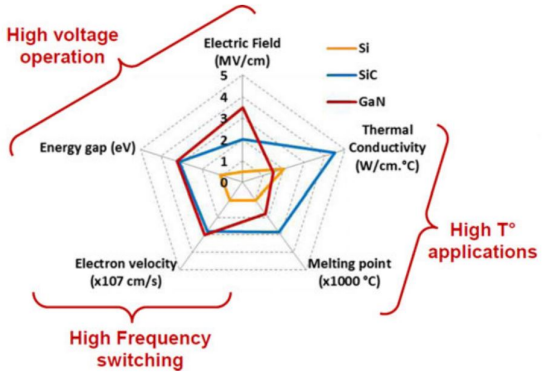


Figure 2.15: Material properties for different semiconductors [5].

A thinner drift layer results in a lower on-state resistance. In theory, using SiC one can achieve an on-state resistance that is 1/300 times the specific on-state resistance for Si per area at the same voltage rating [23]. The lower specific on-state resistance allows for components with smaller die size to be made. This will reduce the parasitic capacitance leading to faster turn-on and turn-off switching than what is achieved using Si counterparts.

Due to the higher band-gap of SiC, the devices can be operated under higher temperatures than Si devices [33]. The operation temperature limit is often restricted due to the thermal reliability of the packages [23]. In 2014 GE announced the first 200°C rated SiC MOSFET [24] which is an example of the ongoing development. This allows creation of new high temperature devices and could be important in the future evolution of power electronic converters. GaN on the other hand does not have the same outstanding temperature dependency. The on-state resistance is low, but they have a positive temperature coefficient similar to the one for Si [34]. This means that they perform poorer when the temperature increases.

The first WBG power device available in the market was a SiC Schottky diode. It was released to the marked in 2001 by Infinion [24]. The first GaN Power device was released by International Rectifier (now Infinion) in 2010 [35]. Ever since, the development have been enormous and more devices are proven to be reliable and introduced to the market. The market forecast presented by IHS Technology at APEC 2016 [35] estimates an increasing market and reduced prices for WBG devices in the coming years. They conclude that SiC will be the leading technology for voltage levels higher than 1000 V, while GaN will offer the most benefit at lower voltage levels.

2.4.2 Si and SiC comparison

Si devices

Si MOSFETs are today commonly used in many applications. The planar MOSFET, which has a structure as shown in Figure (2.2) is the most common. They switch fast, are easily controlled and have low specific on-state resistance. However, because of the relatively

low critical electric field of silicon, the Si MOSFET must be made with a larger drift region when designed for high voltages. This will give a large specific on-state resistance, making the devices impractical. The planar Si MOSFETs are therefore only used up to a couple of hundred volts [3].

To achieve higher voltage ratings and higher switching frequencies, the super-junction MOSFET have been developed. The semiconductor structure is similar to a planar MOSFET, but with multiple pn junctions vertically arranged [36]. This will arrange the electric field to be constant in the drift region allowing devices to be designed with lower specific on-state resistance and gate charge, while still provide the same voltage ratings [37]. The super-junction MOSFET provides lower reverse recovery charge for the body diode as well. However, the reverse recovery time is shorter, meaning that a larger current spike is expected [38]. This should be in mind when designing circuits.

To circumvent the challenges related to losses in high voltage planar Si MOSFETs, attempts to combine MOSFET and BJT was performed [3]. The result was the IGBT which has a structure pretty similar to a MOSFET, but with an extra injection layer in the bottom of the structure as shown in Figure (2.2). This gives the IGBT the ability to block high voltages, while still provide low on-state resistance. The low on-state resistance is due to the injection layer that provides a double injection into the drift region. The double injection gives a higher concentration of excess carriers and is similar to the operation physics of a power diode. The drawback is that the charge stored in the drift region during the on-state needs to be discharged before the device is turned off. This gives a ”tale-current” that will give higher switching losses and limit the switching frequency. Also, as the devices are relatively large, they have large parasitic capacitance which slows down the switching speed. A final challenge with the Si IGBT is the temperature dependency as both the switching losses and the on-state resistance will increase with temperature due to the properties of silicon.

SiC MOSFET

As SiC have much higher critical electric field than Si, devices with lower specific on-state resistance per area can be made. When designing a SiC switch, the bottom injection layer used in IGBTs will therefore not be necessary. Hence, a high voltage MOSFET can be made. Compared to an IGBT, a MOSFET has no tale-current during turn-off. This gives lower switching losses for the MOSFET. In addition, the smaller die size gives smaller parasitic capacitances which enables faster switching transitions. This will further reduce the switching losses of the devices.

The temperature dependency is one of the major benefits with the SiC MOSFETs compared to Si IGBTs. The on-state resistance in silicon devices increases with temperature. In addition, the tale-current of the Si IGBTs during switching is larger at higher temperatures. For SiC MOSFETs on the other hand, both the specific on-state resistance and switching losses is almost constant for different temperatures. This is shown in [33] through experimental lab work. The same article also shows that the switching losses increased by a factor 1.6 for a Si IGBT with similar ratings when the junction temperature increased from 25° to 175°.

As the band-gap of SiC is about three times larger than for Si, the forward voltage drop of the MOSFET body diode will be about three times higher for SiC than for Si as well.

A typical value for the forward voltage drop is around 3V [23]. This means that there will be higher conduction losses during freewheeling through the body diode. Hence, in many applications it will be preferable to use an external anti-parallel freewheeling diode to reduce the conduction losses. On the other hand, the recovery current of SiC MOSFET body diode is shown to be limited to discharging the parasitic capacitances. Hence, the operation is similar to the one of a Shottky diode [23]. This means that the diode recovers much faster than a Si diode, and reduces the switching losses and noise compared to a Si MOSFET body diode. They could therefore still be used as freewheeling diodes to reduce the added complexity or cost by having external anti-parallel diodes.

The development of SiC MOSFETs gives MOSFETs with higher blocking voltage. Currently, SiC MOSFETs rated for 1.7 kV are commercially available from Wolfspeed (Cree). Hence, SiC MOSFETs and Si IGBTs are now available in the same voltage range.

2.4.3 Applications

As already stated, SiC MOSFETs are competing with the commonly used Si IGBT as they offer same voltage ratings. In fact, research already suggests that they can replace IGBTs [39] and reduce the costs in applications such as solar panels [24], [40], wind turbines [41], motor drives [42], and electrical vehicles [24], [43].

When utilizing the strengths of SiC MOSFETs, one could for instance increase the switching frequency and still have the same switching losses. In [42] it is shown that for given Si IGBT and SiC MOSFET package with similar ratings, the total losses in the IGBT at a switching frequency of 10kHz is equal to the losses in the MOSFET at 25kHz at 25°C. For 125°C the switching frequencies are 4kHz and 35kHz respectively. Hence, the switching frequency can be increased giving the same losses. This means that the size of passive elements, for example the filter, can be reduced in addition to improving the harmonic spectrum of the output voltage. Due to the temperature independency of the SiC MOSFET, lower requirements for the cooling systems can be set as well. This will result in converters with increased power density.

The temperature independency of SiC will also be beneficial for operation in locations where high temperatures might occur. An example is solar inverters where SiC will provide a more stable operation [40]. In addition, the possibility to make more power dense converters could be important for rooftop applications where a specific power per weight density is necessary [24]. Another application that will benefit from higher power density are electric vehicles, as reduced size and weight of the vehicle will improve the overall performance.

The possible applications are many. Looking into the marked forecast provided by IHS Technology in 2016 [35], it is assumed that hybrid and electric vehicles will dominate the SiC marked by 2025. Other large technologies that will utilize the benefits from SiC are power supplies, PV inverters and motor drives. This is in good coherence with the technology finding in literature.

Chapter 3

Gate drivers

A gate driver is the circuitry that determines the turn-on and turn-off switching transient of the transistor. The switching transients will depend on the gate-source voltage as discussed in Chapter 2. This chapter presents an overview of gate drivers, and proposes a new gate driver topology.

3.1 Conventional gate driver

When driving a MOSFET in a converter, the turn-on or turn-off signal comes from the control system. Pulse width modulation (PWM) is commonly used. The signal is sent to the buffer IC, where it is amplified to send out either a positive driving voltage (V_{pos1}) or a negative driving voltage (V_{neg1}).

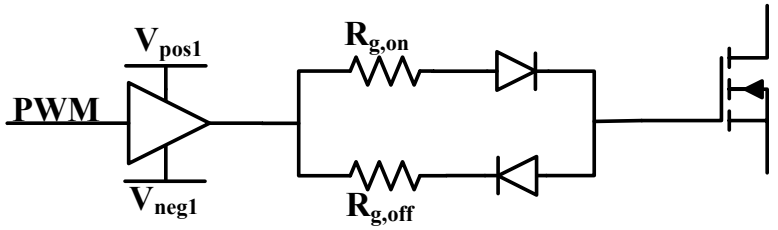


Figure 3.1: Conventional gate driver (CGD) with separate turn-on and turn-off gate resistor.

A schematic diagram of the conventional gate driver (CGD) is shown in Figure (3.1). It consist of a gate resistor that is placed in series between the IC and the MOSFET. The gate resistor will limit the gate current that charges the input capacitor of the MOSFET. This way, by properly choosing the gate resistor, the commutation slopes for current and voltage transitions can be controlled. Very fast switching transitions will result in smaller switching losses. However, due to over-voltages (OV), oscillations or EMI generation, most applications have maximum limits for the allowed commutation rates. Therefore, the

gate resistor is usually chosen large enough to slow down the device to meet the design limit, on the cost of larger delay times and switching losses.

As the turn-on and turn-off behaviour of MOSFETs are slightly different, separate current paths for turn-on and turn-off from the IC to the MOSFET is often provided. This allows for controlling dv/dt for turn-on and turn-off independently. This topology is shown in Figure (3.1). In many applications, CGD is sufficient to control the switching transients. As the CGD also benefits from its simplicity, it is commonly used. In this master thesis, it will be used as the reference point.

3.2 RC driver

As increasing the gate resistor to meet the limit for commutation rates in a given application will increase the delay time and thereby the required dead time when using CGD, gate driver concepts with higher degree of freedom are proposed in literature. One proposal is the RC-driver that targets the delay time [44], [43]. It is presented in Figure (3.2). Compared to other suggestions for delay time minimization (DTM) it benefits from its simplicity.

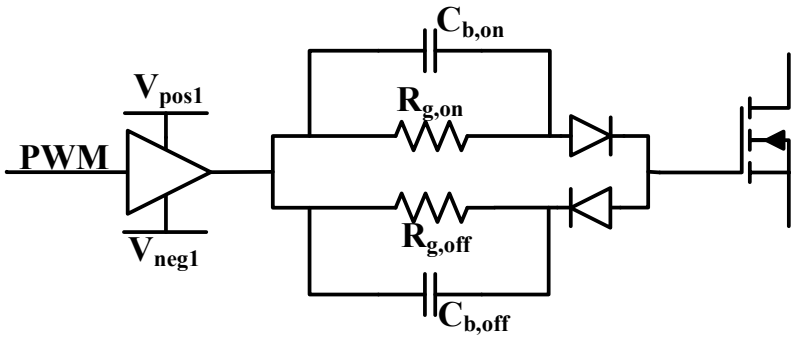


Figure 3.2: The RC driver with separate current paths for turn-on and turn-off.

The RC driver is a CGD where boost capacitors have been connected in parallel with the gate resistors. When the IC goes from a low driving voltage to a high driving voltage, or opposite, the capacitors act as high pass filters giving an initial boost current according to Equation (3.1).

$$i_C = C\frac{dV_C}{dt} \tag{3.1}$$

The current will force turn-on or turn-off to start at an earlier point. The rest of the switching transient will be controlled by the gate resistor, similar as in the CGD. The expected impact from the RC-driver on the switching transient is shown in Figure (3.3), where ΔT_{delay} is the reduction in delay time. The switching transient should be identical to what is achieved with a CGD, only shifted in time due to the improved delay time.

To decide for an appropriate capacitor size in the RC-Driver, the gate charge needed to start the commutations must be known. The goal is only to reduce the delay time and

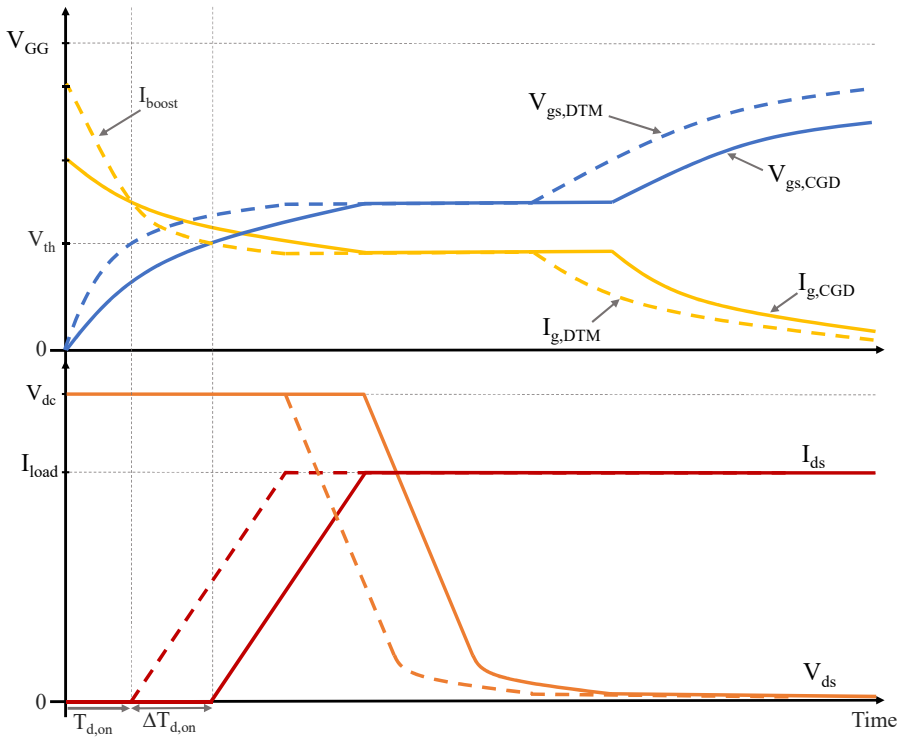


Figure 3.3: Delay time minimization (DTM) switching characteristics compared to CGD.

then let the CGD control the switching transient in terms of dv/dt and di/dt. This means that the charge that should be delivered or discharged from the gate must be equal to the charge needed to change the gate-source voltage from the initial value up to the threshold value for turn-on and down to the Miller plateau for turn-off. This charge can usually be found in datasheets. By integrating Equation (3.1) an estimate for the charge released by the capacitor is found. If the capacitor is assumed to be constant, the charge will be given by Equation (3.2), where ΔV_C is the total difference in the driving voltage.

$$Q_C = C\Delta V_C \tag{3.2}$$

As the threshold voltage will be junction temperature dependent and the Miller plateau load current dependent, the sizes of the boost capacitors must be designed with great care. To not interfere with neither dv/dt nor di/dt, the boosting stage must be ended by the time commutation starts for all operation points. Thus, the boosting capacitors must be designed for worst case which means that the performence might not be optimal during normal operation. To provide a better overall performance, a more advanced gate driver is needed.

3.3 State-of-the-art advanced gate drivers

In this section, the focus will be on state-of-the-art gate drivers designed for SiC MOSFETs. However, some gate drivers originally designed for Si IGBTs will be presented as well, as the operation principle is similar.

The gate driver topologies can be categorized as either open loop or closed loop gate drivers. In open loop gate drivers the switching stages have been pre-calculated based on the known switching characteristics. The different stages is then chosen based on either timing or measurements from the circuit. Closed loop gate drivers however, actively changes the driving parameters based on measurement feedback.

3.3.1 Open loop gate drivers

Gate boost circuit

The gate driver topology presented in Figure (3.4) is termed gate boost circuit and presented in [6]. It aims to reduce the switching losses by increasing the switching speed, and to reduce the generated noise. The main part of the driver is a CGD. In addition, a new stage is added both for turn-on and turn-off. The turn-off path, with the boost capacitor, will not be explained in details as it is similar to the RC driver.

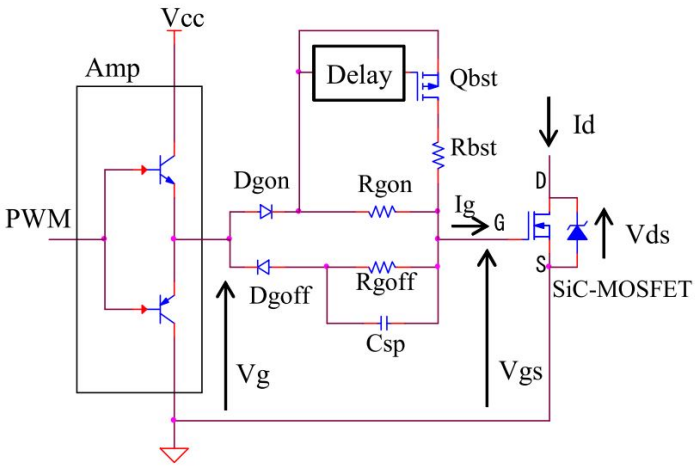


Figure 3.4: The gate boost circuit, proposed in [6].

For turn-on, the amplifier provides a high driving voltage, V_{cc}, and the current starts to charge the gate capacitance of the SiC MOSFET, similar as for a CGD. The delay circuit is a low-pass filter that delays the high driving voltage signal to the gate of the boost MOSFET, Q_{bst}. The signal is delayd until the SiC MOSFET has reached the voltage commutation, dv/dt. With R_{bst} lower than R_{gon}, the path through the boost MOSFET and R_{bst} provides a low resistive path for current to flow. The result is a high, boosting current that will give a faster dv/dt, lowering the switching time and the switching losses.

The challenge with the gate boost driver is the timing of the delay circuit. As the gate driver wants to act on the voltage commutation, it depends on the Miller plateau which varies with load current and junction temperature. Also [32] concludes that the timing of the delay circuit is vital to realize a good performance for the gate boost circuit.

A gate driver with a similar driving strategy as for turn-on of the gate boost circuit is presented in [45]. It aims to reduce the delay times in addition to increasing dv/dt. However, it is designed with logical circuits for operation of IGBTs. If it is suitable for WBG devices is not verified.

Stage-wise gate driver

The stage-wise gate driver, shown in Figure (3.5), is proposed in [7]. The driver provides three different stages for the different parts of the switching transient during turn-on and turn-off. In each stage the gate resistance is changed. Timing for the different stages is controlled by a FPGA. A similar driver topology is presented in [46] where the timing is based on data sheet values. The paper also presents waveforms for converter output when driving a motor load at 100 kHz and fixed dead time. Other proposals with fewer or more resistors exists as well. For instance in [47] where the resistors are divided into a main and a secondary driver with 2^8 and 2^6 different levels respectively.

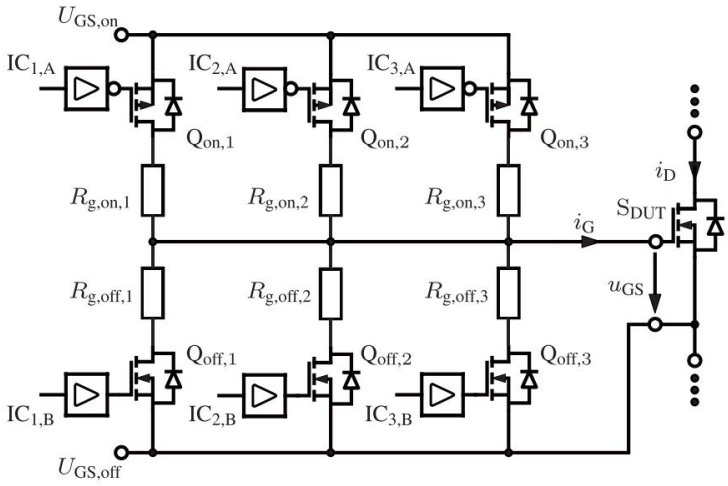


Figure 3.5: The Stage-Wise Gate Driver, proposed in [7].

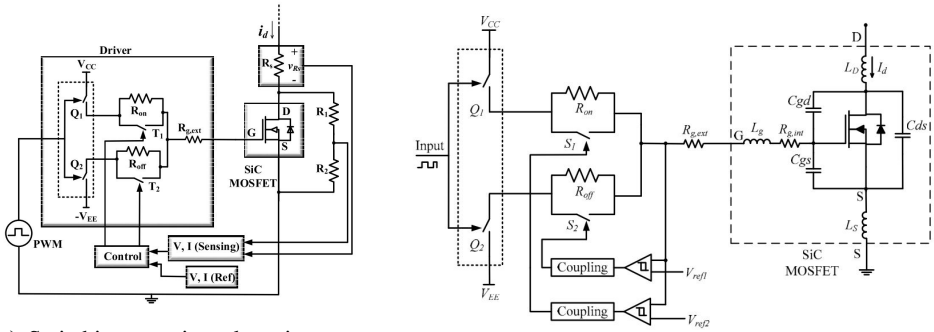
For the driver in Figure (3.5), to reduce the delay time, all three current paths are active during the first period of the switching transient. This provides the lowest possible gate resistance. This is common for both turn-on and turn-off. For turn-on, only one path is active in the next stage during di/dt, giving a high gate resistance. During dv/dt a slightly lower gate resistance is preferred and two paths are therefore active.

The gate signals for the different paths in the stage-wise gate driver is generated in a FPGA. As the SiC MOSFET switches very fast, a very high resolution is needed in the

timing. The author states that a resolution down to 1 ns is needed, while the chosen FPGA has a clock frequency of 300 MHz which only gives a resolution of 3.33 ns. Compensation techniques are used, but the timing is still the main issue.

Active two stage gate driver

The active two stage gate driver is shown in Figure (3.6a) and (3.6b). The drivers are identical, but utilizes different feedback strategies. The left proposal, presented in [48], utilizes measurements from the power circuit. The right proposal however, utilizes measurements of the gate voltage. It is presented in [49] and [50].



(a) Switching transient detection, presented in [48].

(b) Gate voltage detection, presented in [49].

Figure 3.6: Active two stage gate driver.

The driver strategy is similar to the one of a CGD, but with possibility to change the gate resistor depending on the switching transient, similar to the stage-wise driver. As seen in Figure (3.6), the equivalent gate resistor can have two different values when the switches, S1 and S2 (in Figure (3.6b)), are either on or off. The authors suggest to use the low resistor value to reduce the delay time and to increase di/dt. Then, the switch is turned off to provide a higher equivalent gate resistance during dv/dt to slow it down.

To know when to increase the gate resistor value, two different detection methods are used. In [48], the drain current and drain-source voltage is sensed. For turn-on, when the drain current reaches a reference point, the switch T1 is turned off. For turn-off, T2 is turned off when the drain-source voltage reaches a reference value. The ideal behaviour would be to increase the gate resistance exactly when dv/dt or di/dt is over. However, due to time delays in the detection circuit, the reference values is set a bit lower to compensate. In [49] and [50], it is the gate-source voltage that is sensed and compared with reference values. Also here, the reference values are set to compensate the time delays in the control loop.

The gate driver suffers from the challenges regarding the load current and junction temperature dependency on the switching transients. The gate driver is designed for one specific load current and operation with varying load parameters have not been presented. For an industrial application, the reference values must therefore be set for worst case operation point which will result in an overall decrease in performance.

Open-loop gate control

A gate driver topology for controlling dv/dt and di/dt independently during turn-on for SiC MOSFETs is presented in [8]. Due to the fast switching transients of SiC, the gate driver is designed as an open loop. The topology is shown in Figure (3.7).

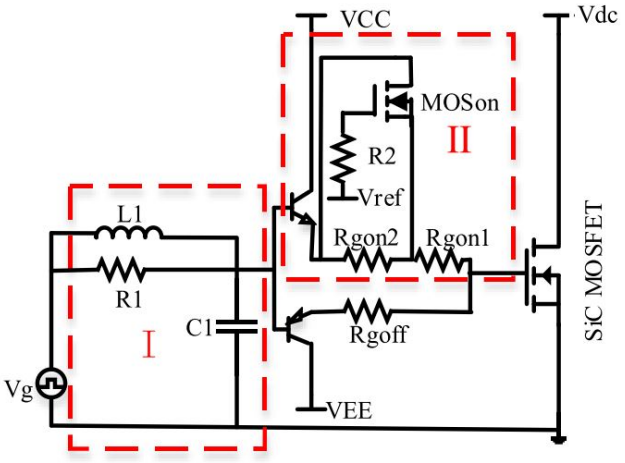


Figure 3.7: Open-loop gate control, presented in [8].

In the gate driver structure, Part I charges the capacitor C_1. During the delay time and the di/dt, MOSon in Part II is open. As R_{gon1} is low, this means that the gate-source voltage of the SiC MOSFET will follow the the voltage across C_1. Hence, di/dt can be controlled by properly choosing R_1, L_1 and C_1.

When the gate-source voltage reaches the miller plateau, the voltage difference between the gate-source voltage of the SiC MOSFET and the voltage across C_1 will increase as the charging of C_1 continues. This gives a larger gate current that will speed up dv/dt. However, before the voltage commutation is over, MOSon should be turned off, forcing the gate current to go through the large R_{gon2} instead. This reduces the last part of dv/dt, which will reduce the oscillations.

The gate driver is validated experimentally using a double pulse test in a setup with 450 V DC-link voltage. The gate driver provided a falling time for the drain-source voltage of 48.52 ns during turn-on. Furthermore, compared to CGD, both lower switching losses and lower overshoots is achieved. However, the operation is depending on the reference voltage chosen for MOSon, as this decides when MOSon is turned off. As the miller plateau will vary depending on the load current, the performance will be sensitive for load variations.

Voltage controlled active gate driver

The voltage controlled active gate driver (AGD), presented in [9], is shown in Figure (3.8). The idea behind is that it should have three voltage levels instead of two (high and low). It is originally proposed for Si IGBTs using Si diodes in anti-parallel. During turn-on, the

middle voltage level is introduced during di/dt to reduce the reverse recovery overshoot. During turn-off the middle voltage level was used to reduce dv/dt in order to reduce the oscillations in drain-source voltage [9].

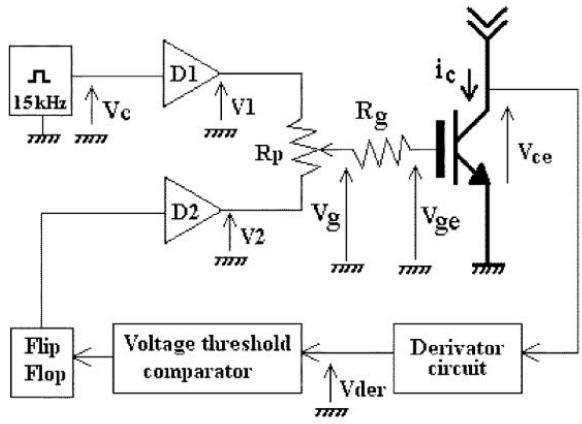


Figure 3.8: Voltage controlled AGD, proposed in [9].

To know when the different stages of the switching transient occurs, the authors suggests to detect the voltage commutation by a derivative circuit and use the results to turn on or off the middle voltage level. Experimental validation is also presented. However, since the gate driver is designed for Si IGBTs which switches slower than SiC MOSFETs, the detection of the switching events is challenging and must be verified if the driver should be used for SiC MOSFETs.

Still, the principle of controlling the driving voltage could be utilized for SiC MOSFETs. This is for instance done in [51] where the gate voltage is changed to slow down the switching transient. After the switching transient, the gate voltage is restored to its nominal value to turn the MOSFET either completely on or off. This is done using an analog feedforward controller. The rest of the control structure is built completely by analog devices as well to avoid delay times from digital to analog converters. The drawback however, is once again that there is no feedback to the controller so that the gate voltage is restored to its nominal value based on timing which makes the driver sensitive for changes in operation parameters.

Timing based active gate driver

The gate driver concept shown in Figure (3.9) is presented in [10]. The driver aims to reduce the voltage and current overshoot during turn-on and turn-off to allow operation with higher load currents and higher DC link voltages.

The operation principle of the driver is to provide an external current path both for turn-on and turn-off. This external current path reduces the gate resistance thus speeding up delay times and commutation rates. For turn-on, the MOSFET P-MOS is turned on for the first part of the switching transient to speed up the turn-on delay time and di/dt. However,

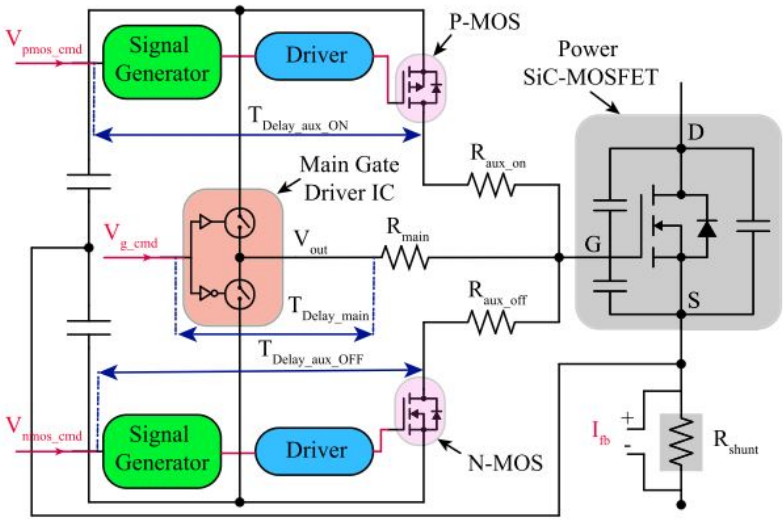


Figure 3.9: Timing based active gate driver, proposed in [10].

it is turned off early enough to reduce the current overshoot. Similar for turn-off, N-MOS is turned on to give a lower gate resistance during the first part of the switching transient hence speeding up the turn-off delay time and dv/dt.

Setting the proper intervals for when P-MOS and N-MOS is turned on is done by measuring load current and temperature. As the switching speed is high, the load current is assumed to be almost constant over a period for the carrier wave. Hence, the time intervals for the gate resistors is calculated and used in the next switching cycle. This way, fast feedback loops that track di/dt or dv/dt are avoided.

3.3.2 Closed-loop gate drivers

Closed-loop dynamic gate driver

An advanced closed-loop gate driver is presented by Lobsieger in [11] and [52]. The schematic diagram is shown in Figure (3.10) and utilizes a PI controller to provide the preferred slope rates for voltage and current commutations.

The reference value, $V_{ref,d/dt}$, is calculated to obtain a certain commutation slope, both for drain current and drain-source voltage. Feedback from the power loop is provided through a derivative circuit. For dv/dt feedback, measurements of the drain-source voltage is done. For di/dt feedback, the measurements are done across the known parasitic emitter inductance. This measurement strategy is utilized in [45] as well. The measurement signals are compared to the reference values and the error given to a PI controller that controls the gate voltage. To ensure a high bandwidth, all circuits are made analog.

The gate driver is able to control delay time, di/dt and dv/dt independently. However, it is made for Si IGBTs and the experimental validation provided in [11] shows switching

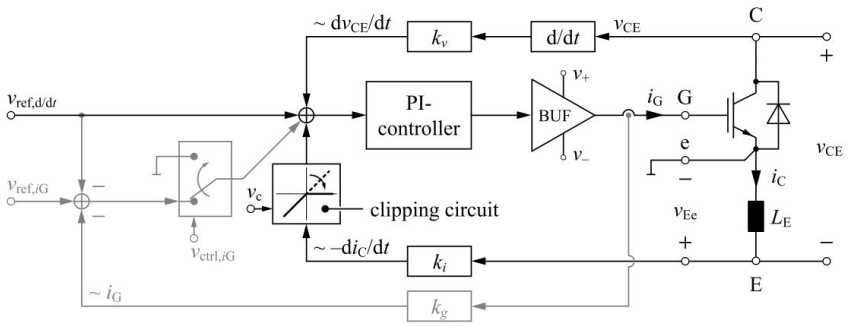


Figure 3.10: Closed-loop dynamic gate driver, proposed in [11].

speeds of maximum 2V/ns. For WBG devices this is considered slow and faster operation needs to be verified if the gate driver should be used for WGB devices such as SiC MOSFETs.

Closed-loop gate current control

A closed-loop gate driver design for SiC MOSFETs is presented in [12]. The schematic diagram is shown in Figure (3.11). The concept is similar to the closed-loop concept by Lobsieger. However, instead of providing feedback from the drain-source voltage and drain current, the feedback loop is related to the gate-source voltage.

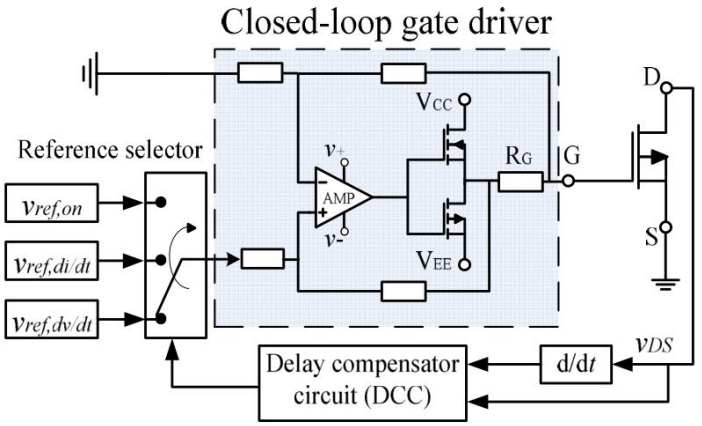


Figure 3.11: Closed-loop gate driver for SiC MOSFETs, presented in [12].

The reference voltages for di/dt and dv/dt is calculated to obtain the desired commutation rates. A delay compensation circuit that estimates the beginning of each stage in the switching transient determines which reference voltage to be used. This increases the bandwidth compared to detecting the actual di/dt and dv/dt due to the time delays in the

feedback loop. However, the reportet switching speed is limited to 4 V/ns, which is in the same range as for Si IGBTs.

A slightly different approach for closed-loop feedback is presented in [13]. The schematic diagram is shown in Figure(3.12). While the main part of the gate current is provided by a conventional gate driver, an IC is designed to detect dv/dt over the switch. The IC can act as a sink or source to slow down dv/dt to the desired value. This way neither the delay times nor di/dt are affected by the IC. The IC does not need to be designed for full gate current either, hence delay times can be reduced. Delay times for the IC lower than 200 ps are reported as well as dv/dt values in the range 6-15 V/ns.

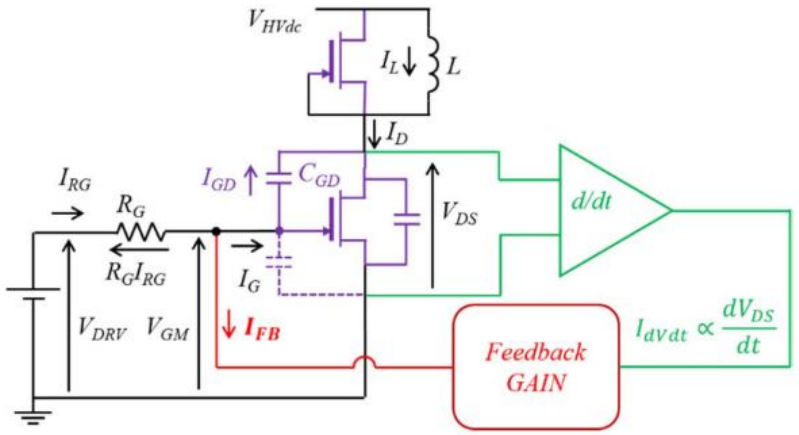


Figure 3.12: Closed-loop gate driver for GaN HEMT, presented in [13].

Gate current controlling gate drivers

Instead of controlling either the resistance in the gate driver or the driving voltage, some authors propose to act directly on the gate current. For instance in [14] an advanced gate current source is created to control a Si power MOSFET in a best possible way. The driving principle is shown in Figure (3.13). The gate driver is programmed into a microchip and closed-loop control is achieved by detecting the different intervals from measurements of drain-source, gate-source and the driving voltages. If the feedback is fast enough to control WBG devices is not verified.

A gate current controlling gate driver designed for SiC MOSFETs are presented in [53]. The goal is to reduce overshoots and ringing during fast switching of freewheeling devices. This is done by closed-loop control which is achieved through di/dt feedback based on parasitic source inductance, similar to what is presented for the closed-loop dynamic gate driver. All measurement circuits have been made analog to ensure high bandwidth, and the performance is validated through lab work.

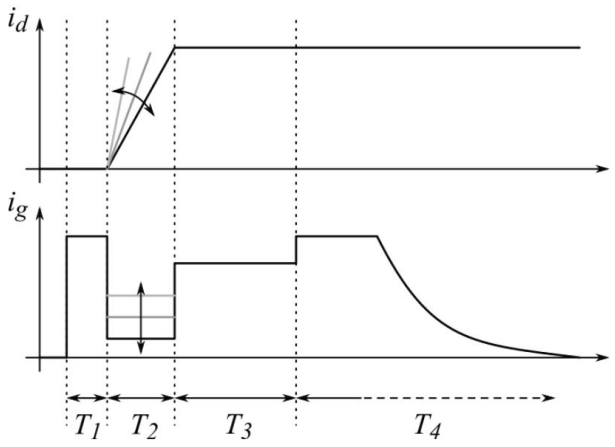


Figure 3.13: Principle of gate current control. Taken from [14].

3.4 Multistage driver

A new gate driver topology designed for SiC MOSFETs, termed the multistage driver, is shown in Figure (3.14). The multistage driver targets delay time minimization both for turn-on switching transients and turn-off switching transients. It was first presented in [54], but was also presented in the specialization project where both simulation and lab results were presented [1].

The driver is an open loop two-stage driver with a conventional stage, similar to the CGD, and a boosting stage with boost voltages V_{pos2} for turn-on and V_{neg2} for turn-off. The operational principle is that for a turn-on or turn-off event, the MOSFET in the boosting stage of the driver $M_{b,***}$ will be turned on quickly as their gates are charged by the capacitors $C_{b,***}$ which act as high pass filters. This provides a low resistive path from the boost voltage to the gate through $R_{b,on}$ or $R_{b,off}$ which allows for a large initial gate current that will charge or discharge the gate faster. Hence, similarly as for the RC-driver, the delay times are reduced as shown in Figure (3.3) for turn-on transients.

The diodes, D_1 and D_2 are inserted to turn the boosting stage off. For turn-off, diode D_2 will become reverse biased when the gate voltage equals V_{neg2} thus closing the current path for the boost current. The rest of the switching transient is then controlled by the conventional part. By choosing V_{neg2} equal to the Miller plateau, the best possible reduction in turn-off delay time can be achieved without changing dv/dt. For turn-on transients, the diode, D_1, will become reverse biased when the gate voltage equals V_{pos2}. Hence, by choosing V_{pos2} so that D_1 blocks when the gate is at the threshold voltage, the best possible reduction in turn-on delay time is achieved without affecting di/dt.

Due to the diodes D_1 and D_2, the multistage driver can be considered to be voltage controlled. As long as the boost voltages are properly chosen, this is considered to be more robust than controlling the driver by timing due to manufacturing tolerances of passive components.

The operation principles of the multistage driver and the RC driver are quite similar.

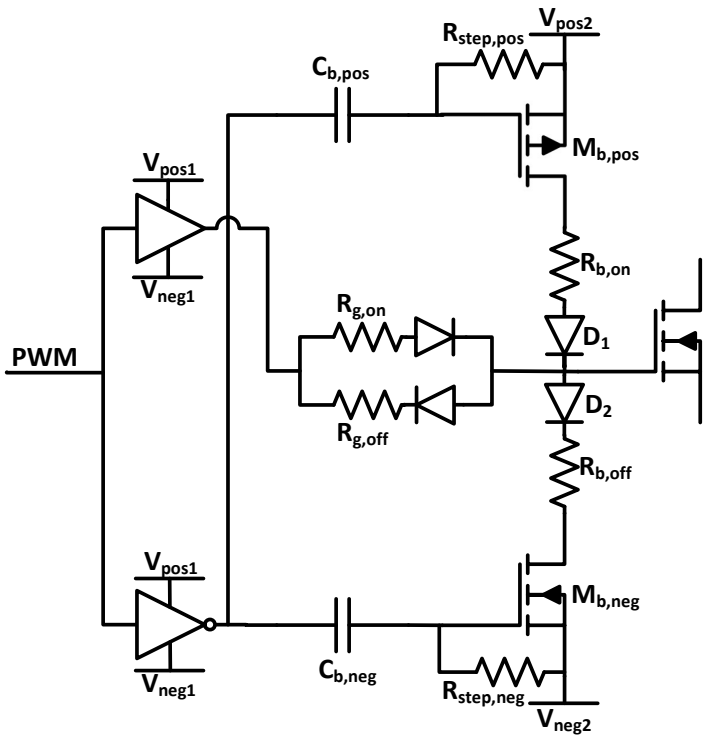


Figure 3.14: Schmatic diagram of the multistage driver.

However, the boost capacitor in the RC driver is fixed and must be tuned for the worst-case operating point. For the multistage driver on the other hand, V_{pos2} and V_{neg2} can be chosen to be optimal at each operation point, thus, reducing the effect of load current and junction temperature dependent delay times. Yet, choosing optimal boost voltages based on the operation point requires measurements and functionality that allows the boost voltages to be changed dynamically. If such functionality is not implemented, V_{pos2} and V_{neg2} must be fixed and the tuning must similarly be done for the worst-case operation point.

Chapter 4

Improved SPICE model of SiC MOSFET

This chapter investigates the SPICE model for the SiC MOSFET that is used in simulations for transient analysis. In the specialization project, the non-continuity in the transfer curve of this model was highlighted. This non-continuity gives convergence errors and results that deviate from observations in lab. Possible improvements of the model are therefore investigated.

Section 4.1 is taken from the specialization project and modified slightly [1]. The rest of this chapter is work that is done for this master thesis and used in the abstract that is submitted to ICSCRM2019. The abstract can be found in Appendix A.2.

4.1 SPICE modeling

The transient behaviour is of interest when simulating the behaviour of gate drivers and the impact they have on the switching waveforms. A simulation tool that solves non-linear equations and that can provide detailed transient behaviour of the semiconductor components is needed.

The industry-standard when evaluating circuit designs is to use the open source simulation tool SPICE (Simulation Program with Integrated Circuit Emphasis) [55]. SPICE models offer precise and fast run-time simulations which includes parasitic properties such as resistors, capacitors and inductors. A power MOSFET model is shown in Figure (4.1). The model is presented in [15], where a SPICE model is built based on a datasheet and validated experimentally with good precision. Rather than building the models selves, many manufacturers offer SPICE models for their products. This allows for testing in simulations before buying the actual component. This gives the opportunity to make more qualified decisions when choosing components.

The program used for SPICE simulations in this master thesis is the free program LTspice by Analog Devices [56]. The program comes with a lot of built-in models, both

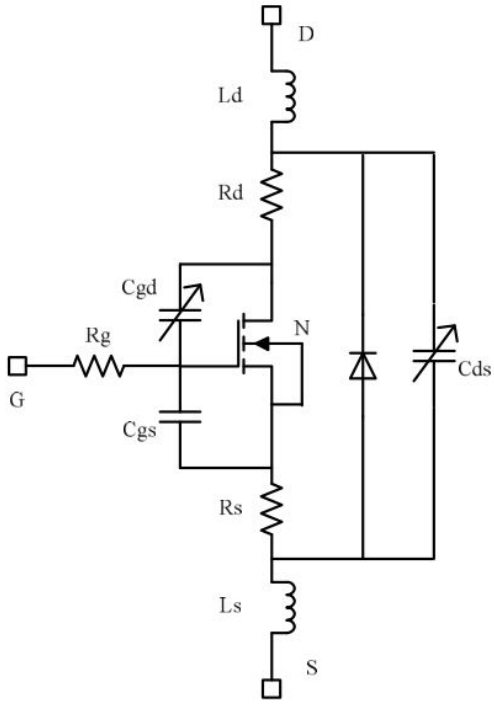


Figure 4.1: Power MOSFET model including parasitics, presented in [15].

ideal models and commercially available models from different manufacturers. Building circuits is straight forward and the program offers a lot of different possibilities to evaluate the simulation results.

4.2 Initial model

The SiC MOSFET chosen for lab-work in this master thesis is the C3M0075120K by Wolfspeed (CREE) which has ratings 1.2 kV and 30 A [2]. Wolfspeed offer SPICE models for all their products. Therefore, to get as precise results as possible, the model offered for C3M0075120K [57] is used in the simulations related to the work.

4.2.1 Convergence error

The LTspice model provided by Wolfspeed has some drawbacks. During simulations with different gate drivers, the model often have convergence problems when using default simulation settings. The problem increases if the gate resistor in the gate driver is chosen to have a large value to slow down the commutation slopes of the MOSFET.

It is not adviced to change the default tolerance settings in LTspice. However, to be

Table 4.1: Key tolerances parameters in LTspice.

Keyword	Description	LTspice default	Used value
gmin	Conductivity added to PN junction	1e-10	1e-6
abstol	Current error tolerance	1e-10	1e-5
reltol	Relative error tolerance	0.001	0.5
vntol	Voltage error tolerance	1e-6	1e-1
chgtol	Absolute charge tolerance	1e-14	1e-6

able to run the simulations without having problems with convergence, the tolerances for the simulation case have been edited as shown in Table (4.1).

With high tolerances in the simulation, the validity of the simulation result decreases. It is therefore not in neither the designers nor the manufacturers interest to allow high tolerances.

To target the reason behind the convergence errors, the transconductance of the MOSFET model have been investigated. Rewriting Equation (2.5) into Equation (4.1) shows that the transconductance is given by the derivative of drain current with respect to gate-source voltage.

$$g_m = \frac{\partial i_d}{\partial V_{gs}} \tag{4.1}$$

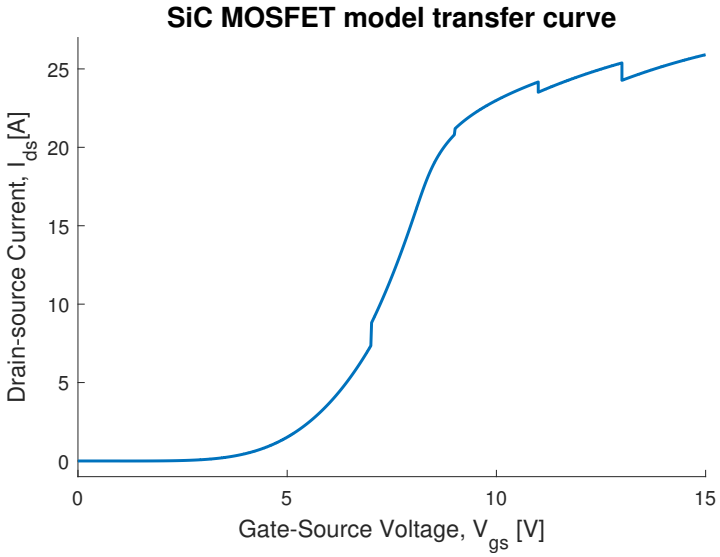
The transconductance is both junction temperature and gate-source voltage dependent. To investigate it in LTspice, a sweep in gate-source voltage from 0 to 15 V have been done as shown in Figure (4.2). In the sweep, a constant voltage source of 20V with a series resistance of 0.7 Ω have been connected to the drain-source connections of the MOSFET. The junction and case temperatures have been held constant at 25°C. Figure (4.2a) shows the drain current response as a function of gate-source voltage and Figure (4.2b) shows the derivative of the drain current with respect to the gate-source voltage, i.e. the transconductance.

Figure (4.2a) shows that the current commutation in the SPICE model is non-continuous at gate-source voltages 7 V, 9 V, 11 V, and 13 V. In addition to the non-continuous behaviour, the transconductance jumps from 4.5 A/V to 5.5 A/V when the gate-source voltage passes 7 V. This means that the current commutation slope changes rapidly which can influence parasitics in the circuit. This piecewise behaviour of the drain current, especially at 7 V gate-source voltage, have caused the convergence errors in simulations. Improvements to the tranceconductance of the model have therefore been investigated.

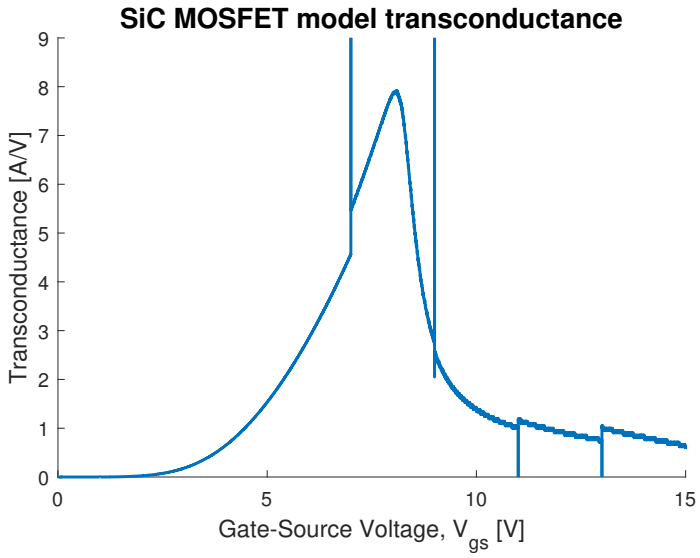
4.2.2 Initial SPICE model

The circuit diagram for the internal structure of the SiC MOSFET SPICE model is visually presented in Figure (4.3). The model have been drawn based on the SPICE code of the LTspice model. The model contains both an electrical part and a thermal part.

The electrical part of the model is connected to the rest of the simulation circuit by two source connections (Kelvin connection), drain and gate. In addition there are two connection points for the thermal part of the model, one for case temperature and one for junction



(a) Transfer curve obtained from LTspice simulations with initial model.



(b) Transconductance obtained from LTspice simulations with initial model.

Figure 4.2: Initial LTspice model.

temperature. For the model to run, at least one of the temperature connections must indirectly be connected to a source while the other one can be used to read out the temperature. A typical setup is to connect the case temperature to match the ambient temperature so that the expected junction temperature can be read. The temperature connections can also be

used to design heat sinks in some applications.

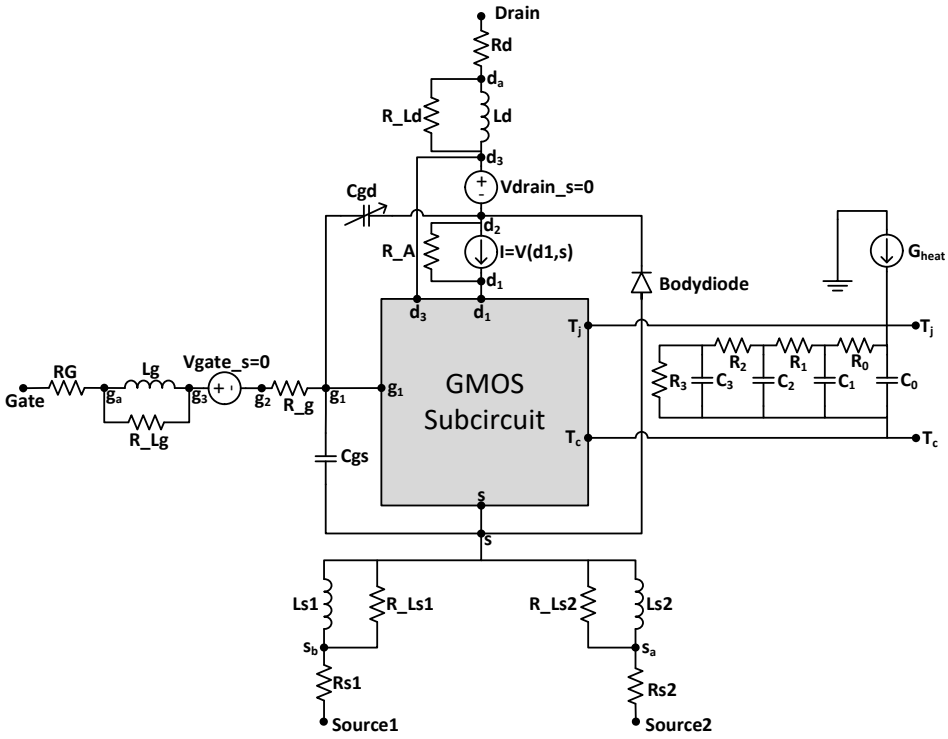


Figure 4.3: LTspice MOSFET model visually represented.

In the electrical part of the model, parasitic inductors and resistors are included at all connection points. The internal gate resistance R_g and the parasitic gate resistance RG are included as well as separate resistor blocks. The gate-source capacitance is modelled as a constant capacitor, Cgs. For the gate-drain capacitance (Miller capacitance) however, it is modelled as a variable current source based on the voltage difference between the nodes d_2 and g_1. This is done in a separate subcircuit that is not investigated further in this master thesis. The antiparallel body diode is modelled with constant parameters, assuming a gate-source voltage of -4 V [57].

As seen from Figure (4.3), constant voltage sources are included in both the gate and the drain arm. Their value is set to zero as the blocks are only used for current measurements. This is common in LTspice simulations.

The inner and outer part of the MOSFET model is connected through nodes g_1, d_1, d_3, s, T_j and T_c. The inner part (GMOS Subcircuit) is illustrated in Figure (4.4). It is modelled as two dependent current sources, G1 and G2, where G1 is active for negative drain-source voltages, while G2 is active for positive drain-source voltages. It is this inner part that decides the transfer characteristics of the SiC MOSFET.

In the GMOS subcircuit in Figure (4.4), the function of node g_2 is to limit the gate-source voltage that is used in the equations within a valid range. As long as the input

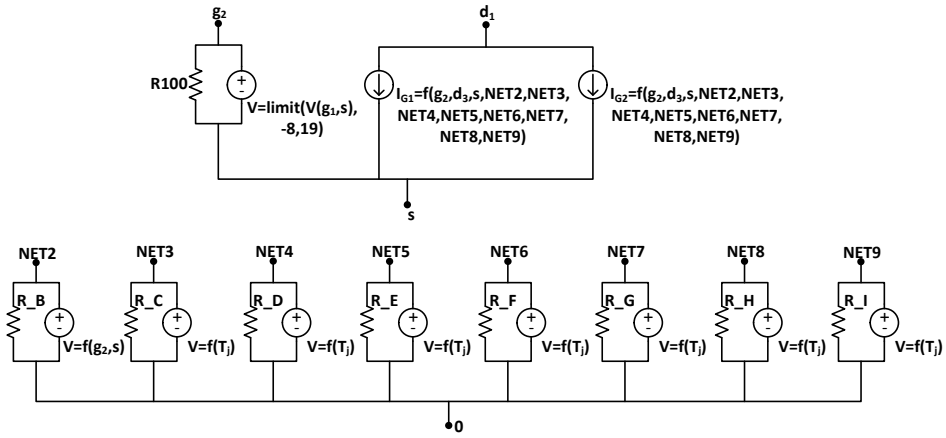


Figure 4.4: Inner part of the LTspice MOSFET model (GMOS Subcircuit).

gate-source voltage (between $g1$ and s) is between -8 V and +19 V, the voltage level in g_2 equals the voltage level in g_1. However, for higher input gate-source voltages than +19 V or lower than -8 V, the voltage level in node g_2 is limited by the range. It is the voltage between g_2 and s that is used as the gate-source voltage in the model equations.

The nodes NET2 to NET9 are connected to variable voltage sources as seen in Figure (4.4). The voltage at node NET2, V_{NET2}, is gate-source voltage dependent while the voltage at nodes NET3 to NET9 depends on junction temperature. As for the g_2 node, all the NET nodes are dummy nodes where the voltage is used in the equations for the variable current sources G1 and G2. As the voltages at the nodes changes with different gate-source voltages and junction temperatures, they provide the dynamic behaviour of the MOSFET model in terms of gate-source and junction temperature dependency.

The equations for G1 and G2 are based on the Enz-Krummenacher-Vittoz (EKV) MOSFET model which provides the possibility to model the MOSFET behaviour over different inversion regions with one equation [58, 59]. The modified EKV model is presented in Equation (4.2), where ϕ_t is the thermal voltage, g_m is the transconductance parameter, K_s is the sub-threshold slope parameter, λ is the channel length modulation parameter, k is the law exponent, and n and a is the triode region parameters [60].

$$I_d = 2g_m\phi_t^2 K_s \left[ln\left(1 + e^{\frac{V_{gs}-V_{th}}{2K_s\phi_t}}\right)^k - ln\left(1 + e^{\frac{V_{gs}-V_{th}-nV_{DS}^a}{2K_s\phi_t}}\right)^k \right] (1 + \lambda V_{DS}) \quad (4.2)$$

The thermal voltage is given by Equation (4.3), where k_B is the Boltzmann constant, T is the absolute temperature and q is the magnitude of the electron charge.

$$\phi_t = \frac{k_B T}{q} \quad (4.3)$$

The equation used to model G1 and G2 in the initial model by Wolfspeed is given in Equation (4.4).

$$I_d = ((V_{NET5} + V_{NET6} + V_{NET7} + V_{NET8} + V_{NET9}) * (V_{g2,s} - V_{NET3})) + V_{NET4}) * \left[ln\left(1 + e^{V_{g2,s} - V_{NET3}}\right)^2 - ln\left(1 + e^{V_{g2,s} - V_{NET3} - V_{NET2} * V_{d3,s}}\right)^2 \right] * (1 + 0.0011 V_{d3,s}) \quad (4.4)$$

By comparison of Equations (4.4) to (4.2) it is seen that V_{NET3} provides the threshold voltage. This is also confirmed by plotting the junction temperature dependency of V_{NET3} and compare it with the datasheet for the device. Moreover, V_{NET2} provides the triode region parameter n while triode region parameter a is set to unity. The law exponent k has value 2, while the sub-threshold slope parameter λ has value 0.0011. From the exponents inside the logarithmic functions it is seen that $2K_s\phi_t = 1$. Inserting this into the first part of Equation (4.2) and comparing to Equation (4.4) yields the equality in Equation (4.5).

$$((V_{NET5} + V_{NET6} + V_{NET7} + V_{NET8} + V_{NET9}) * (V_{g2,s} - V_{NET3})) + V_{NET4}) = g_m \phi_t \quad (4.5)$$

In Equation (4.5), the voltages at nodes NET5 to NET9 occur as the sum of the voltages. However, for gate-source voltages in the range from 1 V to 15 V, only one node has a non-zero voltage at any given time. Outside the range, all nodes have zero voltage. Hence, since ϕ_t, V_{NET3} and V_{NET4} are junction temperature dependent, the voltage levels in nodes NET5 to NET9 shapes the transconductance according to its gate-source voltage dependency. For gate-source voltages between 13 V and 15 V, node NET5 is non-zero. For gate-source voltages between 11 V and 13 V, node NET6 is non-zero, NET7 is non-zero for gate-source voltages between 9 V and 11 V, NET8 for gate-source voltages between 7 V and 9 V, and NET9 is the node that is non-zero for gate-source voltages between 1 V and 7 V. The sum of the node voltages is plotted in Figure (4.5).

Over each gate-source voltage interval, the voltage at each of the nodes in NET5 to NET9 is a constant that depends on the junction temperature. However, in the breaking points, the sum of the node voltages becomes non-continuous thus giving a non-continuous transconductance. These breaking points are at the same gate-source voltages that was highlighted in Figure (4.2), thus they are the reason for the non-continuous behaviour of the initial model. The drain current, given from Equation (4.4) for a positive drain-source voltage of 20 V, is shown in Figure (4.6). Also here, the non-continuous behaviour of the transconductance and the junction temperature dependency is visible.

4.3 Proposed model

To improve the SPICE model for the SiC MOSFET, the transconductance and transfer curve must be made continuous both for different gate-source voltages and for different junction temperatures. At the same time, the model must provide the same steady-state characteristics and the same temperature dependency as the initial model.

By investigating the voltages at nodes NET5 to NET9 in the original model that was shown in Figure (4.5), it is seen that both the maximum point and the amplitude changes

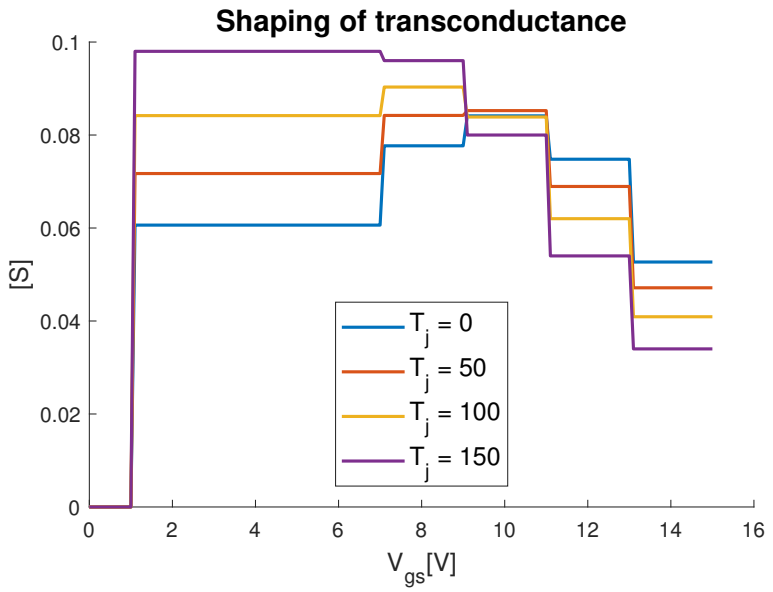


Figure 4.5: Voltage level in nodes NET5 to NET9 as function of gate-source voltage. The voltage levels are shaping the transconductance of the device.

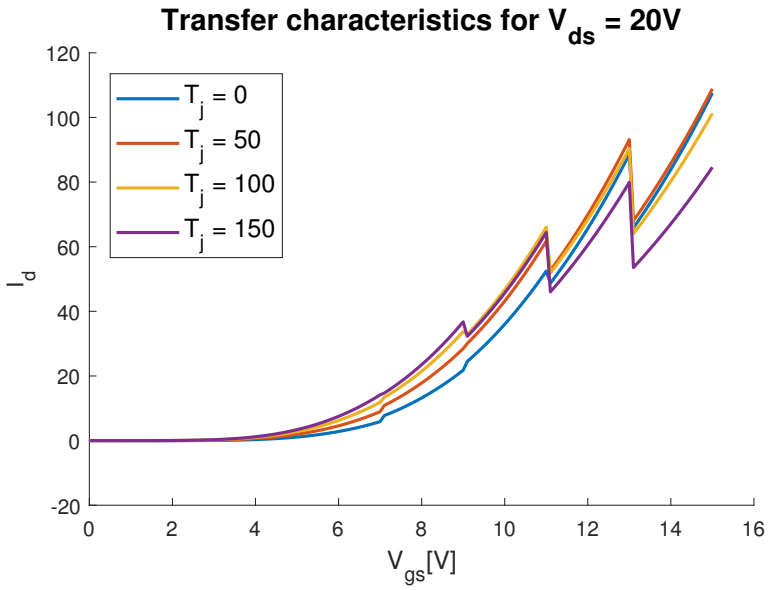


Figure 4.6: Initial LTspice MOSFET model transfer curve.

with junction temperature. As the junction temperature increases, the location of the max-

imum point moves towards zero gate-source voltage and the amplitude in the maximum point increases. This behaviour is similar to what can be expected by the Rayleigh distribution [61]. Therefore, the new model is inspired from this distribution.

The Rayleigh distribution is given by Equation (4.6).

$$f(x) = \frac{x}{\sigma^2} e^{-\frac{x^2}{2\sigma^2}}, x > 0 \tag{4.6}$$

In the equation, σ is the scale parameter that determines how the distribution is spread out. As the total area under the function is constant, σ determines where the maximum point is located. This can be shown by putting the derivative equal to 0, which gives that the maximum point is found at $x = \sigma$.

By using the function from the Rayleigh distribution in the MOSFET model, the maximum point can be made dependent on junction temperature by making σ dependent on junction temperature. Further, to ensure that the amplitude of the function becomes as equal to the initial model as possible, a scaling factor that also is dependent on the junction temperature is introduced. The result is shown in Equation (4.7), where $\alpha(T_j)$ is the amplitude scaling factor and $\sigma(T_j)$ is the scale parameter.

$$h(V_{gs}) = \alpha(T_j) \frac{V_{gs}}{\sigma(T_j)^2} e^{-\frac{V_{gs}2}{2\sigma(T_j)^2}}, V_{gs} > 0 \tag{4.7}$$

From inspection of Figure (4.5), it is seen that the location of the maximum point changes in the range from gate-source voltage 5 V to 10 V for junction temperatures in the range 0°C to 150°C. As the range for the maximum point is relatively short, it is assumed that a linear relationship between the location of the maximum point and the junction temperature can be used with good precision. Hence, $\sigma(T_j)$ is chosen to be a linear function on the form $aT_j + b$. For the amplitude scaling factor however, the relationship to junction temperature is modelled as a second order function on the form $a'X^2 + b'X + c'$.

To determine the constants in $\sigma(T_j)$, square error minimization have been used. The MATLAB code that is used is provided in Appendix B. The procedure was to iterate through multiple combinations of values for a and b. For each combination, the optimal value for $\alpha(T_j)$ have been found for temperatures in the range from 0°C to 150°C. The combination of a, b and $\alpha(T_j)$ that minimized the sum of square errors for all temperatures was stored as the best combination. The final function for $\sigma(T_j)$ is presented in Equation (4.8).

$$\sigma(T_j) = -0.021T_j + 9.5 \tag{4.8}$$

For the amplitude scaling factor, different amplitudes for different temperatures was found. They are plotted in Figure (4.7). As can be seen, the amplitude is estimated in a satisfactory manner by the second order function, which is found by fitting a trend curve to the points using Microsoft Excel. The final function for $\alpha(T_j)$ is presented in Equation (4.9).

$$\alpha(T_j) = 3 * 10^{-6} T_j^2 - 0.0017T_j + 1.2512 \tag{4.9}$$

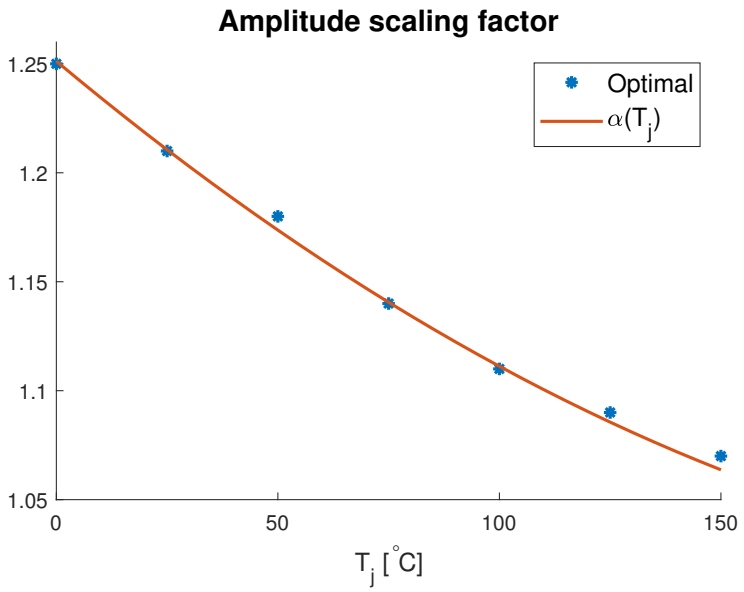


Figure 4.7: Calculated, optimal, values for α and $\alpha(T_j)$.

The Reyleigh distribution will not give an exact fit to the initial model. Therefore, the optimization with square error minimization have been done between gate-source voltages from 4 V to 12 V instead of between 0 V to 15 V as this gives a more precise model in the range for current and voltage commutations. If the model was intended for short-circuit analysis however, the model should be optimized for higher gate-source voltages than 12 V. For gate-source voltages below 4 V, the drain current in Figure (4.6) is seen to be very small and performance of the model is almost not affected by the transconductance. If too much focus is laid on minimizing the square error from 0 V to 4 V gate-source voltage, this will give a very fast initial raise in the transconductance model instead. This will further give an overshoot in the model that will be visible in the transfer curve by too high currents in the range between 5 V to 10 V gate-source voltage.

Comparison between the initial model and the proposed model is shown in Figure (4.8) and (4.9) for the function that shapes the transconductance and the transfer curve respectively. As seen from the figures, the proposed model is continuous and fits the initial model well.

4.4 Verification of proposed model

4.4.1 Experimental work

The reliability of the proposed model is verified by comparing the output characteristics and the transfer curves from both the proposed and the initial model to measurements done in lab.

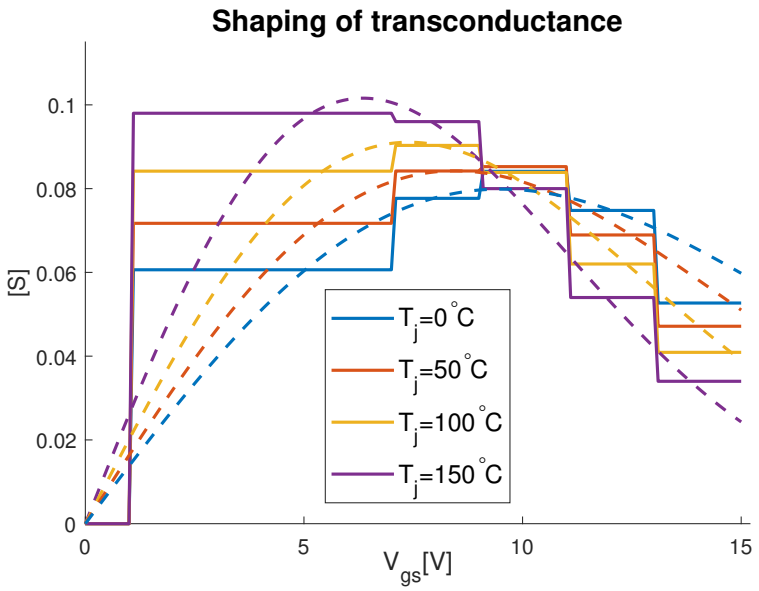


Figure 4.8: LTspice MOSFET model transconductance shaping. Dotted lines are the proposed model.

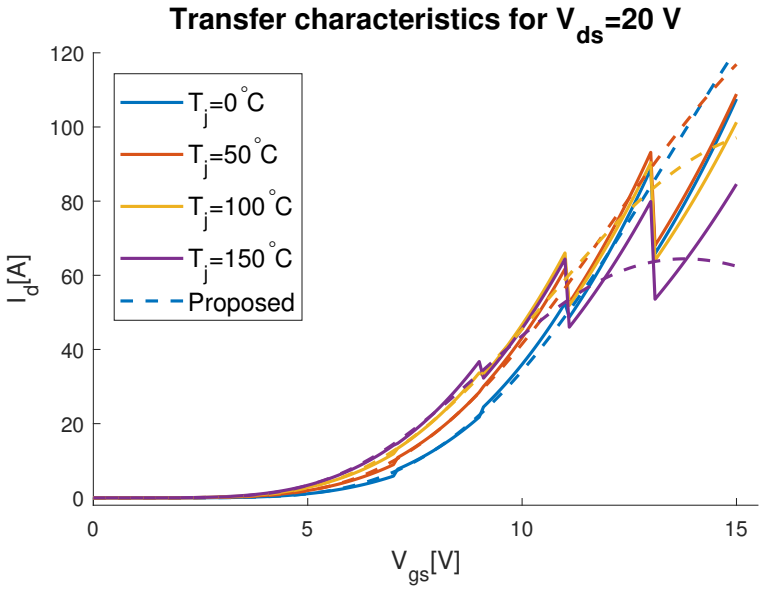
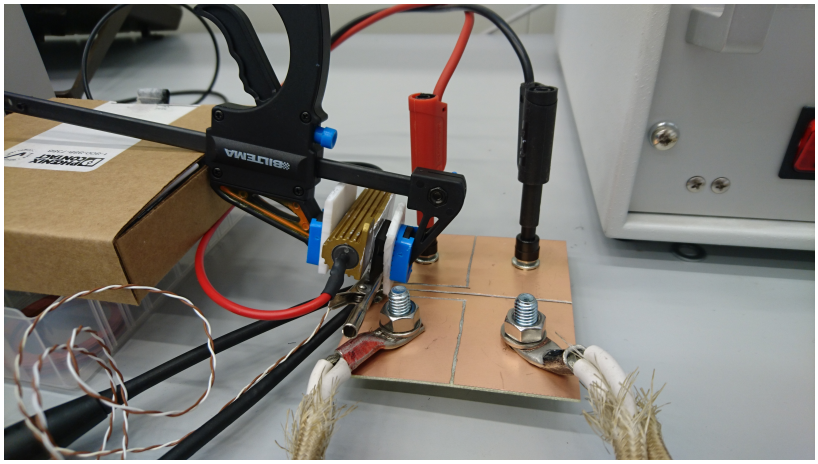
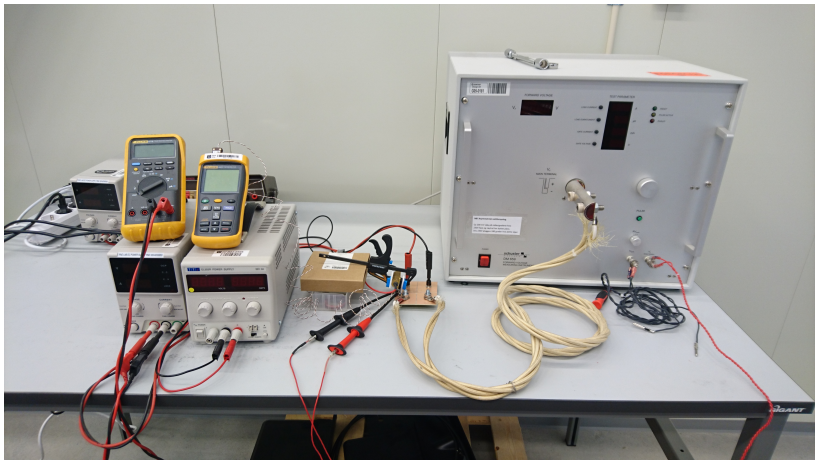


Figure 4.9: LTspice MOSFET model transfer curve. Dotted lines are proposed model.

The lab results are obtained using Schuster electronics DM659, which is a forward



(a) Test board.



(b) Test setup.

Figure 4.10: Laboratory setup for output characteristics measurements.

voltage measuring device. With the device, the gate-source voltage and the drain current that should be applied to the MOSFET are chosen. The DM659 then applies the gate-source voltage and pulses the current. Measurements of the forward voltage drop in the MOSFET are done as long as it does not reach the saturation voltage of 20 V. The pulse length can be adjusted in the range from 100 μs to 500 μs and the currents in the range from 1 A to 5000 A.

The setup is shown in Figure (4.10). In addition to the Schuster DM659, it contains a circuit board that allows for the MOSFET to be connected to the device. For temperature control, a heat dissipation resistor is clamped to the upper part of the drain metal on the backside of the SiC MOSFET (C3M0075120K). The heat is controlled by a DC source, and temperature measurements are done using a T-type thermocouple on the lower part of

the drain metal. As no heatsink is connected to the MOSFET and the tests are run by only using pulses, it is assumed that the measured temperature on the drain metal is equal to the junction temperature inside the MOSFET.

The output characteristics from lab are obtained by measurements at gate-source voltages from 4 V to 15 V. For each gate-source voltage, the forward voltage drop is measured for currents 1-7 A, 10 A, 12 A, 15 A, 17 A, 20 A, 22 A, 25 A, 27 A and 30 A. All the measurements are done at junction temperatures 25°C, 50°C, 75°C, 100°C and 125°C. The results are shown in Figures (4.11) to (4.15) together with the output characteristics provided by both the initial and the proposed model.

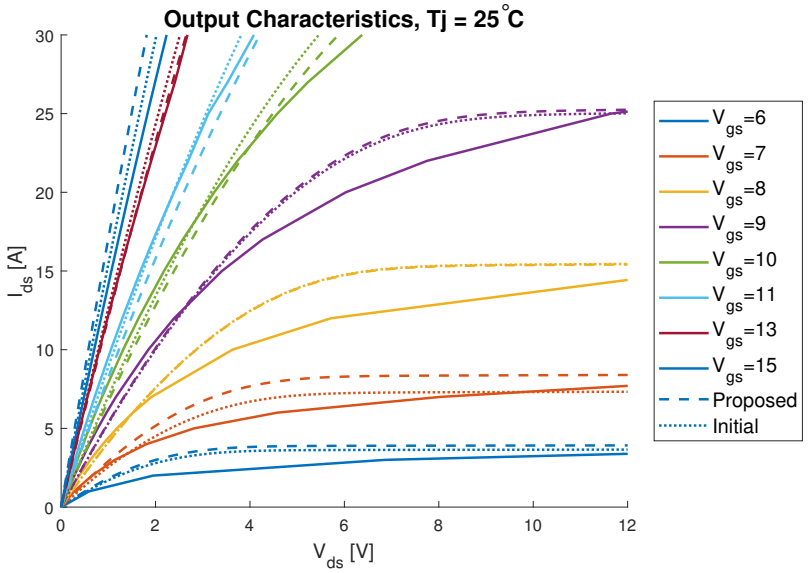


Figure 4.11: Output characteristics from initial and proposed model compared with measurements from lab at junction temperature 25°C.

The output characteristics from the two models are very similar for all junction temperatures. Moreover, results have good correlation with the output characteristics that is measured in lab. Actually, for high junction temperatures it seems like the proposed model is closer to the lab measurements than the initial model for gate-source voltages of 11 V, 13 V and 15 V. However, as the measurements that are done in lab are done for one single discrete component, the lab results does not provide the exact behaviour for all components of the same type. Still, the results indicated that the output characteristics from both the initial and proposed model are reliable.

Even though the output characteristics show that the models can be trusted at steady state, they do not show the dynamics during switching transients that previously caused convergence trouble. To do so, transfer curves are created as shown in Figure (4.16) and (4.17). In Figure (4.16) the initial model is compared to the transfer curve from lab while in Figure (4.17) the proposed model is compared. The curves for the two SPICE models are created by extracting the drain current equation from the internal GMOS subcircuit that

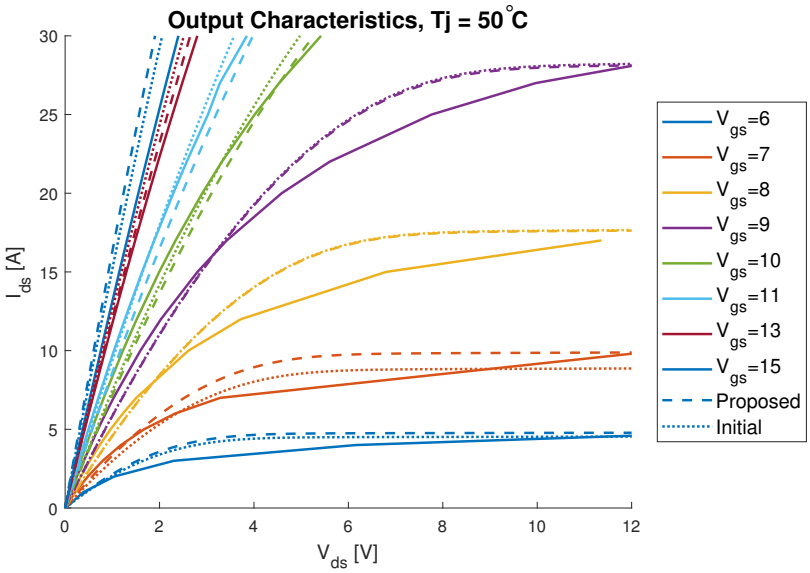


Figure 4.12: Output characteristics from initial and proposed model compared with measurements from lab at junction temperature 50°C.

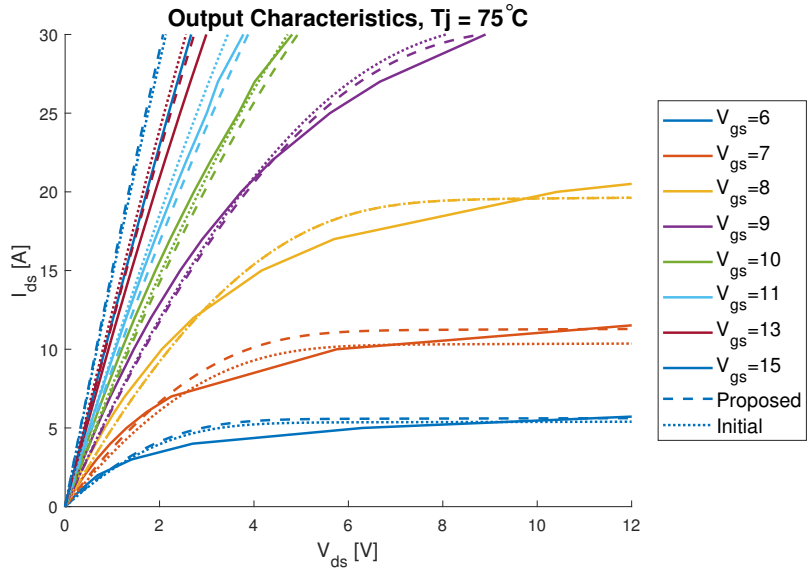


Figure 4.13: Output characteristics from initial and proposed model compared with measurements from lab at junction temperature 75°C.

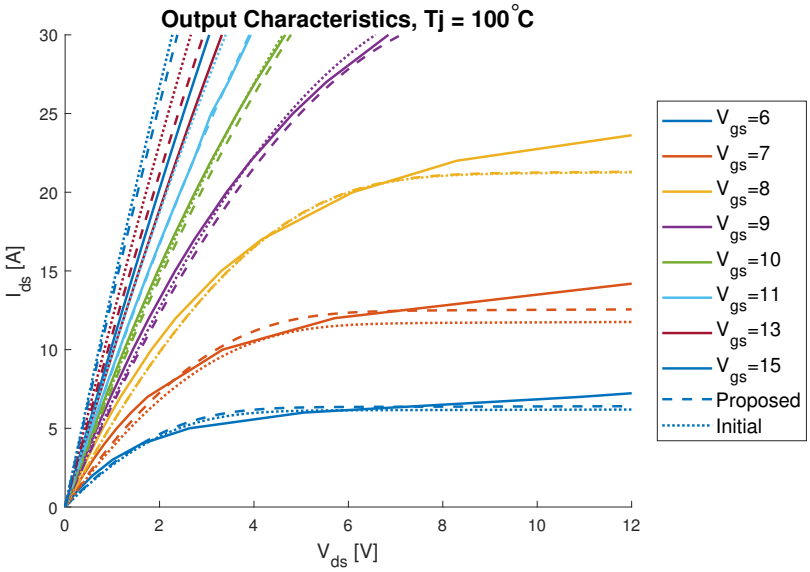


Figure 4.14: Output characteristics from initial and proposed model compared with measurements from lab at junction temperature 100°C.

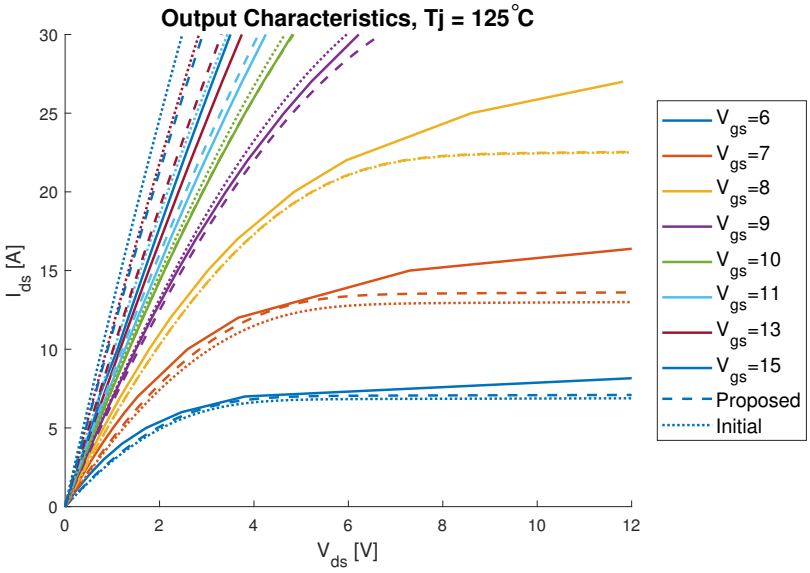


Figure 4.15: Output characteristics from initial and proposed model compared with measurements from lab at junction temperature 125°C.

was illustrated in Figure (4.4). The curves from lab are created by plotting the saturation current for each gate-source voltage. Due to the steps in drain current in lab, the resolution of the graphs are poor, especially in the region around 7 A to 10 A.

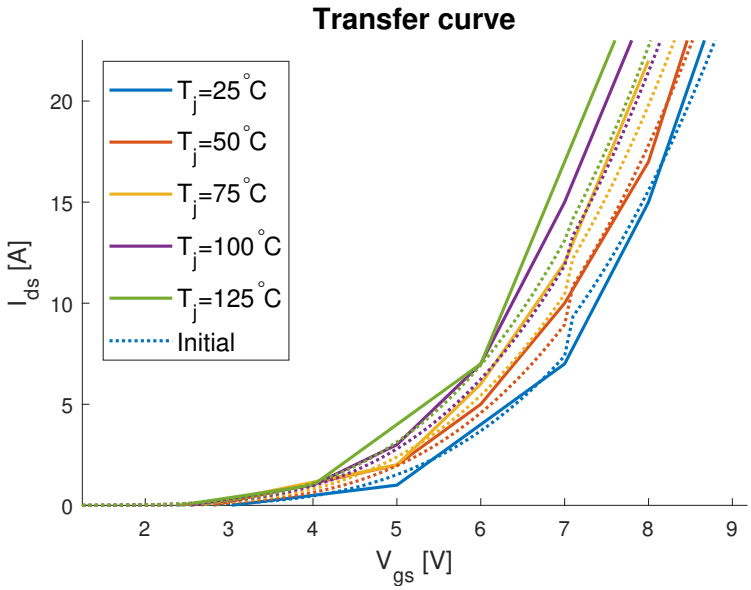


Figure 4.16: Comparison between transfer curve from lab and the initial simulation model.

In the transfer curves, both the initial and proposed model follows the results for the actual MOSFET for junction temperatures 25°C and 50°C. For higher temperatures however, both models deviated equally. The equal deviation is expected as the proposed model is created based on the initial model. The expected behaviour of the models are therefore similar. However, the non-continuous drain current that is present in the initial model at gate-source voltage 7 V is completely gone in the proposed model.

4.4.2 Simulations with proposed model

The Equations (4.7) to (4.9) have been implemented to the LTspice library file for the SiC MOSFET. In the proposed model, provided in Appendix B, the nodes NET5 to NET9 that was shown in Figure (4.4) are replaced with a new node, NET10, that includes the new transconductance shaping equation.

Figure (4.18) shows a sweep in gate-source voltage similar what was presented in Figure (4.2). The orange lines are obtained with the proposed model while the blue line is the same as in Figure (4.2) for the initial model.

From Figure (4.18a) it is seen that the drain current in the gate-source voltage sweep is continuous when using the proposed model and not piece-wise as with the initial model. At the same time, the drain current characteristics in terms of commutation slope and magnitude is in the same range as with the initial model. Also for the transconductance

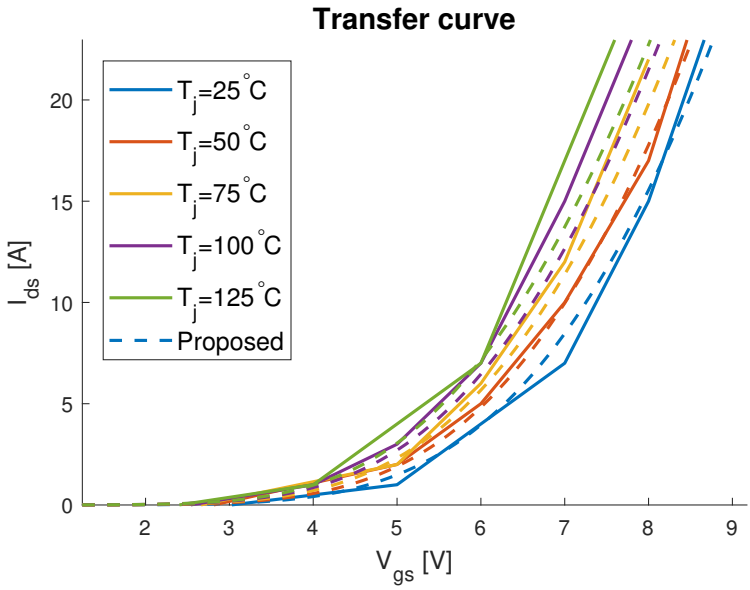
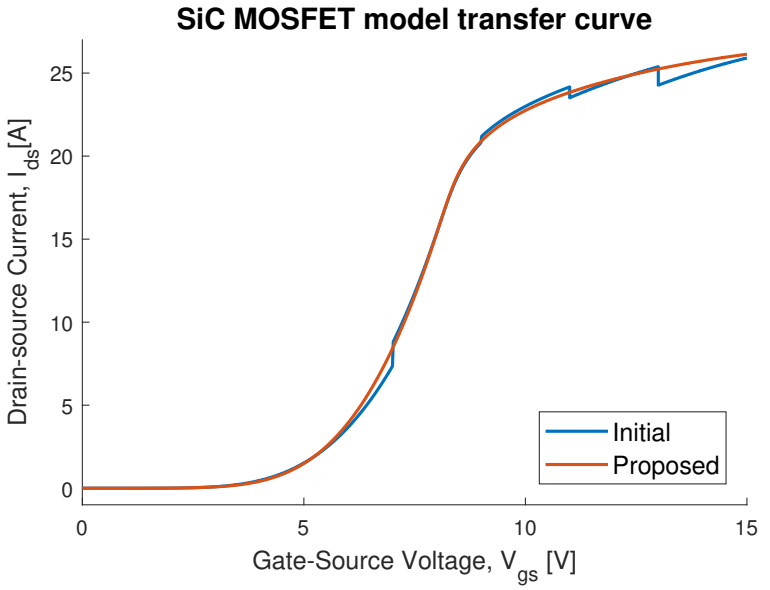


Figure 4.17: Comparison between transfer curve from lab and the proposed simulation model.

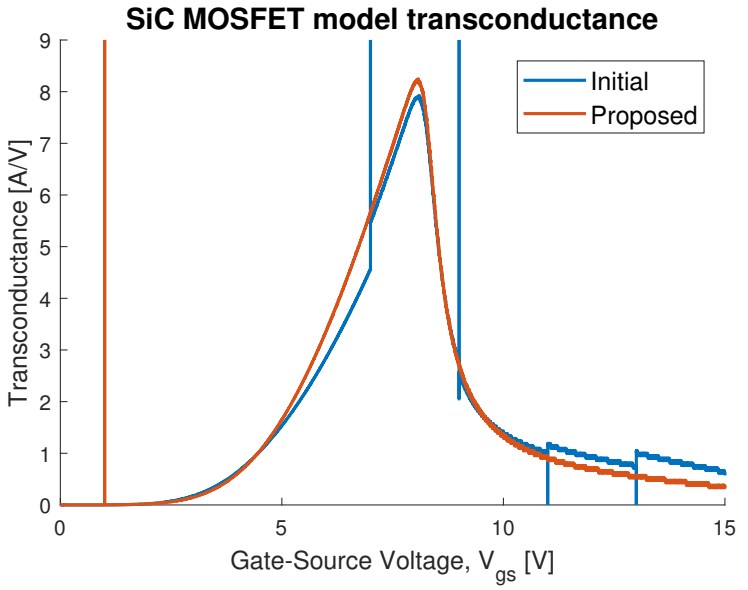
in Figure (4.18b), the characteristics from the initial model and the proposed model are in the same range. However, in the proposed model the transconductance is continuous. Hence, the MOSFET characteristics that was implemented from the manufacturer have been implemented in the proposed model in a continuous manner to improve convergence.

The spike in transconductance at 1 V gate-source voltage in the proposed MOSFET model is due to an if-statement in the shell for the LTspice model. However, as the drain current at this point is approximately zero, it does not lead to convergence errors.

When running simulations using the proposed model, trouble with convergence is gone and tolerances can be reset to default LTspice values. Moreover, the reliability of the simulation results are increased. This is illustrated in Figure (4.19) which shows peak dv/dt measurements for turn-off switching transients when using a conventional gate driver. Compared to lab measurements, the initial model gives a too high dv/dt at 15A. This does also conflict with theory as the dv/dt is determined by the location of the Miller plateau which in this case increases with load current. Therefore, according to theory, the dv/dt should also increase with load current for turn-off as the lab measurements show. The proposed model, gives a response that is much more like the lab measurement.



(a) Transfercurve obtained from LTspice simulations with initial and proposed model.



(b) Transconductance obtained from LTspice simulations with initial and proposed model.

Figure 4.18: Initial and proposed LTspice model.

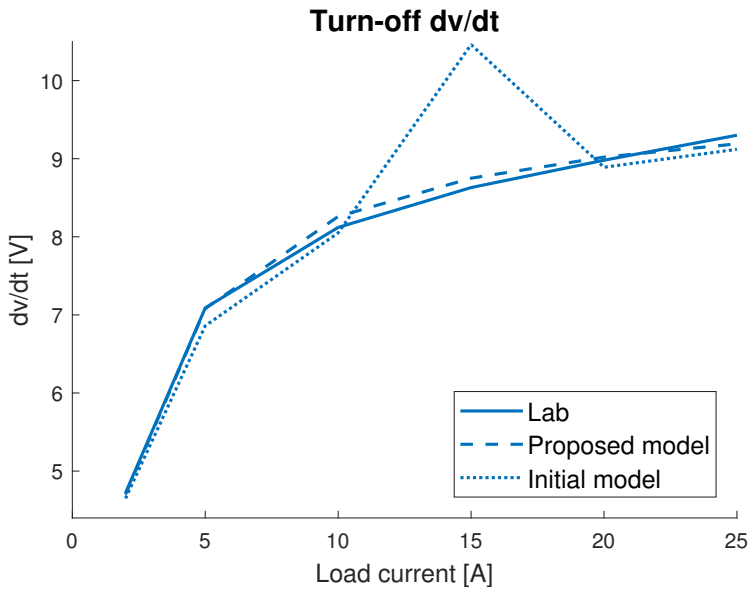


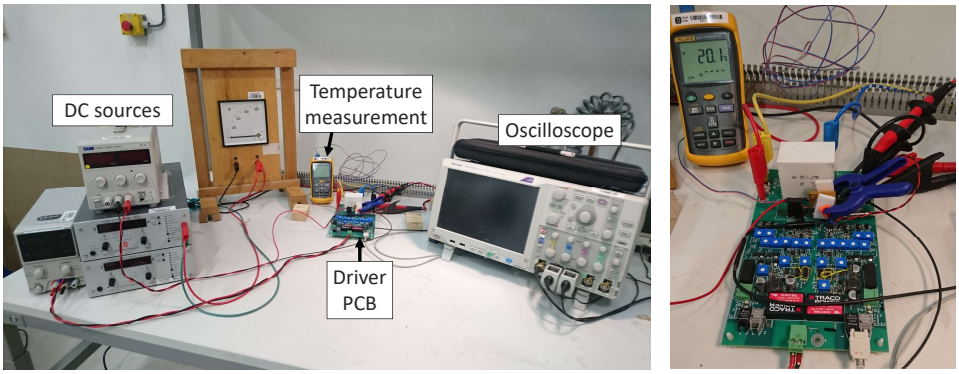
Figure 4.19: Comparison of dv/dt measurements from lab with initial and proposed model.

Chapter 5

Experimental validation of gate driver topologies

In the specialization project [1], the current dependency for turn-on and turn-off for the multistage driver was investigated. While the turn-off transients were found to be load current dependent, the turn-on transients are almost unaffected by the load current. However, theory suggests that both turn-on and turn-off transients are junction temperature dependent. Therefore, experiments to investigate both the load current and junction temperature dependency are done.

5.1 Laboratory setup



(a) Test setup. **(b)** Test board.

Figure 5.1: Laboratory setup.

A PCB including a DC-link, a half-bridge and the possibility to mount different drivers

have been made by SINTEF Energy Research. The PCB is the same that was used in the specialization project [1] and is seen in Figure (5.1 b). The drivers that are supported on the board is the conventional driver, the multistage driver and the RC driver. For investigation of the junction temperature dependency, a heatsink resistor have been clamped to the drain metal on the back of the MOSFET. The temperature of the drain metal is measured using a t-type thermocouple. As no heatsink is connected and with double pulse operation, it is assumed that the temperature of the drain metal is a good estimate for the real junction temperature.

The schematic circuit diagram for the lab setup is shown in Figure (5.2). Two SiC MOSFETs of type C3M0075120K from Wolfspeed [2] is connected in a half bridge supplied from a 600V DC-link. The upper MOSFETs gate is short circuited to source so that it is always turned off and only the body diode is used as a freewheeling diode. The lower MOSFET however is connected to the gate driver. For the double pulse tests, an inductive load is used connected between the AC coupling and DC+ on the PCB. The equipment that is used for sampling are listed in Table (5.1).

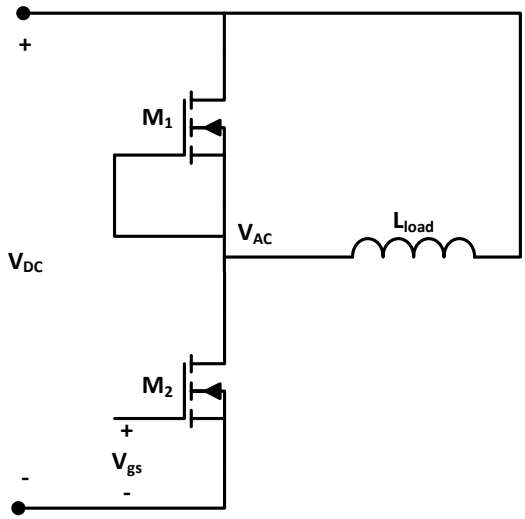


Figure 5.2: Schematic diagram of the experimental setup.

Table 5.1: Equipment used in lab.

Equipment	Name	Bandwidth
Oscilloscope	Tektronix DPO 5104B	1 GHz
Rogowski coils (current measurement)	PEM CWT06	30 MHz
Voltage probe	Tektronix THDP0200	200 MHz

Table 5.2: Test parameters used for the different drivers.

Driver	dv/dt	$R_{g,on/off}$	$C_{b,on/off}$	$V_{pos2/neg2}$
Conventional	10 V/ns	103/150 Ω		
RC driver	10 V/ns	103/150 Ω	470/1500 pF	
Multistage, fixed	10 V/ns	103/150 Ω		4.9/7.1 V

5.2 Method

To provide representative results for a motor drive application, a target dv/dt of maximum 10 V/ns is chosen as this could be a typical limit for applications with fast switching Si IGBTs. The gate resistors that is used to meet this limit are presented in Table (5.2). Moreover, the boost capacitors that is used in the RC driver and the fixed boost voltage levels in the multistage driver is also presented in the table.

The test matrix is shown in Table (5.3). Initially, the gate resistors for turn-on and turn-off was chosen to meet the 10V/ns limit. However, due to the heatsink resistor connected to the drain metal, the drain-source capacitor and gate-drain capacitor have become larger. This does not affect the delay time as the delay time for turn-on and turn-off mainly depends on the gate-source capacitor. However, as the voltage commutation is inverse proportional to the gate-drain capacitor as given by Equation (2.8), dv/dt is slowed down. This will be seen in the results part from Figure (5.5) where the maximum dv/dt is seen to be about 6.5 V/ns when the heatsink resistor is connected. Without the heatsink resistor connected, the maximum dv/dt was measured to be about 9.5 V/ns. This was shown in the specialization project [1].

Two strategies for controlling the boost voltages V_{pos2} and V_{neg2} in the multistage driver have been investigated. The boost voltages can either be fixed at a constant voltage level or optimized at each operation point to provide the largest reduction in delay time without affecting dv/dt or di/dt. The fixed solution is referred to as the fixed multistage driver while the solution with optimized boost voltages is referred to as the adaptive multistage driver. The boost voltages presented in Table (5.2) is used for the fixed multistage driver.

When the fixed multistage driver is chosen, the voltage levels must be fixed according to worst case. For turn-off, V_{neg2} should ideally be as low as possible to give a high initial gate current. Worst case will therefore be for low junction temperatures and high load currents due to the high location of the Miller plateau at that operation point. Hence, V_{neg2} is fixed at 7.1 V in the reported results. For turn-on, the datasheet gives that threshold voltage is reduced by approximately 0.5 V from junction temperature 25°C to 125°C [2]. Hence, as V_{pos2} ideally should be as high as possible to provide a large boost current, worst case is for high temperatures as this gives a lower threshold voltage. V_{pos2} is therefore fixed at 4.9 V in the reported results for the fixed multistage driver. Choosing the size for the boost capacitors in the RC driver must be done for the same operation points as was the worst operation points for the multistage driver and dimensioned so that dv/dt and di/dt are not affected.

In the specialization project it was shown that the turn-on switching transient for SiC MOSFETs does not depend on the load current [1]. Therefore, only the junction temper-

Table 5.3: Test matrix.

			Turn-on	Turn-off
Driver	V_{dc}[V]	$T_j[°C]$	I_d[A]	I_d[A]
CGD	600	25	15	2, 5, 10, 15, 20, 25
	600	50	15	2, 5, 10, 15, 20, 25
	600	75	15	2, 5, 10, 15, 20, 25
	600	100	15	2, 5, 10, 15, 20, 25
	600	125	15	2, 5, 10, 15, 20, 25
Adaptiv multistage	600	25	15	2, 5, 10, 15, 20, 25
	600	50	15	2, 5, 10, 15, 20, 25
	600	75	15	2, 5, 10, 15, 20, 25
	600	100	15	2, 5, 10, 15, 20, 25
	600	125	15	2, 5, 10, 15, 20, 25
Fixed multistage	600	25	15	2, 5, 10, 15, 20, 25
	600	50	15	2, 5, 10, 15, 20, 25
	600	75	15	2, 5, 10, 15, 20, 25
	600	100	15	2, 5, 10, 15, 20, 25
	600	125	15	2, 5, 10, 15, 20, 25
RC-driver	600	25	15	2, 5, 10, 15, 20, 25
	600	50	15	2, 5, 10, 15, 20, 25
	600	75	15	2, 5, 10, 15, 20, 25
	600	100	15	2, 5, 10, 15, 20, 25
	600	125	15	2, 5, 10, 15, 20, 25

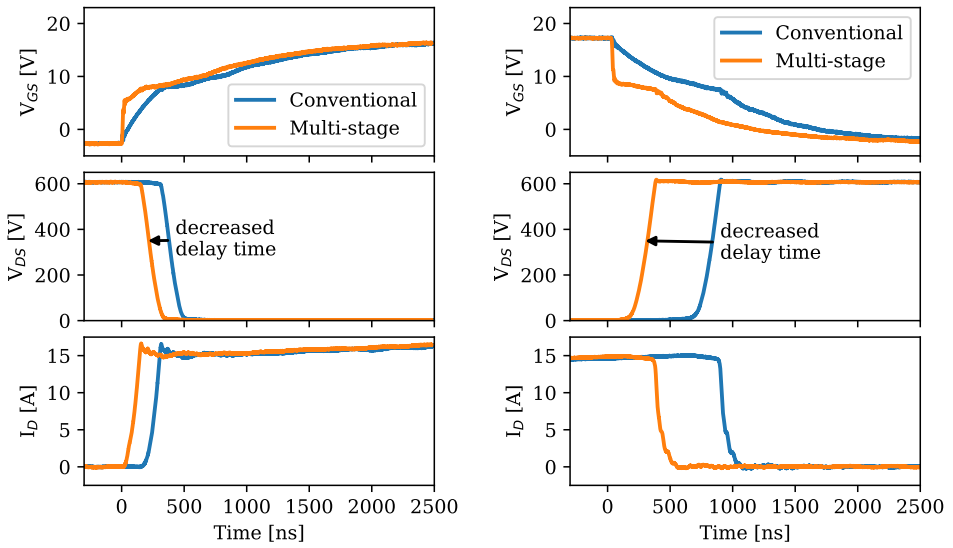
ature dependency is investigated in the master thesis. For each junction temperature, a constant load current of 15 A is used to investigate the turn-on transient in the laboratory work. For turn-off transients however, both the junction temperature and the load current dependency are investigated. Therefore, for each junction temperature, the turn-off transients have been investigated at 2, 5, 10, 15, 20, and 25 A load current.

The reported numerical results are obtained using a MATLAB script. For dv/dt measurements, waveforms from the oscilloscope are filtered and the peak value detected. For turn-on delay times, the point where the drain-source current starts to rise is detected and compared to the point where the gate-source voltage started to rise. For turn-off, it's the drain-source voltage commutation that is detected and compared to the point where the gate-source voltage started to fall. The delay in measuring probes have been compensated according the their datasheet values.

5.3 Lab results

The lab results presented below are the same as was presented at ECCE Asia with some additional results that was left out of the paper [4].

Waveforms that validate the operation principle of the multistage driver is presented in Figure (5.3). Both for turn-on and turn-off it is clear that the multistage driver is able



(a) Turn-on switching transients.

(b) Turn-off switching transients.

Figure 5.3: Waveforms validating the operation principle of the multistage driver.

to change the gate-source voltage faster than the conventional gate driver. This forces the MOSFET to turn on or off faster. Moreover, as seen in the figure, the commutation slopes for di/dt and dv/dt are similar for the conventional gate driver and the boost driver, only shifted in time. Hence, making the multistage driver able to reduce the delay time without affecting the commutation slopes as intended. Waveforms for the RC driver are very similar to the ones obtained with the multistage driver and therefore not presented.

5.3.1 Turn-off switching transients

Figure (5.4) shows the minimum delay times that are obtained for turn-off with different gate drivers at a junction temperature of 25°C. As the Miller plateau increases with increasing load current, the time until the gate-source voltage is lowered to the Miller plateau is reduced when the load current increases. Hence, the delay time is reduced. This is seen from the graph for the conventional gate driver as the delay time is reduced with increasing load current. The same trend is seen for the RC driver and the fixed multistage driver.

When using the fixed multistage driver instead of the conventional gate driver, thus allowing the gate-source voltage to be reduced faster, the possible reduction in turn-off delay time is approximately 100 ns for low load currents and 150 ns for high load currents. Except from the 50 ns difference in reduced delay time between low and high load currents, it seems like the fixed multistage driver gives an almost constant reduction in delay time compared to the conventional gate driver. This is because the fixed boost voltage will always force the turn-off boosting stage to turn off at the same gate-source voltage level.

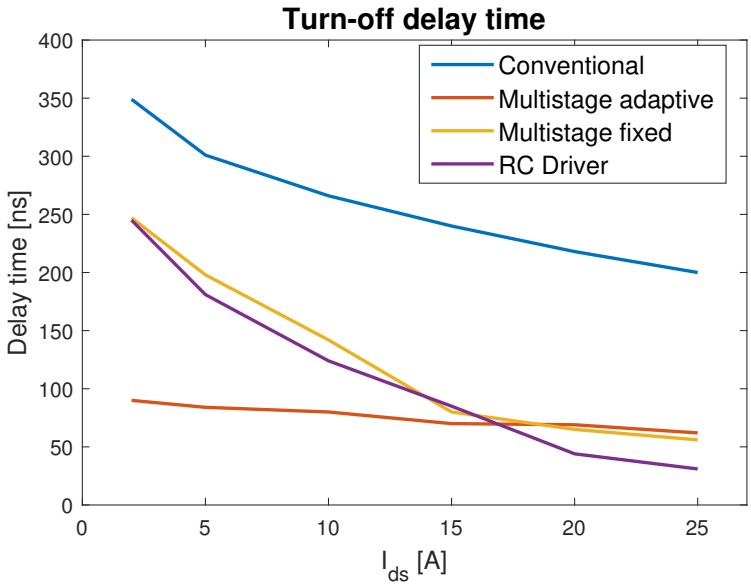


Figure 5.4: Minimum turn-off delay times obtained with different gate drivers as function of load current at junction temperature 25°C.

Hence, the reduced delay time equals the time reduction until the gate-source voltage equals the boost voltage and the blocking diode turns reverse bias, which will be the same for all load currents as long as the junction temperature is the same.

For the RC driver, the delay time improvement for turn-off is similar to the improvement obtained with the fixed multistage driver for low load currents. For high load currents however, the RC driver gives shorter delay times than the multistage driver. However, due to the available discrete values, the boost capacitor used to obtain the results is chosen to be a bit too large and dv/dt is slightly affected for high load currents. This can be seen in Figure (5.5) where the voltage commutation slopes for the different drivers are presented. If the boost capacitor is chosen smaller so that dv/dt is unaffected by the boost capacitor, the improvement in delay time would be similar to the fixed multistage driver for all load currents. Thus, the performance from the RC driver and the fixed multistage driver is similar.

As the Miller plateau is lowered for lower load currents, one can allow a more negative boost voltage as the load current is reduced. When using the adaptive multistage driver, the boost voltage is adjusted to the lowest value possible without affecting dv/dt. This gives the largest improvement in terms of reduced turn-off delay time as seen in Figure (5.4). The boost voltages that is used for the different load currents and junction temperatures are shown in Figure (5.6). They reflect the location of the Miller plateau at the different operation points. The improvement when using the adaptive multistage driver is found to be 259 ns or 74 % for low load currents at 25°C junction temperature compared to the conventional gate driver. When setting the dead time in a bridge leg, the worst delay time will be the design parameter. Hence, by changing from a conventional driver to a

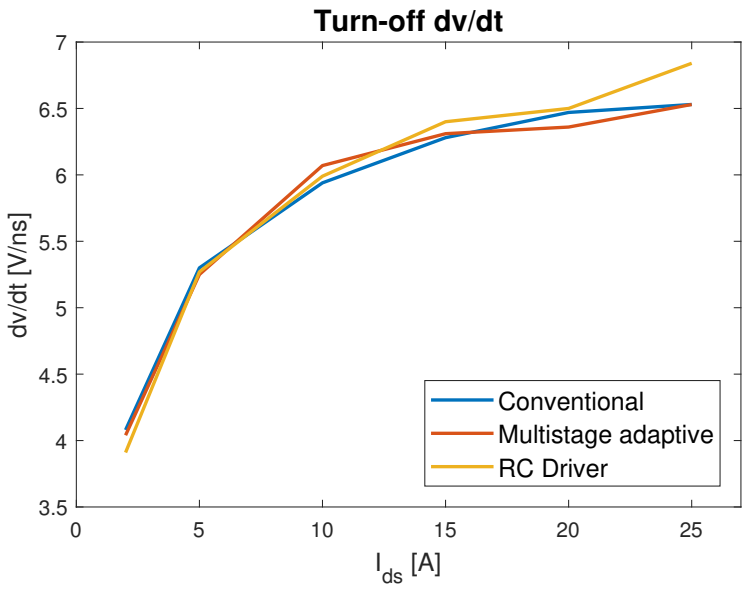


Figure 5.5: Voltage commutation slopes as function of load current for three different driver topologies and junction temperature 25°C.

Table 5.4: Turn-off delay time improvements at 25°C for 2 A load current.

Driver	$T_{d,off}$	$\Delta T_{d,off}$	Improvement
Conventional	349 ns		
RC driver	245 ns	104 ns	30%
Multistage fixed	247 ns	102 ns	29 %
Multistage adaptive	90 ns	259 ns	74 %

multistage driver with adaptive boost voltage, the dead time can be reduced by 259 ns. The delay times for all drivers at turn-off and 25°C are presented in Table (5.4).

As the threshold voltage is lowered for increasing junction temperature, the Miller plateau will be lowered for increasing junction temperature as well for the same load current. This means that for turn-off transients, the gate-source voltage must be reduced more before the voltage commutation starts. Hence, the turn-off delay time increases with increasing junction temperature as seen in Figures (5.7a) and (5.7b).

Figure (5.7a) shows the turn-off delay times at different junction temperatures and load currents for the conventional gate driver. At 2 A load current the delay time is increased by 60 ns, from 349 to 409 ns, when the junction temperature is increased from 25°C to 125°C. This proves that for power electronic design, it is not sufficient to only consider the load current dependency on the turn-off switching transient. If a SiC MOSFET should be used in a bridge leg for example, the requirement for dead time in the half bridge must be increased if the application should have a safe operation at 125°C.

The junction temperature dependency must be considered for the multistage driver as

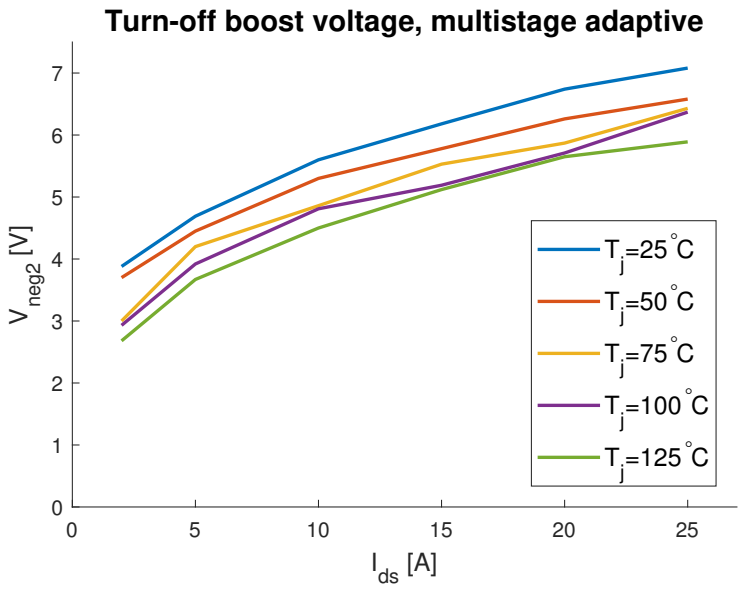
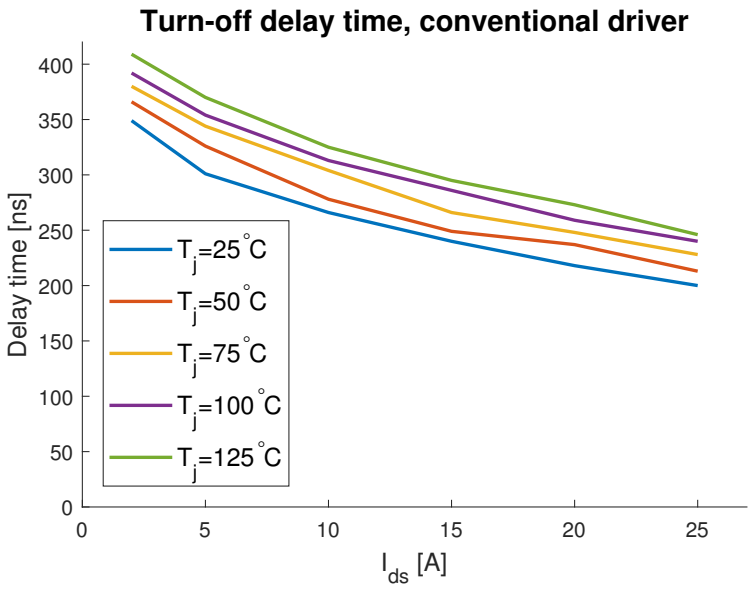


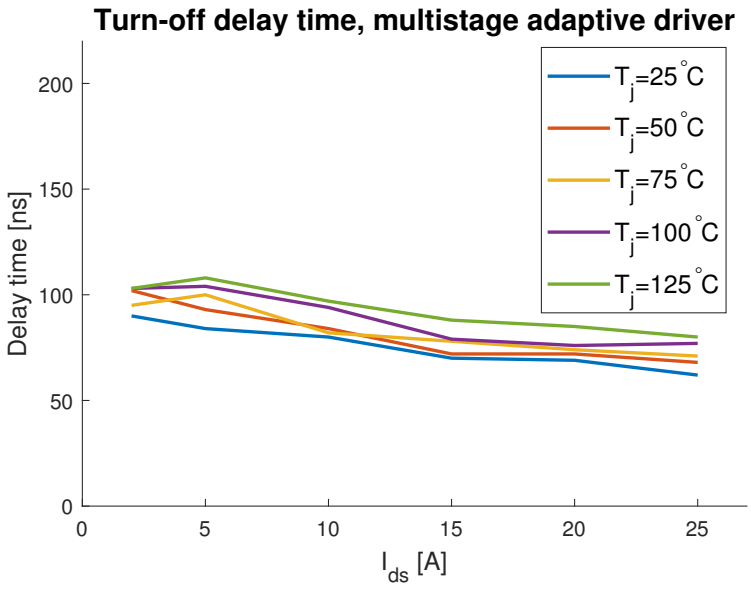
Figure 5.6: Turn-off boost voltages used in the adaptive multistage driver for different load currents and junction temperatures.

well. When the fixed multistage driver is used, the boost voltage for turn-off must be chosen according to the worst operation point which is at high load currents and low junction temperatures. In the presented results, the boost voltage have been chosen according to junction temperature 25°C and a load current of 25 A as this is seen to be the highest value for V_{neg2} according to Figure (5.6). However, the trend in the figure shows that when the junction temperature is reduced, the boost voltage must be increased for turn-off. This means that for this specific setup, if operation with colder junction temperatures than 25°C is planned, the fixed boost voltage must be chosen even higher. However, with colder junction temperatures, the Miller plateau will be at a higher voltage level. This gives a larger voltage difference between the negative driving voltage and the gate-source voltage during voltage commutation which increases the gate current. After Equation (2.8), the increased gate current will increase the voltage commutation slope. To avoid conflicts with the dv/dt target of maximum 10V/ns that is used in the presented results, the gate resistor must possibly be retuned which again will affect the delay times for all operation points. Junction temperature dependency on dv/dt for the conventional gate driver is shown in Figure (5.8). Note that the heatsink resistor for junction temperature control that is connected to the back of the MOSFET slows down the dv/dt as have previously been explained.

Figure (5.6) shows the optimal choice for boost voltages used for turn-off at the different operation points for the adaptive multistage driver. The turn-off delay times that is obtained is presented in Figure (5.7b). Similar as with the conventional driver, the delay times increases with junction temperature. The highest measured delay time is 108 ns at 125°C junction temperature which a 74% reduction compared to the highest delay time obtained with the conventional gate driver. The delay times at 125°C is presented in Table



(a) Conventional gate driver.



(b) Adaptive multistage gate driver.

Figure 5.7: Junction temperature dependency on turn-off delay times for the conventional and the adaptive multistage gate driver.

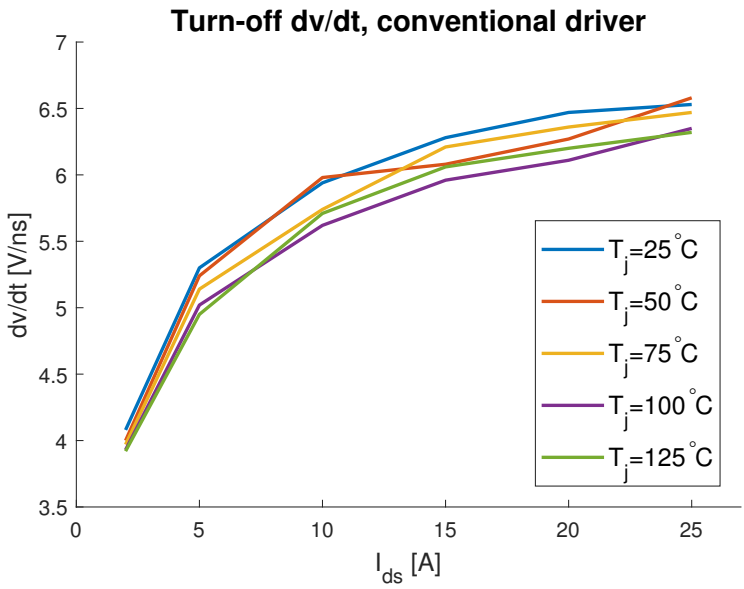


Figure 5.8: Voltage commutation slopes for the conventional gate driver at different junction temperatures.

Table 5.5: Turn-off delay time improvements at 125°C.

Driver	$T_{d,off}$	$\Delta T_{d,off}$	Improvement
Conventional	409 ns		
Multistage adaptive	108 ns	301 ns	74%

(5.5).

The results for the turn-off transients have shown that to provide the largest possible reduction in delay time, the boost voltage in the multistage driver must be chosen optimally. When the Miller plateau is lowered due to increasing temperature or lower load current, a lower V_{neg2} can be allowed without affecting dv/dt during turn-off, thus increasing the effect of the boosting stage in the multistage driver. If V_{neg2} is chosen to be fixed, thus using the fixed multistage driver, it must be chosen according to the lowest operation temperature and highest load current. However, the results show that the possible reduction in turn-off delay time for the fixed multistage driver and the much less complex RC driver is similar while the adaptive multistage driver outperform both.

5.3.2 Turn-on switching transients

Turn-on delay times with the different gate driver topologies are shown in Figure (5.9) as a function of junction temperature. Due to the relatively low difference in threshold voltage for the SiC MOSFET at a junction temperature of 25°C and 125 °C, the variation in turn-on delay times over the tested junction temperatures are small when using the same gate

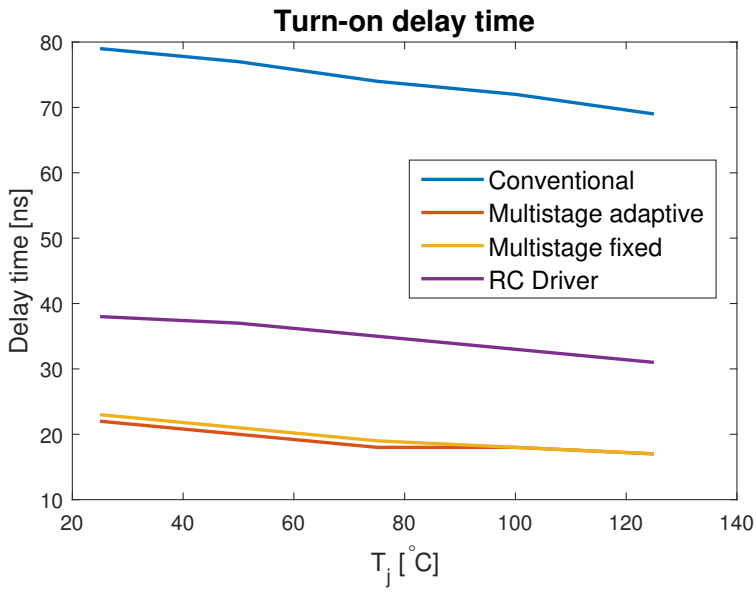


Figure 5.9: Turn-on delay times as function of junction temperature for the different gate driver topologies.

driver. At 25°C the turn-on delay time is measured to be 79 ns when using the conventional gate driver. This is 10 ns more than the delay time at junction temperature 125°C, or 15 % higher. For the previously presented turn-off transients, the difference between the highest and lowest measured delay times at 25°C was 149 ns or 75 % for the conventional gate driver. Hence, the turn-on delay time does not have a too high dependency on the junction temperature.

The improvement in turn-on delay time when changing from the conventional gate driver to the fixed multistage driver is 56 ns or 71 % for 25°C junction temperature. If the adaptive multistage driver is used, the improvement is 57 ns or 72 % for the same junction temperature. A similar percent-wise improvement is found for the rest of the tested junction temperatures as well, both for the fixed and adaptive multistage driver. As the turn-on delay times are not too affected by the junction temperature, the performance from the fixed and adaptive multistage driver is very similar. This can also be seen from the boost voltages that is used in Figure (5.10). While the fixed boost voltage is tuned to 4.9 V for the highest junction temperature, the adaptive solution only allows the boost voltage to vary from 4.9 to 5.1 to not affect di/dt. Hence, making the performance from the adaptive and fixed multistage driver very similar.

For the RC driver, the improvement in delay time during turn-on at 25°C was 41 ns or 52 %. However, due to the available discrete boost capacitor values, the result is not ideal. An improvement in delay time more equal to the one obtained with the multistage drivers can be expected if the best choice for the boost capacitor is made. Hence, the added complexity from introducing the multistage driver can be reduced for turn-on by considering the RC driver. Turn-on delay time improvements for the worst operation point,

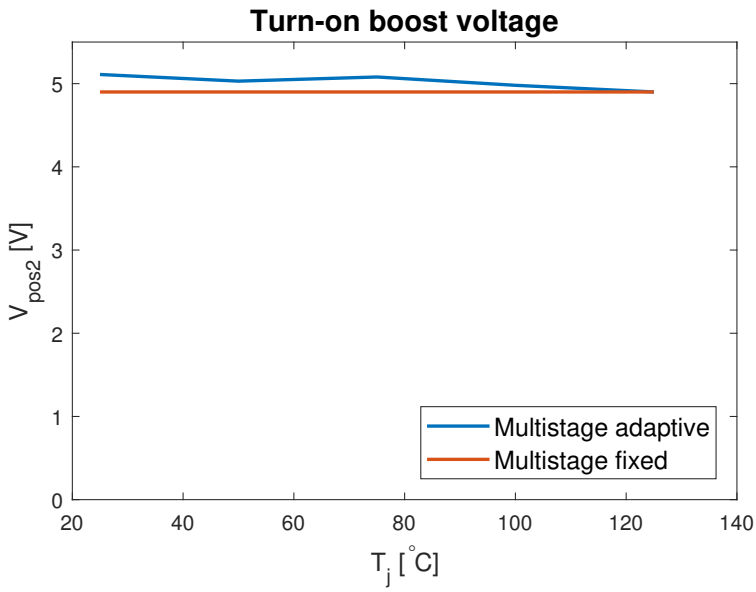


Figure 5.10: Turn-on boost voltages used in the fixed and adaptive multistage driver.

Table 5.6: Turn-on delay time improvements at 25°C.

Driver	$T_{d,on}$	$\Delta T_{d,on}$	Improvement
Conventional	79 ns		
RC driver	38 ns	41 ns	52%
Multistage fixed	23 ns	56 ns	71%
Multistage adaptive	22 ns	57 ns	72%

i.e at the lowest tested junction temperature is presented in Table (5.6).

Chapter 6

Impact of delay time minimization gate drivers

This chapter presents simulation results of the impact that a delay time minimization gate driver has on the voltage and current output quality from a converter in a motor drive application. The results have been presented at ECCE Asia [4], but additional explanations and observations are included in this chapter.

6.1 Dead time requirement

The required dead time in a half-bridge converter and the impact it has on the output voltage during one switching event was discussed in Section 2.3.3. As was shown by Equation (2.9), commutation slopes and the turn-off delay time during the switching event are dimensioning for the required dead time. As the dead time usually is a constant for a given application, it must be chosen large enough to allow safe switching for all possible operation points. Hence, the dead time must be chosen according to the operation point that has the largest dead time requirement.

For the lab work presented in Chapter 5, commutation slopes at turn-off was equal for all the different gate drivers. Hence, it is the worst turn-off delay time for each gate driver that is dimensioning for the dead time as illustrated in Figure (6.1).

The performance when using the CGD and the adaptive multistage driver is compared in a simulation case. From Figure (5.7) it is seen that the largest turn-off delay times that was measured in lab was with a junction temperature of 125°C, which therefore should be dimensioning. For CGD, the largest measured delay time was 409 ns. However, turn-off delay times are inverse proportional to load current, and the smallest load current that was tested was 2 A. Therefore, to ensure safe operation for even lower load currents, a turn-off delay time of 450 ns is assumed in dead time calculations. For the adaptive multistage driver, the largest measured delay time was 108 ns. However, the inverse proportionality with load current is not as dominant for the multistage drivar as for CGD. Therefore, a

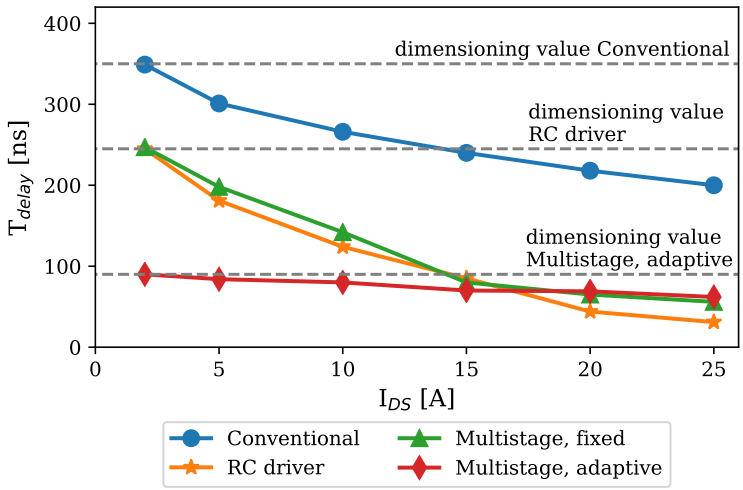


Figure 6.1: Dimensioning values for dead time requirement.

Table 6.1: Simulation parameters.

Driver	dv/dt	di/dt	Dead time	Minimum pulse width
Conventional	10 V/ns	0.3 A/ns	810 ns	2.43 μs
Multistage	10 V/ns	0.3 A/ns	470 ns	1.41 μs

turn-off delay time of 110 ns was used in the dead time calculations.

The dead time in a half-bridge will influence the minimum pulse width (MPW) that can be allowed. In PWM modulation, all pulses shorter than MPW must be cancelled as the delay times and commutation times are too large for the pulses to be realized in the output voltage. In the simulations the MPW have been set to three times the dead time which is the same MPW requirement as was used in [62]. Simulation parameters are presented in Table (6.1).

6.2 Motor model

The simulation case is a motor drive application with a motor model and a voltage source inverter (VSI) as shown in Figure (6.2). The motor is assumed to be a round rotor 15 kW PM synchronous machine, supplied by a 600 V dc-link.

In the simulations, investigations on the VSI performance at different modulation indices are done. However, as the load current magnitude and direction highly influences the output voltage pulses (see Section 2.3.3), it is desirable to have the same load current conditions for all modulation indices for comparison of the results. Therefore, the load current RMS value and the power factor (pf) have been held constant at 21.2 A (30 A peak) and 0.9 respectively. To do so, Equations (6.1) to (6.3) have been used.

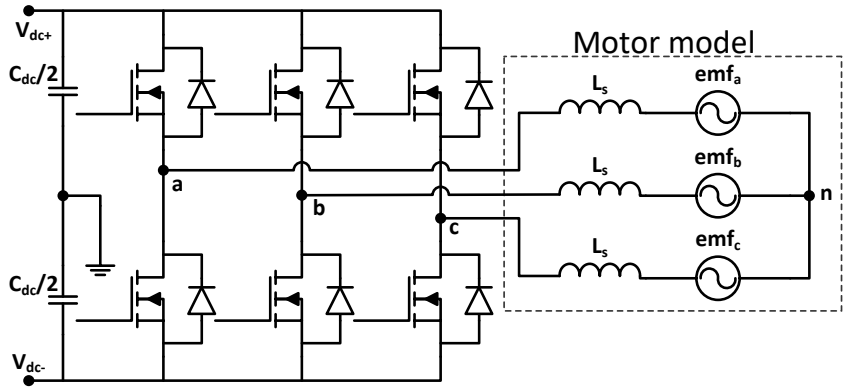


Figure 6.2: Schematic diagram of a three phase inverter and the equivalent motor model.

$$\theta = cos^{-1}(pf) \tag{6.1}$$

$$\delta = tan^{-1}\left(\frac{X_l I_l cos\theta}{V_{ph}^* - X_l I_l sin\theta}\right) \tag{6.2}$$

$$emf = \frac{X_l I_l cos\theta}{sin\theta} \tag{6.3}$$

In the equations, θ is the angle between the phase voltage and line current, δ is the power angle i.e. the angle between the phase voltage and the back emf, $X_l = 2\pi f_0 L_s$ is the synchronous reactance with f_0 as the fundamental electric frequency, and emf is the induced emf in one phase. V_{ph}^* is the expected RMS phase voltage which in the linear region is estimated based on the modulation index (M_a) from Equation (6.4) [3].

$$V_{ph}^* = \frac{V_{dc}}{2\sqrt{2}} * M_a \tag{6.4}$$

6.3 PWM methods

In pulse width modulation (PWM), the amplitude and frequency of the fundamental output voltage are controlled by comparing a control signal, V_c, to a triangular carrier, V_{tri}. Each inverter phase leg is controlled individually. The control signal V_c shapes the phase to neutral output voltage. For an AC output voltage, the control signal must have a fundamental part equal to the desired output voltage and with the desired frequency.

The ratio between the amplitude of the fundamental part of the control signal $\hat{V}_c$ and the triangular carrier wave $\hat{V}_{tri}$, is termed the modulation index M_a [3]:

$$M_a = \frac{\hat{V}_c}{\hat{V}_{tri}} \tag{6.5}$$

In addition to the fundamental part, triplen harmonics can be added to the control signal in a three-phase inverter as they are neutralised in the line voltage [63]. Furthermore, when the VSI drives a load with an isolated neutral point such as a motor, an arbitrary zero-sequence signal can be injected to the control signal in all phases [62, 64].

The simplest solution is to use a control signal consisting only of a sinusoidal wave, termed SPWM. The control signal is then shaped as $M_a sin(2\pi f_o t)$ with the desired frequency f_0 and amplitude M_a. The SPWM technique is linear up to M_a equal to 1, after that overmodulation occurs [3].

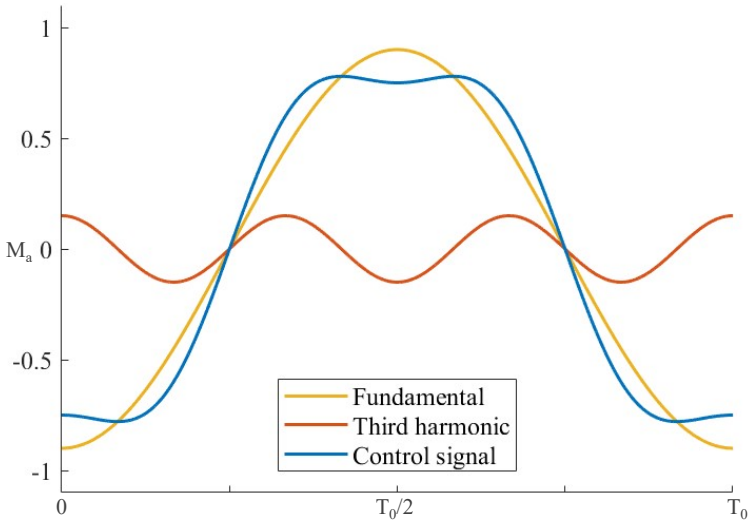


Figure 6.3: Continuous control signal with third harmonic injection (THIPWM).

By injecting a third harmonic signal to the control signal (THIPWM) as shown in Figure (6.3), the linear region for the line voltage can be increased. By choosing the amplitude to be 1/6 of the amplitude of the fundamental part, the linear region can be increased until $M_a = 1.15$. Thus, a 15% higher output line voltage can be achieved without overmodulation [63].

Injecting a discontinuous zero-sequence signal to the control signal (DPWM) is suggested to improve the VSI performance in the overmodulation region in terms of voltage linearity and current harmonics [62, 65]. The control signal is shown in Figure (6.4) for M_a equal to 0.9. If V_{c*} is the fundamental control signal with the largest instantaneous amplitude, the zero-sequence signal V_0 is generated by Equation (6.6) as illustrated in Figure (6.5) [65].

$$V_0 = sign(V_{c*}) - V_{c*} \tag{6.6}$$

When using DPWM, the control signal equals 1 in absolute amplitude for 1/3 of the period thus reducing the number of voltage pulses. This reduces the average switching frequency and the switching losses. The carrier frequency can therefore be increased by a

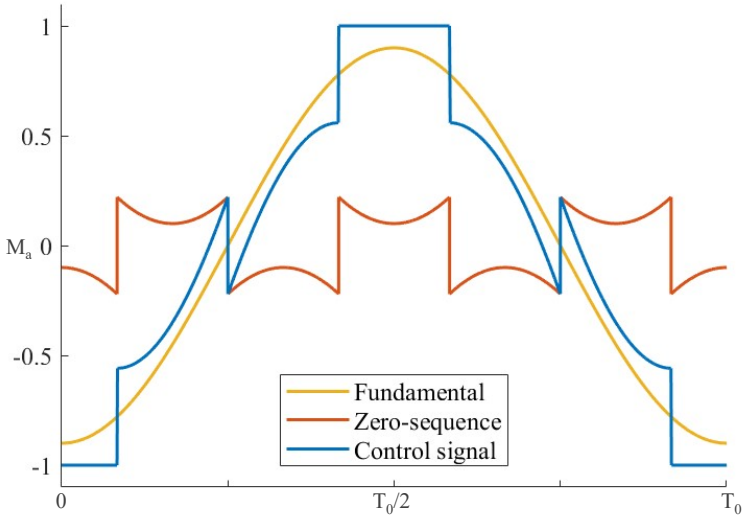


Figure 6.4: Discontinuous control signal with zero-sequence injection (DPWM).

factor of 1.5 to have the same average switching frequency and switching losses as for the continuous PWM methods [62].

6.4 Simulation model

For precise simulations of the VSI with the motor model, a simulation script was built in MATLAB rather than using simulations tools like MATLAB Simulink. The code is available in Appendix C.

In the simulation model, a PWM signal, which controls the switching sequence, is generated and delivered to each half-bridge. SPWM, THIPWM and DPWM are supported and pulses that are shorter than MPW are blanked out. When the PWM signals a switching event, the output from the inverter is delayed according to the delay times and dead time. During freewheeling, the direction of the load current decides the voltage pulses as described in Section 2.3.3. When the dead time is over, the output voltage commutates to its desired value with the commutation slope that is chosen.

The line current magnitude and phase depends on the voltages and impedances in the model as shown by the differential equation for the voltage over the inductor L_s in phase a, given by Equation (6.7).

$$V_a - emf_a - V_n = L_s \frac{di}{dt} \tag{6.7}$$

The voltage V_n is the voltage between the isolated neutral point in the synchronous PM motor and the ground. When the back EMFs in the motor are balanced, i.e. $emf_a + emf_b + emf_c = 0$, the neutral point voltage is given by Equation (6.8).

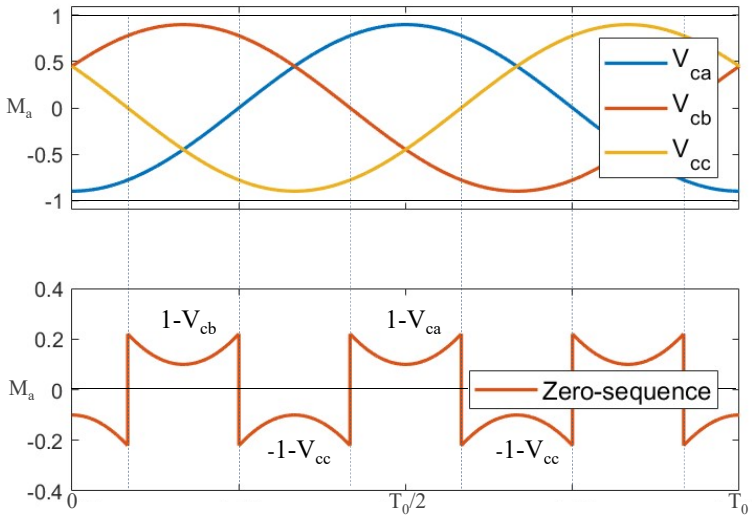


Figure 6.5: Generation of the zero-sequence signal that is used in DPWM.

$$V_n = \frac{1}{3}\Big(V_a + V_b + V_c\Big) \tag{6.8}$$

For numerical solution to the differential equation, the load current differential is estimated by Equation (6.9) and the time differential by Equation (6.10).

$$di = I[k] - I[k-1] \tag{6.9}$$

$$dt = t[k] - t[k-1] \tag{6.10}$$

The load current in phase A can then be calculated by Equation (6.11), which is derived from Equation (6.7) by using Equation (6.9). Phase B and C currents are found similarly with the respective phase voltages.

$$I_a[k] = \frac{dt}{L_s}\Big(V_{an}[k-1] - V_n[k-1] - emf_a[k-1]\Big) + I_a[k-1] \tag{6.11}$$

Output from the simulations are line currents and phase voltages for all three phases. By using MATLABs built in FFT tools, the harmonics spectre for output line voltage and line current are evaluated. In particular, the line voltage magnitude and line current quality is of interest.

To quantify the quality of the line current, total harmonic distortion (THD) is used. If I_1 is the fundamental component and I_h is the h^{th} harmonic for $h \neq 1$, then THD is calculated as:

$$THD = \frac{\sqrt{\Sigma_{h=2}^{\infty} I_h^2}}{I_1} \tag{6.12}$$

6.5 Simulation results

The three different PWM techniques have been investigated in simulations with the conventional gate driver and the adaptive multistage driver.

Simulations are run with a carrier frequency of 15 kHz for SPWM and THIPWM. For DPWM, a carrier frequency which is 1.5 times higher, i.e. 22.5 kHz is used as previously described. The modulation index, M_a, is varied in the range from 0.8 to 1.5 to cover both the linear region and the overmodulation region [3]. For all modulation indices, the load current magnitude and the power factor have been held constant.

Simulation results in terms of fundamental output line voltage magnitude and line current THD are shown in Figures (6.6) and (6.7) respectively. When the conventional gate driver is used, a non-linear bubble shaped output voltage is observed in the last part of the theoretical linear region due to the minimum pulse width. The bubble starts at modulation index 0.92 for SPWM, 1.06 for THIPWM and 1.09 for DPWM. For control signals with an amplitude higher than these values, the voltage pulses are blanked out giving a higher fundamental component and voltage distortion. The distortion is visible in the current THD as well by a large peak for the same M_a as the line voltage becomes non-linear.

As shorter voltage pulses are accepted when using the multistage driver, the control signal is allowed to cross the triangular carrier wave at higher values before the pulses are blanked out. This increases the linear region for the output voltage and reduces the size of the observed bubble as observed in Figure (6.6). The linear regions are increased to 0.95 for SPWM, 1.10 for THIPWM and 1.11 for DPWM as presented in Table 6.2. The same trend is seen for the line current THD as the peak that is found when the voltage becomes non-linear is shifted towards higher modulation indices. At the same time, this peak is reduced.

Within the linear region, the peak output voltage when using the conventional gate driver and the multistage driver are similar. However, due to the reduced delay times for the multistage driver, the current freewheeling is reduced thus providing voltage shapes that are more equal to the ideal. With more ideal voltage pulses, the current harmonics are reduced and THD improved as presented in Table (6.2). When using DPWM, the improvement in current harmonics is found to be 7.7 % which is the largest improvement. However, DPWM is still the PWM method that creates most current harmonics in the linear region. For SPWM and THIPWM, which perform more equal in the linear region, the reduction in THD were found to be 5.1 % and 6.6 % respectively.

Table 6.2: Maximum M_a and current THD for linear regions for different PWM methods.

	SPWM		THIPWM		DPWM	
Driver	$M_{a,max}$	THD	$M_{a,max}$	THD	$M_{a,max}$	THD
Conventional	0.92	0.18 %	1.06	0.17 %	1.09	0.25 %
Multistage	0.95	0.17 %	1.1	0.16 %	1.11	0.23 %
Improvement	3.3 %	5.1 %	3.8 %	6.6 %	1.8 %	7.7 %

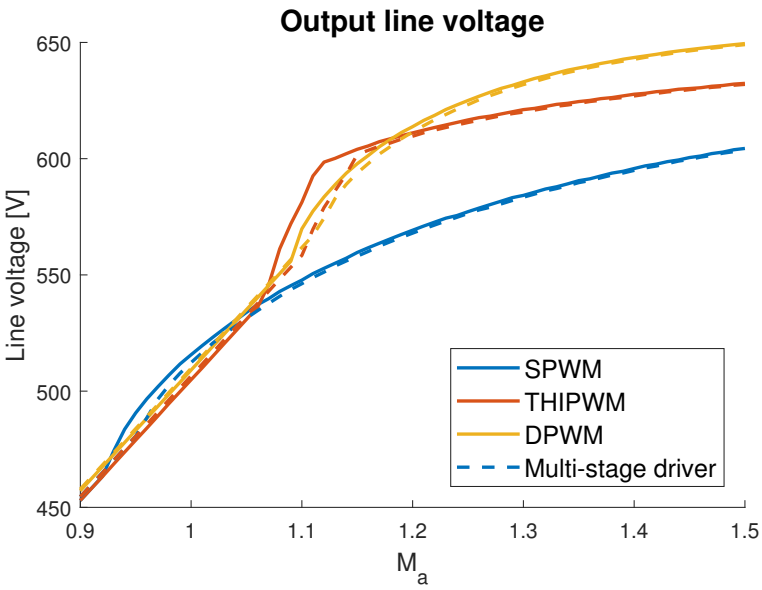


Figure 6.6: Output line voltage magnitude as function of modulation index.

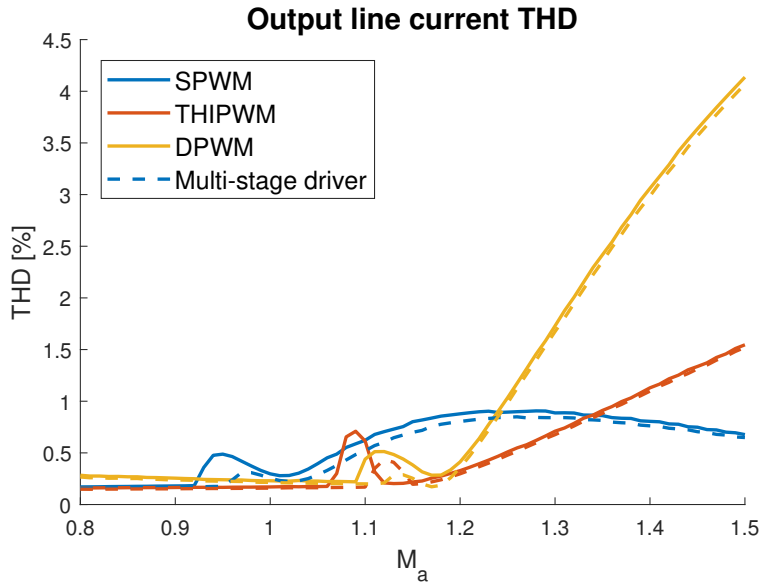


Figure 6.7: Line current THD as function of modulation index.

Chapter 7

Adaptive gate driving

This chapter proposes an adaptive gate driver structure for delay time minimization based on the findings in Chapter 5 and 6.

7.1 Driver topology

As was shown in Chapter 5, the turn-on and turn-off delay times can be reduced when using more advanced gate driver topologies than the conventional gate driver. Moreover, the experimental results gave two main conclusions on the tested gate driver topologies, one for turn-on and one for turn-off switching transients:

- For turn-on, as the results in Figure (5.9) show, the delay times are almost unaffected by the junction temperature. When the boost capacitor in the RC driver is properly chosen, the delay time reduction can be similar to the reduction obtained with the fixed multistage driver. Furthermore, making the multistage driver adaptive based on temperature measurements does not make a significant impact on the delay time either. Hence, the added complexity from the multistage driver compared to the RC driver is unnecessary and can be avoided.

- For turn-off, similar as for turn-on, the RC driver and the fixed multistage driver gives a similar reduction in delay time compared to the delay times obtained with the conventional gate driver. However, due to the load current and junction temperature dependency of the Miller plateau, a significant improvement in delay time can be obtained when using the multistage driver with an adaptive boost voltage, as was shown in Figure (5.4).

An adaptive gate driver topology that aims for delay time minimization is proposed based on the conclusions from Chapter 5. It is shown in Figure (7.1). Its design combines the benefits from the RC driver and the multistage driver which aims to reduce delay times for turn-on and turn-off without affecting either the current or voltage commutations.

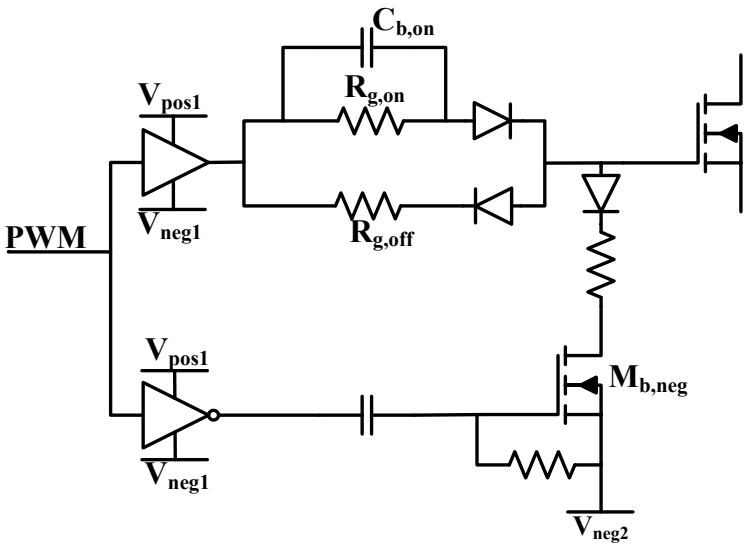


Figure 7.1: Schematic diagram of the proposed adaptive gate driver.

To reduce the delay time during turn-on, the boost capacitor from the RC driver is used. Compared to the multistage driver, the number of voltage levels in the gate driver is reduced as V_{pos2} will not be needed, thus making a simpler PCB design and implementation. For turn-off, the boosting stage from the multistage driver is used. However, only including the boosting stage is not sufficient; the boost voltage must be made adaptive as well to provide the largest possible reduction in delay time.

For design purposes of the adaptive gate driver, only the load current dependency is considered. Hence, it is assumed that the gate driver is operated under constant temperature conditions. Implementing junction temperature dependency can be possible at a later stage.

7.2 Adaptive boost voltage control circuit

To realize the adaptive boost voltage, a control circuit is created. The control circuit takes in load current measurement and provides a reference for the boost voltage. Ideally, the curves provided in Figure (5.6) for the adaptive boost voltage levels should be recreated.

The proposed control circuitry is shown in Figure (7.2). In the control circuit, the load current measurement provides an input voltage, V_{in}, proportional to the load current magnitude. This can either be done by using a current transducer that directly gives an output voltage, or, as indicated in Figure (7.2), using a current transducer that gives a current signal and a resistor R_{in} to provide the desired input voltage.

The operational amplifier (opamp) in the circuit operates as an inverting amplifier with a gain of $-R_2/R_1$. As V_{neg2} should increase with increasing load current, it is desired to have positive values for $V_{op,out}$ for positive load currents. Hence, $V_{op,in}$ and V_{in} must

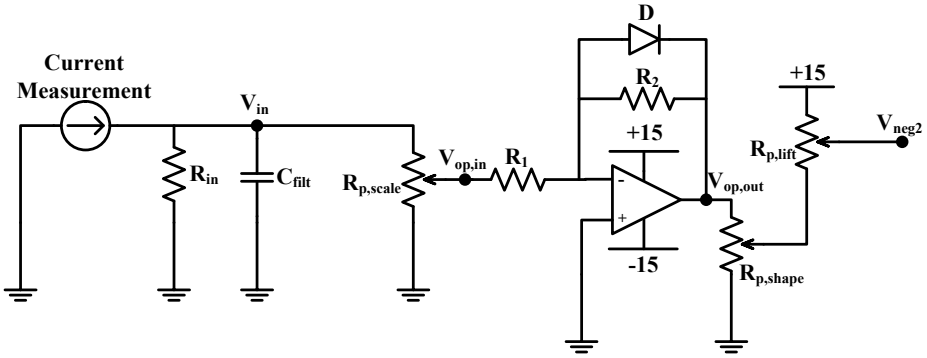


Figure 7.2: Schematic diagram of the boost voltage control circuit.

therefore have a negative correlation with the load current. As most current transducers have a positive correlation between the current measurement and the output signal, the direction of the current measurement must be chosen to be positive for negative load currents.

To ensure safe operation, it is desired that the allowed range for the boost voltage is limited. This means that for load currents that are higher than the maximum allowed load current, the boost voltage should be saturated at the highest allowed value. Similar for low load currents, where the boost voltage should be saturated at the lowest allowed value. To provide the upper and lower limit for the boost voltage, the tuning of the potentiometer $R_{p,scale}$ and the gain over the opamp is chosen so that $V_{op,out}$ reaches the saturation level of +15 V for the maximum allowed load current. For negative load currents however, $V_{op,in}$ will become positive and the diode D becomes forward bias thus giving zero gain. Hence, $V_{op,out}$ is limited between 0 and +15 V in the allowed current range as indicated in Figure (7.3).

Shaping V_{neg2} from $V_{op,out}$ is done by the potentiometers $R_{p,shape}$ and $R_{p,lift}$. Here, potentiometers have been used as they give the opportunity to tune the control circuit after the PCB have been produced. First, $R_{p,shape}$ reduces the signal from $V_{op,out}$ and decides the slope it has with reference to load current. Then, $R_{p,lift}$ lifts the signal up to the desired boost voltage level to give the reference for V_{neg2}. The voltage levels in the adaptive voltage control circuit is illustrated in Figure (7.3).

7.3 PCB design

One of the project goals in this master thesis was to design and produce a new PCB to test the adaptive gate driver. As the PCB used for tests in Chapter 5 provides every possibility except the adaptive boost voltage, only the adaptive boost voltage control circuit have been implemented on a new PCB while modifications have been made to the existing PCB to allow the two boards to be connected.

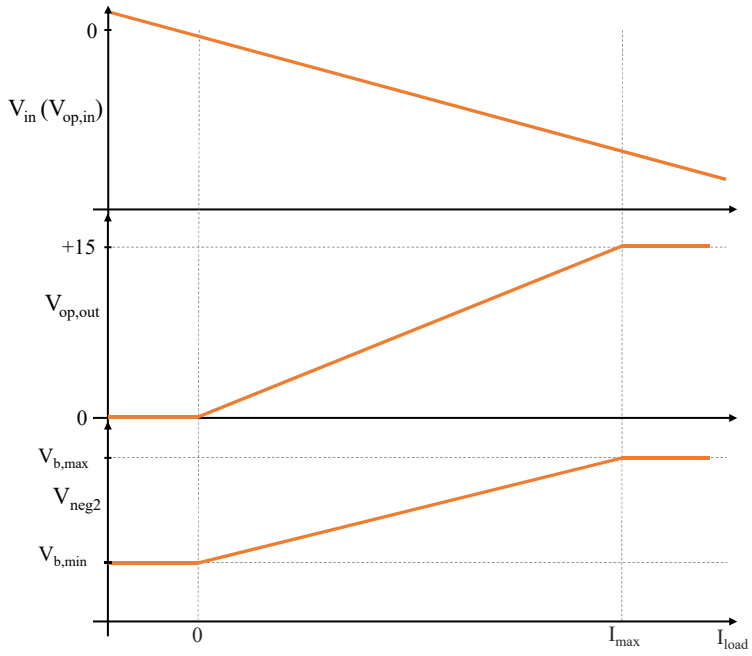


Figure 7.3: Voltage levels in the control circuit.

7.3.1 Prototype

Initially, a prototype was made on a veroboard to test the operation principle of the adaptive boost voltage control circuit. The prototype is shown in Figure (7.4). For current measurements, a LEM LT 300-S current transducer was used. The transducer gives an output current signal with amplitude 1/2000 of the measured current amplitude. However, as the wire was twisted five times around the transducer, the effective ratio was 1/400.

The component selection is listed in Table (7.1). The input resistor is chosen to be 47 Ω which gives an input voltage of -3.53 V for the maximum load current of 30 A. $R_{p,scale}$ is tuned to give $V_{op,in}$ equal to -3 V at 30 A load current. With a gain of -5 over the opamp, this makes the output voltage from the opamp reach the saturation level of +15 V as intended.

To ease the tuning of the output reference V_{neg2}, the potentiometer $R_{p,lift}$ is chosen to be 20 times larger than $R_{p,shape}$. With this choice, $R_{p,shape}$ and $R_{p,lift}$ can be tuned almost independently as most of the voltage from the +15 V voltage supply connected to $R_{p,lift}$ will be over that potentiometer. This will also make it easier to predict the output voltage from the control circuit through calculations. Choosing differently, for example with $R_{p,shape}$ and $R_{p,lift}$ to be equal makes the tuning more challenging as the voltage from the +15 voltage supply will be divided more equally between $R_{p,shape}$ and $R_{p,lift}$.

The prototype and the PCB with the power circuit have been connected so that the ground level on the prototype is connected to the negative driving voltage, V_{neg1}, on the

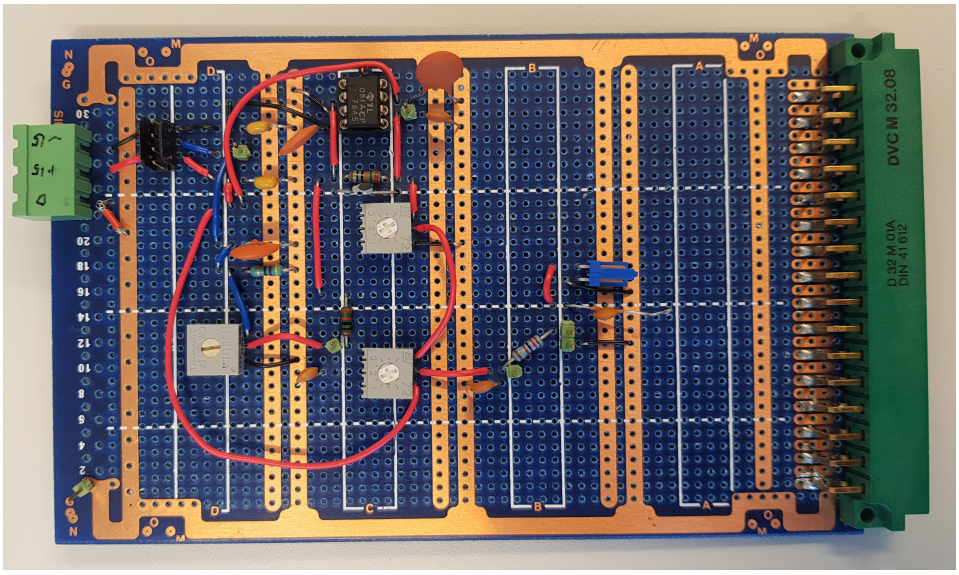


Figure 7.4: Prototype of the boost voltage control circuit.

Table 7.1: Component selection for the adaptive boost voltage control circuit.

Component	Value	Unit
R_{in}	47	Ω
C_{filt}	10	nF
$R_{p,scale}$	0-10	kΩ
R_1	20	kΩ
R_2	100	kΩ
$R_{p,shape}$	0-10	kΩ
$R_{p,lift}$	0-200	kΩ

PCB and the output signal is connected to the V_{neg2} reference. Steady-state results are obtained when a DC source instead of the LEM transducer is connected to the input port on the prototype. The boost voltage measured on the PCB is presented in Figure (7.5) together with the calculated values from an Excel spread sheet and the ideal boost voltage at junction temperature 25°C which were found in Chapter 5. Even though the prototype is not properly tuned, the figure show that the calculations provide a good estimate of the real boost voltage and can therefore be used for tuning purposes.

7.3.2 Design considerations

When designing the adaptive boost voltage control circuit there are two main concerns, high frequency noise and the dynamic response of opamps.

At each switching incident, the fast switching transients of the SiC MOSFET creates high frequency noise that pollutes the voltage levels in the adaptive boost voltage circuit.

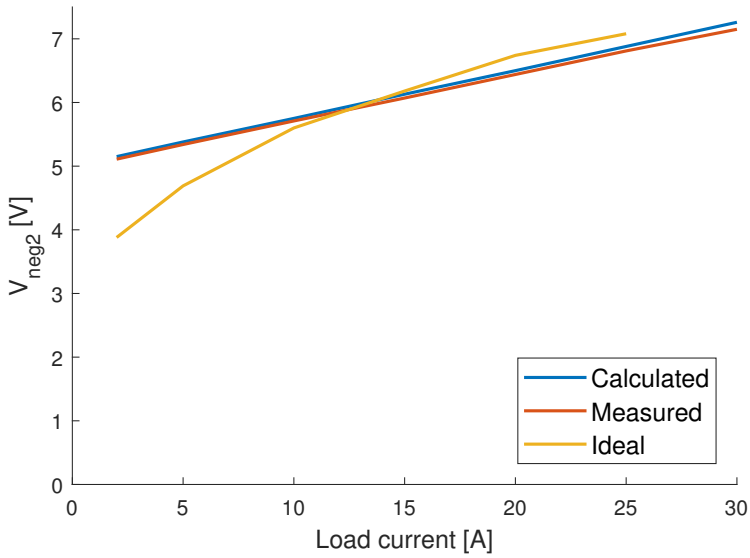


Figure 7.5: Adaptive boost voltages at steady-state from prototype and the ideal boost voltages.

The noise is visible as high frequency ringing that dies out with some time constant at the connection points. To reduce the high frequency noise, capacitors are inserted between connection points and ground multiple places in the circuit. In addition, a small capacitor is added across the opamp. This creates a low-pass filter to ensure that the high frequency noise is not gained. The size of the capacitors have been carefully selected so that the ringing is reduced while not slowing down the response of the adaptive circuit. A list of the inserted capacitors is given in Table (7.2).

Table 7.2: Capacitor inserted to suppress high frequency noise.

Connected from	Connected to	Size
$V_{op,in}$	GND	1nF
Opamp - input	$V_{op,out}$	10pF
$V_{op,out}$	GND	100pF
V_{neg2}	GND	100pF

The dynamic performance is important when choosing the opamp to be used in the adaptive boost voltage circuit. Depending on the application, the boost voltage might have to be able to follow fast changing load currents. In that case, high slew rate is desired when choosing the opamp. For the PCB that is created in this work, the TL071 by Texas Instruments was chosen. It has a slew rate of 13V/μs which gives a bandwidth of 3MHz [66].

7.3.3 PCB layout

The PCB have been designed using Autodesk EAGLE. The board design is shown in Figure (7.6).

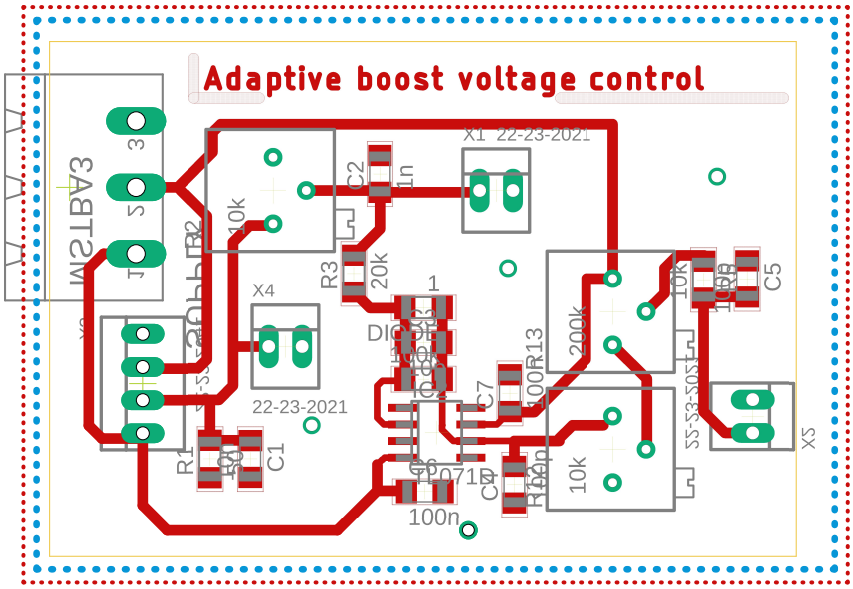


Figure 7.6: Screenshot of the PCB design in Autodesk EAGLE.

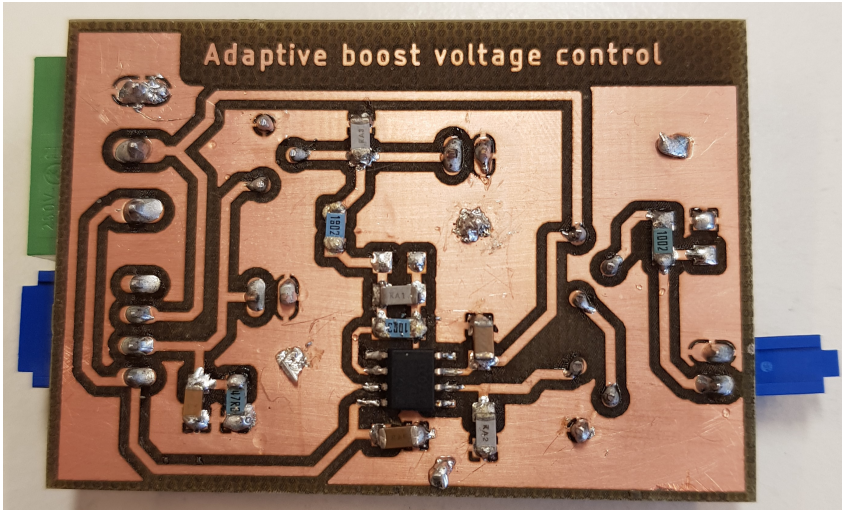
The PCB has a two-layer design. On the top layer, paths for the signal circuit have been made while the bottom layer is used for ground distribution. Resistors, capacitors, the diode D and the opamp are all surface mounted (SMD) components as this increases the PCB density. For source connections, potentiometers and the output port, hole mounted components have been chosen. The final PCB, after soldering, is shown in Figure (7.7).

7.4 Experimental validation

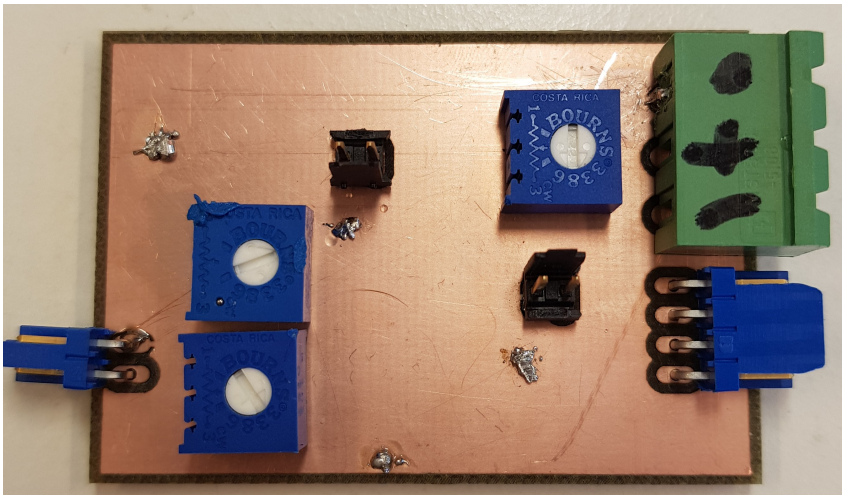
To evaluate the performance of the adaptive gate driver topology, the results in terms of delay time reduction is compared with the results that was obtained in Chapter 5 which is considered as the ideal results. As the turn-on results have already been evaluated as the RC driver, the presented results in this chapter will only focus on the turn-off stage with the adaptive boost voltage circuit.

7.4.1 Laboratory setup

The laboratory setup and equipment that is used is the same as was used for the experimental work in Chapter 5. The difference is that the adaptive boost voltage control circuit is



(a) Front.



(b) Backside.

Figure 7.7: The produced PCB after all components have been mounted.

added and connected to the boost voltage reference on the existing PCB. For current measurements, LEM LT 300-S current transducer is used. The lab setup is shown in Figure (7.8).

7.4.2 Method

As the adaptive boost voltage circuit gives a boost voltage that is linear with respect to load current, it cannot recreate the exact shape that was found to be the ideal boost voltage levels

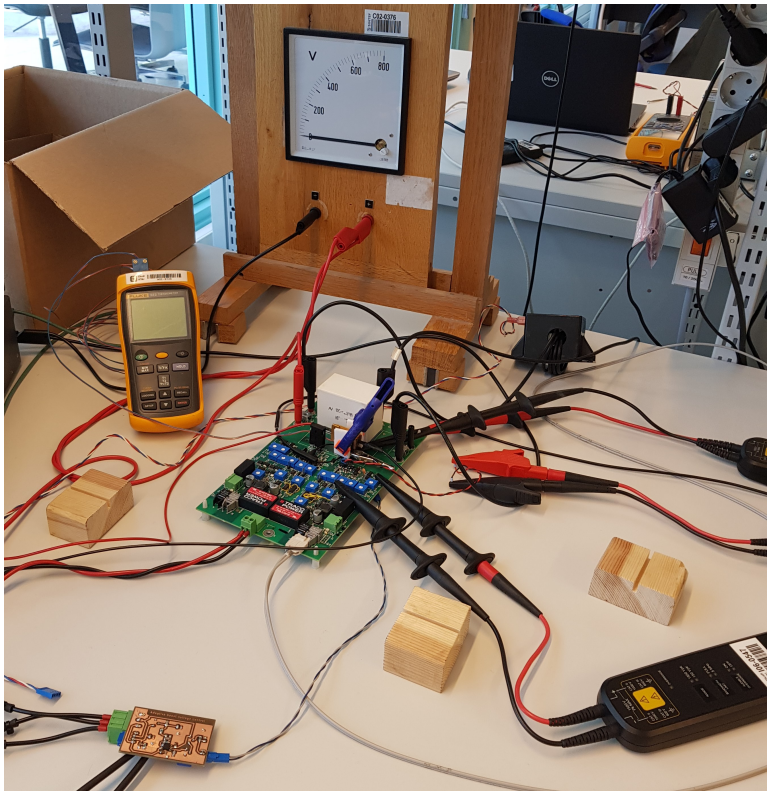


Figure 7.8: Laboratory setup used to evaluate the Adaptive boost voltage control circuit.

in Chapter 5. Therefore, the performance of the adaptive boost voltage control circuit have been evaluated using two different tuning strategies, referred to as tuning 1 and tuning 2. They are shown in Figure (7.9). In addition, the ideal boost voltages that was used for the adaptive multistage driver in Chapter 5 are shown in the figure.

For tuning strategy 1, the goal is to provide a boost voltage that is in the same range as the ideal levels for high load currents. The slope with respect to load current is tuned as steep as possible to avoid conflicts with the maximum commutation slope. As boost voltage is close to the ideal voltage levels for high load currents, the turn-off delay time is expected to be similar as for the adaptive multistage driver in this region. For lower load currents however, the delay time is expected to be higher than for the optimal tuning.

For tuning strategy 2, the goal is to provide the best possible reduction in delay time at low load currents. From Chapter 5 it was found that in this range the largest turn-off delay times was obtained which hence was dimensioning when setting the dead time for the bridge leg in Chapter 6. Therefore, with tuning strategy 2, a boost voltage that is as close as possible to the ideal values for low load currents is desired. For high load currents however, the boost voltage will be higher than the ideal and the delay times are expected to increase compared to the adaptive multistage driver. However, as long as the delay times

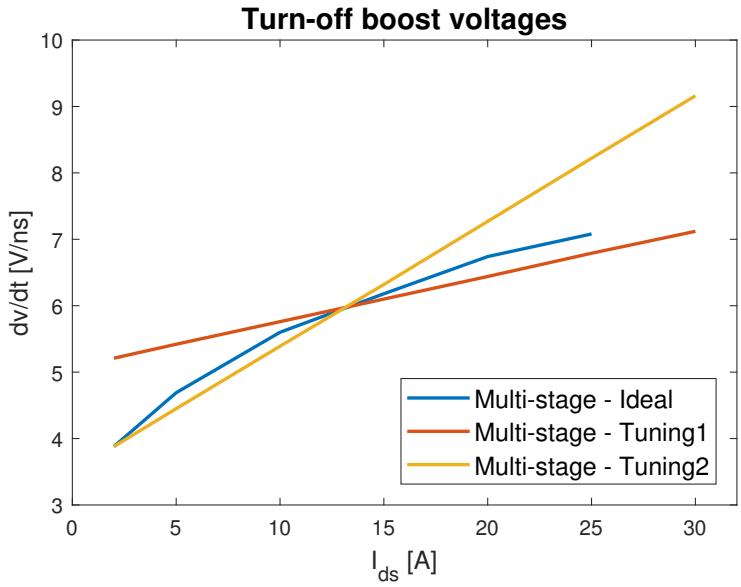


Figure 7.9: Steady-state turn-off boost voltages used for tuning strategy 1 and 2 compared with the ideal boost voltage values found in Chapter 5.

Table 7.3: Test matrix.

Tuning strategy	Transient	V_{dc}[V]	$T_j[°C]$	I_d[A]
1	Turn-off	600	25	2, 5, 10, 15, 20, 25
2	Turn-off	600	25	2, 5, 10, 15, 20, 25

at high load currents does not become larger than the ones at low load currents, they don't become dimensioning for the dead time, and best possible overall performance is achieved.

To be able to compare the results with the adaptive boost voltage circuit with the results from Chapter 5, the experimental validation is done by double pulse testing, similar as in Chapter 5. The test matrix is shown in Table 7.3.

During double-pulse testing, the load current increases rapidly to the desired value. The boost voltage control circuit does not react fast enough to follow these rapid changes in load current, and the current measurements can therefore not be used. However, in a motor drive application, the load current that the adaptive boost voltage circuit follows does not change as rapidly as during a double pulse test. Therefore, to validate that the adaptive boost voltage control is fast enough for a motor drive application, sinusoidal signals with frequency 50 Hz and 200 Hz and an amplitude that corresponds to the load current range have been applied to the input port. For the double pulse tests, instead of using the current transducer, the voltage levels that corresponds to the different load currents have been applied to the input port by a constant DC source.

7.4.3 Results

The turn-off boost voltage measured on the PCB is shown in Figure (7.10) when applying a sinusoidal signal with a frequency of 50 Hz and 200 Hz at the input port of the adaptive boost voltage control. In addition, the steady-state voltage levels for tuning case 2 from Figure (7.9) is included for comparison. As shown in the figure, the adaptive boost voltage circuit follows the input signal equally good for the 50 Hz signal and the 200 Hz signal. Compared to the steady-state boost voltage values it is seen that the correct boost voltage levels are provided in the dynamic response as well. Hence, Figure (7.10) shows that the adaptive boost voltage control circuit is fast enough and accurate enough to be used in a motor drive application.

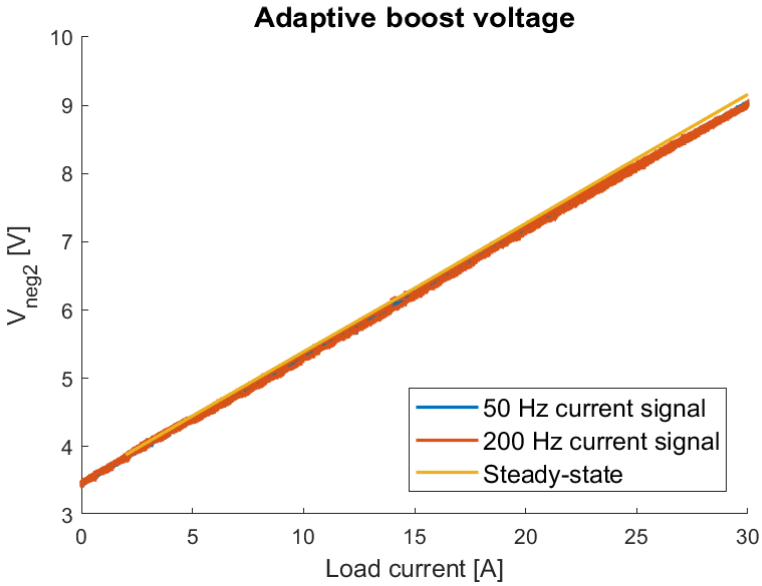


Figure 7.10: Turn-off boost voltage measured on the PCB when a 50 Hz signal and a 200 Hz signal is applied on the adaptive boost voltage circuit.

Figure (7.11) show the delay times that is obtained with the two tuning strategies and compared to the conventional gate driver and the adaptive multistage driver with the ideal boost voltage levels. Both tuning strategies provides delay times that in some regions are similar to the delay times obtained with the ideal tuning for the multistage driver.

For tuning strategy 1, the delay times are reduced with increasing load current. The performance is similar to the performance of the RC driver, but the turn-off delay times are shorter for low load currents. The largest delay time that is obtained is 166 ns at 2 A load current which is a 52 % improvement compared to the conventional gate driver.

For tuning strategy 2, the delay time at low load current is almost at the same level as with the ideal tuning. For large load current however, the delay time is larger than the delay times that was achieved with the ideal multistage driver and with tuning strategy 1. However, even though the delay time increases with load current for higher load currents

Table 7.4: Turn-off delay time improvements for the adaptive boost voltage control circuit for 2 A load current.

Driver	$T_{d,off}$	$\Delta T_{d,off}$	Improvement
Conventional	349 ns		
Multistage ideal	90 ns	259 ns	74 %
Multistage tuning 1	166	183	52 %
Multistage tuning 2	100	249	71 %

than 15 A, the delay time at 2 A load current is still the largest and will be dimensioning for the dead time requirement. A summary of the turn-off delay times and the improvements compared to CGD is provided in Table (7.4).

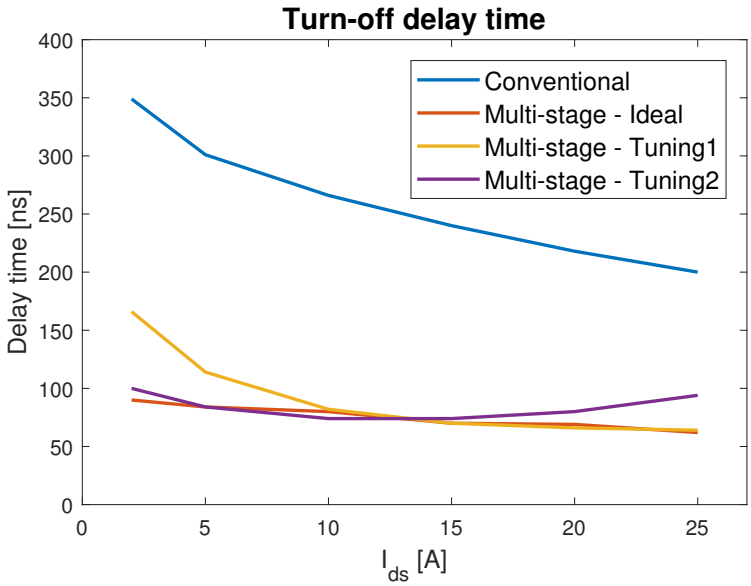


Figure 7.11: Turn-off delay times obtained with the two tuning strategies for the adaptive boost voltage circuit compared to the conventional driver and the ideal tuning of the multistage driver.

Chapter 8

Conclusion and further work

8.1 Conclusion

This master thesis has investigated gate drivers for wide band-gap (WBG) devices with focus on silicon carbide (SiC) MOSFETs. In general, WBG devices can switch faster, block higher voltages, have lower on-state resistance and operate under higher temperatures. These capabilities offer new possibilities in power electronic applications. However, to fully utilize the possible benefits from WBG devices, greater effort must be put into the design stage of the gate drivers.

The simulation model for the chosen SiC MOSFET in this master thesis, provided by the manufacturer, has a non-continuous behaviour. The non-continuous behaviour comes from the internal structure that aims to shape the transconductance according to the device gate-source voltage and junction temperature dependency. The model has been improved by replacing the non-continuous functionality with a continuous function that provides the same gate-source voltage and junction temperature dependency. Steady-state output characteristics for the initial and the proposed model have been investigated and compared to measurements for the actual device in lab. The proposed and the initial model provides equally good steady-state characteristics for all junction temperatures. However, with the proposed model, the convergence errors are avoided.

The conventional gate driver is the most commonly used gate driver topology as it benefits from its robustness and simplicity. In literature however, more advanced gate driver topologies are proposed. The proposed topologies can be divided into open loop and closed loop gate drivers. Most of the open loop gate drivers have a stage-wise design, meaning that they aim to control the different parts of the switching transients by different pre-defined stages of the driver. However, as they usually are based on timing, they are sensitive to variations in operation parameters such as load current or junction temperatures. For the closed-loop gate drivers however, the time delays in the feedback loops are the biggest concern as accuracy down to nanoseconds are needed to cope with the fast switching transients of SiC MOSFETs.

The multistage gate driver that is proposed in this master thesis is a two-stage gate

driver that aims for delay time minimization. Compared to other delay time minimization gate drivers that is found in literature, the multistage driver is voltage controlled rather than timing based which is more robust for fast switching devices. The operation principle of the multistage driver have been verified through experimental work with two different strategies for controlling the boost voltage level. In the adaptive solution, the boost voltage level is made adaptive based on the load current and junction temperature while in the fixed solution the boost voltage level is fixed at a constant value that is chosen based on the worst operation point.

The results in terms of delay times for the multistage driver is compared to a conventional gate driver and the RC driver. Both the fixed and the adaptive multistage driver outperforms the conventional gate driver in terms of delay time, both for turn-on and turn-off switching transients. Compared to the RC driver however, only the adaptive multistage driver provides lower delay times and only for turn-off. For turn-on transients however, the junction temperature dependency of the threshold voltage does not make a large enough impact to give the adaptive solution an advantage over the RC driver in terms of reduced delay time. The fixed multistage driver and the RC driver must both be tuned for the worst operating point. Moreover, both provides similar delay times for both turn-on and turn-off. Hence, the added complexity from the fixed multistage driver can be avoided as the much simpler RC driver performs equally. The delay time improvement from using CGD to using the multistage driver was 71 % at turn-on.

Turn-off switching transients are highly influenced by both variations in load current and junction temperature. This gives an advantage for the adaptive multistage driver as it can adapt to the different operation points. By tuning the turn-off boost voltage to the lowest possible voltage value without affecting the commutation slopes, the smallest possible delay time is achieved. The worst operation point for turn-off delay time is for low load currents and high junction temperatures. In the experimental work, the delay time using CGD was 409 ns at 2 A load current and 125°C junction temperature. For the adaptive multistage driver, the delay time is reduced to 108 ns at the same conditions which is an improvement of 74%.

The dead time requirement and the minimum pulse width when switching a bridge leg depends on the commutation slopes and the turn-off delay time. By using the multistage driver, both the dead time requirement and the minimum pulse width can be reduced. When reducing the minimum pulse width, more voltage pulses are realized in the converter. This gives a more linear response for the output line voltage for high modulation indexes. Moreover, because of the reduced dead time, the harmonics in the output current are reduced in the linear region. When switching at 15 kHz, the linear region can be increased by up to 3.8 % and the THD in the linear region reduced by up to 7.7 % when using the multistage driver instead of the conventional gate driver.

Realizing the adaptive multistage driver based on load current measurements was the final stage of this master thesis. To do so, the adaptive boost voltage control circuit was designed and produced on a PCB. The circuit takes in load current measurements and provides a linear output voltage that is used as the reference for the turn-off boost voltage on the existing gate driver prototype. By properly tuning the circuit, the delay time can be reduced similarly as for the adaptive multistage driver. In the presented results, the best tuning strategy provided a 71 % reduction in turn-off delay time which is close to the 74%

reduction that was obtained in the ideal case.

8.2 Further work

In this master thesis the load current and junction temperature dependency have been investigated in detail. The work have shown that for turn-off, the best boost voltage that can be used in the multistage driver will vary both with load current and junction temperature. However, the adaptive boost voltage control circuit does only consider changes in load current and assumes a constant junction temperature. In the future work, junction temperature dependency should be implemented as well. Moreover, further tuning of the adaptive boost voltage control should be done to realize the best possible reduction in delay time.

The impact that a delay time minimization gate driver have on the voltage and current quality in a converter have been investigated through simulations. In the further work, the gate driver that was suggested in Chapter 7 should be realized on a PCB. The PCB should be tested in an actual motor drive application to verify the simulation results in terms of voltage and current quality compared to a conventional gate driver.

A summary of the proposed further work is listed below:

- Further tuning of the adaptive boost voltage control circuit
- Implement junction temperature dependency for the adaptive boost voltage control circuit
- Realize a gate driver with a boost capacitor at turn-on and the adaptive boost voltage at turn-off on a PCB
- Verify the impact from a delay time minimization gate driver in a motor drive application through laboratory work

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Appendix A

Publications

A.1 ECCE Asia 2019

The following paper have been presented at ICPE2019 10^{th} international conference on power electronics - ECCE Asia in Busan, South Korea 27.-30. May 2019.

Minimization of dead time effect on bridge converter output voltage quality by use of advanced gate drivers

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***Abstract*—This paper presents a voltage-controlled multistage gate driver topology for delay time minimization that improves the converter output voltage quality while supplying a motor load. Three gate driver topologies for SiC MOSFETs are compared based on their dead time requirement in a bridge leg converter. Experimental results of the gate driver delay times are reported and are used as input to a simulated motor drive application. Results show that turn-off delay times can be reduced by up to 74 % for the multistage driver compared to the conventional counterpart when the rate of change for the converter voltage output is limited to 10 V/ns. Furthermore, minimizing the dead time increases the linearity region of the output voltage from the converter by 1.8 % to 3.8 % and reduces the current THD in the linear region by up to 7.7 % when switching at 15 kHz.**

***Index Terms*—Gate driver, wide band-gap, SiC MOSFET, dead time**

I. Introduction

Wide band-gap (WBG) semiconductor devices, such as silicon carbide (SiC) and gallium nitride (GaN) are commercially available and continue to increase their market share. Compared to their silicon (Si) counterparts, they enable faster switching, lower on-state resistance, higher blocking voltages and operation under higher temperatures [1]. Among the two, SiC is currently the most mature technology and it is assumed that SiC devices will take large market shares in high voltage and high power segments within the power electronic markets in the years to come [2], [3].

In motor drives, voltage-source inverters (VSI) are commonly used. A typical setup with a converter fed motor load is shown in Fig. 1. Replacing Si IGBTs with SiC MOSFETs of similar rating can improve converter performance in several ways. As the forward voltage drop of IGBTs are eliminated in MOSFETs, the conduction losses are reduced. Moreover, in motor drives, the switching frequency can be increased while having the same total switching losses as tail current losses are eliminated using SiC MOSFETs [4]. Yet, the switching speed cannot be increased as the cable length, winding insulation and induced bearing currents limit the maximum allowable dv/dt from the converter [5]. Furthermore, slowing down the SiC MOSFET to the same speed as IGBT results in larger turn-on and turn-off delay times ($T_{d,on}$ and $T_{d,off}$) and thus higher dead time (T_{dt}) requirement when using traditional gate drivers.

A. Dead time

To avoid shoot through when switching a bridge leg, a dead time where both switches are turned off must be added as indicated in Fig. 2. The dead time must be large enough so that the conducting switch is turned completely off before it is safe to turn on the complementary switch. In addition, a safety margin is usually added to ensure that the switch will not be turned back on due to the Miller effect when turning on the complementary switch. The minimum dead time is given by Eq. 1 where $T_{dv/dt}$ and $T_{di/dt}$ is the voltage and current commutations and T_{safe} is the added safety margin.

$$T_{dt} = T_{d,off} + T_{dv/dt} + T_{di/dt} + T_{safe} \tag{1}$$

Due to the Miller plateau's dependency on load current and junction temperature, $T_{d,off}$ and, thus, the dead time requirement will depend on the load current and junction temperature as well. Usually, the dead time is set based on the operating point with the largest dead time requirement. However, load current dependent dead time can be decreased by adaptive gate driving [6].

During dead time, the load current will be freewheeling through the anti-parallel diode of either the upper or the lower switch. For a positive load current, it must conduct through the lower anti-parallel diode thus dragging the bridge leg midpoint down to the negative DC-link voltage. Likewise for a negative load current that must conduct through the upper anti-parallel diode thus dragging the bridge leg midpoint up to the positive DC-link voltage. This gives voltage pulses that are load current dependent as shown in Fig. 2. Furthermore, if the body diode of SiC MOSFETs are used as anti-parallel diodes instead of an external Si power diode, the conduction losses during

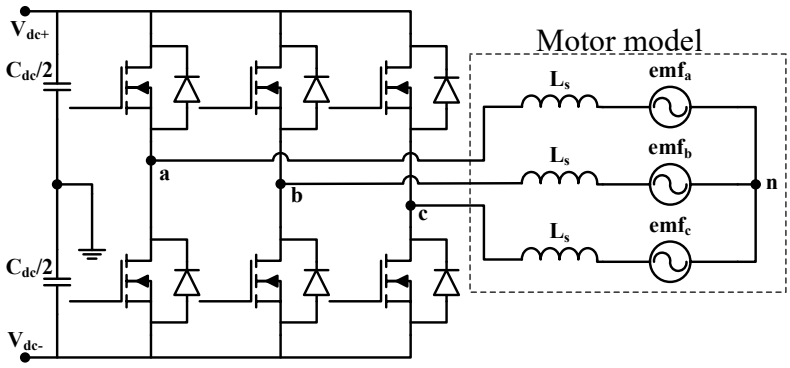

Fig. 1: Schematic diagram of a three phase inverter and the equivalent motor model.

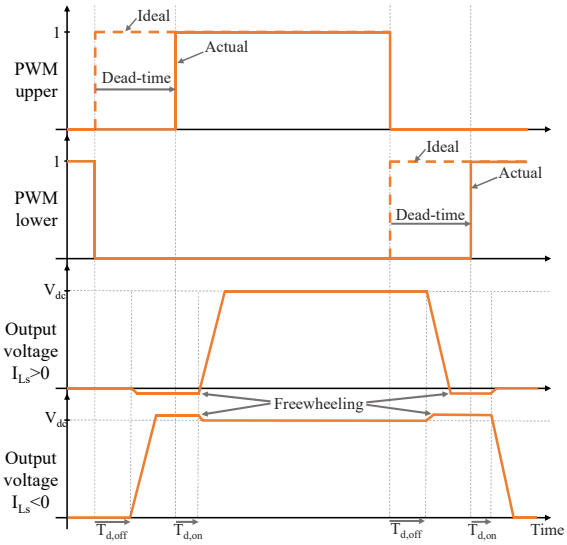

Fig. 2: Theoretical waveforms showing the impact from dead time in a bridge leg.

freewheeling are increased due to the higher forward voltage drop of WBG devices. Hence, minimizing dead time could increase the efficiency as well as the output voltage quality.

The dead time will affect the minimum pulse width (MPW) that can be allowed in PWM modulation. All PWM pulses shorter than MPW are blanked out. Thus, large dead times results in distorted voltage output that is further away from the ideal shape [6], [7].

This paper proposes an advanced multistage gate driver topology designed for minimizing the dead time requirement and investigates the impact from gate drivers on delay times and thus dead time requirements in a motor drive application. Firstly, three different gate driver topologies are presented and experimental results for minimal delay times are reported. Furthermore, the experimental results are transferred to a motor drive application to assess the impact of the gate drivers. Simulations are performed where the motor drive is controlled using three widespread PWM modulation techniques both for a conventional type gate driver and the multistage gate driver. Improvements of the output voltage quality and the THD of the line current are reported.

II. Gate Drivers

A gate driver is the circuitry that controls the turn-on and turn-off switching transients of a transistor. This section presents the three gate driver topologies that are validated experimentally.

The speed of the switching transient is determined according to the gate current delivered to the switching device [8], [9]. The most commonly used gate driver, termed conventional gate driver (CGD) in this paper, is shown in Fig. 3a. Its simplicity makes it an attractive solution, but it has limited degrees of freedom. It consists of a buffer stage with separate gate resistors for turn-on and turn-off. The gate resistor is usually chosen to meet the dv/dt limit for the application. However, as the delay times depends on the time constant created by the gate resistor and the input capacitor of the MOSFET, a large gate resistor gives large time delays thus increasing the requirements for dead time and MPW.

Several other gate driver concepts are found in the literature. A slightly more complex driver shown in Fig. 3b, termed RC driver in this paper, gives a new degree of freedom that boosts the gate current in the initial phase of the switching transient. The initial boost can be used to counter the delay time or even increase the switching speed [10] depending on the size of the chosen boost capacitor. In the experimental validation in this paper, the size of the boost capacitors is chosen to act on the delay times without affecting dv/dt or di/dt.

More complex gate drivers aims to act more directly on the switching transient by providing different gate resistors for the different stages within the switching event. The goal could be reduced switching losses without increasing the

current overshoot by boosting the voltage commutation [11], or achieving separate control of dv/dt and di/dt [12], [13], [14]. However, as they are all based on timing, variation in operation parameters such as temperature and load current can challenge their potential. Dynamic closed-loop gate drivers able to control delay times, dv/dt and di/dt separately have been presented for high power Si IGBTs [15]. However, for SiC MOSFETs, the driver will have challenges related to the bandwidth due to the larger time constants of Si IGBTs. A similar closed-loop gate driver created for SiC MOSFETs is presented in [16]. Yet, even though the gate driver is designed for SiC MOSFETs, the highest presented dv/dt target is 4V/ns, which is in the same range as for Si IGBTs.

The multistage driver, shown in Fig. 3c, is a driver concept aiming at minimizing delay times during a switching transient [9]. The driver is a two-stage driver with a conventional stage, similar to a conventional driver, and a boosting stage with boost voltages V_{pos2} for turn-on and V_{neg2} for turn-off. The operational principle is that for a turn-on or turn-off event, the MOSFET in the boosting stage of the driver $M_{b,***}$ will be turned on quickly to provide a low resistive path from the boost voltage to the gate. This allows for a large initial gate current that will charge or discharge the gate faster thus reducing delay times as seen in Figs. 4a and 4b for turn-off and turn-on respectively. For turn-off, diode D_2 will become reverse biased when the gate voltage equals V_{neg2} thus turning off the boosting stage. The rest of the switching stage is then controlled by the conventional part. By choosing V_{neg2} equal to the Miller plateau, the best possible reduction in turn-off delay time can be achieved without changing dv/dt. For turn-on transients, the diode, D_1, will become reverse biased when the gate voltage equals V_{pos2}. Hence, by choosing V_{pos2} so that D_1 blocks when the gate is at the threshold voltage, the best possible reduction in turn-on delay time is achieved without affecting di/dt.

Due to the diodes D_1 and D_2, the multistage driver can be considered to be voltage controlled. As long as the boost voltages are properly chosen, this is considered to be more robust than controlling the driver by timing due to manufacturing tolerances of passive components.

The operation principles of the multistage driver and the RC driver are quite similar. However, the boost capacitor in the RC driver is fixed and must be tuned for the worst-case operating point. While for the multistage driver, V_{pos2} and V_{neg2} can be chosen to be optimal at each operation point, thus, reducing the effect of load current and junction temperature dependent delay times. Yet, choosing optimal boost voltages based on the operation point requires measurements and functionality that allows the boost voltages to be changed dynamically. If such functionality is not implemented, V_{pos2} and V_{neg2} must be fixed and the tuning is similarly done for the worst-case operating point.

III. Experimental Validation of Driver Topologies

The three different gate driver topologies shown in Fig. 3 are tested experimentally and compared in terms of delay time for changing operational parameters.

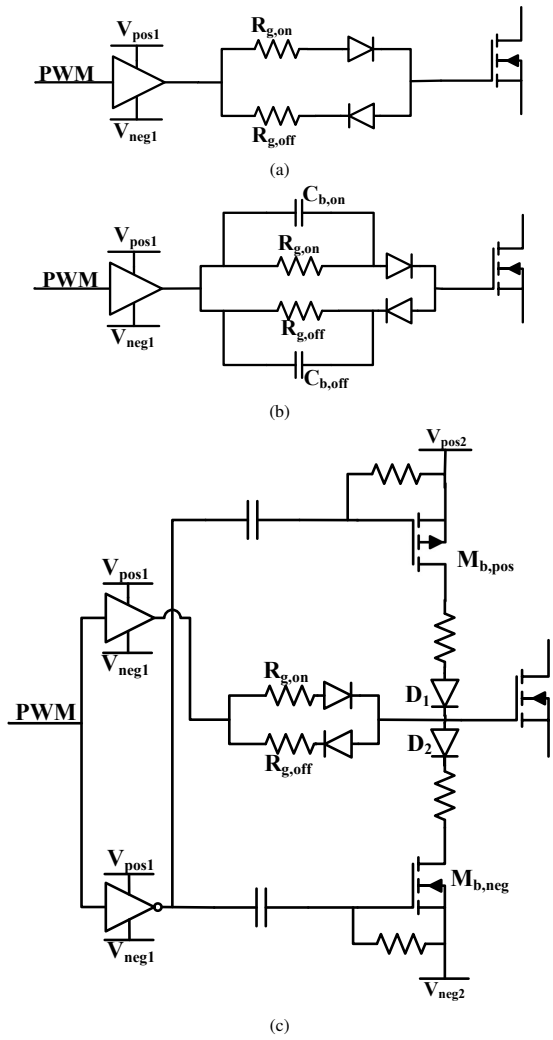

Fig. 3: Schematic diagrams of driver topologies. a) Conventional driver, b) RC driver and c) multistage driver.

A PCB with the possibility to test all three driver topologies was created and tested in the setup shown in Fig. 4c. In the tests, the gate resistors have been held constant while boost capacitors have been added for tests of the RC driver and the boosting stage is added for tests of the multistage driver. The waveforms in Fig. 4 verifies the driver concept for the multistage driver.

The reported results are obtained by double pulse testing of SiC MOSFET C3M007512K from Wolfspeed [17] in a halfbridge configuration with an inductive load. Waveforms are recorded using a Tektronix DPO 5104B 1 GHz oscillo-

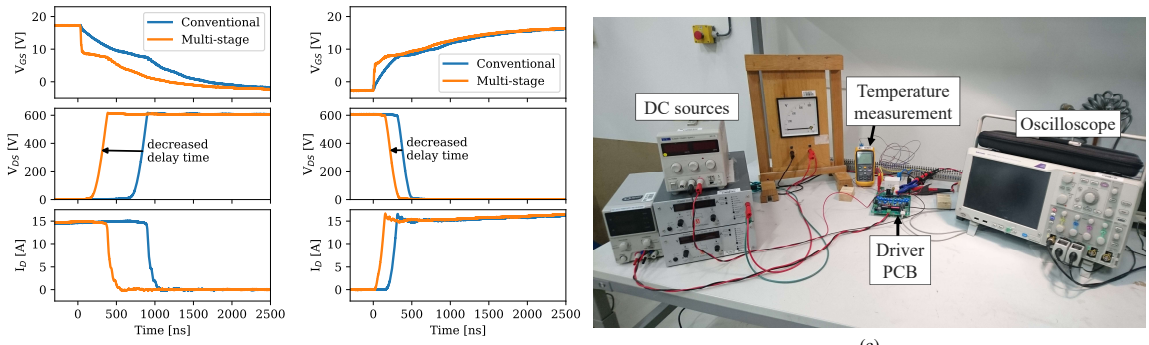

Fig. 4: Experimental waveforms verifying the driver concept. Delay times are reduced while di/dt and dv/dt are unchanged. a) Turn-off, b) Turn-on and c) Test setup.

TABLE I: Test parameters.

Driver	dv/dt	$R_{g,on/off}$	$C_{b,on/off}$	$V_{pos2/neg2}$
Conventional	10 V/ns	103/150 Ω		
RC driver	10 V/ns	103/150 Ω	470/1500 pF	
Multistage	10 V/ns	103/150 Ω		4.9/7.1 V

scope, Tektronix THDP0200 200 MHz voltage probes and a Rogowski PEM CWT06 30 MHz current probe. Time delays of the probes have been compensated according to their datasheet values. Junction temperature control is done by controlling the temperature of the drain metal on the back of the MOSFET die. The temperature is measured with a T-type thermocouple.

The turn-on delay times only depend on the threshold voltage of the SiC MOSFET, which in turn is junction temperature dependent. Hence, the results reported for turn-on is presented by the junction temperature dependency at a constant load current of 15 A. Turn-off delay times, however, depends on the Miller plateau which is affected by both the junction temperature and the load current. Hence, the turn-off results are presented both with the load current and junction temperature dependency.

To provide representative results for a motor drive application, a target dv/dt of 10 V/ns is chosen as this could be a typical value for applications with fast switching Si IGBTs. The circuit parameters are presented in Table I.

Two strategies for controlling the boost voltages V_{pos2} and V_{neg2} have been investigated. The boost voltages can either be fixed at a constant voltage level or optimized at each operation point to provide the largest reduction in delay time without affecting dv/dt or di/dt. The fixed solution is referred to as the fixed multistage driver while the solution with optimized boost voltages is referred to as the adaptive multistage driver. The boost voltages presented in Table I is used for the fixed multistage driver.

If the fixed solution is chosen, the voltage levels must be fixed according to worst case. For turn-off, as V_{neg2} ideally should be as low as possible to give a high initial gate current, worst case will be for low junction temperatures and high load currents due to the high location of the Miller plateau at that operation point. V_{neg2} is therefore fixed at 7.1 V in the reported results. For turn-on, the datasheet gives that threshold voltage is reduced by approximately 0.5 V from junction temperature 25 °C to 125 °C [17]. Hence, as V_{pos2} ideally should be as high as possible, worst case is for high temperatures. V_{pos2} is therefore fixed at 4.9 V in the reported results for the fixed multistage driver. Choosing the size for the boost capacitors in the RC driver must be done for the same operation points and dimensioned so that dv/dt and di/dt are not affected.

Fig. 5a shows the minimum delay times achieved for turn-off with different gate drivers at a junction temperature of 25 °C. The delay times for all drivers are reduced with increasing load current as the Miller plateau is located at higher gate voltage levels. The possible reduction in delay time when going from the conventional driver to the fixed multistage is approximately 100 ns for low currents and 150 ns for high currents. If the RC driver is used, the improvement is similar for low currents. For high currents however, the RC driver gives shorter delay times than the multistage driver. However, due to the available discrete values, the capacitor used to obtain the results is chosen to be a bit too large and dv/dt is slightly affected for high currents. If the capacitor is chosen smaller so that dv/dt was unchanged, the improvement in delay time would be similar to the fixed multistage driver.

The largest improvement in delay time for turn-off is found when using the adaptive multistage driver as seen in Fig. 5a. The improvement is found to be 259 ns or 74 % for low load currents at 25 °C junction temperature. When setting the dead time in a bridge leg, the worst delay time will be the design parameter. Hence, by changing from a conventional driver to a multistage driver with adaptive boost voltage, the dead time can be reduced by 259 ns. The delay times for all drivers at turn-off and 25 °C are presented in Table II.

Turn-on delay times are shown in Fig. 5b. The improvement in delay time when going from the conventional driver to the

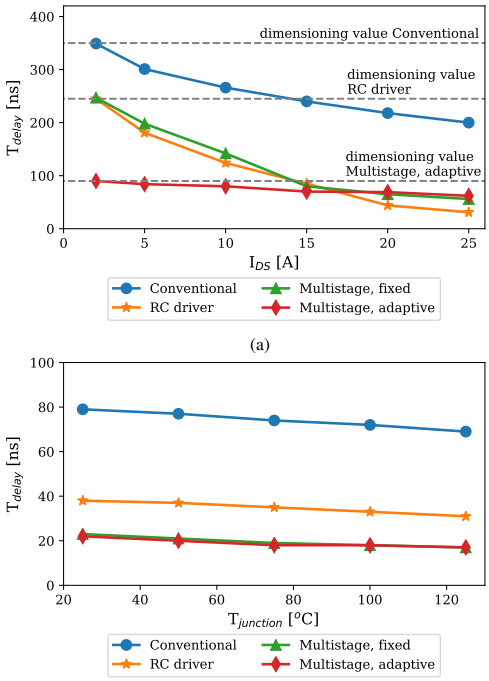

Fig. 5: Experimental results for delay times using different drivers. a) Turn-off, b) Turn-on.

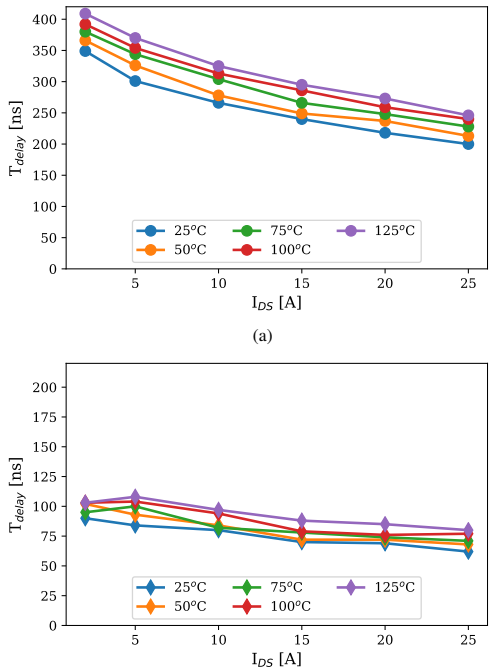

Fig. 6: Experimental results for delay times at different junction temperatures with a) conventional gate driver and b) adaptive multistage driver.

TABLE II: Turn-off delay time improvements at 25 °C.

Driver	$T_{d,off}$	$\Delta T_{d,off}$	Improvement
Conventional	349 ns		
RC driver	245 ns	104 ns	30 %
Multistage fixed	247 ns	102 ns	29 %
Multistage adaptive	90 ns	259 ns	74 %

fixed multistage driver is 56 ns or 71 % for 25 °C junction temperature. If the adaptive multistage driver is used, the improvement is 57 ns or 72 % for the same junction temperature. A similar percent-wise improvement is found for the rest of the tested junction temperatures as well, both for the fixed and adaptive multistage drivers. Due to the relatively low difference in threshold voltage at 25 °C and 125 °C, the performance from the fixed and adaptive multistage driver is very similar.

TABLE III: Turn-on delay time improvements.

Driver	$T_{d,on}$	$\Delta T_{d,on}$	Improvement
Conventional	79 ns		
RC driver	38 ns	41 ns	52 %
Multistage fixed	23 ns	56 ns	71 %
Multistage adaptive	22 ns	57 ns	72 %

For the RC driver, the improvement in delay time at 25 °C was 41 ns or 52 %. However, due to the available discrete capacitor values, the result is not ideal. An improvement in delay time more equal to the one obtained with the multistage drivers can be expected if the best choice for the boost capacitor is made. Hence, the added complexity from introducing the multistage driver can be reduced for turn-on by only consider the RC driver instead. Turn-on delay time improvements for the worst operation point, i.e at the lowest tested junction temperature is presented in Table III.

As the Miller plateau is lowered for increasing junction temperature for the same load current, the turn-off delay times increases with increasing temperature. For the conventional gate driver, the delay times are shown in Fig. 6a. At 2 A the delay time is increased by 60 ns when the junction temperature increases from 25 °C to 125 °C. This increases the requirements for dead time if the application should have a safe operation at 125 °C.

Turn-off delay times when using the multistage driver with an adaptive boost voltage is shown in Fig. 6b. Similar as for the conventional driver, the delay times increases with temperature. The highest measured delay time is 108 ns at 125 °C junction temperature. The delay times at 125 °C is presented in Table IV.

TABLE IV: Turn-off delay time improvements at 125 °C.

Driver	$T_{d,off}$	$\Delta T_{d,off}$	Improvement
Conventional	409 ns		
Multistage adaptive	108 ns	301 ns	74 %

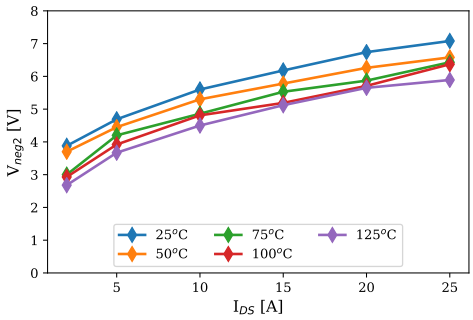

Fig. 7: Turn-off boost voltages at different junction temperatures and load currents for adaptive multistage driver.

To provide the largest possible reduction in delay time, the boost voltage in the multistage driver must be chosen optimally. When the Miller plateau is lowered due to increasing temperature or lower load current, a lower V_{neg2} without affecting dv/dt during turn-off is allowed hence increasing the effect of the boosting stage. Fig. 7 shows the optimal choice for boost voltages used for turn-off at the different operation points. If V_{neg2} is chosen to be fixed, thus using the fixed multistage driver, it must be chosen according to the highest operation temperature and load current. However, the results show that implementing the adaptive multistage driver by far gives the largest reduced delay times during turn-off. Therefore, the adaptive multistage driver is used as benchmark in the following parts of this paper.

IV. Effect of Dead Time on Different PWM Modulation Techniques

In PWM, the amplitude and frequency of the fundamental output voltage are controlled by comparing a control signal, V_c, to a triangular carrier, V_{tri}. Each inverter phase leg is controlled individually. The control signal V_c shapes the phase to neutral output voltage. For an AC output voltage, the control signal must have a fundamental part equal to the desired output voltage and with the desired frequency.

The ratio between the amplitude of the fundamental part of the control signal $\hat{V}_c$ and the triangular carrier wave $\hat{V}_{tri}$, is termed the modulation index M_a [8]:

$$M_a = \frac{\hat{V}_c}{\hat{V}_{tri}} \tag{2}$$

In addition to the fundamental part, triplen harmonics can be added to the control signal in a three-phase inverter as they are neutralised in the line voltage [18]. Furthermore, when the VSI drives a load with an isolated neutral point such as a motor, an arbitrary zero-sequence signal can be injected to the control signal in all phases [19], [20].

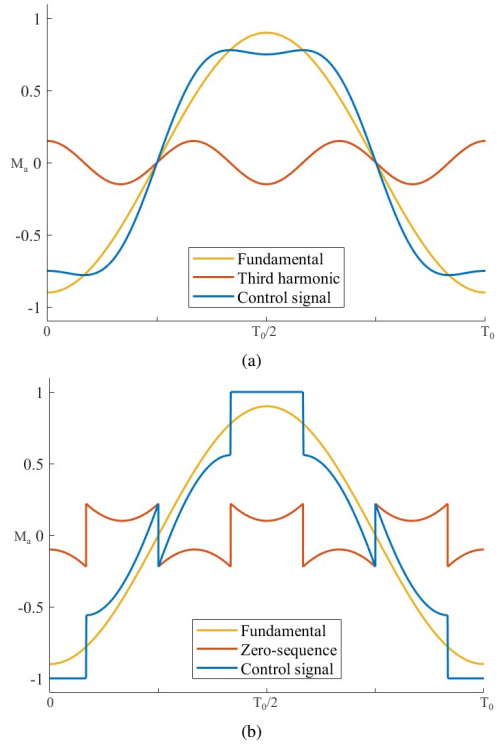

Fig. 8: PWM modulation techniques. a) THIPWM, b) DPWM, SPWM equals the fundamental signal.

A simple solution is to use a control signal consisting only of a sinusoidal wave, called SPWM. The control signal is shaped as $M_a sin(2\pi f_o t)$ resulting in the desired frequency, f_0 and amplitude, M_a. The SPWM technique is linear up to M_a equal to 1, after that overmodulation occurs [8].

By injecting a third harmonic signal to the control signal (THIPWM) as shown in Fig. 8a, the linear region for the line voltage can be increased. By choosing the amplitude to be 1/6 of the amplitude of the fundamental part, the linear region can be increased until $M_a = 1.15$. Thus, a 15 % higher output line voltage can be achieved without overmodulation [18].

Injecting a discontinuous zero-sequence signal to the control signal (DPWM) is suggested to improve the VSI performance in the overmodulation region in terms of voltage linearity and current harmonics [19], [21]. The control signal is shown in Fig. 8b for M_a equal to 0.9.

The control signal equals 1 in absolute amplitude for 1/3 of the period when using DPWM. This reduces the number of voltage pulses, and hence voltage commutations, for the same carrier frequency thus reducing switching losses. The carrier frequency can therefore be increased by a factor of 1.5 to have

TABLE V: Simulation parameters.

Driver	dv/dt	Dead time	Minimum pulse width
Conventional	10 V/ns	810 ns	2.43 µs
Multistage	10 V/ns	470 ns	1.41 µs

the same average switching frequency and switching losses as for the continuous PWM methods [19].

The impact of the multistage driver compared to a conventional driver have been investigated for a motor drive through simulations. The simulations have been done by building a MATLAB script. The simulation case is a motor drive application with a motor model and a VSI, similar to the setup shown in Fig. 1. The motor is assumed to be a round rotor 15 kW PM synchronous machine, supplied by a 600 V dc-link. The three different PWM modulation techniques, SPWM, THIPWM and DPWM, have been investigated with the conventional gate driver and the adaptive multistage driver.

The required dead time for the two drivers have been calculated according to Eq. 1 with the delay times obtained from the experimental work. The safety margin have been set to 200 ns and maximum dv/dt to 10 V/ns at the converter output. The MPW is set to be three times the dead time. All pulses shorter than the MPW are blanked out. Simulation parameters are presented in Table V.

Simulations are run with a carrier frequency of 15 kHz for SPWM and THIPWM. For DPWM, a carrier frequency which is 1.5 times higher, i.e. 22.5 kHz is used as previously described. The modulation index, M_a, is varied in the range from 0.8 to 1.5 to cover both the linear region and the overmodulation region [8]. For all modulation indices, the load current magnitude and the power factor have been held constant at 21.2 A rms (30 A peak) and 0.9 respectively.

To quantify the quality of the line current, total harmonic distortion (THD) is commonly used. If I_1 is the fundamental component and I_h is the h^{th} harmonic for $h \neq 1$, then THD is calculated as:

$$THD = \frac{\sqrt{\Sigma_{h=2}^{\infty} I_h^2}}{I_1} \tag{3}$$

Simulation results in terms of output line voltage and line current THD are shown in Figs. 9 and 10 respectively. When the conventional gate driver is used, a non-linear bubble shaped output voltage is observed in the last part of the theoretical linear region due to the minimum pulse width. The bubble starts at modulation index 0.92 for SPWM, 1.06 for THIPWM and 1.09 for DPWM. For control signals with an amplitude higher than these values, the voltage pulses are blanked out giving a higher fundamental component and voltage distortion. The distortion is visible in the current THD as well by a large peak for the same M_a as the line voltage becomes non-linear.

As shorter voltage pulses are accepted when using the multistage driver, the control signal is allowed to cross the triangular carrier wave at higher values before the pulses are blanked out. This increases the linear region for the output voltage and reduces the size of the observed bubble as

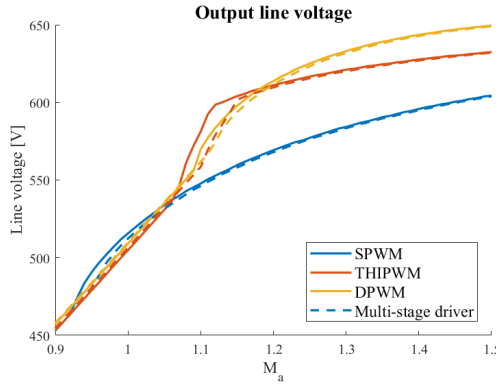

Fig. 9: Output peak line voltage for different PWM modulation techniques. Solid lines are from conventional gate driver while dotted lines are with the multistage driver.

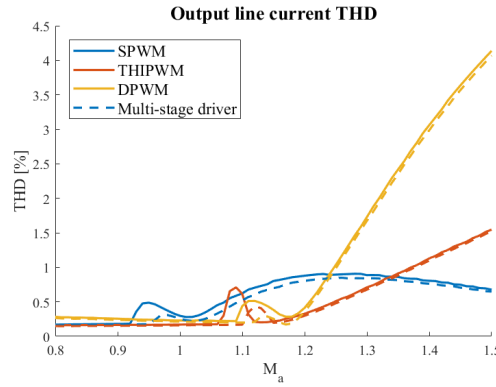

Fig. 10: Line current THD for different PWM modulation techniques. Solid lines are from conventional gate driver while dotted lines are with the multistage driver.

observed in Fig. 9. The linear regions are increased to 0.95 for SPWM, 1.10 for THIPWM and 1.11 for DPWM as presented in Table VI. The same trend is seen for the line current THD as the peak that is found when the voltage becomes non-linear is shifted towards higher modulation indices. At the same time, this peak is reduced.

Within the linear region, the peak output voltage when using the conventional gate driver and the multistage driver are similar. However, due to the reduced delay times for the multistage driver, the current freewheeling is reduced thus providing voltage shapes that are more equal to the ideal. With more ideal voltage pulses, the current harmonics are reduced and THD improved as presented in Table VI. When using DPWM, the improvement in current harmonics is found to be 7.7 % which is the largest improvement. However, DPWM is still the PWM method that creates most current harmonics in the linear region. For SPWM and THIPWM, which perform

TABLE VI: Maximum M_a and current THD for linear regions for different PWM methods.

	SPWM		THIPWM		DPWM	
Driver	$M_{a,max}$	THD	$M_{a,max}$	THD	$M_{a,max}$	THD
Conventional	0.92	0.18 %	1.06	0.17 %	1.09	0.25 %
Multistage	0.95	0.17 %	1.1	0.16 %	1.11	0.23 %
Improvement	3.3 %	5.1 %	3.8 %	6.6 %	1.8 %	7.7 %

more equal in the linear region, the reduction in THD were found to be 5.1 % and 6.6 % respectively.

V. Conclusion

An advanced multistage gate driver designed for delay time minimization was presented and compared experimentally to a conventional gate driver and a RC driver. Possible reduction in delay times and dead time requirements for the multistage driver and the RC driver were reported compared to the conventional gate driver. The experimental results showed a possible reduction in delay time of 71 % for turn-on and 74 % for turn-off while not affecting dv/dt or di/dt by changing from a conventional driver to the multistage driver with adaptive boost voltages. The reduction in required dead time was 42 %. Transferring the dead time reduction to a VSI in a motor drive application, the output voltage linearity region was increased by up to 3.8 % and the current THD reduced by up to 7.7 % in the linear region when using the multistage driver compared to the conventional counterpart. Hence, converter voltage output quality can be improved by implementing the presented driver topology.

Acknowledgment

The authors acknowledges the funds received through the Norwegian Research Council grant 243711 that was used to finance this work.

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A.2 ICSCRM 2019

The following abstract have been submitted to ICSCRM 2019 - international conference on silicon carbide and related materials conference which takes place in Kyoto, Japan, 29. September to 4. October 2019.

Improved SPICE SiC MOSFET model to avoid convergence errors

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SiC MOSFETs are commercially available and are increasing their market share. Their capability to switch faster, have lower on-state resistance and operate under higher junction temperatures offer new possibilities in power electronic applications [1]. However, the increased challenges regarding design of power electronic converters employing SiC MOSFETs increases the use of simulations as a tool in the development. This, however, requires that the simulation model is accurately enough and converges easily.

SPICE simulations are the industry standard for transient analysis of power electronic circuits and many semiconductor manufacturers provide SPICE models for their products [2]. In the preliminary work for the gate driver design presented in [3], the LTspice model provided from Wolfspeed for SiC MOSFET C3M0075120K was used. However, during evaluation of the switching transients, the model tended to run into convergence errors due to its non-continuous behavior. Improvements to the LTspice model have therefore been investigated.

In the internal part of the structure of the LTspice SiC MOSFET model, the transconductance of the device is shaped according to its junction temperature and gate-source voltage dependency as shown in Fig. 1. In the initial model that was provided by the manufacturer (solid lines), this shaping is done piece-wise based on gate-source voltage, where each piece has a constant value that is dependent on junction temperature. In the breaking points between each piece, the model is non-continuous which affects the current commutation as shown by the characteristics in Fig. 2.

The SPICE model has been modified and the piece-wise function is replaced by a continuous function that is inspired by the Rayleigh distribution. The new continuous function has been fitted to the initial model by square error minimization and contains the same junction temperature and gate-source voltage dependency. It is shown with dotted lines in Figs. 1 and 2.

To verify the reliability of the proposed model, the steady-state output characteristics from the initial and the proposed model have been compared to measurements done with the actual device in lab. The results are shown in Figs. 3 and 4 for junction temperatures 25ºC and 125ºC respectively. The results show that the initial and proposed model provides similar steady-state characteristics. Moreover, compared to the lab measurements, none of them outperforms the other one. Thus, equal reliability for the steady-state results from the initial and the proposed model can be assumed.

Fig. 5 shows simulation results for the drain current response for a sweep in gate-source voltage when the junction temperature have been held constant at 25ºC. It is shown that the output characteristics for the drain current with the initial and proposed model clearly follows the same trend. However, when the initial model provides a non-continuous curve, the curve from the proposed model is continuous. This is confirmed in Fig. 6 which shows the derivative of the drain current with respect to the gate-source voltage, i.e. the transconductance. The transconductance for the initial model is seen to change at each breaking point and a spike that shows the non-continuous steps are seen. For the proposed model, the transconductance is continuous for all gate-source voltages except at 1V. However, this is because of an if-statement in the model that activates the current commutation and does not affect convergence.

[1] X. She, A. Huang, O. Lucia and B. Ozpineci, “Review of silicon carbide power devices and their applications”, Transactions on Industrial Electronics, 64(10), p. 8193-8205 (2017).
[2] A. Stefanskyi, L. Starzak, A. Napieralski and M. Lobur, “Analysis of SPICE models for SiC MOSFET power devices”, International conference the experience of designing and application of CAD Systems in Microelectronics (CADSM) (Feb. 2017)

[3] H. L. Hove, O. C. Spro, D. Peftitsis, G. Guidi and K. Ljøkelsøy, “Minimization of dead time effect on bridge converter output voltage quality by use of advanced gate drivers”, International Conference on Power Electronics (ICPE) – ECCE Asia (May 2019).

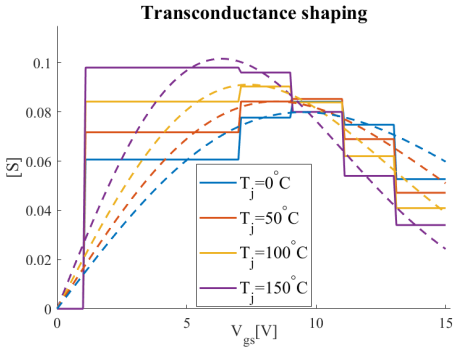

Fig. 1. Simulation results showing how the internal model structure shapes the transconductance based on the gate-source voltage and junction temperature. Dotted lines are proposed model.

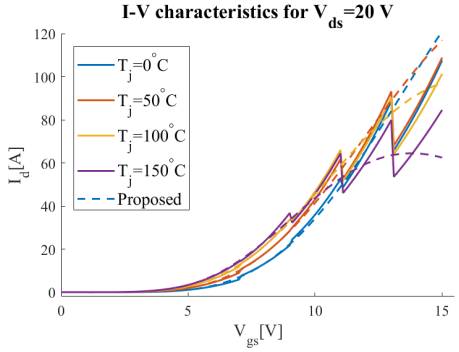

Fig. 2. Simulation results for transfer characteristics for the initial model (solid lines) and the proposed model (dotted lines). Proposed model is continuous.

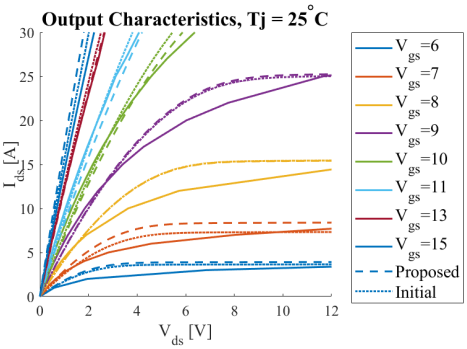

Fig. 3. Static output characteristics from initial and proposed model compared with measurements of the actual device (solid lines) in lab at junction temperature 25ºC.

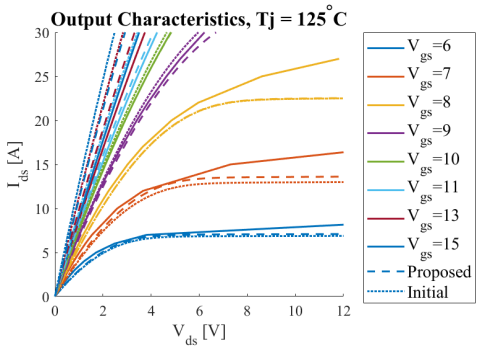

Fig. 4. Static output characteristics from initial and proposed model compared with measurements of the actual device (solid lines) in lab at junction temperature 125ºC.

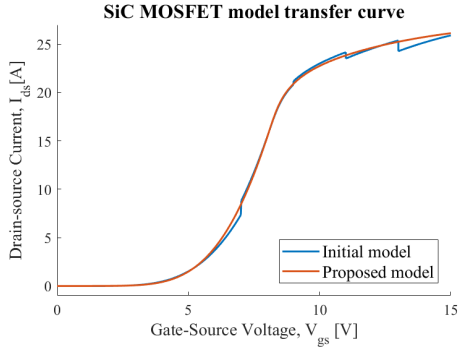

Fig. 5. Drain current for a sweep in gate-source voltage with the initial and the proposed model. Initial model gives a piece-wise response while the proposed models response is continuous.

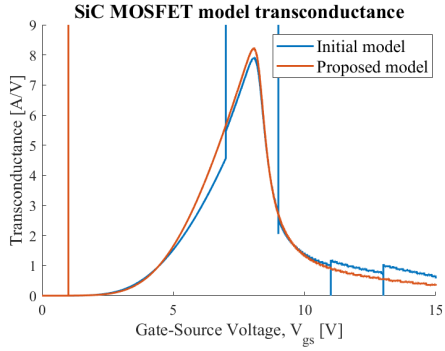

Fig. 6. Derivative of drain current with respect to gate-source voltage (transconductance) for the sweep shown in Fig. 5.

Appendix B

Proposed SPICE model of SiC MOSFET

least_square_weibull.m

```
clear;
% Based on the SiC MOSFET model from Cree
% Finds best approximation to transconductance curve with Weibull
% distribution
%%
Vgs = [0:0.1:15];%0:0.1:15; %V(g2,s)
start_1=find(Vgs==1); start_3=find(Vgs==4); start_7=find(Vgs==7);
start_9=find(Vgs==9); start_11=find(Vgs==11); start_12=find(Vgs==12);
start_13=find(Vgs==13);
Tj = [0 25 50 75 100 125 150];% 200]; %junction temperature
E_min = Inf; %Minimal square error
amp_min = zeros(1,length(Tj)); %Amplitude as function of temperature
a_best = 0; %Optimal coefficients in Sigma function
b_best = 0; %Optimal coefficients in Sigma function

E_temp1 = inf(1,length(Tj)); %Local minimal
E_temp2 = zeros(1,length(Tj)); %Local minimal
amp_temp = zeros(1,length(Tj)); %Local best amplitudes

for a = -0.1:0.001:0
    for b = 8:0.1:10
        E_temp1 = inf(1,length(Tj)); %Set to inf for each iteration
        for i = 1:length(Tj)
            %% Actual model
            NET = zeros(1,length(Vgs));
            % NET5
            NET(start_13+1:length(NET)) = -136.585e-9*(Tj(i)^2)...
                -104.0975e-6*Tj(i) + 52.687e-3;
            % NET6
            NET(start_11+1:start_13) = -214.634e-9*(Tj(i)^2) ...
                - 106.439e-6*Tj(i) + 74.795e-3;
```

```
            % NET7
            NET(start_9+1:start_11) = -500e-9*(Tj(i)^2) ...
                + 47.5e-6*Tj(i) + 84.125e-3;
            % NET8
            NET(start_7+1:start_9) = -85.365e-9*(Tj(i)^2) ...
                + 134.939e-6*Tj(i) + 77.6798e-3;
            % NET9
            NET(start_1+1:start_7) = 273.17e-9*(Tj(i)^2) ...
                + 208.195e-6*Tj(i) + 60.624e-3;

            %% Approximation
            E = zeros(1,length(Vgs)); %Weibull
            Sigma = a*Tj(i) + b;%-0.018*Tj(i)+9.2;

            for amp = 0.9:0.01:1.5
                for k = 1:length(Vgs) %Weibull(Reyleigh)
                    E(k) = amp*Vgs(k)/Sigma^2*exp(-Vgs(k)^2/(2*Sigma^2));
                end
                E_temp2(i) = sum((E(start_3:start_12)...
                    -NET(start_3:start_12)).^2); %Total square error
                if E_temp2(i) < E_temp1(i) %if improved solution
                    E_temp1(i) = E_temp2(i); %Update Error
                    amp_temp(i) = amp; %Update amplitude
                end
            end


        end
        if sum(E_temp1) < E_min
            E_min = sum(E_temp1);
            amp_min = amp_temp;
            a_best = a;
            b_best = b;
        end
    end
end
```

C3M0075120K-Packaged.lib

```
*********************************************************************
*                                     *
*       ,o888888o.     888888888888.    88888888888888 88888888888888     *
*      8888      `88.  888888     `88.  888888           888888           *
*   ,888888        `8. 888888      `88  888888           888888           *
*   8888888            888888      ,88  888888           888888           *
*   8888888            888888.    ,88'  88888888888888 88888888888888     *
*   8888888            888888888888'    888888           888888           *
*   8888888            888888`8b        888888           888888           *
*   `888888        .8' 888888 `8b.      888888           888888           *
*      8888      ,88'  888888    `8b.    888888           888888           *
*       `8888888P'     888888      `88. 88888888888888 88888888888888     *
*                                     *
*********************************************************************
*********************************************************************
**  DISCLAIMER
*********************************************************************
**This model is provided as is, where is, and with no warranty of any kind
```

```
**either expressed or implied, including but not limited to any implied
**warranties of merchantability and fitness for a particular purpose.
*********************************************************************

*********************************************************
****     Cree SiC MOSFET C3M0075120K Spice Library
****     Version 2.0 Date: 11-27-2017
*********************************************************
****     Revision record
****     Version 1    Initial Release
****     Version 2    Include Tc at gmos subcircuit
****
*********************************************************
****Parasitics Included
****Tj = Junction Temperature
****Tc = Case Temperature
*********************************************************

.subckt C3M0075120K d g s1 s2 Tj Tc

xgmos    d3 d1 g1 s Tj Tc gmos_C3M0075120K
RS1      s1   sb   24.88m
Ls1           sb   s    7.574n
R_Ls1         sb   s        20
RS2      s2   sa   3.322m
Ls2           sa   s    3.435n
R_Ls2         sa   s        20
R_g           g1   g2   10.5
RG       g    ga   37.85m
Lg       ga   g3   11.364n
R_Lg          ga   g3   20
Rd       d    da   87.42u
Ld       da   d3        4.366n
R_Ld          da   d3   2
B1       d2   d1        I=V(d1,s)
R_A      d2   d1   1E6
vgate_s       g3   g2   0
vdrain_s      d3   d2   0
Gheat         0    Tj   value = {abs((V(d,s1)*I(Vdrain_s)))+abs((V(g1,g2)
+                                *I(Vgate_s)))}
xCGD          d2   g1   cgdmos_C3M0075120K
CGS      g1   s    1347p
D1       s    d2   bodydiode_C3M0075120K
*Rba          s    va   0.07
*Rbb          va   vb   0.01
*Rbc          Vb   d2   0.05
*Rbd          vb   d2   0.05

R0 N1 Tj 24.985m
R1 N2 N1 59.17m
R2 N3 N2 498.45m
R3 Tc N3 468.96m
C0 Tj Tc 396.233u
C1 N1 Tc 1.22m
C2 N2 Tc 3.926m
C3 N3 Tc 355.24m

```

```
.ends C3M0075120K

****************************************

.subckt gmos_C3M0075120K d3 d1 g1 s Tj Tc

B3        NET3     0    V=20u*(V(Tj)**2)-0.0082*V(Tj)+2.7086
R_C       NET3     0    1E6
B2        NET2     0    V=13.39m*(V(g2,s)**2)-289.14m*v(g2,s)+2.26
R_B       NET2     0    1E6

e4        NET4     0    value = {
+                       if(V(d3,s)<0,
+                       -8.12195u*(V(Tj)**2)+381.34u*v(Tj)+145.54m
+                       ,
+                       -4.639u*(V(Tj)**2)+635.829u*v(Tj)+49m
+                       )
+                       }
R_d       NET4     0    1E6

.param p100 = 3u
.param p101 = -0.0017
.param p102 = 1.2512
.param p200 = -0.021
.param p201 = 9.5

e10       NET10    0    value = {(p100*(V(Tj)**2)+p101*V(Tj)+p102)*(V(g2,s)
+                            /((p200*V(Tj)+p201)**2))*exp(-((V(g2,s))**2)
+                            /(2*((p200*V(Tj)+p201)**2)))}
R_k       NET10    0    1E6


.param p8  = 0.0011
.param p11 = -8
.param p12 = 19

R100 g2 s    1E6
E100 g2 s    value {limit(V(g1,s),p11,p12)}


*******************************
G1 d1 s value = {
+    if(V(s,d3)<0,
+        0
+        ,
+        if (V(g2,s)<1 ,
+        -((0.05)*(v(g2,s)-V(NET3,0)))*(-(1+p8*v(s,d3))*0.008)*(((ln(1+
+        exp(v(g2,s)-V(NET3,0))))**2)-((ln(1+exp(v(g2,s)-V(NET3,0)
+        -(0.854*v(s,d3)))))**2))
+        ,
+        -(((v(NET10,0))*(v(g2,s)-V(NET3,0)))+v(NET4,0))*(1+p8*v(s,d3))
+        *(((ln(1+exp(v(g2,s)-V(NET3,0))))**2)-((ln(1+exp(v(g2,s)
+        -V(NET3,0)-(V(NET2,0)*v(s,d3)))))**2))
+        )
+            )
+            }
G2 d1 s value = {
```

```
+    if(V(d3,s)<0,
+         0
+         ,
+         if (V(g2,s)<1 ,
+         ((0.05)*(v(g2,s)-V(NET3,0)))*(-(1+p8*v(d3,s))*0.008)*(((ln(1
+         +exp(v(g2,s)-V(NET3,0))))**2)-((ln(1+exp(v(g2,s)-V(NET3,0)
+         -(0.854*v(d3,s)))))**2))
+         ,
+         (((v(NET10,0))*(v(g2,s)-V(NET3,0)))+v(NET4,0))*(1+p8*v(d3,s))
+         *(((ln(1+exp(v(g2,s)-V(NET3,0))))**2)-((ln(1+exp(v(g2,s)
+         -V(NET3,0)-(V(NET2,0)*v(d3,s)))))**2))
+         )
+              )
+              }

.ends gmos_C3M0075120K

****************************************

.subckt cgdmos_C3M0075120K d2 g
.param k1=535p
.param k2=0.538
.param ka=20
.param kb=0.5
.param kc=6.5277
G11 g d1 value =     {
+         k1*(
+         (1+(limit(v(d1,g),0,600))*(1+ka*(1+TANH(kb*V(d1,g)-kc))/2))**-k2
+         )*ddt(v(g,d1))
+              }
R_CGD d1 d2 1e-4
.ends cgdmos_C3M0075120K


****************************************
.model bodydiode_C3M0075120K d(is=158.89n cjo=1119p bv=1590 m=0.49
+    EG=2.22827 vj=1.6 n=5.05 rs=0.056 trs1=1u  trs2=-5.5003u Tnom=25
+    tt=5n ibv=500u Xti=0.13 level=1)
```

Appendix C

Simulation model for delay time minimization gate driver impact

runAnalysis.m

```
clear;
%% Set analysis parameters
modIndex = [0.8:0.01:1.5]; %Modulation indexes to be evaluated
swFreq = 15000; %Frequency of triangle carrier wave

% Conventional gate driver delay times
Tdt_conv = 810e-9; %Dead time
Td_OFF_conv = 450e-9; %TurnOff delay
Td_ON_conv = 90e-9; %TurnON delay

% Multistage driver delay times
Tdt_boost = 470e-9; %Dead time
Td_OFF_boost = 110e-9; %TurnOFF delay
Td_ON_boost = 30e-9; %TurnON delay

%% Set certain constraints to the simulation
I = 30/sqrt(2); %Current
pf = 0.9; %Power factor
theta = acosd(pf); %Angle between Van and Ia
Vd = 600; %Dc link voltage
Xl = 30e-3*2*pi*50; %Synchronous reactance of motor

%% Creating structs for results
R = length(modIndex); C = length(swFreq);
% Each row corresponds to modulation index and column to sw.frequency
% Sinusoidal PWM
SPWM = struct('Ma',modIndex,'fsw',swFreq,'NoBoost',struct('V_THD',...
    zeros(R,C),'V_fund',zeros(R,C),'I_THD',zeros(R,C),'I_fund',...
    zeros(R,C)),'Boost',struct('V_THD',zeros(R,C),'V_fund',zeros(R,C),...
    'I_THD',zeros(R,C),'I_fund',zeros(R,C)));
% Third harmonic Injection
```

```
THIPWM = struct('Ma',modIndex,'fsw',swFreq,'NoBoost',struct('V_THD',...
    zeros(R,C),'V_fund',zeros(R,C),'I_THD',zeros(R,C),'I_fund',...
    zeros(R,C)),'Boost',struct('V_THD',zeros(R,C),'V_fund',zeros(R,C),...
    'I_THD',zeros(R,C),'I_fund',zeros(R,C)));
% Discontonous
DPWM1 = struct('Ma',modIndex,'fsw',1.5*swFreq,'NoBoost',struct('V_THD',...
    zeros(R,C),'V_fund',zeros(R,C),'I_THD',zeros(R,C),'I_fund',...
    zeros(R,C)),'Boost',struct('V_THD',zeros(R,C),'V_fund',zeros(R,C),...
    'I_THD',zeros(R,C),'I_fund',zeros(R,C)));

%% Analysis
for r = 1:R
    Ma = modIndex(r);
    for c = 1:C
        fsw = swFreq(c);
        %SPWM
        compensation_type = 0;
        %Update emf
        if Ma <= 1.0
            Va = Vd/(2*sqrt(2))*Ma;
        else
            Va = Vd/(2*sqrt(2))+68*(Ma-1);
            %Estimated peak phase voltage in non-linear region
        end
        delta = atand(Xl*I*cosd(theta)/(Va-Xl*I*sind(theta)))*pi/180;
        E_rms = Xl*I*cosd(theta)/sin(delta); %Induced emf in motor

        % Conventional
        Tdt = Tdt_conv;
        Td_ON = Td_ON_conv;
        Td_OFF = Td_OFF_conv;
        run DistortionCalc.m %Run simulation and update tables
        SPWM.NoBoost.V_THD(r,c) = THD_V;
        SPWM.NoBoost.V_fund(r,c) = fund_V;
        SPWM.NoBoost.I_THD(r,c) = THD_I;
        SPWM.NoBoost.I_fund(r,c) = fund_I;

        % Multistage
        Tdt = Tdt_boost; %Boost
        Td_ON = Td_ON_boost;
        Td_OFF = Td_OFF_boost;
        run DistortionCalc.m %Run simulation and update tables
        SPWM.Boost.V_THD(r,c) = THD_V;
        SPWM.Boost.V_fund(r,c) = fund_V;
        SPWM.Boost.I_THD(r,c) = THD_I;
        SPWM.Boost.I_fund(r,c) = fund_I;

        %THIPWM
        compensation_type = 1;

        % Update emf
        if Ma <= 1.15
            Va = Vd/(2*sqrt(2))*Ma;
        else
            Va = Vd/(2*sqrt(2))*1.15+40*(Ma-1.15);
            %Estimated peak phase voltage in non-linear region
        end
```

```
89          delta = atand(Xl*I*cosd(theta)/(Va-Xl*I*sind(theta)))*pi/180;
90          E_rms = Xl*I*cosd(theta)/sin(delta); %Induced emf in motor
91
92          % Conventional
93          Tdt = Tdt_conv;
94          Td_ON = Td_ON_conv;
95          Td_OFF = Td_OFF_conv;
96          run DistortionCalc.m %Run simulation and update tables
97          THIPWM.NoBoost.V_THD(r,c) = THD_V;
98          THIPWM.NoBoost.V_fund(r,c) = fund_V;
99          THIPWM.NoBoost.I_THD(r,c) = THD_I;
100         THIPWM.NoBoost.I_fund(r,c) = fund_I;
101
102         % Multistage
103         Tdt = Tdt_boost;
104         Td_ON = Td_ON_boost;
105         Td_OFF = Td_OFF_boost;
106         run DistortionCalc.m %Run simulation and update tables
107         THIPWM.Boost.V_THD(r,c) = THD_V;
108         THIPWM.Boost.V_fund(r,c) = fund_V;
109         THIPWM.Boost.I_THD(r,c) = THD_I;
110         THIPWM.Boost.I_fund(r,c) = fund_I;
111
112         %DPWM1
113         fsw = 1.5*fsw; %Higher switching frequency for DPWM1
114         compensation_type = 2;
115
116         % Update emf
117         if Ma <= 1.15
118             Va = Vd/(2*sqrt(2))*Ma;
119         else
120             Va = Vd/(2*sqrt(2))*1.15+60*(Ma-1.15);
121             %Estimated peak phase voltage in non-linear region
122         end
123         delta = atand(Xl*I*cosd(theta)/(Va-Xl*I*sind(theta)))*pi/180;
124         E_rms = Xl*I*cosd(theta)/sin(delta); %Induced emf in motor
125
126         % Conventional
127         Tdt = Tdt_conv;
128         Td_ON = Td_ON_conv;
129         Td_OFF = Td_OFF_conv;
130         run DistortionCalc.m %Run simulation and update tables
131         DPWM1.NoBoost.V_THD(r,c) = THD_V;
132         DPWM1.NoBoost.V_fund(r,c) = fund_V;
133         DPWM1.NoBoost.I_THD(r,c) = THD_I;
134         DPWM1.NoBoost.I_fund(r,c) = fund_I;
135
136         % Multistage
137         Tdt = Tdt_boost;
138         Td_ON = Td_ON_boost;
139         Td_OFF = Td_OFF_boost;
140         run DistortionCalc.m %Run simulation and update tables
141         DPWM1.Boost.V_THD(r,c) = THD_V;
142         DPWM1.Boost.V_fund(r,c) = fund_V;
143         DPWM1.Boost.I_THD(r,c) = THD_I;
144         DPWM1.Boost.I_fund(r,c) = fund_I;
145     end
```

```
146 end
```

DistortionCalc.m

```
1
2  %% Setting parameters
3  points = 4096/4;          %Evaluation points per triangular wave
4                            %Should be a number in 2^x, where x is an integer
5  Tsim = 1;                 %Simulation time in seconds
6  fout = 50;                %Fundamental frequency in Hz
7  Vdc = 600;                %DC link voltage in V
8  Rdon = 80e-3;             %On resistance MOSFET in Ohm
9  phi = 0;                  %Voltage angle in rad
10
11 %% Calculating parameters
12 fsamp = fsw*points;        %Sampling frequency
13 t= [0:(1/fsamp):Tsim];     %Time-vector
14
15 %% Motor back emf
16 emf_a = sqrt(2)*E_rms*sin(2*pi*fout*t-delta);            %Back emf, a-phase
17 emf_b = sqrt(2)*E_rms*sin(2*pi*fout*t-delta+2*pi/3);     %Back emf, b-phase
18 emf_c = sqrt(2)*E_rms*sin(2*pi*fout*t-delta+4*pi/3);     %Back emf, c-phase
19
20 %% Voltage control signals for PWM generation
21 Vca = Ma*sin(2*pi*fout*t+phi);
22 Vcb = Ma*sin(2*pi*fout*t+phi+2*pi/3);
23 Vcc = Ma*sin(2*pi*fout*t+phi+4*pi/3);
24
25 %% PWM compensation type
26 Vc_compensation = PWM_compensation(fout,t,phi,Ma,compensation_type);
27
28 %% PWM signals
29 PWMa = PWM(points,t,Vca+Vc_compensation);
30 PWMb = PWM(points,t,Vcb+Vc_compensation);
31 PWMc = PWM(points,t,Vcc+Vc_compensation);
32
33 %% Min Pulse Width
34 PWMa = minPulseWidth(PWMa,fsamp,3*Tdt);
35 PWMb = minPulseWidth(PWMb,fsamp,3*Tdt);
36 PWMc = minPulseWidth(PWMc,fsamp,3*Tdt);
37
38 %% Output voltages and current
39 [Van,Vbn,Vcn,Ia,Ib,Ic,Vn] = voltageOut_3ph(Vdc,Rdon,fsamp,PWMa,PWMb,...
40     PWMc,Tdt,Td_ON,Td_OFF,emf_a,emf_b,emf_c);
41
42 %% FFT and THD
43 interval=2/fout*fsamp; %Only evaluate steady state conditions
44
45 [fund_V,THD_V] = distortion(Van((length(t)-interval):length(t))...
46     -Vbn((length(t)-interval):length(t)),t((length(t)-interval):...
47     length(t)),fsamp);
48
49 [fund_I,THD_I] = distortion(Ia((length(t)-interval):length(t)),...
50     t((length(t)-interval):length(t)),fsamp);
```

PWM_compensation.m

```
function [Vc_comp] = PWM_compensation(f_fund,t,phi,Ma,type)
    % f_fund = Fundamental frequency [Hz]
    % t      = Time vector [s]
    % phi    = Voltage angle for control signal [rad]
    % Ma     = Modulation index [-]
    % type   = compensation type (0,1,2)

    %    0 for no compensation, 1 for THIPWM and 2 for DPWM1
    switch type
        case 0 % No compensation
            Vc_comp = zeros(1,length(t));
        case 1 %Third harmonic injection
            Vc_comp = Ma/6*sin(3*2*pi*f_fund*t+phi);
        case 2 %Discontinous compensation
            Vc_comp = zeros(1,length(t));
            fsamp = 1/(t(2)-t(1)); %Sampling frequency
            N = fsamp/(6*f_fund); %points to cover pi/3 of a sine wave
            theta = pi/6+pi/6;
            v = 1-Ma*sin(2*pi*f_fund*t(1:N)+theta);
            i = 1;
            sign = -1;
            while i+N <= length(t)
                Vc_comp(i:i+N-1) = sign.*v;
                i = i+N;
                sign=sign*(-1);
            end
        otherwise
            Vc_comp = zeros(1,length(t));
    end
end
```

PWM.m

```
function [pwm] = PWM(points,t,Vctrl)
    %points = points per triangular wave
    %t = time vector
    %Vctrl = control voltage signal

    %% Creating triangular wave
    res = log2(points)-2;
    tri = [0 1 0 -1 0];
    tri2 = zeros(1,points+1);
    tri2(1:length(tri)) = tri;
    for k = 1:(res)
       for i = 2:2:length(tri2)
           counter = length(tri2);
           while counter > i
               tri2(counter) = tri2(counter-1);
               counter = counter-1;
           end
           tri2(i) = (tri2(i+1)+tri2(i-1))/2;
       end
    end

    Vtri = zeros(1,length(t));
    for i = 1:points:length(Vtri)-1
       Vtri(i:i+points) = tri2;
```

```
    end

    %% PWM Signal
    pwm = zeros(1,length(t));
    for i = 1:length(t)
        if Vctrl(i)>Vtri(i)
            pwm(i) = 1;
        end
    end
end
```

minPulseWidth.m

```
function PWM = minPulseWidth(PWM, fsamp, minPulse)
    %Blanks the pulses that are shorter than minPulse [s]
    blankingPoints = floor(fsamp*minPulse);
    for i = 2:(length(PWM)-blankingPoints)
        if (PWM(i) ~= PWM(i-1)) && (PWM(i+blankingPoints) == PWM(i-1))
            for k = i:(i+blankingPoints)
                PWM(k) = PWM(i-1);
            end
        end
    end
end
```

voltageOut_3ph.m

```
function [Van,Vbn,Vcn,Ia,Ib,Ic,Vn] = ...
    voltageOut_3ph(Vdc,Rdon,fsamp,PWMa,PWMb,PWMc,Tdt,Td_ON,...
    Td_OFF,emf_a,emf_b,emf_c)
    % Returns vectors containing output phase voltage and line current
    %% Setting calculation parameters
    dt = 1/fsamp; %Time step
    fsamp = fsamp*10^-9; %Sampling freq in points per nanosec
    Van = zeros(1,length(PWMa))-Vdc/2;  %Empty voltage vector
    Vbn = zeros(1,length(PWMb))-Vdc/2;  %Empty voltage vector
    Vcn = zeros(1,length(PWMc))-Vdc/2;  %Empty voltage vector
    Vian = PWMa*Vdc - Vdc/2;            %Ideal case
    Vibn = PWMb*Vdc - Vdc/2;            %Ideal case
    Vicn = PWMc*Vdc - Vdc/2;            %Ideal case
    Vn = zeros(1,length(PWMa));         %Motor neutral point

    % Initial values:
    [dvdt,didt] = commutations(5);%
    dvdp = dvdt/fsamp; %Voltage change per sampling point
    didp = didt/fsamp; %Amps per sampling point
    Vfw = SiC_Vforward(5);

    %"sampling points delay"
    Pdion = (Tdt+Td_ON)*fsamp*10^9; %Current turn on delay, incl. deadtime
    Pdvon = Pdion + 5/didp; %Updating voltage delay
    Pdvoff = Td_OFF*fsamp*10^9; %Voltage turn off delay

    %% Calculating voltage and current characteristics
    %Setting flag at start initially
    flag_a = 1;
    flag_b = 1;
```

```
31      flag_c = 1;
32
33      % Setting current characteristics
34      L = 30e-3;%15e-3;
35      Ia = zeros(1,length(PWMa)); %Empty current vector. Load current
36      Ib = zeros(1,length(PWMb)); %Empty current vector. Load current
37      Ic = zeros(1,length(PWMc)); %Empty current vector. Load current
38      Ia(1) = 30*sind(-25);%-10; %Initial condition
39      Ib(1) = 30*sind(-25+120);%10; %Initial condition
40      Ic(1) = 30*sind(-25+240); %Initial condition
41
42      for i = 2:length(PWMa)
43          %% Neutral point of motor and load current
44          Vn(i-1) =1/3*(Van(i-1)+Vbn(i-1)+Vcn(i-1)-emf_a(i-1)-...
45              emf_b(i-1)-emf_c(i-1));
46
47          %% Line current calculations by Euler's method
48          Ia(i) = dt*(Van(i-1)-emf_a(i-1)-Vn(i-1))/L + Ia(i-1);
49          Ib(i) = dt*(Vbn(i-1)-emf_b(i-1)-Vn(i-1))/L + Ib(i-1);
50          Ic(i) = dt*(Vcn(i-1)-emf_c(i-1)-Vn(i-1))/L + Ic(i-1);
51
52          %% Phase a voltage
53          if PWMa(i) ~= PWMa(i-1) %Detect change
54              % Assuming lower MOSFET in a halfbridge
55              % Low PWM means that lower switch i turned on
56              flag_a = i; % Set flag for change in PWM
57              [dvdt,didt] = commutations(5); %Update commutation slopes
58              dvdp = dvdt/fsamp; %Voltage change per sampling point
59              Vfw = SiC_Vforward(abs(Ia(i))); %Update voltage drop in diode
60              Pdvon = Pdion + abs(Ia(i))/didt*fsamp; %Updating voltage delay
61          end
62
63          %% Freewheeling characteristics
64          switch Ia(i) >= 0
65              case true %Positiv current => Upper MOSFET controlling
66                  % Phase voltage always seeks towards -Vfw-Vdc/2
67                  % If (Upper MOSFET off) && (Lower MOSFET off):
68                  if (flag_a + Pdvoff <= i) && (i < flag_a + Pdvon) && ...
69                          (Van(i-1) > -Vfw-Vdc/2)
70                      Van(i) = Van(i-1) - dvdp;
71                  else
72                      Van(i) = Van(i-1);
73                  end
74
75              case false %Negative current => Lower MOSFET controlling
76                  % Phase voltage always seek towards Vdc/2 + Vfw
77                  % If (upper MOSFET off) && (Lower MOSFET off):
78                  if (flag_a + Pdvoff <= i) && (i < flag_a + Pdvon) && ...
79                          (Van(i-1) < Vdc/2 + Vfw)
80                      Van(i) = Van(i-1) + dvdp;
81                  else
82                      Van(i) = Van(i-1);
83                  end
84
85              otherwise
86                  Van(i) = Van(i-1);
87          end
```

```
88
89          % Voltage boundary check
90          if Van(i) > Vdc/2 + Vfw
91              Van(i) = Vdc/2+Vfw;
92          elseif Van(i) < -Vfw-Vdc/2
93              Van(i) = -Vfw-Vdc/2;
94          end
95
96          %% Updating with conduction voltage loss
97          Vian(i) = Vian(i) - Ia(i) * Rdon;
98
99          %% Update conduction characteristics
100         if (i >= flag_a + Pdvon) && (Van(i-1) > (Vian(i)))
101             Van(i) = Van(i-1) - dvdp;
102             if Van(i) < Vian(i)
103                 Van(i) = Vian(i);
104             end
105         elseif (i >= flag_a + Pdvon) && (Van(i-1) < Vian(i))
106             Van(i) = Van(i-1) + dvdp;
107             if Van(i) > Vian(i)
108                 Van(i) = Vian(i);
109             end
110         end
111
112         %% Phase b voltage, equal as for phase a
113         if PWMb(i) ~= PWMb(i-1)
114             flag_b = i;
115             [dvdt,didt] = commutations(5);
116             dvdp = dvdt/fsamp;
117             Vfw = SiC_Vforward(abs(Ib(i)));
118             Pdvon = Pdion + abs(Ib(i))/didt*fsamp;
119         end
120
121         switch Ib(i) >= 0
122             case true
123                 if (flag_b + Pdvoff <= i) && (i < flag_b + Pdvon) && ...
124                         (Vbn(i-1) > -Vfw-Vdc/2)
125                     Vbn(i) = Vbn(i-1) - dvdp;
126                 else
127                     Vbn(i) = Vbn(i-1);
128                 end
129             case false
130                 if (flag_b + Pdvoff <= i) && (i < flag_b + Pdvon) && ...
131                         (Vbn(i-1) < Vdc/2 + Vfw)
132                     Vbn(i) = Vbn(i-1) + dvdp;
133                 else
134                     Vbn(i) = Vbn(i-1);
135                 end
136             otherwise
137                 Vbn(i) = Vbn(i-1);
138         end
139
140         if Vbn(i) > Vdc/2 + Vfw
141             Vbn(i) = Vdc/2+Vfw;
142         elseif Vbn(i) < -Vfw-Vdc/2
143             Vbn(i) = -Vfw-Vdc/2;
144         end
```

```
145
146         Vibn(i) = Vibn(i) - Ib(i) * Rdon;
147
148         if (i >= flag_b + Pdvon) && (Vbn(i-1) > (Vibn(i)))
149             Vbn(i) = Vbn(i-1) - dvdp;
150             if Vbn(i) < Vibn(i)
151                 Vbn(i) = Vibn(i);
152             end
153         elseif (i >= flag_b + Pdvon) &&(Vbn(i-1) < Vibn(i))
154             Vbn(i) = Vbn(i-1) + dvdp;
155             if Vbn(i) > Vibn(i)
156                 Vbn(i) = Vibn(i);
157             end
158         end
159
160         %% Phase c voltage, similar as for phase a
161         if PWMc(i) ~= PWMc(i-1)
162             flag_c = i;
163             [dvdt,didt] = commutations(5);
164             dvdp = dvdt/fsamp;
165             Vfw = SiC_Vforward(abs(Ic(i)));
166             Pdvon = Pdion + abs(Ic(i))/didt*fsamp;
167         end
168
169         switch Ic(i) >= 0
170             case true
171                 if (flag_c + Pdvoff <= i) && (i < flag_c + Pdvon) && ...
172                         (Vcn(i-1) > -Vfw-Vdc/2)
173                     Vcn(i) = Vcn(i-1) - dvdp;
174                 else
175                     Vcn(i) = Vcn(i-1);
176                 end
177             case false
178                 if (flag_c + Pdvoff <= i) && (i < flag_c + Pdvon) && ...
179                         (Vcn(i-1) < Vdc/2 + Vfw)
180                     Vcn(i) = Vcn(i-1) + dvdp;
181                 else
182                     Vcn(i) = Vcn(i-1);
183                 end
184             otherwise
185                 Vcn(i) = Vcn(i-1);
186         end
187
188         if Vcn(i) > Vdc/2 + Vfw
189             Vcn(i) = Vdc/2+Vfw;
190         elseif Vcn(i) < -Vfw-Vdc/2
191             Vcn(i) = -Vfw-Vdc/2;
192         end
193
194         Vicn(i) = Vicn(i) - Ic(i) * Rdon;
195
196         if (i >= flag_c + Pdvon) && (Vcn(i-1) > (Vicn(i)))
197             Vcn(i) = Vcn(i-1) - dvdp;
198             if Vcn(i) < Vicn(i)
199                 Vcn(i) = Vicn(i);
200             end
201         elseif (i >= flag_c + Pdvon) &&(Vcn(i-1) < Vicn(i))
```

```
            Vcn(i) = Vcn(i-1) + dvdp;
            if Vcn(i) > Vicn(i)
                Vcn(i) = Vicn(i);
            end
        end
    end
end
```

commutations.m

```
function [dvdt, didt] = commutations(Ids)
    % Returns commutation slopes for voltage and current
    % Possible to make the slopes load current dependent as input is Ids
    dvdt = 10;
    didt = 0.3;
end
```

SiC_Vforward.m

```
function Vfw = SiC_Vforward(I)
    % Give forward voltage for SiC MOSFET C3M0075120K
    % Basis is 3V, then interpolates up to maximum 5V
    % Estimated from datasheet
    % Current limited between 0 and 30 A
    Vfw = 3 + 2.5*I/30;
end
```

distortion.m

```
function [fundamental, THD] = distortion(signal,time,fsampling)
    % Returns peak value of fundamental component and THD based on FFT
    L = length(time);
    Y = fft(signal);
    P2 = abs(Y/L);
    P1 = P2(1:L/2+1);
    P1(2:end-1)=2*P1(2:end-1);
    f = fsampling*(0:(L/2))/L;

    fundamental = 0; n = 0; harmonics = 0; %Initial values
    for i = 1:length(f)
        if P1(i) > fundamental
            fundamental = P1(i);
            n = i;
        end
        harmonics = harmonics + P1(i)^2;
    end
    harmonics = harmonics - fundamental^2;
    THD = sqrt(harmonics)/fundamental;
end
```

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