Lyder Rumohr Blingsmo

Comparison between Si MOSFETs and GaN HEMTs with special emphasis on low load problems occuring in the LLC resonant converter

Master's thesis in Energi og miljø

Supervisor: Roy Nilsen, Tore Marvin Undeland, Ole Christian Spro

June 2019

Master's thesis

NTNU
Norwegian University of Science and Technology
Faculty of Information Technology and Electrical Engineering
Department of Electric Power Engineering

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Kunnskap for en bedre verden

ELTEK
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Preface and acknowledgements

This thesis is written at Norwegian University of Science and Technology(NTNU) during the spring of 2019. It entails 30 credits (ECTS) and represents the final requirement for a degree in Master of Technology with the program Energy and Environmental Engineering with specialization in Electrical Energy Engineering.

The thesis is written in cooperation with Eltek AS in Drammen. Thank you to Erik Myhre, Ibrahim Abuishmais, Morten Hostvedt and Thomas Olsen at Eltek for helping me when I had questions. Thank you also to my supervisors at NTNU, Tore Marvin Undeland and Ole Christian Spro for helpful feedback and valuable input during the semester.

Lyder Rumohr Blingsmo,
Trondheim, June 2019

Summary

Rectifiers for supplying data center with power from the grid are subject to many requirements, one of which is very high efficiency. One of the most common converter architectures consists of a PFC rectifier stage, used for achieving sinusoidal mains current, followed by a DC-link and a LLC resonant converter for the DC-DC conversion. This topology is already quite efficient. However, one possible solution to increasing the efficiency further is lowering the on-state resistance of the transistors used. Regular silicon(Si) metal-oxide-semiconductor field-effect transistors(MOSFET) however are quickly approaching their theoretical limit in terms of tradeoff between die size and on-state resistance. To reduce on-state resistance further, the die size must then be increased. An increased die size comes with the disadvantage of large terminal capacitances, which can lead to problems.

One of the main enabling technologies for increased efficiency is therefore gallium nitride(GaN) high electron mobility transistors(HEMT). This is because they have smaller terminal capacitances for the same on-state resistance, owing to superior material properties. It is expected that replacing the Si MOSFETs in the LLC converter with GaN HEMTs could improve efficiency, while also avoiding the some of the problems that could occur with excessively large output capacitances. Especially low load regulation problems is considered in this regard.

In this report, only the LLC converter will be considered. The PFC converter will not be discussed. More specifically the LLC topology with a half-bridge structure at the input will be considered. On the secondary side a full-bridge diode-rectifier is used. Design methods, transfer functions, zero-voltage switching, operation modes and low load problems are discussed. Other broad topics such as control is only briefly mentioned. Si MOSFETs and GaN HEMTs are the only transistor types considered.

This report starts with a literature study on GaN devices, more specifically GaN HEMT. In the second part the LLC series resonant topology is discussed. Possible implementation of new GaN-switches in the LLC converter is researched. A direct comparison between GaN HEMTs and silicon MOSFETS is done. Special emphasis is put on considerations that are important to soft-switching topologies such as the LLC converter. Simulations in LTSPICE are done to validate some of the discussed concepts, especially the derived transfer function from the fundamental harmonic approximation(FHA), which shows good results. Lab measurements are also done, and it is seen that the GaN HEMT can improve upon the low load problems occurring in the LLC converter when using Si MOSFETs. The results show that this is achieved with the same degree of efficiency, and using GaN HEMTs the efficiency might even be increased.

What is written here is based on a project report previously done by the same author [1].

Sammendrag

Det stilles store krav til likerettere brukt til å forsyne datasentere med kraft. Et av kravene er høy virkningsgrad. En av de vanligste topologiene brukt til dette formålet består av en PFC-likeretter, for å få sinusformet strøm fra nettet, etterfulgt av en DC-link og en LLC-konverter for DC-DC omforming. Disse strømforsyningene har allerede høy virkningsgrad. En mulighet for å øke virkningsgraden ytterligere er allikevel å redusere motstanden til transistorene når de er skrudd på. Men vanlige silisium(Si) 'metal-oxide-semiconductor field-effect transistorer'(MOSFET) nærmer seg raskt sin teoretiske grense for sammenhengen mellom on-state motstand og fysisk størrelse. For å redusere motstanden til en gitt silisium MOSFET enda mer, er da eneste mulig å øke størrelsen. Økt størrelse betyr større parasittiske kapasitanser, noe som kan gi problemer.

En av de viktigste teknologiene for økt virkningsgrad er derfor galliumnitrid(GaN) 'high electron mobility transistor' (HEMT). GaN har overlegne materialegenskaper, og kan derfor gi transistorerer med bedre egenskaper. Dette inkluderer blant annet mindre parasittiske kapasitanser for den samme on-state motstanden. Det forventes derfor at å erstatte Si MOSFET med GaN HEMT i LLC-omformeren kan bedre virkningsgraden, samtidig som man unngår problemene som oppstår ved alt for store utgangskapasitanser. Spesielt lavlast-reguleringsproblemer forventes å kunne bli bedre.

I denne rapporten vil bare LLC-omformeren bli vurdert. PFC-leddet diskuteres ikke. Mer spesifikt er det LLC-topologien med en halvbro-struktur på inngangen, og fullbro diodelikeretter som blir brukt. Designmetodikk, transferfunksjoner, nullspennings-svitsjing, driftmoduser og lavlastproblemer diskuteres. Andre store tema slik som for eksempel kontroll av omformeren nevnes bare kort. Si MOSFET og GaN HEMT er de eneste transistortypene som blir vurdert.

Rapporten begynner med et litteraturstudie på GaN transistor, og da spesielt GaN HEMT. Dette er etterfulgt av det litteraturstudie på LLC-serie-resonansomformeren. Mulig implementering av GaN HEMT i LLC-omformeren blir undersøkt. GaN HEMT og silisium MOSFETer sammenlignes direkte ved hjelp av 'figure of merit'(FOM). Spesiell vekt legges på hensyn som er viktig for 'soft-switching'-topologier slik som LLC-konverteren. Gjennom simulering i LTspice valideres noen av de diskuterte konseptene, spesielt FHA-antagelsen i utledningen av transferfunksjonen. Transferfunksjon blir også målt i lab. Resultatene viser god overensstemmelse mellom teori og simulering og lab. En LLC-modul med GaN HEMT og en annen LLC-modul med Si MOSFETer sammenlignes også gjennom labmålinger. Her vises det at GaN HEMT kan forbedre lavlastproblemene samtidig som virkningsgraden forblir den samme, og kan til og med økes noe.

Det som er skrevet her er basert på et tidligere prosjekt av samme forfatter [1].

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Chapter 1

Introduction

1.1 Motivation

The demand on data traffic is rapidly increasing. Data centers use electrical energy to power server equipment, as well as control and process data. The energy consumed in data centers in 2016 was 416.2 TWh and accounted for about 3 % of the global electricity consumption, and was projected to increase threefold in the next decade [2]. For Google alone, the energy consumption increased from 2.9 TWh in 2012 to 8.0 TWh in 2017 [3]. In the EU in 2016, 30 % of the energy was produced by renewable sources [4], however carbon footprint of data centers will still be significant.

It is in this regard, that a highly efficient AC-DC rectifier would be valuable. Silicon transistors are quickly reaching their fundamental limits set by the material properties [6], and to further improve transistors, other materials must be used. Since as early as the 1950s wide band-gap devices have been announced to be the next generation power devices, after silicon reaches its limits [7].In [5] it is reported that 11 of the 23 major silicon power switch companies have R&D on GaN devices. In fig. 1.1 state-of-the-art silicon devices are compared to the published performance of GaN transistors, and the great potential is clearly seen. As shown in [8] [9] [10] and theoretically discussed in [11] [12] [6] [13] GaN transistors makes it possible to increase the efficiency and power density even further. This makes it possible with a new era of efficient power converters also after silicon reaches its limitations [14]. High efficiency results in less power loss while high density contributes in reducing the size of data center infrastructure resulting in a lower footprint and lower investment cost. However, Si MOSFETs and GaN HEMTs are different in many respects, and some important differences must be investigated before GaNs full potential can be utilized.

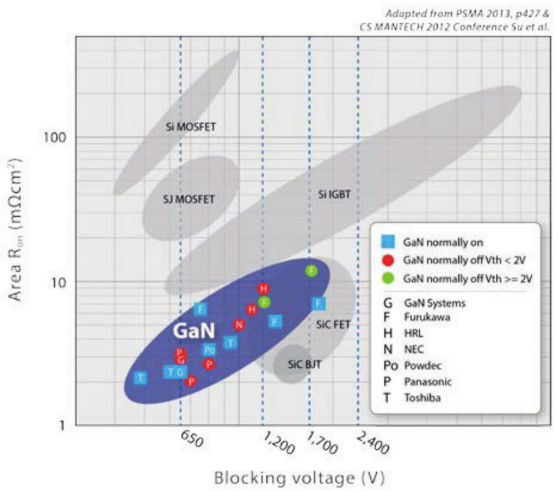


Figure 1.1: The great promise of wide band-gap semiconductors. Obtained from [5].

1.2 Scope of report

Studied here is the design and operation of the LLC resonant converter stage of the complete AC-DC rectifier. Many different topology variations exist. However in this report only the LLC converter with half-bridge at input at full-diode bridge rectification at the output is considered. Other topology variations will only be mentioned briefly for reference. A comparison between the benefits of GaN High Electron Mobility-Transistor(HEMT) compared to the more well-known silicon MOSFET is to be made. Special emphasis will be put on soft-switching topologies. Some important considerations for the implementation of GaN HEMT will be discussed. The goal of the report is to show that low-load regulation problems that are present for low ohmic MOSFETs, could be solved with low-ohmic GaN HEMTs. Degradation of performance is not acceptable, so this should be achieved while also keeping the same efficiency or even improving it.

Although GaN will allow for an efficiency increase in many power electronics devices, in [15] it is shown that as the switches are continuously improved, an absolute performance limit will still be imposed by passive components and the cooling system. Therefore, as the design criteria of devices become ever more stringent, other design considerations will gain bigger importance alongside improvements in transistor technologies. Losses in a converter could be said to arise from three different groups: semiconductors, passive components and auxiliary systems [16]. Mostly the semiconductor part will be considered in this report.

1.3 Project outline

This report starts with the basic theory and literature study on GaN HEMT devices and the LLC resonant converter. The next section validates some of the theoretic results through simulations. Following this is laboratory measurements on an LLC converter. Here Si MOSFETs and GaN HEMTs are compared with special emphasis put on low load problems. Also different measures for increasing the efficiency are tested. The last part contains conclusion and possibilities for future work.

Chapter 2

GaN-transistors

To research the possibility of improvement of operation with GaN devices, a literature search is done in this section.

GaN is an abbreviation for gallium nitride, a wide band gap semiconductor. It is a very attractive alternative for high-voltage, high-frequency and high-temperature applications [14]. Owing to its advantageous material properties, GaN transistors can be produced with better on-state resistance, breakdown voltage, switching efficiency and smaller size compared to its silicon counterpart [11]. This is largely due to its higher breakdown field, allowing for a smaller drift region, which again allows for a smaller on-state resistance. Smaller die size for a given current rating also reduces the parasitic capacitances between the terminals of the transistor[12]. Many different GaN-transistor structures exist [12]. It is common to distinguish between lateral and vertical devices, depending geometric orientation of source and drain in regards to gate.

Here the GaN-transistors, more specifically GaN high electron mobility transistor(HEMT), are compared to the more well-known silicon MOSFET transistors. The HEMT is a lateral structure. HEMT devices are also known as HFET(Heterojunction field-effect transistors) [12]. The name HEMT comes from the existence of a 2D-electron gas formed in the AlGan/GaN intersection due to crystal polarity, augmented by piezoelectric crystal strain because of lattice mismatch[12]. At the layer between AlGaN/GaN there is a discontinuity in conduction band and presence of polarization fields, leading to an electron gas with high electron mobility [14]. There must be a negative voltage applied to the gate to remove the 2DEG [14] [12]. This implies that HEMTs are depletion mode(normally-on) devices. Often, normally-on devices can cause problems and are not wanted in power electronics circuits in general. This is because of the possible shoot-through(short-circuit) at startup or potentially fatal consequences if the control circuit stops working [12]. Measures such as cascading it with a regular silicon MOSFET or altering the gate structure can be taken to make it an enhancement mode(normally-off) device as discussed in [11] [13] [12].

The GaN HEMT and silicon MOSFET are similar in many ways. Most importantly their analytical model is very much the same, which means they are

relatively easy to compare.

Important parameters for transistors, especially with regards to soft-switching topologies such as the LLC converter, is also discussed.

2.1 Material parameters

A transistor is a complex device, and many different parameters are needed to explain its operation when used as a switch in an electrical circuit. It is necessary to differentiate between the material properties of the material of which the transistor is made, and the parameters describing the transistors operation in a circuit. In table 2.1 a comparison of important material properties between silicon and GaN is shown. Also see fig. 2.1, showing the different material properties and what transistor parameter they benefit.

Parameter	Unit	Silicon	GaN
Band-gap E_g	eV	1.12	3.39
Critical Field E_{crit}	MV/cm	0.23	3.3
Electron Mobility μ_n	cm^2/Vs	1400	1500
Relative permittivity ϵ_r	-	11.8	9
Thermal conductivity λ	W/cmK	1.5	1.3

Table 2.1: Silicon and gallium nitride comparison of important material properties for transistors. [11]

2.1.1 The band-gap

E_g describes the strength of the chemical bonds in a material, and a stronger bond implies that it is harder for an electron to jump around in the lattice structure. Notice that GaN has a bigger band gap, hence why it is called a wide-band-gap semiconductor. E_g has a direct impact on the operation and limitations of a given transistor structure.

2.1.2 Critical field

E_{crit} is the strength of electric field needed to start impact ionization. It is therefore directly correlated to the voltage breakdown rating of the device. A larger E_{crit} will in give a higher breakdown voltage.

2.1.3 Electron mobility

μ_n describes how easy an electron can move through a semi-conductor material when an electric field is applied. Higher μ_n is better, in terms of a lower $R_{ds,on}$ for a given breakdown voltage.

2.1.4 Relative permittivity

ϵ_r is a measure the capacitance met when constructing an electric field in a medium. Absolute permittivity is given as $\epsilon = \epsilon_0 \epsilon_r$. Where ϵ_0 is the electric permittivity in vacuum. Higher ϵ is better, in terms of lower $R_{ds,on}$ for a given breakdown voltage.

2.1.5 Thermal conductivity

λ, says how easy it is to transport heat away from the semi-conductor material. The higher the value, the better, since less cooling would be needed.

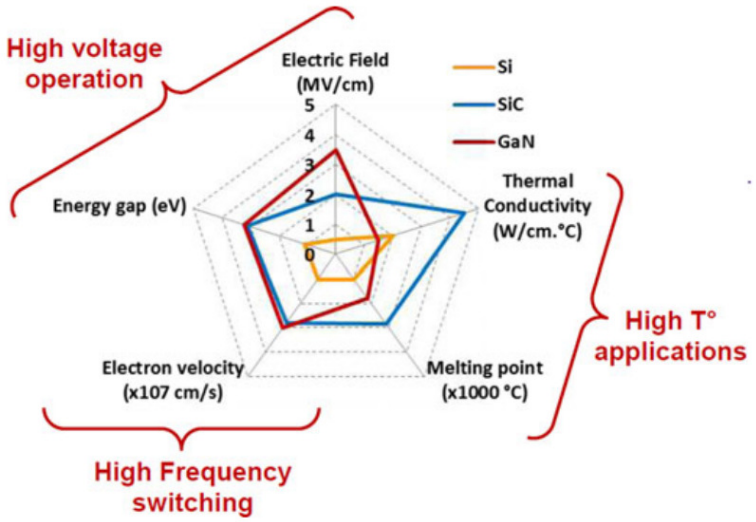


Figure 2.1: Material properties of gallium nitride(GaN), silicon(Si) and silicon carbide(SiC) Obtained from [14].

2.2 Transistor parameters

When designing a transistor, such as a Si MOSFET or GaN HEMT, trade offs between different parameters need to be made, and the limit is set by the material properties of the transistor material. For soft switching topologies, such as the LLC converter, four key transistor parameters are recognized [11].

2.2.1 Breakdown voltage

V_{BR} describes the maximum allowed voltage across the transistor before it is destroyed. The breakdown voltage is limited by the critical field, E_{crit}, and the drift region of the transistor. It can be calculated as

$$V_{BR} = \frac{1}{2} w_{drift} E_{crit} \tag{2.1}$$

Symbol	Expression	Name
C_{iss}	$C_{gs} + C_{gd}$	Input capacitance
C_{oss}	$C_{ds} + C_{gd}$	Output capacitance
C_{rss}	C_{gd}	Feedback capacitance

Table 2.2: Parasitic capacitances in a Si MOSFET. The same model holds for GaN HEMT.

The drift region is a design choice, directly correlated with the physical size of the transistor. Using eq. (2.1) and table 2.1, notice that for a given breakdown voltage, the drift region of the GaN device can be 14 times smaller for the same breakdown voltage. A smaller drift region implies reduction of physical size.

2.2.2 On-state resistance

$R_{ds,on}$, is a measure of the resistance of the transistor during the on-state. It is given as

$$R_{ds,on} = \frac{4V_{BR}^2}{\epsilon_0 \epsilon_r \mu_n E_{crit}^3} \tag{2.2}$$

eq. (2.2) can be plotted for GaN and Si shown in fig. 2.2. The unit is Ωmm^2 because there can always be a trade off between the area and the on-state resistance. Note that this is only a theoretical limit of the devices, and for GaN it does not represent devices currently available on the market. Still, GaN material has a much better theoretical limit.

2.2.3 Stored output charge

Q_{OSS}, is important for the ZVS operation of the resonant converter. It is caused by the parasitic capacitances between the terminals of a transistor. In table 2.2 and fig. 2.3 the different capacitances and their names are summarized. Q_{oss} is directly related to C_{OSS}, and can be calculated using eq. (2.3). Q_{OSS} expresses how much charge is stored during the off-state of the transistor for a given voltage, when the voltage between gate and source is zero. It is an important parameter in soft switching topologies, because it limits how fast the voltage transient during a switching transistion can be for a given current. In essence this limits the switching frequency.

2.2.4 Gate charge

Q_G is a measure of the required charge that must be injected or extracted to fully turn on or off the device. It is dependent on the C_{iss} given in table 2.2 and the applied voltage. Since the gate charge is dissipated at every turn-off, it will result in losses according to[11] $P_G = Q_G V_{gs} f_{sw}$. Here V_{gs} is the gate drive voltage, and f_{sw} the switching frequency.

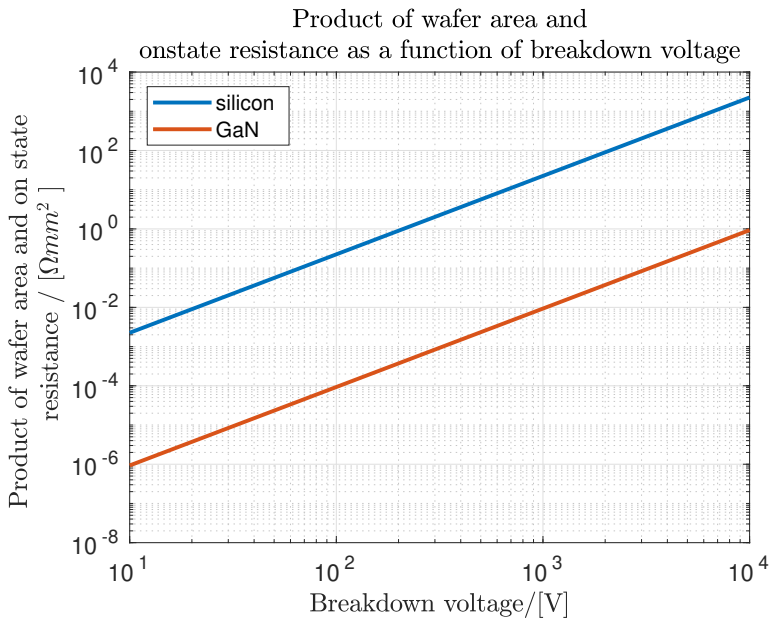


Figure 2.2: Theoretical limit of the product of area and on-state resistance as a function of breakdown voltage for silicon and GaN.

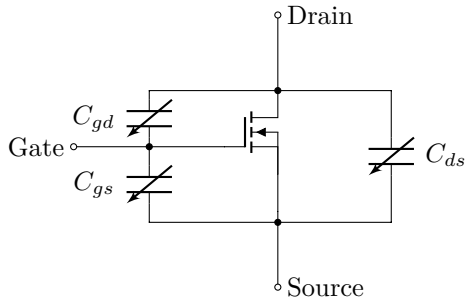


Figure 2.3: Parasitic capacitances of a Si MOSFET. The same model is valid for GaN HEMT. The capacitances are nonlinear and vary as a function of the applied drain-source voltage.

2.3 Types of GaN HEMT

In fig. 2.4 the basic structure of a GaN HEMT is shown. Notice the lateral structure and the 2DEG electron gas. GaN HEMT is inherently a naturally-on device due to the 2DEG electron gas. Two different approaches to this problem is proposed in [12] and [13]. The goal is to make a naturally-off GaN HEMT.

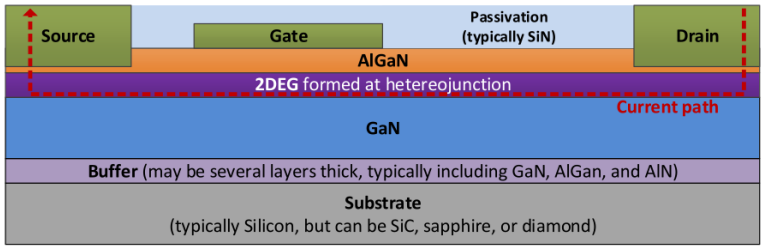


Figure 2.4: Structure of depletion-mode GaN HEMT. Layers are not to scale. Obtained from [13]

2.3.1 Cascode structure

One possible solution for making a normally-on GaN HEMT a normally-off device is cascoding it with a low voltage MOSFET. This means connecting the GaN HEMT in series with the MOSFET as shown in fig. 2.5. The two transistors can be packaged together into a single device. Normally-off GaN HEMT is then controlled by a gate-signal to the Si MOSFET. However new design challenges arise. This includes things such as minimizing the parasitic inductances of the packaging and matching of the capacitances of the two different transistors.

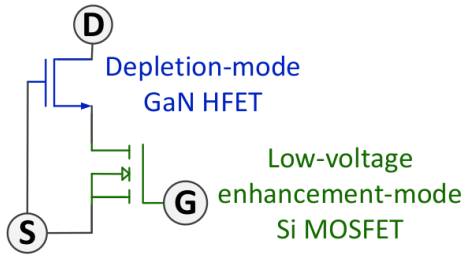


Figure 2.5: Cascode structure for the GaN HEMT. This makes it a normally-off device. Obtained from [13]

2.3.2 Altering the gate structure

Another possibility for making a normally-off GaN HEMT is altering the gate structure by different measures as shown in fig. 2.6. It is seen that several possible solutions exist, all of which includes altering the gate structure in some way.

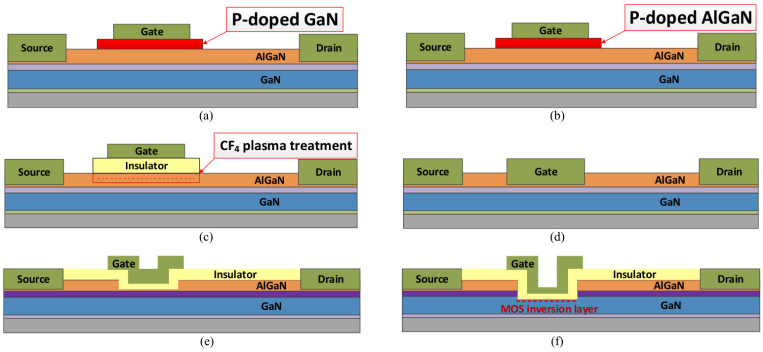


Figure 2.6: Different structure alternatives to make the GaN HEMT normally-off. a) p-doped GaN. b) p-doped AlGaN. c) Plasma treatment. d) Recessed gate. e) Insulated recessed gate. f) Hybrid MIS-HFET. Obtained from [12].

2.4 Nonlinearities

The capacitances given in fig. 2.3 are nonlinear. This means they are functions of the applied voltage across the terminals. More specifically all of the capacitances are functions of the drain to source source voltage, v_{ds} [11]. To get the relevant charges and stored energy, it will then be necessary to integrate over the whole voltage range, and the resulting charge will be valid only for the given voltage. In our case, the relevant charges and energies are Q_{OSS}, Q_G, E_{OSS} and E_G. The integral for charge is given as

$$Q = \int_0^{V_{ds,max}} C(v_{ds}) dv_{ds} \tag{2.3}$$

and for energy

$$E = \int_0^{V_{ds,max}} C(v_{ds}) v_{ds} dv_{ds} \tag{2.4}$$

where in the case for $Q_{OSS} = Q_{ds} + Q_{gd}$ or E_{oss} one would have to integrate both the capacitances C_{ds} and C_{gd} over the relevant voltage range.

From eq. (2.4) and eq. (2.3), one can calculate the so called charge-equivalent and energy equivalent capacitances [17]

$$C_{Q,eq}(V_{ds}) = \frac{Q_{OSS}(V_{ds})}{V_{ds}} \tag{2.5}$$

and

$$C_{E,eq}(V_{ds}) = \frac{2 \cdot E_{OSS}(V_{ds})}{V_{ds}^2} \tag{2.6}$$

Parameter	Symbol	Unit	MOSFET	GaN HEMT
Drain-to-source blocking voltage	V_{ds}	V	600	600
Drain-to-source on resistance at 25 °C	$R_{ds(on)}$	mΩ	70	70
Gate-to-source threshold voltage	$V_{gs(th)}$	V	4	1.2
Reverse recovery charge	Q_{rr}	µC	0.57	0

Table 2.3: Transistor properties comparison between Si MOSFET and GaN HEMT 70 mΩ from Infineon.

which can be used to represent the stored charge or stored energy at a given drain-to-source voltage. This can be useful for simplifying the analysis of the circuit, by neglecting the nonlinear behaviour of the capacitance.

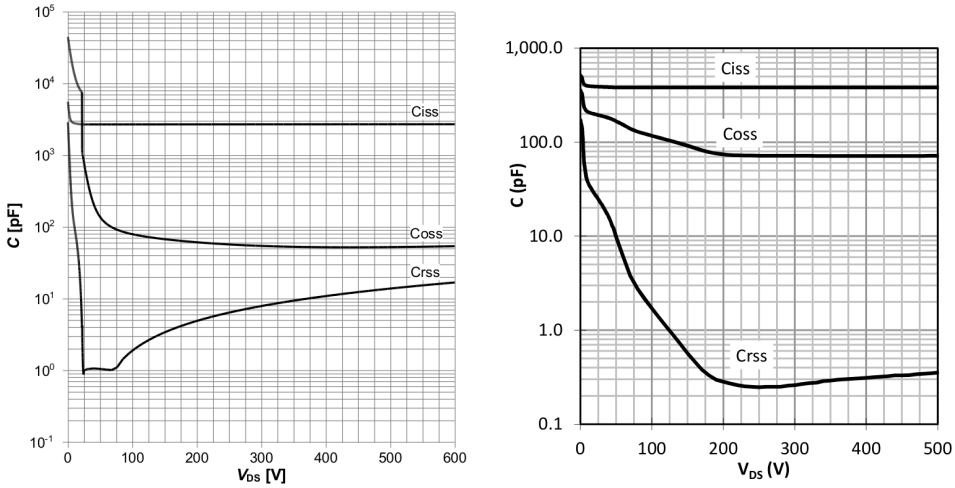
2.5 Comparison of a Si MOSFET and GaN transistor of similar rating

To get a better overview of the difference between Si MOSFETs and GaN HEMTs, a direct comparison of two transistors of similar rating is done. Infineon 600V CoolMOS Power transistor [18] is chosen the Si MOSFET. For the GaN HEMT, an Infineon 600V Enhancement Mode GaN Power transistor[19] is used. In table 2.3 important parameters are compared, and it is seen that the two transistors are quite equal in these parameters, except for the reverse recovery charge. GaN HEMTs have no reverse recovery charge, $Q_{rr} = 0$, which can be exploited in some topologies. Note that all these parameters are dependent on testing conditions. The testing conditions are given in the data sheets.

Comparing the stored charges is more difficult. As explained in section 2.4 the stored charge is nonlinearly dependent on the applied drain-to-source voltage. In fig. 2.7 capacitances are compared. Notice the much lower capacitances for the GaN HEMT, implying better switching characteristics due to less stored charge. The GaN HEMT capacitances also vary less. For the Si MOSFET, the capacitance drops from 40 000 pF to 80 pF when the drain-source voltage increases from 0 V to 100 V. For the GaN HEMT, the capacitance drops from only 300 pF to 70 pF for the same voltage increase. Both capacitances vary the most in the lower voltage region, but converge towards a constant capacitance as the voltage rises.

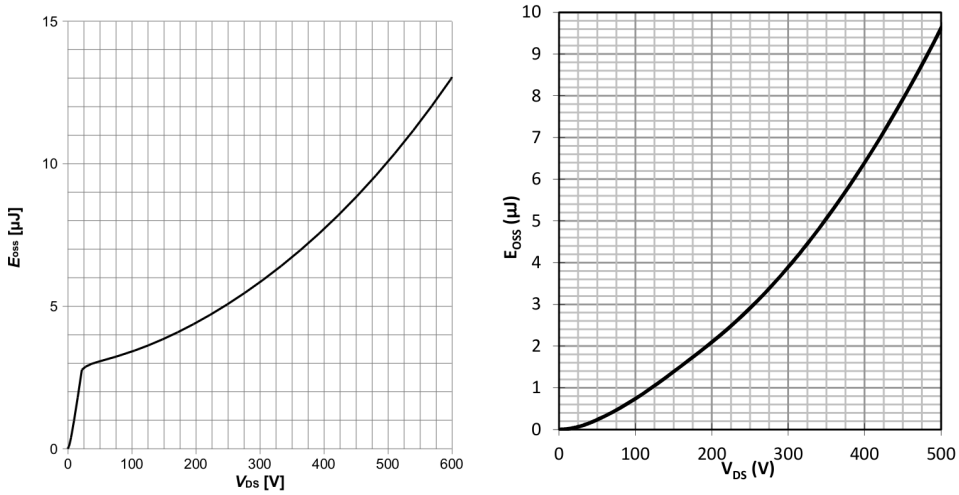
The stored energy can also be compared, and are shown in fig. 2.8, taken from the datasheet. At 400 V the MOSFET and GaN devices have almost the same stored energy. This is not the same as the stored charge, as explained in section 2.4.

A similar comparison for the reverse conduction characteristics is made in fig. 2.9. The GaN device does not have a body diode, but has reverse conduction capabilities. This is true in both cascoded and enhancement mode structures [12]. Ideal reverse conduction characteristics would be zero source-to-drain voltage, implying no reverse conduction losses. The characteristics of the GaN HEMT is much worse in terms of reverse conduction. This is seen because it has a signif-



(a) Si MOSFET capacitances (b) GaN HEMT capacitances

Figure 2.7: Comparison of the capacitances as a function of the drain-to-source voltage. Figures are taken from the respective datasheets [18] [19].

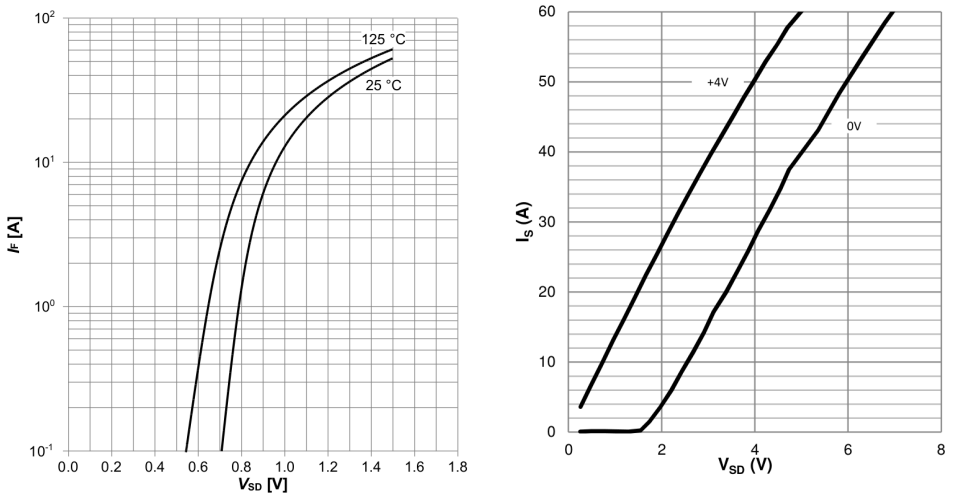


(a) Si MOSFET stored energy (b) GaN HEMT stored energy

Figure 2.8: Comparison of the stored energy as a function of the drain-to-source voltage. Figures are taken from the respective datasheets [18] [19].

icantly higher voltage drop for the same current. With worse reverse conduction characteristics, the allowed deadtime would also be less, because of higher losses.

The GaN HEMT it is also dependent on the gate-to-source voltage, implying that one could turn on the device also when conducting in the reverse direction to



(a) Si MOSFET reverse conduction characteristics

(b) GaN HEMT reverse conduction characteristics

Figure 2.9: Comparison of the reverse conduction characteristics. Figures are taken from the respective datasheets [18] [19].

reduce losses, this would however complicate control.

2.6 Figure of merit(FOM)

In an effort to standardize the comparison between different transistors, some authors propose a figure of merit(FOM) [11] [20]. It is not necessarily straight-forward to know what parameters to emphasise and not, and different FOMs are suggested for hard and soft switching topologies. For the purposes of this report, only the soft switching figure of merit is of interest. In [20] one such FOM is proposed

$$FOM_{SS} = (Q_{OSS} + Q_G) \cdot R_{DS(on)} \tag{2.7}$$

This again emphasises that Q_{OSS}, Q_G and $R_{DS(on)}$ are the main parameters of interest for a soft switching topology. The lower the FOM, the better.

This figure of merit is then used to to compare the two transistors in section 2.5. The results are summarized in table 2.4. Both the charges Q_{oss} are calculated from

	V_{ds}/[V]	Q_{OSS}/[nC]	$Q_G/[nC]$	$R_{ds(on)}$/[mΩ]	FOM/[pCΩ]
MOSFET	400	416	67	70	33810
GaN	400	40	4.1	70	3087

Table 2.4: Figure of merit for Si MOSFET and GaN HEMT 70 mΩ from Infineon.

the capacitance curves in fig. 2.7 and eq. (2.3). The Q_G and $R_{ds(on)}$ values are taken directly from the datasheets. They can be directly compared since they are given at about the same testing conditions. Looking at the score, the GaN HEMT scores significantly better than the Si MOSFET.

Comparing only two devices in this way, using the FOM might not be the most sensible. However, when faced with a choice between several transistors it makes more sense. Then it could be a useful tool in the preliminary design stages, when having to choose the best transistors for further testing among many possible choices.

2.7 Challenges and design considerations

Several other design challenges exist for GaN devices, and should be kept in mind when designing a GaN HEMT converter. In [12] many of them are recognized and discussed. They are briefly summarized here for reference.

A) Switching characteristics: because of smaller die size, the capacitances will be smaller. This results in faster switching characteristics which must be taken into account in design. Waveforms will differ between different transistors and board designs.

B) Device packaging: Because of faster switching transients, the parasitics will play a bigger role in design. Package parasitics should be taken into account. For example integration of the gate driver into the module improves the operation.

C) Gate driver requirements: For cascode GaN HEMT, the gate driver design is very similar to regular MOSFETs. For e-mode GaN HEMT on the other hand, more specific gate drivers are needed. Among other things the threshold voltage is lower.

D) Cross talk: Occurs because of interference between high side and low side devices, i.e upper and lower transistor in a half bridge. It might cause unwanted turn on and shoot-through. It can be prevented by slowing down the turn-on transient, but this will increase losses.

E) Operating temperature and thermal design: GaN HEMT has a positive temperature coefficient for onstate resistance. This is needed for paralleling to distribute the current evenly between devices. The threshold voltage is also quite stable with temperature. Thermal design can however be a challenge, and must be considered.

F) Reliability and qualification: Silicon devices have stringent reliability standards, and years of experience with lifetime models exist. GaN HEMTs might behave differently. Because of the relatively new technology accelerated lifetime testing is a challenge.

G) Device availability: GaN HEMT is a relatively new technology, and therefore has a low availability. This hinders widespread adoption.

H) Dynamic $R_{ds(on)}$: In lateral GaN devices, such as the GaN HEMT, it is in [21] reported that the the onstate resistance is a function of the blocking voltage, switching frequency and pulsed current. This poses a challenge for the development of GaN devices, because it complicates design.

I) Reverse conduction behaviour: Regular GaN HEMTs do not have a body diode. In a cascode or e-mode, body diode-like behaviour is present. However care has to be taken in design, since the behaviour is different than a regular Si MOSFET.

J) Breakdown mechanisms: Many converter designs rely on MOSFETs ability to survive temporary overvoltage. Lateral GaN devices do however not have this ability, and would be destroyed if subject to overvoltages. For this reason the datasheet ratings are often significantly lower than the real breakdown voltage.

Chapter 3

LLC resonant converter

Resonant DC-DC converters has gained popularity due to its high efficiency, high power density and low noise characteristics [22]. Another benefit is that the converter can provide both step-up and step-down operation, and a wide power range can be achieved at the output with only small variation in switching frequency [23] [24]. The converter also has zero voltage switching(ZVS) capabilities for the primary side switches for the whole operating range, and low voltage stress on the secondary rectifier [25]. With three reactive elements, the LLC converter is more complex than the series and parallell resonant loaded converters (SRL and PRL) [26], containing only two reactive elements. However, in [27] it is shown that this converter removes some of the disadvantages of the simpler series and parallel resonant converters, while maintaining its desirable characteristics.

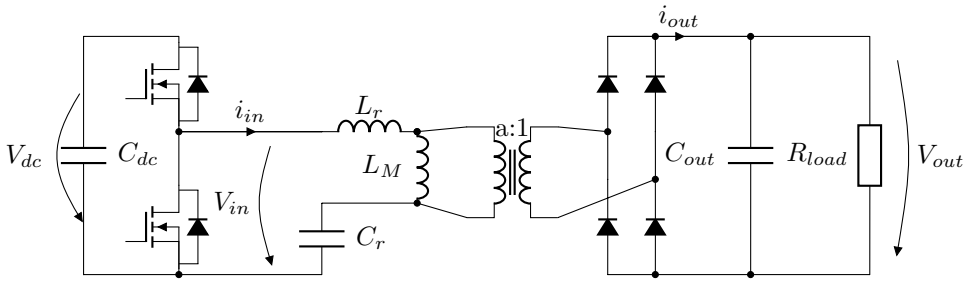


Figure 3.1: LLC converter with a half bridge structure at the input and full-bridge diode rectifier at the output.

An LLC converter is shown in fig. 3.1. C_{dc} and V_{dc} represents the DC-link. L_r, L_M and C_r form a resonant circuit on the primary side. The transformer has a winding ratio of $a : 1$. On the secondary side, the diode full-bridge rectifies the voltage at the output of the transformer. C_{out} is a large capacitance used to filter out the voltage ripple to the load. The load is represented by the resistance R_{load}.

3.1 Fourier transform of input voltage

In the next section, the transfer function of the converter will be derived. However this is only valid for a sinusoidal input. The voltage at the midpoint of the half-bridge shown in fig. 3.1 will be a square wave. The duty cycle will be 50 % [1] and the amplitude will vary between 0 and V_{dc}. To solve this problem, the fourier transform is applied to the square wave signal. The square voltage wave at the input is given as

$$V_{in} = \frac{V_{DC}}{2}[1 + \text{sgn}(\sin(2\pi ft))] \tag{3.1}$$

where $sgn()$ is the sign function [2]. Applying the fourier transform to eq. (3.1) gives [28]

$$V_{in} = \frac{V_{DC}}{2}[1 + \frac{4}{\pi}\sum_{n=1,3,5...}^{\infty}\frac{1}{n}sin(2\pi nft)] \tag{3.2}$$

With the transfer function H the following relation is valid

$$V_{out} = H(s)V_{in} \tag{3.3}$$

and by principle of superposition, using both eq. (3.2) and eq. (3.3), the output voltage will be given by

$$V_{out} = \frac{V_{DC}}{2}[H(0) + \frac{4}{\pi}\sum_{n=1,3,5...}^{\infty}\frac{H(j2\pi nf)}{n}sin(2\pi nft)] \tag{3.4}$$

where V_{in} the midpoint voltage as shown in fig. 3.1 and f the switching frequency.

3.2 Transfer functions

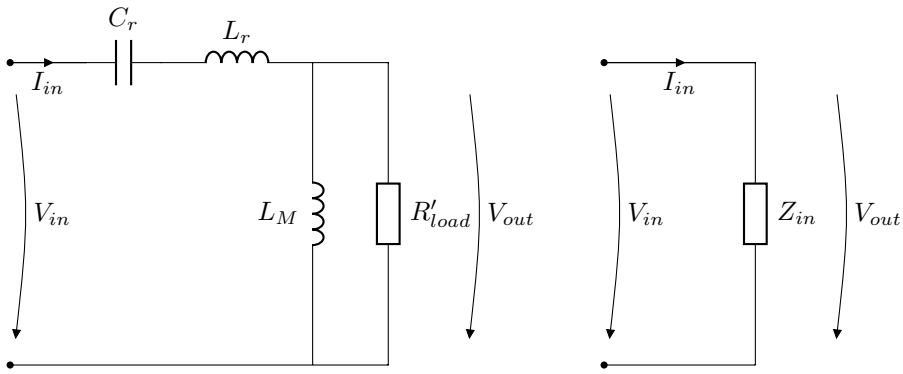
To get an overview of the gain characteristics of the converter, the transfer function is first analyzed. Derivation of the transfer function is done by using fundamental harmonic approximation(FHA) as in [27] [29] [30]. This is because the diode bridge represents a nonlinear element, it can not be included in the transfer function, and some assumptions are needed to justify neglecting it. The simplifying assumptions are [31]

- Steady state is assumed.
- Continous and sinusoidal current through the rectifier is assumed.
- Only the fundamental harmonic component transfers energy to the output. This is justified through the filtering behaviour of the resonant tank.

[1] Not considering the small interlocking delay of the half-bridge.
[2] https://en.wikipedia.org/wiki/Sign_function

- Output voltage ripple is neglected. This is justified because the output capacitance is assumed large.
- Elements are assumed to be ideal. The input voltage is a symmetrical square wave with no deadtime.

The approximations should be good at operating frequencies around the resonance frequency [32] [33]. This allows for a closed form solution of the gain characteristics of the converter. A linear equivalent circuit can then be derived. The resulting circuit is shown in fig. 3.2. In this report the gain characteristics are first calculated and then in chapter 4 the validity of the FHA are checked through simulations.



(a) Discrete components

(b) Impedance seen at the input represented by Z_{in}.

Figure 3.2: Equivalent circuit of the LLC converter using the fundamental harmonic approximation(FHA). Used for obtaining the transfer function.

With the assumptions made earlier, the output resistance will see rectified sinusoidal current with a fundamental component of size [27]

$$I_{out} = \frac{2\sqrt{2}}{\pi} I_{ac,rms} \tag{3.5}$$

and a fundamental component of the voltage

$$V_{out} = \frac{\pi}{2\sqrt{2}} E_{ac,rms} \tag{3.6}$$

meaning that the resistance seen from the input is

$$R_{ac} = \frac{E_{ac,rms}}{I_{ac,rms}} = \frac{8}{\pi^2} \frac{V_{out}}{I_{out}} = \frac{8}{\pi^2} R_{load} \tag{3.7}$$

also taking into account the the turns ratio, a, the resulting load is

$$R'_{load} = a^2 \frac{8}{\pi^2} R_{load} \tag{3.8}$$

Using eq. (3.8) the transfer function of the system can be calculated. The parallel branch formed by the magnetizing inductance and equivalent resistance is

$$sL_M||R' = \frac{sL_M R'}{sL_M + R'} \tag{3.9}$$

and the impedance seen from the input is then

$$\begin{aligned} Z_{in} &= \frac{1}{sC_r} + sL_r + sL_M||R' \\ &= \frac{1}{sC_r} + sL_r + \frac{sL_M R'}{sL_M + R'} \end{aligned} \tag{3.10}$$

The relationship between the voltages is then simply a voltage divider

$$\begin{aligned} H(s) &= \frac{V_{out}}{V_{in}}(s) \\ &= \frac{sL_M||R'}{\frac{1}{sC_r} + sL_r + sL_M||R'} \\ &= \frac{s^2 L_M C_r R'}{s^3 L_M L_r C_r + s^2(L_M + L_r)C_r R' + sL_M + R'} \end{aligned} \tag{3.11}$$

from which the gain of the converter at different frequencies can be calculated.

The transfer function of the current is

$$\begin{aligned} \frac{I_{in}}{V_{in}}(s) &= \frac{1}{Z}(s) \\ &= \frac{s^2 C_r L_M + sC_r R'}{s^3 L_M L_r C_+ s^2(L_M + L_r)C'_R + sL_M + R'} \end{aligned} \tag{3.12}$$

from which it can be calculated whether the resonant tank is capacitive or inductive.

Using eq. (3.11) together with eq. (3.4) the assumption that only the fundamental component of the input voltage is considered can then be justified.

3.3 Operating areas

Next the different operating areas of the LLC converter is discussed.

3.3.1 Gain

As shown in [23], two different resonant frequencies exist. One for when the secondary side diodes are conducting and therefore L_M is short circuited,

$$f_{R1} = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{3.13}$$

and another one for when the secondary side is open and current also flows through L_M.

$$f_{R2} = \frac{1}{2\pi\sqrt{(L_r + L_M)C_r}} \tag{3.14}$$

where $f_{R2} < f_{R1}$.

As done in [29], new variables are introduced. First the Ratio of total inductance to series inductance [3]

$$m = \frac{L_r + L_M}{L_r} \tag{3.15}$$

secondly the normalized switching frequency

$$F = \frac{f_s}{f_{R1}} \tag{3.16}$$

and the quality factor

$$Q = \sqrt{\frac{L_r}{C_r}}\frac{1}{R'} \tag{3.17}$$

Using these variables, the transfer function in eq. (3.11) is rewritten as

$$\frac{V_{out}}{V_{in}}(j\omega) = \frac{F^2(m-1)}{(F^2m-1) + jF(F^2-1)(m-1)Q} \tag{3.18}$$

where j signifies the complex part of the transfer function. Through introducing these variables it is easier to see what parameters matter in the design of the converter. For example, the absolute value of the inductances are not important for the gain characteristics, but rather it is the ratio between them, m, that matters. The same can be said for Q, where it is seen that the ratio of the resistance to the characteristic impedance, $Z_0 = \sqrt{\frac{L_r}{C_r}}$ that matters.

In the same fashion one can rewrite the transfer function for the input current

$$\frac{I_{in}}{V_{in}} = \frac{1}{Z} = R'\frac{(1-F^2m) + j(FQ(m-1)(1-F^2)}{-F^2(m-1) + j\frac{F_x}{Q}} \tag{3.19}$$

which shows that the input current is directly proportional to the load.

The gain of the converter for different ratios of the inductances and different quality factors are shown in fig. 3.3. It is verified here that both buck and boost mode can be achieved. Note that above f_{R1} the gain is always less than one. The frequency of maximum gain is located somewhere between f_{R2} and f_{R1}, depending on the quality factor Q or load R. In fact, the frequency at which the maximum gain occurs is called the *system resonance frequency*.

It is seen that the m values influence the maximum gain of the converter, and also the location of maximum gain. Increasing m lowers the second resonant

[3] Perhaps more well known is the inductance ratio,$\kappa = \frac{L_M}{L_r}$, this gives $\kappa = m - 1$.

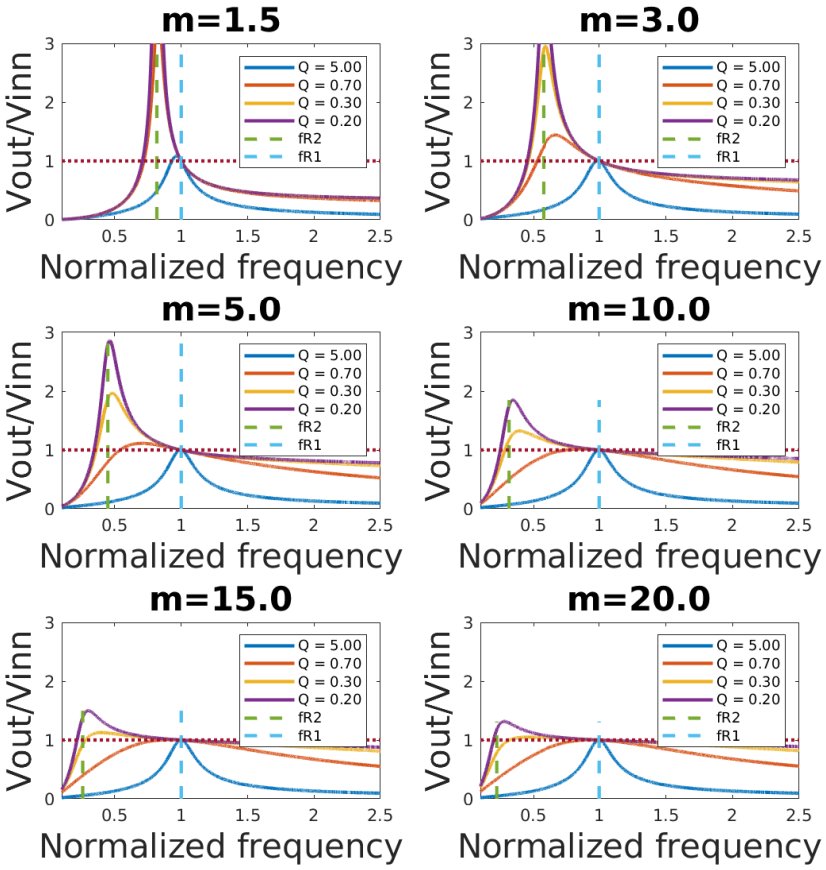


Figure 3.3: Gain curves of the transfer function $\frac{V_{out}}{V_{in}}$ for different component parameters.

frequency f_{R2}. In fact, $f_{R2} = \frac{f_{R1}}{\sqrt{m}}$. Note also that the value of Q decides the maximum gain, and the steepness of the gain-curve around the lower resonance frequency.

In fig. 3.3 it is also seen that the transfer function, H, will have decreasing gain with increasing frequency. Combining this with the fact that the higher harmonic components will have a lower amplitude, they can therefore be ignored. This in essence means that the resonant tank filters out the higher harmonic components [27].

3.3.2 Phase shift

Another imporant aspect of the converter is if it is operating inductively or capacitively. That is to say, if current is lagging or leading the voltage. The details of why, is explained in section 3.4. At frequencies $f < f_{R2}$ the converter is always capacitive, while at frequencies $f > f_{R1}$ the converter is always inductive. However, at frequencies $f_{R2} < f < f_{R1}$ there exists a critical load resistance value [34]

$$R_{crit} = \sqrt{Z_{o_0} \cdot Z_{o_{\inf}}} \tag{3.20}$$

where Z_{o_0} and $Z_{o_{\inf}}$ is the impedance seen from the input in fig. 3.2 with the load short-circuited and open-circuited, respectively. A load $R > R_{crit}$ gives inductive operation and $R < R_{crit}$ gives capacitive operation. The critical resistance is given as

$$\begin{aligned} Z_{o_0} &= \frac{1}{sC_r} + sL_r \\ Z_{o_{\inf}} &= \frac{1}{sC_r} + s(L_r + L_M) \\ R_{crit} &= \frac{\sqrt{(1 + s^2 C_r L_r)(1 + s^2 C_r (L_r + L_M)}}{sC_r} \end{aligned} \tag{3.21}$$

which is a function of the frequency. This means that phase shift in the intermediate region is dependent on both load-resistance and frequency.

An illustrative plot of the different operating areas is shown in fig. 3.4. A positive angle means inductive operation and negative angle means capacitive operation. It is clearly the case that the resonance frequencies that above f_{R1} the operation is always inductive, while below f_{R2} it is always capacitive. See also that as expected, Q, which is dependent on the load resistance, is the decisive parameter in the intermediate region. The system resonance frequency, where maximum gain occurs, marks the boundary between inductive and capacitive operation for a given load.

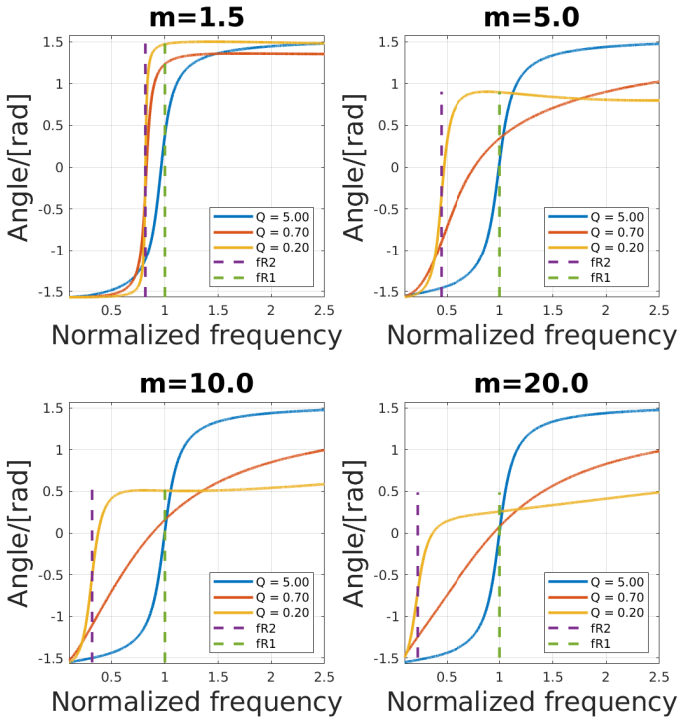


Figure 3.4: Phase shift between voltage and current as seen from the midpoint of the half-bridge at the input of the LLC resonant tank. Shows the different operating areas and whether they are inductive or capacitive.

3.4 Zero voltage and zero current switching

This section explains why the inductive behaviour is important for the operation of the converter. The phase shift between current and voltage seen at the midpoint of the half-bridge, decides whether the converter can be operated with zero voltage switching(ZVS) or zero current switching(ZCS).

To explain this, it is referred to the ZVS transition shown in fig. 3.5. The transition shown is from the lower switch on, to the upper switch on. The current is flowing out of the resonant tank when the transistion begins. When the lower switch turns off, the current starts to commutate from the lower switch to the body diode of the upper switch. Before the body diode of the upper switch can start to conduct, the distribution of charge across the output capacitances of the transitors must be changed. The lower transistor must be charged from 0 to Q_{oss} while the upper must be discharged from Q_{oss} to 0. Q_{oss} is defined in section 2.2.

This transition occurs during the deadtime, $t_{dead} = t_2 - t_1$. The choice and effects of this interlocking delay is further explained in section 3.5. When turning

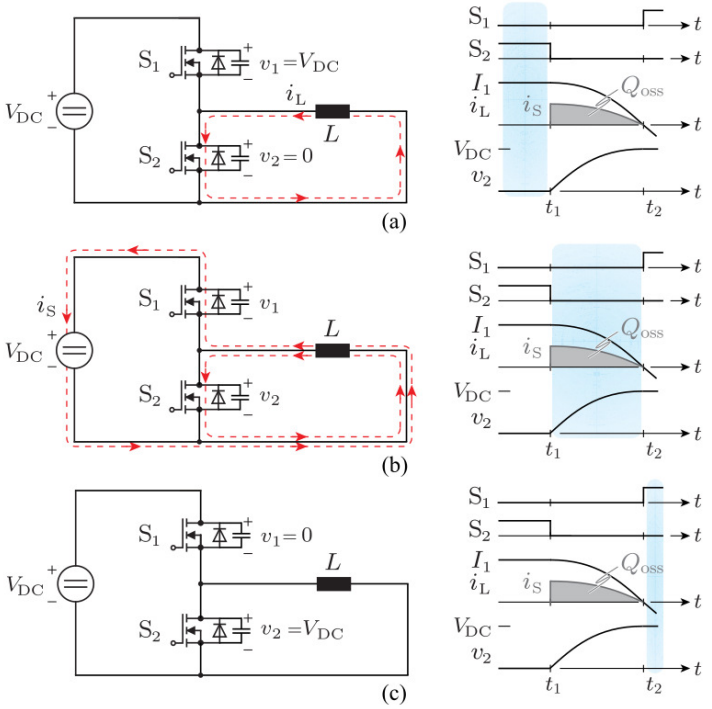


Figure 3.5: A zero voltage switching transition. a) The lower switch is on, and the upper is off. b) The lower switch is turned off, since the inductance clamps the current, it starts to commutate from the lower switch to the upper. c) The voltage across the upper switch reaches zero, and it can be turned on with ZVS. The current still flows in the same direction or is zero depending on operating point. Obtained from [17].

on the upper transistor, the body diode is already conducting, implying that the voltage is zero, and ZVS is achieved.

If the current was in the opposite direction in this case, with current into the resonant tank, the body diode of the upper switch could not conduct, and ZVS would not be achieved. This example indicates that ZVS occurs at **switch-on** of the transistors, when the current lags the voltage. This implies that the tank must be **inductive**.

Inherent to every ZVS operation is the presence of a current clamping inductance, which forces the current to keep flowing during the commutation period from t_1 to t_2. In [17] it is shown that for soft switching to occur

$$\frac{1}{2}LI^2 \geq Q_{oss}(V_{DC}) \cdot V_{DC} \tag{3.22}$$

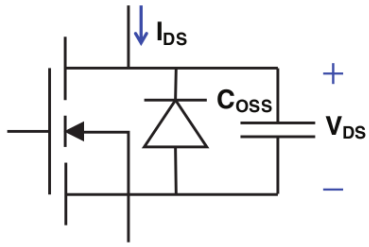
where I_{in} is the current in the resonant tank. For the LLC converter $L = L_r + L_M$.

eq. (3.22) says that the energy stored in the inductance must be bigger than the stored energy in the transistor capacitance. Two conditions must be present for ZVS to occur

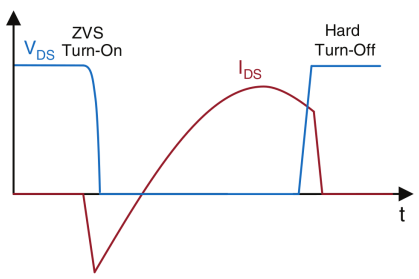
- The current must have the correct direction with regards to the voltage, i.e. inductive behaviour.
- The stored energy in the inductance must be bigger than the stored energy in the transistor capacitances, according to eq. (3.22).

This stored energy requirement also indicated in fig. 3.5. The stored charge must go to zero before the switching transition can be completed with ZVS.

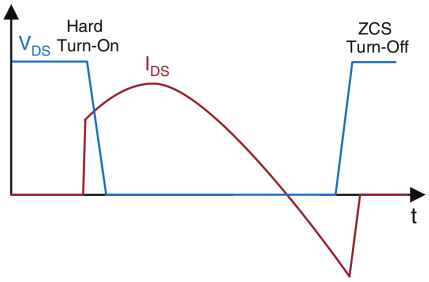
Consider again the same case as before, but when the tank is capacitive. The current in the lower switch would be forced to zero before the voltage would be allowed to rise. This means that **ZCS** appears at **turn off** when the resonant tank is **capacitive**. The switching current and voltage waveforms for ZVS and ZCS for a resonant converter are shown in fig. 3.6.



(a) Labeling of current and voltage in transistor



(b) Zero voltage switching. Occurs for **turn-on** for frequencies above system resonance frequency.



(c) Zero current switching. Occurs for **turn-off** for frequencies below system resonance frequency.

Figure 3.6: Switching waveforms for a transistor in a resonant converter. Obtained from [11].

ZVS is often preferred over ZCS for Si MOSFETs and GaN HEMTs, because of the internal capacitances of the switch [26]. For ZCS, the energy stored in the capacitances need to be dissipated in the switch at every turn on, leading to higher

losses. However, at ZVS these losses do not occur, since the charges are already removed when the voltage is zero. Even though ZVS only occurs at turn on, lossless snubber capacitors can be placed directly across the FET devices without any discharge resistors being needed [27] [26]. In theory then, when operating with ZVS, only the conduction losses persist, since the switching losses are eliminated.

3.5 Deadtime

An interlocking delay, also called deadtime, between the turn-off of one switch and turn-on of the other is needed to avoid short circuiting of a half-bridge structure. An important distinction is made here. When referring to **deadtime** most often the **chosen** time delay in the DSP-controller is what is meant. However, the deadtime is needed because of the inherent delay in a transistor switching process. After the gate-source voltage changes, there is a delay before the drain-source voltage starts changing. This is called **turn-on delay time** or **turn-off delay time** depending on whether the transistor is switched on or off. The deadtime must be bigger than the inherent delay.

It is during the deadtime that the internal output capacitance, explained in section 2.2, of the switch needs to be discharged to make possible the zero voltage switching. The minimal amount of time needed is current dependent, the relation is [20].

$$t_{ZVS} \geq \frac{Q_{OSS}}{I_{ZVS}} \tag{3.23}$$

where t_{ZVS} is the time needed to discharge the effective output charge, Q_{OSS}. I_{ZVS} is the current into the resonant tank during the switching transistion. The term on the right hand side of eq. (3.23) corresponds to the inherent delay time of the switch transition. eq. (3.23) expresses that the chosen deadtime in the DSP must at minimum be larger than the inherent delay. The expression holds when assuming constant current of I_{ZVS} during the commuation of current from one transistor to the other. In the LLC converter this current would correspond to the current that goes into the resonant tank, I_{in}, at the moment of switching.. The assumption of constant current would be valid when the dead-time is small compared to the total switching period. Since no power is delivered to the output during the deadtime, the efficiency is also dependent on the choice of t_{dead}. This means the effective power delivery period would decrease with an increasing deadtime, and therefore for a given power at the output the rms-current would increase according to [20]

$$I_{in,rms} \propto \frac{1}{\sqrt{\tilde{D}}} \tag{3.24}$$

where $\tilde{D}$ is the effective duty cycle

$$\tilde{D} = 0.5 - \frac{2t_{dead}}{T} \tag{3.25}$$

with t_{dead} being the deadtime. T is the time of one switching cycle, dependent on the switching frequency, f, $T = \frac{1}{f}$. eq. (3.25) implies a third requirement for achieving ZVS

- The required deadtime, limited by the inherent delay according to eq. (3.23), must not be too big. In eq. (3.25), $\tilde{D}$ must be bigger than 0. This gives $t_{dead} < \frac{T}{4}$.

3.6 Operation modes

Using the previously derived transfer functions for analyzing the converter, the explicit time behaviour is lost. Different operating modes of the converter in the time domain is presented here.

In [24] six different operating modes are recognized for the LLC converter. They are given for inductive operation and in the region between f_{R2} and f_{R1}, shown in fig. 3.7 and fig. 3.8. Although the analysis is done for a different rectifying bridge on the secondary side, the same principle operating modes hold with a full-bridge rectifier on the secondary side as well.

Because of symmetry, only three of the modes are needed to fully characterize the behaviour. The modes are

- Mode 1: Begins just as the lower switch S2 turns off. It is assumed that the converter is operating in the inductive region, the current is lagging the voltage, and is negative. This means it is flowing out of the resonant tank. This forces the diode D_{s1} to start conducting, and creates zero voltage switching conditions for S_1.
- Mode 2: S_1 is turned on, and the current i_p starts to increase at the same time as the diode on the secondary side starts to conduct. Power is transferred to the load. The voltage across L_M is clamped to the output voltage times the turns ratio, $a \cdot V_o$ and the energy in the magnetizing inductance builds up linearly. This also means that the magnetizing inductance does not take part in the resonant operation in this mode, i.e the resonance frequency is f_{R1} from section 3.3. The mode ends as i_{D1} reaches zero and the diode on the secondary side stops conducting, and $i_p = i_m$.
- Mode 3: The secondary side voltage is now lower than the output voltage, and diodes on the secondary side are reverse biased. The output capacitance must provide the energy to the load during this period. The magnetizing inductance once again takes part in the resonance operation, and the resonance frequency is f_{R2} from section 3.3. The mode ends as the switch S_1 turns off.
- Mode 4-6: Mode 1-3 repeats, only now for the lower switch.

Modes 3 and 6 will disappear if the switching frequency equals f_{R1} [24]. This makes sense as then will switch S_1 off at the exact same time as the diodes on the secondary side stop conducting. The waveforms are shown in fig. 3.8.

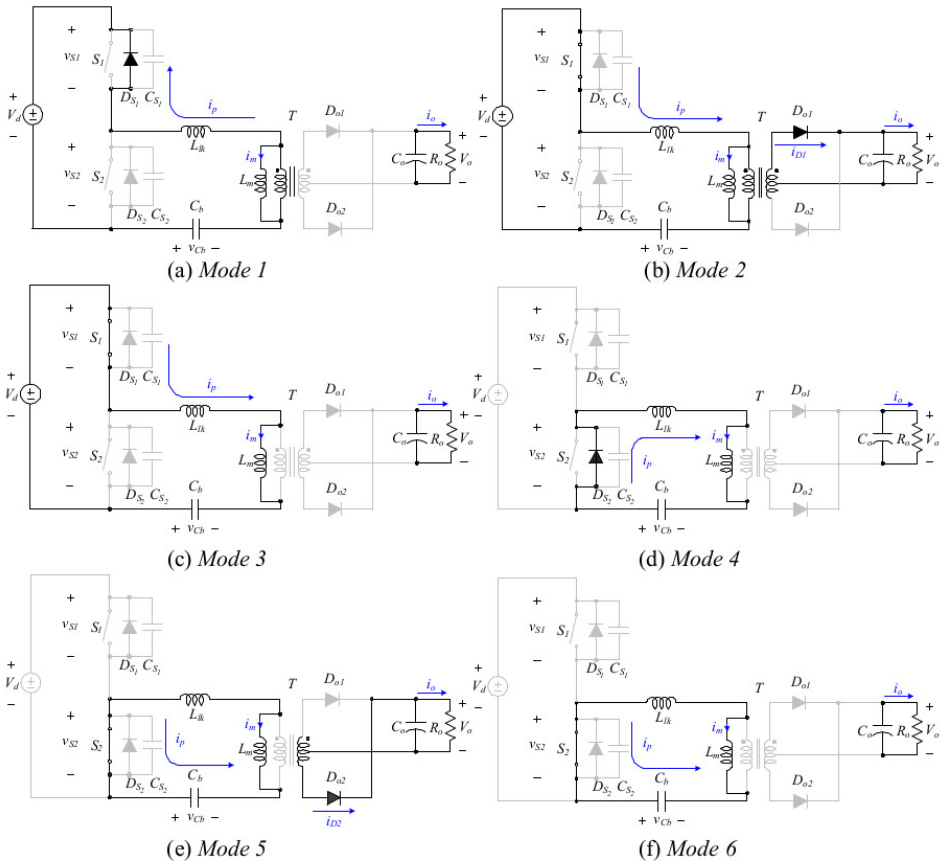
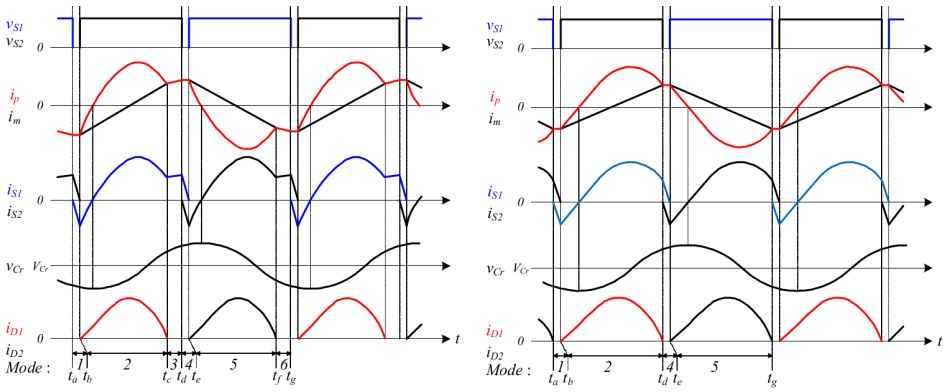


Figure 3.7: Six different operating modes for a LLC converter. Obtained from [24].

Note that energy is only transferred to the load during mode 2 and 5. This is a drawback of the topology, since circulating energy will lead to losses in the converter. This also means that the further away from resonance frequency the converter is operated, the higher the circulating energy and component stresses because the modes 2 and 5 will take up relatively shorter intervals of a whole fundamental period [11].

In [23] several other modes are recognized, for different frequencies, and depending on if the converter is in boost or buck mode. They are categorized into continuous and discontinuous depending on whether or not the diodes on the secondary side conduct through the whole switching period, or not.

It is also interesting with the possibility of a cutoff frequency, above which no power flows to the output. This is a result of the magnetizing inductance never exceeding the voltage at the output, so the diodes are always negatively biased. The normalized cutoff frequency is then [23]



(a) Six mode case (b) Four mode case

Figure 3.8: Analytical waveforms for the LLC resonant converter. V_{Cr} is the same is V_{Cb} in fig. 3.7. Obtained from [24].

$$F_{CO} = \frac{k_1 \frac{\pi}{2}}{cos^{-1}\left(\frac{1}{M(1+l)}\right)} \tag{3.26}$$

where

- M is the ratio of output to input voltage, $M = \frac{V_2}{V_1}$
- l is the ratio of series inductance to parallel inductance, $l = \frac{L_r}{L_M}$. In terms of m, $l = \frac{1}{m-1}$.
- k_1 is the ratio between the two resonance frequencies, $k_1 = \sqrt{\frac{l}{1+l}}$

The existance of this cutoff-frequency depends on design. Looking at eq. (3.26), it is seen that $M(1+l) > 1$ for this too be true, since the term inside the arccos must be below 1.

3.7 Optimal design considerations

Compared to PWM converters, the optimal design of a LLC converter is more difficult, because of the existance of multiple modes of operation, both below and above the resonance frequency [35]. The term *optimal design* means here the design that maximizes the efficiency of the converter.

In regular series resonant converter(SRL) or parallel resonant convert(PRL) designs only the Q-value is needed for design. However when designing the LLC one must also choose the ratio of the inductances m, complicating the design procedure. For a given maximum gains ratio, infinitely many combinations of Q and m values exist, as shown in fig. 3.9

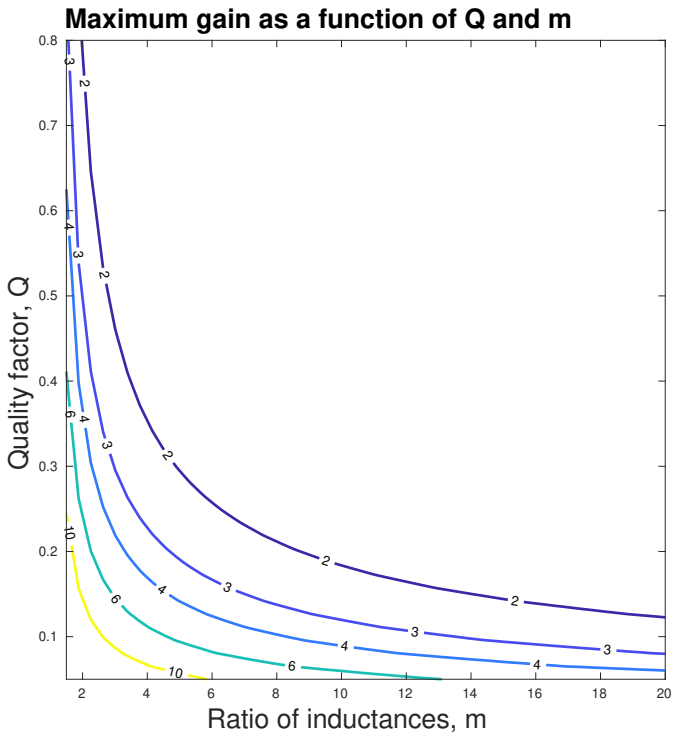


Figure 3.9: Gain curves as a function of Q and m.

There are several different considerations that need to be taken into account. Since the converter has ZVS at turn on, and snubbers for reducing turn-off losses, the switching losses are low. What remains then are the conduction losses. In [36] it is shown that the rms currents(on both primary and secondary side) are inversely proportional to the magnetizing inductance, $I_{rms} \propto \frac{1}{L_M}$. This indicates that the magnetizing inductance should be chosen as large as possible, to limit rms-current and therefore the conduction losses. However, the peak magnetizing current, which is responsible for the discharge of the transistor capacitances to achieve ZVS, is also inversely proportional to the magnetizing inductance [36]. This means that choosing L_M too big would result in loss of ZVS capabilities. The optimal choice of L_M is then the value that makes the current equal to the ZVS requirement, but not bigger. In [36] this is shown to be

$$L_M = \frac{t_{dead} T}{16 C_{oss}} \tag{3.27}$$

where T is the time of one switching cycle, $T = \frac{1}{f}$. t_{dead} is the interlocking delay and C_{oss} is the transistor capacitance as explained in section 2.2. Since the converter is controlled by varying the frequency as discussed in section 3.10.1, T and also t_{dead} will vary, and the choice of L_M will be made in regards to the nominal operating

point.

From the definitions of Q, m and f_{R1} in eq. (3.17), eq. (3.15) and eq. (3.13) results

$$L_M = \frac{R'Q(m-1)}{2\pi f_{R1}} \tag{3.28}$$

where it is seen that for a given L_M, the product of Q and $(m-1)$ is constant. Comparing this to fig. 3.9 and choosing a maximum gains ratio, one could then read out the value for Q and m for a given design.

Other considerations include the switching frequency. Increasing the frequency range would allow for smaller reactive components, and therefore higher power density. This could however lead to thermal problems in the both the transistors and reactive elements. This is because the switching losses increase with frequency, as shown in section 2.2. For reactive elements, phenomena such as skin effect and hysteresis losses play a bigger role at higher frequencies.

3.8 Snubbers

Power electronics transistors are subject to both high current and high voltages. If their operating limits are exceeded, they will be destroyed. In addition to high voltages and high currents, rapid changes, i.e. large $\frac{dv}{dt}$ and $\frac{di}{dt}$ in the transistor are also harmful. Snubbers are often included in the circuit to avoid this problem. Many different solutions exist [26]. In this report, only one snubber is considered. It is shown in fig. 3.10. It consists only of a capacitor in parallel with the transistor. This snubber is chosen because of its simplicity, and suitability for the soft-switching topology at hand. It will later be used in lab measurements.

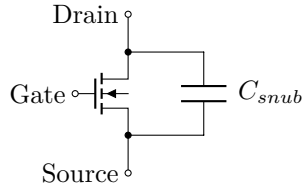


Figure 3.10: Simple capacitor snubber in parallel with the transistor. Parasitic capacitances of the transistor is not included in the figure.

The snubber capacitance, C_{snub}, will appear in parallel with the transistor parasitic capacitance C_{ds} discussed in section 2.2. A large C_{snub} will give a slower rise and fall of the drain-source voltage, i.e. $\frac{dv_{ds}}{dt}$ will be lower, as indicated by the capacitance equation

$$C\frac{dv}{dt} = i \tag{3.29}$$

For a soft switching converter operating with ZVS, the capacitance C_{snub} will also affect the deadtime needed, because it affects the stored charge. Often in

snubbers, a power-dissipating resistor is present, meant to dissipate the stored energy in the snubber capacitor. However, this is not always needed in a soft-switching converter because the capacitances will be discharged through converter operation. Since the capacitance in theory is lossless, it does not directly increase losses.

3.9 Other topology variations

Several other topology variations exist, and should be kept in mind before concluding the final design. Different topology variations can offer different benefits if utilized correctly.

3.9.1 Full bridge on input side

Until now, only the half-bridge structure at the input side of the resonant tank has been considered. However, a full bridge on the primary side is a also a possible choice. For the same power delivered to the load, the full-bridge will have half the rms-current as the half-bridge structure [22]. This is because the full-bridge will have a larger voltage margin, from $+V_{dc}$ to $-V_{dc}$, instead of $+V_{dc}$ to 0 for the half-bridge. This could mean that the conduction losses, $P = RI^2$, could be reduced by a transition to a full-bridge topology. However the onstate-resistance would also double for a fullbridge. Also, because the number of transistors are doubled, the switching losses will increase. This suggests that a fullbridge could be a valid topology, especially for high current applications, however it is not immediately obvious for a given application which one is better.

3.9.2 Split capacitor and clamping diodes

There is a possibility of splitting the capacitance of the resonant tank in two and introducing clamping diodes across the capacitors, as shown in fig. 3.11. In [37] it is argued that this can help limit overcurrent and also reduce current ripple.

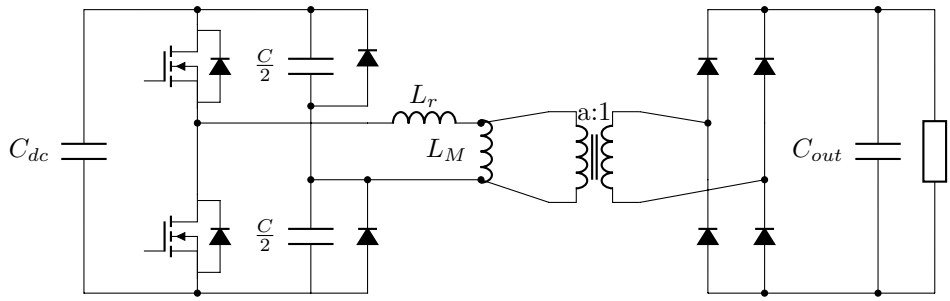


Figure 3.11: LLC converter with split capacitor and clamping diodes to limit overcurrent and reduce current ripple.

3.9.3 Inluding the magnetic components in the transformer

As discussed in [38][39] the transformer can be designed such that the inductances L_r and L_M are the transformer parasitics. L_r being the leakage inductance, often denoted L_σ, and L_M the magnetizing inductance. These inductances come at a low cost then, since isolation is required. The inductances are then present in the circuit through the design of the transformer. The leakage inductance can be varied by controlling the airgap of the transformer. By varying the placement of the windings on the transformer core, the magnetizing inductance can be changed. This saves cost, as the number of inductances needed is decreased. The capacitances are all discrete devices.

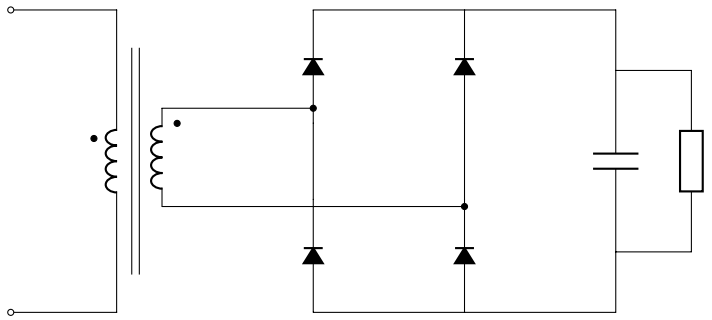
3.9.4 Choice of rectifier at output

Many possibilities exist for rectification at the secondary side of the transformer. Three different possibilities are shown in fig. 3.12. [40] [41].

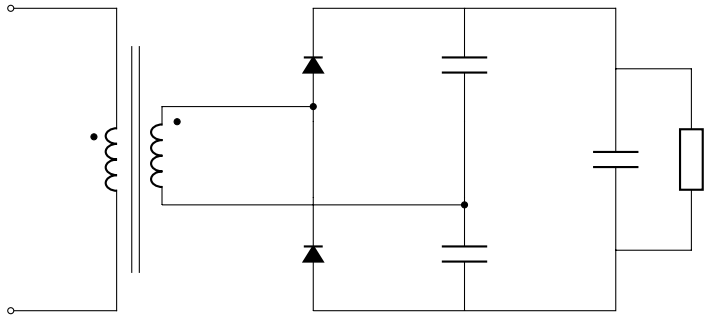
Together with the impact of the parasitics discussed in section 3.10.2, other advantages and disadvantages of the different rectifier solutions must be considered. The full bridge has two diodes in the conduction path at all times, which would be a disadvantage for low voltage outputs. The center tap and the current doubler only has one diode in the conduction path at a given time, but in return the diodes experience double the voltage stress compared to the full-bridge solution.

Synchronous rectification

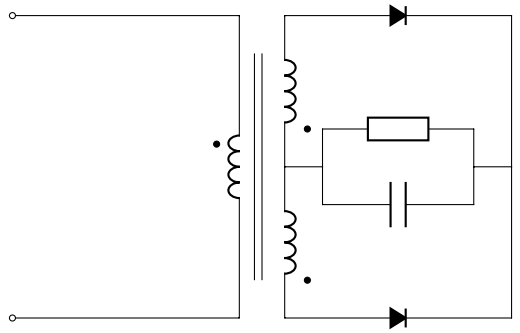
To reduce conduction losses, often the rectifier diodes are replaced by transistors. Diodes have a constant forward voltage drop, while the transistors only have an on-state resistance. For relatively low currents the losses are then reduced. This concept is named synchronous rectification(SR). SR however raises the problem of driving the transistors correctly, avoiding shoot-through but still conducting when needed. One driving scheme for a center-tap rectifier is proposed in [42]. How to control the transistors for synchronous rectification depends on the switching frequency at the input side of the converter. The basic idea of the driving scheme is to detect the drain-to-source voltage of the SR, and adjust the turn-OFF time accordingly, as to minimize the body diode conduction time.



(a) Full bridge rectifier



(b) Voltage doubler rectifier



(c) Center tap rectifier

Figure 3.12: Three possible rectifier solutions.

3.10 Low load problems

One of the essential problems of the LLC resonant converter is that the output voltage cannot be regulated at very light loads [43]. Other problems and challenges arise at low load as well. Below these problems are discussed.

3.10.1 Control problems

Several methods of control for the LLC converter exists, discussed in [44]. Arguably the simplest control method is simple output voltage feedback, and then adjusting the frequency along the gain curves given in section 3.3 to achieve the wanted voltage. However, as discussed in [45], and shown through the gain curves in section 3.3, since the converter gain is heavily influenced by the load variation, this is not a straight-forward task.

From the gain curves shown in fig. 3.3, not considering the parasitics, it can be seen that for low loads the gain curve tends towards 1 for all frequencies above the resonant frequency f_{R1}. This implies that the converter is hard to control for low loads, and might even be uncontrollable, in the sense that the wanted reference voltage might not be attainable. Huge deviations in frequency from the resonant frequency would be needed to change the voltage at the output. Higher frequencies gives increased switching losses, while lower frequency will move the converter into the capacitive region and lose ZVS as discussed in section 3.4. Both result in a reduction of efficiency. This problem is also exaggerated by the effect of parasitics in the converter, discussed later in section 3.10.2.

One possible remedy to this problem is to control the input voltage as well. In the case at hand, this corresponds to controlling the PFC-boost stage of the converter, so that the DC-link at the input of the LLC is changed.

A different approach is discussed in [44] [46] [47]. It is proposed that during low load, burst mode control should be applied. Burst mode means that some of the driver circuit pulses are skipped, meaning that instead of the regular 50% duty cycle squarewave, some periods of time only the lower transistor is turned on. This means no voltage is applied at the input of the resonant tank. Through this modulation technique the output voltage can be controlled also for low loads. However, some new problems may arise. This method induces low frequency ripple with the same frequency as the burst mode, which could lead to problems with EMC-requirements. [4].

3.10.2 Effect of parasitics

In [41] the impact of parasitics on the LLC converter operation is discussed, by introducing the parasitics to the FHA analysis. It is shown that the parasitics influence the converter operation especially at low load[5]. Four different influencing parasitics are discussed [41]

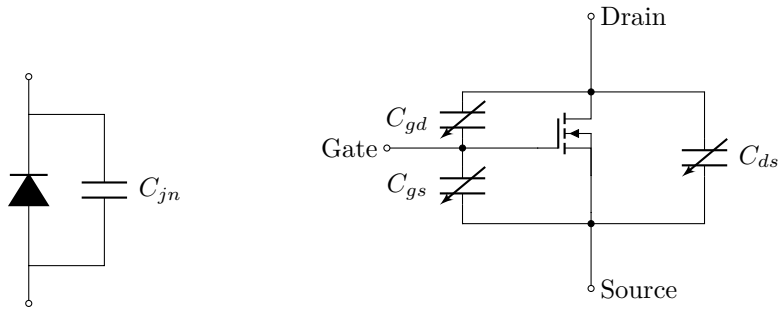
- C_{oss}, output capacitance of MOSFET
- C_{TR}, transformer wiring capacitance
- L_{lks}, leakage inductance at transformer secondary side

[4] One example of a EMC regulation standard that must be met is psophometric noise, https://en.wikipedia.org/wiki/Psophometric_weighting

[5] Since a capacitor is in parallel at the output, meaning constant voltage output, a low load would mean a high resistance, R_{load}.

- C_{jn}, junction capacitance of rectifier diode

An explanation of the C_{jn} and C_{oss} is given in fig. 3.13. In [41] it is found that the junction capacitance of the rectifier diodes have the biggest impact on the operation of the converter, since it increases the voltage gain at very light load condition. This makes the regulation problem at low loads discussed in section 3.10.1 even worse.



(a) Junction capacitance of the diode

(b) Parasitic capacitances of the MOSFET.

Figure 3.13: Diode parasitic capacitance C_{jn}, and Si MOSFET parasitic capacitances, C_{gs}, C_{ds} and C_{gd}. $C_{oss} = C_{gd} + C_{ds}$. The Si MOSFET model is also valid for GaN HEMT.

This can be explained by including the parasitic capacitances in the FHA analysis as seen in as seen in fig. 3.14 [41].

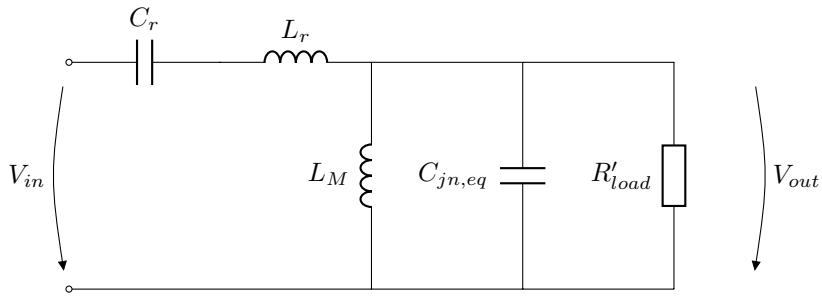


Figure 3.14: Equivalent circuit for the LLC converter from the fundamental harmonic approximation(FHA) analysis with the junction capacitances included.

The figure is equivalent to fig. 3.2, except for the addition of $C_{jn,eq}$. This capacitance comes from the junction capacitance of the diodes of the rectifier. Its value depends on the diodes chosen, the rectifier type and the turns ratio of the transformer. The new transfer function is then

$$\frac{V_{out}}{V_{in}} = \frac{sL_M||\frac{1}{sC_{jn,eq}}||R'}{\frac{1}{sC_r} + sL_r + sL_M||\frac{1}{sC_{jn,eq}}||R'}$$
$$= \frac{s^2 L_M R' C_r}{s^4 L_r L_M R C_{jn} C_r + s^3 L_r L_M C_r + s^2 R'(C_r(L_r + L_M) + C_{jn} L_M) + sL_M + R'} \quad (3.30)$$

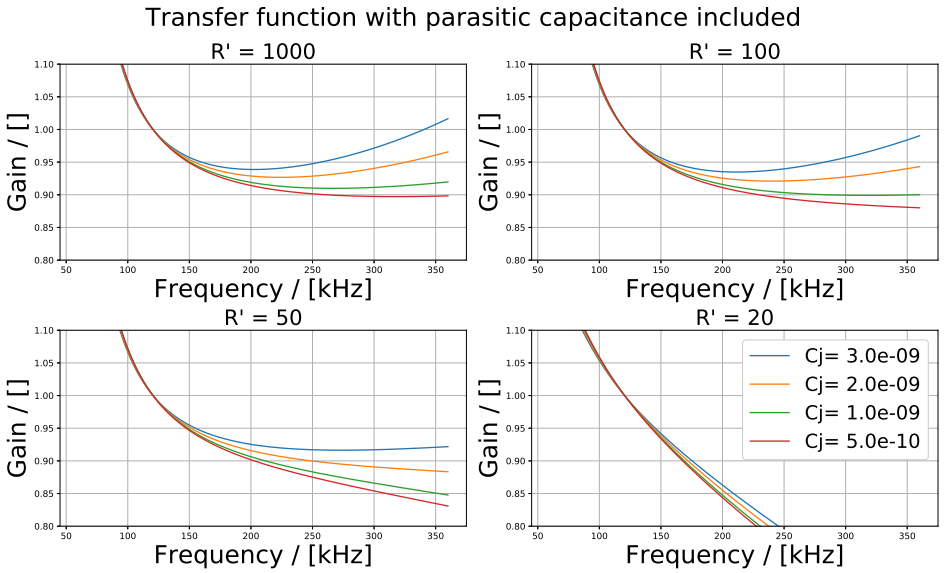


Figure 3.15: Gain of the transfer function $\frac{V_{out}}{V_{in}}$ with the effect of parasitic junction capacitance of the rectifier diodes included. The legend given is valid for all figures.

This new transfer function is plotted for several different loads and junction capacitances in fig. 3.15. The parameters are chosen same as for the converter used in laboratory measurement in chapter 5 and table 5.1. Notice the gain increases at higher frequencies. The gain increase is proportional to C_{jn}. Also, with increasing load[6] the effect is reduced. This means the problem of increased gain at high frequencies only persist at low loads.

Different remedies are proposed to solve light load problems in [41]

- Introducing a dummy load would be one possibility. The principle is shown in fig. 3.16. This essentially means removing low-load problems by removing the low-load situation altogether. However this would mean reducing the converter efficiency, since energy would be wasted in the dummy load.

[6]Decreasing resistance

Rectifier type	Center-tap	Full-bridge	Voltage doubler
Parasitic capacitance	$2 \cdot C_{jn}$	C_{jn}	$0.5 \cdot C_{jn}$

Table 3.1: Equivalent capacitance seen at the secondary side of the transformer caused by junction capacitances of the diodes for different rectifier solutions [41].

- Limiting the maximum switching frequency could be another possibility to limit the operation to the region where the parasitics play only a minor role. This must then be taken into account in the design procedure.
- Adding additional output capacitance in parallel with C_{oss} to reduce the problems at low load is also possible. Both [41] and [43] proposes increasing the capacitance C_{oss} to reduce this effect. Doing this, the input voltage at the resonant tank is no longer a step, but a ramp function, making the output current at low load smaller, reducing the gain. However, one still has to keep in mind that ZVS must be achieved, which would require a higher current or longer deadtime when the capacitance is bigger.
- Selection of rectifier type as discussed in section 3.9.4 is another possibility. The approach here is to reduce the value of the parasitic capacitance seen by the converter by choosing the rectifier smartly. The rectifier topology and the number of diodes will affect what parasitic capacitance that is present at the output. In table 3.1 three different rectifiers are compared in terms of parasitics.

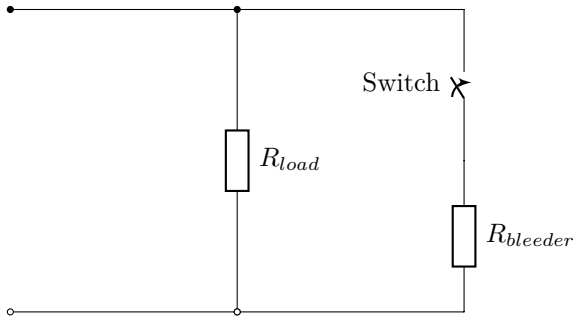
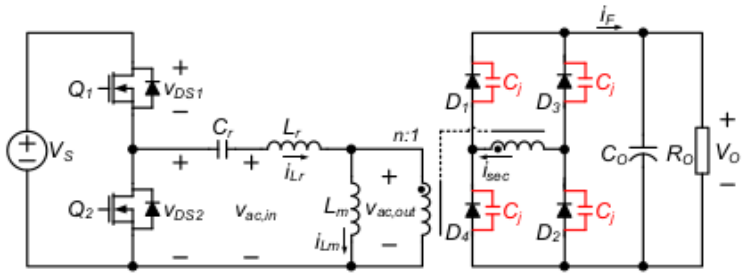


Figure 3.16: Dummy load as possible solution to low load problems. Sometimes also called a bleeder resistance. It is connected in parallel with the load resistance, and connected when needed by closing the switch.

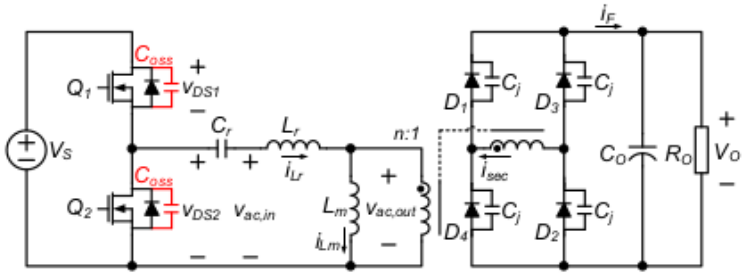
3.10.3 Time domain analysis of effect of C_{jn} and C_{oss}

Looking at [43] the low load regulation problems are analysed through time domain analysis. The equivalent circuits are shown in fig. 3.17, and the relevant waveforms

in fig. 3.18. Both the case where only C_{jn} and the case where both C_{jn} and C_{oss} are considered is shown.



(a) Equivalent circuit for the LLC converter with diode rectifier junction capacitance included

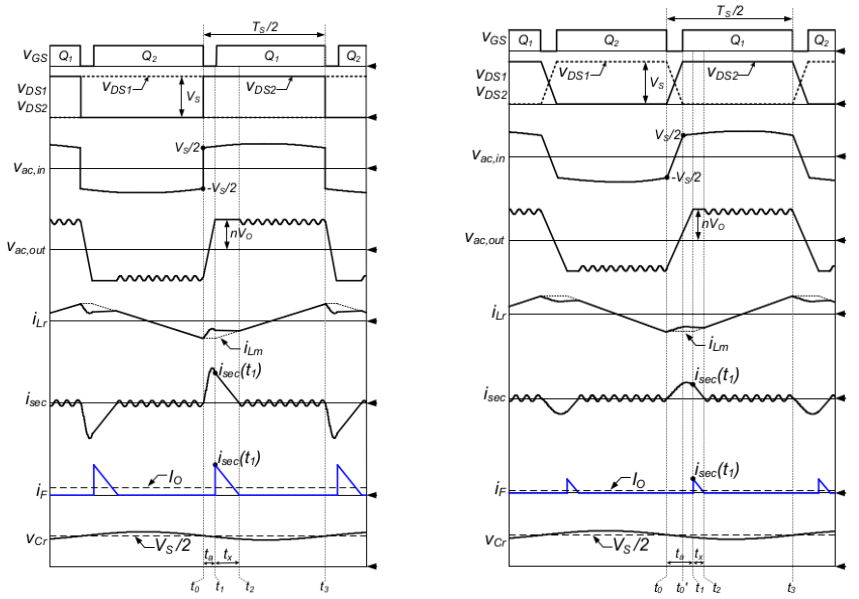


(b) Equivalent circuit for the LLC converter with diode rectifier junction capacitance and output capacitance of transistors included.

Figure 3.17: Equivalent circuits of the LLC converter with different parasitic effects included. Figures obtained from [43].

The relevant time periods are as follows [43]

- **Mode A, t_0 to t_1.** t_0 begins as the lower transistor, Q_2 turns off. The voltage at the input V_{ds2} quickly rises as the current is commutated from Q_2 to the body diode of Q_1. All the rectifier diodes are turned off, and the inductance L_r form a series LC-circuit together with the capacitances C_r and C_{jn}, with constant current source $i_{Lm}(t_0)$. Because of the voltage change at the input, the voltage across L_M quickly rises until $n \cdot V_0$ is reached, and the diodes start conducting. During the time from Q_2 is turned off until $V_{Lm} = n \cdot V_0$, there is a voltage drop over L_r and the current i_{Lr} rises. This leads to a rise in i_{sec}. During this period i_{sec} only flows through the junction capacitances, and i_F is zero.
- **Mode B, t_1 to t_2.** Mode B begins as the rectifier diodes start conducting. The diodes conduct, and power is transferred to the output. This means i_F is the same as i_{sec}. Since the voltage across L_r is negative, both i_F and i_{sec} decrease.



(a) C_{jn} included.

(b) C_{jn} and C_{oss} included.

Figure 3.18: Waveforms for the LLC converter for two different cases. One where only the parasitic effect of the output diodes junction capacitance effect C_{jn} is included. And one where both C_{jn} and parasitic capacitances of the transistors, C_{oss} is included. Obtained from [43].

- **Mode C, t_2 to t_3.** Mode C begins as the current i_{sec} becomes zero, and the diodes stops conducting. In this mode, C_r, L_r, L_M and C_{jn} resonate. No current flows to the output.

The important difference between the two cases in fig. 3.18 is the difference in $V_{ac,in}$. With C_{oss} included it is a ramp, instead of a step function. This causes the voltage $V_{ac,out}$ to take longer time to rise. Since the charge needed to fill the junction capacitances and make the diodes forward biased is the same in both cases, the current i_{Lr} and therefore also i_{sec} is smaller in the ramp case. This again causes the current to the output to decrease during mode A, meaning the gain is reduced. Consequently, the effect of C_{oss} reduces the parasitic effect of C_{jn}.

3.10.4 Long deadtime

As shown in section 3.5 there is a tradeoff between the output capacitance of the transistor and the deadtime in the following way

$$t_{dead} = \frac{Q_{oss}}{I_{ZVS}} \tag{3.31}$$

since

$$Q_{oss} = \int_0^{V_{ds}} C_{oss} dv_{ds} \tag{3.32}$$

meaning that increasing the capacitance C_{oss} would make the deadtime longer. Notice that the stored charge is dependent upon the input voltage, but does not depend on load. The current however, varies with the applied load. It could be interesting then to see at what loads and frequencies the current is the lowest. Looking at the derived transfer function in section 3.2, the no load condition, $R = \infty$ gives

$$\left.\frac{I_{in}}{V_{in}}\right|_{R\to\infty} = \frac{sC_r}{s^2(L_M + L_r)C_r + 1} \tag{3.33}$$

and short circuiting, $R = 0$ gives

$$\left.\frac{I_{in}}{V_{in}}\right|_{R\to 0} = \frac{sC_r}{s^2 L_r C_r + 1} \tag{3.34}$$

The no-load and short-circuit cases are plotted and compared in fig. 3.19. It is then seen that the current is the smallest for no load at high frequencies. In chapter 4 it is seen that the transfer function approximation is good for no load in a wide frequency range, and can therefore be used here.

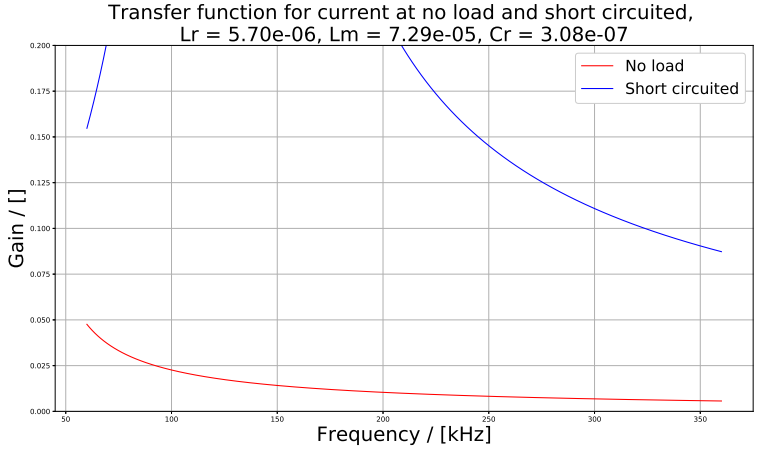


Figure 3.19: Current into the resonant tank at no load and short circuit condition for different frequencies. Calculated from the transfer function $\frac{I_{in}}{V_{in}}$.

Since one of the proposed solutions for solving the problem of parasitic influence at low load is increasing C_{oss}, this would come at a cost of increased deadtime. However when the deadtime increased, it takes up an increasing amount of the total switching period, as discussed in section 3.5. The effective duty cycle is as before

$$\tilde{D} = 0.5 - \frac{2t_{dead}}{T} \tag{3.35}$$

Where t_{dead} is the deadtime, and T the switching period proportional to the frequency, f, $T = \frac{1}{f}$. As discussed in section 3.5, if $\tilde{D}$ gets to small, i.e. deadtime is too large, problems achieving ZVS can occur. When the load is low, the frequency must be increased to keep the voltage at the same value. Since the current is also the smallest at low loads and high frequencies, the problem amplifies. This implies that another form of low load problems can arise, because of the inevitable long deadtimes at no loads. If the needed deadtime at the wanted operating frequency is too big, ZVS will be lost. This will lead to increased losses, and might also cause regulation problems.

Chapter 4

Simulation

In this section, simulations are done to validate some of the concepts discussed in chapter 3. Particularly the validity of the transfer function from FHA-analysis is done.

Chosen parameters for the simulation are shown in table 4.1. The output capacitance is chosen big enough so that the ripple can be disregarded, but still small enough to have the simulation reach steady state in a reasonable amount of time. The load, and therefore the Q-values, are chosen similarly to in [33]. Input voltage, inductances and series capacitance are chosen similarly to the modules used in chapter 5 Also the variables introduced in section 3.3 are included.

Parameter	Value	Unit
V_{input}	400	V
L_M	72.9	µH
L_σ	5.7	µH
C	286	nF
R_{load}	[8-80]	Ω
C_{out}	34	µF
a	1	-
R'	[3.25-32.5]	Ω
m	13.8	-
Q	[1.34 - 0.13]	-
f_{R1}	124.7	kHz
f_{R2}	33.6	kHz

Table 4.1: Component parameters chosen for simulation of transfer function. Upper part gives chosen parameters. Lower part is the variables introduced in section 3.3.

The simulation is done through LTspice [1]. Two models are compared, one

[1] Free simulation software, available on https://www.analog.com/en/design-center/design-tools-and-calculators/ltspice-simulator.html

that represents the simplified circuit shown in fig. 5.2 and one that represents the converter with the diode bridge and output capacitance. A figure of the LTspice model is included in the appendix in fig. A.1. To avoid problems with singular matrices in the solver during simulation, all the reactive elements have an equivalent series resistance(ESR), $R_{ESR} = 10\,\mathrm{m\Omega}$. This is not explicitly shown in the model, but present in the component models for the inductances and capacitances. Since these resistances are significantly lower than the load this should affect the accurace of the simulation results.

4.1 Comparison of gain characteristics

In [33], simulations of the actual LLC converter is compared to the transfer function from FHA analysis. Good results are found around the resonance frequency, but it is seen that the results worsen when moving below or above resonance frequency. This corresponds with the assumptions made in section 3.2 when deriving the transfer function. Because the filtering behaviour of the resonant tank can only be justified close to the resonant frequency.

A similar simulation is done here, to validate the results and the derived transfer function.

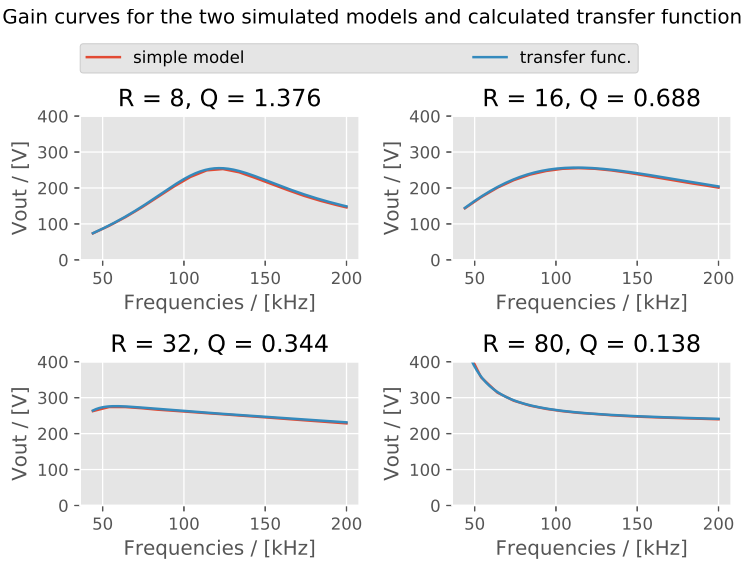


Figure 4.1: Comparison of gain curves for the simulated simple model, complete model and theoretical transfer function from the fundamental harmonic approximation with **sinusoidal** input voltage. Resistances are given in Ω

In fig. 4.1 the gain curves for the transfer function from FHA analysis and the simple simulation model are shown. Here the input voltage is sinusoidal, with an amplitude equal to the fundamental component of the square wave voltage

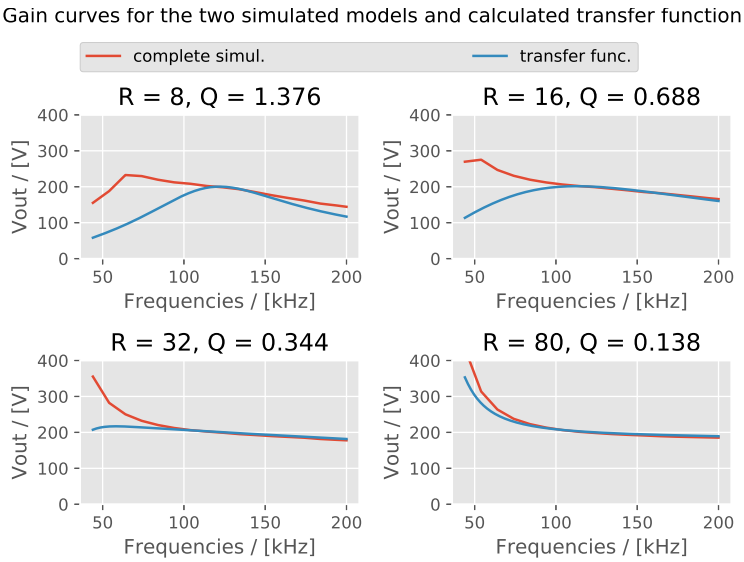


Figure 4.2: Comparison of gain curves for the complete model and theoretical transfer function from the fundamental harmonic approximation with **square wave** input voltage. Resistances are given in Ω

$$V_{in,amplitude} = V_{fundamental,amplitude} = \frac{2V_{dc}}{\pi} \tag{4.1}$$

Almost perfect correspondance between the two gain curves are shown, which validates the analytical expression for the transfer function in eq. (3.11).

Still, the validity of this function compared to the complete model with square wave voltage input must be checked. The results of the simulation is shown in fig. 4.2. Here the transfer function gain is calculated with V_{in} in eq. (3.11) equal to

$$V_{in,tf} = \frac{V_{squarewave}}{2} \tag{4.2}$$

where $V_{squarewave}$ is the amplitude of the input squarewave. It is seen that the transfer function and simulated gain are similar around resonance frequency. For frequencies above resonance, the correspondence is good for high resistances, but worse for low resistances.

The percentage error of the different curves, is given in fig. 4.3. For frequencies significantly below resonance, the result is unacceptable even for low loads. In table 4.2 a summary of the valid frequency ranges as functions of the normalized frequency, F, and the quality factor, Q, are seen, for a arbitrarily 25% error limit.

The results obtained here are similar to what is reported in [33]. The derived transfer function from FHA analysis is quite good at low loads around and above resonance frequency. For high loads it is good only around resonance frequency.

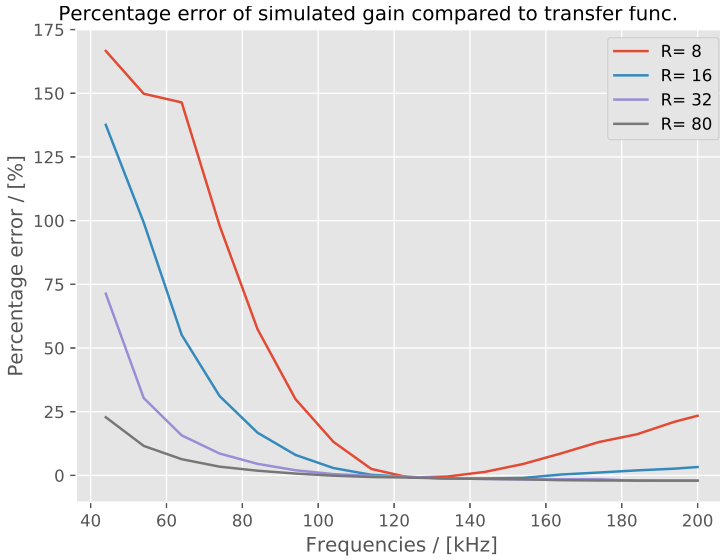


Figure 4.3: Deviation of simulated gains for the complete model compared to calculated transfer function with **square wave** input voltage. Resistances are given in Ω.

R/[Ω]	f_{R1}/[kHz]	$f_{25\%,below}$/[kHz]	$f_{25\%,above}$/[kHz]	F_{range}/[-]	Q/[-]
8	124.5	95	200	[0.76- 1.6]	0.56
16	124.5	75	above 200	[0.60-]	0.28
32	124.5	55	above 200	[0.44-]	0.14
80	124.5	45	above 200	[0.36-]	0.06

Table 4.2: Validity range of the transfer function if 25% is the accepted error margin.

This means, although some criticism to the FHA approach is raised in [48][49] and [31], the FHA seems good as long as the limitations are kept in mind. If for some reason the FHA analysis is not sufficient, [48][49] and [31], also provide some alternative approaches valid for wider frequency ranges.

Chapter 5

Lab measurements

In this section lab measurements comparing gallium-nitride(GaN) HEMT and silicon(Si) transistors in the LLC converter are performed. Two 3 kW modules, shown side by side in fig. 5.1 are used, one for silicon and one for GaN HEMT. The scope of this report is mainly to report low-load problems in the LLC converter and possible improvements with GaN HEMTs. For this reason, in the measurements particular focus is put on low-load problems. To show that this can be achieved without any degradation of performance, attention is also paid to efficiency.

5.1 About the modules and lab setup

The modules are originally AC-DC converters, with a PFC stage for AC-DC conversion followed by a DC-link and a DC-DC LLC converter. The modules used however are modded so as to skip the PFC stage, and control the DC-link voltage directly. A picture of the modded modules is shown in fig. 5.1.

A simplified circuit of the LLC modules is shown in fig. 5.2. The chosen circuit

Parameter	Value
L_r	5.7 µH
L_m	72.9 µH
C_r	308 nF
C_{out}	3400 µF
a	$\frac{20}{6}$
f_{R1}	120.0 kHz
f_{R2}	32.3 kHz
m	13.8
Q	Dependent on load

Table 5.1: Component values used in the LLC converter during lab measurements. Resonant frequencies,m and Q are calculated as explained in section 3.3

Figure 5.1: The two modules used, shown side by side from the bottom side. The resonant inductor L_r is what sticks out. It is desoldered to be able to attach a current probe. The rest of the resonant tank and the transistors is inside the module.

parameters are given in table 5.1. The modules have the following characteristics:

- Nominal output voltage is 53.7 V [1]. The DSP implemented control system tries to regulate it to this value unless another voltage reference is set. The voltage is regulated by changing the the switching frequency, changing the gain as shown in section 3.2. This is all done automatically by the DSP.

- Nominal DC-link voltage at the input is 358 V. This is given from the nominal output voltage and turns ratio of the transformer. Nominal operating frequency should be at the resonance frequency, where the gain is always 1. Since the transformer will see half the input voltage, $V_{in,nom} = 2a \cdot V_{out} = 358\,\text{V}$, with turns ratio $a = \frac{20}{6}$ and nominal output voltage $V_{out} = 53.7\,\text{V}$.

- As seen in table 5.1, the resonance frequency is 120 kHz. It also has an upper frequency limit set by the DSP at 295 kHz. This limit is imposed by different requirements such as switching losses and frequency resolution of the operating range, since it must be represented digitally in the DSP.

- The output rectifier is a full-bridge diode rectifier as discussed in section 3.9.4. No synchronous rectification is used. This leads to quite high losses in the diodes, and is also the reason for only running the module up to 45% of rated load for the efficiency tests. The rectifier diodes used are given in [50].

[1] Corresponds to four 12 V batteries, since their operating voltage is slightly above 12 V

- The magnetizing inductance L_M and series inductance L_r are discrete components. I.e. they are not included through design of the transformer, but are discrete components. The transformers parasitic inductances L_σ and L_{mag} are small and big respectively, meaning they do not impact circuit operation significantly.
- As seen in fig. 5.2 the split capacitor topology explained in section 3.9 is used.
- The converter has a fan for cooling. To be able to compare the efficiency results, the fan should consume the same amount of power across all tests. In the following the fan speed is regulated to 50% of top speed. The fan is then measured to consume about 3.6 W.

To get precise efficiency measurements, a Yokogawa WT3000 Precision Power Analyzer is used. The power analyzer needs measurements of both the current and voltage at input and output to measure the efficiency. Because of the current limit of the power analyzer, the output current is split into two branches. The input voltage is controlled by a DC-source, and the load by a controllable load. A circuit of the setup is shown in fig. 5.3.

Both the power analyzer and the load is connected to a computer for easy logging of measurements and for control of the load. The DC-source is controlled manually. To analyze the low load problems, detailed waveforms from an oscilloscope is also needed. The oscilloscope is used for measuring voltages and currents in the circuit. Specifically the gate-source and drain-source voltages at the lower transistor, and the current into the resonant tank are measured with the oscilloscope. The measured values are shown and explained in fig. 5.6.

The complete list of measurement equipment used and their purpose is given in table 5.2.

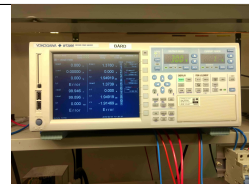
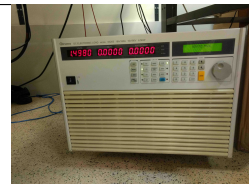
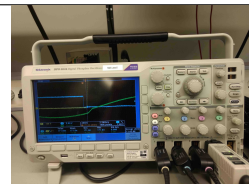
Name	Purpose	Picture
Yokogawa WT3000 Precision power analyzer	Precise efficiency measurements	
Chroma DC Electronic Load Model 63205	Controllable load at output	
Sorensen XFR 600-4	DC-source at input	
Tektronix DPO 3034 Digital Phosphor Oscilloscope (300Mhz, 2.5GS/s)	Measuring waveforms	
Tektronix TCP0030A and Tektronix P6139B	Current probe and voltage probe	
Flir ONE thermocamera	Thermal measurements	
AP Instruments Inc. 15MHz Analog Network Analyzer Model 200	Transfer function measurements	

Table 5.2: Equipment used in lab measurements.

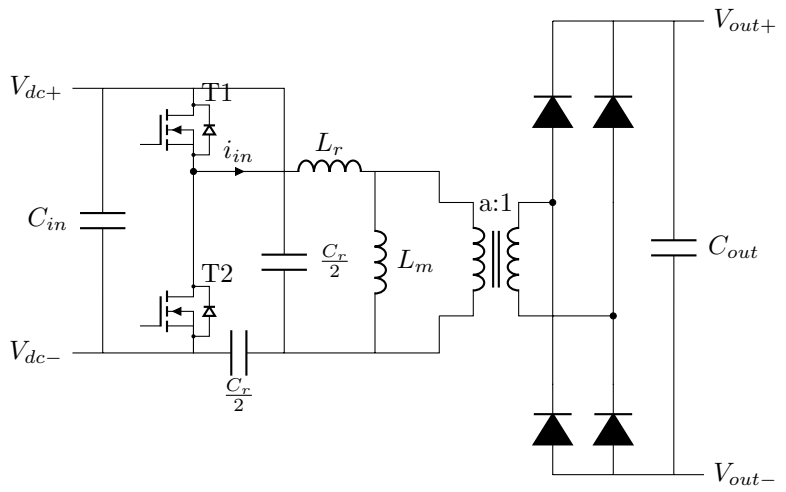
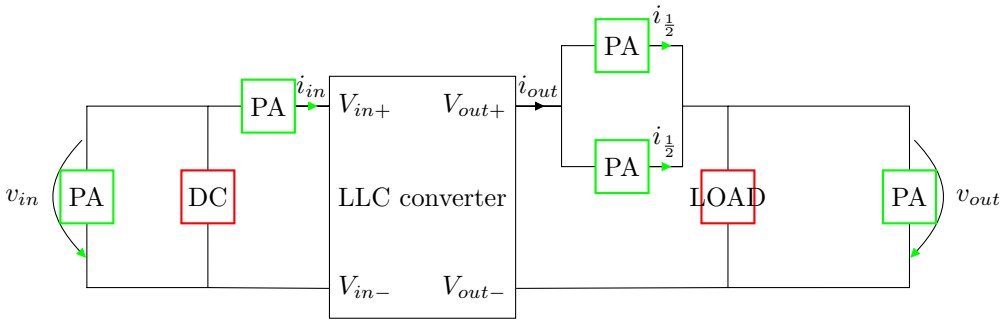
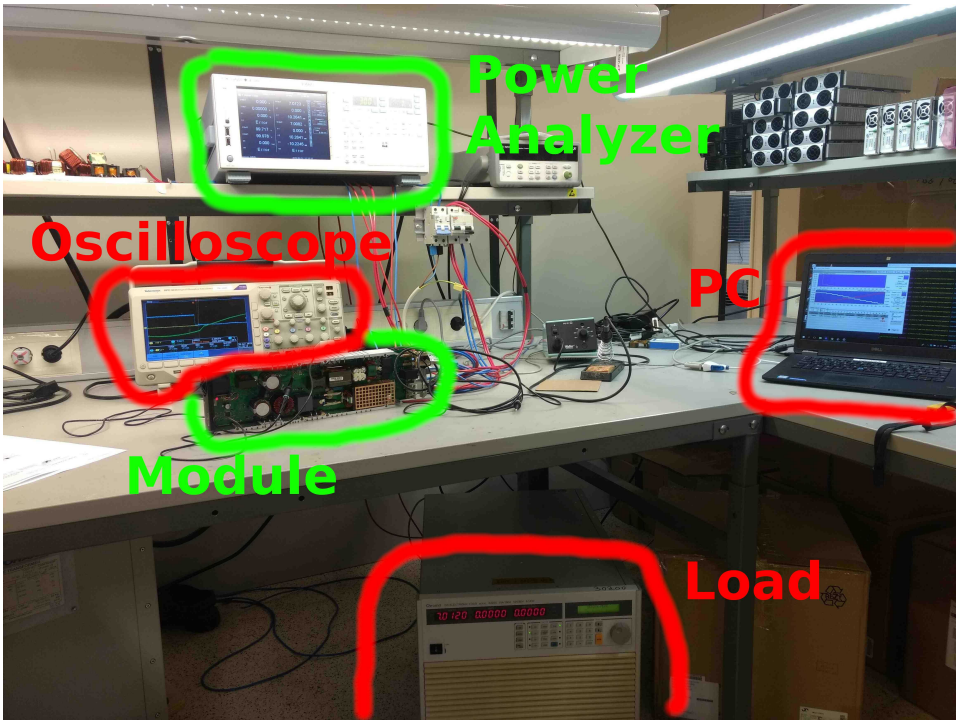


Figure 5.2: Simplified schematic of the LLC converter used. Snubber and junction capacitances are not shown. Also auxillary circuits such as gate drivers, fan etc. are not shown.



(a) Diagram of lab setup. PA means the power analyzer, and it measured both the input and output voltage, as well as the input and output current. DC is the DC source, while LOAD is the controllable load.



(b) Picture of lab setup. The DC-source is not shown in the picture.

Figure 5.3: Schematic and picture of the lab setup.

5.2 Preliminary test

For laboratory measurements, two modules will be tested. One will be modified with Si MOSFETs, and the other with GaN HEMTS. Before any testing is done on the modules, an efficiency test is done to make sure that the two are comparable. This test also serves as a reference to compare the other measurements against. The result is shown in fig. 5.4. Except for at 5% load, it is seen that the two curves almost perfectly overlap, and therefore the modules are assumed to be equal. The discrepancy low load is thought to be caused by tolerances of the setup playing a relatively larger part here. Comparing the modules like this makes sure any differences observed later are from the changes made.

With no synchronous rectification, the diode losses at the secondary side are quite significant. Because of this, the module is only ran up to 45% of rated load, as to not overload the diodes. This is enough to include the efficiency peak of the module, which arguably is the most interesting part. The modules are delivered with Vishay transistors [51], and the efficiency is already quite good, with a peak at 96%.

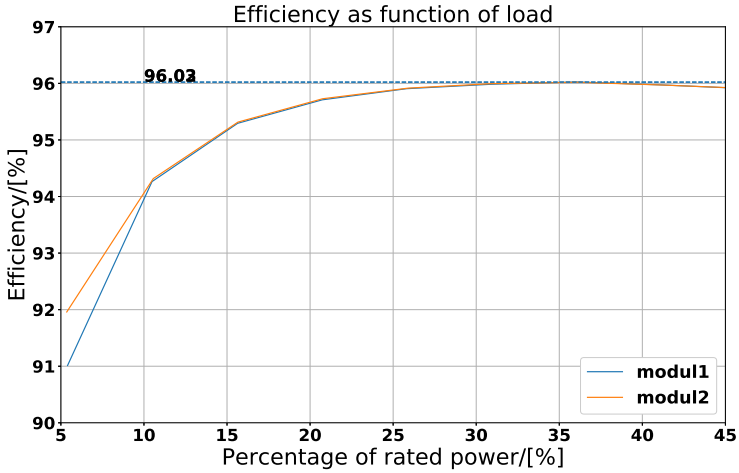


Figure 5.4: The two modules used for lab measurements compared by an efficiency test to make sure they are comparable before further testing.

5.3 Changing $R_{ds,on}$

Last section concluded that the two modules are comparable. Now one is modded with Si MOSFET transistors and the other with GaN HEMTs from Infineon. Both transistor types are tested for two different $R_{ds,on}$ values. The lab tests made are summarized in table 5.3.

Module used	Transistor type	Transistor datasheet
Module 1	Si MOSFET 70 mΩ	[18]
	Si MOSFET 31 mΩ	[52]
Module 2	GaN HEMT 70 mΩ	[19]
	GaN HEMT 31 mΩ	-

Table 5.3: Summary of lab tests done with different $R_{ds,on}$. Two modules are tested, one with GaN HEMT and the other with MOSFETs. Both transistor types are tested for both 70 mΩ and 31 mΩ. For the GaN HEMT 31 mΩ unfortunately no datasheet exist, as it is only an engineering sample, and not yet commercially available.

The resulting efficiency curves are shown in fig. 5.5. The peak efficiencies are given in table 5.4. Notice that the 70 mΩ devices do worse than the 31 mΩ, and GaN HEMTs do worse than Si MOSFETs. However the module is optimized for Si MOSFETs, and none of GaN HEMTs advantages have been leveraged so far. The total difference from the worst to the best case is about 0.25%, which for a 3 kW converter at 30% load corresponds to corresponds to 2.3 W. The change from 70 mΩ to 31 mΩ is about 0.20%, meaning 1.8 W.

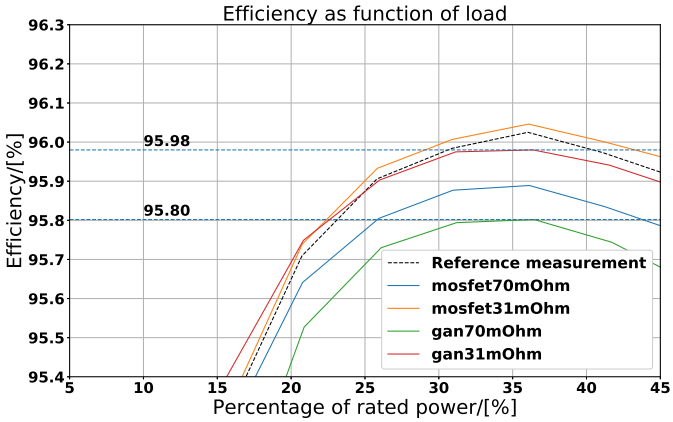


Figure 5.5: Measured peak efficiency for Si MOSFET and GaN HEMT with two different on-state resistances.

$R_{ds,on}$	Si MOSFET	GaN HEMT
70 mΩ	95.89%	95.80%
31 mΩ	96.05%	95.98%

Table 5.4: Measured peak efficiencies with two different on-state resistances for both Si MOSFET and GaN HEMT.

5.4 Deadtime

Deadtime, discussed in section 3.5, is a delay between the switching of the two transistors in the half-bridge in the LLC converter. As explained in section 2.2 and section 2.5, GaN HEMT has a smaller semiconductor die for the same onstate-resistance. This means that GaN HEMT has a smaller output capacitance than its silicon counterpart. For a soft switching converter, this is especially important, because the deadtime needed is directly dependent on the stored output charge.

As in section 3.5, a distinction is made between the **delay time** and **deadtime**. In this section the delay time is measured. The chosen deadtime in the DSP is discussed in regard to this.

5.4.1 Delay time at low loads

The deadtime needed at low loads is considered first. As the deadtime is current dependent in the following way

$$t_{dead} \geq \frac{Q_{oss}}{I_{ZVS}} \tag{5.1}$$

where Q_{oss} is the stored charge and I_{ZVS} is the current into the resonant tank at the time of a switching transition. The current is small at low loads, therefore the deadtime increases at decreasing loads. Since the stored charge is bigger for a Si MOSFET than a GaN HEMT, it is expected that the needed deadtime is larger. Waveforms at no load are presented in fig. 5.7. The colors and curves are explained in fig. 5.6 and are as follows

- Cyan is gate-source voltage at the lower transistor, T_2 in fig. 5.6.
- Blue is the midpoint voltage in the half-bridge, the same as the drain-source voltage of T_2 in fig. 5.6.
- Green is the current into the resonant tank, i_{in} in fig. 5.6

Although it would be illustrative to measure the gate-source voltage of the upper transistor, this is at a high potential with reference to the oscilloscope ground, and therefore not measured here.

The delay time measured is from the fall of the gate-source voltage(Cyan), until the drain-source voltage(Blue) starts rising. The oscilloscope calculates the delay time from the midpoint of the gate-source voltage to the midpoint of the drain-source voltage.

Note that the timescale is unfortunately not the same in all figures. The deadtimes are measured by the oscilloscope, and goes from the midpoint of the gate-source voltage to the midpoint of the drain-source voltage. The most interesting part is the moment when drain-source voltage reaches its peaks, i.e blocks the whole DC- voltage, because the other transistor can then be turned on. The results are also summarized in table 5.5. It is seen that the Si MOSFET has significantly higher delay time than its GaN HEMT counterpart. This is as expected because of the higher output capacitance for the Si MOSFET. See also that Si MOSFET 70 mΩ has a smaller inherent deadtime than Si MOSFET 31 mΩ, which makes sense since it has smaller die size.

For GaN HEMT the currents are not equal for 70 mΩ and 31 mΩ, and the measured delay times are therefore similar. For these small time scales, the measurement error of the oscilloscope also plays a bigger role. It is expected that with the same current value, GaN HEMT 70 mΩ should have smaller delay times than GaN HEMT 31 mΩ.

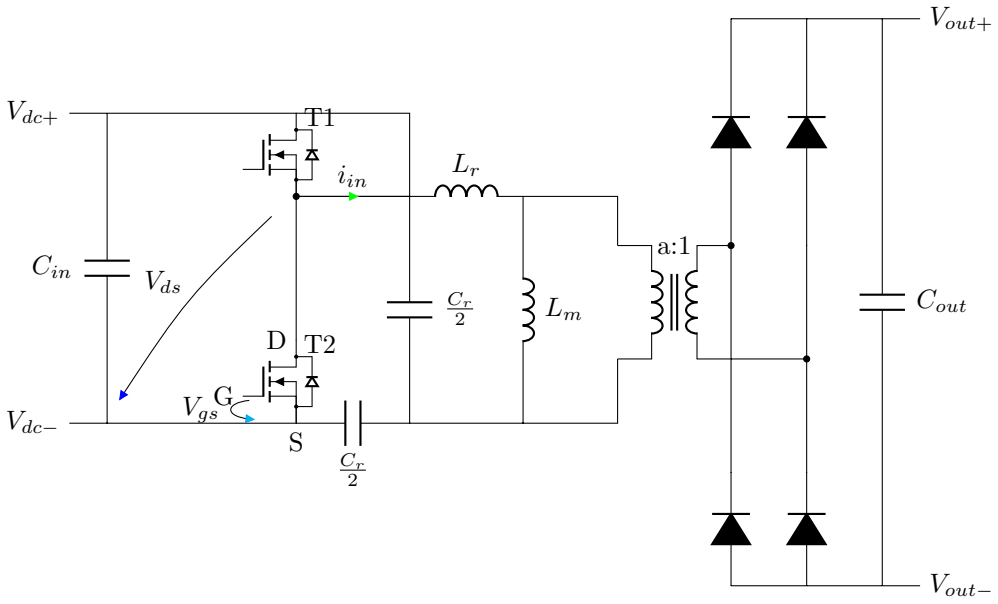
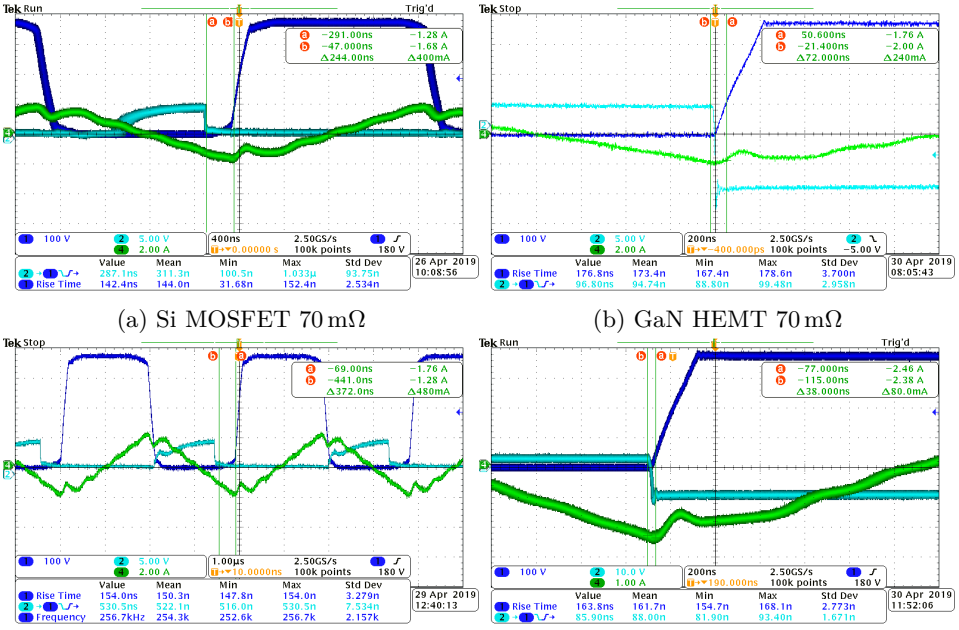


Figure 5.6: Explanation schematic with colors of the labeling of the oscilloscope curves from measurements.

For this converter, the chosen deadtime is hardcoded into the DSP, and is a function of the frequency only. Low loads leads to a large delay time, meaning the deadtime in the DSP must be correspondingly large. If the available deadtime is not long enough, loss of ZVS might occur, as discussed in section 3.10.4. This can give problems regulating the voltage.

Looking at the deadtimes in table 5.5, the Si MOSFET 31 mΩ has the longest delay time by a large margin. From analysis in section 3.10.4 it is known that



(a) Si MOSFET 70 mΩ

(b) GaN HEMT 70 mΩ

(c) Si MOSFET 31 mΩ

(d) GaN HEMT 31 mΩ

Figure 5.7: Delay time at no load for Si MOSFET and GaN HEMT at both 70 mΩ and 31 mΩ.

$R_{ds,on}$	Si MOSFET	GaN HEMT
70 mΩ	142.4ns	96.8ns
31 mΩ	530.5ns	85.9ns

Table 5.5: Measured delay times at no load with two different on-state resistances for both Si MOSFET and GaN HEMT.

Si MOSFET 31 mΩ	GaN HEMT 31 mΩ
876.5 ns	134.7 ns

Table 5.6: Measured delay times for the Si MOSFET 31 mΩ and GaN HEMT 31 mΩ when setting the output voltage reference to 48 V.

excessive deadtimes can cause problems. This indicates that low load problems could be present for the low-ohmic Si MOSFET. The GaN HEMT 31 mΩ does not have this long delay time problem, with a measured delay time of only 85.9 ns.

Setting the output voltage reference to 48 V exaggerates the problem even further, as seen in fig. 5.8. This is because the current decreases, and the delay times grow even larger. The measured delay times for the both 31 mΩ transistors when regulated to 48 V is given in table 5.6.

For the Si MOSFET 31 mΩ, the inherent deadtime is now as large as 877 ns, and the converter operates at max frequency. Unfortunately the output voltage was not measured. However, looking at the operating frequency, it is seen that the converter operates at the minimum gain available to it, i.e. at the maximum frequency limit. This is clear indication of low load voltage regulation problems. The effective duty cycle to achieve ZVS is

$$\tilde{D} = 0.5 - 2 \cdot 877\,\text{ns} \cdot 295.4\,\text{kHz} \approx -0.02$$

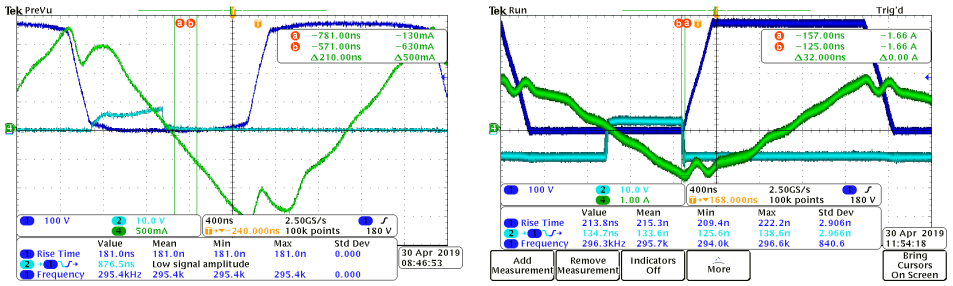
meaning achieving ZVS is not possible here, and the converter is forced to hard-switch. This makes sense when considering the transfer functions in fig. 3.15, the control system tries to regulate down the voltage by moving up in frequency, but reaches the upper frequency limit before the voltage reference is reached. Increasing the frequency also decreases the current into the resonant tank, and the delay time increases. Because of the large output capacitance of the Si MOSFET 31 mΩ the delay time become excessive. Consequently, ZVS is lost, and problems with regulating the voltage occur. These low load problems can not be caused by the parasitic effects of the output diodes junction capacitance, because the large C_{oss} counteracts this problem.

One possible remedy to this problem would be increasing the circulating current by decreasing L_M. However, this would come at the cost of increased conduction losses.

Although the GaN HEMT 31 mΩ also operates at maximum frequency, meaning it has problems regulating the voltage, this is not caused by excessive delay times, but parasitic effects of the output diodes. This problem will be discussed and solved in section 5.5.4.

5.4.2 Delay time as a function of current

The delay time is dependent on the stored charge of the transistor, as well as the current into the resonant tank. In this section the delay time as a function of the current for different transistors is measured. The module is ran at several different



(a) Si MOSFET 31 mΩ (b) GaN HEMT 31 mΩ

Figure 5.8: Delay time for both Si MOSFET and GaN HEMT 31 mΩ when trying to regulate the output voltage to 48V.

loads, while measuring the resonant tank current and delay time. The results are shown in fig. 5.9.

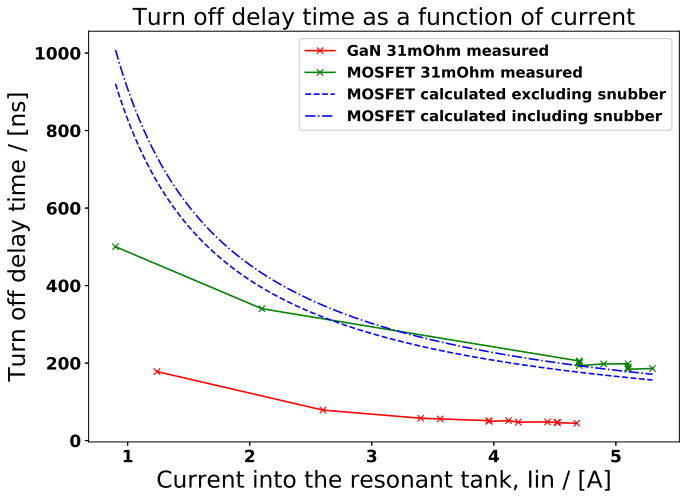


Figure 5.9: Theoretical and measured delay times as a function of current into the resonant tank.

Because of limited time this is only measured for Si MOSFET 31 mΩ and GaN HEMT 31 mΩ. It is also because these two devices are the most interesting for further study, since they have the lowest $R_{ds,on}$.

Although the current varies during the delay time, in the figure it is plotted with the value that the current had at the drop of the gate-source voltage. The assumption of constant current during the delay time is quite good for the GaN HEMT but worse for the Si MOSFET. The theoretically calculated curve, also

shown in fig. 5.9, was calculated from integrating the C_{oss}-curves [2] in the datasheet according to eq. (2.3). Taking into account the DC-link voltage of 358 V and adding on the snubber capacitance, discussed in section 3.8, this gives

$$Q_{oss} = \int_0^{V_{ds,max}} (C_{oss}(v_{ds}) + C_{snub}) dv_{ds} = 78.8\,\text{nC} + \int_0^{358\,\text{V}} C_{oss}(v_{ds}) dv_{ds} \quad (5.2)$$

Where C_{snub} in this case is 220 pF, and gives a total contribution of 78.8 nC when the operating voltage is 358 V. Compared to the C_{oss}, the snubber capacitance is small, and therefore stores relatively little charge. It therefore makes little difference on the delay time. A good fit is found between theory and lab measurements in this case. No theoretic delay time for GaN HEMT is included, because no datasheet exist. This is because it is only an engineering sample. Unfortunately few datapoints were gathered at low current, and the discrepancy between practice and theory is the biggest here. The trend is that the delay times are proportional to $\frac{1}{I_{in}}$. Also the GaN HEMT has significantly lower delay times than Si MOSFET.

5.4.3 Improving efficiency by taking advantage of GaN HEMTs shorter delay time

It was observed that GaN HEMTs delay time is shorter than for Si MOSFETs. Since the original module is made for a Si MOSFET, the deadtime control from the DSP does not take this into account. This opens up for a possibility of improvement when using the GaN HEMTs.

In between the turn-off of one transistor until the turn-on of the other transistor, the anti-parallel diode has to conduct the current. For the Si MOSFET, this is often the body diode inherent in the Si MOSFET-structure. Although GaN HEMT has no body diode per se, it has reverse conduction capabilities. However, looking at the data sheet, these lead to quite big losses. This is shown in fig. 5.10 taken from GaN HEMT 70 mΩ data sheet. Similar behaviour is expected for the GaN HEMT 31 mΩ. The voltage drop is quite high for the reverse conduction current, leading to large losses. The GaN gate driver used here has a negatively biased gate-source voltage at −7 V. Looking at the figure, this means a drain-source voltage drop of several volts, which would lead to substantial losses.

A discrete diode [53] is therefore put in antiparallel to the GaN HEMT, shown also in fig. 5.2. This is true for all tests done with GaN HEMT in this report. It is a SiC Schottky diode and therefore also has negligible reverse recovery losses. However, the diode has a constant forward voltage drop. When the diode conducts, the losses are larger than for when the transistor is turned on. Since the diodes conduct during the deadtime, it should be as small as possible to decrease conduction losses.

The deadtimes are controlled by the DSP, and are a function of the operating frequency of the converter only. Therefore by adjusting the deadtime curves

[2] Often called 'Typical capacitances' or equivalent in the datasheet, showing C_{iss}, C_{rss} and C_{oss} as a function of V_{ds}

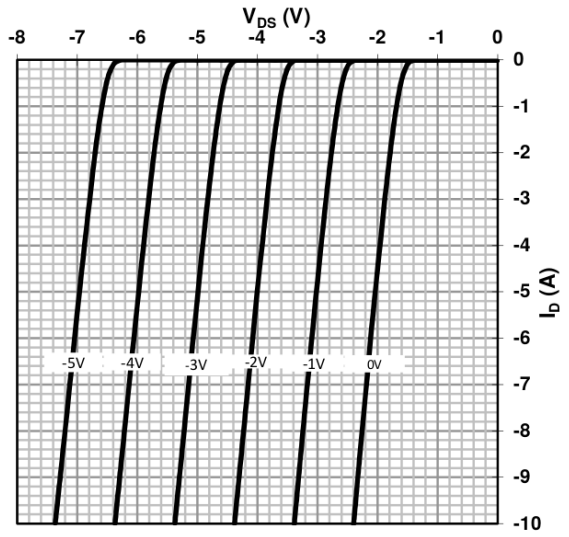


Figure 5.10: Typical channel reverse characteristics of GaN HEMT 70 mΩ taken from the respective datasheet [19]. The voltage given on the curves is the gate-source voltage bias.

	No load	35 % load
Original deadtime curve	242.1 ns	210.5 ns
New deadtime curve	281.6 ns	101.5 ns

Table 5.7: Measured turn-on delay times with old and new deadtime curves used in the DSP.

used by the DSP for control, efficiency might be increased. In figure fig. 5.11 the original curve and a new one is shown. The new curve has shorter deadtimes for the frequencies around resonant frequency, $f_{R2} = 120\,\text{kHz}$. This is the relevant operating range for the peak efficiency.

New oscilloscope pictures of the lower transistor turn-on curves are taken and are shown in fig. 5.12. The results are also summarized in fig. 5.12. Four cases are shown in the figure, the original and new deadtime curve for both efficiency peak load(35% of rated load in this case)[3] and no load. Notice the shorter deadtime, and therefore shorter conduction period of the diode, for the new deadtime curve. It is seen that the converter operates fine, even with shorter deadtimes. The observed deadtimes deviates slightly from the values given in fig. 5.11. This is thought to be because of delays in the gate driver system.

To see if there has been any improvement, the efficiency is tested again. The efficiency with the original deadtime curve is compared to the new to the new one.

[3]Somewhere between 30% and 35%. Waveforms measured are at 35%, but the peak varies between the two depending on modding.

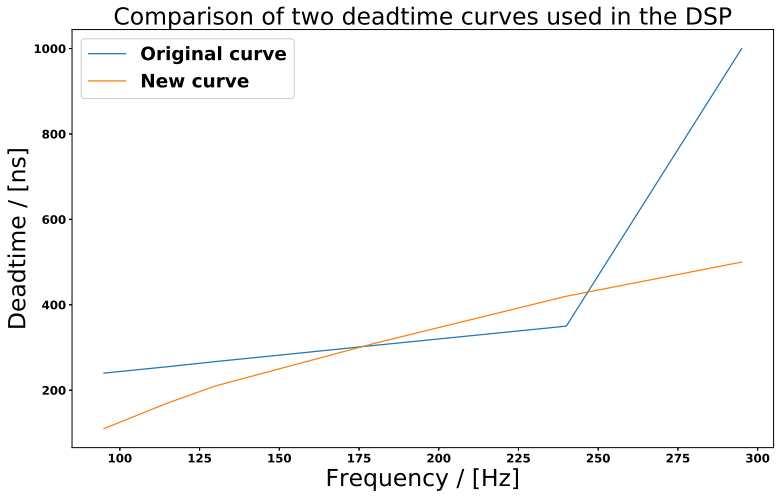
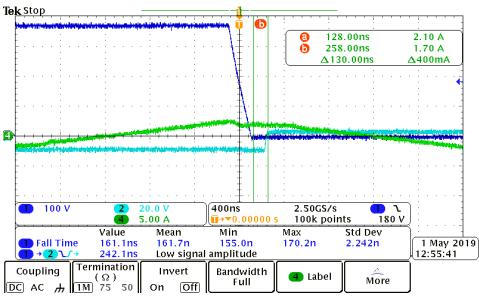


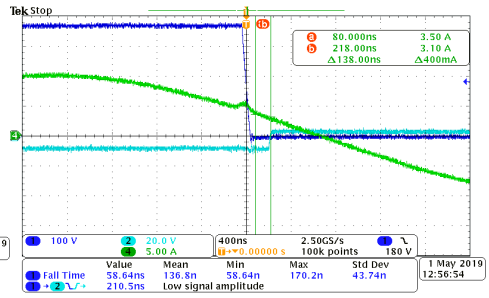
Figure 5.11: New and old deadtime curves used for controlling the switching in the DSP.

The results are shown in fig. 5.13.

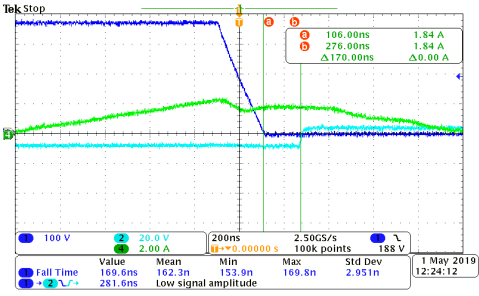
A slightly above 0.1% efficiency increase is observed at the peak. For a 3 kW converter at 30% load this corresponds to 1 W. In addition to the efficiency test, photos of the module, and in particular the anti-parallel diode, with a thermal camera is taken. The results are shown in fig. 5.14. Notice that the diodes are 1 °C hotter for the original deadtime curve.



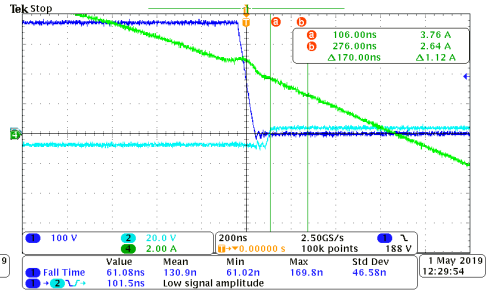
(a) GaN HEMT 31 mΩ at no load, original deadtime curve



(b) GaN HEMT 31 mΩ at 35% load, original deadtime curve



(c) GaN HEMT 31 mΩ at no load, new deadtime curve



(d) GaN HEMT 31 mΩ at 35% load, new deadtime curve

Figure 5.12: Turn on delay time for both new and old deadtime curve at no load and peak efficiency load with the GaN HEMT 31 mΩ.

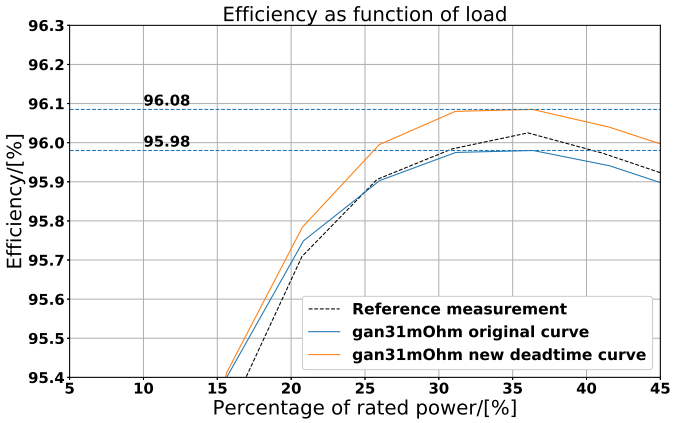
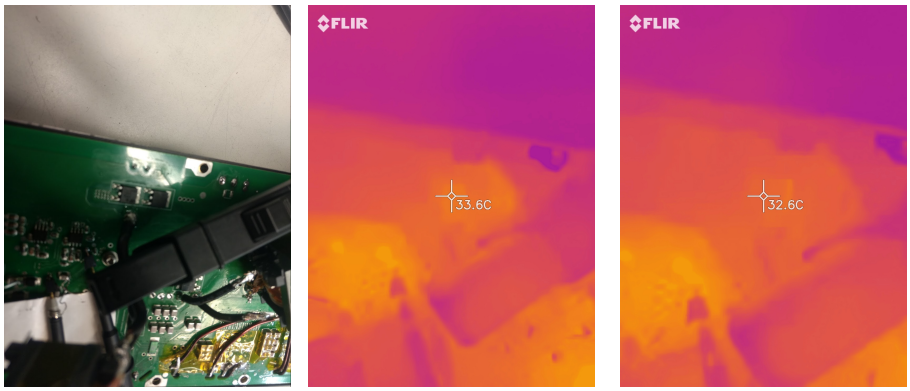


Figure 5.13: Measured peak efficiency for GaN HEMT 31 mΩ for two different deadtime curves in the DSP.



(a) Normal picture of the two diodes mounted on the module.

(b) Thermal photo of diodes with original deadtime curve at 35% load.

(c) Thermal photo of diodes with new deadtime curve at 35% load.

Figure 5.14: Thermal photos of the diodes in antiparallel to the transistors for two different deadtime curves used in the DSP.

5.5 Other measures for increasing the efficiency

Last section concluded that GaN HEMT works fine in an LLC converter, and that it does not have the same low load problems with excessive deadtimes as the low-ohmic Si MOSFET. In this section, other measured for increasing the efficiency is tested. The goal is to show that the efficiency does not deteriorate with GaN HEMT, and it might even be increased.

5.5.1 Changing the DC-link voltage at input

The converter benefits from operating close to the resonance frequency as discussed in section 3.7. It is therefore designed such that it operates close to this frequency at the nominal operating point. From a design perspective, this means choosing the turns ratio, nominal input voltage and nominal output voltage.

At the resonance frequency, the gain of the resonant tank will be equal to the turns ratio of the transformer as shown in section 3.2. Since only half the dc-link voltage will be seen at the transformer, the following relation holds

$$V_{dc} = 2 \cdot a \cdot V_{out} \tag{5.3}$$

and with turns ratio $a = \frac{20}{6}$ and a nominal output voltage $V_{out} = 53.7\,\mathrm{V}$ our nominal dc-link voltage is 358 V. This also means that if a higher voltage is needed at the output, and the converter should still operate at resonance frequency, the dc-link voltage must be increased.

However, the nominal voltage of 358 V is with synchronous rectification at the output. Because diodes are used at the output here, an additional voltage drop appears. This means the input voltage should be higher. Assuming a voltage drop across the diodes at the output of $V_{diode} = 1\,\mathrm{V}$, the input voltage should be

$$\Delta V_{dc} = 2 \cdot a \cdot V_{diode} = 6.66\,\mathrm{V}$$

This is also seen in fig. 5.15, where current and voltage waveforms for three different input voltages are shown in .

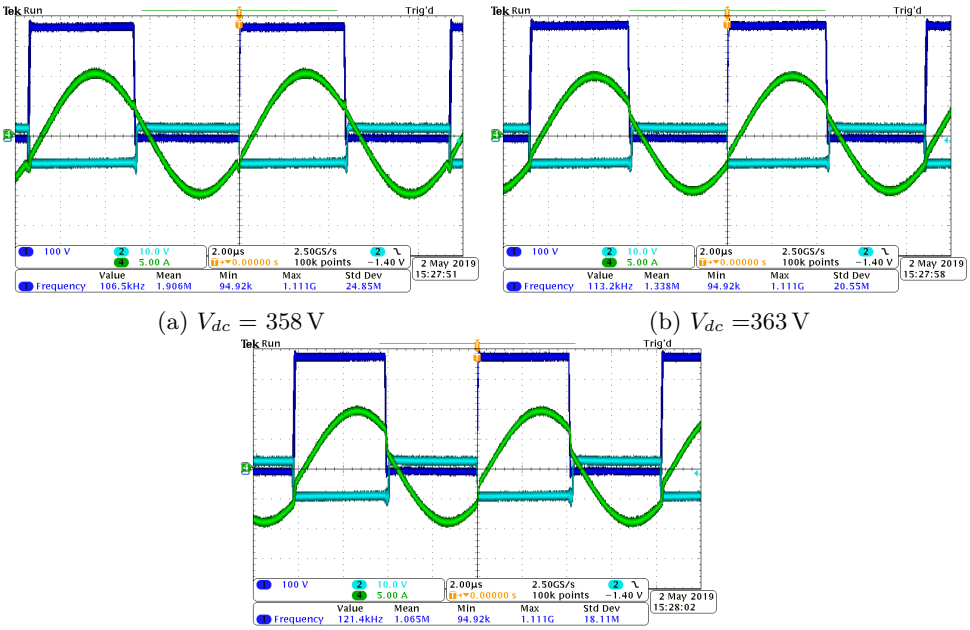
The frequency is recorded by the oscilloscope, and shows that the controller of the module moves closer to the resonance frequency as the input voltage increases. Therefore increasing the input voltage might increase the efficiency even further. To find the ideal voltage, the module is operated at the peak efficiency-load, while manually adjusting the input voltage and observing the efficiency recorded by the power analyzer. The optimal input voltage is then found to be $V_{dc} = 363\,\mathrm{V}$.

A new efficiency test is ran with the new deadtime curve, and adjusted input voltage. The results are shown in fig. 5.16. It is seen that changing the input voltage can increases the efficiency. Although the frequency increases, so the switching losses should be bigger, these increased losses are negligible in comparison to the reduced conduction losses when moving closer to resonance frequency. This is explained in section 3.3. It should be noted that this efficiency increase is not GaN HEMT-specific, but comes from the fact there is an additional output voltage drop from the full bridge rectifier.

5.5.2 Changing R_{gate}

The typical output characteristics for 70 mΩ GaN HEMT [19] is shown in fig. 5.17. Notice that $I_D(V_{ds})$A and therefore the losses is dependent on the gate current I_G.

It is reasonable to assume that the GaN HEMT 31 mΩ would have similar behaviour, and one possibility for efficiency increase could be to increase the gate driver current.



(a) $V_{dc} = 358\,\mathrm{V}$ (b) $V_{dc} = 363\,\mathrm{V}$

(c) $V_{dc} = 368\,\mathrm{V}$

Figure 5.15: Oscilloscope waveforms for three different dc-link voltages at the input of the LLC converter.

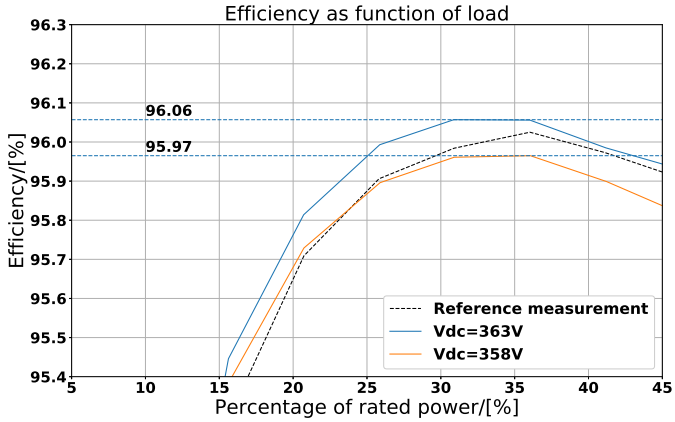


Figure 5.16: Measured peak efficiencies for GaN HEMT 31 mΩ with the new dead-time curve for two different input voltages and $R_{gate} = 470\,\Omega$.

The gate driver circuit is given in fig. 5.18. The voltage at the left node switches between gate- and gate+. The C_{gate} combined with R_a and R_b decides how fast

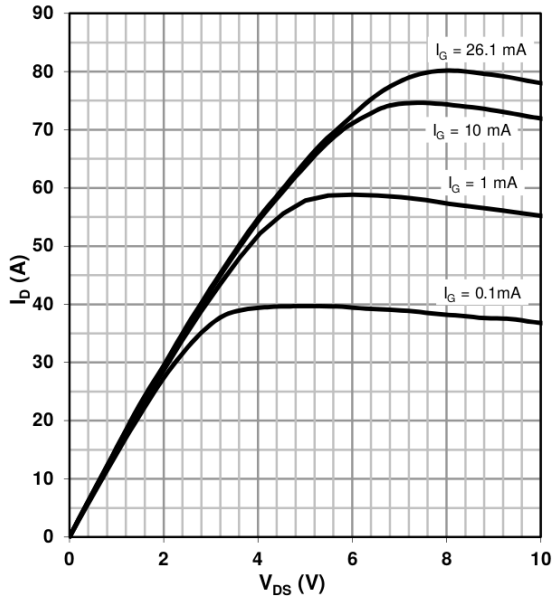


Figure 5.17: Typical output characteristics for GaN HEMT 70 mΩ. Obtained from datasheet [19].

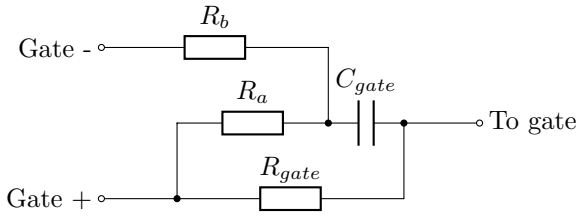


Figure 5.18: Simplified schematic of the gate driver used for driving the transistors in the half-bridge of the LLC converter.

the voltage should rise at the gate. After the transient period, the resistance R_{gate} decides how much current is provided to the gate. Ergo, the gate current during operation can be varied by changing the value of R_{gate}.

The original gate-driver resistance is 4.7 kΩ. After replacing it with an 470 Ω resistance, a new efficiency test is ran, comparing the two. Since the gate-voltage is 3.3 V, this corresponds to an increase in gate current from 0.7 mA to 7 mA. The results are shown in fig. 5.19. The efficiency actually deteriorates when lowering the gate driver resistance. The gate current was already high enough for this load range, and the increased losses in the gate driver reduces the efficiency. If the module was operated at higher loads however, the drain current would increase. This might necessitate higher I_G and gate driver losses, to make sure V_{DS} stays small.

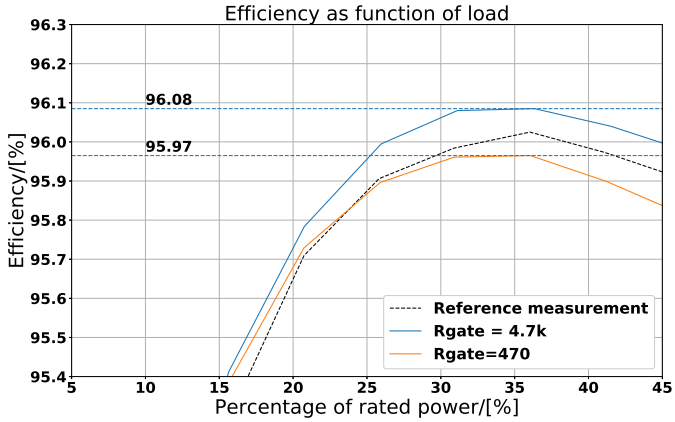


Figure 5.19: Measured peak efficiencies for GaN HEMT 31 mΩ with the new dead-time curve, input voltage of 363 V and two different gate driver resistances.

5.5.3 Changing magnetizing inductance, L_M

Another possible efficiency improvement is changing the magnetizing inductance. Increasing L_M would decrease the circulating current in the converter, as discussed in section 3.7. This could be possible with the GaN HEMTs, since a smaller current is needed to discharge the smaller stored charge. The 72.9 µH magnetizing inductance is desoldered, and a new 87.6 µH magnetizing inductance is soldered on. An efficiency test is done, and the results are shown in fig. 5.20.

An efficiency increase of 0.03% is seen. At 30% load, this corresponds to 0.3 W.

However, after changing the magnetizing inductance, low load problems must be checked. The module is ran again at no load to check if the problems are back. Result is shown in fig. 5.21. It is seen that with the new magnetizing inductance, the converter once again operates at maximum frequency. This indicates that it has problems to regulating the voltage. The delay times are however not excessive, and the low load problems are different from what was observed in section 5.4.

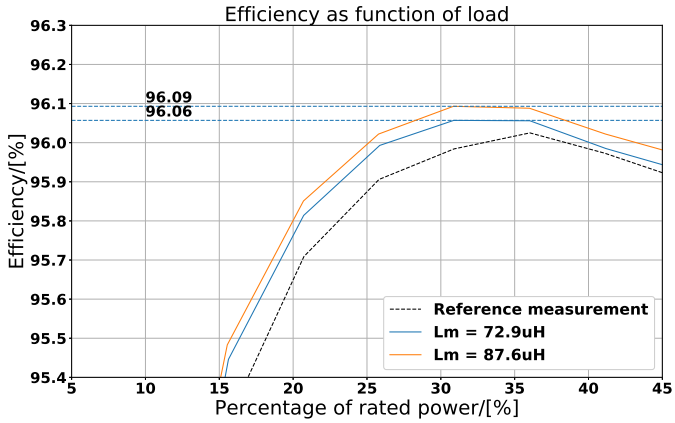
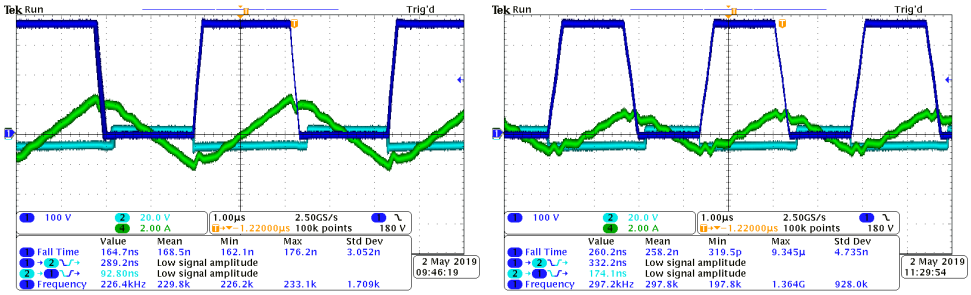


Figure 5.20: Measured peak efficiencies for GaN HEMT 31 mΩ with the new dead-time curve, $V_{dc} = 363$V and $R_{gate} = 470$ with two different magnetizing inductances.



(a) Original no load waveforms with $L_M = 72.9\,\mu$H

(b) No load waveforms for new magnetizing inductance $L_M = 87.6\,\mu$H

Figure 5.21: Oscilloscope no load waveforms for two different magnetizing inductances.

The output voltage at no load was with the new inductance measured to 55.2 V. This is higher than nominal output voltage. This can be explained by looking at the transfer function derived in section 3.10.2.

In fig. 5.22 the transfer function is plotted with the two different magnetizing inductances for no load. The load $R = 1000\,\Omega$ is meant to represent the no load condition. The use of the transfer function at frequencies far above resonance is justified here, because the loads are low, as validated in chapter 4. Looking at the datasheet of the rectifier diode used [50] together with table 3.1, the converter sees a junction capacitance of about 1 nF at the output of the transformer. Although the junction capacitance in reality is nonlinear, it is approximated $C_{jn} = 1\,$nF.

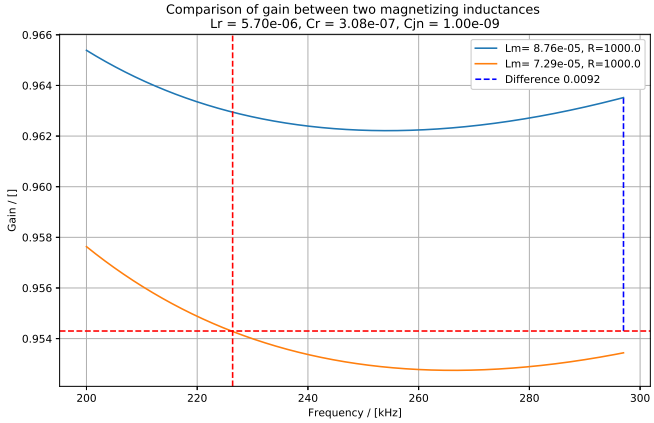


Figure 5.22: Gain curves calculated from the transfer function when including parasitic effect of the rectifier diodes at high frequencies for two different magnetizing inductances.

The no load curves from the oscilloscope in fig. 5.21 shows that the converter originally operates at a switching frequency of 226.4 kHz when the inductance is 72.9 µH. Looking at the red curve in fig. 5.22, the gain needed to achieve nominal output voltage is seen to be 0.9545. Changing to the new inductance of 87.6 µH, the converter tries to regulate to the same gain, but reaches the frequency limit. Notice that the difference in gain between the blue curve and the wanted gain is at $f = 295\,\text{kHz}$ is 0.0092 . With an input voltage of 358 V, this corresponds to a difference at the output of

$$\Delta V = 0.0092 \cdot \frac{1}{2} 358\,\text{V} = 1.65\,\text{V}$$

The measured difference was also 1.6 V. It is then concluded that the effect of the parasitic capacitance of the diode rectifier has a real impact on the gain at low loads.

5.5.4 Changing snubber capacitances, C_{snub}

While increasing the efficiency, the limit of the module was once again reached. After changing the magnetizing inductance L_M, no load problems are back. The question is then, how can the efficiency improvement be kept, while removing the low load problems.

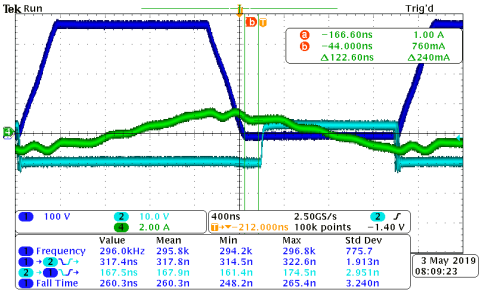
These low load problems are caused by the parasitic effects of the output diodes, as discussed in section 3.10. It makes sense that these low load problems appear here, because when changing to GaN HEMT transistors, the output capacitance was significantly reduced. The effect of C_{oss} was supposed to counteract the low-load parasitic effects of C_{jn}. One possible choice to solve the problem is to

Snubber value	Measured fall time
220 pF	260.3 ns
330 pF	308.8 ns
470 pF	327.2 ns

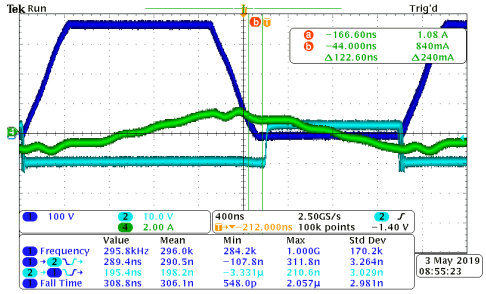
Table 5.8: Measured drain-source voltage fall time for GaN HEMT 31 mΩ with the new deadtime curve and $L_M = 87.6\,\mu H$ for three different snubber capacitances. Also $V_{dc} = 363\,V$, $R_{gate} = 470\,\Omega$

adjust the snubber capacitance, C_{snub}.

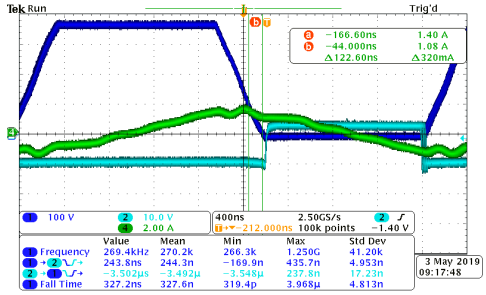
The waveforms for three different snubber capacitances are shown in fig. 5.23. Note the increased fall time of the three different snubbers. The fall times are also given in table 5.8. From the analysis in section 3.10.3, this is known the reduce the gain at low loads, because of increased time to commutate the charges of the junction capacitances of the diodes.



(a) $C_{snub} = 220\,pF$. V_{out} is measured to 55.2 V.



(b) $C_{snub} = 330\,pF$.V_{out} is measured to 54.4 V.



(c) $C_{snub} = 470\,pF$. V_{out} is measured to 53.7 V.

Figure 5.23: Oscilloscope no load waveforms for three different snubber capacitances with $L_M = 87.6\,\mu H$ and new deadtime curve.

The measured output voltages is given in table 5.9. With the largest snubber capacitance, $C_{snub} = 470\,pF$, the output voltage is back to nominal value, and no load problems are gone.

Snubber value	Measured output voltage
220 pF	55.2 V
330 pF	54.4 V
470 pF	53.7 V

Table 5.9: Measured output voltages for GaN HEMT 31 mΩ with the new deadtime curve and $L_M = 87.6\,\mu H$ for three different snubber capacitances. Also $V_{dc} = 363\,V$, $R_{gate} = 470\,\Omega$

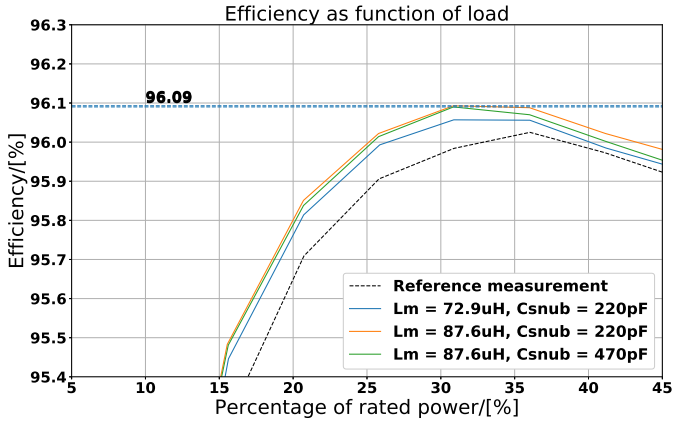


Figure 5.24: Measured peak efficiency for GaN HEMT 31 mΩ with the new deadtime curve, $V_{dc} = 363V$, $R_{gate} = 470$ and $L_M = 87.6\,\mu H$ with two different snubber capacitances.

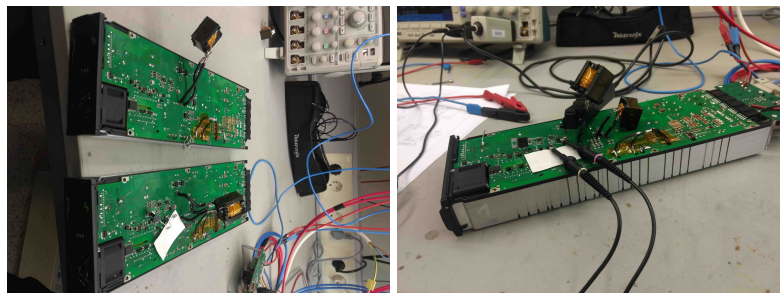
Efficiency is tested again. The results are shown in fig. 5.24. The efficiency decreases when increasing the snubber capacitance. This is probably caused by the additional losses in the snubber circuit, since it conducts current for a longer time period.

However, the efficiency is still increased from the case with $L_M = 72.9\,\mu H$, although not by much. It can then be concluded that increasing the efficiency with GaN HEMT 31 mΩ by a change of magnetizing inductance is purposeful if the snubber capacitance is changed accordingly.

Note also that the real efficiency increase is probably also even larger than what can be seen here, since the module is altered, discussed in section 5.5.5.

5.5.5 Extra cable

After desoldering the magnetizing inductance, and soldering on the new inductance on the back side of the module, as shown in fig. 5.25. In fig. 5.25a as compared to fig. 5.25b, the magnetizing inductance is still on the inside of the module. After this change, efficiency increase was not as big as expected.



(a) Not desoldered. Only one inductance sticks out per module.

(b) Desoldered. Two inductances stick out.

Figure 5.25: Picture of the modules with and without the desoldered magnetizing inductance. Notice the extra cable in the desoldered case.

The observed drop in efficiency could be because of the extra cable and soldering tin. An efficiency test with the desoldered module compared to the original module with proper mounting of L_M is done, with all other parameters being the same. The results are shown in fig. 5.26. The efficiency drops 0.09%, and the drop looks to be proportional to the load. This backs up the hypothesis that the efficiency drop is from the added resistance from the extra cable. This example emphasizes the importance of keeping the setup the same throughout the laboratory measurements.

All other changes that were made with the modules were with surface mounted devices and/or software changes. Therefore, as opposed to the case with the magnetizing inductance, these changes do not alter the setup in such a way that the efficiency would not be comparable from one case to the other.

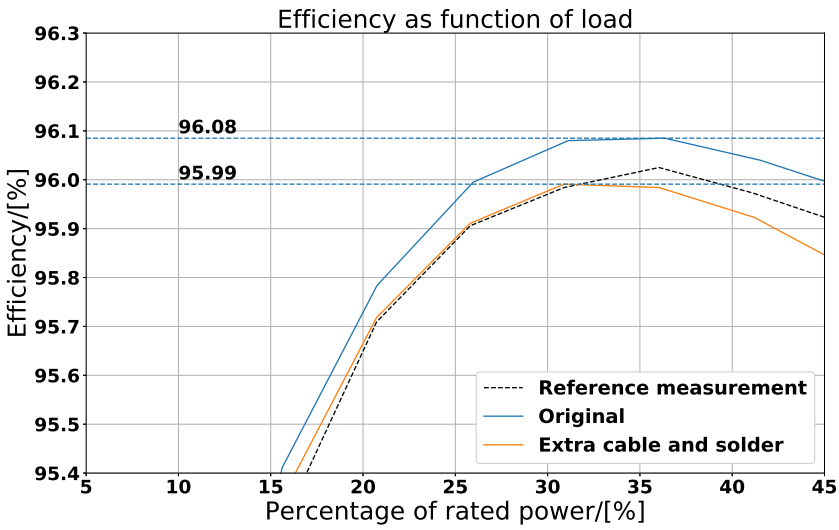


Figure 5.26: Measured peak efficiencies for GaN HEMT 31 mΩ with the new dead-time curve and two different connections for the magnetizing inductance.

5.6 Transfer function

To verify the transfer function calculated in section 3.2 transfer functions measurement are done as well. The AP Instruments Inc. 15MHz Analog Network Analyzer shown in table 5.2 was used for analysis. The goal is to measure the transfer function $\frac{V_{out}}{V_{in}}$. Connection of the lab equipment to the circuit is also shown in fig. 5.27. A picture of the setup is shown in fig. 5.28. The sinusoidal voltage source varies in frequency constantly, and the probes record the voltages at input and output as a function of this frequency. All components used in the circuit was measured with an LCR-meter [54] and their values are recorded in table 5.10.

Evaluating the transfer function with semiconductor elements included is not a straight forward task, since transistors and diodes are non-linear elements, and must be turned on and off with correct timing. They are therefore neglected here. This is justified with the same assumptions as in section 3.2. Also the voltage at the input will in this test setup be sinusoidal, while for the real converter it is approximately a square wave.

This means that these transfer function measurements do not accurately represent the LLC converter for all operating points. However, the explicit expression for the transfer function from the FHA analysis is verified in this section.

In figure fig. 5.29 the results of the transfer function measurement is shown. The theoretically calculated transfer function in section 3.2 is also included for comparison. There is a clear correspondance between theory and lab measurements. For the lowest load, $R = 500\,\text{m}\Omega$, the contact resistance probably also plays a role,

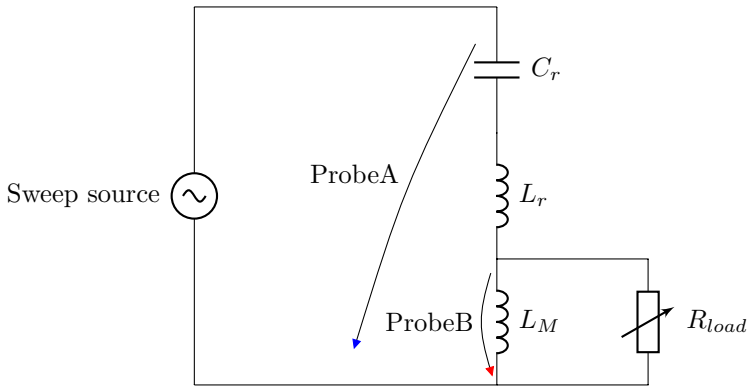
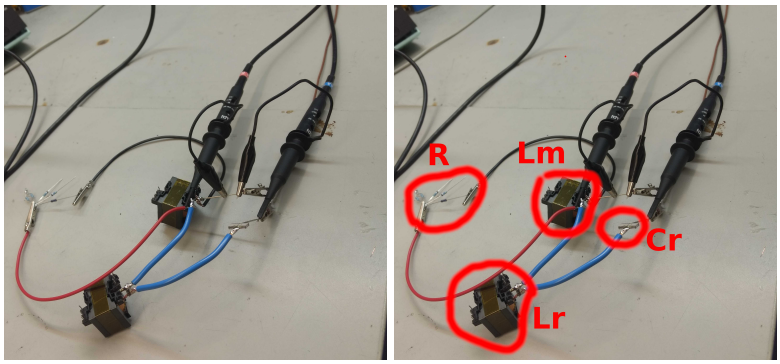


Figure 5.27: Circuit schematic for the circuit used for transfer function measurements.

Component	Value
L_m	73uH
L_r	11.4uH
C_r	153nF
R	Varies

Table 5.10: Components used in measurement of transfer function



(a) Lab setup (b) Explanation of components

Figure 5.28: Picture of the lab setup used for measuring the transfer function.

and could explain the difference between measurement and theory. The angle is also shown. It is seen that the tank goes from capacitive to inductive when crossing the system resonance frequency, as expected from theory.

Note also that in chapter 4 the assumptions made when deriving the transfer function is verified through simulation.

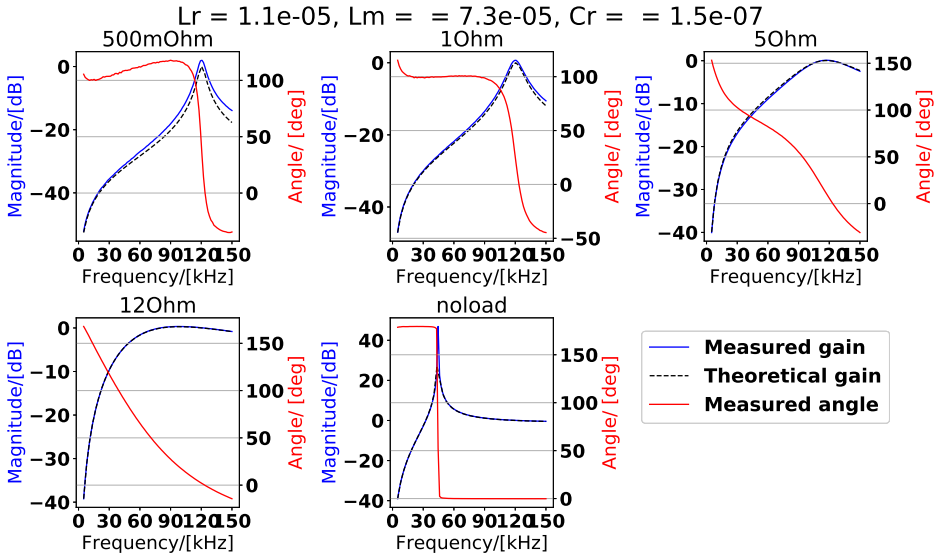


Figure 5.29: Measured gain and phase shift compared to theoretically calculated for different load values.

5.7 Tolerances

All lab measurements are subject to disturbances and noise. The equipment also has limited accuracy and bandwidth, and a discussion on the validity of the results should be included. This is done by looking at the datasheets of the equipment used.

5.7.1 Yokogawa WT3000 precision power analyzer

Since the voltage and current measurements used for calculating the efficiency are done at the input before the DC-link and at the output after the output capacitance, the currents and voltages are DC. The power accuracy is then given in online [55] as *Basic power accuracy: 0.02% of reading*. With reading of about 1 kW, this corresponds to an error of about 0.2 W. The efficiency changes measured in the above sections were on a scale from 0.3 W to 2 W. This is higher than the given tolerance, and can therefore be said to be significant. It is still important to keep the test setup as constant as possible throughout. This is to ensure good repeatability of the measurements, and that one measurement can be directly compared to the other.

5.7.2 Tektronix oscilloscope and probes

The Tektronix DPO 3034 Digital Phosphor Oscilloscope[56] has a sampling frequency of 2.5 GS/s and a bandwidth og 300 MHz. This means it can record time

changes as small as $\frac{1}{2.5 \cdot 10^9} = 0.4\,\text{ns}$ and frequency up to 300 MHz, sufficient for our usage here. However, the oscilloscope can not be better than the probes. The current probe [57] has a bandwidth of 120 MHz, while the voltage probe [58] on the other hand has a bandwidth of 500 MHz, meaning the setup is limited by the current probe. 120 MHz should be sufficient for the purposes of this report, with the converter having a max operating frequency of 295 kHz. The voltage probes are also connected as close to the circuit board as possible to avoid disturbances in the measurements from parasitic influences.

Another aspect of the oscilloscope measurements is the delay time function used. It should be kept in mind that the measurement function of the oscilloscope goes from midpoint to midpoint. Because the real delay time of interest is from the gate-source voltage hits negative threshold, until the drain-source voltage blocks 100% of the dc-link voltage, these values will deviate slightly from the real delay time. However, as long as all measurements are done the same way, the trends should be clear, and this should not pose any problems.

5.7.3 Flir ONE thermocamera

Website specifications for the thermal camera [59] claims an accuracy of $\pm 3\,^\circ\text{C}$. This exceeds the observed temperature difference of $1\,^\circ\text{C}$ by far. These results are therefore not good enough to say anything for certain about the temperature of the diode, other than very rough estimates.

Chapter 6

Conclusion and further work

6.1 Conclusion

A literature study on the LLC topology and GaN devices is concluded. The LLC is seen to be thoroughly researched in literature, and is a suitable topology for many applications, exhibiting both ZVS and buck and boost possibilities. Important design considerations and design methodology for the LLC is discussed. Also for GaN HEMT, many good results are shown in literature.

A direct comparison between a Si MOSFET and GaN HEMT is concluded, showing the superior performance of GaN HEMT devices in soft switching topologies, according to the figure of merit. This shows possibilities for efficiency increase in an LLC converter utilizing GaN HEMT devices. However, some design considerations are shown to be different with GaN devices as opposed to Si MOSFETs.

The transfer function is calculated with the fundamental harmonic approximation(FHA) and is verified through simulation. Some limitations to this approach is shown, especially at high loads far away from the resonance frequency. The derived transfer function is also checked through laboratory measurements, and good correspondence between theory and reality is found.

Through laboratory measurements, many of the theoretically discussed concepts are validated. The delay time as a function for the two devices is measured. In particular, the smaller capacitances of the GaN HEMT is proven to give shorter delay times, and therefore also smaller deadtimes can be chosen in the DSP.

Most importantly, problems occuring at low load is analyzed. Two root causes are identified, one being excessive delay times at low loads from large output capacitance values. The other being parasitic effects of the junction capacitance of the output rectifier diodes. Low ohmic, 31 mΩ, GaN HEMTs and MOSFETs are compared in this regard, with GaN HEMT being the preferred choice. Using GaN HEMT devices, the first problem, excessive delay times, is removed completely. The second problem, the effect of the junction capacitances, is shown to disappear by addition of additional snubber capacitance.

Taking advantage of the reduced delay time for the GaN HEMT, it is seen

Measure	Efficiency improvement at 30% load / [%]	Efficiency improvement at 30% load / [W]
Decreasing $R_{ds,on}$ from 70 mΩ to 31 mΩ	0.18	1.6
New deadtime curve giving shorter deadtimes	0.1	0.9
Increasing V_{dc} from 358 V to 363 V	0.1	0.9
Decreasing R_{gate} from 4.7 kΩ to 470 Ω	-0.11	-1
Increasing L_M from 72.9 µH to 87.6 µH	0.03	0.3
Increasing C_{snub} from 220 pF to 470 pF	0	0
Extra cable	-0.09	-0.8

Table 6.1: Summary of all efficiency improvements made with the GaN module.

that losses can be decreased. Many other efficiency considerations are also made. They are summed up in table 6.1. The original module should be compared with the modded GaN module. Original transistors were Si 33 mΩ, so the efficiency improvement from changing $R_{ds,on}$ can not be included. Summing up the other total positive contributions and also adding on 0.09% if the extra cable was not there, the total efficiency improvement possible with GaN is 0.32% or 2.88 W at 30% load. The module tested is already quite efficient, at about 96 % peak efficiency. Without synchronous rectification, the diodes on the output side account for a significant loss. The fan also consumes just under 4 W. This means that at peak efficiency, which is at 30% load or 1000 W, much of the 36 W of losses is already accounted for. The different measures above for pushing the limits even further, might seem excessive for only 3 W of improvement, but it should be kept in mind that the converter is already quite efficient. A 3 W improvement from 36 W of total losses is a significant improvement.

The assumption here is that all these efficiency improvements are decoupled from one another. This might not be true. Unfortunately, because of limited time, the efficiency measures were not tested all at once, and it is not obvious that they are independent of each other.

The conclusion is then that GaN HEMT solves the low load problems present for the low ohmic Si MOSFET, and this is achieved without any detriment to efficiency. Efficiency might even increase. This shows that a decrease in $R_{ds,on}$ is made possible by GaN HEMT technology, because of the smaller terminal capacitances. As more research is done on GaN HEMTs and the technology matures, even better results can be achieved in the future.

6.2 Further work

The diode bridge on the secondary side has a constant voltage drop, which provides significant losses. To maximize efficiency, synchronous rectification on the secondary side of the transformer should be implemented, as this can decrease the conduction losses even further. The module should be tested with the parameters with assumed best efficiency, to see if they are dependent on each other or not. Smaller capacitances also facilitate faster switching, and a burst mode control approach to the low load problems can also be tested. As GaN HEMTs is a quite new technology compared with Si MOSFETS, the number of commercially available devices and their quality is expected to grow, improving results further.

Bibliography

[1] L. R. Blingsmo, "A review on the llc converter and possible efficiency improvements with wide-bandgap gan devices", Dec. 2018.

[2] T. Bawden, "Global warming: Data centres to consume three times as much energy in next decade, experts warn", *The Independent*, Jan. 23, 2016. [Online]. Available: https://www.independent.co.uk/environment/global-warming-data-centres-to-consume-three-times-as-much-energy-in-next-decade-experts-warn-a6830086.html (visited on 12/18/2018).

[3] T. S. P. Statista. (2018). Energy consumption of google from 2011 to 2017 (in gigawatt hours), [Online]. Available: https://www.statista.com/statistics/788540/energy-consumption-of-google/ (visited on 12/18/2018).

[4] s. e. Eurostat. (2018). Renewable energy statistics, [Online]. Available: https://ec.europa.eu/eurostat/statistics-explained/index.php/Renewable_energy_statistics#of_electricity_generated_come_from_renewable_sources (visited on 12/18/2018).

[5] J. Roberts, H. Lafontaine, and C. McKnight-MacNeil, "Advanced spice models applied to high power gan devices and integrated gan drive circuits", in *Applied Power Electronics Conference and Exposition (APEC), 2014 Twenty-Ninth Annual IEEE*, IEEE, 2014, pp. 493–496.

[6] T. J. Flack, B. N. Pushpakaran, and S. B. Bayne, "Gan technology for power electronic applications: A review", *Journal of Electronic Materials*, vol. 45, no. 6, pp. 2673–2682, 2016.

[7] N. Kaminski, "State of the art and the future of wide band-gap devices", in *Power Electronics and Applications, 2009. EPE'09. 13th European Conference on*, IEEE, 2009, pp. 1–9.

[8] W. Zhang, Y. Long, Z. Zhang, F. Wang, L. M. Tolbert, B. J. Blalock, S. Henning, C. Wilson, and R. Dean, "Evaluation and comparison of silicon and gallium nitride power transistors in llc resonant converter", in *Energy Conversion Congress and Exposition (ECCE), 2012 IEEE*, IEEE, 2012, pp. 1362–1366.

[9] W. Zhang, Z. Xu, Z. Zhang, F. Wang, L. M. Tolbert, and B. J. Blalock, "Evaluation of 600 v cascode gan hemt in device characterization and all-gan-based llc resonant converter", in *Energy Conversion Congress and Exposition (ECCE), 2013 IEEE*, IEEE, 2013, pp. 3571–3578.

[10] M. D. Seeman, S. R. Bahl, D. I. Anderson, and G. A. Shah, "Advantages of gan in a high-voltage resonant llc converter", in *Applied Power Electronics Conference and Exposition (APEC), 2014 Twenty-Ninth Annual IEEE*, IEEE, 2014, pp. 476–483.

[11] A. Lidow, J. Strydom, M. De Rooij, and D. Reusch, *GaN transistors for efficient power conversion*. John Wiley & Sons, 2014.

[12] E. A. Jones, F. F. Wang, and D. Costinett, "Review of commercial gan power devices and gan-based converter design challenges", *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 707–719, 2016.

[13] E. A. Jones, F. Wang, and B. Ozpineci, "Application-based review of gan hfets", in *Wide Bandgap Power Devices and Applications (WiPDA), 2014 IEEE Workshop on*, IEEE, 2014, pp. 24–29.

[14] J. Millan, P. Godignon, X. Perpina, A. Pérez-Tomás, and J. Rebollo, "A survey of wide bandgap power semiconductor devices", *IEEE transactions on Power Electronics*, vol. 29, no. 5, pp. 2155–2163, 2014.

[15] J. W. Kolar, D. Bortis, and D. Neumayr, "The ideal switch is not enough", in *Power Semiconductor Devices and ICs (ISPSD), 2016 28th International Symposium on*, IEEE, 2016, pp. 15–22.

[16] J. W. Kolar, F. Krismer, Y. Lobsiger, J. Muhlethaler, T. Nussbaumer, and J. Minibock, "Extreme efficiency power electronics", in *2012 7th International Conference on Integrated Power Electronics Systems (CIPS)*, IEEE, 2012, pp. 1–22.

[17] M. Kasper, R. M. Burkart, G. Deboy, and J. W. Kolar, "Zvs of power mosfets revisited", *IEEE Transactions on Power Electronics*, vol. 31, no. 12, pp. 8063–8067, 2016.

[18] *600v coolmos cfd7, high voltage superjunction mosfet 70mohm*, IPP60R070CFD7, Infineon. [Online]. Available: https://www.infineon.com/cms/en/product/power/mosfet/500v-900v-coolmos-n-channel-power-mosfet/600v-coolmos-n-channel-power-mosfet/ipp60r070cfd7/.

[19] *Gallium nitride coolgan 600v e-mode power transistor igot60r070d1 for ultimate efficiency and reliability 70mohm*, IGOT60R070D1, Infineon. [Online]. Available: https://www.infineon.com/cms/en/product/power/wide-band-gap-semiconductors-sic-gan/gallium-nitride-gan/igot60r070d1/.

[20] D. Reusch and J. Strydom, "Evaluation of gallium nitride transistors in high frequency resonant and soft-switching dc–dc converters", *IEEE Transactions on Power Electronics*, vol. 30, no. 9, pp. 5151–5158, 2015.

[21] N. Badawi, O. Hilt, E. Bahat-Treidel, J. Böcker, J. Würfl, and S. Dieckerhoff, "Investigation of the dynamic on-state resistance of 600 v normally-off and normally-on gan hemts", *IEEE Transactions on Industry Applications*, vol. 52, no. 6, pp. 4955–4964, 2016.

[22] S. Abdel-Rahman, "Resonant llc converter: Operation and design", *Infineon Technologies North America (IFNA) Corp.*, 2012.

[23] J. F. Lazar and R. Martinelli, "Steady-state analysis of the llc series resonant converter", in *Applied Power Electronics Conference and Exposition, 2001. APEC 2001. Sixteenth Annual IEEE*, IEEE, vol. 2, 2001, pp. 728–735.

[24] J.-h. Jung and J.-g. Kwon, "Theoretical analysis and optimal design of llc resonant converter", in *Power Electronics and Applications, 2007 European Conference on*, IEEE, 2007, pp. 1–10.

[25] X. Xie, Z. Zhao, C. Zhao, J. Zhang, and Z. Qian, "Analysis and optimization of llc resonant converter with a novel over-current protection circuit", in *Telecommunications Conference, 2005. INTELEC'05. Twenty-Seventh International*, IEEE, 2005, pp. 487–490.

[26] N. Mohan and T. M. Undeland, *Power electronics: converters, applications, and design*. John Wiley & Sons, 2007.

[27] R. L. Steigerwald, "A comparison of half-bridge resonant converter topologies", *IEEE transactions on Power Electronics*, vol. 3, no. 2, pp. 174–182, 1988.

[28] E. W. Weisstein, *Fourier series – square wave from mathworld – a wolfram web resource*. [Online]. Available: http://mathworld.wolfram.com/FourierSeriesSquareWave.html.

[29] R. Beiranvand, B. Rashidian, M. R. Zolghadri, and S. M. H. Alavi, "Using llc resonant converter for designing wide-range voltage source", *IEEE Transactions on Industrial Electronics*, vol. 58, no. 5, pp. 1746–1756, 2011.

[30] T. Duerbaum, "First harmonic approximation including design constraints", in *Telecommunications Energy Conference, 1998. INTELEC. Twentieth International*, IEEE, 1998, pp. 321–328.

[31] G. Ivensky, S. Bronshtein, and A. Abramovitz, "Approximate analysis of resonant llc dc-dc converter", *IEEE Transactions on power electronics*, vol. 26, no. 11, pp. 3274–3284, 2011.

[32] S. De Simone, C. Adragna, C. Spini, and G. Gattavari, "Design-oriented steady-state analysis of llc resonant converters based on fha", in *Power Electronics, Electrical Drives, Automation and Motion, 2006. SPEEDAM 2006. International Symposium on*, IEEE, 2006, pp. 200–207.

[33] B. Yang, "Topology investigation of front end dc/dc converter for distributed power system", PhD thesis, Virginia Tech, 2003.

[34] R. W. (W. Erickson, *Fundamentals of power electronics*, eng, Norwell, Mass., 2001.

[35] C. Buccella, C. Cecati, H. Latafat, and K. Razi, "Digital control of a half-bridge llc resonant converter", in *Power Electronics and Motion Control Conference (EPE/PEMC), 2012 15th International*, IEEE, 2012, LS6a–4.

[36] B. Lu, W. Liu, Y. Liang, F. C. Lee, and J. D. Van Wyk, "Optimal design methodology for llc resonant converter", in *Applied Power Electronics Conference and Exposition, 2006. APEC'06. Twenty-First Annual IEEE*, IEEE, 2006, 6–pp.

[37] B. Yang, F. C. Lee, and M. Concannon, "Over current protection methods for llc resonant converter", in *Applied Power Electronics Conference and Exposition, 2003. APEC'03. Eighteenth Annual IEEE*, IEEE, vol. 2, 2003, pp. 605–609.

[38] B. Yang, R. Chen, and F. C. Lee, "Integrated magnetic for llc resonant converter", in *Applied Power Electronics Conference and Exposition, 2002. APEC 2002. Seventeenth Annual IEEE*, IEEE, vol. 1, 2002, pp. 346–351.

[39] D. Fu, F. C. Lee, and S. Wang, "Investigation on transformer design of high frequency high efficiency dc-dc converters", in *Applied Power Electronics Conference and Exposition (APEC), 2010 Twenty-Fifth Annual IEEE*, IEEE, 2010, pp. 940–947.

[40] J. W. Kolar, *Power Electronic Systems I Lecture Notes*. ETH Zürich, 2017.

[41] B.-H. Lee, M.-Y. Kim, C.-E. Kim, K.-B. Park, and G.-W. Moon, "Analysis of llc resonant converter considering effects of parasitic components", in *INTELEC 2009-31st International Telecommunications Energy Conference*, IEEE, 2009, pp. 1–6.

[42] W. Feng, F. C. Lee, P. Mattavelli, and D. Huang, "A universal adaptive driving scheme for synchronous rectification in llc resonant converters", *IEEE Transactions on power electronics*, vol. 27, no. 8, pp. 3775–3781, 2012.

[43] J.-H. HKim, C.-E. Kim, J.-K. Kim, and G.-W. Moon, "Analysis for llc resonant converter considering parasitic components at very light load condition", in *8th International Conference on Power Electronics-ECCE Asia*, IEEE, 2011, pp. 1863–1868.

[44] Z. Hu, Y.-F. Liu, and P. C. Sen, "Bang-bang charge control for llc resonant converters", *IEEE Transactions on Power Electronics*, vol. 30, no. 2, pp. 1093–1108, 2015.

[45] J. Jang, M. Joung, B. Choi, S. Hong, and S. Lee, "Dynamic analysis and control design of optocoupler-isolated llc series resonant converters with wide input and load variations", *IET Power Electronics*, vol. 5, no. 6, pp. 755–764, 2012.

[46] W. Feng, F. C. Lee, and P. Mattavelli, "Optimal trajectory control of burst mode for llc resonant converter", *IEEE Transactions on Power Electronics*, vol. 28, no. 1, pp. 457–466, 2013.

[47] ——, "Simplified optimal trajectory control (sotc) for llc resonant converters", *IEEE Transactions on Power Electronics*, vol. 28, no. 5, pp. 2415–2426, 2013.

[48] B. Yang, F. C. Lee, A. Zhang, and G. Huang, "Llc resonant converter for front end dc/dc conversion", in *Applied Power Electronics Conference and Exposition, 2002. APEC 2002. Seventeenth Annual IEEE*, IEEE, vol. 2, 2002, pp. 1108–1112.

[49] X. Fang, H. Hu, Z. J. Shen, and I. Batarseh, "Operation mode analysis and peak gain approximation of the llc resonant converter", *IEEE Transactions on Power Electronics*, vol. 27, no. 4, pp. 1985–1995, 2012.

[50] *Power schottky rectifier dual diode*, DSSS 35-008AR, IXYS. [Online]. Available: http://ixapps.ixys.com/DataSheet/L654.PDF.

[51] *Ef series power mosfet with fast body diode*, SIHG70N60EF, VISHAY. [Online]. Available: http://www.vishay.com/ppg?91598.

[52] *600v coolmos cfd7, high voltage superjunction mosfet 31mohm*, IPW60R031CFD7, Infineon. [Online]. Available: https://www.infineon.com/cms/en/product/power/mosfet/500v-900v-coolmos-n-channel-power-mosfet/600v-coolmos-n-channel-power-mosfet/ipw60r031cfd7/.

[53] *650 v, 6 a high surge silicon carbide power schottky diode*, STPSC6H065, STmicroelectronics. [Online]. Available: https://www.st.com/en/diodes-and-rectifiers/stpsc6h065.html.

[54] *Handheld lcr meter*, U1733C, Agilent. [Online]. Available: www.sophphx.caltech.edu/Lab_Equipment/Agilent_U1731C_LCR_Meter.pdf.

[55] *Yokogawa wt300 precision power analyzer*, WT3000, Yokogawa. [Online]. Available: https://tmi.yokogawa.com/no/solutions/products/power-analyzers/wt3000-precision-power-analyzer/#Documents-Downloads___downloads_9.

[56] *Digital phosphor oscilloscope (300mhz, 2.5gs/s)*, DPO 3034, Tektronix. [Online]. Available: https://www.tek.com/oscilloscope/mso3000-dpo3000.

[57] *120 mhz, 30 amp ac/dc current probe*, TCP0030A, Tektronix. [Online]. Available: https://www.tek.com/manual/tcp0030a.

[58] *500 mhz passive probe*, P6139B, Tektronix. [Online]. Available: https://www.tek.com/datasheet/500-mhz-passive-probes.

[59] *Pro-grade thermal camera for smartphones*, ONE Pro, FLIR. [Online]. Available: https://www.flir.com/products/flir-one-pro/.

[60] I. Batarseh, "Resonant converter topologies with three and four energy storage elements", *IEEE Transactions on power electronics*, vol. 9, no. 1, pp. 64–73, 1994.

[61] I.-O. Lee and G.-W. Moon, "The k-q analysis for an llc series resonant converter", *IEEE Transactions on Power Electronics*, vol. 29, no. 1, pp. 13–16, 2014.

Appendices

Appendix A

Simulation model

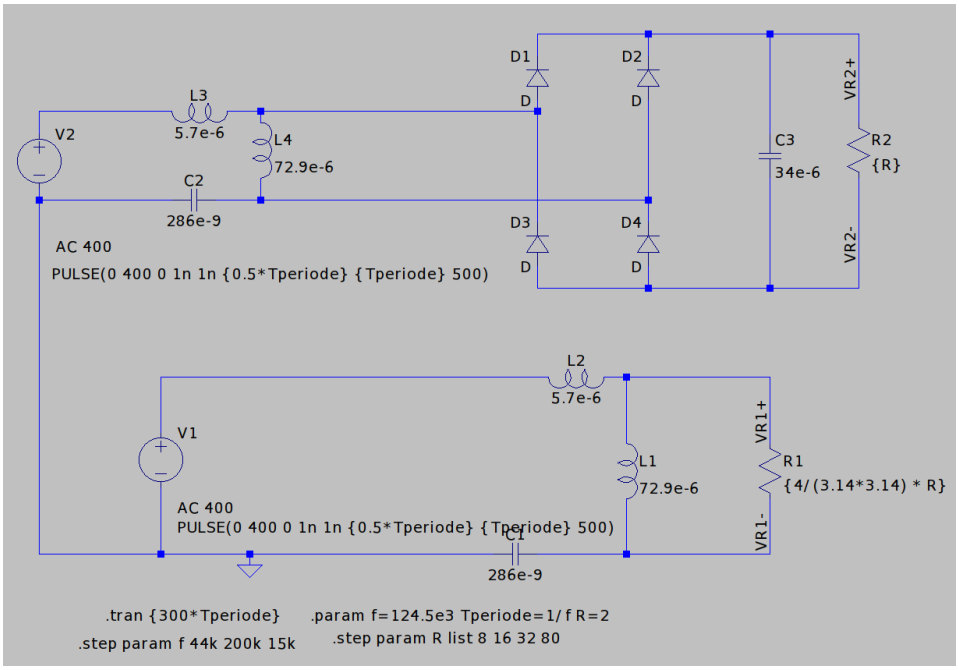


Figure A.1: Simulation model. The upper half is what is referred to as the 'complete model'. The lower part is referred to as 'simple model'.

Appendix B

Report progress

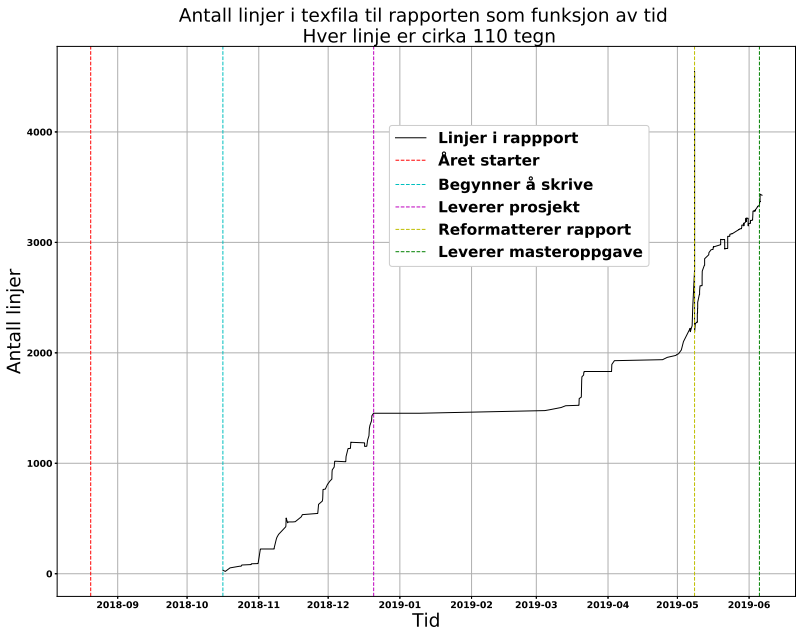


Figure B.1: Report progress as a function of time. Provided as a curiosity.

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Master thesis spring 2019

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