Master's thesis

NTNU
Norwegian University of Science and Technology
Faculty of Information Technology and Electrical Engineering
Department of Electric Power Engineering

Håkon Magne Bye

Investigation of a 200kW SiC-based IBC for high-speed hydrogen ferries

Master's thesis in Energy and Environmental engineering
Supervisor: Dimosthenis Peftitsis, Fredrik Aarskog
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ABSTRACT

In this thesis, an investigation of a 200kW SiC-based 6-ph IBC was carried out. The bus voltage is 1kV, supplied by series connected FC stacks with a voltage range from 520-900V.

Weight and volume are of great concerns for all vehicle applications. Fuel cells also have very low current ripple toleration, making low converter weight and volume hard to realize. Initial estimations showed an FC converter weight of over a ton for the ferry. An eventual criterion of galvanic isolation would further add weight and volume but also cost. Comprehensive interviews with industry, however, revealed that an un-isolated topology in combination with CM filters is considered most favorable. The investigated IBC converter topology was determined to be the topology of choice based on a literature study for the specific ferry application. SiC semiconductor was utilized as they allowed significant weight reduction compared to Si in addition to being well suited for the IBC voltage and currents.

Converter load profiles for an actual high-speed ferry in Trondheim was estimated. Fuel cell behavior based on PowerCell Sweden MS100 stacks was investigated, and an approximate 3-piece linearization was developed as an FC approximation, also accounting for FC aging. IBC behavior for a different number of phases was investigated, and a 6-ph part-load operation scheme was proposed based on the discovered load profiles and semiconductor ratings. An ideal static model was developed together with an approximate dynamic model in Simulink. These models were used together with theory verification to determine the worst-case operating scenarios for all the semiconductor and passive components, respectively. The converter components were then dimensioned correspondingly.

1700V SiC MOSFETs and SiC Schottky diodes provided by Wolfspeed was found adequate for the application allowing 100kHz operation. Semiconductor DP testing in LTspice was found to provide too optimistic results, and datasheets were therefore used for dimensioning. Comparable market-available Si options were found to be disadvantageous. Rough efficiency estimations based on datasheets were also carried out. A suitable capacitor was found in the datasheets, while it was necessary to develop an inductor algorithm to acquire inductor information. A proposed algorithm was created based on ferrite 3F3 and Litz wire for 100kHz application providing weight, volume, and ESR. Liquid coolers were also found assuming the possibility to tap in on a 40°C internal cooling system in the ferry. Liquid cooler datasheets verified that the components fulfilled the specified thermal restrictions.

Finally, the total weight, volume, and efficiency of the converter were determined. Including IP67 casing, the weight and volume were 319.2kg and 180liter respectively, while the lowest efficiency was 98.2%. Furthermore, the maximum current ripple was 2.56% during 8.3% rated operating power. Comparison with both a conventional 100kHz boost converter and a 5kHz corresponding IBC converter showed that both these solutions would lead to weight around

3tons. This indicates that the combination of high-frequency components and IBC utilization is necessary to keep an adequate converter weight under the assumptions given in this thesis.

SAMMENDRAG

I denne avhandlingen ble en undersøkelse av en 200kW SiC-basert 6-fase IBC gjennomført. Bus-spenningen på 1kV ble forskynt med energi av seriekoblede FC stacks med en spenningsvarianse fra 520-900V.

Høy vekt og volum er genrelt problematisk for alle kjøretøyapplikasjoner. Brenselceller har i tillegg svært lav strømrippeltoleranse, noe som gjør lav vekt og volum av omformeren vanskelig å realisere. Innledende estimater basert på komponter tenkt for dagens fergeprosjekter viste en FC omformervekt på over ett ton. Et eventuelt kriterium om galvanisk skille i omformeren vil gi ytterligere vekt og volumsøkninger i tillegg til økte kostnader. Flere intervjuer med industrien førte imidlertid til at en u-isolert topologi i kombinasjon med CM filtre ble regnet som det mest gunstige. Nettopp IBC-omformer topologien ble undersøkt basert på et litteraturstudie for den spesifikke fergeapplikasjonen. SiC halvledere ble benyttet ettersom de tillot betydelig vekt og volumsreduksjon i tillegg til å være godt egnet for IBC'ens spennings og strømnivåer.

Omformerens lastprofiler for høyhastighetsfergesambandet i Trondheim ble anslått basert på data fra Trondheim-Vanvikan distansen. FC atferd ble undersøkt basert på PowerCell Sweden's MS100 stacks og en omtrentlig 3-delt linearisering ble utviklet som en FC-approksimasjon. Denne kompenserte også for FC aldring. Videre ble IBC atferd for ulike antall faser undersøkt, og en 6-fase med part-load operasjon ble foreslått basert på de oppdagede lastprofilene og ratingene til halvlederne. En ideell statisk modell ble utviklet i tillegg til en omtrentlig dynamisk modell i Simulink. Disse modellene ble brukt sammen med verifiserende teori for å bestemme worst-case driftscenarier for alle halvleder- og passive komponenter. Komponentene ble deretter dimensjonert etter disse driftscenariene.

1700V SiC MOSFET'er og SiC Schottky dioder levert av Wolfspeed var de mest gunstige komponentene på markedet, og tillatte 100kHz drift. Halvleder DP testing i LTspice viste seg å gi for optimistiske resultater, så datablader ble derfor brukt for dimensjonering. Sammenlignbare Si-alternativer funnet på markedet viste seg å være utilistrekkelige. Det ble utført grove beregninger av virkningsgrad basert på datablader. En passende kondensator ble funnet via datablader, og det ble utviklet en spole-algoritme for å kunne gjøre estimeringer av spoleparametere. Den foreslåtte algoritmen ble laget basert på Ferrite 3F3 og Litz wire for 100kHz. Algoritmen returnerer vekt, volum og ESR. Liquid coolers ble også funnet under antakelse av et 40°C intern kjølesystem i fergen. Dette ble brukt til å verifisere at komponentene oppfyller termiske restriksjoner.

Til slutt ble totalvekt, volum og virkningsgrad av omformeren bestemt. Inkludert IP67 casing var estimatene for henholdsvis vekt og volum 319.2 kg og 180liter, mens den laveste virkningsgraden for omformeren var 98.2%. Videre var maksimal strømrippel 2.56% under 8.3%

av rated omformerdrift. Sammenligning med både en konvensjonell 100kHz boost omformer og en 5kHz tilsvarende IBC omformer viste at begge disse løsningene vil føre til en vekt rundt 3 ton. Dette viser at både komponenter som kan operere under høy frekvens og IBC struktur bør taes i bruk for å oppnå en rimelig omformervekt og volum under antakelsene gjort i denne avhandlingen.

PREFACE

This TET4900 NTNU MSc is done in collaboration with IFE on the investigation of a converter suitable for hydrogen ferry applications during spring 2019. It is based on suitable converter topologies discovered during the literature search specialization project during fall 2018. To quote the thesis description, this thesis was experienced as “very challenging.” A good understanding of a wide range of topics had to be attained to deliver a satisfactory thesis. As the scope was broad and attainable literature and knowledge often scarce, the hardest part with this thesis was to make reasonable assumptions. Luckily, I was not alone. I want to direct a big thanks to my two supervisors, Fredrik and Dimosthenis, for providing me with excellent help and guidance whenever I needed it. I also want to extend a big thanks to the student advisor Kristoffer, friends, and family for supporting me and helping me structure my life through this challenging time.

24.6.2019, Oslo
Håkon Magne Bye

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ABBREVIATIONS

AC - Alternating current

AVRG - Average

BC - Boost Converter

BOL	Beginning Of Life
CCM	Continuous Conduction Mode
CICM	Continuous Inductor Conduction Mode
CM	Common Mode
DC	Direct current
DICM	Discontinuous Inductor Conduction Mode
DP	Double pulse
EMI	Electro-Magnetic Interference
EOL	End Of Life
ESR	Equal Series Resistance
EV	Electric Vehicles (often used about battery-electric vehicles)
FC	Fuel Cell
FIC	Full bridge Isolated Converter
GaN	Gallium Nitride
GWP	Global Warming Potential
HF	High Frequency
IV	current versus voltage
LF	Low Frequency
MMF	MagnetoMotive Force
PEM	Proton Exchange Membrane
PEMFC	Proton Exchange Membrane Fuel Cell
ph	phase
PN	Positive doped, Negative doped
PWM	Pulse Width Modulation
RMS	Root Mean Square

SC - Short Circuit

Si - Silicon

SiC - Silicon Carbide

SoC - State of Charge

WBG - Wide BandGap

x-ph - x number of phases

1 INTRODUCTION

1.1 BACKGROUND AND MOTIVATION

The threat of global warming and negative pollution-based impacts needs to be addressed by the word society to ensure a worthy future for the coming generations and the earth as a whole. Several countries are setting themselves ambitious climate goals, amongst them Norway. Norway's energy demand is entirely covered by hydro plants, making its energy supply 100% renewable. This makes green transport solutions such as battery and hydrolysis-produced hydrogen highly very efficient in terms of GWP reduction potential. The three major emission sectors in Norway are Transport, Petroleum production, and industry [1]. Emission reduction in the transport sector is especially feasible due to the availability of green options. Consequently, Norway has set itself a goal of a 35-40% cut in emissions by 2030 [2]. Furthermore, resolutions are stating that all new vehicles should utilize zero emission alternatives as soon as the technology allows it [3].

The latter political incentives have already led to Norway being the country in the world with the highest number of EV's per capita by far [4]. Great progress is also being made in other sectors such as maritime transport where over 70 new battery or hydrogen-powered ferries will be in operation by 2022 [5]. Maritime transport in Norway is a major sector to address, as it is responsible for around 9% of the transport emissions [6]. A large fraction of these is caused by high-speed ferries, which is one of the most emission-intensive means of transport per passenger. Electrification of high-speed ferries is more complicated than other forms of traffic, as the ferry is highly weight-sensitive and often require high power storage capacity. This makes the use of battery impossible in certain cases, such as the Trondheim ferry connection [3], [7], [8].

Consequently, hydrogen utilization is the only viable emission-free option, and set strict requirements for the rest of the ferry in terms of weight. Especially the electrical system in a hydrogen ferry needs to be addressed for weight minimization. This is due to mainly two reasons which will be elaborated in later sections. Firstly, the voltage-variable behavior of a fuel cell and its inability to flow reversible power results in need of additional converters compared to battery alternatives. Secondly, fuel cells sensibility to current ripple requires sophisticated converter technologies to achieve an adequate fuel cell converter weight. It is this fuel cell converter that will be investigated in this thesis, mainly in terms of weight but also in terms of efficiency and volume.

Hydrogen powered ferries are not a topic that is yet thoroughly investigated. It is difficult, and many uncertainties exist. It is, however, the only solution that per now is considered viable for electrification of lightweight applications with high power-capacity demand [3], [7], [8]. Building competence here can also be transferable to long-distance air traffic where electrification per now is a distant dream. Norway is a wealthy, highly developed country with substantial marine and electrical competence due to the petroleum industry and being a maritime nation. It is well suited to lead this development.

1.2 OBJECTIVES

The objectives of this thesis are a continuation of the specialization project written in fall 2018. During the specialization project, it was found that the IBC topology was the most suitable topology and that three-phase bridge topologies were the most suitable if galvanic isolation was a requirement. Hence, the following objectives were set for the master thesis:

- Conclude on a converter topology by determining whether galvanic isolation typically is a requirement or advantageous.
- Electrical dimensioning of the power electronic converter.
- Optimization study of the converter in terms of efficiency, volume, and weight.
- Modelling and simulation of the complete system in Simulink under various load profiles.

1.3 METHOD

The first part of this thesis is theory and preliminaries required in addition to basic power electronics to understand why exactly a SiC-based IBC is investigated for the given hydrogen high-speed ferry application. This is done through the utilization of knowledge acquired in the specialization project, and a more specific and thorough literature study on the areas of significance. Further, the different electrical operating conditions are discovered by investigation of existing ferry data and fuel cell behavior based on the information found in the PowerCell Sweden MS100 datasheet. From here MATLAB calculations based on theory and an Ideal Simulink model is used to investigate the IBC behavior. Both methods provide equal results but have a different approach. They are both used whenever possible to verify the results as there are few other comparable references in literature.

LTspice was used in an attempt to dimension semiconductors thermally but found insufficient. Thermal and electrical dimensioning is therefore done manually based on datasheets. The capacitor is dimensioned by comparing simulation results with available datasheets. No comparable components were available for the inductors and, consequently, a design algorithm was created. The current ripple constraint played a key role in weight and volume of the converters. The current ripple constraint was not absolute, but necessary at the majority of the time for fuel cell lifetime. As the steady-state load profiles was found dimensioning, the converter was dimensioned from the steady-state load profiles under the given current ripple constraint.

1.4 SCOPE

The goal of this thesis was not to design all steps in a buildable converter, but to do a possibility study and hopefully a strong foundation for further work. The reason was that the available literature comparable for the application is scarce or non-existing. Hence, the scope was to investigate the feasibility of such a converter with an ideal Simulink model. Furthermore, dimensioning was part of the scope, and estimations in terms of weight, volume, and efficiency was carried out based on existing or realistic components to give an estimate. The IBC, in general, was investigated without any specified number of phases. The coupled IBC and soft switched IBC was omitted in the scope to keep adequate complexity. DICM analysis is omitted as it does not occur in other cases than the start-up of the converter. The investigation of the start-up was considered out of scope as this would require a more advanced FC model. The semiconductor material was also unspecified, but SiC was an area of interest. The converter rating was determined to be 200kW based on two series-stacked market-available fuel cells from the producer PowerCell Sweden in collaboration with IFE and NTNU. Practical experiments were not part of the scope. Hence all behavior caused by non-idealities such as EMI was not in the scope in terms of analysis. Neither was the control system of the converter and the remaining system around the converter. Still, these topics had to be discussed to determine the viability of the system. The main weight of this thesis was put into dimensioning and optimization of the converter.

1.5 STRUCTURE

Chapter 2: Theory and other preliminaries from the specialization project relevant to the thesis are briefly summarized. This includes FC, IBC, galvanic isolation, and SiC theory. A further literature study is also carried out on advanced IBC behavior and CM noise. Also, results from interviews with the industry regarding the CM problematic of this thesis is elaborated.

Chapter 3: The load profile of an actual high-speed ferry application in Trondheim is investigated together with the datasheets of PowerCell Sweden's MS100 FC stack. Thus, the electrical parameters and various load profiles for the converter are determined. Also, the number of phases is decided, and a part-load scheme for the converter is developed.

Chapter 4: The ideal static Simulink model used for dimensioning is developed. An approximate dynamic model is used to confirm that the static load operations are dimensioning, and realization of a complete dynamic model is discussed. A part-load logic structure based on "if" statements are proposed.

Chapter 5: Market-available suitable semiconductor components are found in this chapter. For SiC components DP testing in LTspice provides too optimistic results, and datasheet values are used for the thermal dimensioning. Si options are investigated and found insufficient. Loss calculations are executed on the SiC components based on rough calculations.

Chapter 6: The inductor and capacitor are dimensioned based on theory and simulation results. A suitable capacitor is found via datasheets. A high-frequency inductor algorithm is developed and used to determine inductor parameters.

Chapter 7: The cooling system for the ferry is discussed. Suitable liquid coolers are proposed

Chapter 8: The final results in terms of weight, volume, and efficiency is presented for the converter. The results, in addition to other possible assumptions and converter variations for the thesis, is discussed.

2 THEORY AND PRELIMINARIES

2.1 FUEL CELL OPERATION

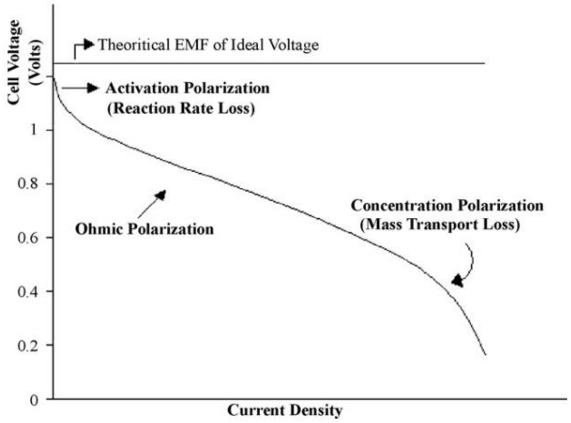

Figure 2.1: The IV curve of a PEM fuel cell [9].

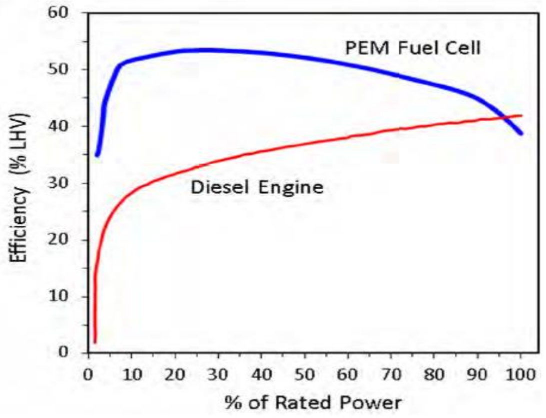

Figure 2.2. The efficiency curve of a PEM fuel cell and a typical diesel engine used in maritime applications [7].

As shown in Figure 2.1. FCs have an output voltage that varies significantly with different power ratings [9]. Thus, many applications require a DC-DC converter for more stable voltage output. FCs are also considered current intensive sources, and especially step-up converter topologies are therefore relevant for FC applications [10], [11]. Looking at Figure 2.2, one can observe that the efficiency of the FC is sinking drastically for very low and very high rating operation. This does not only create additional losses, but in particular, very low rating operation can be damaging to the cell and contribute to faster aging [12]. This is why producers such as PowerCell Sweden recommend a minimum operating current to guarantee a certain lifetime [13]. There are other important FC properties that need to be addressed when utilizing an FC.

Ripple in current and voltage, drawn harmonics and EMI does also contribute to aging in the FC. EMI can also interfere with the internal FC control system according to industry. Especially current ripple is considered crucial [7], [14], [15]. The higher the ripple frequency, the less impact on the cell [10], [16]. PowerCell Sweden recommends less than 2% current frequencies above 1kHz, but the ripple requirement becomes less strict for increased frequency. A capacitor on the input is not considered desirable in FC applications. This is due to the internal capacitive effect of FC [17].

FCs used in automotive applications are also typically not able to flow bidirectional power [18], [19]. The FC cannot handle the rapid increase in power either. The latter can lead to disturbance in the water balance of the cell and oxygen or hydrogen starvation and contribute to aging. Consequences are the cell being unable to deliver the required power and use minutes to recover or, in the worst case, suffer permanent damage [20]–[22]. This is the reason why hybrid systems with FCs and a small battery are typically used in automotive applications where quick power transients are required [19], [23], [24]. Several hybrid systems can be considered [10], [11]. In collaboration with research facilities, the system shown in Figure 2.3 will be used in this thesis. Two identical power systems are divided over two hulls assuming a catamaran ferry. Circuit breakers are applied to disconnect one hull electrical system in case of faults. Having divided the power from FCs over 6 converters, no further redundancy design in the converters are required. A separate converter between the bus and the batteries ensures a constant DC-bus voltage and allows shaping of the load curve the FC stacks must supply.

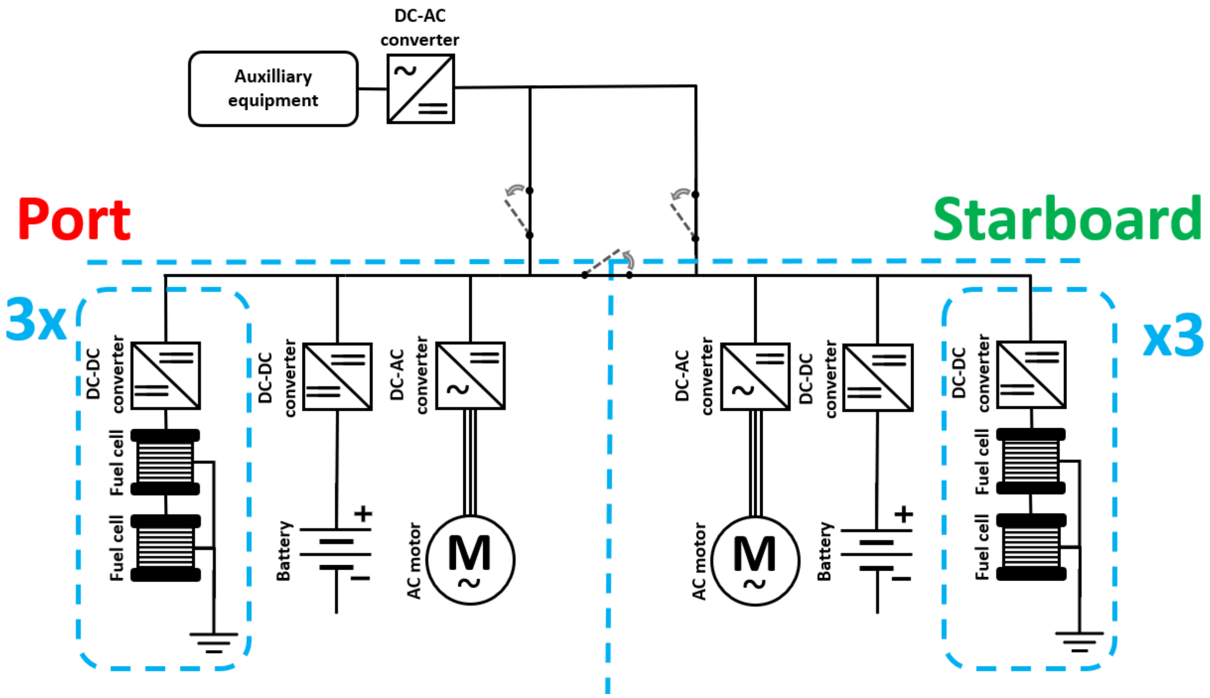

Figure 2.3: The electrical system layout for the hydrogen-powered ferry

2.2 WEIGHT REFERENCES

Table 2-1 shows rough weight estimations of different comparative propulsion systems, including the electrical system shown in Figure 2.3. The power requirement of 1.2MW and hydrogen storage of 450kg was determined in collaboration with research facilities to mimic a future system. Table 2-1 is based on previous estimations in the two following reports [3], [7] and specific datasheets. Simple energy calculations were also done to determine the required storage capacity for the different systems. The weight estimations are only meant to illustrate the weight magnitude. Due to, inter alia, uncertainties in hydrogen piping and miscellaneous electrical components, the actual weight may vary with several tons [7].

Table 2-1 clearly shows the unfeasibility of battery implementation in the given scenario regarding weight. It also shows that a hydrogen system is slightly heavier but comparable to an existing diesel system. Furthermore, it shows that the power electronics make up 2.7 of the 13.3-ton system, which equals 20%. The weight estimations done on the power electronics are based on ABB's HES880 module that is assumed for actual hydrogen ferry projects [25], [26]. Weight reduction of power electronics are therefore beneficial and can have a significant impact on the total weight of the ferry.

Table 2-1: Weight estimations of different energy systems for maritime vessels.

Component	**Specifications**	**Weight [kg]** **Hydrogen system**	**Weight [kg]** **Comparative Diesel system**	**Weight [kg]** **Comparative Battery system**
Engine	2x600kW	1900 [3]	7000+1200 [3]	1900 [3]
Inverter ABB HES880	2x600kW	560 [26], [27]	-	560 [26], [27]
DC-DC battery converter ABB HES880	2x600kW	560 [26], [27]	-	-
DC-DC FC converter ABB HES880	6*200kW	1546 [26], [27]	-	-
Battery	1000V	425 [7]	-	49500 [30]
PEMFC, PowerCell Sweden MS100	12*100kW	1800 [13]	-	-

DC link	1000V	600 [7]	-	600 [7]
Fuel	450kg h2	450	1500	-
Fuel tank	16, Hexagon	5472 [28]	725 [29]	-
sum		**13313**	**10425**	**52560**

2.3 SiC SEMICONDUCTORS

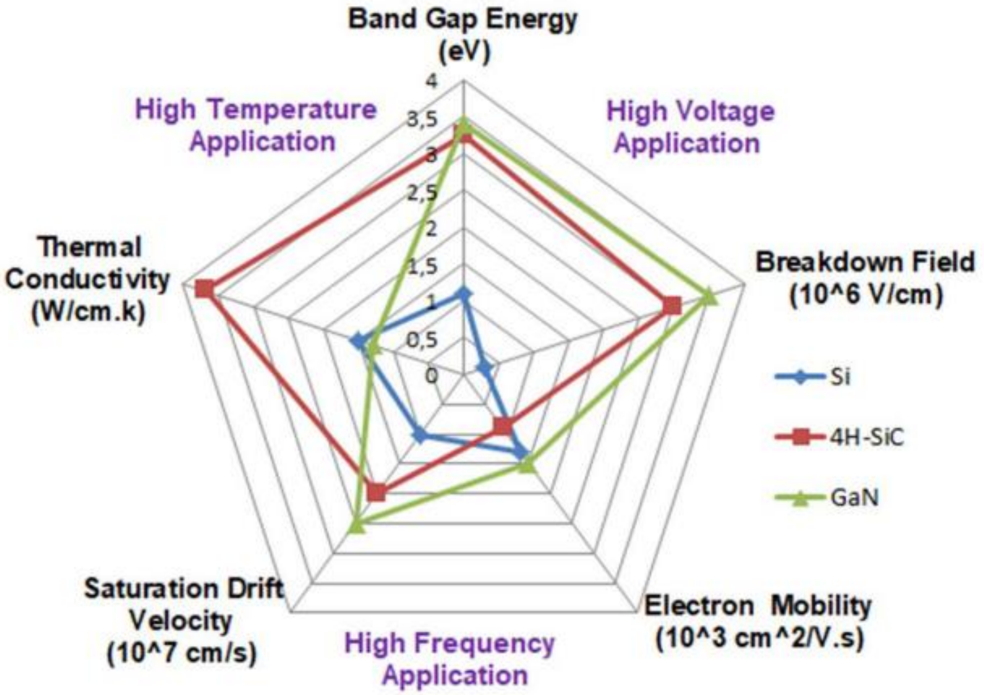

Figure 2.4: Comparison between different properties of Si, SiC and GaN [27].

SiC and GaN are two WBG materials. The key with these materials is superior material properties compared to Si for high voltage, high temperature, and high-frequency operation, as shown in Figure 2.4. These materials are harder to produce and have traditionally been quite expensive, with instability issues in the resulting components [27]–[29]. A recent development is a cause for especially SiC components now starting to penetrate the market [27], [29]. Due to high frequency, high-temperature operation feasibility, and high efficiency, these components allow the passive component and cooling system size reduction. Therefore, they are considered advantageous for lightweight applications such as the automotive industry [30], [31].

For vehicle applications around 200kW, SiC-based power electronics are common in literature [32], [33]. The biggest drawback from SiC utilization is the fast switching transients. This generally leads to increased EMI production in the system. A more advanced gate driver is also required to compensate for instability caused by fast switching in combination with parasitic components [34], [35]. One of the most common SiC component utilization in converters per now is the MOSFET in combination with the Schottky diode. Both these components have relatively poor current capabilities and are, therefore, typically used in multi-leg topologies [36], [37]. Both the Schottky and the MOSFET are available in 1700V ratings, and considered easy to parallel [38], [39].

2.4 GALVANIC ISOLATION

Whether galvanic isolation is required or not for the DC-DC FC conditioner is somewhat an open question. Advantages of galvanic isolation come mainly in terms of reduction of CM interference on the FC stack but also increased safety for human contact and components. It can also be necessary for high step-up ratios. The drawbacks with the galvanic isolation come mainly in terms of cost, especially for SiC, as it at least doubles the number of semiconductor devices needed without reducing the rating requirements significantly. It also adds additional losses, weight, and volume. The complete list of advantages and drawbacks are listed in Table 2-2.

Table 2-2: The advantages and drawbacks with galvanic isolation in terms of a transformer [10], [11], [40].

Advantages galvanic isolation	Drawbacks galvanic isolation
• Reducing CM [41] o Using a shielded transformer reduces CM further [41] • Increases Safety for human interaction in case of fault [42] • Increases safety of components in case of fault [10] • Allows a variable step-up ratio [10], [11]	• Cost [10], [11] o Of the transformer o At least twice as many semiconductor components in relevant topologies, inter alia, for BC and IBC compared to FIC and V6. This is due to bidirectional use of transformer core and clamping [10], [40]. ▪ Most components cannot have decreased rating [10] ▪ Add a major cost with SiC components [29], [43] • Leakage inductance [11], [42] o Harder to achieve high-frequency switching operation o Increase need for clamping circuit • Increased losses [10], [11] o Conduction losses in the transformer o Losses in the required extra components

- Increased weight, volume [10], [11]
    - Weight of the transformer
    - Weight of a bigger cooling system
- Increased complexity [10], [11]

As there exists little published research on the area, the need for galvanic isolation was discussed with several representatives from the following industry and research facilities: DNVGL, ABB, Siemens, PowerCell Sweden, and Clean Marine Switchboards. Unreferenced statements in this section are based on these discussions. All companies agreed that galvanic isolation is not a requirement. All but one of these companies did also believe that a converter without galvanic isolation would be most favorable. Galvanic isolation offers advantages, but these advantages were not strictly required or more easily replaced by simpler measures.

The ABB HES880 used in at least two future hydrogen ferries is a non-isolated topology. Another good sign is that the FC producer company Hydrogenics has purchased this converter, assumingly for testing. Furthermore, battery-powered and diesel-powered ferries does not have galvanic isolation implemented in their DC-DC converters today. For example, the fully electrical MF AMPERE do not have galvanic isolation [44]. Neither do the molten carbonate fuel cell powered Viking Lady [45]. The only common place to implement galvanic isolation is in the inverters to the lower rated electronic components connected to the bus. There is, however, one important difference between PEMFC and diesel or battery systems. While the latter systems can be floating, the PEMFC stack must be grounded. In the case of floating system, static buildup might cause sparks that can ignite potential gas leaks and, hence, create an explosive hazard. Grounding the FC makes it more prone to the generated CM in the circuit [46], [47].

2.4.1 Common Mode noise

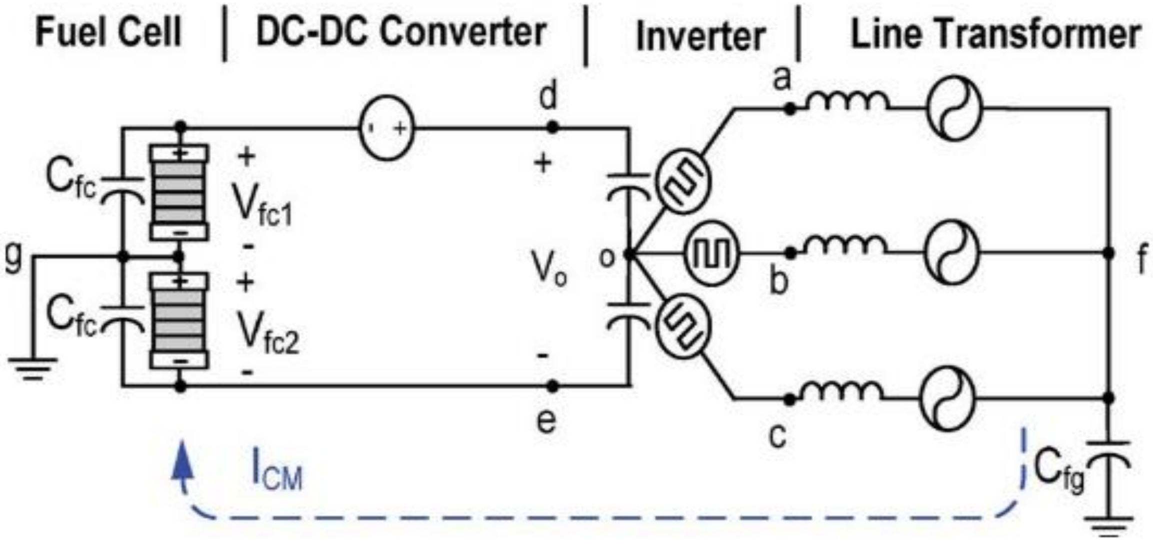

Figure 2.5: A typical common mode path to fuel cell stacks from a transformer or motor with stray capacitance from its neutral point to ground [41].

Figure 2.5 shows how the CM current is typically flowing in an electrical fuel cell system. The CM is here referring to voltage and current generated due switching paths to neutral points that are supposed to be floating but in reality, have a stray capacitance to ground. The most common examples are the neutral points in a transformer or a motor [46], [48]. In the given electrical system, the main CM generation is expected to be from the motor, but also wiring and the DC-busbars, generally everything with a big conductive surface will generate CM. Generated by switching, CM noise is at the switching frequency. The CM currents are generated by the rapid change in voltage, and are therefore worse for devices with fast switching transients, inter alia, SiC components [46]. Figure 2.6 shows the typical CM waveforms that would correspond to Figure 2.5 and the proposed system for this thesis.

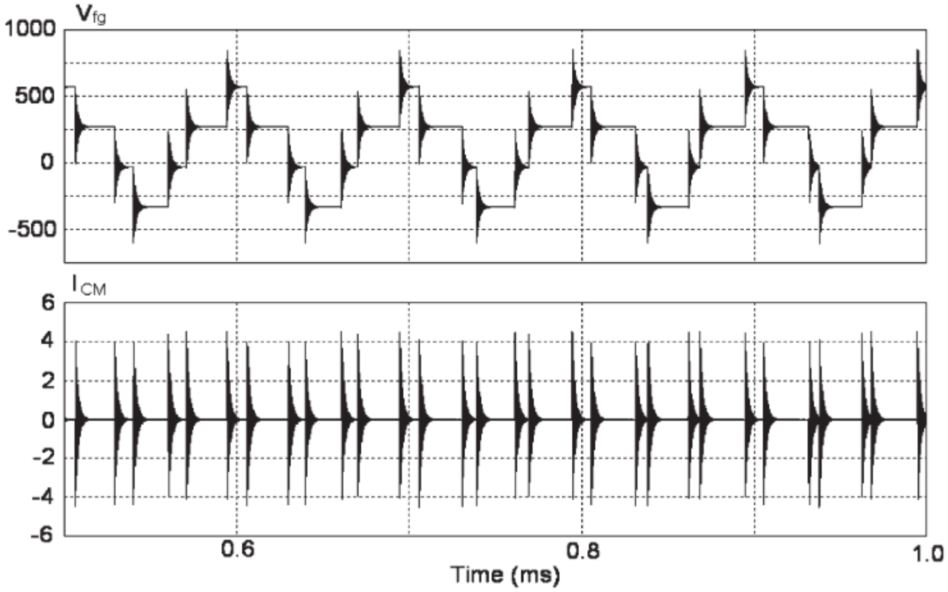

Figure 2.6: Typical CM waveforms generated by a transformer or a motor [41].

2.4.2 Common mode reduction techniques

Fuel cells are known to be sensitive to ripple, and the CM issue needs to be addressed [10], [16]. Several countermeasures can be implemented to reduce CM voltage. One obvious solution is to use galvanic isolation. By physically separating the circuits, you provide no current path for the CM to flow, and ideally, this would cancel the CM noise to the FC completely. There is, however, stray capacitance between the windings in the galvanic isolation, and CM would, therefore, flow even with a transformer. A shielded transformer can be implemented to reduce this capacitance further [41]. A simpler common countermeasure is a CM choke. This is inductors, typically on a common core, that is either between a positive and negative terminal or a three-phase configuration. These inductors designed specifically for filtering away CM noise and other HF EMI [49], [50].

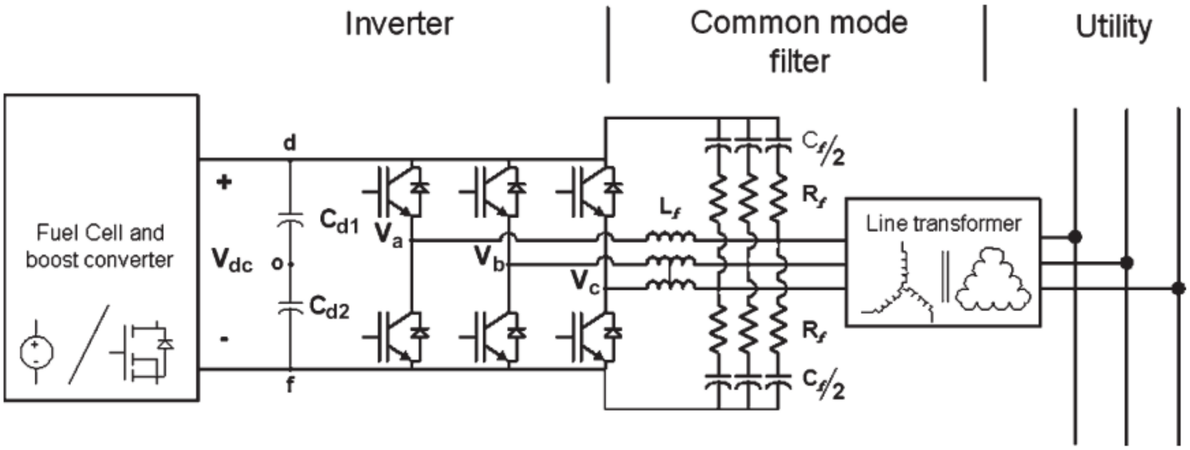

Figure 2.7: Implementation of a CM filter to compensate for the CM generated in a transformer [41].

For SiC frequency operation CM-chokes must be of significant size and weight [49]. Capacitive filters are also common for marine electrical applications. These capacitors should provide a low impedance path for the high-frequency CM current to flow and can be used to lead the CM current away from the FC [41]. As the DC-choke, they can either be in single-phase, or in 3-phase configuration as shown in Figure 2.7. The industry suggests capacitors could also be added in the ground connections to reduce CM noise further. Resistors should then be implemented in series or parallel with the capacitors to prevent static buildup. The capacitor CM filters work better with higher frequencies than galvanic isolation and CM-chokes. These filters are therefore expected to be effective for SiC switching frequencies [41].

A combination of CM-chokes and capacitive filters could also be feasible as discussed for a 200kHz SiC motor drive [49]. There are also several control techniques of the motor drive that can contribute to reduced CM [48], [51]. CM component dimensioning is not done in this thesis, as the CM generated is heavily dependent on the practical condition and not considered viable to anticipate. This is, however, an important design consideration for the given ferry system and a very interesting topic for further work.

2.4.3 Non-isolated topology justification

In addition to all aforementioned measures to reduce CM for the FC, how the FC is grounded is important to consider. In Figure 2.5, the FC is grounded directly through one of its terminals. However, producers such as PowerCell Sweden do now offer their FC stacks with series connection opportunities, implying the ground port electrically isolated from the terminals. It would not be possible to connect more than 2 FCs in series if this is not the case. This reduces the negative impact of CM significantly. Also, if required, improved FC stacks less prone to CM noise by increased isolation levels and a more EMI robust internal control system is likely to be developed. Since it is possible to series-connect the PEMFC stacks, there is no need for a variable step-up ratio. The industry does not consider the damage potential in case of faults to be compromised by not implementing galvanic isolation. Strict safety regulations of electrical systems onboard ships already implement safety in terms of fuses and monitoring equipment. The diode in the typically implemented converters are preventing reversible power flow. The personal safety would not be compromised, as only trained personnel should have access to the electrical components. It is, however, important to choose a fault detection system that is designed to not trigger on CM noise.

To summarize, galvanic isolation advantages in terms of human safety, component safety and variable step-up ratio are considered to have a small impact on the given ferry system. Galvanic isolation would prove to be advantageous in terms of CM noise reduction. However, the common opinion from both industry and research facilities is that galvanic isolation is unnecessary. Especially regarding the disadvantages for SiC applications listed in Table 2-2. Dimensioning appropriate CM reduction filters are expected to be more advantageous than galvanic isolation for CM reduction. Non-isolated FC converter topologies should also prove favorable in terms of transferability from existing diesel-electric and battery vessel systems that per now use non-isolated converter topologies. Further improvement in FC production is expected to make the FC more durable to CM noise, according to the industry. Therefore, this master's thesis will focus on the non-isolated converter considered most suitable, namely the interleaved boost converter. It should, however, be noted that investigating an isolated DC-DC converter could be interesting. New planar transformers are becoming available for the specified power range, and their weight and volume seems to be impressively low [52], [53].

2.5 DESIRED CONVERTER PROPERTIES

Table 2-3 lists the desired properties of the DC-DC converter connected to the FC stack for a hydrogen-powered high-speed ferry shown in Figure 2.3. Several of the properties are based on the FC operation principles discussed in 2.1. Other properties such as weight, safety, and reliability are important because of the transport application. Especially lightweight is considered important. Especially SiC semiconductor utilization can offer high-frequency operation and therefore, considerable weight reductions of passive components in the converter and converter cooling system [29], [54], [55]. Finally, ratings, ripple, and ramp rates have been determined in collaboration with research facilities and the fuel cell producer PowerCell Sweden based on their MS100 module [13].

Table 2-3: Important design considerations for an FC converter used in a high-speed ferry.

Desired property	Design aspects

Unidirectional power flow	• Unidirectional compared to a bidirectional topology: o Reduces cost, complexity, and losses [56]. o Prohibits reversible power flow and damage of cells in case of a fault [18], [19].
Power rating = 200kW Input voltage range =[500-1000V] Output voltage range=1kV Max and nominal current, @500V = 350A Minimum static current for FC health =20A	• High power makes the simplest topologies undesirable [10]. • High current per voltage [11]. o Implies high levels of EMI [57]. Soft switching that avoids fast transients in current and voltage is desired to reduce EMI [58]. o Current sharing between legs is feasible by interleaving or multi-phase topologies [10], [11]. Especially for accessible SiC components [59], [60]. o The current ripple in the converter has a big impact on the losses [56]. • Comparable voltage levels remove the necessity of step-up transformer [10].
Low ripple at FC end Current Ripple above 1kHz should be below 2% [13].	• Current fed topologies are feasible [10], [18]. o Voltage clamping circuitry at the supply end may be required [61]. • Interleaved and multi-phase structures contribute to reduced input ripple per inductance [11], [62]. o Reduces need of clamping [11], [63]. High-frequency switching reduces ripple per inductance [64]. • A capacitor on input is not viable. This is due to the internal capacitive effect of FC [17].
Low harmonic and EMI generation for FC	• Low input ripple contributes to reduced EMI and harmonic production [15], [65]. • SiC components reduce harmonic production but increase CM and other EMI generation [49], [66]. • EMI and harmonics reducing PWM techniques can be implemented [67]. • Filters, chokes, and galvanic isolation can be implemented in the electrical system to reduce EMI and harmonics experienced for the FC [45], [46], [49], [68].

	• Soft switching through resonance parts or clamping reduces EMI and harmonics [69], [70]. • Interleaving and close magnetic couplings increase EMI experienced for the FC [67].
Ramp up power with 10% per second Ramp down power quickly Stable but varying power requirements	• Slow ramp up response from FC gives no restrictions for converter • Possibility for instantaneous power ramp down for FC makes rapid ramp down response for FC feasible, at least for the low rating section to avoid aging [12]. o High frequency and simple control make rapid tuning realizable [56]. o Small passive components allow faster energy transitions [56]. • Stable but varying power requirements make the operation of converter in different operating modes viable to increase overall efficiency [10], [17].
High gravimetric and volumetric converter density Low weight and volume of the cooling system	• Simple structures contribute to low weight and volume [10], [11]. • High-frequency switching contributes to weight and volume minimization of the converter. This is realizable with SiC components [29], [54], [55]. • Interleaved and multi-phase inputs contribute to further weight reduction [11], [62], [71]. • Skipping galvanic isolation contributes to significant weight reduction [15]. • Size of the cooling system gets smaller with high efficiency [56].
High efficiency	• Small passive components, low ripple, and components with low switching loss contribute to high efficiency [56]. • Soft switching is feasible for low switching loss [14], [63], [64]. • Cooling system for the converter can be kept small, reducing weight [56]. • High power implies big losses with low efficiency.
Reliability and operational safety	• Reliability is mainly realized by keeping the power supply connected through several converters. • Low ripple at FC maintaining FC health [7], [14], [15]. • Isolation can be used to protect FC from motor overload conditions and faults [10], [72].

2.6 THE INTERLEAVED BOOST CONVERTER

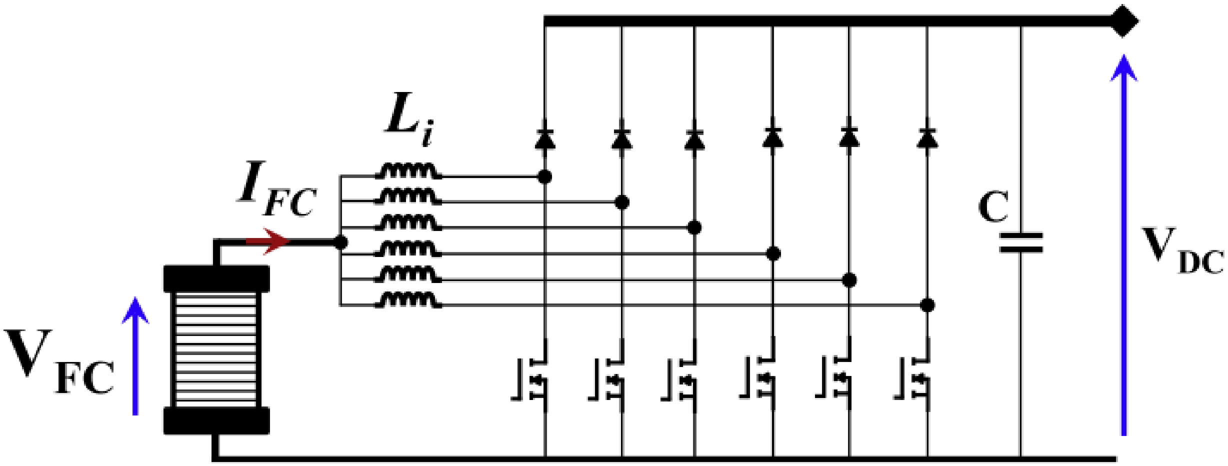

Figure 2.8. The architecture of a general 6-phase IBC [10].

The IBC is the preferred topology for this thesis offering desirable properties for the system investigated. It has high efficiency, relatively simple control strategy, leg current sharing, and superior ripple properties in terms of weight and volume [10], [15], [37]. Literature extensively reports this topology as the suitable choice for applications similar to this thesis [17], [36], [65], [73], [74]. The structure is equal to that of a conventional boost converter but with several sets of legs consisting of an inductor, a diode, and one switch. The number of legs used in IBCs is typically 2,3,4 or 6, where the latter is shown in Figure 2.8 [36], [62], [75].

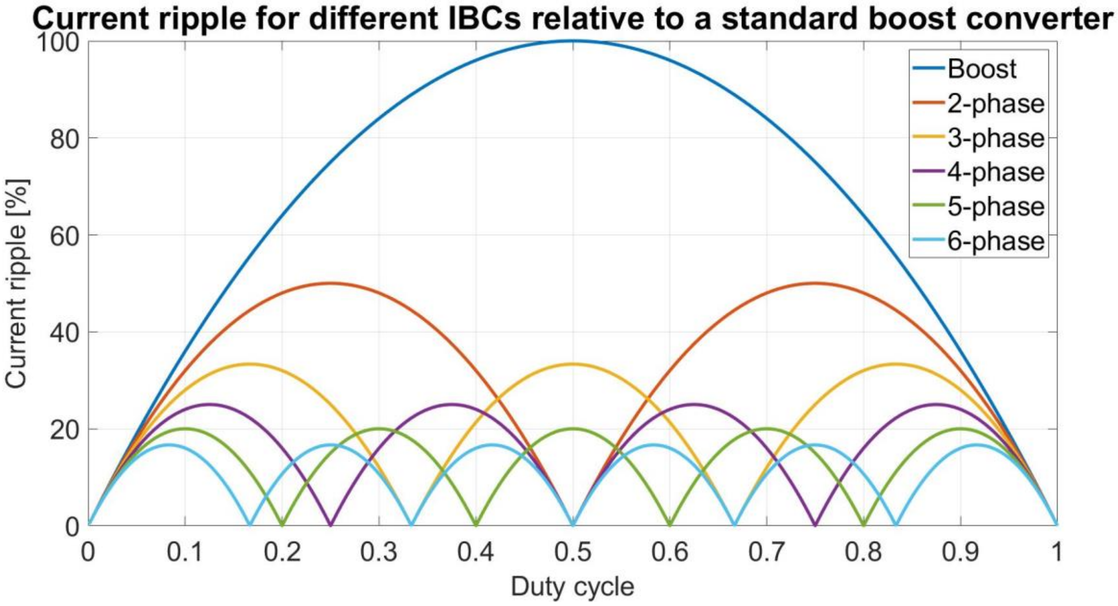

Figure 2.9: The current ripple magnitude as a function of the duty cycle for a different IBCs with the same phase inductance, assuming CICM and a constant output voltage.

The number of legs is an important design consideration that must be tailored for the specific application. The maximum ripple approximately halves when the number of phases doubles for the same phase inductance and current. Also, operating points with complete current ripple cancellation occur. These phenomena are illustrated in Figure 2.9. This plot is generated with Equation 4 in MATLAB using Appendix 1. As the total current is divided into all phases, a high number of phases feasible in terms of inductor weight reduction. Also, the output voltage ripple decreases with an increased number of phases, allowing capacitor size reduction [62], [76], [77]. Based on Equation 8, the voltage ripple for different phases is generated in MATLAB with Appendix 2. This is illustrated in Figure 2.10 for constant capacitance, capacitor voltage, and capacitor current. It is observable that the ripple reduction effect achieved by interleaving is very high.

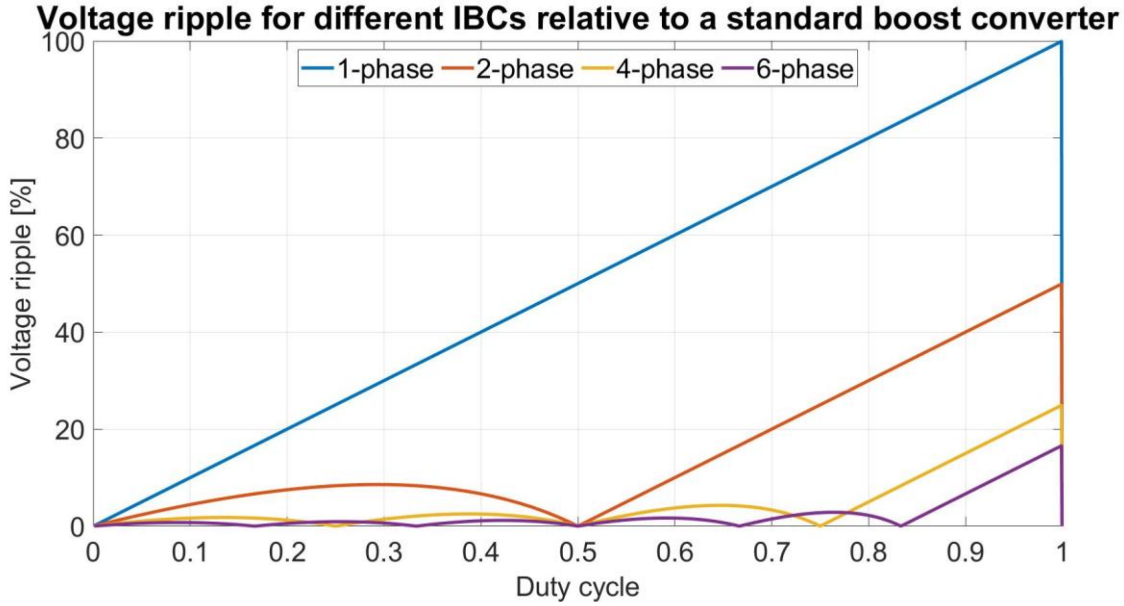

Figure 2.10: The voltage ripples for the even-numbered phases relative to a conventional BC with constant capacitor voltage and current.

2.6.1 Operating principle

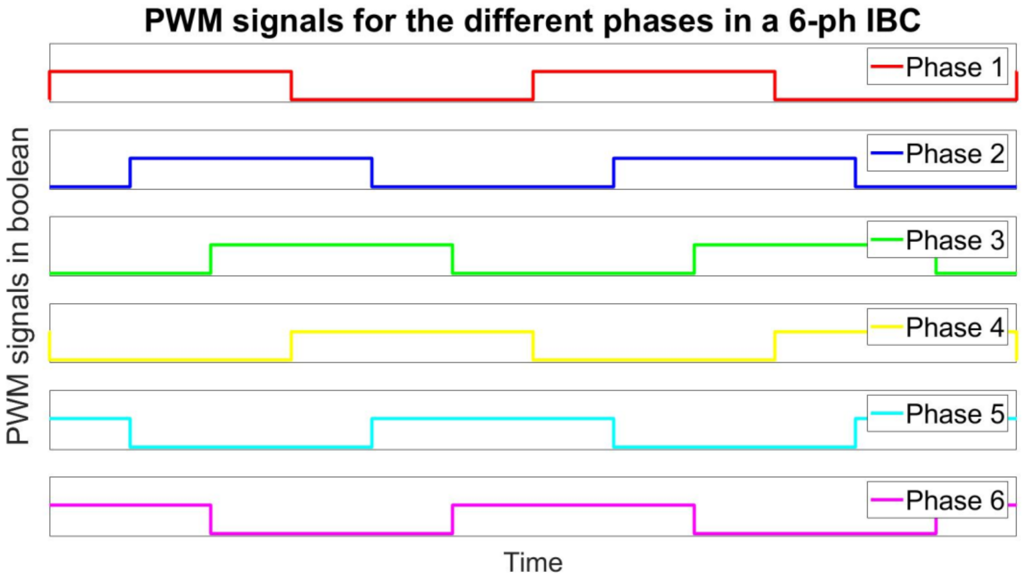

Figure 2.11: The PWM signal for control of a 6-ph IBC at duty cycle= 0.5

Figure 2.11 shows the typical control scheme for a 6-phase IBC generated from a static Simulink model that will be introduced in chapter 4. Figure 2.12 is generated in the same manner and shows the resulting currents. The general control concept of uncoupled IBCs is simple. All switches are applied to the same duty cycle, $D = \frac{T_{on}}{T_s}$ but the signal is applied to each switch with a phase shift equal to $\frac{T_s}{N}$ in respect to the former switch signal where N is the number of phases in the IBC. Consequently, the voltage gain is also equal to that of a boost converter, $V_{DC\ bus} = \frac{V_{FC}}{1-D}$ [62], [76], [78]. PI or PID control with voltage or voltage and current control are sometimes proposed for uncoupled topologies [76], [79], [80]. If exploiting magnetically coupled IBCs, a more advanced controller is desired to deal with non-linearities [81]. IBCs connected to FCs do typically have advanced control anyways due to the FC non-linear behavior [79], [82], [83]. Also, the control scheme and circuit analysis become more complex, with an increased number of phases [81], [84], [85].

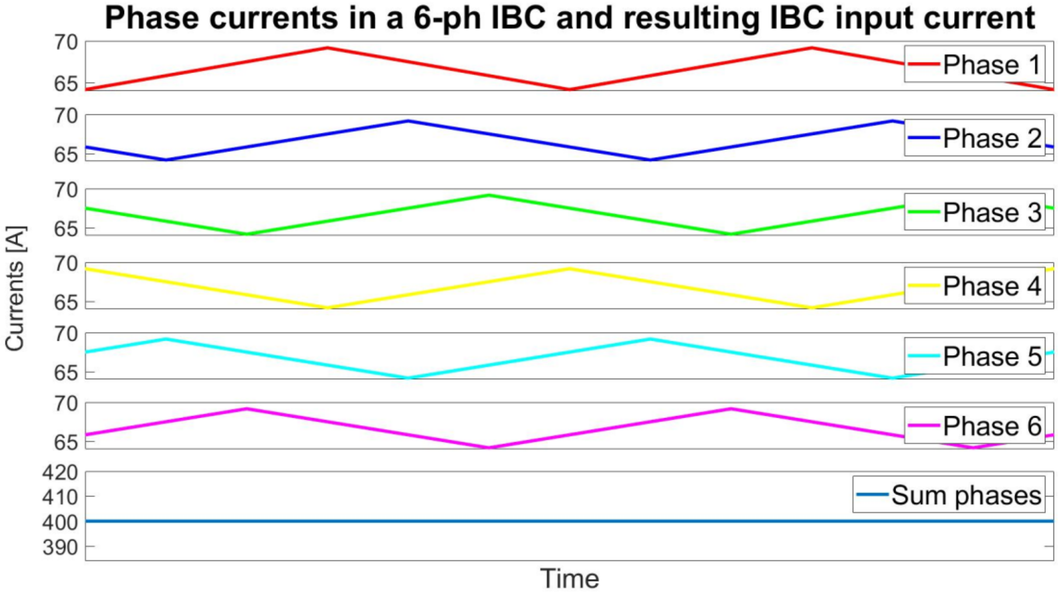

Figure 2.12: The resulting phase currents and total current for an arbitrary current using the PWM signaling shown in Figure 2.11, resulting in perfect ripple cancellation.

The input ripple for the current of an uncoupled IBC in CICM (Continuous Inductor Conduction Mode) with N, and, inter alia, 6 phases can be derived from [62], [76], [77]. The term CICM is introduced for IBCs as the total current can be in CCM even though the current through each of the inductors are not. N is here the number of phases. N_{on} are the number of phases that are conducting at the same time for a given D. d is the rise time of the FC current.

For one phase:
(boost converter)

$$\Delta i_{L,ph} = \frac{V_{FC} D T_s}{L_{ph}}$$

Equation 1

For FC in general with N phases:

$$\Delta i_{FC} = \sum_{j=1}^{N} \Delta i_{L,ph\,j}$$

Equation 2

For 6-phase IBC:

$$\Delta i_{FC} = \Delta i_{L,ph1} + \Delta i_{L,ph2} + \Delta i_{L,ph3} + \Delta i_{L,ph4} + \Delta i_{L,ph5} + \Delta i_{L,ph6}$$

Equation 3

For FC in general with N phases:

$$\Delta I_{FC} = \frac{V_{FC}}{L_{ph}} \left(\frac{N_{on} - ND}{1 - D} \right) \frac{T_s}{N} d$$

Equation 4

For a 6-phase IBC, this implies, inter alia, for $(0 \leq D \leq 0.5)$

$$\Delta I_{in} = \frac{V_{FC}}{L_{ph}} \left(\frac{1 - 6D}{1 - D} \right) \mathrm{T_s} D \qquad for \left(0 \leq D \leq \frac{1}{6} \right)$$

Equation 5

$$\Delta I_{in} = \frac{V_{FC}}{L_{ph}}\left(\frac{2-6D}{1-D}\right)T_s\left(D-\frac{1}{6}\right) for \left(\frac{1}{6} < D \leq \frac{2}{6}\right) \quad \text{Equation 6}$$

$$\Delta I_{in} = \frac{V_{FC}}{L_{ph}}\left(\frac{3-6D}{1-D}\right)T_s\left(D-\frac{2}{6}\right) for \left(\frac{2}{6} < D \leq \frac{3}{6}\right) \quad \text{Equation 7}$$

In the same manner, the CICM output voltage ripple can be derived. Here the DC bus must be modeled as a resistance, $R_{eq,bus}$, based on the power it's absorbing:

For a 6-phase IBC
general with N phases:

$$\Delta V_{bus} = \frac{V_{bus}T_s d(1-d)}{R_{eq,bus}C_{bus}N^2(1-D)} \quad \text{Equation 8}$$

Also, corresponding expressions for CICM-DICM boundary and DICM behavior are shown in the literature [62], [76], [77].

2.6.2 IBC design alternatives

Three phase inductors available on the market are typically magnetically coupled [86], [87]. Magnetic coupling between the inductors in the phases of IBCs is recurrently considered for automotive and FC applications, mainly due to the further weight reduction potential of the inductors [81], [84], [88]–[90]. The inductors can be coupled both directly and inversely, which provide different advantages. Direct coupling is considered especially feasible for FC applications as it contributes to lower FC current ripple and therefore less weight assuming a given ripple level [85], [88], [91]. It also contributes to lower AC core flux and therefore less core losses. On the downside, it creates higher inductor ripple and therefore, higher conduction losses.

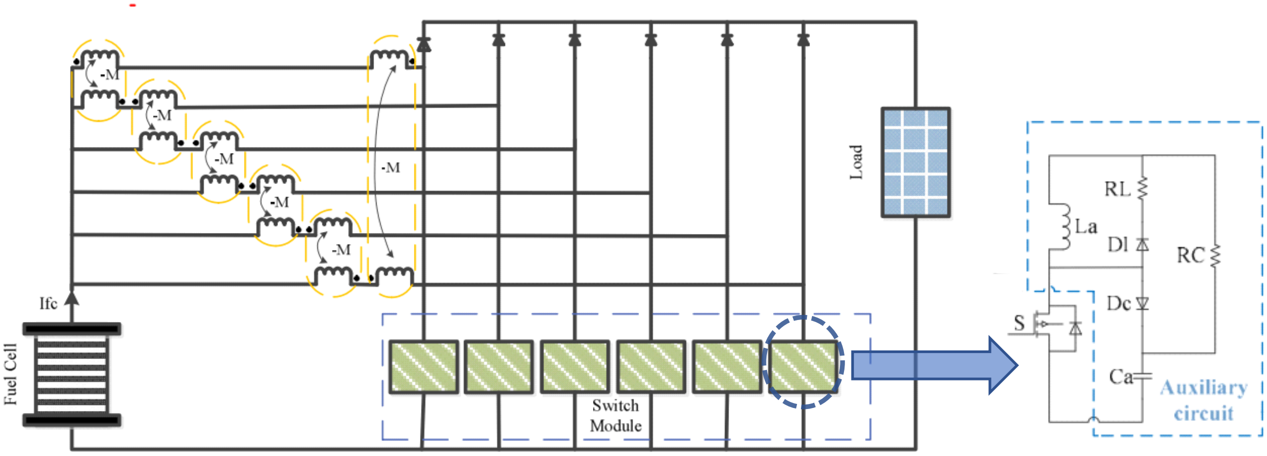

Figure 2.13: A 6-phase IBC with soft switching clamping circuit and one type of inverse coupling implementation [36], [81].

The inverse couplings main advantage is that it reduces the DC core drastically. An inverse coupling scheme for a 6-phase IBC is proposed in Figure 2.13. This allows significant weight and volume savings due to core size reduction. It also reduces conduction losses due to lower inductor ripple, but has higher core loss and input current ripple [85]. Other advantages of magnetic couplings, such as better steady-state and the transient response, have also been reported [75], [81]. EMI generation is, however, a bigger issue when utilizing magnetic coupling due to leakage inductance and significant stray capacitance, especially when utilizing SiC components [49], [67], [92].

Another IBC enhancement that could be implemented soft switching resonance capacitors or more advanced clamping circuits over the switches [10], [36], [81], [93]. An auxiliary circuit for soft switching is also shown in Figure 2.13. This allows the converter to be operated at high switching frequency without suffering unacceptable switching losses [56]. It will also decrease EMI due to smoother transitions. This does, however, add further complexity and operation constraints [56], [81]. To maintain a high efficiency over a wide load range, part-load operation control can be utilized. “Part-load operation” is to operate the converter with only some of the phases active. This can save losses at low operating power [10], [17]. More importantly, it allows the converter to transition between any “n” in Figure 2.9 smaller than the actual number of phases in the IBC. This can contribute to very low ripple over a wide duty cycle range for IBCs with a high number of phases [62].

3 CONVERTER LOAD PROFILES

During this chapter, static loads equivalent to full speed, maneuvering and docking is found. The electrical profiles of these loads are only dependent on fuel cell aging. For the rest of this thesis, the static load with a specific fuel cell aging refers to one distinctive electrical operating scenario found in Table 3-3 or with Figure 3.4. A static load with a specific duty cycle is also used. Both these determinations are valid for one specific operating scenario as it is found that only CICM occur during the scenarios investigated in this thesis.

3.1 THE POWER REQUIREMENT CURVE

Table 3-1: The power requirements of the ferry investigated in this thesis under different speeds.

Speed [knots]	Power requirement [kW]
0	100
20	800
25	1100
30	1700

To determine the load curve, the correlation of speed versus the power requirement must be determined. Table 3-1 is based on data from IFE and shows the correlation for a set of speeds. The correlation of speed versus power in a maritime vessel is a complex function, but can roughly be estimated as linear with the speed of the vessel squared [94], [95]. Thus, a second-degree polynomial curve fitting function in MATLAB could be used to approximate the load-speed curve. A second order polynomial curve fitting function alone was insufficient, but a second-degree polynomial divided by a first-degree polynomial provided quite realistic results. The curve is shown in Figure 3.1. From the given curve, the speed is 26.2knots at full power, 1200kW.

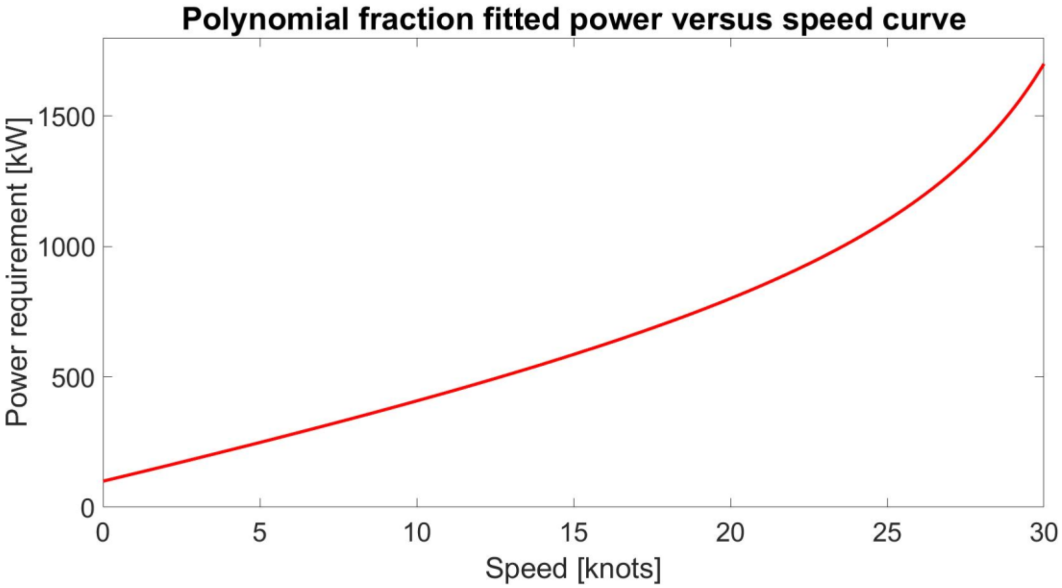

Figure 3.1: A curve fit for the load versus speed data provided for this thesis in Table 3-1.

3.2 CONVERTER LOAD CURVE

Table 3-2: The time spent operating at the different static loads during one FC load cycle.

Time [min]	Power requirement ferry [kW]	Power requirement per converter [kW]
10	100	17
5	250	42
15	1200	200

Further, the required speeds at the required distances can be estimated. Looking at an existing high-speed ferry that goes from Trondheim to Vanvikan, the time estimate of the travel is 25min [96]. The distance traveled is 15.5km according to map measurements. The vessel can manage that distance in 20min at 26.2knots with some margin, leaving about 2.5minutes at maneuvering and low speed at each dock. By inspection, the ferry spends less time than this maneuvering at the port in Trondheim, leaving a further margin.

Maneuvering power requirement is assumed equivalent to approximately 5knots forward speed. This equals 250kW, 21% of full power. Looking at the FC-breeze, maneuvering is 11% of full power, but this ferry is also designed for 35knots and much higher rated power [7]. Thus, the assumed 250kW maneuvering power is expected to be in the right magnitude. The static loads during a load cycle are summarized in Table 3-2. Otherwise, all acceleration and deceleration should be gentle to ensure comfort for the passengers. Recalling that the converter power from Table 2-3, the ferry load should be shared at 6 converters. Consequently, a converter load curve is proposed in Figure 3.2.

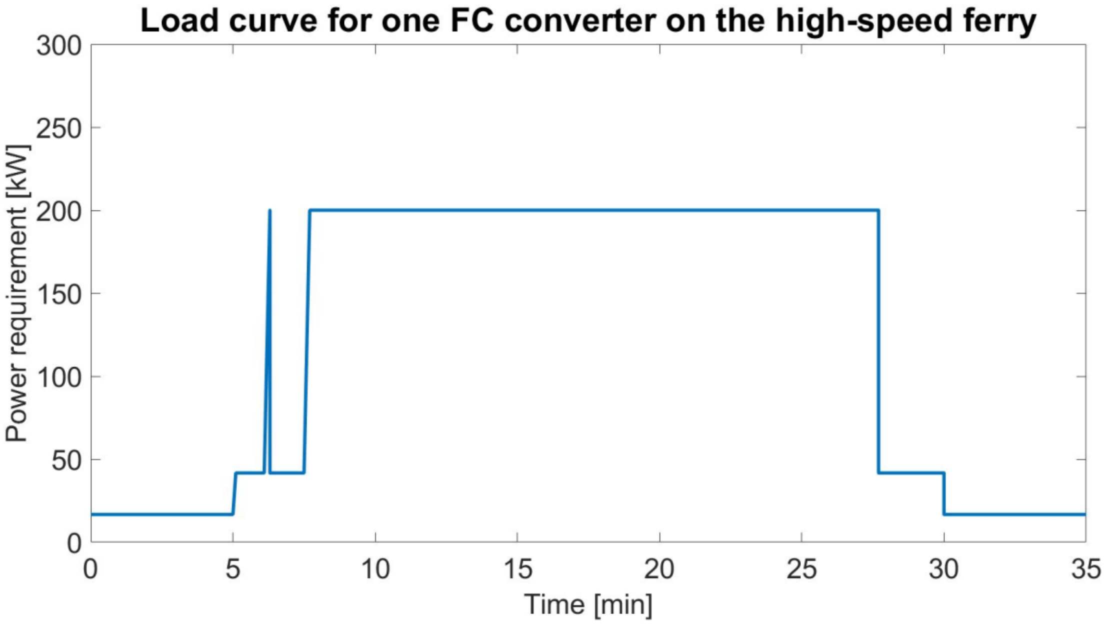

Figure 3.2: A proposed load curve for the FC converter investigated in this thesis

In reality, the periods of 5knots would have highly transient abilities due to maneuvering. As the FC only can ramp up in 10% power per second from Table 2-3, the power transients must mainly be provided by the battery. The FC should not be exposed to too much transient behavior, at least not at low power due to aging [12]. However, the FC converter should be able to support the transient power requirement as far as possible for, inter alia, emergency brakes. This response is simulated as a spike at approximately 7mins with max converter ramp rate in Figure 3.2.

From the given load curve, key converter specifications can be extracted. Firstly, the converter must be able to operate at full power for long time intervals. Also, it must be able to operate long-term on very different power ratings with a low current ripple for all operation [12]. It must also be able to handle the transient related to emergency braking. Furthermore, one could provide another battery size estimation. It is assumed that the ferry should be able to do the entire maneuvering interval on battery in case of a fault. A realistic gravimetric energy density for batteries in ships are 02kWh/kg [97]. Further, it is assumed the SoC of the battery should always be between 15% and 90% to leave some margin implying exploitable 0.15kWh/kg. Quick integrating of the maneuvering phase suggests a battery weight of roughly 100kg. This implies a much lower weight than previously estimated in Table 2-1. A bigger safety margin might however be desirable.

3.3 ELECTRICAL PARAMETERS FOR THE DIFFERENT LOAD CONDITIONS

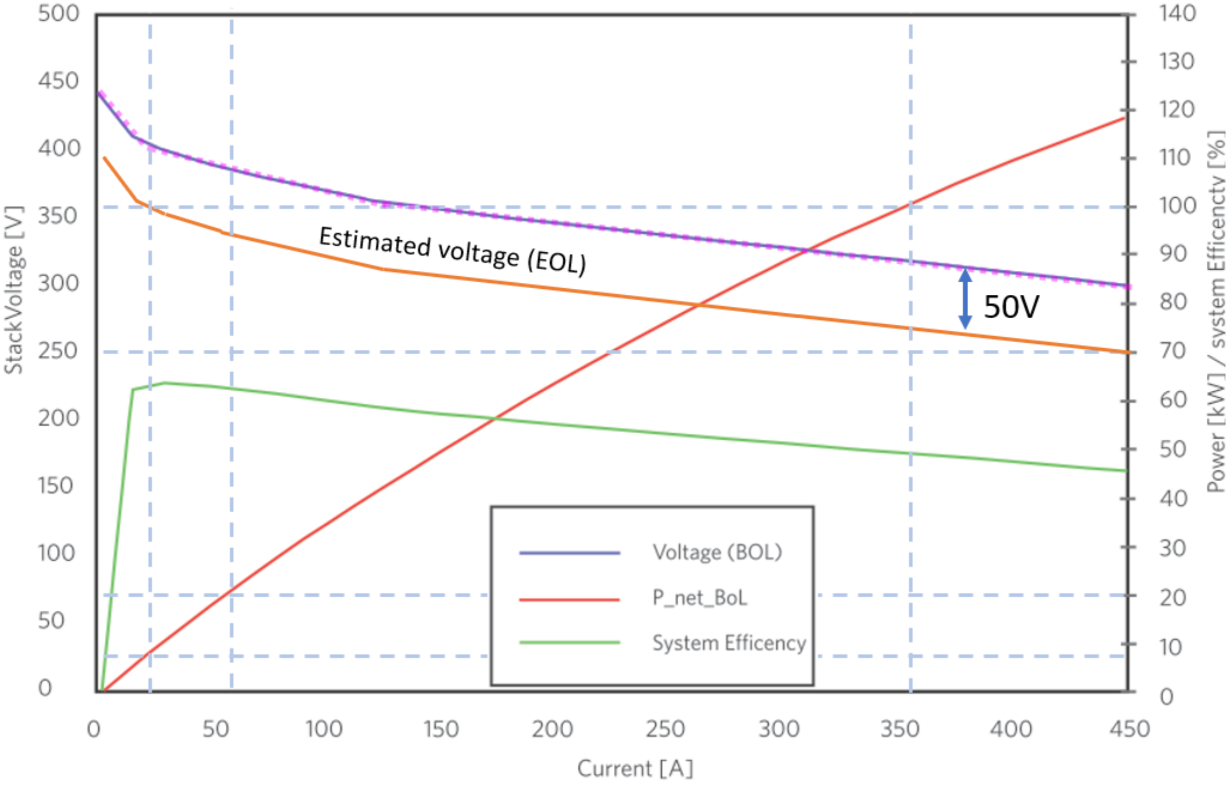

Figure 3.3: A modified version of the PowerCell Sweden MS100 FC datasheet [13].

To construct the Simulink model, the FC characteristics also need to be analyzed. There is a generic FC model in Simulink. This model was investigated and will not be used due to several reasons. The model gave realistic results in static simulations. It did, however, not provide realistic results during dynamic simulations. Also, the implementation of user-defined behavior caused malfunction. Hence, data found in the FC datasheet presented in Figure 3.3 is used for retrieving FC characteristics. For FCs, the IV curve varies with the aging of the FC. The difference in voltage at the beginning of life (BOL) and the voltage at the end of life (EOL) for the FC is 50V [13]. This EOL curve is approximated by shifting the IV curve 50V down from the BOL IV curve in Figure 3.3. The difference between EOL and BOL voltage at low power is expected to be lower, but this approximation leads to a worst-case investigation. Further, one can observe that the FC IV curve can be quite accurately approximated by three linear regions as shown by the purple dotted line over the BOL IV curve. Finally, there is a small mismatch between the net BOL power and the IV product in Figure 3.3. The IV product is used for the power calculations in this thesis. As the scope of this thesis only is to analyze the converter, the proposed 3-segment linearization is considered satisfactory.

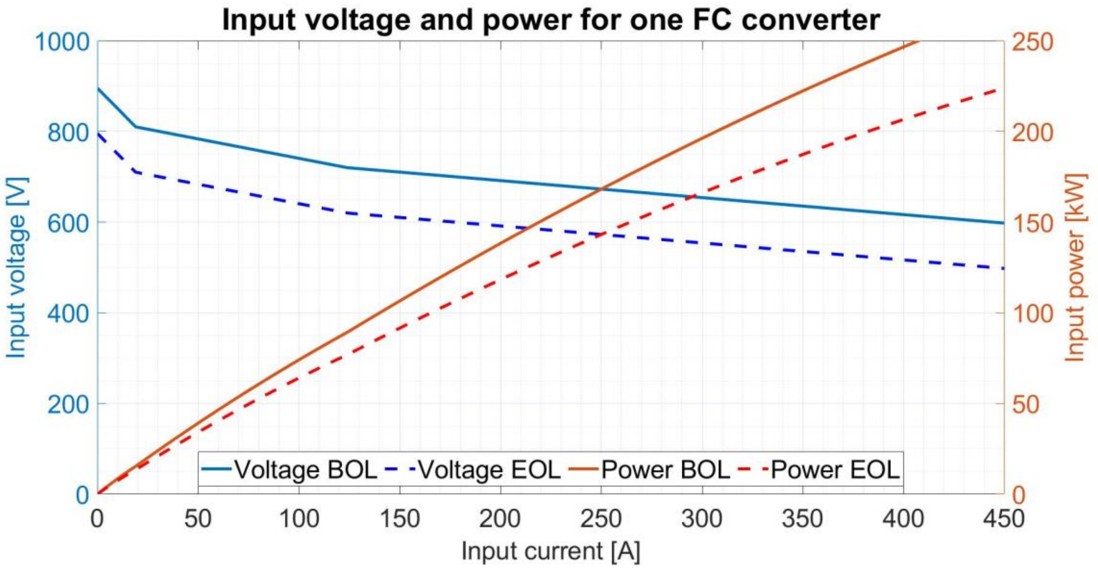

Figure 3.4: Input voltage and power as a function of current assuming the three linear segment approximation shown with purple dots in Figure 3.5

This 3-segment linearization is applied in MATLAB to determine and generate FC and hence, converter input electrical parameters for the rest of the thesis. The BOL and EOL voltage, power, and current for the converter input are shown in Figure 3.4. For a total ferry power requirement of 100kW, approximately 17kW per converter results in a BOL current of 21A. This may be problematic, as allowed minimum output for the FC is 20A as mentioned in Table 2-3. Operation on this limit contribute to further aging. This can be solved by, inter alia, turning off the FCs in one of the catamaran hulls or charging of the battery during the docking interval. Turning an FC on and off does however also contribute to aging. For this thesis, it is assumed that operation on this limit is acceptable. The IV data for the static operating points is summarized in Table 3-3

Table 3-3: The voltage and current of the FC and converter during the relevant static load operations.

Power requirement ferry [kW] **Condition**	**1200** **Full speed**	**250** **Maneuvering**	**100** **Docking**
FC stacks operating	12	12	12
Power requirement per FC [kW]	**100**	**20.8**	**8.3**
FC Voltage BOL [V]	325	391	405

FC Current BOL [I]	312	54	21
FC Voltage EOL [V]	260	336	353
FC Current EOL [I]	392	63	25
Power requirement per converter [kW]	**200**	**42**	**17**
Converter Voltage BOL [V]	650	781	809
Converter Current BOL [I]	312	54	21
CICM ideal duty cycle BOL	0.350	0.219	0.191
Converter Voltage EOL [V]	520	673	706
Converter Current EOL [I]	392	63	25
CICM ideal duty cycle EOL	0.480	0.327	0.294

3.4 THE DESIRED NUMBER OF PHASES

As shown in Figure 3.6, the advantages of increasing the number of phases are clear in terms of current ripple, inductor volume, and consequently weight. This was achieved with a decrease in cost and similar switching losses according to one particular study [62]. Increasing the number of phases beyond 6 is typically not considered. This is because the inductance does not decrease significantly per extra phase above this number. Besides, it leads to increased complexity and may result in DICM at low operating power, making control, and ripple unfavorable[62], [76], [77]. For this thesis, a 6-phase IBC will be investigated. This is due to several reasons. Firstly, as summarized in Table 3-3, the duty cycle will transition between 0.19 - 0.48. Then 5 or 6 phases is most feasible due to the dimensioning current ripple at a low duty cycle. Another reason is that having the number of phases divisible by three allows the purchase of commercially three phase inductors/chokes. Several producers offer such components, also for SiC frequency range [86], [87], [98]. This was recommended in an interview with industry, mainly due to decreased costs. Further, having the number of phases divisible by two leads to easier assembly due to symmetry reasons.

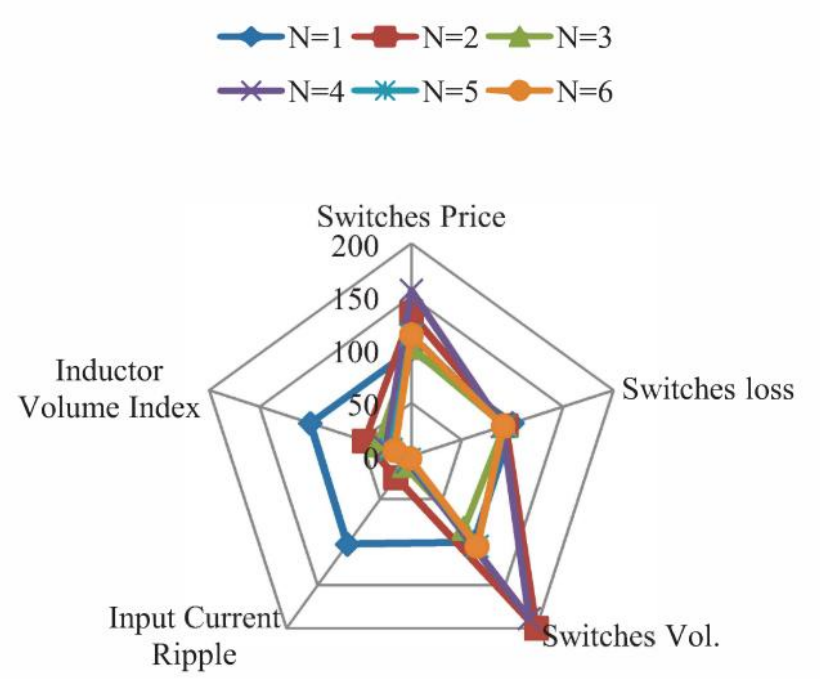

Figure 3.6: An investigation of several entities as a function of the number of phases in the IBC [62].

Finally, the converter should be able to utilize SiC components due to lightweight considerations [29], [54], [55]. Hence, a number of phases that matches market available SiC components would be advantageous. The development of SiC components are happening very fast, and SiC MOSFET modules are now available up to around 72A for 1.7 kV voltage rating [39]. As later will be shown, two of these MOSFETs gives an appropriate safety margin for rated operation when utilized in parallel in a 6-phase IBC. Hence, the margin will be insufficient for a 5-phase IBC. Therefore, 6 phases are also a good fit in terms of available components.

3.5 PART-LOAD OPERATION

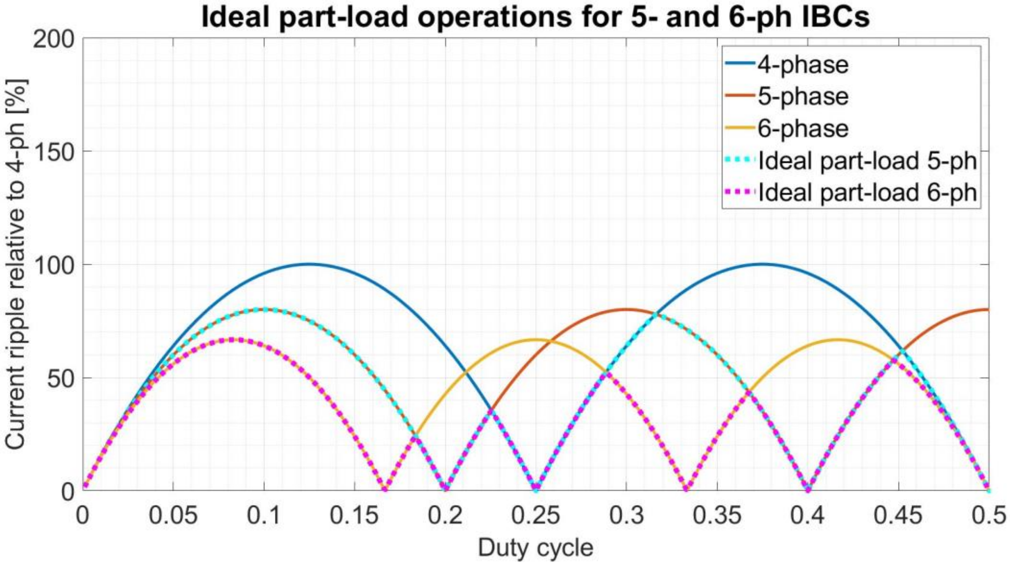

Figure 3.7: Ideal part-load scheme for 5- and 6-phase IBCs, respectively as a function of the duty cycle.

IBC part-load operation to reduce ripple should be investigated for the static operating conditions summarized in Table 3-3 [10], [17]. This is done by investigating the current ripple that was shown in Figure 2.9, using Appendix 1. By operating the converter with the number of phases always corresponding to the lowest ripple for every duty cycle, the operation would look like the purple dotted line Figure 3.7 for a total of 6 phases available. The lower number of phases are not included in the plot as they are factors of the included phases and don't provide any additional ripple paths. Figure 3.7 clearly shows the benefit of part-load operation compared to conventional 6-ph operation. Using Appendix 1, 6-ph part-load operation leads to a minimum ripple decrease of 22%, and an average ripple decrease of 60% in the docking power EOL-BOL duty cycle range.

Comparing the 6-ph part-load scheme to a 5-ph IBC part-load scheme, the ripple is equal for duty cycles between 0.18 - 0.29 seen in Figure 3.7. Hence, there is no ripple reduction utilizing 6-ph instead of 5-ph for docking. The ideal part-load operation scheme in Figure 3.7 cannot be implemented for the converter in this thesis due semiconductor rating constraints as later will be shown. A proposed control scheme is proposed in Figure 3.8. The proposed operation scheme is summarized in terms of active phases in Table 3-4.

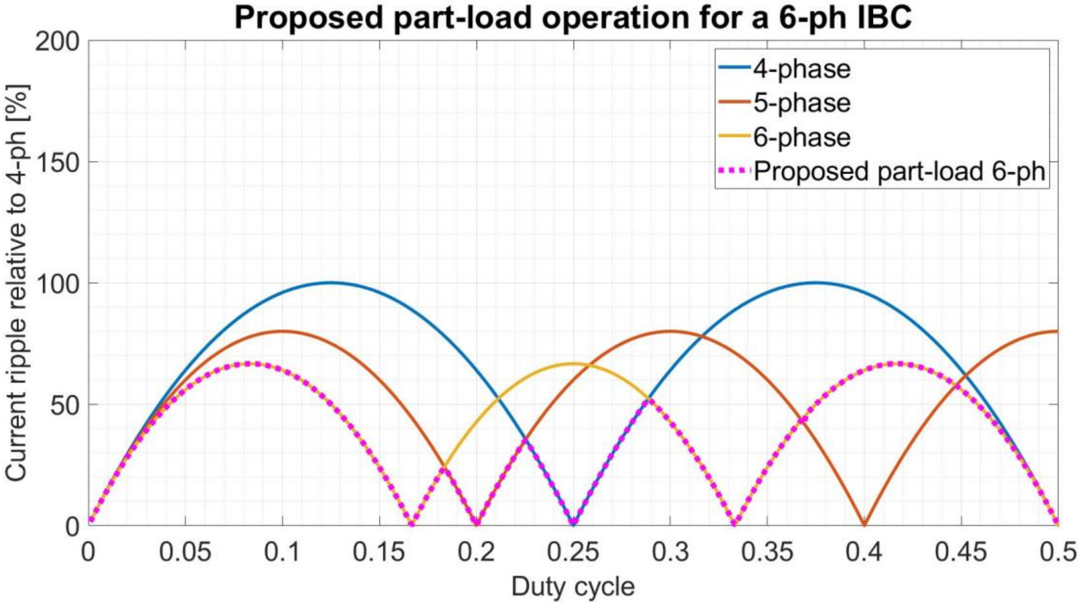

Figure 3.8: A proposed 6-ph part-load operation scheme considering semiconductor component rating constraints.

Having a total of 6 converters, the option of keeping some FC stacks turned off should also be investigated. This could enhance FC efficiency [7]. Since the IBC offer redundancy in terms of several legs and FC stacks offer redundancy with bypass switches for single faulty cells, the opportunity of utilizing two 600kW converters could also be interesting. Still, for this thesis, six 200kW 6-ph IBCs are considered the scope. Part-load operation increases control complexity but can quite easily be implemented as will be later shown. Due to beneficial ripple reduction, the proposed 6-ph part-load scheme is presumed for the converter from now on at duty cycles up to 0.37. Above this, only 6-ph operation should be used to avoid exceeding semiconductor ratings.

Table 3-4: The number of operating phases that lead to the smallest ripple within rating constraints for all relevant duty cycles in this ferry application.

CICM Duty cycle interval	Number of operating phases for minimum FC ripple
0 - 0.18	6
0.18 - 0.23	5
0.23 - 0.29	4
0.29 - 0.37	6
0.37 - 0.45	6 (rating constraint)
0.45 - 0.5	6 (rating constraint)

4 IBC SIMULINK SIMULATIONS

4.1 STATIC SIMULATIONS

4.1.1 Static Simulink model

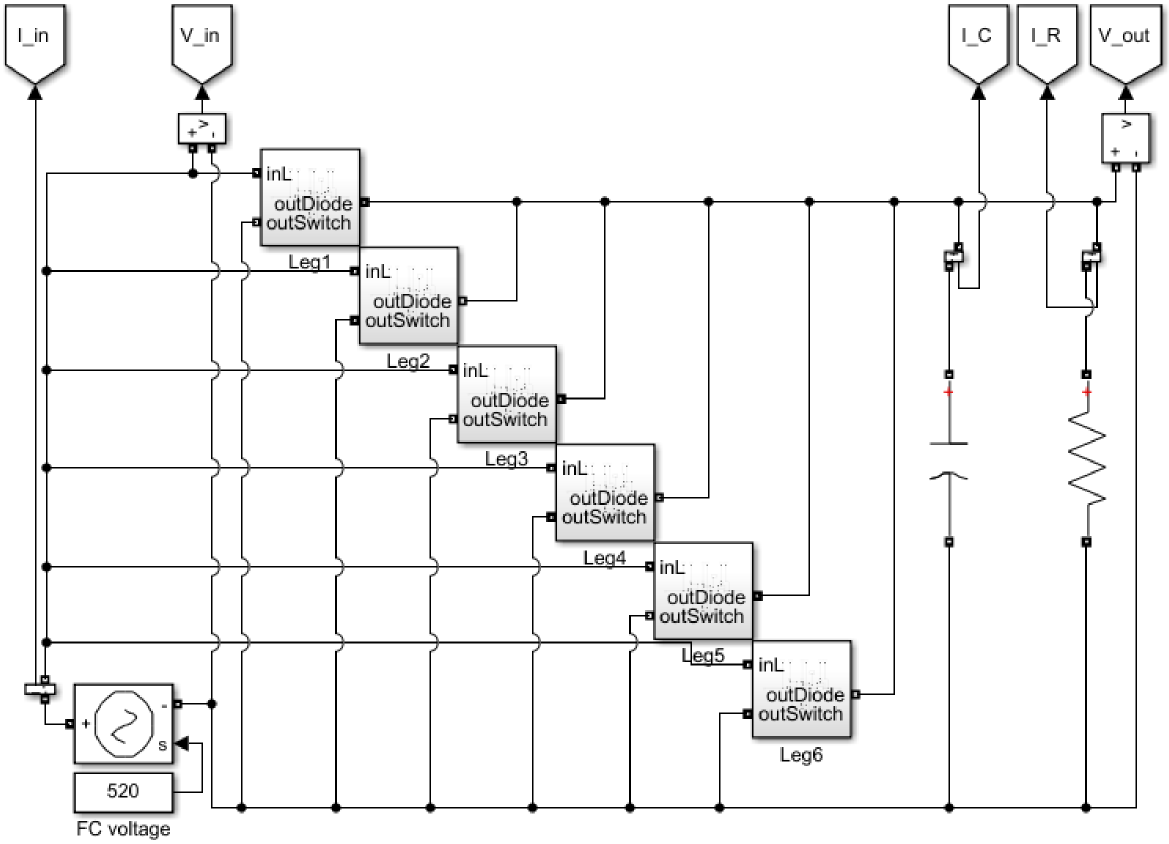

Figure 4.1: A proposed static 6-ph IBC model created in Simulink

Regarding simulation speed and feasibility, the static Simulink model shown in Figure 4.1 is created as simple as possible. For a load profile, the fuel cell voltage is changed manually together with the corresponding duty cycle and resistance. Capacitance, switching frequency, phase inductance, and the number of phases operating are easily controlled with variables saved in model workspace. Each converter leg contains a phase inductance, diode, and switch with separate measurements. The PWM signal is received by the switch exploiting "Goto-From" Simulink tags. The leg subsystem is shown in Appendix 3. The PWM generation system for the static model is shown in Figure 4.2. For each phase, there is a sawtooth carrier waveform with a time delay corresponding to both the phase number and the number of phases operating. The carriers are compared to the duty cycle creating the PWM signal for each phase.

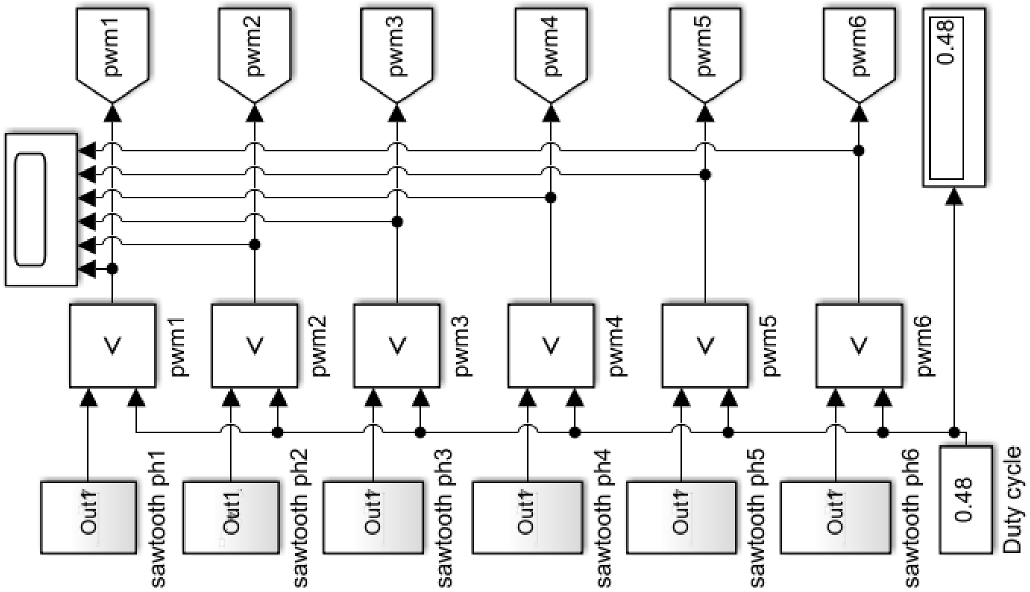

Figure 4.2: The IBC duty cycle generator logic

All the operating scenarios discussed in section 3.3 can be analyzed with the static Simulink model. The model can also analyze DICM behavior, but none of the operating conditions in this thesis were found to be in DICM under the given ripple constraint. The model enables part-load analysis simply by changing a model workspace variable and uncommenting the phases not operating. Ideal components are assumed. Figure 4.3 shows some currents of significance for a 97% aged FC stack during docking generated with the static Simulink model. This is one of the most interesting operating scenarios of the converter for this thesis, as it is dimensioning for the phase inductance.

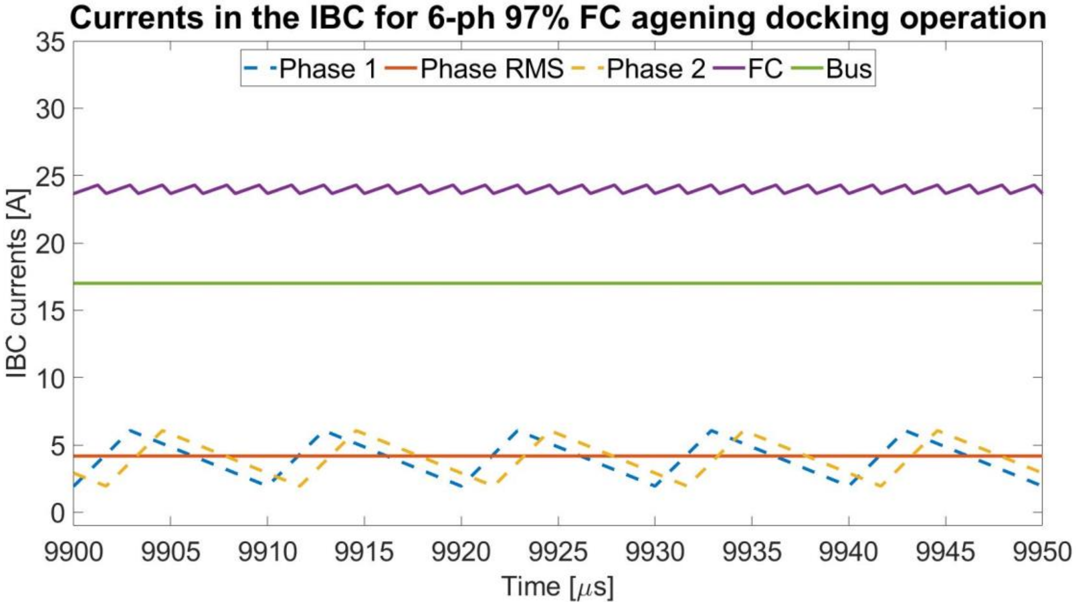

Figure 4.3: Currents during docking operation with 97% aged FC stacks

4.2 DYNAMIC SIMULATIONS

4.2.1 Control system complexity

It would be feasible to construct a functioning control system for the IBC in Simulink. This is, however, considered out of scope for this thesis due to the complexity. A linear control system could be implemented based on approximated linear fuel cell behavior, but it would not be realizable in a real system due to the non-linear FC behavior [79], [82], [83]. Also, it is crucial to get the phase shift timing between the phases correct, so they contribute to ripple canceling and not ripple addition. This is clearly illustrated in Figure 4.4 for 2-ph IBC operation attempted controlled by cascade PI loop control. In physical applications with dead time and other non-idealities, sliding mode control, and other sophisticated structures are, therefore, typically implemented [79], [81], [99].

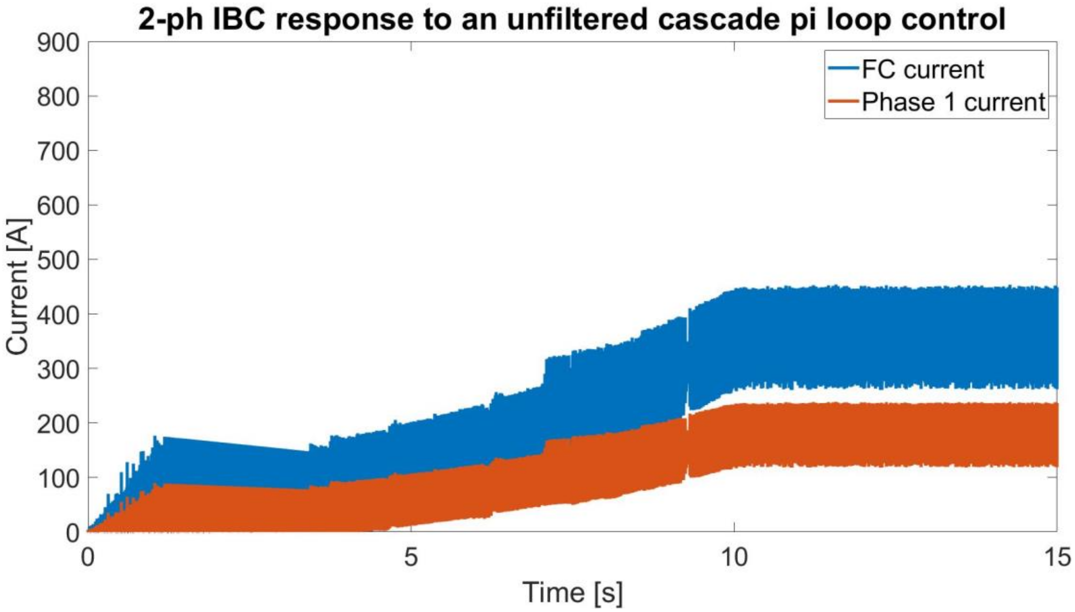

Figure 4.4: An attempted PI cascade loop control of the IBC in 2-ph operation, leading to current ripple addition.

The crossing of the CICM-DICM boundary also contributes to complications for the control system [100]–[102]. The control system must be able to operate accurately through this boundary during turn-on as the FC requires a slow power ramp rate to prevent damage and aging [20]–[22]. Start-up of the FC stacks will require complex dynamic DICM operation and may utilize special techniques. The investigation is, therefore, not considered viable in this thesis. Regarding all aforementioned aspects, the simplest control structure possible is used during the simulations. Due to the low ripple requirement, the converter will remain in CICM during the load curve, assuming no turn-on or turn-off of the FC. Hence, it is trivial to find the required duty cycle curve for a given power ramp rate based on the linear FC approximation shown in Figure 3.3

4.2.2 Dynamic model

A full dynamic model of the converter was considered unfeasible to develop in Simulink in this thesis. This is due to the following reasons. Firstly, for dynamic behavior, a dynamic fuel cell model should be used to provide realistic results. It was not possible to gain access to such a model. Secondly, the control structure is as mentioned extremely hard to implement. There was found no simple way to ensure equal current sharing in each phase while the phases align with the required phase shift for ripple cancellation. This is especially the case for part-load operation, as the inductor currents in each phase that is not utilized will have to increase from zero up to the phase current when activated. With high frequencies and relatively big inductances, the inertia of the coil can be significant. Inter alia, for 0.5mH, the coil would use 32.5μs to reach a current of 65A with 1000V applied. For comparison, the switching period is 10μs for 100kHz operation. Hence, in terms of ripple and adequate conditions for the control system, it would be favorable to ensure operation of all phases during a converter power transient.

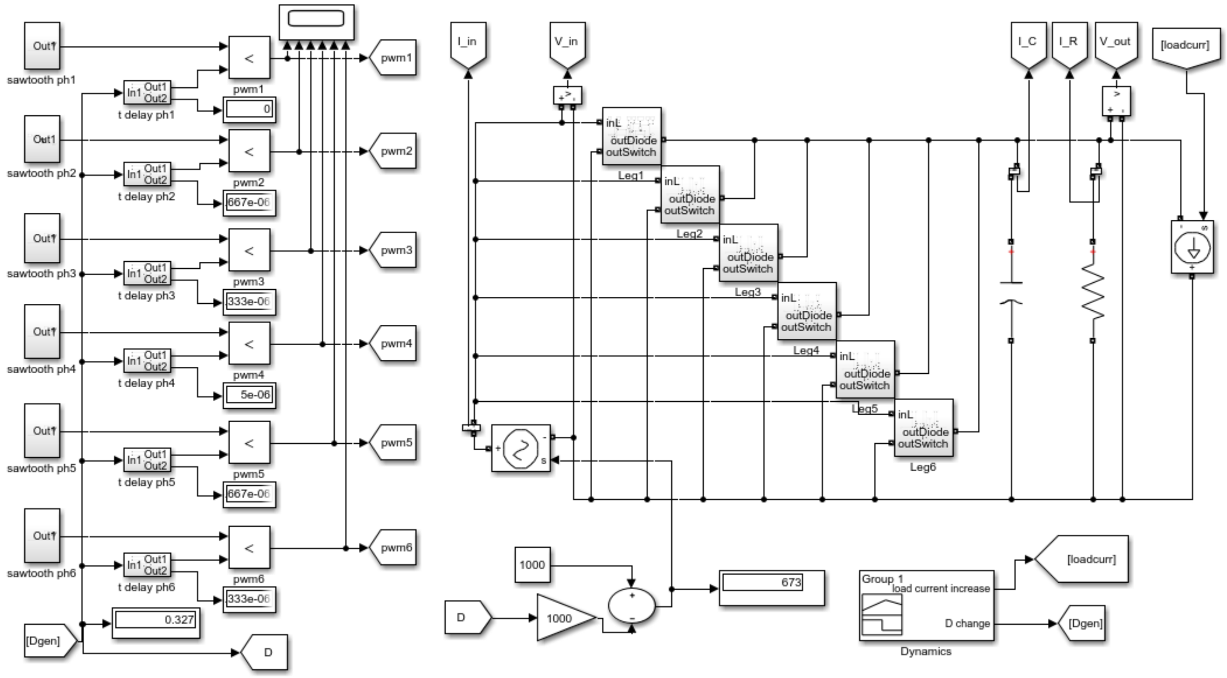

Figure 4.5: The dynamic Simulink model without part-load operation

Furthermore, the dynamic behavior will be more dependent on the bus dynamics, which is also hard to predict. The dynamic ripple will also be dependent on the chosen control structure. Finally, running transient analysis over several seconds with a 100kHz complicated model requires a lot of computing power. However, simple simulations are done to verify that the dynamic ripple is not expected to be dimensioning for the inductor. A dynamic model is proposed in Figure 4.5. It uses a resistive load in parallel with a controllable current source as a variable load. The FC voltage is dynamically changed by CICM relations from the duty cycle. Load increase in relation to the duty cycle is parameterized as a function of time and ran with a signal builder. Finally, to enable dynamic behavior, the dynamic duty cycle must be delayed correspondingly to the sawtooth signal of the phase it should match.

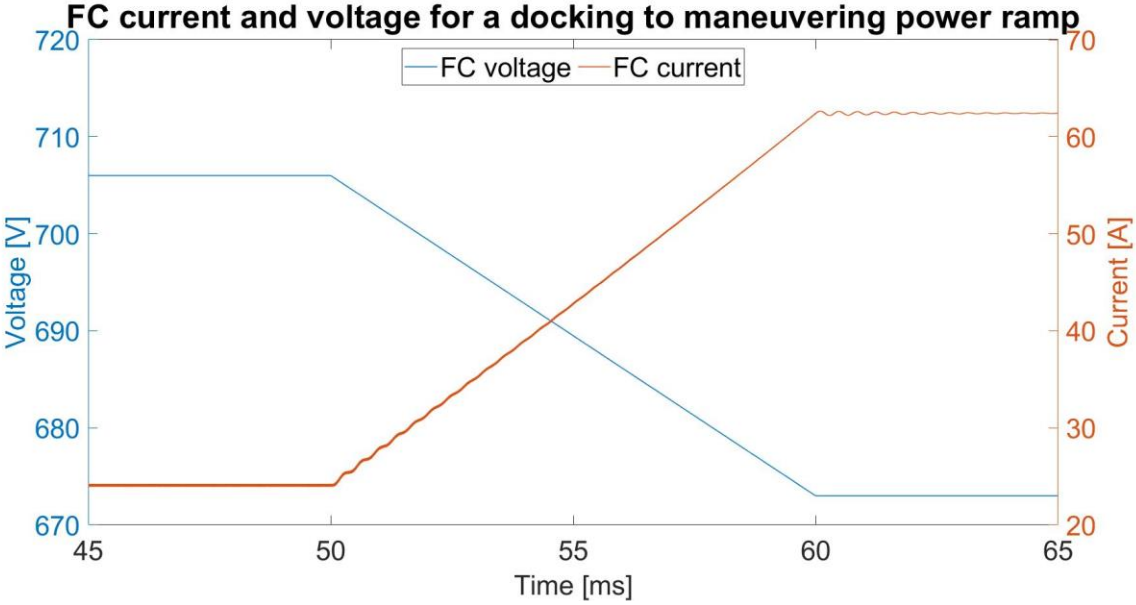

Figure 4.6: FC voltage and current change responding to linear bus power increase from docking to maneuvering at EOL conditions.

Data retrieved from the 3-segment linearization shown in Figure 3.4 is used for dynamic simulation of linear power ramping up from docking to maneuvering under EOL conditions shown in Figure 4.6. The ramp is done over 10ms due to computing power limitations but would, in reality, be in the magnitude of seconds. The ramp is still much slower than the switching frequency, so the ripple should be similar for a slower ramp. Inspection of Figure 4.6 shows that the ripple is decreased during the transient, as the duty cycle is shifting towards a ripple cancellation area. The ripple is increasing at any point during the transient response. This is except for some minor oscillations. Anyhow, the 2% ripple restriction is meant as a general guideline to maintain FC health and can be temporarily exceeded. Exceeding ripple restrictions must, inter alia, be the case for the start-up of the FC stacks. The dynamic current ripple is also found to be smaller or equal to corresponding static ripple for other ramp-ups and ramp-downs with the dynamic Simulink model. Any significant change in voltage ripple is not noted either. Consequently, it is verified that dynamic converter behavior is not expected to require special ripple concerns with an adequate control system.

4.2.3 Proposed Part-load scheme logic

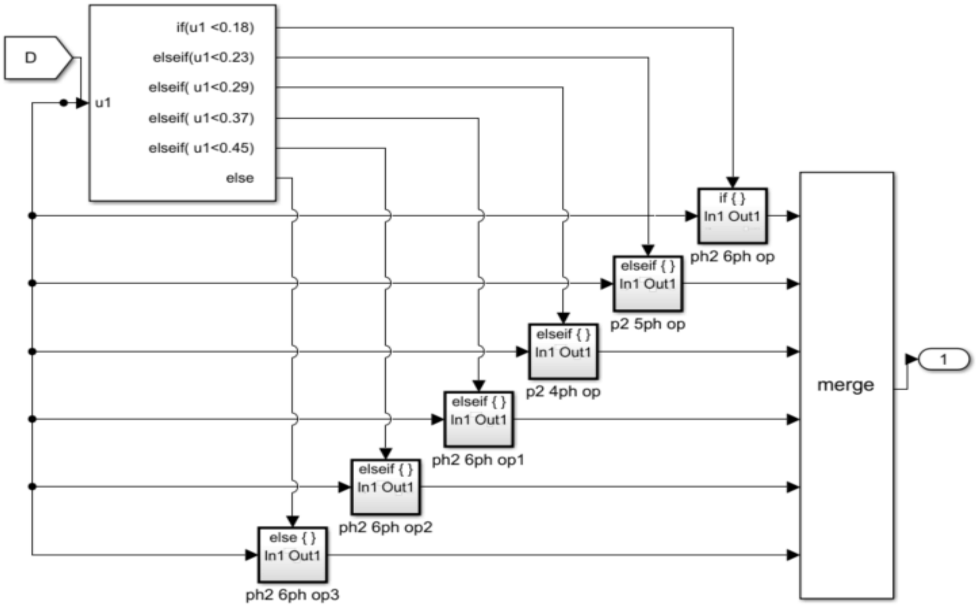

Figure 4.7: The logic determining the number of phases operating in the part-load structure.

In this thesis, part-load utilization is assumed. To justify this utilization, a viable part-load control structure is proposed. From Figure 2.9, the only parameter determining how many phases should be operating for minimum ripple is the duty cycle. Therefore, the control system reads of the duty cycle in real time and uses “if” structures to determine what number of phases leads to optimal operation, as illustrated in Figure 4.7. Each leg contains several sawtooth waveforms corresponding to the included part-load operation variations. The correct waveform for the correct operation is also determined by “if” structures, as shown in Figure 4.8. This proves that a part-load scheme is feasible with relatively simple structures. The proposed scheme works for the static model and would work for the dynamic model with sufficient current balance control structure. It is, however, not used as a standard in the static model due to reduced computing speed.

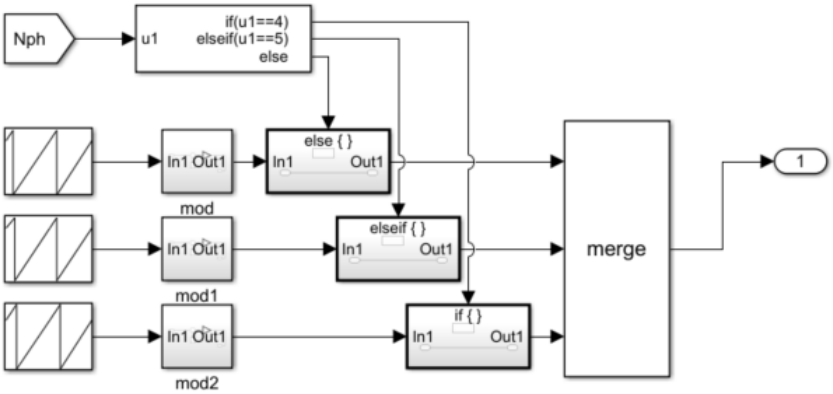

Figure 4.8: The part-load logic structure determining which carrier signal will be utilized for the second phase.

5 SEMICONDUCTOR COMPONENTS

The worst-case scenario for the semiconductors can be seen from Table 3-3 at rated EOL conditions. Assuming CICM, this implies a maximum on-state current of 65A at D=0.48 through the switch. Correspondingly, this will also be the worst case operation for the diodes, with (1-D)=0.52 and same maximum on-state current of 65A. This scenario will be utilized for dimensioning during this chapter. During these conditions, the current ripple will be neglectable in size, and the average value will be 65A, equal to the RMS value for 0.5mH phase inductance. This approximation can also be made for the maneuvering phase, as the difference between RMS value and average value still is below 0.1A. The latter statements are verified with the static Simulink model. This simplifies the calculations that will be done manually later in this chapter. As the maximum losses occur during a static load interval, a static thermal circuit can be used to dimension the components. This is verified in section 5.2. A loss script based on the Simulink models was originally developed for this thesis, but manual calculations were determined to be simpler. The script can be found in Appendix 4.

5.1 SiC COMPONENTS DP TESTING IN LTSPICE

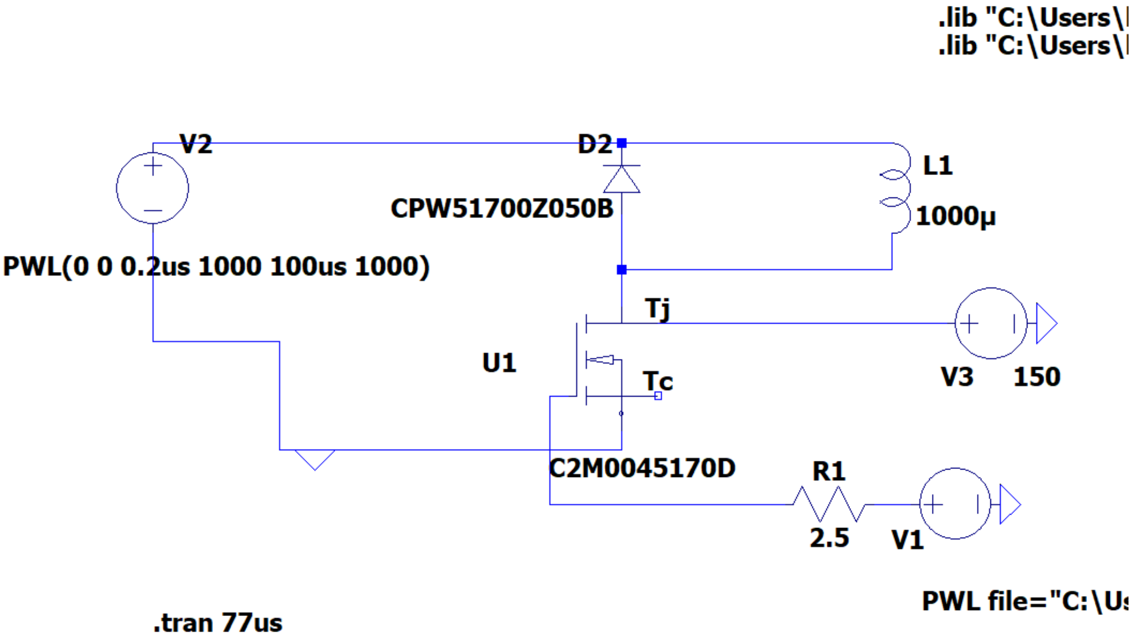

Figure 5.1: The DP test setup for inductive loads with imported SiC 1700V MOSFET and Schottky diode from Wolfspeed [38], [39].

An increased switching frequency contributes to smaller passive components. It is therefore desirable to keep the switching frequency as high as possible for the converter. However, the switching losses increase with increased switching frequency. Consequently, the frequency will be a tradeoff between weight, volume, and losses. To determine the switching frequency, the total losses will be approximated for several switching frequencies. Subsequently, the highest frequency allowed by the utilized devices with acceptable losses will be chosen as the operating frequency. This is the preferred approach as low weight and volume are vital for the given converter. First, the switching losses will be quantified. This is done by executing a double pulse test (DP test) shown in Figure 5.1 and comparing them to results presented in datasheets. The test set-up is corresponding to the tests presented in the following literature [103]–[105].

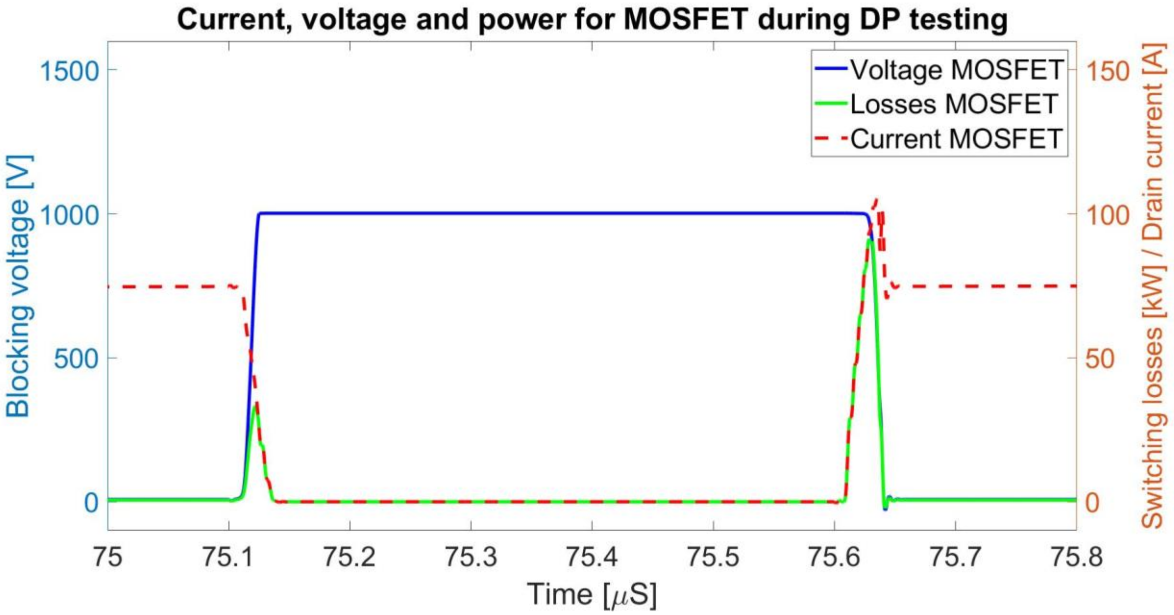

Figure 5.2: Off- and on-state switching losses together with drain current and blocking voltage for the SiC MOSFET during a 72A, 1000V DP test.

The semiconductor components used are imported as LTspice models from Wolfspeed. This producer is currently the only one offering 1700V SiC components with adequate current ratings [38], [39]. The voltage and loss during a switching cycle are shown for the SiC MOSFET at 73A on-state current in Figure 5.2. Wolfspeed claims that their SiC Schottky diode is virtually lossless [106]. This is also the results of the diode in the DP test as the turn off is equal to the negative turn on value for all on-state currents, hence no losses. The MOSFET switching losses are tested for both 150$°C$ and 100$°C$ at 1000V shown in Figure 5.3. In the datasheets, the total loss for one switching cycle increases with increased junction temperature. A clamped inductive test similar to a DP test is also found in the datasheets with similar voltage levels, showing switching losses with over twice the magnitude of those found in Figure 5.3. This test is done on real components and is not from simulations, explaining the big difference. Hence, the DP test results found in this thesis are assumingly too optimistic.

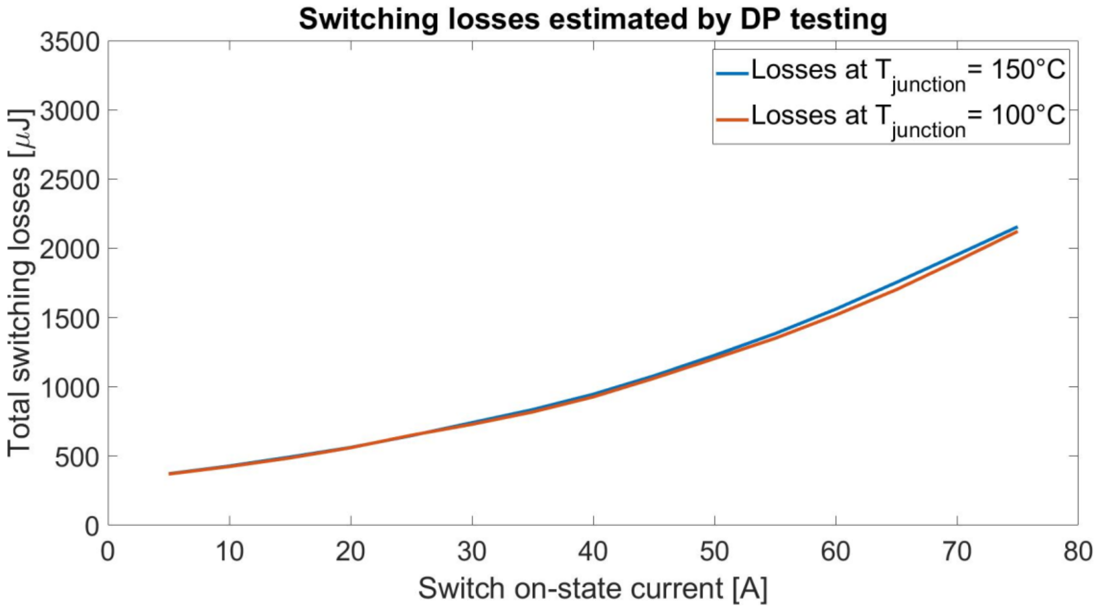

Figure 5.3: DP test results from LTspice with the following SiC MOSFET and diode [38], [39].

Due to very fast switching in the SiC parasitic components, especially stray inductances, should be included in the simulation to achieve realistic results [105], [107]. Another DP test with 1nH on each of the pins on both the diode and MOSFET was executed with slower gate voltage transients. The results provided higher switching losses and loss of control within the maximum gate voltage range for relatively low currents. This illustrates the need for practical testing to be able to estimate realistic behavior and losses. Snubber circuitry, extra gate resistances, and preferably a kelvin node should be utilized to ensure feasible semiconductor functionality [105], [108]. Due to uncertainties, the maximum switching frequency is decided to be 100kHz even though simulations allow a higher frequency. 100kHz at rated power is typically the highest frequency considered for high power SiC devices [36], [37].

5.2 SIC COMPONENTS DIMENSIONING

For this section, 100kHz and the following equations will be used for loss calculation:

Conduction losses MOSFET:	$P_{cond} = R_{DS(on)} \cdot {I_{sw\ RMS}}^2$	Equation 9
Switching losses MOSFET:	$P_{sw} = \left(E_{on} + E_{off}\right) \cdot f_s$	Equation 10
Conduction losses diode:	$P_{cond} = V_F \cdot I_{D\ AVRG}$	Equation 11
Leakage losses diode	$P_{leak} = V_{rev} \cdot I_{leak} \cdot D$	Equation 12
Static thermal circuit:	$\Delta T = R_\theta \cdot P_{loss}$	Equation 13

For comparison, this thesis will first use the DP simulation switching energy values and, after that, the datasheet switching energy values to calculate total losses in the components. The junction temperature will be restricted to 100°C for these calculations. This will leave a safety margin as the investigated components are designed to sustain 150°C operation. Additionally, resistance and losses for a junction temperature of 150°C will be used for calculations, leaving a further margin. A liquid cooling system that keeps the case at 40°C or lower at all times is assumed. With a junction temperature of 100°C, this would allow loss transportation of 270W using the static thermal resistance found in the datasheet [39]. Hence, this is considered the maximum acceptable losses for thesis conditions.

Initially, DP simulation switching energy is used. Comparing the mentioned worst-case scenario, on-state resistance from the datasheet, CICM switch waveforms, and switching losses from Figure 5.2, total losses for the MOSFET can be found using Equation 9 - Equation 13. Utilizing one unparalleled MOSFET per phase would require transportation of around 360W in each component, including both switching and conduction losses. This is unacceptable. Hence, the utilization of two parallel devices is assumed, leading to losses of 130W from each component.

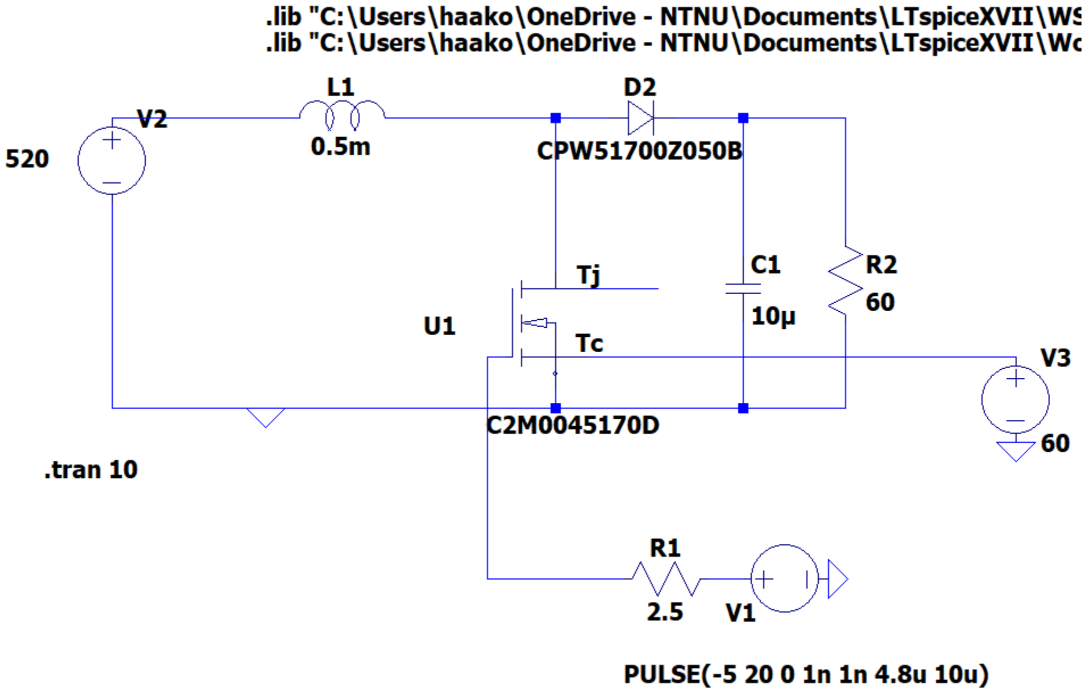

Figure 5.4: MOSFET condition equivalent IBC leg implemented in LTspice under EOL full speed condition with the case temperature locked to 60°C.

To investigate the temperature change in the MOSFET, a simple boost converter representing equivalent MOSFET conditions, one-half phase-leg, is built in LTspice and the switch is supplied with an on-state current of 33A at D=0.48. The remaining parameters are set to thesis specifications. The converter is shown in Figure 5.4. The case temperature is locked to 60°C, and the simulation is run until the junction temperature stabilizes to acquire the steady-state value. The temperature as a function of time is shown in Figure 5.5. The temperature waveform has no overshoot, and the ripple in temperature due to switching is negligible. This is as expected, validating the use of a static thermal circuit in this thesis. As the switching losses from the datasheets were higher than simulations, the actual temperature magnitude is expected to be higher than in Figure 5.5. The temperature waveform is, however, expected to be correct.

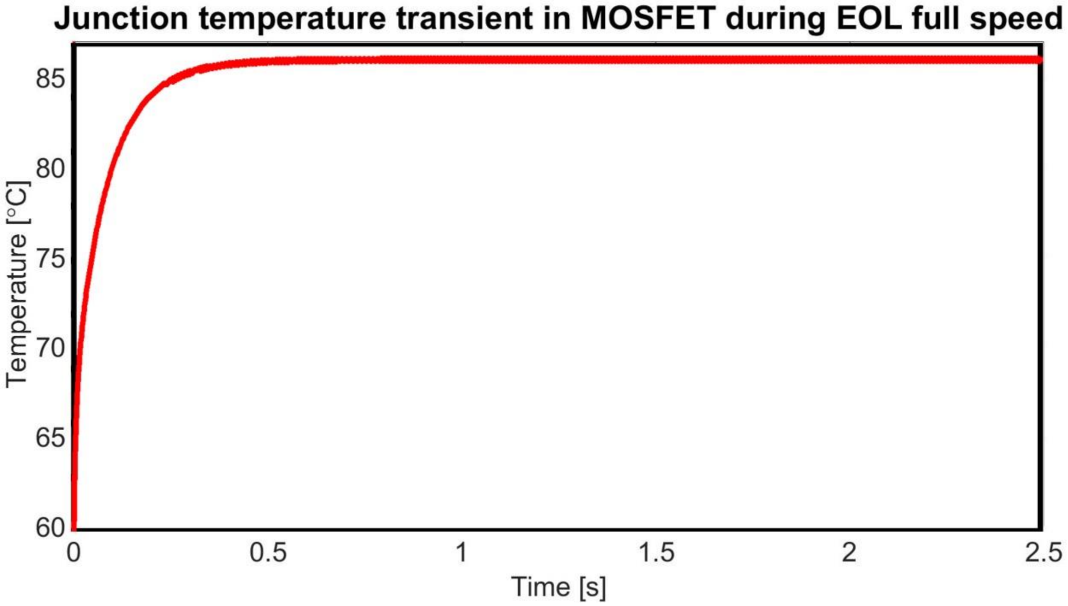

Figure 5.5: Junction temperature of the SiC MOSFET as a function of time during full speed EOL conditions with a case temperature of 60°C.

From the datasheet, one can observe that the switching losses of the MOSFET are practically unchanged with junction temperature when paired with a SiC Schottky diode in DP testing [39]. Calculation of losses based on 150°C datasheet values and interpolation is done to verify further, showing 239W per MOSFET in losses[39]. Hence, the utilization of two parallel devices is therefore considered realizable for the actual converter. Figure 5.6 generated with the static Simulink model shows the two switch currents and diode current together with the inductor current for the first phase under EOL full-speed conditions.

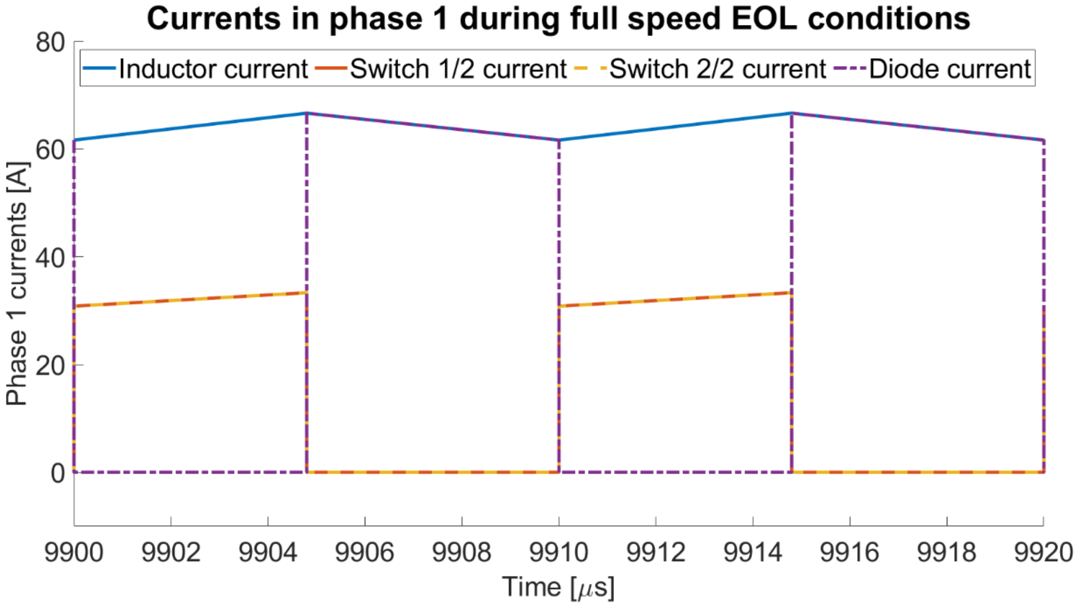

Figure 5.6: The currents in phase 1 during full speed EOL conditions.

Regarding the Schottky diode, Wolfspeed offers both the bare die version that is used in the previous DP tests and a cased option [38], [109]. Looking at the cased option, ratings are much lower presumably due to poor packaging. The packaging specifications for the investigated corresponding MOSFET will, therefore, be assumed for the bare die Schottky in this thesis. This should be a valid assumption as the ratings of the components are similar, and the MOSFET is having the highest losses at the given operating conditions [38], [39]. This implies that the Schottky too will allow transportation of 270W with a junction temperature of 100°C and a case temperature of 40°C.

Looking at the Schottky datasheet, the forward voltage for 65A is about 3V for worst-case temperature. This implies conduction losses of 101W under worst-case full speed CICM conditions [38]. This is also the total losses, presuming no switching losses and leakage losses are found to be negligible for 1000V operation [38]. Hence, total diode losses are 101W. This should also be verified in practical testing of an actual component. Particularly to verify if zero switching loss is achieved, and also considering uncertainties with the casing.

5.3 SIC COMPARABLE SI COMPONENTS

For this section, the following equations is used will be used for loss calculation in addition to Equation 11 and Equation 13:

Conduction losses IGBT: $P_{cond} = (R_{lin} \cdot I_{sw\ RMS}{}^2 + V_{CE(sat)} \cdot I_{sw\ AVRG})$ Equation 14

Switching losses IGBT: $$P_{sw} = \left(E_{on} + E_{off}\right) \cdot f_s$$ Equation 15

Switching losses diode: $$P_{sw} \approx E_{off} \cdot f_s$$ Equation 16

Although this thesis' main focus is SiC components, the available Si components will be investigated for comparison. The only feasible Si component that can replace a 1700V blocking voltage SiC MOSFET is IGBTs. 1700V IGBTs are far more common than 1700V SiC MOSFETs, providing a wide range of current ratings[110]. Si IGBTs are typically cheaper, but with higher losses at high frequency and lower allowed operating frequency than SiC MOSFETs [56], [111], [112]. For a comparison with two 72A continuous current rated SiC MOSFETs, one 150A continuous rated IGBT is considered the most feasible available replacement. This component is, inter alia, sold by Infineon [113] and will be the IGBT module investigated in this thesis. For this current and voltage magnitude, the only market available IGBTs found are sold as bridge leg modules, as shown in Figure 5.7 [113], [114]. One bridge leg will be used for one IBC leg, operating only one IGBT and one diode, keeping the remaining two components idle. This is a sub-optimal solution only chosen due to lack of suitable components.

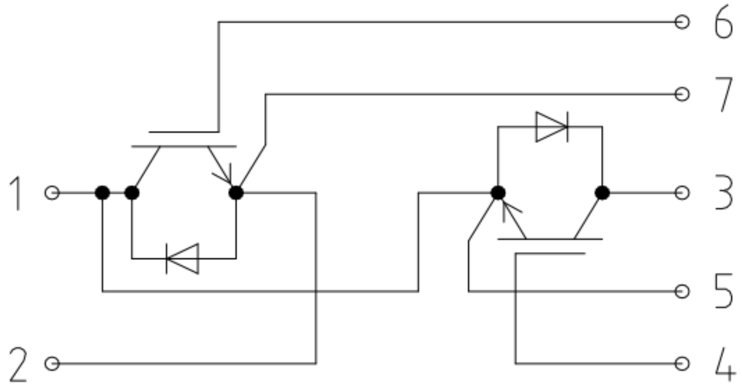

Figure 5.7: The circuit diagram of the dual IGBT module with freewheeling diodes investigated in this thesis[113]

It is hard to find a realistic IGBT model for import to LTspice, and the program offers no integrated IGBT model, making testing of the device tricky. Hence, the datasheet of the IGBT module will be used to determine operation and losses. From Figure 5.8 one can observe that the $V_{CE\ (sat)}$ is approximately 1.05V and R_{lin} is approximately 9.4 $m\Omega$. Furthermore, the switching losses can be found in Figure 5.9. The thermal resistance is 0.135K/W for the IGBT and 0.16K/W for the diode from junction to heatsink [113]. Hence, the maximum heat transportation allowed is 445W and 375W for the IGBT and diode respectively with a junction temperature of 100°C and a case temperature of 40°C. Paste and grease thermal resistivity is neglected for a fair comparison to the SiC components.

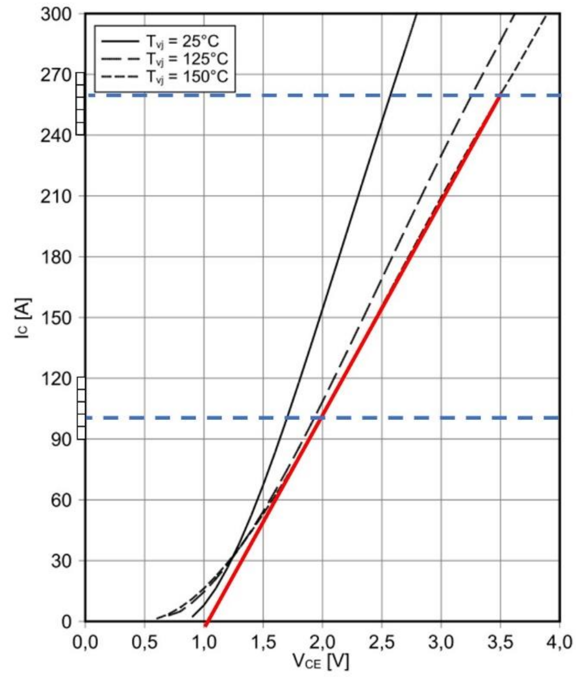

Figure 5.8: A modified IGBT collector-emitter voltage graph [113].

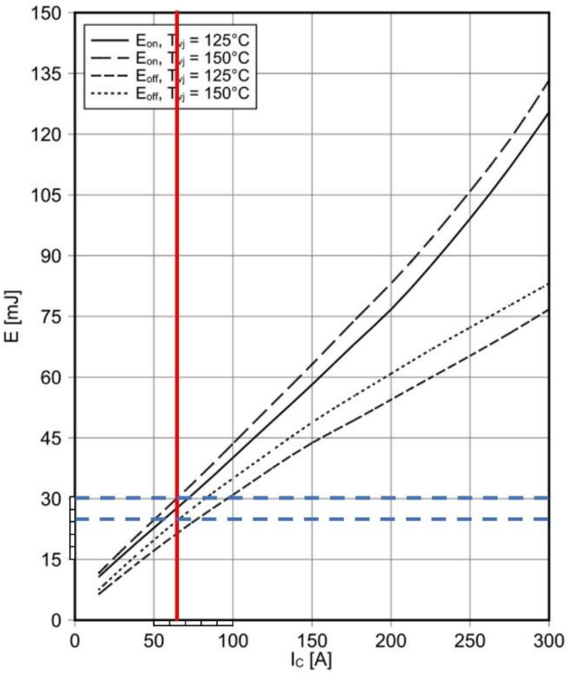

Figure 5.9: A modified IGBT switching loss graph with $V_{CE} = 900V$ [113].

Calculated losses are made with the same worst-case as the SiC counterparts with 150°C junction values from the datasheet. It is found that the diode losses will be dimensioning for the frequency. Using values for reverse recovery energy and forward voltage from the datasheet, it is found that the diodes will have losses of approximately 335W under worst-case semiconductor conditions at 5kHz [113]. To leave some margin for, inter alia, heatsink thermal resistance 5kHz is chosen as the operating frequency. Equal conditions result in around 315W IGBT losses. Rise and fall times including delays are found to both be under $1\mu s$ for inductive loads in the datasheet, confirming that 5kHz IGBT operation is possible. Hence, utilization of 5kHz components should be realizable.

Looking at other market available modules in this voltage and current range all have switching losses and thermal resistance in the same magnitude, resulting in similar operation frequencies. 25kHz operation might be achieved by purchasing and assembling several IGBT transistors, but this seems disadvantageous looking at the available components. For 1200V single transistor IGBTs, current ratings are too low to use them unparalleled. For 600V IGBTs, the voltage rating requires three IGBTs in series to reach a safe 1000V bus operation. IGBTs with voltage ratings between 600 and 1200V are uncommon [110], [115]. Thus, connecting IGBT transistors individually requires 3 or more individual components, and are not considered feasible, especially with a multiphase topology. Hence, Si utilization for the given ferry application will be hard to realize for higher than 5kHz operation. Si components are not investigated further, as it later will be shown that the maximum frequency operation is considered insufficient in terms of weight.

5.4 SIC COMPONENT LOSSES FOR VARIOUS LOADS

Table 5-1: A summary of the semiconductor losses calculated previously.

Component	**Loss calculation method**	**Combined losses, worst-case [W]**	**Maximum allowed losses** $T_j = 100°C$ $T_c = 40°C$
2 SiC MOSFET	DP testing LTspice	260 @100kHz	540
2 SiC MOSFET	Datasheet calculation and interpolation	478 @100kHz	540
1 SiC Diode	DP testing LTspice	101 @100kHz	540
1 SiC Diode	Datasheet calculation and interpolation	101 @100kHz	540
Si module IGBTs	Datasheet calculation and interpolation	315 @5kHz	445
Si module diodes	Datasheet calculation and interpolation	335 @5kHz	375

100kHz operation is assumed from here on unless otherwise is specified. The losses are already found for the worst-case full speed scenario. Using the datasheet losses from Table 5-1, the losses in each leg equals 580W. With the 6 legs, this equals 3.48kW. For maneuvering, the losses can be found in the same manner with the previously stated loss-equations for SiC devices. The EOL is also here the worst-case conditions with a total current of 63A and D=0.327. This duty cycle implies 6-ph operation from the proposed operation scheme in Table 3-4. Under these conditions, the RMS value and the average value is $10.7A_{RMS}$ and 10.6A, respectively, by static model inspection, as shown in Figure 5.10. 10.7A is used as both values for simplicity. Also, the change in on-state resistance of the MOSFET is small and therefore assumed constant and equal to full speed calculations.

Using the same on-state resistance as in Table 5-1, it is found that conduction losses are 3.4W. Switching losses are found via datasheet interpolation to be 65W per leg. For the diode, the losses are 7.8W reading a forward voltage of 1.1V from the datasheet. These add up to a total loss of 457W [38], [39]. An important note is that this is assuming only one of the two switches per leg is operating and 6-ph configuration. This is done because the calculation of losses in the SiC MOSFET below 10A is not viable, as the datasheet does not provide any data, and the DP-testing simulations showed that practical testing is required to achieve realistic results. Besides, this will also be the most favorable operation during low operating power in terms of efficiency. The latter will be shown in this section.

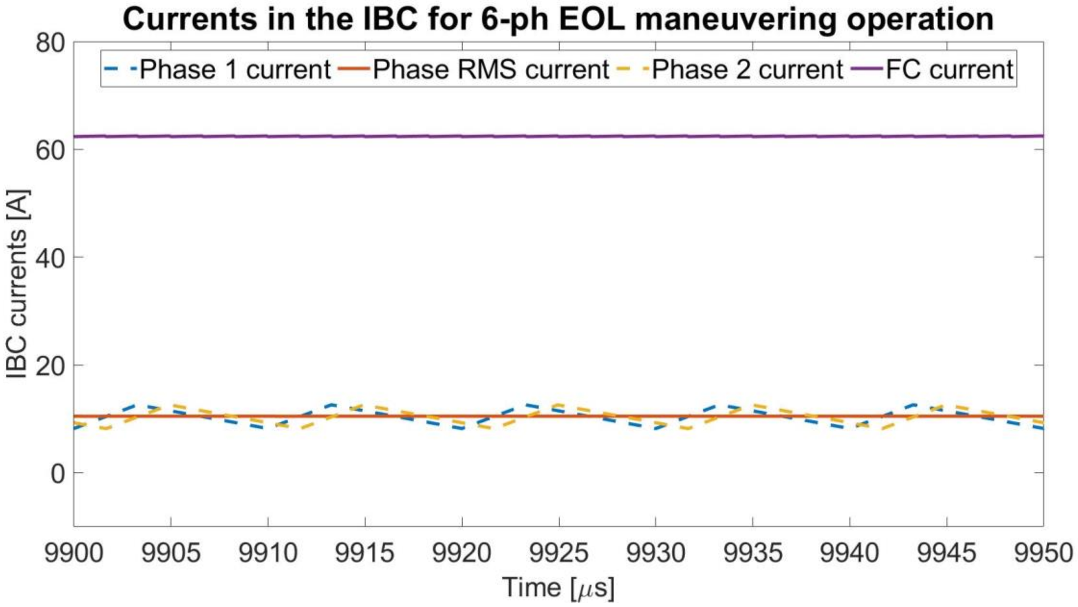

Figure 5.10: Different currents for 6-ph operation of the IBC during EOL maneuvering conditions.

By inspection of Table 3-4, the maneuvering phase transitions from 6-ph to 4-ph to 5-ph operation during the FC lifetime. Investigating BOL conditions, 5-ph operation occurs. By inspection of the static model under 5-ph operation BOL maneuvering, it is found that the phase current is 10.8A_{RMS}. Consequently, the losses are approximately 5/6 of EOL conditions. Furthermore, maneuvering at D=0.25 would imply 4-ph operation. This implies an FC voltage of 750V. By investigation in the static model, an RMS current of 14A_{RMS} is found. The switching losses are now by interpolation about 80W per leg for the MOSFET. The conduction losses are 4.4W [39]. For the diode, the voltage drop is approximately 1.3V. Hence diode losses are 13.6W. This equals a total loss of 392W. For comparison, 6-ph operation for D=0.25 would imply a phase current of 9.4A_{RMS}. By inspection of datasheets, this leads to 60W in switching loss 2W in conduction loss for MOSFET. With a voltage forward drop of 1V, it equals 7W in diode losses. The total is then 444W. Hence, the part-load operation is also clearly feasible in terms of efficiency for the maneuvering power levels.

As previously shown, operating a lower number of phases contributes to increased efficiency for maneuvering current levels. This is also expected to be the case for docking power levels but requires practical testing to verify. This is because for low current levels, doubling the current less than doubles the switching loss. This makes fewer components leading to fewer switching transients favorable. For high current levels, the effect is the opposite, it is observable that doubling the current more than doubles the switching energy [39]. Hence, additional components sharing the total current more will be more efficient. Consequently, a part-load scheme maximizing efficiency will look different than the one proposed minimizing current ripple for low current levels. This is, however, not considered advantageous. It can only be used at power levels where the ripple does not exceed the maximum ripple limit, and the current is low. This is only in transients and the maneuvering phase. The complexity increase is considered too high compared to the gain in efficiency.

6 PASSIVE COMPONENTS

100kHz was determined as the preferred operating frequency in section 5, and will, therefore, be assumed for the rest of this thesis unless other frequencies are specified.

6.1 IBC CAPACITOR

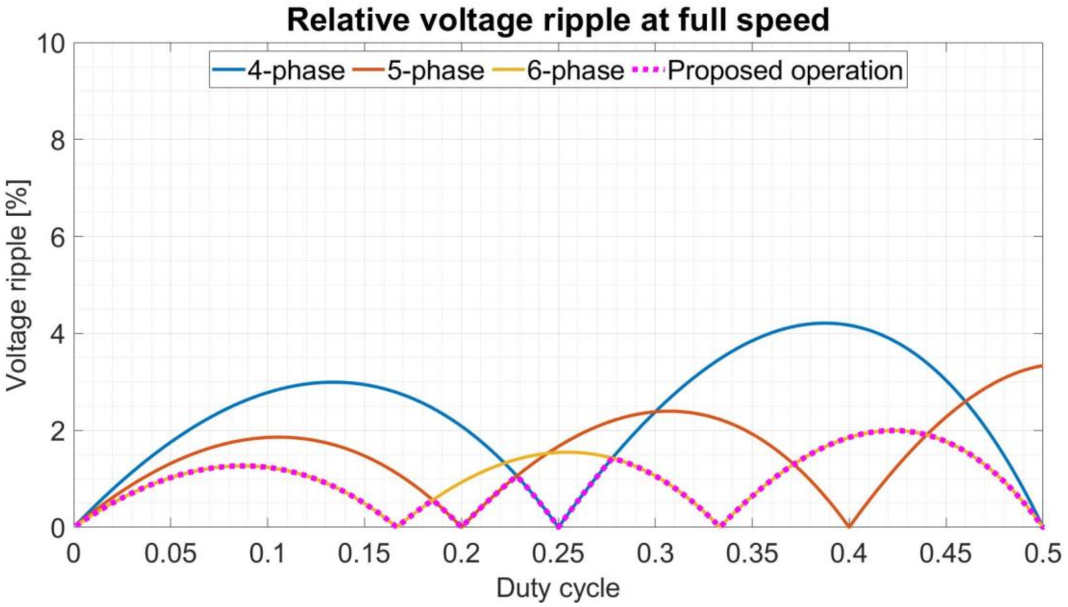

Figure 6.1: Relative voltage ripple in percent at full speed for several phases and the proposed operation scheme for 1.2μF.

For a 1kV bus, a maximum voltage ripple below 2% is considered feasible. The capacitor voltage and current remain unchanged if the power is constant, making the analysis simpler. For voltage ripple, increased power increases the voltage ripple in opposite to current ripple. Hence, if the maximum ripple occurs at a duty cycle that corresponds to full power for certain aging, this will be dimensioning. By inspection of Figure 6.1 generated with Appendix 2, the maximum voltage ripple is 2% for 1.2μF at D=0.422 for the proposed operation scheme. This duty cycle is within the full speed aging range, and hence, dimensioning. Consequently, the minimum capacitance should be 1.2μF.

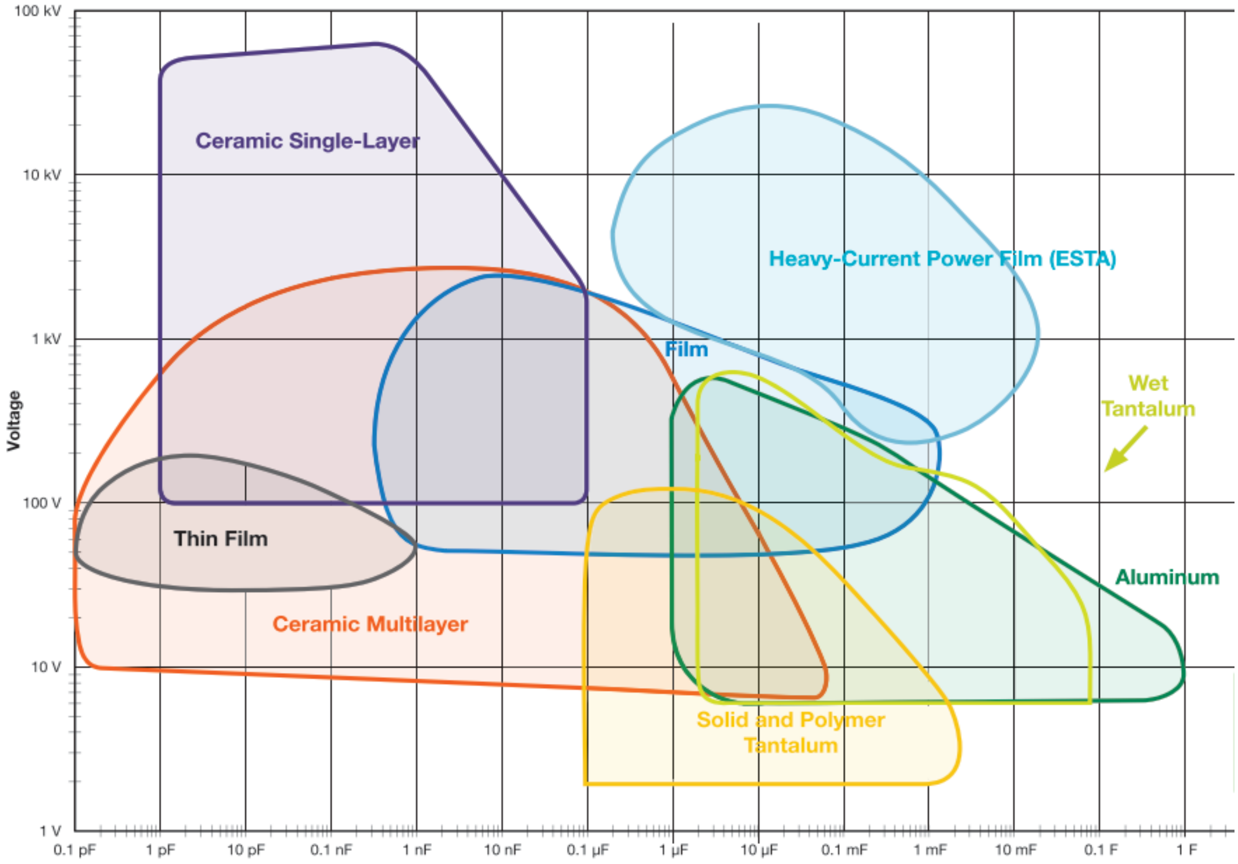

Figure 6.2: The suitable capacitor types in terms of voltage rating and capacitance [116].

From the capacitor utilization chart shown in Figure 6.2, both film and heavy power film capacitors are considered suitable. It is important to consider that due to 6-phase IBC, the capacitor ripple is 600kHz for 100kHz operation. This corresponds to a switching period of 1.67μs. This alongside the waveforms of 1.2μF full speed D=0.422 operation is generated using the static Simulink model in Figure 6.3. This figure further verifies both the ripple found in Figure 6.1 and the switching period. The RMS value of the current is also found to be 31A. The closest capacitors to these specifications are found in datasheets from KEMET and Vishay [117], [118]. The KEMET datasheet has an option of 1200V capacitors for 1-2μF, but these can only sustain 15A in capacitor RMS current. Hence three needs to be paralleled. An option considered more suitable is the 1200V and 10μF option allowing up to 60A RMS. Both aforementioned components have a capacitor limit of 350V/μs, which is sufficient for a maximum 20V ripple and a period of 1.67μs. The 10μF option is chosen for this thesis, and weighs 350g with a volume of approximately 524dm^3.

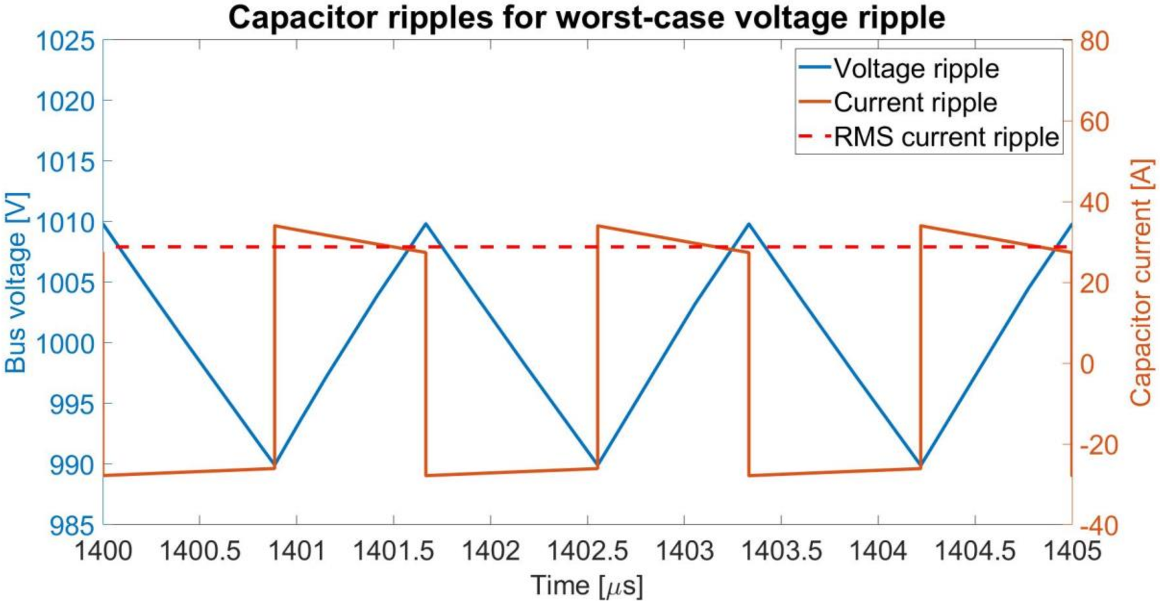

Figure 6.3: Capacitor voltage ripple and current ripple for the full speed D=0.422 operating point with 1.2μF capacitance.

6.2 IBC INDUCTORS

6.2.1 Finding the minimum inductance

The minimum inductance can be found analytical by combining previous results. Comparing data from Table 3-3 with the part-load scheme in Figure 3.7, one can see that the current magnitude increases slightly from BOL to EOL while the current ripple magnitude changes significantly for the same load power. Hence, aging will mainly determine the ripple at a certain static power level. Some ripples for 0.5mH inductance during docking are summarized in Table 6-1 for different FC aging. This table is found with Appendix 1. By utilization of Appendix 1, the maximum current ripple is found during docking operation with 97% FC aging assuming 6-ph part-load scheme. This operating scenario is previously plotted in Figure 4.3.

Table 6-1: Current ripple percentages with 0.5mH phase inductance for the different phases during docking.

FC aging	**Duty cycle docking**	**4-phase ripple [%]**	**5-phase ripple [%]**	**6-phase ripple [%]**
0% (BOL)	0.1919	4.26	3.424	**1.96**
20%	0.212	2.956	**1.01**	2.956
40%	0.232	**1.48**	2.4	3.43
60%	0.253	**0.252**	3.51	3.51

80%	0.273	**1.78**	3.946	3.416
97% (worst ripple)	0.291	2.78	4.022	**2.56**
100% (EOL)	0.294	2.94	4	**2.44**

Utilizing Appendix 1, the current magnitude dominates the current ripple magnitude for increased power, and the load power will, therefore, be dimensioning for the current ripple. This is illustrated in Figure 6.4, generated from Appendix 1. Here, one can observe that current ripple decreases for power increased beyond docking power, regardless of how many phases in the proposed part-load scheme are operating. Hence, it is confirmed that the maximum current ripple is occurring during docking, making the data from Table 6-1 dimensioning. The recommended ripple guidelines for ripple over 1kHz to be 2% from Table 2-3, but higher frequency implies a higher acceptable ripple. It is desirable to keep the inductance as low as possible for weight, volume, and price purposes. Thus, for 100kHz operation, a ripple a little above 2% is considered optimal. With a worst-case ripple of 2.56%, 0.5mH phase inductance seems suitable for 100kHz 6-ph part-load IBC operation. The maximum ripple is also verified with the static Simulink model.

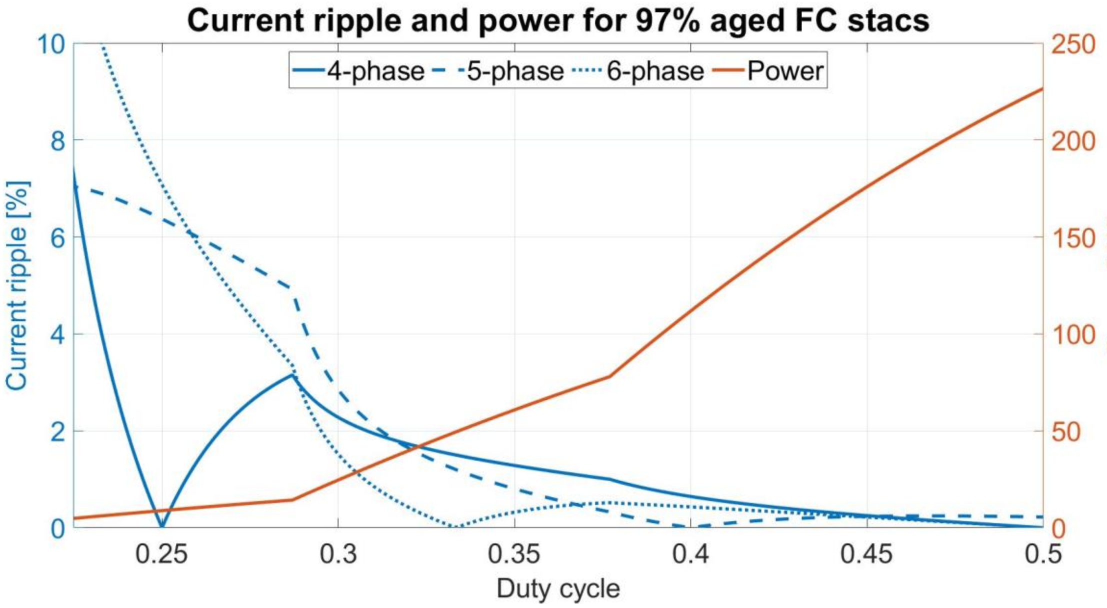

Figure 6.4: Current ripple in the relevant phases and power a function of duty cycle for 97% aged FC stacks and 0.5mH phase inductance during docking operation.

6.2.2 Inductor design

When designing an inductor, several design inputs need to be assembled. This represents the first stage in Figure 6.5. One of these is the frequency, which for SiC semiconductors in this thesis is determined to be 100kHz. Furthermore, the maximum temperatures regarding loss needs to be determined. 100°C is a common maximum inductor temperature besides the maximum temperature assumed for the semiconductor devices and is therefore chosen [56]. An ambient temperature of 40°C is assumed to utilize the liquid cooling system if necessary. The worst-case inductor current must also be found. From Table 3-3, the worst-case current is the rated EOL conditions leading to an RMS current of approximately 65A. For this currents ripple restraint in Table 2-3 makes the current ripple negligible as discussed in section 5. Hence, DC, AC, and peak current are all approximately equal. The minimum inductance was found in the previous section to be 0.5mH. Then the inductor can be designed after the procedure shown in [56], [119]. Consequently, entity nr 1-7 is listed in Table 6-2.

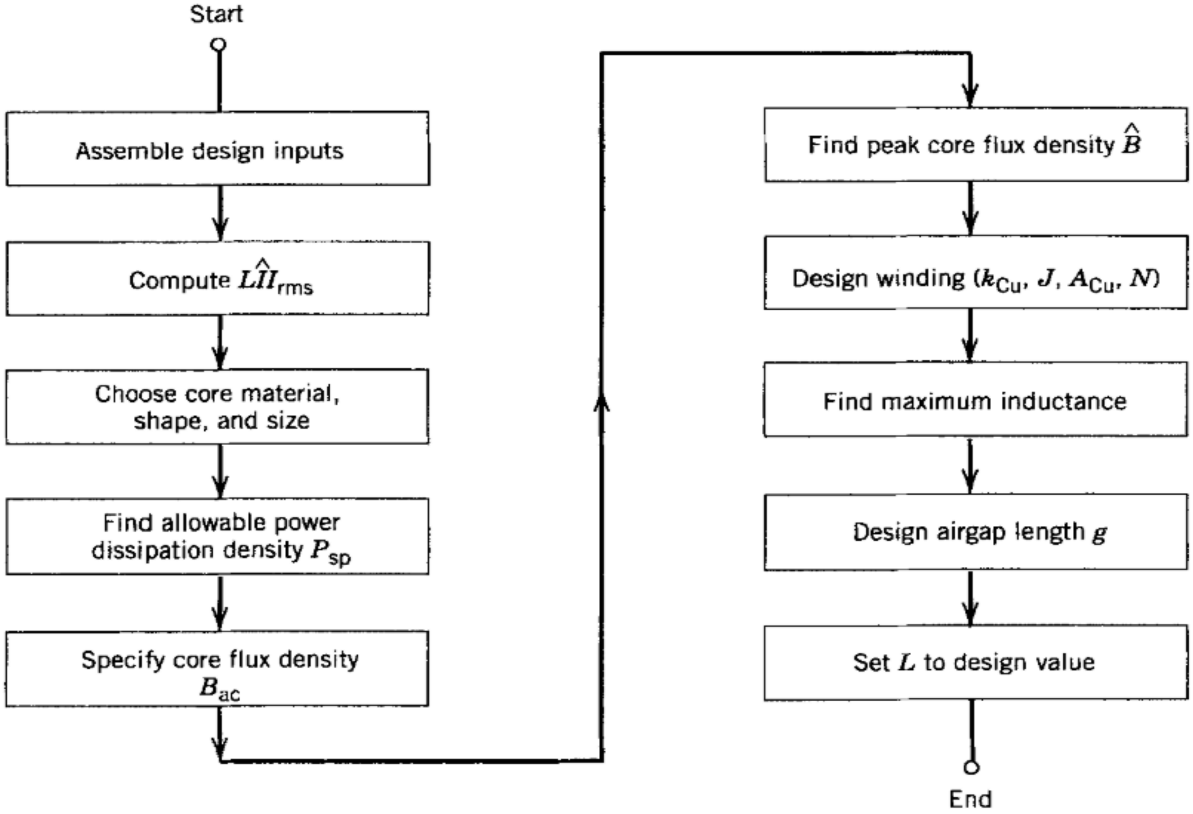

Figure 6.5: A typical inductor design process [56].

From the prior Table 6-2 parameters, Ferrite 3F3 is utilized as it is a typical 100kHz material [56]. This thesis will be based on a datasheet from the producer Ferroxcube, who produces cores in this material. A maximum inductor B-field of 0.35T is decided, and a mass density of 4750kg/m^3 is found from the datasheet [120]. There are materials that contribute to lower weight, inter alia, with higher maximum flux density and distributed airgaps [121]. They are, however, not considered favorable for the given ferry application due to high material cost. Furthermore, double E and EI cores are both good candidates for 100kHz applications [56],

[122]. Choosing an EI core, the fringing flux from the air gap won't interfere with the windings to the same extent of what it would in a double E core. However, double E core would result in lower fringing flux due to the air gap being inside the windings. A double E core is chosen due to being seemingly the most common core on the market. Thus, entity 8-10 is added in Table 6-2.

Table 6-2: The required electrical parameters for a simple inductor design

Entity nr:	**Gathered design inputs:**	
1	Inductance value L	0.5mH
2	Rated peak current $\hat{I}$	65A
3	Rated DC current I_{DC}	65A
4	Rated RMS current I_{RMS}	65A
5	Operating frequency f	100kHz
6	Maximum inductor surface temperature T_s	100°C
7	Maximum ambient temperature T_a	40°C
8	Core material	Ferrite 3F3
9	Maximum core flux density $\hat{B}_{core}$	0.35T
10	Core shape	Double E
11	Wiring	Litz wire
12	Maximum current density $\hat{\rho}_{cu,I}$	$3A/mm^2$
13	Window fill factor $k_{cu,fill}$	0.3
14	Maximum resistivity wiring	$22\Omega/nm$
15	Mass density wiring $\rho_{cu,mass}$	$8960kg/m^3$
16	Mass density core $\rho_{core,mass}$	$4750kg/m^3$

As this is an HF application, Litz wire will be utilized. Then both proximity and skin effect can be neglected. A typical window fill factor for Litz wire is 0.3 or a little above [56], [122]. 0.3 is therefore assumed as the fill factor for the window area, regardless of the number of turns, bobbin size, and wire thicknesses. This estimation is rough, especially for small inductors. A bobbin should be used for HF applications to keep the worst fringing field away from the windings. For small window areas the bobbin will take up a considerable size, and generally, less copper can be fitted within the same area assumed equal wire bundle diameter. The copper current density is typically recommended to be between 3.5-4A/mm^2 for various applications. As a similar inductor design with Litz wire is proposed has a current density a little above $3A/mm^2$, this current density will be used [122]. The resistivity of copper at 100°C is 22Ω/nm, and the mass density of copper is 8960kg/m^3 [56]. That concludes Table 6-2.

Table 6-3: Three possible inductor designs for Table 6-2 parameters.

Design number	Airgap [mm]	Number of turns	B-field [T]	Core weight [kg]	Total weight [kg]	Total volume [liter]	Copper ESR [$m\Omega$]
1	7	40	0.35	5.11	7.70	2.0	4.1
2	9	49	0.35	4.33	7.45	2.1	4.9
3	19	69	0.29	3.33	7.73	2.3	6.9

To efficiently analyze different inductors, a simple inductor design algorithm is created. The code is shown in Appendix 5. The code is based on similar algorithms found in [56], [119], [122] and will be described in rough steps. The code starts with Table 6-2 as input parameters and iterates on airgap and number of turns. The core cross section is found from the required stored energy, and the window area is based on the number of turns. From there optimal E-core symmetry and square box fringing approximation found in [56] is used to create different inductor designs. Filters extract viable design options to a table. From here, the most favorable design must be chosen by inspection. The code is used to generate three favorable designs listed in Table 6-3.

The inductor designs have about the same weight but an increasing airgap and hence, number of turns to create a corresponding MMF. Also, volume and Copper ESR increases with increased turns. The ESR increases simply because of the increased current path length and should be as low as possible regarding losses. The volume increases due to the low window factor causing window volume to result in lower weight than core volume. For ferrite cores, a higher number of turns is desirable as the core price is high in opposite to LF iron core designs. Consequently, the choice is a multi-variable tradeoff. Core number 2 is considered favorable for this thesis as it has adequate values for all aforementioned entities. Based on Table 6-2, inductor data for different inductances and otherwise equal operating scenarios can be retrieved with Appendix 5. Suitable inductors for each new inductance are found by inspection. The results are presented in Figure 6.6. For this figure, a maximum air gap of 30mm was set due to fringing considerations. The number of turns was unconstrained. The figure clearly illustrates the advantageousness of low inductance in terms of weight and volume reduction.

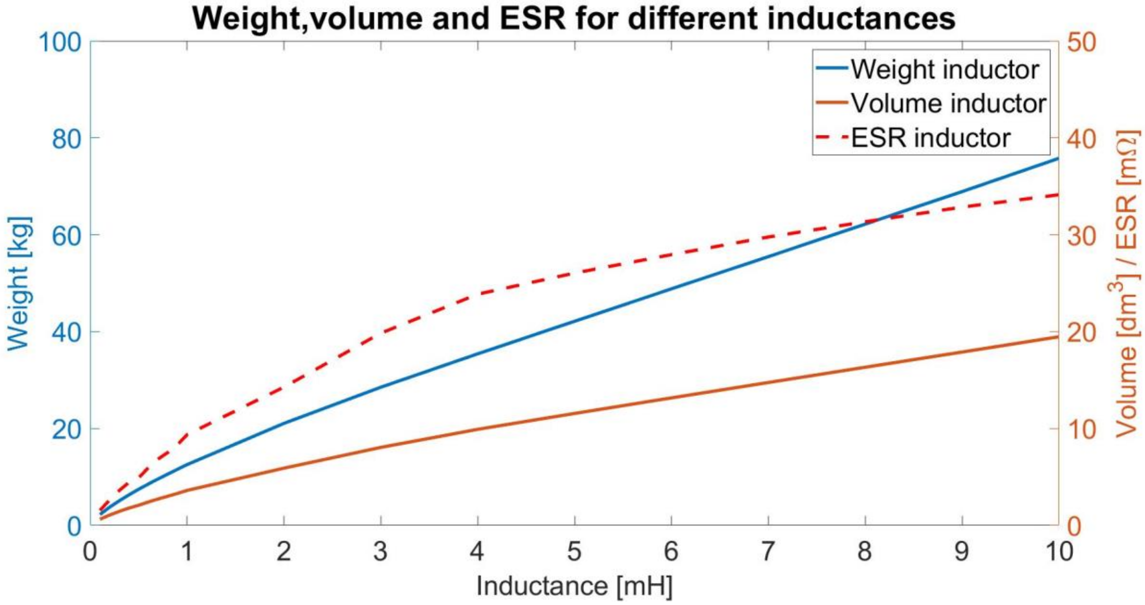

Figure 6.6: Inductor weight, volume and copper ESR for varying L, but otherwise equal to Table 6-2 parameters.

7 COMPONENT COOLING

When designing cooling for electrical components, there are typically 3 methods of doing this. Air cooling, air fan cooling, and liquid cooling. The ABB HES880 converter used for weight references earlier is liquid cooled [123]. This component does also have an IP67 protection code, which means it can be safely installed about anywhere in the ferry. ABB offers corresponding modules that can be, inter alia, installed in existing electrical cabinets requiring less strict IP protection codes. These can be air-cooled [124]. Although, for safety and flexibility in the placement, the semiconductors will be assumed liquid cooled for this thesis. According to talks with industry, there will be an existing internal liquid cooling system in the ferry for, inter alia, the battery. The FC system will certainly also have a cooling system, but this might be an external system based on seawater. The internal cooling system does typically use a freshwater-glycol solution at 40°C which will be assumed for this thesis.

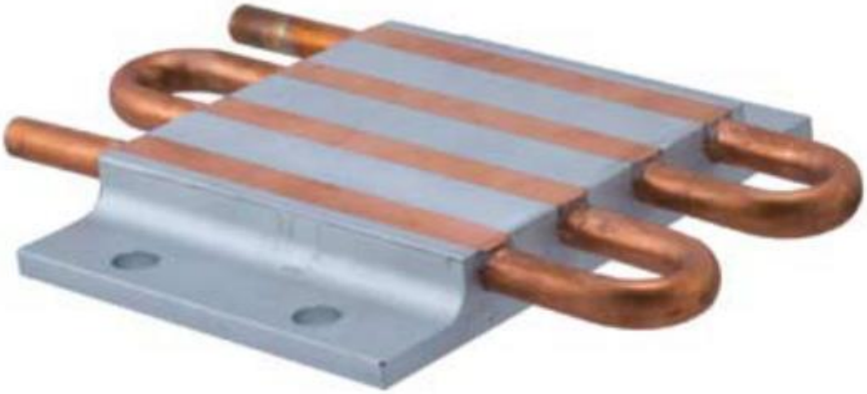

Figure 7.1: A four-passed liquid cooler with copper and aluminum from Ohmite [125].

When choosing a liquid cooled heatsink more correctly referred to as a cold plate, the industry recommends using a noble metal such as copper to prevent corrosion of the heatsink. This is desirable when there are several other components sharing the cooling system that might contain corroding substances. Also, the thermal resistance must be low, and a relatively high price on the cooling plate can be justified. This is because if the thermal resistance is too high, then extra semiconductor devices need to be paralleled to sustain acceptable junction temperature in the devices. Inter alia, for SiC, this would lead to a considerable extra expense of 800NOK per MOSFET and around 60NOK for a suitable driver circuit, and added complexity [126], [127].

This is, fortunately, not an issue, as several producers provide cold plates with thermal resistivity options below 0.02K/W [125], [128]. Ohmite's heatsink is four-passed and copper-tubed, as shown in Figure 7.1. It has a thermal resistance of 0.018K/W at the nominal flow rate and pressure drop. The thermal resistance graph is shown in Figure 7.2. The weight is 0.8kg, and the price is approximately 700NOK at Mouser [125]. The surface is considered big enough to mount two SiC MOSFETs and one SiC Schottky diode. This corresponds to the semiconductors of one leg in the IBC. The resulting power requirement for the assumed mounting roughly leads to a temperature increase of 5-11°C from case to coolant based on Table 5-1 datasheet values. For comparison, one IGBT module on the same liquid cooler leads to a temperature increase up to 12°C. The temperature increase is considered acceptable for both cases.

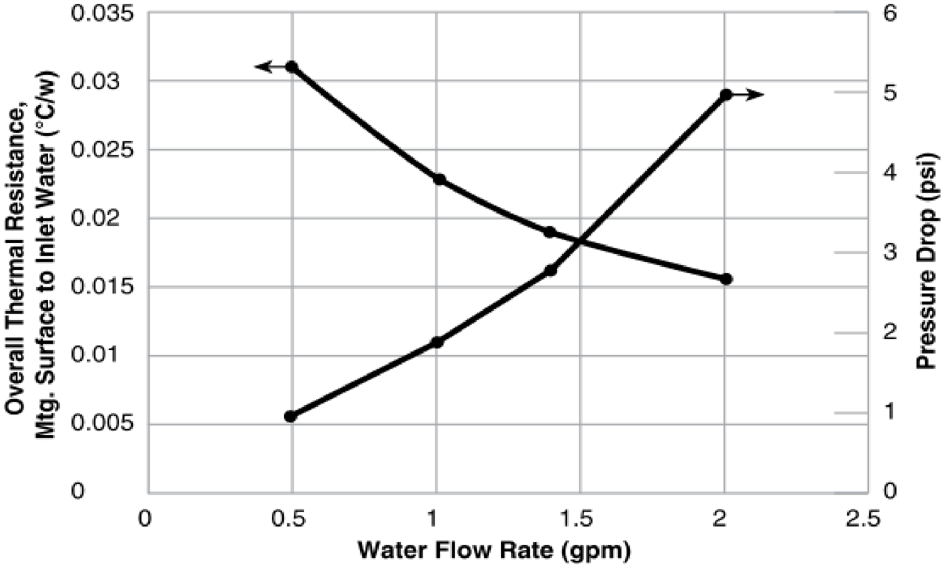

Figure 7.2: The thermal resistance and pressure drop in the liquid cooler as a function of water flow rate[125].

If the thermal resistivity of the liquid cooler is desired lower, then Wakefield-Vette offers one that has a nominal thermal resistance as low as 0.004K/W but has a weight and cost of approximately 5kg and 2500NOK respectively [128], [129]. For comparison with fan cooling, a heatsink from ABL can achieve a thermal resistance of around 0.06K/W assuming a heatsink temperature of 60°C and cooled air at 2m/s[130]. The weight of such a component can be estimated to nearly 6kg. This shows the feasibility of utilization of a liquid cooling system when it is available, especially if the price of semiconductors is high.

For the capacitor, the ESR is 2mΩ resulting in a loss right under 2W, assuming the same ripple as for the discussed 1.2μF full speed scenario. With a thermal coefficient of 1.4K/W, there is no need for external cooling [118]. For the inductor at 100kHz, 0.5mH phase inductance results in below 7% inductor current ripple at full speed, leading to below 24.5mT flux ripple which is not listed or even extrapolate-able in the datasheet [120]. Flux ripple does only decrease at lower power levels. Hence, the core losses are negligible for all power levels. Furthermore, the inductor ESR was determined to be 4.1mΩ. For a maximum current of 65A, this leads to 17.3W of ESR losses per coil. These losses are significant in terms of efficiency, but natural convection is considered sufficient. Consequently, no external cooling need, in addition to natural convection, is considered necessary for the passive components.

8 RESULTS AND DISCUSSION

8.1 FINAL RESULTS

Table 8-1: A summary of the price, weight, and volume of the investigated entities in the different sections

Entity	Price [NOK]	Weight [g]	Volume [cm^3]
SiC MOSFET [39]	800	negligible	negligible
SiC MOSFET driver [127]	60	negligible	negligible
SiC Schottky [38]	Not yet available, see next row	negligible	negligible
Corresponding: 2x SiC Schottky [109]	1100	negligible	negligible
Corresponding IGBT module [113]	1000	340	190
Heatsink [125]	700	805	300
Phase inductor 0.5mH	-	7450	2100
Power capacitor 10μF	-	350	524

The base-case in this thesis is the 6-ph uncoupled IBC with part-load operation implemented. For this case, variables summarized in Table 8-1 is utilized. Two paralleled devices of SiC MOSFET and one SiC Schottky for each IBC leg was determined necessary. Also, one liquid cooler was considered optimal for each phase leg. Consequently, the total weight and volume of the suggested converter are 49.9kg and 14.9liter. If considering the casing weight of this converter, IP67 is considered most viable as it allows placement anywhere on the ferry. The industry then suggests that a 30liter quadratic 2mm thick aluminum box should be adequate for weight estimations. Using the weight density of aluminum of 2.8g/cm^3 and simple geometry, the weight of the casing equals 3.3kg, and the total weight of the converter equals 53.2kg. Wiring, additional piping for the cooling system, and miscellaneous smaller components will add further weight, but this is not feasible to estimate. Thus, the total weight of the 6 FC converters is 319.2kg. The volume of the converters included the casing is 180liter.

In terms of efficiency, the considerable losses are the semiconductor losses found to be 3.48kW. Under same conditions phase inductance, ESR is causing phase losses of 17.3W. Hence the total loss is 3.58kW, causing an efficiency of 98.2%. This is the worst-case efficiency for all operating scenarios, occurring at full speed. The worst-case losses during maneuvering, is 457W assuming only one of the two parallel switches are used for the semiconductors. For the inductors, losses are now down to 0.56W per phase. Hence, the efficiency is 98.9%. The losses during docking are considered unfeasible to attain without practical testing of the components. The calculated losses show that a high efficiency can be expected with this converter. However, a more thorough investigation of the losses should also be done in laboratory experiments.

8.2 DISCUSSION

8.2.1 Comparison to a 100kHz boost converter and 5kHz base-case operation

1-ph part-load operation is equivalent to a standard boost converter. From Figure 2.9 and static model inspection with 1ph part-load operation, it can be found that the maximum ripple now occurs at EOL conditions for docking. Using the same phase inductance, the ripple is now found to be 17.2% for the FC current. This ripple is 6.72 times as high as it was with the part-load 6-ph worst-case. Hence, the phase inductance must be increased 6.72 times to achieve the same ripple, resulting in an inductance of 3.36mH. 2.56% ripple is verified with the static Simulink model for this inductance. The boost converter currents are shown in Figure 8.1, and created with the static Simulink model under 1-ph operation.

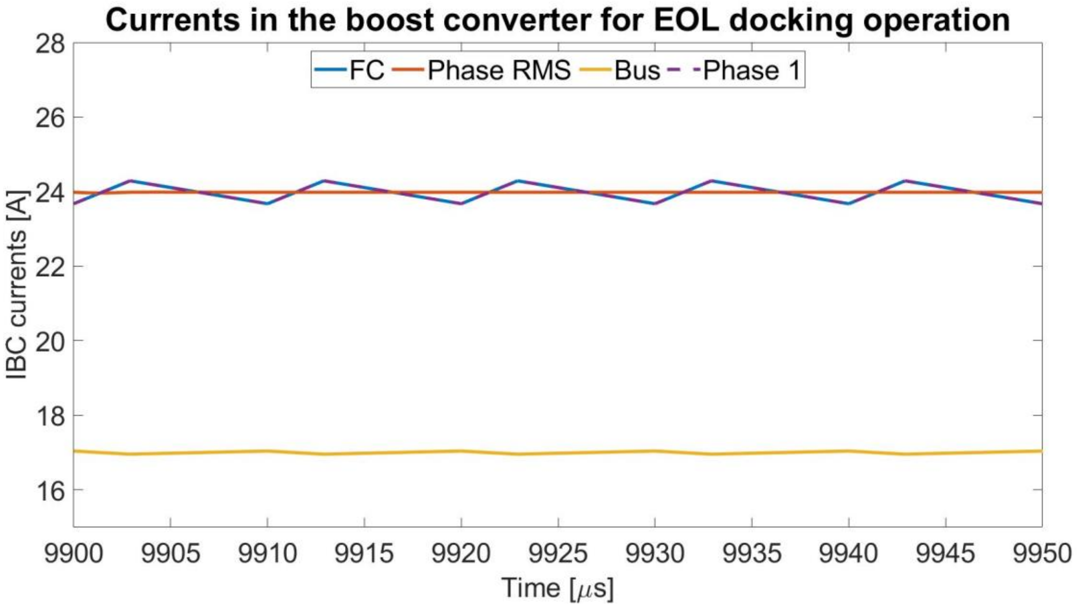

Figure 8.1: Currents of significance for boost converter operation under EOL docking for 3.36mH inductance, 100kHz.

The same inductor design algorithm from Appendix 5 is now utilized, but one inductor must now handle the entire FC current itself. Hence the required inductor current is 392A, and the required inductance is 3.36mH. Then the inductor would weight about 1200kg with a maximum inductor airgap of 30mm assumed. To give boost topology the benefit of the doubt, the maximum air gap is unrestricted. For 10cm airgap, the weight is then 550kg. The minimum weight occurs at airgaps around 30cm at 470kg. It should be noted that this air gap is hardly viable. Based on these estimations, the resulting weight of the inductors in the 6 converters will be in the range of 2.8-7.2 tons. This clearly shows the advantageousness of IBC utilization, and that non-interleaved topologies are unfavorable for the converter under the restrictions decided in this thesis.

5kHz switching frequency is interesting as this was the highest feasible operating frequency found with market-available Si components. Utilizing 5kHz as the switching frequency, analysis is equal to that of 100kHz switching frequency when the inductance is 20 times higher. Hence, the inductance needs to be increased to 10mH, but the analysis is otherwise the same. This can also be verified with the static Simulink model. Then, the weight is already found to be about 78kg per phase from Figure 6.6. This equals a total inductor weight of 2.8 tons for 6 converters. It should, however, be noted that for 5kHz, a material with higher maximum flux density and wiring that allows higher fill factor can be utilized. Consequently, the weight and volume might be lower, but is still expected to be intolerably high. Hence, high-frequency operation must also be considered necessary to gain an adequate inductor weight. A weight comparison of the total inductor weights estimated for the ferry is shown in Table 8-2.

Table 8-2: Total inductor weight for the 6 200kW converters power conditioning the given ferry application under different scenarios.

Investigated scenario	**Weight of inductors for six 200kW converters**
Base-case	268.2kg
100kHz boost	2800-7200kg
Base-case with Si components	2800kg

Inductances of these sizes will also contribute to high losses. Inter alia, the ESR for the 100kHz boost converter will result in losses of 1kW. Moreover, the capacitor voltage ripple will also further increase in any of these two scenarios. It is not further investigated as neither of the scenarios is considered realizable. This section makes an important observation. The ABB HES880 is a Si-based topology. The weight references found in section 2.2 is, therefore, assumingly too optimistic for the operating constraints assumed in this thesis. As further will be discussed, the operating conditions assumed in this thesis might be too strict. The constraints and other modifications for further weight reduction will now be discussed.

8.2.2 Alternative assumable weight-reducing constraints

For this thesis, the constraints determined in collaboration with IFE was 2% current ripple, which is typical guidelines for 1kHz and above. 2.56% is considered acceptable as a worst-case. The ripple requirements typically decrease for higher frequency [131]. A 100kHz 6-ph IBC has a current ripple of 600kHz, and the ripple requirements for the FC might be lower for this ripple frequency. Inter alia, a comparable 100kHz 6-ph IBC reports that FC ripple must be kept below 10% [81]. It must also be considered that the ripple will be further reduced as CM-filters are required. If the ripple, in reality, could be twice the magnitude, the inductance could be halved. Thus, the inductor could be almost half the weight, as shown in Figure 6.6. As the inductors cause the majority of the weight, this would lead to an extensive weight reduction of the converter. This may, however, lead to DICM behavior which require a more complex analysis. For scenarios with static operation points in DICM, reducing the number of phases to reach CICM may prove favorable.

Several other aspects could also be considered reducing the weight of the converter in terms of phase inductance reduction. One is to only operate the IBC at one of the ripple cancellation points during docking and let the battery absorb or provide the remaining power. Then the ripple requirements could be dimensioned for the maneuvering phase. This would lead to a significant weight reduction but may also require DICM analysis. Utilizing a higher operating frequency for low power operation during docking may also prove desirable. This would reduce the required inductance without DICM concerns, but switching losses will increase substantially, and core losses may also become considerable. Keeping half the FC stacks turned off during docking would also ease the ripple requirement without any DICM concern. Frequently turn on and turn off fuel cells are, however, known to cause aging as well.

8.2.3 Other advantageous topology variations

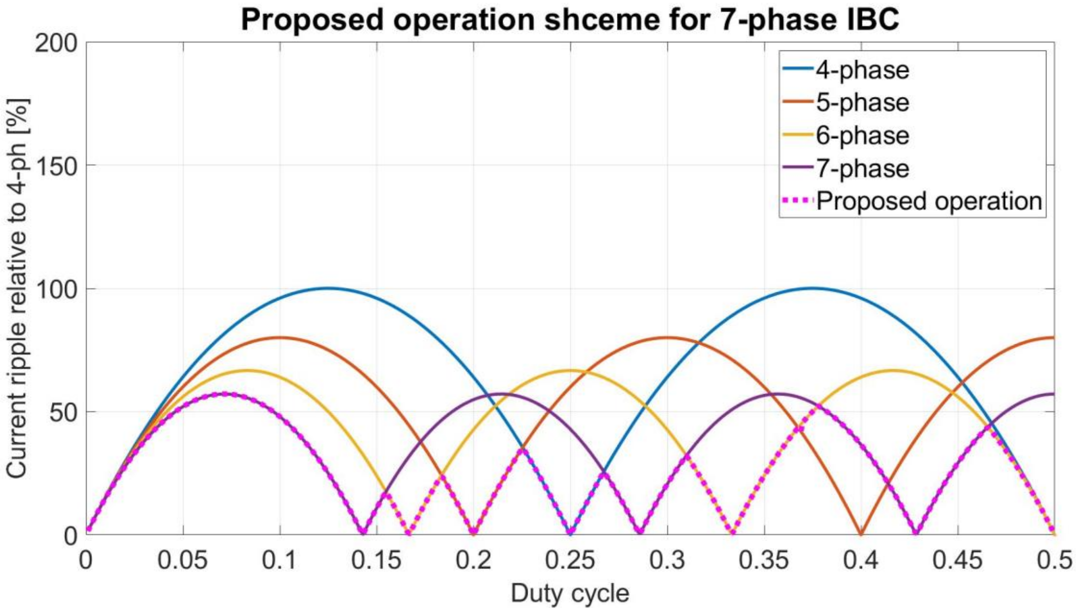

Figure 8.2: A proposed part-load operation scheme for a 7-ph IBC in CICM.

As was shown in Figure 3.7, a 5-ph part-load operating converter will have the same current ripple as a 6-ph part-load operating one for the dimensioning docking scenario. Hence, as other suitable SiC components become market-available, the 5-ph IBC might be the preferred choice for this specific application. Furthermore, a 7-ph IBC could improve the ripple substantially utilizing a part-load scheme. Such a scheme is shown in Figure 8.2 generated with Appendix 1. Comparing this scheme to a proposed 6-ph scheme, as shown in Figure 3.8, it is observable that the maximum phase ripple reduction is 31%. This could contribute to a considerable weight reduction. It does, however, require extra semiconductor components and adds further complexity. Also, DICM can become an issue for static operation.

Besides changing the number of phases, more complex topology variations can be investigated. Soft switching can be implemented, heavily reducing losses for high frequencies. This can, inter alia, reduce the need to only one SiC MOSFET per phase in the 6-ph IBC and also allow further increased frequency operation. The increased frequency will allow for weight reduction. Soft switching is also reported to reduce EMI and could, therefore, be beneficial as EMI is expected to be an issue with the given ferry application [10], [36], [81], [93]. A soft switching auxiliary circuit can be designed using only passive components and diodes, as previously shown in Figure 2.13. If utilization of Si components is to be attempted, the soft switching scheme can prove very advantageous in terms of allowed operating frequency due to high switching losses discovered in section 5.3.

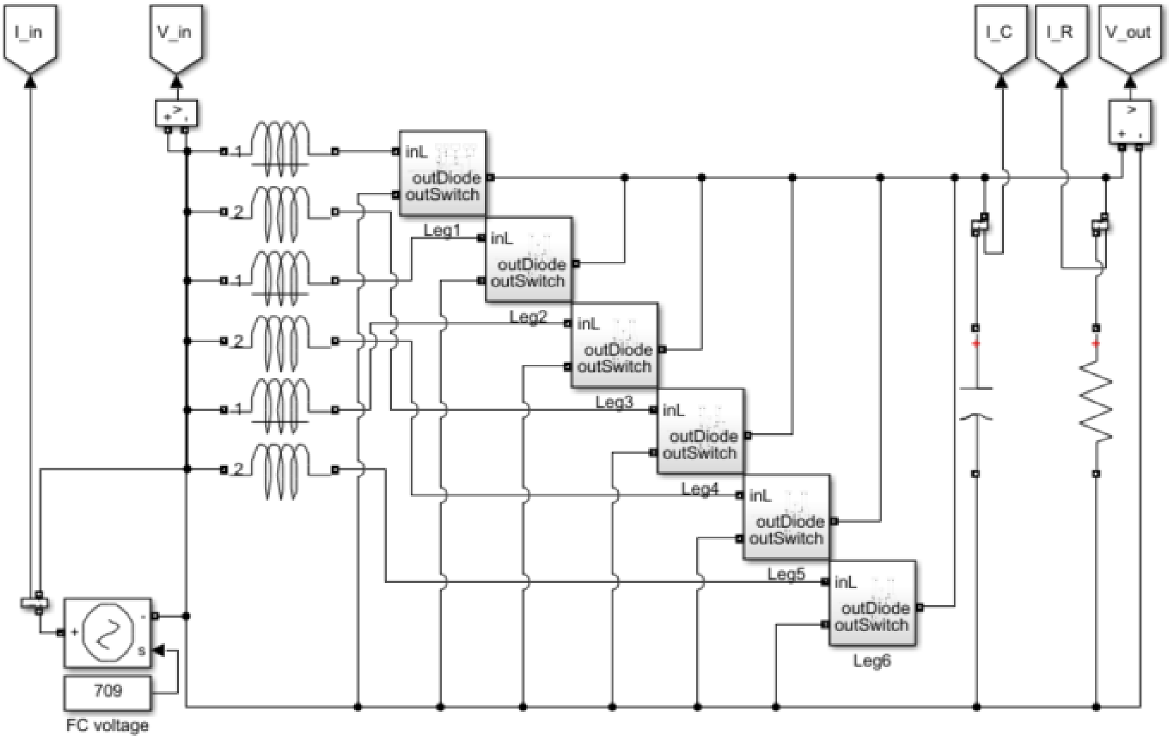

Figure 8.3: A MATLAB model that utilizes pairwise coupled coils.

The coupled coil topology is another interesting option. The coils can be coupled directly or inversely, but inversely is of major interest as it can reduce the DC-flux in the core quite drastically. Looking at the base-case, the core weight makes up 4.5kg out of the 7.45kg from Appendix 5. For this thesis and in general other FC applications, the size of the core is mainly caused by DC-flux. One comparable source reports a possible core weight reduction of 94% [81] using coupled coils versus uncoupled for the same inductance. However, the FC current ripple may increase due to altered waveforms. Several coupling coefficients and coupling configurations can be investigated. Coupled coils are possible to investigate in Simulink with the mutual inductance block offering mutual inductance between 2 or 3 different inductors. Figure 8.3 shows a proposed coupled coils scheme where the phases with adjacent currents are coupled together. However, analysis of this scheme requires sophisticated control. Analysis of the inductor design is also advanced. Coupled topologies might also lead to increased EMI [67]. For this thesis, both the soft switching and coupled coil topologies are considered out of scope due to complexity. They can, however, be an interesting topic for further work.

9 CONCLUSION

This thesis shows that a 6-ph SiC-based IBC with a part-load scheme is a favorable converter for a 200kW high-speed hydrogen ferry application. Initially, the requirement of galvanic isolation was considered due to fault and EMI protection. Several interviews with industry did, however, reveal that the recommendation was an un-isolated topology as already strict safety requirements made most of the galvanic isolation advantages superficial. Dimensioning of CM and other EMI reduction filters and measures was found to be necessary.

Investigation of an existing high-speed ferry in Trondheim revealed that the load profiles mainly were static for the converter. Besides, FCs should not ramp up power faster than 10% per second due to poor FC dynamics. Hence, the existing battery on the ferry must handle the majority of the dynamic transients. Further, the PowerCell Sweden MS100 datasheet revealed that FC behavior could be quite accurately estimated by a three-piece linearization, but voltage degradation caused by aging of the cell requires operation over a wide duty cycle range for the static load profiles. Several numbers of phases were investigated for the IBC, but a 6-ph configuration was considered most feasible in terms of available components and ripple. Implementing a part-load scheme was considered favorable for further ripple reduction and efficiency increase for lower power levels. Both 5-ph and 7-ph configurations were also found to be favorable solutions that should be investigated for similar applications.

While an ideal static model was trivial, the development of a dynamic model in Simulink showed that the control structure of such a model must be advanced. Assuming a perfect control system, the dynamic analysis showed that the dimensioning ripple operation for both the inductor and capacitor happens during static operation intervals. Further, it was found that a part-load scheme can be implemented in terms of simple “if” logic and that using this during non-static operation may lead to stability concerns. Both the static model and theory was used to find the dimensioning ripple levels for both the input current and the capacitor voltage. Both ripples were desired to be at a maximum of 2% during long-term operation but allowed to exceed these restrictions for shorter periods. A maximum ripple of 2.56% near EOL conditions during docking operation was determined acceptable leading to a phase inductance of 0.5mH. Full speed operation was dimensioning for the capacitor, leading to a minimum capacitance of 1.2μF for 2% output voltage ripple.

The market available SiC components found viable was a 1700V MOSFET and a Schottky diode, both produced by Wolfspeed. DP simulations of the components in LTspice showed correct waveforms but resulted in switching losses under half of what was listed in the datasheets. The datasheet losses were based on experimental testing and therefore considered more realistic. Consequently, the datasheets were used in dimensioning of the components designing for a junction operating temperature of 100°C and a casing temperature of 40°C based on liquid cooling. It was found that one Schottky diode and two MOSFETs in parallel was sufficient for each leg. Si market-available alternatives were investigated but found unsatisfactory as they only allow 5kHz operation, which would lead to too high weight. Liquid coolers weighing 805g per IBC leg were found which lead to adequate thermal performance of the converter.

A market-available 10μF capacitor was found most suitable due to the RMS capacitor current constraint. The developed inductor algorithm was used to find a suitable 0.5mH inductor. Combined with datasheets, it was shown that the only loss that is not negligible for the passive components are inductor ESR. The semiconductors were found to dominate the losses while the inductors were found to dominate the weight and volume. Including an IP67 casing, the total weight and volume of the converter were 319.2kg and 180liter respectively, while the lowest efficiency was 98.2% at full speed EOL conditions. The inductor design algorithm developed showed that either using SiC in a standard boost topology or substituting SiC with the investigated Si components would lead to a weight of almost 3 tons. Hence, both IBC structure and high-frequency components utilization are considered necessary for a satisfactory weight of the converter under the ripple requirements assumed in this thesis.

10 FURTHER WORK

As mentioned in the scope of this thesis, only a possibility study is executed. Hence, there are several interesting topics for further work listed below.

Control system and dynamics: As this thesis was written from a power electronics point of view, the control system for the converter was not properly developed as it turned out to be very complex. Developing a feasible control system is a necessity for the realization of the converter. However, FCs are complex, and an actual component or at least a realistic model of the FC stack should be utilized to determine the viability of such a control system. Also, the control system must be able to handle DICM for the start-up of the FC stacks in addition to CICM. Practical experiments should be executed to determine the feasibility of the control system due to high complexity. The problematic is briefly discussed in section 4.2.1. The converter in dynamic behavior should then be analyzed for the given control system.

Harmonic analysis: Harmonic analysis was one of the industry's biggest concern regarding the realization of an FC-powered energy system in this ferry. Especially CM noise from the engine-inverter was a major concern. FCs are sensitive to EMI, and the fact that FCs have to be grounded due to safety worsen the experienced EMI. Also, the FC converter investigating are utilizing SiC components which are infamous for high EMI generation. This was discussed in section 2.4. Research should be carried out on the EMI tolerance of the fuel cell, and further EMI filters and other EMI suppression techniques should be dimensioned according to practical experiments. Again the complexity is expected to be too high for simulations to be sufficient.

Component verification: This thesis has carried out rough estimates in terms of volume, weight, and efficiency. However, as shown in 5.2 ideal simulations can prove insufficient for semiconductor components, especially in fast switching components such as SiC due to parasitic elements. The inductor algorithm is also a rough approximation. Hence, an inductor should be built, or at least a thorough model in Maxwell or COMSOL should be carried out to achieve realistic results. The capacitor should also be experimentally tested.

Cooling system: The assumptions used for the cooling system in this thesis is based on talks with industry, and quite rough. Dimensioning and investigation of a cooling system realizable for the ferry were out of scope for this thesis, but it is required to determine the actual thermal performance conditions of the other components.

Advanced topologies: Both the soft switching and coupled coils topology variations are an interesting topic for further investigation. According to theory, significant benefits in terms of weight, volume, and efficiency can be achieved. The complexity is, however, very high, and there is not considered feasible to extract useful data out of simulations on these topologies before a more complex model is developed. Still, this is a very interesting topic for further work.

The thesis shows that the choice of the FC converter can be of great significance in the emerging hydrogen ferries. Hopefully, this thesis can be a foundation for further research on the area. If another master's thesis were trailing this thesis, the recommended work would be developing and investigating the most feasible IBC control system, including both DICM and CICM behavior. Such a control system is a necessity for the investigation of many of the other topics mentioned in further work. The eventual researcher continuing this work is encouraged to contact the author of this thesis, as code, model, and knowledge happily will be shared.

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12 APPENDIX

12.1 APPENDIX 1: CURRENT RIPPLE GENERATION CODE

This code shows in different sections how plots and theory verification has been executed in this thesis for inductor current ripple. Minor adjustments are required to generate all the different scenarios investigated.

```
%% generate part-load plot with constant current
clear all;
V0=1000; %vout
L=1e-3;
Iin=350;
Nphmax=7;
fs=100e3;
acc=0.001;
data=zeros(2000,5);
count=0;
D=0;
Irip=0;
for Nph=1:1:Nphmax
    for ph=1:1:Nph
        for sweep=0:acc:1/Nph
            if count<1000
            D=D+acc;
            count=count+1;
            Non=ceil(D/(1/Nph));
            d=(D-(Non-1)/Nph)*Nph;
            IripA=V0/(L*fs)*(Non-Nph*D)/(1)*1/(Nph)*d; %change
(1) to (1-D) if Vin is used as V
            Irip=IripA/Iin*100/(0.7143/100)*4;
            %part-load optimum alternative
%             if
(Irip<data(count,3)||data(count,3)==0)&&Nph<6&&Nph>3
%                 data(count,3)=Irip;
%             end
%             if Irip<data(count,4)||data(count,4)==0
%                 data(count,4)=Irip;
%             end
            if (Irip<data(count,4)||data(count,4)==0)
                data(count,4)=Irip;
            end
            if (Nph==6&&D>=0.37)
            data(count,4)=Irip;
```

```
            end

            data(count,1)=D;
            data(count,2)=Irip;
            end
        end
    end

    if Nph>3
    data(data(:,2)==0,:)=[];
    plot(data(:,1),data(:,2),'LineWidth',3);
    set(gca,'FontSize',25);%axis font size
    xlabel('Duty cycle','FontSize',25);
    ylabel('Current ripple relative to 4-ph
[%]','FontSize',25);
    title('Proposed operation shceme for 7-phase
IBC','FontSize',30);
    axis ( [ 0 0.5 0 200])
    grid on;
    grid minor;
    hold on;
    else
    end
    D=0;
    count=0;
end
plot(data(:,1),data(:,4),'m:','LineWidth',5);
legend({'4-phase','5-phase','6-phase','7-phase','Proposed
operation'},'FontSize',25);
hold off;

%% fining avrg ripple from 6-ph and 6-ph part operation (run
above script first)
count=0;
sumconv=0;
sumpart=0;
for i=0:acc:0.5
    count=count+1;
    if i>=0.191&&i<=0.294
    sumconv=sumconv+data(count,2);
    sumpart=sumpart+data(count,4);
    end
end
avrgconv=sumconv/count;
avrgpart=sumpart/count;
```

```
imporv=avrgpart/avrgconv;

%% Generate standard simple current ripple plot
clear all;
V0=1000; %vout
L=1e-3;
Iin=350;
Nphmax=6;
fs=100e3;
acc=0.001;
data=zeros(2000,5);
count=0;
D=0;
for Nph=1:1:Nphmax
    for ph=1:1:Nph
        for sweep=0:acc:1/Nph
            if count<1000
            D=D+acc;
            count=count+1;
            Non=ceil(D/(1/Nph));                    %rounds to
next integer
            d=(D-(Non-1)/Nph)*Nph;
            IripA=V0/(L*fs)*(Non-Nph*D)/(1)*1/(Nph)*d; %change
(1) to (1-D) if Vin is used as V
            Irip=IripA/Iin*100/(0.7143/100);
            data(count,1)=D;
            data(count,2)=Irip;
            end
        end
    end

    if Nph>0        %chose how many Nph included in plot
    data(data(:,2)==0,:)=[];
    plot(data(:,1),data(:,2),'LineWidth',3);
    set(gca,'FontSize',25);%axis font size
    xlabel('Duty cycle','FontSize',25);
    ylabel('Current ripple [%]','FontSize',25);
    title('Current ripplefor different IBCs relative to a
standard boost converter','FontSize',30);
    legend({'Boost','2-phase','3-phase','4-phase','5-phase','6-
phase'},'FontSize',25);   %'NumColums',2,'Location','north',
    axis ( [ 0 1 0 100])
    grid on;
    grid minor;
    hold on;
```

```
    else
    end
    D=0;
    count=0;
end
%% standard with XOL current (change 0.97 to 0.% aging)
clear all;
voltage=[450, 405, 360, 300];
current=[0  ,  20, 125, 445];
VtoIB= fit(voltage'*2,current', 'linearinterp');
VtoIX=fit((voltage'-50*0.97)*2,current', 'linearinterp');
V0=1000; %vout
L=0.5e-3;
Nphmax=6;
fs=100e3;
acc=0.001;
data=zeros(2000,5);
count=0;
D=0;
for Nph=1:1:Nphmax %plotter for hver part-load N
    for ph=1:1:Nph %# bulker
        for sweep=0:acc:1/Nph %generer data for hver bulk
            if count<1000
            D=D+acc;
            Vin=V0*(1-D);
            Iin=VtoIX(Vin);                    %extracting
current
            count=count+1;
            Non=ceil(D/(1/Nph));                         %rounds to
next integer
            d=(D-(Non-1)/Nph)*Nph;
            IripA=V0/(L*fs)*(Non-Nph*D)/(1)*1/(Nph)*d; %change
(1) to (1-D) if Vin is used as V
            Irip=IripA/Iin*100;
            data(count,1)=D;
            data(count,2)=Irip;
            data(count,3)=Vin*Iin;
            end
        end
    end

    if Nph>3        %chose how many Nph included in plot
    data(data(:,2)==0,:)=[];
    yyaxis left
    plot(data(:,1),data(:,2),'LineWidth',3);
```

```
    set(gca,'FontSize',25);%axis font size
    xlabel('Duty cycle','FontSize',25);
    ylabel('Current ripple [%]','FontSize',25);
    title('Current ripple and power for 97% aged FC
stacs','FontSize',30);
   %'NumColums',2,'Location','north',
    axis ( [ 0.225 0.5 0 10])
    grid on;
    grid minor;
    hold on;
    else
    end
    D=0;
    count=0;
end
yyaxis right
 plot(data(:,1),data(:,3)/1e3,'LineWidth',3); %looks crooked
due to 3p approx for FC curve
 ylabel('Power [kW]','FontSize',25);
 axis ( [ 0.225 0.5 0 250])
    legend({'4-phase','5-phase','6-
phase','Power'},'FontSize',25,'Location','north','Orientation',
'horizontal');
 hold off;


%% Part-load with BOL current
voltage=[450, 405, 360, 300];
current=[0  ,  20, 125, 445];
VtoIB= fit(voltage'*2,current', 'linearinterp');
VtoIX= fit((voltage'-50)*2,current', 'linearinterp');

clear all;
V0=1000; %vout
L=1e-3;
Iin=350;
Nphmax=6;
fs=100e3;
acc=0.001;
data=zeros(2000,5);
count=0;
D=0;
for Nph=1:1:Nphmax %plotter for hver part-load N
    for ph=1:1:Nph %# bulker
        for sweep=0:acc:1/Nph %generer data for hver bulk
```

```
            if count<1000
            D=D+acc;
            count=count+1;
            Non=ceil(D/(1/Nph));                    %rounds to
next integer
            d=(D-(Non-1)/Nph)*Nph;
            IripA=V0/(L*fs)*(Non-Nph*D)/(1)*1/(Nph)*d; %change
(1) to (1-D) if Vin is used as V
            Irip=IripA/Iin*100/(0.7143/100)*4;
            %part-load optimum
            if
(Irip<data(count,3)||data(count,3)==0)&&Nph<6&&Nph>3
                data(count,3)=Irip;
            end
            if Irip<data(count,4)||data(count,4)==0
                data(count,4)=Irip;
            end
            data(count,1)=D;
            data(count,2)=Irip;
            end
        end
    end

    if Nph>3
    data(data(:,2)==0,:)=[];
    plot(data(:,1),data(:,2),'LineWidth',3);
    set(gca,'FontSize',25);%axis font size
    xlabel('Duty cycle','FontSize',25);
    ylabel('Current ripple','FontSize',25);
    title('Relative Current ripple in % for constant phase
inductance, voltage and current','FontSize',30);
    legend({'4-phase','5-phase','3-phase','4-phase','5-
phase'},'FontSize',25);   %'NumColums',2,'Location','north',
    axis ( [ 0 0.5 0 100])
    grid on;
    grid minor;
    hold on;
    else
    end
    D=0;
    count=0;
end
% data(data(:,3)==0,:)=[];
% data(data(:,4)==0,:)=[];
plot(data(:,1),data(:,3),'c:','LineWidth',5);
```

```
plot(data(:,1),data(:,4),'m:','LineWidth',5);
hold off;
```

Appendix 1

12.2 APPENDIX 2: VOLTAGE RIPPLE GENERATION CODE

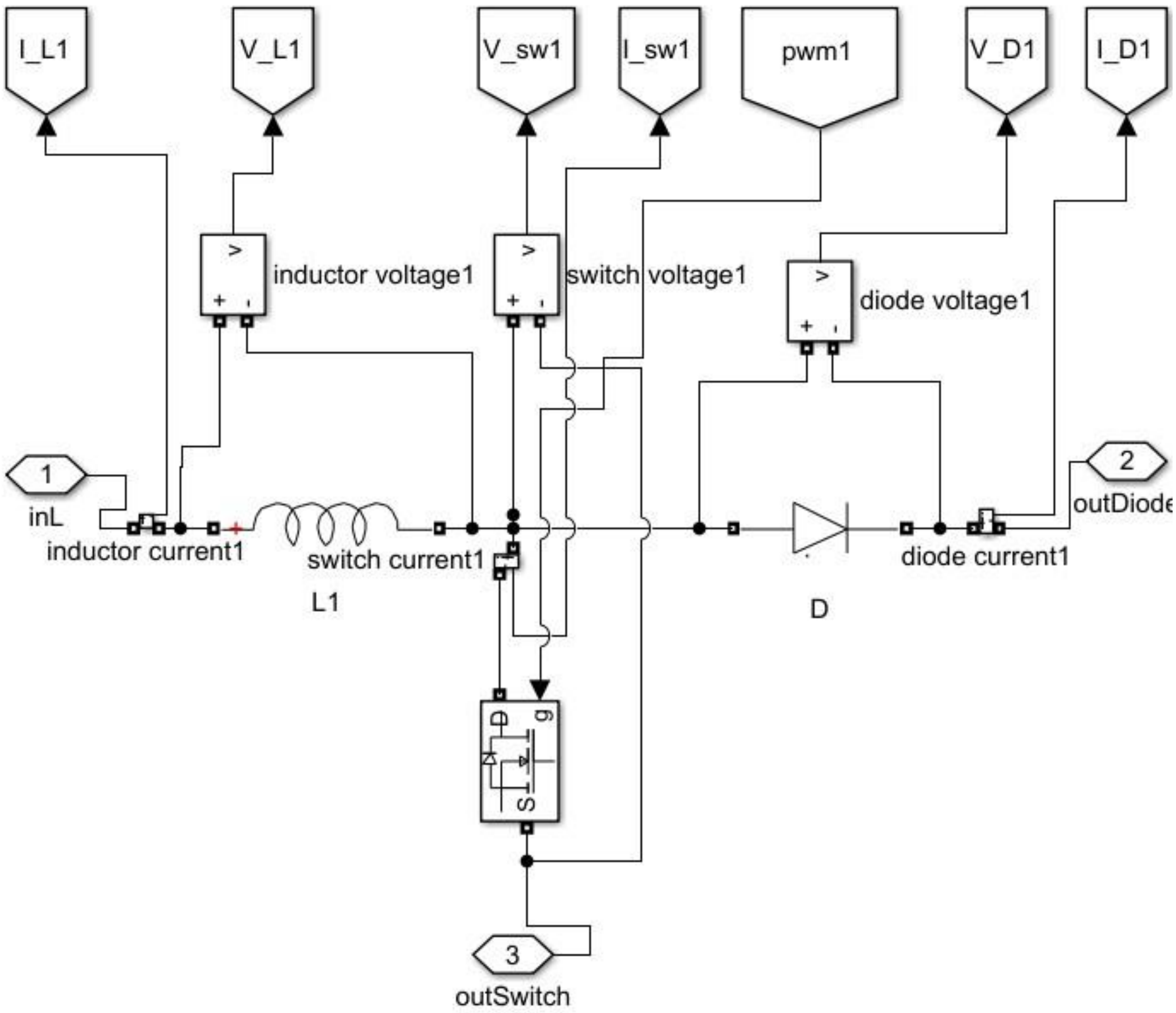
This code shows in different sections how plots and theory verification has been executed in this thesis for output voltage ripple. Minor adjustments are required to generate all the different scenarios investigated.

```
%% simple capacitor ripple plot
clear all;
V0=1000; %vout
C=1.2e-6;   %at D= 0.422
Power=200e3;
Req=V0^2/Power;
Nphmax=6;
fs=100e3;
acc=0.001;
data=zeros(2000,5);
count=0;
D=0;
Vrip=0;
for Nph=1:1:Nphmax
    for ph=1:1:Nph
        for sweep=0:acc:1/Nph
            if count<1000
            D=D+acc;
            count=count+1;
            Non=ceil(D/(1/Nph));                    %rounds to
next integer
            d=(D-(Non-1)/Nph)*Nph;
            VripA=V0*d*(1-d)/(fs*Req*C*Nph^2*(1-D));
            Vrip=VripA/V0*100;
            %part-load optimum
            if (Vrip<data(count,4)||data(count,4)==0)
                data(count,4)=Vrip;
            end
            if (Nph==6&&D>=0.37)
            data(count,4)=Vrip;
            end
            data(count,1)=D;
            data(count,2)=Vrip;
            end
```

```
        end
    end

    if Nph>3
    data(data(:,2)==0,:)=[];
    plot(data(:,1),data(:,2),'LineWidth',3);
    set(gca,'FontSize',25);%axis font size
    xlabel('Duty cycle','FontSize',25);
    ylabel('Voltage ripple [%]','FontSize',25);
    title('Relative voltage ripple at full
speed','FontSize',30);
    axis ( [ 0 0.5 0 10])
    grid on;
    grid minor;
    hold on;
    else
    end
    D=0;
    count=0;
end
data(data(:,4)==0,:)=[];
plot(data(:,1),data(:,4),'m:','LineWidth',5);
legend({'4-phase','5-phase','6-phase','proposed
operation'},'FontSize',25,'Orientation','horizontal','Location'
,'north');
hold off;
%% capacitor ripple plot worst case and increasing power
clear all;
voltage=[450, 405, 360, 300];
current=[0  ,  20, 125, 445];
VtoIX=fit((voltage'-50)*2,current', 'linearinterp');
V0=1000; %vout
C=2e-5;
Nphmax=6;
fs=100e3;
acc=0.001;
data=zeros(2000,5);
count=0;
D=0;
Vrip=0;
for Nph=1:1:Nphmax
    for ph=1:1:Nph
        for sweep=0:acc:1/Nph
            if count<1000
            Vin=V0*(1-D);
```

```
            Iin=VtoIX(Vin);
            Power=Vin*Iin;
            Req=V0^2/Power;
            D=D+acc;
            count=count+1;
            Non=ceil(D/(1/Nph));                    %rounds to
next integer
            d=(D-(Non-1)/Nph)*Nph;
            Vrip=V0*d*(1-d)/(fs*Req*C*Nph^2*(1-D)); %change (1)
to (1-D) if Vin is used as V
            data(count,1)=D;
            data(count,2)=Vrip;
            data(count,3)=Vin*Iin;
            end
        end
    end

    if Nph>3
    data(data(:,2)==0,:)=[];
    yyaxis left
    plot(data(:,1),data(:,2),'LineWidth',3);
    set(gca,'FontSize',25);%axis font size
    xlabel('Duty cycle','FontSize',25);
    ylabel('Voltage ripple [%]','FontSize',25);
    title('Voltage ripple relative to a standard boost
converter','FontSize',30);
    axis ( [ 0 1 0 10])
    grid on;
    grid minor;
    hold on;
    else
    end
    D=0;
    count=0;
end
yyaxis right
 plot(data(:,1),data(:,3)/1e3,'LineWidth',3); %looks crooked
due to 3p approx for FC curve
 ylabel('Power [kW]','FontSize',25);
 axis ( [ 0.225 0.5 0 250])
legend({'4-phase','5-phase','6-phase','6-phase','5-phase','6-
phase'},'FontSize',25,'Orientation','horizontal','Position','no
rth');
hold off;
```

12.3 APPENDIX 3: PHASE LEG STRUCTURE



Appendix 3

12.4 APPENDIX 4: LOSS CALCULATION CODE

This code shows in different sections how conduction losses can be generated based on Simulink simulations.

```
%% load variables
clc;
clear all;
load('I_L1.mat')
load('I_L2.mat')
```

```
load('I_C.mat')
load('I_D1.mat')
load('I_sw1.mat')
%% define values
switch_type=        'MOSFET';
% MOSFET or IGBT
ESR_L1=             0.5e-3;
%==L2,L3...
ESR_C=              0.5e-3;
N_phases=           2;
Vdrop_D1=           0.5;
Ron_sw1=            0.5e-3;
%==R_l for IGBT
Vdrop_sw1=          0.5;
%only for IGBT
%% inductors
%assuming inductor loss equal in all phases as it should be

inst_loss_L=N_phases*ESR_L1*(I_L1(2,:)).^2;
%instantaneous loss value
avrg_loss_L=inst_loss_L;                          %creating
vector
avrg_loss_L(:)= mean (inst_loss_L);               %assingning
average loss vector value

plot (I_L1(1,:),inst_loss_L,I_L1(1,:),avrg_loss_L);

%% capacitor
inst_loss_C=ESR_C*(I_C(2,:)).^2;
avrg_loss_C=inst_loss_C;
avrg_loss_C(:)= mean (inst_loss_C);

plot (I_C(1,:),inst_loss_C,I_C(1,:),avrg_loss_C);

%% diodes
inst_loss_D=N_phases*Vdrop_D1*I_D1(2,:);
avrg_loss_D=inst_loss_D;
avrg_loss_D(:)= mean (inst_loss_D);

plot (I_D1(1,:),inst_loss_D,I_D1(1,:),avrg_loss_D);
%% switch MOSFET (standard)
switch switch_type
    case 'MOSFET'
        inst_loss_sw=N_phases*Ron_sw1*I_sw1(2,:).^2;
        avrg_loss_sw=inst_loss_sw;
```

```
        avrg_loss_sw(:)= mean (inst_loss_sw);

        plot (I_sw1(1,:), inst_loss_sw, I_sw1(1,:),
avrg_loss_sw);
    case 'IGBT'
%% IGBT
        inst_loss_sw=N_phases*(Ron_sw1*I_sw1(2,:).^2 +
Vdrop_sw1*I_sw1(2,:));
        avrg_loss_sw=inst_loss_sw;
        avrg_loss_sw(:)= mean (inst_loss_sw);

        plot (I_sw1(1,:), inst_loss_sw, I_sw1(1,:),
avrg_loss_sw);
    otherwise
        disp('invalid switch')
end

%% SEMCON LOSSES
inst_loss_D=N_phases*Vdrop_D1*I_D1(2,:);
%didode losses
avrg_loss_D=inst_loss_D;
avrg_loss_D(:)= mean (inst_loss_D);

switch switch_type
    case 'MOSFET'
%switch losses
        inst_loss_sw=N_phases*Ron_sw1*I_sw1(2,:).^2;
        avrg_loss_sw=inst_loss_sw;
        avrg_loss_sw(:)= mean (inst_loss_sw);
    case 'IGBT'
        inst_loss_sw=N_phases*(Ron_sw1*I_sw1(2,:).^2 +
Vdrop_sw1*I_sw1(2,:));
        avrg_loss_sw=inst_loss_sw;
        avrg_loss_sw(:)= mean (inst_loss_sw);
    otherwise
        disp('invalid switch')
end

%semcon losses
inst_loss_semcon=inst_loss_D+inst_loss_sw;
avrg_loss_semcon=avrg_loss_D+avrg_loss_sw;

plot (I_sw1(1,:), inst_loss_semcon, I_sw1(1,:),
avrg_loss_semcon);
```

```
%amplitude of instantaneous is equal as losses occur in off/on
respectively
%% Passive elements LOSSES
inst_loss_L=N_phases*ESR_L1*(I_L1(2,:)).^2;           %inductor
losses
avrg_loss_L=inst_loss_L;
avrg_loss_L(:)= mean (inst_loss_L);

inst_loss_C=ESR_C*(I_C(2,:)).^2;                       %capacitor
losses
avrg_loss_C=inst_loss_C;
avrg_loss_C(:)= mean (inst_loss_C);

inst_loss_passive=inst_loss_L+inst_loss_C;             %passive
losses
avrg_loss_passive=avrg_loss_L+avrg_loss_C;

plot (I_sw1(1,:), inst_loss_passive, I_sw1(1,:),
avrg_loss_passive);

%% total conduction losses
inst_loss_D=N_phases*Vdrop_D1*I_D1(2,:);
%didode losses
avrg_loss_D=inst_loss_D;
avrg_loss_D(:)= mean (inst_loss_D);

switch switch_type
    case 'MOSFET'
%switch losses
        inst_loss_sw=N_phases*Ron_sw1*I_sw1(2,:).^2;
        avrg_loss_sw=inst_loss_sw;
        avrg_loss_sw(:)= mean (inst_loss_sw);
    case 'IGBT'
        inst_loss_sw=N_phases*(Ron_sw1*I_sw1(2,:).^2 +
Vdrop_sw1*I_sw1(2,:));
        avrg_loss_sw=inst_loss_sw;
        avrg_loss_sw(:)= mean (inst_loss_sw);
    otherwise
        disp('invalid switch')
end

%semcon losses
inst_loss_semcon=inst_loss_D+inst_loss_sw;
avrg_loss_semcon=avrg_loss_D+avrg_loss_sw;
```

```
inst_loss_L=N_phases*ESR_L1*(I_L1(2,:)).^2;         %inductor
losses
avrg_loss_L=inst_loss_L;
avrg_loss_L(:)= mean (inst_loss_L);

inst_loss_C=ESR_C*(I_C(2,:)).^2;                    %capacitor
losses
avrg_loss_C=inst_loss_C;
avrg_loss_C(:)= mean (inst_loss_C);

inst_loss_passive=inst_loss_L+inst_loss_C;          %passive
losses
avrg_loss_passive=avrg_loss_L+avrg_loss_C;

inst_loss_tot=inst_loss_semcon+inst_loss_passive;   %total
losses
avrg_loss_tot=avrg_loss_semcon+avrg_loss_passive;

plot (I_sw1(1,:), inst_loss_tot, I_sw1(1,:), avrg_loss_tot);
```

Appendix 4

12.5 APPENDIX 5: INDUCTOR DESIGN ALGORITHM

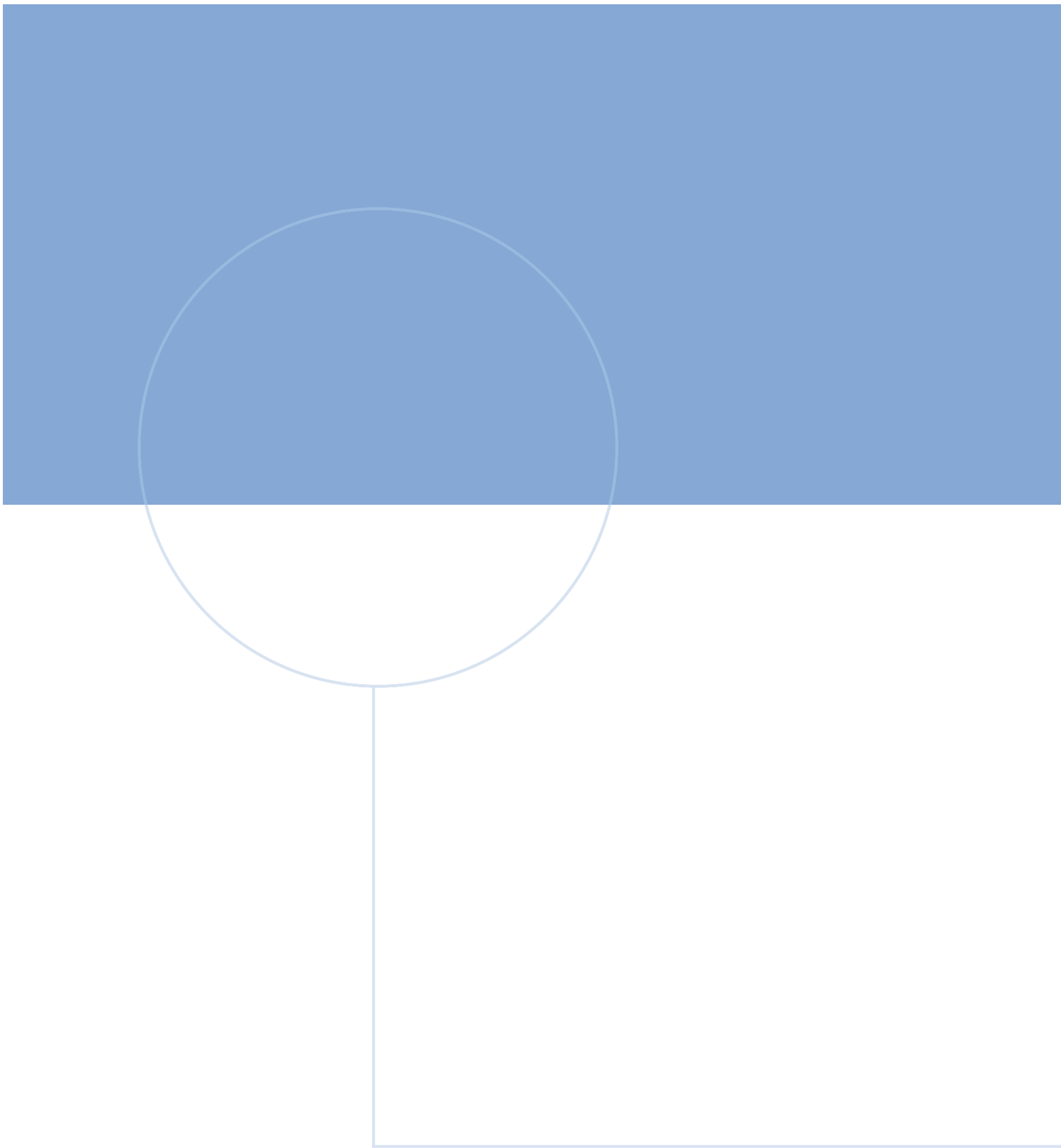
This code finds suitable inductor designs based on inductor design theory. The most suitable inductor has to be chosen by the generated “gapdata” array by inspection.

```
%% Optimalization algorithm Inductor
%constants
my0=1.257e-6;       %per m
rhoFer=4750;        %kg/m3
rhoCu=8960;         %kg/m3
resCu=2.2e-8;       %resistiivty in ohm/m at 100*C
kfill=0.3;          %litz, assuming completely filling window
with 0.3 times area of copper

L=0.5e-3;           %desired inductance
J=3e6;              %A/m2
Irms=392/6;            %current, DCcurrent=ACcurrent
Bmax=0.35;           %setting maximum B-field

%intializing
gapdata=zeros(1000,11);
count=0;
optcount=0;
```

```
for gap= 1e-3:1e-3:100e-3
for N=1:1:500
count=count+1;

%given directly by N
Aw=Irms*N/(J*kfill);    %winding window area
RgapL=N^2/L;            %desired gap for specified L

% finding gap and flux param
Acore=L*Irms^2/(Irms*N*Bmax);      %setting core cross section
based on stored energy requirement
width=sqrt(Acore/1.5);          %optimum core cross section
[Hart 2010]
Rgapwide=
gap*0.5/((width+gap*0.5/2)*(1.5*width+gap*0.5/2)*my0);
%determining gap reluctance using square box approximation,
total air gap distr50-50 on wide and slim E-tags
Rgapslim=
gap*0.5/((width*0.5+gap*0.5/2)*(1.5*width*0.5+gap*0.5/2)*my0);
Rgap= Rgapwide+0.5*Rgapslim;
%Req of the magnetic circuit
flux=N*Irms/Rgap;       %determining actual flux
Bfield=flux/(Acore);    %determining actual B-field
Lact=N^2/Rgap;          %fdetermining actual L
check1 = Rgap/RgapL;    %should be one, constraint between 0.98
og 1.2
check2 = kfill*Aw*Acore*Bfield*J/(Lact*Irms^2);     %core
energy coparison, should be 1
check3 = Acore/Aw;  %core cross section compared to window
area, optimum around 1.07 [Hart 2010]

%finding weight
w=width;
rhoFer=4750;        %kg/m3
rhoCu=8960;         %kg/m3
wwin=sqrt(Aw/2.5);      %assuming window lengths 1:2.5
hwin=2.5*sqrt(Aw/2.5);
totAcore=2*((w+wwin)*(2*w+hwin)-(wwin*hwin));   %Finding core
Area neglecting Airgap
totVcore=1.5*w*totAcore;
totAcu=((2*wwin+w)*(2*wwin+1.5*w)-(w*1.5*w));   %Finding copper
volume, assuming filling window and evently distributed 0.3
totVcu= totAcu*hwin*0.3;
totVol=totVcore+totVcu/0.3;     %total volume
```

```
WeightCore=rhoFer*totVcore;     %finding weights
WeightCu=rhoCu*totVcu;
totWeight=WeightCore+WeightCu;

%finding ESR
MLT=(2*(w+wwin)+2*(1.5*w+wwin))*N;
resCu=2.2e-8;       %resistiivty in ohm/m at 100*C
ESR=MLT*resCu/(Aw/N);      %core loss neglible due to low AC
flux

%finding a rough price estimate
NOKpercorekg=116;        %NOK/kg, based on kg price of large
quanta sale of existing 3F3 E-cores
NOKpercukg=60;           %typical copper price.
NOKcore=NOKpercorekg*WeightCore;
NOKcu=NOKpercukg*WeightCu;
NOKtot=NOKcore+NOKcu;


if(check1>0.98&&check1<1.2&&check2>0.98&&check2<102&&Bfield<0.4
)
optcount=optcount+1;
gapdata(optcount,1)=gap;            %lgap
gapdata(optcount,2)=N;              %#turns
gapdata(optcount,3)=width;          %bredde
gapdata(optcount,4)=check1;         %Rgap/RgapL, must
epsilon(0.98,1.2)
gapdata(optcount,5)=Bfield;         %Bfield, must <0.4T
gapdata(optcount,6)=ESR;            %Equal series resistance
inductor
gapdata(optcount,7)=check3;         %Acore/Aw,
gapdata(optcount,8)=totVol;         %total inductor volume
gapdata(optcount,9)=totWeight;      %total inductor weight
gapdata(optcount,10)=WeightCore;    %total core weight
gapdata(optcount,11)=NOKtot;        %best-case price estimate
gapdata(optcount,12)=check2;
end

end
end
```

Appendix 5



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