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A Chopper Offset-Stabilized Operational Amplifier in 22nm FD-SOI

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A Chopper Offset-Stabilized Operational Amplifier in 22nm FD-SOI

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Master of Science in Electronics Systems Design and Innovation
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Summary

A chopper offset-stabilized amplifier has been designed. The design has been analyzed using Monte Carlo simulations with mismatch and process variations enabled on typical transistor models on a schematic netlist. A 22nm transistor technology has been used but the IO transistors available in the 22nm technology are used all over to be able to operate at a supply voltage of $1.8\,\mathrm{V}$. The design is able to maintain an offset voltage below $130\,\mu\mathrm{V}$ at a 4 sigma level, for temperatures between $-40\,^{\circ}\mathrm{C}$ and $85\,^{\circ}\mathrm{C}$. The chopping frequency is $2\,\mathrm{MHz}$ and a continuous-time approach has been used for ripple-reduction. Flicker noise is reduced and is together with the offset voltage translated into a ripple voltage at the chopping frequency. The output noise is kept below $323\,\mu\mathrm{V}$ for all conditions and temperatures. The Gain-Bandwidth product is above $1\,\mathrm{MHz}$ and the DC-gain is above $100\,\mathrm{dB}$ for all conditions. All capacitors used, have been kept on an ideal level.

The design features a rail-to-rail input and output stage. The input stage is implemented using complementary differential pairs and gm-equalization is implemented with a current switch. A class-AB output stage has been designed to be able to deliver currents up to $10\,\mathrm{mA}$. With a $10\,\mathrm{mA}$ load current, the output is able to swing up to $1.55\,\mathrm{V}$ and down to $0.210\,\mathrm{V}$ with a supply voltage of $1.8\,\mathrm{V}$.

Sammendrag

En chopper offset-stabilisert forsterker har blitt designet. Designet har blitt analysert ved bruk av Monte Carlo simuleringer på skjema-nivå med påførte mismatch og prosessvariasjoner. En 22nm transistor teknologi har blitt brukt, men IO-transistorene som er tilgjengelig i den aktuelle teknologien har blitt brukt for å være kompatibel med en 1.8V forsyningsspenning. Designet er i stand til å opprettholde en offset-spenning under $130\,\mu\mathrm{V}$ på et 4 sigma nivå, for temperaturer mellom $-40\,^{\circ}\mathrm{C}$ og $85\,^{\circ}\mathrm{C}$. Chopping frekvensen er $2\,\mathrm{MHz}$ og et tidskontinuerlig filter er brukt for å redusere rippelet. Flicker støy blir redusert og blir sammen med offset, mikset opp til en rippel spenning rundt chopping frekvensen. Utgangs-støyen holder seg under $323\,\mu\mathrm{V}$ for alle simulerte forhold og temperaturer. Gain-Bandwidth produktet er over $1\,\mathrm{MHz}$ og DC-gainet er over $100\,\mathrm{dB}$ for alle simulerte forhold. Alle kondensatorer som er brukt i designet oppfører seg ideelt.

Designet inneholder et inngangstrinn og utgangstrinn som kan operere fra rail til rail. Inngangstrinnet er bygd opp rundt komplementære differensielle par og utligning av transkonduktansen er gjort ved hjelp av en strøm-bryter. Et klasse-AB utgangstrinn har blitt designet for å være i stand til å levere en strøm på opp til $10\,\mathrm{mA}$. Med en $10\,\mathrm{mA}$ last, er utgangsspenningen i stand til å svinge opp til $1.55\,\mathrm{V}$ og ned til $0.210\,\mathrm{V}$ med en forsyningsspenning på $1.8\,\mathrm{V}$.

Preface

The work in this thesis was carried out during Spring 2019 at NTNU, Trondheim. I would like to thank my supervisors Johnny Bjørnsen from Silicon Labs and Professor Trond Ytterdal at NTNU, for their support throughout this project. I am grateful for the time they have spent teaching and guiding me during the design, simulation and writing. I have really learnt a lot from them during this period.

Thanks to my family and friends for supporting me throughout my studies.

Lastly, I would like to thank my girlfriend Saskia for her patience and love.

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Abbreviations

A_{V0}	:	DC-gain
BW	:	Signal Bandwidth
C_L	:	Load capacitance
C_M	:	Miller capacitor
CM	:	Common-mode
CMFB	:	Common-mode Feedback
CMOS	:	Complementary metal–oxide–semiconductor
f_{ug}	:	unity-gain frequency
GBW	:	Gain Bandwidth Product
$I_{out,max}$	:	Maximum output current
ICMR	:	Input common-mode range
MHNMC	:	Multipath Hybrid Nested Miller Compensation
MOSFET	:	Metal–oxide–semiconductor field-effect transistor
OCMR	:	Output common-mode range
OPA	:	Operational Amplifier
OTA	:	Operational Transconductance Amplifier
PM	:	Phase-margin
PSD	:	Power Spectrum Density
V_{os}	:	Offset voltage
VDD	:	Supply voltage

Chapter 1

Introduction

When an amplifier is used as part of a high-accuracy measurement system, low-offset amplifiers are required. Such systems can involve strain gauges, thermocouples, piezoelectric sensors, Hall sensors and photodiodes that typically produces a small and slow-moving signal that needs to be sensed as accurately as possible [4]. Developments in CMOS technology has made it economically favourable to integrate advanced mixed-signal systems and is, therefore, the preferred technology for many applications. The downside of CMOS technology is its rather poor performance in terms of the offset voltage. The typical input offset for a CMOS amplifier can be several millivolts [5] and the flicker noise corner frequency can range from several kHz to tens of kHz [6].

When manufacturing amplifiers in a CMOS process, there will be part-to-part variable offset due to random and systematic processing effects [7], which is discussed in chapter 2.2.2. Consequently, when devices are designed to fulfil a certain specification there is a probability for some devices to not uphold the criteria stated in the specification. The ratio between functional and defective devices can be termed yield, and a high yield is desirable. Statistical modelling of the manufacturing process can be used to describe the yield and expressed in the form of a sigma level. The design done in this work aims at keeping the offset below $1\,\mathrm{mV}$ and the noise level below $500\,\mu\mathrm{V}$ [RMS] where the output noise is defined as including both device noise and ripple. This must be fulfilled at a sigma level of 4, at temperatures ranging from -40°C to 85°C. This will result in a yield of $99.38\,\%$ and an estimated 6210 defective parts when 1 million are produced.

In [8], a relationship between random variations of transistor parameters and area is described. Using that relationship it is possible to show that increasing the transistor area leads to smaller offset voltages. However, in many cases, the area needs to be increased extensively to be able to fulfil a specification at a sigma rating of 4. As increasing the area is expensive and impractical, this is not a viable option in many cases. Another approach

is to use calibration and trimming to reduce the offset. The downside of this approach is that the offset voltage also shows a temperature and time dependency [4]. A one-time calibration procedure will not be able to account for this effect, pointing to the need for a continuous correction method. One such method is the chopping technique. The offset and the flicker noise is up-modulated to a higher frequency and can be looked upon as converting a DC-signal to an AC ripple voltage, occurring at the chopping frequency. This technique will be discussed in detail in chapter 2.3.1.

One major challenge with this technique is keeping the magnitude of the ripple at an acceptable level. This ripple can be regarded as unwanted noise and can be separated from the input signal by setting the chopping frequency higher than the signal bandwidth, but it has to be filtered out somehow. One way to filter it out is to insert a low-pass filter on the output, that lets the inputs signal through and filters the ripple. The downside of this method is that the bandwidth for the amplifier will be too severely limited for many applications. A technique termed chopper offset-stabilization [9] is introduced in chapter 2.3.2 to get around this limitation by having two parallel gain paths. The usage of two gain paths requires some specialized frequency compensation schemes [4], which will be discussed in chapter 2.5.

Auto-zeroing is another technique that can be used to dynamically compensate for the offset [10]. This is a sampling-based technique which measures the offset during one sampling phase and subtracts it during another phase. Because of the sampling, noise is folded back into the baseband and causes more in-band noise [10] when compared to a chopper implementation. On the other hand, the auto-zero technique does not produce the large ripple associated with the chopper technique. Based on the increased baseband noise associated with the auto-zeroing technique, this work focuses on the usage of chopping.

Several techniques have been presented in the literature to deal with the ripple voltage. A continuous-time (CT) integrator is used in [1] to filter it out. This can potentially require large capacitors to obtain a low enough cut-off frequency. In [9] a switched capacitor notch-filter is used. This is very power efficient but comes with the cost of a residual offset and complexity. This work is based on operating at a relatively large chopping frequency of $2\,\mathrm{MHz}$, when compared to [1] [9]. This is enabled by the 22 nm technology used, characterized by having low power loss at high switching speed. For this work, the IO-transistors available in the 22 nm technology are used all over to be able to operate at a supply voltage of $1.8\,\mathrm{V}$. The high chopping frequency leads to relaxed requirements for the cutoff-frequency when a CT integrator is used for ripple reduction. Based on this, it is decided to use a CT integrator to reduce the ripple, implemented as part of a design very similar to the work done in [1], but operating at a higher frequency.

Another aspect of using a high chopping frequency and the usage of chopper offset-stabilization is that a high signal bandwidth can be realized. This work features a signal bandwidth of $1\,\mathrm{MHz}$. The capacitors used for compensation provide additional damping of the ripple.

With the ongoing trend of lowered supply voltages, it gets important to maximize the

dynamic range. The amplifier design covered in this work employs a rail-to-rail input and output stage at a supply voltage of $1.8\,\mathrm{V}$, which is the voltage rating for the technology. To be useful in general purpose applications, an amplifier should be able to deliver current to a load with an acceptable efficiency in terms of its quiescent current, such as the one shown in [5]. Because of this, the amplifier features a class-AB output stage, implemented as part of the summation stage of a folded cascode as shown in [2].

The specification for the amplifier designed in this work is summarized in table 1.1.

VDD	$1.8\,\mathrm{V}$
GBW	$1\,\mathrm{MHz}$
A_{V0}	$100\,\mathrm{dB}$
C_L	$50\,\mathrm{pF}$
$I_{out,max}$	$10\,\mathrm{mA}$
V_{os}	$< 1\,\mathrm{mV}$
$ICMR$	Rail-To-Rail
$OCMR$	Rail-To-Rail
$V_{out,noise}$	$500\,\mu\mathrm{V}$ [RMS]

Table 1.1: Specification

Chapter 2

Theory

2.1 Literature Review

Similar to many techniques used in today's circuit design, the chopping technique originally originates from the days of vacuum-tube based designs. The technique was first developed in the late 1940s [11]. In the early 1980s, fully monolithic amplifiers employing the chopping technique started to be available commercially [12]. The constant improvement and development of CMOS process technologies enable the realization of highly integrated and high-quality switches. In the mid-2000s designs with a very good noise-power ratio was reported in [9], and a commercial product based on this design is the Texas Instruments OPA333 [13].

The idea of using a multipath amplifier architecture to obtain a high gain-bandwidth product with minimal noise in a chopper amplifier was presented in [14]. The co-author of this paper, Johan H. Huijsing has been a central figure in the development of chopper-stabilized amplifiers and amplifier design in general. Techniques such as gm-compensated differential pairs, multipath hybrid nested miller compensation, feedforward compensation and class-AB biasing schemes stem from this authors contribution in the field of amplifier design.

2.2 Non-idealities in an operational amplifiers

The behaviour of an operational amplifier (opamp) can be modelled with different amounts of realism to portray the behaviour of a real device. A list of ideal characteristics can

be combined to form what is called an ideal opamp model [15]. By introducing non-ideal effects a more realistic and accurate model is obtained. Two of these non-ideal effects is discussed in detail in the following sections, Offset voltage due to random device mismatch, and device noise.

2.2.1 Offset Voltage

The input offset voltage is defined as the differential voltage that must be applied to the input to produce zero output voltage. This offset voltage can be modelled as a voltage source in series with the inverting input of an opamp as shown in figure 2.1.

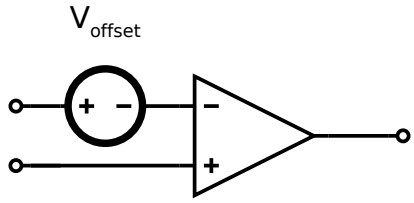

Figure 2.1: Input offset voltage.

In a real device, the offset voltage can never reach zero and is caused by random or systematic effects in the opamp design. Random device mismatch will be discussed in detail in chapter 2.2.2. Systematic variations are caused by systematic errors done during design, manufacturing or packaging [7], and can be avoided. The degree of offset that can be tolerated depends on the application and the required accuracy of the amplifier. It is possible to calibrate and trim the opamp to compensate for the offset but the offset is also found to be temperature dependent which means it can drift over time [1]. One technique to correct for a dynamic offset voltage is presented in chapter 2.3.1. The type of technology that is used to implement the circuit also influences the degree of offset. The offset of an amplifier designed in CMOS technology can in some cases be found to be up to ten times larger compared to a bipolar amplifier [16].

2.2.2 Device mismatch

If identical transistors are fabricated under the same conditions, there will always be random variations in width, length, oxide thickness and doping levels in the transistor channel. These kinds of variations are called random device mismatch. Because of small random variations in transistor parameters, there will also be variations in the drain currents. When referred to the input this results in an offset voltage.

It has been shown [7] that threshold voltage differences ΔV_t and current factor differences $\Delta\beta, \beta = \mu C_{ox}\frac{W}{L}$ are the dominant sources of mismatch in a matched transistor pair and

that they can be viewed as independent random variables. These variations are found to be normally distributed, with a variance inversely proportional to the device area [8], as shown in equation 2.1 and 2.2.

$$\sigma^2(\Delta V_t) = \frac{A_{Vt}^2}{WL} \tag{2.1}$$

$$\sigma^2(\frac{\Delta\beta}{\beta}) = \frac{A_{\beta}^2}{WL} \tag{2.2}$$

These equations show that by increased area usage, the mismatch can be reduced. Chapter 2.3.1 will present a technique to avoid having to increase the area extensively to reduce offset. The equations are valid for closely spaced devices ($< 1\,\mathrm{mm}$) [7].

In the basic building blocks of analog design, the differential pair and the current mirror [17] the effect of mismatch plays out differently. A differential pair can be viewed as current-biased. In this case, the gate-source voltage error is important. For a current mirror which can be looked upon as voltage-biased, the drain-source current error is important. Using a drain current model that is valid for a transistor operating in the saturation region for all inversion levels such as in [18], the variance for the drain-source current error and the gate-source voltage error can be mathematically derived to be the following [7].

$$\sigma^2(\frac{\Delta I_{ds}}{I_{ds}}) = \sigma^2(\frac{\Delta\beta}{\beta}) + (gm/Id)^2\sigma^2(\Delta V_t) \tag{2.3}$$

$$\sigma^2(\Delta V_{gs}) = \sigma^2(\Delta V_t) + \frac{1}{(gm/Id)^2}\sigma^2(\frac{\Delta\beta}{\beta}) \tag{2.4}$$

From this result, it can be seen that in the case of differential pairs, the effect of current factor mismatch can be minimized by providing low overdrive and using a large area to minimize the effect of threshold mismatch. For current mirrors, current factor mismatch can be minimized by using large area and threshold mismatch can be minimized by providing high overdrive.

In many cases, the current-factor error can be neglected when compared to threshold mismatch [7]. With this assumption, a circuit analysis is performed to determine the input-referred offset voltage for a folded cascode, shown in figure 2.2. The operation of this circuit is discussed in detail in section 2.4.2.

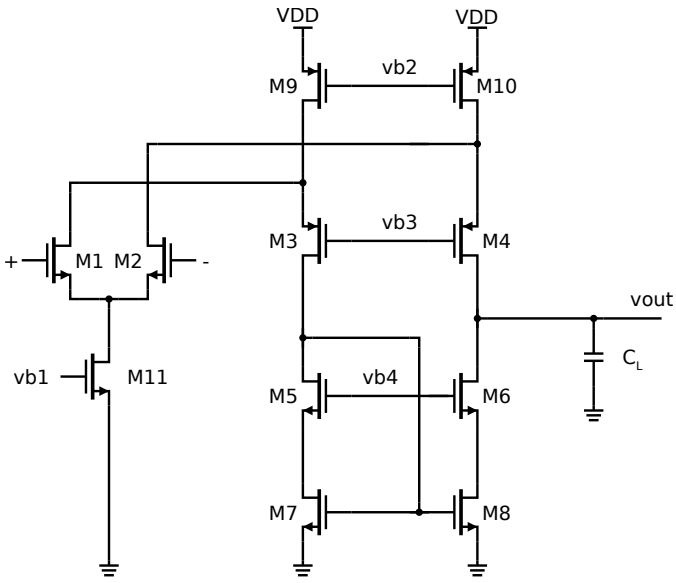

Figure 2.2: Folded cascode.

The variance for the input-referred offset can be found by calculating the gate-source voltage errors for the input pair, calculate the drain-source current errors for the current sources, referring all offsets to the input and then combine the independent sources using sum propagation. The offset for the cascode transistors can be neglected [4], as their contribution will become small when referred to the input.

$$\sigma^2(V_{os}) = \sigma^2(\Delta V_{t1,2}) + (\frac{gm_{7,8}}{gm_{1,2}})^2\sigma^2(\Delta V_{t7,8}) + (\frac{gm_{9,10}}{gm_{1,2}})^2\sigma^2(\Delta V_{t9,10}) \tag{2.5}$$

As can be seen from this analysis, operating all the input transistors in weak inversion (meaning low overdrive) results in reducing the offset. For the current sources and current mirrors, the opposite is true. It will be shown in chapter 2.2.3 that this result also bears true to obtain low thermal noise.

2.2.3 Device noise

A MOSFET transistor contains several sources of noise. Two noise sources will be considered in this work: thermal noise in the channel and flicker noise. Thermal noise is due to the thermal excitation of charge carriers in a conductor [19]. It is proportional to absolute temperature, has a white spectral density and can be modelled as a noise current source in parallel with the transistor and approximated by the following equation.

$$I_d^2(f) = 4kTgm\gamma \tag{2.6}$$

The γ factor is process dependent and has been observed to increase for submicron CMOS technologies [20]. It is also bias sensitive and can depend significantly on the length [21].

Flicker noise is characterized by having a spectral density that is inversely proportional to the frequency. This type of noise can be modelled as a noise voltage source in series with the gate of a transistor and is described by the following equation.

$$\bar{V_i}^2(f) = \frac{K}{WLC_{ox}f} \tag{2.7}$$

Where the constant K is process dependent and W, L, and Cox represent the transistor's width, length, and gate capacitance per unit area [19]. From this equation, it can be seen that by increasing the area, flicker noise is reduced.

The point where the intersection between the flicker noise and the thermal noise occurs is termed the flicker noise corner frequency. This value is bias sensitive and depends on the physical characteristics of the process used [21]. It can be estimated and included in the design process as shown in [21], which can be useful in applications where it should be kept below a certain point as it dominates the lower part of the frequency spectrum.

By assuming zero current at the gate of the transistor, the thermal noise described in equation 2.6 can be referred to the input. This can be done by dividing the term with gm^2, as the transconductance is what defines the gain between the voltage at the gate and the drain current. The transistor itself is now considered noiseless and the equivalent noise of the transistors is applied at the input. The resulting input-referred noise for one single transistor is shown in equation 2.8.

$$\bar{V_i}^2 = \frac{4kT\gamma}{gm} + \frac{K}{WLC_{ox}f} \tag{2.8}$$

This concept can also be used to refer all relevant noise sources in an amplifier stage to the input. The input-referred thermal noise for the folded cascode shown in figure 2.2 is shown in equation 2.9. Noise contributions from the cascode transistors have been neglected.

$$\bar{V_i}^2 = 2V_{n1,2}^2 + 2(\frac{gm_{7,8}}{gm_{1,2}})^2V_{n7,8}^2 + 2(\frac{gm_{9,10}}{gm_{1,2}})^2V_{n9,10}^2 \tag{2.9}$$

Where V_n^2 equals the following.

$$\bar{V_n}^2 = \frac{4kT\gamma}{gm} \tag{2.10}$$

From this result, it can be seen how the thermal noise can be reduced by increasing the transconductance of input transistors and that the opposite is true for the transistors acting as current sources. This can be related to the transistor dimensions, resulting in a high W/L ratio for the input transistors and a low W/L ratio for the current sources. If only considering noise contributions from the input pair and assuming $\gamma = 2/3$, the following estimate is obtained.

$$\bar{V}_i^2 = \frac{16kT}{3gm_1} \tag{2.11}$$

When working with cascaded gain stages it can be shown that by having large gain at the first stage, the gain of the first stage will reduce the noise contributions of the later stages [19]. This illustrates the importance of having low noise and high gain in the first stage of an amplifier and makes it possible to estimate the total noise performance based on the first stage. This also applies for the offset voltage as discussed in chapter 2.2.2.

The concept of noise bandwidth [19] provides a simple way to estimate the total output noise when assuming that the noise source has a completely white characteristic. In the case of a first-order lowpass filter exited by a white noise source, the resulting output noise can be calculated by multiplying the equivalent input-referred noise with the noise bandwidth which is $\pi/2$ times the signal bandwidth. This is shown in equation 2.12.

$$\bar{V}_o^2 = \bar{V}_i^2 BW \tag{2.12}$$

This is useful for doing noise estimates in amplifier design, as the frequency characteristic often can be approximated as a first-order low pass filter. The unity-gain frequency for a folded cascode can be expressed as follows [15].

$$f_{ug} = \frac{gm_1}{2\pi C_M} \tag{2.13}$$

As this expression relates the Miller capacitor and the bandwidth, an useful expression can be derived that relates the Miller capacitor with the output noise. This way, a noise estimate can be obtained based on the sizing of the Miller capacitor. If assuming that the input differential pair is the major contributor to thermal noise and using the concept of noise bandwidth, the following relation is obtained.

$$\bar{V}_o^2 = \frac{16kT}{3gm} BW = \frac{4kT}{3C_M} \tag{2.14}$$

2.3 The Chopping Technique

2.3.1 Chopper Amplifier

A chopper amplifier utilizes the chopping technique to up-modulate offset and 1/f noise away from DC. The simplest model for a chopper amplifier consists of two synchronized choppers [10] in addition to the amplifier itself. This can be seen in figure 2.3.

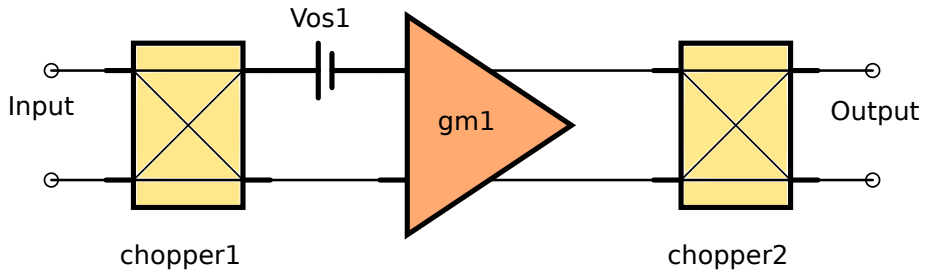

Figure 2.3: Chopper amplifier.

The choppers can be implemented with 4 switches as shown in figure 2.4. It can be driven by a clock signal with two complementary phases, here illustrated as CLK1 and CLK2.

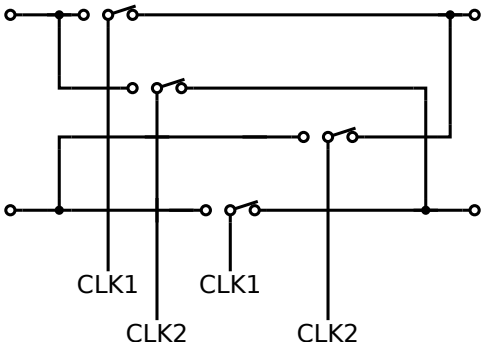

Figure 2.4: A chopper.

The first chopper is placed in front of the input of the opamp. This will move the input signal up to the odd harmonics of the chopping frequency f_{chop} and can be viewed as performing conversion of a DC signal to an AC signal. This up-modulated signal will then be amplified by the amplifier gm_1 which is having an offset voltage V_{os1}. The second chopper is placed on the output of the amplifier and will down-modulate the amplified input signal to the original frequency and up-modulate the offset and 1/f noise of the opamp to the chopping frequency. The input signal and the offset voltage have now been separated in frequency. The offset voltage is still present but now in the form of an AC ripple. This operation is illustrated in the frequency spectrum in figure 2.5.

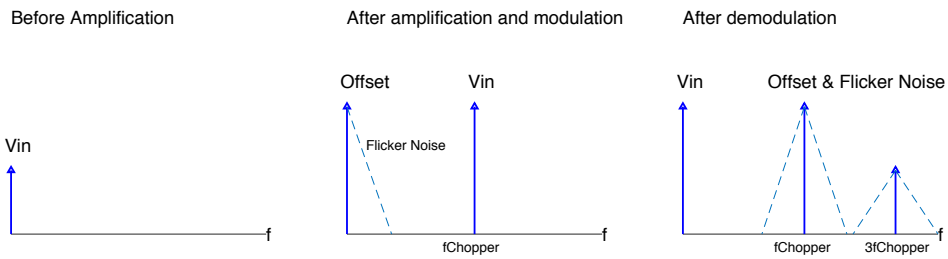

Figure 2.5: Chopper amplifier - frequency spectrum.

Depending on the parameters used in the design, the ripple consisting of frequency components at the chopping frequency and beyond, can in many cases become relatively large compared to the input signal and demand some form of ripple reduction. Different techniques for performing ripple reduction have been reported in [9] and [1]. A continuous-time approach can be implemented as the two-stage amplifier shown in figure 2.6. The effective DC gain of the amplifier is equal to the gain of gm_2 at f_{chop} which is usually lower than the gain at DC. It is therefore common to employ several gain stages [22].

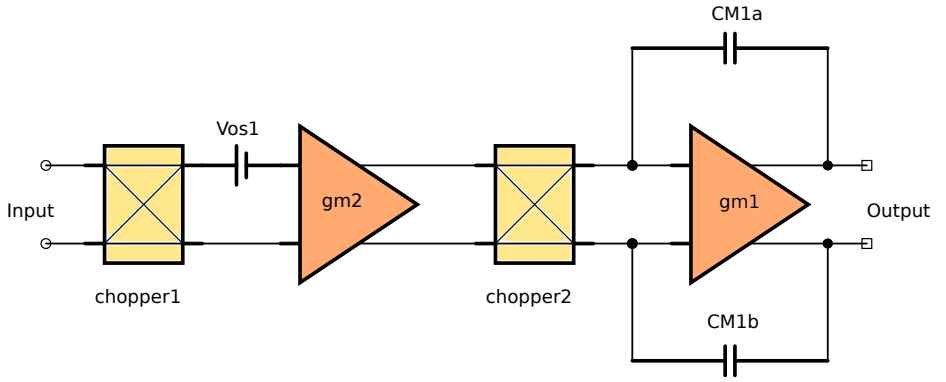

Figure 2.6: Two stage chopper amplifier with low-pass filter.

In this case, the miller capacitors $C_{M1a,b}$ will provide some attenuation of the ripple because of the integrating mechanism of the second stage, acting as a low-pass filter. The filtered ripple will take the form of a triangular wave and the peak-to-peak voltage can be estimated by the following equation, assuming that the bandwidth of the amplifier is lower than the chopping frequency [22].

$$V_{ripple} = \frac{V_{os1} gm_2}{2 f_{chop} C_{m1,m2}} \tag{2.15}$$

Another aspect of this configuration is the band-limiting nature of the second stage. While reducing the bandwidth reduces the ripple, it also limits the opamps bandwidth. A way to

get around this limitation will be presented in chapter 2.3.2.

How efficient the continuous-time approach will be able to suppress the ripple is related to the size of the capacitors used. Unless the chopping frequency is increased, the only way to reduce the ripple is by increasing the capacitance. Obtaining a sufficiently low cutoff-frequency, can in many cases lead to an unacceptably large area for the capacitors.

2.3.2 Chopper offset-stabilization

One technique to maintain high bandwidth while performing chopping is called chopper offset-stabilization. This is done in [1] and a possible implementation is shown in figure 2.7.

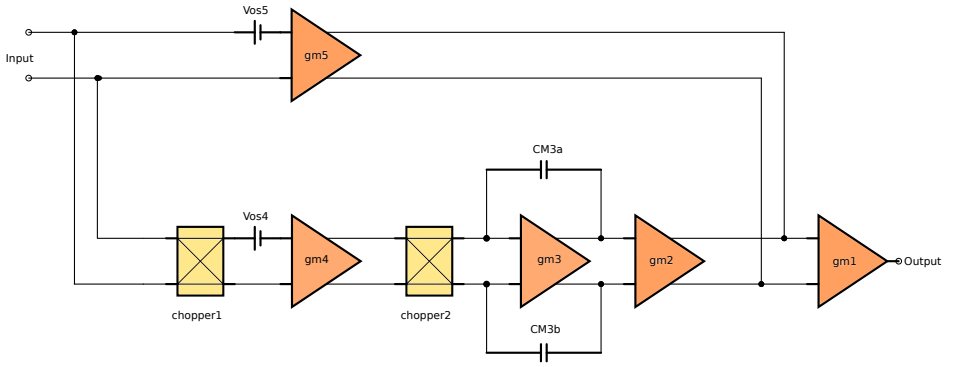

Figure 2.7: Chopper offset-stabilization amplifier [1].

An additional gain stage, gm_5 is placed in parallel with the chopper amplifier, gm_4. gm_3 is configured as an integrator, providing extra gain to compensate for the offset of gm_5 as well as performing ripple reduction due to the offset of gm_4. gm_2 act as an auxiliary amplifier and gm_1 is a single-ended output stage. The chopper amplifier itself will perform in the same manner as described in chapter 2.3.1, up-modulating the offset and the flicker noise. The outputs of gm_5 and gm_3 are connected together via gm_2 and when configured with negative feedback, the offset of gm_5 will be amplified by the chopper amplifier which can then compensate for the offset on the output via gm_2. This way it is possible to achieve both high bandwidth and high DC accuracy. Power consumption will increase because of the two signal paths involved.

How much the lower branch can correct the offset of gm_5 is given by the following equation [1].

$$V_{os} = \frac{V_{os5}A_5}{A_4A_3A_2} \tag{2.16}$$

The lower branch containing the chopper amplifier will produce a ripple voltage due to the chopping of the offset voltage associated with gm_4. The peak-to-peak voltage of this ripple can be expressed by the following equation [1].

$$V_{ripple} = \frac{V_{os4} gm_4 gm_2}{2 f_{chopper} C_{M3} gm_5} \tag{2.17}$$

To effectively correct for flicker noise, the bandwidth of the lower branch should exceed the corner frequency of the flicker noise as pointed out in [1]. gm_3 will also contribute with an offset because no chopping is used for this amplifier. This effect is caused by the potential parasitic output capacitance associated with gm_4 that gets charged and discharged by the chopped voltage. The effect is reduced by increased gm_4 and worsened by an increased chopping frequency. An expression for this effect is shown in equation 2.18 [4].

$$V_{os,parasitic} = \frac{2 V_{os3} f_{chopper} C_{par4}}{gm_4} \tag{2.18}$$

In [1], a technique termed residual offset reduction is presented to reduce this effect. This technique does however come with an increase in complexity. Increasing the area used to implement gm_3 is also an option to reduce V_{os3}.

2.3.3 Switches

The chopper in figure 2.4, consists of four switches that can be realized using MOSFET transistors. A MOSFET switch can have a high off-resistances in the $G\Omega$ range when operated in the cutoff-region, which is important to minimize charge leakage. The on-resistances can be in the $k\Omega$ [19] range, where it is important to keep it low enough for the signal to be able to settle in less than half of the clock period. The on-resistance can be lowered by increasing the W/L ratio and increasing the overdrive voltage. This is true for switches implemented with NMOS or PMOS transistors. There is however a limit in the signal range the switches can process when they are in the on-state. For a NMOS transistor with a threshold voltage of $0.45\,\mathrm{V}$ this translates to a range of about $0\,\mathrm{V}$-$1.3\,\mathrm{V}$ and about $0.5\,\mathrm{V}$-$1.8\,\mathrm{V}$ for a PMOS switch.

If more signal range is required, one possible solution is to use transmission gates [17]. By using a PMOS and NMOS switch in parallel a full signal range can be processed. This type of configuration is shown in figure 2.8.

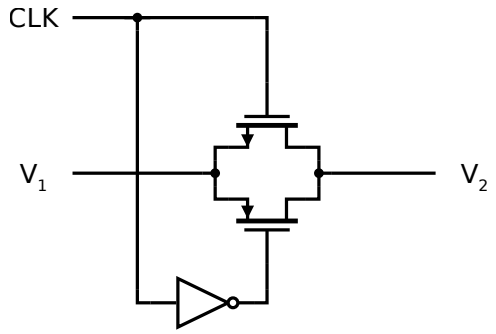

Figure 2.8: Transmission gate.

The clock signal CLK is used to operate the two transistors. An inverter is necessary to operate the PMOS switch. In the context of chopper amplifiers, the non-ideal behaviour of MOSFET switches must be taken into account during the design process. One such non-ideality that has to be considered is charge-injection [19]. This effect is caused by two things: parasitic capacitive feed-through and the redistribution of channel charge [4]. When a transistor switch is turned on and off, charge in the channel will flow out of the source and the drain terminal. The channel charge for a transistor where $V_{ds} = 0\,\mathrm{V}$ can be described by the following equation [19].

$$Q_{ch} = WLC_{ox}(V_{gs} - V_t) \tag{2.19}$$

As can be seen from this equation, the channel charge can be reduced by using smaller switches. When employing a fully-differential structure, such as the one shown in figure 2.7, the charge injection errors will ideally be cancelled in the differential structure. Care must be taken during layout in order to balance the two clock line capacitances to avoid differences in the delay between the moment the signal is applied at the gate of the switches and the moment the actual switching occurs [4]. Because of mismatch and the fact that perfect symmetry never can be obtained in a manufactured circuit, there will be a mismatch in the charge injection and this can cause a differential signal. Detailed layout guidelines are provided in [4].

The consequence is that transistor switches can cause both extra residual offset and residual ripple. Charge-injection related errors will increase for an increased chopping frequency as pointed out in [4], due to the parasitic capacitors and asymmetry. The conclusion is that using minimum sized transistor switches, using a fully differential topology and taking care of the symmetry in the layout can be used to minimize the effects of charge injection.

2.4 Amplifier Design

2.4.1 Folded Cascode

The folded cascode is a popular topology that realizes a single stage amplifier with relatively high gain [15]. The high gain is a product of the increased output resistance due to the use of cascoding. Having high gain in an opamp is useful in many applications as it can be used to enhance the performance of the opamp through the use of negative feedback. One example is increased gain accuracy. When manufacturing an opamp there will be variations in gain from circuit to circuit and temperature dependencies. By operating the opamp in closed loop, a high gain can be traded for a lower gain with high accuracy. Other properties that can be improved are bandwidth and linearity [19]. In terms of noise and offset it is useful to maximize the gain of the first stage in a multi-stage amplifier. The noise and offset of the succeeding stages will be attenuated by the gain of the input stage as discussed in chapter 2.2.3.

Cascoding is a technique that uses a transistor, configured as common-gate to provide current buffering for the output of a current source amplifier [15]. It requires cascoded current mirrors to be able to realize the full gain that is available. This leads to reduced output swing. The folded cascode reduces the problem of stacking several transistors when a limited supply voltage is available, as compared to a telescopic cascode [15]. The structure of a general folded cascode amplifier is shown in figure 2.2.

The one-stage amplifier features a NMOS input pair, consisting of M1 and M2. The usage of NMOS transistors sets a limitation on the input common-mode voltage, effectively meaning the range of input voltages that keeps all the transistors in saturation. This limitation is described in the equation below.

$$V_{dsat11} + V_{gs1} < V_{CM,input} < V_{tn} + V_{DD} - |V_{dsat9}| \tag{2.20}$$

Transistors M3-M4 are the cascode transistors, M9-M10 act as current sources, M11 is the tail current source for biasing M1-M2 and M5-M8 forms a wide-swing current mirror. The wide-swing current mirror requires one more bias point (Vb4) compared to diode-connected M5 and M7 but comes with an increased output voltage range, allowing the output to swing down to $2V_{dsat}$ above the lower rail [15]. The bias voltage Vb4 must at least be equal to $V_t + 2V_{dsat}$ to ensure that all transistors operate in saturation. Vb3 must allow for a voltage drop across M9 and M10, that is at least equal to their overdrive voltages to ensure operation in the saturation region while Vb2 is responsible for setting the bias current and operating M9 and M10 with an appropriate overdrive voltage to ensure good enough output swing. Vb1 is similar and must be set to provide the required bias current and operate with an acceptable overdrive.

The gain of the amplifier can be derived to be the following [15].

$$A_v = gm1[gm_4 r_{o4}(r_{o2}||r_{o10})]||(gm_6 r_{o6} r_{o8}) \tag{2.21}$$

One important characteristic of the folded cascode is that it has only one high-impedance node, located at the output of the amplifier. This leads to a good high-frequency response. There are three poles present; one at the input, one at the connection between the common-source and common-gate transistors and one at the output. Generally, the poles at the input and between the transistors are at very high-frequency [15]. Since the load capacitance, C_L generally is relatively large, the single-stage folded cascode acts as a single-pole amplifier and can be considered unconditionally stable. This means that the amplifier will be compensated and made stable by the load itself, creating a dominant pole. The outcome is an increased phase margin (PM) and decreased unity gain frequency. If the load capacitance is not large enough to achieve this, it can be augmented [15]. The unity gain frequency is given by the following relation.

$$f_{ug} = \frac{gm_{1,2}}{2\pi C_L} \tag{2.22}$$

It is also possible to use a folded cascode gain stage as an input stage, as part of a multi-stage amplifier but this demands a frequency compensation scheme which will be discussed in chapter 2.5.

2.4.2 Folded Cascode With Complementary Input Pairs

As can be seen from equation 2.20, the input common-mode range is limited. With the trend towards lower supply voltages, it gets important to maximize the dynamic range. A rail-to-rail swing at the input provides the highest possible dynamic range. This becomes important in applications where an opamp is used in an unity-gain configuration and needs to be able to follow a rail-to-rail output voltage. It means that the transistors must be kept in saturation for every common-mode input voltage between VSS and VDD.

One way to implement rail-to-rail operation is by using two complementary differential pairs in parallel [2]. The NMOS pair can work up to the upper rail and beyond while the opposite is true for the PMOS pair at lower values. This configuration is shown in figure 2.9.

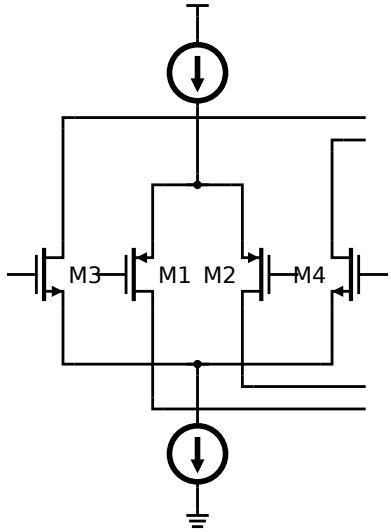

Figure 2.9: Complementary differential pairs [2].

The supply voltage in this configuration must fulfil the following relation.

$$V_{DD} \geq V_{gs,n} + V_{gs,p} + 2V_{dsat} \tag{2.23}$$

The problem with this configuration is that the total transconductance gm_{tot} will vary with the input common-mode voltage. In theory it will equal $gm_n + gm_p$ when the input common-mode is $V_{DD}/2$ which can lead to distortion and stability problems [16]. There exist several ways to combat this effect and provide a gm equalization in the crossover region. One way, suitable for input pairs biased in weak inversion is shown in [3]. It involves the use of a current switch and a current mirror. The complementary differential pairs can be used in place of the single differential pair shown in figure 2.2. In figure 2.10 a folded cascode amplifier featuring complementary input pairs and gm-equalization is shown.

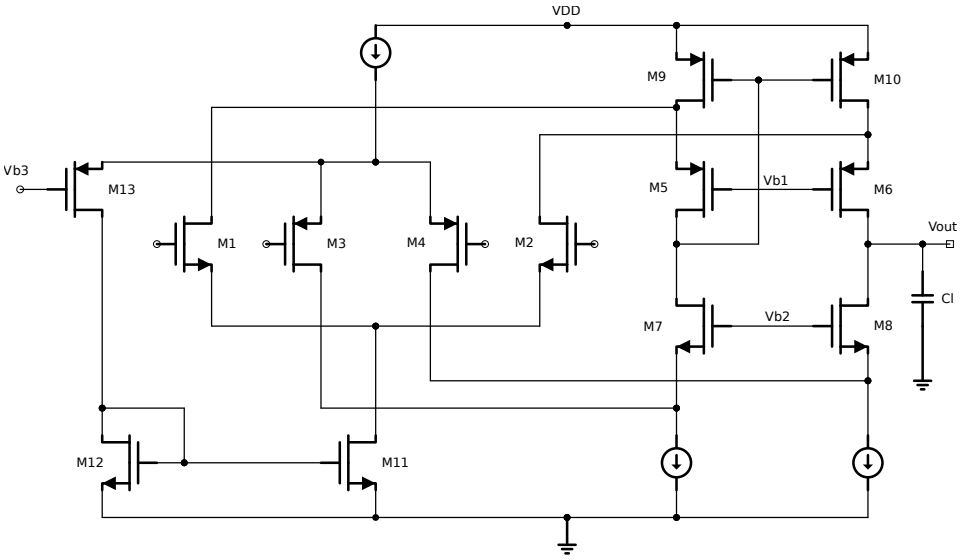

Figure 2.10: Folded cascode with complementary Pairs and gm-equalization [2].

For an increasing common-mode voltage the current switch M13 will start to lead parts of the current coming from the upper current source trough M12 and mirror it with M11, and this way increase the bias current in M1 and M2. This effectively leads to a lower total transconductance in the middle region VDD/2 when both pairs are active. M13 starts to turn on when the common-mode reaches $VDD - Vb_3$ and appropriate biasing must therefore be applied at the gate of M13.

It is also possible to provide a differential output with minor changes to the summation stage, however, this requires common-mode feedback. This is necessary to accurately control the output common-mode voltage.

2.4.3 Output Stage

An output stage is needed in order to deliver the necessary power to the load with minimum distortion of the signal. This must be done in an efficient way, meaning that the ratio between the maximum current that can be delivered to the load and the quiescent current biasing the transistors must be high. By maximizing the output voltage, the maximum power output is also increased, which emphasize the importance of having rail-to-rail output capability.

Amplifiers are classified by their construction and operating characteristics where class-AB with rail-to-rail capability provides a good tradeoff between linearity, efficiency and finds widespread use in low voltage environments [3]. A class-AB amplifier is characterized by having a small quiescent current flowing for improved linearity as compared to

class-B, with improved efficiency as compared to class-A. Two complementary transistors are used to operate in a pull/push fashion, structured similar to a digital inverter stage. To achieve AB-biasing the voltage between the gates of the two transistors are held constant. The basic concept is illustrated in figure 2.11.

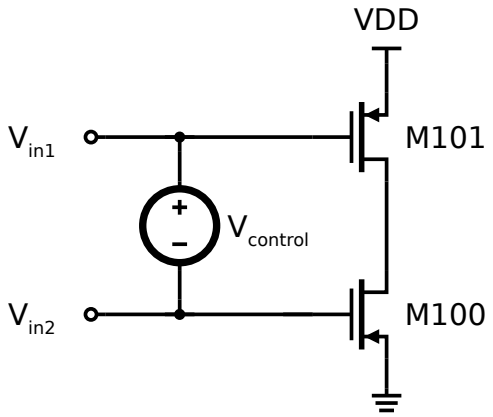

Figure 2.11: class-AB ideal control circuit.

The voltage driving the output transistors on the gate is a limiting factor in terms of the maximum current the output stage can deliver. The idealized circuit in figure 2.11, can be realized by the control circuit shown in figure 2.12. It uses a feedforward scheme suitable for operation in low-voltage environments [3].

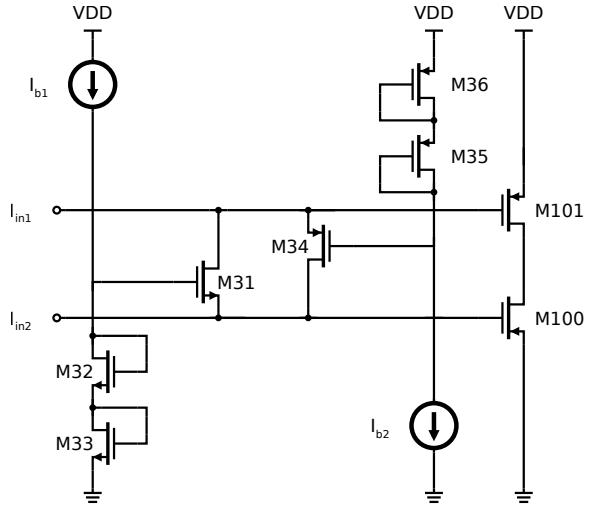

Figure 2.12: class-AB control circuit [3].

The voltage between the gate of M101 and M100 is fixed by the use of transistors M31 and M34. This makes the quiescent current running in the output transistors well defined.

The bias branches consisting of M32-M33 and M35-M36 are responsible for biasing M31 and M34. This forms a pair of translinear loops and if sized correctly such that the drain current of M31 equals M32, their gate-source voltage will be matched. What follows is that the gate-source voltage of M100 will equal M33. This way, it possible to derive an expression for the quiescent current running in the output transistors and it is given as follows [3].

$$Iq = \frac{W_{100}L_{33}}{W_{33}L_{100}}I_{b1} \tag{2.24}$$

As this topology requires a supply voltage in excess of two stacked diode-voltages and one vd_{sat} for the two bias branches, it imposes a limitation when used in low-voltage environments.

The output stage should ideally be largely immune to supply voltage and process variations. There is some degree of supply voltage dependency present in the circuit discussed in figure 2.12. Supply variations will lead to a voltage variation over the transistors in the control circuitry which again lead to a variation in quiescent current. This can be accounted for by biasing the control circuitry with a floating current source. Any supply variations will then be compensated for the by the floating current source as it has the same structure as the control circuit. In [2], it is shown how this circuit can be embedded into the summation circuit of a folded cascode amplifier, where the control circuit is biased directly by the cascodes. This leads to a very compact two-stage amplifier avoiding the drawbacks associated with adding an intermediate stage [3]. This variant is shown in figure 2.13, embedded into the circuit discussed in chapter 2.4.2.

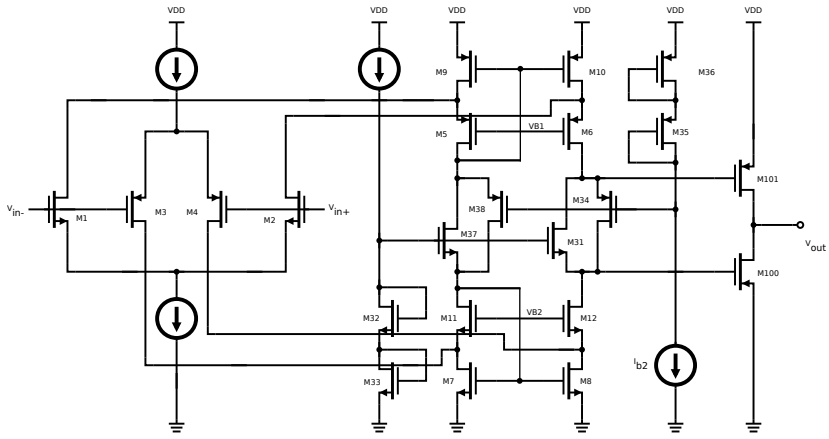

Figure 2.13: Two stage amplifier with class-AB output stage [2]

Transistors M38 and M37 form the floating current source that corrects for any variations in supply voltage and keeps the current in M101 and M100 as constant as possible. The

transconductance of the output transistors will influence the stability of the opamp, as will be discussed in the next chapter.

2.5 Frequency Compensation

Generally, amplifiers used with negative-feedback must avoid having any gain at frequencies where the input signal experiences more than a 180-degree phase shift as this can lead to self-oscillation [23]. This must be accounted for in the design process by applying frequency compensation that gives adequate phase margin to avoid peaking in the frequency domain or shooting in the time domain.

A thorough discussion of frequency compensation for different numbers of gain stages in series and parallel is done in [23]. Multipath Hybrid Nested Miller Compensation (MHNMC) is of particular interest in applications involving chopper offset-stabilization amplifiers, as it involves two parallel paths. To fully understand the mechanisms involved in MHNMC some time will be spent to study miller compensation used in the context of a two-stage amplifier (MC).

2.5.1 Miller Compensation

If a two-stage amplifier is generalized into two cascaded gain stages with their corresponding resistances and capacitances it can be described as in figure 2.14 [19]. Capacitor C_{M1} is the miller capacitor.

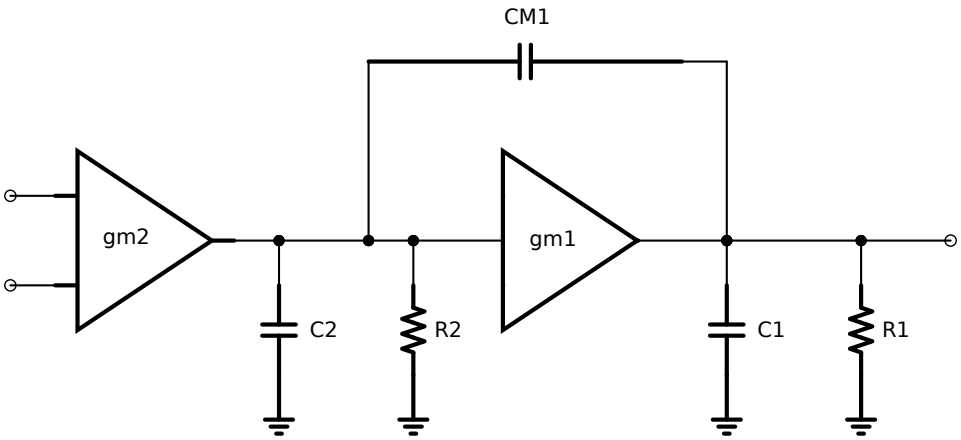

Figure 2.14: Miller compensation.

As can be seen from the figure there are two poles present. Separation of the pole frequencies f_1 and f_2 is necessary to avoid instability. This requirement can be generalized

into the following expression to guarantee stability at a phase margin of 60 degrees, which gives a good tradeoff between power consumption and overshoot [23].

$$\frac{f_1}{f_2} \leq 2A_{V0} \tag{2.25}$$

If assuming that the pole of gm_2 is caused by parasitics and the pole of gm_1 is caused by the load it is unlikely that the condition stated in equation 2.25 is fulfilled without any compensation. By connecting the capacitor C_{M1} between the inverting input and the output of gm_1 a large capacitor on the output of gm_2 can be realized by utilizing the Miller-effect [17]. A larger capacitor will result in a lowering of f_2. Simultaneously, an increase of f_1 occurs because of the feedback action. The location for the two poles is now given by the following equations [15].

$$f_1 = \frac{gm_1}{2\pi C1} \tag{2.26}$$

$$f_2 = \frac{1}{2\pi R_1 R_2 gm_1 C_M} \tag{2.27}$$

As can be seen from the equations, the poles can be split apart by increasing gm_1. The unity-gain frequency can now be derived by multiplying the gain of the amplifier with the lowered pole at f_2.

$$f_{ug} = A_{V0} f_2 = \frac{gm_2}{2\pi C_M} \tag{2.28}$$

A by-product of the Miller compensation is a zero occurring in the right half-plane at the following frequency.

$$f_z = \frac{gm_1}{2\pi C_M} \tag{2.29}$$

This zero can be troublesome in many applications as it causes the phase margin to drop considerably. It can be compensated for by the methods described in [19].

2.5.2 Multipath Hybrid Nested Miller Compensation

In figure 2.7, a chopper offset-stabilization amplifier is shown. This amplifier can be viewed as having two parallel paths. The upper path contains one stage of amplification that is connected to the output stage of the lower path. The lower path is a four-stage

amplifier consisting of an input stage, a second gain stage, intermediate stage and the output stage. MHNMC can be implemented in the chopper offset-stabilization amplifier discussed in chapter 2.3.2 as shown in figure 2.15 [1].

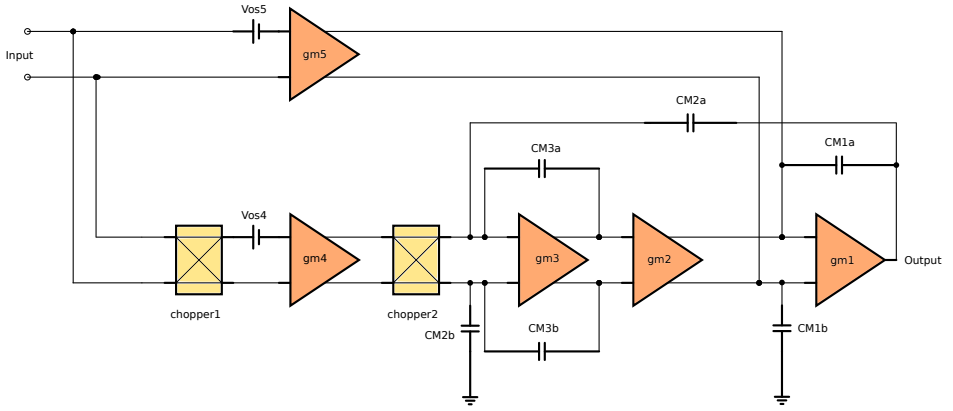

Figure 2.15: chopper offset-stabilization amplifier utilizing MHNMC.

This can be done in order to make the amplifier stable, which is important when used as a general purpose amplifier. By obtaining separation of the two paths, a straight frequency characteristic can be achieved. This works when the mid-range gain of the input stages are equal. The lower path has high gain at low frequencies while the upper path takes over for high frequencies with a seamless transition in the middle region.

For a phase-margin of $60°$ or higher, the following relationships must be obeyed.

$$f_{p5} = f_{p4} \leq \frac{1}{2} f_{p1} \tag{2.30}$$

The miller capacitors C_{M1} and C_{M2}, can be found by the following relations.

$$C_{M1} = \frac{gm5}{2\pi f_{p5}} \tag{2.31}$$

$$C_{M2} = \frac{gm4}{2\pi f_{p4}} \tag{2.32}$$

Since their pole frequencies are equal, separation of the two paths is achieved and they will form a straight roll-off in the frequency domain. The capacitors C_{M2a} and C_{M2b} adds a low-frequency zero that cancels one of the low-frequency poles, as done in [1]. By utilizing the miller effect the poles present will experience a pole-splitting effect and with a load capacitor present on the output C_L, the output pole frequency can be found as described in equation 2.26.

As pointed out in [23], the following relation must also be fulfilled to avoid having the lower path dominating the upper path at higher frequencies.

$$\frac{C_{M2}}{C_{M3}} \frac{gm_2}{2\pi C_{M1}} \leq \frac{1}{3} \frac{gm_5}{2\pi C_{M1}} \tag{2.33}$$

The bandwidth over supply power ratio is comparable to the two-stage Miller compensation scheme [23], apart from the currents needed for the two extra stages.

Chapter 3

Design

The technology used is a 22nm technology. For this project, the IO-transistors available in the 22nm technology are used all over to be able to operate at a supply voltage of 1.8V. A transistor characterization is performed to map the performance of the available technology. This is done early in the design process to establish a scope of what is expected in terms of gain and matching. Next, a high-level model is built to provide a basis for the circuit design and to extract key design parameters. The gain cells are modelled ideally and are used as building blocks for simulating the dynamic behaviour of the opamp. The design equations presented in [1] is used to design the different gain stages. Based on the results obtained from the transistor characterization and the high-level model, the amplifier is designed on transistor level in order to fulfil the specification listed in table 1.1. All schematics implemented in virtuoso are shown in appendix A.

3.1 Transistor Characterization

A testbench is implemented in virtuoso for NMOS and PMOS devices. The basic structure for a NMOS device is shown in figure 3.1, a similar structure is implemented for a PMOS device.

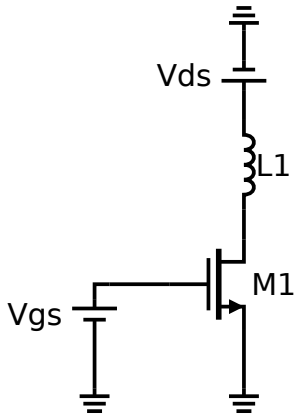

Figure 3.1: Testbench used for transistor characterization of NMOS.

Vds is held constant while Vgs is swept over a relevant range for observing the transistor over different inversion levels. The width is held constant while different lengths are applied. A large inductor in the GH range is inserted between the drain and the power supply. This is done to bias M1 with a DC-current, while at the same time avoid loading the output resistance of M1 at the AC frequencies of interest [21]. Relevant data is extracted from virtuoso and a gm/Id characterization procedure as depicted in [24] is performed. The most notable result is acquired when simulating the intrinsic gain for the NMOS which was simulated to be on the order of 40-70dB per stage, depending on biasing conditions. The PMOS intrinsic gain is somewhat lower, but compared to earlier work [1] this design might require fewer stages to achieve a comparable gain. The gm/Id ratio can be viewed as an efficiency factor, describing how much transconductance is achieved for a given current consumption.

Since this design requires rail-to-rail performance on the input, it is decided to use complementary differential pairs for the input stages. As the PMOS performance is somewhat lower in terms of intrinsic gain, it becomes the limiting factor as it is desirable with a matched transconductance in the input pair. A gm/Id ratio of 25 is set as a design metric based on the acquired characterization, as it is regarded as realistic to achieve for both NMOS and PMOS. Operating the input transistors in weak inversion can be done to obtain a high gm/Id ratio. The definition of weak-inversion operation region according to [25] is when the gate-source voltage is below the threshold voltage V_t by at least $72\,\mathrm{mV}$ for a typical bulk CMOS process at room temperature. This results in high transconductance with a low current consumption, at the expense of reduced speed. The transit frequency f_t is observed at the applicable gm/Id ratio. Based on the specification of the design it is concluded that the reduced speed is not problematic.

Monte Carlo simulations on a schematic netlist are performed in order to extract the proportionality constants. The results obtained from simulation are in agreement with the values stated in the documentation for the technology and shows good performance when compared to other technologies listed in [7], as well as showing similar performance be-

tween NMOS and PMOS. These values will be used in the design procedure to size the transistors as it affects the matching performance.

3.2 High-Level Modelling

Due to the high intrinsic gain in the technology found during the transistor characterization, it is decided to try to design with fewer stages when compared to previous work [1]. A circuit diagram is shown in figure 3.2. It is identical to figure 2.15 from chapter 2.5 but is repeated here for convenience. This diagram shows a chopper offset-stabilized opamp employing MHNMC for frequency compensation. It is the selected topology for this work as it provides high bandwidth due to the parallel paths, high gain in the chopper branch and ripple-reduction by the use of gm_3.

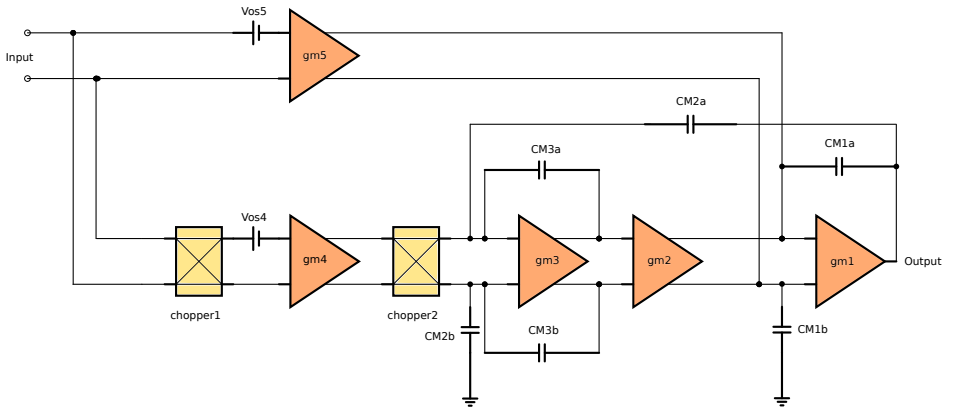

Figure 3.2: Chopper offset-stabilization amplifier [1].

This topology is implemented in the virtuoso design environment with ideal gain cells for quick design evaluation. gm_5, gm_4 and gm_3 is implemented as an ideal differential OTA as shown in figure 3.3, consisting of voltage controlled current sources in parallel with resistors. gm_2 is implemented as in 3.4, acting as an auxiliary amplifier to sum the currents between the upper and lower branch. gm_1 is modelled as a single-ended output stage shown in 3.5, with a voltage-controlled voltage source on the output to perform differential to single-ended conversion and provide a low output resistance.

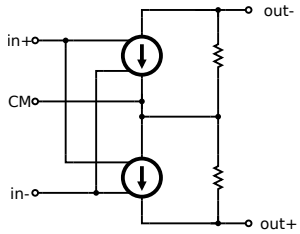

Figure 3.3: Differential OTA.

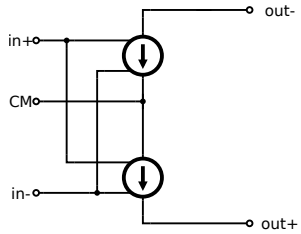

Figure 3.4: Auxillary amplifier.

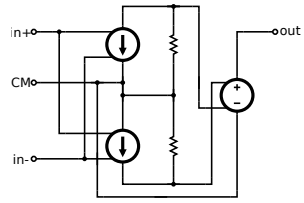

Figure 3.5: Single-ended OPA.

There are two main design equations that have to be considered; equation 3.1 describing the residual offset of gm_5 and equation 3.2, that describes the magnitude of the ripple due to the offset of gm_4. They are identical to equation 2.16 and 2.17 but are repeated here for convenience.

$$V_{os} = \frac{V_{os5} A_5}{A_4 A_3 A_2} \tag{3.1}$$

$$V_{ripple} = \frac{V_{os4} gm_4 gm_2}{2 f_{chopper} C_{M3} gm_5} \tag{3.2}$$

As a starting point, the specification is used to determine the required transconductances for the different stages to be able to use the equations. It is decided to not implement any residual offset reduction circuitry, as done in [1], as it is regarded as realistic to fulfil the specification without it. To get started it is important to establish how much offset is expected of gm_5 and gm_4. Since the specification states rail-to-rail ICMR, it is decided to use complementary pairs as discussed in chapter 2.4.2 to implement gm_5 and gm_4 with the corresponding gm-equalization circuitry to maintain a stable phase margin. Because of the complementary pairs, the offset voltage will show a common-mode dependency. The worst-case offset must be calculated for common-mode=Vdd/2 when both input pairs are active. The concepts discussed in chapter 2.2.2 can be used to come up with an estimate for the expected offset. In the case of gm_5, assuming that only threshold-mismatch from the input pairs contributes to the offset and all other contributions are neglected, the following estimate is obtained.

$$\sigma_(\Delta V_{os5}) = \sqrt{\sigma_(\Delta V_{t1})^2 + \sigma_(\Delta V_{t3})^2} \tag{3.3}$$

Where V_{t1} and V_{t2} represents the threshold voltage for the two different pairs and $\sigma_(\Delta V_{t1})^2$ is expressed by the following equation.

$$\sigma_(\Delta V_t)^2 = \frac{A_{vt}^2}{WL} \tag{3.4}$$

This is an estimate with limited accuracy as the current sources in the summation stage also can contribute with considerable offset errors, but it is accepted as a first estimate since the design process will be an iterative process.

A higher value of V_{os5} requires more gain in the chopper branch to force the residual offset inside the specification. Based on the transistor characterization, it looks like a lot of gain easily can be realized. An area of about $22\,\mu\mathrm{m}^2$ dedicated for both pairs, will result in $\sigma_(\Delta V_{os5}) \approx 500\,\mu\mathrm{V}$. This is considered as reasonable area usage. To provide a high yield, the design should be inside the specification for a value of 4σ. This results in an offset voltage of $2\,\mathrm{mV}$ having to be reduced below $1\,\mathrm{mV}$ when chopping is applied. V_{os5} is likely to rise when also the current source transistors are taken into account in the full realization. It can be reduced by reducing the W/L ratio for the current sources, but for now, some margin is applied and the worst-case V_{os5} is estimated to be $5\,\mathrm{mV}$.

A similar estimate is carried out for the gm_4 stage. The consequence of an increased offset, in this case, is an increased ripple. As the specification states a maximum output noise of $500\,\mu\mathrm{V}$, this offset must also be limited. It is decided to size gm_4 similar to gm_5, resulting in a worst case offset $V_{os4} = 5\,\mathrm{mV}$.

The specified residual offset of $< 1\,\mathrm{mV}$ is used to find an expression for the gain relationship between the upper and lower branch with a worst case $V_{os5} = 5\,\mathrm{mV}$. This leads to the conclusion that the lower branch must have at least 5 times more gain, which is easily realized since it features several stages.

In the case of equation 3.2, gm_4 is together with gm_5 constrained by the noise requirement of $500\,\mu\mathrm{V}$ as a lower bound because the thermal noise depends on the transconductance. Higher transconductances will also lead to higher power consumption, as well as larger capacitors for compensation leading to an increase in area. It is decided to size the transconductance of both input stages to be equal, as this is expected to result in acceptable performance according to equation 3.1 and 3.2. When gm_4 and gm_5 are sized identically, it follows that they have the same thermal noise performance and there are three variables that can be adjusted to lower the ripple: Increasing the chopper frequency, increasing C_{M3} and decreasing gm_2. gm_2 is constrained by equation 2.33, as an upper bound.

It is decided to explore the use of a relatively high chopping frequency of $2\,\mathrm{MHz}$ when compared to previous work [1]. This is possible because of the low power loss at high switching speeds for this technology. The specified bandwidth of 1 MHz also means that the capacitors used for compensation will provide additional damping of the ripple due to the specified $1\,\mathrm{MHz}$ bandwidth.

In order to be able to solve 3.2, some noise budgeting is done. There are three noise contributors that have to be considered: Thermal noise, flicker noise and the ripple voltage produced by the amplifier itself due to the chopping technique. As an initial approximation, it is assumed that flicker noise will be completely removed by the chopping action. Using the concept of noise-bandwidth as described in chapter 2.2.3 and equation 2.14, an expression relating the compensation capacitors and the output noise due to thermal de-

vice noise can be used to provide an estimate. The thermal output noise should be kept below the specified maximum output noise voltage by a healthy margin, considering that the ripple potentially can be the dominating noise contributor. The area usage of the Miller capacitors should also be minimized. A capacitance value of $2\,\mathrm{pF}$ is considered as an upper limit for the compensation capacitors. According to equation 2.14, this will result in an output noise of approximately $53\,\mu\mathrm{V}$ at a temperature of $27\,^{\circ}\mathrm{C}$. As it is an overly optimistic estimate because the noise in the current sources is neglected, some margin should be applied. $80\,\mu\mathrm{V}$ is regarded as a reasonable estimate. A capacitor value of $2\,\mathrm{pF}$ is therefore accepted as it leaves a headroom of about $420\,\mu\mathrm{V}$ for the ripple noise to occur. Now that the size for the compensation capacitors has been established, the required transconductance for the input stages can be calculated according to the specified bandwidth as shown in equation 3.5.

$$gm = 2\pi C_M f_{ug} \tag{3.5}$$

The result calls for a transconductance larger than $13\,\mu\mathrm{S}$. The input stages are designed for transconductances around $15\,\mu\mathrm{S}$ to allow for some margin. The specified DC gain of $> 100\,\mathrm{dB}$ must be fulfilled, as well as equation 3.1. The gain for the individual stages is based on these two criteria's. The total gain for the whole amplifier is expressed in equation 3.6.

$$A_{V0} = ((A_{V4}A_{V3}A_{V2}) + A_{V5})A_{V1} \tag{3.6}$$

Only preliminary gain values are set for now, based on the fact that a large amount of gain can be realized in a multi-stage amplifier. The results obtained by the hand calculations are summarized in table 3.1, and the values are implemented into the high-level model.

	gm_1	gm_2	gm_3	gm_4	gm_5
gm	$10\,\mu\mathrm{S}$	$1\,\mu\mathrm{S}$	$50\,\mu\mathrm{S}$	$15\,\mu\mathrm{S}$	$15\,\mu\mathrm{S}$
A_V	10	100	5000	1500	1500

Table 3.1: Preliminary gain and transconductance values for the different stages.

The amplifier is compensated by the technique discussed in chapter 2.5. Based on the noise requirements, bandwidth requirement and the compensation scheme, the size of the compensation capacitors C_{M1} and C_{M2} are set equal to each other.

$$C_{M1} = C_{M2} = \frac{gm}{2\pi f_{ug}} \tag{3.7}$$

After implementing the frequency compensation, the frequency characteristic for the ideal amplifier is simulated and the resulting bode plot is shown in figure 3.6.

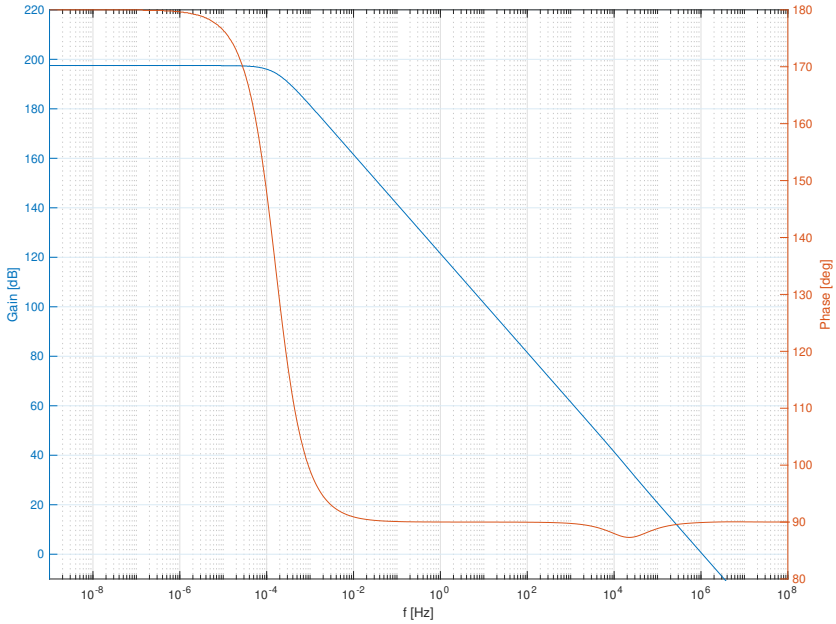

Figure 3.6: Ideal AC characteristic.

A high DC-gain is observed and is in agreement with the theoretical value calculated using equation 3.6 which equals $198\,\mathrm{dB}$. A total phase shift of $90°$ is also expected as the output buffer is modelled ideally and there is no load capacitor on the output node implemented. There is a small artefact on the phase response occurring due to the use of MHNMC compensation where the low-frequency zero cancels out the low-frequency pole.

The ripple is simulated for different chopping frequencies according to equation 3.2 at the expected worst case of $V_{os4} = 5mV$. The resulting peak-to-peak to values are plotted logarithmically versus a chopping frequency from $2\,\mathrm{kHz}$ to $2.2\,\mathrm{MHz}$ in figure 3.7. The modelled ripple is also shown.

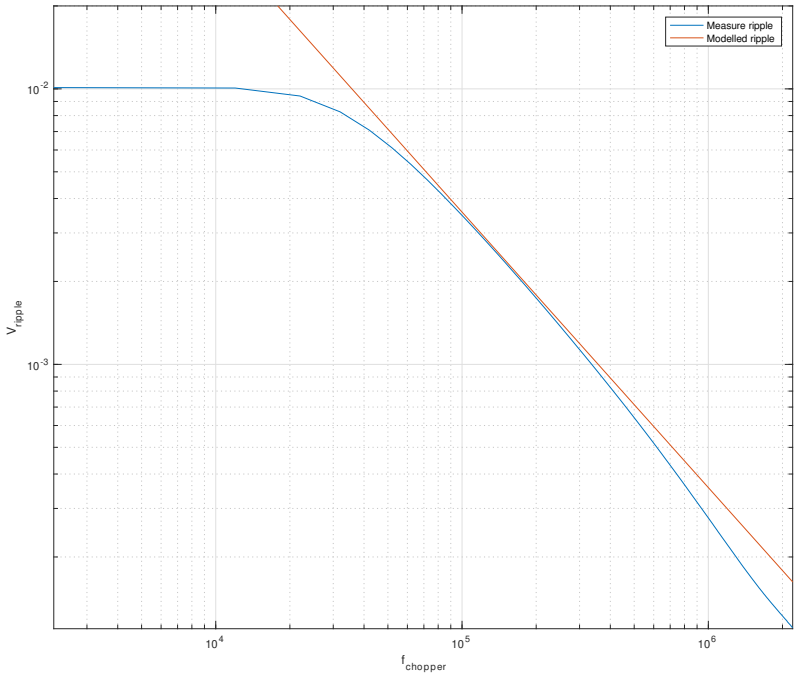

Figure 3.7: Ripple plotted against chopping frequency.

The simulated ripple starts to flatten out at lower frequencies, as it occurs as a pure square wave due to no filtering taking places. For medium high frequencies around 100 kHz to 300 kHz, equation 3.2 and the simulated values are very much in agreement. For higher frequencies, the simulated curve starts to deviate from the modelled. This is because the additional filtering function of the compensation capacitors has not been incorporated into the equation.

A simulation is also done to check the behaviour for the residual offset reduction according to equation 3.1. V_{os5} is set to the expected worst case of $5\,\mathrm{mV}$, and the gain of gm_4 is gradually increased by increasing the output resistance r_{out4}, providing more and more attenuation of the offset occurring at the input of gm_5. The gain starts at around 1 and is increased up to 150. The gain for gm_3 is set to 50. The modelled and simulated values are shown in figure 3.8.

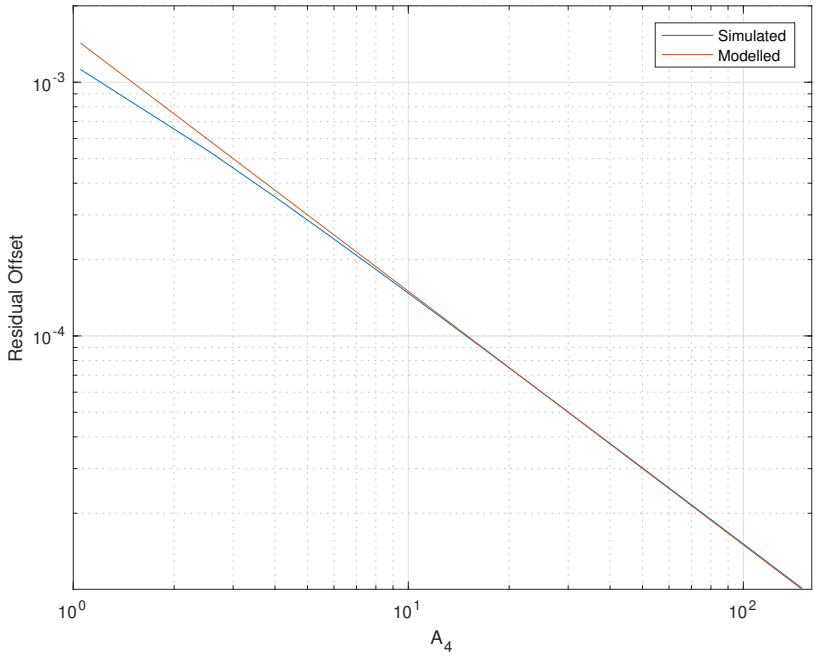

Figure 3.8: Residual offset reduction.

The results show that the high-level model simulates well according to equation 3.8. When the gain for gm_4 is equal to 150, the gain of the lower branch equals 118 dB. When the gain of gm_5 equals 63.5 dB, this results in a residual offset of $10\mu V$. The exact gain values for the different stages will be determined during the transistor design, but this result shows that the specified residual offset of $< 1mV$ can be achieved rather easily when three stages are used.

The results obtained during the high-level modelling act as a reference during the transistor-level design and somewhat similar performance is expected.

3.3 Transistor-design

3.3.1 Design of gm_5

The design of gm_5 is built around the topology described in chapter 2.4.2. A schematic is shown in figure 3.9.

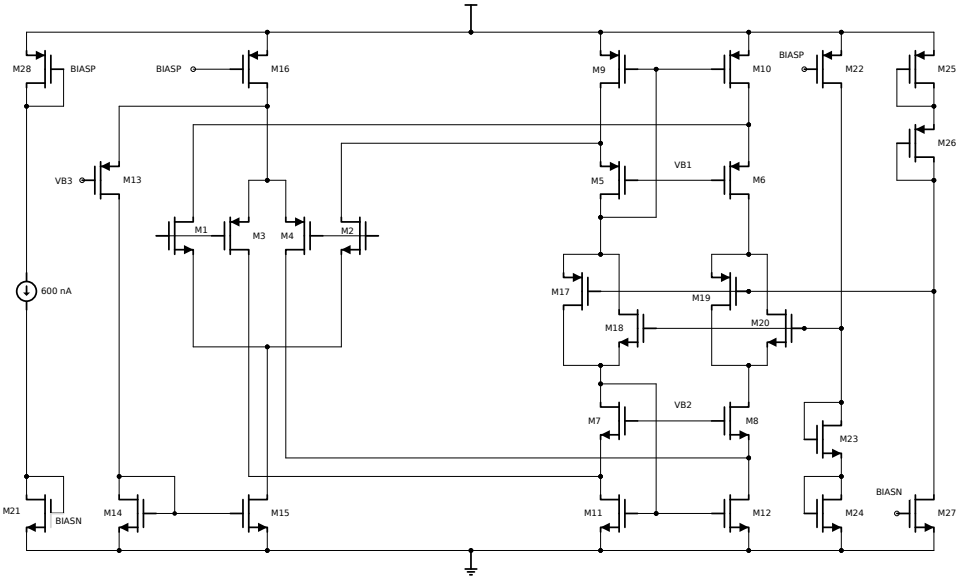

Figure 3.9: gm_5 schematic.

The transistors M1-M4 realizes the complementary input pairs. The gm-equalization circuitry consists of the current switch M13 and the current mirror M14-M15, as described in chapter 2.4.2. The floating current source is inserted into the summation stage, and consists of transistors M17-M18, which together with the output stage control circuitry M19-M20 is biased by the two branches consisting of transistors M22-M27.

Based on the results obtained during the transistor characterization and high-level modelling, the input pairs should operate at gm/Id ratio of 25 where gm=$15\ \mu\mathrm{S}$. This transconductance corresponds to a drain current of $600\ \mathrm{nA}$. The mismatch calculations were done during the high-level modelling points towards an area of $22\ \mu\mathrm{m}$ for each input pair. This constraint makes it possible to find the required W/L ratio for the input pairs. The transconductance should be matched between the NMOS and PMOS pair to avoid large deviations of phase margin as the common-mode input changes.

With this in mind, a diode-connected transistor is used in the simulator to extract the W/L ratio that corresponds to gm=$15\ \mu\mathrm{S}$ at the given area and current. The lengths have to be increased somewhat relative to minimum length to be able to match the transconductances and to be able to operate at the given gm/Id. The resulting W/L ratios and areas are shown in table 3.2. The corner frequency for the flicker noise is also extracted by visually inspecting the intersection between the thermal and flicker curves, as it is important to keep the corner frequency sufficiently low in order to effectively suppress it by the chopping action.

	W	L	W/L	Area	gm	f_{co}
NMOS	7.4u	3u	2.5	22.2 um^2	15.1 uS	16 kHz
PMOS	16u	1.4u	11.5	22.4 um^2	15.1 uS	3 kHz

Table 3.2: Input pair dimensions - gm_5

The bias voltage for the PMOS current switch M13 is set to $700\,\mathrm{mV}$. The W/L ratio for the switch is set to 6. This is rather low compared to the input transistors (11.5), as pointed out in [3] as a way to maximize the common-mode-rejection-ratio. The total transconductance is obtained by adding them together and it is plotted against a swept common-mode voltage from 0 to 1.8V. The result is shown in figure 3.10, with and without gm-equalization enabled.

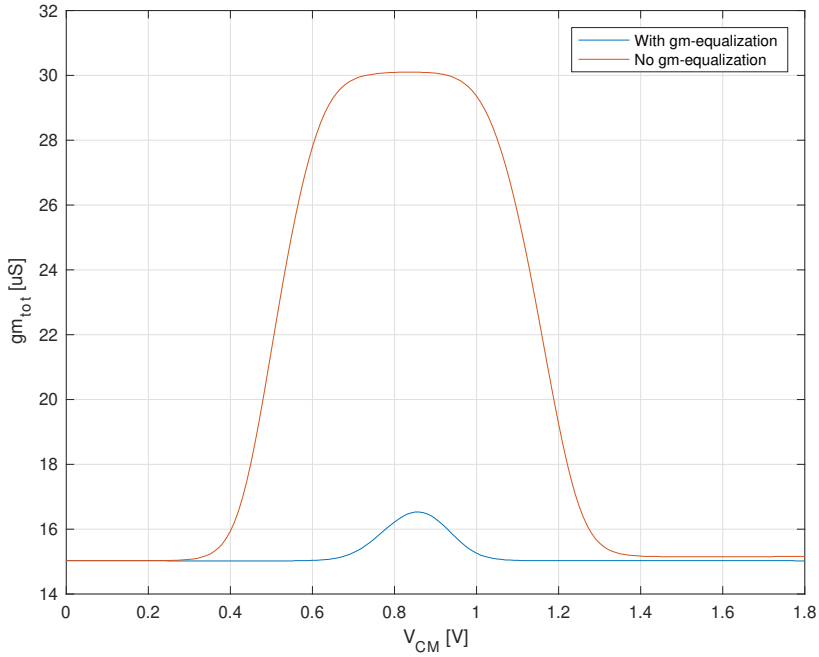

Figure 3.10: gm-equalization.

The bump in the overlap region can never be totally removed with this method and the result is therefore treated as acceptable for this work.

Next, the summation stage is designed. The sizing of the transistors used in the summation stage is determined by the concepts discussed in chapter 2.2.1 and 2.2.3, mismatch and noise. Based on this, the transistors used as current sources are biased in strong inversion resulting in a relatively low W/L ratio. The limitations for how large the overdrive voltage

can get is set by the supply voltage and the required output swing. The bias circuit for the output stage control-circuit requires two stacked gate-source voltages and one v_{dsat} voltage to operate in saturation.

With this in mind, the strategy is to use a unit ratio that gives adequate noise, mismatch performance and scale the width with a multiplication factor according to the bias current. The bias current is realized by a $600\,\mathrm{nA}$ ideal current source, where two diode-connected transistors, M28 and M21 are used to generate the bias points BIASN and BIASP. They are set to operate with a V_{dsat} around $150\,\mathrm{mV}$. This results in the following dimensions for the bias transistors shown in table 3.3.

	W	L	W/L	Area	V_{dsat}
NMOS	$1\,\mu\mathrm{m}$	$6\,\mu\mathrm{m}$	$1/6$	$6\,\mu\mathrm{m}^2$	$153\,\mathrm{mV}$
PMOS	$3\,\mu\mathrm{m}$	$6\,\mu\mathrm{m}$	$1/2$	$18\,\mu\mathrm{m}^2$	$172\,\mathrm{mV}$

Table 3.3: Bias transistor dimensions - gm_5

All other currents are derived from this network. Both of the tail current sources, M15-M16 are therefore scaled with a multiplication factor of 2 to provide each input transistor with a current of $600\,\mathrm{nA}$. The transistors used in the floating current source carry each half of the current running in one summation branch. The floating current source is biased by the biasing branch constisting of M22-M24, and these transistors are therefore scaled with a multiplication factor 1/2 to have a current of $300\,\mathrm{nA}$ in each branch of the floating current source. The two current sources at the bottom, M11-M12, is part of a wide-swing cascoded current mirror. The bias voltage VB2 is set to ensure that they are kept in saturation while maintaining a decent voltage swing. VB2 is set to $750\,\mathrm{mV}$ to provide some margin, and the m-factor is set to 3 to have a current of $1.2\,\mu\mathrm{A}$ flowing when the PMOS pair, M3-M4, is active at the lower common-mode input range. A similar configuration is done for the upper current sources, M9-M10, where the bias voltage VB1 is set to $800\,\mathrm{mV}$, to ensure operation in the saturation region. The cascodes, M5-M8, are set to an m-factor of 2 so they operate in strong-inversion, but they are not as critical in terms of mismatch and noise as the current sources and they can operate in more moderate-inversion levels.

As the gain stages gm_2 and gm_1 will eventually be embedded into gm_5, their design will be covered in the next two chapters.

3.3.2 Design of gm_2

The design of gm_2 is realized by a NMOS differential-pair injecting currents into the upper part of the summation stage. This is done to be able to correct for the offset of gm_5 as discussed in chapter 2.3.2. A schematic is shown in figure 3.11.

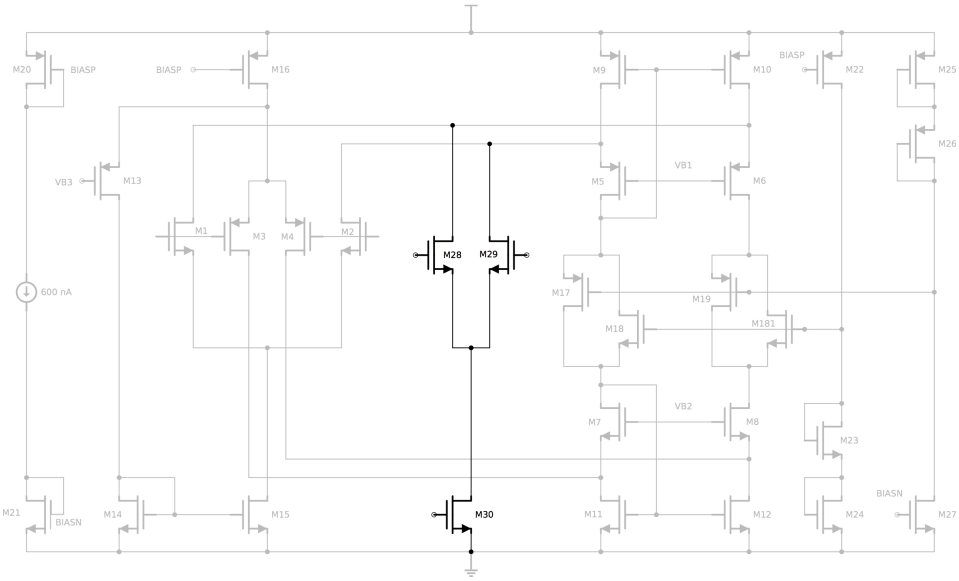

Figure 3.11: gm_2 schematic.

The transistors M28-M29 are biased by the tail current source M30, providing a current of $200\,\mathrm{nA}$ and is sized with a m-factor of 1/3, to derive the current from the bias network. The sizing of the input transistors is not critical because when referred to the input its mismatch and noise contributions will be rather small. The transconductance of this stage will influence the ripple according to equation 3.2. The W/L ratio is set to 1/3 with near minimum device width of $200\,\mathrm{nm}$ and the length is set to $600\,\mathrm{nm}$. This results in weak-inversion operation with a gm/Id of 24.

3.3.3 Design of gm_1

The output stage must be able to provide a current of 10 mA to the load as stated in the specification. The control-circuit have already been designed as part of the summation stage in gm_5. A PMOS and NMOS transistor is designed in an inverter-like fashion to act as output transistors as discussed in chapter 2.4.3. A schematic is shown in figure 3.12.

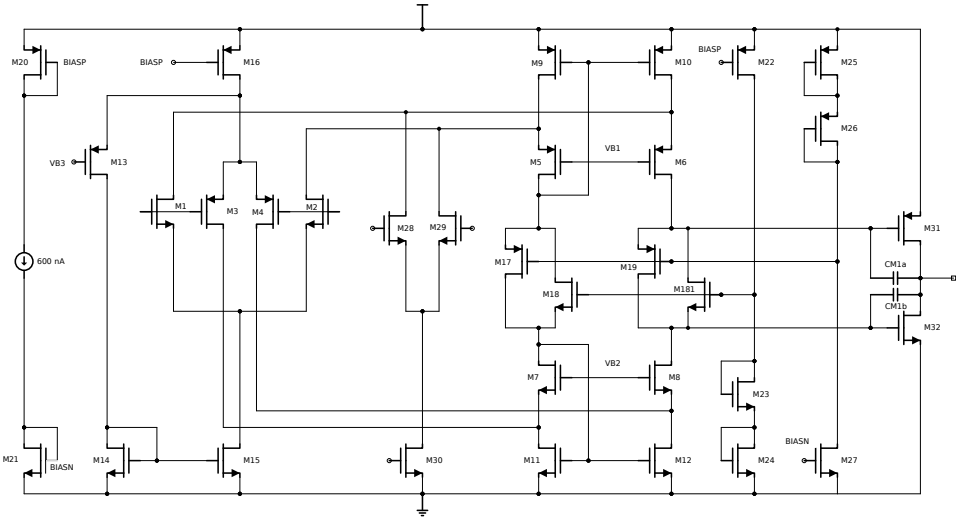

Figure 3.12: gm_5, gm_2 and gm_1 schematic.

The dimensions for the output transistors M31-M32, must be figured out. This must be evaluated both in terms of current capability and frequency response, as its transconductance affects the placement of the output pole, as discussed in chapter 2.5. It is also important to maximize the ratio between quiescent current and max current.

With the designed control circuit, the gate voltages for the PMOS and NMOS resides at about $1\,\mathrm{V}$ and $600\,\mathrm{mV}$ respectively with no load. Minimum length is set for the output transistors and width of $40\,\mu\mathrm{m}$ is set for the NMOS and $120\,\mu\mathrm{m}$ is set for the PMOS. This results in a quiescent current of around $420\,\mu\mathrm{A}$, which is treated as acceptable for this work. It is expected that the output stage will dominate in terms of power consumption. The transconductance equals $5.3\,\mathrm{mS}$, meaning that the transistors operate in strong-inversion. The theoretical gain is calculated according to equation 3.8.

$$A_V = \frac{gm}{gds_1 + gds_2} \tag{3.8}$$

It is found to equal around $41.3\,\mathrm{dB}$. It is important that the gate-source voltages are held constant for a varying common-mode input to maintain a predictable quiescent current. The resulting gate drive voltages and quiescent current are plotted in figure 3.13, for a varying common-mode input voltage spanning from rail-to-rail.

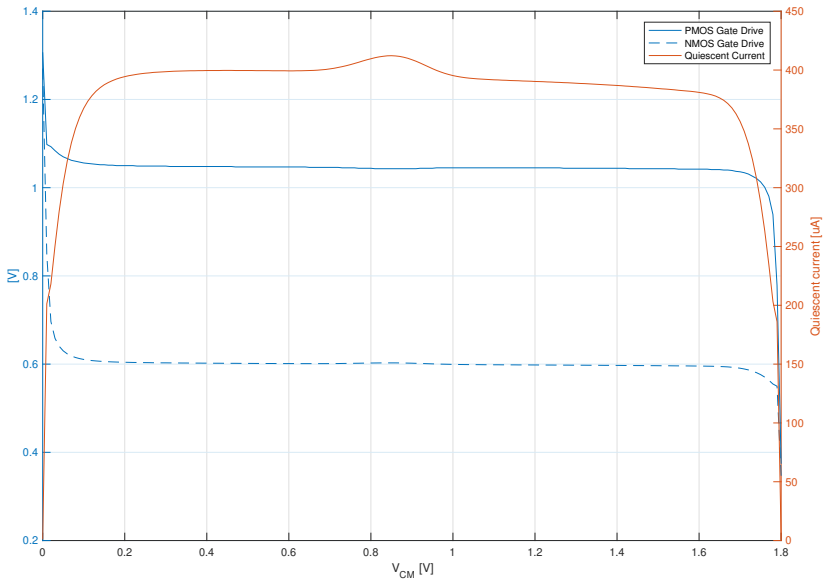

Figure 3.13: Control voltages and quiescent current in the output stage.

A relative constant drive voltage is maintained for both transistors up to around $50mV$ distance to each rail. One of the output transistors will go into the linear region for common-mode voltages close to the rails, resulting in a steep drop for the quiescent current, approaching zero. The theoretical gain for gm_5 calculated according to equation 2.21. The necessary values are extracted from a DC-analysis and it is found to equal around $103\,\mathrm{dB}$. The theoretical gain for the two stages in cascade is therefore found to be $144\,\mathrm{dB}$. The two capacitors C_{M1a} and C_{M1b}, are used in parallel to provide miller compensation as done in [3]. Together they equal $2\,\mathrm{pF}$ to make the unity-gain equal to $1\,\mathrm{MHz}$, when the input transconductance is $15\,\mu\mathrm{S}$.

An output capacitor of $50\,\mathrm{pF}$ is inserted at the output node, according to the specification in table 1.1. No load is applied. The loop gain is simulated to study the DC-gain and frequency response for the two cascaded stages. The resulting bode-plot is shown in figure 3.14.

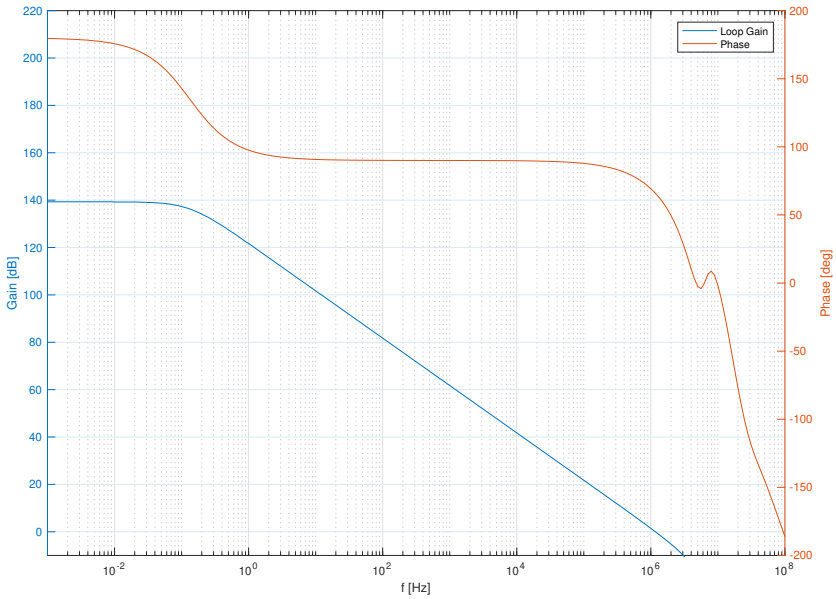

Figure 3.14: Bode plot for gm_5 and gm_1 in cascade.

The resulting simulated DC-gain of $139\,\mathrm{dB}$ is treated as valid, as some deviation from the theoretical value of $144\,\mathrm{dB}$ is expected. The dominant pole resides at a very low-frequency and causes a $20\,\mathrm{dB/Dec}$ roll-of all the way down to the unity-gain frequency at $1\,\mathrm{MHz}$. The phase-margin is reported to be $66°$ which is regarded as sufficient, leading to the conclusion that the transconductance for the output transistors is sufficient.

Next, the rail-to-rail performance is evaluated. An ideal current source is inserted on the output node to source current. The output stage will then deliver current via the PMOS transistor. A parametric sweep is performed where a current source is increased from $0\,\mathrm{mA}$ to $10\,\mathrm{mA}$ and the input common-mode voltage is swept from 0 to $1.8\,\mathrm{V}$. The result is shown for the two extreme cases of zero load and maximum load in figure 3.15.

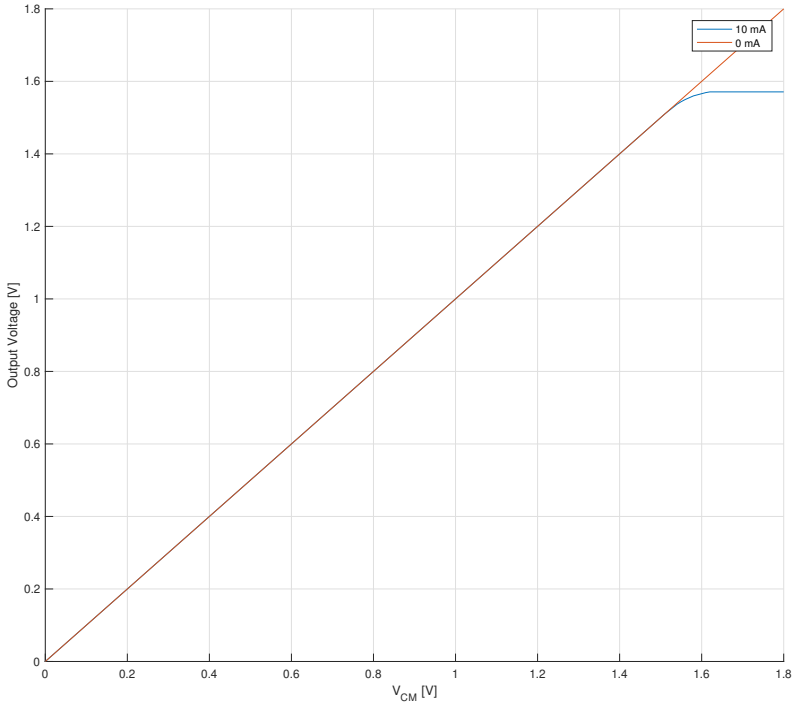

Figure 3.15: Rail-To-Rail performance at maximum load.

As can be seen in the figure, the rail-to-rail performance degrades for an increased load. For zero load, the output can fully reach the upper rail. In the case of a $10\,\mathrm{mA}$ load, the output can only reach $1.55\,\mathrm{V}$. The transistors biased by the floating current source quickly falls out of the saturation region for an increasing output voltage in combination with a heavy load. The NMOS output transistors start entering the subthreshold region and eventually gets cut off. The lower right part of the summation stage enters the linear region. A similar result is obtained when a current sink is applied on the output, resulting in a minimum voltage of $210\,\mathrm{mV}$ with maximum load.

The conclusion is that the output stage is able to operate up to about $250\,\mathrm{mV}$ away from the upper rail and down to $210\,\mathrm{mV}$ away from the lower rail, at maximum load. Operation very close to the rails can be done at lower loads. The performance of the output stage is regarded as good enough, as designing a highly optimized output stage is outside the scope of this work.

A Monte Carlo simulation is performed on the schematic netlist to evaluate the expected offset. The simulation is done using 200 iterations, performing DC-analysis on the am-

plifier configured as a voltage-follower. The offset is defined as how much the output voltage deviates from VDD/2 when VDD/2 is applied on the input. The result is shown in a histogram in figure 3.16.

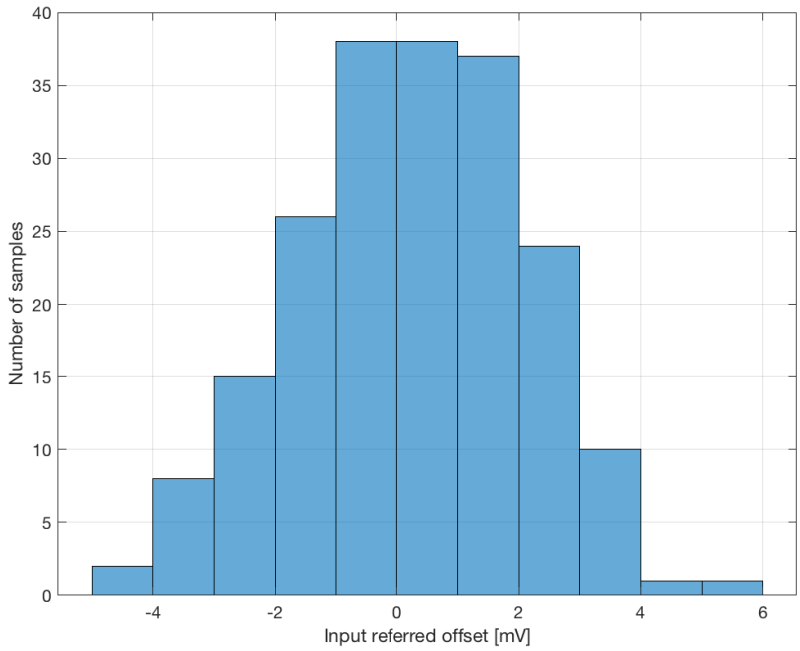

Figure 3.16: Simulated input-referred offset for gm_5 - 200 iterations.

As can be seen from the figure, chopping will be needed to fulfil the specified offset of $< 1\,\mathrm{mV}$ at a sigma level of 4 with the current area usage. The Mismatch Contribution Analysis in the Virtuoso Analog Design Environment, reveals the top mismatch contributors. They are all due to threshold mismatch and M1, M2, M9, M10 and M12 are the top contributors. The methods discussed in chapter 2.2.2 can be used to lower the mismatch in these transistors, but since chopping will be applied, this result is treated as acceptable.

The input-referred noise is simulated to be $64\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$. This result is accepted, as the estimate according to equation 2.11 equals $38\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ when the temperature is equal to $27\,^{\circ}\mathrm{C}$. This estimate only takes thermal noise from the input pairs into account, and the exact noise coefficient γ has not been extracted. Since some noise contributions are expected from the current sources and γ is assumed to be a little higher than $2/3$ for a submicron-process, this result is treated as valid. This will result in a RMS value for the given bandwidth of $84\,\mu\mathrm{V}$. This is treated as acceptable, as it leaves some room for the ripple noise to occur while staying below the specified value of $500\,\mu\mathrm{V}$.

3.3.4 Design of gm_4

The design of gm_4 bears many similarities to gm_5 as they target the same gm/Id. Because of this, the input pairs, M1-M4, are sized identically to gm_5, according to table 3.2. The most notable difference is the required differential output and the absence of an output stage. This requires common-feedback circuitry which is kept at an ideal level in this work. It is implemented by a voltage-controlled voltage source acting as an error amplifier with a gain of 10 and a significantly larger bandwidth compared to the amplifier itself, to avoid stability problems. The resistors R1 and R2 used for sensing the output voltage are sized with a large resistance of $100\,\mathrm{T\Omega}$, to avoid loading the output. A schematic is shown in figure 3.17.

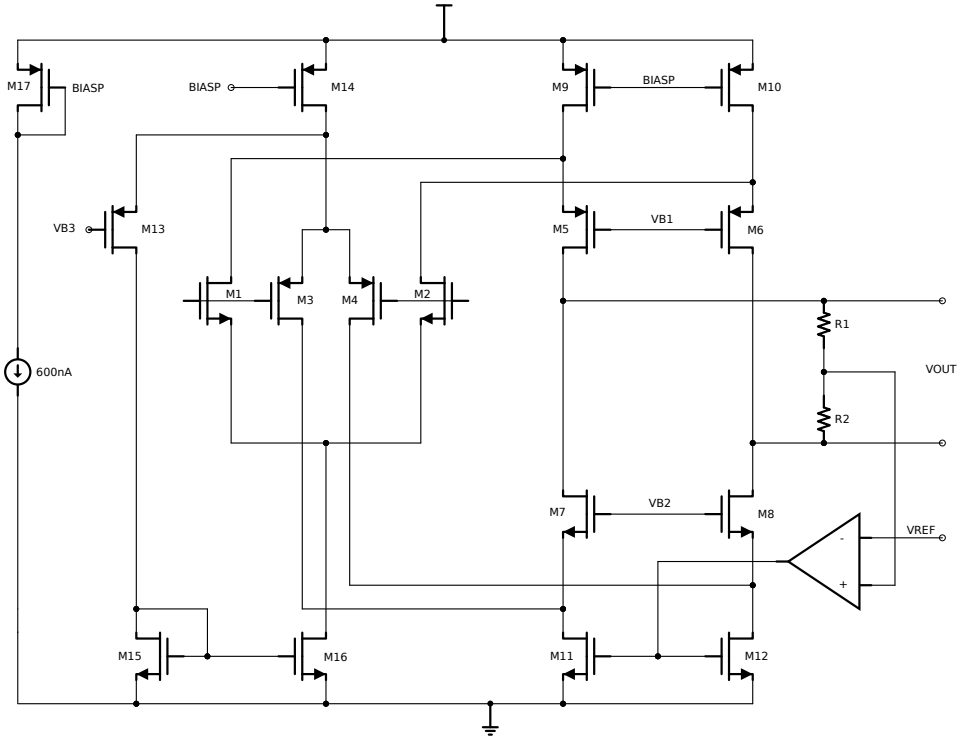

Figure 3.17: Schematic for gm_4.

Due to the absence of the control circuit for the output stage used in gm_5, more headroom is available. This available headroom is used to increase the overdrive for the transistors used as current sources. This is ideal in terms of both thermal noise and offset voltage as discussed in chapter 2.2.1. As the ripple voltage is proportional to the offset of gm_5 as shown in equation 3.2, increasing the overdrive will lead to a reduction of the ripple. This is done for all current sources and results in a relatively low W/L ratio of 2/30 for the NMOS and 3 times 2/30 for the PMOS. The width is set almost at minimal width to obtain a low W/L ratio to avoid having excessive area usage. The resulting dimensions and V_{dsat}

is shown in table 3.4.

	W	L	W/L	Area	V_{dsat}
NMOS	$200\,\mathrm{nm}$	$3\,\mu\mathrm{m}$	$2/30$	$0.6\,\mu\mathrm{m}^2$	$217\,\mathrm{mV}$
PMOS	$600\,\mathrm{nm}$	$3\,\mu\mathrm{m}$	$6/30$	$1.8\,\mu\mathrm{m}^2$	$250\,\mathrm{mV}$

Table 3.4: Bias transistor dimensions - gm_4

The bottom and top current source transistors are multiplied with a m-factor of 2, as well as the cascodes. The theoretical gain is calculated to be around $103\,\mathrm{dB}$. The simulated value is found to be very similar. Input-reffered noise is simulated to be $59\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$.

3.3.5 Design of gm_3

The design of gm_3 is realized by a NMOS differential pair with a current source load and differential output since the available technology enables a large amount of gain to be realized in a single stage. An ideal common-mode feedback circuit, similar to the one used in gm_4 is implemented. A schematic is shown in figure 3.18.

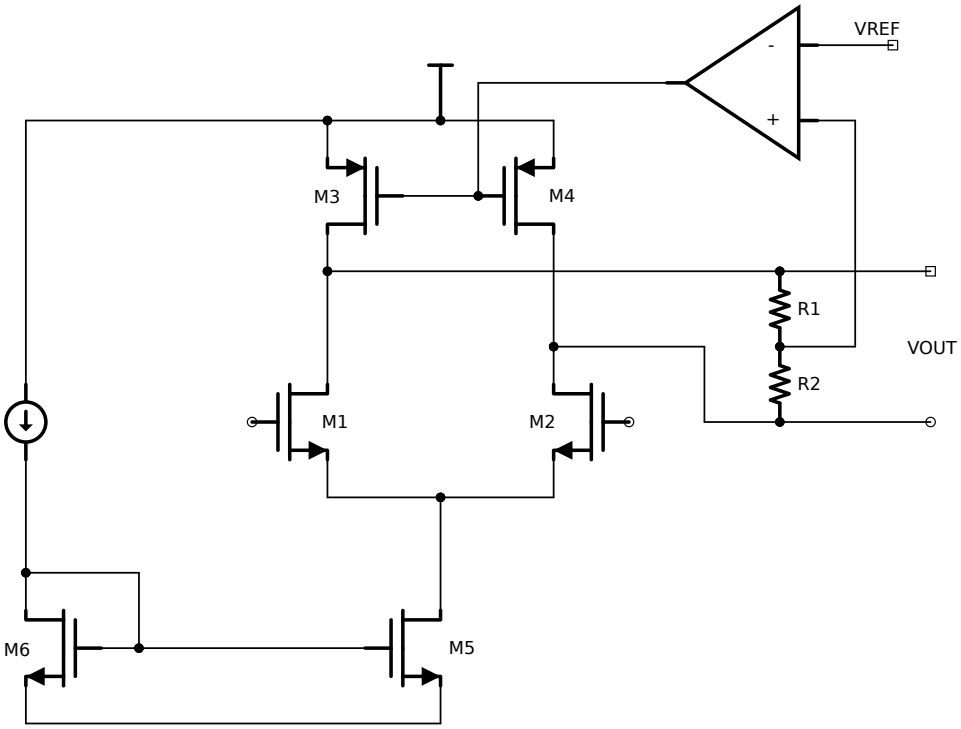

Figure 3.18: Schematic for gm_3.

The offset contribution of this stage will be somewhat reduced due to gm_4 sitting in front of it when referred to the input, but as pointed out in 2.3.2, there will be a residual offset present due to gm_3 that can be considerable at higher chopping frequencies.

It is decided to perform some simulations for the complete amplifier to determine an optimal value for the gain and transconductance of gm_3. It is responsible for filtering the ripple in combination with C_{M3}, as well as boosting the gain of the lower branch to reduce the residual offset. Initially, the sizing of the input transistors is set to a W/L ratio of 5 near minimum length, resulting in a gm/Id ratio of 28 when the bias is current is $600\,\mathrm{nA}$.

First, the ripple is evaluated. The peak-to-peak ripple is observed while the bias current of gm_3 is increased from $600\,\mathrm{nA}$ to $16\,\mu\mathrm{A}$. C_{M3} is set to $7\,\mathrm{pF}$ while V_{os4} equals $5\,\mathrm{mV}$.

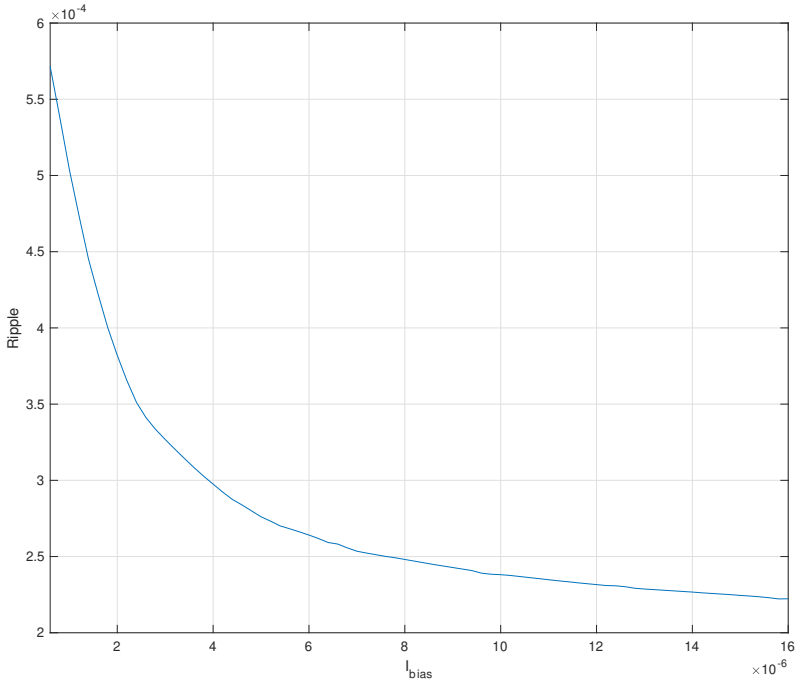

Figure 3.19: Ripple plotted against bias current of gm_3

The ripple shows a dependency on the transconductance of gm_3. At around $8\,\mu\mathrm{A}$ the lowering trend starts to fade out. Based on this result it this decided to increase the width of the input transistors with a factor 5 to operate at a transconductance of $100\,\mu\mathrm{S}$ at a bias current of $4\,\mu\mathrm{A}$. The ripple voltage at the expected worst case of V_{os4} now equals $250\,\mu\mathrm{V}$ peak-to-peak. For further attenuation, C_{M3} can be increased but there is a price to pay in terms of area usage. As $250\mu V$ peak-to-peak equals $177\,\mu\mathrm{V}$ [RMS], this result is treated as acceptable. Also, considering that the size of C_{M3} now is about 3-times larger than the

capacitors used for compensation, it is decided to not increase it any further.

Next, the residual offset is evaluated. Some smaller runs of Monte Carlo simulations with mismatch enabled is performed to see the effect of V_{os3}. The theoretical gain is calculated to be about $44.3\,\mathrm{dB}$. The simulated value shows an identical result. Because the lower branch now consists of several amplifiers with considerable gain, the residual offset should according to equation 3.1 approach zero. But, as uncovered by the Monte Carlo simulations considerable residual offset remains as described by equation 2.18.

The dimensions for the input pair is summarized in table 3.5.

	W	L	W/L	Area
NMOS	$5\mu m$	$200nm$	25	$1\mu m^2$

Table 3.5: Input transistor dimensions - gm_3

The sizing of the bias transistors is summarized in table 3.6.

	W	L	W/L	Area
NMOS	$1\,\mu\mathrm{m}$	$200\,\mathrm{nm}$	5	$0.2\,\mu\mathrm{m}^2$
PMOS	$3\,\mu\mathrm{m}$	$200\,\mathrm{nm}$	15	$0.6\,\mu\mathrm{m}^2$

Table 3.6: Bias transistor dimensions - gm_3

3.3.6 Design of choppers

The design of the two choppers is based on the structure shown in figure 2.4. Each switch is implemented using transmission gates as discussed in chapter 2.3.3. An increase in voltage spikes is observed for an increase in on-resistance. The inverter is implemented using minimum width and length. The NMOS and PMOS are sized equally with a $1\,\mu\mathrm{m}$ width and $160\,\mathrm{nm}$ length. With this dimension, the on-resistance for the switch is simulated to be $2.47\,\mathrm{k}\Omega$ and the resulting voltage spikes have a magnitude of $10\,\mu\mathrm{V}$. This result is treated as acceptable for this work.

Chapter 4

Results

The design is simulated and analyzed with the aid of the Spectre simulator. This is done in order to verify that the design upholds the specification stated in 1.1. All the results presented in the following sections are obtained using the designed amplifier configured as a voltage follower, with a $50\,\mathrm{pF}$ load capacitor on the output and an input common-mode voltage equal to VDD/2 = $900\,\mathrm{mV}$. All capacitors used are ideal and typical transistor models are used. The testbench is shown in figure 4.1.

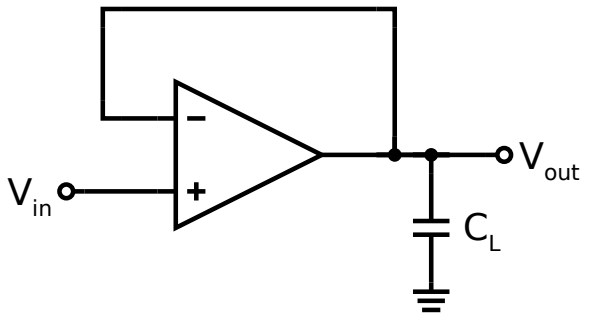

Figure 4.1: Testbench used for generating the results.

4.1 Gain and Frequency Response

The DC-gain for the different stages are analyzed individually with no mismatch enabled at a temperature of $27\,^{\circ}\mathrm{C}$. The results are shown in table 4.1.

Stage	$gm5$	gm_4	gm_3	gm_2	gm_1
DC-gain	103 dB	103 dB	44.3 dB	90.9 dB	37.0 dB

Table 4.1: Gain - individual stages.

The gain and the frequency response for the total amplifier is analyzed with no mismatch enabled at a temperature of 27 °C and the resulting bode-plot is shown in figure 4.2. The DC-gain is reported to be 270 dB, the phase-margin is 65° and the unity-gain frequency is 1.17 MHz, for unity-gain feedback.

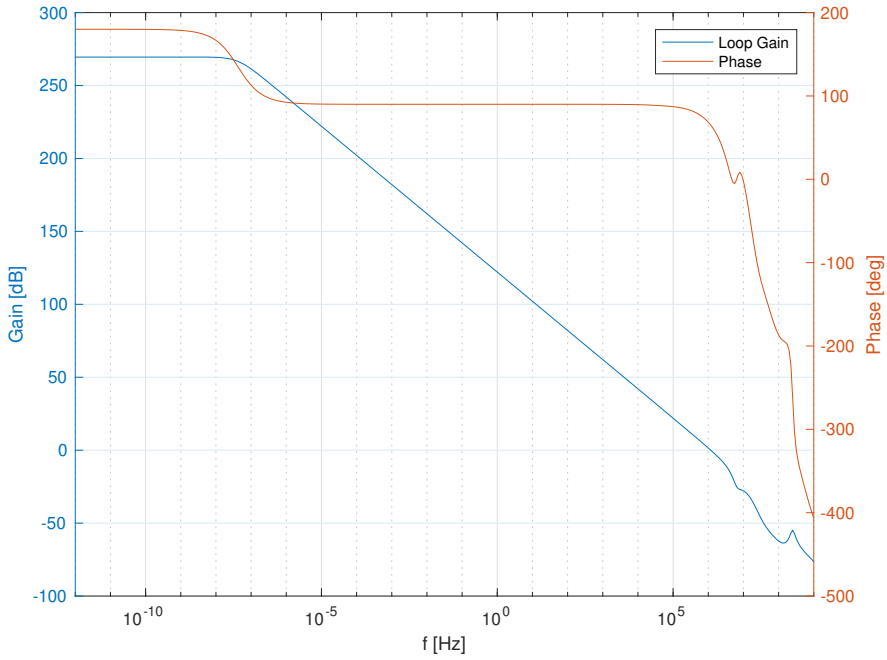

Figure 4.2: Bode plot of amplifier at 27 °C.

A Monte Carlo simulation with mismatch enabled is performed on a schematic netlist. The gain and frequency response is analyzed. This is done for three different temperatures, −40 °C, 27 °C and 85 °C. 10000 iterations are performed and the result is shown in table 4.2.

Temp	DC-gain,min	DC-gain,max	fug,min	fug,max	pm,min	pm,max
$-40\,°\mathrm{C}$	$146\,\mathrm{dB}$	$307\,\mathrm{dB}$	$1.39\,\mathrm{MHz}$	$1.75\,\mathrm{MHz}$	$54.8°$	$60.5°$
$27\,°\mathrm{C}$	$269\,\mathrm{dB}$	$286\,\mathrm{dB}$	$1.17\,\mathrm{MHz}$	$1.44\,\mathrm{MHz}$	$60.8°$	$65.2°$
$85\,°\mathrm{C}$	$257\,\mathrm{dB}$	$269\,\mathrm{dB}$	$1.17\,\mathrm{MHz}$	$1.44\,\mathrm{MHz}$	$64.3°$	$68.1°$

Table 4.2: Small signal quantities - mismatch enabled.

The same procedure is done with process variations enabled. 10000 iterations are performed and the result is shown in table 4.3.

Temp	DC-gain,min	DC-gain,max	fug,min	fug,max	pm,min	pm,max
$-40\,°\mathrm{C}$	$280\,\mathrm{dB}$	$319\,\mathrm{dB}$	$1.48\,\mathrm{MHz}$	$1.63\,\mathrm{MHz}$	$55.2°$	$58.8°$
$27\,°\mathrm{C}$	$269\,\mathrm{dB}$	$292\,\mathrm{dB}$	$1.26\,\mathrm{MHz}$	$1.35\,\mathrm{MHz}$	$61.7°$	$63.7°$
$85\,°\mathrm{C}$	$256\,\mathrm{dB}$	$272\,\mathrm{dB}$	$1.26\,\mathrm{MHz}$	$1.35\,\mathrm{MHz}$	$65.3°$	$66.9°$

Table 4.3: Small signal quantities - process variations enabled.

4.2 Offset

The offset of the amplifier is analyzed with and without chopping enabled. A transient analysis with noise enabled up to $100\,\mathrm{MHz}$ is used and 10000 Monte Carlo mismatch simulations are performed. The result is shown in table 4.4.

Temp	σ_{Vos} - Chopping disabled	σ_{Vos} - Chopping enabled
$-40\,°\mathrm{C}$	$1.93\,\mathrm{mV}$	$22.2\,\mu\mathrm{V}$
$27\,°\mathrm{C}$	$1.94\,\mathrm{mV}$	$25.7\,\mu\mathrm{V}$
$85\,°\mathrm{C}$	$1.99\,\mathrm{mV}$	$32.1\,\mu\mathrm{V}$

Table 4.4: Offset

The same result as shown in table 4.4 for σ_{Vos} - Chopping enabled at $27\,°\mathrm{C}$, is shown as a histogram in figure 4.3.

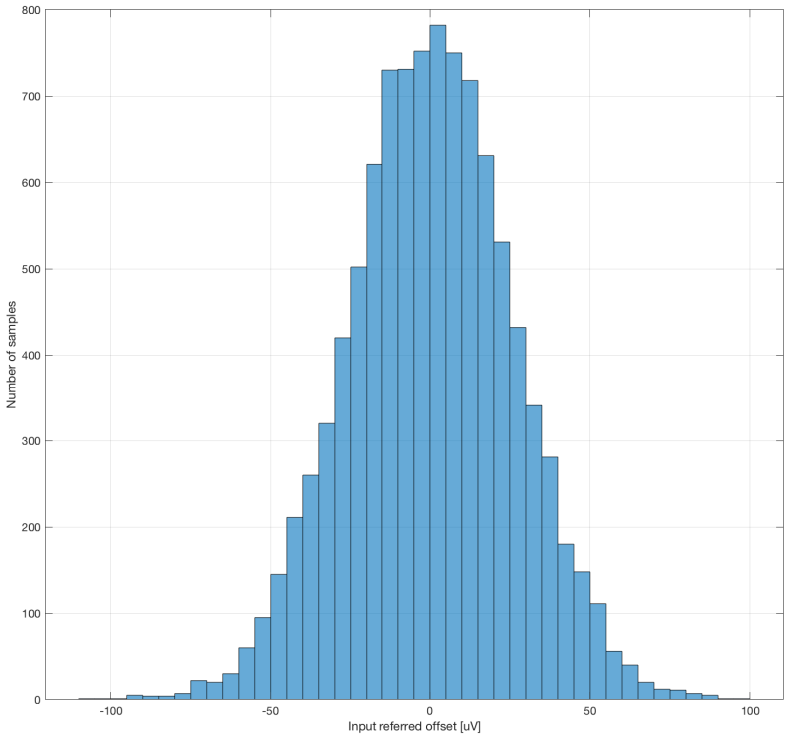

Figure 4.3: Offset histogram - chopping enabled at 27 °C.

The same result as shown in table 4.4 for σ_{Vos} - Chopping disabled at 27 °C, is shown as a histogram in figure 4.3.

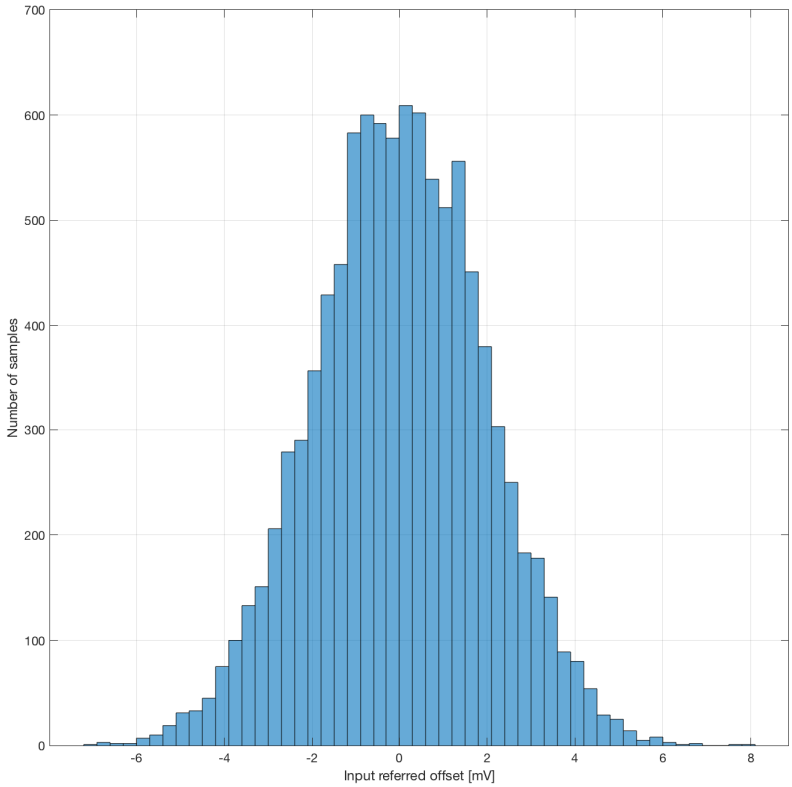

Figure 4.4: Offset histogram - chopping disabled at 27 °C.

4.3 Noise

The noise of the amplifier is analyzed with and without chopping enabled. A transient analysis with noise enabled up to 100 MHz is used. 10000 iterations are performed. The total integrated output noise, which includes device noise and ripple, with chopping enabled is shown in table 4.5.

Temp	Output Noise [RMS]
−40 °C	323 μV
27 °C	231 μV
85 °C	212 μV

Table 4.5: Output noise - chopping enabled.

A PSD is plotted in figure 4.5 with chopping disabled. The result is generated using 100 iterations of a transient analysis with noise up to 100 MHz enabled at 27 °C. Each iteration is run with a different noise seed and is presented as a periodogram.

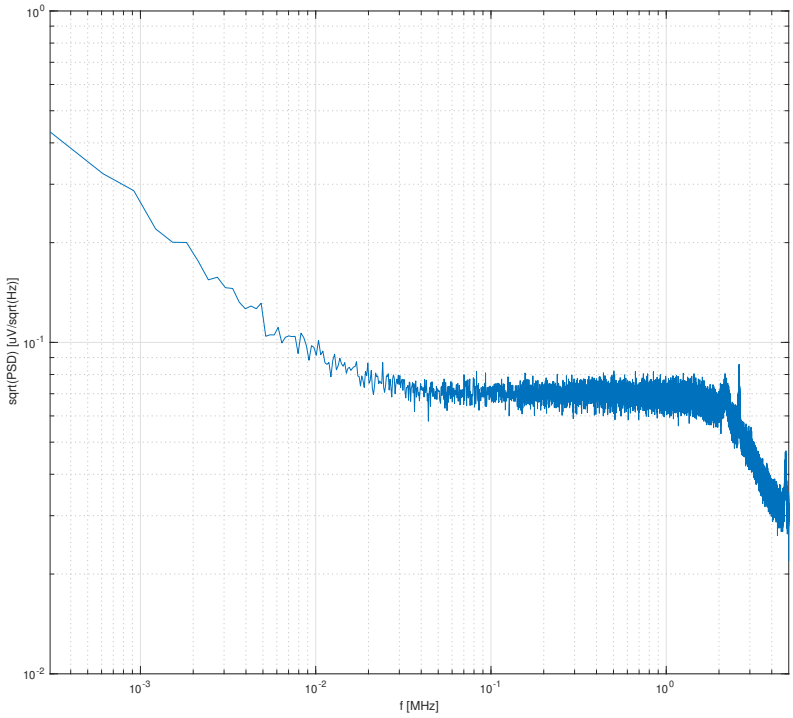

Figure 4.5: PSD - chopping disabled at 27 °C

Figure 4.6 is generated the same way as figure 4.5, but with chopping enabled.

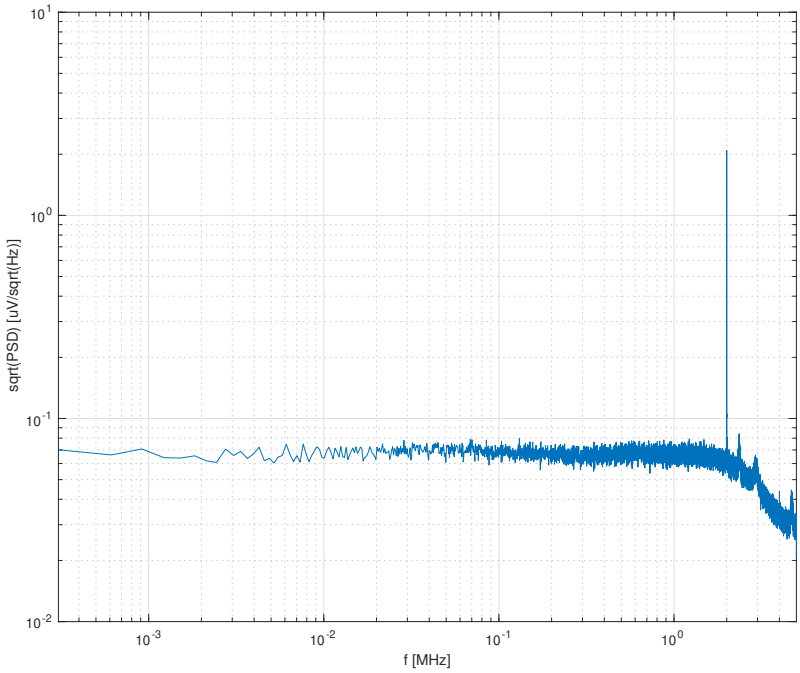

Figure 4.6: PSD - chopping enabled at 27 °C

Chapter 5

Discussion

A large DC-gain is reported both in table 4.2 and 4.3. The gain is regarded as so large that one could speculate wether the models provided by the foundry are erroneous. However, as some of the gain stages employ cascoding and a four-stage amplifier is used in the chopper branch, a higher gain than the specified $100\,\mathrm{dB}$, is regarded as realistic.

The gain can be calculated according to equation 3.6, based on the measured gain for the individual stages at a temperature of $27\,^{\circ}\mathrm{C}$ shown in table 4.1. The calculated gain with no mismatch and process variations for the total amplifier equals $274\,\mathrm{dB}$. A simulated bode plot for the amplifier with no mismatch and process variations at $27\,^{\circ}\mathrm{C}$ is shown in figure 4.2. The dominant pole is observed to reside at a very low frequency due to the large gain of $270\,\mathrm{dB}$ and a $-20\,\mathrm{dB/Dec}$ roll-off is observed down to the unity-gain frequency $1.17\,\mathrm{MHz}$. This is due to the Multipath Hybrid Nested Miller Compensation scheme. The calculated and simulated DC-gain are regarded as similar and therefore treated as valid as the calculation is only a theoretical approximation.

The DC-gain at $-40\,^{\circ}\mathrm{C}$ with mismatch enabled, is characterized by having a large spread. The lowest reported values around $146\,\mathrm{dB}$ occur six times out of 10000 and the unity-gain frequency is reported to be increased up to $1.75\,\mathrm{MHz}$. This will influence the noise performance at lower temperatures for some devices and will be discussed further below. All reported values fulfil the specified DC-gain of $100\,\mathrm{dB}$.

The phase margin is reported to be kept in the range 54.8° to 68.1° for all variations and temperatures. Because capacitors are kept at an ideal level in this work, this is regarded as overly optimistic and more variation should be expected in an actual realization. Since no phase margin is specified in the specification, this result is treated as acceptable.

Table 4.4 shows that by activating the chopper stabilization, σ_{Vos} is reduced by a factor

varying between 60 to 90, depending on the temperature. Without chopping, the design would not fulfil the specification. With chopping, it fulfils the specification with a healthy margin in terms of σ_{Vos} at a 4 sigma level in the specified temperature range. The worst case offset is reported to be $128\,\mu\mathrm{V}$. Due to the high gain in the chopper branch, equation 3.1 would suggest that the offset should be in the nV range with chopping enabled. Because of the offset associated with gm_3 and charge injection, one sigma for the residual offset is observed to be residing at about 20-30 μV. Since no layout has been implemented or simulated, this should be treated as an overly optimistic result, as the residual offset is expected to increase in post-layout simulations. Further reduction can be done by implementing residual-offset reduction as done in [1].

The variation of σ_{Vos} is $60\,\mu\mathrm{V}$ over the whole temperature range when chopping is disabled. This temperature variation is so small that one could speculate if the models provide limited accuracy in terms of temperature dependency. It varies $10\,\mu\mathrm{V}$ with chopping enabled for the same range.

All the noise measurements reported in table 4.5 fulfil the noise specification. The output noise is dominated by the ripple, shown in figure 4.6, as a spike at the chopping frequency $2\,\mathrm{MHz}$. Table 4.5 shows that the noise decreases for an increase in temperature. Thermal noise is shown to be increasing for an increase in temperature as shown in equation 2.6. Because the ripple noise dominates this trend is not shown in table 4.5. The increase of noise at lower temperatures is related to the increased unity-gain reported in table 4.2. The maximum unity-gain frequency is reported to be $1.75\,\mathrm{MHz}$. This results in less filtering of the ripple and thus increased output noise. Since the output noise criteria are fulfilled, it is shown that the continuous-time ripple-reduction approach using gm_3, provides adequate ripple reduction at a chopping frequency of $2\,\mathrm{MHz}$.

By comparing figure 4.6 and 4.5 the reduction of flicker noise is observed. The flicker noise at $305\,\mathrm{Hz}$ is reduced by a factor of 6 with chopping enabled. The input-refered noise is found to equal around $67\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ at a frequency of $100\,\mathrm{kHz}$.

Since layout has not been performed, the numbers presented are of limited accuracy compared to a manufactured design and generally presents overly optimistic results. Because of this, it is hard to estimate the total area usage and the performance of the design. It also makes it hard to compare to other designs.

With that being said, some comparisons will be done with the design in [1] and [5]. In [1], the chopping frequency is $16\,\mathrm{Khz}$, while in this work it is 125-times higher. This difference has enabled the use of smaller capacitors of $7\,\mathrm{pF}$ in the CT filtering compared to $40\,\mathrm{pF}$ used in [1] as documented in [4]. However as [1] utilizes a sample-and-hold for ripple-reduction in addition to the integrator, the ripple is reduced below the noise floor. One could argue that due to the increased power consumption and residual offset associated with operating at a chopper frequency in the MHz range it is more sensible to implement a more effective ripple-reduction and operate on a lower frequency. A more thorough analysis of the power consumption in this design must be done to be able to conclude on this issue.

Compared to the commercial general purpose amplifier shown in [5], the design done in this work provides a significantly lower offset over the same temperature range. The unity-gain frequency is reported to be kept above $1\,\mathrm{MHz}$ in all conditions. This enables the design to be used in general-purpose applications and shows comparable performance to [5] in terms of bandwidth. In terms of output noise, this design performs significantly worse. In some cases, the output noise in this design is a factor of 2 higher. To be able to show a more comparable performance, a more effective ripple-reduction might be required, as done in [1] and [9].

Chapter 6

Conclusion

The goal of this work was to design an amplifier that fulfils the specification stated in table 1.1. Realizing a robust design was emphasized, where one of the goals was keeping the offset below $1\,\mathrm{mV}$ and the noise level below $500\,\mu\mathrm{V}$, at a sigma level of 4, in the temperature range $-40\,^{\circ}\mathrm{C}$ to $85\,^{\circ}\mathrm{C}$. This condition has been analyzed using Monte Carlo simulations on a schematic netlist. Based on the results presented in this work, this seems to be fulfilled.

The most prominent tradeoff in chopper amplifiers is the relation between the bandwidth and ripple. The design is using a chopper offset-stabilized architecture and a chopping frequency of $2\,\mathrm{MHz}$ to realize a signal bandwidth of $1\,\mathrm{MHz}$. A continuous-time approach has been used to perform ripple-reduction. Large area usage is associated with this approach due to the capacitors necessary for filtering. Two $7\,\mathrm{pF}$ capacitors have been used in the filter and the area usage depends on capacitance density in the used technology. The output noise is kept below $500\,\mu\mathrm{V}$. The flicker noise is observed to be attenuated and translated into the ripple voltage occurring at the chopping frequency.

The large gain in the chopper branch of the amplifier successfully compensates for the offset. Without chopping, the design would not be able to fulfil the specification. With chopping enabled, σ_{Vos} is reduced with a factor of 60 to 90 depending on the temperature and kept below $1\,\mathrm{mV}$.

The design features a rail-to-rail input and output stage. Gm-equalization has been used to reduce the transconductance in the overlap region. A compact design, where a control circuit for the class-AB output stage has been embedded into the summation stage for a folded cascode has been designed, as done in [2]. With a $10\,\mathrm{mA}$ load current, the output is able to swing up to $1.55\,\mathrm{V}$ and down to $0.210\,\mathrm{V}$ with a supply voltage of $1.8\,\mathrm{V}$. Multipath Hybrid Nested Miller Compensation have been used for frequency compensation. Because

of this, a $-20\,\mathrm{dB/Dec}$ roll-off is obtained up to the unity-gain frequency.

Future Work

The capacitors in the design needs to be implemented with non-ideal devices. The ideal CMFB circuit needs to be replaced with a real implementation. Ideal current sources have been used in this design to generate bias currents. A non-ideal and robust bias generator that is able to provide a predictable current over a wide temperature range should be implemented. The quiescent current in the output stage can potentially be lowered. The switched-capacitor notch filter described in [9] can potentially lead to a substantial ripple reduction if implemented as a part of the chopper branch. This also opens up the possibility of realizing a bandwidth of several MHz's, as band-limiting the ripple is not needed. The residual-offset reduction circuitry described in [1] can probably be used to lower the offset to a couple of μV's but an evaluation of the increased complexity must be done. Performing Layout is an important step to be able to evaluate the design more accurately. Relevant layout guidelines are provided in [4]. Power consumption must be investigated in greater detail than what has been done in this work.

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Appendix A

Virtuoso schematics

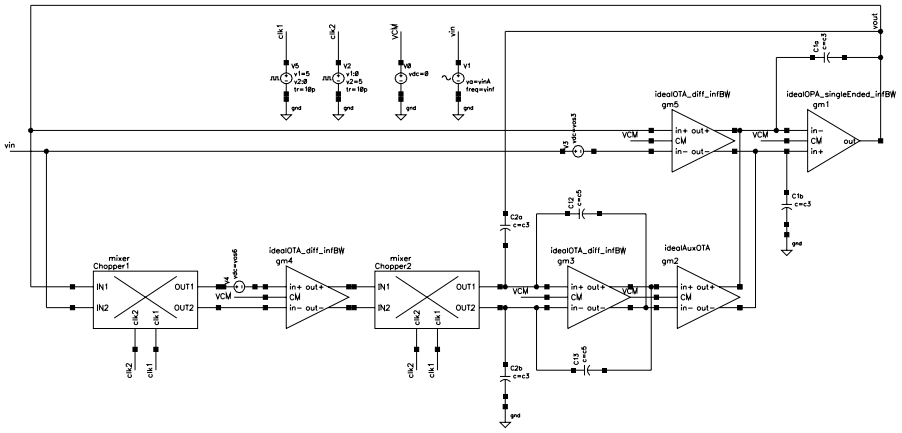

Figure A.1: High-level model - virtuoso schematic.

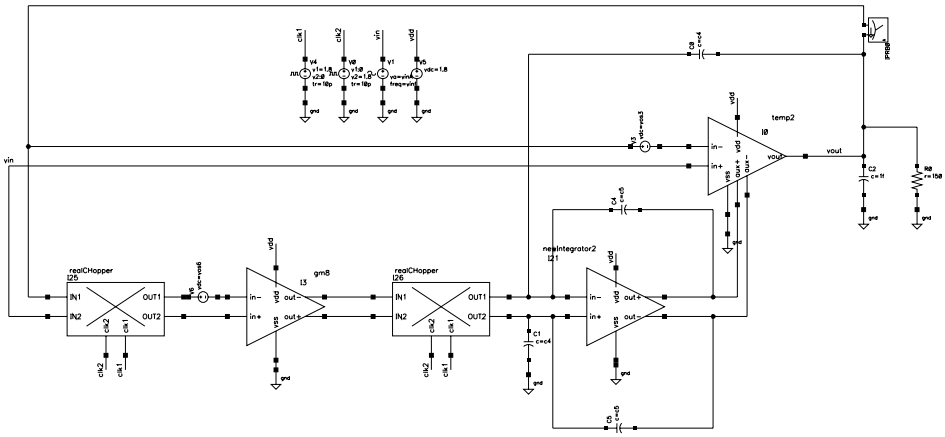

Figure A.2: Testbench - virtuoso schematic.

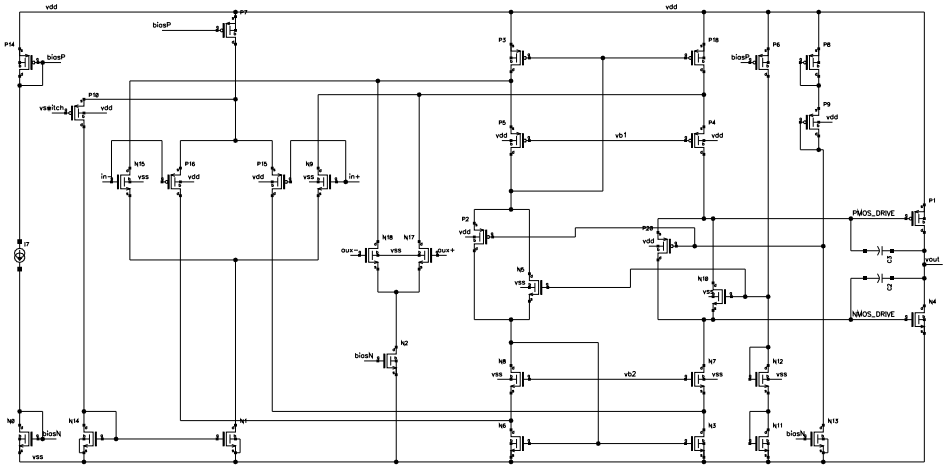

Figure A.3: gm_5, gm_2, gm_1 - virtuoso schematic.

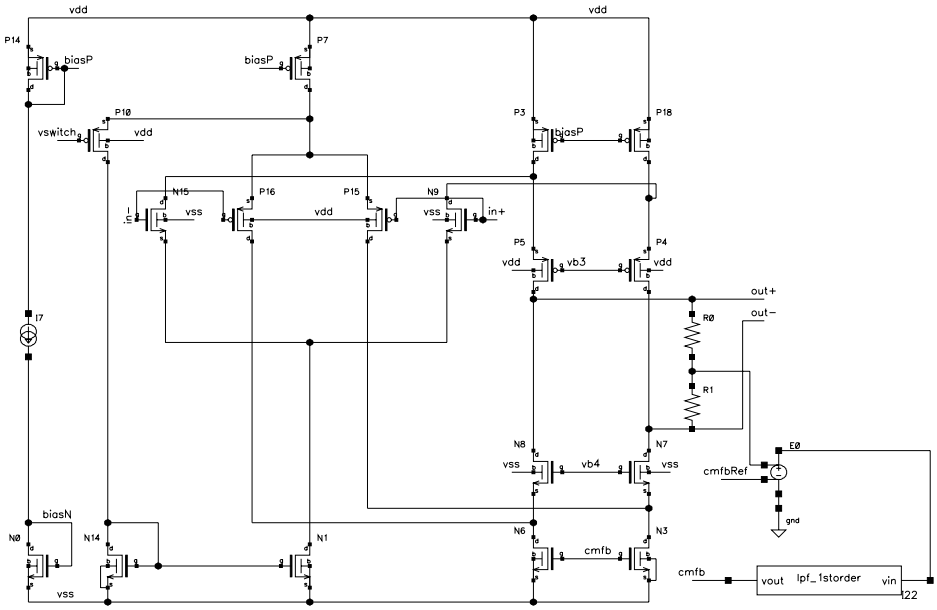

Figure A.4: gm_4 - virtuoso schematic.

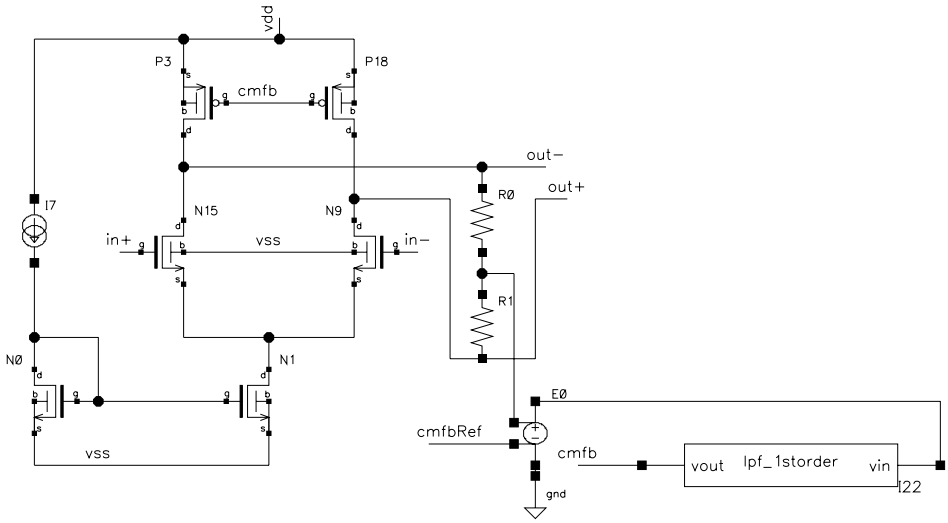

Figure A.5: gm_3 - virtuoso schematic.

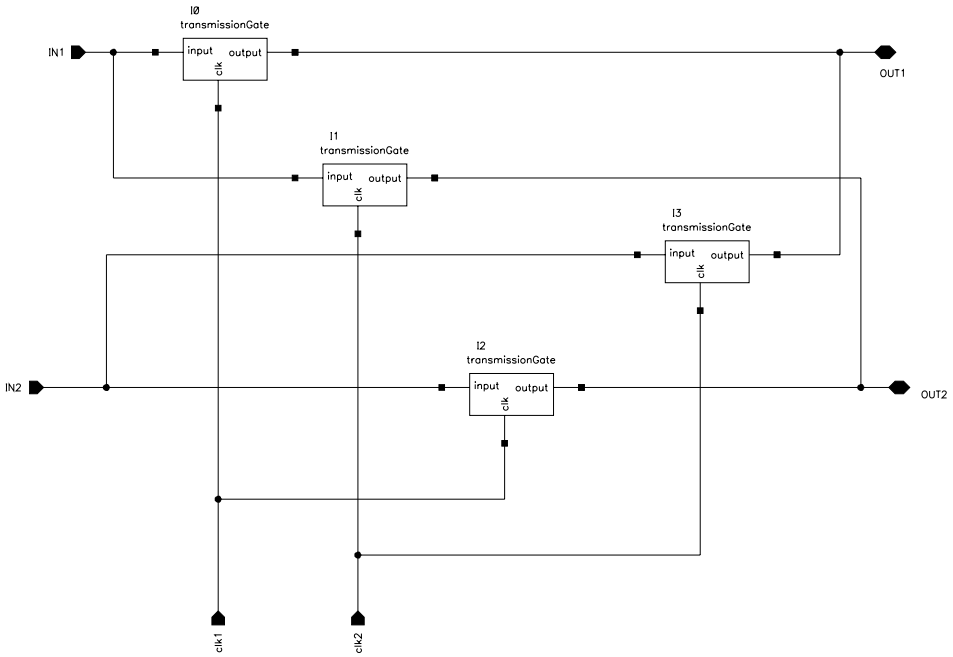

Figure A.6: Chopper - virtuoso schematic.

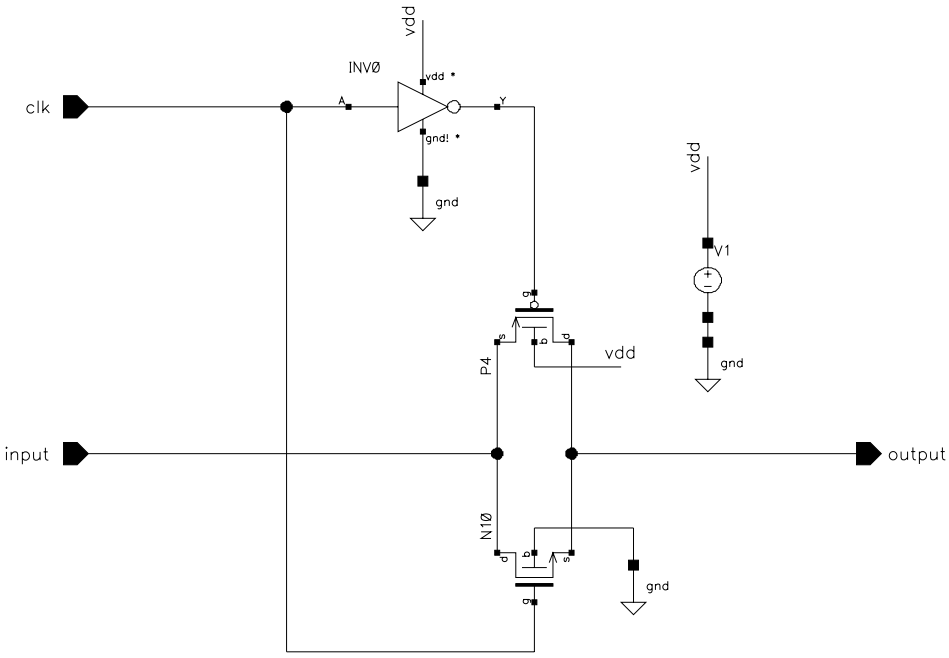

Figure A.7: Transmission gate - virtuoso schematic.