# High-voltage and high-frequency design of planar transformer with minimum coupling capacitance

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## Acknowledgments

## Keywords

## Abstract

This paper investigates the design of a planar transformer operating at 6.78 MHz and with a target maximum isolation voltage of 40 kV using 2D FEM simulations as a tool. In addition, minimal coupling capacitance must be ensured for the target application of auxiliary power supply for medium voltage converters with high EMI immunity. The design space for a transformer with target inductance and coupling capacitance of 1 μH and 10 pF is explored with varying number of winding layers and turns. From the simulation design space, five designs are prototyped for experimental validation. Overall, the prototypes show good coherence with the simulated values with inductance and coupling factors within an error margin of maximum 7%. Results show that different designs can achieve the same transformer efficiency although with different isolation voltages.

## Introduction

There is an increasing interest in medium voltage converters, as targeted applications can obtain lower operating costs or lowered total system costs. Main applications for medium voltage (up to 36 $kV_{RMS}$) converters include several industrial drives (fans, mills, pumps), wind turbines with fully-rated converters, medium voltage dc distribution grids for marine vessels, urban transportation, and flexible AC transmission systems (FACTS) used in medium voltage grids [1, 2, 3, 4]. Regardless of the medium voltage converter topology, dedicated auxiliary power supplies for the gate drivers in these converters give added system benefits such as improved safety and diagnostics of the medium voltage converter [5]. Typical power requirement for such an auxiliary power supply is 10 W [6]. If the medium voltage converter consists of SiC MOSFETs as switching devices, the output voltage of the auxiliary power supply should be above 20 V to match typical driving voltages for such devices (+15V/-4V). The insulation barrier of the auxiliary power supply will have to sustain the full dc-link voltage, which can reach several tens of kilovolts. Additionally, the coupling capacitance over the isolation transformer (see Fig. 1) in the auxiliary power supply constitutes a path for circulating current during switching events with high dv/dt [7]. Minimising the coupling capacitance will minimise the circulating current and, hence, reduce any related EMI issues.

Isolated power supplies feeding gate drivers in medium voltage converters are studied in several publications. In particular, auxiliary power supplies that consist of separate inverters that feed a single gate
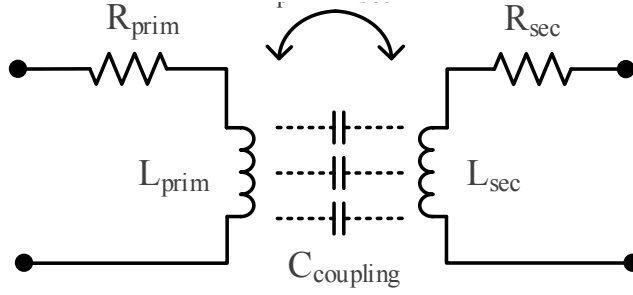
Fig. 1: Schematic circuit model of the transformer.
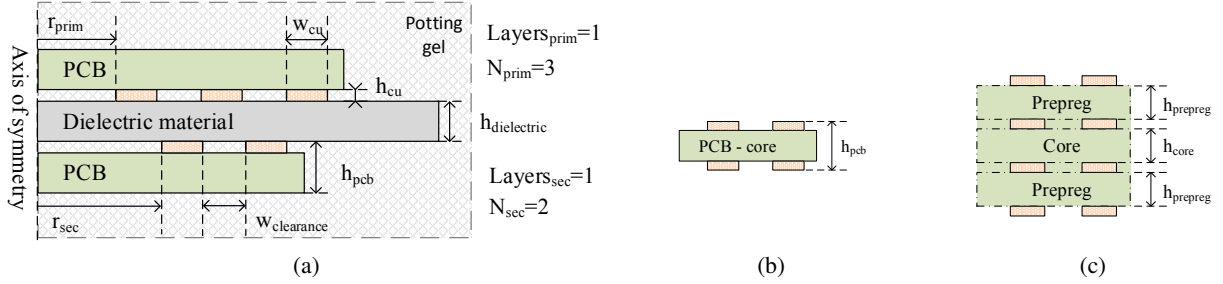


(a)                    (b)                    (c)

Fig. 2: a) Axisymmetric geometry of the transformer. Cross-section of b) two layer PCBs and c) four layer PCBs showing the stack build-up of multi-layered PCBs.

driver load are of interest [5, 8, 9]. The transformer of the auxiliary power supply is commonly designed with magnetic material and a small airgap in which a non-magnetic insulating material is placed. The high breakdown voltage of the dielectric material enables a high insulation voltage. The transformer is later potted to avoid air pockets. This dielectric design gives the isolated power supply a small footprint. However, it is reported that any increase in the gap distance, and hence the insulation voltage, drastically decreases the converter efficiency [8]. By selecting a suitable topology for the auxiliary power supply and increasing the frequency, the gap distance can be increased without seriously affecting the efficiency. Additionally, a planar transformer without a magnetic core can be used, further simplifying the manufacturing process and cost.

In this work, the dielectric design of such a planar, coreless transformer is investigated. The transformer will have to fulfil two requirements: high insulation voltage and low coupling capacitance. The transformer is designed for a fixed operating frequency of 6.78 MHz, a popular frequency in the available frequency bands among wireless power transfer systems. The investigation is performed using finite element method with 2D axi-symmetry. Section II defines the different transformer characteristics and the design goals of the paper. Then, the modelling and simulation procedures are described and the results of the simulations are presented in Section III. Experimental validation is presented and discussed in Section IV before the conclusions are drawn in Section V.

## Transformer characteristics

The circuit model of the transformer is shown in Fig. 1, where the primary and secondary sides consist of inductances ($L_{prim}$, $L_{sec}$) in series with an equivalent resistance of the winding ($R_{prim}$, $R_{sec}$). Furthermore, the transformer is characterised by a coupling factor ($k$) and a coupling capacitance ($C_{coupling}$) between the primary and secondary side. In addition, the transformer has a rated isolation voltage given by the dielectric design. All of these characteristics are coupled together through the geometry and the choice of materials.

### Transformer geometry

Each side of the planar transformer is printed as a spiral inductor on a PCB. Consequently, the winding geometry can be modelled as an axisymmetric problem. The geometry of the transformer is illustrated

Table I: PCB and winding parameters for the different design cases.

| Number of layers | Range of windings *prim/sec* | Height PCB core | Height PCB prepreg | Copper height | Copper width | Track clearance |
|---|---|---|---|---|---|---|
| 1 | from 2 to 5 | 0.9 mm | - | | | |
| 2 | from 1 to 5 | 0.9 mm | - | 35 μm | 3.0 mm | 0.5 mm |
| 4 | from 1 to 3 | 0.33 mm | 0.24 mm | | | |

in Fig. 2, where *prim* and *sec* indicate the primary and secondary side, respectively. Fig. 2a illustrates the windings as the number of winding layers ($\text{Layers}_{\text{prim}}$, $\text{Layers}_{\text{sec}}$), the number of turns on each layer ($N_{\text{prim}}$, $N_{\text{sec}}$), the width of the track ($w_{\text{cu}}$), the height of the track ($h_{\text{cu}}$), the distance between tracks ($w_{\text{clearance}}$), and the radius from centre to the inner winding ($r_{\text{prim}}$, $r_{\text{sec}}$). Furthermore, the height of the dielectric material placed between the primary and secondary side of the transformer is defined as $h_{\text{dielectric}}$. While Fig. 2a shows a transformer with primary and secondary sides made up of single layer PCBs, alternatively, the windings on either side of the transformer can be chosen to be made as multi-layer PCBs. The geometry of double layer and four layer PCBs are shown in Fig. 2b and 2c. For single and two-layer PCBs, the definition of the board height includes the copper layers. Consequently, the PCB core height is chosen as the total height minus the copper height. When producing a higher number of layers, there are different methods of building the PCB stack. A common stack for four-layer PCBs is shown in Fig. 2c. The two centre-layers are produced on a core as for a double-layer PCB and the additional layering is done by adding sheets of prepreg and copper. The consequence of the production method is that there are added degrees of freedom for PCBs of four or more layers. In this work, all PCBs are designed to have a total height of 1 mm, i.e. $h_{\text{pcb}} = 1$ mm, and the internal layer heights are adjusted accordingly (see Table I). For the investigation in this paper, the number of layers and windings is varied over a range as indicated in Table I.

Transformer designs across different number of layers, turns and dielectric height can be compared using a figure of merit (FOM) used for coupled inductors

$$FOM = \text{k}\sqrt{Q_{\text{prim}}Q_{\text{sec}}} = \text{k}\omega\sqrt{\frac{L_{\text{prim}}L_{\text{sec}}}{R_{\text{prim}}R_{\text{sec}}}} \tag{1}$$

where k is the coupling factor, $\omega$ is the angular frequency, and Q, L, and R represent the quality factor, inductance and resistance of either the primary or secondary side as indicated by the subscript. The FOM is a direct measure for the transformer efficiency [10]. For a target inductance value, the transformer efficiency is improved by lowering the track resistance and increasing the coupling factor. For an optimal coupling factor, the winding number, number of layers and the inner radius are set equal for the primary and secondary side [11]. It can be shown that the track resistance increases with increasing turn number [12]. Hence, minimum resistance is obtained for a single turn. However, this increases the effective area of the coil which in turn increases the coupling capacitance. This leads to increased gap distance and a reduction in the coupling factor. Hence, the optimal design is no longer trivial.

**Dielectric properties**

The isolation voltage criteria of the auxiliary power supply is met by choosing a dielectric material with the appropriate height ($h_{\text{dielectric}}$). The ideal dielectric material is non-magnetic, has a low permittivity and can sustain high electric fields. The insulation voltage of the transformer will depend on the material thickness and the maximum field it can sustain without breakdown. Assuming uniform electric field, the isolation voltage becomes

$$V_{\text{breakdown}} \leq E_{\text{max}} \cdot h_{\text{dielectric}} \tag{2}$$

where $E_{\text{max}}$ is the maximum electric field that the matieral can sustain. However, since the field in a practical geometry is rarely perfectly uniform, the actual breakdown will be lower than the maximum

Table II: Main design parameters for the transformer in this work.

| Insulation materials | Target inductance | Target capacitance | Operating frequency |
|---|---|---|---|
| Teflon (PTFE), Midel 7131 | $1.0\,\mu\text{H}$ | $10\,\text{pF}$ | $6.78\,\text{MHz}$ |

value as indicated by the inequality in Eq. 2. In addition, the material must not contain any voids or air pockets as these could lead to a premature breakdown. Hence, the transformer should be submerged in a dielectric liquid or potted in a gel to avoid flashovers. Examples of dielectric materials and a liquid are FR4, Teflon, Midel 7131. In addition to being non-magnetic, the dielectric constants are relatively low at 4.4, 2.0 and 3.15, respectively [13, 14, 15]. Although the whole transformer geometry could be produced as a single FR4 PCB, Teflon is used as the dielectric material in this work since it has lower permittivity and can withstand higher electric fields than FR4 material.

**Coupling capacitance**

The transformer coupling capacitance can be approximated as a plate capacitor, for which the capacitance is defined as

$$C = \frac{\varepsilon_0 \varepsilon_r S}{d} \tag{3}$$

where the plate area, $S$, is proportional to the area of the primary and secondary side windings, the gap distance, $d$, is approximately equal to the thickness of the dielectric material, and the permittivity, $\varepsilon_0 \varepsilon_r$, is given by the dielectric material. The geometry of the windings and the choice of the dielectric material will affect the final coupling capacitance value. For an accurate estimation of this value, a finite element analysis is required for which these variables are taken into consideration.

## Simulation results

To investigate the performance difference between the design cases and transformer geometries given in Table I, finite element analysis is used. Furthermore, Table II list materials and target values for the design space. The inductance and capcitance goals of $1\,\mu\text{H}$ and $10\,\text{pF}$ are set as reasonable values for the operating frequency and the application. For each combination of the number of layers and winding turns, the inner radius is adjusted to obtain the target inductance value. For 1, 2, and 4 layer windings, a maximum number of turns is set to 7, 5, and 3, respectively. This results in a minimum inner radius for which the 2D problem can be reproduced as experimental prototypes with minimal errors. The track width, height and clearance are unchanged between designs. Moreover, the height of the insulation material is dimensioned to obtain the target coupling capacitance. As the inductance and capacitance values are slightly cross coupled through the geometry, the design becomes an iterative process. The process is continued until the inductance and capacitance are found to be within $\pm 1\%$ of the target value. The simulations are carried out using *FEMM*, a free software for solving 2D problems using the finite element method [16]. Since spiral coils are used, the problem is defined as an axisymmetric problem. The same transformer geometry is used for the magnetic and electrostatic simulations. The self and mutual inductances, as well as equivalent series resistance (ESR), are calculated by changing the current in each coil. An example view from the simulation is shown in Fig. 3 when running current only in the primary coil. The coupling capacitance is found by applying a dc voltage potential between the conductors on the primary and the secondary side, and then calculate the capacitance from the calculated charge stored on the primary side conductors.

Figure 4a shows the ESR of the primary side windings, which is equal to the ESR of the secondary side. As expected, the lower turn number results in the lowest ESR. Similarly, a lower number of layers also decreases the resistance. Low ESR is preferred as it increases the transformer efficiency. Figure 4b shows the coupling factor of the transformers. A higher number of layers results in a higher coupling. This is due to the lower height of the dielectric for transformers made with multi-layer windings. This is explained by Eq. 3, as multiple layers give the same inductance but with a lower effective area between
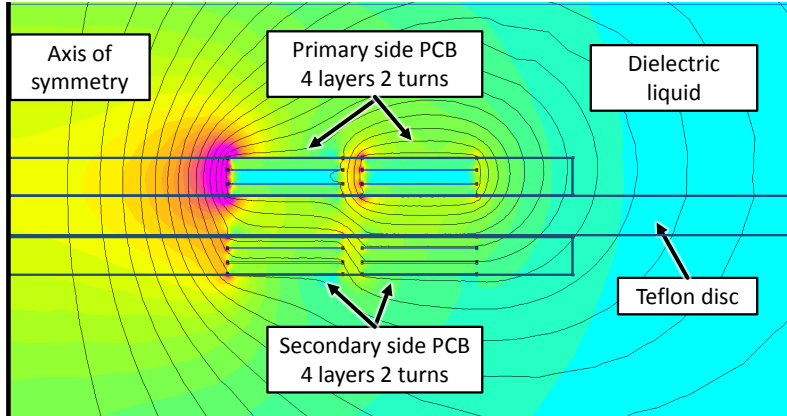
Fig. 3: Example view from FEMM of a magnetostatic problem of a planar transformer with 4 layer and 2 turns PCBs. The field lines are shown as black lines while the field density is coloured for a current running only in the primary side coil. The field density decreases as the colour changes from pink to yellow to cyan.
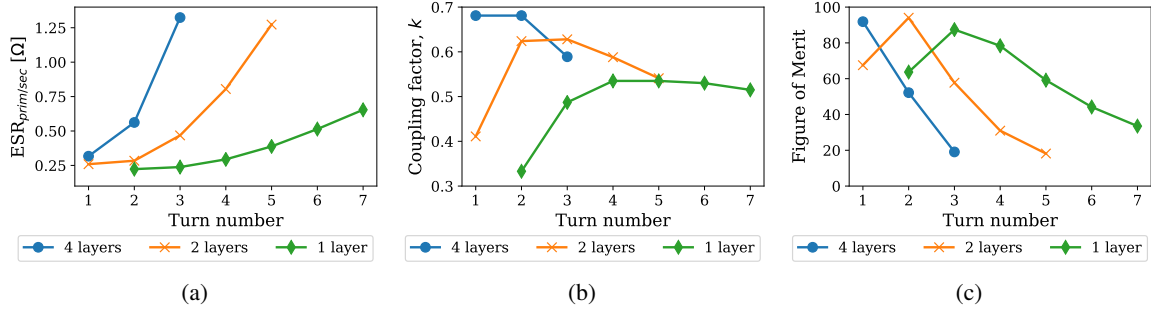


(a)                    (b)                    (c)

Fig. 4: FEM simulation results of a) equivalent series resistance (ESR) of either primary or secondary coil and b) the coupling between the two coils. c) shows the resulting FOM.

the primary and secondary side. In this situation, the 4 layer designs have the highest ESR and highest coupling, both of which affect the transformer performance. To compare the transformer efficiency, the FOM of all transformer designs are shown in Fig. 4c. It is observed that multiple designs can obtain a similar FOM, and the 2 and 4 layer designs obtain the highest FOM values of 94 and 92, respectively.

Although important, the efficiency is not the only performance parameter of a transformer. For the application targeted in this work, the dielectric height will be important as this is related to the transformer insulation voltage. Furthermore, the volume or area of transformer is important to achieve high power density. For these planar transformers, the outer winding radius is used as area parameter. The three parameters, the FOM, the height of the dielectric and the outer radius of the windings, are shown in Fig. 5 and indicate efficiency, maximum breakdown voltage and size of the transformer. For low number of turns and layers, the effective area between the coils becomes high as the radius needed to achieve 1 μH becomes large (Fig. 5c). As a result, the dielectric height is increased substantially as seen in Fig. 5b, e.g. 19 mm for 1 layer 1 turn coils compared to approximately 1 mm thickness for coils made on 4-layer PCBs. In terms of maximum transformer efficiency, the FOM matrix in Fig. 5a shows a diagonal trend. As indicated by the colouring, approximately the same FOM can be obtained across different number of layers and turns. On the other hand, 4 layer coils obtain the smallest size while 1 layer coils can sustain higher isolation voltages due to the increased height of the dielectric. Hence, the optimal design choice will depend on the application requirements.

| | PCB Layers | | |
|---|---|---|---|
| Turns | 1 | 2 | 4 |
| 1 | - | 68 | 92 |
| 2 | 64 | 94 | 52 |
| 3 | 87 | 58 | 19 |
| 4 | 78 | 31 | - |
| 5 | 59 | 18 | - |

(a)

| | PCB Layers | | |
|---|---|---|---|
| Turns | 1 | 2 | 4 |
| 1 | - | 10.5 | 1.3 |
| 2 | 19 | 3.1 | 1.0 |
| 3 | 9.0 | 2.6 | 1.1 |
| 4 | 7.0 | 2.6 | - |
| 5 | 6.5 | 2.8 | - |

(b)

| | PCB Layers | | |
|---|---|---|---|
| Turns | 1 | 2 | 4 |
| 1 | - | 52.5 | 19.2 |
| 2 | 59.2 | 24.3 | 12.2 |
| 3 | 38.4 | 19.2 | 12.2 |
| 4 | 31.2 | 18.2 | - |
| 5 | 28.4 | 18.6 | - |

(c)

Fig. 5: Main parameters of the design space used for the evaluation of best individuals. a) figure of merit b) height of dielectric material c) winding outer radius.

Table III: Comparison of designs chosen for prototyping.

| Prototype | #1 | #2 | #3 | #4 | #5 |
|---|---|---|---|---|---|
| Layers | 1 | 2 | 2 | 4 | 4 |
| Turns | 5 | 2 | 3 | 1 | 2 |
| FOM | 59 | 94 | 58 | 92 | 52 |
| Dielectric height [mm] | 6.5 | 3.1 | 2.6 | 1.3 | 1.0 |
| Outer radius [mm] | 28.4 | 24.3 | 19.2 | 19.2 | 12.2 |

## Experimental validations

From the design space identified in simulation, five designs with similar FOM and outer radius are selected for prototyping and experimental validations. These designs are presented and compared in Table III. The prototypes, seen in Fig. 6a, were printed on four-layer PCBs. Two identical windings were used as primary and secondary coils. They are placed in a fixture together with the dielectric material and then characterised using an impedance analyser (Keysight E4990A), see Fig. 6b. At the time of testing, Teflon was available in thicknesses of 1, 3, and 6.2 mm. To simplify the testing, these Teflon samples were used to construct the 4, 2 and 1 layer transformers, respectively. Hence, the actual dielectric height deviated slightly from simulated values reported in Fig. 5. However, when reporting the measured characteristics of the transformers, the simulation is redone with the actual geometry.

The prototypes have been measured using the impedance analyser. Five impedance measurements were done per transformer over the frequency range of 1 kHz to 120 MHz, the upper frequency limit of the test equipment. Both primary and secondary side are measured twice while the opposite side is either shorted or in open circuit. These measurements are used to characterise the inductive parameters of the transformer. The last measurement consists of measuring the impedance between the primary and secondary side while the terminals on both the primary and secondary side are shorted. This measurement method is used to characterise the coupling capacitance as described in [17]. The impedance data over the whole frequency range is then matched to a lumped parameter model using a genetic optimisation method. The identified lumped parameter values are summarised in Table IV.

Except for the prototype #5, the measured inductance values and coupling factors are within a maximum error margin of 7%. This shows that the simulated component results can be reproduced experimentally with good accuracy. The prototype #5 have an error of 15% compared to the simulated result. The PCB manufacturer reported challenges with the production related to this prototype, hence the large discrepancy is disregarded. Although, additional errors are expected for multi-layer and multi-turn transformer design as the via-connections are not modelled in the 2D problem. Such effects increase in gravity as component size becomes smaller.

The coupling factor for all transformers is within -6% of the simulated value, which again shows a good correlation between simulations and measurements. It should also be considered that the measured value could be affected by errors in alignment between the primary and the secondary PCBs.

Table IV: Comparison of transformer values between simulation and the experimental measurement.

| | Experimental value (error %) | | | | |
|---|---|---|---|---|---|
| Prototype | #1 | #2 | #3 | #4 | #5 |
| | 1 layer 5 turns | 2 layers 2 turns | 2 layers 3 turns | 4 layers 1 turn | 4 layers 2 turns |
| $L_{prim}$ [nH] | 1075 (6%) | 982 (-2%) | 1008 (-1%) | 998 (<1%) | 862 (-15%) |
| $L_{sec}$ [nH] | 1083 (7%) | 984 (-2%) | 1003 (-1%) | 995 (<1%) | 858 (-15%) |
| k | 0.503 (-2%) | 0.610 (-2%) | 0.562 (-6%) | 0.685 (-4%) | 0.643 (-4%) |
| $C_{coupling}$ [pF] | 8.18 (-24%) | 8.44 (-20%) | 7.44 (-19%) | 8.84 (-26%) | 8.46 (-14%) |
| $R_{prim/sec}$ [mΩ] | 328 (-16%) | 284 (-2%) | 468 (0%) | 359 (13%) | 712 (27%) |
| $FOM_{measured}$ | 70 (19%) | 92 (-2%) | 52 (-11%) | 81 (-12%) | 33 (-36%) |

The coupling capacitance values have a higher error in percentage, down to -26%. This results in an absolute error of approximately 2 pF. The average measurement error of the impedance meter is found to be around ±2%, hence the meter can not be the source of the tota l error. Small offsets in the placement of the two PCBs would result in a decreased area, and hence, decreased coupling capacitanc. Still, the authors hypothesis that the relatively large error is due to either over-estimation of the capacitance from the simulation or a static error of the measurement setup. The later could stem from the calibration step. Regardless of this, the measured capacitance is lower than the target value, which constitutes an advantage for the application.

The measured series resistance of the the prototypes is also reported. Although it shows large variations compared to the simulated value (-16 to +27%) this is within the measurement error band. The resistance greatly affects the value of the measured FOM, which is also reported in Table IV. Despite the large error band for the measured resistance, the FOM calculated from the measured values follows the trend found in simulation.
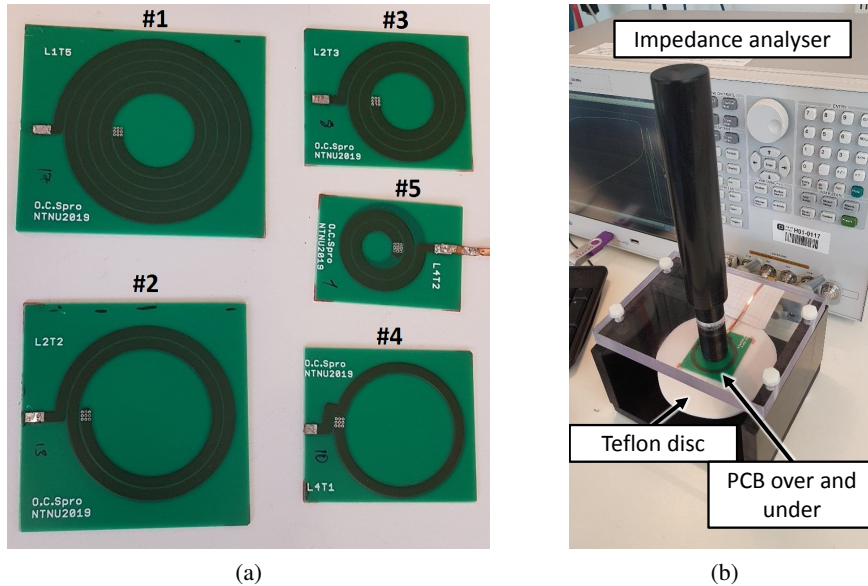


(a)                                    (b)

Fig. 6: a) The five transformer prototypes used in the experimental validation. b) Impedance measurement of the transformer using a fixture.

**Performance in converter operation**

To demonstrate the effect of FOM for the prototype transformers, the transformers are used in a simulated resonant converter. A series-series compensated resonance converter was selected due to its relative low component count. The converter schematic with added parasitic resistance elements is shown in Fig. 7. A dc voltage is supplied to an inverter leg that generates an ac voltage at the resonance frequency. The
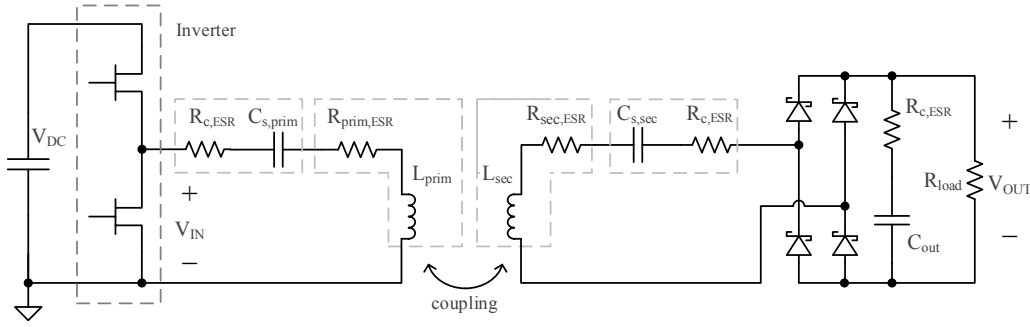
Fig. 7: Schematic diagram of the series-series compensated resonant converter. Probe symbols indicate the measurement points of the oscilloscope.

resonance capacitors, $C_{s,prim}$ and $C_{s,sec}$, are dimensioned so as to compensate the leakage inductance of the primary and secondary side, respectively. Hence the capacitance value is selected as

$$C_{s,prim/sec} = \frac{1}{\omega^2 L_{prim/sec}(1-k)} \tag{4}$$

where $\omega$ is the angular speed related to the switching frequency, $L_{prim/sec}$ is the self-inductance of either side of the transformer and $k$ is the coupling factor. This configuration leads to a constant voltage output, meaning that the output voltage is approximately constant for varying load resistor [18]. The parameters for the five transformers reported in Table IV are used in the simulation of the resonant converter. The inverter leg is modelled as a trapezoidal voltage with a maximum value of 48 V and with rise and fall times equal to 10 ns operating at a frequency of 6.78 MHz. An ESR of 100 mΩ is added to the capacitors and the inverter. The rectifier diodes are modelled as ideal diodes with a forward voltage drop of 0.5 V and a series resistance of 50 mΩ. The ESRs stay fixed for all tests and give a more realistic representation of the converter. The load resistor is varied from 45 to 2000 Ω. The resulting output voltage and output power match the application as described in the introduction. The simulations are carried out using LTSpice.

The output voltages and efficiencies are shown in Fig. 8 as a function of output power. The efficiency is calculated from the ac output to the load, although including the conduction losses of the inverter. It is observed that the output voltage is approximately constant over the whole power range for all transformer prototypes, as expected. By zooming in on the output voltage, a small difference in the output character-istics can be identified. The output voltage at maximum output power follows approximately the same trend as the transformers' FOM with a maximum difference of 0.4 V. If the circuit supplying the load resistance is modelled as a Thévenin equivalent, the difference in impedance would be related to the difference in transformer characteristics. Designs with lower FOM would have higher source impedance and hence increased voltage drop with increasing output power. Regarding the system efficiency seen in Fig. 8b, the efficiency is observed to also depend on the transformers' FOM over the whole output power range. Peak efficiency is obtained by prototype #4 at 90.7 %, compared to the worst case of prototype #5 at 85.1 %.

However, the efficiency of resonant converters is sensitive to small changes in operational parameters. Especially the output power, since the fixed losses are high compared to other converter types, e.g. circu-lating current. To obtain a fairer comparison, the input voltage, $V_{DC}$, is adjusted per transformer so that the output voltages are equal at maximum output power. The prototype with the highest output voltage in Fig. 8a is used as reference, i.e. prototype #2. The input dc voltage for prototypes #1, #3, #4 and #5 are increased from 48 V to 48.14 V, 48.78 V, 48.12 V and 48.85 V. The resulting output voltage curves and efficiencies are shown in Fig. 9. The spread in efficiency observed in Fig. 9b decreases compared to what is found in Fig. 8b. The peak efficiency is obtained by prototype #4 at 90.7 %, compared to the worst case of prototype #5 at 86.8 %. However, between the top three performing transformers, the difference in efficiency is small (#4 at 90.7 %, #2 at 90.5 %, and #1 at 90.2 %).
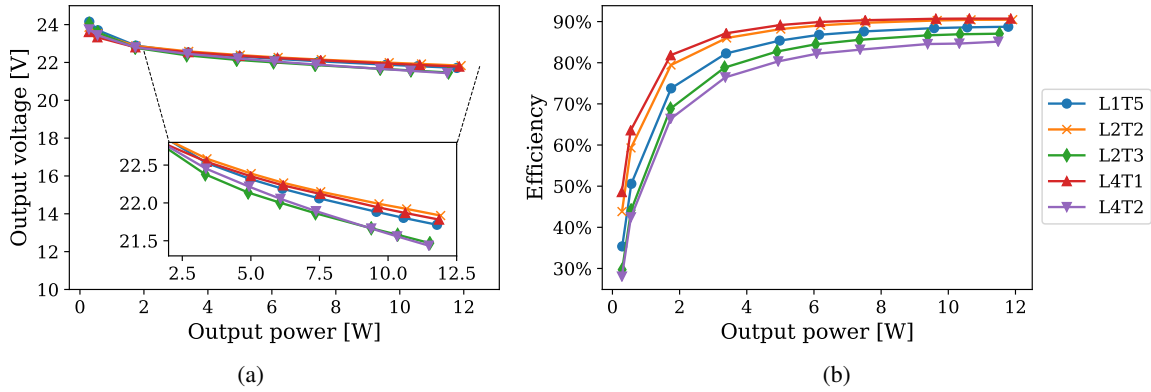
Fig. 8: Simulation results of the a) output voltage and a) efficiency as a function of output power. The input voltage is fixed between all five prototypes.
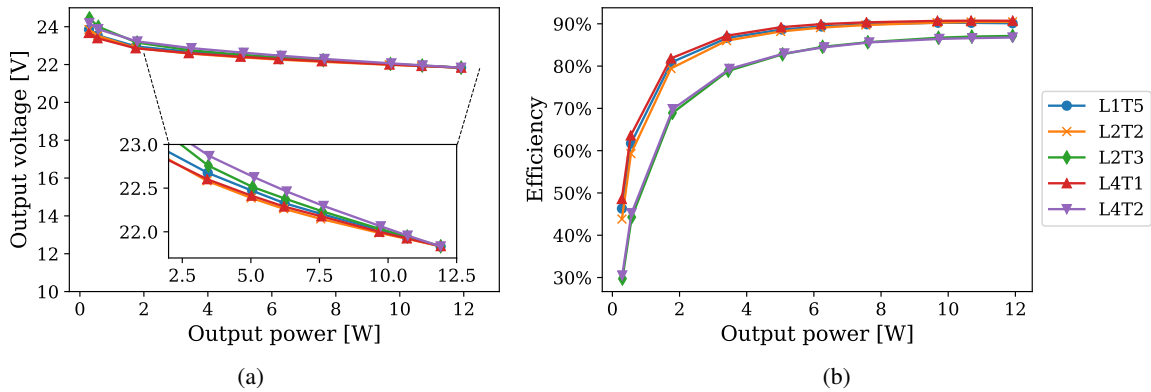


Fig. 9: Simulation results of the a) output voltage and a) efficiency as a function of output power. The input voltage is adjusted so that the the output voltage is equal for all five prototypes at maximum output power.

# Conclusion

This paper investigates the design of a high frequency planar transformers for auxiliary power supplies rated for an isolation voltages of 40 kV. The design space for a transformer with target inductance and coupling capacitance of 1 μH and 10 pF is explored with varying number of winding layers and turns. A figure of merit of approximately 90 is found to be obtainable for 1, 2 and 4 layer designs with 3, 2 and 1 turn, respectively. However, the dielectric height is different between them, which affects the maximal isolation voltage. From the simulation design space, five designs are prototyped for experimental validation. Overall, the prototypes show good coherence with the simulated values with less than 7% error. Hence, the design procedure is confirmed as suitable for the application. The performance of the prototypes are also investigated through simulated operation in a resonant converter. The results confirms that the FOM influences the converter efficiency. However, the comparison show that the difference in efficiency is small for the best transformers. Hence, other design constraints for the converter system could be more critical for the total system performance. Future work will focus on investigation of the dielectric properties of the transformer, in particular experimental testing of the breakdown voltage.

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