Electro-thermal Design of a Solid-State MVDC Circuit Breaker

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***Abstract*—This paper investigates the impact of several design parameters on the electro-thermal performance of a solid-state circuit breaker (CB) for medium voltage DC (MVDC) grids. The parameters studied are the cooling system design along with the ambient temperature under steady-state. The impact of the current limiting inductor and the threshold current that trips the breaker on the CB operation under short circuit condition was also investigated. The performance of the breaker is evaluated in terms of conduction power losses, dissipated power and junction temperature in the power electronic devices used. Four electro-thermal models for heat flux and junction temperature estimation have been developed and presented. The simulations highlighted the superiority of the "RC" equivalent thermal network in terms of required computational time and accuracy. Finally, the importance of designing the breaker according to the electrical and thermal limitations of the power electronic devices used is also highlighted.**

***Index Terms*—Solid-state circuit breaker, MVDC grids, thermal performance, cooling system.**

I. Introduction

Recently, medium voltage DC electric grids have gained momentum due to their inherent advantages over MVAC counterparts [1], [2]. The main reason to this is the expansion of distributed generation including the ever-increasing installations of renewable energy sources, as well as, energy storage systems dealing with intermittency of renewables. This paradigm shift in distribution grids faces a few crucial barriers that have to be tackled. Among them, one showstopper is the lack of high-performance protection schemes against DC short-circuit faults due to the absence of natural zero crossing of the current [3]. Hence, the use of the conventional mechanical circuit breakers used in AC power systems is ineffective. Furthermore, the relatively short cables and the absence of transformers in MVDC grids lead to excessive rates of fault current rise. Therefore, the development of high speed DC CBs is currently an inevitable development step for realizing MVDC grids. Mechanical CBs along with active or passive resonance circuits, solid-state CBs and hybrid CBs have been proposed in the open scientific literature for DC fault current handling [4]. In MVDC grids, the solid-state CBs seem to gain more attention due to their inherent advantages, such as, fast clearance times and low maintenance requirements. This leads to lower short-circuit currents compared to other CB topologies and thus, to lower thermal stress anticipated in the involved power electronics equipment of the grid (e.g. voltage-source converters) [5]. In literature, several different solid-state CB topologies have been presented, such as the interrupting CB and the resonance CB [6]. The interrupting CB exhibits a lower complexity compared to the others, and thus an increased reliability. Therefore, in this study, the interrupting solid-state CB has been adopted and presented.

One of the main drawbacks of the solid-state DC CBs is related to the excessive conduction power losses during normal operation, which leads to thermal stress of the power electronic devices [7]. At elevated junction temperatures of the power semiconductors, the conduction power losses increase and a more severe thermal stress is experienced. Therefore, the design of a high-performance cooling system is required to ensure an efficient operation of the DC CBs. For this purpose, a heatsink is used in order to dissipate the thermal energy generated in the chips to the ambient within a reasonable time period [8]. This will lead to lower temperature at the junction, and hence, the conduction losses will also be minimized. There are three different approaches regarding the thermal modeling and performance evaluation of power electronic systems; (i) analytical method, (ii) numerical method (i.e. Finite Element Method (FEM)) and (iii) equivalent thermal network approach [9]. For the last method, two models have been proposed, namely the Foster and the Cauer models. Both approaches use "RC" thermal networks of the equivalent thermal impedance to simulate the thermal performances.

In this paper, analytic investigations and design considerations for the interrupting CB topology are presented with an emphasis on the thermal stress of power electronic devices employed. The impact of several design and operating parameters on the conduction losses and the design of the cooling system is examined. Such parameters are the value of the current limiting inductor, the tripping fault current of the CB, as well as, the ambient temperature. In addition to these, the heatsink requirements are also investigated aiming to minimize the junction temperature and, thus, the conduction losses caused in the power semiconductor devices.

Finally yet importantly, the aim of this study is twofold. Firstly, the electro-thermal design of a solid-state DC CB taking into account several constraints of the power electronic devices used, such as maximum power dissipation and peak current is studied. For this purpose, four different thermal models have been developed and presented below. Secondly, the investigation of various parameters and their impact on the thermal performance of the CB is also presented and analyzed. The paper is organized as follows: Section II presents the different thermal strategies and models applied for power electronic devices. Section III analyzes the design principles of a solid-state DCCB, while the thermal analysis is shown

in Section IV. The next section describes both the electrical and thermal limitations associated with the power electronic devices. The case study along with the different applied thermal strategies are presented in Section VI. Lastly, Section VII illustrates the simulation results followed by conclusions in Section VIII.

II. Thermal analysis of power electronics

The thermal analysis of power electronic systems is of great importance as the requirements for high efficiency along with high power density increase. The basic thermal principles and the different developed thermal models which allow the accurate prediction of both heat flux and temperature within power electronic modules are discussed in this Section.

A. Heat transfer and heatsink design

The current that flows through a power electronic device generates heat within the chip layer. Therefore, this heat must be removed as fast as possible. Otherwise, the expected efficiency will decrease due to the temperature rise, while device reliability will also be affected. The heat can be transferred by means of; (i) conduction, (ii) convection and (iii) radiation. The design of an efficient cooling system is therefore required. Several different cooling systems have been proposed and presented in literature [10]. For high power applications, the use of fluid cooling system is more applicable.

B. Electro-thermal models

The optimization of the thermal performance of power electronics requires the development of appropriate electro-thermal models. The heat generation and propagation within the power electronic modules must be predicted precisely using these models. There are three mainly approaches for the electro-thermal modelling as follow.

1) Analytical models: The first approach is based on mathematical expressions. More specifically, heat diffusion equations have been used for the electro-thermal analysis of power electronic systems. The solution of these equations gives the temperature variation within the module and the heat flux as well. However, the existing power electronic modules with complex designs that consist of multiple layers prohibits the use of this method.

2) Numerical models: The second category includes computational fluid dynamics (CFD) and FEM numerical simulation methods. The temperature distribution can be obtained with high accuracy by adopting this approach. However, the geometry of the system under investigation along with the properties of the various materials used must be known. This might be highly challenging in certain cases, where the geometry of the system is complex. Moreover, the required simulation time for these cases can be long enough [11]. Therefore, the electro-thermal analysis under transient states (i.e. during a short-circuit, load variation etc) using this approach is not recommended.

3) Thermal network models: The development of electro-thermal models in order to predict the heat flux and the temperature distribution with respect to power losses can also be obtained through equivalent thermal circuits based on the thermal resistance (R) and the thermal capacitance (C). The derived circuit is in analogy to electrical circuits. Two different "RC" models have been developed, namely Cauer thermal network model and Foster thermal network model. Fig. 1 illustrates these two equivalent networks. On top of that, the manufacturer's datasheet of a power electronic device usually provides the required thermal "RC" values that are referred to the Foster model. It must be noted that all the nodes of both thermal network models do not have physical meaning. The junction temperature (on top of the chip) and the case temperature can only be obtained. The short required simulation time is the main advantage of this approach compared to others [9], [11]. This allows different investigations (i.e. variable load) to be conducted within short times.

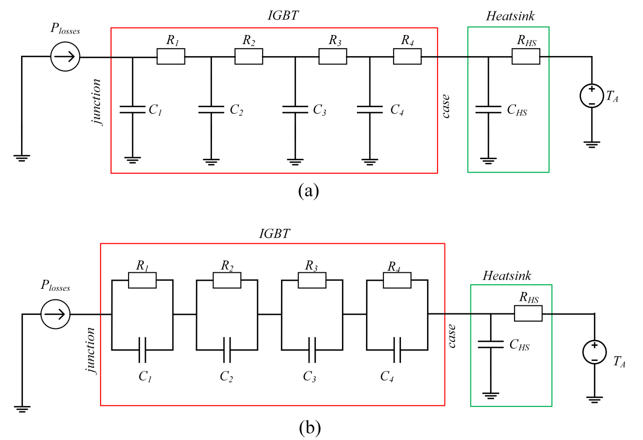

Fig. 1. (a) Cauer thermal network model and (b) Foster thermal network model.

Table I gives a theoretical comparison between the aforementioned thermal models in terms of the required computational time, model accuracy, geometry requirements (materials, dimensions etc.) and cooling system design. The last term is referring to the possibility for the actual construction of the heatsink, i.e. geometry design, materials used etc. and not simply to the equivalent thermal impedance of a heatsink (i.e. represented by "RC" components).

TABLE I
Comparison of the three different thermal models

	Thermal models		
	Analytical	***Numerical***	***"RC" Network***
Computational time	High	High	Low
Accuracy	High	High	Medium
Geometry requirements	Yes	Yes	No
Heatsink design	Yes	Yes	No

III. Design Principles of Solid-State DC CBs

Several different types of solid-state DC CBs have been identified in literature. They can be categorized into interrupting topologies and self-excited (or resonant-based) topologies. In the first type, the trigger of the CB is made by an external circuit. For this reason, a current sensor must be connected to the power circuit. When the sensed current exceeds the threshold current, a command for turning off the CB is provided to the control circuit of the power electronic devices. The self-excited topologies do not require current sensors for their interrupting operation. The fault current itself triggers the turn-off process of the solid-state breaker. Thyristor-based topologies have been mostly identified and presented in literature regarding the self-excited DC CB type [12].

Fig. 2 illustrates an interrupting solid-state DC CB. It consists of a current limiting inductor, power electronic devices (i.e. Insulated Gate Bipolar Transistors (IGBTs)), snubber circuits and Metal Oxide Varistors (MOVs). The grid components are also depicted, such as the line inductances and resistances prior and after the fault location, as well as the direct voltage source and the load. It should be mentioned that a number of "n" series-connected power electronic devices must be considered in order to withstand the voltage level of an MVDC power grid. Commercially available individual Silicon-based IGBT devices exhibit a maximum breakdown voltage of 6.5 kV. More information on this is given in Section V.

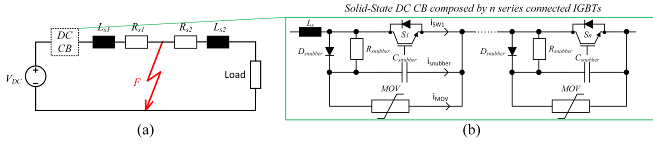

Fig. 2. (a) Schematic diagrams of simplified DC power grid and (b) solid-state DC CB.

A. Current limiting inductor design

The future MVDC grids are expected to have short-distance power lines. Hence, the inductances involved will also be low, leading to high rate of fault currents (di/dt), and, thus, a current-limiting inductor is externally connected in series with the DC line to limit di/dt. Therefore, an appropriate design of the current limiting inductor is essential for the protection of all involved components of the power grid. Neglecting the significantly low line inductances and resistances, the value of the current limiting inductor can be calculated based on the following equation:

$$V_{DC} = L_s \frac{di_{sc}}{dt} \tag{1}$$

where V_{DC} is the grid voltage, L_s the inductance of the current limiting inductor and i_{sc} the short-circuit current. It can be concluded, that the role of the current limiting inductor is twofold. It can limit both the maximum short-circuit current and the current rise.

B. Power electronic devices

Several different power semiconductor devices have been identified in literature as potentially candidates for a high power solid-state DC CB [13]. In particular, IGBTs [14], Gate Turn-Off (GTO) thyristors [15], Gate-Commutated Thyristors (GCTs) [16] and few other non-commercially available devices have been proposed and presented in literature [17], [18]. Currently, the high power Silicon-based IGBTs seem to have gained momentum over the other counterparts. Therefore, the solid-state DC CB evaluated in this study is designed based on IGBTs. Different structures related to IGBTs packaging have been identified and proposed [19]. They can be divided into three categories; (i) Discrete (ii) Modules and (iii) Press packs. For high voltage, high power applications, the last two types have been utilized. An analytic description of these is presented in [19]. The main advantage of the press pack IGBTs is that they ease the reliable series connection of multiple devices for higher blocking voltages.

ABB has commercialized the "StakPak IGBT", which belongs to the press pack family [20]. The main advantages of these devices are; (i) ability to carry the load current in a failure mode (Short Circuit Failure Mode (SCFM)), (ii) ability for double-sided cooling and (iii) easiness for series connection of multiple devices. Fig. 3 illustrates the main structure of StakPak IGBTs.

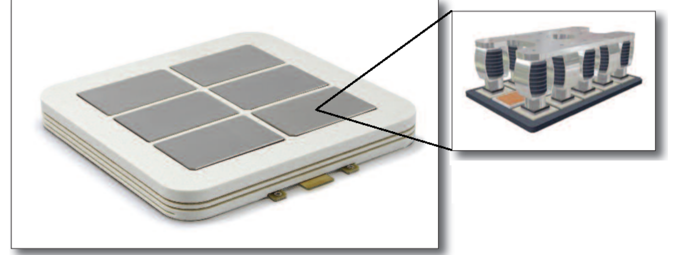

Fig. 3. StakPak structure with six submodules [20]

C. Snubber circuit and MOV design

In addition to the di/dt limitation, the dv/dt during the turn-off procedure must also be considered. The presence of both line and current limiting inductances, along with high rate of current rise can lead to overvoltages as well. Therefore, the use of a protective turn-off snubber circuitry is necessary, which usually contains a resistor, capacitor and diode (RCD). The basic snubber design principles followed in this study, rely on [21].

Apart from that, a MOV must also be connected as an energy dissipation device. When a short-circuit occurs, the power electronic devices are turned off. Then, the fault current is commutated from the main path (i.e. through the power electronic devices) to snubber circuitry. The final stage includes the current commutation from snubber circuit to MOV path. Therefore, the design of a MOV is very crucial for the efficient dissipation of the residual energy of the line. Furthermore, it is worth mentioning that for series connected devices, it is

a common practice to connect separate snubber circuits and MOVs, as illustrated in Fig. 2.

D. Design of the CB control

The solid-state controller consists of a comparative unit and a time delay module. The output produces the final signal that trips the breaking operation by turning off the power electronic devices. The value of the tripping current of the CB is crucial not only for the proper operation of the solid-state DC CB, but also for the entire DC power grid and its protection. It depends on the ratings of the current-sensitive electrical equipment involved in the grid, which mostly concern the connected power converters. The delay unit includes multiple potential delays, such as sensing delay, coordination strategy delay and tripping delay.

E. Impact of the grid parameters and fault resistance

Last but not least, a CB designer have to consider the parameters of the MVDC grid as well. The line inductance and resistance along with the fault resistance could influence the solid-state DC CB operation. Therefore, all the power system components must be taken into account for the optimal design and operation of the DC CB.

IV. Thermal Design of a Solid-State DC CB

The amount of heat that must be dissipated from the power semiconductors is caused by the direct current that flows continuously through the CB. As long as heat is generated in the chips, the junction temperature of the devices will rise, and as a result, the conduction losses will also increase due to the positive temperature coefficient of the on-state resistance of the IGBT. A fast and efficient heat dissipation is therefore desirable. The time constants involved in thermal analysis are usually high, leading to the different applied analyses in steady state and in dynamic responses.

A. Steady-state analysis

In normal operation of a solid-state CB, the heat that needs to be dissipated is equal to the conduction power losses of the power electronic devices. When IGBTs are used, the conduction losses are given by the following equation:

$$P_{losses} = I_{rms}^2 r_{on(Tj)} + u_{CE0(Tj)} I_{DC} \quad (2)$$

Where, I_{rms} is the RMS value of the current that flows through the power electronic device, $r_{on(Tj)}$ is the collector-emitter on-state resistance of the IGBT depending on the junction temperature T_j, I_{DC} is the average value of the collector current and lastly, $u_{CE0(Tj)}$ is the on-state zero-current collector-emitter voltage of the IGBT depending slightly on the junction temperature. For a continuously flowing direct current, the RMS value of the current is equal to the average value. It must be noted that the on-state resistance increases with respect to junction temperature rise, leading to higher losses at high temperatures. Therefore, an efficient cooling system design could potentially reduce the losses.

B. Transient analysis

The heat must be dissipated as fast as possible in order to keep the junction temperature below certain limits. When a short-circuit occurs, the current rises inversely proportional to the inductances of the DC line according to Eq. 2. As mentioned above, in a future MVDC grid, the line inductance will be low, leading to high current increase. As a consequence, the conduction power losses will also be excessively high. Hence, the power electronic devices must be able to dissipate the generated heat as efficiently as possible. Furthermore, the heat is transferred from the junction to the case and afterwards to the heatsink and ambient. It must be mentioned that the heat extraction usually needs several milliseconds. This leads to the conclusion that the rate of the current rise is a crucial design aspect not only from the electrical stress point of view, but also from the thermal stress perspective, making the heatsink design particularly challenging.

V. Electrical and Thermal Limits of Power Electronic Devices/IGBTs

The capability of a solid-state DC CB to operate and interrupt the fault current in a desired way is defined by several parameters. The current semiconductor technology determines mostly the limits of the power electronic devices. This section describes the key parameters that have to be considered when IGBTs are used in a CB configuration. They can be categorized into electrical and thermal limiting factors [22], [23]. In addition to these, there are also some mechanical limitations. These are mostly related to the proper mounting of IGBTs with heatsinks and to the force that a power semiconductor device must be clamped with. Further analysis related to mounting instructions for StakPak devices is given in [24].

A. Electrical limiting factors

The most significant limiting factors for power semiconductor devices are related to their physical structure. The design of a solid-state DC CB relies on the constraints of the power electronic device used. Regarding the electrical restrictions of an IGBT, i.e. voltage and current ratings, the following parameters must be considered.

V_{CES}: Maximum blocking voltage of the device. If the collector-emitter voltage exceeds this value, even for a short period, the device might possible fail. The potential overvoltages along with cosmic radiation leads the operating voltage to be significantly lower than the maximum blocking voltage given by datasheet.

I_{CM}: Peak collector current. The maximum collector current that the IGBT can turn off without latch up. Higher currents than this limit may lead to turn-off failures. Furthermore, the device might be overheated if the duration is long enough.

di/dt: Maximum rate of collector current change during turn on. The current can not be changed instantaneously, and therefore some limitation are applied to the rate of the collector current.

dv/dt: Maximum rate of the voltage change during turn off. Similarly to the previous limitation, the voltage across the

device can not be changed instantaneously. Some physical constraints prohibit the step change of the applied voltage.
t_{psc}: Maximum duration of a short-circuit current pulse under specific given conditions. Exceeding this time might lead to device failure.

B. Thermal limiting factors

Apart from the above electrical limits, the datasheet of an IGBT device provides some thermal constraints as well. The aforementioned factors are the following:
P_{tot}: Maximum power dissipation in the IGBT. The IGBT can handle and dissipate a certain amount of heat. Exceeding this limit, the device might fail by overheating.
T_{vj}: Maximum junction temperature. The chips that comprising the IGBT device can withstand temperatures up to that level.
$T_{vj(op)}$: Maximum junction operating temperature. This limitation applies for the materials used in the IGBT device.
T_c: Maximum case temperature. The case of the IGBT device must also be within certain temperature limits, which are given by datasheet.

VI. Case Study and electro-thermal modeling

The DC power grid shown in Fig. 2 has been adopted. The purpose of this study is twofold. Firstly, the investigation of the impact of several parameters on the thermal performance of the power electronic devices employed in a solid-state DC CB configuration. Two analyses have been conducted and presented below. The first examination is referring to steady state analysis, while the second to the dynamic state, i.e. during the short-circuit. The under consideration parameters are the following:

1) Ambient temperature, T_A.
2) Inductance of the current limiting inductor, L_s.
3) Threshold current, I_{det}.
4) Heatsink requirements in terms of its thermal resistance, R_{HS}.

The second purpose is related to a comparison between different thermal models for power electronic devices. As mentioned in Section II, different thermal strategies can be applied in order to estimate the heat flux and the temperature within a power electronic device. In particular, in this study a solid-state DC CB has been examined and the power electronic device used is the IGBT Press Pack. Four different thermal models have been developed and compared in terms of accuracy, computational time, ability for transient analysis, geometry requirements and finally, ability for applying optimization methods. These four approaches made for the thermal evaluation of power electronic devices employed in CBs are given below.

A. Model 1: Using PLECS

The PLECS software has been used for the simulation of the solid-state DC CB along with the entire DC power grid. The thermal analysis can also be conducted since PLECS allows it by importing the specific model of the power electronic device used. The junction temperature therefore can be found. The heatsink design can be done by means of thermal impedance $R_{HS}C_{HS}$ estimation as illustrated in Fig. 1.

B. Model 2: Using FEM/COMSOL

COMSOL have been considered for the evaluation of the thermal performance of a Press Pack IGBT comprising a solid-state DC CB as a numerical thermal model. The appropriate modelling of Press Pack power electronic devices can be highly challenging since it requires the knowledge of the geometry analytically (i.e. dimensions, materials used etc.). For the purposes of this study, the power losses estimated by PLECS have been used as a heat source in COMSOL model. Since the heatsink design is beyond the scope of this paper, it has been considered a bulky heatsink with specific equivalent thermal impedance in consistency with the other models.

C. Model 3: Using "RC" Foster thermal network model

The datasheets of power electronic devices usually give their equivalent thermal impedance, Z_{th} of Foster thermal network. Therefore, by using the electrical-thermal analogy, it is possible to estimate the junction temperature of the devices used. It must be noted that there is no physical interpretation of each node in this model. However, the junction and the case temperatures can be derived via this approach. Similar to "Model 1", the heatsink design has been performed by means of its thermal impedance $R_{HS}C_{HS}$.

D. Model 4: Using Analytic thermal model for steady state analysis geometry-based

When the geometry of an under investigation object is known analytically, then a thermal model based on the dimensions and the materials used can be built. Therefore, this approach takes into account the geometry of the Press Pack IGBT used as illustrated in Fig. 3. The complexity of the geometry of these devices though, has led to the development of a simple "R" (thermal resistance) thermal model instead of an "RC". Therefore, the transient analysis can not be done by means of this approach. Finally, the heatsink design has been made similar to other models, i.e. with its equivalent thermal impedance $R_{HS}C_{HS}$.

Table II illustrates the considered parameters as base case. Furthermore, five series-connected IGBTs of the type 5SNA 2000K450300 (StakPak) were used in order to withstand the direct voltage of the grid. This device consist of 6 submodules. Each submodule includes 12 chips, with an IGBT to diode ratio of 1:1.

VII. Simulation Results

As mentioned above, the DC power grid illustrated in Fig. 2 has been modelled through PLECS. Fig. 4 illustrates the current and voltage across each power electronic device and the four currents of a solid-state DC CB, that is the MOV current, switch current, snubber current and fault current. The short-circuit has been assumed to occur at the time instant $200msec$. A fault clearance time of $450\mu sec$ is observed. In

TABLE II
BASIC PARAMETERS OF THE UNDER CONSIDERATION POWER GRID

Parameters	***Symbol***	***Value***	***Unit***
DC voltage	V_{DC}	15	kV
Load	P_{load}	22.5	MW
Line inductances	L_{s1}, L_{s2}	1	μH
Line resistances	R_{s1}, R_{s2}	1	$m\Omega$
Ambient temperature	T_A	35	C
Current limiting inductor	L_s	150	μH
Threshold current	I_{det}	3	kA
Heatsink thermal resistance	R_{HS}	10	K/kW
Total delays (i.e. sensing etc.)	t_d	1	μsec

addition to this, it is clear that both the peak switch current (i.e. $3.6kA$) and voltage (i.e. $3.4kV$) are within the SOA of the devices used.

Regarding the electro-thermal analysis, a steady-state and a dynamic have been conducted and presented below.

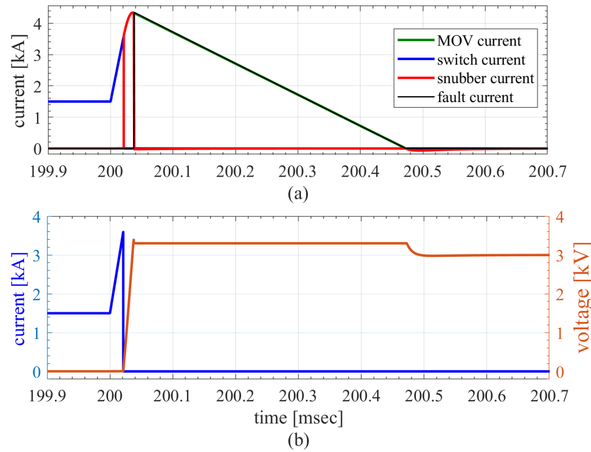

Fig. 4. Simulation results of (a) the various currents in solid-state DC CB, and (b) current and voltage across the IGBT.

A. Steady-state analysis

The impact of the ambient temperature, T_A along with the heatsink design on the thermal performance of an interrupting solid-state DC CB is illustrated in Tables III-V. The results summarized in these tables are referring to a single power electronic device. The positive temperature coefficient of the IGBT on-state resistance leads to increased conduction losses by considering higher ambient temperature. More specifically, every 10° rise of ambient temperature, a drop of 2.5% of the efficiency has been observed. Apart from that, the cooling system can also influence the junction temperature and, thus, the conduction losses. Furthermore, a higher efficiency can be achieved, by taking into account a lower thermal resistance for the heatsink. In particular, a reduction of 30% of the thermal resistance may increase the efficiency of the device by 10%.

Apart from the impact of the ambient temperature and the heatsink design, a comparative study between various electro-thermal models have been conducted and presented. As shown

TABLE III
IMPACT OF THE AMBIENT TEMPERATURE ON CB THERMAL STRESS WITH $R_{HS} = 5K/kW$

$T_A[^oC]$	$T_c[^oC]$	$T_{vj}[^oC]$	***Conduction losses [W]***
25	44.5	60.5	3909
35	55	71.4	4007
45	65.5	82.3	4104
55	76	93.2	4202

TABLE IV
IMPACT OF THE AMBIENT TEMPERATURE ON CB THERMAL STRESS WITH $R_{HS} = 10K/kW$

$T_A[^oC]$	$T_c[^oC]$	$T_{vj}[^oC]$	***Conduction losses [W]***
25	66.1	82.9	4110
35	77.1	94.3	4212
45	88.2	105.8	4315
55	99.2	117.2	4418

in Section VI, four different strategies have been investigated and evaluated. Among them, the "model 2" is referring to a FEM (COMSOL-based) approach. Fig. 5 illustrates the temperature distribution within a single IGBT StakPak module.

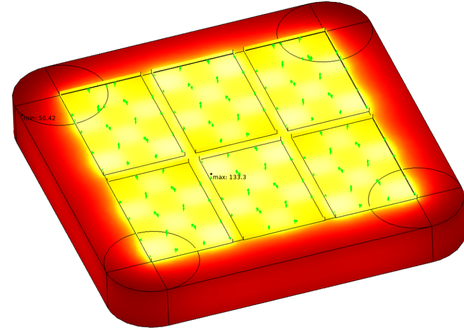

Fig. 5. Temperature distribution within an IGBT StakPak.

Fig. 6 depicts the comparison between the 4 electro-thermal models under six different current cases and hence, 6 different power loss amounts associated with power electronic device used. It is concluded that the three thermal models (i.e."models 1-3") achieve similar performance to each other, while "model

TABLE V
IMPACT OF THE AMBIENT TEMPERATURE ON CB THERMAL STRESS WITH $R_{HS} = 15K/kW$

$T_A[^oC]$	$T_c[^oC]$	$T_{vj}[^oC]$	***Conduction losses [W]***
25	89.9	107.6	4331
35	101.5	119.6	4440
45	113.1	131.6	4548
55	124.7	143.7	4655

4” seems to loose accuracy at high power losses and therefore high junction temperatures. Last but not least, it should be mentioned that “model 3” required the shortest computational time (i.e. in the range of microseconds), while “model 2” needed the longest time (i.e. in the range of minutes) to perform the same simulation studies.

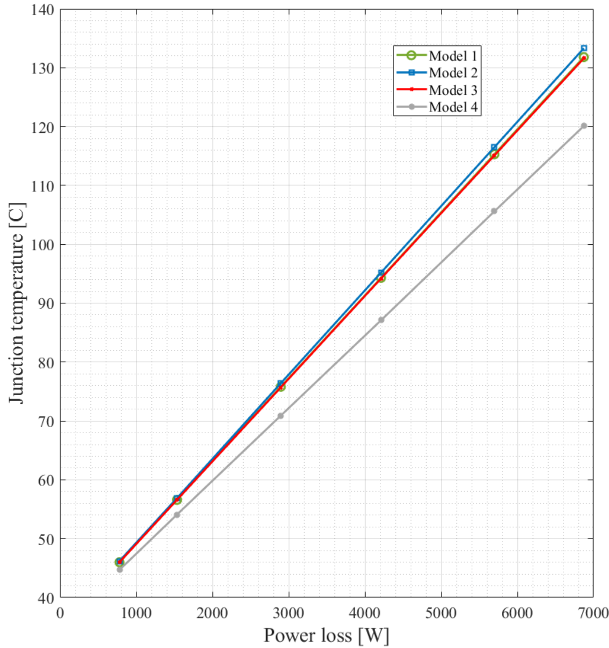

Fig. 6. Temperature distribution within an IGBT StakPak.

B. Transient analysis

A short-circuit in a DC line may cause severe damages in the equipment involved as it has been described above. Consequently, several constrains must be taken into account for the solid-state DC CB design. In this section, the impact of the current limiting inductor along with the threshold current that trips the breaker on the CB design is investigated and presented. Figures 7-8 show this impact in terms of peak fault current and power dissipation within the chip area of a single device. Keeping the inductance value of the current limiting inductor high, both the power dissipation within the chip area and the peak fault current are reduced. It must also be noted that the fault current reaches higher values than the threshold current because of the considered delays. Furthermore, the increase of the threshold current results in fault current rise and power dissipation rise as well.

The proper design of the current limiting inductor and the selection of the threshold current can then be determined, keeping in mind the limitations of the power electronic devices used. In particular, the IGBT considered in this study has $25kW$ maximum power dissipation and $4kA$ maximum collector current. Therefore, it can be concluded that the considered values as the base case of $150\mu H$ and $3kA$ for the inductance of the current limiting inductor and the threshold current respectively are within the acceptable range.

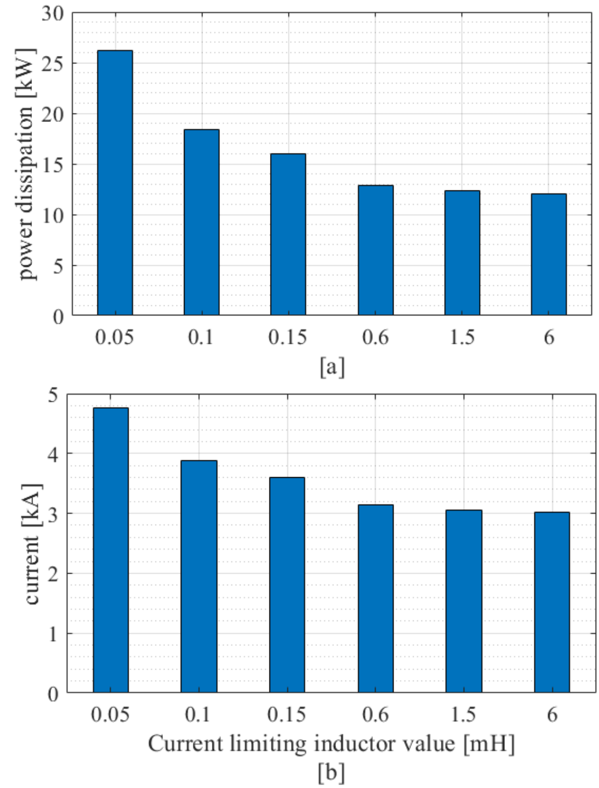

Fig. 7. Impact of the limiting current inductor on CB thermal stress with $T_A = 35^o$ and $R_{HS} = 10K/kW$. (a) power dissipation within chip area [kW] and (b) peak value of the fault current with respect to six different inductances.

VIII. Conclusion

MVDC power grids must tackle the protection challenges resulted from the inherent features of a DC system, i.e. lack of natural zero crossing point for the short-circuit current along with low line inductance values. On top of that, a solid-state DC CB seems to meet the requirements for fast capability of current interruption and hence, it could minimize the severe consequences of a high fault current. Therefore, the design of an efficient solid-state DC CB is very crucial. The high power losses associated with the power electronic devices used in a solid-state DC CB is currently the main showstopper for their realization. An electro-thermal analysis of power electronic devices must be therefore considered.

This paper presented an electro-thermal analysis of a solid-state DC CB. The impact of the heatsink design and the ambient temperature was investigated under steady-state. In particular, a 30% decrease of the equivalent thermal impedance of the considered heatsink resulted in a 10% efficiency increase. Similarly, a rise of 10° of ambient temperature led to a 2.5% efficiency decrease. Apart from that, four different thermal models for junction temperature and heat distribution within the power electronic device estimation were developed. The results indicated the superiority of the “RC” equivalent

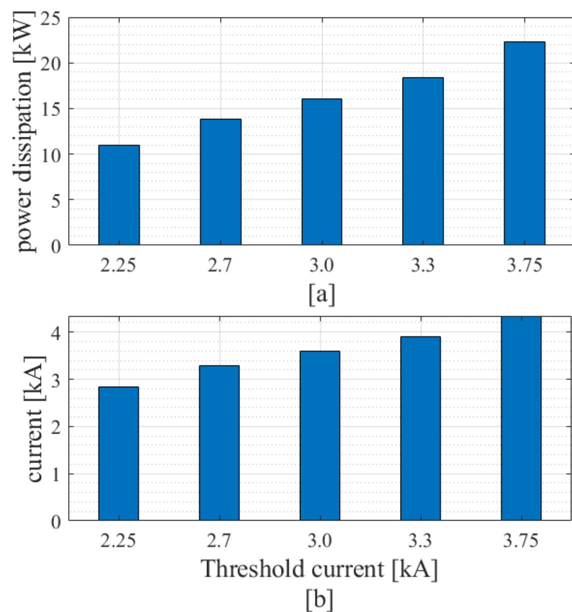

Fig. 8. Impact of the threshold current on CB thermal stress with $T_A = 35^o$ and $R_{HS} = 10K/kW$. (a) power dissipation within chip area [kW] and (b) peak value of the fault current with respect to 5 different threshold currents.

thermal network, since it minimizes the required time and simultaneously, it can achieve performance similar to the other time-consuming methods (i.e. FEM models). Finally yet importantly, the impact of both current limiting inductor and threshold current during the short-circuit condition (i.e. transient analysis) on the operation of the solid-state DC CB were examined and presented. The results indicated the importance of keeping the inductance value of the current limiting inductor high enough to prevent the power dissipation within the chip area of the IGBT to exceed its limitation. Similarly, the importance of the threshold current has been highlighted.

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