SCA3000 Product Specification

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General Information

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1 General Description

1.1 Introduction

SCA3000 is a three axis accelerometer family targeted for products requiring high performance with low power consumption. It consists of a 3D-MEMS sensing element and a signal conditioning ASIC packaged into a plastic Molded Interconnection Device package (MID).

Block diagram of the SCA3000 product family is presented in the Figure 1 below.

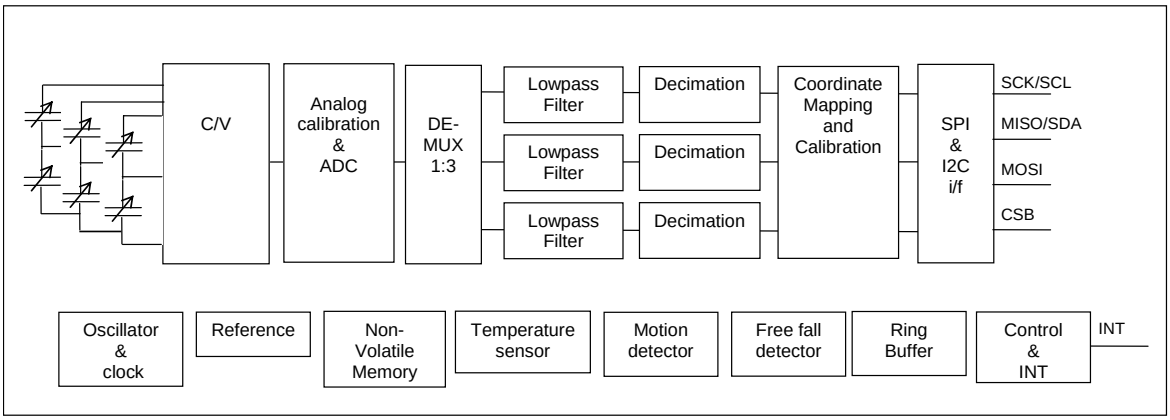

Figure 1 SCA3000 Block Diagram.

This document no. 8257300 describes the product specification (e.g. operation modes, user accessible registers, electrical properties and application information) for the SCA3000 family. The specification for an individual sensor is available in the corresponding datasheet.

1.2 Functional Description

1.2.1 Sensing element

Sensing element is manufactured using the proprietary bulk 3D-MEMS process enabling robust, stable and low noise & power capacitive sensors.

Sensing element consists of three acceleration sensitive masses. Acceleration will cause capacitance change that will be then converted into voltage change in the signal conditioning ASIC. Due to mechanical construction, element's measurement coordinates are rotated 45° compared to conventional orthogonal X,Y,Z coordinate system.

1.2.2 Interface IC

Sensing element is interfaced with a capacitance-to-voltage (CV) converter. Following the calibration in analog domain, the signal is converted with successive approximation type of analog-to-digital converter (ADC). ADC's signal is de-multiplexed into three signal processing channels, where it is low pass filtered and decimated. After that the signals will be mapped into orthogonal coordinates (X-Y-Z) and transferred to output registers. Depending on the product, SCA3000 sensor supports fully digital serial SPI or I^2C interface. In normal measurement mode acceleration data can be read via the serial bus. Other supported features are separate motion detection mode and parallel free fall detection. In these modes the sensor will generate an interrupt when a pre-defined condition has been met.

SCA3000 includes internal oscillator, reference and non-volatile memory that enable sensor's autonomous operation in system. Temperature sensor is used in some products to enhance the temperature stability. In that case temperature information can also be read out from the device.

1.2.3 Factory calibration

Sensors are factory calibrated and the trimmed parameters are gain, offset and the frequency of the internal oscillator. Calibration parameters will be read automatically from the internal non-volatile during the startup of the sensor.

1.2.4 Supported features

Features supported by individual SCA3000 product are listed in Table 1 below.

Table 1 SCA3000 devices summary

Features	SCA3000-D01	SCA3000-D02	SCA3000-E01	SCA3000-E02
Supply voltage	2.35 V – 2.7 V	2.35 V – 2.7 V	2.35 V – 2.7 V	2.35 V – 2.7 V
I/O voltage	1.7 V – 2.7 V	1.7 V – 2.7 V	1.7 V – 2.7 V	1.7 V – 2.7 V
Measuring range	±2 g	±2 g	±2 g	±2 g
Resolution	11 bits 2mg / 0.1°	11 bits 2mg / 0.1°	9 bits 8mg / 0.45°	9 bits 8mg / 0.45°
Output buffer	User enabled, 64 samples / axis	User enabled, 64 samples / axis	User enabled, 64 samples / axis	User enabled, 64 samples / axis
Motion detection	User enabled	User enabled	User enabled	User enabled
Free fall detection	User enabled	User enabled	User enabled	User enabled
Interface	SPI max 1.8 MHz	I^2C fast mode	SPI max 360 kHz	I^2C std mode
Temperature output	Yes	Yes	No	No
Clock	Internal	Internal	Internal	Internal

1.2.5 Operation modes

1.2.5.1 Measurement

SCA3000 is in normal measurement mode by default after start up. The sensor offers acceleration information via SPI or I^2C when master requires it. Master can acquire one axis acceleration or all three axis acceleration depending on the application. Measurement resolution depends on the product type (see Table 1).

1.2.5.2 Motion Detection

Motion Detection (MD) mode is intended to be used to save system level power consumption. In this mode SCA3000 activates interrupt via INT-pin when motion is detected. Sensitivity levels can be configured via SPI or I^2C bus for each axis. Moreover, detection condition can be defined using sensitivity directions with AND / OR / mux logic. Once the interrupt has happened, detected direction can be read out from the corresponding status register.

Normal acceleration information is not available in MD mode.

1.2.6 Free Fall Detection

Free Fall Detection (FFD) is intended to be used to save system resources. This feature activates interrupt via INT-pin when free fall is detected. Minimum detectable distance depends on the product.

Normal acceleration information is available when FFD is enabled.

1.2.7 Interrupt

SCA3000 has a dedicated output pin (INT) to be used as interrupt for master controller. Interrupt conditions can be activated and deactivated via SPI or I^2C bus. Once the interrupt has happened, interrupt source can be read out from the corresponding status register.

1.2.8 Temperature output

Some SCA3000 products provide 8-bit temperature information via the serial interface. See Table 1 for detailed product information.

1.2.9 Output ring buffer

In applications, where real time acceleration information is not needed, ring buffer memory can be used to buffer acceleration data. This will release µC resources to other tasks or e.g. to power saving mode while SCA3000 samples acceleration data into its buffer memory.

Acceleration data is sampled at a constant sample rate of the sensor. Buffer is FIFO type (First In First Out) where the oldest data is shifted out first. It has separate read and write address pointers, so it can be read and written simultaneously. If the buffer overflows the oldest data is lost and the new data replaces the oldest samples.

Ring buffer logic can be configured to give an interrupt when the buffer is ½ or ¾ full. The entire ring buffer content can be read by one read sequence.

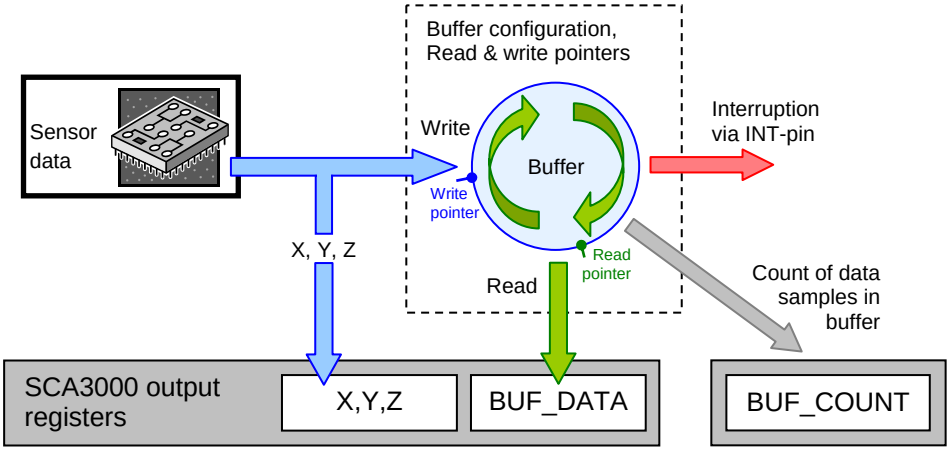

Figure 2 SCA3000 output ring buffer.

2 Reset and power up, Operation Modes, HW functions and Clock

2.1 Reset and power up

SCA3000 has an external active low reset pin. Power supplies must be within specified range before the reset can be released.

After releasing the reset, SCA3000 will read configuration and calibration data from the non-volatile memory to volatile registers. Then SCA3000 will make check sum calculation to the read memory content. STATUS register's CSME-bit="0" shows successful memory read operation.

2.2 Measurement Mode

2.2.1 Description

SCA3000 enters the measurement mode by default after power-on and CV-converter will start to feed data to the signal channel (Figure 1). Data will be reliable in the output registers after the product specific turn on time.

2.2.2 Usage

Acceleration data can be read from data output registers X_LSB, X_MSB, Y_LSB, Y_MSB, Z_LSB and Z_MSB. Each of these registers can be read one by one or using decrement register read, which is described in section 4.1.3.2 for SPI and 4.2.1.3 for I^2C interface. See section 3.3 for output register details.

2.3 Motion Detection Mode

2.3.1 Description

In MD mode ADC's data is not fed to the signal processing channel shown in Figure 1 but to MD block. It consists of a digital Band Pass Filter (BPF), threshold level programmable digital comparator and a configurable trigger function.

BPF's -3 dB high pass frequency is ***TBD*** Hz and -3 dB low pass frequency is ***TBD.*** See Figure 3 below.

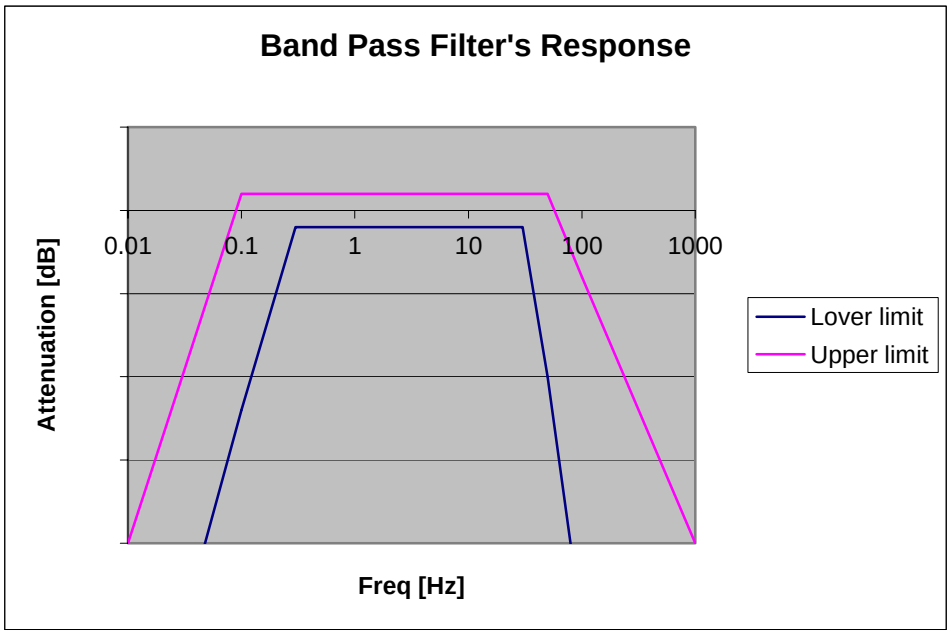

Figure 3 MD Band Pass Filter's frequency response

Programmable Threshold Level (TL) is *Lover Limit TBD*<TL<*Upper Limit TBD* g and it is divided into 256 values (8 bits) for each three channels (X,Y,Z). NOTE: Due to power consumption optimization, step size between each step may not be the same.

Triggering condition can be defined using OR/AND logic:
1. Any sensing direction can be configured to trigger the interrupt (OR condition).
2. Any sensing direction can be configured to be required to trigger the interrupt (AND condition).

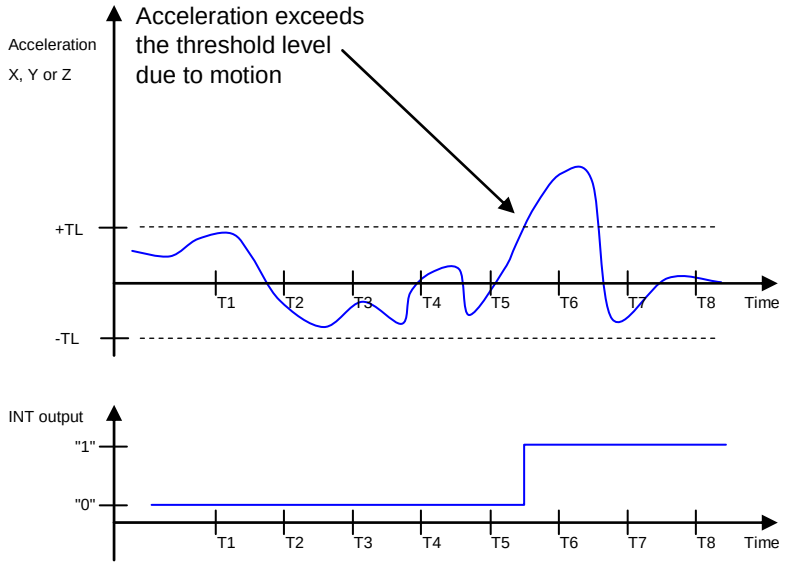

Figure 4 MD operation

2.3.2 Usage

MD mode can be enabled by setting MEAS bits in MODE register to "011". Trigger condition can be defined by setting REQ_Z, REQ_Y, REQ_X, EN_Z, EN_Y and EN_X bits in MD_CTRL register and Z_TH, Y_TH and Z_TH bits in MD_Z_TH, MD_Y_TH and MD_X_TH registers respectively. See section 3.4 for configuration register and section 2.7 for interrupt functionality details.

In MD mode acceleration data is not available in registers X_LSB, X_MSB, Y_LSB, Y_MSB, Z_LSB, Z_MSB and BUF_DATA.

2.3.3 Examples

A simple example of motion detection usage:
1. Write "00000011" (03h) into MODE register (enable motion detection mode, MODE = '011')
2. Acceleration data is not available when SCA3000 is in motion detection mode
3. INT-pin is activated when motion is detected, see section 2.7 for detailed INT-pin information.

In the next example the motion detector is configured to give an interrupt on motion only in X- OR Y-axis direction:
1. Write "00000011" (03h) into MODE register (enable motion detection mode, MODE = '011')
2. Write "00000000" (00h) into UNLOCK register
3. Write "01010000" (50h) into UNLOCK register
4. Write "10100000" (A0h) into UNLOCK register

(2.–4.) Unlock sequence for register lock

5. Write "00000010" (02h) into CTRL_SEL register (to select indirect MD_CTRL register)
6. Write "00000011" (03h) into CTRL_DATA register (this data is written into MD_CTRL register, enable trigger on Y-channel, EN_Y = '1', enable trigger on X-channel, EN_X = '1')
7. Acceleration data is not available when SCA3000 is in motion detection mode
8. INT-pin is activated when motion is detected in X- OR Y-axis direction (Z-axis direction is ignored), see section 2.7 for detailed INT-pin information.

2.4 Free Fall Detection

2.4.1 Description

During free fall in gravitation field all 3 orthogonal acceleration components are ideally equal to zero. Due to practical non-idealities, detection must be done using Threshold Level (TL) greater than 0.

When enabled Free Fall Detection (FFD) will monitor 8 MSB's of the measured acceleration in X, Y and Z directions. If the measured acceleration will stay within TL's longer than time TFF (Figure 5 below), which corresponds approx TBD cm drop distance, FFD will generate an interrupt to INT-pin.

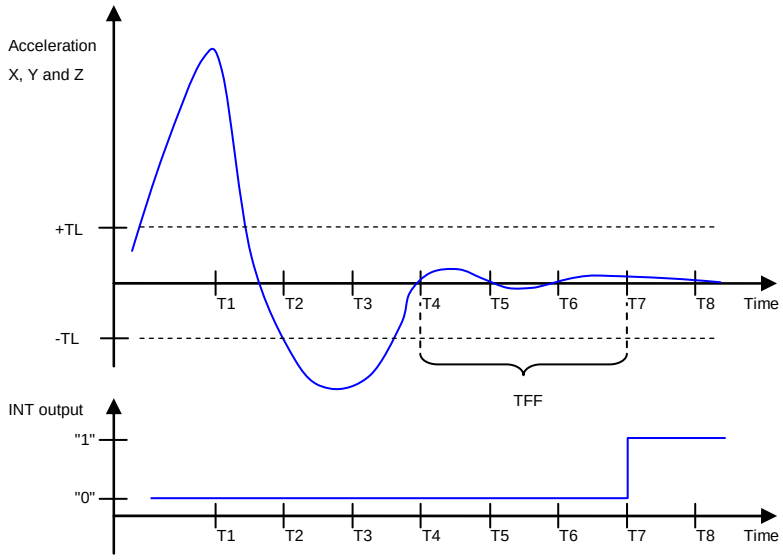

Figure 5 Free Fall condition

2.4.2 Usage

Free fall detection can be enabled by setting FFD_EN bit in MODE register to "1". See section 3.4 for MODE register details.

Acceleration data is available in registers X_LSB, X_MSB, Y_LSB, Y_MSB, Z_LSB, Z_MSB and BUF_DATA as in measurement mode. See section 3.3 for output register and section 2.7 for interrupt functionality details.

2.4.3 Example

A simple example of free fall detection usage:

1. Write "00010000" (10h) into MODE register (enable free fall detection, FDD_EN = '1')
2. Acceleration data can be read normally
3. INT-pin is activated when free fall is detected, see section 2.7 for detailed INT-pin information.

2.5 Ring Buffer

2.5.1 Description

SCA3000's Ring Buffer is 192 acceleration data samples long (64 samples of 11 bit three axis data) internal memory to relax the real time operation requirements of the host processor. The following parameters are configurable:

1. Each measurement axis can be individually disabled. If measurement data from e.g. Y-axis is not needed, available memory can be used for X- and Z-axis data.
2. Buffer data length can be changed from 11 to 8 bits. In 8-bit mode data can be read out using shorter read sequence.
3. Ring buffer's input sample rate can be the same as the sensor's data rate or divided by 2 or 4. When the divider is e.g. 2, only every 2nd acceleration data will be stored.
4. Interrupt condition, when enabled, can be selected between two: interrupt in INT-pin occurs when the buffer is 50% or 75% full.

2.5.2 Usage

Ring Buffer can be enabled by setting BUF_EN bit in MODE register to "1". After enabling the buffer, acceleration data can be read from BUF_DATA register using decrement register read, which is described in section 4.1.3.2 for SPI and 4.2.1.3 for I^2C interface.

Each measurement axis can be individually disabled by setting corresponding bits in BUF_X_EN, BUF_Y_EN and BUF_Z_EN in OUT_CTRL register to "0".

Output data length can be changed from 11 bits to 8 bits by setting bit BUF_8BIT in MODE register to "1". See section 3.3 for bit level descriptions.

The count of available data samples in output ring buffer can be read from BUF_COUNT register. Register value is updated only when it is accessed over the SPI or I^2C.

Data shift out order is X,Y,Z. In 11 bit mode two bytes must be read to get all 11 bits out. In that case MSB byte is 1st. Examples:

1. 11 bits data length, X&Y&Z axis enabled:
   X1_MSB, X1_LSB, Y1_MSB, Y1_LSB, Z1_MSB, Z1_LSB, X2_MSB, X2_LSB, ... latest Z_LSB
2. 11 bits data length, Y&Z axis enabled:
   Y1_MSB, Y1_LSB, Z1_MSB, Z1_LSB, Y2_MSB, Y2_LSB, Z2_MSB, Z2_LSB, Y3_MSB, Y3_LSB, ..., latest Z_LSB
3. 8 bits data length, all axis enabled:
   X1, Y1, Z1, X2, Y2, Z2,..., latest Z
4. 8 bits data length, X&Z axis enabled:
   X1, Z1, X2, Z2, X3, Z3, ..., latest Z
5. 8 bits data length, Z axis enabled:
   Z1, Z2, Z3, ... , latest Z

See section 2.7 for interrupt functionality details.

Acceleration data is available in X_LSB, X_MSB, Y_LSB, Y_MSB, Z_LSB and Z_MSB when the ring buffer is enabled.

2.5.3 Examples

A simple example of output ring buffer usage:

1. Write "10000000" (C0h) into MODE register (enable output ring buffer, BUF_EN = '1')
2. Acceleration data can be read normally
3. INT-pin is activated when buffer is ½ full, see section 2.7 for detailed INT-pin information.

In the next example the output Ring Buffer is configured to sample only the Z-axis acceleration data with 8 bit resolution and reduced data rate (only every second sample is stored into output ring buffer). In addition the SCA3000 is configured to give an interrupt when the output ring buffer is ¾ full:

1. Write "11000000" (C0h) into MODE register (enable output ring buffer, BUF_EN = '1', set data length to 8 bits, BUF_8BIT = '1')
2. Write "00000000" (00h) into UNLOCK register
3. Write "01010000" (50h) into UNLOCK register

} Unlock sequence for register lock

4. Write "10100000" (A0h) into UNLOCK register
5. Write "00001011" (0Bh) into CTRL_SEL register (to select indirect OUT_CTRL register)
6. Write "00000101" (03h) into CTRL_DATA register (this data is written into OUT_CTRL register, store Z-axis data, BUF_Z_EN = '1', divide data rate by 2, BUF_RATE = '01')
7. Write "10000001" (81h) into INT_MASK register (set buffer interrupt level to ¾ full, BUF_F_EN = '1', set INT-pin to active high, INT_ACT = '1')
8. Acceleration data can be read normally for all axis and with full resolution. The buffer data can be read from BUF_DATA register
9. INT-pin is activated when the output ring buffer is ¾ full of Z-axis acceleration data, see section 2.7 for detailed INT-pin information.

2.6 Temperature measurement

2.6.1 Usage

8 bit temperature information is available in TEMP register, if the feature is enabled in the product (see Table 1). It is updated with the latest temperature data when accessed. See section 3.3 for register details.

2.7 Interrupt function (INT-pin)

2.7.1 Usage

Motion Detector and Free Fall Detector will generate an interrupt to INT-pin when the corresponding function is enabled and the interrupt condition is met. SCA3000's ring buffer will generate an interrupt when interrupt functionality has been enabled. Setting BUF_F_EN bit in INT_MASK register "1" results in interrupt when the register is 75% full. Setting BUF_H_EN bit in INT_MASK register "1" results in interrupt when the register is 50% full.

Setting INT_ALL bit in INT_MASK register will mask all interrupts.

Interrupt polarity (active high/low) can be configured with INT_MASK register's INT_ACT bit.

Once the interrupt has happened, INT_STATUS register must be read to acknowledge the interrupt.

1. If at least one of MD bits in INT_STATUS register is "1", motion has been detected.
2. If FFD bit in INT_STATUS register is "1", free fall has been detected.
3. If BUF_FULL bit is "1", Ring Buffer is 75% full. Correspondingly, if BUF_HALF is "1", the Ring Buffer is 50% full.

See section 3.3 for INT_STATUS register details.

2.8 Clock

SCA3000 has an internal factory trimmed oscillator and clock generator. Internal frequencies vary product by product.

3 Addressing Space

SCA3000 register contents and bit definitions are described in more detail in next sections.

3.1 Register Description

SCA3000 addressing space is presented in Table 2 below.

Table 2 List of registers.

Add.	Name	Description	Mode (R, W, RW, IA)	Reg. type	Locked
00h	REVID	ASIC revision ID number	R	Conf	
01h		Reserved			-
02h	STATUS	Status	R	Conf	
03h		Reserved			-
04h	X_LSB	X-axis LSB frame	R	Output	
05h	X_MSB	X-axis MSB frame	R	Output	
06h	Y_LSB	Y-axis LSB frame	R	Output	
07h	Y_MSB	Y-axis MSB frame	R	Output	
08h	Z_LSB	Z-axis LSB frame	R	Output	
09h	Z_MSB	Z-axis MSB frame	R	Output	
0Ah ... 0Eh		Reserved			-
0Fh	BUF_DATA	Ring buffer output register	R	Output	
10h ... 12h		Reserved			-
13h	TEMP	Temperature	R	Output	
14h	MODE	Operating mode selection, control and configuration for: - mode selection - output buffer - free fall detection	RW	Conf	
15h	BUF_COUNT	Count of unread data samples in output buffer	R	Output	
16h	INT_STATUS	Interrupt status register: - output buffer is not full, ½ full or ¾ full - free fall detected / not detected - information of which axis triggered motion	R	Output	
17h	I2C_RD_SEL	Register address for I^2C read operation	RW	Conf	
18h	CTRL_SEL	Register address pointer for indirect control registers	RW	Conf	x
19h ... 1Dh		Reserved			-
1Eh	UNLOCK	Unlock register	RW	Conf	
1Fh ... 20h		Reserved			-
21h	INT_MASK	Interrupt mask register (register for possible interrupts): - interrupt when output buffer is ¾ full	RW, NV	Conf	

Add.	Name	Description	Mode (R, W, RW, IA)	Reg. type	Locked
		(enable / disable) - interrupt when output buffer is ½ full (enable / disable) - mask all interrupts on INT-pin (enable / disable) - INT-pin activity (INT active low / INT active high)			
22h	CTRL_DATA	Data to/from register which address is in CTRL_SEL (18h) register	RW, NV, IA	Conf	x
23h ... 3Fh		Reserved			-

Add. is the register address in hex format.
RW – Read / Write register, R – Read-only register, NV – Register mirrors NV-memory data (NV = non-volatile).
IA – indirect addressing used.
Registers whose read and write access is blocked by register lock is marked in "Locked" column.

3.2 Non-volatile memory

SCA3000 has internal non-volatile memory for calibration and configuration data. Memory content will be programmed during production and is not user configurable. Initial configuration values can be found in the following section 3.4.

3.3 Output Registers

SCA3000 output register (marked with 'Output' in Table 2) contents and bit definitions are described in this section. Output registers contain information of measured acceleration and temperature as well as information of the operating state and interrupts of SCA3000.

Address: **04h**
Register name: **X_LSB**, X-axis LSB frame

Bits	Mode	Initial Value	Name	Description
7:0	R	00h	DATA	X-axis LSB frame

Address: **05h**
Register name: **X_MSB**, X-axis MSB frame

Bits	Mode	Initial Value	Name	Description
7:0	R	00h	DATA	X-axis MSB frame

Address: **06h**
Register name: **Y_LSB**, Y-axis LSB frame

Bits	Mode	Initial Value	Name	Description
7:0	R	00h	DATA	Y-axis LSB frame

Address: **07h**
Register name: **Y_MSB**, Y-axis MSB frame

Bits	Mode	Initial Value	Name	Description
7:0	R	00h	DATA	Y-axis MSB frame

Address: **08h**
Register name: **Z_LSB**, Z-axis LSB frame

Bits	Mode	Initial Value	Name	Description
7:0	R	00h	DATA	Z-axis LSB frame

Address: **09h**
Register name: **Z_MSB**, Z-axis MSB frame

Bits	Mode	Initial Value	Name	Description
7:0	R	00h	DATA	Z-axis MSB frame

The bit level description of acceleration data from X_LSB ... Z_MSB registers is presented in Table 3. The acceleration data is presented in 2's complement format. At 0 g acceleration the output is ideally 00h.

Table 3. Bit level description for X_LSB ... Z_MSB.

Byte	MSB byte								LSB byte					
Bit number	B7	B6	B5	B4	B3	B2	B1	B0	B7	B6	B5	B4	B3	B2:B0
Acceleration [mg]	Sign	2048	1024	512	256	128	64	32	16	8	4	2	1	
SCA3000-D0x resolution 11 bits + ov 2 mg	S	ov	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0	n	xxx
SCA3000-E0x resolution 9 bits + ov 8 mg	S	ov	d7	d6	d5	d4	d3	d2	d1	d0	n	n	n	xxx

s = sign bit
ov = data overflow bit
n = noise bit (can be used in averaging to improve resolution)
x = not used bit

Address: **0Fh**
Register name: **BUF_DATA**, ring buffer output register

Bits	Mode	Initial Value	Name	Description
7:0	R	00h	DATA	Ring buffer output register

The bit level description of output ring buffer acceleration data from BUF_DATA register is presented in Table 4. The acceleration data is presented in 2's complement format. At 0 g acceleration the output is ideally 00h.

Table 4. Bit level description for BUF_DATA.

Byte	MSB byte								LSB byte			
Bit number	B7	B6	B5	B4	B3	B2	B1	B0	B7	B6	B5	B4:B0
Acceleration [mg]	sign	2048	1024	512	256	128	64	32	16	8	4	
SCA3000-D0x ring buffer in 11 bit mode resolution 4 mg	s	ov	d8	d7	d6	d5	d4	d3	d2	d1	d0	-
SCA3000-D0x ring buffer in 8 bit mode resolution 32 mg	s	ov	d5	d4	d3	d2	d1	d0	-	-	-	-
SCA3000-E0x ring buffer in 11 bit mode resolution 8 mg	s	ov	d7	d6	d5	d4	d3	d2	d1	d0	n	-
SCA3000-E0x ring buffer in 8 bit mode resolution 32 mg	s	ov	d5	d4	d3	d2	d1	d0	-	-	-	-

s = sign bit
ov = data overflow bit
n = noise bit (can be used in averaging to improve resolution)
x = not used bit

Address: **13h**
Register name: **TEMP**, temperature register

Bits	Mode	Initial Value	Name	Description
7:0	R	00h	TEMP	Temperature register

The bit level description of temperature data from TEMP register is presented in Table 5.

Table 5. Bit level description for TEMP.

Bit number Temperature [°C]	B7	B6	B5	B4	B3	B2	B1	B0
SCA3000-D0x								

Address: **15h**
Register name: **BUF_COUNT**, output ring buffer status

Bits	Mode	Initial Value	Name	Description
7:0	R	00h	COUNT	Count of available data samples in output ring buffer.

Address: **16h**
Register name: **INT_STATUS**, interrupt status register

Bits	Mode	Initial Value	Name	Description
7	R	0	BUF_FULL	Output ring buffer is ¾ full 1 – Ring buffer is ¾ full 0 – Ring buffer is not full
6	R	0	BUF_HALF	Output ring buffer is ½ full 1 – Ring buffer is ½ full 0 – Ring buffer is not full
5:4				Reserved
3	R	0	FFD	Free fall detection 1 – Free fall detected (0 g acceleration) 0 – Free fall not detected
2:0	R	000	MD	Motion detector triggered channel indication 1xx – Trigger on Y-axis x1x – Trigger on X-axis xx1 – Trigger on Z-axis

3.4 Configuration Registers

SCA3000 configuration register (marked with 'Conf' in Table 2) contents and bit definitions are described in this section. Configuration registers are used to configure SCA3000 operation and the operation parameters.

Address: **00h**
Register name: **REVID**, ASIC revision ID number tied in metal

Bits	Mode	Initial Value	Name	Description
7:4	R		REVMAJ	Major revision number
3:0	R		REVMIN	Minor revision number

Address: **02h**
Register name: **STATUS**, status register

Bits	Mode	Initial Value	Name	Description
7:6				Reserved

5	R	0	LOCK	Status of lock register 0 – Lock is closed 1 – Lock is open
4:2				Reserved
1	R	0	CSME	EEPROM checksum error 1 – EEPROM checksum error 0 – No error
0	R	0	SPI_FRAME	SPI frame error. Bit is reset, when next correct SPI frame is received. 1 – SPI frame error 0 – No error

Address: **14h**
Register name: **MODE**, operation mode selection

Bits	Mode	Initial Value	Name	Description
7	RW	0	BUF_EN	Output ring buffer 1 – Enabled 0 – Disabled (Buffer in power down)
6	RW	0	BUF_8BIT	Output ring buffer data length 1 – Ring buffer is read in single 8 bit frame per stored axis (8 bit mode) 0 – Ring buffer is read in two 8 bit frames per stored axis (9-11 bit mode). Unused bits are set to 0.
5				Reserved
4	RW	0	FFD_EN	Free fall detection 1 – Enabled 0 – Disabled (detection in power down)
3				Reserved
2:0	RW	000	MODE	Selects SCA3000 series operation mode 000 – Normal measurement mode 011 – MD, Motion Detector Other combinations are reserved

Address: **17h**
Register name: **I2C_RD_SEL**, register address for I^2C read operation

Bits	Mode	Initial Value	Name	Description
7:0	W	00h	ADDR	Address of register to be read via I^2C. Register is used only for I^2C read access.

Address: **18h**
Register name: **CTRL_SEL**, Control register selector, **UNLOCK REQUIRED**

Bits	Mode	Initial Value	Name	Description
7:5	RW	000		Reserved
4:0	RW	00000	SELECT	Indirect control registers, select register address for read / write access 00010 – MD_CTRL (Motion Detector control) 00011 – MD_Y_TH (Motion Detector Y-threshold) 00100 – MD_X_TH (Motion Detector X-threshold) 00101 – MD_Z_TH (Motion Detector Z-threshold)

				01011 – OUT_CTRL (Output control) Other combinations are reserved

CTRL_SEL register works as an address pointer for registers listed below. When this register is written the content of selected register is available for reading/writing from/to register CTRL_DATA.

Address value: **00010**
Register name: **MD_CTRL**, Motion Detector control (Indirect access via CTRL_SEL)

Bits	Initial Value	Name	Description	Note
7:6			Reserved	
5	0	REQ_Z	1 – Require trigger on Z-channel 0 – Not required	Bits 5:3 can be used to build logical AND operation between channels. Example: X and Y = Require X and Y → 00 011 111
4	0	REQ_X	1 – Require trigger on X-channel 0 – Not required	
3	0	REQ_Y	1 – Require trigger on Y-channel 0 – Not required	
2	1	EN_Z	1 – Enable trigger on Z-channel 0 – Not required	Bits 2:0 can be used to build logical OR operation between channels. Example: X or Y = Disable Z → 00 000 011
1	1	EN_X	1 – Enable trigger on X-channel 0 – Not required	
0	1	EN_Y	1 – Enable trigger on Y-channel 0 – Not required	

Address value: **00011**
Register name: **MD_Y_TH**, Motion Detector Y-threshold (Indirect access via CTRL_SEL)

Bits	Initial Value	Name	Description
7:0	10h	Y_TH	Threshold for Y-acceleration change when MD is used.

Address value: **00100**
Register name: **MD_X_TH**, Motion Detector X-threshold (Indirect access via CTRL_SEL)

Bits	Initial Value	Name	Description
7:0	10h	X_TH	Threshold for X-acceleration change when MD is used.

Address value: **00101**
Register name: **MD_Z_TH**, Motion Detector Z-threshold (Indirect access via CTRL_SEL)

Bits	Initial Value	Name	Description
7:0	10h	Z_TH	Threshold for Z-acceleration change when MD is used.

Address value: **01011**
Register name: **OUT_CTRL**, Output configuration (Indirect access via CTRL_SEL)

Bits	Initial Value	Name	Description
7:5			Reserved
4	1	BUF_X_EN	Store X-axis acceleration data to ring buffer 1 – enabled 0 – disabled
3	1	BUF_Y_EN	Store Y-axis acceleration data to ring buffer 1 – enabled 0 – disabled
2	1	BUF_Z_EN	Store Z-axis acceleration data to ring buffer 1 – enabled 0 – disabled
1:0	00	BUF_RATE	Additional data rate reduction after calibration before data is loaded to ring buffer (no effect on output registers data rate) 11 – No rate reduction

			10 – divide rate by 4 01 – divide rate by 2 00 – No rate reduction

Address: **1Eh**
Register name: **UNLOCK**, Unlock register lock

Bits	Mode	Initial Value	Name	Description
7:0	RW	00h	KEY	Lock can be opened by writing the following sequence into this register: 00h, 50h, A0h Writing any other sequence closes the lock. Lock state can be read from STATUS register.

Address: **21h**
Register name: **INT_MASK**, interrupt mask register

Bits	Mode	Initial Value	Name	Description
7	RW	0	BUF_F_EN	Interrupt when output ring buffer is ¾ full 1 – Enabled 0 – Disabled
6	RW	1	BUF_H_EN	Interrupt when output ring buffer is ½ full 1 – Enabled 0 – Disabled
5:2				Reserved
1	RW	0	INT_ALL	Mask all interrupts (only effects on the INT-pin) 1 – Mask all interrupts (including free fall detection and motion detector) 0 – Mask interrupts according to configured mode
0	RW	1	INT_ACT	INT-pin signal activity 1 – INT active high (INT-pin high) 0 – INT active low (INT-pin low)

Address: **22h**
Register name: **CTRL_DATA**, Control register data, **UNLOCK REQUIRED**

Bits	Mode	Initial Value	Name	Description
7:0	RW	00h	DATA	Data bits [7:0] of selected 8-bit control register. Write this register to actually perform the write operation to selected location. See register CTRL_SEL for information on register contents.

4 Serial Interfaces

Communication between SCA3000 sensor and master controller is based on serial data transfer and dedicated interrupt line (INT-pin). Two different serial interfaces are available for SCA3000 sensor: SPI and I^2C (Phillips specification V2.1). However, only one per product is enabled by pre-programming in the factory. SCA3000 acts as a slave on both SPI and I^2C bus.

4.1 SPI Interface

SPI bus is full duplex synchronous 4-wire serial interface. It consists of one master device and one or more slave devices. The master is defined as a micro controller providing the SPI clock, and the slave as any integrated circuit receiving the SPI clock from the master. The SCA3000 sensor always operates as a slave device in master-slave operation mode. A typical SPI connection is presented in Figure 6.

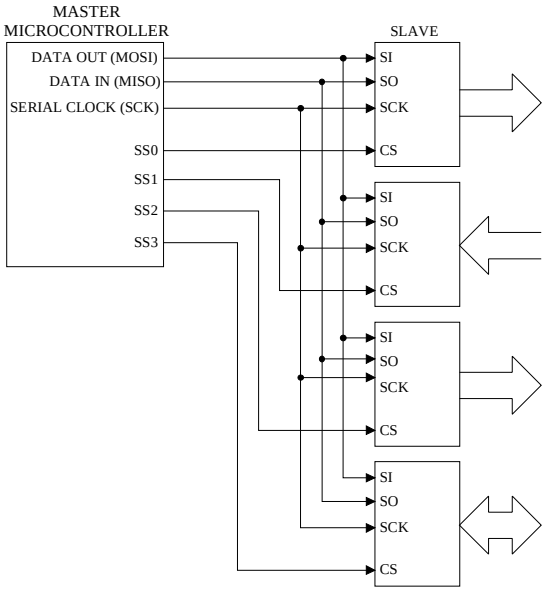

Figure 6 Typical SPI connection.

The data transfer uses the following 4-wire interface:

MOSI	master out slave in	µC → SCA3000
MISO	master in slave out	SCA3000 → µC
SCK	serial clock	µC → SCA3000
CSB	chip select (low active)	µC → SCA3000

4.1.1 SPI frame format

SCA3000 SPI frame format and transfer protocol is presented in Figure 7.

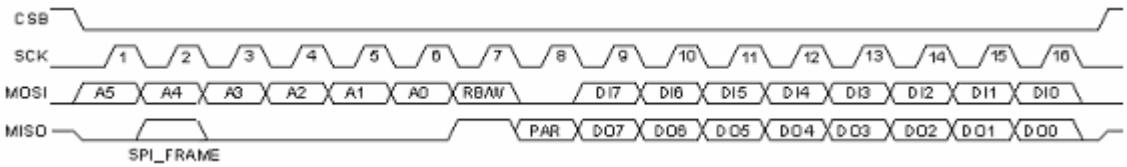

Figure 7 SPI frame format.

Each communication frame contains 16 bits. The first 8 bits in MOSI line contains info about the operation (read/write) and the register address being accessed. The first 6 bits define 6 bit address for selected operation, which is defined by bit 7 ('0' = read '1' = write), which is followed by one zero bit. The later 8 bits in MOSI line contain data for a write operation and are don't-care for a read operation.

The first bits in MISO line are frame error bit (SPI_FRAME) of previous SPI frame and odd parity bit (PAR). Parity is calculated from data which is currently sent. Bit 7 is always '1'. The later 8 bits contain data for a read operation. During the write operation, these data bits are previous data bits of addressed register.

For write commands, data is written into the addressed register on the rising edge of CSB. If the command frame is invalid as described in the section data will not be written into the register (please see "error conditioning" in section 4.1.2).

For read commands, data is latched into the internal SPI output register (shift register) on the 8th rising edge of SCK. The output register is shifted out MSB first over MISO output.

When CSB is high state between data transfers, MISO line is in high-impedance state.

4.1.2 SPI bus error conditioning

While sending a SPI frame, if CSB is raised to 1

- before sending 16 SCKs or
- the number of SCK pulses is not divisible by 8,

the frame error is activated and the frame is considered invalid. Status bit STATUS.SPI_FRAME is set to indicate the frame error condition. During next SPI frame error bit is sent out as SPI_FRAME bit (see SPI_FRAME in MISO line in Figure 7). STATUS.SPI_FRAME bit is reset, if correct frame is received.

When an invalid frame is received, the last command is simply ignored and the register contents are left unchanged. If frame error happens while sending multiple samples in ring buffer mode, only the last output value is considered invalid.

4.1.3 Examples of SPI communication

4.1.3.1 Example of register read

An example of 11 bit X-axis acceleration read command is presented in Figure 8. Master gives the register address to be read via MOSI line: '05' in hex format and '000101' in binary format, register name is X_MSB (X-axis MSB frame). 7th bit is set to '0' to indicate the read operation.

The sensor replies to asked operation by transferring the register content via MISO line. After transferring the asked X_MSB register content, master gives next register address to be read: '04' in hex format and '000101' in binary format, register name is X_LSB (X-axis LSB frame). The sensor replies to asked operation by transferring the register content MSB first.

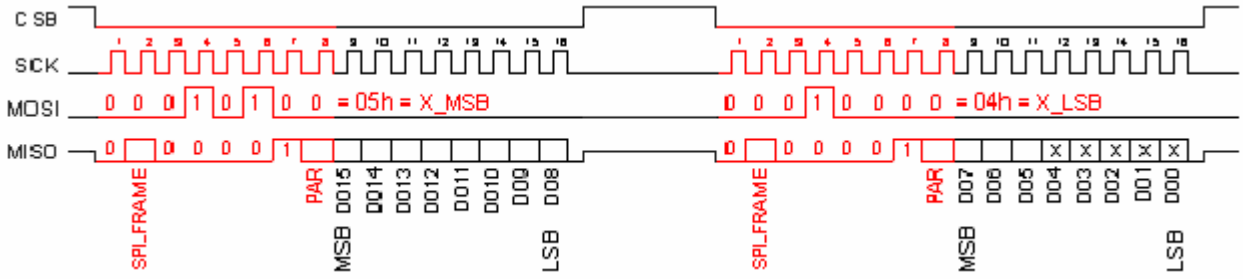

Figure 8 An example of SPI read communication.

4.1.3.2 Example of decremented register read

In Figure 9 is presented a decremented read operation where the content of four output registers is read by one SPI frame. After normal register addressing and one register content reading the µC keeps CSB line low and continues supplying the SCK pulses. After every 8 SCK pulses the output

data address is decremented by one and the previous DOUT register's content is shifted out without parity bits. Parity bit in figure 4 is calculated and transferred only for the first data frame. From X_LSB register address the SCA3000 jumps to Z_MSB. Decremented reading is possible only for registers X_LSB ... Z_MSB.

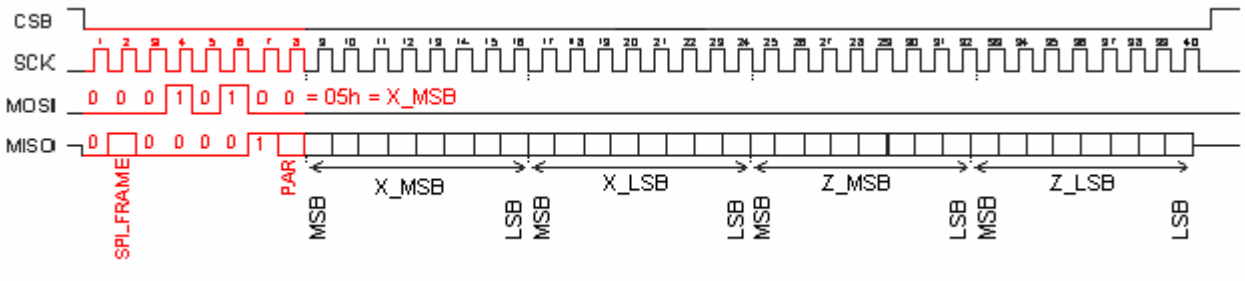

Figure 9 An example of decremented read operation.

4.1.3.3 Example of ring buffer read

An example of output ring buffer read by one SPI frame is presented in Figure 10. The whole ring buffer read procedure is very similar to decremented read described above. The output ring buffer is addressed (register name BUF_DATA). The SCA3000 sensor continues shifting out the ring buffer content as long as µC continues supplying the SCK pulses.

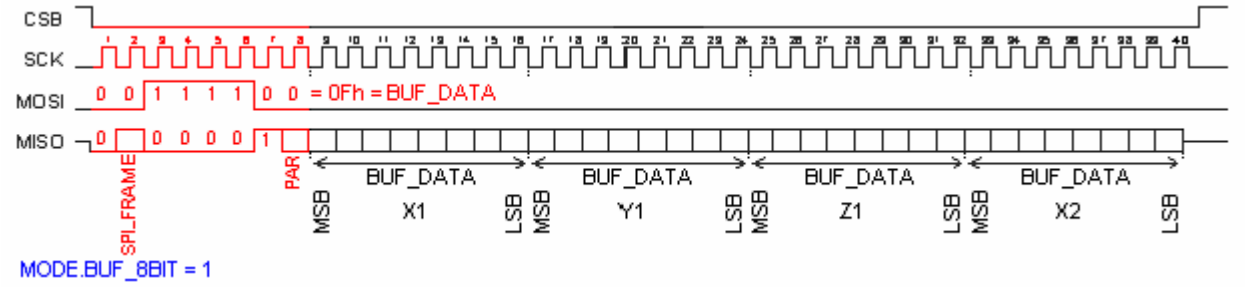

Figure 10 An example of output ring buffer read operation.

4.2 I²C Interface

I²C is a 2-wire serial interface. It consists of one master device and one or more slave devices. The master is defined as a micro controller providing the serial clock (SCL), and the slave as any integrated circuit receiving the SCL clock from the master. The SCA3000 sensor always operates as a slave device in master-slave operation mode. When in SPI interface a hardware addressing is used (slaves have dedicated CSB signals), the I²C interface uses a software based addressing (slave devices have dedicated bit patterns as addresses).

SCA3000 is compatible to the Philips I²C specification V2.1. Main used features of the I²C interface are:

- 10-bit addressing
- Supports standard mode and fast mode.
- Start / Restart / Stop
- Slave transceiver mode
- Designed for low power consumption

In addition to the Philips specification, the SCA3000 I²C interface supports multiple write and read mode.

4.2.1 I²C frame format

4.2.1.1 I²C write mode

In I²C write mode the first 8 data bits after device address define the SCA3000 internal register address to be written. If multiple data words are transferred by the master, the register address is being decremented automatically by one (see cases 1 and 2 in Figure 11).

4.2.1.2 I²C read mode

Read mode operates as described in Philips I²C specification. I²C read operation returns the content of the register which address is defined in I2C_RD_SEL register. So when performing the I²C read operation, the register address to be read has to be written into I2C_RD_SEL register before actual read operation. Read operation starts from register address that has been written earlier in I2C_RD_SEL register. Read data is acknowledged by I²C master. Automatic read address change depends on the selected start address (see cases 3 and 4 in Figure 11).

- If address is some of registers between X_LSB → Z_MSB the register address is automatically cycled as follows:
  ... →Y_MSB → Y_LSB → X_MSB → X_LSB → Z_MSB → Z_LSB → Y_MSB → Y_LSB → ...
- If the start address is any other register, the read address is NOT automatically incremented or decremented (the data transfer continues from the same address.) This enables the burst read from output ring buffer (register BUF_DATA).

4.2.1.3 Decremented register read

Decremented reading is possible only for registers X_LSB ... Z_MSB. Refer to decremented read with SPI interface section 4.1.3.2.

4.2.2 Examples of I²C communication

Examples of I²C communication are presented below in Figure 11.

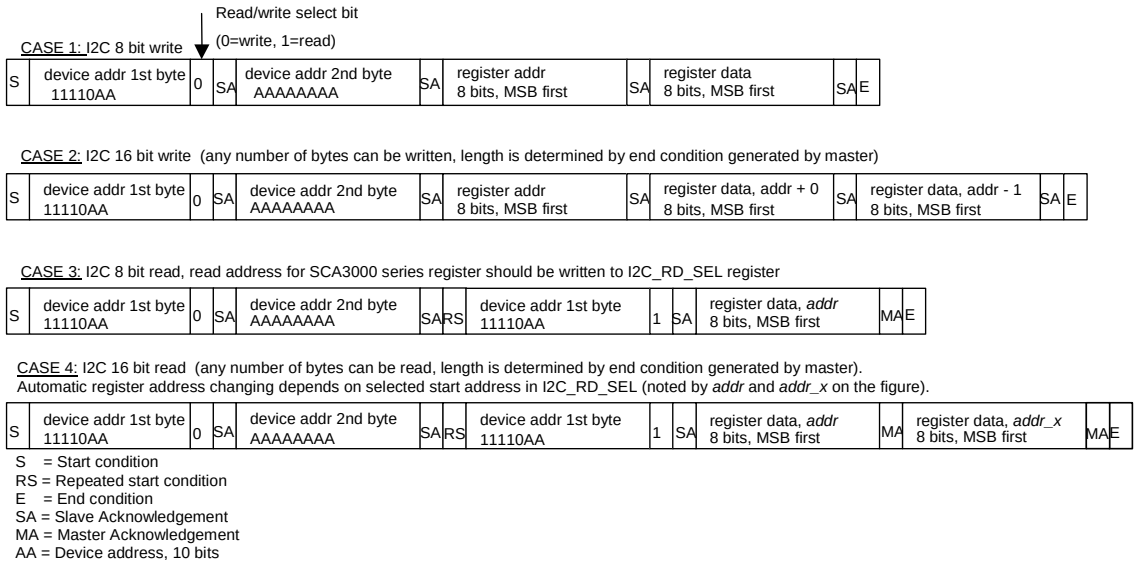

Figure 11 I²C frame format.

5 Electrical Characteristics

All voltages are reference to ground. Currents flowing into the circuit have positive values.

5.1 Absolute maximum ratings

The absolute maximum ratings of SCA3000 are presented in Table 6 below.

Table 6. Absolute maximum ratings of SCA3000

Parameter	Value	Unit
Supply voltage (V_{dd})	-0.3 to +3.6	V
Voltage at input / output pins	-0.3 to (V_{dd} + 0.3)	V
ESD (Human body model)	±2	kV
Storage temperature	-40 ... +125	°C
Storage / operating temperature	-40 ... +85	°C
Mechanical shock	> 10 000	G

5.2 Power Supply

Please refer to corresponding product specification.

5.3 Digital I/O Specification

5.3.1 Digital I/O DC characteristics

Table 7. DC characteristics of digital I/O pins.

No.	Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Input: CSB, MOSI, Xreset, SCK_SCL has no pull up / pull down							
1	Pull up current: CSB	V_{IN} = 0 V	I_{PU}	10		50	µA
2	Pull down current: MOSI	V_{IN} = Dvio	I_{PD}	10		50	µA
3	Pull up current Xreset	V_{IN} = 0 V	I_{PU}	3		10	µA
4	Input high voltage		V_{IH}	0.7*Dvio			V
5	Input low voltage		V_{IL}			0.3*Dvio	V
6	Hysteresis		V_{HYST}	0.1*Dvio			V
Output terminal: MISO_SDA, INT							
7	Output high voltage	I > -4 mA	V_{OH}	0.8*Dvio		Dvio	V
8	Output low voltage	I < 4 mA	V_{OL}	0		0.2*Dvio	V
9	Tristate leakage	0 < V_{MISO} < 2.7 V	I_{LEAK}	-2		2	µA

5.3.2 Digital I/O level shifter

All SCA3000 products have internal level shifter that can be used to interface e.g. microcontroller using lower supply than SCA3000. Level shifter is "programmed" by providing the supply voltage of the interfaced device to the DVIO-pin. Please refer to corresponding product specification for details.

5.3.3 SPI AC characteristics

The AC characteristics of SCA3000 SPI interface are defined in Figure 12 and in Table 8.

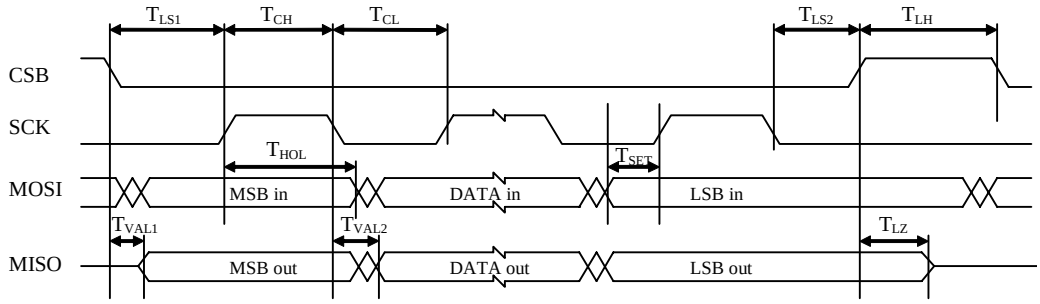

Figure 12 Timing diagram of SPI communication.

Table 8. AC characteristics of SPI communication.

	Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Terminal CSB, SCK							
1	Time from CSB (10%) to SCK (90%)[1]		T_{LS1}	$T_{per}/2$			Ns
2	Time from SCK (10%) to CSB (90%)[1]		T_{LS2}	$T_{per}/2$			Ns
Terminal SCK							
3	SCK low time	Load capacitance at MISO < 35 pF	T_{CL}	0.80* $T_{per}/2$	$T_{per}/2$		Ns
4	SCK high time	Load capacitance at MISO < 35 pF	T_{CH}	0.80* $T_{per}/2$	$T_{per}/2$		Ns
5	SCK Frequency		fsck = $1/T_{per}$			Product specific	MHz
Terminal MOSI, SCK							
6	Time from changing MOSI (10%, 90%) to SCK (90%)[1]. Data setup time		T_{SET}	$T_{per}/4$			Ns
7	Time from SCK (90%) to changing MOSI (10%, 90%)[1]. Data hold time		T_{HOL}	$T_{per}/4$			Ns
Terminal MISO, CSB							
8	Time from CSB (10%) to stable MISO (10%, 90%)	Load capacitance at MISO < 35 pF	T_{VAL1}			$T_{per}/4$	Ns
9	Time from CSB (90%) to high impedance state of MISO[1].	Load capacitance at MISO < 35 pF	T_{LZ}			$T_{per}/4$	Ns
Terminal MISO, SCK							
10	Time from SCK (10%) to stable MISO (10%, 90%)[1].	Load capacitance at MISO < 35 pF	T_{VAL2}			1.3* $T_{per}/4$	Ns
Terminal MOSI, CSB							
11	Time between SPI cycles, CSB at high level (90%)		T_{LH}	$4xT_{per}$			Ns

5.3.4 I^2C AC characteristics

Please, see Phillips Semiconductors, The I2C bus specification, Version 2.1, January 2000, pp. 31-33.

6 Package Characteristics

6.1 Dimensions

The package dimensions are presented in Figure 13 below (dimensions in millimeters, [mm]).

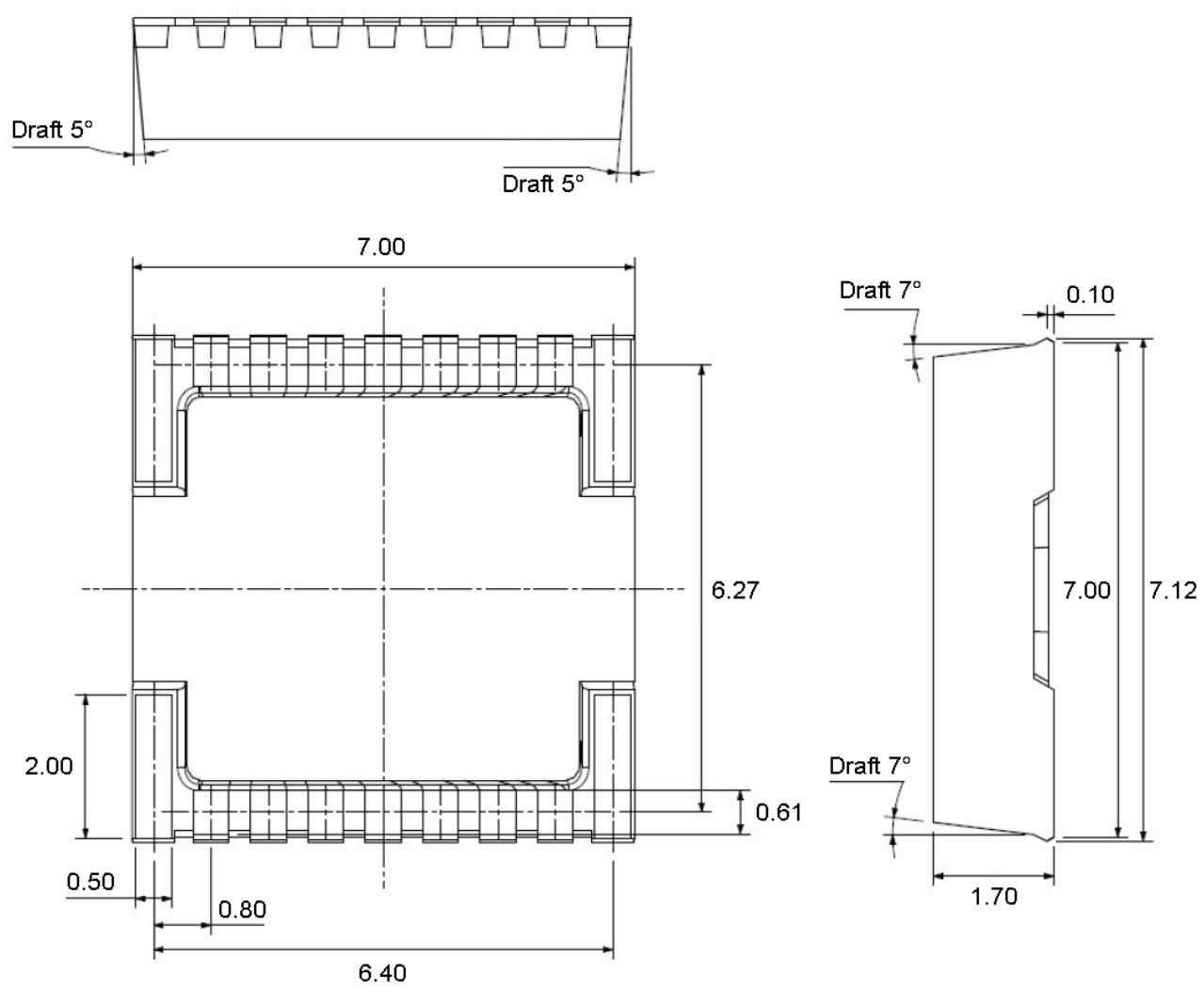

Figure 13 SCA3000 package dimensions.

6.2 Reflow

Recommended reflow profile for SCA3000.

7 Application information

7.1 Pin Description

SCA3000 pin numbers are presented in Figure 15 below and pin descriptions in Table 9.

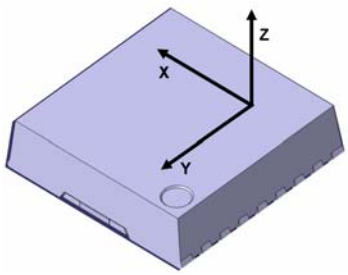

Figure 14 Sensing directions

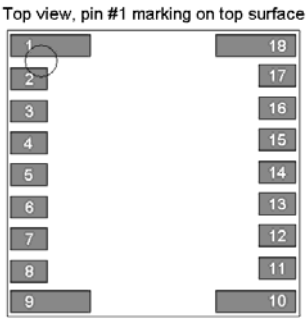

Figure 15 SCA3000 pin numbers.

Table 9. SCA3000 pin description.

Pin #	Name	SCA3000-D01 SCA3000-E01	SCA3000-D02 SCA3000-E02
1	NC	Not connected	Not connected
2	XRESET	External reset, active low	External reset, active low
3	INT	Interrupt output	Interrupt output
4	CLK	Not connected	Not connected
5	DVSS	Digital ground	Digital ground
6	DVDD	Digital supply	Digital supply
7	DVIO	Digital I/O supply	Digital I/O supply
8	CSB	Chip select	Not connected
9	NC	Not connected	Not connected
10	NC	Not connected	Not connected
11	SCK_SCL	SPI serial clock (SCK)	I^2C serial clock (SCL)
12	MISO_SDA	SPI data out (MISO)	I^2C data in / out (SDA)
13	MOSI	SPI data in (MOSI)	Not connected
14	AVDD	Analog supply	Analog supply
15	AVSS	Analog ground	Analog ground
16	AVSS	Analog ground	Analog ground
17	ATSTIO	Not connected	Not connected
18	NC	Not connected	Not connected

7.2 Recommended circuit diagram

1. Connect 100 nF SMD capacitor between each supply voltage and ground level.
2. Connect 1 µF capacitor between each supply voltage and ground level.
3. Use one regulator for analog and digital supply (AVDD and DVDD).
4. Use separate regulator for digital IO supply (DVIO).
5. Xreset is needed always in start up: when Xreset is low, raise power supplies inside specification, then set Xreset high.
6. INT-pin is used with output buffer as well as in Free Fall and Motion Detection mode.
7. Serial interface (SPI or I^2C) logical '1' level is determined by DVIO supply voltage level.

Recommended circuit diagram for SCA3000 with SPI interface is presented in Figure 16 below.

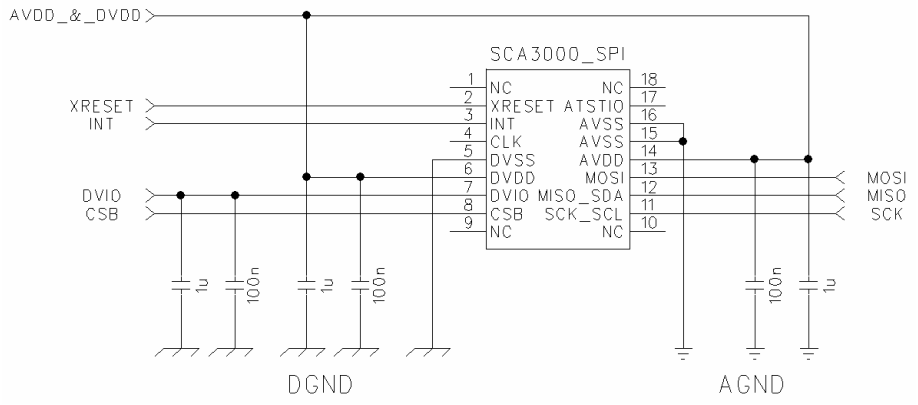

Figure 16 Recommended circuit diagram for SCA3000 with SPI interface.

Recommended circuit diagram for SCA3000 with I^2C interface is presented in Figure 17 below.

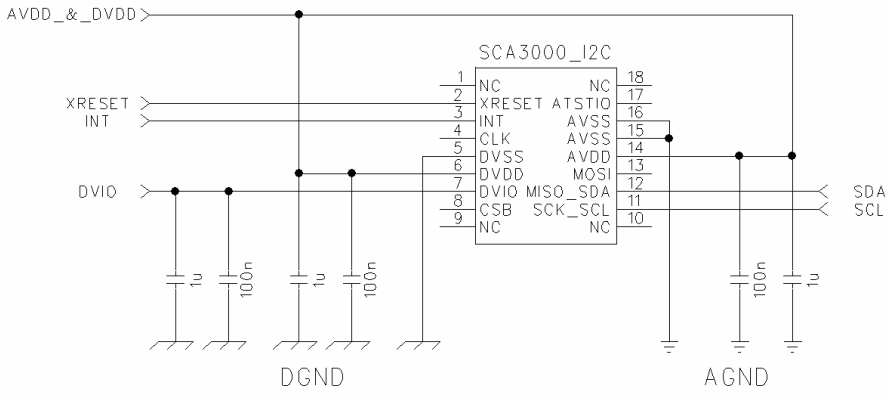

Figure 17 Recommended circuit diagram for SCA3000 with I^2C interface.

7.3 Recommended PWB layout

General PWB layout recommendations for SCA3000 products (refer to Figure 16, Figure 17 and Figure 18):

1. Locate 100 nF SMD capacitors right next to SCA3000 package.
2. 1 µF capacitors can be located near the node where AVDD and DVDD are routed on separate ways.
3. Use separate ground planes for AGND and DGND. Connect separate ground planes together on PWB.
4. Use double sided PWB, connect the bottom side plane to DGND.

Recommended PWB pad layout for SCA3000 is presented in Figure 18 below (dimensions in millimeters, [mm]).

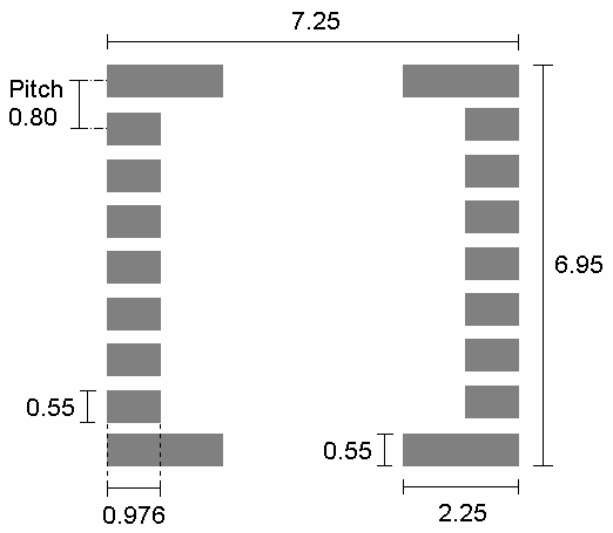

Figure 18 Recommended PWB pad layout for SCA3000.

Recommended PWB layout for SCA3000 with SPI interface is presented in Figure 19 below (circuit diagram presented in Figure 16 above).

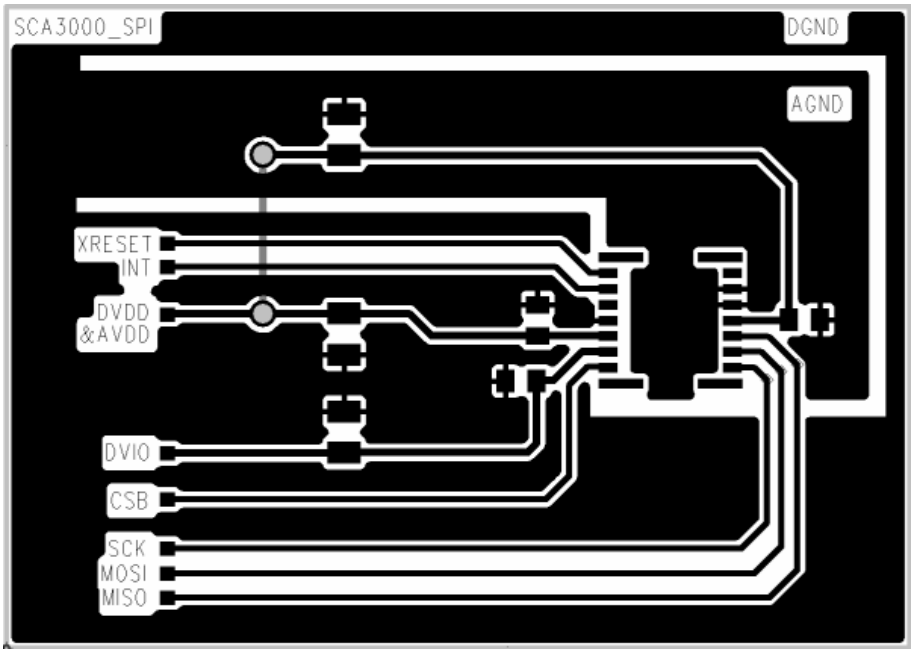

Figure 19 Recommended PWB layout for SCA3000 with SPI interface.

Recommended PWB layout for SCA3000 with I^{2}C interface is presented in Figure 20 below (circuit diagram presented in Figure 17 above).

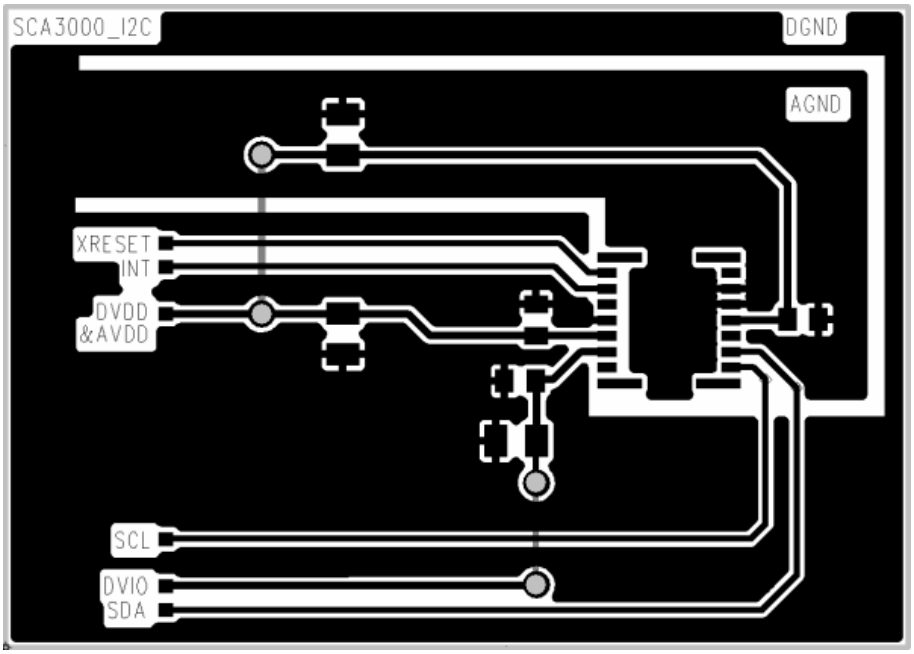

Figure 20 Recommended PWB layout for SCA3000 with I^{2}C interface.

7.4 Recommended stencil parameters

1. Stencil thickness 5 mils (127 µm).
2. Stencil openings 1:1 to PWB pad sizes.

8 Reference measurement setup

8.1 Linearity

8.2 Offset