Interfacing the 3 Volt DataFlash™ with a 5 Volt System

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As the semiconductor processes transitions to deep sub-micron lithography, supply voltages need to be reduced accordingly. The transition from 5 volt tolerant systems to 3 volt systems is accelerating in the current market place, however not all components have migrated to the lower voltages and system designers are encountering difficulty specifying the entire bill of materials in a single power supply range. This is an even greater problem for companies facing maintenance of legacy systems and spares sourcing where complete redesigns are not practical but at the same time due to obsolescence the original parts are not available in the original supply voltage range.

Atmel has kept this in mind when designing the AT45DBxxxB series, 3 Volt only DataFlash family. The 3 Volt DataFlash Family can be used in 5 Volt Systems. This applications note endeavours to discuss the conditions of using a 3 Volt DataFlash devices in a 5 Volt system or systems with mixed voltage environments.

AC Characteristics and Operational Conditions

Supply Voltage Requirements

The power supply to the DataFlash device must be between 2.7V and 3.6V for correct operation. Exceeding these levels may result in incorrect operation or damage to the device. Max ratings are shown in the AC Characteristics and Max ratings tables in the datasheets.

Logic Level Definitions

The majority of systems today conform to one or two logic interfacing standards, these being TTL or CMOS. It is therefor necessary to consider the effects of interfacing a 3 Volt Dataflash to a 5 Volt system that is either CMOS or TTL compatible

TTL Logic Levels

The minimum V_{IH} requirement of a TTL compatible input is 2.0V to register a logic 1, and the V_{IL} requirement of a TTL compatible input is 0.8V to register a logic 0. Refer to the manufacturers datasheet to ensure full compliance with the Input and output logic level requirements.

CMOS Logic Levels

The minimum VIH requirement for a CMOS compatible input is 0.7 x VCC to register a logic 1, where VCC is the supply voltage of the input device. For a CMOS device operating with a VCC of 4.5V to 5.5V this gives a VIH requirement of 3.15V to 3.85V. The VIL requirement of a CMOS compatible input is 0.2V to register a logic zero.

System Considerations and Problem Definition

To fully review the implications of operating a 3V DataFlash device in a 5V system, two aspects need to be considered:

1. Device Input and Output Level requirements.
2. Voltage Regulation to the Dataflash

Device Input and Output Level requirements

The DataFlash input pins are tolerant to 5 Volt input levels and will not present a problem in either CMOS or TTL compatible systems. The input and output pins for the DataFlash are shown top righ column:

The output pins however will only operate within the specification of the DataFlash and the limits of the VCCDF power supply. The Dataflash has one output pin in Serial Mode and 8 output pins in Parallel data mode. The RDY/BSY signal is an open collector output which indicates the current status of the device and is not discussed in this application note.

Dataflash Input Pins

- SI — Serial Data In
- SCK — Serial Clock
- /CS — Chip Select
- Reset — Reset input
- /WP — Write Protect

DataFlash Output Pins

- SO — Serial Data Out
- SO_0 – SO_7 — Data Out bit 7 through bit 0
- RDY/BSY — Ready Busy Signal

This applications note will only consider Serial Data mode.
The parallel data mode option is not available on all devices.

Driving a TTL compatible load

A DataFlash driving into a TTL compatible input will meet minimum TTL input logic level requirements. The DataFlash output will drive to VCCDF – 0.2V, therefore under worst case or lowest VCCDF conditions the minimum output level achievable by the DataFlash will be VOH=2.7V-0.2V = 2.5V. Figure 1 illustrates a typical system where the DataFlash is driving a TTL Compatible load.

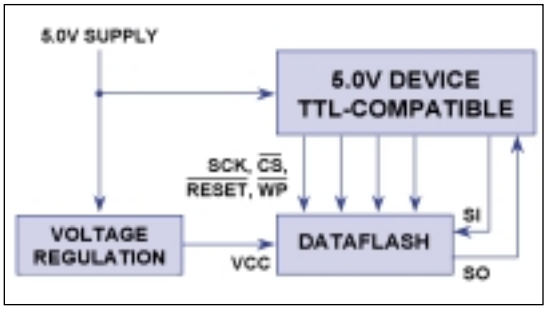

Figure 1: TTL Compatible Device Interface Diagram

Driving a CMOS compatible load

A problem arises when considering the Output drive levels provided by the Serial Output pin (SO) of a Dataflash when driving into a CMOS compatible interface. A standard 5V compatible CMOS input requires a VIH input of 3.15V minimum, greater than the output drive level a Dataflash can provide under worst-case conditions. As the Output of the DataFlash is not capable of driving a 5V CMOS load directly a level shifter or alternative method of translating the DataFlash output logic levels to those compatible with the input device is required. Figure 2. Illustrates the requirement for a level shifter in the Serial Data Output signal of the Dataflash when driving a 5V compatible CMOS input.

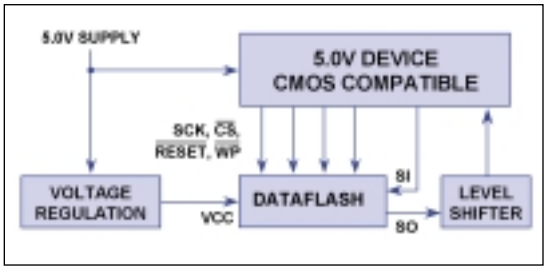

Figure 2: CMOS Compatible Interface Diagram

As the semiconductor processes transitions to deep sub-micron lithography, supply voltages need to be reduced accordingly. The transition from 5 volt tolerant systems to 3 volt systems is accelerating in the current market place, however not all components have migrated to the lower voltages and system designers are encountering difficulty specifying the entire bill of materials in a single power supply range.

Voltage Regulation

Few systems will provide both 5V and 3V regulated VCC rails in the same circuit, therefore a system or method to step down and regulate the voltage to the Dataflash is required. The choice of voltage regulator depends on the host system power supply characteristics, the maximum current drawn by the dataflash device, and the costs associated with adding a voltage regulator. In legacy systems this may also require additional thought towards the practical implementation of the chosen solution.

Programming Current

It is essential to consider the maximum current requirements of the Dataflash when selecting an appropriate method of voltage regulation. Maximum load or peak current draw occurs when the Dataflash is in programming or erase mode and will range from 70mA to 80mA. It is also important to consider RMS current requirements of the DataFlash during these operations. Current starvation will increase noise in the whole system and also lead to the incorrect operation and possible data corruption in the dataflash device during programming or erase operations.

System Solutions

By ensuring that the input signals to the Dataflash remained 5 volt tolerant, Atmel has minimised the overall impact of these essential process and device changes on end applications and customers. However two issues have been identified in the discussion above when attempting to use a Dataflash device in a 5V system as follows:

- A secondary Voltage Regulator will be required when using a Dataflash in a 5V system
- A Level Shifter will be required to translate the output logic level of a DataFlash output when used in a 5V CMOS compatible system.

Practical and workable solutions for these two issues will be wide ranging and many innovative solutions will be found. The following section will look at a some of the more conventional possibilities.

Voltage Regulation Solutions

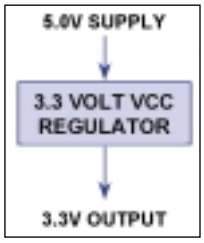

Figure 3: Voltage Regulator Diagram

Many off-shelf-voltage regulators or DC to DC converters exist today that would provide the DataFlash with a 2.7V to 3.6V regulated VCC supply from an input supply range of 4.5V to 5.5V. Figures 3 and 4 illustrate a typical voltage regulator solution utilising a Linear Technology LT1761 series Low Drop Out, Low Noise regulator. Other solutions could be implemented using a wide range of single chip voltage regulators or converters available from different manufacturers. Table 1 provides a short list of semiconductor manufacturers offering voltage regulators or DC/DC converters suitable for this application. Any voltage regulator based design would need to consider current delivery requirements and may require additional external components such as capacitors, resistors or inductors to ensure correct operation, regulation and current delivery. Please consult appropriate vendors datasheets and applications notes on the individual component specifications.

Figures 5 and 6 illustrate a simple three-diode regulator scheme. The threshold voltage (Vt = 0.7V apx.) for each diode would contribute to a total series

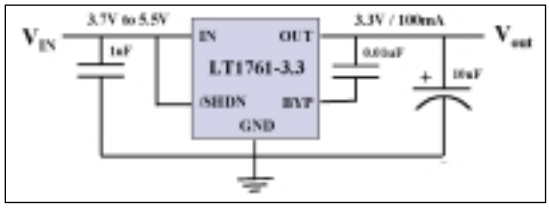

Figure 4: Example Voltage Regulator Solution

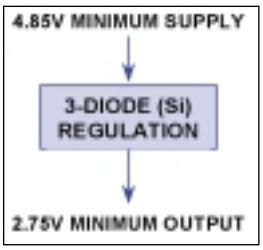

Figure 5: Example of a Simple Diode Voltage Regulator

voltage drop across the circuit of 2.1Volts. The advantage to this kind of regulation scheme is cost and space. One limitation of this circuit is the input voltage range, which must remain at or above 4.8V to ensure a minimum supply at the DataFlash remains above 2.7V. Selecting diodes with higher or lower Vt thresholds would allow for finer tuning of the circuit operation.

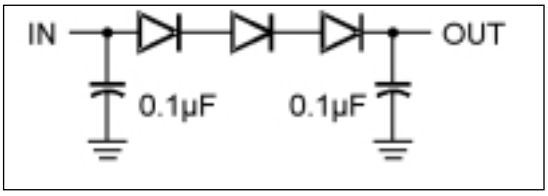

Figure 6: Simple Diode Regulator Circuit Diagram

Output Voltage Level Translation Solutions

The circuit illustrated in figure 7, utilises a Maxim MAX3370 Level translator circuit to level shift the low voltage output of the DataFlash device to a high voltage output compatible with the 5V CMOS circuit. The MAX3370 is capable of 2Mbps data transfer rates, which should be suitable for the majority of applications. Table 1 provides a short list of semiconductor manufacturers offering Level translators suitable for this application.

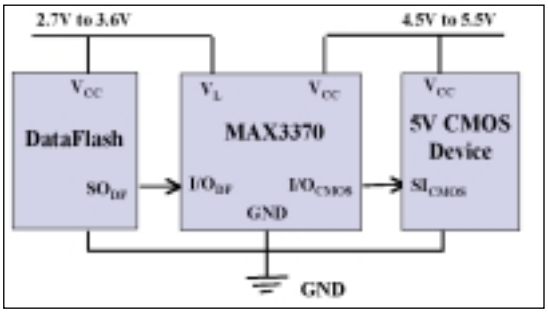

Figure 7: Example of a Voltage Level Translator

Function	Manufacturer	Web Site
Voltage regulation	Linear Technology	www.linear-tech.com
Voltage regulation	Texas Instrument	www.ti.com
Voltage regulation	Analog Devices	www.analog.com
Level Translators	Maxim	www.maxim-ic.com
Level Translators	Dallas Semiconductor	www.dalsemi.com

Table 1 – A short list of potential Voltage regulator and Level translator, manufacturers.

Conclusion

As this application note detailed, Atmel's AT45DBxxxB 3 volt DataFlash family can be easily interfaced to 5-volt devices in new systems or where legacy designs need to be supported. The system designer needs only to account for the proper I/O levels on the output side of the DataFlash device, peak current requirements during erase /programming cycles, and VCC supply voltage demands. The solution to overcome the differences in interface voltages will be determined ultimately by several factors, cost, space, practicality, system specification and performance. The scope of these changes has been minimised by Atmel's advance consideration of the impact of essential technology migration and evolution by ensuring that the Dataflash inputs remain 5 volt tolerant irrespective of supply voltage. ❑