Design considerations of power semiconductor devices employed in VSCs under short-circuit fault conditions in MVDC distribution grids

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Abstract

Electric energy distribution using medium voltage DC (MVDC) enables an advantageous performance compared to the state-of-the-art MVAC counterparts. Among others, a crucial challenge currently is related to the need for developing high-performance protection schemes against DC short-circuits and, thus, to prevent severe conditions of electric and thermal stress in the involved power electronics equipment. This paper presents an evaluation of design requirements and performance of four types of active rectifiers employed in MVDC grids under a DC short-circuit condition when using either an AC circuit breaker (AC CB) or a solid-state DC CB. The focus is on freewheeling diodes and the evaluation is performed in terms of power semiconductors stress, fault handling capability and chip area requirements by using simulations and calculations. The superior performance of DC CB over AC counterparts for all rectifier types is highlighted.

Introduction

Recently, the direct current (DC) power grids have gained momentum due to their inherent advantages compared to alternating current (AC) counterparts. The superiority of DC over AC grids is mainly found in the higher efficiency under the same voltage level, lack of reactive power compensation and no need for frequency synchronization [1], [2]. Today, transmission of large amounts of electric power over long distances using high voltage DC (HVDC) is an established technology, while MVDC distribution grids have also been identified as advantageous alternatives to MVAC grids not only by academia [1] but also by the leading industrial players of the field [3]. This is mainly due to the development of high-power semiconductor devices, which enable high-efficiency electrical energy conversions at various voltage levels. MVDC power electronic converters will potentially replace the bulky 50 and 60 Hz transformers used in MVAC grids, while they will also enable more flexible power control and ease the integration of distributed energy generation systems including renewable energy sources (RES) (e.g. wind power and solar) and large-scale energy storage systems. Other application areas of MVDC grids include marine vessels-shipboards [4], railways [5], data centers [6], as well as oil and gas platforms [7].

Power electronic converters used in DC grids can be categorized based on their specific topology design and their functionality (e.g. DC/AC, DC/DC etc.). In this study, active rectifiers (AC/DC) are discussed and presented. In a MVDC grid the most common rectifiers used are: (i) 2-level Voltage Source Converters (VSCs) [8]; (ii) 3-level Neutral Point Clamped (NPC) VSCs [6]; (iii) Modular Multilevel Converters (MMCs) based on Half Bridge (HB) submodules (SMs) and (iv) MMCs based on Full Bridge (FB) SMs [9].

Regardless of the specific topology used, the transition towards DC infrastructure faces a few crucial drawbacks that must be tackled. One of the greatest challenges of DC grids today is related to DC faults handling [10]. This refers not only to the protection of the DC lines as such, but also to the protection of power converters including their power semiconductor devices. Considering the currently operating HVDC transmission lines, DC faults are cleared by installing conventional mechanical breakers on the AC-side. The AC CBs operate reliably at a cost of relatively high peak values of the fault current and excessively long clearing times, which can exceed a few tens of milliseconds. On the other hand, various concepts of hybrid DC circuit breakers (CBs) for HVDC grids have been proposed [11], [12], which perform in significantly shorter times compared to the AC counterparts. Even though most of the proposed DC CB concepts have been experimentally evaluated, DC CBs have not been commercialized yet.

The majority of DC grids are interfaced with the AC grid and AC loads using three-phase VSCs. Under a DC fault condition in the DC grid, the power semiconductor devices and especially the freewheeling diodes face a severe stress in terms of current. In particular, under the fault condition, the VSC operates as a passive rectifier with the diodes in each phase leg carry a current that equals the total fault current, which is significantly higher than the nominal load current of the converter. It is, therefore, clear that the design of the converter must be made considering the surge current capability of the antiparallel diodes in order to ensure a safe and stable operation of the VSC under DC fault conditions. The surge current capability of the diodes can be either increased by increasing the available chip area of the diodes or by parallel-connecting several diodes with low current ratings [13].

The minimization of the excessive stress or even failure of the diodes in the VSC is directly connected with an efficient and reliable protection scheme with fast response against DC faults. As mentioned above, two approaches can be followed in order to handle faults in DC grids. The first approach is to connect a mechanical breaker on the AC side and the second one to connect a DC CB on the DC side. The most serious disadvantage of the mechanical CBs located in AC side is the relatively long clearing times. Mechanical AC CBs use the zero point crossing of the current, and thus they can interrupt the fault current within few cycles of the fundamental frequency. On the contrary, by commercially establishing DC CBs as an alternative to the AC counterparts, potential DC faults will be cleared within 2-5 ms in case of hybrid DC CBs, whereas this time can be shorter than 1 ms if pure solid-state DC CBs are employed. Thus, the anticipated surge current stress (i.e. thermal stress) of the VSC diodes will also be reduced. The latest is only feasible in low and medium voltage DC grids, where the number of series-connected semiconductor switches is still low compared to the corresponding numbers in a hypothetical solid-state DC CB for HVDC systems. Therefore, the conduction power losses of a solid-state DC CB in MVDC grids can still be moderate provided that an optimized design is followed.

The focus of this paper is limited to MVDC grids, where the choice of employing either an AC CB or a solid-state DC CB is still open. In particular, this paper studies the electrical performance and design of various types of VSCs interfacing an MVDC grid under two different protection approaches. The first approach relates to the use of an AC CB while the second one refers to the use of a pure solid-state DC CB connected on the DC line. The overall goal is to compare these two protection methods regarding the current stress caused in power electronic devices used in each of the four power converter topologies described above. The crucial factor of the comparison will be the current generated by a short-circuit in the DC side and its impact on the stress in the freewheeling diodes. Design guidelines for the considered VSCs in terms of power semiconductor devices will also be given. The structure of the paper is as follows: in Section II the four basic types of VSCs are discussed; Section III presents the DC grid under consideration; the simulation results are presented in Section IV; last but not least, Section V shows the conclusions.

Active Rectifiers for MVDC distribution grids

Transmission of large amounts of electric power over long distances is performed using HVDC lines, while the state-of-the-art technology for electricity distribution is AC grids. Recently, several studies have turned their attention to the MVDC grids for distribution of electric power. The MVDC grids can be considered as a platform that assists the integration of RES and energy storage systems with the AC grid, supply of emerging DC power loads and they generally address various future trends and needs of flexible and liberalized electric energy exchanges in a more optimized manner. Regardless of the specific application area, the heart of MVDC grids is the active rectifiers, which interfaces MVDC grids with AC counterparts and enable high-efficiency electrical energy conversions. The following active rectifiers will be studied in this paper: (i) 2-level VSC, (ii) 3-level NPC VSC, (iii) HB-based MMC with 5 SMs per arm and (iv) FB-based MMC with 5 SMs per arm.

Fig. 1 illustrates the basic schematic diagrams of each converter type. It should be mentioned that each power semiconductor device must withstand the blocking voltage and load current of the converter. Thus, series and parallel connections of switches and diodes might be an inevitable design approach for

MVDC systems. This increases the design and operating complexity of the system. The required devices for each type of rectifier will be analyzed in the next section.
In this study, a performance comparison between the above rectifiers is presented under the assumption of a short-circuit fault occurring in the DC side. Considering the topology of the FB-based MMC it is clear that it is able to operate as a current interrupter without the need of a CB. This is due to the current suppressing operation of full bridge circuits. Consequently, CBs are not necessary to be connected in the DC grid. However, the requirement for galvanic isolation still exists, which is beyond the scope of this study. On the other hand, the rest of the converter types always require a CB to protect against short-circuit faults.

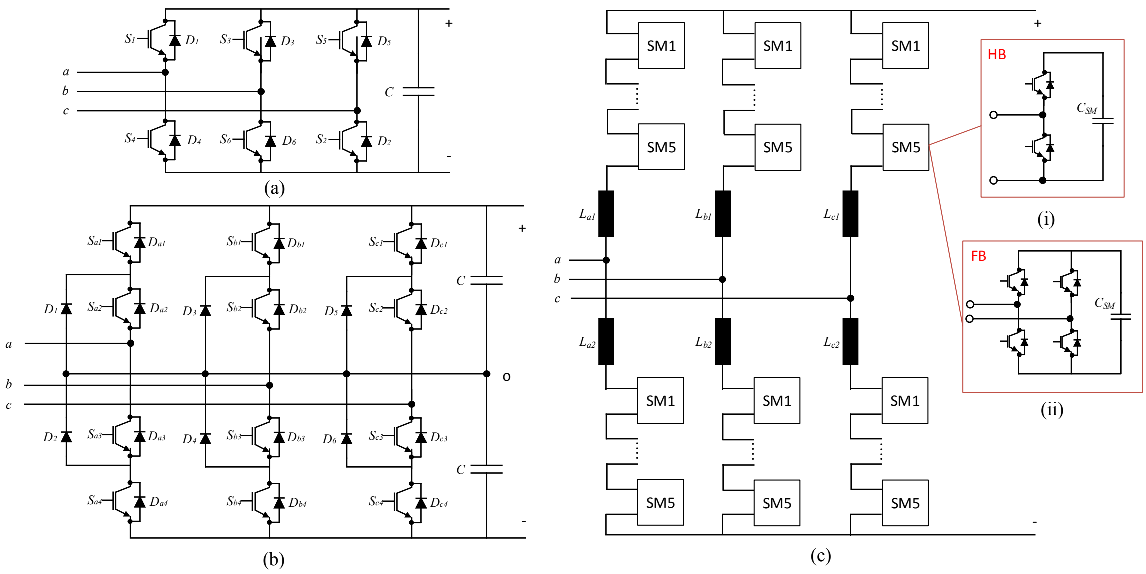

Fig. 1: Schematic diagrams of the basic types of active rectifiers. (a) 2-level VSC, (b) 3-level NPC and (c) MMC consisting of (i) HBs and (ii) FBs.

It is worth mentioning that, in literature there is also the line commuted converter (LCC) rectifier topology, composed by thyristors. Even if the use of thyristors is more popular in high voltage applications due to theirs inherent characteristics to withstand higher voltages and currents, the improvement of power semiconductor technology has led to replace the semi-controlled thyristors with fully-controllable semiconductor devices, such as insulated-gate bipolar transistors (IGBTs). Therefore, the LCC rectifier will not be presented in this study.

Protection schemes implemented in MVDC grids

Today, a major barrier towards the MVDC grid realization is the development of high-performance circuit breakers. In this context, high-performance refers to not only short clearing times and moderate transient overvoltages, but also low power losses during normal operation. These are the desired design and operating characteristics of a DC CB. The low line inductance along with the absence of a low-frequency transformer (i.e. no high leakage inductance) can lead to high fault currents during a DC short-circuit. On the other hand, AC grids use mechanical CBs to interrupt the fault current. Even if the clearance time of a short-circuit can be within tens of milliseconds by using mechanical CBs, this may not be a serious problem in AC grids due to the presence of high inductances and the anticipated lower rate of fault current increase. In DC grids, there is no natural zero crossing for the fault current, and therefore, the use of a conventional mechanical CBs is inadequate.
Two different approaches can be applied for short-circuit protection in DC power grids. The first uses the power converters not only to convert the power into desirable values but also as protection schemes. This power converter-based protection presupposes that the converters (e.g. VSCs or DC/DC) must be capable of interrupting the fault current. Thyristor-based converters and FB-based MMCs are two common examples of such converters. The second approach, namely DC CB-based protection strategy, requires an additional circuit connected in the DC line in order to clear fault currents. In literature [10],

[14], [15], there have been several different DC CB types presented. Several protection schemes that could be connected to MVDC grids are briefly analyzed as follows:

i. Power Converter-based protection

As mentioned above, the first protection method that can be applied in a MVDC grid uses the design and operating characteristics of power converters. In particular, two different approaches regarding the power converter-based protection can be identified in literature [10].

a. Power converters with inherent capability for current interruption

In several power converter topologies, there are freewheeling diodes that allow the fault current to flow resulting serious damages to them. On the other hand, other topologies (e.g. LCCs or FB-based MMCs) have the capability to interrupt the fault current inherently.

b. Power converters with employing an AC CB

When freewheeling diodes exist, the current interruption becomes more challenging. One solution to that might be the presence of the well-developed AC mechanical CBs connected to AC grid. Although it can interrupt the current, its operation time is relatively slow having a possibility to cause damages to the freewheeling diodes of the VSCs.

ii. Fuses

Fuses offer an alternative solution for overcurrent protection. They have been adopted in AC low voltage grids, providing a low cost and reliable solution. Their main drawback is related to the one-time operation, which means that right after their activation, they should be replaced due to the strip melting. Thus, they can only be utilized as a backup protection scheme in DC applications [16].

iii. DC CB

There are three main topologies of DC CB, which are analyzed as follows:

a. Mechanical DC CB with active or passive current injection

The basic principle of these breakers is to create an artificial zero crossing point for the current by means of a snubber circuit which is connected parallel to a mechanical breaker. Two approaches have been discussed in literature [14], namely CB with active or passive current injection. The analysis of them is beyond the scope of this study. Generally, the advantage of this approach is the low on-state losses. On the other hand, the maintenance requirements and the slow operating speed are the drawbacks.

b. Solid-State DC CB

The second type of DC CB replaces the mechanical breaker with solid-state CB, composed by power semiconductor devices [17], [18]. The modeling of a DC CB based on solid-state devices will be presented in the next section. The key advantages are the fast clearance times and the low maintenance requirements. The high power losses and the complexity are on the other hand, the major barriers.

c. Hybrid DC CB

The combination of a mechanical CB with power semiconductor devices constitute the last type, which is called hybrid CB. These breakers combine the advantages of mechanical breakers with the beneficial technology of power electronics in order to achieve short operating times and low on-state losses. Although it achieves faster operating times compared to mechanical CBs, always the remaining question is how adequate is that speed, having in mind the thermal stress of power semiconductor devices employed in VSCs. In literature many hybrid topologies have been identified and proposed [19].

iv. Galvanic isolator

A galvanic isolator [18] is required in order to eliminate the risk of leakage current in specific cases of CBs, such as solid-state and hybrid DC CBs. This device provides a physical isolation through a mechanical method and it operates right after the main breaker achieves to interrupt the fault current.

v. Fault current limiting methods

In a DC grid the line inductance is very low leading to high fault currents. Therefore, series-connecting inductors in the line could be a solution to limit the increased fault current. The drawbacks of this approach are the (i) additional power losses, (ii) high installation cost, (iii) volume and (iv) weight of the inductors. This method is used in HVDC grids [20] and it has been commercialized (e.g. ABB [21]). However, in a MVDC grid, the volume and the weight could be more critical (e.g. electric ships), and therefore, this approach seems to be less applicable. On the other hand, this method may offer solution to multi-terminal MVDC systems, where the interruption and isolation of the fault is critical in order to avoid undesirable power interruptions of healthy areas. On top of that, either CB or special designed power converters (e.g. Power Electronics Building Blocks, PEBB converters [22]) are usually placed along with these inductors at a high cost.

Modelling of the MVDC grid

The two DC grid configurations based on the protection scheme that have been considered for this study, are depicted in Fig. 2. The protection scheme of the first DC grid configuration (Fig. 2(a)) utilizes CBs employed on the AC side. Typical mechanical breakers based on Cassie model, which is appropriate in high power applications where high arc temperatures are expected [23] were modeled and simulated. The second DC grid under investigation uses a solid-state DC CB connected on the DC grid, as illustrated in Fig. 2(b).

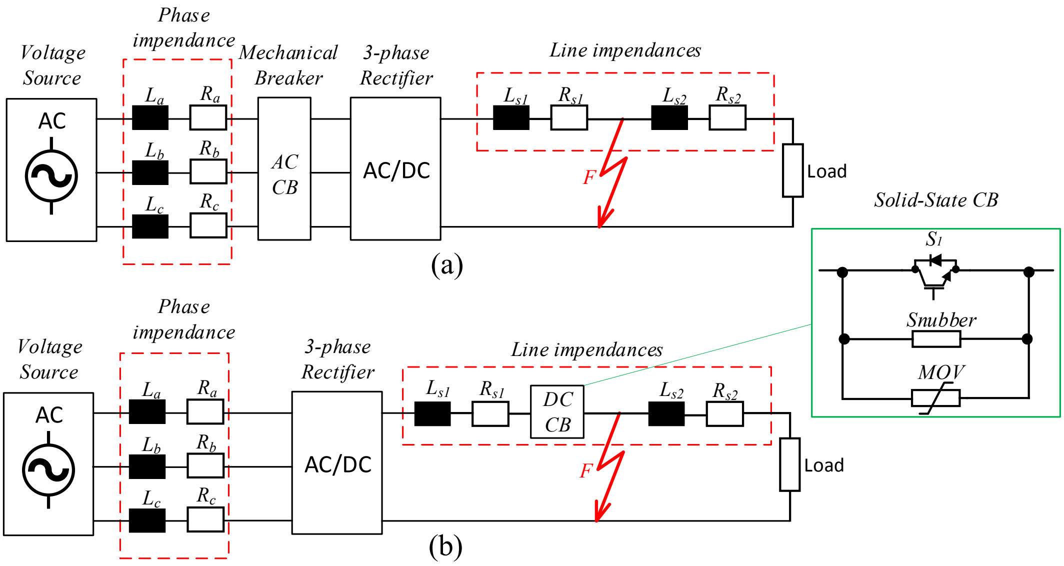

Fig. 2: Schematic diagrams of the two DC grid configurations under study: (a) Protection using an AC CB on the AC side and (b) protection using a solid-state DC CB on the DC side.

Although there is no any standards regarding the voltage distinction between low, medium and high-voltage DC systems, it is recommended [4] that the nominal voltage level of MVDC grids starts around 1-3 kV and reaches approximately 69 kV. In this study, the nominal MV direct voltage was set to 15 kV. The power rating of the load equals 22.5 MW (thus the nominal current is 1.5 kA). In Fig. 2, L_{s1}, R_{s1} and L_{s2}, R_{s2} represent the line inductances and resistances prior and beyond the fault point, respectively. Based on the study presented in [24], the line inductances and resistances in DC power lines were set to 0.347 mH/km and 0.089 Ω/km. Additionally, the length of the line is equal to 1 km and the fault occurs in the middle of the power line. It should be mentioned that due to the low line inductance, the point that the fault occurs is not particularly important. This means that the impact of

Table I: Parameters of the MVDC grid under study

Parameter	Symbol	Value	unit
AC Voltage - Line to Line RMS value	V_{LL}	12.25	kV
DC Voltage	V_{DC}	15	kV
Phase inductance	$L_{a,b,c}$	3.255	mH
Phase resistance	$R_{a,b,c}$	3	mΩ
Line inductance prior the fault point	L_{s1}	0.174	mH
Line resistance prior the fault point	R_{s1}	45	mΩ
Line inductance beyond the fault point	L_{s2}	0.174	mH
Line resistance beyond the fault point	R_{s2}	45	mΩ
Load	P_L	22.5	MW

the fault on the power converter in the MVDC grid will not differ significantly if the fault would have been occurred just on the DC output of the VSC. Table I summarized all the design and operating parameters of the considered MVDC grid. Finally, the commercially available power IGBT with antiparallel diode used in this study, is the ABB 5SNA 3000K452300 [25]. Since the focus of this paper is to investigate the current and thermal stress of each power diode employed in the VSCs, the crucial parameters given by the datasheet related to the diodes are as follows: the nominal current equals 6 kA, the breakdown voltage is 4.5 kV, the surge current of the diodes is given as 21 kA, the limiting integral load is 2.2 kA^2sec, and the ratio between IGBTs and diodes is 2:1. Moreover, it comprises of 6 submodules and each submodule contains 12 chips. As a result, each power module has 72 chips (48 IGBTs and 24 diodes). The required chip area for the freewheeling diodes connected to each VSC topology can be extracted based on the aforementioned parameters.

The modeling of the various under consideration components will be presented below:

i. Modeling of mechanical breaker

In literature, several mechanical breaker models have been identified. The detailed analysis of the mechanical breaker is beyond the scope of this study. Herein, the Cassie arc model [26] was adopted due to the high generated currents. A brief description of various arc models is given in [26].

ii. Modeling of solid-state DC CB

The solid-state DC CB (Fig. 2(b)) consists of IGBTs, a RCD snubber circuit and a MOV. In order the breaker to withstand the transient voltage during the turn off process, a series connection of IGBTs must be applied. Considering the design parameters of the investigated MVDC grid, 5 series-connected IGBTs are needed to withstand the 15 kV.

iii. Modelling of 2-level VSC

The 2-level VSC considered is illustrated in Fig. 1(a). A crucial process is the output capacitor design. When the short-circuit occurs, the capacitor discharge initially takes place. Thus, the capacitance determination is of high importance. The following equation gives the required capacitance:

$$C_{VSC} = \frac{S}{2\pi f V_{DC} \Delta V_{DC}} = 34.65\ mF$$

where, S is the apparent power, f the grid frequency, V_{DC} the DC voltage and ΔV_{DC} the acceptable voltage ripple (i.e. 10%).

iv. Modelling of 3-level NPC

Fig. 1(b) illustrates the 3-level NPC power converter. Similarly to the previous case, the output capacitors design is also significant due to their primary discharge process. Herein, two capacitors are connected. Each capacitor has been calculated in a similar way as in the 2-level VSC. The resulting values for each capacitor due to series connection is 69.3 mF.

v. Modelling of the HB-based MMC

Fig. 1(c(i)) shows the HB-based MMC that contains 5 SMs per arm. Furthermore, the capacitors in each sub-module have been calculated based on the formula shown in [27]:

$$C_{cell} = \frac{2NE_{nom}}{V_{DC}} = 19.1\ mF$$

where, E_{nom} is the required energy stored in the capacitor and N is the number of SMs per arm. Based on [27], the required energy stored in each capacitor was calculated to 72 kJ/MVA. Furthermore, a 10% voltage ripple was considered in order to be in accordance with the previous cases. Besides the capacitors, the MMC topology requires inductors connected on each arm [28] as illustrated in Fig. 1(c).The purpose of these inductors is threefold. Firstly, the limitation of short-circuit current, secondly the reduction of circulating current between the phases and lastly, the current ripple reduction due to high switching frequency. In fact, in grid-connected applications, suitable values of the arm inductors could very well be in the range of 0.1 p.u [27]. Therefore, the arm inductances were defined to 13 mH.

vi. Modelling of FB-based MMC

The FB-based MMC consists of 5 SMs per arm, as illustrated in Fig. 1(c(ii)). The capacitors and the arm inductors follows the same principle with the HB-based MMC configuration.

Simulation results

For the purposes of this study, seven system configurations in terms of CBs and VSCs were modeled and simulated in Matlab/Simulink. The cases of the converter and breaker type combinations are itemized as follows: (i) 2-level VSC with AC CB, (ii) 2-level VSC with DC CB, (iii) 3-level NPC with AC CB, (iv) 3-level NPC with DC CB, (v) HB-based MMC with AC CB, (vi) HB-based MMC with DC CB, (vii) FB-based MMC without CB.

In all scenarios, the applied fault was a pole-pole short-circuit occurring at the time point *t=0.5 sec*. Apart from that, the command to trigger the CB, is given when the current exceeds 2 per unit, which in this study corresponds to 3 kA.

Fig. 3 illustrates the short-circuit current flowing in the DC line for all the aforementioned scenarios. The first two rectifier topologies (i.e. 2-level VSC in Fig. 3(a) and 3-level NPC in Fig. 3(b)) show similar performances under the examined fault condition. In case of employing an AC CB (waveforms shown with black lines in Fig. 3), the fault current becomes extremely high, while for its complete clearance several milliseconds are required. In particular, the fault current in both 2-level VSC and 3-level NPC topologies is approximately 140 kA and its clearance time approximately 28 msec. This implies significant electrical stress causing apparently serious damages on power electronics components, unless they are properly dimensioned for this. On the other hand, by using a DC CB (waveforms shown with red lines in Fig. 3), the fault current is considerably limited and the clearance time also becomes much shorter. More specifically, the peak fault current in both 2-level VSC and 3-level NPC topologies is approximately 4 kA and the clearance is achieved within 152 μsec. The results using the HB-based MMC are depicted in Fig. 3(c). Similarly, employing an AC CB the fault current is higher than employing a DC CB. In the AC CB scenario, the fault current reaches 4.6 kA, while in the DC CB case, it is approximately 3 kA. The difference is not as high as it was in the previous case, but it may still result in a sever condition for the converter. Obviously, the reason for the significantly lower current, is the arm inductors that are connected in the converter and limit the rise of the fault current, as it was analyzed earlier. Another consequence of that is the long clearance time achieved in AC CB case (758 msec in AC CB case and 5.3 msec in DC CB). The last system under investigation is the FB-based MMC topology where there is no need for a CB (except of the need for galvanic isolation). Fig 3(d) shows the short-circuit current in the FB-based MMC case. The short clearance time along with the low fault current, indicate the good performance of this fully controllable

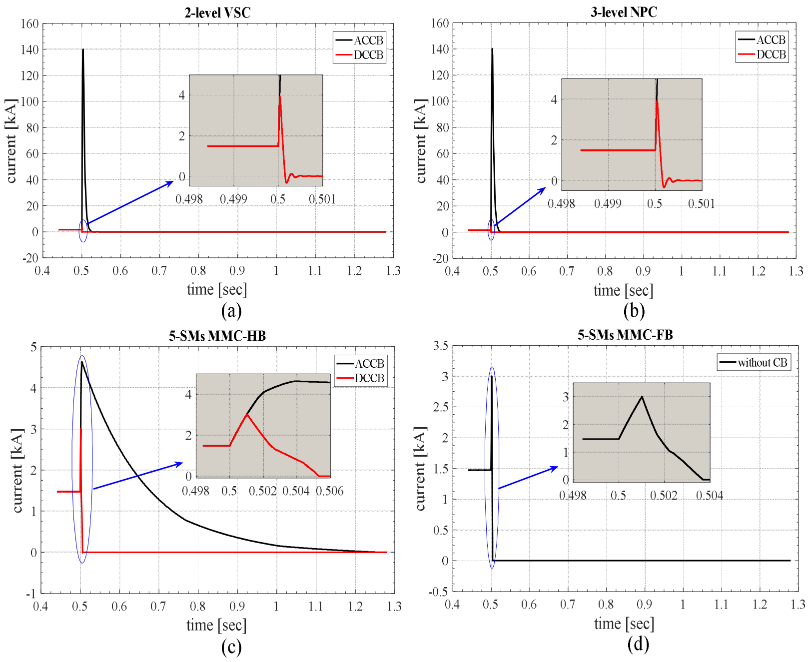

Fig. 3: Simulation results of the performance of the short-circuit current in the 4 different topologies under study when employing either AC CB (black line) or DC CB (red line) (a) 2-level VSC, (b) 3-level NPC, (c) HB-based MMC and (d) FB-based MMC.

type of rectifier during fault conditions. From the simulations, it was found that the short-circuit current reaches up to 3 kA and the fault is cleared within 3.7 msec.

The fault current that flows through the antiparallel diodes in each scenario is depicted in Fig. 4. It should be mentioned that the fault current flows through the freewheeling diodes in all three phases, but it is not equally distributed. Therefore, Fig. 4 depicts the diode current with the highest stress, considering the applied fault shown in Fig. 2. Moreover, in Figs. 4 (a) and 4 (b) the significantly lower fault current anticipated using the DC CB over the AC counterparts prevents serious damages to the power electronics equipment. As an example, the diode current is reduced by 200 times. Furthermore, a reduction of the fault current that flows through the freewheeling diodes in HB-based MMC topology (Fig. 4 (c)) by using DC CB instead of AC CB can also be observed. This reduction is approximately 18%. Finally, in FB-based MMC topology, the diode peak current equals 2.62 kA when the short-circuit is applied.

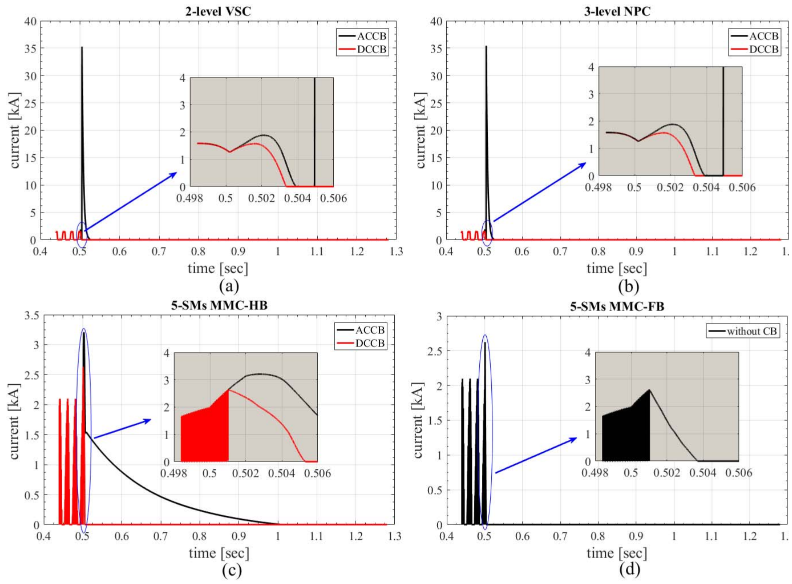

Fig. 4: Simulation results of the diodes current in the 4 test cases of VSCs when employing either AC CB (black line) or DC CB (red line) (a) 2-level VSC, (b) 3-level NPC, (c) HB-based MMC and (d) FB-based MMC.

Table II summarizes various simulated performance parameters of all types of converters in case of employing an AC CB, while Table III shows the same results in case of using a DC CB. The performance evaluation parameters for the above-mentioned cases are: (i) the peak value of both short-circuit and diodes currents, (ii) the clearance time and (iii) the thermal stress of diodes in terms of load integral. The information presented in these tables is based on the simulation results shown in Figs. 3 and 4. In addition to this, all VSC topologies achieve a better performance with the DC CB instead of AC counterparts, in terms of faster clearance times and lower fault currents. Thus, the anticipated current and thermal stresses for the diodes are also lower.

Table II: Simulation results using the AC CB

Type of rectifier	Peak current of diodes [kA]	Short-circuit current [kA]	Clearance time [msec]	Load integral of diodes [kA^2sec]
2-level VSC	35.3	140.1	27.97	2.6
3-level NPC	35.43	140.1	27.35	2.6
HB-based MMC with 5 SMs	3.21	4.63	758	0.32
FB-based MMC with 5 SMs*	2.62	3.001	3.7	0.01

*case without CB

Table III: Simulation results using the DC CB

Type of rectifier	Peak current of diodes [kA]	Short-circuit current [kA]	Clearance time [msec]	Load integral of diodes [kA^2sec]
2-level VSC	1.58	3.912	0.152	0.01
3-level NPC	1.58	3.912	0.152	0.01
HB-based MMC with 5 SMs	2.63	3.012	5.3	0.02
FB-based MMC with 5 SMs*	2.62	3.001	3.7	0.01

*case without CB

Finally yet importantly, Table IV illustrates the required chip area for the freewheeling diodes. It was assumed that each diode chip has an area of 1 cm^2. The parameters given in the datasheet were taken into account as well. Three cases were considered for the appropriate dimensioning of the diodes, based on nominal current, peak current and thermal stress (i.e. load integral). The worst cases for each VSC in terms of required chip area are highlighted in the aforementioned table. In AC CBs configurations, the proper dimensioning should be based on peak value of the current that flows through the freewheeling diodes for the 2-level VSC and 3-level NPC, while in the rest of the cases, the nominal current dominates as it dictates the worst case in terms of required chip area. On the other hand, when a DC CB is employed, the diodes must be dimensioned only based on the nominal current. This concludes that the over-rated dimensioning of the diodes can be avoided when a DC CB is employed. More specifically, in both 2-level VSC and 3-level NPC converters, the area gain of employing a DC CB is approximately 335% compared to AC counterparts. That gives a significantly reduction of size and design complexity of the converter. Lastly, the number of diodes used in each topology was calculated based on the blocking voltage of each module (i.e. 4.5 kV) and the grid voltage (i.e. 15 kV). As a result, series-connected power semiconductor devices must be considered.

Table IV: Simulation results for the determination of the required chip area for freewheeling diodes

Type of rectifier	Number of diodes	Chip area based on nominal current [cm^2/diode]		Chip area based on peak current [cm^2/diode]		Chip area based on thermal stress [cm^2/diode]	
		AC CB	DC CB	AC CB	DC CB	AC CB	DC CB
2-level VSC	30	12	12	40.3	1.8	28.4	0.1
3-level NPC	54	12	12	40.5	1.8	28.4	0.1
5-SMs MMC-HB	60	16.8	16.8	3.7	3	3.5	0.2
5-SMs MMC-FB*	120	16.8	16.8	3	3	0.1	0.1

*case without CB

Moreover, it is worth mentioning that in the case of the FB-based MMC topology, the requirements for power semiconductors is the highest resulting in a more complex converter design. Apart from that, it is necessary to emphasize that in cases of MMC used, the passive elements considered (i.e. arm inductors and capacitors of SMs) increase the design complexity, volume and apparently the cost of the complete system compared to the other examined topologies. However, using an MMC, a better transient performance is achieved under a fault condition. Last but not least, when a DC CB is used, the observed differences in peak fault currents, electrical stresses of the semiconductors and clearance times among all the investigated VSC topologies are extremely small. As a result, this is also a clear indication of choosing the solid-state DC CB technology for high-performance short-circuit fault clearance instead of the conventional AC CBs. Nevertheless, this is achieved at a cost of higher conduction losses under regular operation of DC CB compared to AC counterparts.

Conclusion

MVDC grids are expected to be expanded within the next decade. Active rectifiers will be one of the most significant system component of the future MVDC grids. This paper presented a comparative study among four types of VSCs under a short-circuit condition on the DC side. Two different approaches of the required protection schemes were considered. The first is based on a mechanical AC CB connected on the AC side, while the second approach concerns a solid-state DC CB connected on the DC line. The evaluation criteria were the fault current flows through the freewheeling diodes, the fault clearance time, the thermal stress and the required chip area for the power diodes employed in each VSC topology. The study extracts a few significant observations. Firstly, the DC CB achieves a faster response in all VSC cases compared to AC breakers and, consequently, lower peak fault currents. More specifically, it clears the fault within less than 160 μsec in 2-L VSC and 3-L NPC while when an AC CB is employed, the corresponding times are approximately 200 times longer. Regarding the difference between the two approaches, similar results are also obtained in the case of HB-based MMC topology. On top of that, the fault currents were 20 times higher in AC CB approach for the first two rectifier topologies. A second conclusion is that the thermal stress in case of employing the DC CB is significantly lower (in the order of 200 times for the first two VSCs, 15 times for HB-based MMC). The third conclusion refers to the case of AC CBs, where the FB-based MMC (case without CB as mentioned above) achieves the best performance in terms of clearing time, peak fault current and thermal stress due to its inherent fault handling capability. On the other hand, the main drawback is related to the design complexity of this FB-based MMC, which requires more power electronic devices compared to other VSCs. In addition to that, the required chip area for the freewheeling diodes was investigated. In both 2-level VSC and 3-level NPC topologies, the implementation of DC CB resulted in a significant reduction of the required area compared to using AC CB. Last but not least, using the DC CB approach, the differences in currents stresses among all VSCs are almost eliminated due to the fast operation of this CB.

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