Comparison of Ultra Low Power Full Adder Cells in 22 nm FDSOI Technology

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***Abstract*—Five ultra low voltage and low power full adders have been designed and analyzed with CMOS logic structure. To compare these adders, different metrics including worst case delay, average power, PDP, and PDP*Leakage have been investigated in the supply voltage varying from 140-160 mV. All the full adders have been designed and verified with Cadence Virtuoso design in a commercially available 22 nm FDSOI technology. An extended body bias voltages introduced in a 22 nm FDSOI technology have been used to balance Pull Up/Pull Down Networks and have a high functional yield. The test bench has been used to verify the functionality of full adders automatically in different conditions of temperature and supply voltage. The simulation results show that an Xor based adder is the best of all having the lowest delay, power, PDP, and PDP*Leakage in different conditions.**

***Index Terms*—ultra low voltage, low power, 22 nm FDSOI technology, extended body bias, PDP, PDP*Leakage.**

I. Introduction

In Internet of Things (IOT) applications, the design of implantable medical devices such as pacemakers, that could save a patient's life in emergency situations, is very critical [1], [2], [3]. Power consumption is a key issue in such applications which have long stand-by time. Using minimum possible supply voltage where it is below the absolute value of MOS threshold voltage makes circuits reduce power consumption. Operating at the subthreshold regime has been investigated since the sixties [4]. Considering the exponential relationship between current, temperature, threshold and supply voltage is a key concern in order to investigate the functionality of the circuits in different conditions in this regime. Fully Depleted Silicon on Insulator (FDSOI) technology has emerged to tackle the problems of ultra low voltage design. In this technology, the efficiency of body biasing technique has been increased by controlling the channel. Body bias technique in FDSOI and CMOS technology has been used in many works to reduce supply voltage and hence circuit power consumption [5], [6], [7]. In this paper, an extended body bias technique has been used in a commercially available 22 nm FDSOI technology. This method has been applied to design five full adders in supply voltages below the absolute value of MOS threshold voltage and is applicable for implantable medical IOT applications. Full adders have been designed at temperature range 27-50°C, which is appropriate for implantable medical applications and with ultra low supply voltages varying from 140-160 mV to reduce the power consumption. Simulation for all adders has been done at 1 kHz frequency which is relevant for many IOT applications and max operating frequency. To achieve this goal, different aspects of digital circuits design in the subthreshold regime have been considered. Then, a new test bench has been suggested for the functionality of such circuits. Different performance metrics of five full adders have been simulated and the results have been compared. It is concluded that Xor based adder is the best option in this supply voltage range which yields the lowest delay, power, PDP, and PDP*Leakage.

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II. Design Consideration in the Subthreshold Regime

Expressed by the following simplified equation, NMOS transistor subthreshold current has an exponential relation with the gate-source and threshold voltage [8].

$$I_{ds} = I_0.(e^{(kV_{gs}/V_T)}e^{((1-k)V_{bs}/V_T)})(1 - e^{-V_{ds}/V_T} + V_{ds}/V_0) \quad (1)$$

Where I_0 is a constant related to the channel width and length of the MOS transistor. V_T and V_0, are the thermal and the Early voltage, respectively. k is approximately 0.7-0.75 which is related to subthreshold slope factor $(1 + C_{dep}/C_{ox})$. This equation can also be applied for PMOS with opposite polarity. Static power consumption is a dominant source for the total energy of the low frequency system. To reduce leakage and improve performance in CMOS logic gates, balancing of PUN/PDN[1] is a strong knob. The strength of the transistors can be tuned by using both body biasing and aspect ratio as well as device type [9] which will be discussed in more details in this section. Based on equation (1), digital circuits in the subthreshold regime are more sensitive to PVT (process, voltage, and temperature) variations than those of superthreshold. Threshold voltage variations caused by RDF (random dopant fluctuation) increase process variation which is proportional to the inverse of the square root of the transistor area.

[1]Pull Up/Pull Down Network

A. Design Strategies

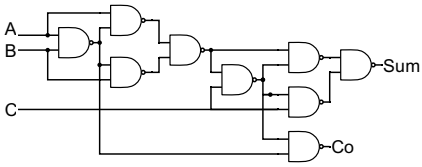
According to the above information, subthreshold circuit designers should avoid taking minimum length and width for the transistors in order to decrease the variability. High width PMOS transistor causes larger capacitance in the circuit and hence more area and power consumption. Choosing the ratio of two for W_{PMOS}/W_{NMOS} is suitable to improve mismatch variation because of having a regular layout. Using HVT devices is recommended for reducing the leakage current which is the first priority in such an application. Body biasing is one of the techniques used for tuning the PUN/PDN. This method manipulates threshold voltage by change back gate voltage. The goal is to find a body bias voltage for both NMOS and PMOS transistors which results in a reasonable functional yield in full adders.

B. Full Adders Circuits Design

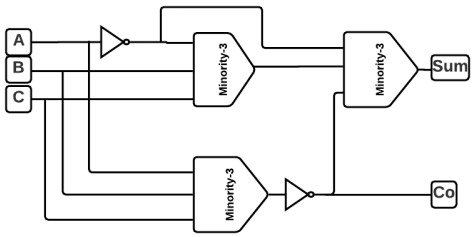
Schematics for five different full adders are shown in Fig.1. It has been proved that in the subthreshold regime and especially at the ultra low supply voltages, I_{on}/I_{off} is lower than that of the superthreshold regime. Gates having a maximum fan-in of 2-3 should be used to avoid robustness problems occurred in circuits and improve the functional yield [9]. Therefore, in this study, Minority-3 based, Nand based, Xor based and Nand-Nor based full adders have been selected for simulation [10]. The results then have been compared to the 28 transistors standard adder [10].

All gates have been designed and verified using Cadence Virtuoso design in a commercially available 22 nm FDSOI technology. They have been designed with HVT transistors optimized for reverse back biasing in order to reduce the leakage current. As shown in Fig.2, either subthreshold current or leakage current is highly affected by the sizing of transistor length, L.

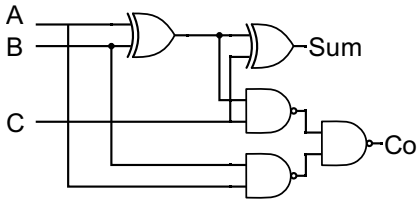
Leakage current variation due to the change of transistor length is very high between 20-28 nm in comparison with 28-36 nm. Therefore the length of 28 nm is used for both reducing leakage and improving threshold voltage variation. The width for all NMOS and PMOS transistors is 200 nm and 400 nm, respectively, except for PMOS in Minority-3 which is 600 nm. The goal is to select the best body bias that has less leakage current and variability. To do so, leakage current variation of inverter designed with HVT transistors versus different back bias voltages has been simulated and shown in Fig.3. Leakage current variation of the transistor due to the changing of back bias voltage of both PMOS and NMOS transistors is very high between 0-300 mV in comparison with 300 mV to 2 V. Increasing reverse back bias voltage increase the variability. In order to decrease both leakage current and variability, selected body bias voltages have been tabulated in TABLE I.



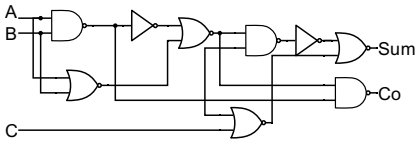
(a) Nand based adder



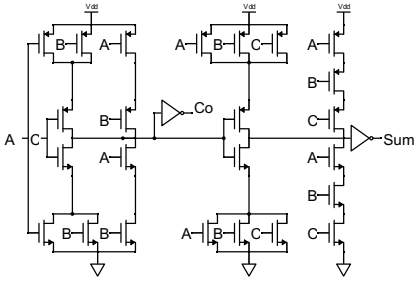
(b) Minority based adder



(c) Xor based adder



(d) Nand-Nor based adder



(e) 28 transistors Standard adder

Fig. 1: Five different adders

III. Results

A. Test Bench

Digital circuits are affected by so much variation in the subthreshold regime that they may not be functional in the worst case condition. Therefore using a systematic way is essential to evaluate the functionality of the circuits in the all different conditions. The suggested automatic test bench is shown in Fig. 4.

An ideal 3-bit ADC has been used to produce different inputs of one bit full adder in DC simulation. In result capture block, the outputs of the adder have been compared with

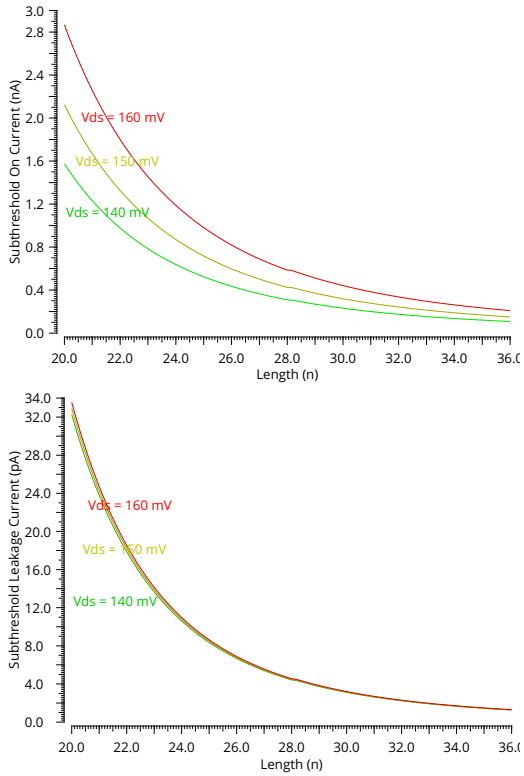


Fig. 2: Subthreshold On and Leakage currents versus length for NMOS transistor in different supply voltages, V_{ds} =140, 150, 160 mV, W=200 nm

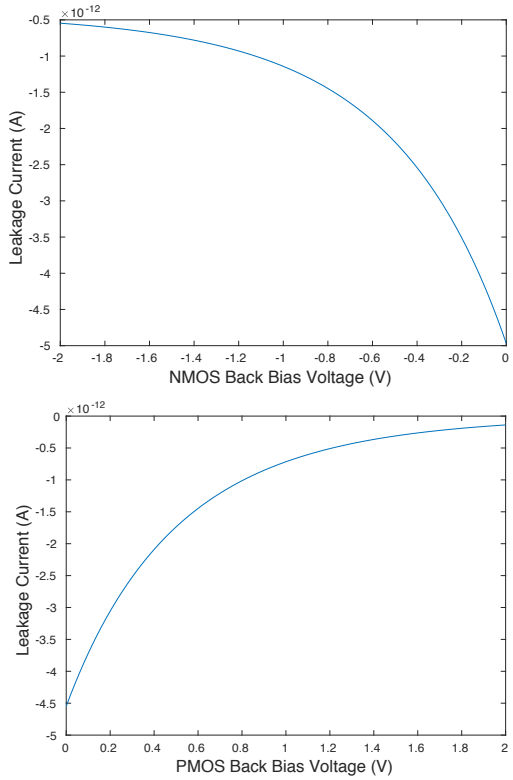


Fig. 3: Leakage current of inverter versus Back Bias Voltages, W_{PMOS}/W_{NMOS}=400 nm/200 nm, L=28 nm

TABLE I: Back Bias Voltages for PMOS and NMOS transistors in different gates.

GATES	VBBN[a]	VBBP[b]
Minority-3 and Nor	-300 mV	0
Nand and Inverter and Xor	0	V_{dd}
Transistors in Standard adder	0	V_{dd}

[a]NMOS Back Bias Voltage.
[b]PMOS Back Bias Voltage.

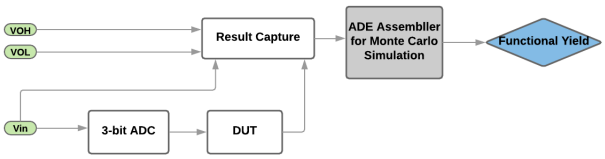


Fig. 4: Test Bench for functional yield simulation.

both maximum acceptable low voltage (V_{OL}) and minimum acceptable high voltage (V_{OH}) which are equal to 0.25*vdd and 0.75*vdd of the full adder, respectively. To see the effect of process and mismatch variation, the output of result capture goes to the ADE Assembler in order to perform sufficient number of 1 k Monte Carlo simulation [11], [12] and obtain the functional yield of the full adder automatically. The driving power has been considered by using output FO4 load inverters [13].

B. Simulations

Different circuit metrics calculated from simulations for the full adders have been compared together. Full adders have been simulated at 1 kHz frequency which is the case for many IOT applications, at temperature range 27-50°C, which is appropriate for implantable medical applications with the supply voltage varying from 140-160 mV to reduce the power consumption. The suggested test bench result showed that Monte Carlo simulation for five full adders in different conditions has not been failed for all 1 k iterations. The plots for inputs and outputs of Xor full adder at a supply voltage of 150 mV has been shown as an example in Fig. 5.

Since the changing of an input transition may not necessarily alter the output results, for accurate power measurement, all different input transitions should be considered. Fig. 5 shows the different input transitions used for estimating the average power consumption of the full adders [13]. Fig. 6 demonstrates the test bench used to find the critical path resulting in the worst case delay. Verilog-AMS has been used to simulate the test bench. The same load as the test bench for functional yield has been used for full adders to create more realistic output capacitance which affects the delay of the circuit. All combination of transitions for three different inputs has been

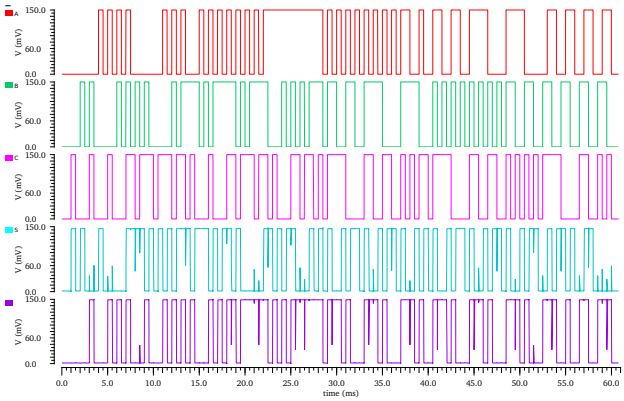


Fig. 5: Inputs and Outputs of the Xor based full adder at a supply voltage of 150 mV and 1 kHz frequency.

considered in the input generator. In result capture block, the rise and fall time of different transitions have been calculated. Circuit metrics including average power, worst case delay, and

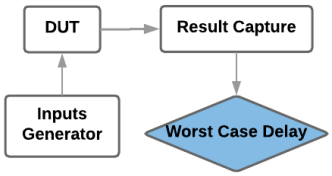


Fig. 6: Test Bench for worst case delay.

leakage current for a range of supply voltages between 140-160 mV at 1 kHz frequency are summarized in Tables II, III, IV, V and VII. Energy per operation at this frequency can be calculated with $P = E/T$. Since each addition is done in half of the period, T in this equation is 500 us for 1 kHz frequency. In order to have a comparison for the area of adders, W_N=200 nm has been assumed as one unit, the considered area for Xor, Nand based adder is 54 units. This metric for Nand-Nor and Minority-3 based adders and the standard adder is 48, 66 and 42 units, respectively.

TABLE II: Nand based adder metrics at 27°C and 1 kHz.

Vdd(mV)	Power(pW)	Delay(us)	Leakage(pA)
140	7.20	7.99	46.3
150	7.91	6.34	47.4
160	8.74	5.03	48.6

TABLE III: Minority-3 based adder metrics at 27°C and 1 kHz.

Vdd(mV)	Power(pW)	Delay(us)	Leakage(pA)
140	3.52	14.0	21.0
150	3.94	11.1	21.9
160	4.37	8.73	22.8

Energy per operation (which is PDP at max operating frequency) for all full adders at the maximum operating

TABLE IV: Xor based adder metrics at 27°C and 1 kHz.

Vdd(mV)	Power(pW)	Delay(us)	Leakage(pA)
140	2.24	5.84	12.7
150	2.46	4.68	13.1
160	2.69	3.73	13.5

TABLE V: Nand-Nor based adder metrics at 27°C and 1 kHz.

Vdd(mV)	Power(pW)	Delay(us)	Leakage(pA)
140	6.24	7.34	41.4
150	6.90	5.81	42.8
160	7.60	4.59	44.3

TABLE VI: Standard adder metrics at 27°C and 1 kHz.

Vdd(mV)	Power(pW)	Delay(us)	Leakage(pA)
140	3.95	8.60	22.8
150	4.357	6.9	23.4
160	4.74	5.54	23.9

frequency of 150 mV supply voltage have been listed in TABLE VII.

IV. Discussion

According to the simulation results for 1 kHz frequency shown in Tables II, III, IV, V and VII, the Xor based full adder achieved the lowest power consumption, leakage and delay. The second one in terms of consumption of power and leakage is the Minority-3 based adder. TABLE VII shows four metric indicators at the max operating frequency for each adder. Xor based adder is the best of all because not only consumes the least power consumption but also is the fastest among five adders and has the least energy per operation. At 150 mV supply voltage, the Nand based adder consumes 3.22 times as much as the Xor based adder consumes. Among the five adders, Minority based adder is the slowest. The delay of the Minority-3 based adder is more than 2X of that for the Xor based adder. Since all adders are designed with HVT devices and they have reverse back bias voltages for NMOS or PMOS devices, huge delays have been observed. In spite of the huge delays, these adders are more desirable for low frequency applications. The static power consumption is a dominant part of the total energy of low frequency systems. As listed in Tables II, III, IV and V, the leakage current of the full adder based on Nand is the largest and it is 1.11, 2.16, 2.03 and 3.62 times as much as that of the full adders based on Nand-Nor, Minority, standard and Xor, respectively. To see

TABLE VII: Energy per operation of five full adders at maximum operating frequency and Vdd= 150 mV.

Type	Power (mW)	Fmax (kHz)	Energy Per Operation (aJ)	Energy Per Operation *Leakage*10^{-29}
Minority-3 Based	8.87	25.0	177	388
Nand based	28.4	83.3	170	809
Xor Based	6.15	58.9	52.2	68.4
Nand-Nor Based	24.9	83.3	149	638
28 Standard full adder	13.2	62.5	106	247

TABLE VIII: Energy per operation and leakage for 1-bit full adders proposed in [6] and [14].

Reference	Energy Per Operation	Leakage	Vdd	Device
[6]	0.65 fJ	46.4 pA	300 mV	RVT
[14]	6.48 fJ	739 pA	300 mV	RVT/LVT

the effect of both PDP and leakage in different full adders, the PDP*Leakage metric has been invented and calculated in TABLE VII. As we can see, the amount of this indicator for the Xor based adder is much lower than others. TABLE VIII shows the amount of energy per addition and the leakage current for [6] and [14] in 28 nm FDSOI technology; these parameters have been compared with the result of this study. It has been done to see the effect of 22 nm versus 28 nm FDSOI technology on ultra low voltage design problems. Energy per operation and leakage current obtained for all full adders in this study are much lower than [6] and [14]. The amount of energy per addition for [6] is more than 12X of that for the Xor based adder in this study. Leakage is a key issue in ultra low voltage design. Since all full adders have been designed with HVT devices with reverse back bias voltage, leakage current for the five full adders in this study is much lower than the amount showed in TABLE VIII. The leakage current of the 1-bit adder in [6] is more than 3X that of the Xor based adder in this study.

V. Conclusion

Five reliable ultra low voltage full adders have been designed in a commercially available 22 nm FDSOI technology. To have a high functional yield, extended body bias voltages introduced in this technology have been used. All adders have been designed with HVT devices optimized for reverse back biasing. It is done to reduce the leakage of the full adders. They are functional at temperature range 27-50°C, which fits for implantable medical applications and the supply voltage varying from 140-160 mV. It is concluded that Xor based adder is the best option in this supply voltage range which yields the lowest delay, power, PDP, and PDP*Leakage.

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