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HVDC Transmission Using a Bipolar Configuration Composed of an LCC and MMC

Operating Characteristics of Skagerrak 3 and Skagerrak 4

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Problem Description

The thyristor-based Line-Commutated Converter (LCC) is a mature and trusted technology for HVDC transmission throughout the world. It is the technology of choice when transferring large amounts of power over long distances. Although the LCC results in low converter losses, large filters and shunt capacitors are necessary to compensate for the switching of the thyristors and the reactive power consumption of the converter. It also requires a relatively strong AC grid in order to achieve proper commutation of the thyristors. The Voltage Source Converter (VSC) adresses these issues with independent control of active and reactive power. It is based on controllable switches (IGBTs), and gives a great dynamic performance due to high switching frequency. As a result, filters are hardly necessary. The losses are still higher for the VSC compared to the LCC, due to the high switching frequency and the lower power capability of the IGBTs. A further development of the VSC is the Modular Multilevel Converter (MMC), which utilizes a multilevel topology instead of two and three levels. The result is a more dynamic response, less harmonic disturbance and lower losses.

By the end of 2014, two HVDC links between Norway and Denmark are to be combined. One of the interconnections is Skagerrak 3, a thyristor-based LCC installed in 1993 with a capacity of 440 MW at 350 kV. The other interconnection, named Skagerrak 4, utilizes the state-of-the-art MMC technology and has a capacity of 715 MW at 500 kV. They are to be connected in a bipolar manner with an intricate switching scheme in order to change the direction of the transmitted power. The LCC swaps the voltage polarity across the HVDC link in order to change the power direction, while the MMC is dependent on a constant voltage polarity, and changes the direction of the current.

Simulation models of the two Skagerrak links are to be made using the simulation software PSCAD. The LCC and MMC links will be based on already existing PSCAD models developed by Cigré and Manitoba HVDC research center in Canada, respectively. The LCC and the MMC operational behavior are first to be validated separately, before combining them in a bipolar configuration. Different fault situations are to be investigated, and will define if the MMC can help the LCC, or vice versa, during a fault. The interesting faults to be looked at are:

- AC fault –three-phase to ground
- AC fault –single-phase to ground
- DC fault on each HVDC link

Assignment given:	Trondheim 20.01.2014
Supervisor:	Tore Marvin Undeland
Co-supervisors:	Raymundo E. Torres-Olguin, NTNU
	Tarjei Midtsund and Øyvind Rui, Statnett

Preface

This thesis has taught me a great deal about HVDC power transmission and the available technologies found today. The strengths and weaknesses of the LCC and VSC topologies have thoroughly been investigated, together with the implemented control strategies. I am left with a much better understanding of the simulation program PSCAD and how to approach the construction of a simulation model.

I have had a lot of help along the way in order for this thesis to be realized. First, I would like to thank my supervisor, Tore M. Undeland, for helping me find an interesting topic that have increased my understanding of power systems and converter technology. His broad understanding of both the mature and state-of-the-art converter technologies has introduced me to new and interesting perspectives. Another person who has been very helpful is Raymundo E. Torres-Olguin. Raymundo has provided me with the PSCAD models and helped me achieve an understanding of the converter operations. He has also helped me with analyzing the system simulations and proofreading of the thesis. Finally, I would like to address a thank to my two co-supervisors in Statnett, Tarjei Midtsund and Øyvind Rui. They have encouraged me to chose an interesting topic for the thesis and provided me with input parameters for the simulation models.

Åsa H. Kjørholt
Tronheim, June 2014

Abstract

The operational properties of a bipolar configuration composed of a Line-Commutated Converter (LCC) and a Voltage Source Converter (VSC) in a multilevel topology (MMC) are investigated. Simulation models are made in the PSCAD software in order to represent the two bipolar HVDC-links between Norway and Denmark, named Skagerrak 3 and Skagerrak 4. The topology combines two fundamentally different converter technologies with an intricate switching scheme for the function of power reversal.

The objective of this thesis is to validate the three simulation models; a monopolar LCC model, a monopolar Modular Multilevel Converter (MMC) model, and an LCC-MMC model in a bipolar configuration. By investigating the interaction of the combined LCC model and MMC model, a better understanding of the challenges of the bipolar link is achieved. The steady state behaviors of the three systems are as expected based on the theory. The LCC consumes reactive power, and require reactive power compensation and filtering. When combined with the MMC, the MMC is able to provide the reactive power consumption by the system. There is an interaction between the MMC and the passive filters of the LCC, resulting in the need to redesign the filters in the bipolar configuration. Also, the DC voltages in the combined model are found to be divided somewhat unevenly between the HVDC-links.

When a three-phase to ground fault is applied to the inverter side of the models, the LCC suffer from failure of commutation. This is due to the reduction in the AC voltage, and is to be expected. A DC chopper is placed at the MMC DC-link and reduces the DC voltage overshoot significantly during the fault. When the LCC and MMC systems are combined, they operate in an independent manner, and as a result, no additional protection arrangements are necessary.

A single-phase to ground fault at the inverter side of the models, gives rise to harmonic disturbances due to the unbalance of the fault. The reduction in AC voltage results in failure of commutation at the LCC inverter side. The LCC and MMC systems are still almost unaffected by each other during the fault, and so no additional protection systems are required for the combined model.

Finally, a DC pole to ground fault is applied to the three simulation models. The LCC model does not recover from the fault, because of loss of controllability in the PI controllers. There are solutions for this problem, for example anti-windup PI controller. An interesting result is observed when the two models are combined

into the bipolar configuration. The MMC is able to support the LCC in such a way that it recovers. DC breakers are required for high voltage and current spikes during the DC fault at the MMC link. The LCC and MMC systems are no longer operating independently, and different protection strategies must be implemented when compared to the monopolar models.

Sammendrag

De operative egenskapene til en bipolar konfigurasjon bestående av en linje-kommuterende omformer (LCC) og en spenningskilde omformer (VSC) i en multilevel topologi er undersøkt. Simuleringsmodeller er laget i programvaren PSCAD for å representere den bipolare HVDC-forbindelsen mellom Norge og Danmark, kalt Skagerrak 3 og Skagerrak 4. Topologien kombinerer to fundamentalt forskjellige omformerteknologier med en intrikat bryterordning for å oppnå effekt-reversering.

Målet med denne avhandlingen er å validere de tre simuleringsmodellene; en LCC-modell i monopol, en multilevel-basert VSC omformer (MMC) i monopol, og en LCC-MMC-modell i en bipolar konfigurasjon. Ved å undersøke samspillet i den kombinerte LCC-MMC-modellen, er en bedre forståelse av utfordringene tilknyttet den bipolare koblingen oppnådd. Atferden ved stabil tilstand av de tre systemene er som forventet. LCC omformeren forbruker reaktiv effekt, og krever reaktiv effekt kompensasjon og filtrering. I kombinasjon med MMC-modellen, er MMC omformeren i stand til å forsyne systemet med reaktiv effekt. Et samspill mellom MMC omformeren og de passive filtrene i LCC systemet, resulterer i et behov for å beregne nye filtre i den bipolare konfigurasjonen. I tillegg viser likespenningen i den kombinerte modellen seg å være noe ujevnt fordelt mellom HVDC-koblingene.

Når en tre-fase til jordslutning er påført vekselretter-siden av modellene, lider LCC omformeren av kommuteringssvikt i vekselretteren. Dette er på grunn av reduksjon i AC-spenningen, og er en forventet reaksjon. En DC chopper er tilkoblet MMC DC-forbindelsen og reduserer DC spenningsoverskridelsen betydelig gjennom feilperioden. Når LCC og MMC-systemene kombineres, opererer de uavhengig av hverandre, og resulterer i at ingen ytterligere beskyttelsesforholdsregler er nødvendige.

En en-fase til jordslutning på vekselretter-siden av modellene, gir opphav til harmoniske forstyrrelser på grunn av ubalanse i feilen. Reduksjonen i vekselspenningen resulterer igjen i kommuteringssvikt i LCC vekselretteren. LCC-og MMC-systemene kommer seg gjennom feilen nesten upåvirket av hverandre, og resulterer i at ingen ekstra beskyttelsessystemer er nødvendig for den kombinerte modellen.

Til slutt er en DC-pol til jordslutning påført de tre simuleringsmodellene. Etter at feilen er klarert, klarer ikke LCC modellen å gjenopprette systemet tilbake til stabil tilstand, på grunn av tap av kontrollbarhet i PI-regulatorene. Det finnes løsninger på dette problem, for eksempel en anti-windup PI-regulator. Et interessant resultat observeres når modellene kombineres til den bipolare konfigurasjonen. MMC systemet er i stand til å støtte LCC systemet på en slik måte at det gjenvinner

kontrollen. DC brytere er nødvendig på grunn av høy vekst i spenning og strøm under DC-feil på MMC-forbindelsen. LCC-og MMC-systemet opererer ikke lenger uavhengig av hverandre og ulike beskyttelsesstrategier må iverksettes.

Contents

Abbreviations

CCSC	Circulating Current Suppression Control
CSC	Current Source Converter
CTL	Cascaded Two-Level
FACTS	Flexible AC Transmission System
HVDC	High Voltage Direct Current
IGBT	Insulated-Gate Bipolar Transistor
LCC	Line-Commutated Converter
MMC	Modular Multilevel Converter
PLL	Phase-Locked Loop
pu	per unit
PWM	Pulse Width Modulation
rms	root mean square
SK3	Skagerrak 3
SK4	Skagerrak 4
VDCL	Voltage Dependent Current Limiter
VSC	Voltage Source Converter

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Chapter 1

Introduction

1.1 Background

Over the past decades, Statnett has expanded the installation of High Voltage Direct Current (HVDC) subsea links to the continent. The interconnections increase security of power supply throughout the countries, and contribute greatly in terms of integrating more renewable energy into the grid. Norway mainly produces electricity from hydro power, which is a renewable and highly controllable energy resource. In combination with other intermittent renewable sources, for example wind and sun, hydro power is particularly valuable.

In 1976, two HVDC subsea cables named Skagerrak 1 and 2 (SK1 and SK2) were installed between Norway and Denmark, each with the capacity of 250 MW at 250 kV. The converters were built with thyristor valve technology and the cables connected in a bipolar scheme. A third Skagerrak link with a capacity of 440 MW at 350 kV went into operation in 1993. To reduce the earth current, SK1 and SK2 were converted into monopolar links and connected with opposite polarity to Skagerrak 3 (SK3). In 2008, the HVDC NorNed link between Norway and the Nederlands was installed, with the ability to transmit 700 MW. A fourth Skagerrak subsea cable is currently being installed between Norway and Denmark, and is scheduled to be operating by the end of 2014 with a rating of 715 MW at 500 kV. The converter technology chosen for SK4 is Voltage Source Converter (VSC) with a multilevel topology. At the moment, Statnett is planning two new HVDC subsea links to Germany and England, scheduled for 2018 and 2020, respectively [6].

This thesis will look at the remarkable connection of the SK3 and SK4 bipolar configuration, as illustrated in Figure 1.1. The topology combines two very different converter technologies with an intricate switching scheme. SK3 is based on Line-Commutated Converters (LCC) with thyristor valves. The LCC technology is mature and robust and provides efficient and reliable power transmission. SK4 is based on the fairly new Voltage Source Converter (VSC) technology. The first installation of a VSC converter in a real power network was achieved by ABB in 1997, when a HVDC transmission line between Hellsjön and Grängesberg in Sweden was

successfully installed. The VSC technology has proven many advantages compared to the classical LCC converters.

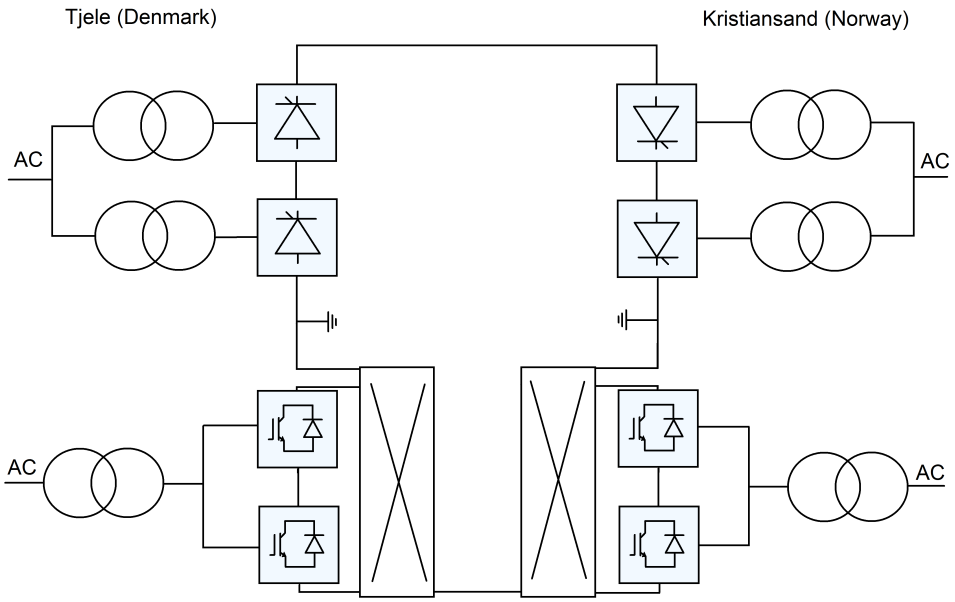


Figure 1.1: Bipolar configuration of SK3 and SK4

At the SK4 converters, the polarity of the DC cable is swapped between +500 kV to -500 kV according to the power direction. It will be possible to operate each pole in monopolar mode with ground return during maintenance or if a failure occurs.

1.2 The simulation models

Simulations of the Skagerrak 3 and 4 interconnections are performed in a simulation program called PSCAD/EMTDC. An LCC-HVDC Benchmark model created by Cigré is utilized for representing SK3. The LCC Benchmark model was introduced in 1991 as a first attempt to create a common reference for HVDC studies, especially related to control strategies and recovery performance [7]. The MMC PSCAD model utilized for simulating SK4 is developed by Manitoba HVDC research center in Canada.

1.3 Thesis remarks

The simulation models used in this thesis differ from the real SK3 and SK4 connections in some aspects. The Cigré Benchmark model and the MMC Manitoba model employed have not been altered to have the same control configurations as the real Skagerrak projects. This kind of information is difficult to get access to, and it creates much more complex problems if the systems are to be constructed

from the beginning. However, the operational concepts stay the same, as well as the system behavior.

Some of the system parameters of SK3 and SK4 are attracted from a previous Master thesis written by Alemayo Tadese at Aalborg University in 2010 [5]. The thesis was written in co-operation with Energinet in Denmark, who provided information on the HVDC systems.

The AC voltage level of the SK4 bus at Kristiansand has been upgraded to 400 kV. In this thesis, it is assumed that SK3 and SK4 share the same voltage bus of 300 kV at Kristiansand.

1.4 Thesis overview

The thesis is divided into three sections with a theory part, model parameter calculations, and simulation results.

- *Chapter 1* gives an introduction to the background of HVDC technology which has resulted in the Skagerrak connections. In addition, remarks about the model and thesis are pointed out.
- *Chapter 2* presents the LCC, VSC, and MMC technology. Their operating principles are introduced, together with system components and control strategies.
- In *Chapter 3* the Skagerrak 3 and Skagerrak 4 system parameter are found. These parameters are implemented in the PSCAD simulation models.
- *Chapter 4* presents the steady state simulations of the LCC monopolar model, the MMC monopolar model, and the LCC-MMC bipolar configuration.
- In *Chapter 5* a three-phase to ground fault is applied at the inverter side of the three simulation models.
- In *Chapter 6* a single-phase to ground fault is applied at the inverter side of the three simulation models.
- In *Chapter 7* a DC pole to ground fault is applied to the DC links of the three simulation models.
- Lastly, a *Conclusion* of the simulation results is made, accompanied by *Further work*.

Chapter 2

HVDC Overview

This chapter gives an overview of the main HVDC technologies available today. First, the characteristics of the LCC, VSC, and MMC converter technologies are presented. Then, a brief overview of the HVDC configurations utilized in todays networks are presented. Finally, the operating and control principles of the LCC, VSC, and MMC are introduced.

2.1 HVDC technology

High Voltage Direct Current (HVDC) transmission is a safe and efficient technology designed to deliver large amounts of electrical power over long distances with minimal losses and at low costs. HVDC links require expensive converters and filters at both terminal stations, but the overall savings with fewer and thinner transmission lines and lower losses make it advantageous. HVDC technology can synchronize AC power networks that are otherwise incompatible. Today there are more than 100 HVDC installations in the world, and the ratings are in the 100–10,000 MW range [8]. The core component of the HVDC system is the power converter that connects the DC and AC systems together. The conversion from AC to DC, and vice versa, is achieved through electronic switches.

There are two main topologies of electronic converters for HVDC transmission available today; Line-Commutated Converters (LCC) and Voltage Source Converters (VSC). The classical topology is the LCC with thyristor valves from the 1970's, which is present in most of the HVDC systems in operation today. The VSC technology was first utilized in a real network by ABB in 1997, when a HVDC transmission line between Hellsjön and Grängesberg in Sweden was successfully installed [9]. The technology has proven efficient with its many advantages compared to LCC. A further development of the VSC technology, with a multilevel topology, is the Modular Multilevel Converter (MMC). It was first successfully installed in 2010 with the Trans Bay Cable project in San Francisco where Siemens delivered HVDC PLUS converters [10]. ABB has upgraded its HVDC Light converter to the fourth generation, an MMC variant called Cascaded Two-Level converter (CTL) [11]. Most

HVDC converters are bidirectional and can function in either rectification mode (AC to DC) or inversion mode (DC to AC). This property makes bidirectional power flow possible.

Most HVDC schemes in operation today employ line-commutated thyristor valve converters, and it is still being installed for bulk power HVDC transmission with ranges up to several thousand MW. The LCC is a Current Source Converter (CSC) because the DC current is kept constant by using a large inductor, thus forming a current source at the DC side. The technology is mature and robust and provides efficient and reliable power transmission for many applications. Flexible AC Transmission System (FACTS) controllers are used combined with the LCC in order to enhance controllability and increase power transfer capability. LCCs have some technical restrictions. The commutation of the thyristors is carried out by the AC system voltage, and require proper conditions in the AC network, such as minimum short-circuit power. In order to avoid commutation failure, a rotational device such as a generator or a synchronous compensator is therefore necessary on the inverter side to provide a commutation voltage for the thyristor valves. In addition, capacitor banks are required at both rectifier and inverter side to compensate for the reactive power consumption of the converter. The LCC generates low-order harmonics, and suppression requires large filters [2]. For power reversal in the LCC-HVDC link, the voltage polarity is swapped. The main advantages of LCC converters lies in the low conversion losses, and the maturity of the technology. More details about the operating principles of the LCC are described in section 2.2.

Voltage Source Converters (VSC) are based on controllable switches, mainly Insulated-Gate Bipolar Transistors (IGBTs). IGBTs are self-commutating with two degrees of freedom, and can therefore be both switched ON and OFF. This property presents the advantage of switching many times per cycle and improving the harmonic distortion of the output signal. The result is reduced space requirements as less harmonic filtering is necessary. The VSC topology enables rapid and independent control of active and reactive power in all four operating quadrants. Accordingly, no reactive compensation with switch yards and capacitor banks is necessary. Challenges regarding VSC technology are high losses due to high frequency switching and higher on-state losses of the IGBTs compared to thyristors. To achieve high blocking voltage, the IGBTs are connected in series, and require sophisticated gate drive circuits to switch simultaneously. VSC converters do not require any short-circuit power in the connected AC grid. This results in the ability of a black start and to feed power into an AC network consisting of only passive loads, by building up a 3-phase AC voltage using the transmitted DC voltage [12]. This is advantageous for weak networks or remote locations such as islands, mining districts, and offshore platforms that can be supplied with power from the main grid. Power reversal is achieved by changing the direction of the current, while the voltage polarity remains unaffected. This makes the VSC links more suited for multi-terminal HVDC systems.

There are three main VSC designs; two-, three-, and multi-level converters. A two-level structure can switch between two discrete voltage levels, $V_d/2$ and $-V_d/2$, while a three-level has the additional opportunity to switch between a neutral point and improve the harmonic performance of the converter. A Pulse-Width Modulation

(PWM) switching scheme is applied to the switches in order to create the right output signal. The multilevel converter topology can switch between multiple voltage levels. More details about the operating principles of the VSC are described in section 2.3.

Table 2.1 presents the different aspects between the line-commtated converter and the voltage source converter.

LCC	VSC
Mature technology	Rapid growth in technology
High power transmission	Medium power transmission
Thyristors	IGBTs and anti-parallel diodes
Commutation failure	No commutation failure
Lower losses (0.8% per converter)	Losses reducing (1-2%)
Requires a strong AC grid	Helps the AC grid
Consume reactive power	Provide and regulate reactive power
Low-order harmonics	High-order harmonics
Large filters	Small or no filters
Power flow changes with voltage polarity	Power changes with current direction
Paper-insulated cable	Paper-insulated and cross-linked polyethylene

Table 2.1: Comparison of the LCC and VSC HVDC technology

The Modular Multilevel Converter (MMC) is an advancement of the VSC, and is able to achieve very good characteristics. MMC is constructed in a similar way as a two-level converter with three phase units, each comprising of two converter arms, one positive and one negative. Each arm consists of a reactor and a module. While in a regular two-level converter each valve or module consist of a large number of series-connected switches, the MMC modules are made up of a number of identical and independent submodules or sometimes called cells. Each submodule is constructed in a half-bridge structure and having its own storage capacitor. The series-connected submodules, typically 30-100 submodules per phase arm, are switched through several intermediate voltage levels. They act as independent two-level converters, generating either 0 V or the voltage across the capacitor, V_C. The result is a stepped output voltage close to a sinusoidal waveform [3].

Because of the many submodules, the converter has many operating levels. Consequently, the harmonic performance is excellent, and is able to eliminate the low-order harmonics that usually require large filters. The rate of dv/dt across the valves are reduced as only a fraction of the DC voltage is switched at a time. Each cell is switched at a low switching frequency, typically about 150 Hz. If there are N submodules per arm, the effective switching frequency per phase leg becomes $2N150$

Hz. This frequency is about 10 times of a regular 2-level VSC, which indicates that the dynamic response of an MMC converter is excellent [11]. As a result of the low switching frequency per cell, the switching losses of an MMC are significantly reduced compared to a two-level VSC. Low harmonic distortion reduces the harmonic losses in the reactors. Consequently, the converter losses of an MMC are as low as 1% [11]. More details about the operation of the MMC are found in section 2.4.

2.1.1 HVDC system configurations

There are multiple HVDC configurations that can be chosen when designing new HVDC links. Factors like location, power and voltage capability of the link, chosen cable technology and so on, are used to deside which configuration to use.

Monopolar

A monopolar link consists of a single conductor and a return path through the ground or the sea by the use of electrodes. Many subsea cables are installed as a monopolar scheme to reduce costs. However, the use of return path through the sea or earth leads to questions of corrosion on metallic objects and other environmental concerns [2]. In some areas, conditions are not conductive enough for earth or sea return, such as fresh water cable crossings, or areas with high earth resistivity. In such cases, a metallic neutral- or low-voltage cable is used for the return path, and the DC circuit uses a simple local ground connection for potential reference [13].

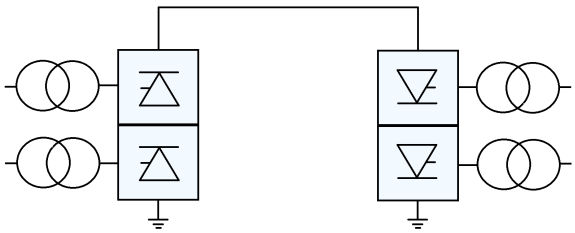


Figure 2.1: Monopolar configuration

Bipolar

A bipolar HVDC system configuration consists of two poles, one with positive polarity and one with negative polarity, each with their neutral points grounded. In steady state, the current flows in a loop, causing no current to go through the grounded return, and creating no corrosion concerns. In case of a fault on one of the two poles, the other can function as a monopolar link with ground return. The amount of transmitted power in a bipolar configuration is double that of a monopolar system. Reversal of the power flow can be controlled by changing the polarities of the two poles [2]. Skagerrak 3 and Skagerrak 4 are connected together in a bipolar configuration, but has an interesting twist to the way they are operated, due to the

two different technologies. Hence, a switching scheme at the VSC pole has to be applied in order for constant current direction in the two links.

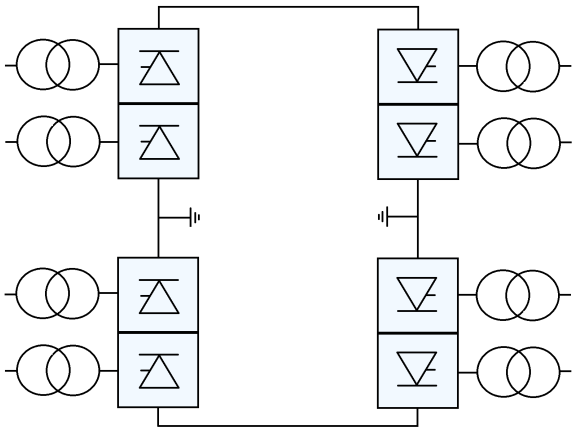


Figure 2.2: Bipolar configuration

Back-to-back

A back-to-back HVDC system is used as an interconnection of asynchronous AC networks, or between two systems with different frequencies. In such systems, the power transfer is limited to the relative capacities of the connected AC systems [13]. The two converters are located close to each other, often at the same station.

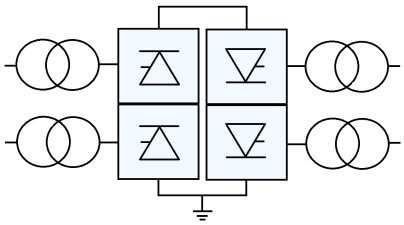


Figure 2.3: Back-to-back configuration

Multi-terminal

A multiterminal system is referred to as a HVDC system consisting of three or more converter stations, as illustrated in Figure 2.4. The objective of the multiterminal configuration is to save costs and conversion losses, while providing enhanced reliability and functionality. One of the potentials for multiterminal HVDC activity is offshore interconnections of windfarms or oil and gas rigs.

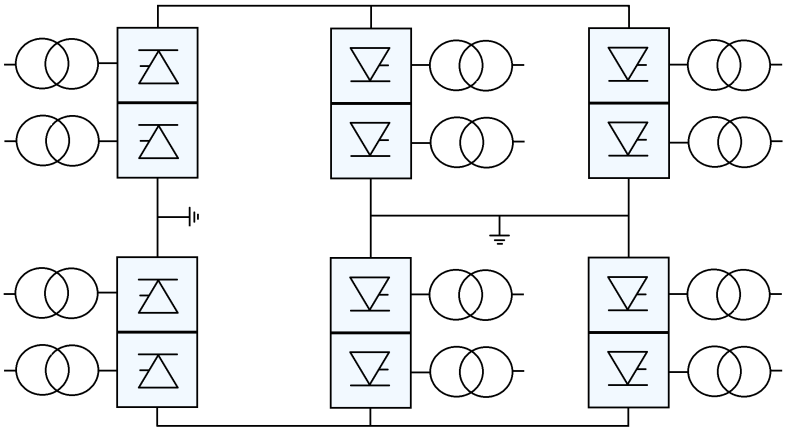


Figure 2.4: Multiterminal configuration

2.1.2 Network fault statistics

A fault is defined as a condition where a system unit has lacking or reduced ability to perform its operational duty. A statistical report from 2011 made by Statnett [14], presents the total number of registered faults in Norway in the 33-420 kV grid. In 2011, a total of 938 faults occured, of which 49.5 % were faults on the power transmission lines. Of these faults, 330 were temporary and 140 permanent. The yearly weather conditions are responsible for many of the faults, and cause fluctuations in the number of faults per year.

2.1.3 Short circuit level and short circuit ratio

The Short Circuit Level (SCL) of the AC system is a measure of the current that can be delivered into a solid three-phase fault at a particular bus in an AC system, assuming nominal driving voltage [15].This relationship is presented in Eq. 2.1.

$$SCL = \frac{E_{ac}^2}{Z_{ac}} \tag{2.1}$$

Where E_{ac} is the AC voltage of the system and Z_{ac} is the AC system impedance. The Short Circuit Ratio (SCR), which is an expression of the relationship between the SCL of the AC system bus and the quantity of HVDC scheme power, can further be calculated as in Eq 2.2.

$$\begin{aligned} SCR &= \frac{SCL\,[MVA]}{P_d\,[MW]} \\ &= \frac{E_{ac}^2}{P_d \cdot Z_{ac}} \end{aligned} \tag{2.2}$$

Where SCL is the short circuit level and P_d is the DC operating power. A strong AC system is defined to have an SCR greater than 3, while a weak AC system is defined to have a SCR between 2 and 3 [15]. If the SCR becomes less than 2, commutation failure in the thyristors may occur frequently. During the winter, the SCR in Kristiansand and Tjele is approximately 7.5, but during summer this ratio can reduce to less than 2. If this occurs, the import capacity of the LCC connections has to be reduced [16].

2.2 Line-commutated converter operation

2.2.1 LCC operating principles

Thyristor

The main component of an LCC converter is the thyristor switch. It is very suitable for LCC-HVDC systems because of its large voltage blocking capability and current conduction capability, low switching losses, and robustness [1]. The thyristor behaves like a controllable diode, and current is conducted from the anode to the cathode when the thyristor is positively biased (the anode has a higher potential with respect to the cathode), and when a small current signal is supplied to the gate terminal. It will then continue to conduct until the current drops to zero. In order to achieve the desired DC voltage rating, the thyristors are stacked together in series. It is generally necessary to connect an RC snubber circuit across the power semiconductor device, in order to protect it from system transients, dv/dt, and high recovery voltages [2].

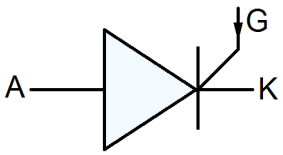


Figure 2.5: Thyristor circuit symbol

The firing angle, α, of the thyristor is defined from the zero crossover point of the phase voltage, which is the earliest point when a thyristor can assume conduction, and until a gate signal is supplied. The extinction angle, γ, is the angle which is necessary for the thyristor to recover its ability to withstand positive voltage after conducting current.

3-phase converter

Conventional LCC converters require a synchronous voltage source in order to ensure proper commutation of the thyristor valves. Commutation is the transfer of current from one phase to another in a synchronized firing sequence of the thyristor valves [13]. The basic building block for three-phase conversion is the 6-pulse converter configuration illustrated in Figure 2.6, also referred to as a Graetz bridge. When conducting, the current I_d will flow through one of the thyristors of the top group

(T_1, T_3, and T_5), and one of the bottom group thyristors (T_2, T_4, and T_6) [1]. The commutation from one thyristor to the next occur naturally, as they are 120° apart.

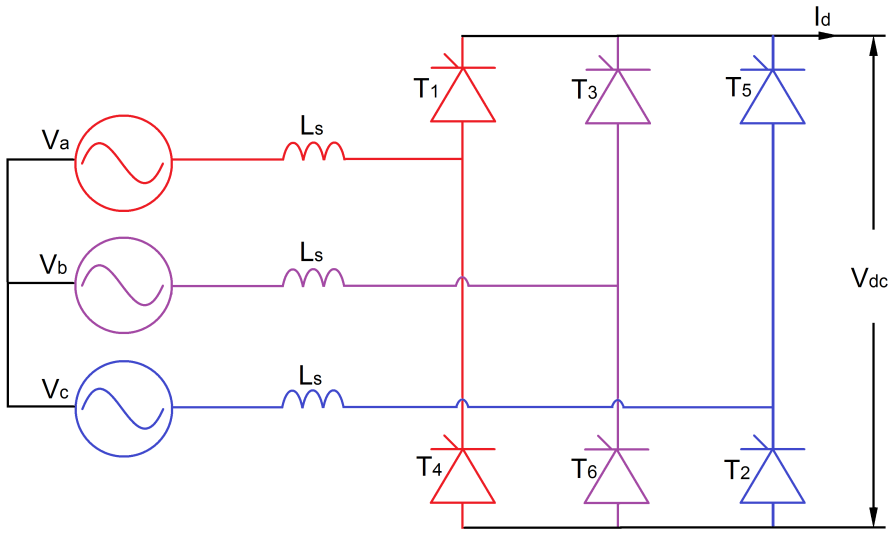


Figure 2.6: Basic thyristor converter circuit with 6-pulse Graetz bridge

The converter operates at a lagging power factor, because the firing of the converter has to be delayed relative to the voltage crossing in order to control the DC voltage [2]. By adjusting the firing angle, α, the average value of the DC voltage at the terminals can be controlled through phase control. The relationship can be seen in Eq. 2.3, which is the value of the average DC voltage with respect to the applied AC voltage and α for a converter [1]. The desired DC voltage can therefore be achieved in two ways: controlling the firing angle or the magnitude of the applied AC voltage.

$$V_{dc} = \frac{3\sqrt{2}}{\pi} V_{LL} \cos\alpha - \frac{3\omega L_s}{\pi} I_d \tag{2.3}$$

Assuming $L_s = 0$, the terminal voltage is proportional to $\cos\alpha$. At $\alpha = 0$, the thyristor can be considered to be operating as a diode. When $\alpha = 90°$, the DC voltage reaches zero, and with further increase in the angle, the DC voltage becomes negative. At this point, the converter is in inverter mode as illustrated in Figure 2.7, and the direction of the power flow is reversed. As the thyristors only conduct current in one direction, it is the voltage polarity that changes when the power direction is reversed.

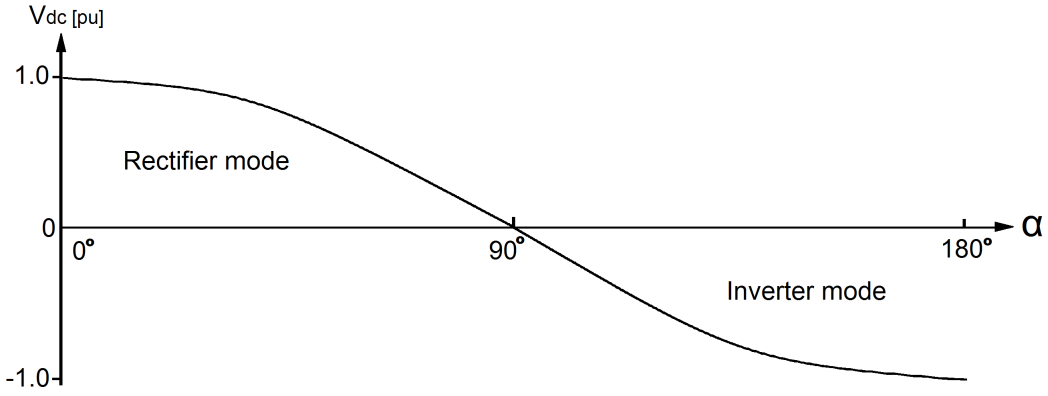


Figure 2.7: Converter mode as a function of the firing angle α [1]

In reality, the commutation of direct current requires a certain amount of time, due to leakage inductance of the converter transformer. It only permits a limited change of current, di/dt. As a result, the releasing and receiving phases are carrying current simultaneously in a duration called commutation overlap, and it is defined with the overlap angle, μ. During the commutation overlap, the line-to-line voltage is shorted and the energy in the system is absorbed by the AC inductances, L_s, until the current transfer is completed [2]. Figure 2.8 illustrates the commutation overlap during rectifier operation. As indicated in Eq. 2.3, the size of the inductors reduces the overall DC voltage output.

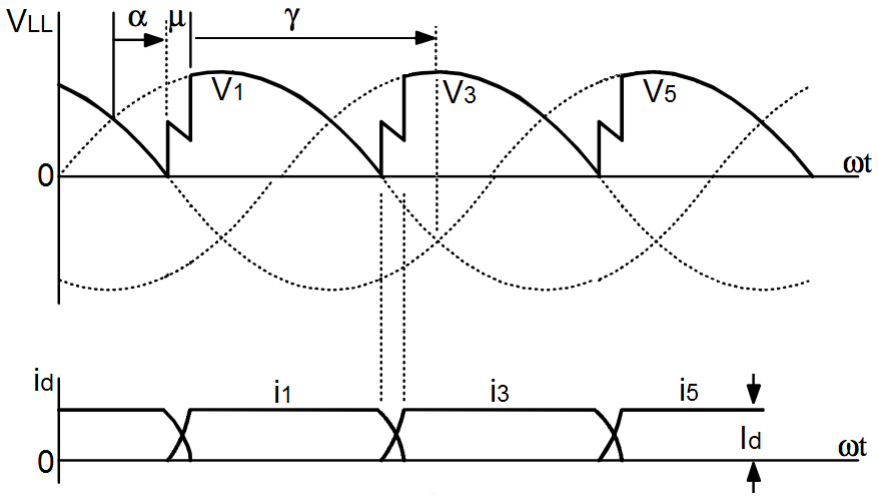


Figure 2.8: Commutation on rectifier side [2]

During inverter operation, presented in Figure 2.9, the commutation process has to end before the voltage intersection, in order for the thyristor to regain its blocking capability. As a result, the commutation overlap angle is very significant at the inverter side, as it determines how large the firing angle α can be increased. This minimum advance limit angle for safe commutation is called β [2], and is related

to μ and the extinction angle, γ, by Eq. 2.4. The relationship between α and β is given by Eq. 2.5.

$$\beta = \mu + \gamma \tag{2.4}$$

$$\alpha = 180° - (\mu + \gamma) = 180° - \beta \tag{2.5}$$

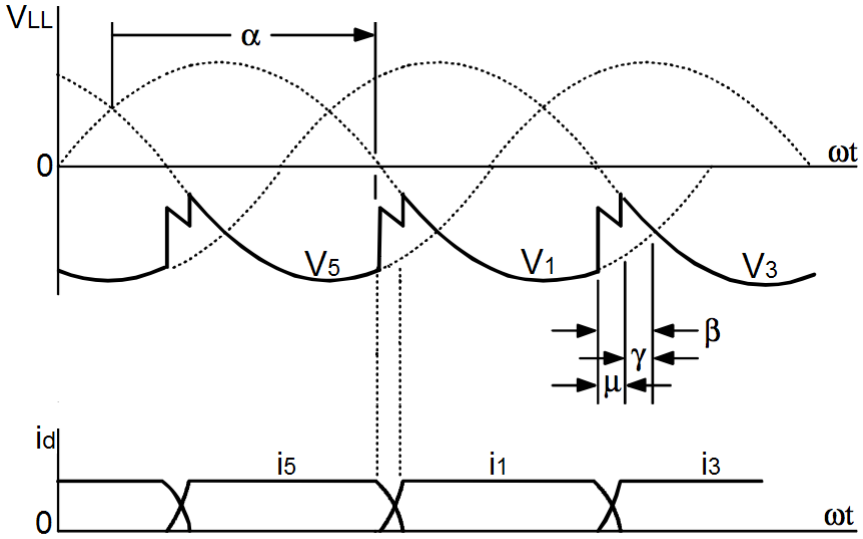


Figure 2.9: Commutation on inverter side [2]

An ideal thyristor should stop conducting at the instant when the current reaches zero, and thereafter recover its full ability to block voltages and dv/dt of either polarity. However, real thyristors will continue to conduct for a short period after zero current, resulting in a period of reverse recovery stored charge, Q_{rr} [15].

Failure of commutation occurs when the commutation of current from one valve to another has not been completed before the commutating voltage reverses across the ongoing valve. Only after the reverse recovery, the device is capable of blocking a forward voltage without going into its on state [1]. In order for the thyristors to commutate successfully, a minimum turn-off time (t_{off}) is required. t_{off} is defined from the time when the current conducted in the forward-biased thyristor reaches zero, and until the thyristor recovers its ability to block the forward-biased voltage again. The turn-off time corresponds to the extinction angle by $\gamma = \omega t_{off}$ [2]. Commutation failure is therefore primarily an issue at the inverter side of the converter.

It is very important to avoid failure of commutation, as it may result in high short circuit currents and damage the converter components. The sensitivity of the inverter to commutation failure depends on the strength of the AC network and the control system. The reason for most commutation failures is a too small extinction angle during system disturbance. As a result, there is a minimum extinction angle

(γ_{min}) consistent with safe commutation of the thyristor valves. The AC system fault affects the commutation margin by voltage magnitude reduction, increased overlap due to higher dc current, and phase angle shifts. One solution in order to mitigate the commutation failure is to have a large commutation margin during normal operation. But a large commutation margin also leads to higher reactive power consumption, which can be expensive. Another solution is to advance the firing instant immediately after the control system detects an ac system disturbance. The problem for this solution is that the control system is often too slow to react to such a disturbance [17].

2.2.2 Control strategy

In the conventional control strategy of the line-commutated converter, the rectifier and inverter have different controlling responsibilities. The rectifier is normally operated in DC current control mode, and is responsible for the DC power transmitted. A reference current limit is supplied from the inverter to the rectifier side by Constant Current Control (CCC) technique with Voltage Dependent Current Limiter (VDCL) control. The reference current depends on the DC voltage available at the inverter side in case of a fault or a decline in load demand, and will only return to its original current order level when the DC voltage has recovered sufficiently. In order to keep the DC current at the rectifier at an ordered value, the firing angle α is regulated in response to the operating conditions, as can be seen in Figure 2.10. As the firing angle can be adjusted cycle-by-cycle, very fast control responses can be achieved with firing angle control, and an output of any value, within the operating range of the converter, can be achieved [15].

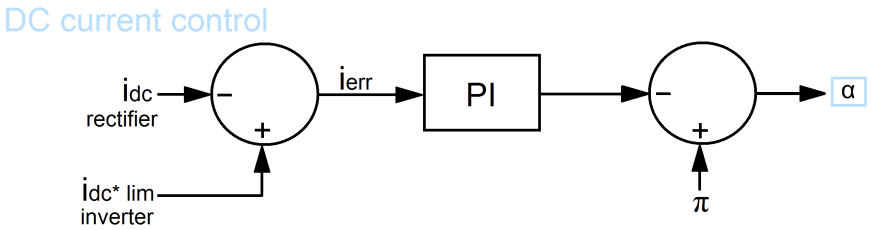


Figure 2.10: Rectifier DC current control

As the primary parameter at the inverter side is the extinction angle γ, it is normally the main operation mode of the inverter. The firing instants of the valves will be controlled in such a manner to maintain the inverter extinction angle at an ordered constant value in order to avoid commutation failure. A secondary mode of operation is the control of the DC current in the event where the rectifier is unable to deliver the required DC current. When utilizing DC voltage control, the operating DC voltage is maintained at a target value while the extinction angle γ is allowed to vary as the power transmitted varies [15]. The different control strategies at the inverter side are presented in Figure 2.11.

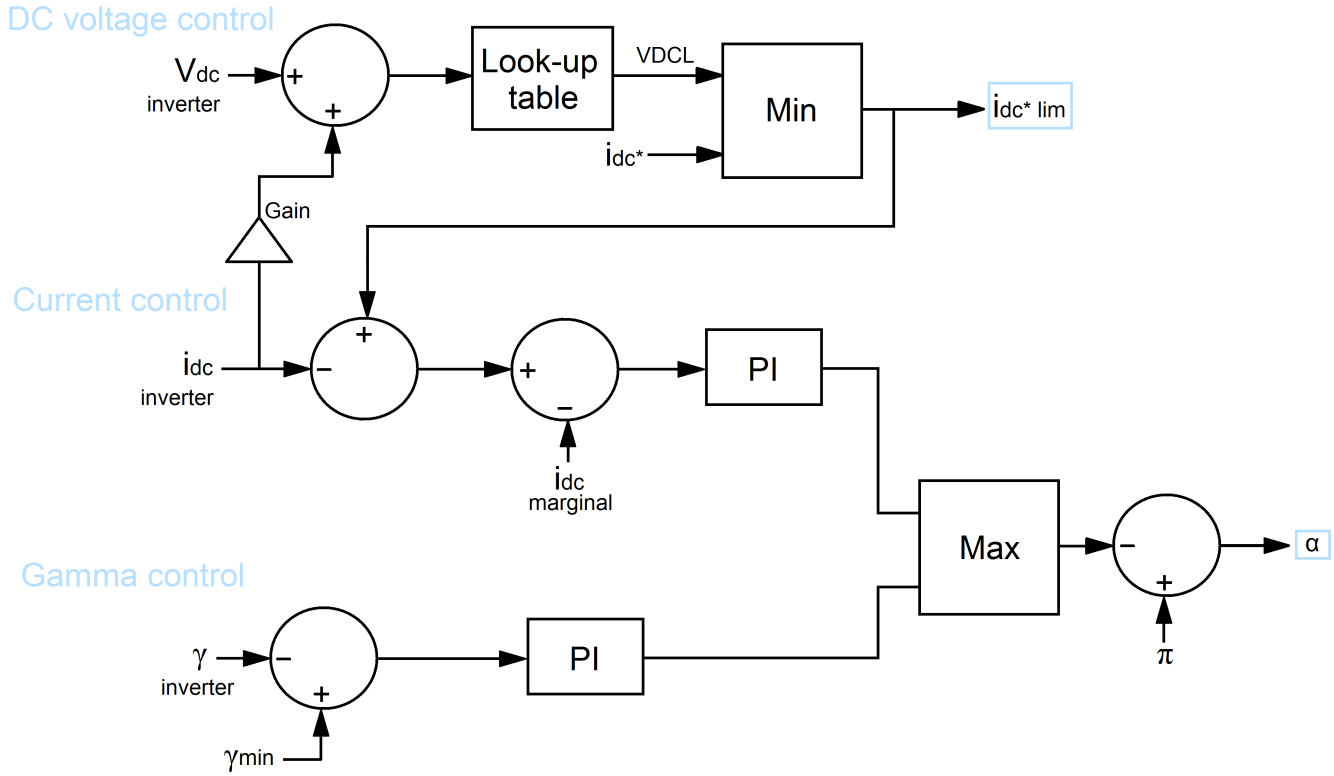


Figure 2.11: Inverter current and gamma control and VDCL

The rectifier and inverter mode must have controllers in operation that are opposite of each other. If not, the operational intersection point (OP) will not be created, and it becomes impossible to perform stable control [2]. The different rectifier and inverter operating strategies are illustrated in Figure 2.12.

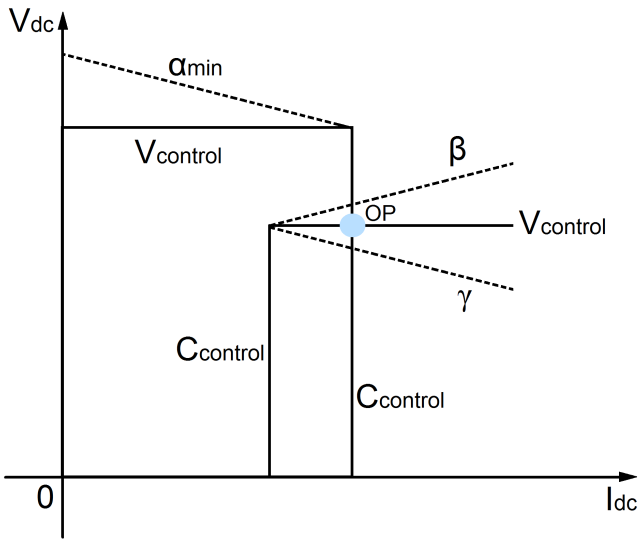


Figure 2.12: Control strategies of an LCC [2]

2.2.3 Harmonics and filtering

Harmonics within a power system are defined as the modulation of the voltage or current as an integer multiple of the fundamental frequency [15]. Excessive current harmonics result in voltage distortion, additional losses, overheating, and harmonic interference, and must therefore be limited. The 12-pulse LCC converter operates as a source of current harmonics on the AC side, and as a source of voltage harmonics on the DC side. Harmonic filtering is therefore required on the AC side, with the function of limiting the current distortion caused by the converter harmonics, and compensate for the reactive power absorbed by the converter due to the lagging operation. The presence of harmonic distortion is an issue of power quality and can have serious consequences on connected equipment.

The two 6-pulse bridges that make up the 12-pulse converter are connected to a Y-Y and a Y-Δ transformer, respectively. As a result, the AC voltage supplied to each bridge has a 30°C phase shift, as illustrated in Figure 2.13. Each bridge has a ripple component that is six times the fundamental frequency, and so connecting the bridges in series, the ripple component is reduced.

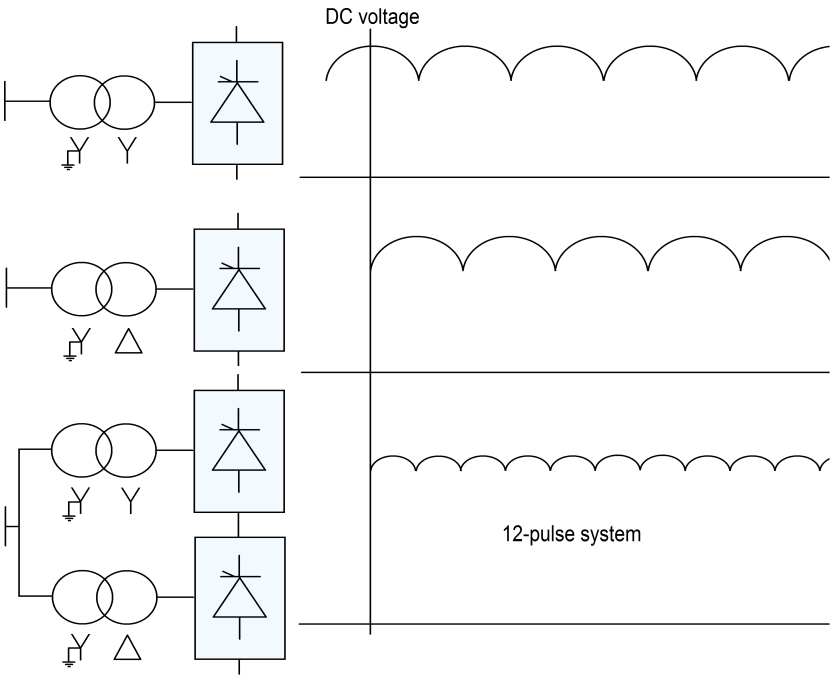


Figure 2.13: DC voltage waveform with harmonic disturbance [2]

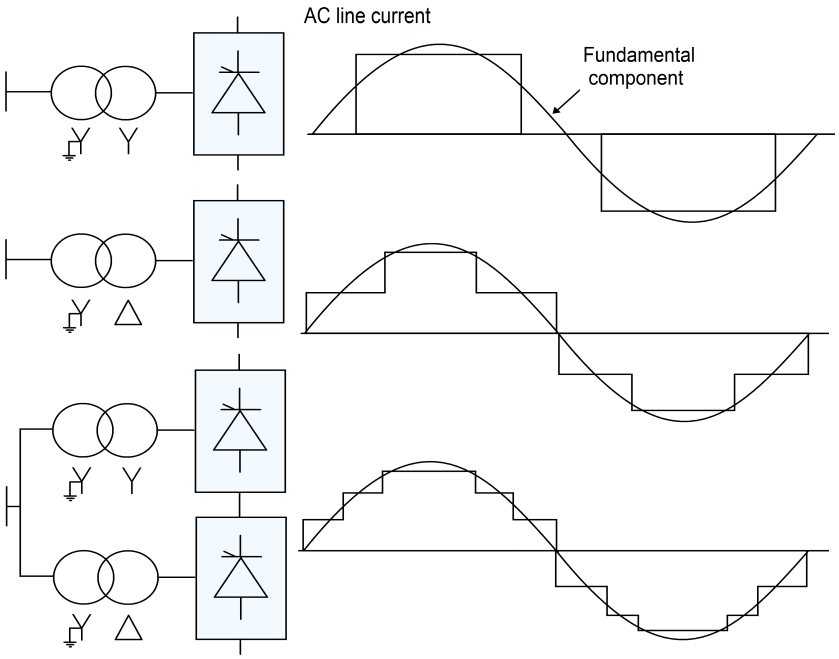


Figure 2.14: AC current waveform with harmonic disturbance [2]

Figure 2.14 illustrates the AC phase current supplied to the converter after leaving the transformer. The current has fundamental and harmonic components in its waveform. The waveform of the Y-Y connected transformer is rectangular, while more stepwise for the Y-Δ transformer. The total AC current of the 12-pulse converter is the sum of the two 6-pulse currents [2], and a clear reduction in harmonic distortion can be observed.

Characteristic harmonics are related to the pulse number of the converter, and are int the order of $k \pm 1$ for the AC side and in the order of k for the DC side, where k is any integer. This results in harmonics on the AC side in the order of 11th, 13th, 23rd, 25th and so on, and harmonics in the order of 12th, 24th on the DC side. Tuned filters or band-pass filters are utilized to tune out one or several harmonic frequencies. A resistor, a capacitor and an inductor in series often construct the filter, or the resistor can be in parallel with the inductor. These filters are used in order to remove the 11th and 13th harmonics. High-pass filters offer low impedance over a broad band of frequencies, and can be used to filter out the 12th and 24th harmonics. High-pass filters always include a resistor in parallel with an inductor, which produces a damped characteristic at frequencies above the tuning frequency [15]. More information about filter calculations are found in Appendix C.

2.2.4 DC smoothing reactor

LCC-HVDC schemes require the use of DC reactors at both ends, in order to eliminate discontinuous current under steady-state operation, limit commutation failure currents, and limit the magnitude of transient current surges due to lightning strikes. The reactor is a part of the DC harmonic filtering on DC overhead lines or

cables [15]. As a rule of thumb, the smoothing reactor value is usually chosen to be approximately 0.15 pu of the system base impedance [18].

2.3 Voltage source converter operation

2.3.1 Half-bridge converter

The fundamental operation of a VSC-based HVDC converter implies the presence of a voltage source on the DC side. The voltage source maintains a prescribed voltage across its terminals regardless of the magnitude or polarity of the current flowing through the converter [3]. Figure 2.15 illustrates the basic operating principles of a single phase, two-level VSC, also referred to as a half-bridge. The half-bridge consists of an upper and lower switching cell. Each cell is composed of a fully controllable, unidirectional switch (normally an IGBT) connected to an anti-parallel diode. Hence, the bridge voltage only has one polarity, while the current can flow through the bridge in both directions. The DC system maintains the net voltage by split capacitors, and V_t is the AC terminal voltage. The converter is called two-level because the two IGBT switches are turned ON and OFF in an opposite manner, making the output voltage equal the discrete capacitor value of either $V_{dc}/2$ or $-V_{dc}/2$, as can be seen in Figure 2.15 next to the half-bridge. The IGBTs can be switched ON and OFF in a desired pattern using a Pulse Width Modulation (PWM) control scheme. However, it is important that the switches are not simultaneously conducting, as it can lead to short circuiting of the DC capacitors and can cause severe damage to the converter equipment. In order to avoid this outcome, a small blanking period of a few microseconds is required. The current path will go through the freewheeling diodes during this period [3].

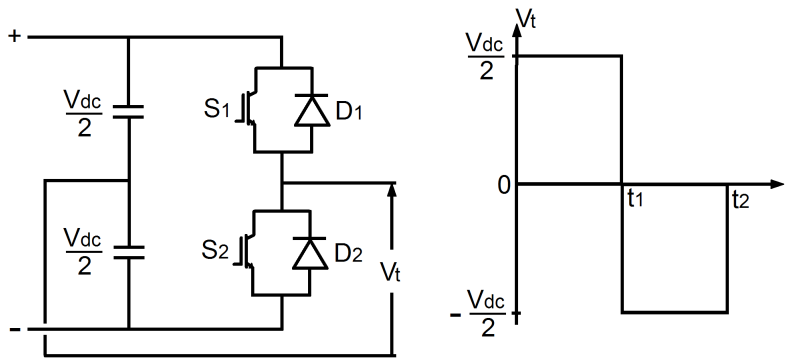


Figure 2.15: Two-level basic operation [3]

The switching steps of the half-bridge example are listed below.

- *t = 0, S_1 ON, S_2 OFF:* The AC terminal is connected to the positive terminal of the DC capacitors through the switch (S_1) and freewheeling diode (D_1) pair with respect to the midpoint potential. The voltage output is the same as

across the upper capacitor, $V_{dc}/2$, and the current can flow through the pair in either direction.

- *Blanking time, $t = t_1$, S_1 OFF, S_2 OFF:* When the current goes from the AC terminal to the positive terminal of the DC capacitor through the D_1, the voltage remains at $V_{dc}/2$. During the blanking time, the AC terminal voltage polarity depends on the current direction in the switch pair to be turned off. The polarity remains therefore unchanged even though the upper switch S_1 is turned off.

- *$t = t_1$, S_1 OFF, S_2 ON:* The AC terminal is connected to the negative terminal of the DC capacitors through the switch (S_2) and freewheeling diode (D_2) pair with respect to the midpoint potential. The voltage output is the same as across the lower capacitor, $-V_{dc}/2$, and the current can flow through the pair in either direction.

Insulated-gate bipolar transistor and anti-parallel diode

The Insulated-Gate Bipolar Transistor (IGBT) switch is an important building block in the VSC converter with its controllable gate, providing the device with two degrees of freedom, and hence, the ability to turn both ON and OFF. The IGBT is a unidirectional switch, and can only conduct if the current flows from the collector (C) to the emitter (E). The operation of the IGBT is based on an internal interaction between the simple gate-drive of the MOSFET, and the low on-state conduction losses of the Bipolar Junction Transistor (BJT). It is a rugged switch with easy gate controllability, superior switching speed, and a wide Safe Operating Area (SOA). The IGBT has low driving power and require only a simple drive circuit in order to operate. Although the IGBT present excellent switching characteristics, a converter based on IGBTs still suffer from higher losses than a thyristor based converter.

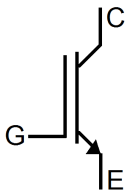


Figure 2.16: IGBT circuit symbol

In order to achieve the high voltage levels necessary to increase power capacity and reduce losses, the converter valves consist of many series-connected IGBTs. Similarly, to match the high current ratings, the switches are connected in parallel. This has lead to the release of several IGBT devices housed in "hockey-puck" packages, which are easily stacked.

The anti-parallel diodes in the VSC combine to form an uncontrolled rectifier bridge. The diodes have to be designed to be able to withstand the stresses created by faults in the system. Voltage source converters are defenseless against DC faults, as their anti-parallel diodes conduct as rectifier bridges to feed the fault. The IGBTs are helplessly by-passed, unable to extinguish the fault current [19]. The diodes must also be able to withstand high inrush currents.

2.3.2 Pulse width modulation and switching frequency

Pulse Width Modulation (PWM) is a method used to generate the switching signals supplied to the gates of the IGBTs in the inverter. The simplest version of the PWM is seen in Figure 2.17, where a sinusoidal control signal at a desired frequency is compared with a triangular waveform in order to produce a sinusoidal output voltage waveform.

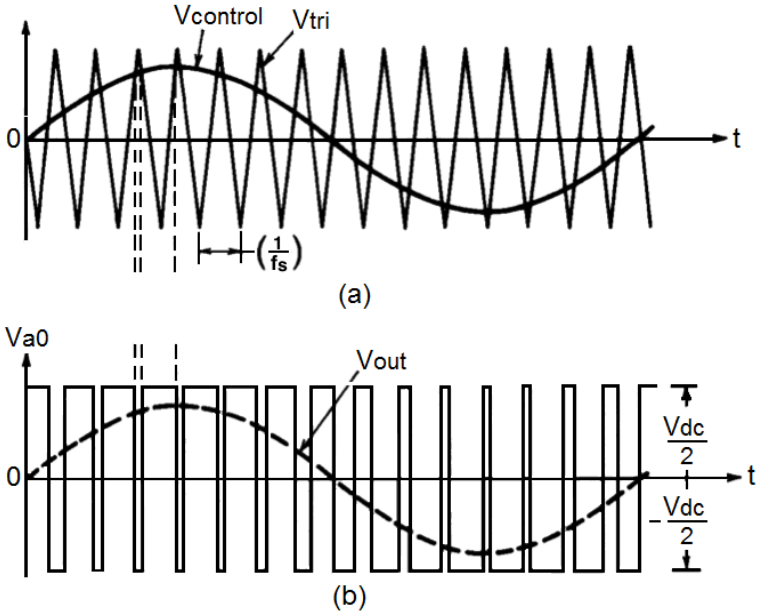


Figure 2.17: PWM operation [1]

The frequency of the triangular waveform establishes the switching frequency of the converter, and is usually kept constant along with its amplitude [1]. The amplitude modulation ratio m_a is defined in Eq. 2.6, where $\hat{V}_{control}$ is the peak value of the control signal, and $\hat{V}_{tri}$ is the amplitude of the triangular signal.

$$m_a = \frac{\hat{V}_{control}}{\hat{V}_{tri}} \tag{2.6}$$

$m_a < 1.0$ is referred to as the linear range, while $m_a > 1.0$ is referred to as overmodulation. Operation in overmodulation mode is not desired, as it reduces the controllability of the switches. m_f from Eq. 2.7 is the frequency modulation ratio, where f_s is the switching frequency established by the frequency of the triangular waveform, and f_1 is the fundamental frequency of the output voltage, established by the frequency of the control signal, $v_{control}$ [1].

$$m_f = \frac{f_s}{f_1} \tag{2.7}$$

The resulting duty cycle of the switches seen in Figure 2.17(b) is created by comparing the two signals in (a). The two output voltages are generated by Eq. 2.8 with the same configuration as the two-level converter in Figure 2.15, and are independent of the current direction.

$$\begin{aligned} v_{control} > v_{tri} \qquad S_1\, is\, ON \qquad v_{A0} = \frac{1}{2}V_d \\ v_{control} < v_{tri} \qquad S_2\, is\, ON \qquad v_{A0} = -\frac{1}{2}V_d \end{aligned} \tag{2.8}$$

Where $v_{control}$ is the control voltage with fundamental frequency and v_{tri} is the triangular signal. The peak amplitude of the output voltage v_{out} is $m_a\frac{1}{2}V_d$, assuming $m_a < 1.0$.

The duty cycle phase angle related to the reference signal is an important controllable variable for active power control. If the converter is connected to an active AC system, the duty cycle is synchronous with the AC system, and if the converter is connected to a passive system, the duty cycle frequency has to be controlled independently.

An important factor in the modulation principle is the frequency modulation ratio m_f, defined in Eq. 2.7. It determines the harmonic spectrum for a certain degree of control and for a given modulation pattern. A large m_f will reduce the low-order harmonics significantly, but will generate high switching losses due to the high modulation frequency. The harmonics in the output voltage waveform of the inverter appear therefore as sidebands centered around the switching frequency and its multiples (m_f, $2m_f$ $3m_f$, ...) [1].

2.3.3 DC capacitor

A VSC converter requires a DC capacitor across the converter bridge with the purpose of stabilizing the DC voltage. Consequently, the voltage level is well defined and is normally considered independent of the switching operation of the converter. The average DC voltage can be controlled by charging or discharging the capacitor, which is attained by active power exchanges between the AC and DC sides [3]. The effective DC voltage ripple reduces with increasing switching frequency. Hence, the DC capacitor size is reduced with increasing switching frequency of the valves.

2.3.4 AC reactor

The connection between the AC-side terminal and the AC grid is established through an interface reactor. The AC terminal voltage is a switched waveform produced by the converter bridge and contains voltage ripple. Thus, the interface reactor acts as a filter and ensures a low ripple for the AC current [20]. As a rule of thumb, the AC reactors are usually around 0.15 pu of the base impedance.

2.3.5 Vector control

The control method of the VSC is based on fast dynamic vector control, and the analysis of the configuration include an inner and outer control loop. The result is constant active power and AC voltage control (through reactive power regulation) at the rectifier side, and constant DC voltage and AC voltage control (through reactive power regulation) at the inverter side. The outer control loop receives measured values from the system and further supplies current references for the highly dynamic inner control loop. Next, the inner loop supply the control voltage to the PWM generator that controls the IGBTs in the VSC [4]. Figure 2.18 illustrates the different vector control steps.

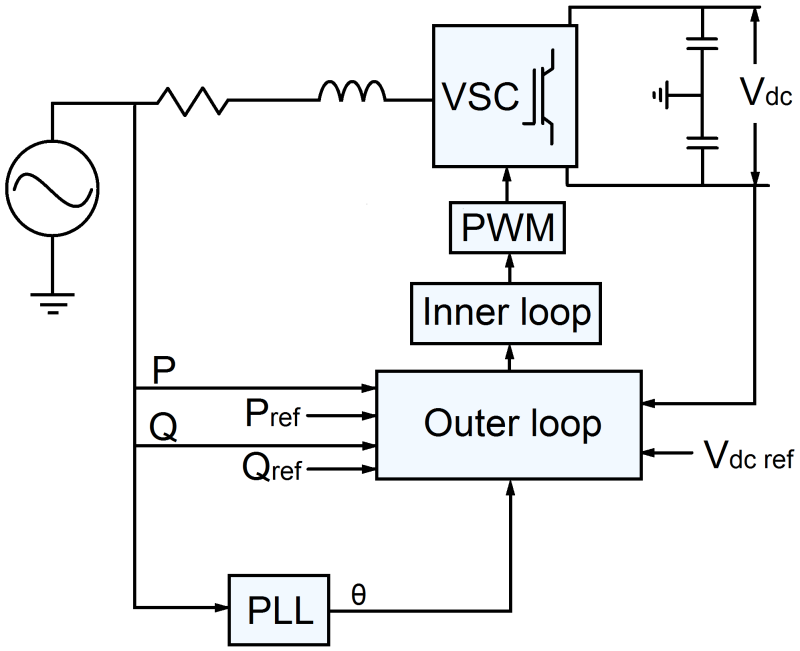


Figure 2.18: Vector control overview

In order to simplify the analysis of the three-phase system and utilize vector control, a two-dimensional *dq*-frame is introduced. Park transformation is performed in order to represent the system in terms of space vectors in reference to a stationary frame. The transformation is carried out according to Eq. A.1 and A.2 in Appendix A using the estimated angle of the grid voltage, θ, provided by a Phase-Locked Loop (PLL). θ is synchronized or locked in phase with the input voltage V_a by forming an error signal that speeds up or slows down the phase-locked oscillator, in order to match the phase of the input. The real and reactive power components exchanged between the VSC and the grid become proportional to the *d*- and *q*-axis components of the converter current. As a result, the reference commands i_{d_ref} and i_{q_ref} are the outputs of the real and reactive power compensators, respectively [20].

Outer loop control

The active and reactive power exchange between an AC and DC system illustrated in Figure 2.19, can be described as in Eq. 2.9 and 2.10.

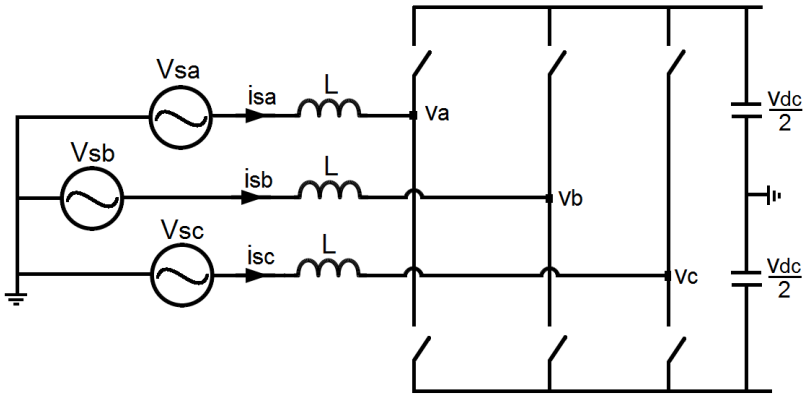


Figure 2.19: Basic VSC system

$$P_s = v_{sa}i_a + v_{sb}i_b + v_{sc}i_c \tag{2.9}$$

$$Q_s = \frac{(v_{sa} - v_{sb})i_c + (v_{sb} - v_{sc})i_a + (v_{sc} - u_{sa})i_b}{\sqrt{3}} \tag{2.10}$$

Further, the expressions can be converted to the dq-frame with a synchronous rotating coordinate system [21].

$$P_s = \frac{3}{2}(v_{sd}i_d + v_{sq}i_q) \tag{2.11}$$

$$Q_s = \frac{3}{2}(v_{sd}i_q + v_{sq}i_d) \tag{2.12}$$

The expressions can further be simplified into Eq. 2.13 and 2.13 by selecting the grid voltage vector as the d-axis, which makes $v_{sq} = 0$ [21].

$$P_s = \frac{3}{2}v_{sd}i_d \tag{2.13}$$

$$Q_s = \frac{3}{2}v_{sd}i_q \tag{2.14}$$

From equation 2.13 and 2.14, it is evident that the active power P_s can be controlled by regulating i_d, and the reactive power can be controlled by regulating i_q. Further,

i_{d_ref} and i_{q_ref} are found through a PI-controller as illustrated in Figure 2.20 and 2.21, and sent to the fast inner control loop.

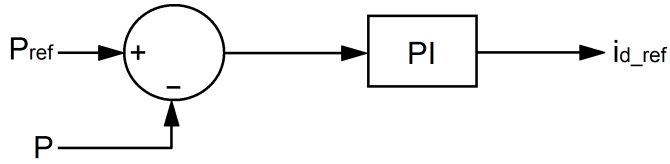


Figure 2.20: Active power control [4]

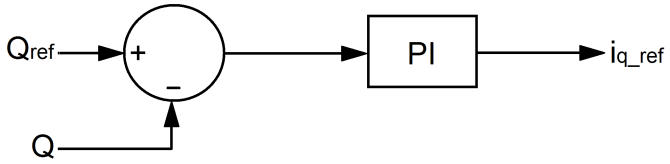


Figure 2.21: Passive power control [4]

It is common to control the DC voltage at the inverter side, which can also be regulated by controlling the active current i_{d_ref} and keeping the active power at a constant value. Figure 2.22 illustrates the DC voltage outer loop control.

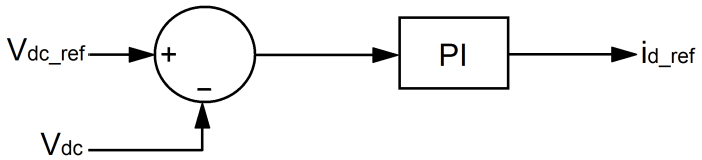


Figure 2.22: DC voltage control [4]

Inner loop control

The dynamic behavior of the current in the VSC converter in Figure 2.19, can be expressed as Eq. 2.15.

$$L\frac{d\vec{i_s}}{dt} = \vec{v_s} - \vec{v} \tag{2.15}$$

Where the vector representations in the equation are $\vec{i_s} = [i_{sa} i_{sb} i_{sc}]^T$, $\vec{v_s} = [v_{sa} v_{sb} v_{sc}]^T$ and $\vec{v} = [v_a\ v_b\ v_c]^T$. The next step is to express each space vector in Eq. 2.15 in terms of its dq-frame components based on $\vec{x}(t) =\mid x_d(t) + jx_q(t) \mid e^{j\theta(t)}$ [22]. The resulting system dynamics are presented in Eq. 2.16 and 2.17.

$$L\frac{di_d}{dt} = \omega L i_q + v_{sd} - m_d\frac{v_{dc}}{2} \tag{2.16}$$

$$L\frac{di_q}{dt} = -\omega L i_d + v_{sq} - m_q\frac{v_{dc}}{2} \tag{2.17}$$

The phase-voltage $\vec{v}$ is controlled by the PWM modulation scheme of the VSC, and can be expressed as $\vec{v} = \vec{m}\frac{v_{dc}}{2}$. This modulation index is the input control of the system dynamics. The phase synchronous angle, θ, is the estimated output angle of the PLL, and is related to ω by the relationship in Eq. 2.18.

$$\frac{d\theta}{dt} = \omega(t) \tag{2.18}$$

The control objective of the system is to make the input current follow the reference current; $i_d \to i_{d\_ref}$ and $i_q \to i_{q\_ref}$, where i_{d_ref} and i_{q_ref} are the reference values from the outer loop. Expressions for the errors are presented in Eq. 2.19 and 2.20.

$$\tilde{i_d} = i_d - i_{d\_ref} \tag{2.19}$$

$$\tilde{i_q} = i_q - i_{q\_ref} \tag{2.20}$$

Deriving the expressions, and Eq. 2.21 and 2.22 are left.

$$\frac{\mathrm{d}\tilde{i_d}}{\mathrm{d}t} = \frac{\mathrm{d}i_d}{\mathrm{d}t} \tag{2.21}$$

$$\frac{\mathrm{d}\tilde{i_q}}{\mathrm{d}t} = \frac{\mathrm{d}i_q}{\mathrm{d}t} \tag{2.22}$$

In order for these error currents to go towards zero as $t \to \infty$, a controller in the form of Eq. 2.23 and 2.24 is necessary. Since the expressions are first-order differential equations, the error currents goes towards zero as $t \to \infty$ when the expressions are integrated.

$$L\frac{\mathrm{d}\tilde{i_d}}{\mathrm{d}t} = -k\tilde{i_d} \tag{2.23}$$

$$L\frac{\mathrm{d}\tilde{i_q}}{\mathrm{d}t} = -k\tilde{i_q} \tag{2.24}$$

The next step is to propose a controller from the input control of the system, $\vec{m}\frac{v_{dc}}{2}$, which in closed loop with the dynamics of the system in Eq. 2.16 and 2.17, achieve the desired current error expression as in Eq. 2.23 and 2.24 above. The input control proposed is expressed below in Eq. 2.25 and 2.26.

$$m_d\frac{v_{dc}}{2} = v_{sd} + \omega L i_q + k\tilde{i_d} \tag{2.25}$$

$$m_q\frac{v_{dc}}{2} = v_{sq} - \omega L i_d + k\tilde{i_q} \tag{2.26}$$

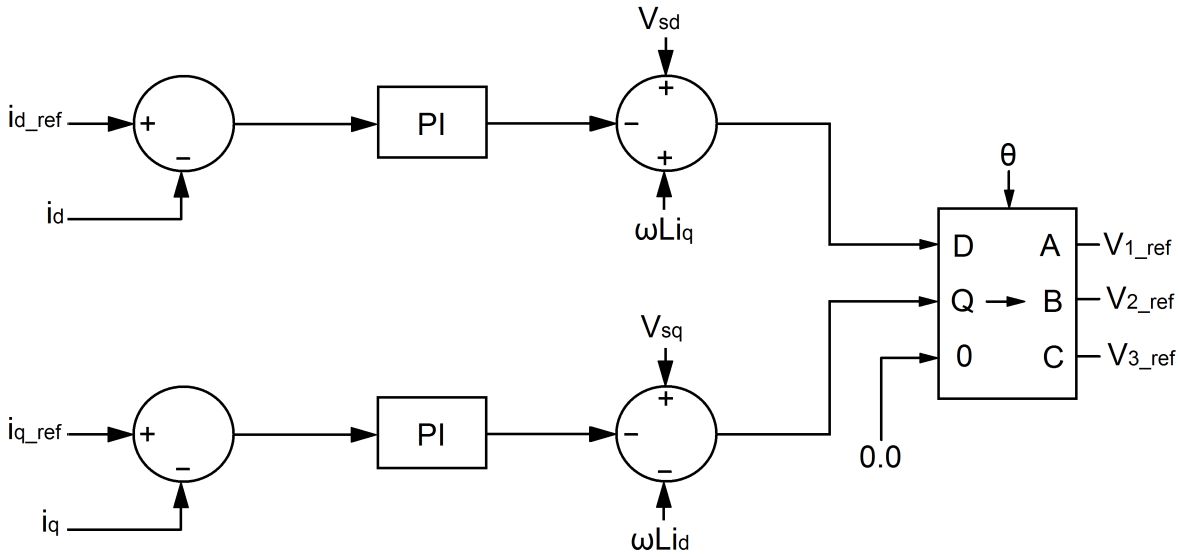


Figure 2.23: Inner loop control

The resulting inner loop control system is illustrated in Figure 2.23, where i_{d_ref} and i_{q_ref} regulates the voltage control signal supplied to the PWM scheme. The result of the vector control is that the rectifier controls the active power (dmode) and the AC voltage by controlling the reactive power (qmode), and the inverter controls the DC voltage (dmode) and the AC voltage by controlling the reactive power (qmode).

2.4 Modular multilevel converter operation

The MMC converter, or sometimes referred to as Cascaded Two-Level converter (CTL), is based on the same operating and control principles as the VSC, but each phase-arm consists of several two-level submodules, as can be seen in Figure 2.24. The MMC converter addresses and solves many of the limitations of the VSC converter. New technology makes the converter scalable up to the highest transmission voltages, and losses are reduced to approximately 1% per converter [11].

Due to multiple operating levels, the output voltage is close to a sinusoidal waveform, making the harmonic performance of the MMC excellent. It is able to eliminate the low-order harmonics that usually require large filters. Each submodule is constructed as a half-bridge, two-level converter with two IGBTs in anti-parallel with diodes, and a capacitor across the two switching pairs, as illustrated in Figure 2.25. Switching of the submodules have three possibilities, as described below [11].

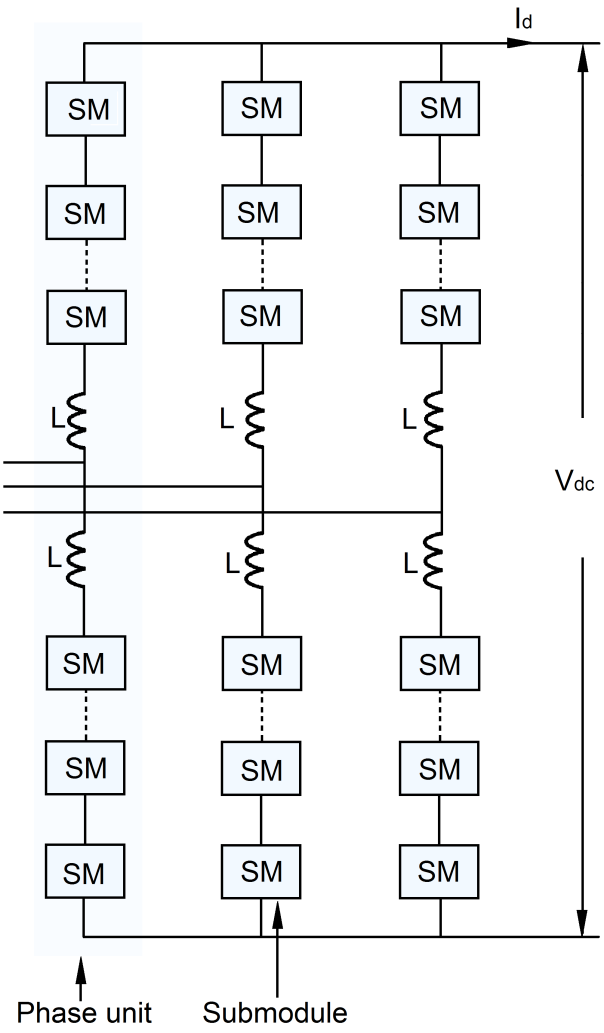


Figure 2.24: Three-phase modular multilevel converter [3]

- S_1 OFF and S_2 ON, the submodule is said to be *incerted*, and the submodule output voltage equals the capacitor voltage. The capacitor charges when the arm current is positive, and discharges otherwise.

- S_1 ON and S_2 OFF, the submodule will give zero voltage output. The capacitor in then *bypassed* and its voltage remains constant.

- S_1 OFF and S_2 OFF, the submodule becomes *blocked*, and current is only conducted through the diodes. The capacitor will then only charge when the arm current is positive, and not discharge.

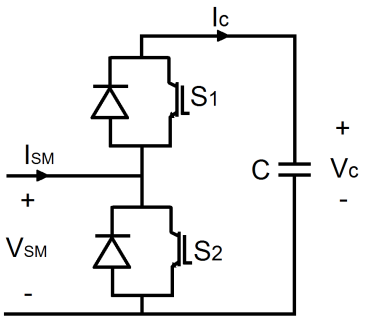


Figure 2.25: MMC submodule circuit

Each submodule is switched at a low frequency. A typical switching frequency is about $f_{sw} = 150\,Hz$, which is a pulse number of about 3 for a fundamental frequency of 50 Hz. If there are N submodules per arm, the effective switching frequency per phase leg becomes $2N150\ Hz$. With a number of submodules of around 40, the frequency is about 10 times of a regular 2-level VSC, which indicates that the dynamic response of an MMC converter is excellent [11].

Since the MMC topology is a voltage source converter, the same control strategy with an inner and outer loop control is utilized. In addition, the MMC requires controllers in order to stabilize internal variables like submodule capacitor voltage and second order harmonic circulating phase currents. The harmonic circulating currents are generated by voltage imbalances between the arm phases of the MMC, and increase the ripple of the submodule voltages [23]. This polluted circulating current can be eliminated by using active control of the AC voltage reference, V_{ac_ref}, or placing split-capacitors across the phase arms. The reduction of the second harmonic component of the circulating current, and thus reducing the DC voltage ripple, is performed using a Circulating Current Suppression Control (CCSC), as illustrated in Figure 2.26.

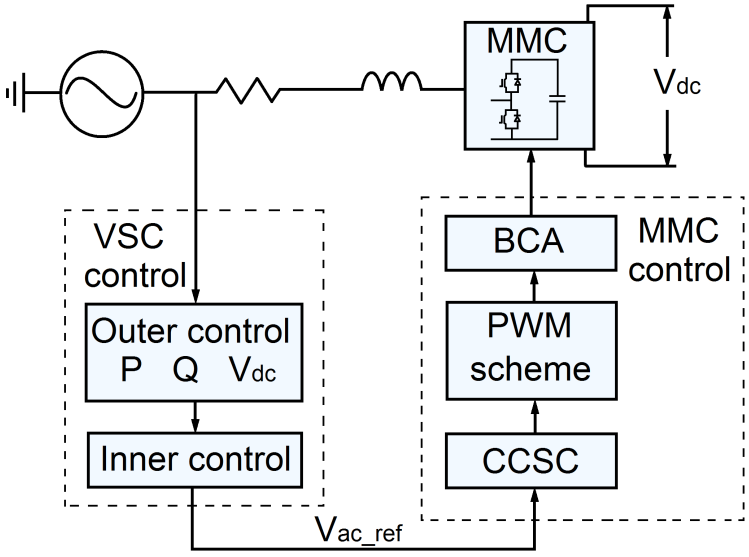


Figure 2.26: Vector control overview

There are varius PWM modulation techniques developed for MMC topologies that utilize different staircase-type methods for the intricate switching of the submodules. After the PWM modulation, the next step is a Balancing Control Algorithm (BCA) in order to balance the capacitor voltages of all the submodules during operation. The capacitor voltages are monitored, and the capacitors are switched ON and OFF based on a balancing control system [23]. Figure 2.26 illustrates the correlation between VSC control and MMC control.

Chapter 3

System Parameters

In this chapter the parameters for the LCC (SK3) and MMC (SK4) PSCAD models are found. Some values are provided by a Master thesis witten by Alemayo Tadese at Aalborg Universty in 2010, and some values are given by Statnett.

3.1 DC network

The nominal power and voltage ratings for SK3 and SK4 are listed in Table 3.1 below.

	power capacity [MW]	DC voltage [kV]
SK3	440	350
SK4	715	500

Table 3.1: DC system parameters [5]

3.2 AC network

The AC systems at Kristiansand and Tjele are the same for both HVDC systems, as they are connected to the same voltage bus. Table 3.2 presents the nominal AC voltages and short circuit capacites at both ends. Due to lack of available information, it is assumed that the minimum short circuit capacity at Tjele is the same as on the Kristiansand side, which is a provided parameter by Statnett.

	AC voltage[kV]	min short circuit capacity[MVA]	frequency[Hz]
Kristiansand	300	3000	50
Tjele	400	3000	50

Table 3.2: AC system parameters [5]

The AC networks at Kristiansand and Tjele are modelled as equivalent R-R/L circuit impedances, as can be seen in Figure 3.1, that represent the strength of the connected grid.

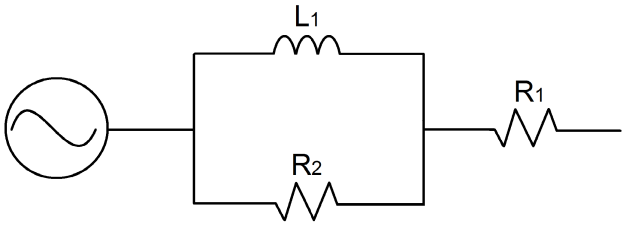


Figure 3.1: The AC network equivalent

The component values of the R-R/L circuit can be calculated using the Short Circuit Level (SCL) and Short Circuit Ratio (SCR) of the system, as discussed in Section 2.1.3. A strong AC system is defined to have an SCR greater than 3, while a weak AC system is defined to have a SCR between 2 and 3 [15].

The impedance of the AC system can be solved for using Eq. 2.1 and 2.2.

$$Z_{ac} = \frac{E_{ac}^2}{SCR \cdot P_d} \tag{3.1}$$

The moderational ratio of the system, $\frac{X}{R}$, is provided by Statnett and is set to be 14, which is a typical value for a semi-weak grid. Further, the impedance is found in Eq. 3.2 below.

$$Z_{ac}\angle\theta = Z_{ac}\angle \tan^{-1}\frac{X}{R} = a + jb \tag{3.2}$$

In order to calculate the component values, the R-R/L circuit can be expressed as in Equation 3.3.

$$\begin{aligned} Z_{ac}\angle\theta = R_1 + R_2 \parallel jX_L = R_1 + \frac{R_2 \cdot jX_L}{R_2 + jX_L} \\ = R_1 + \frac{X_L^2 \cdot R_2 + jX_L \cdot R_2^2}{R_2^2 + X_L^2} \\ = R_1 + \frac{X_L^2 \cdot R_2}{R_2^2 + X_L^2} + j\frac{X_L \cdot R_2^2}{R_2^2 + X_L^2} \end{aligned} \tag{3.3}$$

The SCR differs throughout the year, but in order to model the AC network with an equivalent impedance and a voltage source, numbers from Table 3.1 and 3.2 are used. The AC system equivalent stays the same, even though the combinations of

connected HVDC links change. It is therefore only calculated for the combined SK3 and SK 4 system.

Total DC power = 715 MW + 440 MW = 1155 MW.

Kristiansand station

$$SCR = \frac{3000\,MVA}{1155\,MW} = 2.59$$

Equation 3.1 is then used to calculate the AC impedance, Z_{ac}:

$$Z_{ac} = \frac{300\,kV^2}{2.59 \cdot 1155\,MW} = 30.08\,\Omega$$

$$30.08\angle \tan^{-1}(14) = 30.08\angle 85.91^\circ = 2.14 + j30.00\,\Omega$$

From Equation 3.3, the values of R_1 and L_1 can be found. R_2 is set to be the constant value of 1000 Ω.

$$2.14 = R_1 + \frac{X_L^2 \cdot R_2}{R_2^2 + X_L^2} \text{ and } j\,30.00 = j\,\frac{X_L \cdot R_2^2}{R_2^2 + X_L^2}$$

Tjele station

The same calculations are applied at the Tjele side in order to find the equivalent values.

$$SCR = \frac{3000\,MVA}{1155\,MW} = 2.59$$

$$Z_{ac} = \frac{400\,kV^2}{2.59 \cdot 1155\,MW} = 53.48\,\Omega$$

$$53.58\angle \tan^{-1}(14) = 53.58\angle 85.91^\circ = 3.82 + j53.44\,\Omega$$

3.2.1 AC network equivalent

The parameter values for the AC equivalents are gathered in Table 3.3, where $X_L = \omega L = 2\pi f L = 100\pi L$.

	L_1 [H]	R_2 [Ω]	R_1 [Ω]
Kristiansand	0.096	1000	1.24
Tjele	0.17	1000	0.95

Table 3.3: AC network equivalent parameters

3.3 Transformer parameters

The SK3 transformer parameters are found in the schematic of the Skagerrak connections in appendix B, and the SK4 transformer parameters are given by the Aalborg thesis [25]. Table 3.4 presents the transformer values.

Transformers	Primary [kV]	Secondary [kV]	S [MVA]
SK3 Kristiansand	300	143.9	256
SK3 Tjele	400	143.9	256
SK4 Kristiansand	300	150	500
SK4 Tjele	400	150	500

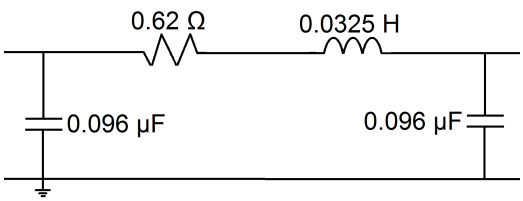
Table 3.4: Transformer values [5]

The transformer models are considered ideal with a leakage reactance of 0.18 p.u.for the SK3 and SK4 converter stations, which is a typical value for transformers used in HVDC links [5].

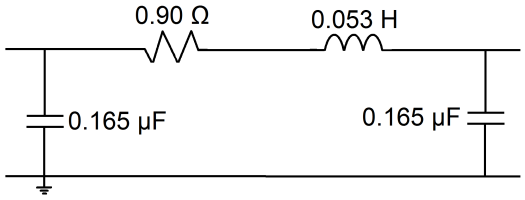
3.4 DC cable equivalent

The SK3 DC cable consists of an overhead line from the converter station in Kristiansand to the ocean, and one from the Tjele station out to the ocean. They are connected together by a subsea cable of approximately 125 km long. In total, the length of the HVDC link is approximately 240 km [16].

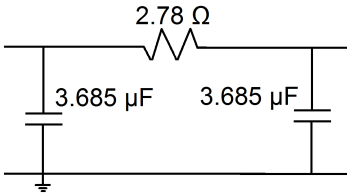
Cable model parameters are supplied by Energinet.dk [5], and are illustrated in Figure 3.2, where Figure 3.2a) is the equivalent for the overhead line at Kristiansand, Figure 3.2b) is the overhead line at Tjele, and Figure 3.2c) is the subsea cable equivalent. It is assumed that the SK3 and SK4 cables can be modelled by the same π-equivalents.



(a) Overheadline Kristiansand



(b) Overheadline Tjele



(c) Subsea cable

Figure 3.2: SK3 and SK4 cable equivalents

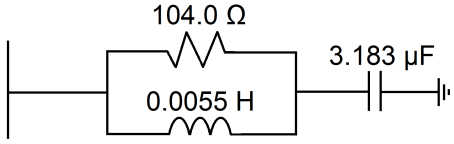
3.5 LCC AC filters

There are AC filters connected to each converter terminals. SK3 requires more filtering than SK4, because of more harmonic disturbance and reactive power consumption of the converter. The SK3 AC filters at Kristiansand are presented in Table 3.5, where number of filters, type of filter, and the capacities are given.

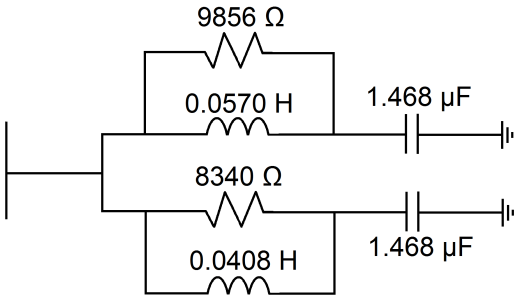
Type of filer	Capacity [MVAr]	# of filters
High-pass	90	2
11th	83	2
13th	83	2
Shunt capacitor	80	1

Table 3.5: SK3 AC filters at Kristiansand [5]

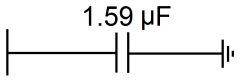
The SK3 AC filters at the Kristiansand side are illustrated in Figure 3.3.



(a) 90 MVAr high pass filter



(b) 83 MVAr 11th/13th filter



(c) 45 MVAr shunt capacitor

Figure 3.3: SK3 AC filters at Kristiansand [5]

Table 3.6 shows the SK3 AC filters at Tjele, and Figure 3.4 is the constructed AC filter.

Type of filer	Capacity [MVAr]	# of filters
High-pass	65	4

Table 3.6: SK3 AC filters at Tjele [5]

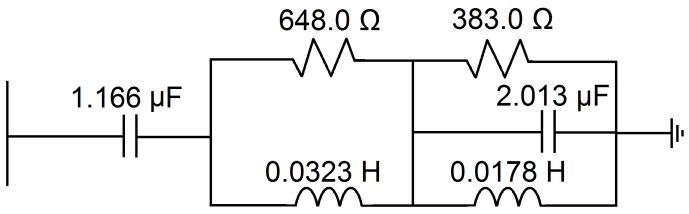


Figure 3.4: 65 MVAr high-pass filter at Tjele [5]

3.6 SK3 DC smoothing reactor

There are smoothing reactors on the SK3 DC side of both the rectifier and inverter. The value is set to be 225 mH for a current of 1260 A [5].

3.7 MMC submodules

Submodule switching frequency

The switching frequency of each submodule is provided by Statnett and is set to be 168.5 HZ, which is 3.37 times that of the fundamental frequency.

Number of submodules

The number of submodules in each converter arm used in SK4 is set to 30, a number provided by Statnett.

Submodule capacitor

The submodule capacitor size given by Statnett is $1.2\,mF$. This value is found to give a high ripple in the simulated DC voltage, and harmonic disturbance in the DC current. Another approach in order to find a more suitable capacitor value is investigated. By using the standard PSCAD model by Manitoba, the ratio between capacitance in each module devided by the number of modules is used.

From Manitoba:
$C_{ratio} = \dfrac{5100\,\mu F}{74 cells} = 68.92$

SK4:
$C_{module} = 68.92 \cdot 30 submodules = 2068\,\mu F$

3.8 SK4 converter reactor

It is a common rule of thumb to set the converter reactor, L_s, to be approximately $0.15\,pu$ of the base impedance, Z_{base}. Calculations to find the reactor value are performed below.

$$Z_{base} = \frac{V_{base}^2}{S_{base}} = \frac{150^2}{715} = 31.47\,\Omega$$

$$0.15\,pu = 31.47\,\Omega \cdot 0.15 = 4.72\,\Omega$$

$$L_s = \frac{4.72\,\Omega}{2\pi 50} = 0.015\,H$$

3.9 MMC DC chopper

A DC chopper is connected to the DC link with the purpose of reducing the DC voltage during start-up and fault. It consists of a variable resistor that is regulated based on the measured DC voltage. The DC chopper is a built in function of the Manitoba PSCAD model, and is illustrated in Figure 3.5.

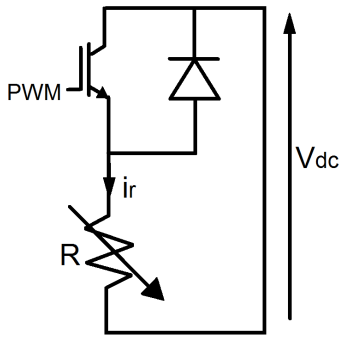


Figure 3.5: DC chopper circuit

3.10 LCC-MMC bipolar configuration

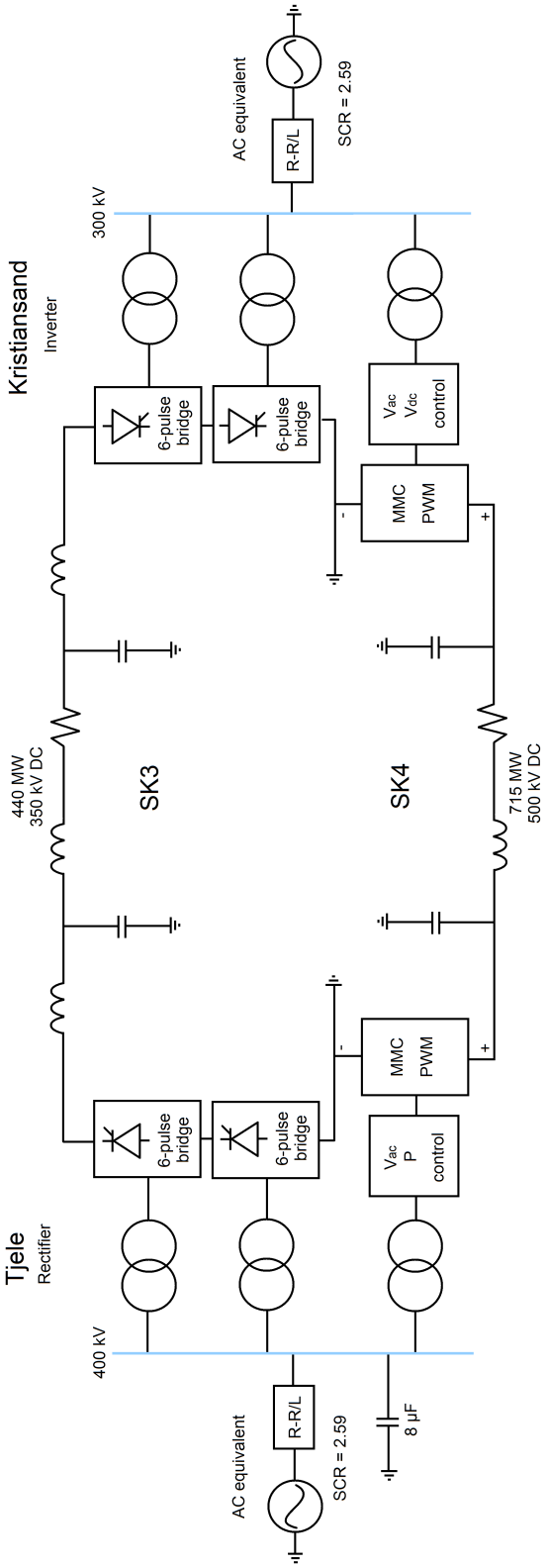


Figure 3.6: LCC-MMC bipolar configuration

Chapter 4

Steady State

In this chapter the steady state characteristics of the LCC model, the MMC model and the bipolar combination of the two are discussed. The purpose of the steady state analysis is to observe how the HVDC links are performing during normal operation, and to have a basis to compare and verify that the models are operating in a correct manner. All simulations are performed for four seconds and are given in per unit values.

4.1 LCC-HVDC steady state behavior

Figure 4.1 illustrates the steady state characteristics of the LCC-HVDC system with a DC power level of 440 MW at 350 kV. The AC rms voltage at the rectifier side (Tjele) is 400 kV, and 300 kV at the inverter side (Kristiansand). The simulations are performed for four seconds, making the system able to reach steady state operation. First, Figure 4.1(a) shows the AC rms voltage at both the rectifier and inverter side. The voltages reach their respective nominal values of 1 pu after approximately $0.2\,s$. Next, Figure 4.1(b) shows the DC voltage, which is also responding fast and reaches 1 pu. It contains some ripple, which is quite normal for the DC voltage as a result of the switching process. The ripple is approximately 12 times the fundamental frequency. Lack of filtering may also result in some harmonic noise. Next, the DC power reaches quickly 1 pu in Figure 4.1(c), indicating that all the required power is being transmitted. Finally, Figure 4.1(d) shows the DC current, which also gets to the nominal value, as expected based on the DC power and voltage. As a result, the operating properties of the LCC model are very respectable.

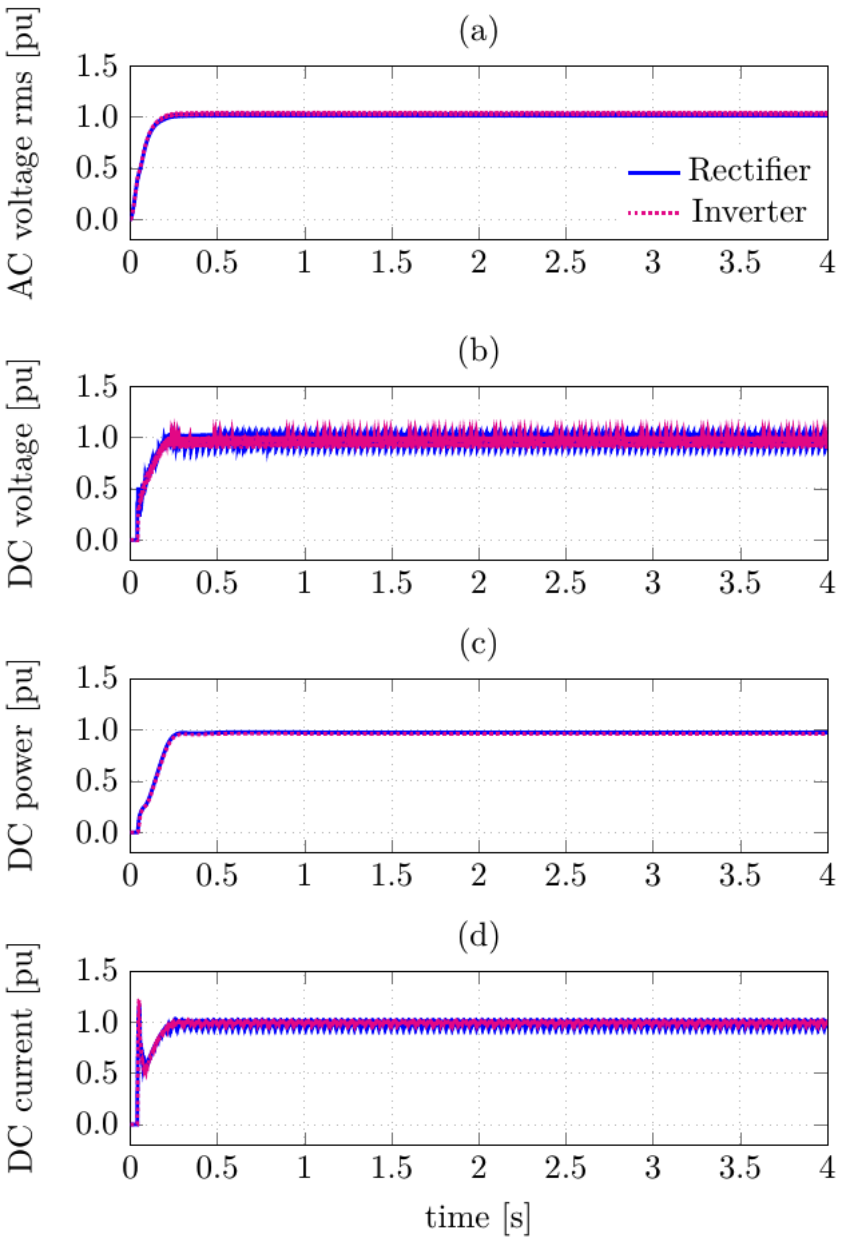


Figure 4.1: LCC steady state operation

Figure 4.2 presents the control objectives of the LCC model at steady state. As mentioned in section 2.2, the rectifier side of the LCC controls the DC current, while the inverter regulates the DC voltage. Figure 4.2(a) shows the DC current control at the rectifier. The reference current is supplied from the inverter by Voltage Dependent Current Limiter (VDCL) control. It is evident that the current regulation is operating properly, as the rectifier current follows its respective reference current. Next, the control objective at the inverter side can be seen in Figure 4.2(b). Constant extinction angle control is utilized in order to regulate the DC voltage. The extinction angle at the inverter follows the constant reference angle of 18°. As a result, the LCC model is verified to be operating in a desired manner. All objectives are fully satisfied and the model has been validated.

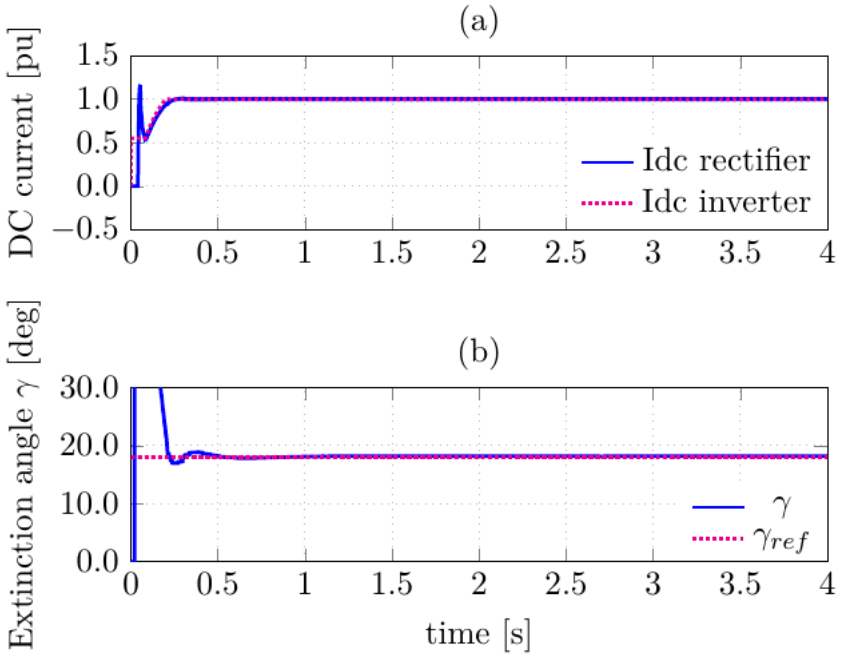


Figure 4.2: LCC control objectives at steady state

4.2 MMC-HVDC steady state behavior

The MMC-HVDC simulation model has a rated power of 715 MW at 500 kV DC voltage, as discussed in chapter 3. The AC rms voltage at the rectifier side is 400 kV and 300 kV at the inverter side. Figure 4.3 presents the steady state characteristics of the MMC model during the first 4 seconds. As discussed in section 2.3, the rectifier side controls the active power and the AC voltage through reactive power control, while the inverter side controls the DC voltage and the AC voltage through reactive power control. At $t = 0.2s$, the control objectives at the inverter side are deblocked in order to regulate the DC voltage. At $t = 0.6\,s$, the control objectives at the rectifier side are deblocked, making it possible to regulate the DC power in the system. First, Figure 4.3(a) shows the AC rms voltage at the rectifier and inverter side. One can clearly see where the deblocking of the controllers occur, as the AC voltages experience small transients at these points. Next, the DC voltage can be seen in Figure 4.3(b). It reaches steady state without much trouble and any overshoots, but contains concerning amounts of ripple. This behavior is normal, due to polluted circulating currents in the converter, and because the DC voltages in the submodules are only state variables. In order to reduce the ripple, the modulation technique must change or a large capacitor can be connected across all of the submodules, in order to create a stable voltage source. Next, Figure 4.3(c) shows the DC power, which does not start being regulated until $t = 0.6s$. There is a ramp controlling the power during the fist period of $500\,MW/s$, causing the slow increase. If increasing the ramp rating, the AC voltage may experience voltage overshoot due to fast regulation. Finally, the DC current can be seen in Figure 4.3(d). It stays at zero pu as long as the DC power is zero, but turns negative along with the power when the regulation kicks

in at $t = 0.6\ s$, thus changing the direction of the power flow. The DC current drops to approximately -2.5 pu at the most extreme point. These undershoots have values that the converter diodes may have problems handling. All the objectives reach the steady state condition of 1 pu at $t = 2.2\ s$, after experiencing short periods of transients. Hence, the MMC steady state characteristics are operating after satisfaction.

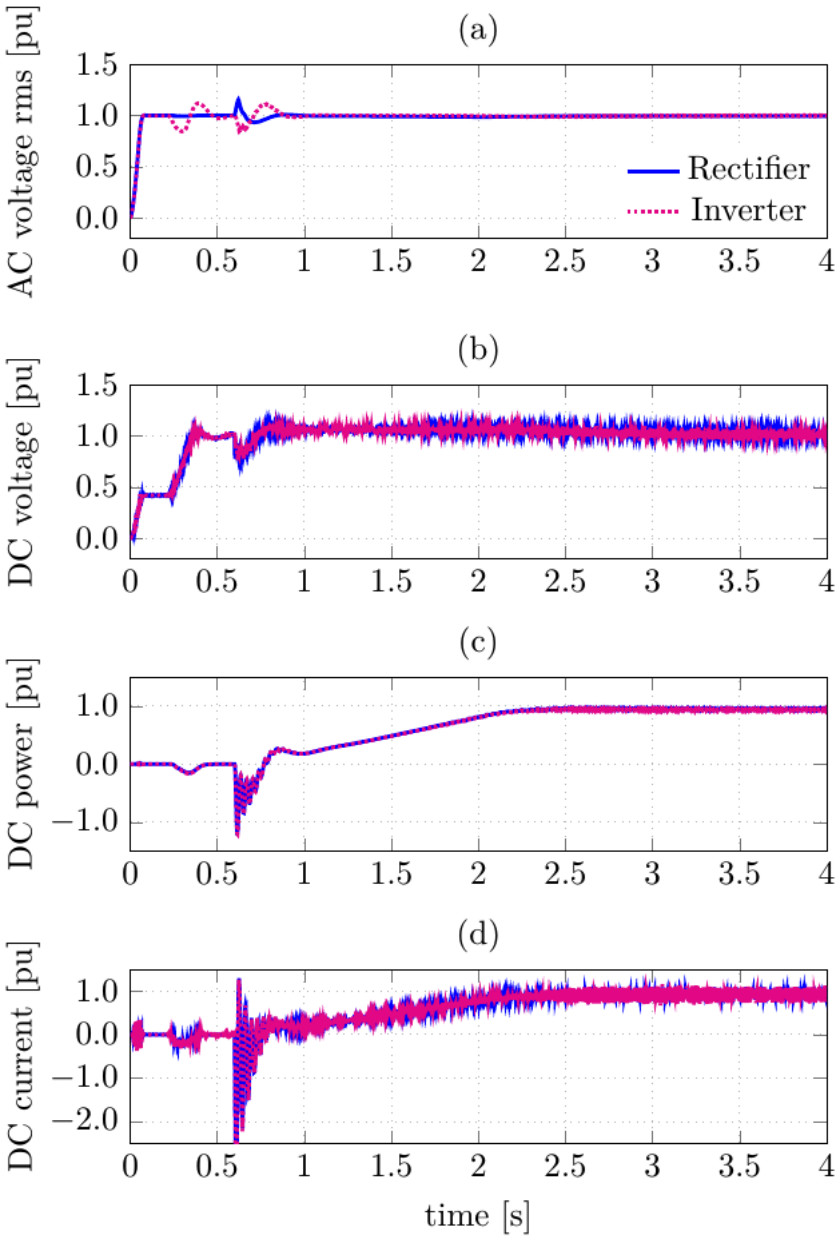


Figure 4.3: MMC steady state operation

The inner loop control objectives of the MMC at the rectifier and inverter side are presented in Figure 4.4. As discussed in subsection 2.3.5, the outer loop control provides the reference currents for the active power control (dmode) and passive power control (qmode) using vector control. First, Figure 4.4(a) shows the DC

power control at the rectifier. The reference current is zero until the control unit starts to operate at $t = 0.6\,s$, and starts to increase slowly in the same pace as the power ramp. Next, Figure 4.4(b) shows the AC voltage control through reactive power regulation at the rectifier. The current follows the reference current, which is, as expected, approximately zero pu. Further, Figure 4.4(c) shows the DC voltage control at the inverter. At $t = 0.2\,s$, it is evident that the controller starts to operate and regulate the voltage in the system, and after $t = 2.5\ s$ the reference current stabilizes at 1 pu. Finally, Figure 4.4(d) shows the AC voltage control objective at the inverter. Fluctuations occur when both the controllers start to operate, and the reference current stabilizes at zero pu at $t = 1.0\ s$. From the fluctuations in the system currents, it is clear that the vector control is continuously working hard to keep the system currents following their respective reference currents.

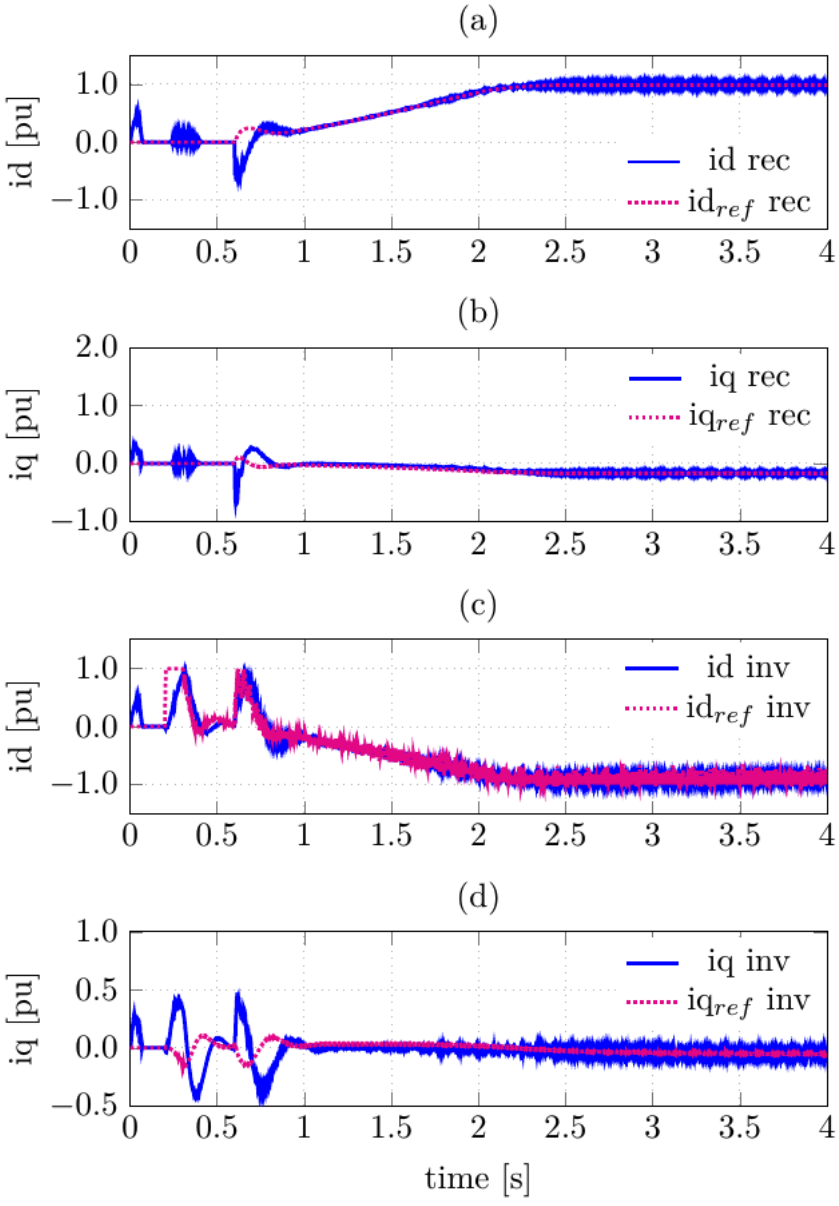


Figure 4.4: MMC control objectives at steady state

An excellent steady state behavior is expected from the MMC, as it can control active and reactive power independently, and suffer from minimal harmonic disturbance due to the multilevel voltage output. The MMC presented in Figure 4.3 is working correctly, and reaching the desired operating values. However, there are some harmonic disturbances in the DC voltage and current, due to the modelation technique and polluted circulating currents in the converter. Apart from the disturbance, the model is operating after satisfaction and can be trusted.

4.3 LCC-MMC steady state behavior

In this section, the two HVDC systems are combined in an LCC-MMC bipolar configuration as illustrated in Figure 3.6 from chapter 3. The HVDC-LCC link has a rated power of 440 MW at 350 kV, and the HVDC-MMC link has a rated power of 715 MW at 500 kV. The AC rms voltage at the rectifier side is 400 kV, and 300 kV at the inverter side.

At $t = 0.2\ s$, the DC voltage in the MMC starts regulating at the inverter side. Then, at $t = 0.6\ s$ the DC power starts regulating at the rectifier with the help of a ramp signal of 500 MW/s, thus maintaining a steady increase in power. Figure 4.5 shows the shared AC system characteristics at the rectifier and inverter side. First, Figure 4.5(a) shows the AC rms voltage at both converter ends. The AC voltage quickly reaches the rated value of 1 pu, after a short voltage overshoot at the rectifier side at $t = 0.6\ s$. This reaction is due to the regulation of the power at the rectifier side, and the same behavior can be seen in the MMC system in Figure 4.3(a), indicating that the MMC is regulating the AC voltage as expected. Next, the AC power can be seen in Figure 4.5(b). The ramp regulation for the power in the MMC link begins at $t = 0.6\,s$, and slowly increases until reaching approximately 1 pu. The AC power at the inverter side is a little lower than the power at the rectifier side. This is probably a result of power loss in the DC cable. Finally, the reactive power of the AC system can be seen in Figure 4.5(c). As there are no filters connected to the terminals, with the exception of a shunt capacitor of 8 μF at the rectifier side (which corresponds to roughly 400 MVA), the MMC is providing most of the reactive power to the system.

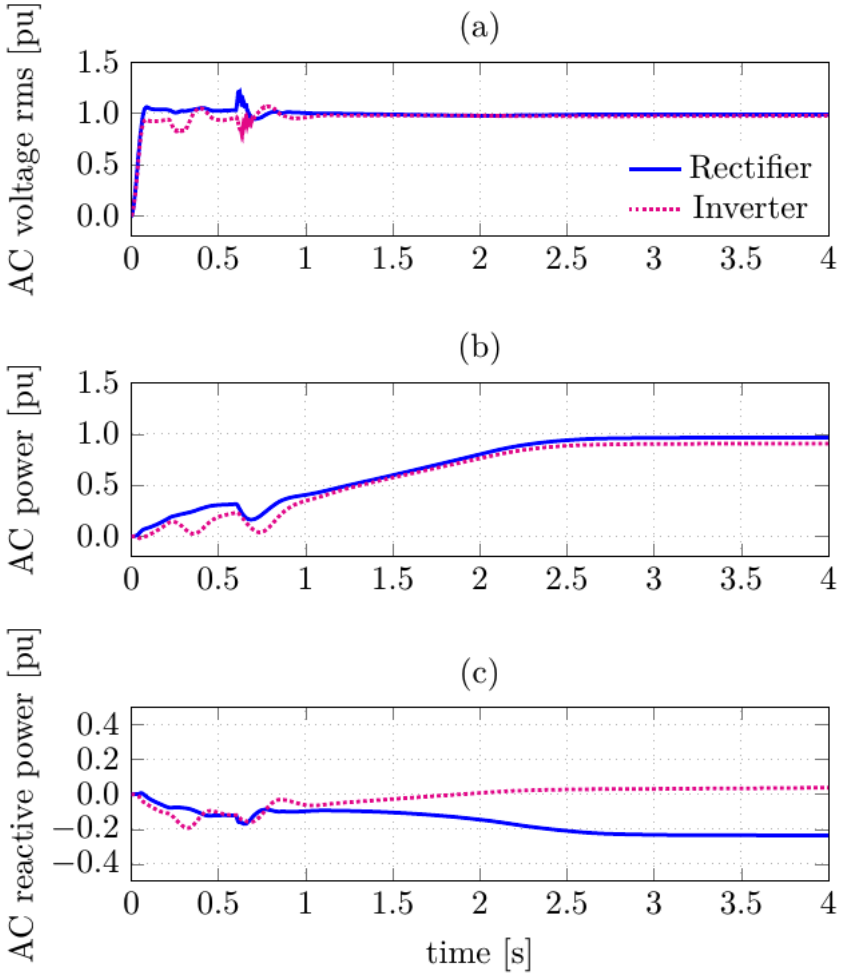


Figure 4.5: LCC-MMC AC system steady state operation

Figure 4.6 presents the LCC and MMC DC values. First, the DC voltage of the LCC and MMC link can be seen in Figure 4.6(a). There is a voltage unbalance between the two systems. The LCC voltage is lower than expected, and the MMC is higher than expected. This is an interesting outcome of the combined configuration. The harmonic disturbance in the LCC voltage is due to the switching operation of the thyristors, and can be reduced with a well-designed filter. The ripple has a frequency of approximately 12 times the fundamental frequency. The ripple in the MMC is also normal, and is due to polluted circulating currents in the converter. Power reversal in the LCC is carried out by changing the voltage polarity of the link, while in the MMC the current changes direction. Power reversal of the MMC link occurs at $t = 0.6\ s$ for a period of approximately $0.2\ s$, due to the start of power regulation at the MMC inverter. This is the reason for the LCC voltage undershoot in (a), and the negative MMC DC power in (b) and DC current in (c). Figure 4.6(b) shows the DC power, which reaches 1 pu after the ramp function at the MMC rectifier. Finally, Figure 4.6(c) shows the DC current. The MMC current still has an extreme undershoot at $t = 0.6\ s$ as in Fig. 4.3(d), but both values reach 1 pu after roughly $2.5\ s$. Comparing the characteristics of the LCC and LCC-MMC bipolar configuration, the LCC is affected by the regulation in the MMC, especially the power regulation at $t = 0.6\ s$.

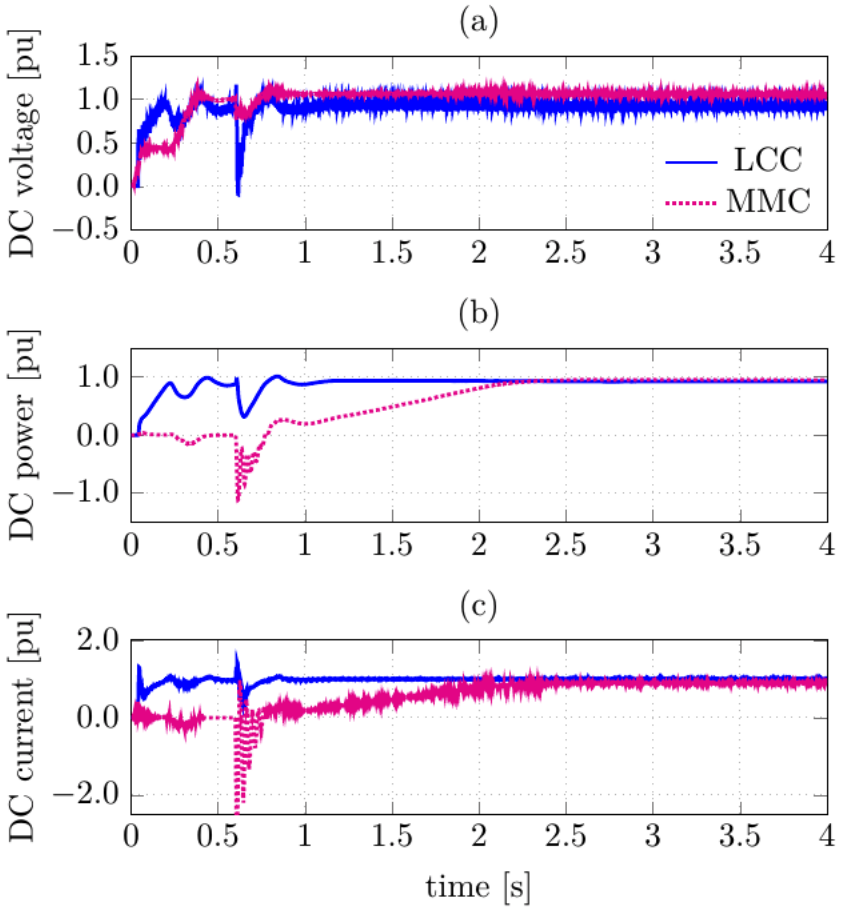


Figure 4.6: LCC-MMC DC system steady state operation

Figure 4.7 presents the control objectives of the LCC with DC current control in (a) and minimum extinction control in (b). In Figure 4.7(a), a reference DC current is supplied from the inverter to the rectifier side by Voltage Dependent Current Limiter (VDCL). The DC current at the rectifier is following the reference current as expected. The extinction angle control in Figure 4.7(b) stabilizes at 18° at approximately $t = 1.2\ s$, after a short period of transient behavior. The first transient is a result of the deblocking of the DC voltage regulation at $t = 0.2\ s$. At $t = 0.6\ s$, the DC power regulator is deblocked, creating fluctuations in the extinction angle, and a short period of failure of commutation when the angle reaches zero degrees. This is due to the AC voltage drop experienced by the LCC at $t = 0.6\ s$. The control objectives are restored after a short period (approximately $0.4\ s$) after the deblocking, and operate as expected.

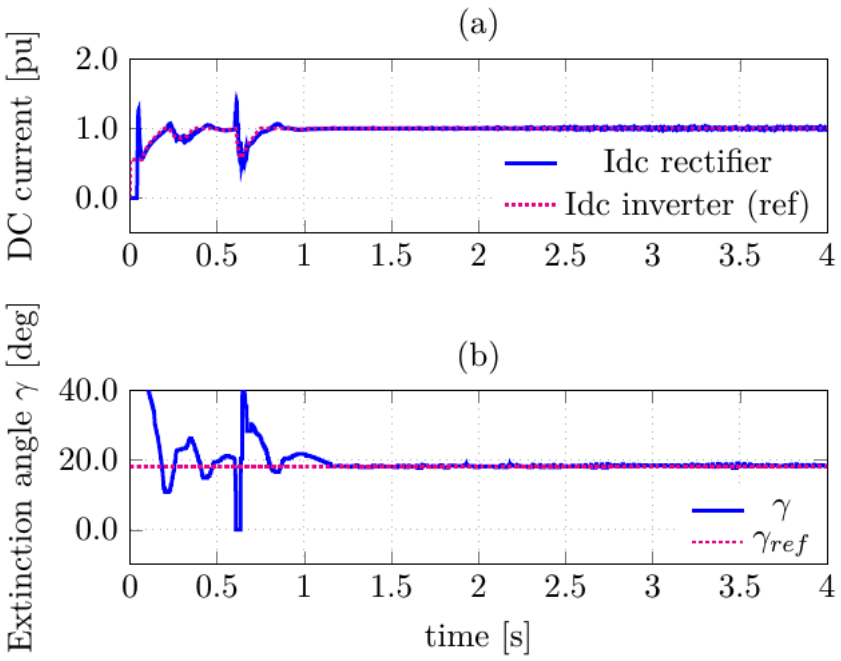


Figure 4.7: LCC control objectives at steady state

The MMC system currents in Figure 4.8 show the inner loop control of the rectifier side and inverter side. The outer loop provides the reference currents to the inner loop. First, Figure 4.8(a) shows the DC power control, which is regulated by the current i_d. Next, Figure 4.8(b) shows the AC voltage control carried out by controlling the reactive power at the rectifier. Then, Figure 4.8(c) shows the DC voltage control at the inverter. And Finally, the AC voltage control through reactive power regulation can be seen in Figure 4.8(d). The vector control is operating as it is supposed to, and all current objectives are following their respective reference currents.

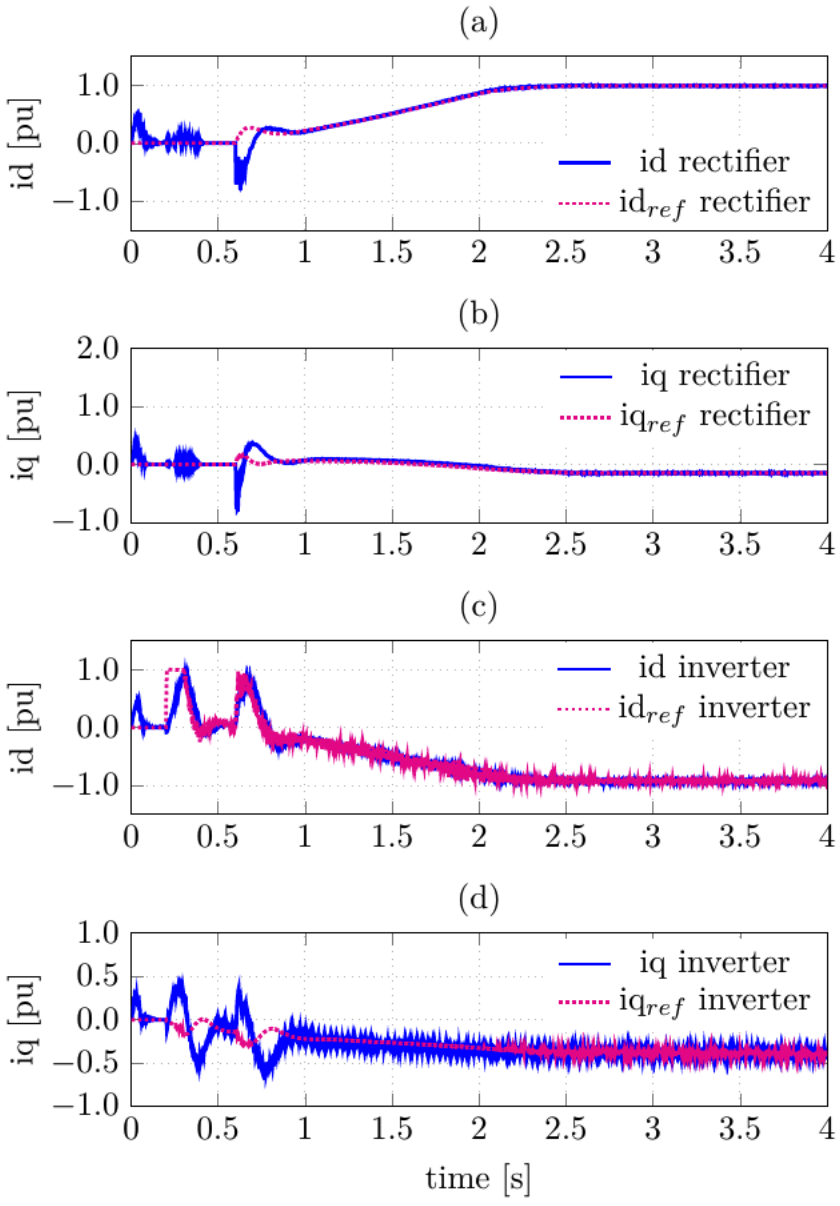


Figure 4.8: MMC control objectives at steady state

4.4 Summary

The objective of the steady state analysis is to verify that the three models are operating as expected from the theory presented in the thesis. The LCC at steady state is operating as desired. All the system values stabilizes at 1 pu after a short rise time of approximately 0.25 s. The DC voltage contains ripple due to the switching process in the thyristor bridges. The ripple has a frequency of roughly 12 times the fundamental frequency. The control objectives are operating as desired, where the DC current at the rectifier follows the reference current supplied by Voltage Dependent Current Limiter (VDCL) control at the inverter, and the extinction angle follows the minimum extinction angle of 18°.

The MMC is operating as expected based on the verification process. The DC voltage and power control are deblocked in steps, making the system able to stabilize into steady state. A ramp of 500 MW/s is supplied to the power, in order to avoid overshoots in the AC voltage. The DC voltage and current contain some amounts of ripple. This behavior is normal to a certain degree, and is a result of polluted circulating currents in the converter and because the DC voltage in each submodule is a state variable. Utilizing a different modulation technique or connecting a large capacitor across the positive and negative phase-arm can lower the ripple.

When the two models are combined into an LCC-MMC bipolar configuration, the LCC filters are removed. The system operates well without the filters, because the MMC provides the necessary reactive power for the system. Although, some filtering should be implemented in order to remove portions of the 11th and 13th order harmonics in the LCC, redesigning of the filters require a lot of effort and is a task for further work. There is a voltage difference between the DC voltages in the combined system, which is interesting because it indicates that the voltage is not divided across the two cables as is ought to. This phenomenon can be interesting to look at in further work. The deblocking of the power regulation in the MMC system at $t = 0.6\ s$ result in some fluctuations in the LCC system, and a short period of commutation failure in the thyristor valves.

It can be concluded that the implemented systems are validated.

Chapter 5

AC Fault –Three-Phase to Ground

In this chapter, a three-phase to ground fault at the inverter side is simulated. Although it is a rather rare fault, three-phase to ground is a balanced fault that is simple to analyze, and presents a good basis for further fault simulations. After the system has recovered approximately 80%, the fault is defined as being cleared. The fault simulations are first executed for the LCC system, then the MMC and the combined LCC-MMC system. Simulations with the MMC link are performed both without and with a DC chopper connected to the DC link.

5.1 LCC-HVDC three-phase to ground fault behavior

For a strong AC system with a SCR of more than 3, the variations in the AC voltage are relatively minor, and commutation failure rarely occurs in the converter. However, in a semi-weak AC system such as this one with a SCR of 2.59, AC variations may result in harmonic resonance, instability and frequent commutation failures [2]. It is important to investigate the inverter side of the LCC converter, as it is most vulnerable towards failure of commutation in the thyristor bridges. The AC rms voltage at the rectifier side (Tjele) is 400 kV, and 300 kV at the inverter side (Kristiansand).

Figure 5.1 presents a three-phase to ground fault characteristics of an LCC-HVDC system with a DC power level of 440 MW at 350 kV. The fault is applied at $t = 2.5\,s$ and lasts for a duration of $100ms$ (5 cycles). Figure 5.1(a) shows the AC rms voltage at the rectifier and inverter side. It is clear that a three-phase fault to ground has occurred at the inverter side, since the AC voltage drops to zero at $t = 2.5s$. After the fault duration of $0.1\,s$, the AC voltage at the inverter starts to recover, and reaches steady state roughly $0.1\,s$ after the fault has stopped. The rectifier AC voltage is almost unaffected as there is a DC link acting as a "buffer" between the connected AC systems. Next, Figure 5.1(b) shows the DC voltage. The voltage drops down to zero, indicating that failure of commutation has occurred in the thyristors at the

inverter. As a result of the DC voltage reaching zero voltage, the DC power in Figure 5.1(c) will also reduce to zero transmission during the fault. Finally, the DC current can be seen in Figure 5.1(d). The current experiences an overshoot at the beginning of the fault due to the small impedance of the cable. When the current is trying to recover, it drops to zero pu at approximately $t = 2.63\,s$. At this point, the rectifier loose all controllability of the current, which results in another current overshoot and DC voltage drop, and the inverter suffers from another failure of commutation.

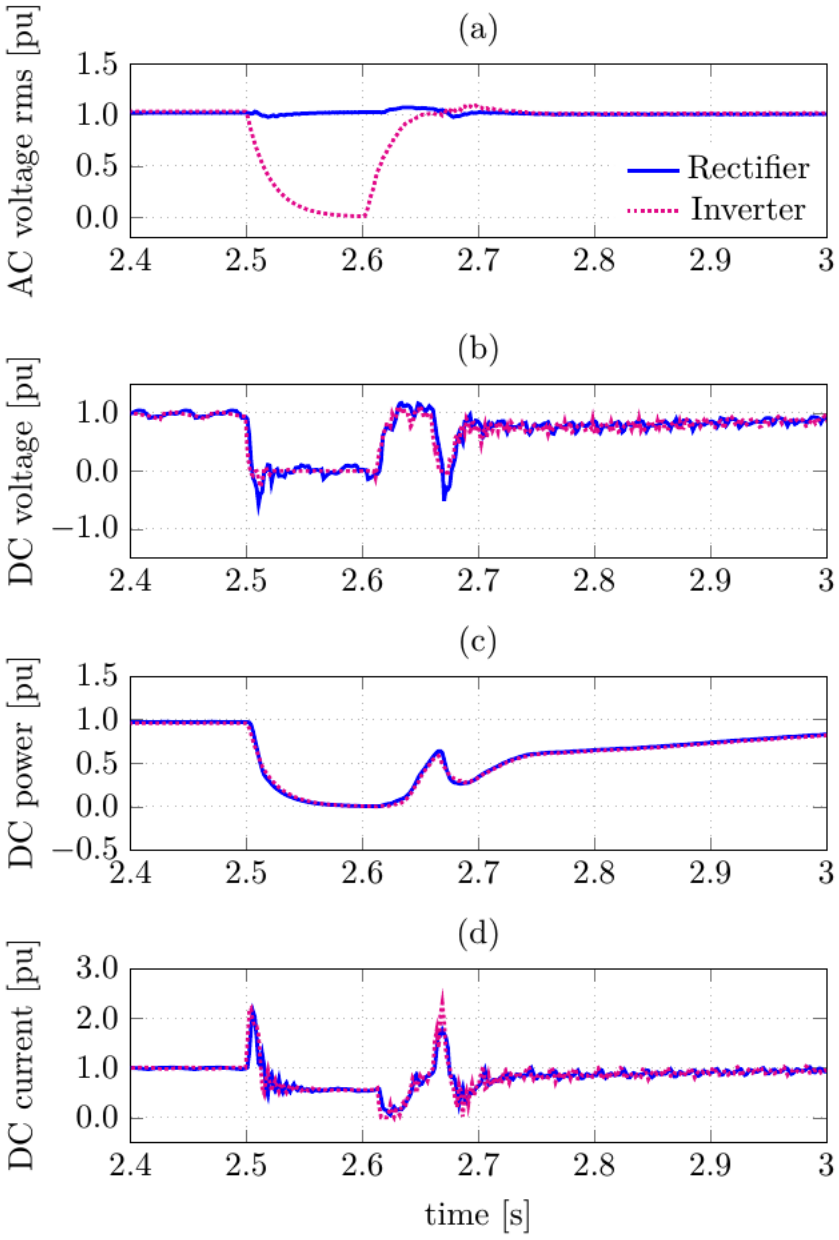


Figure 5.1: LCC system with three-phase to ground fault

Figure 5.2 presents the DC current control at the rectifier and the minimum extinction angle control at the inverter. The reference current in Figure 5.2(a) is provided by the inverter side by Voltage Dependent Current Limiter (VDCL) control. This reference value is reduced to approximately 0.5 pu during the fault, due to the drop in the DC voltage. During the fault, the rectifier current experience the same overshoots as in Figure 5.1(d). Figure 5.2(b) shows the minimum extinction angle control, with the purpose of delivering an extinction angle large enough for proper commutation of the thyristors. When the AC fault occurs at $t = 2.5\ s$, the extinction angle drops from 18° to 0° and it is evident that failure of commutation is occurring. At $t = 2.64\ s$, the commutation failure recovers, but suffers another failure from $t = 2.66\ s$ to $2.7\ s$. This double failure of commutation is a result of the severe AC fault, where the controllers loose controllability and struggle to stabilize the system after the fault.

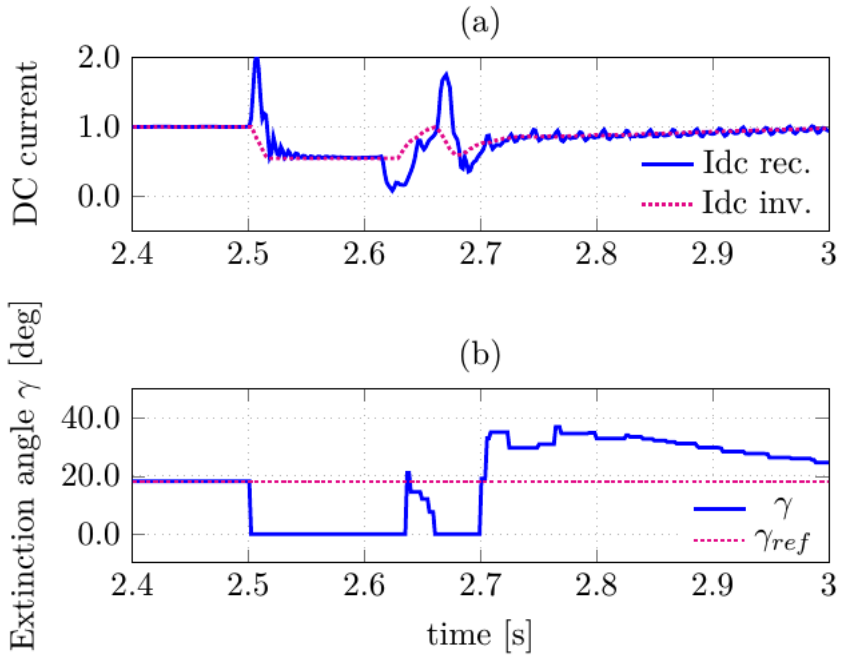


Figure 5.2: LCC control objectives at three-phase to ground fault

5.2 MMC-HVDC three-phase to ground fault behavior

The MMC-HVDC model has a power capacity of 715 MW at 500 kV DC voltage, and the AC rms voltage at the rectifier side is 400 kV, and 300 kV at the inverter side.

5.2.1 MMC without DC choppers

The simulation results from the MMC system without a DC chopper connected to the DC line, are presented in Figure 5.3. After the fault takes place, the AC voltage in Figure 5.3(a) drops to zero, as all the phases are connected to ground. When the voltage tries to recover from the fault, an overshoot at the inverter side occurs. This voltage overshoot is approximately 1.6 pu at the most, which is equivalent to 480 kV rms. This value is very high and is critical for the system. The AC voltage at the rectifier side is almost unaffected by the fault, which is as expected.

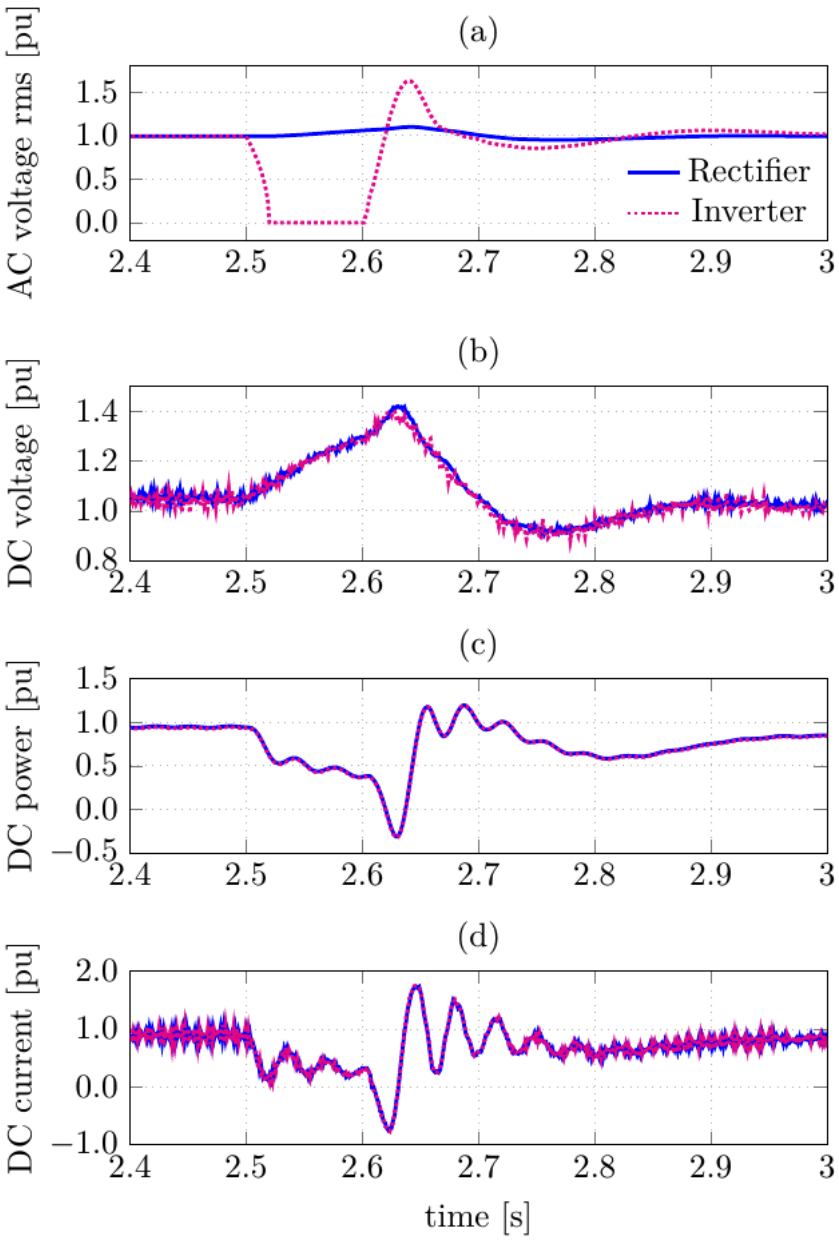


Figure 5.3: MMC system without DC chopper at three-phase to ground fault

Next, the DC voltage that can be seen in Figure 5.3(b), which has a very high

voltage top of above 1.4 pu. This is mainly because the MMC inverter is not able to control the DC voltage, so the rectifier side is still pushing power into the system. This energy is stored into the submodule capacitors, making the high DC voltage. If this is to happen in a real MMC converter, the diodes and IGBTs are in danger of burning up. A DC chopper is therefore connected to the HVDC link in subsection 5.2.2, with the purpose of reducing the DC voltage overshoot by drawing extra power, as discussed in section 3.9. Next, Figure 5.3(c) shows the DC power during the AC fault. It experiences some transient behavior and become negative and changes direction at $t = 2.63\,s$, at the same time of the AC and DC voltage overshoots. The same can be observed for the DC current in Figure 5.3(d). It becomes negative, and changes direction, which is possible in the MMC because of the bidirectional switching-pairs in the converter.

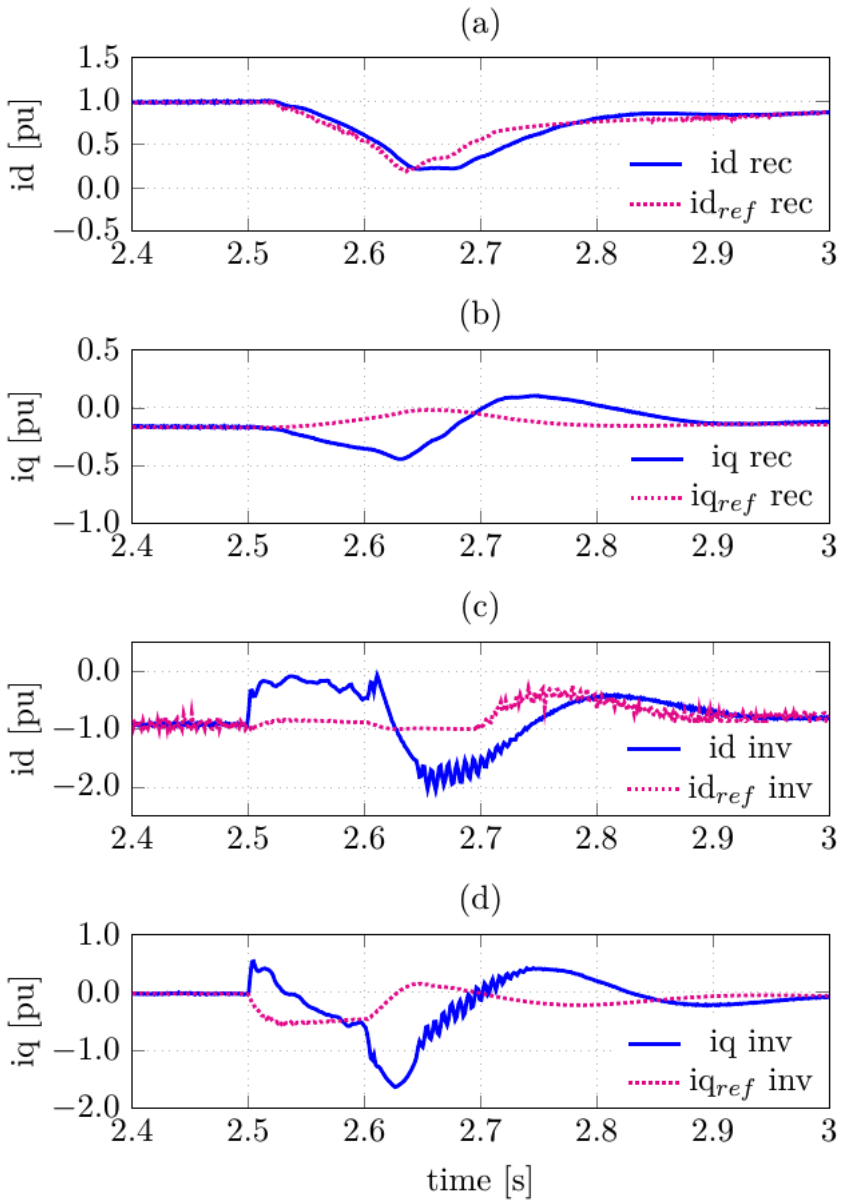


Figure 5.4: MMC control objectives at three-phase to ground fault, without DC chopper

Figure 5.4 presents the control objectives of the MMC without a DC chopper during the three-phase to ground fault. First, Figure 5.4(a) shows i_d and the reference current i_{d_ref} provided by the outer loop in order to control the DC power. Then, Figure 5.4(b) shows i_q and the reference current i_{q_ref} provided by the outer loop in order to control the AC voltage through controlling the reactive power in the system. Then, Figure 5.4(c) shows the currents at the inverter, which control the DC voltage. Finally, Figure 5.4(d) shows the inverter passive mode control, which controls the AC voltage through reactive power regulation. All the control signals experience a period of instability for a duration of approximately 0.35 s from the beginning of the fault. This is normal, because the PI-controllers are having trouble regulating the system during such an extreme fault.

5.2.2 MMC with DC choppers

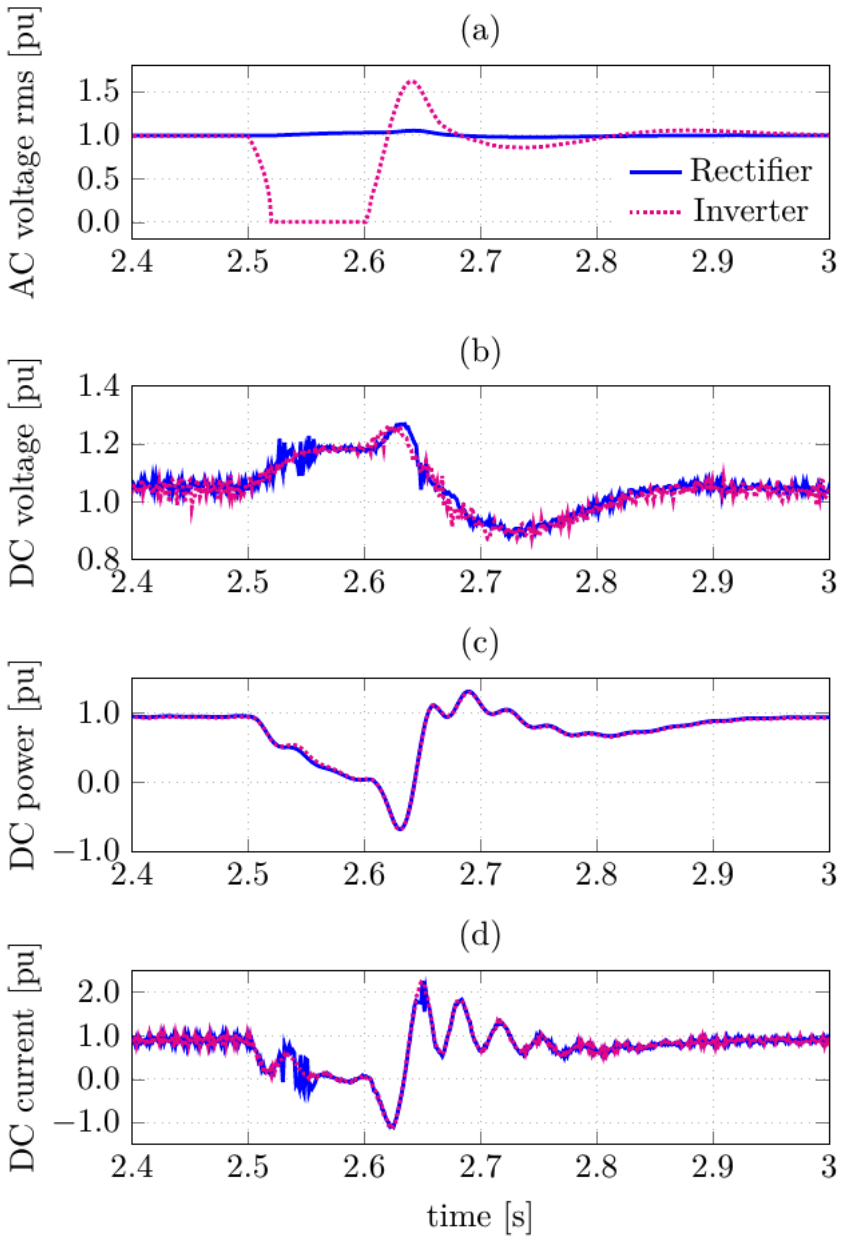


Figure 5.5: MMC system with DC chopper at three-phase to ground fault

Figure 5.5 presents the simulation results of the MMC model with a DC chopper connected to the HVDC link. The AC voltage in Figure 5.5(a) is similar to Figure 5.3(a), as the change is only applied to the DC side. A great change can be seen in Figure 5.5(b), where the DC voltage has been reduced from above 1.4 pu to a little over 1.2 pu. This value is still not optimal, and can still do damage to the converter. Selecting another DC chopper, or redirecting the power from the rectifier during the fault may improve the DC voltage increase. The DC current in Figure 5.5(d) has a slightly higher transient peak with the DC chopper, as is expected since the DC

voltage is reduced while the transmitted power is almost unaffected by the chopper.

Figure 5.6 presents the control objectives of the MMC with a DC chopper during the three-phase to ground fault. The overall control objectives in Figure 5.6 are similar to the MMC without the DC chopper, discussed in subsection 5.2.1. The only difference that can be observed is the control objectives at the rectifier side, which are less affected by the fault in Figure 5.6(a)(b) than in Figure 5.4(a)(b). Without the DC chopper, the controllers at the rectifier side become saturated and loose more controllability.

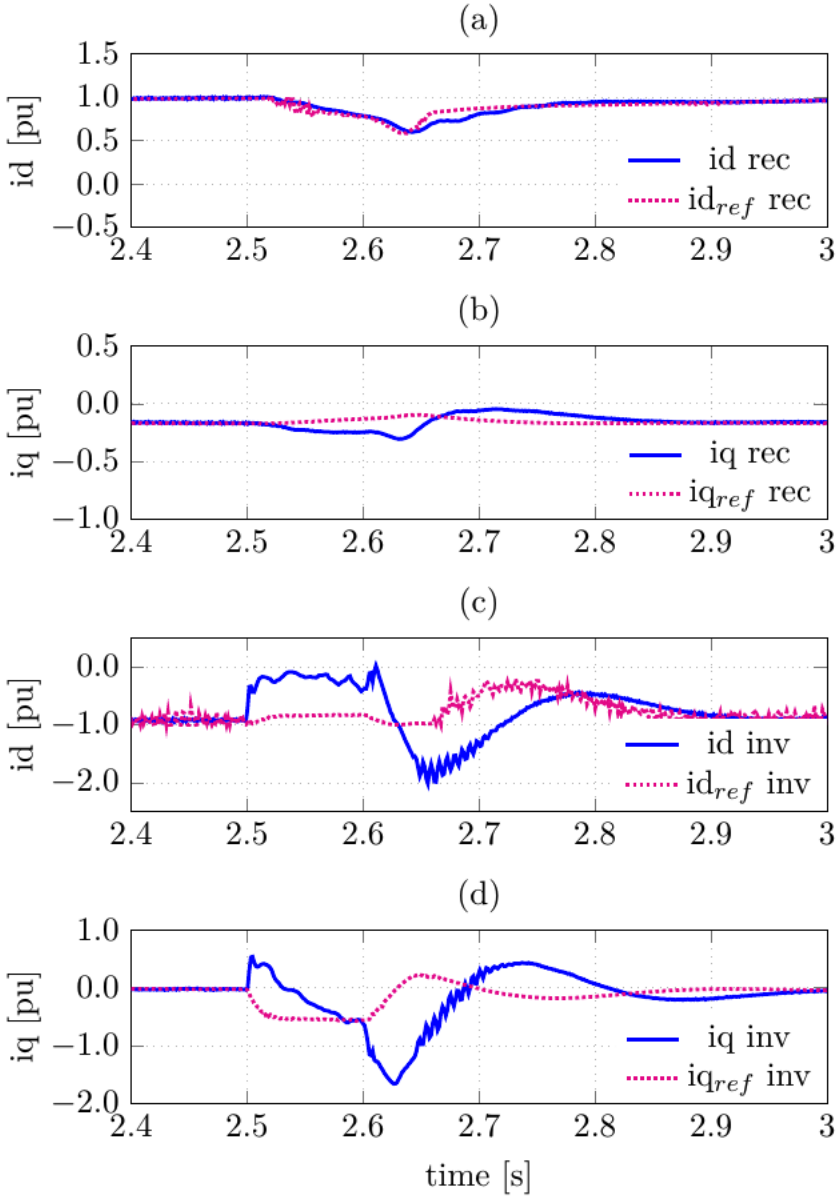


Figure 5.6: MMC control objectives at three-phase to ground fault, with DC chopper

5.3 LCC-MMC three-phase to ground fault behavior

5.3.1 LCC-MMC without DC chopper

Figure 5.7 presents the AC system of the LCC-MMC bipolar configuration, without a DC chopper connected to the MMC DC-link. The power rating of the LCC link is 440 MW at 350 kV, and for the MMC the power rating is 715 MW at 500 kV. The AC rms voltage at the rectifier side is 400 kV, and 300 kV at the inverter side. A three-phase to ground fault is applied to the AC inverter side at $t = 2.5\ s$ for a duration of 0.1 s. This can be observed in Figure 5.7(a), where the AC voltage at the inverter drops to zero for the duration of the fault. After the fault has cleared, the AC voltage at the inverter side experiences a severe voltage overshoot of around 1.5 pu. The rectifier side experiences an increase in the AC voltage as well, which is not as expected due to the DC link "buffer" in between.

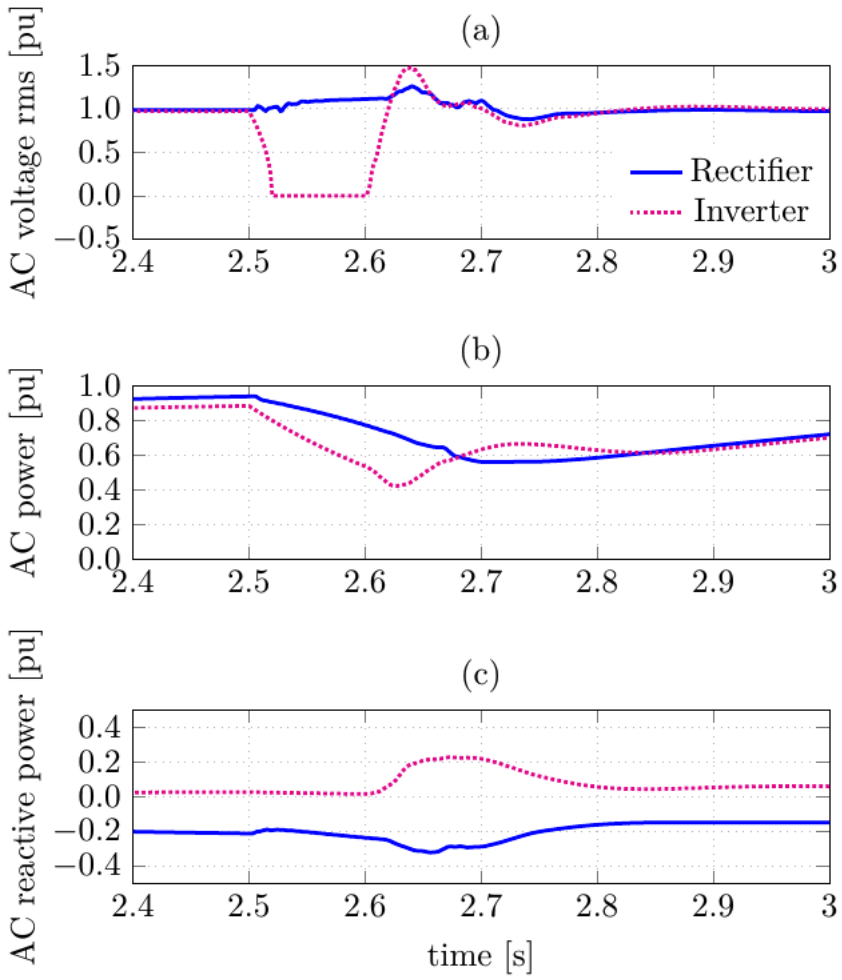


Figure 5.7: LCC and MMC AC system with three-phase to ground fault

Next, Figure 5.7(b) shows the AC power at the rectifier and inverter side. The

AC power at the inverter decreases due to the decrease in the AC voltage at the inverter. The AC power at the rectifier is also affected by the fault, because the LCC is reducing its current reference supplied to the rectifier using VDCL. The DC current order is lowered when the DC voltage is reduced, and will keep the lowered current limit during recovery. Only when the DC voltage has recovered sufficiently, will the DC current return to its original value. Finally, the reactive power can be seen in Figure 5.7(c). It starts to compensate for the change in reactive power in the system at $t = 2.62\ s$, in order to recover from the fault.

The DC simulation results during the fault are presented in Figure 5.8. The DC voltage of the LCC and MMC in Figure 5.8(a) are very similar to the results when a fault is applied to each separate model. The LCC DC voltage experience an increase in overvoltage from around 1.2 pu to approximately 1.4 pu at $t = 2.63s$, compared to Figure 5.1(b). As for the MMC, the voltage stays the same as for the MMC without DC chopper in subsection 5.2.1, which is approximately 1.4 pu. These values are critical for both systems, and will have to be reduced in order for the system to operate safely.

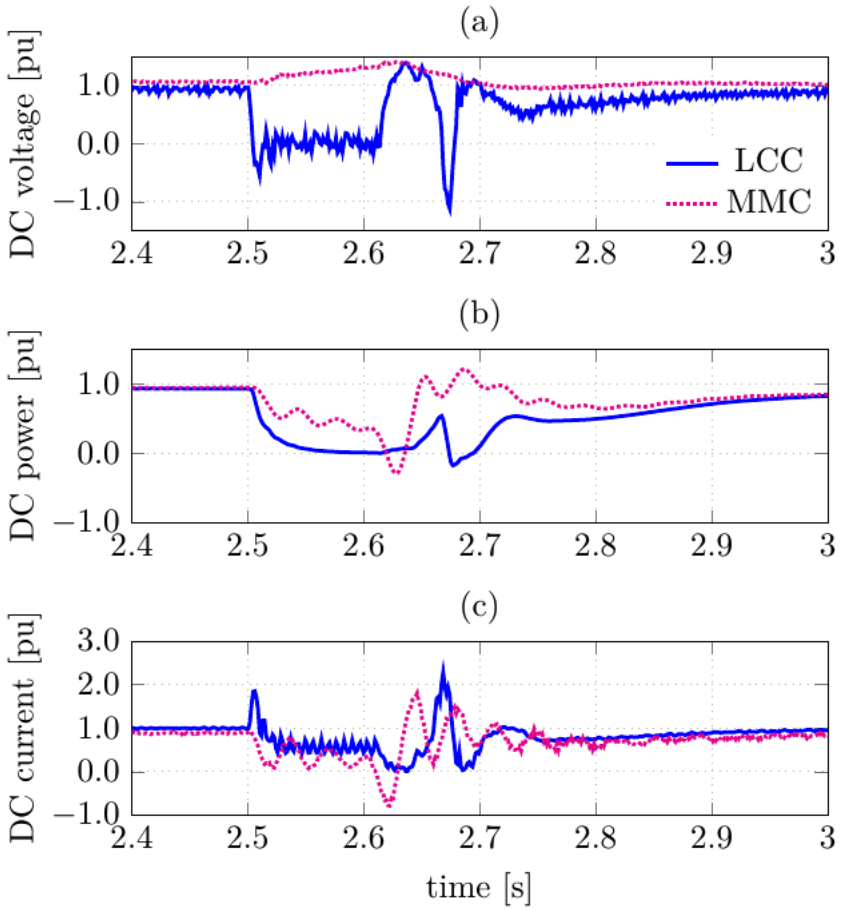


Figure 5.8: LCC and MMC DC system with three-phase to ground fault

Next, Figure 5.8(b) shows the DC power for the LCC and MMC link. The LCC DC power differ slightly from the separate LCC model in Figure 5.1(c), as the power

becomes negative at around $t = 2.68\,s$. As for the DC current in Figure 5.8(d), no changes can be observed for either the LCC or the MMC.

The LCC control objectives are presented in Figure 5.9. Figure 5.9(a) shows the DC current control at the rectifier, and Figure 5.9(b) shows the minimum extinction angle control at the inverter. Both control objectives are responding almost identical to the LCC model in Figure 5.2 during the fault. Double failure of commutation can be observed by the extinction angle of 0° in (b), from when the fault occurs at $t = 2.5\,s$ until $t = 2.7\,s$.

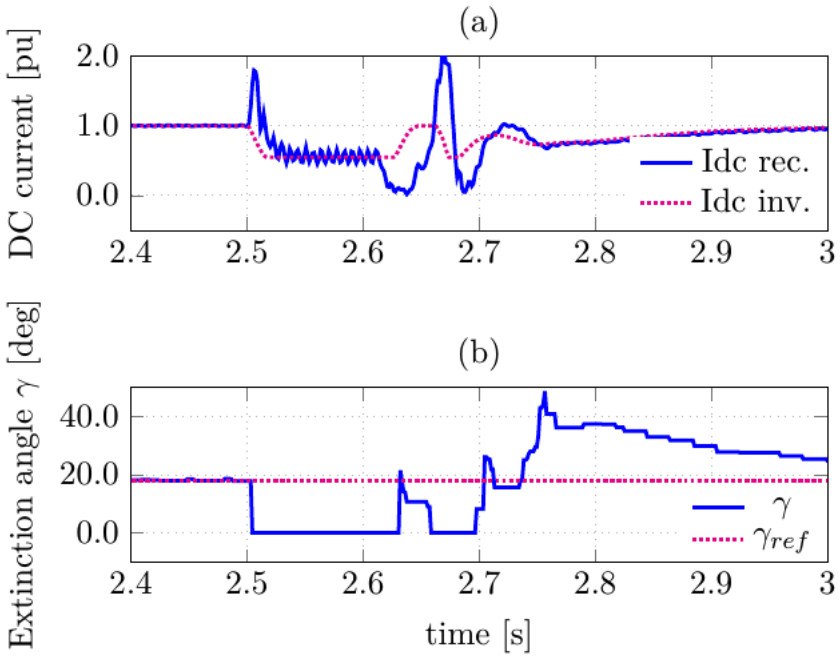


Figure 5.9: LCC control objectives at three-phase to ground fault

Figure 5.10 shows the control objectives of the MMC during the three-phase to ground fault. All the inner loop control currents are very similar to the MMC model in Figure 5.4, indicating that the MMC control system is operating in the same way even though it is connected in a bipole with the LCC. The only difference is that the currents i_d and i_q are being regulated with more fluctuations when following their respective reference values in Figure 5.10, because of the complexity of the system.

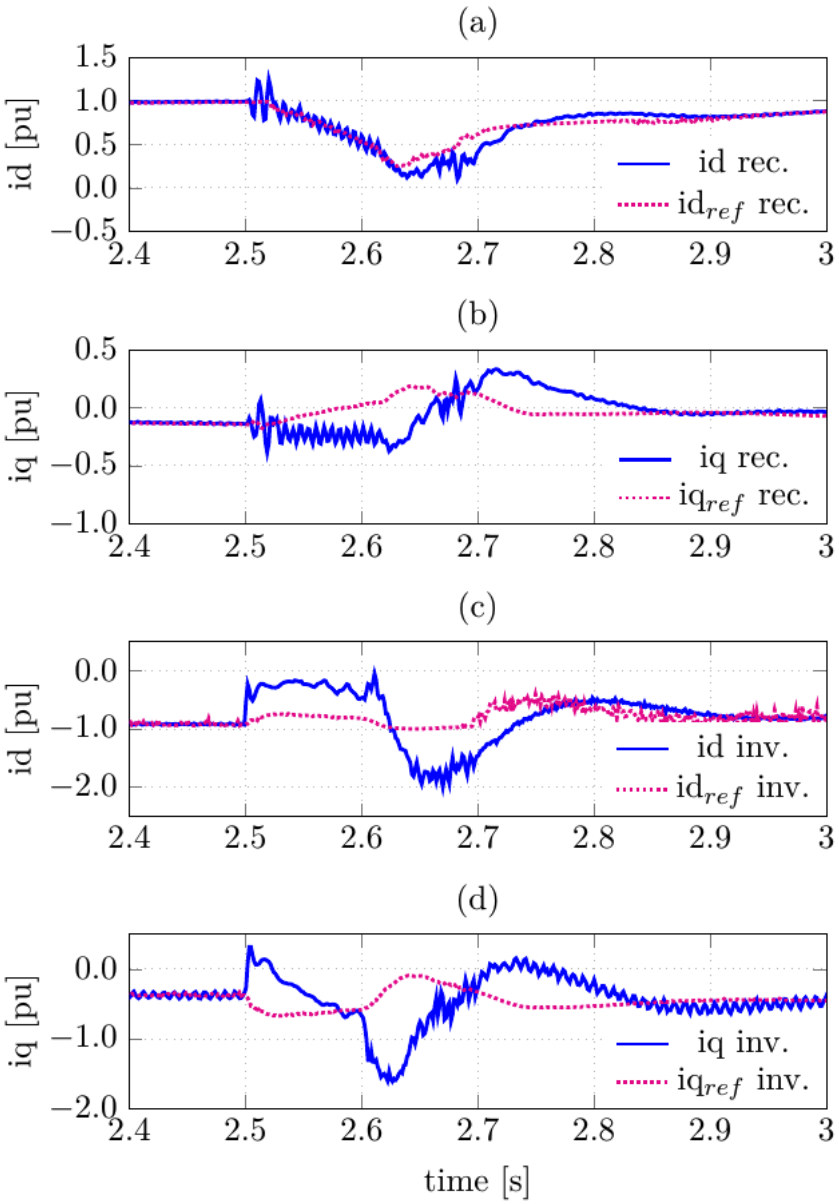


Figure 5.10: MMC control objectives at three-phase to ground fault

5.3.2 LCC-MMC with DC chopper

The three-phase to ground fault at the inverter side is now performed with a DC chopper connected to the MMC DC link. The purpose of the DC chopper is to reduce the DC voltage during the fault. Figure 5.11 shows the AC characteristics of the LCC-MMC bipolar configuration with DC chopper. As expected, the AC voltage in Figure 5.11(a) response in the same way as without the chopper seen in Figure 5.7(a). This is because the DC chopper does not affect the AC side voltage as it is connected to the DC link. Figure 5.11(b) shows the AC power at the rectifier and inverter side. There is a slight reduction in the drop of AC power at the rectifier side from roughly 0.5 pu to 0.7 pu. Finally, the AC reactive power can be seen in (b), which is operating as expected by balancing the reactive power in the system.

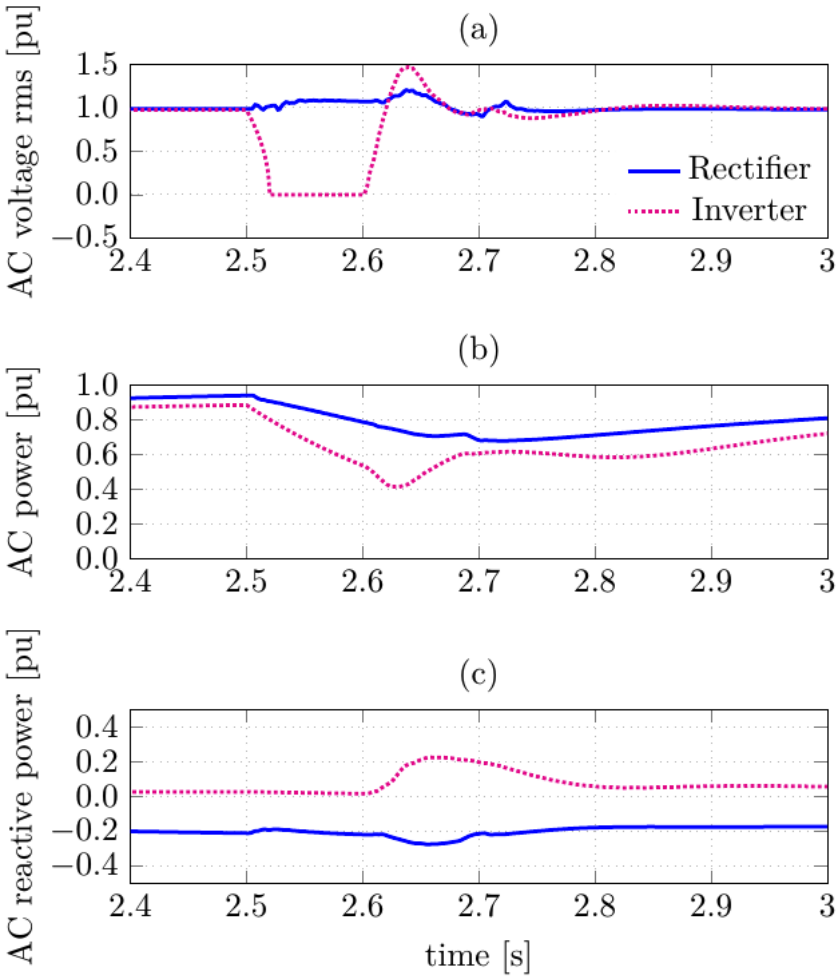


Figure 5.11: LCC-MMC AC system with DC chopper and three-phase to ground fault

Figure 5.12 shows the DC values of the LCC-MMC system during the fault. First, Figure 5.12(a) shows the DC voltage at the LCC and MMC link. The MMC DC voltage overshoot has been reduced from approximately 1.4 pu to 1.25 pu at $t = 2.63\,s$ due to the DC chopper. The DC chopper has not affected the LCC DC voltage overshoot, as it is connected at the MMC side. However, the negative voltage at $t = 2.7\ s$ is not as severe as without the chopper and is reduced from -1.25 pu to -1.0 pu. Next, Figure 5.12(b) shows the DC power at each HVDC link. Compared to Figure 5.8(b), the LCC power does not become negative and, thus, does not change direction at $t = 2.68\ s$. The MMC DC power remains seemingly unaffected. Finally, the DC current can be seen in Figure 5.12(c). The current in the LCC has been reduced at $t = 2.69\ s$ from 2.5 pu to 2.0 pu. The current in the MMC is more or less identical to the current in Figure 5.8(c) with no DC chopper.

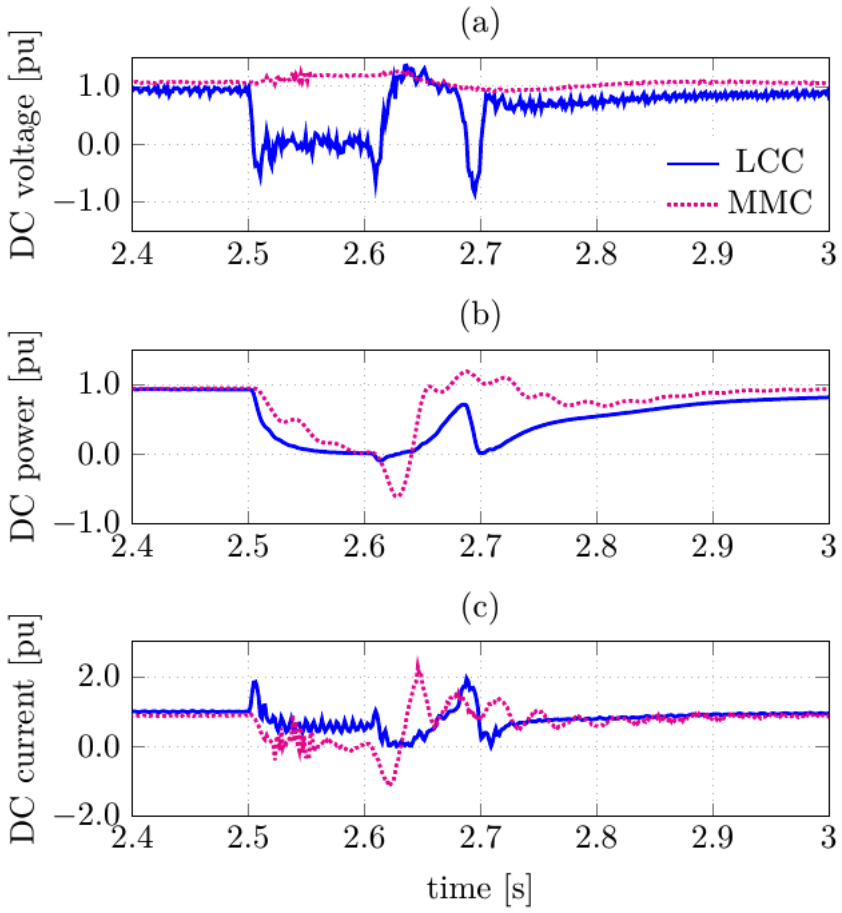


Figure 5.12: LCC-MMC DC system with DC chopper and three-phase to ground fault

Figure 5.13 presents the control objectives of the LCC converter during the three-phase to ground fault. First, Figure 5.13(a) shows the DC current control at the rectifier. Compared with the system without a DC chopper in Figure 5.9(a), the recovery time after the fault has increased from around $t = 2.7\ s$ to $t = 2.73\ s$. The same tendency can be seen in Figure 5.13(b), which shows the minimum extinction angle control at the inverter. The commutation failure in the inverter thyristor bridge last until $t = 2.73\ s$ as well. This means that adding the DC chopper at the MMC-HVDC link actually increases the duration of failure of commutation in the LCC inverter.

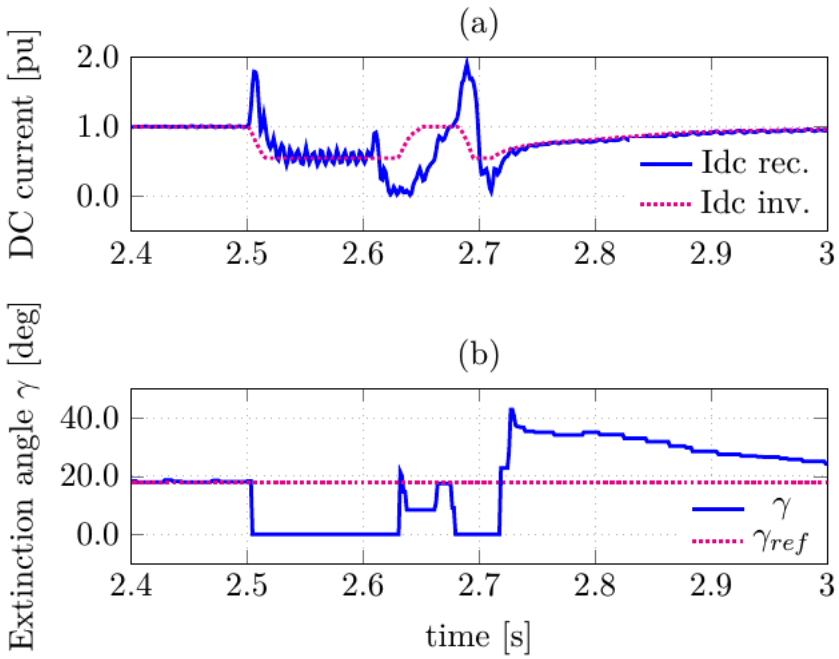


Figure 5.13: LCC control objectives at three-phase to ground fault

Figure 5.14 shows the control objectives at the rectifier and inverter side of the MMC. All the reference currents remain unchanged from Figure 5.10 after connecting the DC chopper. There is one small exception in the reference current, i_{d_ref}, in Figure 5.14(a), as it does not reduce as much during the fault. It is because the controllers at the rectifier do not loose as much controllability now that the DC voltage is reduced during the fault.

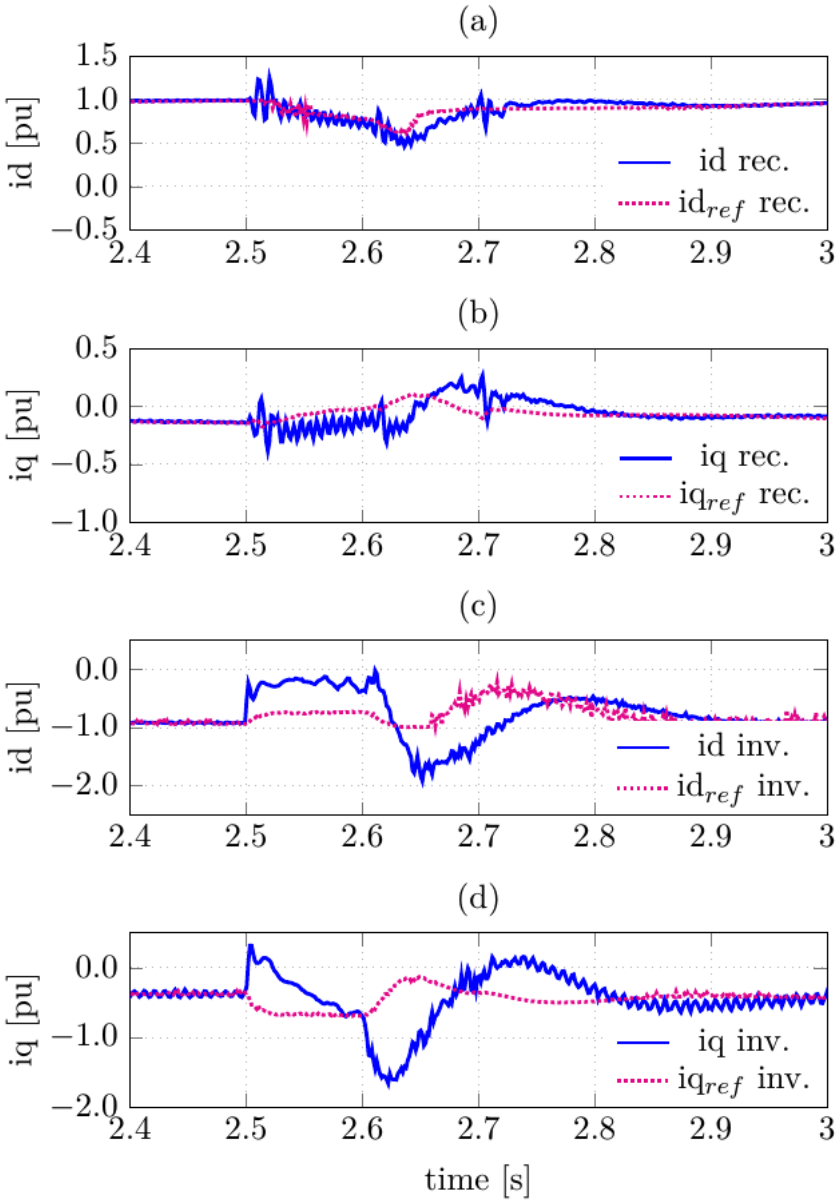


Figure 5.14: MMC control objectives at three-phase to ground fault

5.4 Summary

A three-phase to ground fault at the AC inverter side is simulated in this chapter. From the theory, it is expected that failure of commutation will occur in the LCC inverter side, due to the reduction of the AC voltage. A double failure of commutation can clearly be observed in the LCC simulation, as the controllers are loosing controllability of their respective objectives.

The MMC model is first simulated without a DC chopper and then with one. The result is a lowered DC voltage from approximately 1.4 pu to 1.2 pu during the fault, meaning that the DC chopper serves its purpose. The DC voltage may decrease even more by selecting a different DC chopper, or redirecting the power from the rectifier during the fault.

Finally, the two models are combined in a bipolar configuration, both with and without a DC chopper at the MMC side. The MMC DC voltage decreases with the DC chopper, in the same way as when the system is not connected to the LCC. However, adding the DC chopper increases the period with failure of commutation in the LCC inverter by $0.02\,s$. Apart from this, the two systems are almost operating as induvidual systems, but with the MMC providing the reactive power.

Based on the simulations, it can be concluded that the bipolar configuration does not need any addtitional protection systems. The same protection requirements for the monopolar LCC and monopolar MMC should be sufficient for the combined system.

Chapter 6

AC Fault –Single-Phase to Ground

In this chapter, a single-phase to ground fault is applied to the AC inverter side of the system. This type of fault is unbalanced, which means that there will be some unsymmetrical responses in the system due to the fault. The fault is first applied to the LCC system, then the MMC system, and finally to the LCC-MMC bipolar configuration. The AC systems for all the different configurations have the AC rms rated voltage of 400 kV at the rectifier side and 300 kV at the inverter side.

6.1 LCC-HVDC single-phase to ground fault behavior

The LCC-based HVDC link is designed for a capacity of 440 MW at 350 kV. A single-phase to ground fault is applied at the AC inverter side of the HVDC system at $t = 2.5s$ for a duration of $100ms$. The fault is applied at the inverter side, because the thyristor bridge at the inverter is vulnerable towards failure of commutation when the AC voltage is reduced. Figure 6.1 presents the characteristics of the system during the fault. First, Figure 6.1(a) shows the AC rms voltage at the rectifier and inverter side. The inverter side voltage drops to approximately 2/3 pu of the steady state value of 1 pu during the fault. This is expected, since one of the three phases are connected to ground at this point. After the fault has cleared at $t = 2.6\ s$, the inverter side voltage starts to increase again, and reaches 1 pu at $t = 2.65\ s$. The rectifier voltage is almost unaffected, due to the DC link in between. Next, Figure 6.1(b) shows the DC voltage. When the fault occurs at $t = 2.5\ s$, the DC voltage drops to -1 pu before oscillating around 0.0 pu. It is clear that the AC voltage drop has resulted in commutation failure in the inverter. After the fault is cleared at $t = 2.6\ s$, the DC voltage recovers and reaches nominal value at around $t = 2.8\ s$. Compared to the three-phase to ground fault in Figure 5.1(b), the DC voltage at single-phase to ground have a lot more harmonics during the fault. This is a result of the unbalanced fault, and is expected. Next, Figure 6.1(c) shows the DC power during the fault. Since the DC voltage reduces to zero, the power transmitted will also be zero during the fault. At $t = 2.63\ s$, the DC power starts increasing again,

and have fully recovered at $t = 2.9\,s$. Finally, the DC current can be seen in Figure 6.1(d). The current experiences an overshoot at the beginning of the fault due to the small impedance of the cable. At $t = 2.52\,s$, the current starts to oscillate around 0.5 pu, before is recovers at $t = 2.75\,s$. The high content of harmonic disturbance in the DC current is also a result of the unbalanced fault.

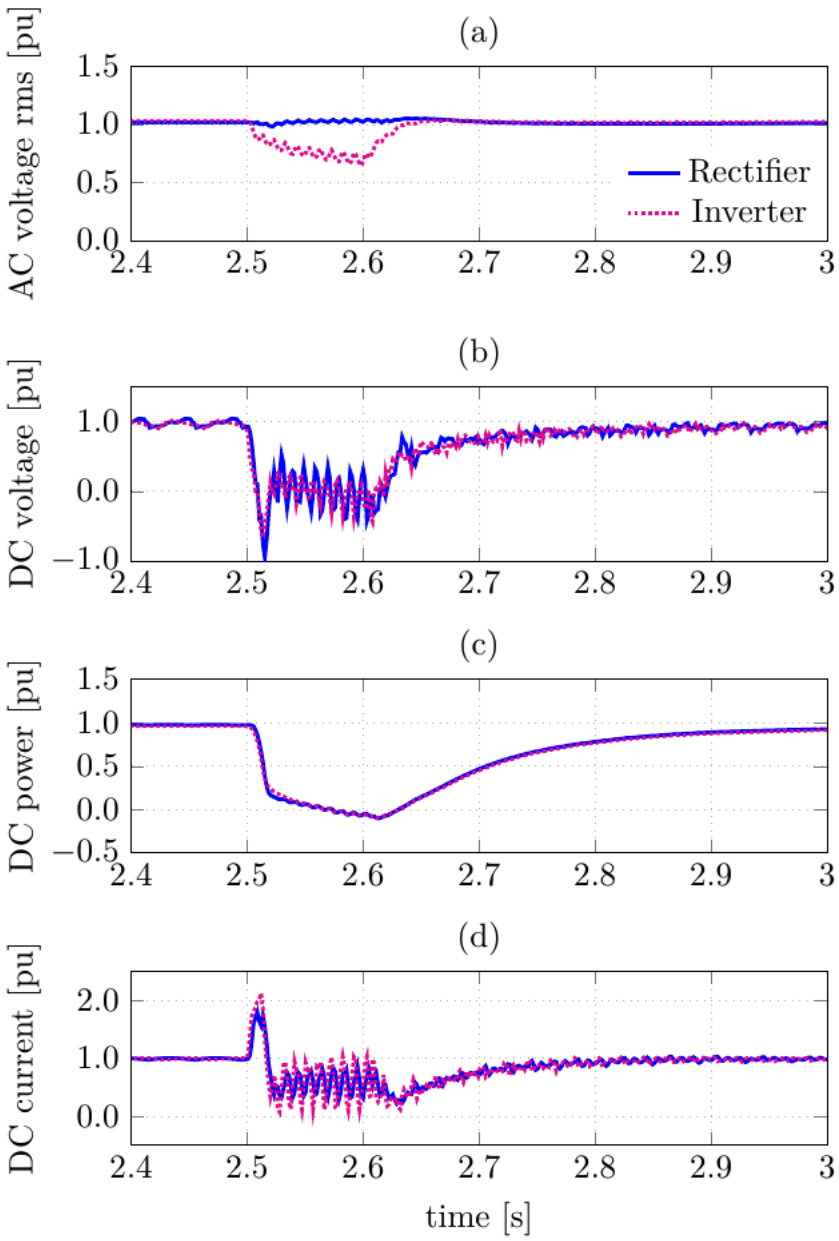


Figure 6.1: LCC-HVDC system with single-phase to ground fault

Figure 6.2 presents the control objectives of the LCC at the rectifier and inverter side during a single-phase to ground fault. Figure 6.2(a) shows the DC current control at the rectifier side, where the reference current is provided by the inverter side through Voltage Dependent Current Limiter (VDCL) control. The DC voltage decreases to around zero during the fault, resulting in a decrease in the reference current provided

to the rectifier. After the fault is cleared, the reference current regains its steady state value, and the DC current at the rectifier follows the reference value. Figure 6.2(b) shows the minimum extinction angle control at the inverter. The reference value (γ_{ref}) is set to 18°, in order to avoid failure of commutation in the inverter. When the fault occurs at $t = 2.5\,s$, the extinction angle drops to 0°, and it is evident that failure of commutation has happened. $0.02\,s$ after the fault is cleared, the angle increases quickly to 70° before stabilizing at 18° again at $t = 3\ s$. Compared to the three-phase to ground fault in section 5.1, the system recovers a lot faster with just a single-phase to ground fault. The three-phase to ground fault results in a double failure of commutation and the system does not recover until $t = 2.7\,s$. The single-phase to ground, however, recovers at $t = 2.62\,s$.

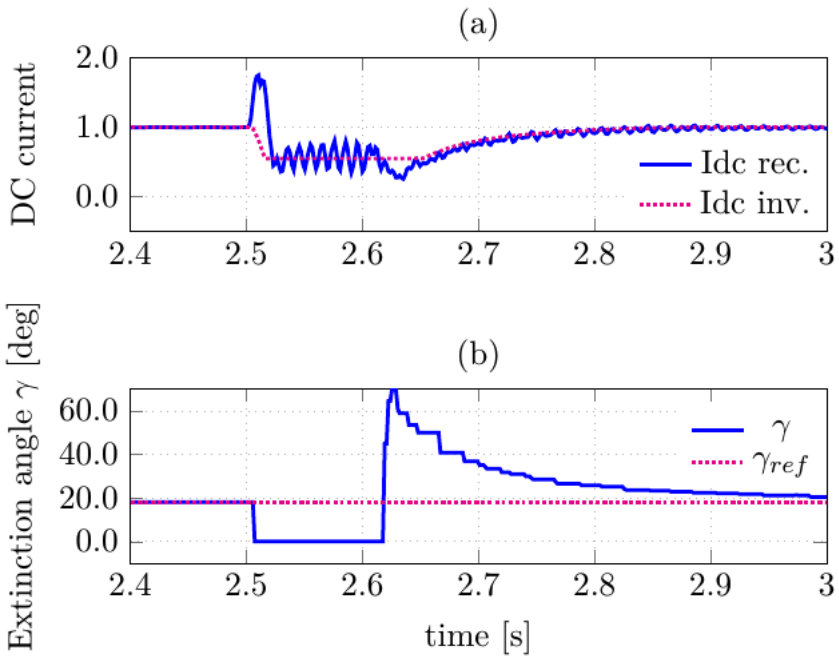


Figure 6.2: LCC control objectives at single-phase to ground fault

6.2 MMC-HVDC system with single-phase to ground fault at the inverter side

The MMC-HVDC link has a nominal capacity of 715 MW at 500 kV. In this section, there is a DC chopper connected to the DC link, and the characteristics of the system without the DC chopper can be found in Appendix D, subsection D.1.1. Figure 6.3 presents the characteristics of the MMC-HVDC link during a single-phase to ground fault. First, Figure 6.3(a) shows the AC rms voltage at the rectifier and inverter side. The AC voltage at the inverter side drop to around 0.7 pu during the fault from $t = 2.5\,s$ to $t = 2.6\,s$. This is approximately 2/3 of the steady state value, due to the grounding of one phase. The inverter voltage then experiences a small overshoot of approximately 1.2 pu after the fault is cleared. The rectifier AC voltage is unaffected

by the fault. Next, Figure 6.3(b) shows the DC voltage, which experiences a small increase of approximately 0.18 pu during the fault. The voltage ripple is normal for MMC operation, and can be reduced by improving the modulation technique or placing a large capacitor across the submodules. Because of the unbalanced fault, the rectifier DC voltage has more harmonics during the fault than at steady state.

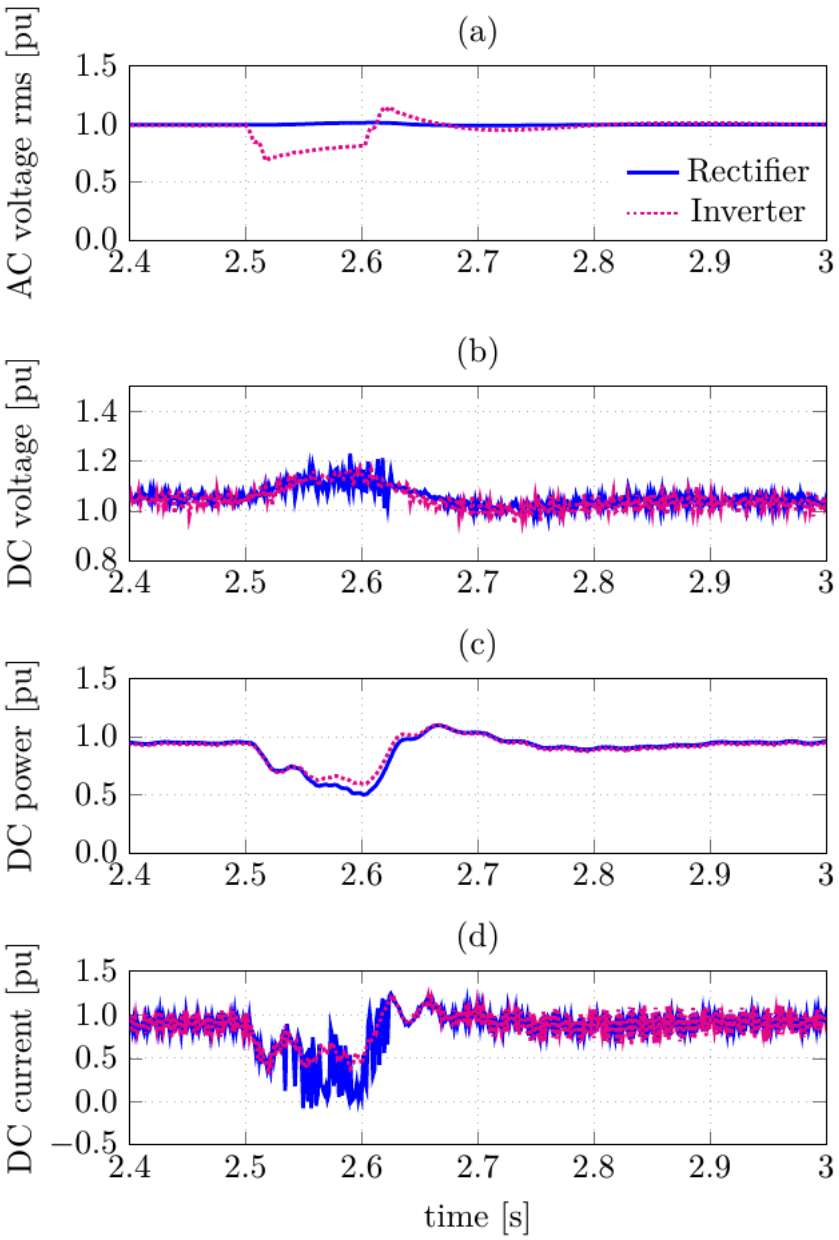


Figure 6.3: MMC-HVDC system with single-phase to ground fault

Next, Figure 6.3(c) shows the DC power during the AC fault. The increase in the DC voltage is due to overmodulation of the control signal at the rectifier. The power controller experience saturation, and loose some controllability of the DC power. This is the reason for the DC power decrease from the occurrence of the fault at $t = 2.5\ s$, until the fault is cleared at $t = 2.6\ s$. The power then starts to increase

and stabilizes at approximately 1 pu. Finally, Figure 6.3(d) shows the DC current at the rectifier and inverter side. It decreases along with decreasing power. There are a lot of harmonics in the current during the fault, created by the unbalanced fault.

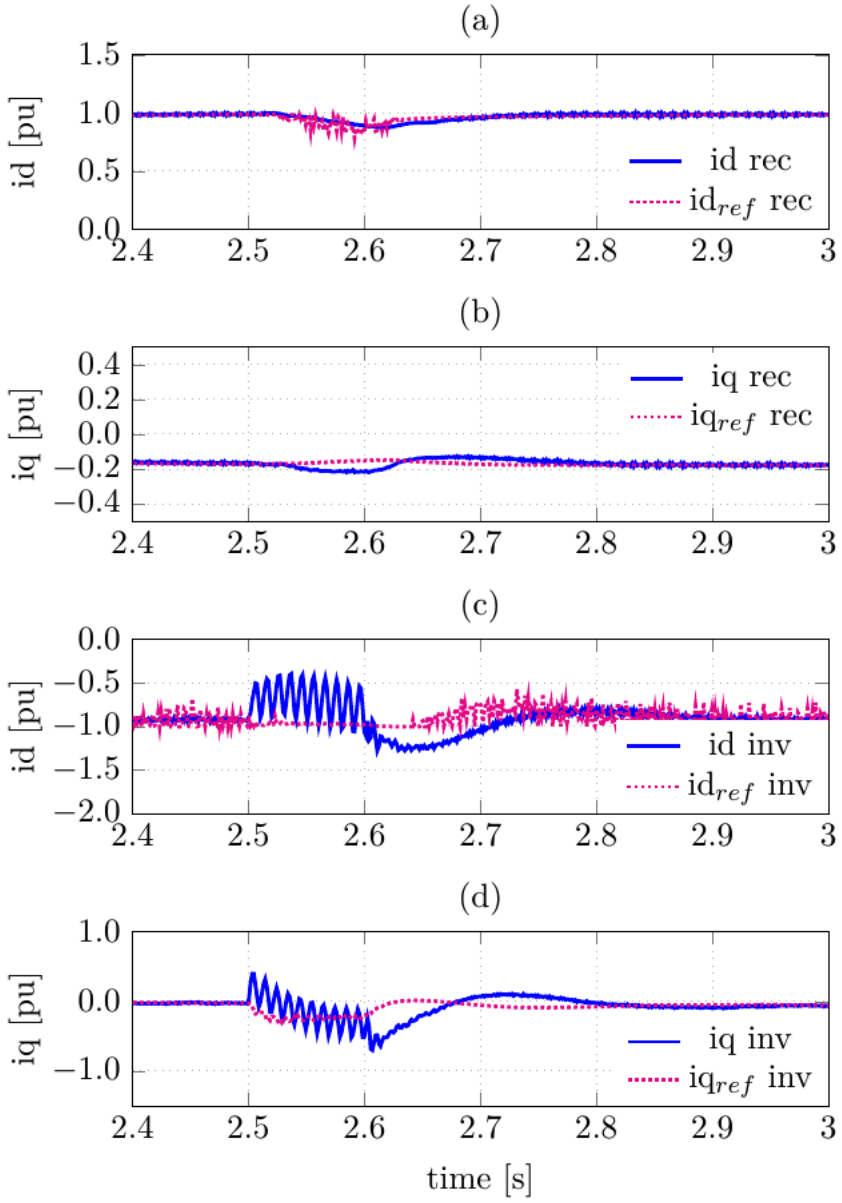


Figure 6.4: MMC control objectives at single-phase to ground fault

Figure 6.4 presents the dynamic behavior of the system current at the rectifier and inverter side of the MMC-HVDC system. Figure 6.4(a) shows i_d and the reference current i_{d_ref} provided by the outer loop in order to control the DC power. The control objective is almost unaffected by the fault, and hardly looses any of the controllability. The same can be observed for Figure 6.4(b), which is the other inner control loop at the rectifier, which regulates the AC voltage through controlling the reactive power in the system. Next, Figure 6.4(c) shows the current at the inverter

which controls the DC voltage. The controller looses some of its controllability, but quickly recovers after the fault. The same can be observed in Figure 6.4(d), where the current regulates the AC voltage at the inverter side through reactive power control.

6.3 LCC-MMC single-phase to ground fault behavior

In this section, the two systems from section 6.1 and 6.2 are combined into an LCC-MMC bipolar configuration. The AC system at the rectifier side has an AC rms voltage of 400 kV, and 300 kV at the inverter side. There is a DC chopper connected to the MMC DC link, and the characteristics of the system without the DC chopper can be found in Appendix D, subsection D.1.2. There are no filters connected to the converter stations, as the MMC is able to provide the system with reactive power. Only a shunt capacitor of 8 μF is placed at the rectifier station.

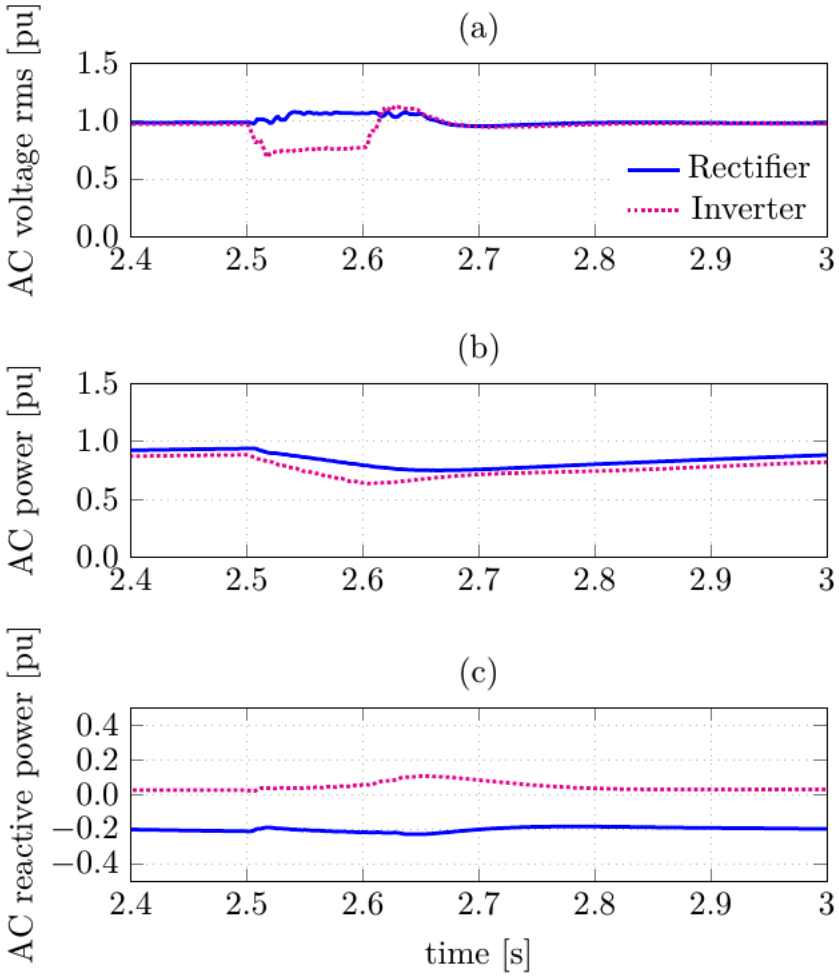


Figure 6.5: LCC-MMC AC system at single-phase to ground fault

Figure 6.5 presents the AC characteristics of the system at the rectifier and inverter side. First, Figure 6.5(a) shows the AC rms voltage at both AC systems. The fault occurs at the inverter side at $t = 2.5\,s$, and can be observed in the simulation where the inverter voltage decreases to approximately 2/3 pu. The rectifier AC voltage is slightly affected by the fault, even though the DC line in between the stations acts as a buffer for the fault. At $t = 2.66\,s$, the voltages have recovered and are back to normal operating values of 1 pu. Next, Figure 6.5(b) shows the AC power at the rectifier and inverter side. The AC power at the inverter decreases to roughly 0.6 pu at $t = 2.6\,s$, before slowly recovering again. This response is due to the reduction in the AC voltage at the inverter. The AC power at the rectifier is also affected by the fault, because the LCC is reducing its current reference supplied to the rectifier using VDCL. Finally, the reactive power can be seen in Figure 6.5(c). The MMC starts providing some reactive power after the fault at $t = 2.6\,s$, in order for the system to recover.

Figure 6.6 presents the DC characteristics of the LCC-MMC system. First, Figure 6.6(a) shows the DC voltage at the LCC and MMC link. Both systems are responding to the fault in the same way as when they are separate in sections 6.1 and 6.2. The harmonics in the DC voltages during the fault are a result of the unsymmetrical fault applied, which generates harmonic disturbance. Next, Figure 6.6(b) shows the DC power. Again, the simulations are almost identical to the simulations of the separate models. Finally, the DC current can be seen in Figure 6.6(c). The currents are also identical, and it is evident that the two systems are operating independently of each other.

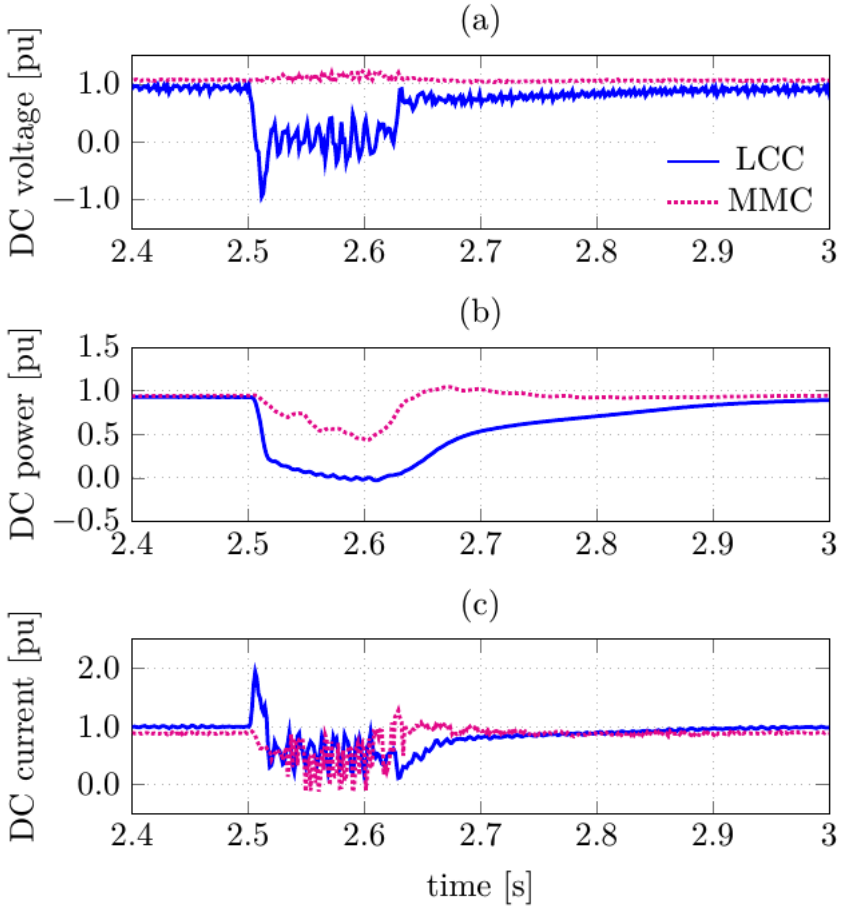


Figure 6.6: LCC-MMC DC system at single-phase to ground fault

Figure 6.7 presents the control objectives of the LCC during the single-line to ground fault. First, Figure 6.7(a) shows the DC current control at the rectifier, where the reference current is supplied by the inverter side by VDCL control. The currents are very similar to the ones in Figure 6.2(a), which is the current control of the LCC system alone. The only difference is a bit higher fluctuations in the combined system. Figure 6.7(b) shows the minimum extinction angle control at the inverter, where $\gamma_{min} = 18°$. During the fault, the extinction angle is reduced to 0° and failure of commutation occurs in the inverter. When the fault is cleared at $t = 2.6\ s$, the angle increases slightly, before recovering at $t = 2.62\ s$.

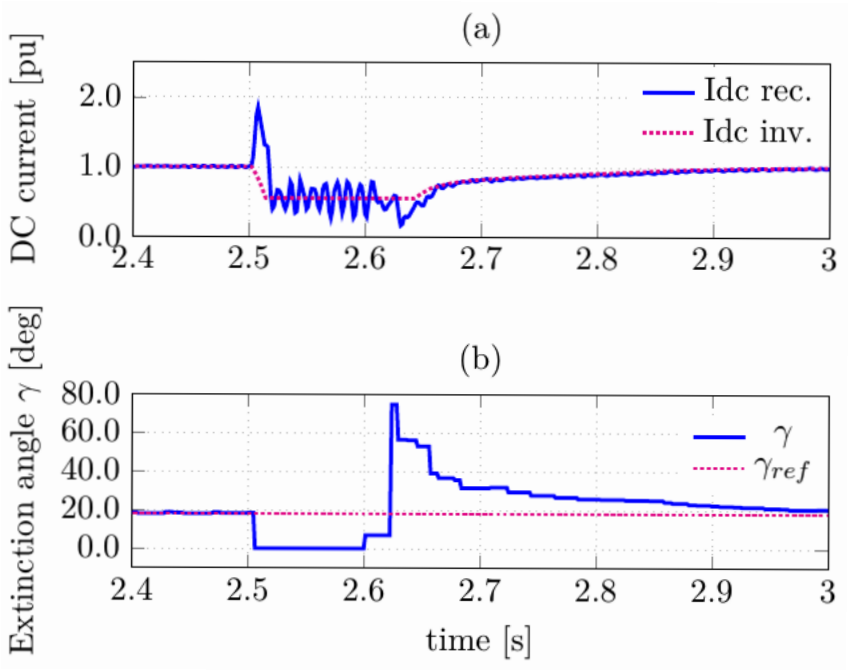


Figure 6.7: LCC control objectives at single-phase to ground fault

Figure 6.8 presents the MMC control objectives for the LCC-MMC system. First, Figure 6.8(a) shows the active power control at the rectifier, and Figure 6.8(b) shows the AC voltage control at the rectifier side. Figure 6.8(c) and (d) show the DC voltage control and AC voltage control at the inverter side, respectively. All the reference currents supplied by the outer loop are identical to the ones in Figure 6.4, where the MMC-HVDC link is simulated alone. The system currents are also very similar, but contain more harmonic disturbance during the fault in the combined model.

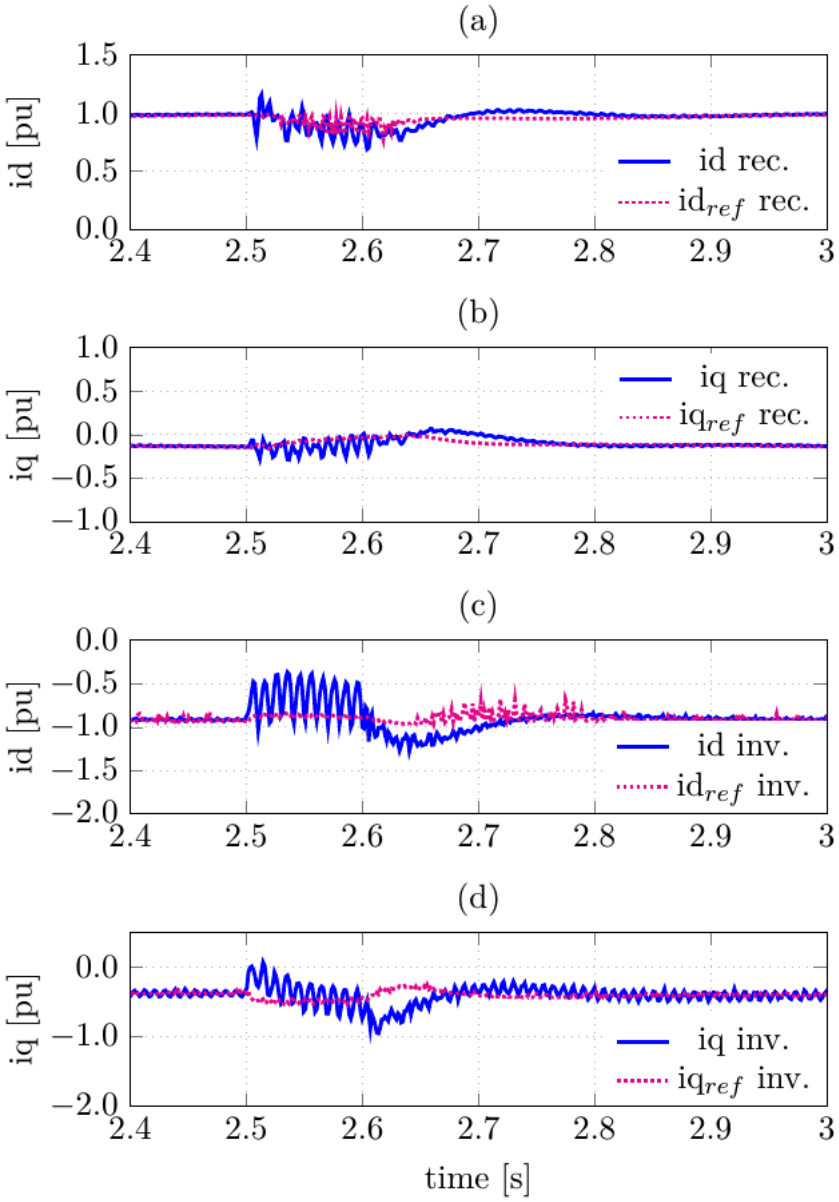


Figure 6.8: MMC control objectives at single-phase to ground fault

6.4 Summary

A single-phase to ground fault is applied at the AC inverter side of the three simulation models. Since the fault only occurs at one of the phases, it is an unbalanced fault. The LCC model experiences failure of commutation during the fault due to the reduction in the inverter AC voltage. As a result, the DC voltage is reduced, and the reference current sent to the rectifier controller is lowered. The DC voltage and DC current have a high content of harmonic disturbance during the fault, due to the unsymmetrical response of the fault.

The MMC model experiences a DC voltage increase of approximately 0.18 pu during

the fault. Due to some loss of controllability in the power controller, the DC power and current are reduced to 0.5 pu during the fault. The DC voltage and current have a high content of harmonic disturbance, as a result of the unbalanced fault. The reference currents supplied by the outer control loop are almost unaffected by the fault, while the system currents fluctuates during the fault.

At the end, the two systems are combined in an LCC-MMC bipolar configuration. The LCC and MMC systems are almost unaffected by each other during the fault, and it is evident that the two systems operate independently. The same harmonic disturbances during the fault are still present, and may even be a bit more exaggerated in the bipolar configuration. It can be concluded based on the simulations that the bipolar configuration does not require additional protection systems. The same protection for the monopolar LCC and the monopolar MMC systems should be sufficient.

Chapter 7

DC Fault –Pole to Ground

In this chapter, a DC pole to ground fault is applied to the LCC and the MMC DC-link. In the last section (section 7.3), the LCC and MMC systems are connected and the fault is applied at each cable, making it possible to observe how the combined system reacts to the different situations. It is interesting to see if the other HVDC system can give support to the DC link with fault if necessary.

7.1 LCC-HVDC Pole-to-Ground DC fault behavior

The LCC-HVDC link has a power capacity of 440 MW at a DC voltage of 350 kV. The AC rms voltage at the rectifier side is 400 kV, while at the inverter side the AC rms voltage is 300 kV. Figure 7.1 presents the characteristics of the LCC-link during the DC pole to ground fault, which is applied at $t = 2.5\,s$ for $0.1\,s$. First, Figure 7.1(a) shows the AC voltage at the rectifier and inverter side. The inverter voltage experiences a small voltage increase of around 1.1 pu when the fault occurs, while the rectifier side is almost unaffected. Second, Figure 7.1(b) shows the DC voltage at both sides. The fault occurs at the inverter side, and as expected, the inverter DC voltage drops to zero at the instant of the fault. However, after the fault is cleared at $t = 2.6\,s$, the voltage does not recover to the steady state value and remains at zero. At $t = 2.5\,s$, the DC voltage at the rectifier drops to -1.0 pu before fluctuating around 0.0 pu. Next, Figure 7.1(c) shows the DC power at both sides of the HVDC link. As a result of the DC voltage becoming zero, there is no power transmitted in the HVDC system. Finally, the DC current can be seen in Figure 7.1(d). At the inverter side, the current drops to zero at the moment of the fault, but recovers to approximately 0.5 pu of the nominal value. The current at the rectifier experiences a current overshoot of roughly 2.6 pu when the fault occurs, before settling at approximately 0.6 pu. Although the inverter experience saturation, the rectifier is still controlling the expected current. The rectifier current overshoot is probably the reason why the system is not able to recover from the fault. The large overcurrent saturates the voltage controller, which does not utilize anti-windup PI

controllers.

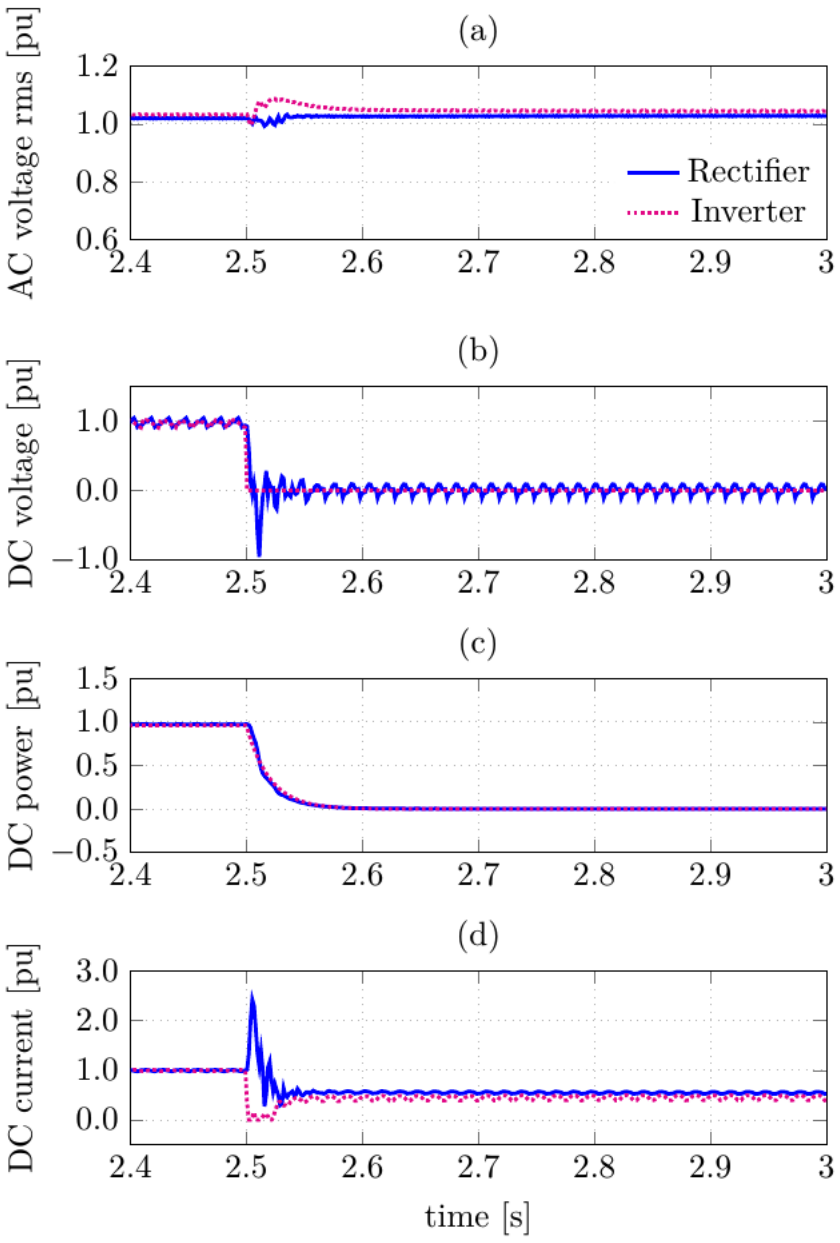


Figure 7.1: LCC system with DC fault to ground

Figure 7.2 illustrates the control objectives of the LCC during the DC fault. Figure 7.2(a) shows the DC current control at the rectifier, where the reference current is supplied by the inverter side through VDCL control. The reference current drops to approximately 0.5 pu after the fault because of the decrease in DC voltage. Figure 7.2(b) shows the minimum extinction angle control at the inverter. Approximately 0.02 s after the occurrence of the fault, the extinction angle (γ) reaches almost 90° and saturates. From Eq. 2.5, $\alpha = 180° - (\mu + \gamma)$, and when $\gamma \approx 90°$, then $\alpha \approx 90°$. From Figure 2.7, $V_{dc} = 0$ pu at this angle, which corresponds to Figure 7.1(b).

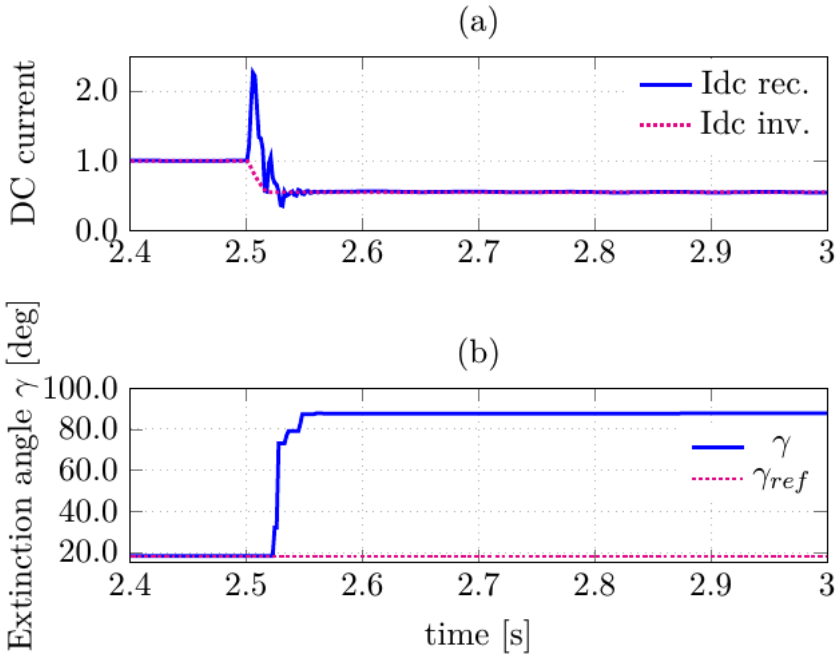


Figure 7.2: LCC control objectives at DC fault to ground

7.2 MMC-HVDC pole-to-ground DC fault behavior

The MMC-HVDC link has a nominal power capacity of 715 MW at 500 kV DC voltage. The AC networks are the same as for the LCC, with an AC rms voltage of 400 kV at the rectifier side and 300 kV at the inverter side. Figure 7.3 presents the characteristics of the MMC system during the DC to ground fault at the inverter side. First, Figure 7.3(a) shows the AC rms voltage at the rectifier and inverter during the fault. At both sides, the AC voltage drop down to approximately 0.6 pu after the fault, but starts to recover at $t = 2.64s$. Then, the inverter side experiences a voltage overshoot of around 1.3 pu before stabilizing at 1.0 pu. Next, Figure 7.3(b) shows the DC voltage during the DC fault at the inverter. The DC voltages at both sides drops to zero during the fault, as expected. At $t = 2.6\,s$, the inverter voltage increase extremely to a value of 8 pu. After $t = 2.7\,s$, the DC voltage at both sides stabilizes at 1.0 pu. Next, the DC power can be seen in Figure 7.3(c). The power at the inverter side decreases to zero after the fault, and reaches -1.2 pu at the moment the fault is cleared at $t = 2.6\,s$. The power at the rectifier side experiences an overshoot of 2.5 pu at the instant of the fault, before slowly decreasing to zero and stabilizes at 1.0 pu again. Finally, Figure 7.3(d) shows the DC current during the fault. At the instant of the fault at $t = 2.5\,s$, the DC current experience a severe increase in value and reaches around 19 pu at the most. At $t = 2.7\,s$, the current stabilizes at around 1 pu. Voltage source converters struggle against DC faults, as their anti-parallel diodes conduct as rectifier bridges to feed the fault. The IGBTs are helplessly by-passed, unable to extinguish the fault current [19]. In this case,

the DC current and voltage reach very high peak values at the beginning and at the end of the fault. DC breakers are necessary in order to avoid the diodes and the IGBTs from burning up.

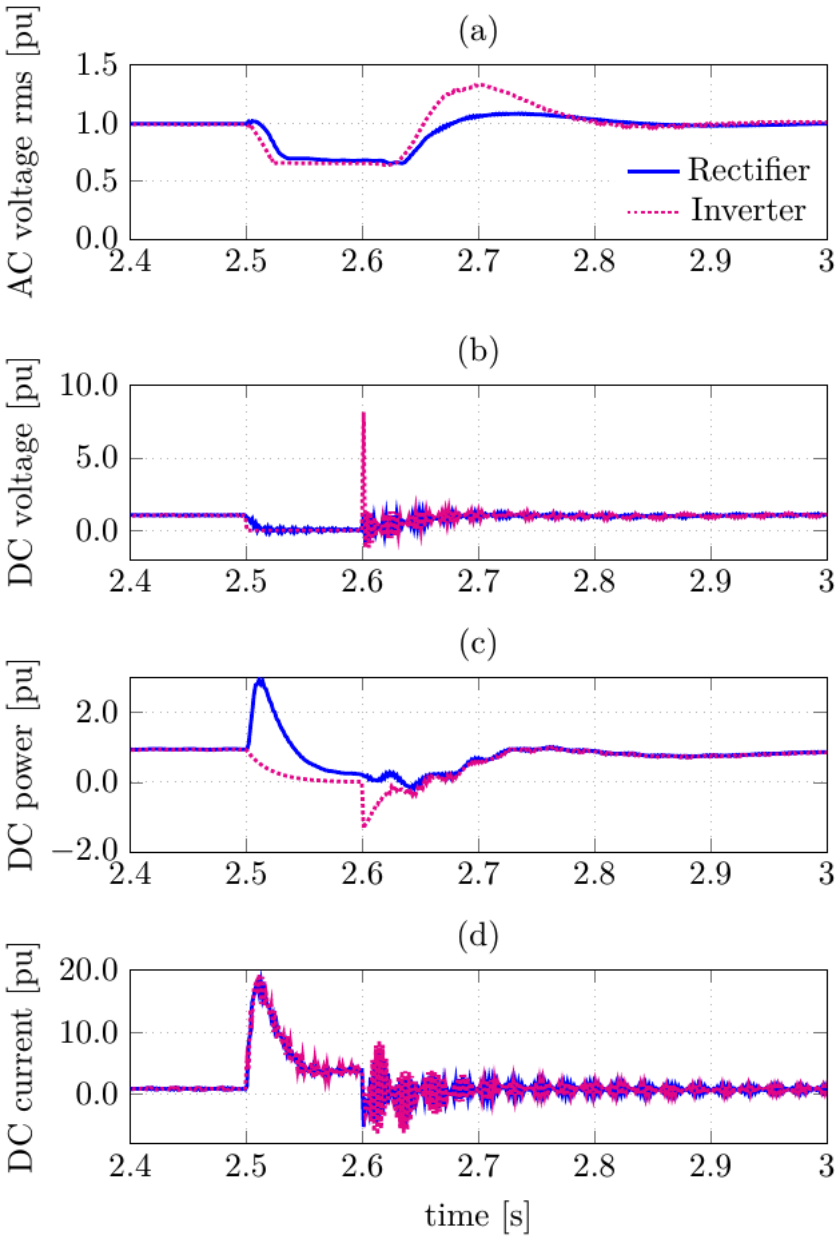


Figure 7.3: MMC system with DC fault to ground

Figure 7.4 presents the inner loop control objectives of the MMC during the DC fault. First, Figure 7.4(a) shows i_d and the reference current i_{d_ref} provided by the outer loop in order to control the DC power. The reference value stays more or less constant throughout the fault, while the system current at the rectifier experience oscillations. At $t = 2.75\,s$, the control objective has stabilized to steady state value. The same can be observed for Figure 7.4(b), where the reference current controls the AC voltage at the rectifier side through reactive power regulation. Next, Figure

7.4(c) shows the DC voltage control at the inverter side. The reference current supplied by the outer loop control increases from -1 pu to 1 pu at the moment of the fault at $t = 2.5\,s$. After the fault is cleared at $t = 2.6\,s$, the reference current oscillates between these values, until slowly settling down back to approximately -1 pu. The system current tries to follow the reference current, and at around $t = 2.9\,s$ the control system has stabilized. Finally, Figure 7.4(d) shows the inner loop AC voltage control at the inverter side. During the fault, the system current oscillates around 1.0 pu, before settling down at 0.0 pu again at $t = 2.8\,s$. The reference current supplied by the outer loop control is almost unaffected by the DC fault.

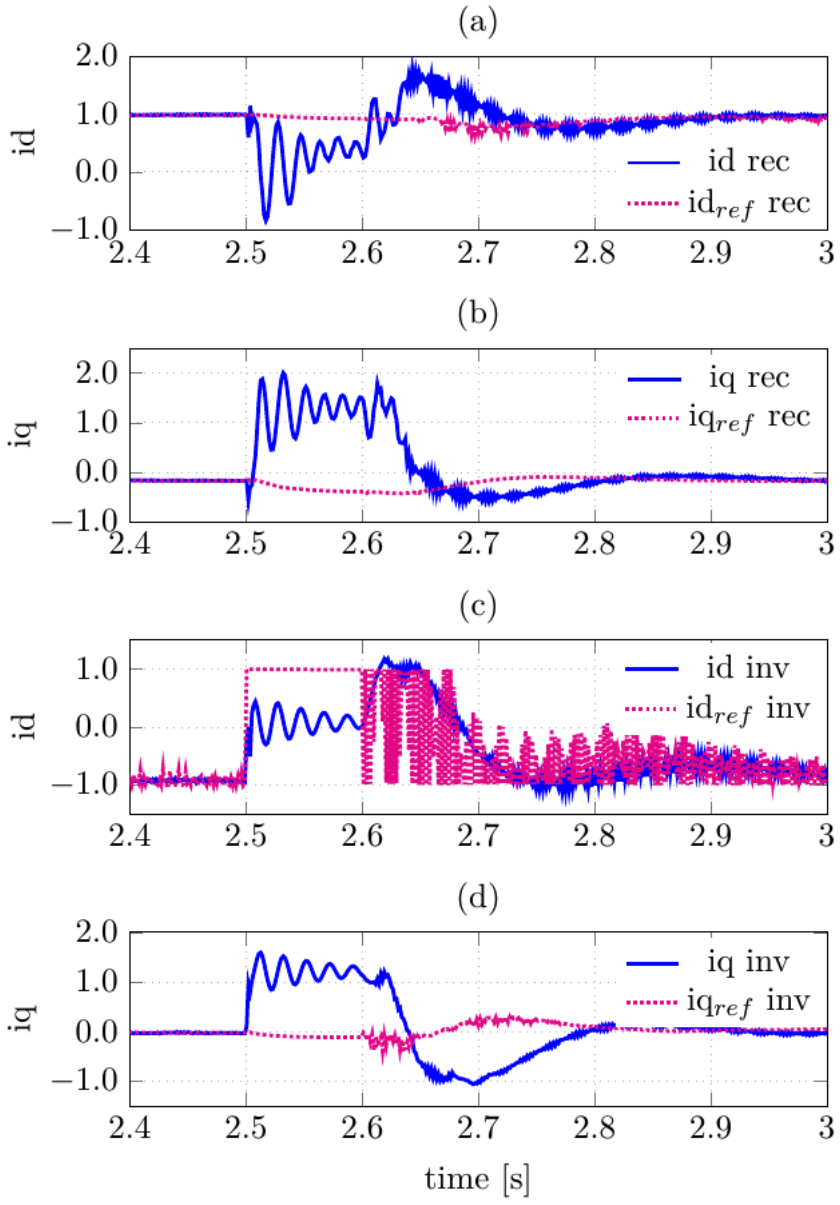


Figure 7.4: MMC control objectives at DC fault to ground

7.3 LCC-MMC DC pole to ground fault behavior

In this section, the LCC and MMC models are combined into a bipolar configuration. The rating of the LCC DC system is 440 MW at 350 kV, and the rating for the MMC DC system is 715 MW at 500 kV. The AC rms voltage at the rectifier side is 400 kV, while the voltage is 300 kV at the inverter side. A DC fault is first applied at the LCC DC-link, and then at the MMC DC-link.

7.3.1 DC fault on LCC inverter side

Figure 7.5 presents the AC characteristics of the LCC-MMC bipolar configuration during a DC fault at the LCC link. First, the AC rms voltages can be seen in Figure 7.5(a), which are almost unaffected by the fault at both sides of the HVDC-link.

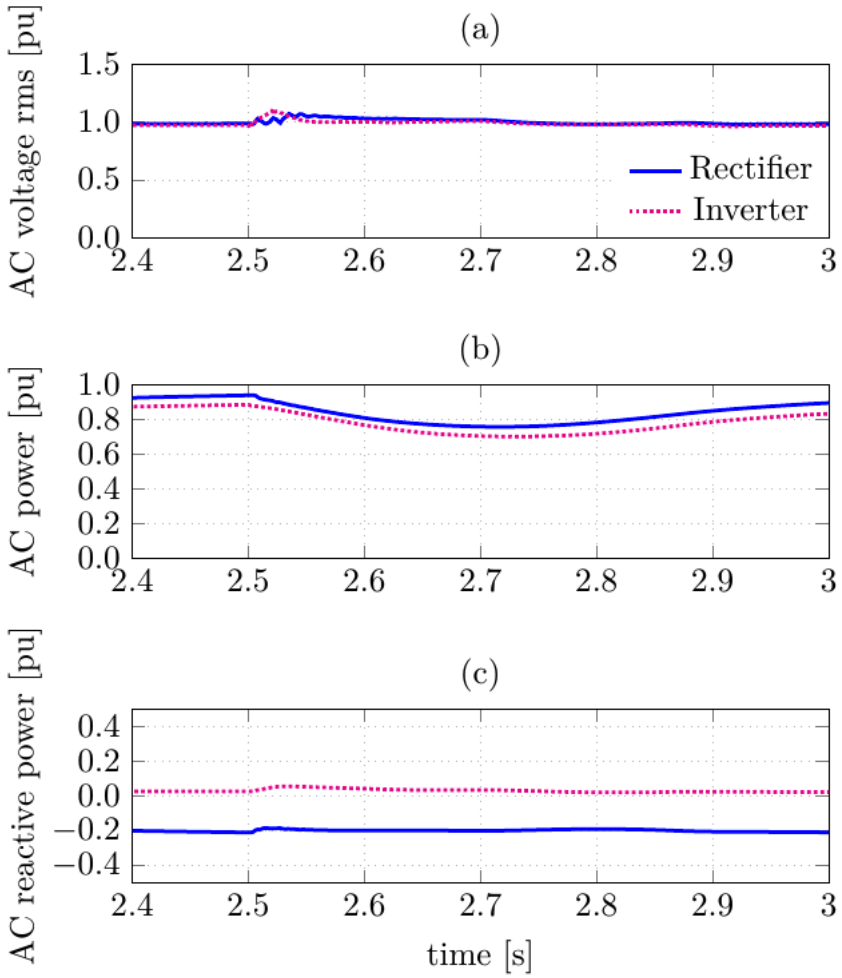


Figure 7.5: LCC and MMC AC system with DC fault to ground at the MMC link

Then, Figure 7.5(b) shows the AC power at the rectifier and inverter side. From the instant of the fault at $t = 2.5\ s$, the AC power at both sides slowly decreases

to roughly 0.7 pu. The AC power at the rectifier is affected by the fault, because the LCC is reducing its current reference supplied to the rectifier using VDCL. The power at the inverter side is slightly lower than at the rectifier side, due to losses in the cable. At $t = 2.9\ s$, the AC power has stabilized back to normal value again. Finally, the AC reactive power of the system can be seen in (c), which is almost not affected by the DC fault.

Figure 7.6 presents the DC characteristics of the LCC-MMC system during the DC fault at the LCC side. Figure 7.6(a) shows the DC voltage at the LCC and MMC link. The MMC voltage is unaffected by the DC fault, as expected. However, the LCC voltage oscillates around 0.0 pu for the duration of the fault. When the fault is cleared at $t = 2.6\ s$, the voltage start to increase again, and returns to steady state value at around $t = 2.8\ s$. The same situation can be observed with the LCC DC power in Figure 7.6(b). After the fault has passed, the power starts to increase and reaches steady state at around $t = 2.88\ s$. The MMC power is almost unaffected, with the exception of a small increase in power at the beginning of the fault.

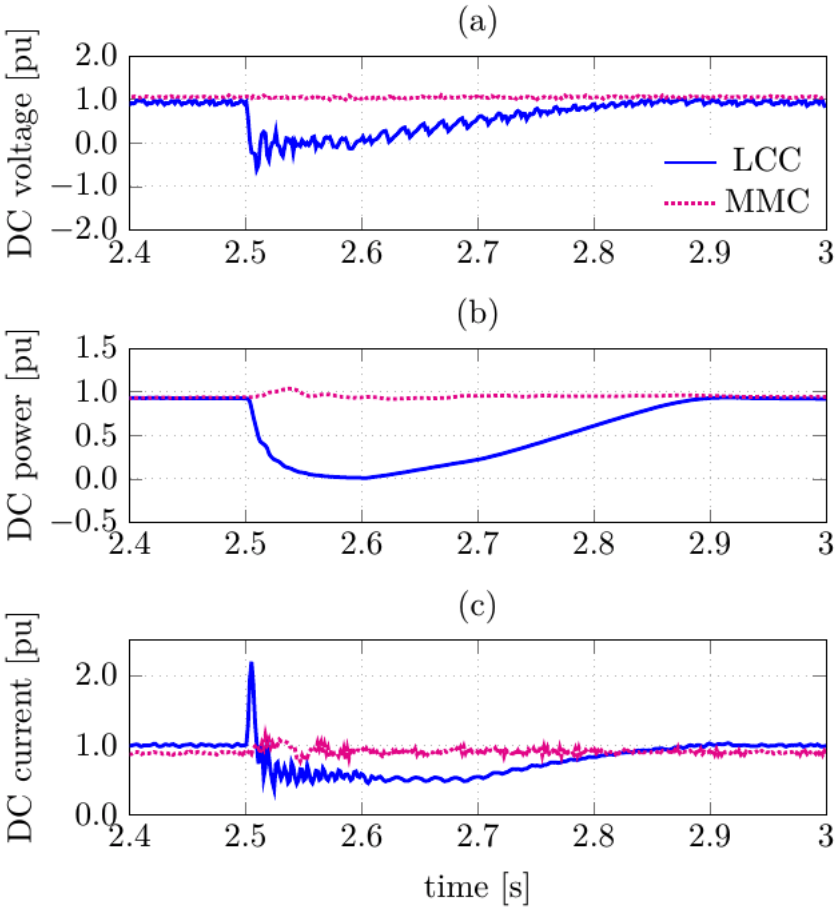


Figure 7.6: LCC and MMC DC system with DC fault to ground at the MMC link

Finally, the DC current can be seen in Figure 7.6(c). Compared to the LCC system in Figure 7.1(d), the current responds in the same way during the fault. However, at $t = 2.7\ s$, the current through the LCC link recovers and reaches steady state at

$t = 2.8\ s$. It is evident that the presence of the MMC link connected in a bipolar configuration with the LCC, helps the LCC system recover from the DC fault. The saturated voltage controller at the LCC inverter side retrieve controllability and is able to stabilize the DC voltage to steady state operation.

Figure 7.7 presents the control objectives of the LCC at the rectifier and inverter side during the DC fault. The LCC-MMC DC current control in Figure 7.7(a) and the minimum extinction angle control in Figure 7.7(b) respond in the same way to the DC fault as when there is just the LCC-HVDC link in section 7.1. However, when the fault is cleared at $t = 2.6\ s$, the control objectives are restored to their steady state behavior. The reference current in Figure 7.7(a) increases to 1.0 pu again, and the extinction angle in (b) reduces to 18°.

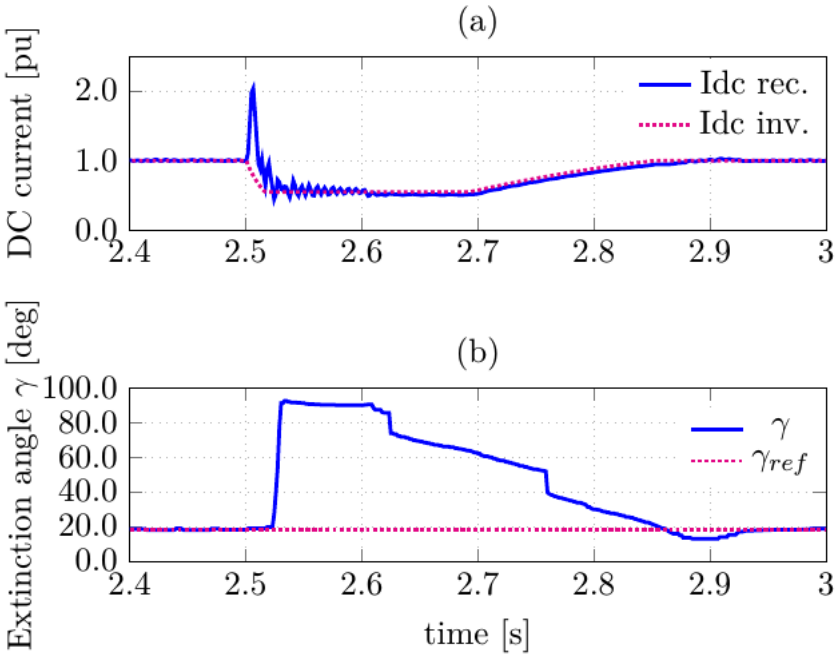


Figure 7.7: LCC control objectives at DC fault to ground

Figure 7.8 shows the control objectives of the MMC during the DC fault in the LCC link. None of the DC currents, i_d, or the reference currents, i_{d_ref}, are noteworthy affected by the DC fault. This is to be expected, as the fault occurs at the LCC DC-link and the same AC terminals connect the two systems.

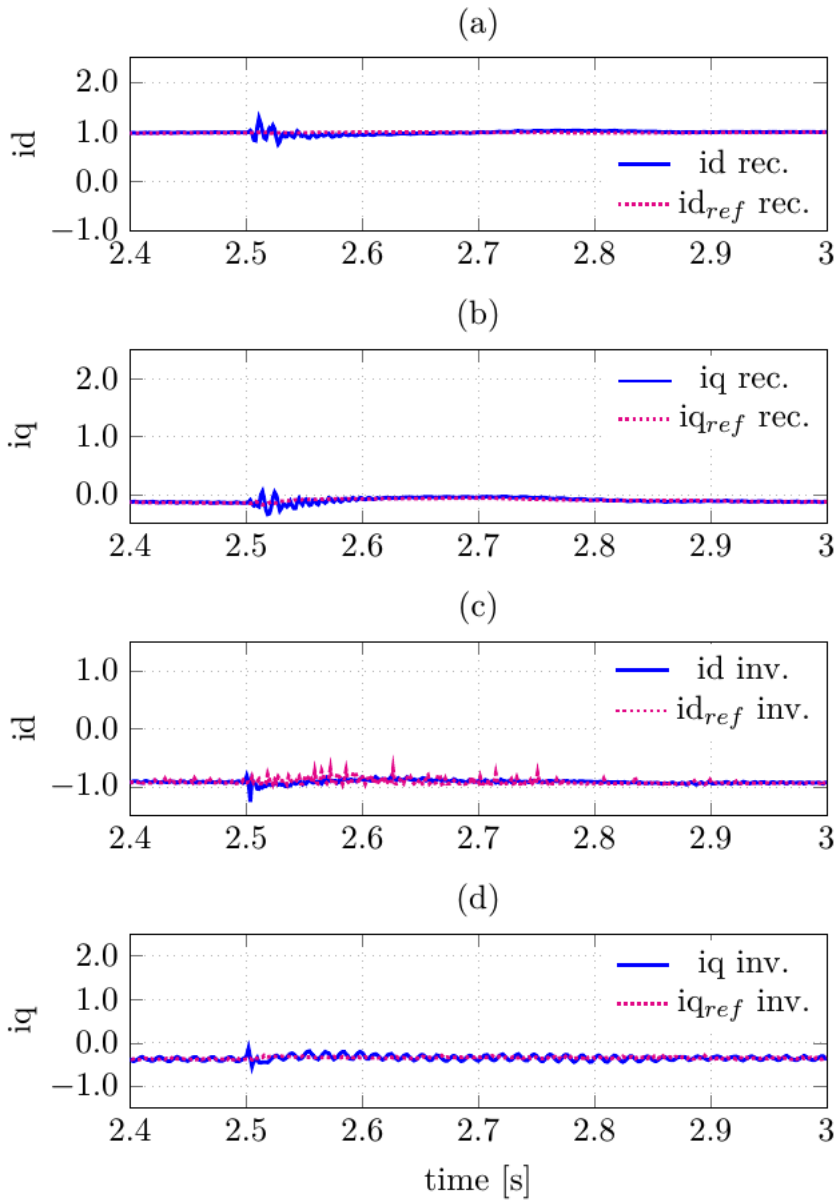


Figure 7.8: MMC control objectives at DC fault to ground

7.3.2 DC fault on MMC inverter side

Figure 7.9 presents the AC characteristics of the LCC-MMC bipolar configuration with a DC fault at the MMC side. First, Figure 7.9(a) shows the AC rms voltage at the rectifier and inverter side. When the fault occurs at $t = 2.5\ s$, the AC voltages at both sides starts to decrease to around 0.6 pu. This is because the MMC is

controlling the AC voltage, and without DC voltage in the system, the controllers are not able to work properly. At approximately $t = 2.64$, the voltages start to increase again, and the inverter voltage experience a voltage overshoot of 1.25 pu. Both voltages stabilize again at 1.0 pu at $t = 2.8\ s$. Next, Figure 7.9(b) shows the AC power at both sides. The AC power at both the rectifier side and inverter side decrease due to the AC voltage decrease. The rectifier voltage decrease due to the drop in LCC DC voltage as seen in Figure 7.10(a). The reference current supplied to the LCC rectifier is reduced, and causes the reduction in the AC power. The inverter AC power is more affected and drops as low as approximately 0.25 pu. Finally, Figure 7.9(c) shows the reactive power at the rectifier and inverter side. When the fault occurs at $t = 2.5\ s$, the MMC starts to support the systems by regulating the reactive power. At $2.9\ s$, the reactive power compensation is back to steady state.

Compared to Figure 7.5, where the fault is applied to the LCC link, the MMC fault has a much larger impact on the AC system.

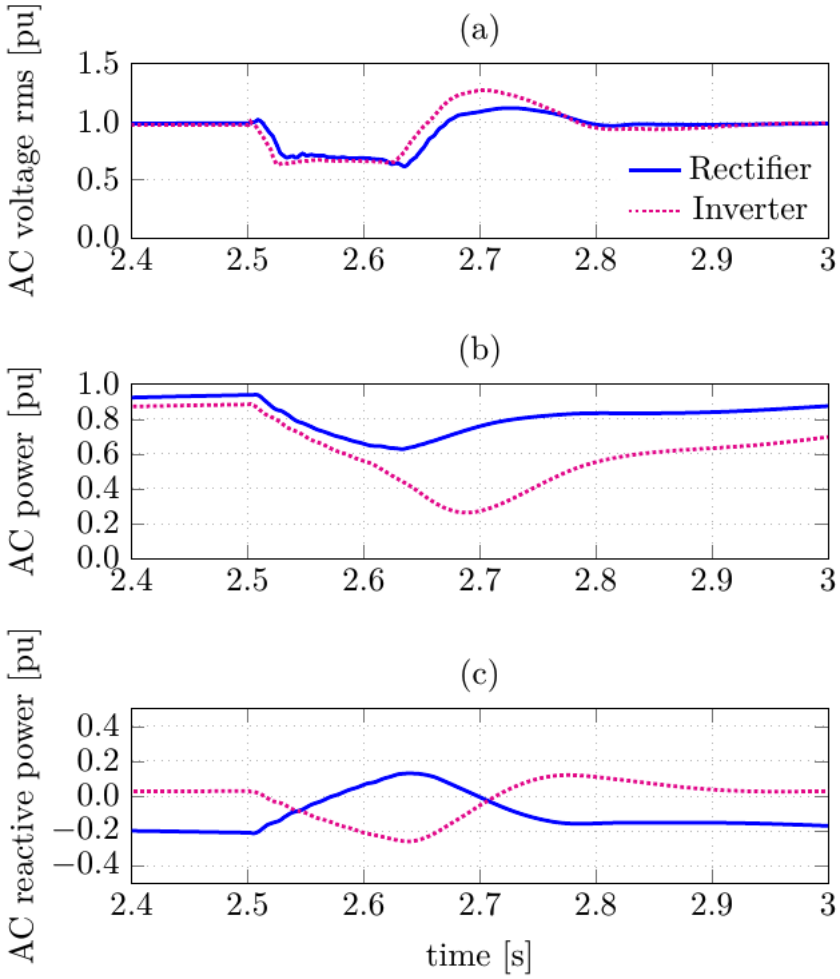


Figure 7.9: LCC and MMC AC system with DC fault to ground at the MMC link

Figure 7.10 presents the DC characteristics of the LCC and MMC link during the

DC fault. First, Figure 7.10(a) shows the DC voltage at both HVDC links. The LCC voltage is reduced to zero when the fault occurs at $t = 2.5\,s$, but start to increase again and reaches 1 pu at $t = 2.67\,s$. The DC voltage at the MMC reduces also to zero when the fault occurs, as expected. When the fault is cleared at $t = 2.6\,s$, the MMC DC voltage spikes up to 14 pu, before returning to zero pu and slowly starts the rise back to the steady state value. The combined model has increased the voltage overshoot from 8 pu to 14 pu, making the MMC respond worse to the fault when connected to the LCC. Next, Figure 7.10(b) shows the DC power. The LCC power decreases to approximately 0.2 pu after the fault, but slowly start to increase back to 1.0 pu. The MMC DC power is identical to Figure 7.3(c) where the MMC is a monopolar system. When the fault is cleared at $t = 2.6\,s$, the DC power becomes negative and the direction of the power flow changes. At around $t = 2.73\,s$, the power is back at steady state value of 1 pu.

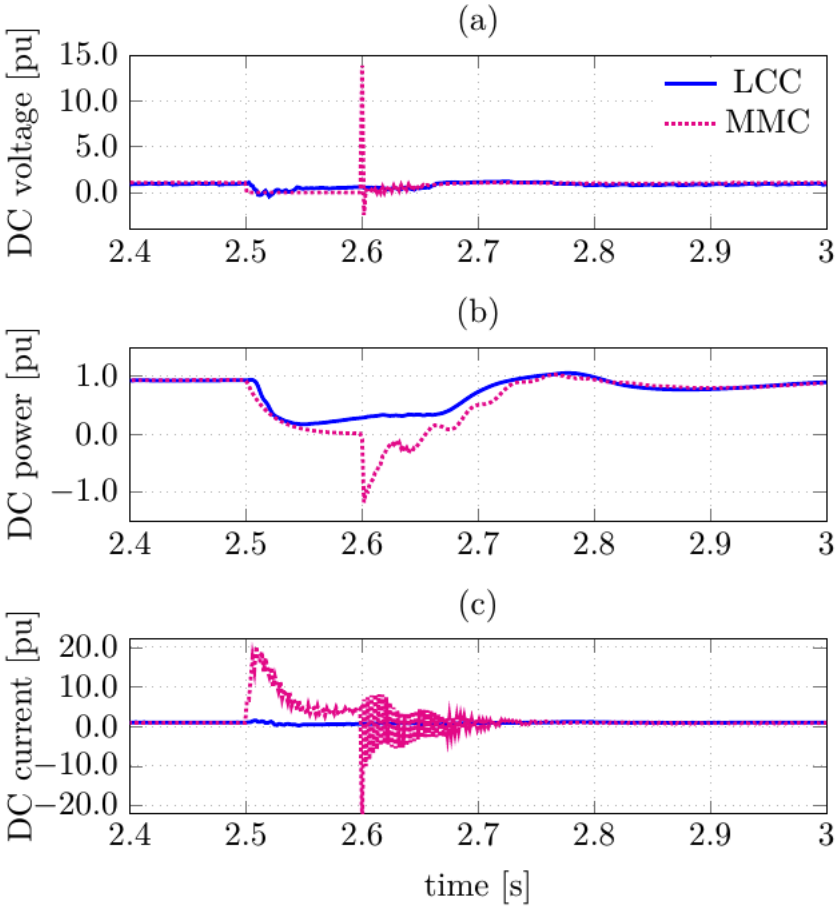


Figure 7.10: LCC and MMC DC system with DC fault to ground at the MMC link

Finally, the DC current can be seen in Figure 7.10(c). The LCC current is unaffected by the MMC DC fault, and stays at 1 pu throughout the fault. The MMC DC current, however, increases severely when the fault occurs, and reaches 20 pu. When the fault is cleared at $t = 2.6\,s$, the current drops to -20 pu, changing the direction of the power flow. This negative drop is more extreme for the combined system,

than for just the MMC where the most negative value is -8 pu. At $t = 2.72\ s$, both currents are stable at 1 pu. It is evident that the LCC-MMC bipolar configuration makes the overvoltage and -current of the MMC system worse during the fault, than without the combination.

Figure 7.11 presents the control objectives of the LCC during the DC fault at the MMC link. Figure 7.11(a) shows the DC current control at the rectifier, with a reference current supplied by the inverter side through VDCL control. The reference current is lowered to around 0.6 pu during the fault, due to the LCC DC voltage reduction. When the fault is cleared, the reference value is restored back to 1 pu. Figure 7.11(b) shows the minimum extinction angle control at the inverter. When the fault occurs at $t = 2.5\ s$, the extinction angle drops to 0°, and it is clear that failure of commutation is happening in the inverter. At approximately $t = 2.54\ s$, the extinction angle increases to almost 60° before starting to decrease towards the reference angle of 18°.

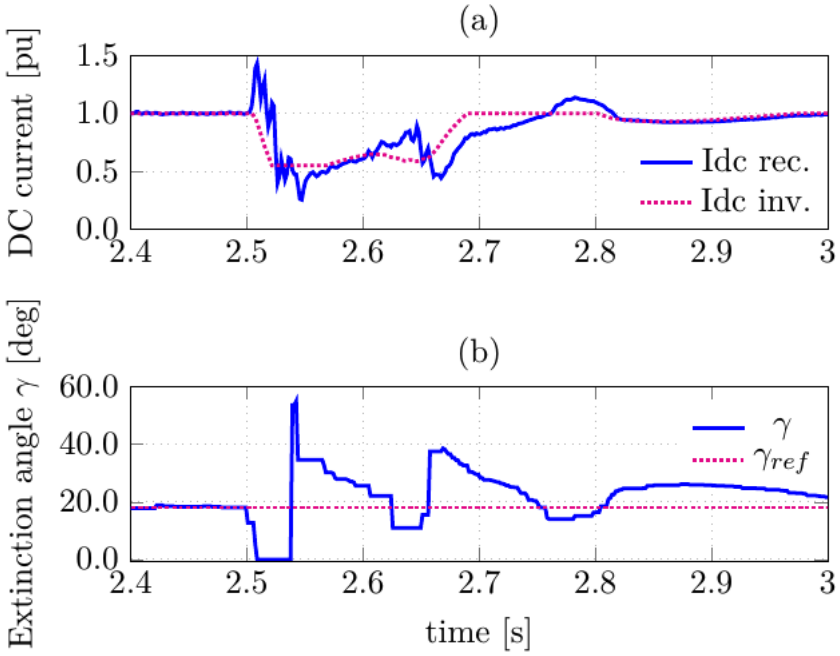


Figure 7.11: LCC control objectives at DC fault to ground

Figure 7.12 presents the MMC control objectives during the DC fault at the MMC link. The behavior of the reference currents, supplied by the outer loop control, and the system currents are almost identical to Figure 7.4, where the fault is applied to the monopolar MMC system. This is to be expected, as the fault is the same.

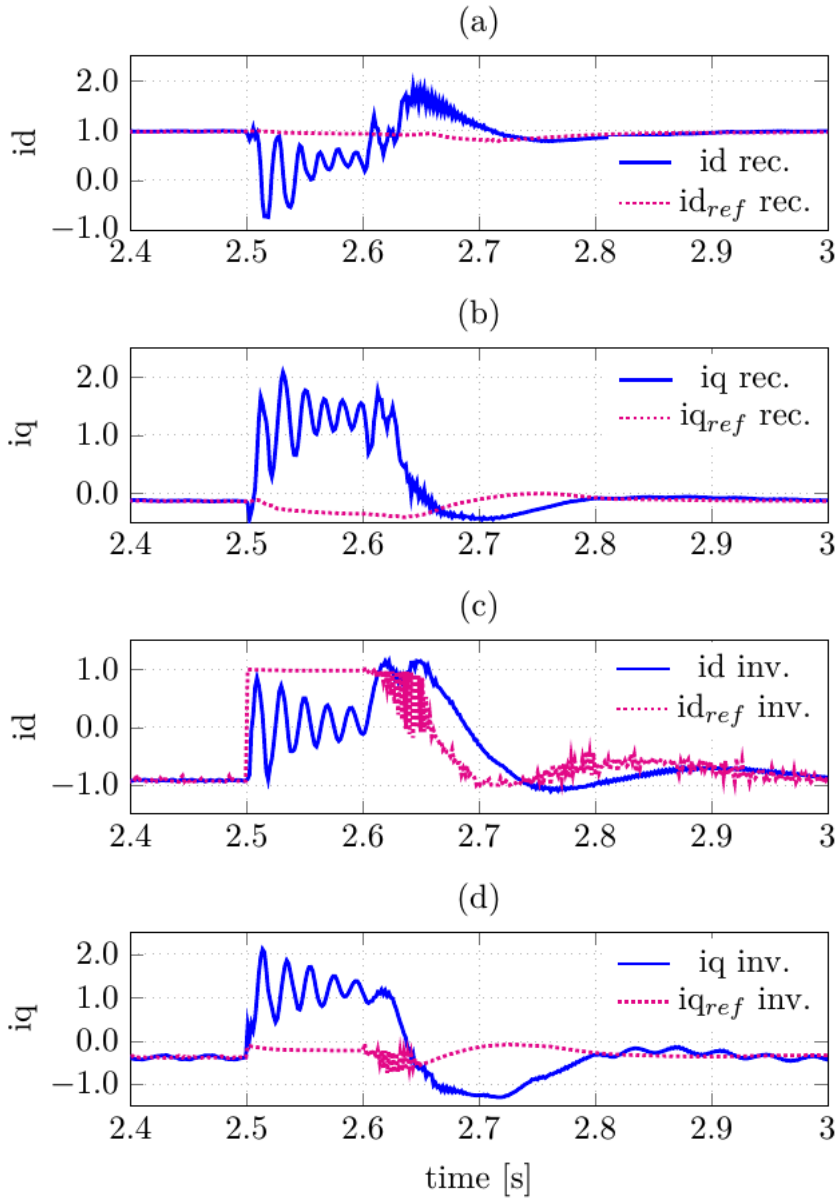


Figure 7.12: MMC control objectives at DC fault to ground

7.4 Summary

A DC pole to ground fault is applied to the three different simulation models. When the fault is applied to the LCC system, the AC voltages at both stations are almost unaffected by the fault. Due to a large overcurrent at the beginning of the fault, the voltage controller at the inverter become saturated and looses controllability of the DC voltage, and cannot recover from the fault. This is probably because the PSCAD model does not utilize anti-windup PI controllers, and thus, looses the controllability when the fault occurs. By restarting the PI controllers, this situation may be avoided, and the system can manage to recover from the fault. Implementing a different control arrangement during a DC fault can be looked at in future work.

The DC fault is then applied to the MMC DC-link. The fault reduces the AC voltages at both stations because the MMC is not able to control the AC voltage during the fault. The DC voltage experiences a large spike of 8 pu at the end of the fault. The DC current is also experiencing extreme values during the fault, and at the beginning of the fault the current reaches almost 20 pu. This overvoltage and -current are very high and require DC breakers to save the diodes and IGBTs of the converter from being destroyed. Implementing a DC breaker into the system is not included in the scope of this thesis.

There are two situations simulated when the LCC and MMC are connected together in a bipolar configuration. First, there is a DC fault applied at the LCC side, which gives an interesting result. The system manages to recover from the fault, due to the help from the connected MMC link. The MMC system adds stability to the total system, making the LCC recover the controllability of the controllers. How the MMC manages to help the LCC system needs to be investigated in future work. Further, the DC fault is applied to the MMC link. The simulation results are very similar to the MMC system alone, but experiences more severe voltage and current spikes. Voltage source converters struggle against DC faults, because the anti-parallel diodes start to conduct and feed the fault. Sophisticated DC protection is therefore necessary, as the converters cannot handle such high overvoltages and -currents.

It can be concluded, based on the simulations during the DC fault, that the LCC and MMC systems are not operating independently when connected in the bipolar configuration. The MMC helps the LCC system recover from the fault, while the LCC increases the voltage and current overshoots of the MMC. Different protection strategies must therefore be implemented in the combined model compared to the separate monopolar models.

Conclusion

Through simulations performed in PSCAD, the monopolar LCC model, the monopolar MMC model, and the LCC-MMC bipolar configuration model have been validated. Steady state behavior and different fault scenarios have been investigated in order to analyze the behavior of the models.

At steady state, the three models have been validated to be operating as expected. When the two monopolar systems are combined into a bipolar system, the passive filters from the LCC model are removed. There is an interaction between the MMC and the passive filters, which requires the demanding task of redesigning the filters. The DC voltages in the combined model are divided somewhat unevenly between the HVDC links based on the nominal voltages, and can be interesting to investigate in further work. Ripple in the DC voltage of the MMC model arises due to polluted circulating currents in the converter, and can be reduced by using a different modulation technique or by placing a large capacitor across the converter arms.

A three-phase to ground fault has been applied at the inverter side of the models. Double commutation failure occurred in the LCC inverter due to the severe reduction in AC voltage. A DC chopper placed at the MMC DC-link reduced the DC voltage overshoot during the fault significantly. It has been concluded through simulation that the bipolar configuration does not require any additional protection systems, and that the same protection used in the monopolar systems should be sufficient.

When a single-phase to ground fault has been applied at the inverter side of the models, harmonic disturbances arise in the voltages and currents due to the unbalance of the fault. The LCC has suffered from failure of commutation in the inverter, because of the reduction in the AC voltage. The LCC and MMC systems were almost unaffected by each other when combined. Additional protection systems are therefore not necessary for the bipolar configuration.

A DC fault has been applied to the three simulation models. The LCC system did not recover from the fault, due to lost controllability of the inverter controller. By utilizing anti-windup PI controllers or a different control arrangement during the fault, the system may recover. When connected to the MMC system, the LCC has been able to recover from the fault with help from the MMC. The monopolar MMC system restored its nominal values after the fault, but suffered from very high voltage and current spikes. This is because VSCs struggle against DC faults, as the anti-parallel diodes start to conduct and feed the fault. The LCC and MMC systems did not operate independently when connected in a bipolar manner, and different protection strategies must be implemented when compared to the monopolar models.

Further Work

This thesis covers only a small part of what needs to be investigated concerning the Skagerrak 3 and Skagerrak 4 bipolar configuration. The objective of the thesis is to analyze how the two HVDC systems are affecting each other during steady state and during faults. A list of further work that can be carried out using the PSCAD models, can be seen below.

- *Redesign the harmonic filters for the combined configuration.* There is an interaction between the MMC and the passive filters, an so new passive filters must be designed.
- *Reduce noise in the MMC DC voltage.* By applying a different modulation technique or removing the second harmonic circulating current in the converter.
- *Try other control strategies during the faults.* In order to avoid failure of commutation in the LCC, a larger commutation margin can be chosen during the fault. It will lead to higher reactive power consumption, but this can be supplied by the MMC. During an AC fault in the MMC, a better DC chopper can be used in order to lower the DC voltage, or finding a solution to redirect the power from the rectifier. Restarting of the PI controllers in the LCC during a DC fault.
- *Investigate the unevenly divided DC voltage in the bipolar configuration.*
- *Power reversal.* Implement a switching scheme for the polarity of the MMC link, and analyze how the bipolar configuration handles power reversal. It is the first time that an LCC and a VSC are connected in a bipolar configuration, and it is very interesting to investigate how the system reacts to power reversal, and voltage reversal for the VSC as well.
- *Introduce protection devices.* There are a lot of overvoltages and -currents during the various faults that the converters need to be protected against. DC-breakers should be implemented for DC faults.
- *Analyze more fault scenarios.* Analyze phase-to-phase AC faults and pole-to-pole DC faults.
- *Perform simulations with 400 kV at the SK4 converter station.*

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Appendices

Appendix A

Power System Equations

A.1 Per Unit system

Single-phase	**Three-phase**
$I_{base} = \frac{S_{base}}{V_{base}}$	$I_{base} = \frac{S_{base}}{V_{base} \times \sqrt{3}}$
$Z_{base} = \frac{V_{base}}{I_{base}} = \frac{V_{base}^2}{S_{base}}$	$Z_{base} = \frac{V_{base}}{I_{base} \times \sqrt{3}} = \frac{V_{base}^2}{S_{base}}$
$Y_{base} = \frac{1}{Z_{base}}$	$Y_{base} = \frac{1}{Z_{base}}$

A.2 Base value calculations

In order to display the system values in a perspicuous way, all values are given in per unit. The system quantities are devided by a defined base unit quantity.

A.2.1 SK3 base values

DC

$$V_{dc\_base} = 350\ kV \qquad \frac{1}{V_{dc\_base}} = \frac{1}{350} = 0.00286$$

$$P_{dc\_base} = 440\ MW \qquad \frac{1}{P_{dc\_base}} = \frac{1}{440} = 0.00227$$

$$I_{dc\_base} = \frac{440\ MW}{350\ kV} = 1.257\ kA \qquad \frac{1}{I_{dc\_base}} = \frac{1}{1.257} = 0.795$$

AC

Tjele:

$$V_{ac\_base} = 400\ kV \qquad \frac{1}{V_{ac\_base}} = \frac{1}{400} = 0.00250$$

$$P_{ac\_base} = 715\ MW \qquad \frac{1}{P_{ac\_base}} = \frac{1}{715} = 0.00140$$

$$I_{ac\_base} = \frac{440\ MW}{\sqrt{3}400\ kV} = 0.635\ kA \qquad \frac{1}{I_{dc\_base}} = \frac{1}{0.635} = 1.574$$

Kristiansand:

$$V_{ac\_base} = 300\ kV \qquad \frac{1}{V_{ac\_base}} = \frac{1}{300} = 0.00333$$

$$P_{ac\_base} = 715\ MW \qquad \frac{1}{P_{ac\_base}} = \frac{1}{715} = 0.00140$$

$$I_{ac\_base} = \frac{440\ MW}{\sqrt{3}300\ kV} = 0.847\ kA \qquad \frac{1}{I_{dc\_base}} = \frac{1}{0.847} = 1.181$$

A.2.2 SK4 base values

DC

$$V_{dc\_base} = 500\ kV \qquad \frac{1}{V_{dc\_base}} = \frac{1}{500} = 0.0020$$

$$P_{dc\_base} = 715\ MW \qquad \frac{1}{P_{dc\_base}} = \frac{1}{715} = 0.00140$$

$$I_{dc\_base} = \frac{715\ MW}{500\ kV} = 1.430\ kA \qquad \frac{1}{I_{dc\_base}} = \frac{1}{1.430} = 0.699$$

AC

Tjele:

$$V_{ac\_base} = 400\ kV \qquad \frac{1}{V_{ac\_base}} = \frac{1}{400} = 0.00250$$

$$P_{ac\_base} = 715\ MW \qquad \frac{1}{P_{ac\_base}} = \frac{1}{715} = 0.00140$$

$$I_{ac\_base} = \frac{715\ MW}{\sqrt{3}400\ kV} = 1.032\ kA \qquad \frac{1}{I_{dc\_base}} = \frac{1}{1.032} = 0.969$$

Kristiansand:

$$V_{ac\_base} = 300\ kV \qquad \frac{1}{V_{ac\_base}} = \frac{1}{300} = 0.00333$$

$$P_{ac\_base} = 715\ MW \qquad \frac{1}{P_{ac\_base}} = \frac{1}{715} = 0.00140$$

$$I_{ac\_base} = \frac{715\ MW}{\sqrt{3}300\ kV} = 1.376\ kA \qquad \frac{1}{I_{dc\_base}} = \frac{1}{1.376} = 0.727$$

A.2.3 SK3 and SK4 base values

AC

Tjele:

$$V_{ac\_base} = 400\ kV \qquad \frac{1}{V_{ac\_base}} = \frac{1}{400} = 0.00250$$

$$P_{ac\_base} = (440 + 715)\ MW = 1155\ MW \qquad \frac{1}{P_{ac\_base}} = \frac{1}{1155} = 0.000866$$

$$I_{ac\_base} = \frac{1155\ MW}{\sqrt{3}400\ kV} = 1.667\ kA \qquad \frac{1}{I_{dc\_base}} = \frac{1}{1.667} = 0.600$$

Kristiansand:

$$V_{ac\_base} = 300\ kV \qquad \frac{1}{V_{ac\_base}} = \frac{1}{300} = 0.00333$$

$$P_{ac\_base} = (440 + 715)\ MW = 1155\ MW \qquad \frac{1}{P_{ac\_base}} = \frac{1}{1155} = 0.000866$$

$$I_{ac\_base} = \frac{1155\ MW}{\sqrt{3}300\ kV} = 2.223\ kA \qquad \frac{1}{I_{dc\_base}} = \frac{1}{2.223} = 0.450$$

A.3 Park Transformation

abc to dq0

$$\begin{bmatrix} d \\ q \\ 0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos(\theta) & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ \sin(\theta) & \sin(\theta - \frac{2\pi}{3}) & \sin(\theta + \frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \cdot \begin{bmatrix} a \\ b \\ c \end{bmatrix} \tag{A.1}$$

dq0 to abc

$$\begin{bmatrix} a \\ b \\ c \end{bmatrix} = \begin{bmatrix} \cos(\theta) & \sin(\theta) & 1 \\ \cos(\theta - \frac{2\pi}{3}) & \sin(\theta - \frac{2\pi}{3}) & 1 \\ \cos(\theta + \frac{2\pi}{3}) & \sin(\theta + \frac{2\pi}{3}) & 1 \end{bmatrix} \cdot \begin{bmatrix} d \\ q \\ 0 \end{bmatrix} \tag{A.2}$$

A.4 PI controller

The PI controller is a continuous Proportional-Integral controller as seen in Fig. A.1. The motive of the integral is to supply infinite amplification at low frequencies with the purpose of achieveing zero steady-state variation. While at high frequencies, the PI controller operates as a P controller with only a proportional gain [24].

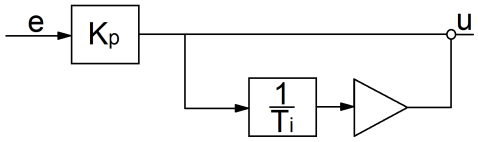

Figure A.1: PI controller

The transfer function of the PI controller can be expressed as below.

$$h_r(s) = K_p(1 + \frac{1}{T_i s}) = K_p \frac{1 + T_i s}{T_i s} \tag{A.3}$$

Where K_p is the proportional gain, and T_i is the integration time. By increasing K_p, the system will respond quickly trying to reach the reference value. Overshoots may occur, leaving the system oscillating around the reference value until finally stabilizing. If the proportional gain is set too high, the system can become unstable, and never reach the reference value. The integral component is slower than the proportional controller. It will integrate the input signal, and the output signal will increase when the deviation is positive, and decrease when the deviation is negative. Sometimes the transfer function is also referred to as Eq. A.4.

$$h_r(s) = K_p + \frac{K_i}{s} \tag{A.4}$$

where $K_i = \dfrac{K_p}{T_i}$.

Appendix B

Schematic of SK3 and SK12

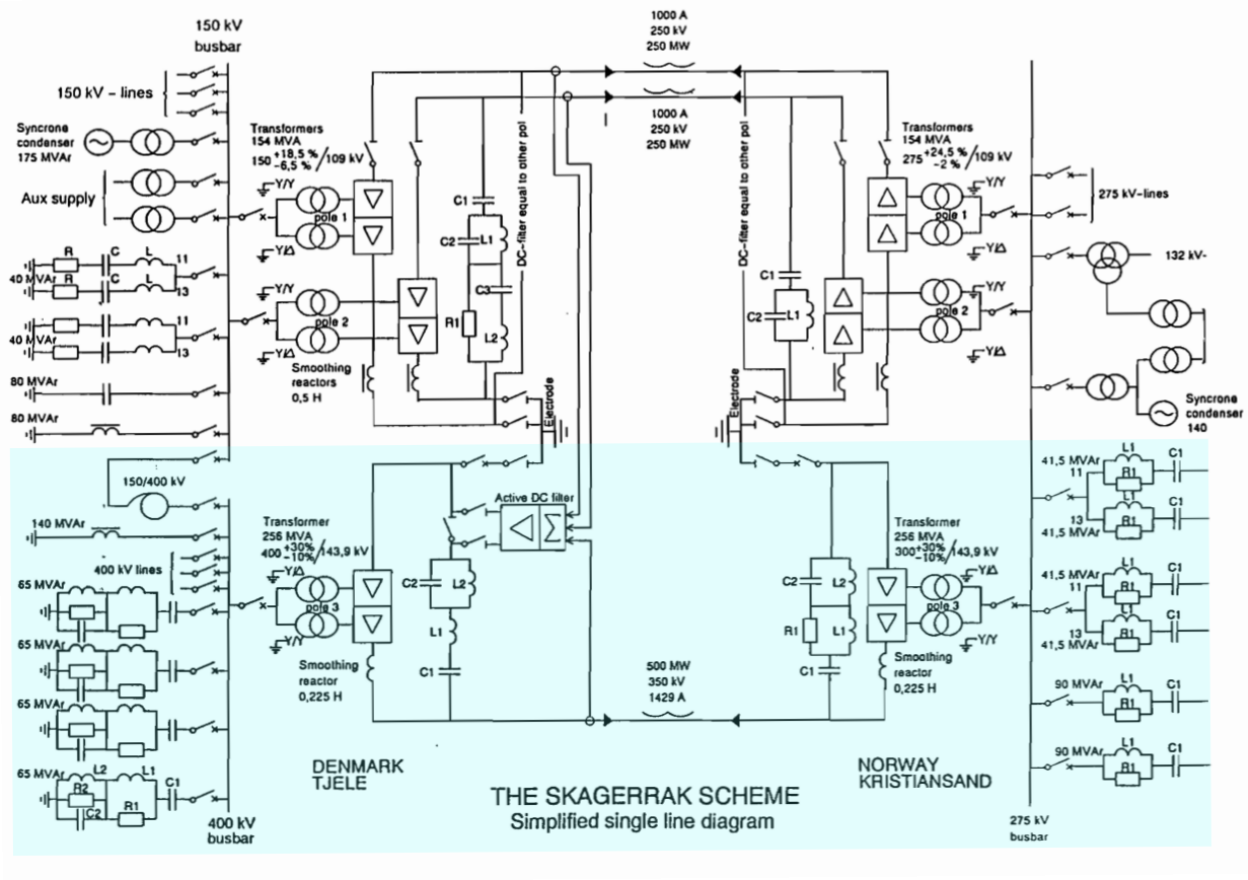

Figure B.1: Schematic of SK3 (shaded area) in connection with SK12 [5]

Appendix C

Filter Calculations

C.1 Tuned filter

Figure C.1: RLC filter

V_{LL} = Line to line voltage

V_ϕ = Phase voltage = $\frac{V_{LL}}{\sqrt{3}}\, kV$

Finding the values for the resistance (R), inductance (L), and capacitance (C) of the filter.

Q = Quality factor = $\frac{\omega_r L}{R}$

MVAr requirement per phase = Q_ϕ

Filter impedance $Z = \sqrt{R^2 + (\omega L - \frac{1}{\omega C})^2}$

$$Z = R^2 + \left(\omega L - \frac{1}{\omega C}\right)^2 = \frac{\omega^2 L^2}{Q^2} + \left(\frac{\omega^2 LC - 1}{\omega C}\right)^2$$

Defining $\omega_r = \frac{1}{\sqrt{LC}}$ in the equation above

$$Z^2 = \frac{\omega^2/\omega_r^2 + Q^2(\omega^2/\omega_r^2 - 1)^2}{Q^2 \cdot \omega^2 \cdot C^2}$$

$Q_\phi = \frac{V_\phi^2}{Z^2 \cdot \omega C}$ and defining $\frac{\omega}{\omega_r} = M$, the equation solved for C is

$$C = \frac{Q_\phi}{V_\phi^2} \cdot \left(\frac{M^4 + Q^2 \cdot (M^2 - 1)^2}{Q^2 \cdot \omega}\right), \quad L = \frac{1}{\omega_r^2 \cdot C} \quad \text{and} \quad R = \frac{\omega L}{Q}$$ [25]

C.2 High-pass filter

The impedance of the filter can be expressed

$$Z = \frac{1}{j\omega C} + \left(\frac{1}{R} + \frac{1}{j\omega L}\right)^{-1}$$

Resonant frequency: $\omega_r = \frac{1}{\sqrt{LC}}$

Per unit frequency: $f_{pu} = \frac{\omega}{\omega_r} = \frac{f}{f_r}$

Characteristic impedance: $X_0 = \sqrt{\frac{L}{C}}$

Quality factor: $Q = \frac{R}{X_0}$

Q is an index of tuning sharpness, and varies between 0.5 - 2.0 [25]

Replacing the parameters in the filter impedance

$$Z = \frac{1}{jf_{pu}} + \left(\frac{1}{Q} + \frac{1}{jf_{pu}}\right)^{-1}$$

Reactive power requirement per phase: Q_{ph}

The impedance of the parallel branch is negligible, and the expression for reactive power can be expressed [25]:

$$Q_{ph} = V_{ph}^2 \cdot \omega C \quad \text{finding C} \quad C = \frac{Q_{ph}}{V_{ph}^2 \cdot \omega}$$

$$L = \frac{1}{\omega_r^2 \cdot C}$$

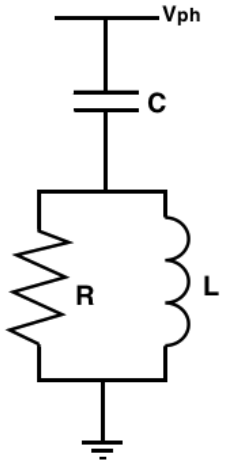

Figure C.2: High-pass filter

C.3 Shunt capacitor

$$Q_\phi = \frac{Q}{3} \qquad Q_\phi = \frac{V_\phi^2}{X_c}$$

$$X_c = \frac{1}{\omega C} \qquad C = \frac{1}{X_c \cdot \omega}$$

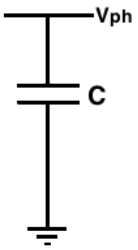

Figure C.3: Shunt capacitor

Appendix D

Simulations

D.1 AC Fault –Single-Phase to Ground on Inverter Side

D.1.1 MMC without DC chopper

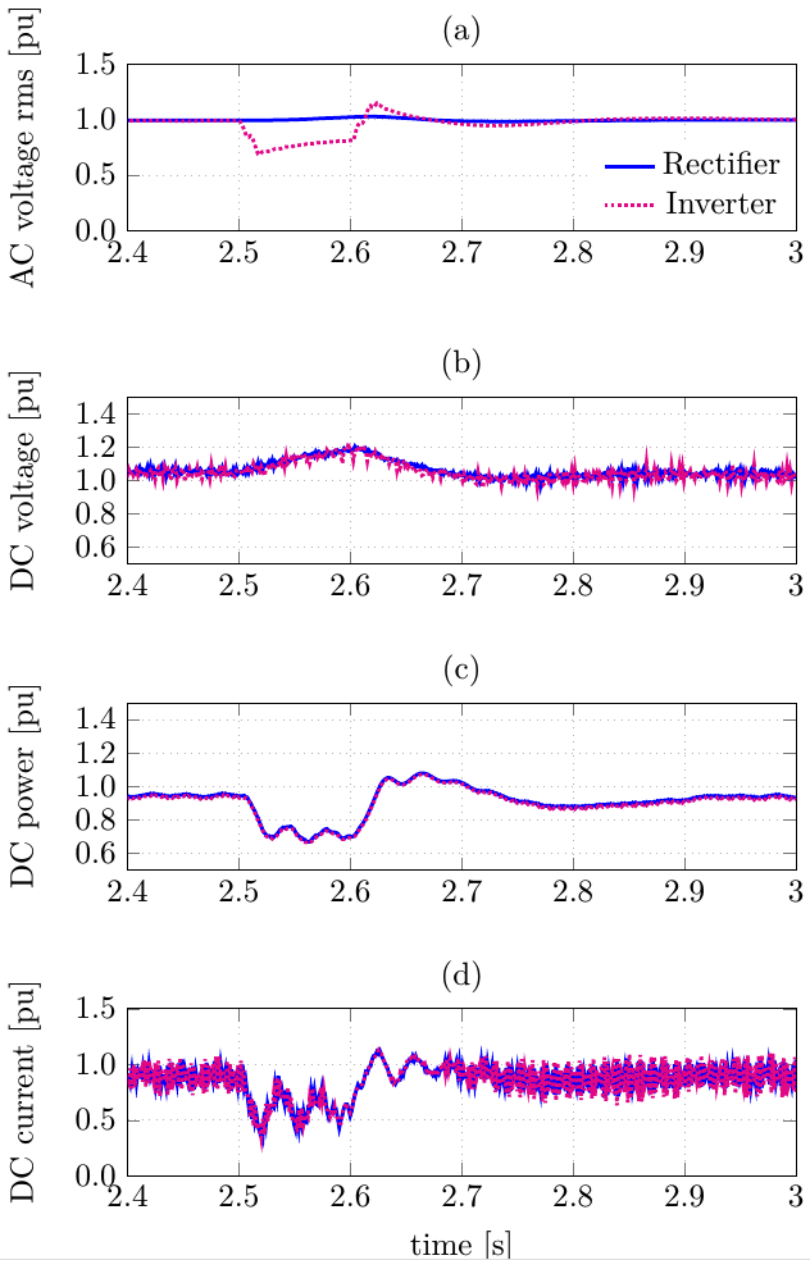

Figure D.1: MMC system without DC chopper at single-phase to ground fault

Control objectives

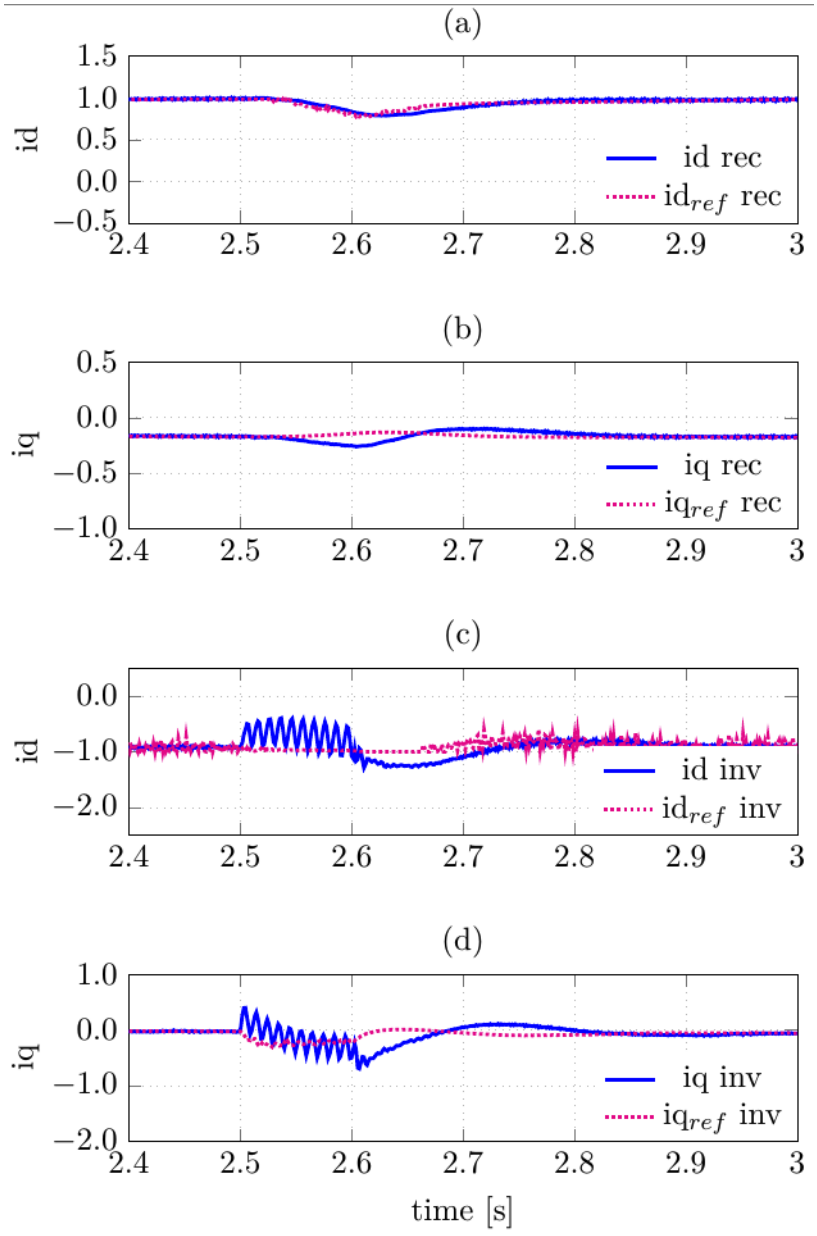

Figure D.2: LCC control objectives at single-phase to ground fault

D.1.2 LCC and MMC without DC chopper

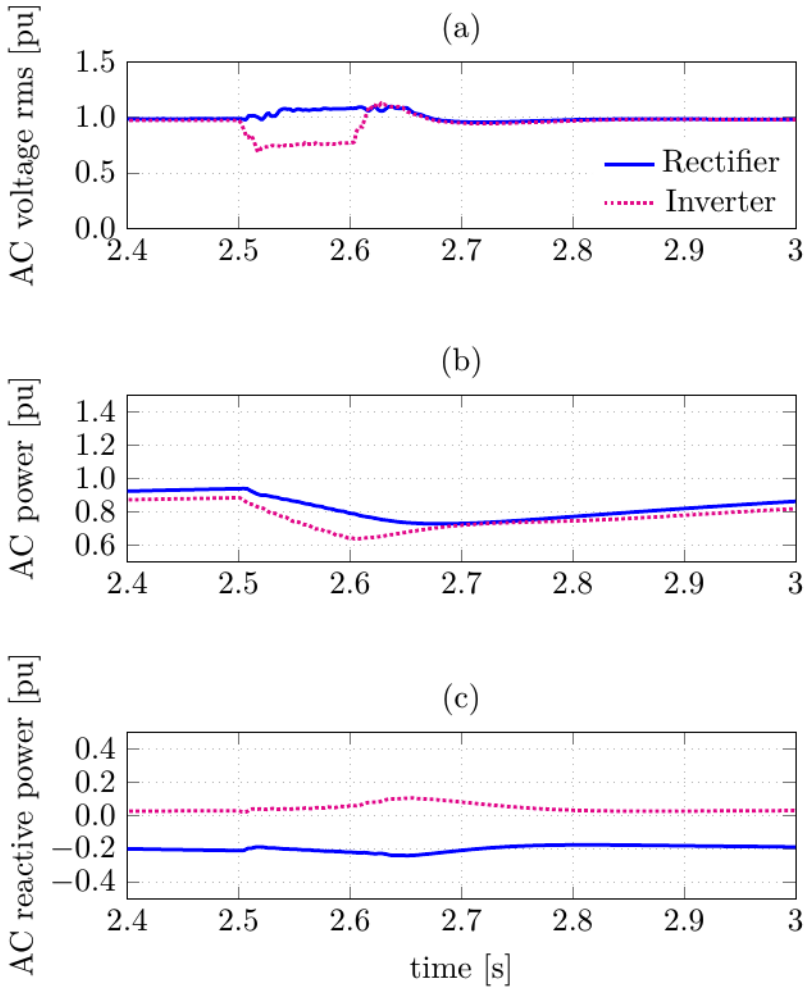

Figure D.3: LCC-MMC AC system without DC chopper at single-phase to ground fault

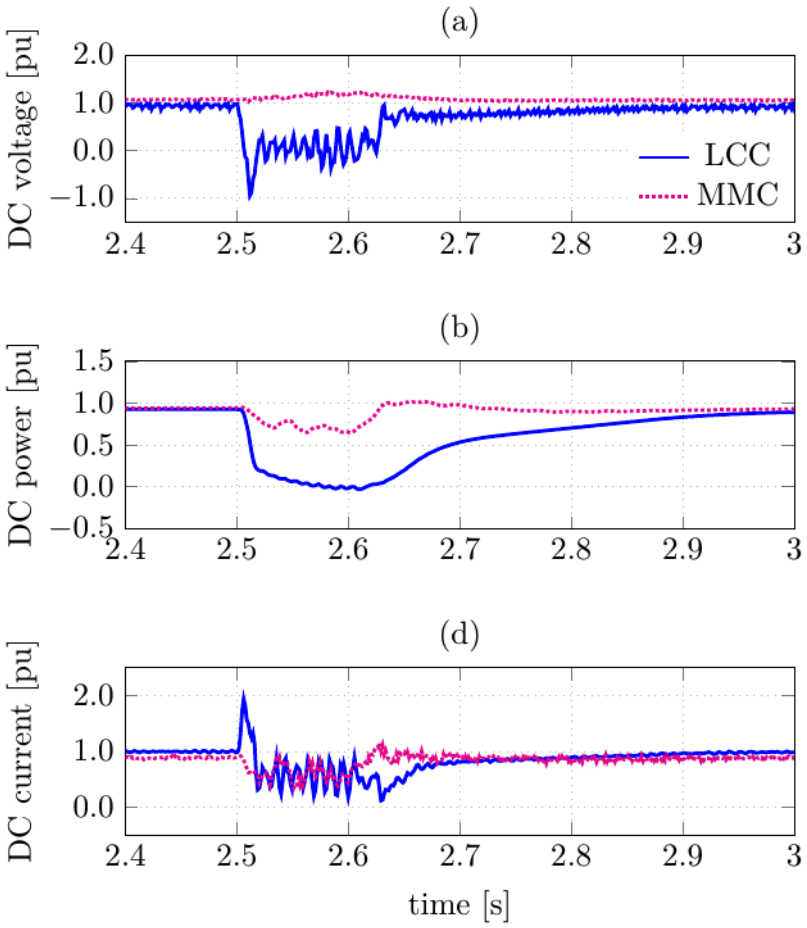

Figure D.4: LCC-MMC DC system without DC chopper at single-phase to ground fault

D.1.3 Control objectives

LCC

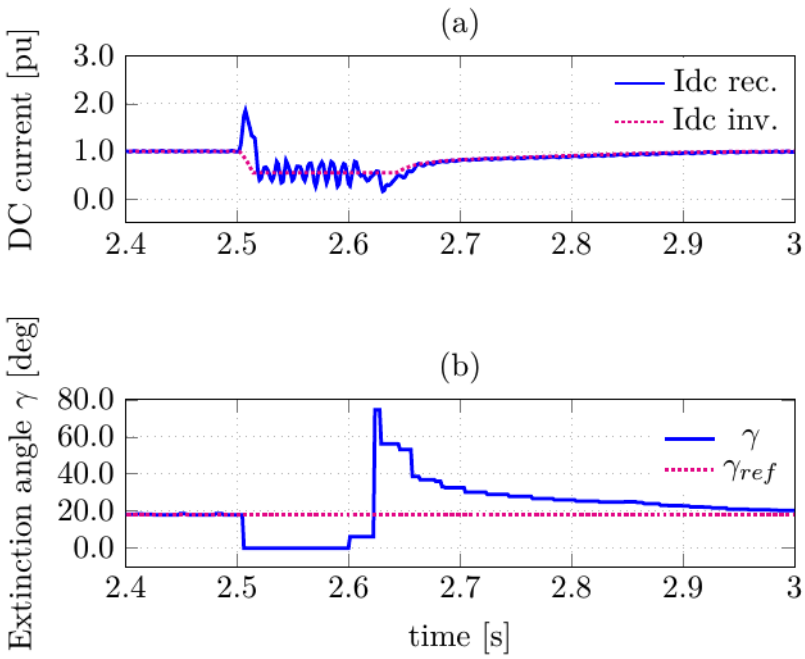

Figure D.5: LCC control objectives at single-phase to ground fault

MMC

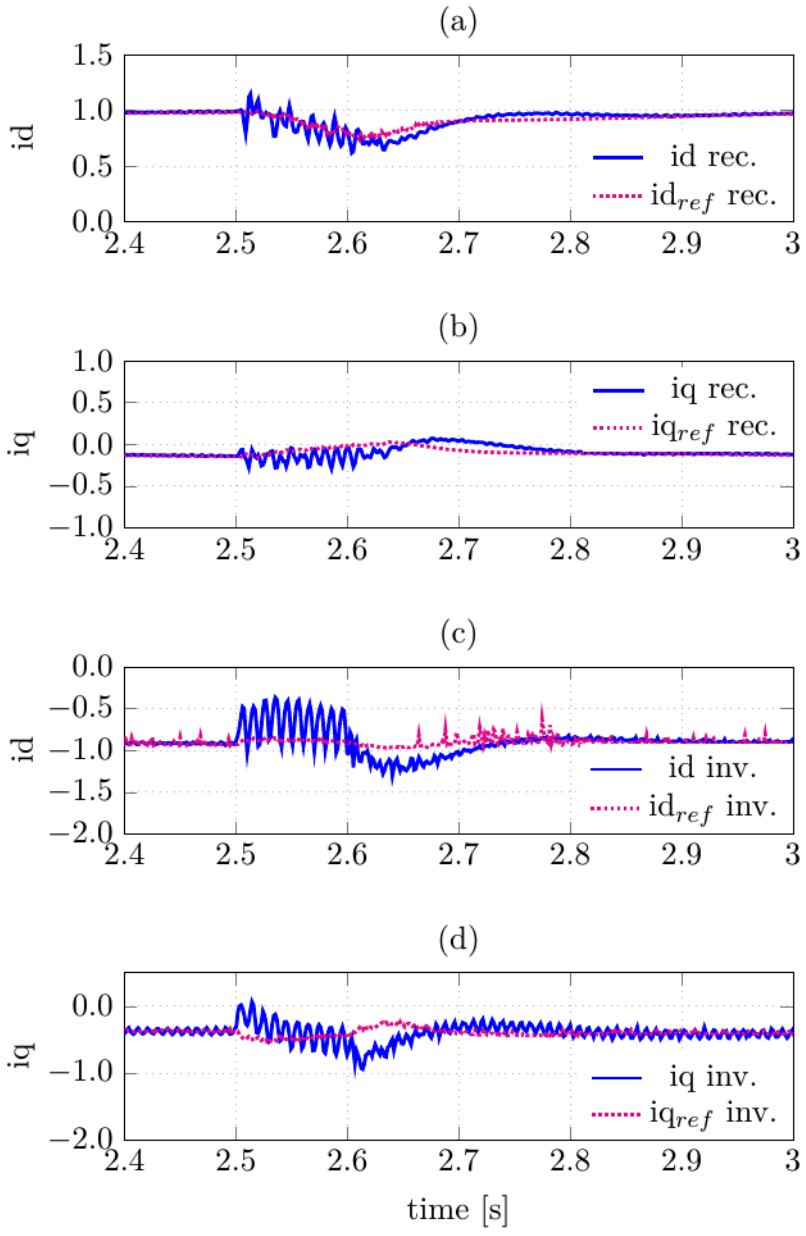

Figure D.6: MMC control objectives at single-phase to ground fault