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Reliability testing of Power Schottky Diodes used for high current rectifying

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Summary

This project was done in cooperation with the TE-EPC-LPC section at CERN. They were experiencing failures in one of their power converter from the rectifying power diodes, and were interested in finding the reason for the failure. They were observing a high leakage current in some of the diodes. The purpose of this project was therefor to investigate the reliability of a diode, and its different failure mechanisms. Diodes can fail from multiple mechanisms some of which can be detected under operation of the diode, in this project the possibility of predicting the lifetime of the diode from its reverse leakage current was investigated.

CERN suspected that the failure was either due to avalanche currents in the device or because thermal cycling in the device. Therefor was a non-repetitive avalanche current test, repetitive avalanche current test and a power cycling test performed on the diode. The non- repetitive avalanche current test gave no failures, proving that single event avalanches were not the reason for failure. In the repetitive avalanche current test the diodes was crashed, but no connection between leakage current and time before failure could be observed. In the power cycle test it was observed that failure was induced much faster in a diode with a much higher reverse leakage current than another.

Sammendrag

Dette prosjektet ble gjort i samarbeid med TE-EPC-LPC seksjonen ved CERN. De var interessert i å finne ut hvorfor en Schottky likeretterdiode feilet i en likerettermodul. De observerte en høy lekkstrøm i noen av diodene. Hensikten med dette prosjektet var derfor å undersøke påliteligheten til dioden, og de forskjellige feilmekanismer den kan gjennomgå. Dioder kan svikte av flere mekanismer og noen av disse kan tenkes å kunne påvises under drift av dioden, i dette prosjektet undersøkes muligheten for å forutsi levetiden for dioden fra den lekkstrømmen.

CERN mistenkte at feilen var enten på grunn av skredstrømmer i enheten eller pga termiske svingninger. Derfor var en ikke-repeterende skredstrømtest, repeterende skredstrømtest og en power cycle- test utført på dioden. Den ikke-repeterende skredstrømtesten i ingen sammenbrudd, noes om beviste at enkeltpuls skred ikke var årsaken til feilen. I den repeterende skredstrømtesten ble diodene kortsluttet, men ingen sammenheng mellom lekkstrøm og sammenbruddstid kunne observeres. I power cycle-testen ble det observert at svikt ble indusert mye raskere i en diode med en mye høyere lekkstrøm enn i en annen diode.

Contents

1 Motivation

CERN is the European Organization for Nuclear Research. Here is about 2 500 employees and 10 000 scientist working to understand more about the smallest parts of matter. The organization was founded in 1954 and sits on the border between France and Switzerland, with most of its workers in the Swiss canton of Geneva.

At CERN, physicists observe what happens when particles collide, to do that they need two kinds of instruments. First, they need to accelerate the particles up to a velocity close to the speed of light with a particle accelerator, and then the particles are collided in huge detectors observing the fragments of the collision's mass and electrical charge to find the particles energy. The accelerators start of as quite small linear accelerators, and the particles are progressively accelerated through a network of growing accelerators, until they end up in the Large Hadron Collider (LHC), the biggest accelerator on earth.

LHC is a 27 km long particle accelerator situated, on average, 100 meters below the soil of the earth. It accelerates protons and lead ions from 450 GeV and up to 4 TeV. It uses radiofrequency cavities to accelerate the particles and superconducting electro magnets to bend the particle beam around the pipe. In the LHC, there are 1232 dipole magnets of 15 meters in length, each used for bending the beam, and there are 392 quadrupole magnets used for focusing the beam. The main dipoles use a current of almost 12 kA to create a magnetic field of 8.4 tesla.

To supply the magnets with current, numerous power converters with different specifications are used. It is the domain of the Electrical Power Converter group (EPC) to design, develop, operate and maintain the power converters. The group is divided into eight sections, each with a different mandate, varying from low power converters to high power converters and control systems. In total, the group consists of about 100 engineers and technicians.

The LHC is normally operated during four years before it is shut down during two for general maintenance and upgrading. During the four years of operation, it is of great importance that everything works. The Low Power Converter section of the EPC group experiences that the rectifying diode of the power module in their LHC

4-6-8 kA -08V converter fails prematurely. The converter under investigation is used for the LHC superconductive magnets. Build from four converter modules, the converter can easily be adapted to diverse load situations. The converter is a 25 kHz switch mode power converter designed to operate in 1st quadrant.

The problem is with a 300 A Schottky rectifier in the TO-244 package. The reasons for the failure are unknown and severe, because it in worst case can obstruct the operation of the accelerator. It is therefore of great importance to the LPC section to understand what causes the failure, and if there are any means to hinder the malfunction. A large number of diodes, which have been operated in the accelerator, have been disassembled from their power converters, and will be used for comparison with unused diodes to investigate the remaining lifetime for a given failure mode.

1.1 Aim of study

The aim of this project will be to help the LPC section at CERN to investigate the cause of failure for their rectifying diode in the LHC 4-6-8 kA -08V converter. It will also be investigated if the reverse leakage current of the diode can be tied to the influential failure. The LPC section suspects that the failure is due to either avalanche currents or thermal cycling in the device. Therefore, both an avalanche current test and a power cycling test will be developed and performed on the diode in question.

2 Diodes

Diodes are semiconductor devices which lead current only in one direction. They are used in a lot of electrical applications, from small signal devices to high power applications. There are numerous different diode types with different attributes, the most commonly used is the PIN diode. Diodes can for instance be used for rectifying, freewheeling or voltage limiting.

The PIN diode is the most common diode sort. It is made up of one silicon crystal. The silicon crystal is N-doped and P-doped, creating a sharp junction. In the N-doped region, electrons are the major carrier charge, while in the P-doped region holes are the major carrier charge. The high concentration of charge carriers on each side of the junction causes diffusion of carriers across the junction. After the diffusion, ionized impurities are left behind, creating an electric field. The electric field opposes further diffusion, creating equilibrium of carrier flow [1]. When a

reverse voltage is applied to the diode, the electric field is enhanced by the external voltage. Therefore, flow of carriers is furthermore reduced. When a forward voltage is applied, it opposes the natural field and opens up for the flow of current.

Whenever the external voltage changes the diode from forward biased to reverse biased, there is a transition time for the current drop time. This is due to diffusion of carriers across the junction, before equilibrium is achieved. The carriers must be withdrawn from the diffusion layer before the diode can be forward biased.

2.1 Schottky diodes

A schottky diode is a diode where the boundary between the different doping in the silicon is replaced by a boundary between doped silicon and a metal interface. Either a N-doped or P-doped silicon can be used, but because of the higher mobility of electrons as the majority charge carrier, N-doped silicon is preferred.

Because the junction in the schottky diode is between a silicon wafer and a metal surface, the diffusion of the carriers is not due to the different concentrations, but the different absolute potential energy in the electrons [1]. The electrons potential energy is much higher in the silicon. Therefore, the electrons flow from the semiconductor into the metal, and hence forming a net negative charge there, while the silicon holds positive charge adjacent to the junction. The electric field created by this division of charges creates the electric field stopping further flow of charges.

Compared to conventional PIN diodes, schottky diodes normally have a shorter transition time from forward conduction mode to reverse bias, and vice versa. On the other hand, the reverse leakage current is larger for the schottky diode than for the PIN-junction diode [1].

The schottky diode is a majority carrier device making conductivity modulation impossible. This makes the forward voltage more dependent on the forward current than in equivalent PIN-diodes. The forward voltage of schottky diodes has negative temperature dependency, meaning the forward voltage is dropping for increasing temperatures. On the other hand, the reverse leakage current is significantly increasing with increased temperature.

2.2 Diode packaging technologies

A schottky diode is in itself a silicon chip connected to a metal interface in both ends. To make the capabilities of the chip applicable to conventional operation, the chip needs to be encapsulated. The encapsulation gives mechanical protection and thermal conduction while maintaining good electrical properties.

The schottky diode technology gives a very low forward voltage drop and short switching times, which result in very low power losses in the semiconductor, compared to conventional diodes. Still, the power losses can amount to several hundreds of watts. The high demand for compact component design sets high requirements to the device package. The package must be able to transport the generated heat away from the chip, ensuring that the temperature within the device is kept at a level which ensures a good reliability. A bigger package will, with the right design, give better thermal conduction capabilities, but at the expense of higher parasitic electrical properties, such as parasitic resistance, parasitic capacitance and parasitic inductance.

For low power applications, discrete packaging is the most chosen. In discrete packages, the semiconductor chip is soldered directly on a solid copper base. This limits the number of semiconductor chips to one per package. On the other hand, the package technology ensures short thermal conduction paths and good electrical performance. The most common discrete package design is the “transistor outline” (TO).

For higher power losses, for example in IGBT's and MOSFET's modules, packaging is favourable. In a module, the chips are electrically insulated from the heat, dissipating mounting surface [2]. This allows for paralleling of chips. And the module can contain integrated circuits, increasing the performance of the device. The modules are, in general, bigger than the discrete packages, which allow better heat conduction.

2.2.1 Discrete packaging for Diodes

Discrete packaging is used for simple electrical devices with low power dissipation. In discrete packages, the semiconductor chip is soldered straight on to a heat dissipating copper plate. The copper plate is in this way used as both electrical and thermal conductor. This design removes the opportunity for electrical insulation, and each package can therefore only serve one electrical task. In the bigger

modules, integrated circuits can enhance performance or perform different operations.

2.2.2 TO package for Diodes

There are many package designs for discrete semiconductors. The most commonly used is the TO- 220 and TO-247. These designs enable electrical contact to the epoxy encapsulated diode chip trough copper leads. The anode lead is connected to the chip with aluminium or copper bond wires, while the cathode lead is directly connected to the copper baseplate. A principal design for a TO package is shown in Figure 1.

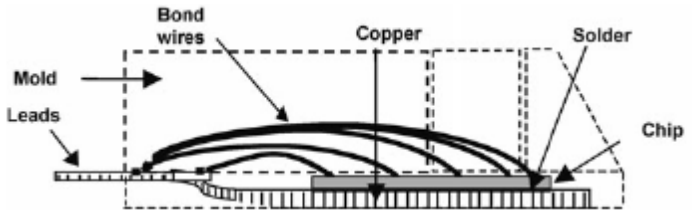


Figure 1 TO package, principal design [2, fig 11.5]

The diode under investigation in this work is packed in the TO-244 package. A TO-244 package can be seen in Figure 2. In the TO-244 package, electrical contact to the anode is given by screw connections on the top of the package. The copper baseplate ensures good thermal connection to a heat sink and serves as an electrical connection for the anode side of the diode. The diode interior is encapsulated in epoxy. This allows for operation and storage temperatures in the range of -55 °C to 175 °C.

Figure 2 Diode in TO-244 package

All the materials used in the design must hold the same electrical and mechanical parameters for the entire temperature range the device is designed for. The package is encapsulated in epoxy, which is a hard plastic with high mechanical strength for a large temperature range, and it shows good electrical insulation. The encapsulation must be closed off to protect the silicon from environmental pollution and damage. To completely protect the silicon from pollution, the silicon is sheltered in a silicone gel. The gel will give complete protection from contamination, and ensures better electrical insulation than air [2].

The copper baseplate is normally screwed on a heat sink under operation. To ensure optimal thermal connection between the baseplate and the heat sink, a thermal paste should be smeared thinly on the metallic interface between them. The paste fills up voids in the metals, excluding the presence of air. Air has poorer thermal conduction abilities than the paste. To optimise the thermal connection, the baseplate is slightly curved, so that when the baseplate heats up, it expands to get optimal thermal connection to the heat sink at high temperatures.

As can be seen in Figure 1, the chip is soldered directly on the copper baseplate. The soldering is done by vacuum soldering, which ensures an even solder layer to get good electrical and thermal conduction. Air voids in the solder layer would increase the thermal impedance of the solder, as will be further discussed in chapter 3.4.

The bond wires connecting the anode to the silicone chip are normally made of aluminium, but trends are going towards copper bonds for higher current applications. The bonds are connected to the anode and the chip using ultrasonic

wedge bonding [3]. This technique ensures strong connection, while avoiding excessive temperatures in the connection process. The number and thickness of bond wires are determined by the rated current of the application.

All the different materials inside the semiconductor package have different coefficients of thermal expansion (CTE). This mismatch in CTE creates stresses at the metallic interfaces when temperatures are altered. The design of the interfaces are normally made so that the thermal expansion is least stressing under the rated load conditions for the device.

2.3 Estimation of Tj from Vf(T)

In a power cycle test, the stress is determined by the temperature swing and the absolute temperature of the junction. It is therefore important to be able to measure exactly the temperature in the diode junction. The maximal junction temperature ($T_{j,max}$) and the junction temperature swing (ΔT_j) is defining the stress level, and are therefore essential for the components lifetime under the test.

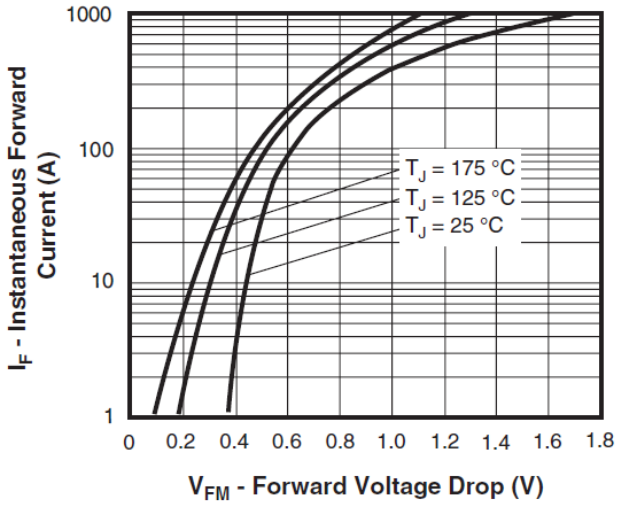


Figure 3 Maximum Forward Voltage Drop Characteristics [Datasheet].

Because the diode chip is packed in neither physical contact nor free vision to the chip can be established. This makes accurate measurements of the chip temperature very challenging. Instead of directly measuring T_j, the diodes thermal and electrical parameters can be used. Since the forward voltage of the diode has a negative temperature dependency, the voltage will drop linearly with increased temperature, the voltage decays linearly with approximately -2 mV/K. Figure 5 shows a calibration curve for a schottky diode.

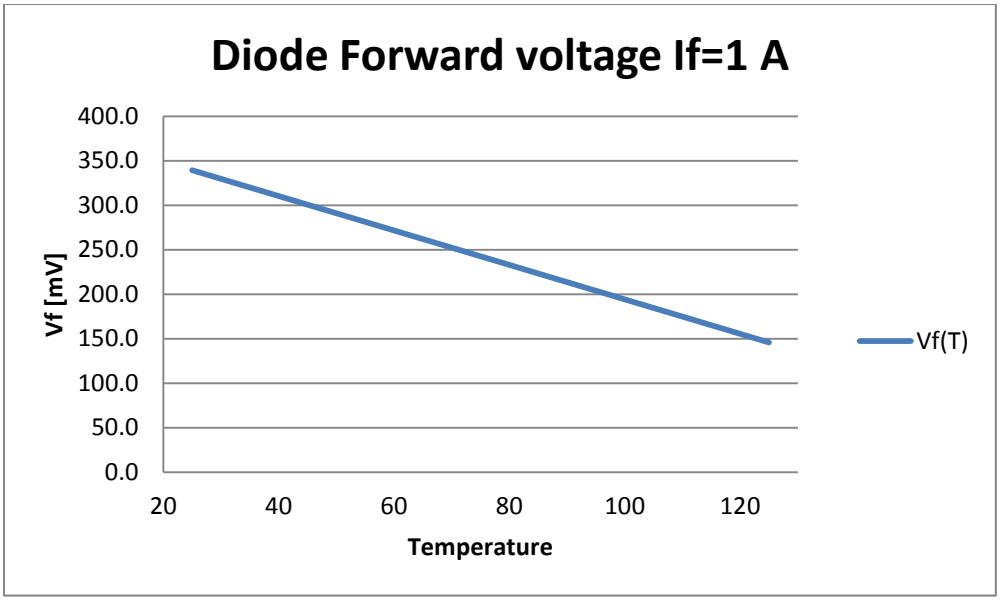


Figure 5 Linear fit of Vf(T) for calibration

By constantly conducting a small sensing current through the diode, an accurate temperature estimation can be made from the voltage drop. The measured voltage can be compared to the calibration curve seen in Figure 5 for reference.

3 Failure mechanisms in power semiconductors

There are numerous reasons why a semiconductor can fail. In this chapter, some of them will be discussed. Because of the severe operation conditions power semiconductors normally are operated in, they are prone to repeated stress, and small irregularities can cause fatalities. When analysing the failure of a device, the key failure mechanism can be hard to pinpoint, because they are strongly interdependent. The interdependency creates the possibility that failure mechanisms accelerate each other.

3.1 Overheating

The theoretical upper limit on the internal temperature of a semiconductor device is the so-called intrinsic temperature, T_i, which is the temperature at which the intrinsic carrier density in the most lightly doped region of the semiconductor device equals the majority carrier doping in that region [1]. However, a power semiconductor will fail from high temperatures before the intrinsic temperature is

reached in the silicon junction. Excessive temperatures can cause materials inside the package to melt or burn. Semiconductors are therefore normally rated for temperatures between 125 °C and 175 °C. Burnout failures are often observed as a final act of wear-out, or as a consequence of a reason for failure occurring randomly [4].

3.2 Bond Wire Fatigue

The wire bonds which connect the active area of a semiconducting device with the electrical connection to the case are very thin and prone to thermo-mechanical stresses. Bond wires normally have a diameter up to 500 µm. The thin wires are subjected to high temperatures caused by both the power dissipation in the silicon and the wire itself. Bond wires fail predominantly because of shear stresses between the bond pad and the wire, or by repeated flexure of the wire [4]. A failure in wire bonds will lead to current redistribution or a change in the contact resistance, causing the forward voltage to increase [4].

There are normally two ways a bond wire can fail: Bond wire lift off and bond wire heel cracking. A bond wire lift off can be seen inFigure 6. In the picture, it can be seen how the bond wire loses contact with the metal interface.

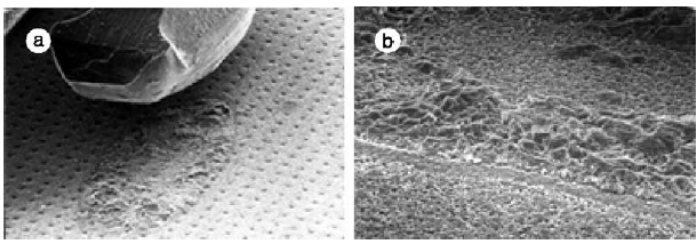


Figure 6 (a) Bond wire lift off. (b) Footprint off an aluminium wire after lift-off [4, fig 5]

The foot of the bond wires is connected to the metal interface in a longer junction. At the end of the foot, the wire is bent up away from the chip towards the copper lead. The bend is an especially fragile part. When a bond wire is undergoing thermal cycles, it is flexed. During the flexing, the foot is fixed to the surface, while the rest of the bond is moving. The relative motion of the wire with regards to the foot causes a shift in the angle of the bend, which creates small ruptures in the bend, eventually causing it to break. The rupture can cause full disconnection of the wire or greatly reduce the electrical contact to the chip.

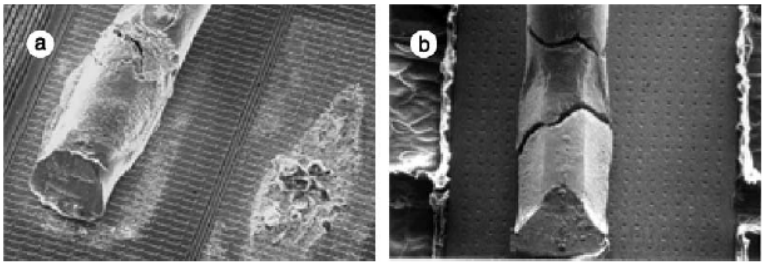


Figure 7 Two examples of bond wire heel cracking [4, fig 7.]

In Figure 7, it can be seen how the bond heel can crack. In picture (a), the wire still is in connection with the chip, but the contact surface is greatly reduced.

3.3 Reconstruction of metallization

Under thermal cycling of the semiconductor, chip reconstruction of the contact aluminium film can occur. This may be due to periodical compressive and tensile stresses caused by the significant difference in their coefficients of thermal expansion (CTE) between aluminium and silicon [4]. The silicon is very stiff and only expands with a coefficient of 2-4 ppm/K, while aluminium can expand as much as 23.5 ppm/K [2]. The stress relaxation can cause extrusion of aluminium grains or cavitation effects in proximity of the grains by diffusion creep, grain boundary sliding or plastic deformation [4]. The effects of reconstruction of metallization can be optically observed as a dark spot on the metal film, as the roughness of the reconstructed metal scatter the light.

The roughness of the metal film reduces the effective cross section of the layer, this results in a higher electrical resistance. The increase in electrical resistance can be observed as an increase in the forward voltage for the device [4].

Ciappa (2002) [4] reports that aluminium reconstruction does not appear for temperatures below 110 °C. However, current redistribution by bond wire fatigue causes an increased temperature adjacent to the remaining bonds, which eventually can cause reconstruction of the metal film. On the other hand, it has been reported [2] that reconstruction can be more extensive in areas not covered by other materials, and that a cover layer can supress movement of aluminium grains.

3.4 Solder fatigue

In semiconductors, solder alloys are used to hold different metallic parts together. The solder is one of the most fragile parts of the semiconductor module. The great mismatch in the CTEs of the different materials causes fatigue in the solder under thermal cycling.

When soldering metals together, the bonds are mainly created by intermetallic phase located between the bulk of the metal and the solder [4]. The high temperatures the device is operated under causes such metallic phases to coarsen, and subsequently to crack.

In the process of soldering, voids can occur within the solder or between the solder and the semiconductor layers. These voids and consequential cracks can increase the thermal impedance (R_{th}) of the device [4]. This increase in R_{th} raises the junction temperature further, and hence accelerates failures in the device. In particular, large gaps in the solder limit the local heat transfer from the junction to the case. Increased heat resistance leads to increased temperatures which can lead to unbalanced current distribution and enhanced stress.

3.5 Current filaments

Current filaments are narrow current channels occurring in the semiconductor. They can occur in both the semiconductors conducting state and the blocking state during avalanche conditions. Current filaments cause the temperature to increase locally creating a hot spot in the silicon. In the hot spot, temperature can reach catastrophic levels, resulting in thermal runaway and burnout [5].

4 Accelerated Life- Time Stress Tests

Reliability is the ability of a system or component to perform its required functions under stated conditions for a specified amount of time [6]. For power semiconductors, this time can range from a few years and up 30 years. Because of the long operational time of the device, accelerated life-time testing is a helpful tool to establish the expected lifetime. In an accelerated life-time test, the components or system under test are exposed to higher or more frequent stress than under their operating condition. The result from the tests can be used to predict the lifetime of a device in an application given its operational conditions.

Accelerated life-time tests are developed to only test a very specific part of the operation. Lifetime should therefore be predicted with basis in numerous tests. Every test should be applied to a different critical phenomenon in the application. However, under operation, all the components are exposed to the full range of stresses, and failure assessment can be more intricate. A good understanding of all the tests and how the failures affect each other is important to correctly predict the life-time.

An exact failure limit must be defined to know the goal of the test. A robust product is defined as a product that is sufficiently capable of functioning correctly and not failing under varying application and production conditions [6]. From this, each manufacturer or system designer must define acceptable limits to the components.

In this project, the focus is on the avalanche current test and power cycle testing. Before a more extensive description of those test are given, a short description of some common reliability tests are presented.

4.1 High Temperature Reverse Bias Test (HTRB)

In the high temperature reverse bias test, the device under investigation is subjected to a reverse voltage in the range of its blocking capability, while the ambient temperature is close to the operational limit of the device. The test can reveal existing weaknesses or degradation effects in the field depletion structures at the device edges and in the passivation area. Ions can accumulate in areas of high field strength and create surface charge. Ions are unwanted in the silicon, but can occur as contaminations from assembly process or excess doping agents. The surface charge can impact the electric field and generate higher leakage current [2].

The failure criterion of the test is an increase in the reverse leakage current at rated blocking voltage, after the device is cooled down. An increase in the reverse leakage current after a given test duration would verify an instability in the devices leakage current, which is the goal of the test [2].

4.2 Temperature Humidity Bias Test (H3trb)

The temperature humidity test is confirming the impact of humidity on the long term performance of a power component. Power module packages are not necessarily hermetically sealed, and humidity can with time intrude the package.

Once inside the package, the humidity can reach the chip surface and junction passivation where it can initiate degradation processes such as corrosion [2].

4.3 Temperature Storage Test

Different materials may degrade in high or low temperatures. In the storage test, the materials performance is tested at high and low temperatures. It is necessary that all the materials keep their abilities in the whole storage temperature span. Storage temperature is for semiconductors meant as the non-operational temperatures for a power electronic device installed in an application [2].

4.4 Thermal cycling and thermal shock test

In thermal cycling and thermal shock tests, the tested semiconductor is subjected to temperature swings from external sources. The difference between thermal cycling and thermal shock is the difference in the rate of change for the temperature around the test object. In thermal cycling, the temperature can change with about 10- 40 °C/min, while in a thermal shock test the complete ambient temperature swing is done in less than a minute. The thermal shock can often be performed by moving the test object between two chambers, holding different temperatures [2].

It is important that thermal equilibrium is achieved for every cycle, so that all the materials in the device experience the full mechanical stress of the test. Different mediums give different coefficients of heat transfer. A liquid-to-liquid thermal shock test can give the fastest temperature swing for the whole system [2].

When temperature in a semiconductor is changing, the materials are expanding or contracting with the temperature. Different materials have different CTEs, and so the flexing of the materials causes mechanical stress. The combination and design of materials determines the lifetime under temperature swings. Smaller packages are less prone to thermal cycling than bigger modules.

4.5 Radiation test

For the power converter placed in the LHC tunnel, radiation can have a huge impact on a semiconductors lifetime. It is therefore necessary to find semiconductors with a high ruggedness towards total ionizing dose, displacement damage and single event effect [7].

4.6 Avalanche current test

In rectifying and switching circuits, the leakage and stray inductances causes high reverse currents in the semiconductors blocking mode. These currents are known as avalanche currents. The avalanche currents are unwanted, because they can cause current filaments and local overheating which can destroy the device.

There are mainly two topologies where avalanche currents are considered hazardous to semiconductors. In rectifier modules in power converters there can be placed a transformer. Rectifying diodes is placed so that the voltage and current in the transformer becomes unipolar after the diodes. The leakage inductance in the transformer creates a delay in the current with regards to the voltage which makes the current continue to flow after the diode goes into reverse bias.

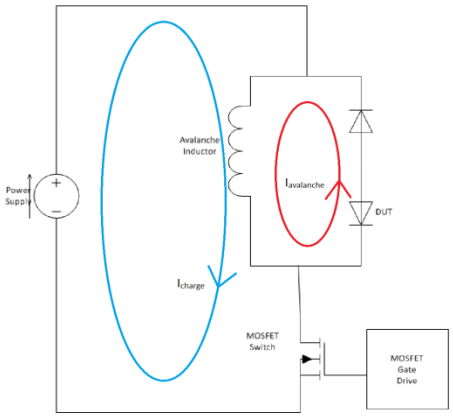


Figure 8 Example of avalanche current test setup

The other operation condition for avalanche events is if a power semiconductor switch is switching an inductive load, and the switch is opened while current is high. This is normally termed hard switching.

In the avalanche current test, or unclamped inductive switching test, a power semiconductor's ability to withstand hard switching is verified. A load current is ramped up through an inductor and a switch. When the inductor holds the desired energy, the switch is triggered to open, and since the current cannot change instantaneously, the current continues to flow. Dependent on which type of semiconductor is under testing, the current either continues through the blocking switch or is rerouted in a secondary loop through a blocking device with lower blocking capability. An example of an avalanche current test setup where a diode is being tested is shown in Figure 8, the blue circle indicates the current path during the charging phase. The red circle is the current loop after the switch is opened and the current is forced through the device under test (DUT).

Because the semiconductor is in blocking mode, the blocking voltage will increase up to the device's stationary breakdown voltage. After the breakdown voltage is exceeded, the device goes into avalanche mode. In avalanche mode, the behaviour of the device resembles a zener diode. The voltage is kept steady during the avalanche period, while the current decreases linearly. The energy stored in the inductor will be dissipated in the semiconductor junction. During the power dissipation, the junction heats up rapidly, and excessive temperatures can lead to failure. Failure can also occur from formation of current filaments [8]. The energy dissipation of one avalanche can be calculated as:

$$E = \frac{1}{2} * V_{breakdown} * I_{peak} * t_{ava}$$

Where E is the energy, $V_{breakdown}$ is the voltage level on the test object, I_{peak} is the initial peak current in the inductor, and t_{ava} is the time until the current reaches zero ampere. The avalanche time is very dependent on the inductor size and peak current. Typical avalanche waveforms are shown in Figure 9.

A semiconductor which experiences avalanches normally has two ratings related to avalanche events, one for single event avalanches and one for repetitive avalanches. Both of the ratings are equally important, and should therefore be verified. To test the non-repetitive avalanche ruggedness of the device, the inductive energy must be many times higher than in the repetitive test. The failures from the test are expected to be similar, but in the repetitive test it is important to remove the dissipated heat between the avalanches. Lack of heat removal could result in failure from overheating unrelated to the avalanches.

The desired failure mechanisms arise from the fact that the avalanche currents carry high power densities. All this power is dissipated internally in the semiconductor. Current filaments may occur in the silicon crystal. Current filaments can cause localized overheating which can be destructible for the device [9]. Failure can also occur from high power densities in the avalanches, causing rapid uniform heating of the diode.

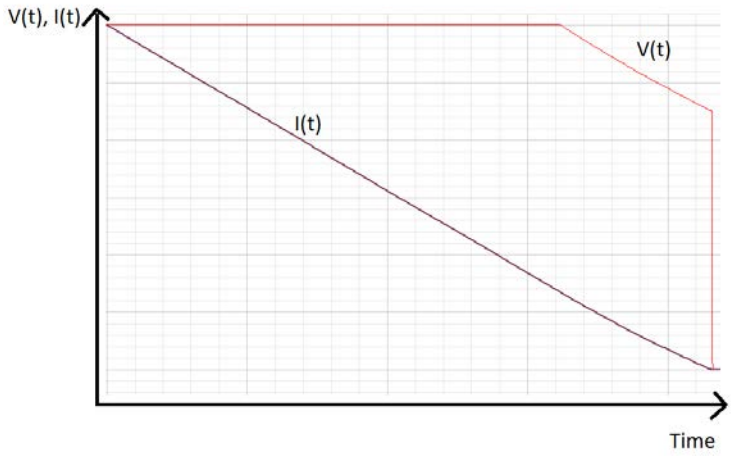


Figure 9 Voltage and current waveforms in the reverse direction of the semiconductor during avalanche

4.7 Power cycling

The Power cycling test is an accelerated lifetime test, which verifies a power semiconductors ability to sustain repeated temperature cycles. In the test, a semiconductor is repeatedly heated by the forward conduction losses in the device. The purpose of the test is to simulate a situation where a cyclic load is causing a repeated heating and cooling of the junction of a semiconductor.

There are two operation conditions which can cause detrimental power cycling. Low operating frequency would allow the generated heat from conduction losses to be transferred away from the semiconductor junction, and a low temperature to be reached before the next load cycle reheats it. This kind of load profile can for example be found in wind power generators, electric vehicles or traction applications.

The other operation condition which leads to power cycling of the power converter components is a cyclic load. At CERN, the superconducting electromagnets creating the magnetic field for the LHC require a current of 12 kA. Because of the great inductance of the magnet coil, the current is ramped up during approximately 20 min. The converter is only operating while the current is ramped. Once the desired current is reached, the converter is disconnected. This gives a relatively short load pulse where the converter is heated before it cools

down. Each rectifying diode, in the 4- 6- 8 kA-8V converter, can under operation conduct a peak current of 250 A. This current, with a voltage drop of ca. 0.7 V, result in a power loss of 175 W. The power loss, calculated with thermal impedance of the diode, creates a junction temperature increment of 42 °C to the heat sink. When the converter is unloaded, the diode junction cools down to the heat sink temperature. How often the magnet current needs charging is varying, and is depending on which projects will be performed in the accelerator.

Another example of a cyclic load profile can be in electric vehicles that are driven several times per day. The converter heats during operation of the car and cools when the car is parked. A normal usage pattern can cause thousands of power cycles during a year.

Because different materials have different coefficient of thermal expansion, mechanical stress occurs at the material interfaces when the junction is heated. The materials experiences strain and relaxations following the temperature profile in Figure 9. This thermal stress leads in the long run to fatigue of materials and interconnections [2]. The fatigue can lead to failures as bond-wire lift off, bond-wire heal cracking, aluminium reconstruction, and crack propagation as described in chapter 3.

In a power cycle test, a load current is conducted through a power semiconductor. The semiconductor is heated by its internal losses. When the desired junction temperature is reached, the load current is switched off. The test object should be placed on a heat sink, so that it cools down to its low temperature, normally close to the heat sink temperature, during the off period. Once the T_{low} is reached, the load current can be reapplied. During the test, cooling on the heat sink should be so extensive that the heat sink temperature is relatively steady, while the junction of the tested semiconductor experiences sharp temperature fluctuations. The case of the semiconductor will have a temperature somewhere in between the junction and heat sink.

The difference in temperature, ΔT_j, is normally used as the defining parameter for the test. ΔT_j is dependent on two parameters, the on-time (t_{on}) and the load current magnitude. The on-time is the time duration of the load current pulse on the test object. The load current is normally chosen to the rating of the device or the current it will be conducting in the application it is tested for. t_{on} is then chosen to give the desired ΔT_j.

Next a reference temperature must be chosen. Studies by Bouarroudj (2008) [10] have shown that the degradation is strongly dependent on temperature levels, $T_{j,max}$ and $T_{j,min}$. The coolant temperature is normally defining the $T_{j,min}$. Together with the cooling time period (t_{off}), it defines the lower temperature the device will be able to reach. The coolant temperature would normally be chosen equivalent to the storage temperature for the device application. The reference temperature can also be given by the medium temperature $T_{j,m}$. This is defined as $T_{j,m} = T_{j,min} + \frac{T_{j,max} - T_{j,min}}{2}$ [2].

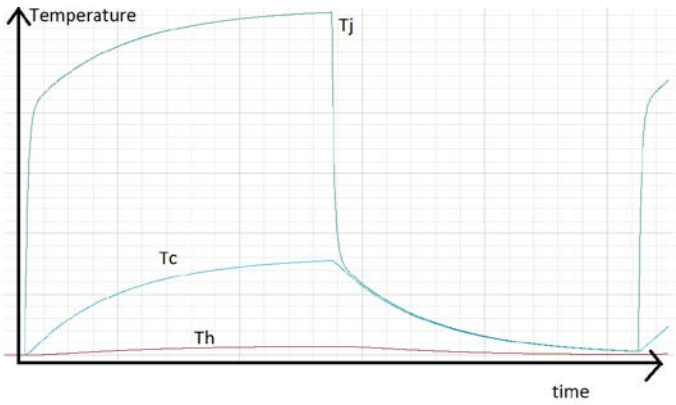


Figure 10 Temperature development from one power cycling pulse

Figure 10 shows a temperature profile of the semiconductor junction and case for one load cycle of a power cycle test. The figure shows the junction temperature changes rapidly compared to the case. This is because of a great difference in heat capacitance. Because of the big difference in heat capacitance, steep temperature gradients occur from the junction to the case.

In switching semiconductors such as IGBTs or MOSFETs, both active and passive power cycling can be applied. In passive power cycling, an external switch is used to switch the load current between the DUT and a secondary circuit. In passive power cycling, the test object is continuously switched on. In active power cycling, the tested semiconductor is switching the load current itself. Active power cycling can therefore not be used for diodes. In active power cycling, pulse width modulated switching can be used to control the current, this may cause higher stress on the device, since also switching losses must be considered.

4.7.1 Failure limits in power cycle testing

As described in chapter 3, there are numerous failure mechanisms in power semiconductors. The failures cause changes in the electrical or thermal parameters of the device. A close eye should be kept at the development of V_f and R_{th}, as both these parameters are dependent on materials affected by the failures. An increase of up to 20 % in both these values will typically indicate imminent breakdown, as the failures have a tendency to escalate as there are close correlation between the failure mechanisms [4, p. 392].

In this work, the test will be run until the diode collapse completely. Monitoring of parameters remains important, as they give a good indication of deteriorating in the device and to control the stress level in the test.

5 Methods

The device to be tested, is a power schottky diode in the TO-244 package. The diode is rated for 300 A, and the maximal reverse voltage is 45 V. The diode has an avalanche rating of 202 mJ for non-repetitive avalanche currents, and the repetitive avalanche current rating is 30 A. The TO-244 package consists of two diodes, with a common copper plate as a cathode. The terminals for the diodes and anodes are separated, so they can be paralleled.

This project consists of mainly three tests. Two of them are reliability test, and the third one is a parameter test. The tests are performed on diodes which have previously been operated in a power converter in the LHC at CERN.

5.1 Reverse current tester

In this project, the significance of the reverse current on the reliability of the device will be investigated. Therefore, the reverse current is measured of every test object on beforehand. This is done by connecting a small 10 ohm resistor in series with the diode. The reverse current is found by measuring the voltage drop over the resistor when the rated reverse voltage is applied to the diode.

With the small resistor and the leakage currents low magnitude, the voltage drop across the resistor will be in a major order of magnitude lower than the voltage across the test object. The datasheet specifies a reverse leakage current of 10 mA for T_j = 25 °C and 90 mA for T_j = 125 °C. The datasheet gives the upper limit for the device, so the experienced reverse leakage current should be significantly lower.

The reverse leakage current should also be investigated at increased temperature. This will be achieved by placing the test object on a regulated heat plate. The reverse current is strongly dependent on the temperature, and its dependency can be different between the different devices. This means that the reverse current at both high and low temperature should be taken into consideration.

To find upper and lower limits, as well as expectation value and standard deviation, for actual reverse leakage current, 40 diodes will be tested at both 25 °C and 125 °C under the rated voltage of the device. The reverse current will also be found for every diode about to undergo avalanche current or power cycle testing.

The reverse leakage current test will be performed by applying the rated voltage of 45 V from the cathode to the anode of each DUT, while measuring the voltage drop over a 10 Ω resistor. Forty diodes will be tested, with a baseplate temperature of 25 °C, and thereafter retested at 125 °C, to find the expected reverse current and the standard deviation. The reverse leakage current will also be tested, at 25 °C and V_r= 45 V, for all devices about to undergo avalanche current or power cycle testing.

5.1.1 TO- 244 heat plate

The heat plate is custom made for this diode package type. By series connecting the two diode legs of a diode in the TO-244 package, a heat source capable of heating the DUT baseplate up to temperature of 175 °C can be achieved. The forward losses of the diode legs are used to create a uniform temperature in the baseplate of the heat plate. The test object is then placed with its baseplate on top of the heat plate, electrically isolated with thermal pads for good thermal conduction.

The temperature is controlled by placing a linearized NTC thermistor between the two baseplates. The NTC is connected to a differential amplifier creating a temperature dependent voltage, which can be used to control the output of the power source.

5.2 Avalanche current test setup

In an avalanche current test, an inductive current is forced on the reverse direction of the test object. This can be achieved by charging an inductor with a current before it is switched from the power source and on to the DUT. The current is then forced through the reverse direction of the diode making it behave like a zener diode.

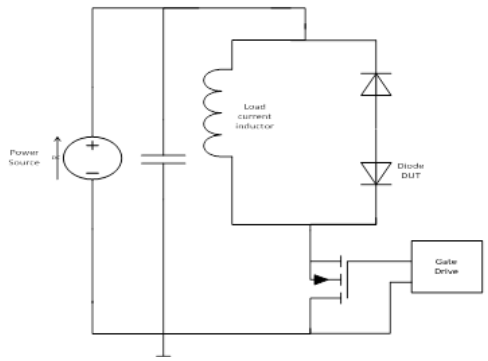


Figure 11 Simplified electrical circuit for the avalanche current test

There are many possible circuit setups that can be used for the avalanche test. In this project, a single switch setup was chosen, with a double diode parallel to the inductor. A setup with only one switch, as can be seen in Figure 11, is preferable, because it makes the operation of the circuit easier and more reliable. The switching MOSFET should be chosen so that the breakdown voltage is much higher than the blocking voltage of the DUT. This ensures that the test object goes into avalanche mode before the MOSFET. For this project, a MOSFET with blocking capability of 500 V was chosen.

To verify the current through the test object, a pulse transformer should be connected in series with the diode. With its short response time, the pulse transformer can accurately measure the peak of the avalanche current. Because the pulse transformer field current shortly draws part of the transformed current,

the pulse transformer is not suitable for longer signals. However the duration of the avalanches is so short that an accurate measurement of the entire pulse can be achieved.

The voltage measurements would preferably be done over the DUT, but that would require a floating oscilloscope or a differential probe. However, the MOSFET drain source voltage will have the same shape as the avalanche voltage of the diode. This allows for measuring the drain voltage of the MOSFET, and subtracting the voltage in the capacitor.

To ensure clean measurements, a small snubber should be placed on the MOSFET, reducing the hardness of the switching slightly. The snubber should be made, so that it filters noise while not conducting big portions of the load current. A big snubber would reduce the stress on the test object by draining part of the current.

In the single pulse event, the capacitor of Figure 10 can be omitted, and the constant current of the power source will then be the peak avalanche current. The MOSFET is kept closed until a stable current is supplied from the power source, and the switch is then opened and the inductor current forces through the DUT.

In the repetitive operation of the circuit, the capacitor is used to supply the peak currents and ensure stable voltage in the circuit. By demanding a maximal voltage drop of 5% during the charging of the inductor, it can be found that a capacitor value of at least 2 mF is necessary.

The diode connected to the DUT's anode ensures that the load current goes into the inductor and not forward, biasing the test object.

As mentioned in chapter 4.6, the repetitive avalanches power dissipation heat the diode junction. It is of importance to the test results to keep average T_j of the test object below the rated temperature. This will be maintained in two ways. First by placing the DUT on a heat plate so that the dissipated heat is absorbed in the heat capacitance of the plate. The increased heat capacitance ensures a slower system. The system is not cooled, so eventually the base plate temperature can rise to excessive levels.

The second moment is that the thermal impedance from junction to case is strongly dependent on the duty cycle of the switching, see Figure 12. Higher energies give higher duty cycle, because of a longer avalanche time. This means

that an increase in the avalanche energy equivalent to a certain power loss will in fact cause a greater increase in temperature than a corresponding forward conduction loss.

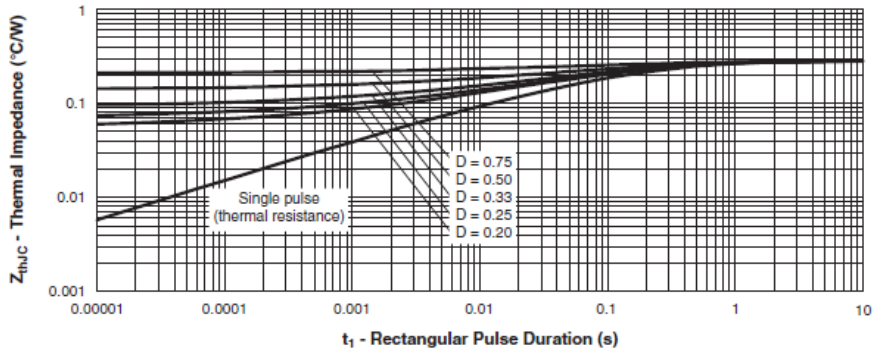


Figure 12 Thermal impedance for given Duty cycles vs pulse time from datasheet

It is of great importance with a clean switching, so that the stress on the test object is as severe as anticipated, therefore the current routes should be as short as possible. This is to reduce any unnecessary stray inductances in the switching circuit. Stray inductances will enhance the current fall-time through the switch and increase the current rise-time through the DUT circuit branch.

To be able to compare devices ability to withstand avalanche currents to their reverse current, the reverse current must be obtained from each DUT before the test is commenced.

In the non-repetitive avalanche current test, the DUT is placed in a test circuit as shown in Figure 10. First, the MOSFET will be turned on by applying 15 V from its gate to source, while the MOSFET is turned on the current ramps up in the inductor. Once the inductor current is at the desired level, V_{gs} on the MOSFET is switched to -15 V opening the switch. All the current is then forced on the DUT cathode. Before the test is started, every DUT's reverse current will be tested.

The test will be started at the energy level specified in the datasheet. Then the current will be stepwise increased until the energy stored in the inductor is sufficient to destroy the device. If not a sufficient current can be found, the inductor size will be increased from the initial 1 mH.

The same setup is used for the Repetitive Avalanche current test, as for non-repetitive, except for the 2 mF decoupling capacitor showed in Figure 10. A square voltage signal controls the MOSFET switch by giving respectively 15 V and -15 V to close and open the switch. The square wave has a frequency of 20 kHz and a duty cycle of 0.29 with the positive voltage as t_{on}. With a capacitor voltage of 23.5 V, the peak current in the inductor did charge up 23.5 A. This corresponds to an avalanche energy of 4 mJ in the 14.5 mH inductor. During the test, the DUT will be placed on a heat plate holding 100 °C. The test will be performed on approximately 50 devices until they fail.

5.3 Power cycling test setup

Purpose: In the power cycling test, the junction of the tested semiconductor is heated by the losses in the device, as explained in chapter 4.7. By switching the power on and off the temperature of the die is cycled between high and low temperatures. The thermal flexing of the materials creates stresses, eventually destroying the device. To achieve this cycling, a constant load current will be switched between two test objects.

In the power cycle tester, the diode will be kept in a forward biased state, while the current is switched between two current paths by MOSFET switches. This is described as passive switching for switching semiconductors, in comparison to active power cycling, where the test object is actively switching the current. Active power cycling cannot be done with diodes.

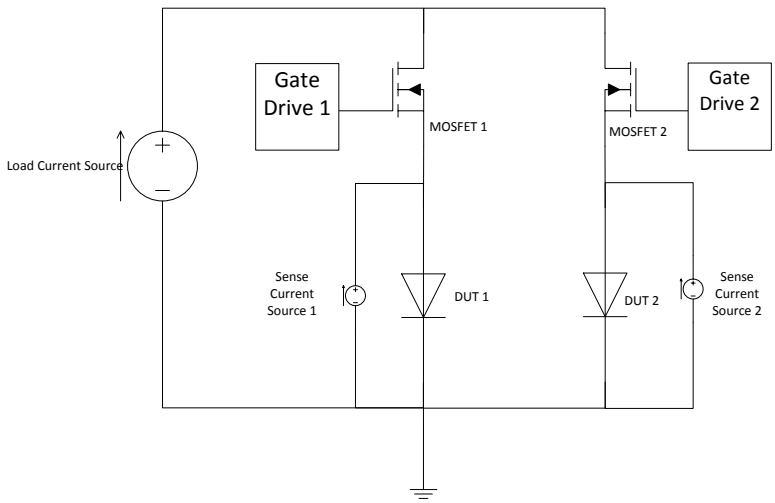


Figure 13 Electrical circuit of the power cycle tester.

In Figure 13, the electrical circuit of the power cycle tester is shown. The circuit diagram shows how the load current is supplied to identical electrical branches. The MOSFETs are controlled in anti-phase, so that the constant load current is alternated between the two test objects in equal time periods.

The sense current shown in Figure 13 is a current constantly conducted through the test objects, in the forward direction. The magnitude of each sense current is 1 A. The forward voltage drop from the sense current enables estimation of T_j during the cooling period of each DUT. The low value of the current allows it to be lead through each test object for the entire test period, without affecting the results.

In Figure 13, it is indicated that there are two test objects in the circuit. This is practical for several reasons. For one it makes comparison of the test objects faster, as they are compared directly under exactly the same conditions. This allows for faster testing than if a similar diode would be replaced. Also, by placing to equal diodes in the two circuit legs, it is ensured the best possible voltage distribution. The only voltage difference from the branches would be the difference due to the temperature dependency of forward voltage in the semiconductors (about 0.2 V for 100 °C and 300 A, from the datasheet). A steady voltage ensures a constant current. The test objects must be from the same manufacturer, because the base plate has different volume, and therefore unalike heat capacitance. A higher heat capacitance would give a slower temperature

development, and hence a lower max temperature. This would give a lower stress on the junction, and therefor alter the test results.

The switches are also conducting the load current. To reduce the power dissipation in the MOSFET, and by that limit their life time limiting power cycling, two paralleled MOSFET are used for each switch. By placing two MOSFETs for each switch, the power dissipation is halved and the stress on each of the switches is reduced. The MOSFETs used should be packaged so that the switch has low thermal impedance, leading to a reduced temperature swing in the MOSFET. To avoid excessive power losses and heat production, the on-resistance of the switch should be as low as possible. These two factors would reduce the probability of power cycle related failures in the MOSFET. The positive temperature dependency of the MOSFET on-resistance makes them ideal for paralleling. An unevenly distributed current would lead to higher power loss in one MOSFET, increasing T_j and hence the resistance. The increased resistance would in turn reduce the current. [1]

The load current is switched between two DUTs in equal time intervals. In the time when the current is lead through one diode, the conduction losses heat it up. After the time interval is over, the current is switched. Since there is no significant power dissipation in the diode, it cools down. The thermal behaviour of one test object can be presented schematic, as shown in Figure 14.

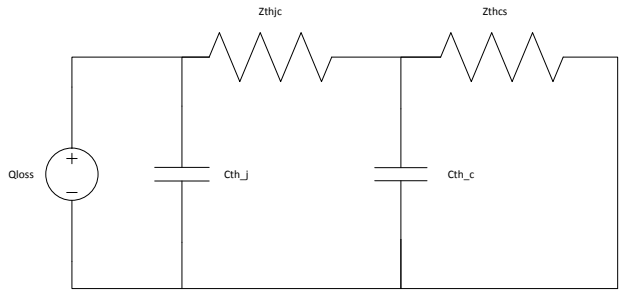


Figure 14: Thermal equivalent DUT

In Figure 14, the thermal behaviour of a power semiconductor is illustrated. Q_{loss} are the electrical losses in the junction of the device. The heat is transported from the junction and off the device through the case. The capacitor C_{th_c} is the heat capacity of the semiconductor case. In the TO-244 package, it consists mainly of the copper base plate connecting the device to heat sink. The capacitor Cth_j,

given in [J/K], is the heat capacity of the interior of the semiconductor. It can normally be neglected for calculation purposes, because of its small magnitude compared to Cth_c. The two impedances represent the temperature drop through the materials. They are given in [K/W]. The heat sink would be represented as a big capacitor with a small thermal impedance to ambient or cooling medium's temperature. As this causes the heat sink temperature to be fairly constant, the heat sink is represented as a short circuit.

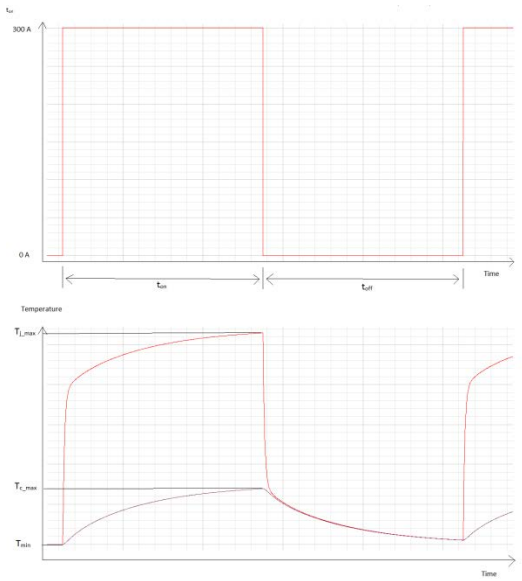


Figure 15 Current and temperature waveforms in one test object

Figure 15 shows how the junction and case temperature of one tested diode will wary in line with the current. To establish the magnitude of T_{j_max} and T_{min}, the voltage should be measured shortly after the current is switched off, and just before it is switched on.

The test circuit should be made so that the inductances are reduced. Stray inductance reduces switching speed and causes voltage spikes, because of rapid current change during commutation. Low inductance is achieved by reducing the length of all the current paths and using the heat sink as a low side conductor.

When the MOSFETs are switched, there is a moment where both the legs are blocked. In this instant, the voltage will increase rapidly causing a voltage spike.

The voltage spike causes an over current spike when one current path is reopened. To reduce the voltage spike, a capacitor of 400 µF is placed between the drain of the MOSFETs and the reference point at the circuits ground. The capacitor charges off the current supplied in the period where both the switched are closed. This reduces the voltage spike and the over currents.

5.3.1 Cooling

To cool the semiconductors, forced air cooling is used. The circuit is placed in the middle of a heat sink designed for 400 W of dissipation power. Two DC fans, each with 12.5 W of blowing power, are creating the wind through the wings of the heat sink. Using an air cooled system is disadvantageous to a water cooled system, in the sense that the air temperature cannot be controlled. The ambient air will be blown through the system, and hence the input temperature of the coolant will be limited to room temperature.

The power cycle test is performed by applying 200 A, 8 s current pulses to two DUTs. The diodes are placed on an air cooled heat sink, and a one ampere sensing current is used to estimate the junction temperature during the cooling period. A 400 µF capacitor is used to reduce voltage spikes during MOSFET switching.

6 Results and discussion

6.1 Reverse current

6.1.1 Reverse current at 25 °C.

At 25 °C, the DUT with the least reverse current was DUT 19 with a reverse current of 64 µA. DUT 32 had the highest reverse current leaking 150 µA at V_{rr}. The mean value for the group was 80 µA with a standard deviation of 18 µA. The values are plotted in Figure 15, and the full table are given in attachments.

6.1.2 Reverse current at 125 °C

At 125 °C, the DUT with the least reverse current was DUT 30 with a reverse current of 45 mA. DUT 29 had the highest reverse leaking current with 75 mA at V_{rr}. The mean value for the group was 63 mA with a standard deviation of 6 mA.

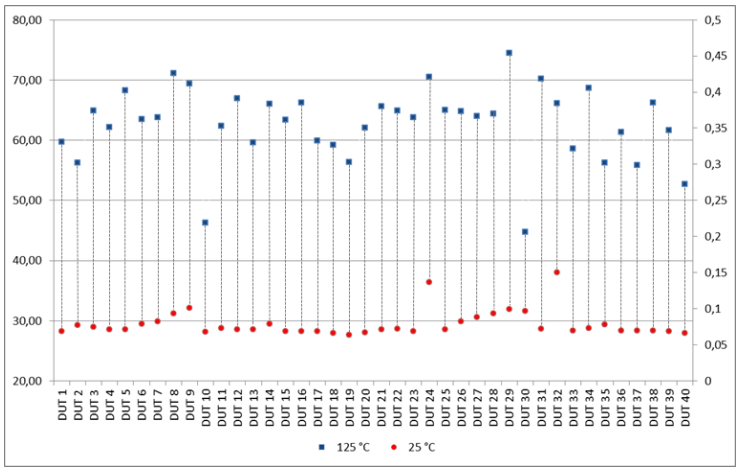


Figure 16 Ir at 25 °C and 125 °C for 40 diode DUTs. Vr = 45 V

In Figure 16, the reverse current is showed for each diode for both 25 °C and 125 °C. On the left, the reverse leakage current is indicated for 125 °C (blue dots) in mA, and on the right the reverse leakage current is given in mA for 25 °C (red dots).

The Pearson Correlation Coefficient between the reverse leakage current at high and low temperature is 0.299, p=0.061. This shows that a diode with high reverse leakage current at low temperature is more likely to have a high reverse leakage current at high temperature. This can be an indication to that the diodes temperature dependent performance is increasing parallel between the different

DUT. This is a good help if characterisations must be calculated from low to high temperatures.

6.2 Avalanche current tests

There were performed to avalanche current tests. First, a non-repetitive avalanche current test was performed. Secondly, the diodes resilience towards repetitive avalanche currents was tested.

6.2.1 Non- Repetitive Avalanche Current test

The datasheet for the investigated diode specifies an upper limit for non-repetitive avalanche energy per leg as 202 mJ from a 1 mH inductor at 25 °C. To verify the specifications in the datasheet, the test was started with the limits given in the datasheet, this corresponding to a current peak of 20 A.

There were no signs of degradation for the tested devices, so the current peak was increased in steps of 5 A until a weakness occurred, or to the limit of the power supply (45 A). After 10 DUTs had been tested with avalanche current of 45 A with the 1 mH inductor, and no signs of degradation were observed, the inductor size was increased and the current peak reset to 20 A. At 45 A, the energy stored in the 1 mH inductor is 1.01 J, more than five times the diodes rating. The process was repeated for inductors up to 4.5 mH without any failures. At 4.5 mH and 45 A the avalanche energy is more than 4.5 J, more than 20 times higher than the specifications. This lead to the conclusion that non-repetitive avalanche currents could not be the reason for failure in the power converter, and the test was stopped.

6.2.2 Repetitive avalanche current test

The test was performed on 51 DUTs until they failed into short circuit. The tested diodes had previously been operated in the converter, so there was great spread in their performance. The time from first avalanche until failure was measured and used to compare with the leakage current of the respective DUTs, to see if there could be a correlation. The reverse leakage current on the tested diodes ranged from 55 µA to 70 mA. And the time before failure (TBF) ranged from 35 s up to 207 s. A plot of each DUTs TBF vs I_r is shown in Figure 15. The plot shows that there might be a tendency to grouping in the didoes performance. By drawing a line along the TBF = 100 s and I_r = 1000 µA, four areas are separated.

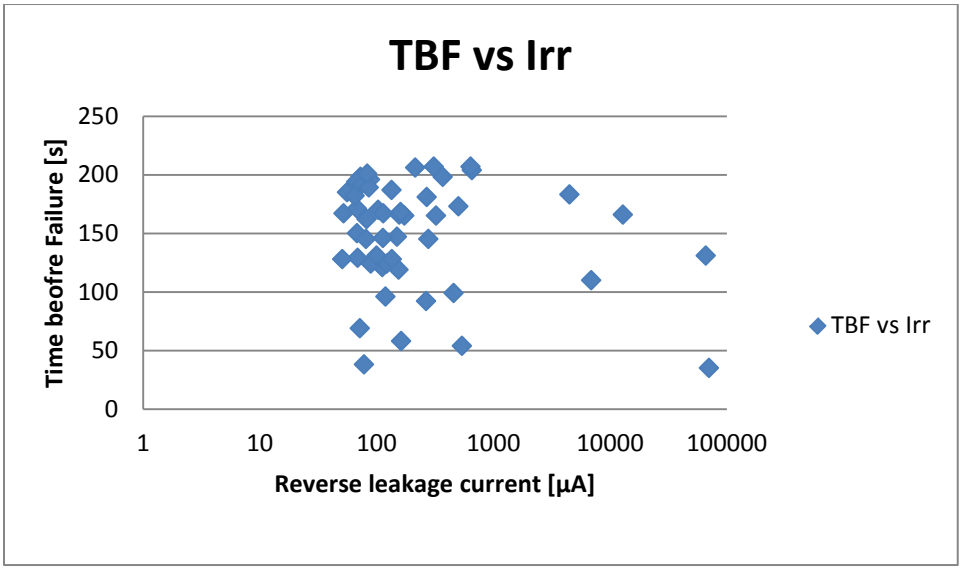


Figure 17 Time before failure vs Irr in the RAC test. The time is measured in seconds and the current is measured in µA

From Figure 17, the correlation between the diodes can be found. From the chart it appears to be three groups of diodes. Group 1 is the bulk group where most of the devices will be placed. They survived the test for more than 100 s and have I_r < 1000 µA. 76 % of the diodes belong in this category. These diodes must be considered the healthiest diodes with the least signs of degradation.

There were eight diodes which failed before 100 s. Out of these, 7 had a leakage current below 1000 µA, these can be labelled group 2. And one had I_r > 1000 µA, more exactly it was 70 mA. These diodes have shorter lifetime in the test than the others. This group consist of 16 % of the diodes. These diodes survived the shortest time in the test, but still their reverse current was no higher than what could have expected.

There are in total five diodes which have a reverse leakage current higher than 1000 µA. One of these is destroyed before 100 s. five diodes amount 10 % of the sample group. There are four diodes with I_r >1000 µA and TBF>100 s, they are placed in Group 3. These are diodes which show great degradation with regards to reverse leakage current, but still they survive a reasonable amount of time in the test.

This leaves one single diode left in group 4, one DUT is 2 %. The total division of groups can be seen in Table 1.

Table 1 Distribution of diodes in repetitive avalanche current test

		Ir	
		< 1000 µA	> 1000 µA
TBF	> 100 s	39	4
	< 100 s	7	1

The data basis is not big enough to say much about the correlation. But the fact that group 4 is so much smaller than both group 2 and 3 is an indication that there is no correlation between reverse leakage current and avalanche ruggedness. That group 1 is by far the biggest group is a healthy sign, indicating that the most of the diodes are not deteriorated in any degree relevant to this test. This shows that a low reverse leakage current can be a sign of a rugged diode.

The Pearson correlation coefficient for the data shows a negative correlation between TBF and I_r, this indicates coexistence between high TBF and low I_r. The coefficient was calculated to -0.303, p = 0.031, which is at a significance level below 5%. It is important to note that correlation is no proof of casual relations between the measurements.

6.3 Power cycling test

For the first setup, two diodes with remarkable different reverse current performances were tested. DUT 1 had a reverse leakage current of 50 µA at 25 °C with V_r = 45 V, while DUT 2's I_r was 50 mA. At 25 °C, both DUTs had a forward voltage of 0.348 V conducting a sensing current of 1 A. The diodes had already been mounted in a power converter, so it was expected that some deterioration already had occurred.

At the beginning of the test, DUT 1's forward voltage at high temperature is measured to 220 mV. For a 1 A sensing current this corresponds to T_j = 86.7 °C.

$T_{j,min}$ is estimated to 42.2 °C from a V_f =306 mV. The diode baseplate temperature is measured to cycle between 42 and 48 °C. This gives a ΔT_j = 44.5 °C. The difference in temperature between $T_{j,max}$ and $T_{case,max}$ can be used to estimate the thermal impedance of the device. The power dissipation in the diode is measured to 144 W. The temperature difference of 38.7 °C gives a $R_{th,j-c}$ = 0.27 K/W, which is slightly higher than the datasheet specifications.

DUT 2 forward voltage is measured to be slightly lower for T_j, V_f = 300 mV. This corresponds to a junction temperature of 45.3 °C. The high temperature is found to be 97.0 °C. The diode case undergoes the same temperature swing as for DUT 1. This gives ΔT_j = 52.3 °C and a thermal resistance from junction to case of 0.34 K/W.

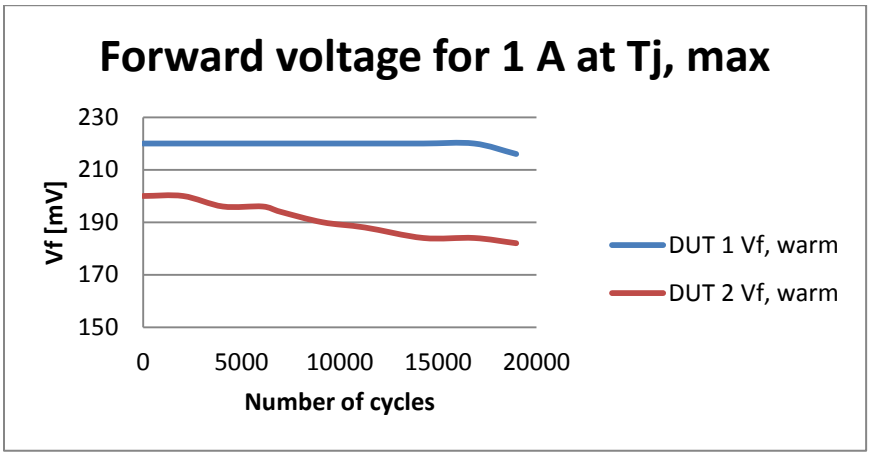


Figure 18 Vf,sens warm during power cycling

During the test, it was observed that the forward voltage from the sense current at the warmest point in the cycle was dropping for DUT 2, see Figure 18. This is an indication that the temperature is increasing in the junction. Both the load current and forward voltage in the diode during the load current period remained constant. This can therefore be an indication that the thermal resistance in the device is increasing. The voltage at low temperature remained stable during the entire test period.

The test was stopped after 19 000 cycles. It was found that the maximum temperature in the DUT 2 had increased from 97.0 to 106.3 °C. This corresponds to an increase in thermal resistance $R_{th,j-c}$ from 0.34 W/K to 0.40 W/K. This is an increase of 19 %. 40 W/K is 40 % higher than what the datasheet is stating as the maximum thermal resistance for the diode. The reverse leakage current, at Vr = 45

and 25 °C, had increased from 50 mA to 52 mA, an increase of 4 %. There was no observable increase in Vf.

The thermal resistance in DUT 1 had, after the test increased from 0.27 K/W to 0.28 K/W, an increase of 5 %. This level is still within the specifications of the datasheet. The reverse leakage current had increased from 50 µA to 120 µA. Vf remained constant.

Table 2 Characteristics of diodes before and after power cycle testing

Characteristics of DUT 1			
N° of cycles	Vf [V]	Ir [µA]	Rth,j-c [K/W]
0	0.348	50	0.27
18968	0.348	120	0.28

Characteristics of DUT 2			
N° of cycles	Vf [V]	Ir [mA]	Rth,j-c [K/W]
0	0.348	50	0.34
18968	0.348	52	0.40

In Table 2, the relevant characteristics for the diodes are given from before the test is started and after approximately 19 000 power cycles.

The increase in thermal resistance observed in DUT2 is a clear indication of degradation. As discussed in chapter 3.4, solder fatigue is a failure mechanism which can lead to increased thermal resistance. Increased thermal resistance leads to increased temperature in the junction during operation, and with increased temperature comes higher thermal stress. Solder fatigue is seldom observed as a final wear out mechanisms. But the enhanced stress from the poorer performance of the solder accelerates or triggers other failures.

The temperature outside the window of the lab where the test was performed was changing a lot from day to day. The lowest temperature measured outside was 18 °C, with rain, while on the warmest days the temperature could reach 30 °C, with strong sun directed at the window into lab, especially after noon. This change in outside temperature affected the ambient temperature in the lab. This change in temperature could have affected the results by moving the reference temperature.

(The temperature swing would have remained the same.) Since $T_{j,max}$ observed in DUT 2 was consistently increasing, and $T_{j,min}$ remained constant, an eventual effect was probably insignificant.

The big difference in reverse leakage current between the diodes compared to their performance in the test can be an indication to that the high reverse leakage current in DUT 2 in fact is an indication of degradation. No conclusion can be drawn on the basis of only the two tested devices, but the tendency is clear. However tests must be performed on more devices with different sets of parameters. Comparisons must be done with devices much more alike in performance and for a longer test period.

7 Conclusion

In this project the reliability of a diode was investigated. The emphasis was on the importance of the reverse leakage current for the tested diodes avalanche ruggedness and power cycle capability. The reverse leakage current test showed the spread of the I_r among a group of diodes. And it was found a correlation for $I_r(T)$ for the devices. The non- repetitive avalanche current test gave no failures, which lead to the conclusion that single avalanches not could be the reason for failure in the power converter the diode is placed in. In the repetitive avalanche current test 50 diodes was tested until failure. The test indicated that the reverse leakage current not can be used to as indicator for avalanche current induced failures. In the power cycle test only two devices have been tested. The two devices had big differences in reverse current. It was observed in the test that the DUT with high reverse leakage current was impaired much faster than the other.

A continuation of the project must include power cycle test of more diodes to get a bigger data base to more accurately describe the events. A bigger certainty in the results of the repetitive avalanche current behaviour could also be gotten by getting a bigger sample group.

8 References

1. Mohan N, Undeland T & Robbins W. Power Electronics. 3. Edition, USA: Wiley; 2003
2. Lutz J, Schlangenotto H, Scheuermann U, De Doncker R. Semiconductor Power Devices: Physics, Characteristics, Reliability. Berlin, Germany: Springer 2011
3. Stockmeier T. From Packaging to "Un"-Packaging Trends in Power Semiconductor Modules. IEEE, 2008; 20: 12-19. DOI: 10.1109/ISPSD.2008.4538886
4. Ciappa M, Selected Failure Mechanisms of Modern Power Modules. Microelectronics Reliability, 2002; 42: 653-667. DOI: 10.1016/S0026-2714(02)00042-2
5. Hurkx G. A. M, Koper N. A Physics- Based Model for the Avalanche Ruggedness of Power Diodes. IEEE, 1999; 11: 169-172. DOI: 10.1109/ISPSD.1999.764089
6. SAE/SVEI. Handbook for Robustness Validation of Automotive Electrical/Electronic Modules, ECS, 2008
7. Georges M, R2E-EPC [Internett]. Prevessin: CERN; 17/01/2012 [17/01/2012;23/07/2014]. Available from: http://te-epc-lpc.web.cern.ch/te-epc-lpc/context/radiations/r2e_cots.stm
8. Pawel I, Siemieniec R. A newsimulation Approach to Investigate Avalanche Behaviour, Elleithy K, red. Innovations and Advanced Techniques in Systems, Computing Sciences and Software Enginering. Netherlands: Springer; 2008. 9- 14.
9. Schulze H, Niedernostheide F, Pfirsch F, Baburske R, Limiting factors of the safe operating area for power devices. IEEE, 2013; 60(2): 551-562. DOI: 10.1109/TED.2012.2225148
10. Bouarroudj M, Khatir Z, Lefebvre S. Temperature Level Effects on the Thermo- Mechanical Behaviour of Solder Attach During Thermal Cycling of Power Electronic Modules. IEEE, 2008; 2435-2440. DOI: 10.1109/PESC.2008.4592306

Attachments

Attachment 1 Diode datasheet

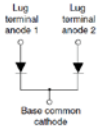
VISHAY

301CNQ...PbF Series

Vishay High Power Products

Schottky Rectifier, 300 A

TO-244



FEATURES

- 175 °C T_J operation
- Center tap module
- Low forward voltage drop
- High frequency operation
- Guard ring for enhanced ruggedness and long term reliability
- Lead (Pb)-free
- Designed and qualified for industrial level

RoHS COMPLIANT

DESCRIPTION

The 301CNQ... center tap Schottky rectifier module series has been optimized for low reverse leakage at high temperature. The proprietary barrier technology allows for reliable operation up to 175 °C junction temperature. Typical applications are in high current switching power supplies, plating power supplies, UPS systems, converters, freewheeling diodes, welding, and reverse battery protection.

PRODUCT SUMMARY	
$I_{F(AV)}$	300 A
V_R	40/45 V

MAJOR RATINGS AND CHARACTERISTICS			
SYMBOL	CHARACTERISTICS	VALUES	UNITS
$I_{F(AV)}$	Rectangular waveform	300	A
V_{RRM}	Range	40/45	V
I_{FSM}	t_p = 5 µs sine	16 000	A
V_F	150 Apk, T_J = 125 °C (per leg)	0.59	V
T_J	Range	- 55 to 175	°C

VOLTAGE RATINGS				
PARAMETER	SYMBOL	301CNQ040PbF	301CNQ045PbF	UNITS
Maximum DC reverse voltage	V_R	40	45	V
Maximum working peak reverse voltage	V_{RWM}			

ABSOLUTE MAXIMUM RATINGS						
PARAMETER		SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum average forward current See fig. 5	per leg	$I_{F(AV)}$	50 % duty cycle at T_C = 132 °C, rectangular waveform		150	A
	per device				300	
Maximum peak one cycle non-repetitive surge current per leg See fig. 7		I_{FSM}	5 µs sine or 3 µs rect. pulse	Following any rated load condition and with rated V_{RRM} applied	16 000	
			10 ms sine or 6 ms rect. pulse		3200	
Non-repetitive avalanche energy per leg		E_{AS}	T_J = 25 °C, I_{AS} = 21 A, L = 1 mH		202	mJ
Repetitive avalanche current per leg		I_{AR}	Current decaying linearly to zero in 1 µs Frequency limited by T_J maximum V_A = 1.5 x V_R typical		30	A

ELECTRICAL SPECIFICATIONS					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum forward voltage drop per leg See fig. 1	V_{FM} (1)	150 A	T_J = 25 °C	0.69	V
		300 A		0.90	
		150 A	T_J = 100 °C	0.59	
		300 A		0.76	
Maximum reverse leakage current per leg See fig. 2	I_{RM} (1)	T_J = 25 °C	V_R = Rated V_R	10	mA
		T_J = 125 °C		90	
Maximum junction capacitance per leg	C_T	V_R = 5 V_{DC} (test signal range 100 kHz to 1 MHz) 25 °C		5200	pF
Typical series inductance per leg	L_S	From top of terminal hole to mounting plane		7.0	nH
Maximum voltage rate of change	dV/dt	Rated V_R		10 000	V/µs

Note

(1) Pulse width < 300 µs, duty cycle < 2 %

THERMAL - MECHANICAL SPECIFICATIONS					
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS
Maximum junction and storage temperature range	T_J, T_{Stg}	- 55	-	175	°C
Thermal resistance, junction to case per leg	R_{thJC}	-	-	0.28	°C/W
Thermal resistance, junction to case per module		-	-	0.14	
Thermal resistance, case to heatsink	R_{thCS}	-	0.10	-	
Weight		-	68	-	g
		-	2.4	-	oz.
Mounting torque		35.4 (4)	-	53.1 (6)	lbf · in (N · m)
Mounting torque center hole		30 (3.4)	-	40 (4.6)	
Terminal torque		30 (3.4)	-	44.2 (5)	
Vertical pull		-	-	80	lbf · in
2" lever pull		-	-	35	

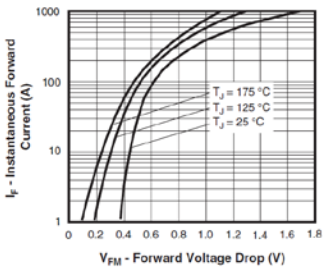


Fig. 1 - Maximum Forward Voltage Drop Characteristics (Per Leg)

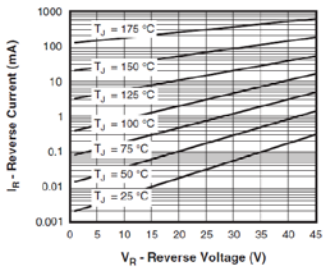


Fig. 2 - Typical Values of Reverse Current vs. Reverse Voltage (Per Leg)

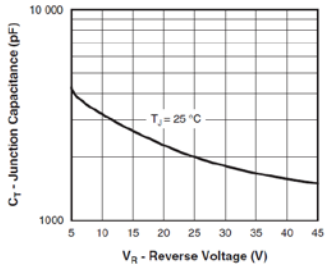


Fig. 3 - Typical Junction Capacitance vs. Reverse Voltage (Per Leg)

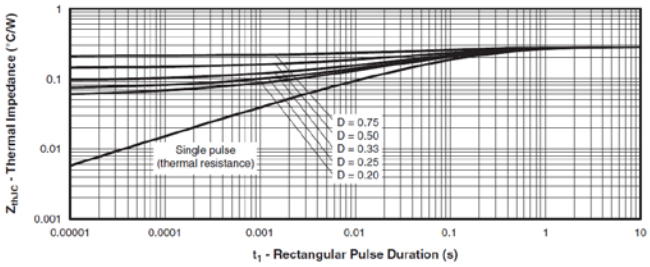


Fig. 4 - Maximum Thermal Impedance Z_{thJC} Characteristics (Per Leg)

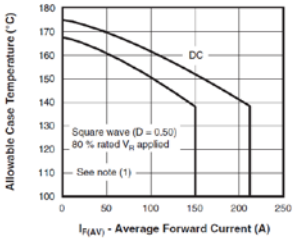


Fig. 5 - Maximum Allowable Case Temperature vs. Average Forward Current (Per Leg)

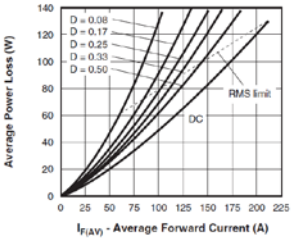


Fig. 6 - Forward Power Loss Characteristics (Per Leg)

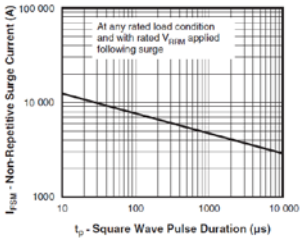


Fig. 7 - Maximum Non-Repetitive Surge Current (Per Leg)

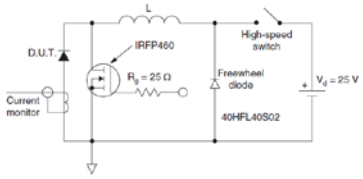


Fig. 8 - Unclamped Inductive Test Circuit

Attachment 2 Reverse current measurements

	45 V	
	125 °C	25 °C
DUT 1	59.71	0.069
DUT 2	56.27	0.077
DUT 3	64.90	0.075
DUT 4	62.16	0.071
DUT 5	68.24	0.071
DUT 6	63.43	0.079
DUT 7	63.73	0.082
DUT 8	71.08	0.093
DUT 9	69.41	0.101
DUT 10	46.27	0.068
DUT 11	62.35	0.073
DUT 12	66.96	0.071
DUT 13	59.61	0.071
DUT 14	65.98	0.079
DUT 15	63.33	0.069
DUT 16	66.18	0.069
DUT 17	59.90	0.069
DUT 18	59.22	0.066
DUT 19	56.37	0.064
DUT 20	62.06	0.067
DUT 21	65.59	0.071
DUT 22	64.90	0.072
DUT 23	63.73	0.069
DUT 24	70.49	0.137
DUT 25	65.00	0.071
DUT 26	64.80	0.082
DUT 27	64.02	0.088
DUT 28	64.41	0.093
DUT 29	74.51	0.099
DUT 30	44.71	0.097
DUT 31	70.20	0.072
DUT 32	66.08	0.150
DUT 33	58.63	0.070

DUT 34	68.63	0.073
DUT 35	56.27	0.078
DUT 36	61.37	0.070
DUT 37	55.88	0.070
DUT 38	66.18	0.070
DUT 39	61.67	0.069
DUT 40	52.65	0.066
mean	63	0.0791
standard deviation	6	0.018
min	45	0.064
max	75	0.150