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Multilevel Converters for Offshore Wind Systems

A Comparative Study

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Master Thesis of Science

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Multilevel Converters in Offshore Wind Systems
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For obtaining the degree of Master of Science in Electrical Engineering at Delft University of Technology and in Technology-Wind Energy at Norwegian University of Science and Technology.

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Of

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The undersigned hereby certify that they have read and recommend to the European Wind Energy Master - EWEM for acceptance a thesis entitled **"Multilevel Converters in Offshore Wind Systems"** by **Abel A. Taffese** in partial fulfillment of the requirements for the degree of **Master of Science**.

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Problem Statement

Offshore wind farms are getting more attention because of stronger and steadier wind compared to on-land farms. Economic benefits and growing opposition from environmental activists against onshore wind farms, are also the driving factors for offshore installations. Different farm layouts have been developed in light of cost effectiveness, power system stability, and contingency management. Among these layouts, the ones involving DC transmission are favored because of possibility of longer step-out and connection to weak points in the grid.

Accompanying these DC links, are high voltage power electronic converters at different points in the system. There are different converter topologies advertised by main players in the industry and academic researchers. The market of these converters is shifting towards Modular Multilevel Converters (MMC) because of their modular design, reliability and a number of attractive features. However, the development of such converters is at its early stage. Therefore, more investigation is required to understand their operation and quantify their merit in contrast to existing proven technology. Comparison of these topologies with respect to generated harmonics, power loss, ease of control, and cost, is main goal of this thesis.

The thesis will be approached in three phases: Phase I, preliminary research to identify three dominant topologies; Phase II, detailed comparison using simulation of the selected topologies to come up with the most promising candidate; Phase III, validate the theoretical work with experiment on the selected candidate topology. The thesis was proposed by Statiol and it involves both analytic and experimental work.

Assignment Given: Feb 2014, Trondheim
Supervisor: Prof. Tore M, Undeland

Summary

Offshore Wind systems have recently gained popularity. However, as the distance from shore increase, different challenges arise. The use of HVDC link to shore helps to overcome most of the challenges. Current Source converters have long been used as HVDC converters despite of their large footprint and reactive power consumption challenges. Recent development in the converter led to the use of Voltage Source Converters (VSC).

There are a number of VSC topologies proposed by the industry and academic researchers. The purpose of this thesis was to compare the dominant converter topologies and identify their merits. The work was done in three phases. Phase I was initial study and literature review where three dominant topologies were selected at the end. Two level VSC, Three level NPC, and Modular Multilevel Converter (M2C) were selected at the end of Phase I.

Phase II involved detailed modelling and simulation of the selected converter topologies. The simulation was mainly focused on harmonics and losses. The M2C was found to produce lower harmonics and losses under the same operating conditions and using the same switching device. The M2C also exhibits modular design which gives it scalability. This is critical in todays power system which changes very frequently. The M2C was selected for next phase analysis because of the above and a number of other reasons.

Phase III was the final part which included practical work on the selected topology. This task was undertaken on a small scale setup of M2C with 3 cells. The purpose of the setup was to verify theoretical results obtained from simulation. The results showed good correspondence with the ones obtained from simulation. The overall study pointed in the direction of M2C for future HVDC installations despite of the capacitor ripple and complex control challenges.

Acknowledgements

I would like to extend my heart felt gratitude to my Supervisors Prof. Tore M. Undeland and Prof. J.A. Ferreira for their invaluable comments and support. I would also like to thank everyone in the Electric Power Engineering service lab, especially Vladimir Klubicka, for their help on the experimental setup.

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Acronyms

AC	Alternating Current
DC	Direct Current
HVDC	High Voltage Direct Current
VSC	Voltage Source Converter
CSC	Current Source Converter
NPC	Neutral Point Clamped
M2C	Modular Multilevel Converter
EMI	Electromagnetic Interference
PI	Proportional-Integral
PLL	Phase Locked Loop
MO	Modulus Optimum
SO	Symmetric Optimum
THD	Total Harmonic Distortion
WTHD	Weighted Total Harmonic Distortion
IGBT	Insulated Gate Bipolar Transistor

Chapter 1

Introduction

Offshore wind farms are getting more attention because of stronger and steadier wind compared to on-land farms. Economic benefits [6] and growing opposition from environmental activists against onshore wind farms, are also the driving factors for offshore installations. Offshore power systems are typically characterized by challenges in power transmission, grid interface and local grid designs. Different wind farm layout were studied in [7]. Transmission challenges are mainly related to capacitance of AC cables used to connect to onshore system. The problem becomes worse as the distance from shore is increased. HVDC based solution are used to overcome this challenge through the use of DC cables. There are different ways in which the wind farm is laid out: Small AC, Large AC, Mixed AC/DC, Small DC, Large DC and Series DC [7].

Small AC layout does not require offshore station and is very suitable for small wind farms located close to shore. The Large AC has offshore connection point and substation making it a good candidate for large wind farms located at distances where reactive compensation for the cable is acceptable. Local AC grid with DC transmission makeup the Mixed AC/DC layout. AC power coming from each wind turbine is stepped up, collected and rectified at an offshore converter station. Onshore inverter then interfaces the farm to the power system. Small DC and Large DC are similar to the AC counterparts with the transformer station replaced by DC-DC converters and inverters. The Series DC, on the other hand, does not need any transformer or DC-DC converter to connect to HVDC transmission system.

Choice among these layouts is dependent on the specific project and there is no single best solution. But, the industry and researchers are focusing more on the ones with DC transmission because of possibility of longer step-out and connection to weak points in the grid. This fact made power electronic converters very important part of the the power system. Use of power electronics converters introduces other set of problems like harmonics, power losses, and Electromagnetic Interference (EMI).

The main focus of this thesis is to study different power converter used in such a system and compare their performance with respect to these generated harmonics, power loss, scalability, and fault handling capability. These performance measures will be discussed in detail in subsequent sections. The system used to compare the different converters is the Mixed AC/DC layout shown in Figure 1.1.

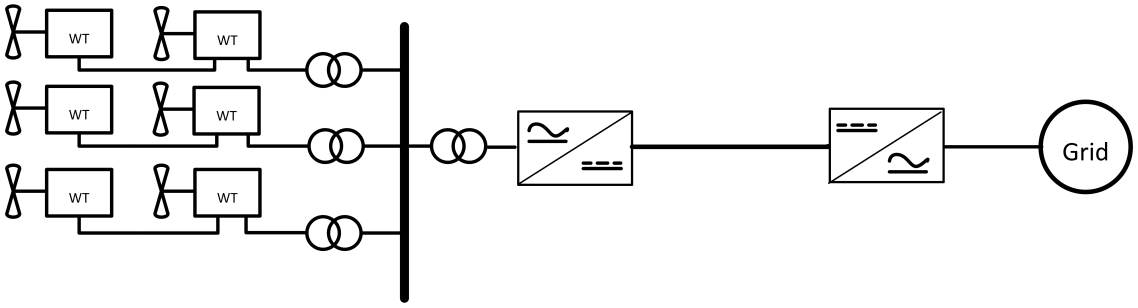


Figure 1.1: *Mixed AC/DC Wind farm layout*

1.1 Harmonics

Almost all components of a power system generate harmonics at different levels. Among these sources, power converters are one of the dominant ones. In wind-generator systems, these are generated whenever the voltage or current of the converter deviates from the sinusoidal fundamental component. These could be due to the converter topology, characteristic harmonics, or operating point and control scenario of the individual converter, non-characteristic harmonics.

One of the main effects of harmonics is the possibility of amplification of harmonic levels resulting from series and parallel resonances[8]. These resonances are due to the interaction of various inductive elements with capacitive elements like cables and reactive power compensators. Voltage harmonics produce series resonances while current harmonics produce parallel resonances.

A reduction in the efficiency of the generation, transmission and utilization of electric energy is also caused by harmonics. The losses in the system is increased in the presence of harmonics. This is because of two reasons: increased Ohmic losses due to increased RMS current, and losses due to Eddy currents and skin effect.

Harmonics also result in aging of insulation of electrical plant components with consequent shortening of their useful life. They could also cause malfunctioning of system or plant components. This is observed in system components like protection devices and measurement instruments. Interference with external system like communication is also unfavorable effect of harmonics.

If proper measures were not taken in the design of individual wind generator, connecting a wind park to a grid may result in amplification of harmonic content [9].

Having listed some of the effects of harmonics on the power system, it has been taken as one of the measures of performance.

1.2 Power Loss

Power losses are due to non-ideality of semiconductor devices and passive components in the converter [10]. There are two types of power losses: conduction loss and switching loss. Conduction losses are caused by nonzero resistance of the switches and passive components. Conduction loss depends on construction of the devices and the number of devices, in a given topology, connected in series.

Switching loss, on the other hand, is caused by overlap between current and voltage during switching. This type of loss is dependent on switching frequency of the switch and the number of switches in the converter. Some converters, like M2C, employ a technique that allows the switches to be switched at lower frequency while the converter is still running at higher frequency.

In optimizing for power loss, the number of components should be kept to the minimum. This reduces both switching and conduction losses. Switching frequency should also be kept minimum to reduce switching loss. These factors will be considered when comparing different converter topologies.

1.3 DC Fault Management

This aspect is specially important when considering Multi-terminal or Meshed HVDC networks. If a DC short circuit occurs, the fault should be isolated without affecting the AC side considerably [11]. This is desired in order for the other, non faulty, terminals to continue transmission. This issue arise because of the absence of simple and inexpensive protection equipment like the AC circuit breakers. This puts a demand on the Converter to have a certain way to isolate such faults by itself.

For point-to-point connection, however, fault handling is not a big issue because there is only one link and if there is a fault it will be disconnected. So the AC side circuit breaker in conjunction with current rise limiter inductance can be used to isolate DC side faults. But Multi-terminal DC grids are inevitable in the future, so having fault isolation capability is advantageous.

1.4 Converter Topologies

A number of topologies have been studied in literature for HVDC application. However, in actual installation, the number of topologies is quite low. The topologies fall into two categories; Voltage source and Current source.

Current Source Converters

Current source converter based HVDC stations have long been in the industry with the first installation going back to 1954 [12]. Each node actc as a current source where power flow direction is dictated by polarity of the voltage. These converters use Thyristors, which are line commutated [10], valves as switching devices. Being line commutated, the converters have a reactive power demand which is undesired [13],[14]. For this reason, these converters are slowly being replaced by other topologies.

Voltage Source Converters

Voltage source converter emerged for the first time in 1999[15] with the benefits of flexible reactive power support for the grid [5]. From VSCs, three topologies have been used in existing HVDC installations[5]. These are, the two level VSC, three level NPC, and Modular Multilevel Converter. These topologies were selected for detailed study in subsequent chapters.

1.5 Thesis Outline

The selected topologies are compared with detailed simulation model. Chapter 2 gives description of the case study model which is used for comparison. Chapters 3,4, and 5 give analysis and simulation results pertaining to each of the selected topologies. Chapter 6 summarizes the comparison. The experimental setup is described in Chapter 7. The thesis then finalizes with conclusion in Chapter 8.

Chapter 2

Case Study Model

2.1 Introduction

After the discussion presented in the previous chapter, three converters have been selected. To perform analysis on these converters, a common framework is required. For this purpose, the case study model was developed. This chapter describes the model in detail. A method to quantify the figures of merit is also presented. It should be noted that the objective of the comparison is not to identify best state-of-the-art converter topology. This would require access to techniques used by the different manufacturers which, in most cases, are confidential. Therefore the comparison will focus on advantages and challenges inherent to each topology. The same semiconductor device will be used in each of the topologies to have a reasonable comparison.

2.2 Shared System Components

The system used in the comparison is shown in Figure 2.1.

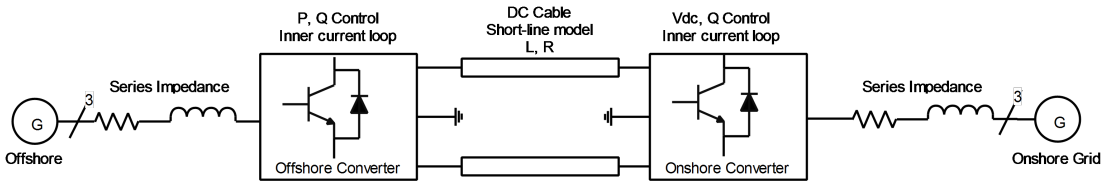


Figure 2.1: *Case Study Model block diagram*

The system has AC offshore grid that is collected and stepped up before being fed in to the offshore rectifier station. The power is transmitted via a 100 km DC cable to

the onshore inverter station that is directly connected to the main grid. The system base values are V = 100 kV and S = 100 MVA, f = 50 Hz. The DC bus voltage is chosen to be 160 kV to achieve 0.9 modulation index with harmonic injection. Some of the components that are common to all the topologies will be discussed in what follows.

2.2.1 Grid Models

The onshore grid is assumed to be strong since it is coupled without transformer and under the assumption that there are large generating stations nearby. A small impedance, equivalent to 4 GVA (40 p.u.), is included to account for transmission system impedance onshore. The offshore grid, on the other hand, is assumed to be coupled via a transformer at the collection point. Therefore, leakage impedance of the transformer, 15%, is included. In either case, the grid is modelled with a stiff voltage source in series with equivalent impedance. Frequency stiffness of the grid is not modelled because the scope of this study does not include frequency dynamics and control.

2.2.2 DC Cables

There are two HVDC cables which are 100 km long each. Since 100 km is considered medium length [16] π-model is used for the cable. The model is shown in Figure 2.2 and the parameters are given in Table 2.1.

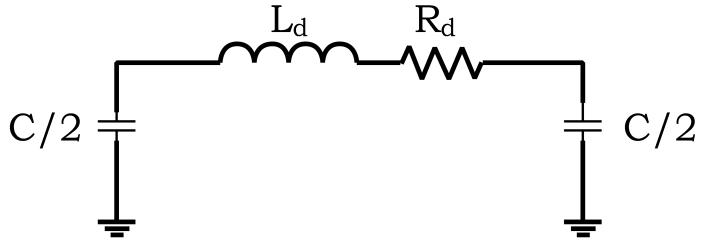


Figure 2.2: *π model for medium length line*

2.2.3 Converter Stations

The converters are voltage source type which can assume one of the three implementations: Two level, Three level NPC, and Modular Multilevel Converter. For simulation purpose, the converters are modelled as detailed switching converter. This approach takes longer to simulate compared to average models for the same

Parameter	Value
Resistance	10 $m\Omega/km$
Inductance	1 mH/km
Capacitance	50 nF/km
Length	100 km

Table 2.1: *DC cable parameters*

simulation period. But, it allows access to detailed waveforms that enable loss calculation and harmonic analysis. Implementation details vary between the topologies except for the top level system controller. Therefore, only system controller is described here.

2.2.4 Harmonic Filters

Harmonic filters are placed in the system to improve harmonic distortion introduced by the converter. There are a number of ways to provide harmonic filtering that can be grouped in to two: Active and Passive [1]. Active filters are more efficient but they are more expensive. Therefore, passive filters are considered because of the cost advantage. There are different filtering topologies as shown in the Figure 2.3 [1]. Single tuned filter is used to provide low impedance path at a specified frequency. To remove more than one harmonic components a number of filters are connected in parallel. A more economically efficient implementation is to use high pass circuit. Harmonic filters might not be needed in some of the converter because the waveforms are inherently clean.

2.2.5 System Modelling and Control

In this section, top level modelling and control of the system will be presented. From the controller's point of view, all the topologies similar; they all produce a commanded AC reference signal. The low level details are disregarded with the exception of delay introduced by the modulator. The system model is divided into three blocks as shown in Figure 2.4. Each of these block will be derived in subsequent sections.

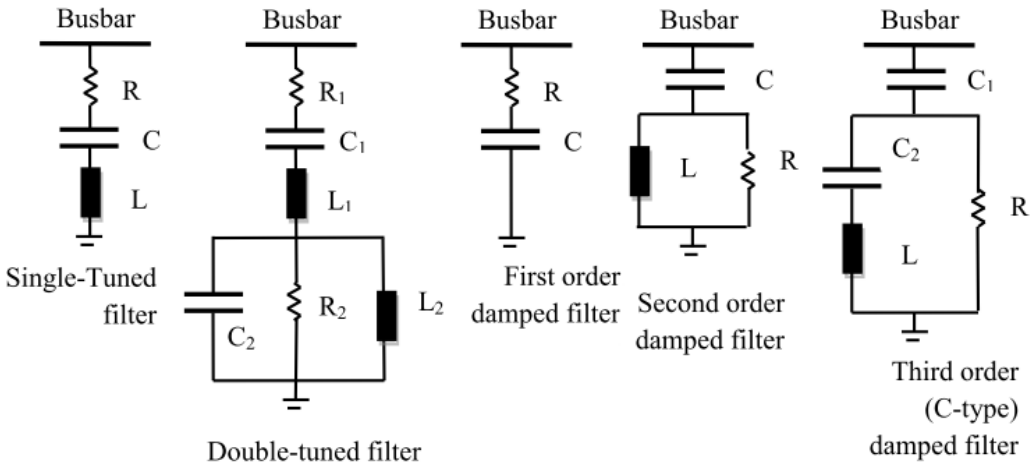


Figure 2.3: *Different harmonic filters*

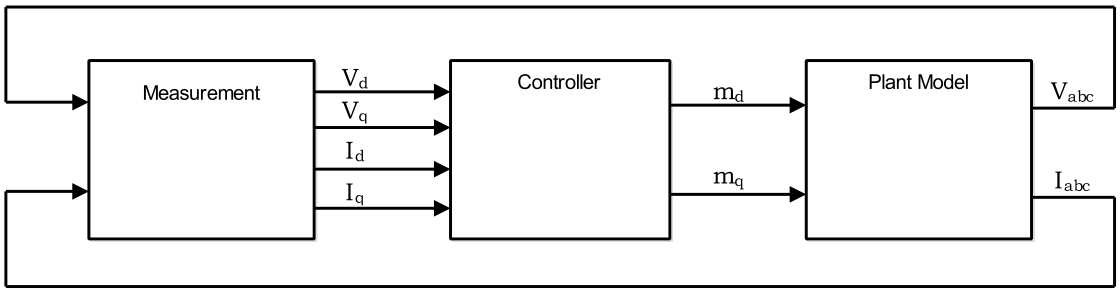


Figure 2.4: *High level system model components*

Measurement

This block represents all measurement, transformation, and filtering functions in the converter control. The basic building block is *dq0-transform* [17] which is used to transform quantities from *abc* reference frame to *dq*0 frame. A version of the transform, implemented in Simulink, is given in equation (2.1) and equation (2.2).

$$T = \frac{2}{3}\begin{bmatrix} \sin(\omega t) & \sin\left(\omega t - \frac{2\pi}{3}\right) & \sin\left(\omega t + \frac{2\pi}{3}\right) \\ \cos(\omega t) & \cos\left(\omega t - \frac{2\pi}{3}\right) & \cos\left(\omega t + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{2.1}$$

$$T^{-1} = \begin{bmatrix} \sin(\omega t) & \cos(\omega t) & 1 \\ \sin\left(\omega t - \frac{2\pi}{3}\right) & \cos\left(\omega t - \frac{2\pi}{3}\right) & 1 \\ \sin\left(\omega t + \frac{2\pi}{3}\right) & \cos\left(\omega t + \frac{2\pi}{3}\right) & 1 \end{bmatrix} \tag{2.2}$$

Since the controller is implemented in discrete time, anti-aliasing filters are required to limit frequency range of the input[18]. Detail of the filter design depends on the sampling and switching frequencies which are in turn dependent on the topology. For the transformation to work, it requires phase angle from the grid which is often obtained via the use of Phase Locked Loop (PLL) [19].

A simple PLL configuration is shown in Figure 2.5. A number of other PLL configurations are described in [20] with the aim of improving harmonic rejection and operation under unbalanced conditions. However, for the purpose of this thesis, the simple configuration is adequate and hence adopted. The transfer function PLL(s) represents the compensator which in this case is PI type. Dynamics of the PLL can be approximated by an integrator as long as the error is small. The closed loop transfer function of the PLL is given in equation (2.3).

$$G_{cl}(s) = \frac{k_p s + k_i}{s^2 + k_p s + k_i} \tag{2.3}$$

The equation has the form of a standard second order transfer function. It can be seen that the controller gains K_p and K_i can be independently used to set the

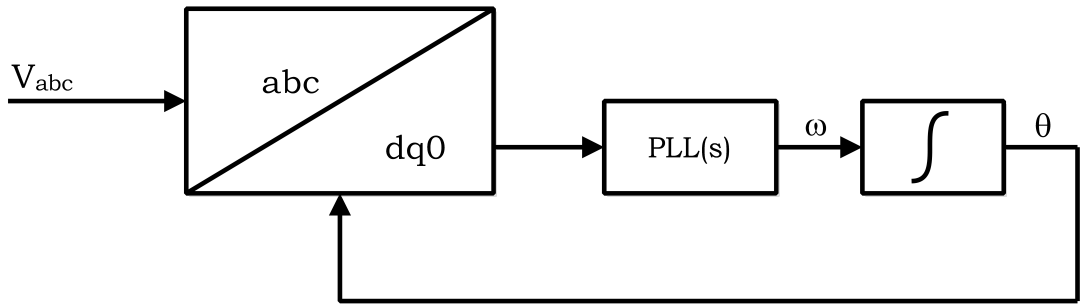


Figure 2.5: *PLL block diagram*

natural frequency and damping. This make the controller design straightforward. A damping of $\zeta = \frac{1}{\sqrt{2}}$ and $\omega_n 2\pi \times 10$ are selected. The controller can be designed to have faster dynamics. But, it is shown that if the controller is too fast, it could result in harmonic resonance and voltage instability [21]. The PLL response is drastically affected by deviation of the initial values of frequency from the nominal values. Therefore, output of the integrator should be saturated not to deviate from the nominal value by large quantity.

Plant Model

The plant model is developed with the objective of inner current control and outer P,Q and V_{dc} control. The plant model takes reference waveforms m_d and m_q as inputs and returns phase voltages and current as outputs. The grid and DC side are assumed to be ideal. This results in a simplified single phase equivalent circuit in *abc* frame shown in Figure 2.6. The filter model, shown by dotted lines, is not considered since it does not have significant effect at low frequencies. The filter is normally has corner frequency close to the switching frequency. This allows the aforementioned approximation to be valid as long as the model is used for analysis far below the switching frequency.

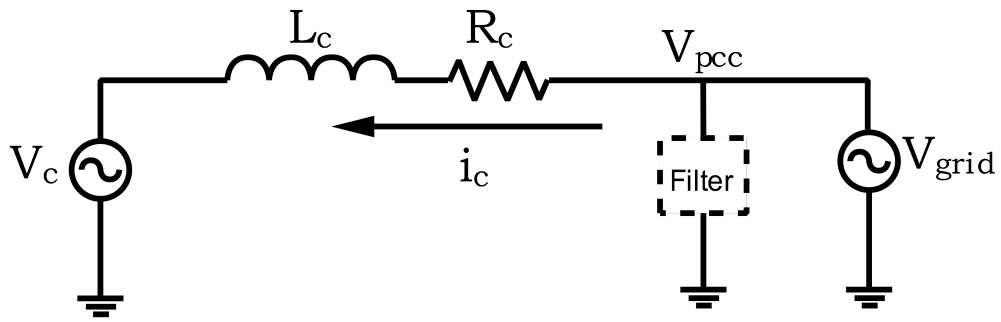


Figure 2.6: *Simplified AC side circuit*

From Figure 2.6, dynamics of the converter can be derived as shown in what follows. The derivation assumes a balanced system, constant DC bus, and good PLL design.

$$L_c \frac{di_c^{abc}}{dt} = v_{pcc}^{abc} - R_c \cdot i_c^{abc} - v_c^{abc} \tag{2.4}$$

$$v_c^{abc} = m^{abc} \cdot \frac{V_{dc}}{2} \tag{2.5}$$

By using dq0 Transform and combining equation (2.4) and equation (2.5), an equation in dq frame can be derived.

$$L_c \frac{d\left(T^{-1} i_c^{dq0}\right)}{dt} = T^{-1} v_{pcc}^{dq0} - R_c \cdot T^{-1} i_c^{dq0} - T^{-1} v_c^{dq0} \tag{2.6}$$

Left multiplying both sides with T gives the following.

$$L_c T \frac{d\left(T^{-1} i_c^{dq0}\right)}{dt} = v_{pcc}^{dq0} - R_c \cdot i_c^{dq0} - v_c^{dq0} \tag{2.7}$$

Expanding left hand side of equation (2.7),

$$L_c T \frac{d\left(T^{-1} i_c^{dq0}\right)}{dt} = L_c \left[T \frac{dT^{-1}}{dt} i_c^{dq0} + \frac{di_c^{dq0}}{dt} \right] \tag{2.8}$$

The first term on the right hand side of equation (2.8) represents mutual coupling between the dynamics along the different axes introduced by the transformation. For a balanced system ($0-axis$ component ignored), the final plant model becomes

$$L_c \frac{d}{dt} \begin{bmatrix} i_c^d \\ \\ i_c^q \end{bmatrix} = \begin{bmatrix} v_{pcc}^d \\ \\ v_{pcc}^q \end{bmatrix} - R_c \begin{bmatrix} i_c^d \\ \\ i_c^q \end{bmatrix} + \begin{bmatrix} 0 & \omega L_c \\ \\ -\omega L_c & 0 \end{bmatrix} \begin{bmatrix} i_c^d \\ \\ i_c^q \end{bmatrix} - \begin{bmatrix} m^d \\ \\ m^q \end{bmatrix} \cdot \frac{V_{dc}}{2} \tag{2.9}$$

The plant model derived so far does not consider effect of delay in converter due to modulation. To account for the delay a small time constant, τ_{PWM}, will be added to the last part of equation (2.9). The delay differs from converter to converter so it will not be quantified here. After Laplace transform is applied to equation (2.9), the complete plant block diagram is shown in Figure 2.7.

Active and Reactive power at the point of common coupling can be calculated from the quantities in $dq0-$frame as shown in equation (2.10) and equation (2.11).

$$p(t) = \frac{3}{2}\left(v_{pcc}^d i_c^d + v_{pcc}^q i_c^q\right) \tag{2.10}$$

$$q(t) = \frac{3}{2}\left(v_{pcc}^q i_c^d - v_{pcc}^d i_c^q\right) \tag{2.11}$$

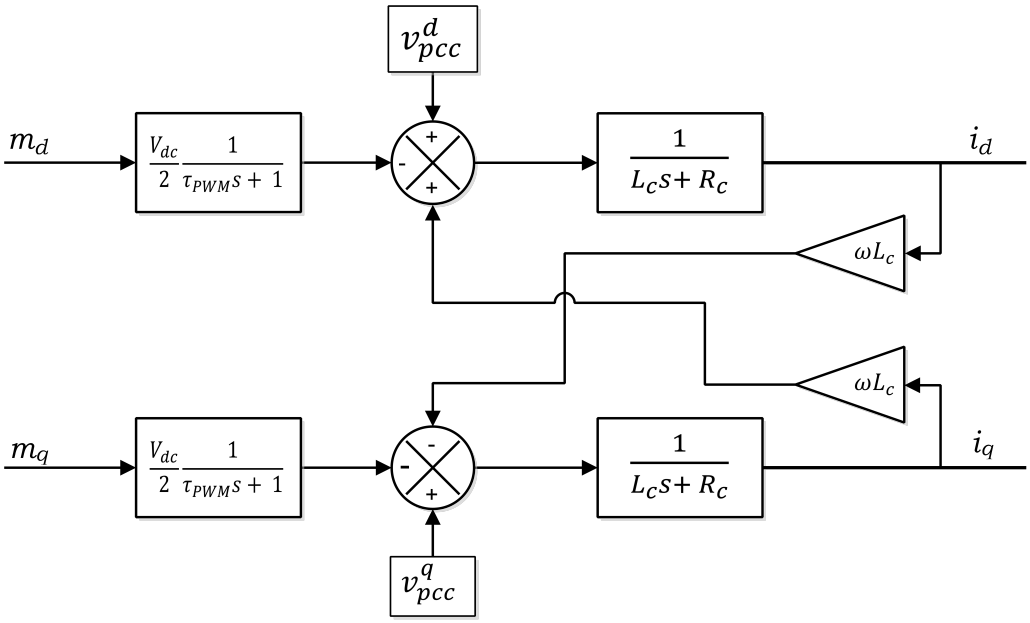


Figure 2.7: *Plant block diagram in dq-frame*

Model for DC voltage dynamic varies between the topologies; therefore, it is given under each topology in subsequent chapters.

Controller

There are different ways to control a voltage source converter system [18, 22]. Cascaded control topology with PI controllers is adopted for this thesis because of its simplicity and widely acceptable application. The PI controllers in this scheme can be tuned in a number of ways that can be broadly grouped into two: trail-and-error and model-based approaches. Trail and error approach might provide a simple solution when little is known about the system dynamics. However, the controller designed in such a way should be tested thoroughly to avoid unforeseen instabilities. An elegant alternative is to use the model available in the design process. One of the most popular model-based approaches, in control design for power converters, is the use of Modulus Optimum (MO) method for the inner loop and Symmetric Optimum (SO) for the outer loop with slow pole [22]. These tuning criteria are presented in the following paragraphs.

Modulus Optimum: In this method, the plant is assumed to have one dominant time constant and a number of other fast poles that can be grouped together [REF] as shown in equation (2.12).

$$G_p(s) = \frac{K}{(sT_a + 1)\,(sT_{eq} + 1)} \tag{2.12}$$

where T_a is the dominant time constant, K is the plant gain, and T_{eq} is equivalent time constant other delays, like anti-aliasing filters, in the plant. According to MO criterion, the dominant pole should be canceled by zero of the PI controller which results in the following relations.

$$\frac{k_p}{k_i} = T_a \tag{2.13}$$

$$G_{cl}(s) = \frac{K \cdot k_i}{T_{eq}s^2 + s + K \cdot k_i} \tag{2.14}$$

where $kp + \frac{k_i}{s}$ is the assumed controller structure and $G_{cl}(s)$ is the closed loop transfer function. The second step in MO is to choose the value of k_i so that the closed loop system has a damping of $\frac{1}{\sqrt{2}}$. Referring to equation (2.14), the previous statement implies that k_i is given by equation (2.15). The closed loop system can be approximated by a first order system with time constant $2 \cdot T_{eq}$.

$$k_i = \frac{1}{2 \cdot K \cdot T_{eq}} \tag{2.15}$$

Symmetric Optimum: This method is used whenever pole cancellation is not feasible due to the presence of a pole close to the origin. Cancellation of such a pole could ,in best case, deteriorate disturbance rejection performance of the closed loop system and in worst case it could destabilize the system. The plant model considered for SO design is shown in equation (2.16).

$$G_p(s) = \frac{K}{sT_a\left(sT_{eq} + 1\right)} \tag{2.16}$$

where T_a is time constant of the slow pole. The tuning rule in SO is to optimize for maximum phase margin [22]. Zero of the controller forms a lead-lag network with pole of the plant at $-\frac{1}{T_{eq}}$. The controller zero is then placed in order to attain maximum phase boost at the desired crossover frequency ω_d which is shown in equation (2.17).

$$\omega_d = \frac{1}{\sqrt{T_{eq}T_c}} = \frac{1}{a^2 T_{eq}} \tag{2.17}$$

where $T_c = \frac{k_p}{k_i}$, a is a design parameter recommended to be between 2 and 4 [22]. The equation derived in this section will be utilized for tuning controllers in subsequent sections.

2.3 Quantifying Figures of Merit

Some of the performance metrics are purely qualitative in the context of this thesis: reliability and complexity. Losses and Harmonic content, on the other hand, can be quantified. A method used to calculate these quantities will be given in this section.

2.3.1 Harmonic Content

Comparison of harmonic performance indicators is discussed in [23]. Total Harmonic Distortion (THD) and Weighted Total Harmonic Distortion (WTHD) are used in this thesis. THD is the ratio of RMS value of unwanted components, in the voltage or current waveform, to the desired fundamental component as shown in equation (2.18).

$$THD = \sqrt{\left(\frac{V_{rms}}{V_{1,rms}}\right)^2 - 1} \tag{2.18}$$

where V_{rms} is the total RMS voltage, $V_{1,rms}$ is RMS value of the fundamental component. THD is not a good measure of harmonic performance because it only portrays harmonic content not really displaying its significance. WTHD is better because it gives more weight to harmonic components that have the most severe effect; namely, low frequency harmonics. With WTHD it is clear and easy to compare to systems.

$$WTHD = \frac{\sqrt{\sum_{n=2}^{\infty}\left(\frac{V_n}{n}\right)^2}}{V_1} \tag{2.19}$$

where V_n is the n^{th} harmonic voltage, V_1 is the fundamental component. Both THD and WTHD will be used to compare the topologies.

2.3.2 Converter Losses

In this section, a method to calculate losses in converter is presented.

General equations

The losses in a semiconductor are grouped as conduction and switching losses. Conduction losses are caused by parasitic resistance of the device and overlap between voltage and current after the switching process has completed. Switching losses, on the other hand, are caused by overlap of voltage and current during the switching

process. These losses are commonly parameterized with the device on-state voltage and switching energies. The following description will adhere to these conventions.

On state voltages and switching energies of the device are specified as functions of the device current and junction temperature. Dependence on junction temperature will be differed to latter sections. Hence, device on state voltages are given approximately by equation (2.20).

$$v_{on}(i_{dev}) = V_0 + i_{dev} \cdot R_0 \tag{2.20}$$

where v_{on} is the on-state voltage, i_{dev} is the device current, V_0 and R_0 are parameters to be determined by curve fitting. The switching energies are denoted by E_{on}, E_{off}, and E_{rec}. By using these parameters the average switching and conduction losses are given by equation (2.21) and equation (2.22).

$$Pcon, av = \frac{1}{t - t_0} \int_{t_0}^{t} v_{on}(i_{dev}) \cdot i_{dev} \cdot dt \tag{2.21}$$

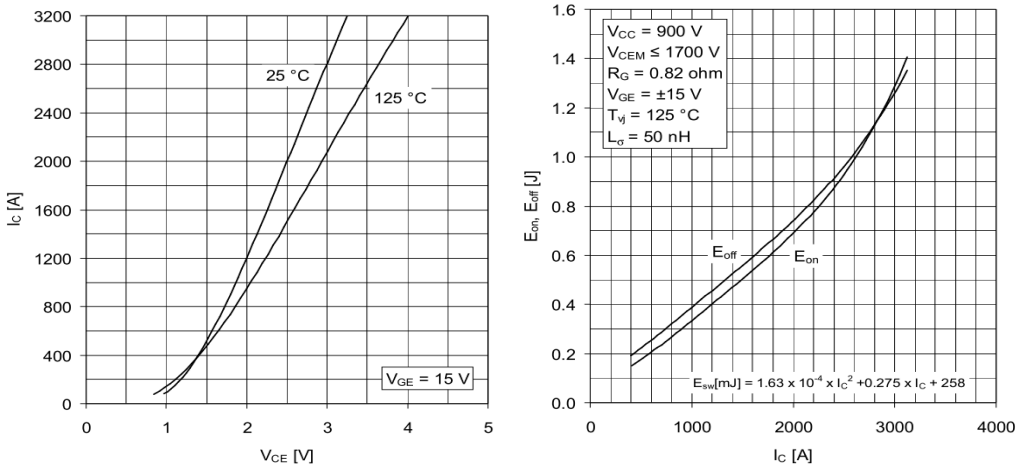
$$Psw, av = \frac{E_x(i_{dev}, v_{on})}{t - t_0} \tag{2.22}$$

where x denotes on, off, and rec.

Datasheet Parameters

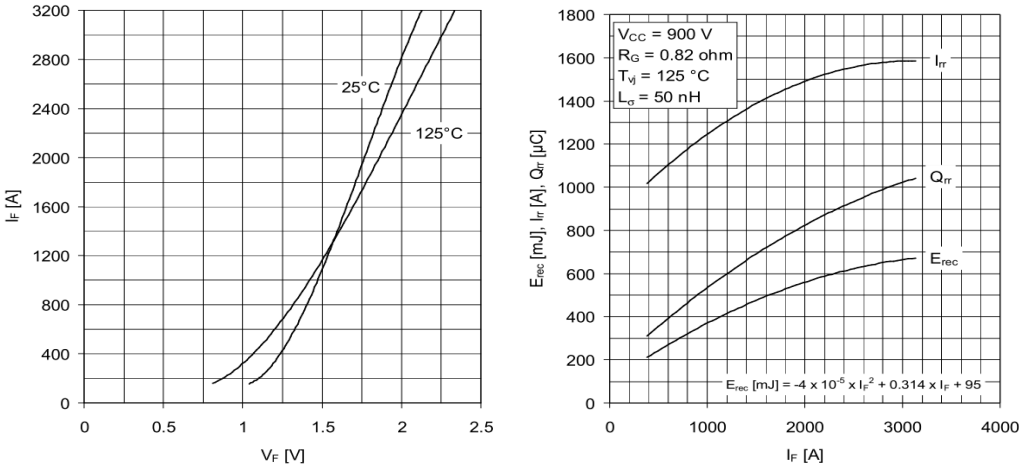
In this section, datasheet parameters of the selected device (5SNE0800M170100) will be presented. First, IGBT parameters will be presented. Common notation for the device current and on-state voltage are I_c and V_{ce} respectively. Figure 2.8 shows the relevant parameters. It can be seen that the on-state voltage depends only on the device current which makes it possible to implement it using 1-dimensional lookup. The switching energies, however, also depend on the device voltage, V_{cc} besides the devices current. So, it will be implemented using a 2-dimensional lookup table.

In the same manner, the diode characteristics, on-state voltage and switching energies, can also be found from the datasheet. These parameters are often denoted by V_F and E_{rec} respectively. These parameters are shown in Figure 2.9. One peculiar feature of the diode characteristics is that it's turn on and off losses are negligible; but, a phenomena called reverse recovery results what is known are reverse recovery losses denoted by E_{rec}. This phenomena is related to the finite amount of time it takes to remove the reverse recovery charge stored in the diode. The data points from these graphs will be fed into 1- and 2-dimensional lookup tables similar to the ones described for the IGBT.



(a) *On-state voltage vs. i_c* ***(b)*** *Switching energies vs. i_c*

Figure 2.8: *IGBT Datashet parameters*



(a) *On-state voltage vs. i_f* ***(b)*** *Switching energies vs. i_f*

Figure 2.9: *Diode Datashet parameters*

Junction Temperature Feedback

The parameters, descried so far, are all dependent on the junction temperature. But, the junction temperature is also dependent on the power losses forming a loop. This is a challenge, specifically, for hand calculation and analytic results. One approach to overcome this challenge is to assume a constant junction temperature which might be acceptable in some cases. The second, and more attractive, approach is to incorporate thermal model of the system and dynamically calculate junction temperature and feed it back to the loss calculation.

Thermal model of the device is described in the application note [24] where Cauer model was proposed for interconnected systems. The equivalent Cauer model is shown in Figure 2.10.

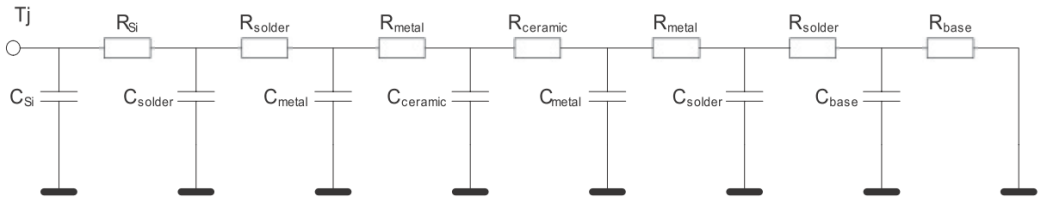


Figure 2.10: *Cauer equivalent of the thermal network*

Since the model also includes heatsink properties, the only input required is the ambient temperature. Each of the lookup tables will have one more dimension to account for junction temperature.

2.3.3 Implementation of the calculation

The loss calculation implementation in Simulink® is described in this section. The material in this section derived from [25]. For conduction loss, the values from the graph are fed into a 2-D lookup table where the on state voltage can be read for each current. Multiplication of the on state voltage and current gives the conduction loss. The Switching losses uses the voltages and currents just before switching, pre-switching, and just after switching, post-switching. Turn on and Turn off losses are described in the following paragraphs.

Turn-on loss: Pre-switching value of the voltage across the device, post-switching value of the device current, and the junction temperature are used to read the energy losses from a 3-D lookup table. This energy is converted into a power pulse which is injected into the thermal network. The power pulses are then filtered to get the average turn-on power loss.

Turn-off loss: This is similar to Turn-on except for the fact that pre-switching value of the device current and post-switching value of the voltage across the device are used

Reverse recovery loss of the diode is also calculated in a similar fashion.

Chapter 3

Two Level VSC

3.1 Introduction

Two level VSC is the simplest and most studied VSC topology used in HVDC installations. This converter is the first VSC to be used in HVDC installation [26]. The topology is shown in Figure 3.1.

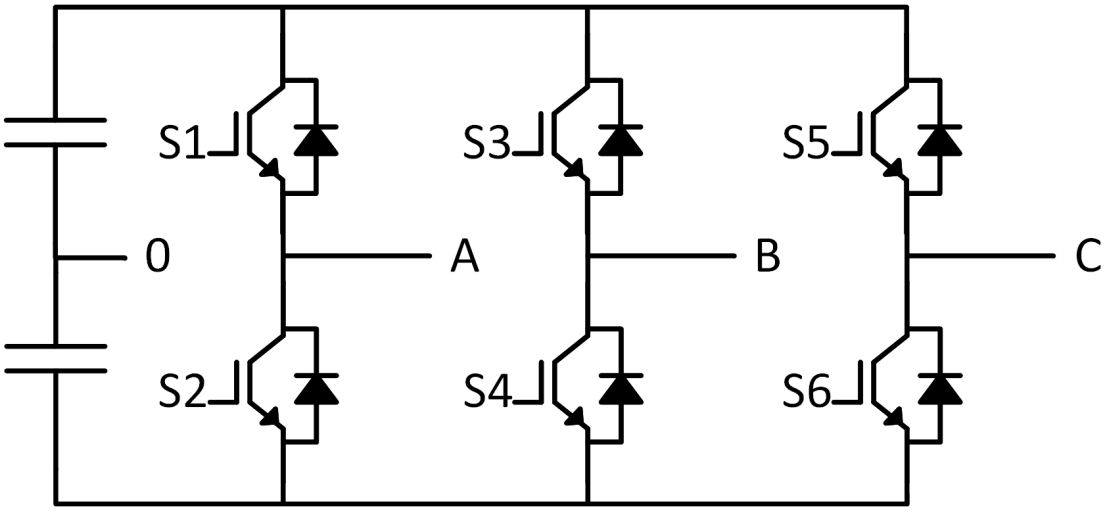


Figure 3.1: *Two level VSC circuit*

3.2 Operation Principle

Two level VSC has a half bridge as its building block as shown in Figure 3.2.

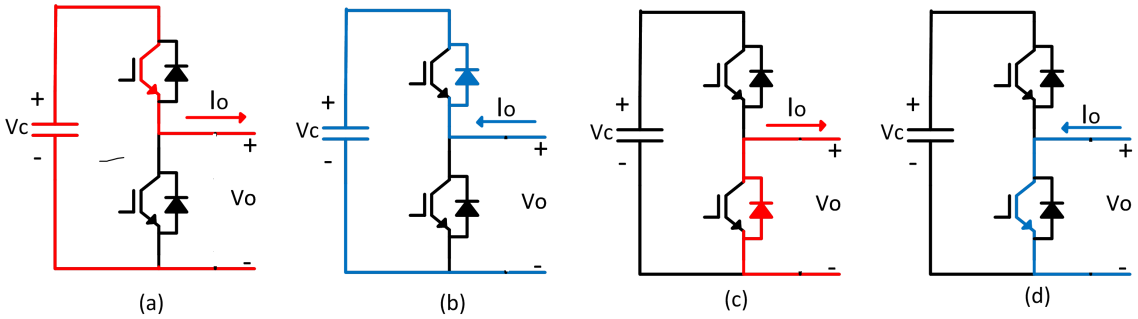


Figure 3.2: *Half bride converter and its operation*

S_1	S_2	i_{out}	Conducting Device	V_{out}
0	0	> 0	D_2	0
0	1	> 0	D_2	0
1	0	> 0	S_1	V_{dc}
0	0	< 0	D_1	V_{dc}
0	1	< 0	S_2	0
1	0	< 0	D_1	V_{dc}
1	1	< 0	S_1, S_2 (Short circuit)	0

Table 3.1: *Operating states of Half bridge converter*

State of the output voltage, V_{out}, is controlled by inputs S_1 and S_2 (Figure 3.2. The output is either 0 or V_{dc}. To get AC voltage variation, swing between positive and negative, mid-point of the DC side is taken as reference. This is only required for single phase case. For three phase, there will be three parallel connected half bridges, Figure 3.1, which allows star point of the load connection to be taken as reference.

Conduction state of each device is also dependent on direction of the AC side current, Table 3.1. The last entry in Table 3.1 should be avoided, by using complementary control, as it might damage the converter. Different ways to produce a desired AC waveform using this converter is discussed in next section.

3.3 Modulation

Modulation refers to techniques used to control switches in a converter to produce a desired waveform on average. Modulation can also be used to achieve secondary goals: reducing loss and harmonic content. The simplest form of modulation is carrier comparison (Figure 3.3). The operation is very simple; the pulse sent to the top switch is 1 whenever the reference is above the triangle waveform. Harmonic analysis indicate that the output voltage has the correct fundamental component and harmonics centered at multiples of the switching frequency [10]. The frequency modulation ratio, m_f, is 10 in the figure.

Space Vector Modulation (SVM) is another scheme widely used in VSC which has the advantage of better DC voltage utilization. A similar advantage can be gained by injecting a common mode voltage on top of the phase references (Figure 3.4). There are different ways to generate the common mode voltage depending on the goal. In this analysis, the goal is to extend the DC voltage utilization and hence a triangular common mode voltage, Figure 3.4, as calculated in equation (3.1) is used. Figure 3.4 shows that injection of the common mode results in reduction in the reference waveforms indicating better DC bus utilization.

$$v_{com} = \frac{max\left(v_a, v_b, v_c\right) + min\left(v_a, v_b, v_c\right)}{2} \tag{3.1}$$

$$v^{abc}_{ref,new} = v^{abc}_{ref} - v_{com} \tag{3.2}$$

3.4 Analysis

The converter's interaction with the AC and DC sides, in steady state, will be analyzed in this section. Main focus is on DC side current and ripple.

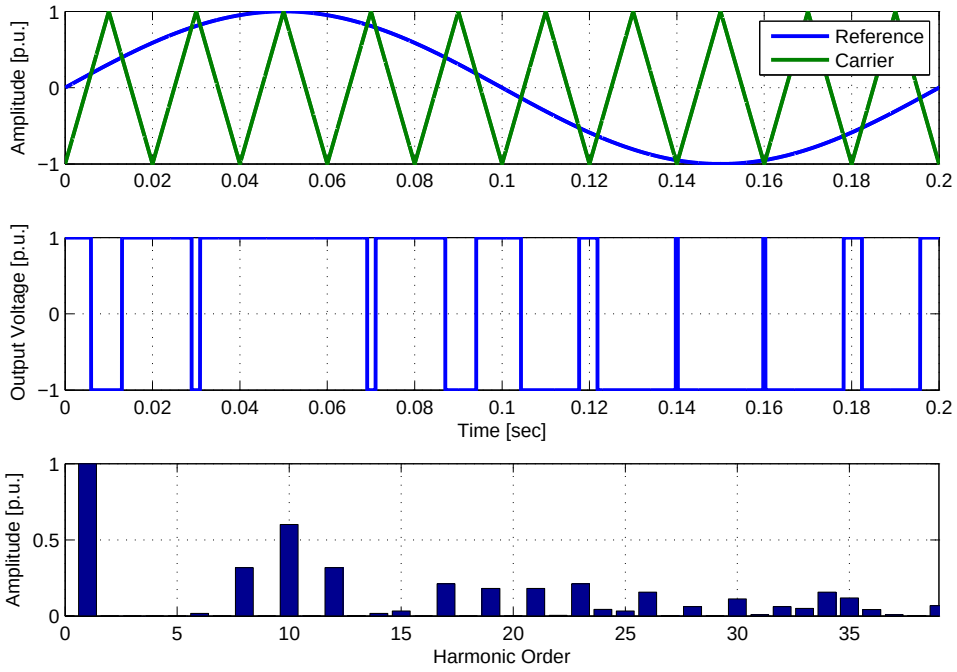


Figure 3.3: *Triangle comparison modulation waveforms*

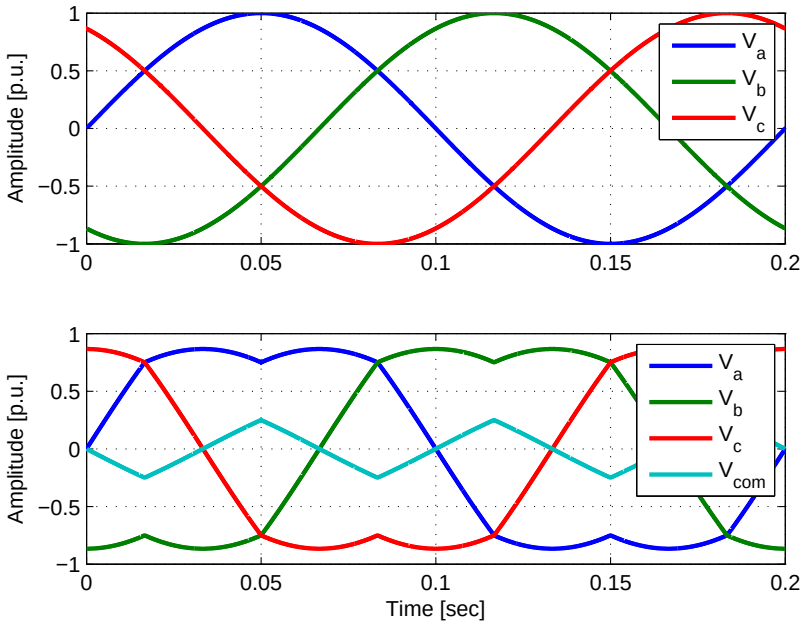


Figure 3.4: *Common mode injection on the reference*

$$\begin{aligned} v_a &= V\sin(\omega t) \\ v_b &= V\sin\left(\omega t - \frac{2\pi}{3}\right) \\ v_c &= V\sin\left(\omega t - \frac{4\pi}{3}\right) \end{aligned} \tag{3.3}$$

where V is peak of the AC voltage. The AC side current is assumed to be ripple free and having peak I and a phase lag, ϕ, with respect to the voltage.

$$\begin{aligned} i_a &= I\sin(\omega t - \phi) \\ i_b &= V\sin\left(\omega t - \frac{2\pi}{3} - \phi\right) \\ i_c &= V\sin\left(\omega t - \frac{4\pi}{3} - \phi\right) \end{aligned} \tag{3.4}$$

3.4.1 DC Side Voltage Ripple

From equation (3.3) and equation (3.4), average values of apparent, active, and reactive power are give in equation (3.5).

$$S = \frac{3}{2}VI \quad P = \frac{3}{2}VI\cos(\phi) \quad Q = \frac{3}{2}VI\sin(\phi) \tag{3.5}$$

Average value of the DC side current in thus:

$$i_{dc,av} = \frac{2}{3}\frac{VI}{V_{dc}} \tag{3.6}$$

However, the DC side current also contains addition harmonic content due to switching action. The actual current is difficult to write analytically in closed form, therefore a time domain simulated waveform is used for the analysis. Equations (3.7) to (3.9) are used in the calculation of the DC current shown in Figure 3.5.

$$S_x = \begin{pmatrix} 1, & for\ S_1 = on \\ -1, & for\ S_1 = off \end{pmatrix} \quad x \in \{a, b, c\} \tag{3.7}$$

$$i_{dc,x} = S_x i_x \tag{3.8}$$

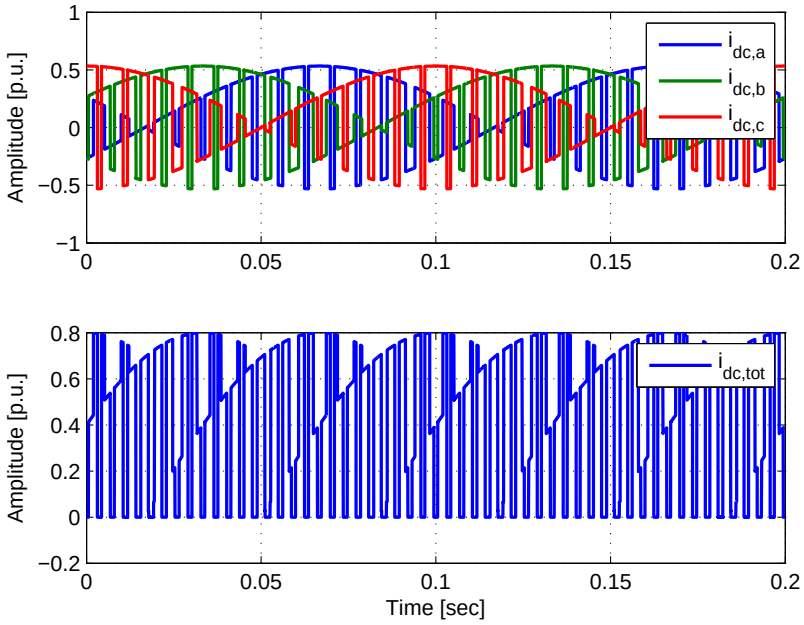


Figure 3.5: *DC side current,* $m_f = 27$, $V = 0.9p.u.$, $I = 0.8p.u.$, $\phi = \frac{\pi}{6}$

$$i_{dc,tot} = \sum_x S_x i_x \tag{3.9}$$

Three important points should be noted from Figure 3.5.

- The DC side exhibits current switching at high frequency. This could introduce over voltages on every switching if the DC side is inductive.
- Average value of the DC side current is constant (DC).
- Switching component of the current is responsible to ripple voltage on the DC link capacitance. Size of the capacitor is inversely proportional to the capacitance value, Figure 3.8.

3.4.2 AC Side Current Ripple

To analyze the AC side current ripple, the grid is assumed to be a harmonic free voltages source in series with inductive impedance. With this assumption, the AC side circuit can be simplified to the equivalent circuit shown in Figure 3.7. V_{ripple} is the difference between generated output voltage and the fundamental component referred to neutral point. The neutral point voltage is calculated by equation (3.10).

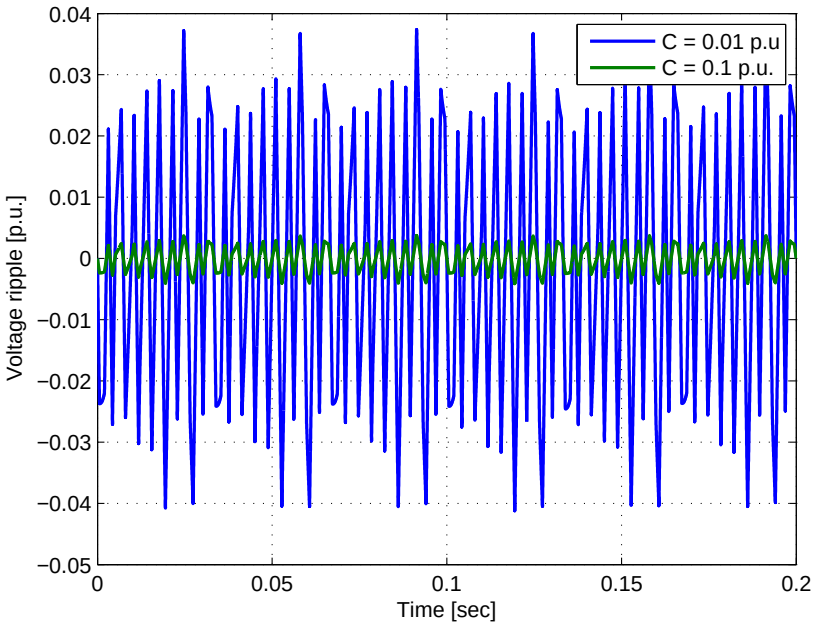


Figure 3.6: *Capacitor ripple for for two choice of capacitance*

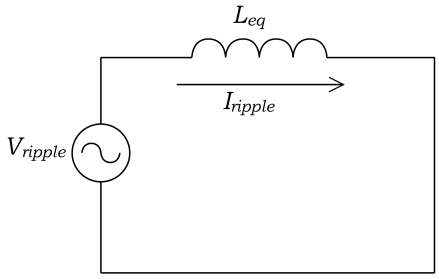


Figure 3.7: *Equivalent circuit for AC side ripple*

$$v_n = \frac{1}{3}\left(v_a + v_b + v_c\right) \tag{3.10}$$

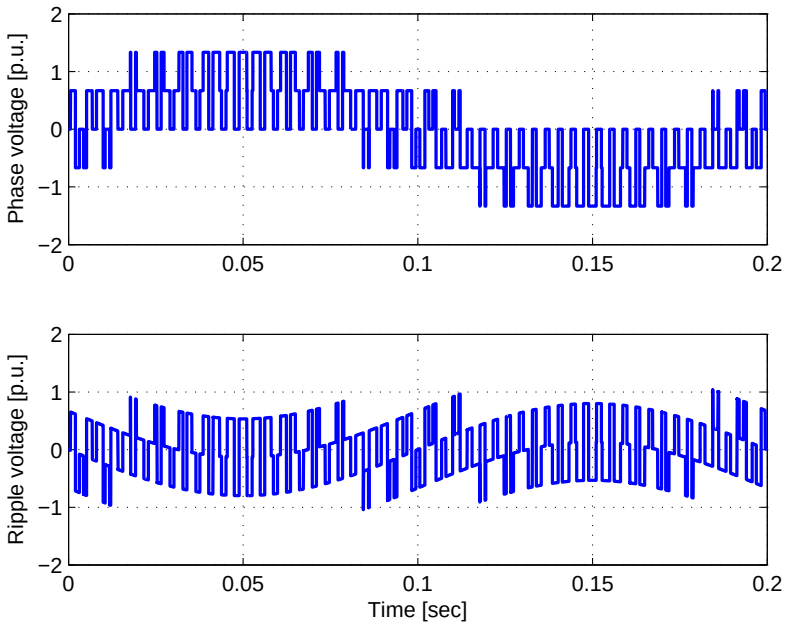


Figure 3.8: *Output voltage and ripple component*

Phase to neutral voltage and the corresponding ripple component are shown in Figure 3.8.This ripple voltage is applied as a source in Figure 3.9 to produce AC ripple current as governed by equation (3.11).

$$i_{ripple} = \frac{1}{L_{eq}} \int_0^t v_{ripple}(\tau) d\tau \tag{3.11}$$

The ripple has the following characteristics:

- The ripple is independent of amplitude of current. This implies that harmonic distortion is high when the current amplitude is low.
- The ripple has peak around zero crossing of the phase voltage. As modulation index, the number of peaks in the ripple increases.
- Peak of the ripple decrease with increasing value of L_{eq}
- It is mainly due to switching and has harmonic components centered around the switching frequency.

Putting these facts together, sizing of components is presented in next section.

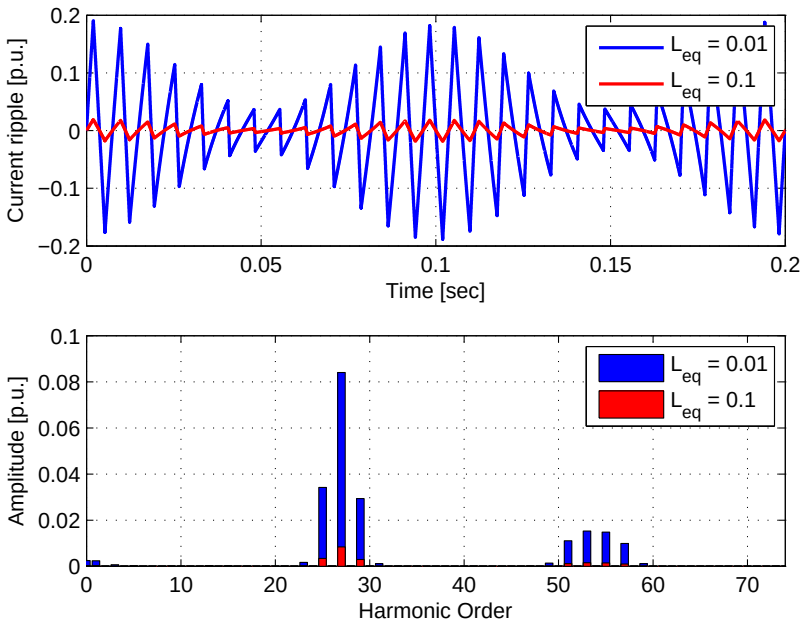


Figure 3.9: *Output current ripple and its spectrum,* $m_f = 27$

3.5 Dimensioning

This section deals with selection of components and their ratings. The frequency modulation ratio, m_f, is chosen to be 27 in order to achieve a good compromise between losses and filtering requirements. in [10], it is recommended that m_f be multiple of three to eliminate certain harmonics.

3.5.1 DC Capacitor

The purpose of DC link capacitor is limit the ripple in DC bus. Its value is selected to meet two opposing constraints. The first requirement is that of low ripple which demand capacitance to be as large as possible (Figure 3.8). The second one is related to transient response of the converter; if the capacitance is to high, the converter response will be slow. The response time is quantified as time constant [27], equation (3.12).

$$\tau = \frac{1}{2}\frac{CV_{dc}^2}{S_N} \tag{3.12}$$

where S_N is nominal apparent power, V_{dc} is the DC bus voltage, and C is the capacitance value. The value of capacitance as a function of the ripple is given by

equation (3.13) where inverse relation between ripple magnitude and capacitance is depicted.

$$C = \frac{S_N}{2V_{dc}\omega} \cdot \frac{1}{\Delta v_{dc}} \tag{3.13}$$

where ω is fundamental frequency and Δv_{dc} is ripple magnitude. With the system parameters, $S_N = 100MVA$, $V_{dc} = 160kV$, the capacitance was chosen to be $C \approx 80\mu F$. This choice results on time constant of $\tau = 10ms$.

3.5.2 Series Reactor

The purpose of this reactor is three fold: filtering harmonics from the AC current, limiting fault current, and providing means for power transfer. The first two objective require high value of the reactance. The third objective, on the other hand, requires low reactance since average active power is inversely proportional to the reactance. The value is chosen to be 0.15 p.u. [27].

3.5.3 Switching Devices

Although the design is centered around a chosen device, this section presents rating of the component to verify that they are within operating limits. Peak value of the current and voltage on the device are $669A$ and $1300V$ which have acceptable safety margins.

3.6 Control

Modulus and Symmetric optimum method are are used in this section to tune controller gains. The controller structure is described in previous chapter. It has inner and outer control loop. The outer loop can be DC voltage, active power, or reactive power controller. The inner is current controller and it will be treated first.

3.6.1 Inner Current Loop

The model derived in section 2.2.5, model of the system from modulation index to currents in *dq*-frame was derived. Feed-forward is used to decouple the two axes and

hence the coupling is ignore for controller tuning. The open-loop transfer function for current control is given by equation (3.14).

$$G_{ol}(s) = \frac{V_{dc}}{R_c}\left(\frac{1}{\frac{L_c}{R_c}s+1}\right)\left(\frac{1}{T_{eq}s+1}\right)\left(k_p + \frac{k_i}{s}\right) \tag{3.14}$$

where all the quantities are in per unit. T_{eq} is the total delay in the loop. The first part is PWM delay approximated to equal half the switching period [22]. The other is delay due to anti-aliasing filter cornered at half the switching frequency. Adding these delays together gives $T_{eq} \approx 600\mu s$. The controller gains are calculated, as per Modulus Optimum criterion, to be $k_p = 0.4$ and $k_i = 1.25$. To verify the design and check it robustness, Bode plot and step response of the controller are plotted in Figure 3.10.

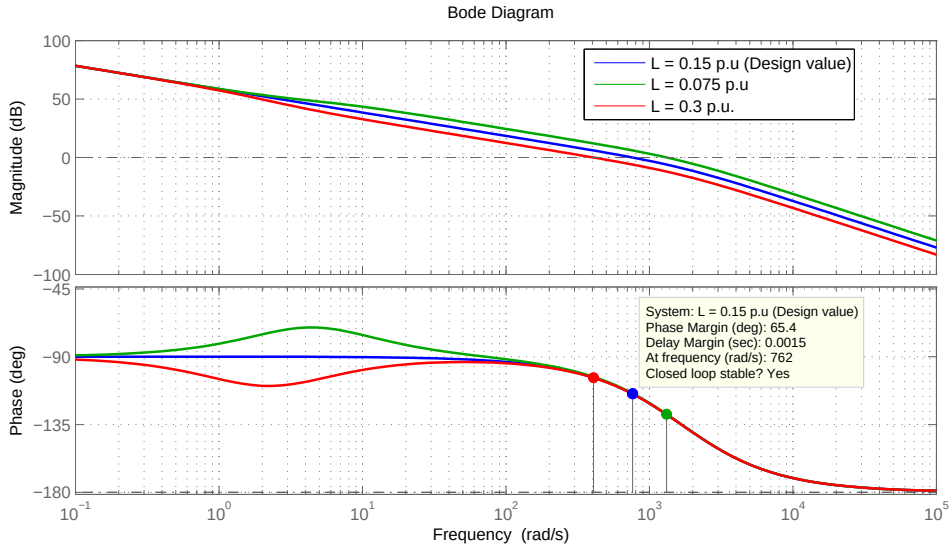


Figure 3.10: *Frequency response of the current controller for different values of inductance*

At the design value, the controller exhibits the expected phase margin of $\approx 65^{\text{deg}}$. Robustness of the controller under deviation of inductance value can be seen on the same figure. Increase in inductance, compared to design value, results in more damped system which is slower and more stable. In contrast, reduction of inductance reduces the phase margin resulting in faster system with more overshoot. This is confirmed by step response plot in Figure 3.11.

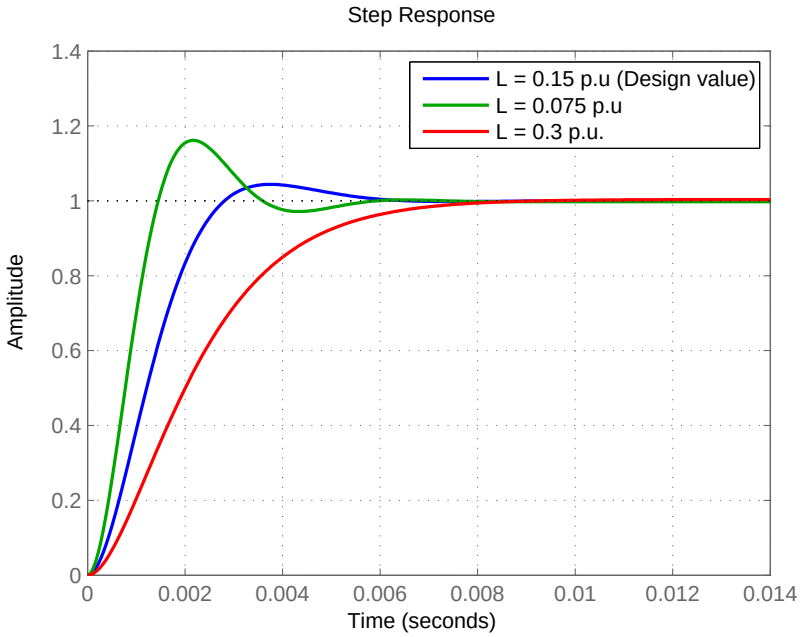


Figure 3.11: *Step response of the current controller for different values of inductance*

3.6.2 Outer P,Q Controller

Active Power, P, and Reactive Power, Q, are identical as derived in this section. The PLL is set to lock to grid phase angle which implies that there will be no q-axis component in the grid voltage at the point of coupling. Under this condition P and Q in per unit are

$$P = \left(\frac{v_d}{v_{dc}}\right) i_d \quad Q = -\left(\frac{v_d}{v_{dc}}\right) i_q \tag{3.15}$$

Since the current controller in d and q axis are identical, dynamics of P and Q controller is the same with the only difference being sign. Therefore, P controller will be designed and the same controller will be applied to Q. Anti-aliasing filter delay and closed loop response time of the current loop are included in the open loop transfer function,

$$G_{ol}(s) = \left(\frac{v_d}{v_{dc}}\right) \frac{1}{T_{eq}s + 1} \left(k_p + \frac{k_i}{s}\right) \tag{3.16}$$

The values are once again in per unit. T_{eq} is the sum of filter delay and current loop response time. Its value is $\approx 1.4ms$. k_p and k_i are calculated to be 0.243 and 552 ,respectively, in order to achieve damping of $\zeta = \frac{1}{\sqrt{2}}$ and natural frequency of $\omega_n = 628rad/s$.

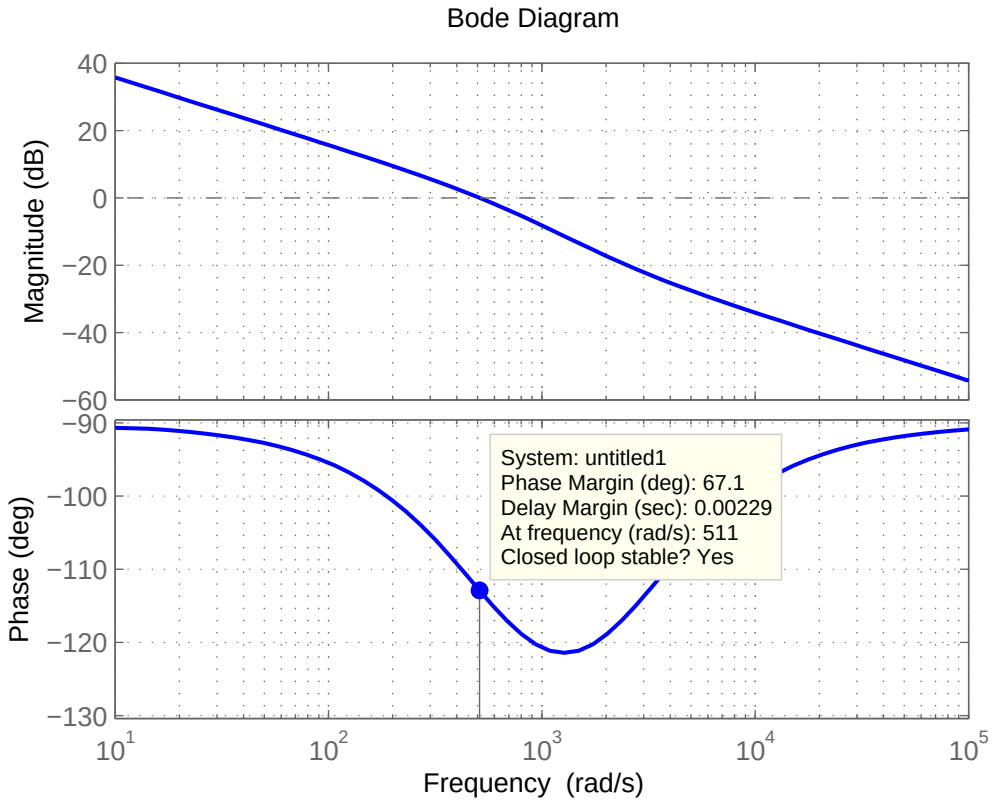


Figure 3.12: *Frequency response of the P controller*

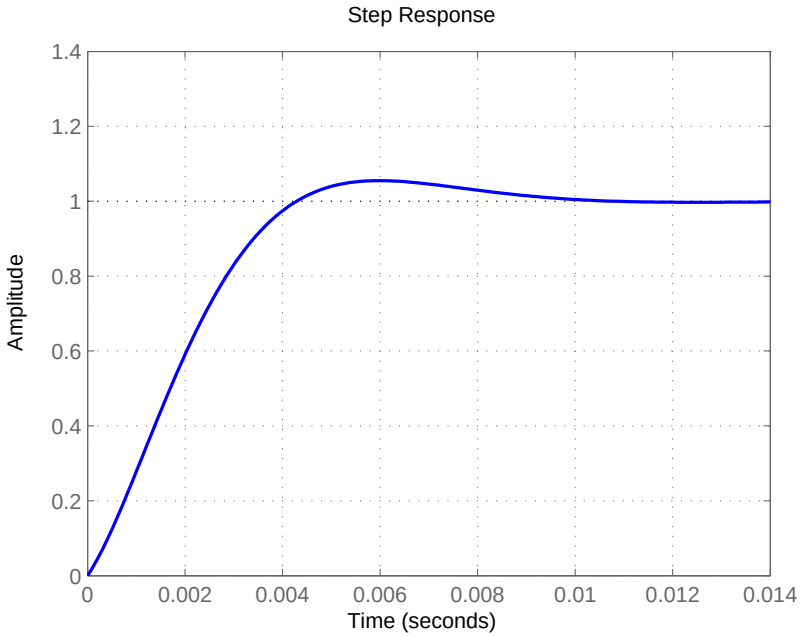


Figure 3.13: *Step response of the P controller*

Figures 3.12 and 3.13 show frequency response and the respective step response once again showing good correlation between phase margin and overshoot.

3.6.3 DC Voltage Regulator

The DC bus control problem is more of a regulation problem with the aim of rejecting disturbances, like load current change. Dynamics of the system from current input to DC bus voltage output is given by

$$G_{ol}(s) = \left(\frac{v_d}{V_{dc}}\right)\left(\frac{1}{Cs}\right)\left(\frac{1}{T_{eq}s+1}\right)\left(k_p + \frac{k_i}{s}\right) \tag{3.17}$$

where all the quantities are in per unit and T_{eq} represents sum of all delays including the current loop response; $T_{eq} \approx 3ms$. Cancellation of slow poles to improve system performance is not advised since these poles would appear as closed loop poles on the disturbance to output transfer function making the system's rejection performance very poor. To overcome this problem Symmetric Optimum design is adopted. Using this method, the controller gains are calculated to be $k_p = 9.87$ and $k_i = 365$ setting the parameter a to be 3. Figures 3.14 and 3.15 show response of the regulator designed. The step response exhibits large overshoot. However, the main objective is to reject disturbances and the system show satisfactory $100ms$ rejection time for 1.0 p.u disturbance without ringing.

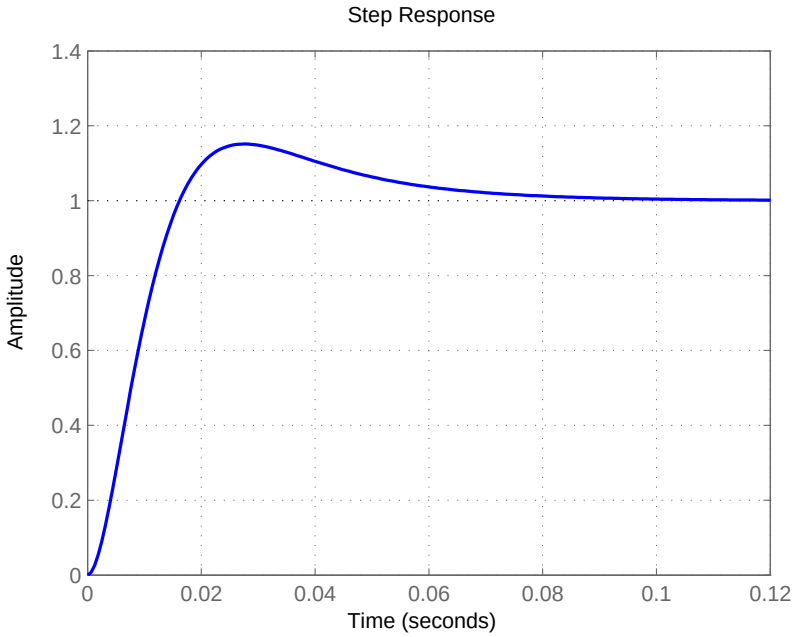


Figure 3.14: *Step response of the DC bus regulator*

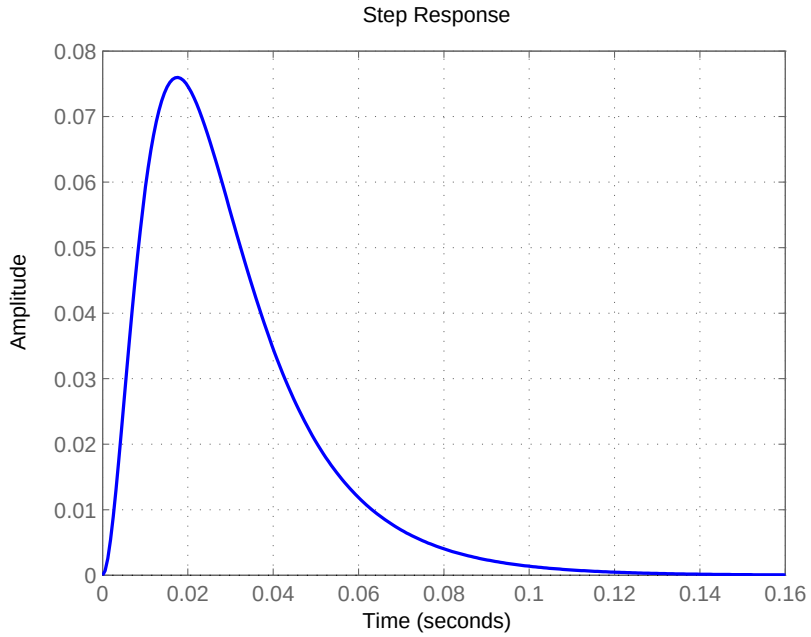


Figure 3.15: *Load current disturbance response of DC bus regulator*

All the controllers designed so far are put into time domain simulation model described in [CASE STUDY MODEL]. This will be the topic of next section.

3.7 Simulation

The simulation model has been described in Chapter 2. Here simulation results under different test cases are presented.

3.7.1 Controller Performance

This test is performed to evaluate tracking and regulation performance of outer control loops as defined in the previous section. The reference tracking of the offshore converter to ramp and step changes is shown in Figure 3.16. The tracking performance is quite satisfactory since it track the ram signal with no error and the step response has no overshoot. Change in active power offsets the balance between power flowing into and out of the DC link causing the DC voltage to change. This is dealt with by the DC voltage regulator by passing the extra power to the grid, thus, restoring the balance.

Figure 3.17 shows regulation of the DC bus voltage where it has been zoomed around $t = 8.5sec$ to show rejection of step disturbance in active power in the offshore station. The rejection time is inline with the one predicted by the linear transfer function.

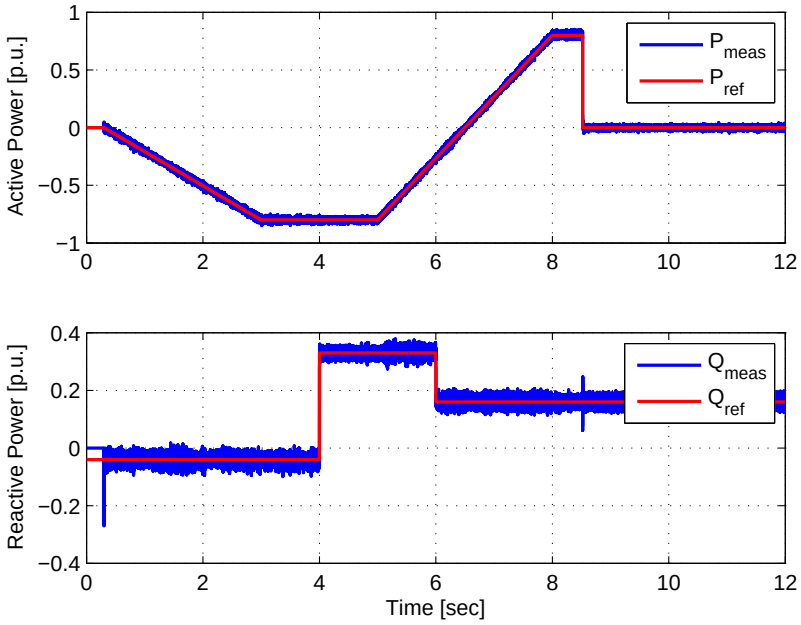


Figure 3.16: *Active and Reactive Power tracking in the Offshore Station controller*

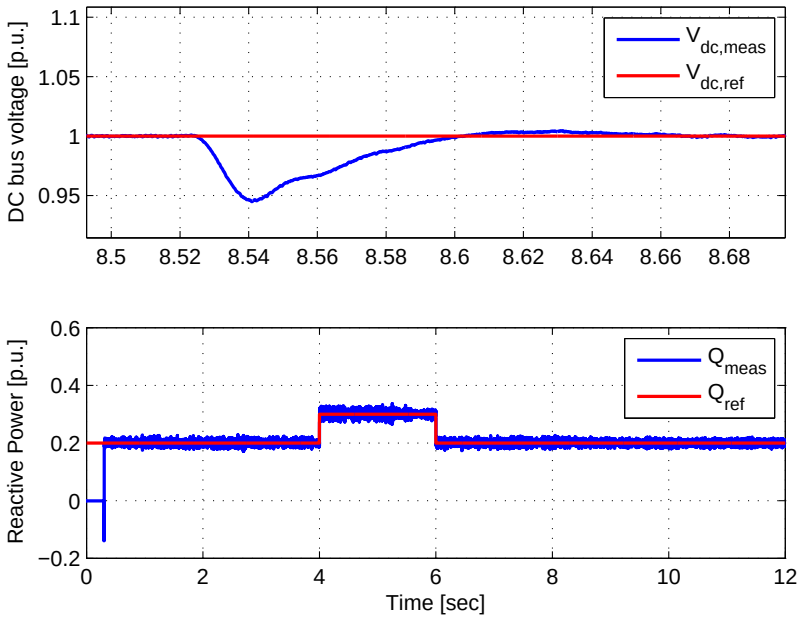


Figure 3.17: *V_{dc} regulation and Reactive Power tracking in the Onshore station controller*

3.7.2 Harmonics

Harmonic content in current and voltage waveforms of the AC side are presented in this section. Phase voltage waveform at the terminal of the converter,together with its harmonic content, is shown in Figure 4.4. Two harmonic distortion indicators are shown on the figure. The THD, $\approx 83\%$, indicates that is highly polluted. However, the harmonics are centered around the switching frequency which is relatively high, $m_f = 27$. Out of the harmonics, the ones having more pronounced effect on filtering requirement are those with low frequency. Therefore, THD is not a good measure of performance for filtering requirement. WTHD, $\approx 1.9\%$, is related to the current harmonics which propagate in the system and increase the losses.

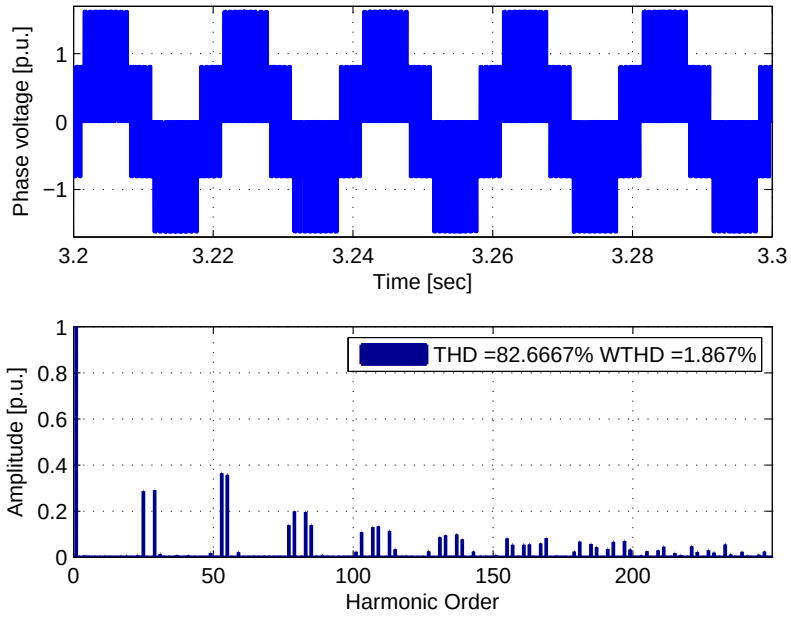


Figure 3.18: *Phase to neutral voltage of offshore converter*

The relation between WTHD of the voltage and THD of the current is given by equation (3.18).

$$THD_i = \frac{WTHD_v}{X_{pu}} \tag{3.18}$$

where X_{pu} is per unit series impedance between the converter and the grid. The current waveform and its harmonic content is shown in Figure 4.6. The current waveform exhibits THD of $\approx 14.6\%$ which is close to the one predicted with equation (3.18), $\approx 13\%$

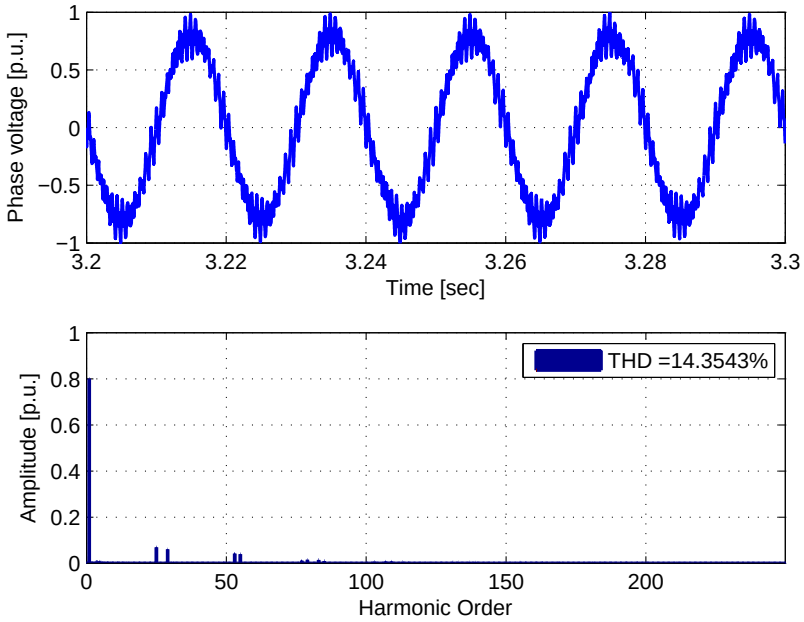


Figure 3.19: *Line current of offshore converter*

3.7.3 Loss

Power loss in the converter under different operating conditions is shown in Figure 4.7. The losses vary when active power directions is reversed. This is due to the fact that different devices (IGBT or Diode) conduct for longer duration depending on the operating condition. The figure also shows breakdown of the loss into switching and conduction. The total loss in in the range $0.5\% \backsim 0.7\%$ of the converter rating under all the condition considered.

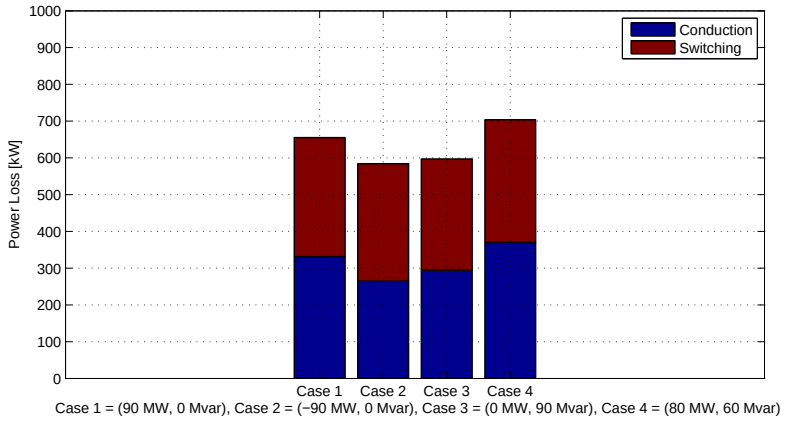


Figure 3.20: *Loss under different conditions*

Chapter 4

Three Level NPC VSC

4.1 Introduction

This chapter deals with three level NPC converter used in HVDC transmission. The circuit topology is shown in Figure 4.1. Most of the components are similar to the two level VSC. Therefore, it is not treated in great detail.

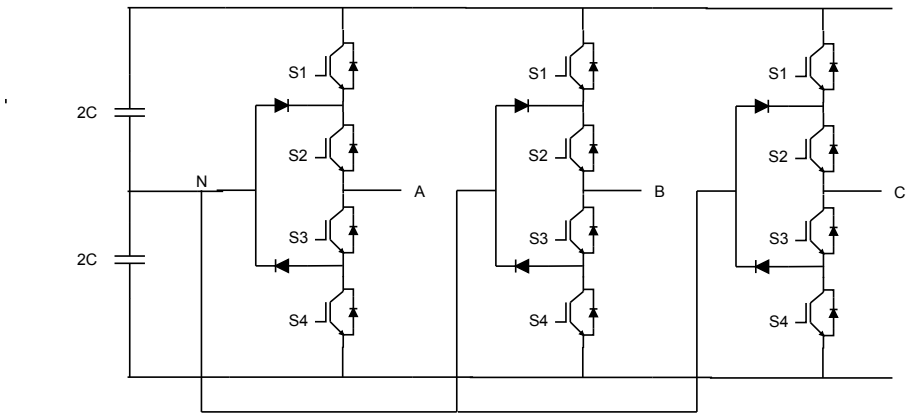


Figure 4.1: *Three level NPC circuit*

4.2 Operating Principle

The NPC is a combination of two half bridges described in the previous chapter. These are S_1 and S_3 forming the first half bridge while S_2 and S_4 forming the second one. Table 4.1 depicts operation of the converter under each of the four feasible states when the two bridges are operated in complementary mode. The bar on top

State	$S_1/\bar{S_3}$	$S_2/\bar{S_4}$	V_{out} for $i_{out} > 0$	V_{out} for $i_{out} < 0$
1	1	1	$\frac{V_{dc}}{2}$	$\frac{V_{dc}}{2}$
2	0	1	0	0
3	0	0	$-\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{2}$
4	1	0	$-\frac{V_{dc}}{2}$	$\frac{V_{dc}}{2}$

Table 4.1: *Switching States of NPC converter*

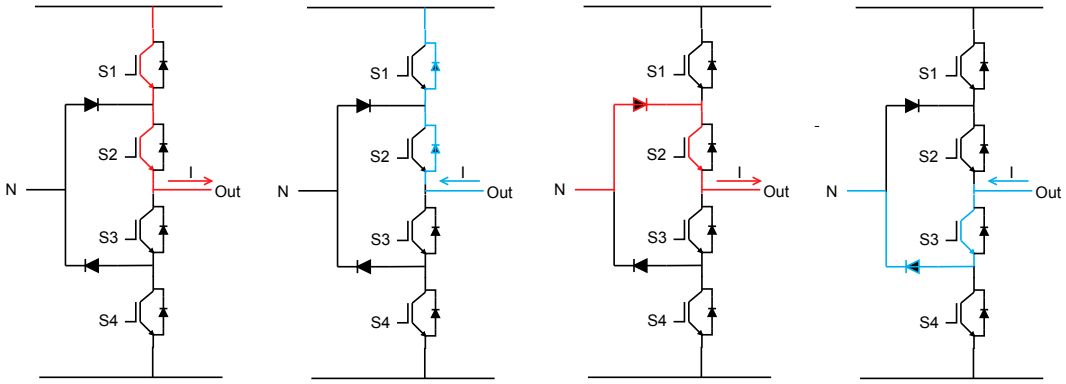
of the switching states, S_x, indicates logical NOT. The fourth state gives different outputs depending on the current direction. The first three, on the other hand, produce the same output irrespective of the current direction. These states can be used to produce three different voltages and hence the name three-level. The output voltage is referred to the DC mid point.

Figure 4.2 indicates which device is conducting for each state and current direction combination.

4.3 Modulation

As described in the previous section, the NPC has two independent half bridges driven by two pair of complementary signals. Different modulation techniques have been described in literature [28], [19] to generate the gating signals. These can be grouped in the same manner as two level modulation strategies. One group uses multiple carriers while the other use multiple modulating signal. Since generating modulating signals is generally easier than generation carriers, the second approach will be utilized.

From Table 4.1, it can be seen that positive output voltage can be generated when the second half-bridge is high (upper switch turned on). In this scenario, the output jumps between $\frac{V_{dc}}{2}$ and 0 generating average positive voltage over the switching period. To generate negative voltage, the first half bridge has to be low (lower switch turned on). This would imply that when a certain polarity voltage is to be generated, only one half bridge is actively switching while the other is forced to either high or low state. Therefore, the modulating signal, and 180° shifted version of it, can be used with a carrier that spans from 0 to 1 to generate the gating signals for the two half bridges. This arrangement, together with the three level output, is shown in Figure 4.3.



(a) State 1 *(b) State 2*

(c) State 3 *(d) State 4*

Figure 4.2: *States of a single leg of NPC with current flow*

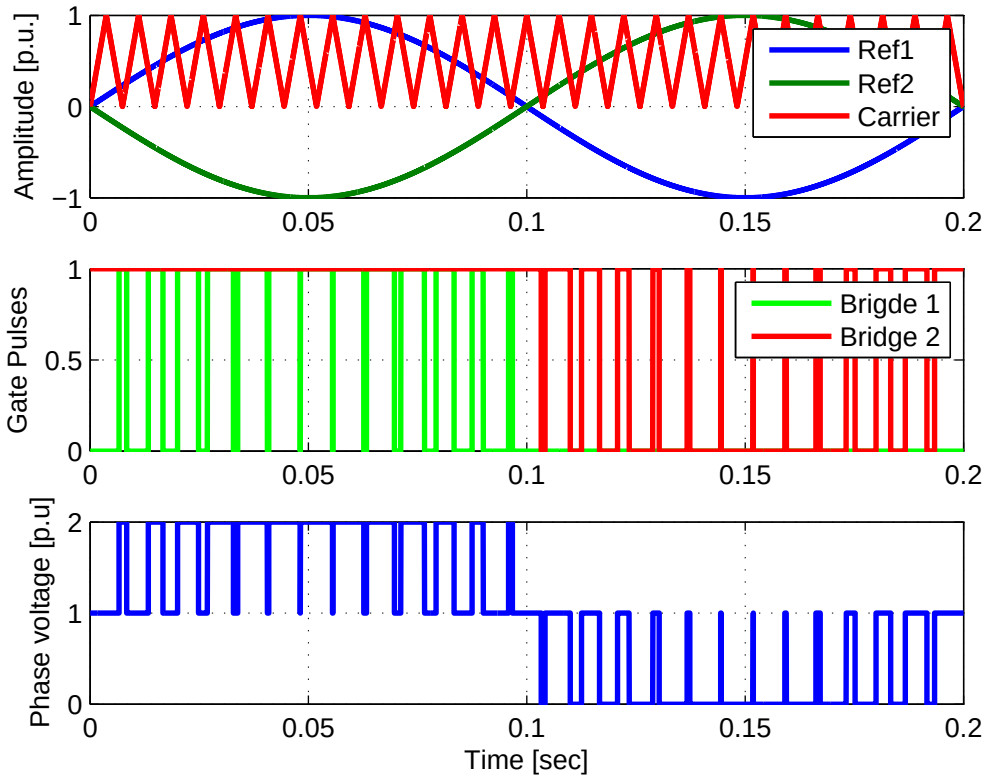


Figure 4.3: *Modulation waveforms for three level NPC*

4.4 Analysis

Analysis of the NPC focuses on AC side current ripple and the DC voltage ripple as was the case for two level VSC. The AC side current ripple has the same equivalent circuit as the two level VSC. The DC voltage ripple, on the contrary, has a different mechanism due to the mid point current. This section briefly describes peculiar properties of the NPC to avoid repetition.

4.4.1 Mid point current

The current through the DC mid point is superposition of the value for positive voltage and negative voltage. When generating positive voltage, the load current, i, is the sum of positive bus current and the mid point current. Similarly, when generating negative voltage, the load current is sum of negative bus current and mid point current. Putting these two arguments together, the mid point current is give by equation (4.1) [19]

$$i_{mid} = i - (i_p + i_n) \tag{4.1}$$

where i_p and i_n are currents in the positive and negative buses respectively. Average value of the mid point current over a switching interval is given by equation (4.2).

$$\bar{i}_{mid} = i - m \cdot i \left(sgn(m) - sgn(-m)\right) \tag{4.2}$$

where m is fundamental voltage reference, $sgn(\cdot)$ returns 1 when its argument is positive and 0 otherwise. In [19] simplified analysis of the mid point current of three phase NPC was performed. The result shows that the mid point current contains triplen harmonics with third harmonic being the most dominant one. It was also shown that the amplitude of the third harmonic lies between 51% and 76% of the AC side current the worst case occurring when operating at zero power factor.

4.4.2 DC Voltage Ripple

The DC voltage ripple is generated by the same mechanism as two level VSC. The current through the capacitor charge and discharge the capacitor depending on its direction. Additional component of the capacitor current that is related to the NPC is the mid point current. As discussed in the previous section, the mid point current contains a dominant third harmonic component which is split between the two DC link capacitors. This results in third harmonic ripple on each capacitor. The capacitance plays a major role in attenuating the ripple. [[19] analyses effect of DC voltage ripple on harmonic content of the AC side voltage. The results reflect that the dominant third harmonic ripple in the DC voltage imposes third and fifth

harmonic voltages on the AC side. This would require bulky filtering and hence it is considered a major drawback.

4.5 Dimensioning

Since the objective of this thesis is to compare merits inherent to the topology, most of the components had to be chosen to be similar. In light of this argument, the series reactor and DC link capacitance (total series combination) are kept the same as the two level counterpart. The major difference is rating of semiconductor devices used. In contrast to two level VSC, all the semiconductor devices (valves) are rated to half the DC bus voltage. Therefore, each valve contain series connection of 75 devices giving the same safety margin as the two level VSC.

4.6 Control

The controller used for the NPC is the same as the two level counterpart therefore, it is not presented here.

4.7 Simulation

This section presents simulation results for the three level NPC used in the case study model. The controller exhibits the same transient response as it did with the two level VSC. Therefore, it is not repeated here. Harmonic and Loss results are presented in what follows.

4.7.1 Harmonics

Phase voltage, together with its harmonic content, is shown in Figure 4.4. It exhibits a strong third harmonic that is caused by the DC side mid point current, Figure 4.5. The waveform has three levels which resulted in a lower THD , $\approx 65\%$, than the two level VSC. However, the third harmonic in the DC side produces lower order harmonics which are more difficult to filter.

Phase current, before shunt filters, is shown in Figure 4.6 together with its harmonic spectrum. THD of the current is $\approx 18.5\%$ which can be approximated from WTHD of the phase voltage using equation (3.18). The THD indicates that shunt filtering is required to meet grid requirements.

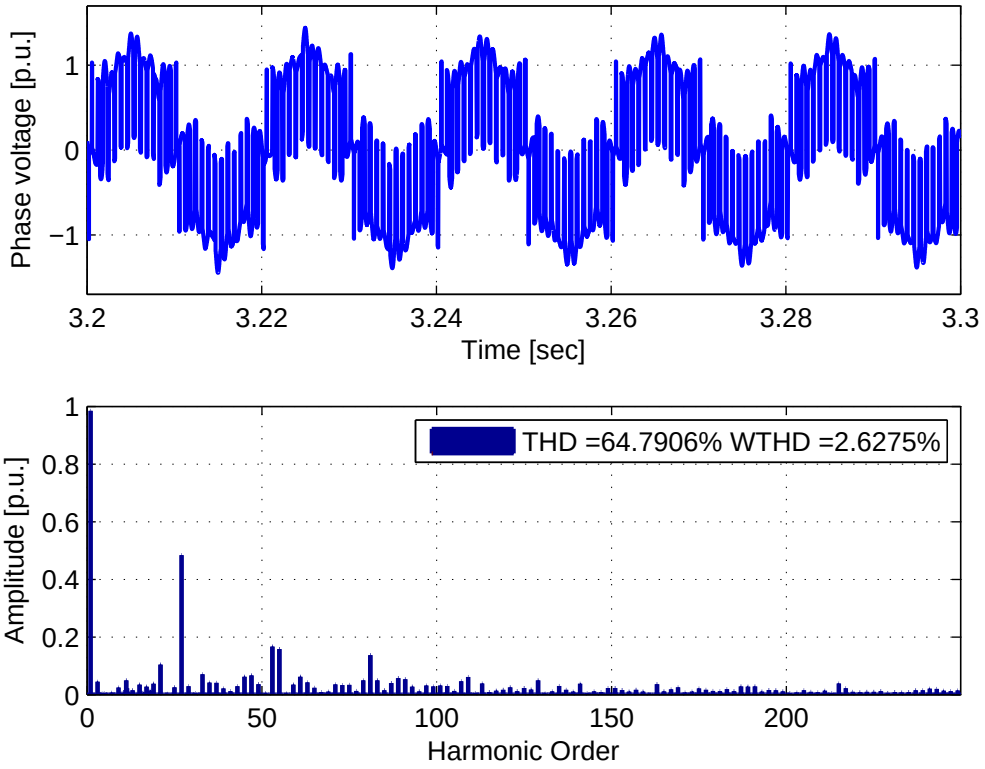


Figure 4.4: *Phase to neutral voltage of offshore converter, NPC*

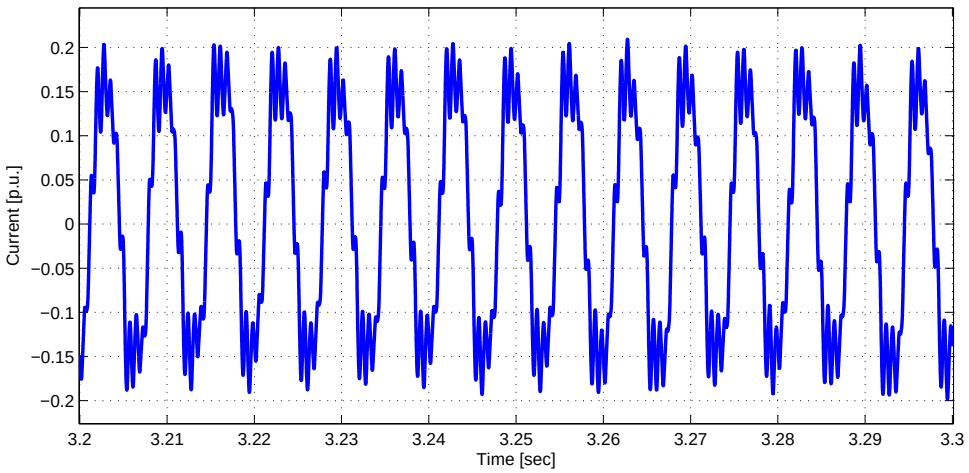


Figure 4.5: *Mid point current of offshore converter, NPC*

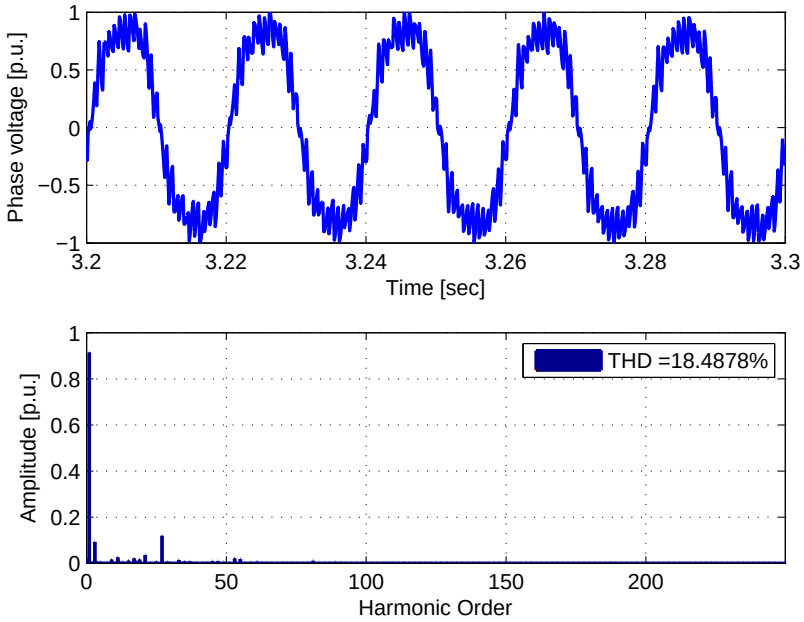


Figure 4.6: *Line current of offshore converter, NPC*

4.7.2 Loss

The loss of NPC under different loading conditions are depicted in Figure 4.7. Two features can be observed comparing to two level VSC. First is that the total loss is lower. The second point is that the conduction loss takes more share in the total loss. The switching losses take lower share because of the fact that each valve blocks half the DC bus voltage and hence results in lower switching energy. There is also a significant difference between Inverter mode (Case1) and Rectifier mode (Case2) because the diodes are used often in the later case resulting in higher conduction loss.

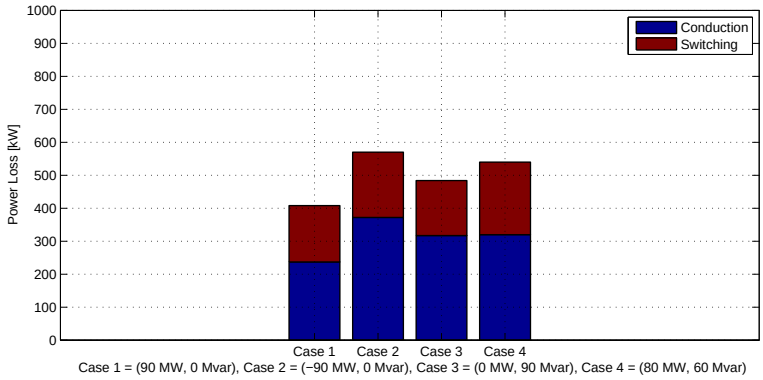


Figure 4.7: *Loss under different conditions, NPC*

Chapter 5

Modular Multilevel Converters (M2C)

5.1 Introduction

Multilevel converters compare favorably to 2 Level and 3 Level converters mentioned in the previous chapters. The reason being lower harmonic generation, elimination of series connection of switches, and lower insulation stress, dv/dt. A number of multilevel converter topologies were described in [28]. But, most of the topologies described are not modular in design and hence lack scalability [29],[30],[14],[31]. A more attractive solution is the M2C which was first proposed by Marquardt and Lesnicar in 2003[14]. The cascaded H bridge also satisfies the scalability requirement but , it requires isolated DC supply for each sub-module which is undesirable and hence it is not considered in this section.

The M2C is composed of a series connection of cells (sub-modules) which are identical. This basic structure is shown in Figure 5.1. Each phase leg is composed of upper and lower arm each consisting of half the number of cells per phase. The DC link capacitance is distributed between the cells. This results in lower peak current during hard discharge due to DC side fault [30].

Each arm also has an arm inductance whose purpose is two fold; to limit circulating current and to limit the rate of rise of arm current during fault. The bypass switch at the output of the cell can be realized with a Thyristor in parallel with a mechanical switch. Its function is to bypass faulty cell and to protect the cell in the event of DC side short-circuit [11]. Therefore, DC fault is handled by limiting the slope of arm current, turning off all IGBTs, and tripping the AC circuit breakers.

There is a variety of M2C depending on the design of the cell [32],[11],[33],[34]. Most of the cell designs are motivated by the need for fault blocking capability which is

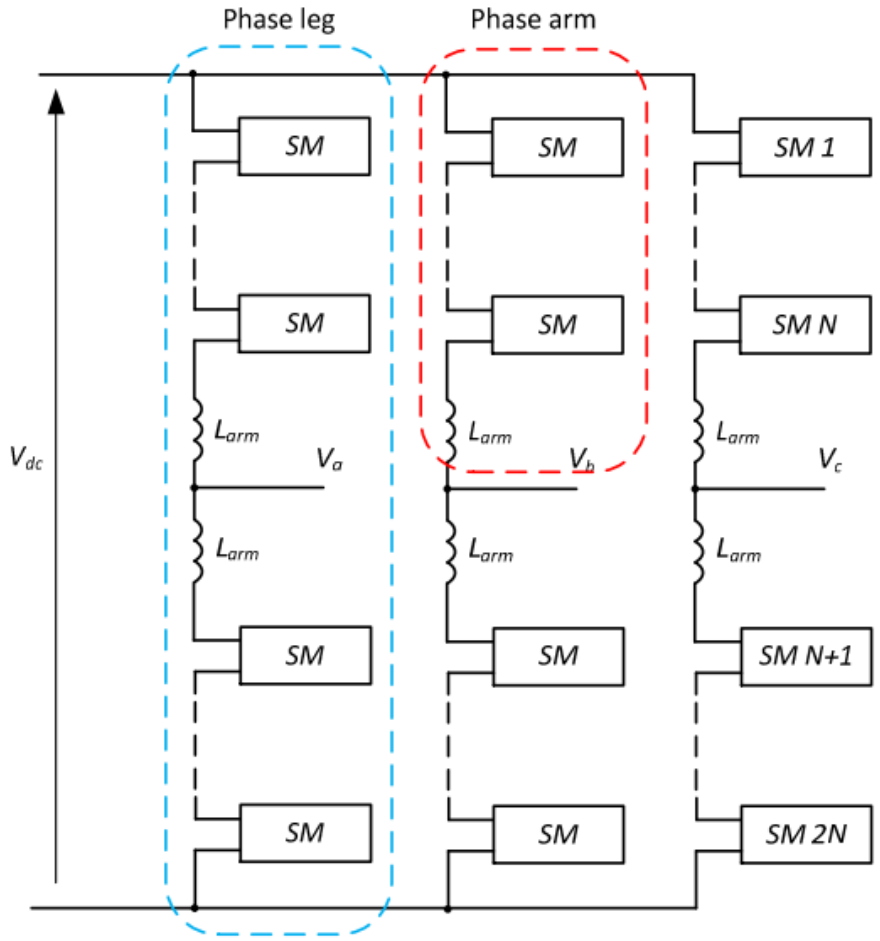


Figure 5.1: *M2C Basic Structure*

required in multi-terminal DC networks [11]. But for this work, the half bridge will be considered.

5.2 Principle of Operation

The half-bridge is the simplest cell which consists of two transistors and a capacitor as shown in Figure 5.2. The AC terminal of the cell is shown by V_o and there is no DC source required [11]. AC output voltage of the cell jumps between 0 and V_c while charging or discharging the capacitor depending on the direction of current in the arm.

The current directions and active switches are also shown in Figure 5.2. In Figure 5.2(c) and (d), the capacitor is bypassed and its voltage will remain constant if parasitic discharge is ignored. In (a), the capacitor is discharging while in (b) it is charging. One switching state, not mentioned in the table, is when both switches

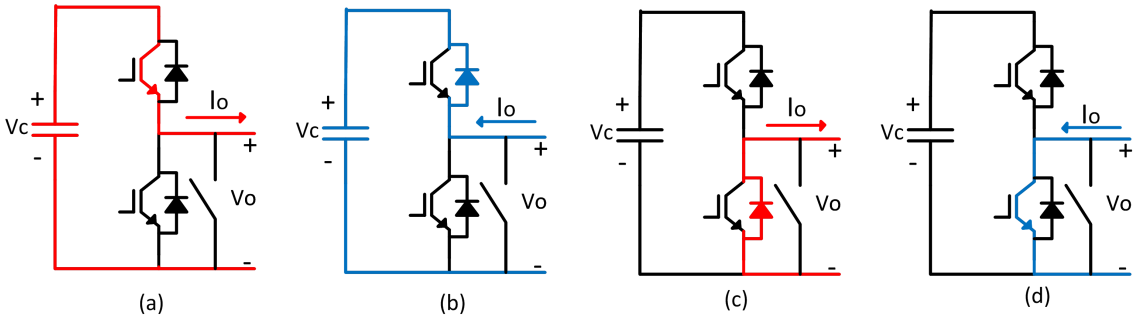


Figure 5.2: *Half Bridge cell and its operating modes*

are turned off. This could happen during fault. The cell will take either state (b) or (c) depending on direction of current.

Mode No.	Conducting Switch	V_o	I_o	Capacitor	Figure
1	Top	V_c	Positive	Discharging	Figure 5.2 (a)
2	Top	V_c	Negative	Charging	Figure 5.2 (b)
3	Bottom	0	Positive	Not affected	Figure 5.2 (c)
4	Bottom	0	Negative	Not affected	Figure 5.2 (d)

Table 5.1: *Half Bridge Cell Operating Modes*

5.3 Modulation Techniques

Modulation techniques, in Multilevel converters, are broadly divided in to High frequency and Fundamental frequency techniques [28]. The classification is based on the number of commutations in a fundamental period. Fundamental frequency techniques are used with high number of cells where the harmonic distortion is acceptable.

5.3.1 High Frequency Techniques

A common feature of High frequency techniques is their ability to produce the desired reference in average at the end of each switching period. The most important members of this group are Multilevel Sinusoidal Pulse Width Modulation (SPWM) and Space Vector Modulation.

The Multilevel SPWM generates gating signals by comparing sinusoidal reference with multiple triangular carriers. The carriers are either phase shifted or displaced in amplitude [35]. The phase-shifted version is provides equal duty cycles and loss distribution unlike level shifted counterpart. To achieve loss and duty cycle equalization additional methods such as carrier rotation can be implemented [35]. As the number of levels increase, the number of carriers required becomes very large and impractical.

Space vector modulation is well known preferred technique for 2 level converters because it provides better DC voltage utilization.Figure 5.3 shows switching states of an N-level converter.It can be seen that, even for 5 level converter, selecting a switching state is very difficult because of redundant states [28]. Therefore, it is not used in M2C Converters with large number of levels.

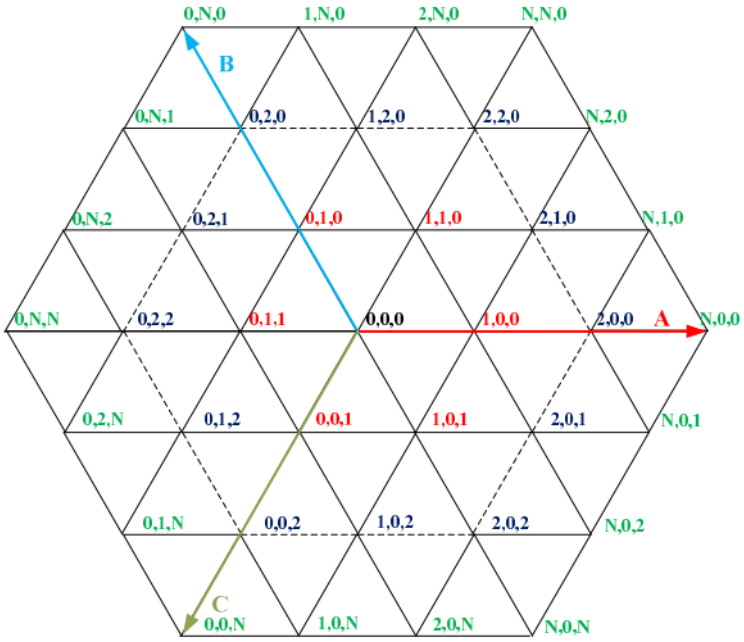


Figure 5.3: *Switching states of Space vector Modulation [2]*

5.3.2 Fundamental Frequency Techniques

This group of techniques are characterized by a stair case output. Most of the techniques in this group have one or two commutation per fundamental period [28]. Staircase waveform is optimized for harmonic content. The switching instants are calculated in such a way that output voltage has the lowest harmonic content.

An alternative approach is based on the space vector theory, Space Vector Control(SVC). Switching state that is closest to the reference is chosen. This method does not involve high frequency switching. Since the number of levels is large, the

error incurred is not significant. Nearest level modulation [2],[36] is an improvement to SVC where one cell is switched at high frequency (PWM Cell) while the remaining cells are selected as per SVC technique. This technique is applicable to any level and produced low harmonics on the output. At any sampling instant, there will be at least one PWM cell. A method for selection of cells to take on different roles is discussed in [36]. Because of its low switching frequency, the Nearest Level Modulation (NLM) with one PWM cell will be used for further studies on M2C in this thesis.

In NLM, the number of cells to be fully on , $N_{on,up}$ and $N_{on,low}$, are calculated using equations (5.1) and (5.2).

$$N_{on,up} = \lfloor N \cdot \left(\frac{1}{2} - \frac{V_{ac,ref}}{V_{dc}} \right) \rfloor \tag{5.1}$$

$$N_{on,low} = \lfloor N \cdot \left(\frac{1}{2} + \frac{V_{ac,ref}}{V_{dc}} \right) \rfloor \tag{5.2}$$

where $\lfloor \cdot \rfloor$ represents floor rounding function, N is the number of cells per arm of the M2C. Once these numbers are calculated, the remaining task is to calculate the error introduced by the rounding function and compensate for it using PWM on one of the cells. Waveforms of NLM applied to a 5 cell M2C with common mode injection is shown in Figure 5.4. The second plot shows the error incurred by the rounding function. This error is compared with a triangle function spanning from 0 to 1 to generate the gating signals for the PWM cell.

Assuming a constant DC voltage the harmonic spectrum of the output of Figure **??** is shown in Figure 5.5. The first dominant harmonic is the third harmonic which is due to the common mode voltage injection followed by the PWM frequency , $27 \cdot f_1$. Sampling frequency greatly impacts harmonic content of NLM.

Impact of sampling frequency on harmonic distortion and number of levels of the AC side voltage is studied in [37] where it a criteria for selection of sampling frequency is provided. Selection of the sampling interval used for simulation, later in this chapter, is done based on this method.

5.4 Analysis

The M2C has different operating mechanism which also makes the analysis different. Analysis of M2C focuses on capacitor voltage ripple and arm currents. This can be done by developing a simplified model for the MMC.

The upper and lower cells can be considered as a group producing voltage $v_u(t)$ and $v_l(t)$, respectively. With this assumption, the equivalent circuit of a phase leg is shown in Figure 5.6. Applying KVL around the loop equation (5.3) and

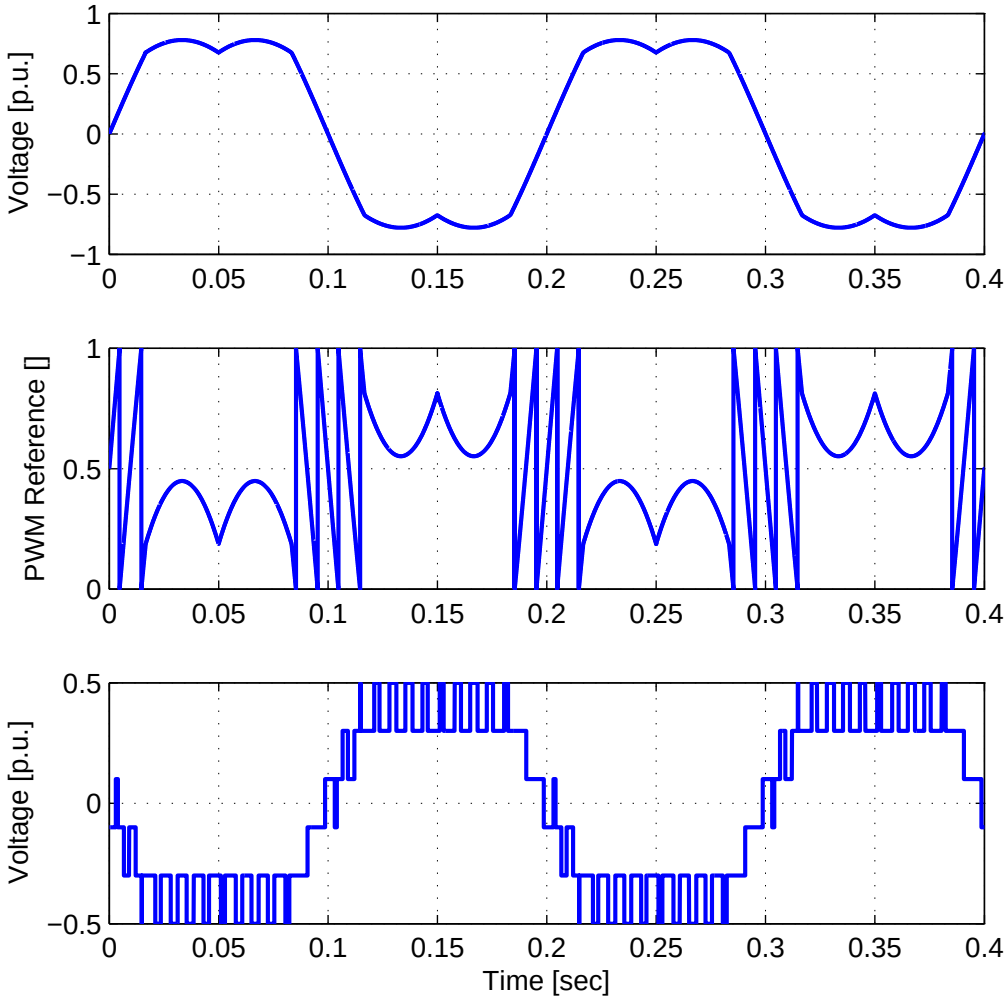


Figure 5.4: *M2C Modulation Waveforms*

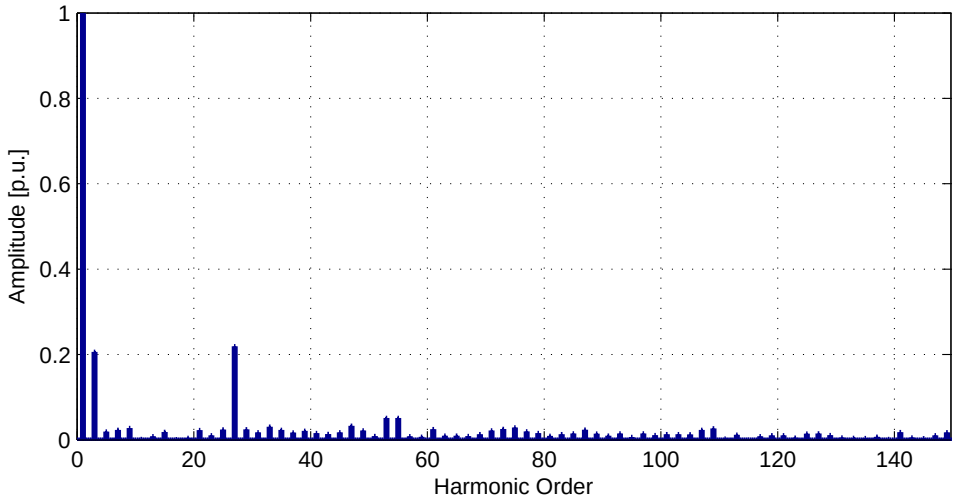


Figure 5.5: *Harmonics in 5 cell M2C,* $m = 0.9$*,* $m_f = 27$

equation (5.4) can be found. In this analysis, the voltage ripple on the DC side is ignored.

$$v_{ac}(t) = \frac{V_{dc}}{2} - v_u(t) - L\frac{di_u(t)}{dt} - Ri_u(t) \tag{5.3}$$

$$v_{ac}(t) = -\frac{V_{dc}}{2} + v_u(t) + L\frac{di_u(t)}{dt} + Ri_u(t) \tag{5.4}$$

Where L is the arm inductance and R is the effective resistance representing ohmic losses in the arm.

Since the circuit is symmetric, impedance of the upper and lower arms are equivalent. Therefore, the AC side current will divide equally between the upper and lower arms. If there is non-symmetry due to component tolerances or other factors, it can be modeled by introducing current sharing factor between the upper and lower arms. There will also be a circulating current component on top of half the AC current in each arm giving rise to equation (5.5) and equation (5.6).

$$i_u(t) = i_{circ}(t) + \frac{i_{ac}(t)}{2} \tag{5.5}$$

$$i_l(t) = i_{circ}(t) - \frac{i_{ac}(t)}{2} \tag{5.6}$$

From equation (5.5) and equation (5.6), the circulating and AC side currents are given by average and difference of the two arm currents respectively. A given desired AC voltage can be realized by choosing appropriate reference values to the upper

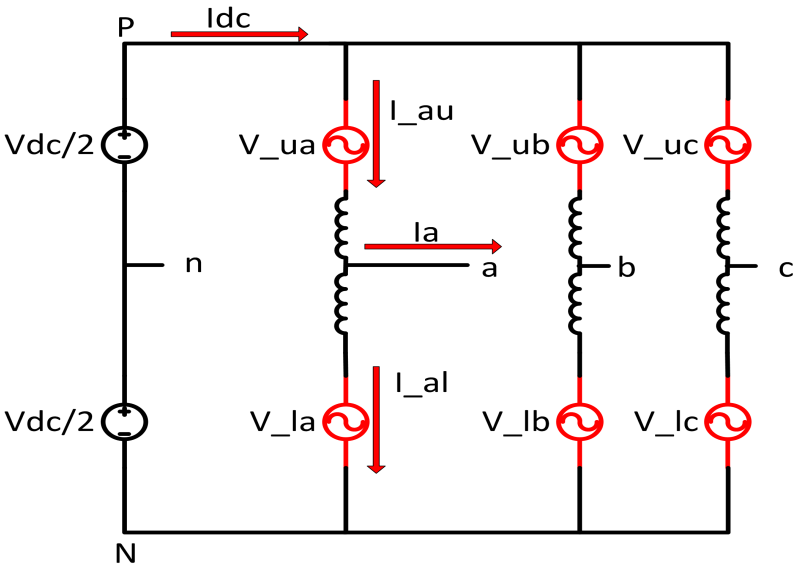


Figure 5.6: *Model of M2C as voltage source*

and lower arms. There are two ways to do this [38]; by applying zero voltage to the arm inductor and by allowing some voltage in the arm inductor. The latter gives additional degree of freedom in controlling the circulating current but it results in hogher circulating current ripple [38]. Therefore, the first approach us adopted and the references are given by equation (5.7) and equation (5.8).

$$v_u^{ref}(t) = \frac{V_{dc}}{2}\left(1 - m\sin(\omega t)\right) \tag{5.7}$$

$$v_l^{ref}(t) = \frac{V_{dc}}{2}\left(1 + m\sin(\omega t)\right) \tag{5.8}$$

where m is the modulation index and ω is the fundamental frequency. It can be seen that sum of the upper and lower arm reference voltage is equal to the DC link voltage so there will be zero voltage applied to the arm inductance.

Simulation of MMC can be time consuming and demanding for computer because of large number of measurements and processing. In light of this challenge an average MMC model was developed in [39]. The model is developed by making two basic assumption.

- There are infinite number of cells in an arm so that the number of cells inserted is a continuous function of time.
- There are no harmonic components in the AC output voltage.

By subtracting equation (5.4) from equation (5.3) and rearranging yields a differential equation describing the dynamics of circulating current in equation (5.9)

$$L\frac{di_{circ}(t)}{dt} = V_{dc} - (v_u(t) + v_l(t)) - Ri_{circ}(t) \tag{5.9}$$

The arm voltages can be defined in terms of the total capacitor voltage in the respective arm and the continuous insertion indexes $m_l(t)$ and $m_u(t)$

$$v_u(t) = m_u(t)v_{tot,u} \qquad and \qquad v_l(t) = m_l(t)v_{tot,l} \tag{5.10}$$

The rate of change of the total voltages in each arm is related to the capacitance and arm current as given by

$$C_{eff}\frac{dv_{tot,u}(t)}{dt} = m_u(t)i_u(t) \qquad and \qquad C_{eff}\frac{dv_{tot,l}(t)}{dt} = m_l(t)i_l(t) \tag{5.11}$$

Combining equation (5.9), equation (5.10), and equation (5.11) gives a nonliner set of differential equations that can be solved numerically.

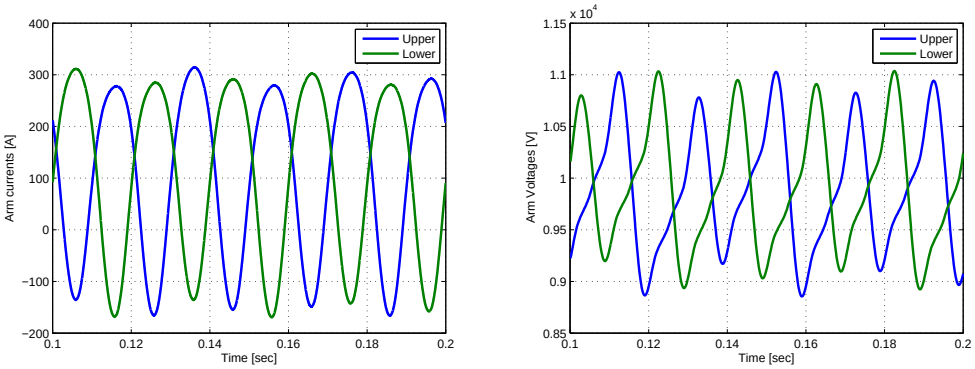
$$\frac{d}{dt}\begin{bmatrix} i_{circ}(t) \\ v_{tot,u}(t) \\ v_{tot,l}(t) \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & -\frac{m_u(t)}{2L} & -\frac{m_l(t)}{2L} \\ \frac{m_u(t)}{C_{eff}} & 0 & 0 \\ \frac{m_l(t)}{C_{eff}} & 0 & 0 \end{bmatrix} + \begin{bmatrix} \frac{V_{dc}}{2L} \\ \frac{m_u(t)i_{ac}(t)}{2C_{eff}} \\ -\frac{m_l(t)i_{ac}(t)}{2C_{eff}} \end{bmatrix} \tag{5.12}$$

The effective capacitance is series equivalent of the number of cells inserted as shown in

$$C_{eff} = \frac{C_{cell}}{m_x(t)n} \tag{5.13}$$

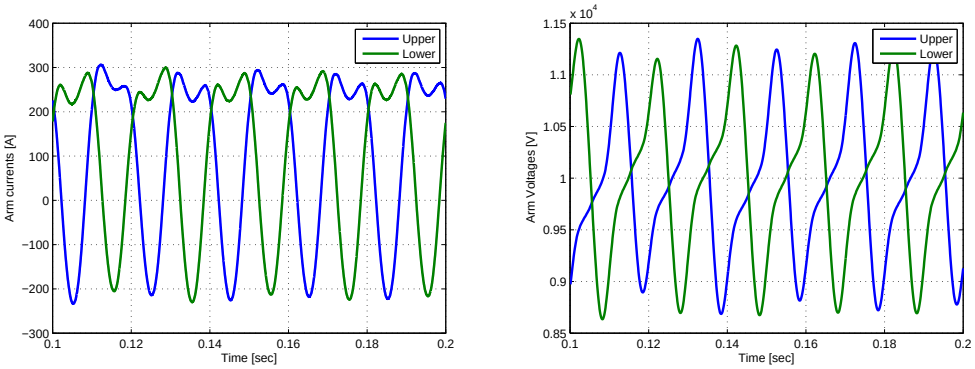
where $x \in \{l, u\}$ and n is the number of cells per arm.

Two cases were simulated using the simplified model developed: large inductance, 16 mH, and Small inductance, 8 mH. The system is a 10 kV, 6 MW converter. The results are shown in Figures 5.7 and 5.8. These waveforms are quite different from conventional converter waveforms. The capacitor exhibits large fundamental and second harmonic ripples which can be considered as disadvantage since it might require a larger capacitance.



(a) Arm Current *(b) Arm Voltage*

Figure 5.7: *Arm voltages and currents with large arm inductance*



(a) Arm Current *(b) Arm Voltage*

Figure 5.8: *Arm voltages and currents with large arm inductance*

5.5 Dimensioning

Because of modular design of M2C, its design is done at a sub-module level. This section presents dimensioning criteria for sub-module capacitor and arm inductor. The number of cells is decided based on the voltage rating of of the IGBT used in the comparison and simulation capacity requirement. Even with moderate number cells, e.g. $N = 10$, simulation can take significant amount of time and resources. In light of this issue, the number of cells was decided to be $N = 15$ to have a good compromise between simulation resources and performance of M2C. Each cell is then made with valves of 10 IGBTs in series.

5.5.1 Capacitance

Different empirical relations have been developed to calculate required capacitance for M2C sub-modules [2],[40]. But, a more analytic approach described in [41] is followed here. The analysis is based on the circuit shown Figure 5.1. The equations developed in the previous section are used in the design.

Referring to Figure 5.6, steady state versions of the upper and lower arm voltages of equation (5.7) and equation (5.8) can be written as:

$$\begin{aligned} v_u &= \frac{V_{dc}}{2}\left(1 - m\sin(\omega t)\right) \\ v_l &= \frac{V_{dc}}{2}\left(1 + m\sin(\omega t)\right) \end{aligned} \tag{5.14}$$

Because of symmetry in the circuit, the DC side current divides equally between the three phases and the AC current splits equally between the upper and lower arms [41]. This gives the following relation.

$$\begin{aligned} I_{au} &= \frac{1}{3}I_{dc} + \frac{1}{2}I_a\sin(\omega t - \phi) \\ I_{al} &= \frac{1}{3}I_{dc} - \frac{1}{2}I_a\sin(\omega t - \phi) \end{aligned} \tag{5.15}$$

To eliminate the peak I_a from equation equation (5.15), power balance between the DC and AC sides is used. In this calculation, losses in the converter are neglected.

$$\begin{aligned} V_{dc}I_{dc} &= 3\left(\frac{mV_{dc}}{2\sqrt{2}}\right)\left(\frac{I_a}{\sqrt{2}}\right)\cos(\phi) = \frac{3}{4}mV_{dc}I_a\cos(\phi) \\ I_a &= 2\left(\frac{1}{3}I_{dc}\right)\left(\frac{2}{m\cos(\phi)}\right) = 2\left(\frac{1}{3}I_{dc}\right)k \end{aligned} \tag{5.16}$$

The parameter k relates the DC current with the AC current. The arm currents can, now, be written as:

$$\begin{aligned} I_{au} &= \frac{1}{3} I_{dc} \left(1 + k \sin(\omega t - \phi)\right) \\ I_{al} &= \frac{1}{3} I_{dc} \left(1 - k \sin(\omega t - \phi)\right) \end{aligned} \tag{5.17}$$

The instantaneous power of the upper arm is:

$$S_u(t) = \frac{1}{6} V_{dc} I_{dc} \left(1 - m \sin(\omega t)\right) \left(1 + k \sin(\omega t - \phi)\right) \tag{5.18}$$

It can be seen that instantaneous power of the arm is a sixth of the total power which is a consequence of the symmetry assumed. Integrating equation equation (5.18) over the interval where $S_u(t)$ is positive, energy storage requirement of the arm can calculated as: [41]

$$W_{cu} = \frac{2}{3} \frac{V_{dc} I_{dc}}{\omega m \cos(\phi)} \left(1 - \left(\frac{m \cos(\phi)}{2}\right)^2\right)^{3/2} \tag{5.19}$$

But, the apparent power $S_u = \dfrac{V_{dc} I_{dc}}{\cos(\phi)}$ where the losses are ignored. Therefore equation equation (5.19) can be written as:

$$W_{cu} = \frac{2}{3} \frac{S_u}{\omega m} \left(1 - \left(\frac{m \cos(\phi)}{2}\right)^2\right)^{3/2} \tag{5.20}$$

This positive energy will cause an increase in capacitors' voltage from V_{min} to V_{max}. If proper balancing is performed, the energy calculated will equally divide between sub-modules in the arm. For M2C with n sub-modules per arm, the energy is given by:

$$W_{c,SM} = \frac{2}{3} \frac{S_u}{\omega m n} \left(1 - \left(\frac{m \cos(\phi)}{2}\right)^2\right)^{3/2} \tag{5.21}$$

This energy can also be written in terms of the voltage change and sub-module capacitance as:

$$W_{c,SM} = \frac{1}{2} C_{SM} \left(V_{max}^2 - V_{min}^2\right) \tag{5.22}$$

$$= C_{SM} \left(V_{max} - V_{min}\right) \left(\frac{V_{max} + V_{min}}{2}\right) \tag{5.23}$$

$$= C_{SM} \Delta V_{max} V_{av} = \frac{C_{SM} \Delta V_{max} V_{dc}}{n} \tag{5.24}$$

If the peak-to-peak ripple factor ,ξ, is defined as percentage of the nominal capacitor voltage, the capacitance can be calculated as:

$$C_{SM} = \frac{n^2 W_{c,SM}}{\xi V_{dc}^2} \tag{5.25}$$

This choice of capacitance, with a proper balancing algorithm, ensure that the peak-to-peak ripple is below ξ. The ripple value is set to 1% which results in calculated minimum capacitance of $\approx 6.04mF$. The value used in simulation is $6mF$

5.5.2 Arm Inductance

The main functions of the arm inductor are to suppress circulating current and limit rate of rise of fault current. In [42], analytic way of calculating arm inductance to fulfill these requirements is presented. But the selection arm inductance is closely related to the control system performance. Additional requirements of avoiding resonance at harmonics of the circulating current is investigated in [40].

There are also empirical methods, [2], that select the arm inductance based on per unit value selected based on experience. The fault limiting requirement usually results in a higher value of inductance. Therefore, in order to limit fault currents the inductance is chosen to be 0.1 p.u. [42]. The series reactor is reduced to 10% to maintain the total equivalent impedance to 15%.

5.6 Control

Control of M2C is broadly categorized into three different tasks: balancing of capacitor voltages, suppression of circulating current, and system level control [43]. Voltage balancing and System control will be discussed in subsequent sections. Circulating current control is not dealt with because of time limitation.

5.6.1 Voltage Balancing

The purpose of voltage balancing controllers is to achieve equal voltage sharing, atleast on average, between the cells in the M2C. Figure 5.9 shows the importance of having a proper balancing algorithm. Different balancing techniques are suitable for different modulation techniques [43].

For Nearest level modulation, sorting method is suitable [36]. The capacitor voltages are regularly measured and sorted in ascending (descending) values. From the sorted list, the ones that have the lowest voltage will be inserted when the arm current direction is in such a way the they will get charged and vice versa. This method could result in many switching instants with in a fundamental period [43]. To

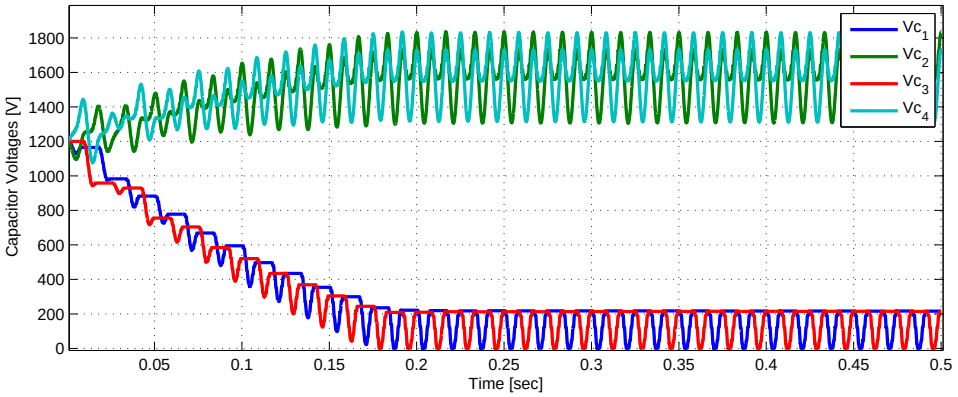


Figure 5.9: *Capacitor voltages without balancing algorithm, 4 cell*

mitigate this problem, insertion method with a defined voltage threshold is proposed in [44]. Overvoltage and under voltage thresholds are defined and switching is only carriedout if either of the limits are exceeded. By using this method it is possible to reduce the switching frequency; but, it is difficult to define the values of these thresholds [45]. Another improvement to the method, where definition of the thresholds is not required, is given in [45]. This method considers only the change in the number of cells to be inserted.

For Level shifted PWM, the same sorting method is applicable; but, in this case different carriers are assigned to a cell depending on its voltage [43]. The same method can be applied to Phase shifted PWM even though it does not, in theory, need additional balancing algorithm.

Due to its simplicity and ease of implementation, the sorting method was adopted for balancing control. Simulation with the aforementioned sorting method was done and the result is shown in Figure 5.10. One can see that the capacitor voltages are balanced on average but there exist some deviation that is well defined. A closer look at the current waveforms and the sorting method revealed that the situation is caused by the circulating current. The sorting algorithm operated by using the sign of line current but the actual arm current also contains a circulating component. Therefore, there might be cases where the arm current and line current have opposite signs causing the deviation under investigation.

To rectify the problem, the sorting algorithm was supplemented with voltage direction indicators. This will avoid any wrong sorting direction that is caused by the circulating current. Simulation result with this solution is shown in Figure 5.11.

5.6.2 System Control

The system level control is very similar toe the conventional decoupled (d-q-0) control system as long as there is an effective balancing control. Development of

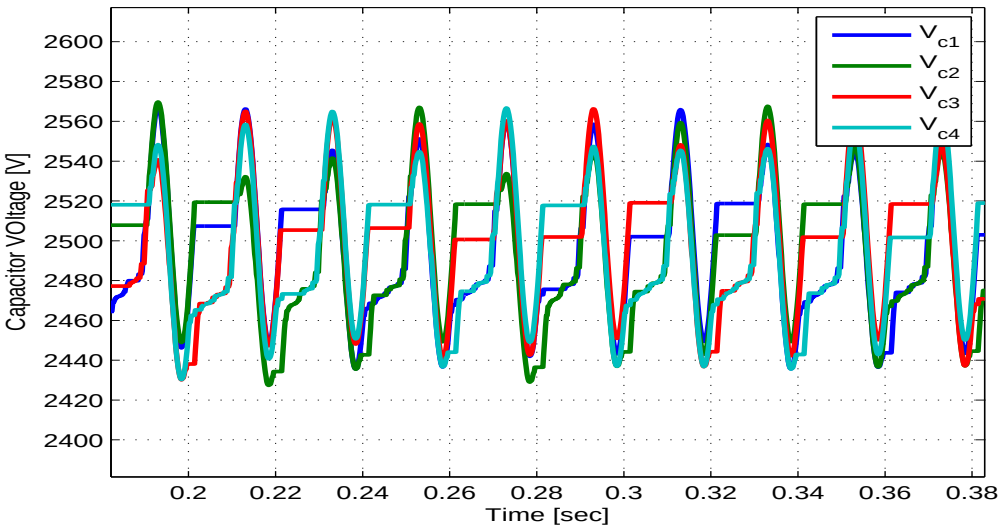


Figure 5.10: *Capacitor voltages with sorting method*

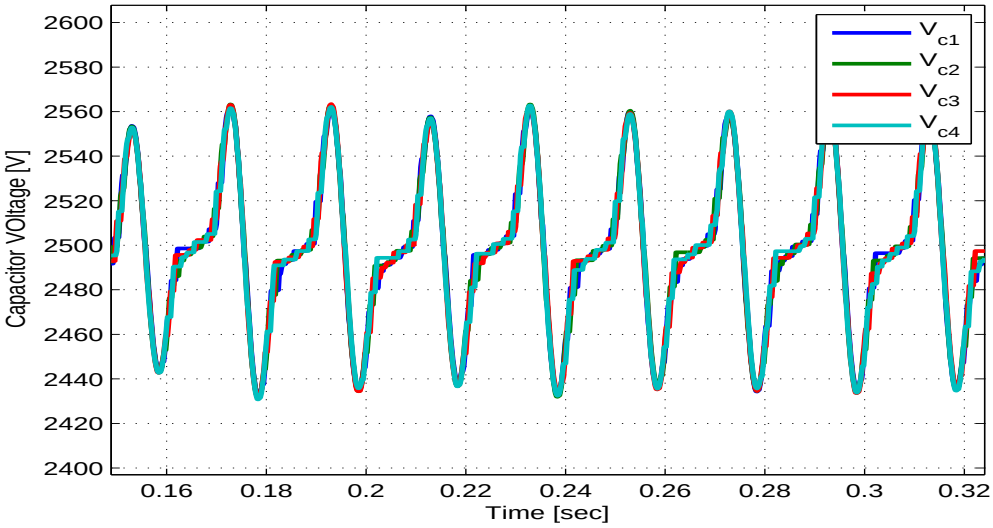


Figure 5.11: *Capacitor voltages with sorting method and supplementary logic*

decoupled control will be presented in Chapter 2. The PLL and other parts of the system remain the same as the other converters discussed so far.

Current Loop

The plant model for the current loop, derived in section 2.2.5, is applicable to M2C. The only difference is that the series impedance is equivalent impedance as given

in equation (5.26).

$$Z_c' = Z_c + \frac{Z_{arm}}{2} \tag{5.26}$$

Where Z_{arm} is the arm impedance, Z_c is the series impedance connected to the converter, and Z_c' is equivalent impedance between the M2C generated voltage and PCC. The controller structure and the way it was tuned is exactly the same as the previous two cases. Modulus Optimum technique was used for the tuning.

Outer Loop

The outer loop is a P-Q controller in the offshore side and V_{dc}-Q controller on the onshore side. The model and tuning method for P and Q controller is the same as described previously. The major peculiarity of M2C outer control is on the DC bus voltage control. The M2C has variable DC bus capacitance which has a constant (N per leg) number of capacitors connected in series. The DC bus equivalent capacitance of the M2C is given by equation (5.27). After this point, the tuning follows Symmetric Optimum method as ti was done previously.

$$C_{dc,eq} = \frac{3 \cdot C_{cell}}{N} \tag{5.27}$$

5.7 Simulation

Simulation results of the M2C in the case study model is presented in this section.

5.7.1 Controller Performance

The controller performs in a similar manner as the previous two cases, Figures 5.12 and 5.13. The second harmonic component in the capacitor voltage is observed in P and Q plots. Nonetheless, the average tracking performance is good.

5.7.2 Harmonics

In addition to the results on the case study model, harmonic content of terminal voltage using different number of cells will be presented in this section. Harmonic content of the line voltage in MMC is dependent on the type of control, number of cells, and modulation index. First, an open loop control with different number of cells will be presented.

Simulation was performed with the parameters in Table 5.2.

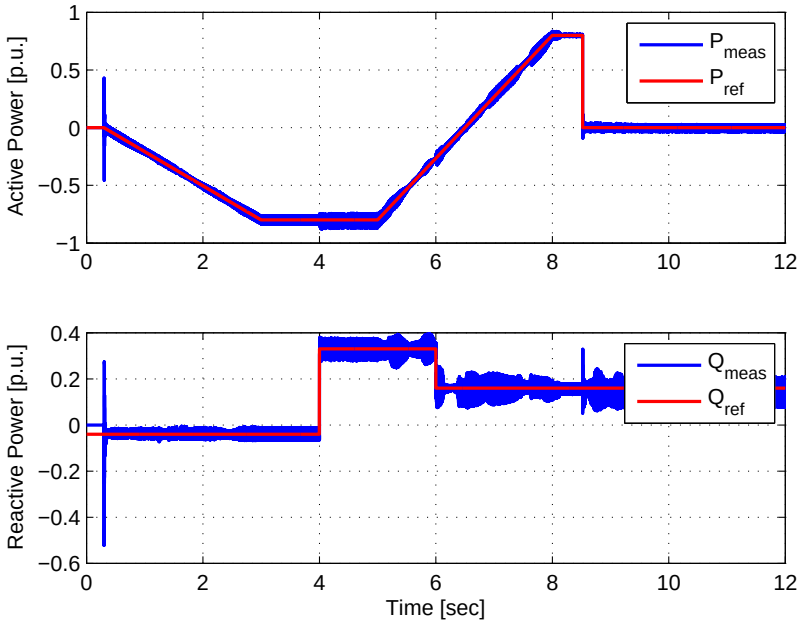


Figure 5.12: *Offshore Active and Reactive Power response, M2C*

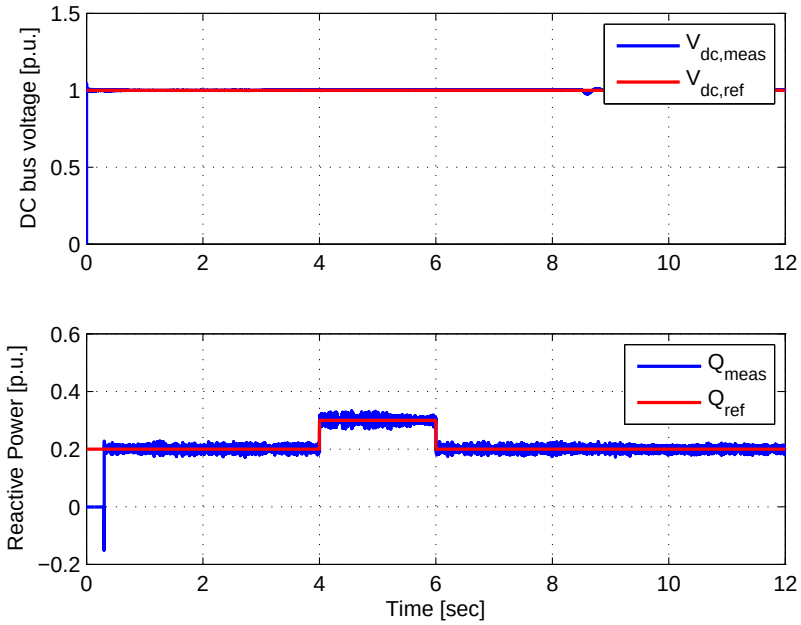
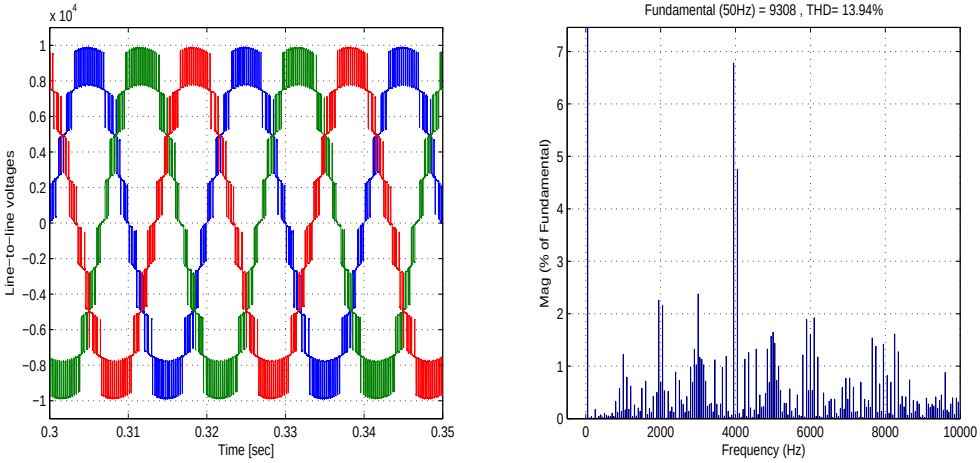


Figure 5.13: *Offshore DC bus voltage and Reactive Power response, M2C*

Parameter	Value
No. of cells	4, 8, 16, 32
Modulation index (phase)	0.57
Switching frequency	2 kHz
DC bus voltage	10 kV
AC side load	4 MW

Table 5.2: *Parameter values for simulation*

Simulation results for the three different number of cells is shown in Figures 5.14, 5.15, 5.16, and 5.17. These results show that the harmonic content in gets lower and lower as the number of cells is increased. This is to be expected since the step size in the voltage is reduced when the number of cells is increased which, in turn, imply that there will be a small error between the desired reference and the generated voltage.

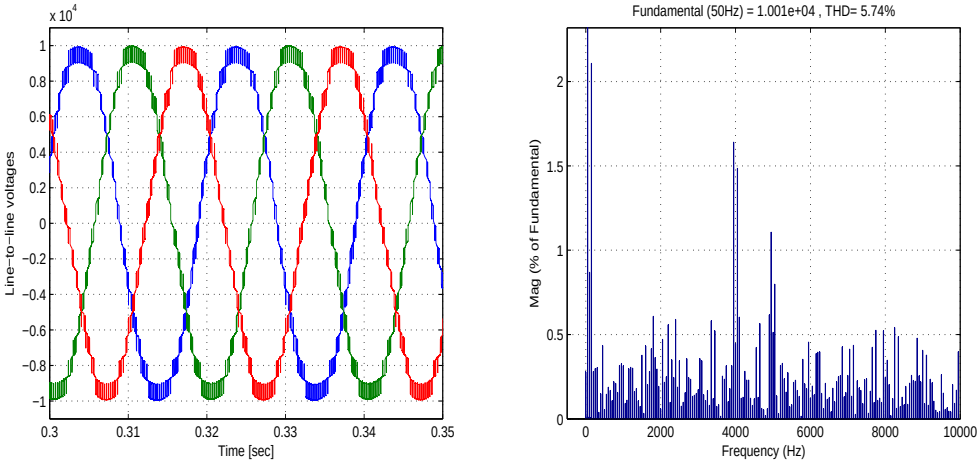


(a) *Line-to-line voltage, 4 cell* ***(b)*** *Harmonic content, 4 cell*

Figure 5.14: *4 cell MMC*

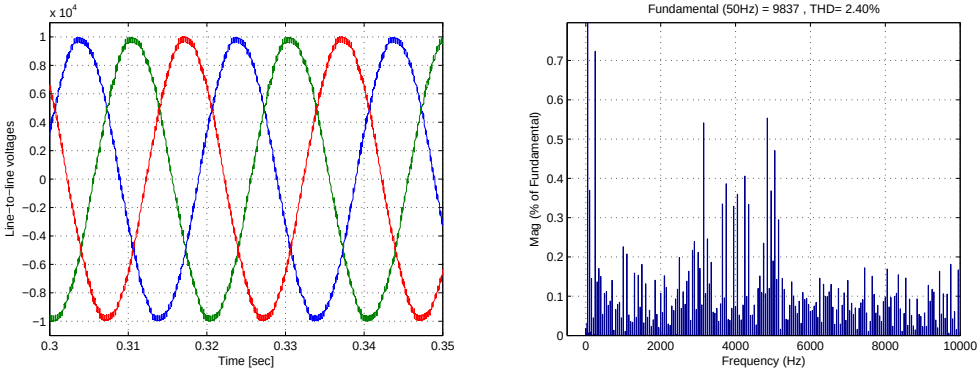
The need for harmonic filters slowly fades away as the number of cells is increased. This is particularly true for the case of 32 cells shown in Figure 5.17.

The results obtained from the case study model are given in what follows. Phase voltage at the terminal of the converter and its harmonic spectrum is shown in Figure 5.18. The voltage looks significantly cleaner than the other cases as indicated



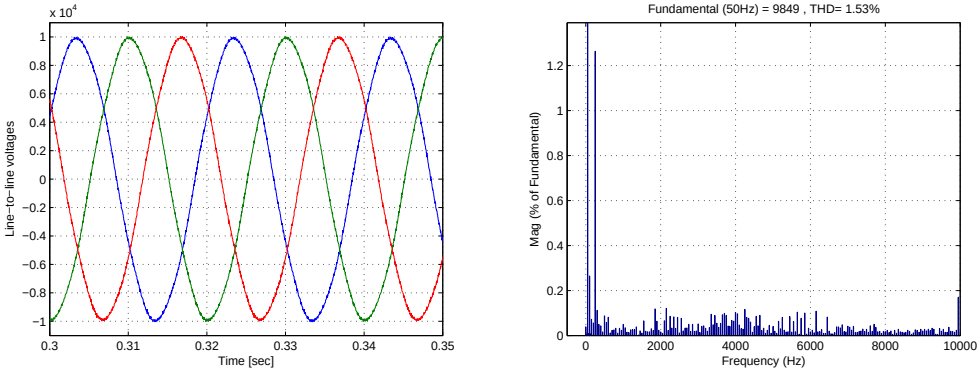
(a) Line-to-line voltage, 8 cell *(b) Harmonic content, 8 cell*

Figure 5.15: *8 cell MMC*



(a) Line-to-line voltage, 16 cell *(b) Harmonic content, 16 cell*

Figure 5.16: *16 cell MMC*



(a) Line-to-line voltage, 32 cell *(b) Harmonic content, 32 cell*

Figure 5.17: *32 cell MMC*

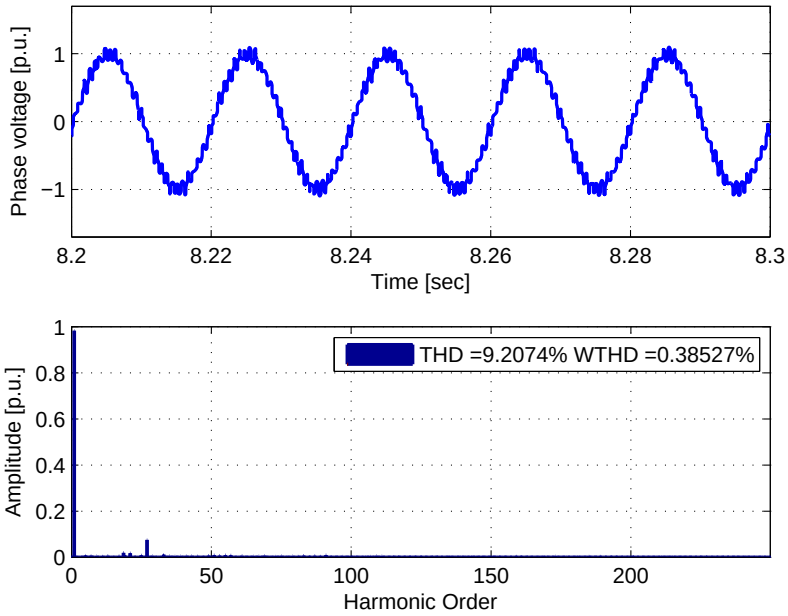


Figure 5.18: *Phase voltage and its harmonic spectrum, M2C*

by THD and WTHD figures.

The current is also very clean, Figure 5.19, as can be predicted from the WTHD.

5.7.3 Losses

Losses under different operating conditions are shown in Figure 5.20. The losses are the lowest of the three and predominantly conduction.

5.7.4 Capacitor Voltages

As previously discussed, the ripple in capacitor voltage contain a second harmonic that has varying phase shift with respect to the fundamental depending on the loading condition. This fact is illustrated in Figures 5.21 and 5.22. The ripple under full active power transfer is 1.1% which is close enough to the design value, 1.0%.

When supplying purely reactive power, the ripple is higher. However, the purpose of the offshore station is to supply full active power supplying local reactive power demand. Therefore, the higher ripple during full reactive power is not a concern.

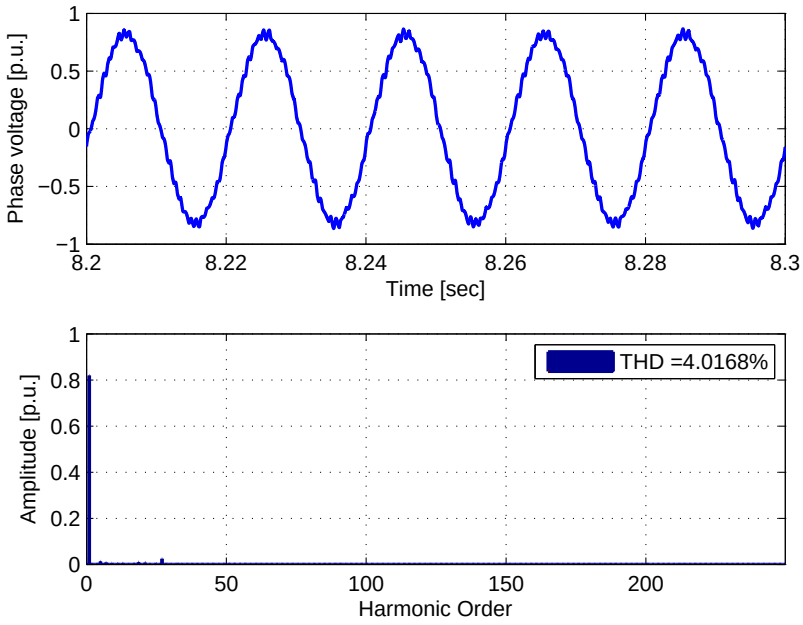


Figure 5.19: *Phase current and its harmonic spectrum, M2C*

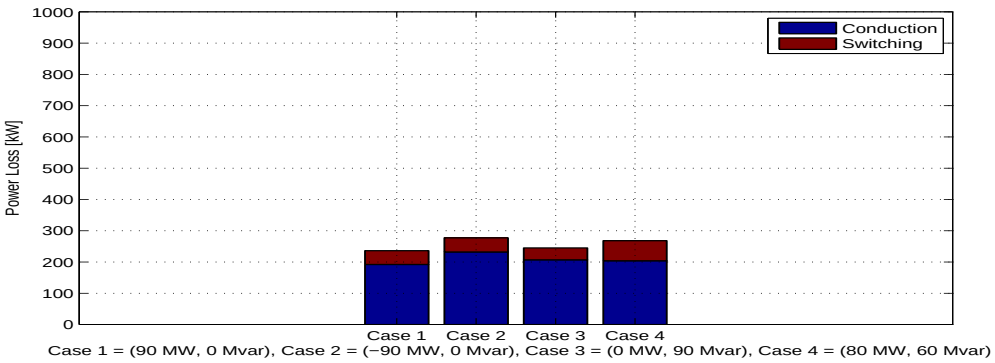
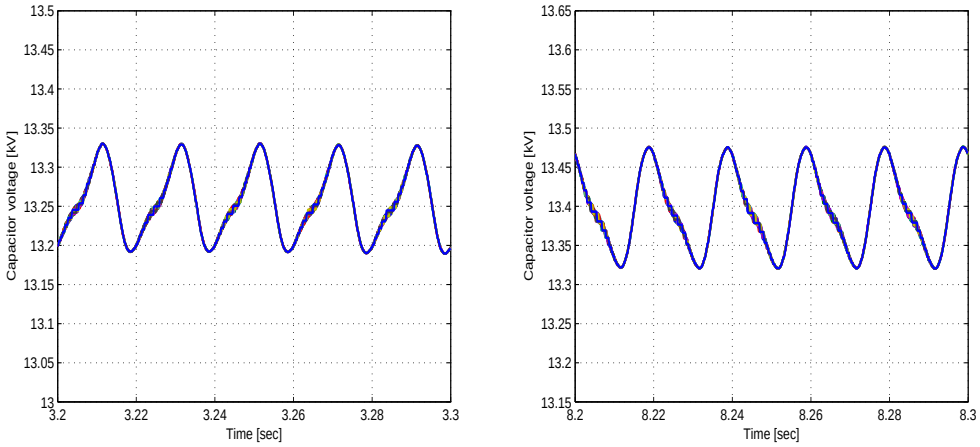
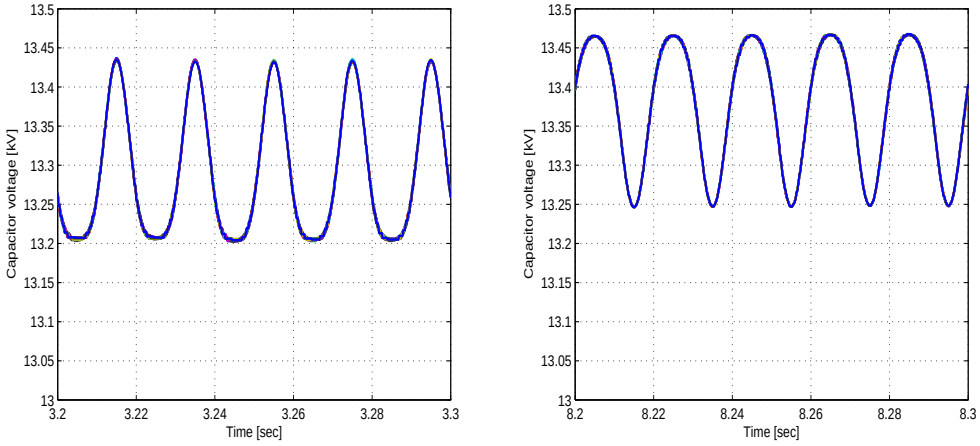


Figure 5.20: *Losses under different conditions, M2C*



(a) $P = 1.0p.u.,\ Q = 0$ ***(b)*** $P = -1.0p.u.,\ Q = 0$

Figure 5.21: *Capacitor voltages when transferring Active Power*



(a) $P = 0, Q = 1.0p.u.$ ***(b)*** $P = 0,\ Q = -1.0p.u.$

Figure 5.22: *Capacitor voltages when transferring Reactive Power*

Chapter 6

Comparison

Comparison of the three converter topologies is the subject of this chapter. Qualitative and quantitative measures of performance are presented in subsequent sections.

Scalability

Present day power system changes very rapidly requiring its components to be easy to up- and down-grade. This implies that scalability is a vital requirement. In two level converter, every component has to be modified to adapt to a new voltage level. This is because the valves are made in a special process where it is desired to have IGBTs from the same production line in the same valve in order to have easy matching. Therefore upgrading would mean replacing the whole valve which is a major drawback. The DC link is also another point where the two level converter suffers. The three level NPC also exhibit similar drawbacks.

The M2C, on the contrary, is very suited for scaling because of its modular design. Adapting to a new, higher, voltage level amounts to simply adding a couple of cells. This is very favorable making the M2C ideal choice.

Availability

Availability, in this context, is used to refers to the converters ability to function in the event of components failure. The two level and three level converters suffer, once again, with respect to availability. This conclusion can be drawn by considering failure of an IGBT in a valve. This would take the whole valve out of service forcing the converter to go offline for maintenance. In the case of M2C, the same failure forces the cell instead of the arm. The failed cell can be bypassed and the remaining cell operate beyond their rating.

Cost

Simple cost analysis is presented in this section. The cost is broken down in to running cost, mainly due to losses, and initial cost, mainly because of number of devices used.

The loss results obtained from simulation showed that the M2C has the lowest loss. The M2C losses can be even lower with higher number of cells where the PWM can be skipped. Advanced modulation techniques, such as optimal PWM [ABB], have been used to lower the losses in two level converter. But, the reduction is not enough to make it better than the M2C.

The number of switches used in M2C is larger than the other converters. However, standard switches can be used in M2C, as opposed to the special valves. This make the switches, and hence the whole converter, cheaper. The analysis in this section is based on rough approximation and detailed analysis is required to make cost comparison of the converters.

Harmonics

Harmonics content of current is a critical grid requirement. Quality of the generated current decides the need for additional filters which have great cost implications. The M2C, clearly, has the upper hand on this aspect. The THD figure decrease with increase in number of modules upto a point where no additional filtering is required.

Two level and three level converter generate current whose THD is reduced by the series reactor. Shunt filters are often required to meet grid requirements.

Other Factors

Besides the factor mentioned above, there are other issues that need to be considered. The first issue is DC side short circuit. In the case of two and three level converters, the DC link capacitance appears directly across the fault aggravating the condition by dissipating its stored energy. In M2C, on the other hand, the energy stored in the capacitor can be bypassed by the auxiliary switch provided in the case of half bridge cell. This avoids risk of explosion and damage of components.

The second issue is related to series connection of IGBTs. The main challenges are simultaneous gating, achieving short circuit failure mode, and insulation. Last but not least is system complexity in which the M2C performs poorly.

Summary

Among the converters considered in this thesis, the M2C is the most promising topology for future HVDC installations. Table 6.1 gives summary of the ongoing comparison. The M2C stands out in may aspects although it suffers a from a challenging and complex control system design. The other major drawback of M2C is ripple in the capacitor voltages which is a topic of research in recent years [Ferreira].

Metric	2 Level	NPC	M2C
Scalability	-	-	++
Availability	-	-	++
Cost	-	-	+
Harmonics	-	+	++
Complexity	++	+	-

Table 6.1: *Summary of comparison of the topologies*

where - implies poor, + indicates good, and ++ means better.

6.1 Industry Experience

To have better idea of where the HVDC industry stands, a brief overview of the industry experience is give in this section. Different VSC based HVDC converter installations were discussed in [5]. These installations were done by the major manufacturers of HVDC converters: ABB, Siemens, and Alstom. The following sections will discuss the different implementations followed by these suppliers.

ABB - HVDC Light®

The first VSC based HVDC converter, Generation 1, was produced by ABB in 1997 [3] with the trade name HVDC Light®. It was a two level converter with high frequency switching. It had higher losses than classic HVDC solutions so, ABB considered options to improve it. This led to Generation 2 which is a three level converter. This generation has lower losses but the cost of additional components was high giving rise to Generation 3 which is, once again, a two level. The loss was reduced by using optimized switching algorithm [3]. This algorithm combines

elements of programmed selective harmonic-elimination PWM and third harmonic injection to significantly reduces system losses [5].

ABB is currently shifting towards the Cascaded Two Level (CTL) converter for its Generation 4 HVDC LIght® [3],[5]. The converter is a modular multilevel converter with half bridge cell. Evolution of losses with generations is shown in Figure 6.1. Operation and control of CTL is described in [46]. The cells are composed of IGBTs with or without series connection.

The Modulation technique used with CTL is phase shifted multilevel SPWM [3] with a typical switching frequency of $150Hz$ [46]. The apparent switching much higher than switching frequency of each cell: specifically, multiplied by the number of sub-modules. This provides good dynamic response at low switching losses.

Control of CTL is organized in two levels: upper and lower [46]. The upper level is responsible for controlling currents and voltages at the arm level. The lower level control, on the other hand, controls cells individually and is responsible for balancing of voltage between each sub-module. The balancing scheme adopted is by adding a balancing component to the modulating reference signal [46].

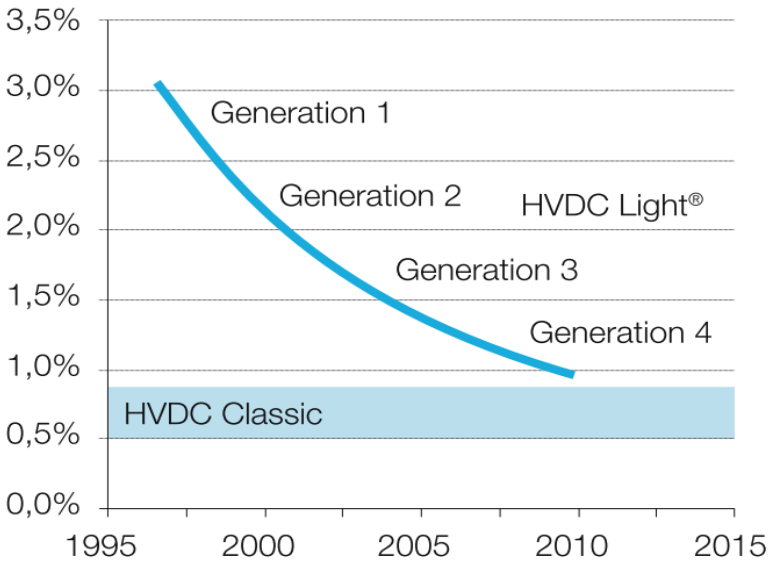


Figure 6.1: *Evolution of HVDC Light® [3]*

Siemens - HVDC PLUS®

Siemens installed the world's first HVDC converter based on M2C, HVDC PLUS®, in 2010 [47]. It's implementations is based on a generic M2C shown in Figure 5.1 with a half bridge sub-module. The modulation scheme is based on insertion and bypassing of sub-modules which results in a staircase waveform [47],[4]. Since many levels are used (typically 200+), the resulting output waveform appears to be virtually sinusoidal eliminating the need for DC and AC filters [5].

The converter is controlled by a central control system, PLUSCONTROL, which handles both upper level and lower level controls discussed in the previous section [4]. The sub-module voltage balancing technique resembles the sorting method described in [30],[2]. PULSCONTROL is equiped with fiber-optic communication link to send gating signals to the sub-modules and feed measurements back to the controller.

The sub-module used in HVDC PLUS® is equipped with bypassing Thyristor, Figure 6.2, that is fired to divert DC side short circuit current from the diode. This will help in avoiding doide failure because of excessive current flow untill the AC side circuit breaker open [4].

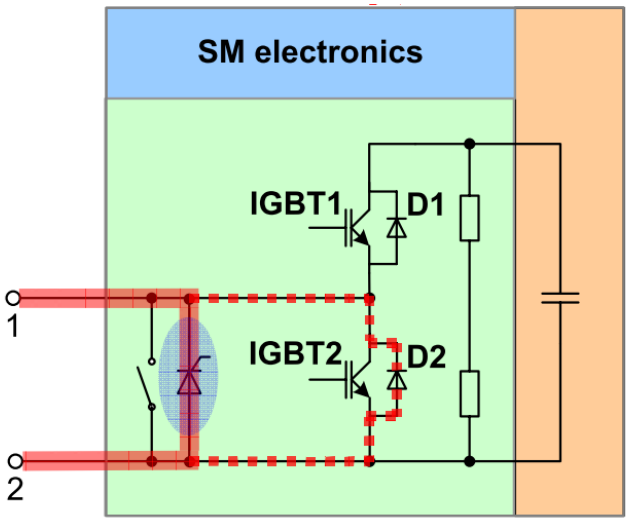


Figure 6.2: *Fault Protection in HVDC PLUS® Sub-module [4]*

Alstom - MaxSine®

Alstom has built HVDC station which is based on M2C with half bridge sub-modules [48]. Alstom is also considering full bridge cells [49]. The full bridge was chosen because of its capability to block DC side fault currents. It is also operated with low switching frequency and hence lower losses.

Figure 6.3 shows summary of major products in the VSC based HVDC market. It can be seen that ABB has done, relatively, many installations with VSCs. But, M2C is still at its early stage with Siemens being the first to install it.

Technology	Year first scheme commissioned	Converter Type	Typical Losses per converter (%)[a]	Switching frequency (Hz)[b]	Example Project
HVDC Light 1st Gen	1997	Two-Level	3	1950	Gotland
HVDC Light 2nd Gen	2000	Three-level Diode NPC	2.2	1500	Eagle Pass
	2002	Three-level Active NPC	1.8	1350	Murraylink
HVDC Light 3rd Gen	2006	Two-Level with OPWM	1.4	1150	Estlink
HVDC Plus	2010	MMC	1	<150*	Trans Bay Cable
HVDC MaxSine	2014	MMC	1	<150*	SuperStation
HVDC Light 4th Gen	2015	CTL	1	=>150*	Dolwin 2[c]

*switching frequency is for a single module/cell.

Figure 6.3: *Evolution of VSC based HVDC Converters [5]*

Chapter 7

Experimental Work

7.1 Objective

The main goals of the experimental work are:

- To understand operation of the M2C in detail and validate some of the theoretical assumptions.
- To investigate practical aspects/challenges of M2C.

7.2 Scope

Although the objective has been specified in the previous section, realistic bounds have to be specified in light of time and resource limitations. Scope of the experiment is limited to modulation, not closed loop control, of 3-cell M2C.

7.3 System Description

The system used in the experiment is described in this section. The system has two components; hardware and software. Each of these components are briefly described in subsequent sections.

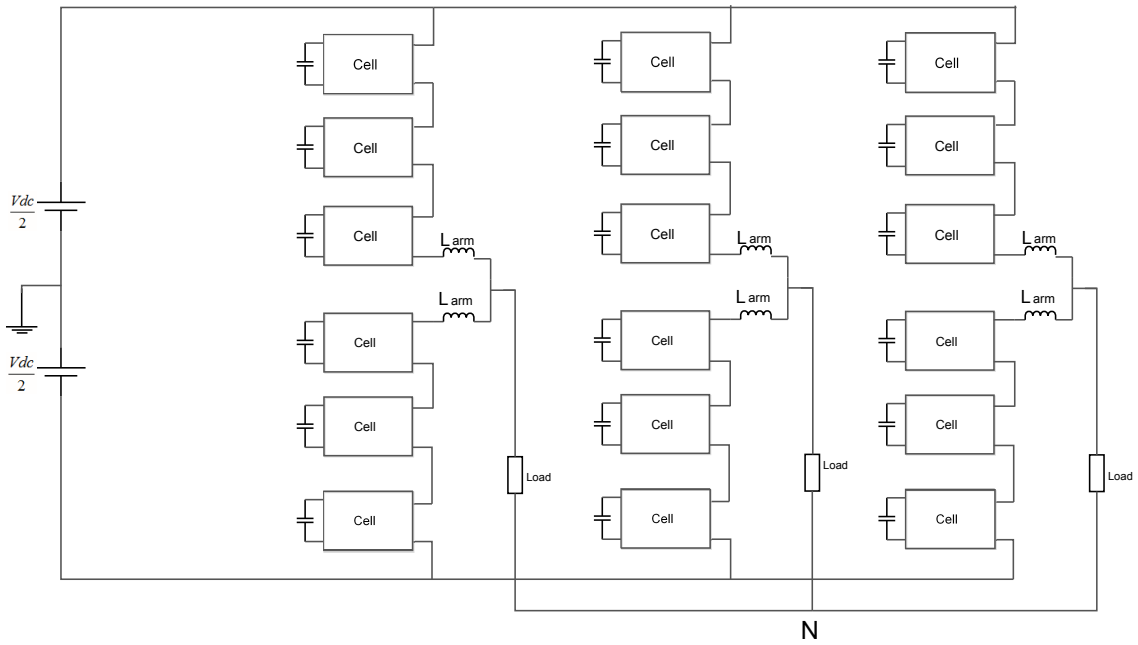


Figure 7.1: *Practical setup of 3 cell M2C converter circuit*

Parameter	Value
Arm Inductance	$1.3mH$
Cell Capacitance	$6800\mu F$

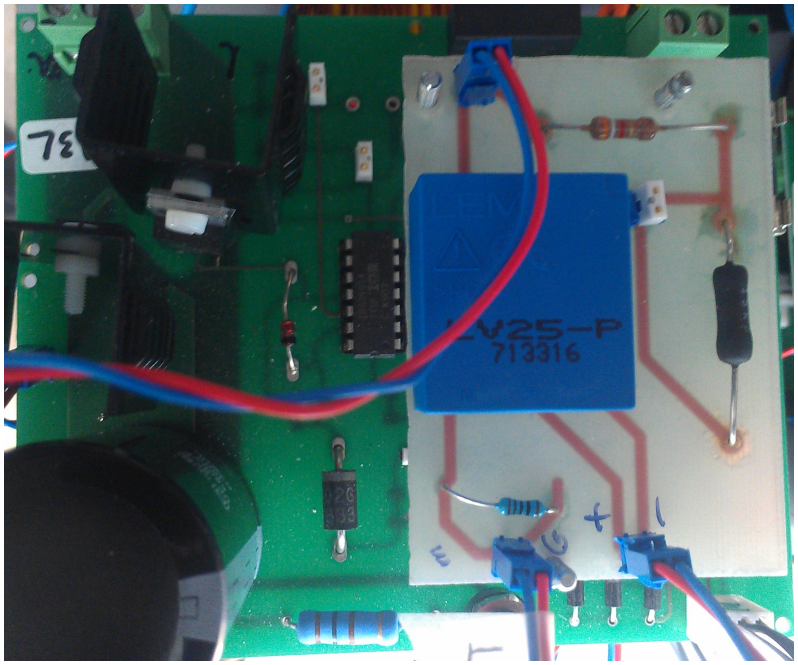
Table 7.1: *Circuit parameters of the converter*

7.3.1 Hardware

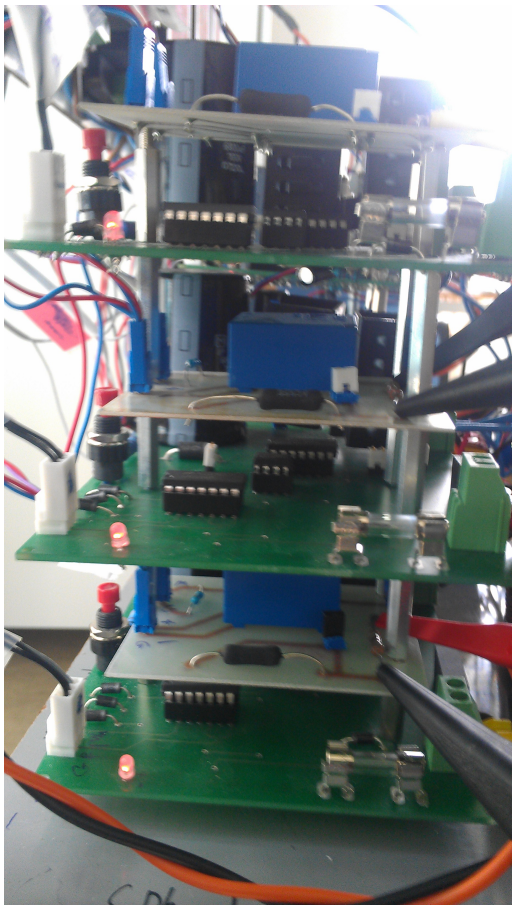
The converter is a 3 cell M2C which is rated for $100V$, $500VA$. The system rating is very far from a realistic HVDC converter. Nonetheless, operation of the converter can be observed and verified against simulation. The converter circuit is shown in Figure 7.1. The circuit parameters are given in Table 7.1.

Each cell in the circuit is composed of a half bridge made of MOSFETs. The cells also contain complementary gate drives and isolated capacitor voltage measurement. Figure 7.2 shows picture of the M2C practical setup.

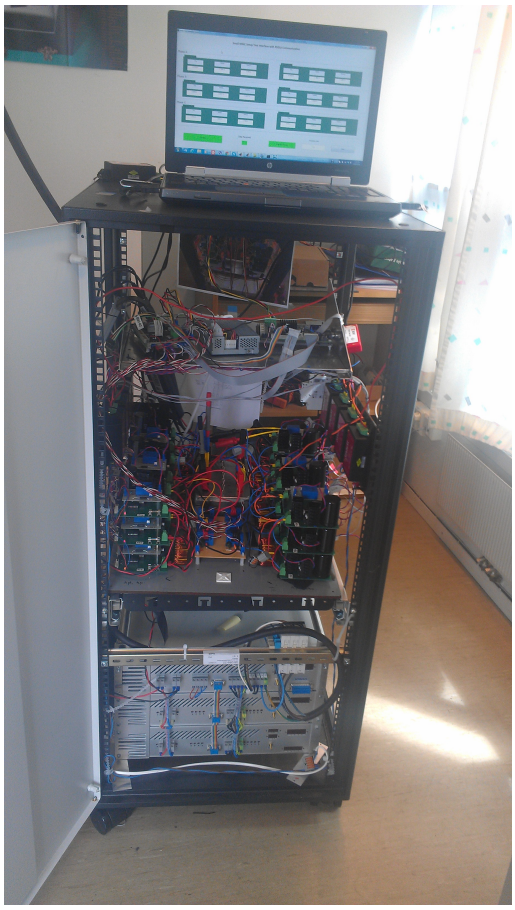
The most important part of the setup, not explicitly shown in the pictures, is the control board. Two control boards, DPS and FPGA, both developed in SINTEF Energi AS, were used in the setup. Role of the FPGA is to expand the IO capability of the DSP board. The two boards were connected via a custom 16-bit parallel interface.



(a) Cell circuit



(b) Arm Circuit



(c) Converter Circuit

Figure 7.2: *Pictures of the experimental setup*

7.3.2 Software

The software has four core building blocks: Main state machine, ADC state machine, Modulator, Communication. Thees blocks will be described in following sections. The software was developed in Simulink® Coder with TI blocksets.

Main State Machine

Main state machine handles operating state of the converter. The converter has three states: Idle, Start-up, and Run. In Idle mode, the converter awaits command from the user while doing nothing. When a Run command is received, the converter state is changed to start-up where the task is to charge the capacitors. Once the capacitor are charged, the state is changed to Run in which the converter supplies power. A stop command put the converter back to Idle state. In case of fault, the converter goes to Idle state. Main state machine is shown in Figure 7.3.

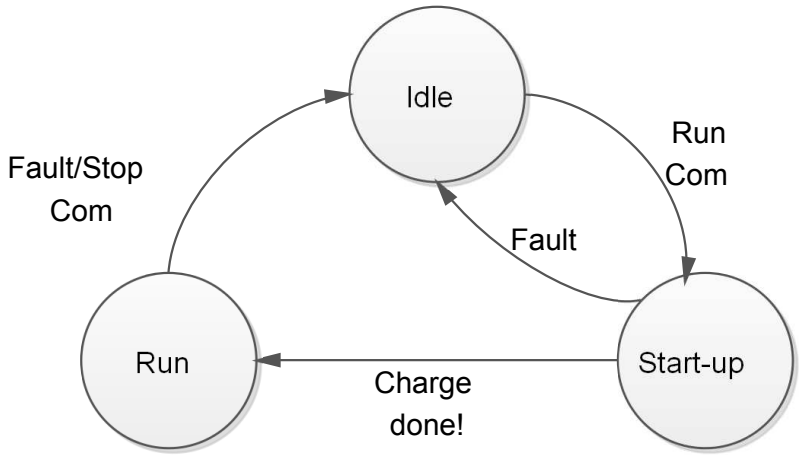


Figure 7.3: *Main state machine*

ADC State Machine

For proper operation the converter, at least 24 measurements are required (18 cell voltages and 6 arm currents). However, the DSP board has only 16 channels out of which 8 are multiplexed. In order to have all the required measurements on every PWM period, the measurements are categorized in to two groups. The first group include the currents and 10 cell voltages. The second group contains the remaining 8 cell voltages. The DPS has the capability to be triggered in synchronously with the PWM module. The first group measurement is triggered by PWM event while the second group is triggered by software at the end of the first measurement.

Modulator

The modulator is Nearest level modulator which was described in previous chapter. Since the DSP is fixed-point processor, every computation is done in fixed-point with fraction length of 25. The first part in the modulator is sinusoidal reference generator which is implemented using lookup table. To make the computation more efficient, one sine and one cosine are generated. Then, the three phase reference is generated as per equation (7.1).

$$\begin{aligned} v_{a,ref} &= \sin(\theta) \\ v_{b,ref} &= \sin(\theta)\cos\left(\frac{-2\pi}{3}\right) + \cos(\theta)\sin\left(\frac{-2\pi}{3}\right) \\ v_{c,ref} &= \sin(\theta)\cos\left(\frac{2\pi}{3}\right) + \cos(\theta)\sin\left(\frac{2\pi}{3}\right) \end{aligned} \tag{7.1}$$

where θ is the angle. These reference are passed to the nearest level modulator.

Communication

The setup has two communication channels: between the two control boards and to the test PC. The communication to FPGA is done to pass state of each cell every control time step. It is implemented using parallel 16 bit interface with custom protocol. The PC communication has two functions; reporting 18 call voltages to PC display every second and sending commands to the converter. This channel is implemented using serial interface. There are three commands that can be entered through the display interface on the PC. The commands are Start/Stop, Modulation index, and enable/disable common mode injection to extend modulation range.

7.4 Simulation Benchmark

To validate the simulation model used in this thesis, model of the experimental setup is run in Simulink. The parameters used in the setup are shown in Table 7.2. Since the voltage and current waveforms depend on the connection to the DC mid point, the simulation results include wavefroms with and without grounded neutral.

Figure 7.4 shows phase voltages when the neutral is grounded. The 4 level output is obvious despite the fact that the voltage drop on the arm inductor made the level look curved. Since the load is resistive, the current follows the voltage waveform, Figure 7.5. For this reason, the current waveform will not be presented for the remaining cases to save space. Triplen harmonics of the voltage waveform are visible in Figure 7.6 because there is a completer circuit for zero sequence current.

Parameter	Value
DC Bus Voltage	$20V$
Number of cells	3
Load	10Ω Resistive
Arm Inductance	$1.3mH$
Cell Capacitance	$6800\mu F$
Switching Frequency	$5kHz$

Table 7.2: *parameters of the Test Setup, Simulation*

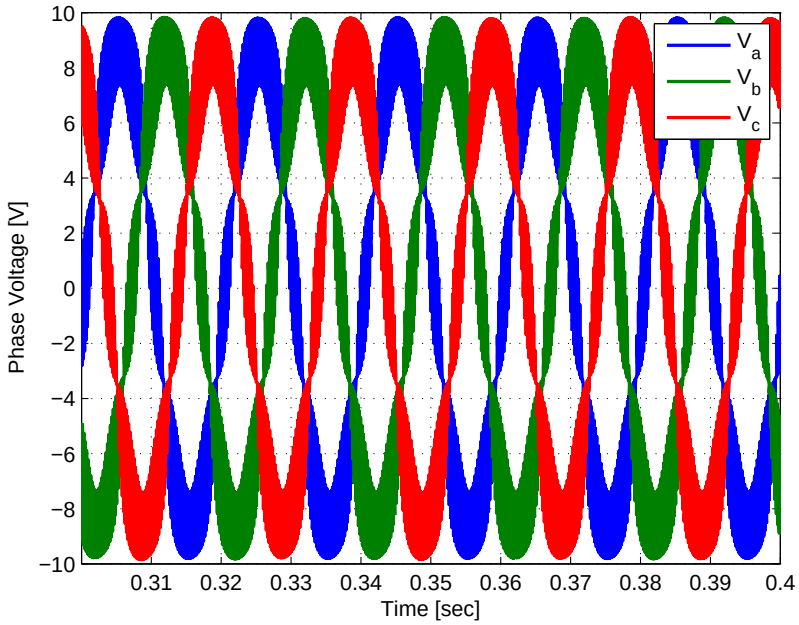


Figure 7.4: *Three phase voltages with grounded neutral, Simulations*

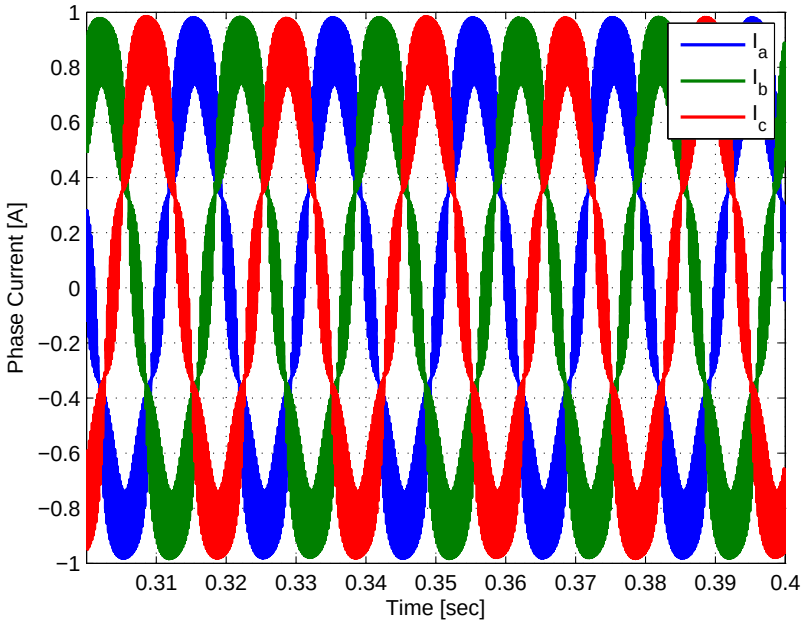


Figure 7.5: *Three phase Currents with grounded neutral, Simulations*

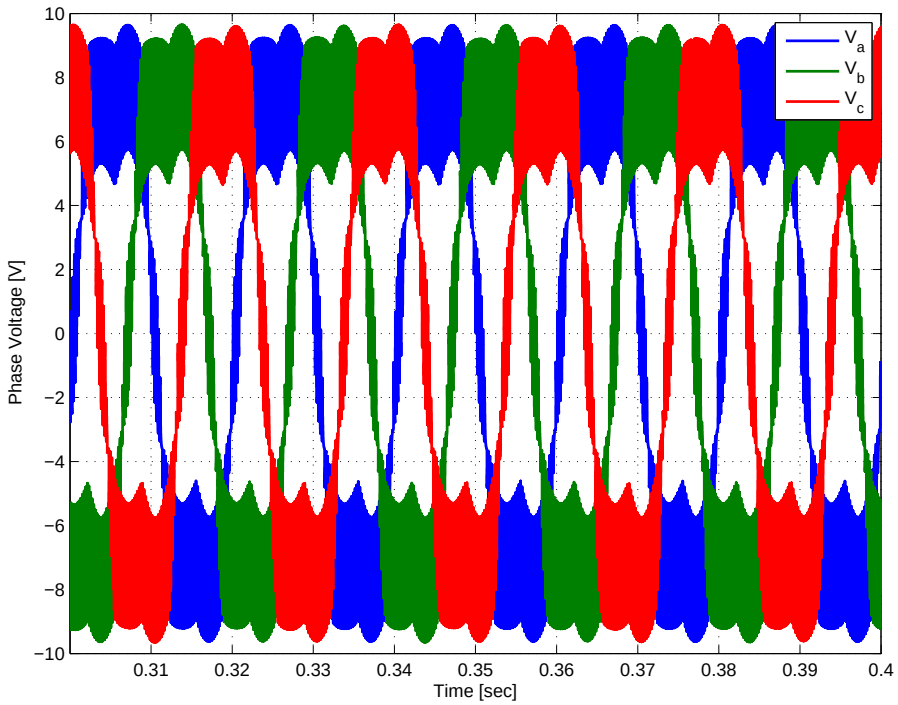


Figure 7.6: *Three phase voltages with grounded neutral and Harmonic injection, Simulations*

When the load side neutral is left floating, the voltage becomes cleaner with more levels. This is because there are not triplen harmonics and the neutral voltage is a multilevel voltage, Figure 7.8, resulting in more number of levels.

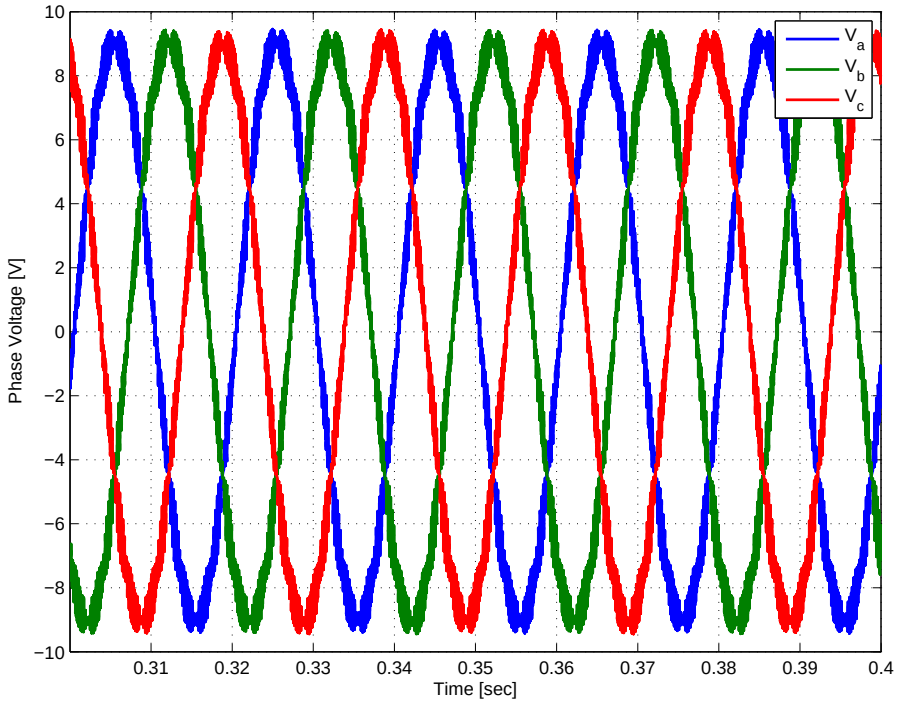


Figure 7.7: *Three phase voltages with out grounded neutral, Simulations*

Capacitor voltages are balanced with the sorting algorithm. The result is shown in Figure 7.9. Each capacitor deviates from the group over a portion of the cycle because phase current, instead of arm current, used for sorting. The situation can be rectified by using arm current.

7.5 Experimental Results

The results presented in this section closely follow the ones in the previous section in order to have a clear validation of the model. Figures 7.12 to 7.13 were taken from the experimental setup. These waveforms are in good agreement with the simulated result in the previous section.

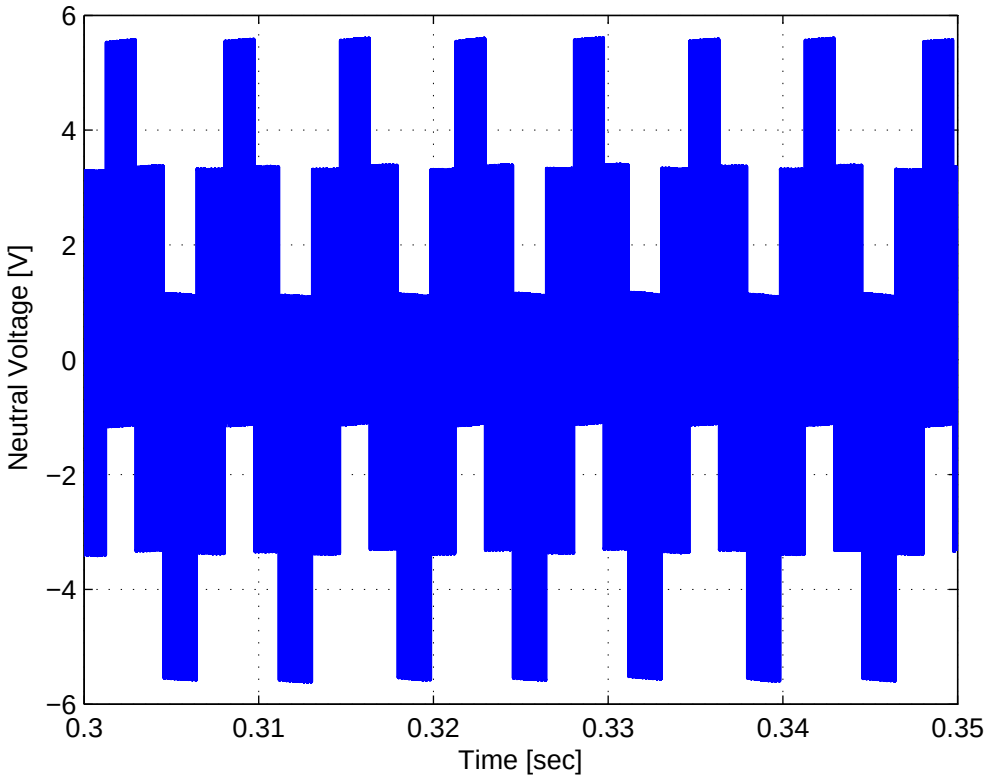


Figure 7.8: *Neutral voltage referred to DC mid point, Simulations*

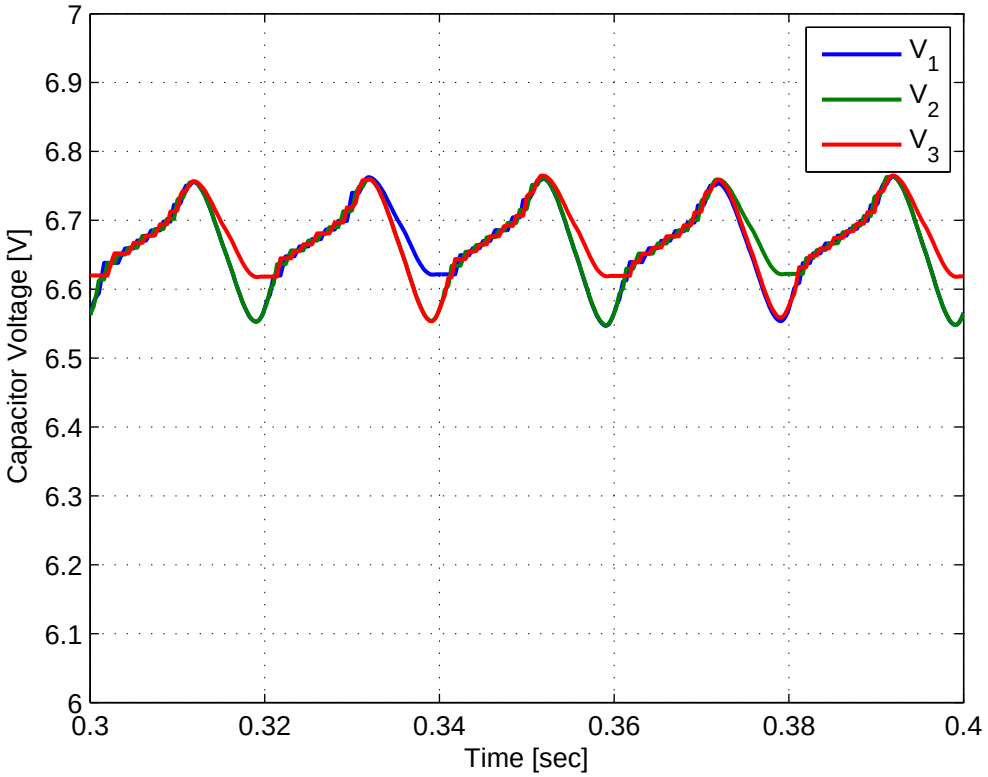
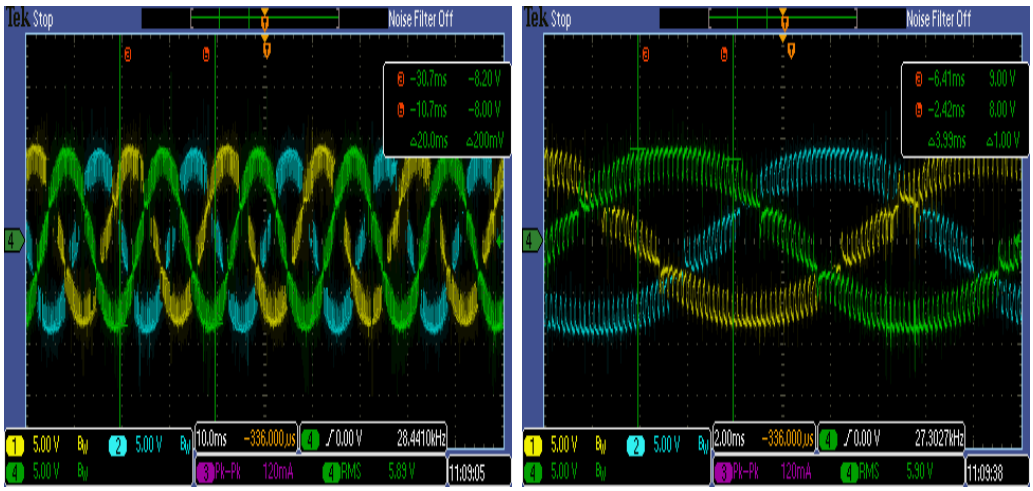


Figure 7.9: *Capacitor voltages, Simulations*



(a) ***(b)*** *Zoomed*

Figure 7.10: *Three phase Currents with grounded neutral, Experiment*

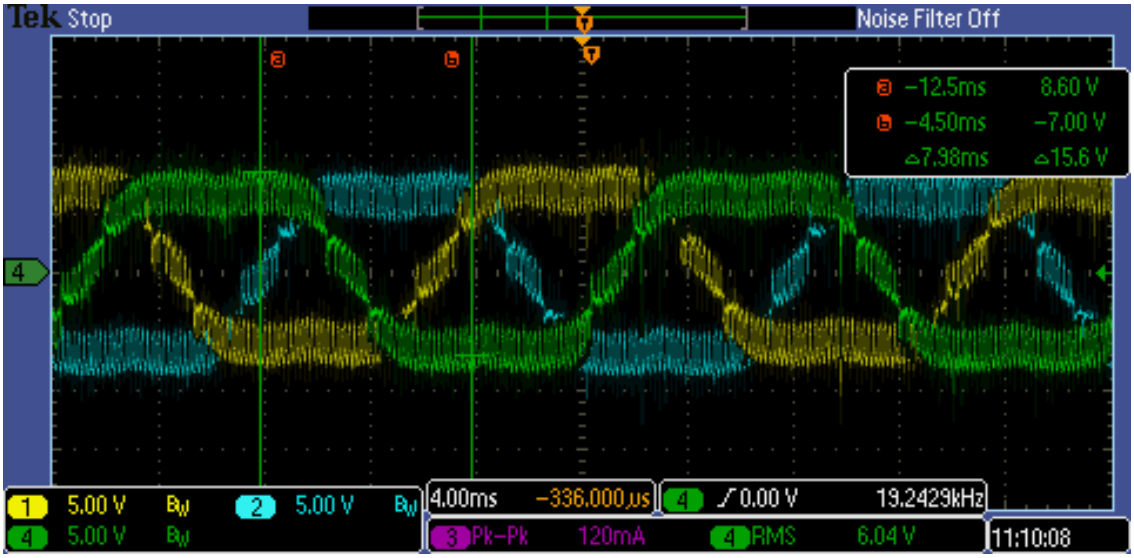
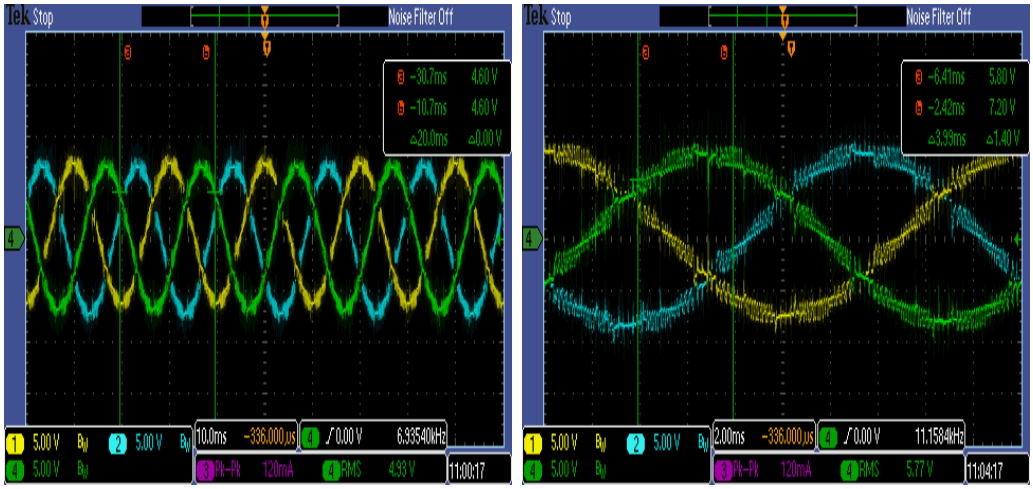


Figure 7.11: *Three phase voltages with grounded neutral and Harmonic injection, Experiment*



(a) ***(b)*** *Zoomed*

Figure 7.12: *Three phase Currents without grounded neutral, Experiment*

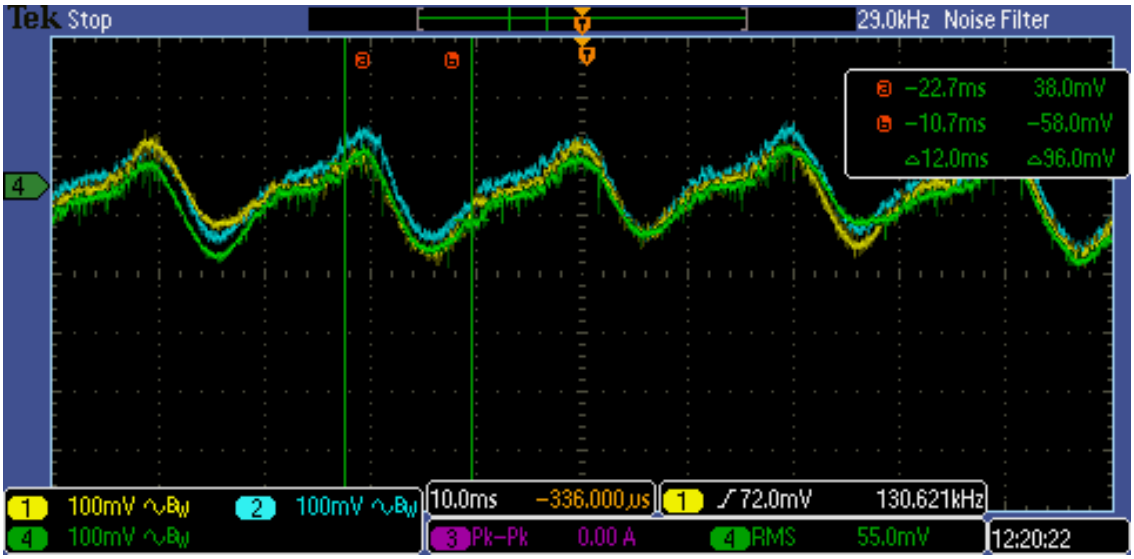


Figure 7.13: *Capacitor voltages, Experiment*

Chapter 8

Conclusion and Future Work

From the analysis and simulation results obtained in this thesis, it can be conculded that the M2C is the converter of choice for future offshore HVDC installation. This statement is, however, drawn from a technical point of view. Other converters might prove to be economically viable depending on particular needs of the installation. To make this work more complete, the following task might be undertaken in the future.

- Implement more advance control techniques to each of the topologies
- Build a prototype with a higher power rating this can be used verify the efficiency calculation done in this thesis.
- Include different cell implementations for the M2C
- Extend the efficiency calculation the the whole HVDC system.
- On the experimental setup, implementation of closed loop control. This was differed due to unavailability of sufficient analog inputs on the control board.

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