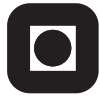


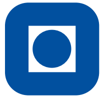
NTNU – Trondheim
Norwegian University of
Science and Technology

Analyzing and Testing of New Silicon Carbide Components for Down Hole Oil Applications

Xiaoxia Yang

Master of Science in Electric Power Engineering
Submission date: July 2014
Supervisor: Tore Marvin Undeland, ELKRAFT
Co-supervisor: Richard Lund, SmartMotor AS.

Norwegian University of Science and Technology
Department of Electric Power Engineering



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Problem Description

High ambient temperature is one of the challenges for operating power converters in down hole oil exploitation activities. Switching devices are important parts of power converters. Due to material limitation, the traditional silicon power device can only work up to 150 °C, which further limits the available depth of an oil well. Whereas, the increased oil consumption means exploiting more oil from deeper oil reservoirs. Consequently, the operation ambient temperature of power converter may exceed 150 °C or higher. SiC (Silicon Carbide) technology becomes one of the possible solution for high temperature power converters.

The main properties of SiC include: wide bandwidth, high critical breakdown electrical field and high thermal conductivity, which make it can theoretically work at 600 °C junction temperature without performance various. Commercial SiC power devices started to be available from 2001, and keep developing in power electronic markets. The first commercial power module manufactured by CREE Inc. in 2011 was a six-pack, three phase SiC MOSFET power module, with rated operating junction temperature 150 °C. High temperature over 150 °C can be achieved by advanced packaging technology. Nevertheless, SiC is not a mature technology compared to its Si corresponding, verifications should be done properly to ensure the reliable performance of SiC based applications.

In this thesis work, a power converter board with new SiC MOSFET power semiconductors which will be provided by SmartMotor is to be analyzed and tested. Simulation work is to be realized with LTspice software. Components for the simulations may be difficult to obtain in LTspice, and models for components which are close could be used. Gate drivers are important, and the candidate should be developed and tested including the dead times. Besides, commercial drivers should be included. The gate driver schematics, PCB (Printed Circuit Board) layout design should be realized with CadSoft EAGLE PCB design Software. A CCS050M12CM2 3-phase SiC MOSFET power module from CREE is to be used for the power converter. SiC MOSFET overcurrent protection has to be designed and implemented. The DPT (Dual Pulse Test) provides inductive testing of turn-on and turn-off with controlled current and junction temperature. It should be tested on both single MOSFET in the power module and on paralleled devices. The possible voltage or current oscillations and ringing might be observed in the laboratory work. If this is the case, the corresponding analyst and improved solutions should be implemented.

If there is enough time, testing of the module in some converter configurations could be done.

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Abstract

High temperature power converter becomes possible due to the development of SiC power technology. The inherent properties of wide bandwidth, high breakdown electrical field and high thermal conductivity give commercially available SiC power devices up to $150\,^{\circ}\mathrm{C}$ operational junction temperature. However, due to immature of the SiC technology, the laboratory verification tests have to be done for SiC technology based power converter design.

In this thesis work, a bridge leg gate driver has been designed with 700 ns dead time and reliable 20 V and -5 V gate driver voltages for on and off state separately. Digital overcurrent protection has been implemented to protect SiC power module during DPT (Dual Pulse Test). The PCB (Power Circuit Board) was provided by SmartMotor AS. The initial laboratory tests contained significantly voltage and current oscillations and ringing. The reasons were diagnosed as the parasitic elements. An improved waveform has been achieved by adding damping gate resistor, which resulted in slow switching speed. Furthermore, the stray capacitance which was due to the parallel configuration of SiC MOSFETs slowed down the turn-off speed. The more significant slow-down influences were observed at smaller drain current conditions.

To finalize clean switching voltage and current waveforms, a minimized parasitic elements configuration has to be first realized. But there was not enough time to arrange a new improved design. All the measurement results had been done on the un-optimized power converter configuration, but with improved measurement instruments. The thesis work had also implemented DPTs with different drain current levels under voltage 300 V and 500 V separately.

Preface

This master thesis project has been continuously cooperated with SmartMotor AS, Norge after my summer job and specialization project in 2013. The report also documented my final year of study in NTNU (Norges teknisk-naturvitenskapelige universitet) during the school year 2013-2014.

It has been a really challenging experience as a novice into power electronics. However, when looked back, I did work hard and learn a lot both in theoretical knowledge and practical skills. It also turned out to be a process of experiencing the western cultures with equality, care and risk-taking. The experience has strongly come into my mind, especially when I was struggling with the laboratory work within no more than one month to the deadline.

Now, it is at the end of my master thesis work, what in my mind is so much grateful to the people who helped me all the way around. First of all I would like to thank my supervisor Prof. Tore M. Undeland for all his help, encouragement and support. He also deserve my special appreciation for the opportunity of presenting part of my thesis work on his retirement seminar. Dr. Richard Lund from SmartMotor AS has been my supervisor since my summer job. Especially, in the final semester, he kept meeting me through Internet or in person each week. Thanks for his time, patient and throughout explanations. I would like to also give my acknowledgment to Bård Almås as my lab-supervisor. He has spent so much time to help me with looking for suitable instruments, giving me suggestions with the unfitted power module connection, and doing some of the challenging soldering work. Without his generous help I would not able to finish my lab work within one month.

A special thanks to Dr. Supratim Basu from India, he spent one Sunday in the Lab to guide me with lab work. Thanks for his generous sharing of his wonderful knowledge and experience.

There are so much thanks in my heart to be spoke out to people who have helped me. Vladimir and Aksel from NTNU - Elkraft service lab. My classmate Kristian who spent his time on checking my grammar mistakes. Also, thanks to Krishna, Abel they have kindly shared their lab experience all the time.

The final but never be last thanks I want give to my husband Yuwer Fei, thanks for all what he has done to encourage and support me for the time we have started to know each other, especially these two years of my master education.

Xiaoxia Yang
Stavanger, Norge, July, 2014

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Chapter 1

Introduction

1.1 Background

1.1.1 High Temperature Power Converters

Power electronics are one of the important technologies. It is estimated that in developed countries, around 60% of the electric energy will go through some kind of power electronics converters before its final usage. The power electronic devices cover a lot of fields, which include: industry, transportation, utility system, space technology and many other areas.

Power electronics have been contributing to energy savings due to the better performance in both power supply and electric control. These advantages become more prominent as the power electronics technology is advanced.

Consequently, the development of new wide energy gap semiconductor materials, such as Silicon Carbide (SiC), will significantly extends the benefits of the power electronic devices. Comparing to Silicon, SiC has the properties of wide bandwidth, high critical breakdown electrical field and high thermal conductivity. These advantages give SiC devices the properties of high blocking voltage, small power losses, high operational junction temperature. Correspondingly, It will benefit the SiC based power converter in the same manners. In addition, the reduced switching power losses allow high frequency operation. It helps to reduce the overall system cost.

1.1.2 Power Converters for Down Hole Applications

The requirements for deep oil extraction applications are quiet challenging: most of the system are expected to run continuously at high ambient temperature for at least five years without much thermal cycling. In addition, it has a high level regulation on reliability which is due to the high cost of the downtime and the difficulties of repairing a down hole machine.

Traditionally, the down hole actuator system is based on hydraulic technology. Electronics has been limited to monitoring and logging functions. However, to reduce the complexity of hydraulic system and meet the demand of increasing oil well productivity the technology is developing towards pure electrical solutions. Power converters will be commonly used in power supplies and actuator control, in a distributed fashion [2]. It requires the power converter to be located as close as possible to the down hole applications.

The first serious challenge for down hole power converters will be high temperature. As known, the earth temperature increases with the application depth. The geothermal gradient averages from 25 to $30\,°\mathrm{C}/km$. The down hole temperature is calculated by adding the surface temperature to the product of the depth and the geothermal gradient [3]. In addition, oil reservoirs with higher depths are being planned to be exploited. According to [4], the average depth of exploratory and development oil wells has reached to 5.964 km in 2008. In some severe condition, the temperature may exceed $180\,°\mathrm{C}$. Limited space if the other critical factor of down hole power converters.

Consequently, SiC power converters are one of the emerging solutions for down hole oil applications. However, SiC-based power converter technology is not as mature as the Si-based power applications, verifications should be done properly to ensure reliable performance.

1.2 Objectives

The objectives of this thesis work are exploring the SiC power converters which is mainly studied on CREE's SiC SMOFET power module.

It includes:
Grasping the knowledge of power converter design;
Learning LTspice - power electronics design software;
Studying Cadsoft EAGLE - printed circuit board design software;
Learning laboratory test and measurement skills.

1.3 Scope of Work

This master thesis work is the first stage of the high temperature power converter design for down hole oil applications, which is cooperated with SmartMotor AS. The scope of this thesis work include:

1. Bridge Leg Gate Driver Design
   It contains circuit design, simulation, PCB (Printed Circuit Board) design, and components soldering. The requirements of the gate driver are:
   (a) Appropriate dead time for complementary controlled SiC MOSFETs.
   (b) 20 V on and -5 V off gate source voltage.
   (c) Flexibility of gate configurations.
2. Overcurrent Protection Circuit
   Fast digital overcurrent protection circuit would be designed for DPTs (Dual Pulse Tests), which requires the accurate response.
3. Laboratory Test and Measurement
   (a) Construct the lab setup.
   (b) Results analysis and problem solving.

1.4 Limitations

1.4.1 Discrete Passive Components

High temperature down hole converter design on the other hand is a systematic work. The high temperature discrete passive components and compatible gate driver might be the limitation factors. For example, high temperature inductor, capacitor which can reliably work up to 150 °C are not commercially available in the power converter level. In addition, high temperature gate driver hasn't been developed for SiC MOSFET devices.

1.4.2 Packaging Limitation

The maximum operational junction temperature of the SiC devices has be limited by the current packaging technology. In this thesis work, the used CREE's CCS050M12CM2 SiC MOSFET power module has the maximum junction temperature 150 °C. Except the packaging technology limitation, the theoretical available temperature is up to 600 °C.

In addition, high pressure, serous vibration and more other conditions have to be carefully dealt with before the power converter is applied into use.

However, it is not a one step affair for the target power converter design. For this thesis work, the task has been defined to explore the high temperature properties of SiC power components - the switching devices of the power converter.

1.5 Report Outline

The report would be arranged in the following manner:

Chapter 1:	Background introduction.
Chapter 2:	Introduction of the SiC power electronics development in general.
Chapter 3:	Theories of some power converter configurations.
Chapter 4:	Bridge Leg gate driver design.
Chapter 5:	Introduction of SiC Power Circuit Board design.
Chapter 6:	Description of laboratory setup.
Chapter 7:	LTspice simulation for SiC MOSFET dual pulse tests and overcurrent protection design.
Chapter 8:	Laboratory work documentations.
Chapter 9:	Conclusion and Scope of the future work.

Chapter 2

Power Electronics Development

Power electronics are used to control or convert electrical power. This technology covers a wide spectrum of electronic converters [5] and has broad energy processing range. In consumer electronics, AC/DC rectifier is the most typically used power electronics device. The power range is from tens of watts to several hundreds watts. Whereas in the industry, AC/AC, AC/DC and DC/AC power converters are commonly used, the power ranges can spread from a few hundred watts to tens of megawatts.

The core elements of the power converters are semiconductor devices, i.e. the switching components [5]. They are the dominant factors for power rating and switching frequency of a power converter system.

2.1 Development of Power Electronics Devices

Switching power electronics development can be divided into two different stages according to the main power device materials, which are Silicon (Si) and Silicon Carbide (SiC).

2.1.1 Si Devices

Mercury-arc valves were dominated in power conversion before Si power devices were developed. It was first invented in 1902, and used as the primary method of high power rectification into 1970s.

The era of power electronics dominated by to silicon semiconductor devices started from the late 1950s when the first silicon based thyristor was invented. In this era, three generations of silicon based power devices have been developed.

- 1956-1975 is considered as the period of first generation of semiconductor power devices. Thyristor technology is dominating in this field.
- 1975-1990 was the time for second generation power devices. Transistors become the primary developed technology. The metal-oxide semiconductor field-effect transistors(MOSFETs), npn and pnp bipolar transistors (BJTs) and gate turn-off thyristors (GTO) were investigated in this period. The microprocessor and specified integral circuits and power integral circuit (such as power modules) were produced as well.
- In the 1990s, it was established insulated gate bipolar transistor(IGBT) as the third generation power switch.

During this period, all known Si switching devices are invented and developed. Silicon based power electronics became an independent subject and research field. With decades of development, silicon power electronics became the mature technology in electrical engineering.

2.1.2 SiC Devices

It is estimated that the next era of power electronics will be dominant by silicon carbide (SiC) semiconductor based. The year 2005 has even been marked as the year of SiC [6]. However, this was not the very beginning of SiC power device. The history from SiC material to finalized SiC power devices has a long history. The first natural crystal of SiC was discovered in 1905. In 1995, the first SiC semiconductor crystal was produced. In 2001, the first SiC diode was manufactured. The evolution of SiC semiconductor devices after late 1950s can be considered as followed several stages [6].

- The First Stage
  It began in 1955 when a new high quality SiC crystal growing concept was presented by Lely. At that stage, SiC was considered as the most brightest semiconductor material compared to Si and Ge. However, due to the technology defect of making SiC wafer, and the rapidly increased Si technology, SiC lost it its popularity.

- The Second Stage
  Even though the semiconductor technology and markets were dominated by Si technology since 1960s, the development of SiC material were still continuing. A developmental milestone was the discovery of making purity SiC wafer in 1978.

- The Third Stage
  The stage started with the ”step-controlled epitaxy” method which performs the high quality epitaxy at low temperature on off-axis substrates [7]. The main progress in this stage was on the improvement of wafer diameter and quality.
  A few companies started to emerged with this technology, Such as CREE. It manufactured the first blue SiC LED and began to sell SiC wafers in 1989.

- The Forth-Ongoing Stage
  In 2001, the first manufactured CREE SiC diode started this stage. it also marked the beginning of the latest wave in SiC evolution [6]. Infineon has launched its Schottky diode product line. More and more SiC power devices such as SiC JFET, MOSFET and "All SiC" FET power modules become commercially available and have hit the marketplace.
  In this stage, the SiC technology has basically three branches. One of them is the continuous development of the wafer technology, which still focus on increasing the wafer diameters and quality. The second is the research and development of the SiC semiconductor devices to attain higher power rating and frequency available devices. The third branch focuses on the application of SiC power devices, such as power converters which used in power supply and control applications.

2.2 Commercially Available SiC Power Devices

SiC technology is continuously being developed in the last decades. SiC as a semiconductor material has unique advantages in high power and high temperature applications. Table 2.1 [8, 9] lists a few main properties comparison of Si and SiC materials.

Compared to Si, the roughly ten times higher critical breakdown electric field of 4H-SiC material gives approximately three orders of magnitude improvement of the on-resistance for a given blocking voltage. The smaller device size can also be achieved for a certain voltage rating due to the high critical breakdown electrical field property. The wider bandwidth and higher thermal conductivity give the possibility of high temperature operation. To fully implemented these advantages, extensive amount of effort has been invested in demonstrating and commercializing SiC devices for power electronic applications [10].

Table 2.1: Physical Properties of Si and SiC materials

Property		Si	3C-SiC	4H-SiC	6H-SiC
$E_g(ev)$	bandgap	1.11	2.2	3.26	2.86
$\lambda(W/cm\,^{\circ}\mathrm{C})$	Thermal conductivity	1.5	4.9	2.7	4.9
$E_B(V/cm) * 10^6$	Break down voltage	0.3	3	3	4
ε_c	Relative dielectric constant	111.8	9.66	9.7	9.7
$V_{sat}(cm/s) * 10^7$	Saturation velocity	1	2.5	2	2
μ_n	Electron mobility	1350	1000	900	500

With the continuous research and development, the SiC power semiconductor industry has matured to a point. SiC industries' market penetration has surprised even the industry analysts from IMS and Yole [11]. It has also been commonly agreed by the industry and researchers that the 150 mm diameter wafer will scale up the volume of SiC power

semiconductor industry. There are two reasons behind. First, the increased wafer size will improve the SiC device productivity but with a decreased cost. Second, the increased system efficiency and switching frequency will lead to a cost-effective SiC power electronics system. In addition, the gradually proved high quality performances of SiC devices and their corresponding applications are also one of the reasons for the scaled up SiC utilization.

2.2.1 SiC Diode

The world first SiC power devices were Silicon Carbide Schottky Barrier Diode (SBD). It was studied as early as 1974 [12], and first commercially available in 2001. SiC SBDs with break down voltage higher than 10 kV have been reported [13]. In addition, SiC Merged P-i-N Schottky diode (MPS) and SiC Junction Barrier Schottky (JBS) diode technologies and products have been extensively investigated as well.

SiC diodes have taken a big stake of the SiC power devices market in 2010. According to Yole and IMS analysts, the SiC power device market had over 100 million dollars, and which was primary for SiC diode. The SiC diode technology is continuing to mature rapidly, there are 100 different SiC diode part numbers on the market [11] from Infineon, Cree, Rohm and others. These products have a wide specification spectrum: breakdown voltage available rating from 600 V to 1.7 kV, current rating from 1 A to 50 A, and a wide assortment of package options - through hole, ceramic, bare die and surface mount.

SiC SBCs are commonly used in kilowatt range power converters. The features of this type diodes are [14]:

- Zero reverse recovery
- Zero forward recovery
- High frequency operation
- Temperature independent switching behavior
- Extremely fast switching
- Positive temperature coefficient on V_F

With these advantages, the limitation of reverse recover times has been avoided which is about 50 ns to 100 ns for the fastest Si power diodes in 600 V to 1.2 kV voltage range. In [15], it reported that a reduction factor $2 - 6$ of switches energy can be realized by using SiC diodes. Furthermore, the switching speed of the power circuit has be improved by SiC diode. Conventionally, Si diode is the limitation factor which has slower speed than most the power switches [10]. Besides, the high temperature capability of SiC diode together with SiC switches offers the possibility of producing high temperature tolerant power converters.

Taking reliability into consideration, SiC diodes is also a great candidate compared to Si diodes. In [16], it pointed out that Cree's SiC diodes have a failure in time rate that is less than 0.5 per billion operation hours. Infineon's second generation schottky diode are

reported that the failure rate is less than 0.15 ppm [17].

To conclude, the market of SiC diode keeps on expanding, especially in the conditions when high power level, fast switching frequency, smaller size, high temperature and high reliability power applications are required.

2.2.2 SiC MOSFET

In 2011, CREE released the industry's first commercial SiC power MOSFET, which is destined to replace its Si corresponding devices in high-voltage ($\geqslant 400\ V$) power electronics [18]. This type of SiC MOSFETs have voltage rating 1200 V and maximum current rating 50 A . It has the on-resistance of 80-160 $m\Omega$, junction temperature tolerance of $125\,^{\circ}\mathrm{C}$. It is available in plastic through hole package, and bare die type.

CREE's second generation Z-FET C2M0025120D has extremely low on-resistance with only 25 $m\Omega$, the continuous drain-source current reaches to 60 A, the operating temperature goes up to $150\,^{\circ}\mathrm{C}$.

There are more and more manufacturers have been involved into SiC MOSFET technology. Rohm has started to release SiC MOSFET since 2011 with voltage rating 600 V, now it also has developed SiC power MOSFET with 1200 V and 40 A electrical ratings, The junction operating temperature has reached to $175\,^{\circ}\mathrm{C}$.

The common features of the SiC MOSFETs are:

- High speed switching with low capacitances
- High blocking voltage with low on-resistance
- Easy to parallel
- High tolerance to high temperature operation

These features benefit a power converter in the following perspectives: low gate driver power requirement; lower switching power losses and conduction losses; high switching frequency; higher voltage operational system and high temperature operation capability.

SiC MOSFETs are ideal for high voltage applications where energy efficiency is critical. One of the CREE's demonstration SiC MOSFET solar inverter test results have shown an average saved switching losses up to 30%. With all-SiC system - SiC Barrier Schottky Diodes and SiC MOSFETs - the overall system efficiency has exceeded 99% [18]. In [18], it also compared the performances of CREE's CMF20120D SiC MOSFETs and the best Si IGBTs. The CREE's system efficiency has been improved 2% by switching SiC MOSFET system at 2 to 3 times of the Si IGBT optimal frequency. Even higher efficiency could be achieved by further increased frequency. This is possible since the significantly reduced switching power losses of SiC devices allow much higher switching frequency compared to Si transistors. Fast frequencies also reduce the passive components in the power circuit, which finalized a reduced system size, weight and cost. A few recorded test data has

demonstrated SiC MOSFET is a highly reliable transistor. Its life time test results depicts that SiC devices' FIT rate is less than 20 fails per billion device hours. The field accelerated life time data predicts a MTTF of one million years at 75% of continuous rated voltage [11].

With all these benefits, SiC MOSFETs become popular, the applications range from industrial power supplies to commercial power converters. It is expected the maturity of the SiC MOSFET technology with newer fully released MOSFET products.

2.2.3 SiC Power Modules

In November 2012, CREE released the industry first commercially available all-SiC half bridge power module [19]. The module includes SiC MOSFETs and SiC Schottky diodes in a 50-mm half-bridge configuration rated to $150\,^{\circ}\mathrm{C}$ maximum junction temperature. The all-SiC devices extend the existing discrete SiC MOSFET and diode products into higher power application. It is rated at 100 A current handling and 1.2 kV voltage blocking capability. In addition to its high junction temperature tolerance and the high power handle capability, the whole SiC power module has demonstrated up to 100 kHz switching frequency, which enable the module to be reduced in size, weight, cooling requirement and overall cost of the power conversion system. Regarding to reliability, the modules have gone through full, standard JEDEC qualification, along with more stringent power cycling out to 20 M cycles without failure [11].

In May, 2013, CREE released the industry's first commercially available SiC six-pack, three phase MOSFET power module (with part No. CAS100H12AM1) in an industry-standard 45-mm package [20]. The basic specifications are: rating voltage 1.2 kV and current 50 A. The 50 A SiC power module is equivalent to a 150 A Si module for a given power level; The power losses can be reduced by 75% which leads to around 70% heat sink reduction; Consequently, the power density is improved about 50%. In addition, it is possible to use the SiC power module at less derating current level, since the conduction power losses is significantly reduced compared to Si IGBT devices [11].

Rohm Co. Ltd has also been highly involved in the all-SiC power module technology. It has released an all-SiC full bridge power module in March 2012 [21] which rated at 1.2 kV blocking voltage and 100 A current handling capability. With this power module, about 85% power losses can be saved, maximum switching frequency can up to 100 kHz which is 10 times higher than Si IGBT power module. Due to the low power losses and fast switching characteristics, the rated 100 A SiC power module can replace a 200 - 400 A Si IGBT module. In addition, the module size can be reduced to only half of a 400 A class Si IGBT power module. The newly released Rohm's bridge leg power module (with parts No. BSM180D12P2C101 and BSM120D12P2C005) have even improved current ratings of 120 A and 180 A, respectively [22, 23].

The emerged SiC power module technology allows power converter to have a better performance, i.e. with improved efficiency, power density, reliability, fast switching frequency and also small weight size, weight. Consequently, the overall power converter system can

be operated with an high quality performance without cost increment. Especially, when it is with the respect to the high temperature operation environment and limited space, SiC technology will be a better candidate.

2.3 SiC Technology

The literature study have showed three development branches of SiC technology, which include:

- SiC Transistors Development
  The SiC Transistors have been growing in two directions. In one direction, the SiC devices are developed towards higher power ratings and faster switching frequencies. In the other way, new product parts of transistor families are keeping being realized, also different families of SiC devices are under long-term research and investigation.

  Power semiconductor devices are most functional part in power electronics. Although only a few SiC semiconductor power devices are commercially released, a lot of different types of SiC transistors with increased switching frequency and different power handling capabilities are under sampling and testing. In [17], a few megawatt level power handling capability SiC devices with extremely high power density and high operating temperature possibility are under developing. Such as PIN SiC diode which has voltage rating of 19 kV, current density 100 A/cm^2 and maximum operational temperature 200 $^\circ$C. The maximum voltage level of SiC BJT recorded in [17] is up to 6 kV. SiC MOSFET family has a voltage range from a few hundred to 14 kV with low conduction-resistance. For 14 kV voltage blocking MOSFET it is only 228 $m\Omega$. SiC normally-on JFET in a few kilovolt range and 11.1 kV normally off TI-VJFET with 124 $m\Omega$ on-resistance were documented. A 10 kV SiC IGBT was first reported in 2005. ARPA Team has been putting efforts on developing 15 kV Grid-Scale power conversion SiC power module, which is expected to be available by May, 2014 [24]. In addition, SiC thrystors (and GTO) ranged from hundred volt to 12.7 kV has been documented.

- SiC power Electronics Applications
  SiC devices together with the promising packaging technology, mature Integrated Circuit (IC) technology and control technology have been keeping investigated to develop high power handling capability, fast switching frequency, high power efficiency and high temperature reliable power electronics applications.

  On December 25, 2013, Mitsubishi Electric Cooperation announced that it has lunched a rail-car traction inverter system for 1500 V DC centenaries which incorporates the world's first all-SiC power modules [25].

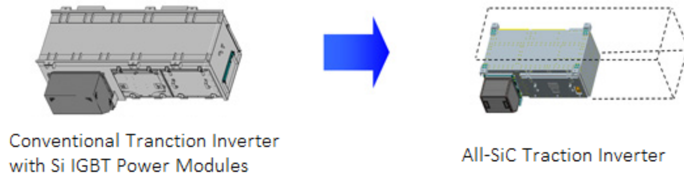


Figure 2.1: Size Comparison of Si IGBT and All-SiC Traction Inverters

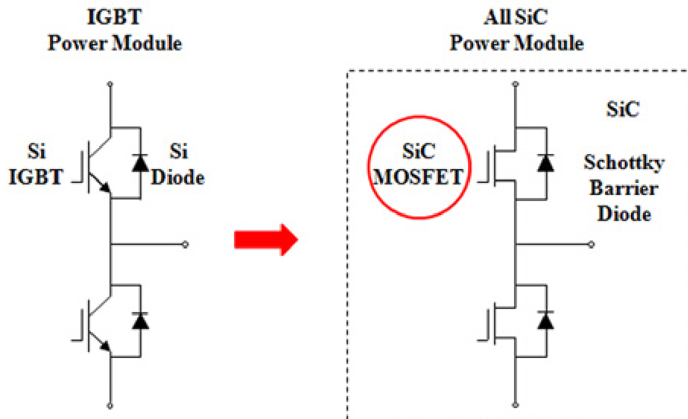


Figure 2.2: Reduced Number of Components

The primary properties of the all SiC inverter system is greatly reduced power losses, size, and weight compared to conventional Si IGBT power modules or hybrid power modules which mix both Si transistors and SiC diodes. According to its record, the switching loss of the new traction system is approximately 55% reduced than Mitsubishi conventional Si IGBT power modules system. There are about 65% (See Figure 2.1) and 30% size and weight reduction compared to Si IGBT and Hybrid inverter system individually. In addition, the number of components integrated in the inverter system is reduced by integrating SiC transistors and diodes into one package per inverter circuit phase (See Figure 2.2).

A CREE's demonstration interleaved boost converter with 100 kHz, 10 kW has be built based on CREE's 1.2 kV SiC MOSFETs and Schottky Diodes [26]. The Boost system has achieved the peak efficiency up to 99.1% [27].

In [28] it compared CREE's 1200 V SiC MOSFET power module with conventional Si IGBT modules in Voltage Source inverter (VSI) applications. The SiC-based system cost was reduced by low switching losses. This advantage started to be seen at lower switching frequency. According to the documentation, CREE's 100A SiC

module is capable of replacing at least a 150 A Si module with significant performance and reliability advantages at 5 kHz operation. At modest 16 kHz operation, the SiC module can even replaces a Si module up to 300 A without overload and thermal margin requirements.

Nowadays, after the release of the SiC transistors and SiC power modules, more and more customs are starting to put efforts on SiC technology. The target applications range from industry power supplies to commercial inverters and converters. For less than 50 kW system, one of the more popular all-SiC 1200 V MNPC topology is commonly used by many vendors, including Vincotech [11]. The main applications of this circuit type are used in three-level inverters and UPS (Un-interrupted Power Supply) [29].

- High Temperature SiC Power Electronics (HTPE)
  SiC power devices perfectly suit for the elevated temperature, limited space and critical reliability required fields, such as down hole oil drilling, aerospace, automobiles and so on. In this extent, high temperature electronic will become another big branch of SiC technology.

  A lot of companies, organizations, research centers and even governments are involved in developing high temperature power electronics technology. A lot of efforts are put to discover the high temperature properties of SiC material with improved package technology. APEI Inc is developing a motor drive solution with high temperature multi-chip power module. It aims to address robotic probes and landers in the harsh environment on Venus with a surface temperature of 485 $^{\circ}$C [30] .

  SINTEF energy research, Norway are involved in exploring advanced High Temperature Power Electronics (HTPE) power converters for down hole, automotive and aerospace applications. The target ambient operation temperature is in the range of $200 - 250\,^{\circ}$C [31].

  SmartMotor AS is taking the project named as "Innovative efficient and survivable electric drive systems for subsea and down hole applications" under the projects program of PETROMAKS. One of the challenging factors is the severe down hole environment, with elevated temperature, high pressure and severe vibration. SiC technology together with advanced packaging technology are the dominant solutions.

  A lot of universities and research organizations start to have SiC HTPE or SiC power electronics as one of their topics. Governments have started to fund the SiC technology. These activities have been significantly increasing the speed of SiC technology maturity and spreading the SiC technology and products into broader fields.

2.4 SiC Markets

Thanks to the advantages of SiC technology, SiC semiconductors and electronics have emerged as a prominent field, which is predicted as the replacement candidate of traditional Si technology. It is expected in the next 10 years, SiC will become a part of mass manufacturing in both power device and power electronic applications. SiC technology and industry will penetrate into high temperature semiconductors, opto-semiconductors as well as power device and power application sectors [32].

The overall SiC power semiconductors market already takes about 1% of the total power semiconductors market with less than 15 years development. Moreover, the increment of the SiC market is rapid. Even with the severe downturn of power electronics (almost -20% deceasing) which started in late 2011, SiC power device market still keeps on growing with 38% increasing rate each year. A common sense of the power semiconductor industry is that the displacement of Si has already begun [33]. Yole Développment's report "SiC Market 2013" has indicated the growing trend for next 10 years (See Figure 2.3 [33]).

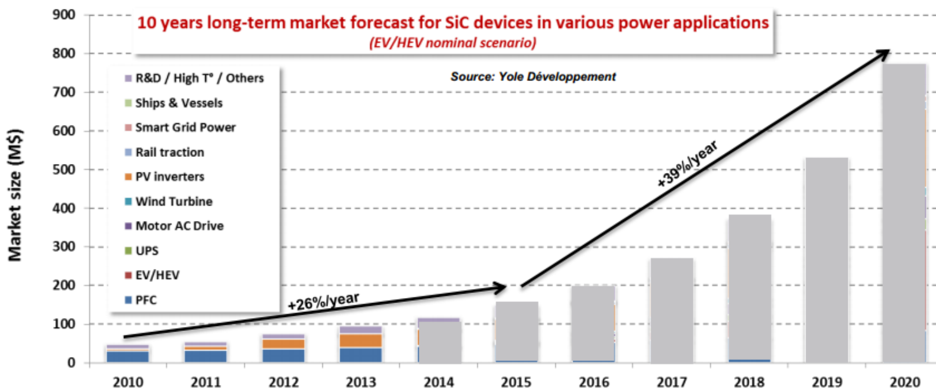


Figure 2.3: 10 Years Market Forecast for SiC Devices

In the report "Silicon Carbide (SiC) Semiconductor Materials and Devices (Discretes & Chips) Market, Global Forecasts & Analysis (2012-2022)" [34], it predicted the 38% yearly increasing rate of power devices will continuously grow to 2022. It forecasts the SiC devices market will reach $\$$ 5.34 billion by the end of 2022. For SiC power SiC power electronics market, the phenomenal growth rate is about 35% to 50%. With an expected growing rate of 45.65% to 2022, the SiC power semiconductors will exceed $\$$ 4 billion, which will take a share of 13% of the total power semiconductor market.

In 2012, SiC device market is strongly dominated by Infineon and CREE [34]. However, the competition is more and more grabbing market share with other aroused companies. The most two followed competitors are STMicroelectronics and Rohm. MicroSemi and GeneSiC. Up to 2013, more than 30 worldwide companies have established a dedicated

SiC device manufacturing capability with related commercial and promotion activities. In addition, more and more companies are emerging and developing as the foundry services or contract manufacturing services. It depicts that the SiC market chains have already started to form, from foundries to research organizations, and followed contract manufacturers (See Figure 2.4) [33].

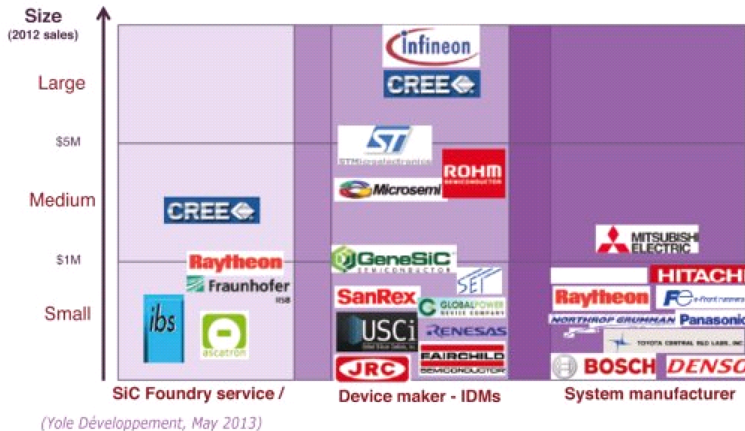
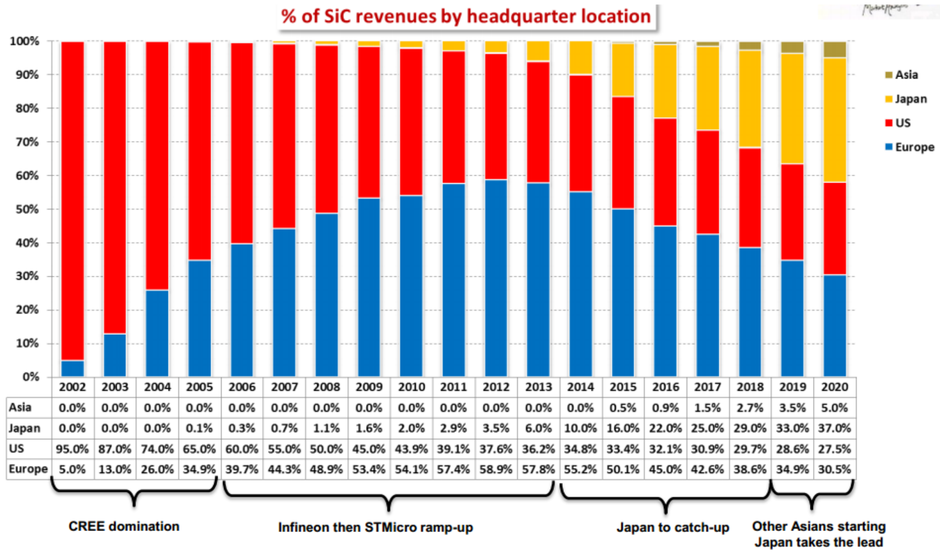


Figure 2.4: SiC Revenues by Headquarter Location: Source Yole

The SiC markets are mainly distributed in Asia and US (See Figure 2.5 [33]). The main players in Asia are dominated by Japanese companies [34], such as Panasonic, Toshiba, which are clearly identified as credible contenders. Mitsubishi Electric, Fuji Electric are running within the Japanese national program. A big market share of Chinese companies are suspected to be emerging according its investment plan in R & D. Most of the existing companies are distributed in US, which makes US SiC industry as the most dominated market share.

According to Yole Développment [33], the reshaping of SiC industry is started from the discrete device business into the power module business. It forecasts that SiC power module sharing will exceed \$ 100 million by 2015 and about top \$ 800 million in 2020 if the SiC technology penetrates into automotive industry.

To summarize, SiC power electronics will be one of the main competitors in power electronics market. The conventionally Si-based power devices dominated market will be influenced to a different stage since the replacement of the SiC activities has started to take force. Three trends of SiC semiconductor businesses will be SiC semiconductor device market, SiC power application market and SiC high-temperature semiconductor market. SiC business model has been developed as a chain from upstream to downstream with SiC foundry service, device maker and volume manufacturer.



	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020
Asia	0.0%	0.0%	0.0%	0.0%	0.0%	0.0%	0.0%	0.0%	0.0%	0.0%	0.0%	0.0%	0.0%	0.5%	0.9%	1.5%	2.7%	3.5%	5.0%
Japan	0.0%	0.0%	0.0%	0.1%	0.3%	0.7%	1.1%	1.6%	2.0%	2.9%	3.5%	6.0%	10.0%	16.0%	22.0%	25.0%	29.0%	33.0%	37.0%
US	95.0%	87.0%	74.0%	65.0%	60.0%	55.0%	50.0%	45.0%	43.9%	39.1%	37.6%	36.2%	34.8%	33.4%	32.1%	30.9%	29.7%	28.6%	27.5%
Europe	5.0%	13.0%	26.0%	34.9%	39.7%	44.3%	48.9%	53.4%	54.1%	57.4%	58.9%	57.8%	55.2%	50.1%	45.0%	42.6%	38.6%	34.9%	30.5%

Figure 2.5: Main Players and Related Business Models in SiC Device Industry

Chapter 3

Theories of Power Converters

The basic power converter types related to this thesis work include step down converter, Synchronized Buck Converter (SBC) and DC-AC inverter.

3.1 Step Down Converter

Step down converter is also known as chopper or buck converter. The basic function is to step dwon input voltage to a lower level. The basic construction seen as Figure 3.1 [1]. A resistive load is presented in the circuit.

The equivalent switching circuit is shown as Figure 3.2 [1] for on and off state separately. The relationship between the input and output voltage is:

$$V_o = D * V_d \tag{3.1}$$

Two different operating modes of this circuit is Current Continue Mode (CCM) and Current Discontinue Mode (CDM). If the inductor is fully demagnetized, the step down converter works in CDM. Otherwise, it works in CCM. For power efficiency consideration, it is commonly designed to work at CCM. The mathematical boundary of CCM and CDM can be expressed by the inductor current:

$$I_{LB} = \frac{1}{2} i_{L,peak} \tag{3.2}$$

$$i_{L,peak} = \frac{V_o T_s}{2L}(1 - D) \tag{3.3}$$

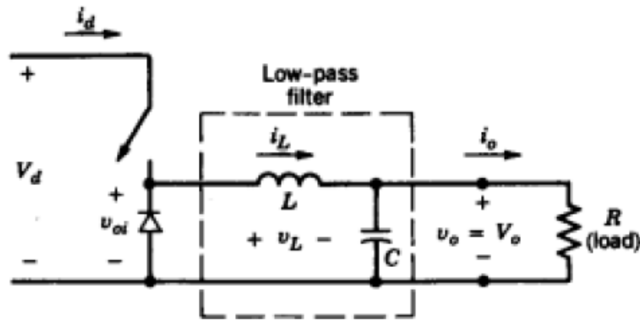


Figure 3.1: Step Down Converter

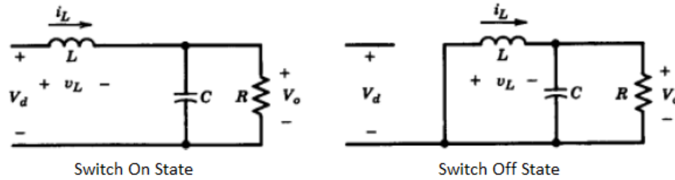


Figure 3.2: Equivalent Step Down Switching Circuit

3.2 Half Bridge Converter

Figure 3.3 has despited the half bridge converter configuration. In this thesis work, CREE CCS050M12CM2 SiC MOSFET power module have been constructed in parallel configuration (See Figure 3.4). Consequently, the three legs power module is operated as half-bridge converter. Different functional converters can be realized with this half-bridge construction.

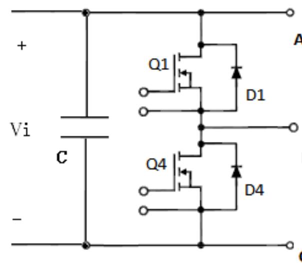


Figure 3.3: Half Bridge Configuration

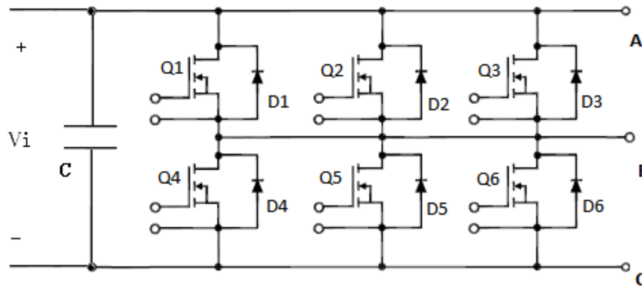


Figure 3.4: Parallel Half Bridge Configuration

- Step Down Converter
  To operate a bridge leg converter in the step down configuration, only a pair of transistor and freewheeling diode are active. If Q1 is activated by applying the gate drive signal, Q1 and D4 will work together, the load is connected between the output port B and C in Figure 3.3. When Q1 switches on, current goes through Q1 to the load. When Q1 off, the current commutates with D4. In the Q1 and D4 combination, Q1 source is a voltage floating point. To avoid the source floating, load can be connected between ports A and B, Q4 and D1 work as the switch and diode pair.

- SBC
  The primary difference of SBC and conventional step down converter is using a complementary controlled switch to replace the freewheeling of diode. In Figure 3.3, Q1 and D4 are used the same as conventional step down converter, Q4 is added as the complementary switch. Q1 and Q4 conducts alternately. The main advantage is at CCM operation, the turn-off diode D4 power loss will be replaced by a lower Q4 turn-on power loss. In this manner, the converter power efficiency is improved. However, the disadvantage are obvious: the proper complementary gate control circuit have to be efficiently implemented; DCM detecting circuit has o be applied to keep the it works at CCM.

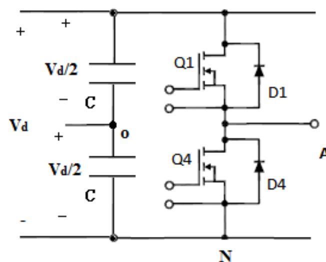


Figure 3.5: Single Phase Inverter

- Single Phase Inverter
  Controlling transistors switching states is one of the dominant technology of inverter operation. To operate the bridge leg as a single phase inverter, square-wave control and Pulse-Width Modulated (PWM) control approaches are commonly used to shape the output voltage. To simplify the analysis, two large capacitors are connected seriously to the input of the bridge leg (See Figure 3.5).

  In PWM control, a sinusoidal control signal with frequency f_1 and peak magnitude $\hat{V}_{control}$ is compared with a triangular waveform with switching frequency f_s and peak amplitude $\hat{V}_{tri}$. The comparison results is used as the control signal to switch devices. The ratio of the peak amplitude of control signal and triangular signal is defined as amplitude modulation.

$$m_a = \frac{\hat{V}_{control}}{\hat{V}_{tri}} \tag{3.4}$$

  According to m_a, it can be divided into linear modulation ($m_a \leqslant 1$) and nonlinear modulation ($1 < m_a \leqslant \frac{4}{\pi}$). For UPS applications, the linear modulation methods are commonly used. Both modulation methods can be used for motor drivers.

  In the same way, the frequency modulation m_f is defined as

$$m_f = \frac{f_s}{f_1} \tag{3.5}$$

  m_f is commonly selected as a triple number of 3 and larger than 9 to decrease the output harmonics dependence of m_f.

  In the inverter showed in Figure 3.5, Switches Q1 and Q2 work as a complementary pair, and both are controlled by the comparison results of the controller, the switching condition will be:

  $v_{control} > v_{tri}$

$$Q1 on, v_{Ao} = \frac{V_d}{2} \tag{3.6}$$

  or

  $v_{control} < v_{tri}$

$$Q2 on, v_{Ao} = -\frac{V_d}{2} \tag{3.7}$$

  Since Q1 and Q2 are never on/off at the same time, the output voltage fluctuates between $\frac{V_d}{2}$ and $-\frac{V_d}{2}$ 3.6 (b). The peak amplitude of the fundamental-frequency components $(\hat{V}_{Ao})_1$ can be derived according to the following steps:

$$v_{control} = \hat{V}_{control} sin(w_1 t) \tag{3.8}$$

in Equation (3.8) $w_1 = 2\pi f_1$

$$v_{Ao} = \frac{v_{control}}{\hat{V}_{tri}} \frac{V_d}{2} \tag{3.9}$$

$$(v_{Ao})_1 = \frac{\hat{V}_{control}}{\hat{V}_{tri}} sin(w_1 t) \frac{V_d}{2} \tag{3.10}$$

Which gives the output voltage fundamental $(\hat{V}_{Ao})_1$:

$$(\hat{V}_{Ao})_1 = m_a \frac{V_d}{2} \tag{3.11}$$

v_{Ao} fundamental frequency is f_1. Figure 3.6 [1] has demonstrated the control scheme and the inverted output voltage waveform.

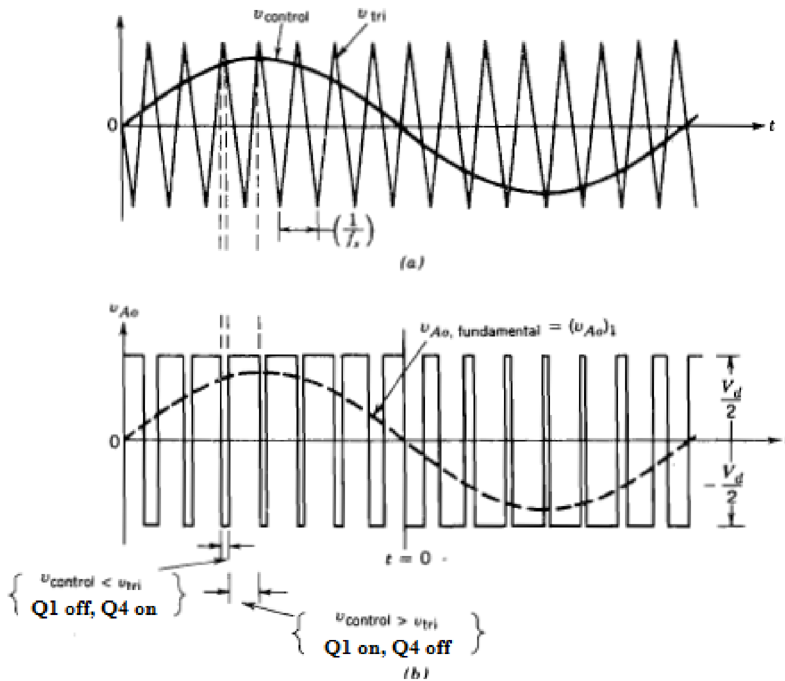


Figure 3.6: Single Phase Inverter Operation Waveforms

3.3 SiC MOSFET Gate Drivers

A literature study of gate driver circuit including high temperature gate driver had been documented in specialization project report. Therefore, only a few main point of SiC MOSFETs gate driver requirements will be briefly repeated. In addition, basic theory of

paralleled MOSFETs gate driver will be introduced.

- Basic Gate Driver Requirements
  A MOSFET gate drive supplies voltage pulses which switch the device from one state to another state. The fast switching is important to avoid long transient of the MOSFET ohmic region operation. In the on time, an appropriate positive gate drive voltage should be applied to keep the on-resistance as low as possible. To make sure a fast turn-off and reliable off state, a negative bias gate voltage should be implemented, which also prevents transient stray signal triggering on the parasitic BJT of MOSFET, which has been detailed explained in the specialization project report, in 2013.

- Isolation Requirement
  Gate driver is the middle bridge which connects the control circuit and the power circuit. It also connects the a few watt gate driver circuit and a few kilowatt or even higher level power circuit. An isolation gate driver is essential for protecting the signal level control circuit from destroying by the higher power side.

  In half-bridge gate driver circuit, the Q1 source terminal will float between positive V_d and ground voltage potential, whereas the corresponding gate driver circuit keeps to ground potential. An isolated gate drive will avoid the high voltage potential invading the logical side of the gate driver.

- Dead Time Controller
  In bridge circuits, the blanking time must be provided to avoid the bridge-leg overshoot. The schematics of generating dead time will be implemented in the gate driver design chapter.

- CREE's SiC MOSFET Gate Driver [35]
  CREE Inc. has published an demonstration isolated gate drive circuit which is suitable for testing and evaluating SiC MOSFETs in various allocations [35].

  +20 V positive and -2 V to -5 V negative bias voltage are specified as an optimal gate driver voltage. Capable sourcing and sinking gate current pulses should be realized to maximize the switching speed. The gate driver should locate as close as possible to the SiC MOSFET. A separated source return path will reduce the conductor stray inductance which will correspondingly limits the induced voltage $L_p \frac{di}{dt}$.

3.4 Parallel Construction of MOSFETs

The advantages of using SiC MOSFETs are obvious. First the gate drivers are relatively simpler and cheaper when compared to BJTs or JFETs. This is due to its capacitive gate and source configuration which makes MOSFET a type of voltage controlled devices. Therefore, it does not require conducting gate current or reverse bias current to sustain its on or off

state. In this way, a relatively small gate driver power is required. Second, MOSFETs can withstand simultaneous application of high voltage and current without undergoing destructive failure. Third, the MOSFET devices can be switched at higher switching speed, because it is a majority carrier device, no current injection and no tail current during the switching cycle which results in relatively low power losses.

Another advantage of MOSFETs is that it is easier to parallel. this is due two reasons: One of the reason is MOSFETs' on-resistance has a positive thermal resistance coefficient, which helps to ensure the thermal stability of the MOSFETs devices. The other reason is due to narrow part-to-part parameter distribution. It helps the current sharing and ensure the reliability of parallel connection [36]. A parallel configuration is especially beneficial to the conditions where the higher level power or current derating is required. Figure 3.7 [1] shows the typical paralleled MOSFETs configuration.

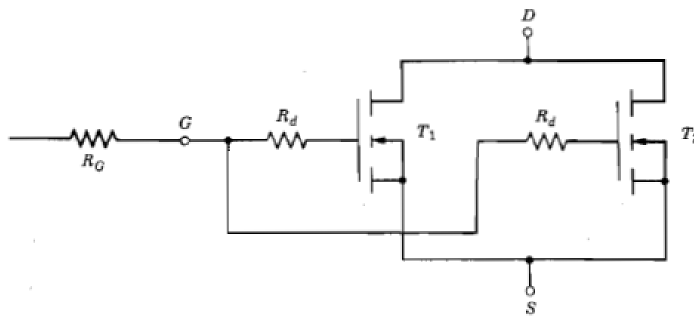


Figure 3.7: Parallel Connection of MOSFETs

SiC MOSFETs has high voltage blocking capability. Its conduction-resistance is significantly smaller compare to conventional Si devices. As the only one commercially available SiC power device type, which is the best candidate suits for the parallel constructed circuit.

For down hole oil applications, the main reason of using parallel connection is to reduce the conduction power losses. The cooling size and the space of the power converter will be saved. In addition, the converter temperature will be relatively stable, which increases the system reliability.

Theoretically, for the paralleled power module the on-resistance is reduced to 1/3. The current goes through each device will be 1/3 to the original value. For each device, the power loss is 1/9 to un-paralleled MOSFET. The overall conduction power losses have be reduced to 1/3 of un-paralleled configuration.

The disadvantages of paralleling MOSFET is the increment of capacitance. The gate capacitance will be three times to the original value, a increased gate driver power solution has to be figured out. The drain-source stray capacitance will also be tripped, It will influence the drain current falling speed, the overall system switching speed might be limited.

3.5 Gate Driver of Paralleled MOSFETs

For a parallel connection MOSFETs, current sharing is important to reach the expectation of thermal stability, reducing on-resistance and so on. As known, the current in each MOSFET is determined by its transfer characteristics (see Figure 3.8 [1]). Therefore, it is better to keep the paralleled MOSFETs gate-source voltage V_{gs} balance to make sure similar current level will be reached during the switching processes. Therefore, a common gate driver would be the simplest solution to fulfill this requirement.

However, the gates cannot be connected directly, a small resistance R_d or ferrite bead must be used in series with the individual MOSFET gate. The function of R_d is to damp down the unwanted oscillation.

Furthermore, the symmetrical layout of the paralleled MOSFETs, with balanced gate driver circuits will ensure similar parameter distribution, which will also help to balance the load current sharing [1].

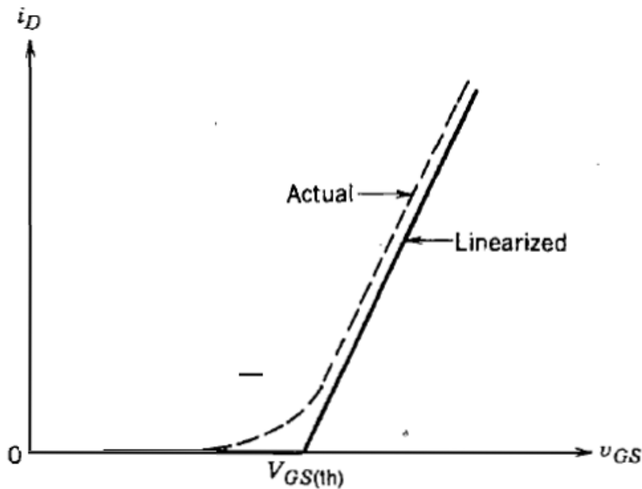


Figure 3.8: MOSFET Transfer Curve

3.6 KPIs of Down Hole Power Converters

KPIs stands for Key Performance Indicators. The criteria to evaluate the power converters differs from case to case. In the following a few main indicators which can be used to value the high temperature power converter are discussed.

- Reliability
  Reliability depicts two meanings. First, the power converter can work appropriately within its life time and a certain harsh working environment. Second, it fails in a safe manner once the failure cannot be avoided. The failure should be under control, without causing significant cost and safety risks. For down hole power converters, the reliability of 5-year continuous working, under high ambient temperature without too much thermal cycling is commonly required.

- High operational Temperature
  As mentioned previously, high temperature is one the challenging factor for a down hole power electronics devices. Therefore, an appropriate temperature rating with sufficient should be achieved.

- Efficiency
  Efficiency indicates how much power can be efficiently used by the final consumer. In a low efficient system, most of the waste power converted to heat. It will increase partial or the overall system temperature. It might influence the performance of the power converter. In some severe cases, it might cause failure. Furthermore, a more efficient cooling setup will be needed, which is unappropriated in narrow down hole environment.

  The most commonly cared power losses will be the semiconductor power losses. Therefore, low on-resistance, low switching power loss SiC transistors and low forward voltage drop, zero-recovery SiC diodes are beneficial for improving the efficiency.

- Power Density/Converter Size
  Power density is usually evaluated $\frac{kW}{m^3}$. It can be indicated by the size of power converter when the power level is certain. In a down hole environment, the power converter size might be limited by the space and other surroundings. cooling apparatus and the switching frequency are two of the factors which influence the power converter size.

- Power Rating and Switching Frequency
  The power rating for down hole applications are not critical, since no extreme high power will be required. An optimal high switching frequency will be advantageous for reducing other passive devices and overall system cost, it also beneficial for an optimal converter size.

Chapter 4

Bridge SiC MOSFET Gate Driver

CREE's SiC MOSFETs, single bridge 55 mm and six-pack (three phase) 45 mm power modules are all available for immediate shipping through Digi-key Cooperation and Mouser Electronics. Gate-driver ICs suitable for CREE's SiC MOSFETs are available from IXYS and Texas Instruments. Complete single MOSFET gate driver boards CRD-001 are available as samples from CREE upon request [20].

CRD-001 gate driver is applied for testing and evaluation of SiC MOSFETs in variety of applications [35]. It has an input 12 V, adjustable output voltage difference up to 35 V, a -5 V reverse bias output is available. The peak output current pulses can reach to 9 A for charging and discharging the SiC MOSFET gate capacitance. The schematic of CRD-001 see Appendix A.

In this project, the 6-pack SiC MOSFET power module with part No. CCS050M12CM2 is used and constructed as a bridge leg converter prototype. The half bridge gate driver is not available in the on-stock market. Therefore, efforts were put on bridge leg gate driver design. The power electronics design software LTspice had been used for simulation. PCB (Printed Circuit Board) design software Cadsoft EAGLE has been used to design the gate driver layout. At last, the laboratory tests of the bridge leg gate driver have been realized.

4.1 Dead Time Controller

In a bridge circuit, the cross conduction will short out of the input voltage which will destroy the converter system and cause dangerous. One possible reason of the shoot over is that the turn-off delay of one MOSFET while the other MOSFET has been conducted. To avoid this type of failure, an conservative turn-on delay time should be preset to make sure the second MOSFET switch-on only after the first MOSFET switched-off.

Therefore, two complementary control signals with conservative dead time should be provided to the gate drivers.

The dead time is commonly designed according to the worst-case maximum storage time of the MOSFETs. So in normal operation there will be practically longer dead time the designed time. However, the dead time has to be carefully limited. When both of the MOSFETs are turned off, the output voltage will be controlled by the output current instead of the switch devices. If this condition exceeds a certain time, the converter system might be unstable. The dead time can be minimized by the design enhancements to gate driver [1], which include the use of anti-saturation diodes with BJTs, driver circuit with bipolar outputs, speed-up capacitors and so on. In this thesis work, the bipolar output gate driver is used, and if necessary, the speedup capacitor gate configuration can be realized by the reserved space on gate driver board.

The blanking time controller was realized by means of the circuit showed in Figure 4.1.

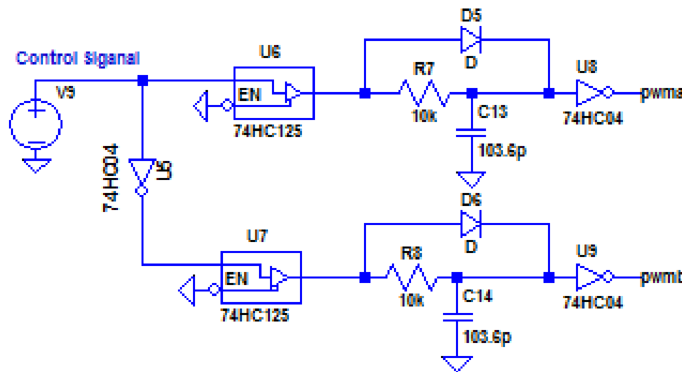


Figure 4.1: Dead Time Control Schematics

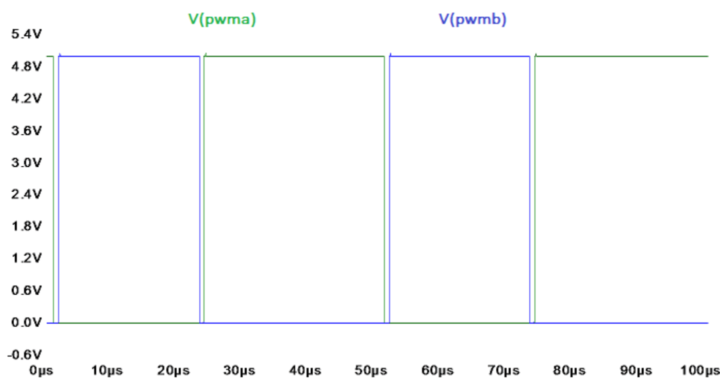


Figure 4.2: Simulation Result of Dead Time Controller

At the inputs and outputs of control signals, Schmitt buffers are used to make sure the similar distributed parameters, which will make sure the control signal have the similar properties. 74HC125 has a standard output voltage of 5 V, 74HC04 has a high level voltage 2.45 V . The delay time can be theoretically calculated through RC discharging circuit.

$$V_{cap} = V_c e^{-\frac{t}{\tau}} \tag{4.1}$$

$$\tau = RC \tag{4.2}$$

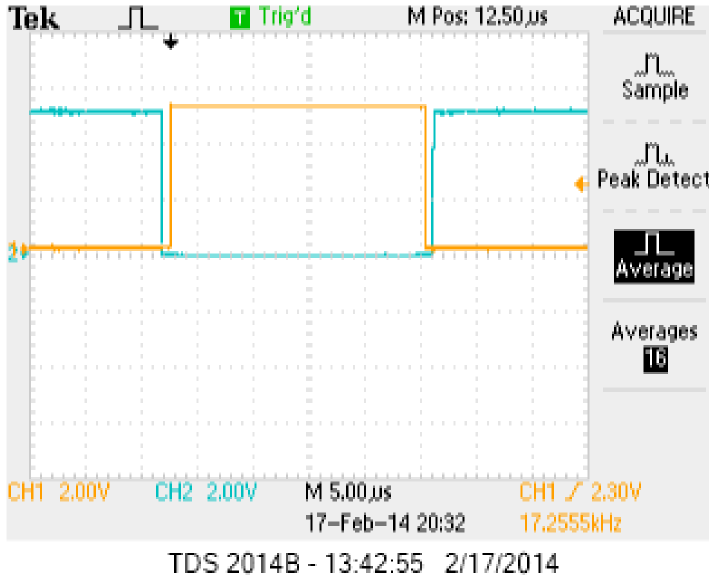


Figure 4.3: Lab Test Results of Dead Time Controller

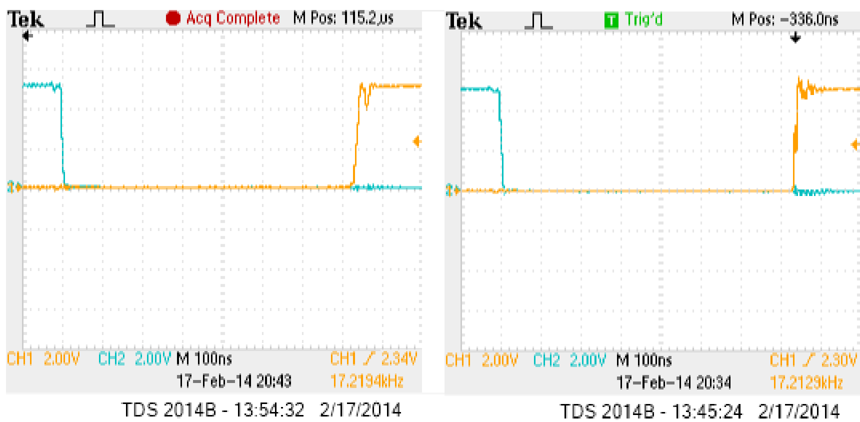


Figure 4.4: Turn-on Delay of Dead Time Controller

The theoretical calculation gives a delay time of 713 ns. The LTspice simulation result and the laboratory test all give the close results of around 720 ns . Figure 4.2 shows the simulation result. Figure 4.3 and Figure 4.4 depict the lab test result, the complementary control signal waveforms and detailed dead time have been documented individually.

In a $20kHz$ switching frequency system, the blanking time has taken less than 1.5% of the switching period, which can be taken as an appropriate option.

4.2 Gate Driver

A topology of CREE's single SiC MOSFET gate driver is modified to fit the bridge leg gate driver design. A single gate driver schematic see Figure 4.5. The finalized gate driver printed circuit board is depicted in Figure 4.6.

Figure 4.5: SiC MOSFET Gate Driver Schematic

4.2.1 Zener Diode Voltage Regulator

As discussed in the previous chapters, an isolated power supply for gate drive circuit is required. For different functional components the voltage rating are not the same. Besides, CREE's SiC MOSFET requires a -5 V reverse bias voltage. Therefore, a simpler Zener diode shunt voltage regulation method is used. The principle of Zener diode voltage regulator can be explained by Figure 4.7 [37].

Zener diode is decided by the regulated voltage level and the power rating. Special attention should be paid on the series resistor R_s. On one hand, it should be as larger as possible to decrease the resistive power loss. On the other hand, it should be keep into a certain range

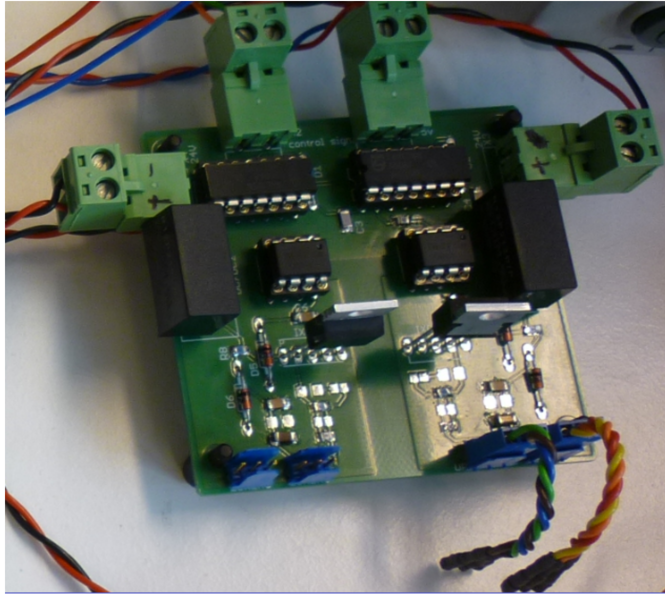


Figure 4.6: Bridge Leg Gate Driver Board

to ensure it works at the revers current region.

The R_s can be derived according to Equation (4.3).

$$R_s = \frac{V_{in} - V_z}{I_z + I_L} \tag{4.3}$$

In the target circuit both 18 V and 5 V voltages have to be regulated. The corresponding series resistors are shown in the schematics diagram.

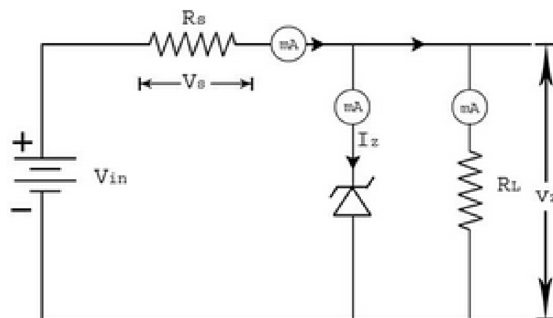


Figure 4.7: Zener Diode Voltage Shunt Regulator

4.2.2 Isolated Power Supply

Suggested by Richard Lund, SmartMotor AS, for a high voltage power circuit up to 700 $V \sim 800\ V$, a 5 kV isolated DC power supply should be used to prevent the interaction of different power level circuits. Both the calculation and laboratory tests have been performed to verify power requirement of the isolated power supply (See Appendix B). It has demonstrated a 2 W power rating is suitable for the above gate driver prototype with 40 kHz frequency and 45 nF capacitor load. Isolated power supply output voltage 24 V is directly used for IXDN609CI gate drive, regulated 18 $\sim$ 20 V for opto-coupler and another regulated 5 V used for -5 V reverse bias voltage.

The isolation was realized by the opto-coupler with part No. ACPL4800. It has a fast response time and relatively small propagation delay time. The primary side and the secondary side of this devices have been placed on isolated ground plates.

4.2.3 Alternative Gate Configurations

Current sourcing and sinking capability directly relates to SiC MOSFET switching speed. In the designed SiC power MOSFET gate driver, a few alternative gate configurations are designed. It can be flexibly realized by soldering the desired components on the gate driver board. Such as the changeable gate resistance, speedup capacitor with small damping resistor and the anti-paralleled Schottky diode. In this way, an optimized gate configuration can be constructed for a desired SiC MOSFET switching characteristics.

4.3 Simulation Results

4.3.1 Single SiC MOSFET Gate Driver

Due to the absent of -5 V "GND" LTspice gate drive module, an alternative totem-pole gate driver was simulated. The MOSFET gate capacitance was simulated by an 22.5 nF ideal capacitor load which is close to the value of three paralleled gate capacitance of SiC

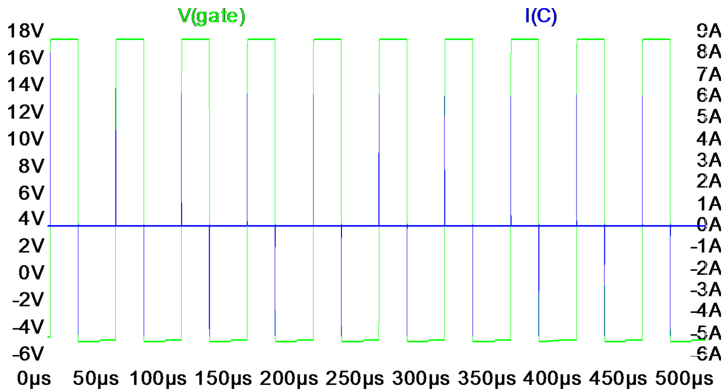


Figure 4.8: Gate Driver Simulation Results

MOSFETs in CCS050M12CM2 power module. One of the simulation results are shown in Figure 4.8. The corresponding simulation circuit can be seen in Appendix C Figure C.2.

To explore the influences gate driver characteristics with different gate configurations, another two simulations have been studied, which can be found in Appendix C.

4.3.2 Bridge Leg Gate Driver

A bridge leg gate driver simulation has been done with IXDD409 gate driver model since the IXDD609CI LTspice model is not available. Therefore, an +15 V on state voltage should be adjusted to +20 V according to their similar driver configuration. The simulation was done under a Synchronized Buck Converter (SBC) prototype. The gate configuration uses a single 6.8 Ω gate resistor. See Figure 4.9 and Figure 4.10 for simulation schematics and simulated gate driver results.

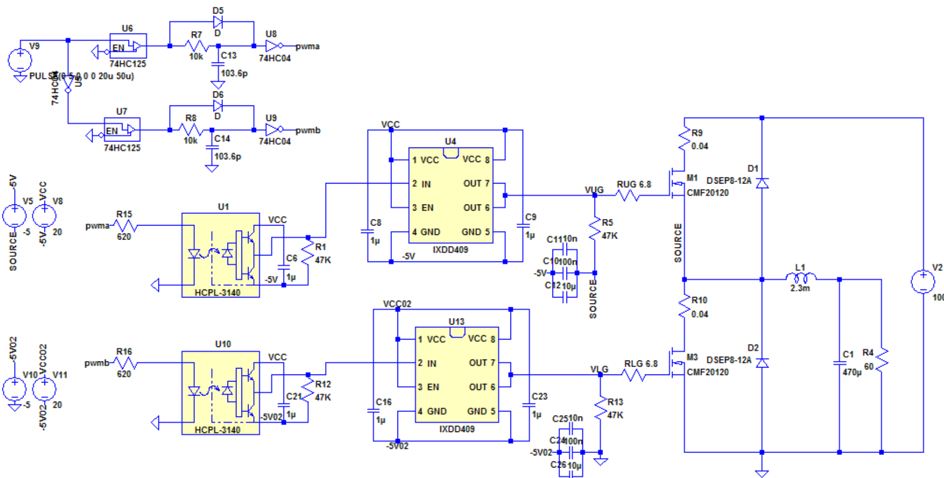


Figure 4.9: Bridge Leg gate Driver Schematic

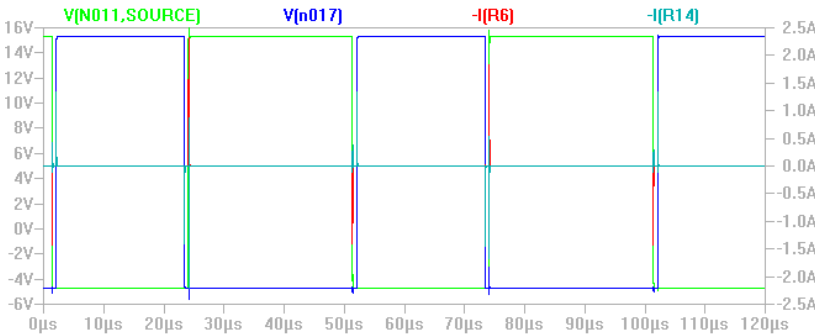


Figure 4.10: Bridge Leg Gate Driver Simulation Results

4.4 Lab Test Results

Figure 4.11 and Figure 4.12 depicts one set of the simulation results. The corresponding gate configuration was a 9 Ω resistor, a 6.8 nF capacitor load was applied to the gate driver. The voltage waveform was captured at the lower gate driver output. The green waveform is the current with peak value up to 2 A. The pink is the gate source voltage with positive 20 V and negative -5 V. The switching on/off time are less than 100 ns. The faster charging/discharging capability have be achieved with optimized gate configuration.

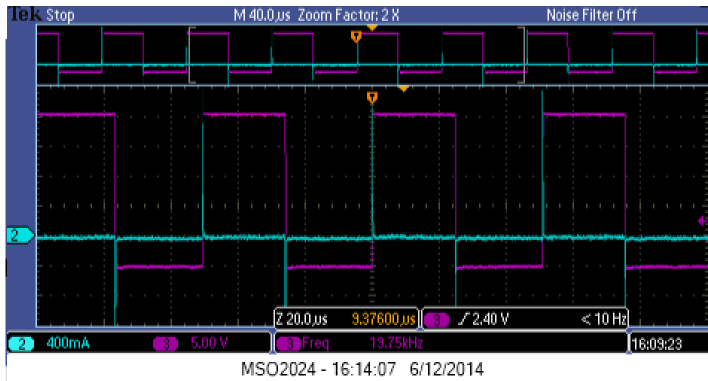


Figure 4.11: Bridge Leg Gate Driver Lab Test Results

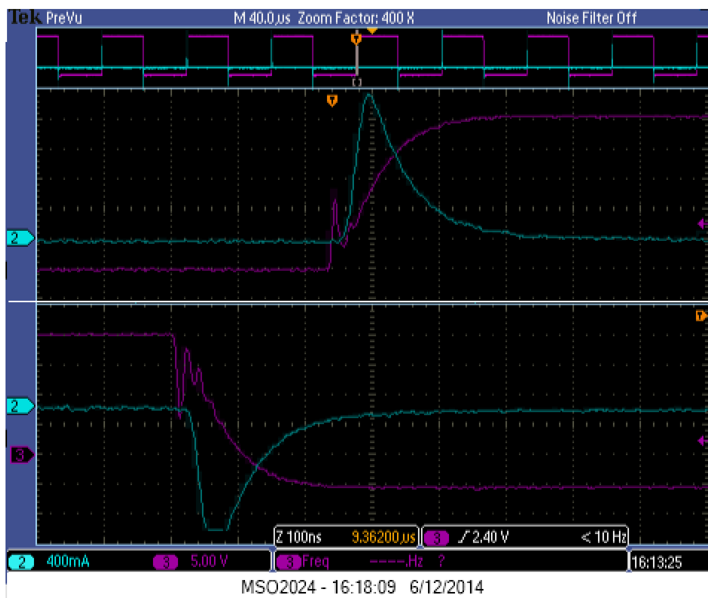


Figure 4.12: Gate Driver Switching Waveforms

Chapter 5

SiC Power Circuit Board

The SiC power circuit board was provided by SmartMotor, Dr. Richard Lund. The target design is a three phase all-SiC power inverter with CREE's six-pack 1.2 kV, 50 A SiC MOSFET power modules. Each module is connected in parallel configuration as a single phase, three power module are used for the target design.

The aims of the parallel connection are to reduce the power dissipation of the down hole power converter, and the current stress of the power module. Theoretically, each device conduction power loss can be reduced to 1/9, the total power losses will be recude to 1/3 with the paralleled configuration. In the power board design some of the main considerations include:

- DC-Link Capacitors
- Snubber Circuit
- Power Losses
- Heat Sink
- PCB Layout

5.1 Specifications of SiC Power Circuit Board

The target power converter are realized through the Printed Circuit Board (PCB). The main features of the board are:

1. The Inverter Specifications
    (a) 400 $V \sim$ 750 V nominal DC input V_{dc}.
    (b) Output line to line voltage V_{LL} is $0.69 * V_{dc}$, which gives an line to neutral voltage $\frac{0.69 * V_{dc}}{\sqrt{3}}$, in the range of 160 $V \sim$ 300 V. It works at the non-linear modulation range, with m_a 1.13.

   (c) 34 kW output voltage at 400 V V_{LL}, RMS current I_{rms} 50 A, power factor $cos\varphi$ 0.9. In its corresponding single phase, the voltage is 230 V, current 50 A, active power rating around 10 kW.

2. Auxiliary Circuits

   (a) It included three isolated current measurements for each phase output and one DC-bus voltage measurement. It is used also for control purpose. The measurement ICs are designed for output frequency, which is commonly a few hundred factor lower than the system switching frequency. Therefore, for the characteristics test of SiC MOSFETs, external compatible measurement equipment should be used.

   (b) A internal "NTC" SiC power module temperature sensor, and lockout auxiliary circuit are included. It will detect the power module temperature to realize the safety and reliability control.

   (c) The power supply for the auxiliary circuit has 24 V isolated voltage supply and local 5 V voltage regulation.

5.2 DC-Link Capacitors

The DC-link capacitor is also known as "decoupling capacitor". It connects the output of the DC power supply which is rectified from an 230 V AC grid and input of the switching network. The switching network output generates large transients at the switching frequency. The DC-link capacitor helps to keep these transients from revering back to the DC power supply. It also prevents the switching system from oscillating or triggering to short inadvertently at some fault cases.

The input capacitor is selected mainly according to its ripple current rating. In [38], the expression of required current handling capability is demonstrated in RMS under the DC/DC step down converter configuration.

$$I_{C,rms} = I_{out,max}\frac{\sqrt{V_{out}(V_{in} - V_{out})}}{V_{in}} \tag{5.1}$$

For inverter configuration, the input capacitor current rating requires:

$$I_{C,rms} = \hat{I}\sqrt{m[\frac{\sqrt{3}}{4\pi} + cos^2\psi(\frac{\sqrt{3}}{4\pi} - \frac{9m}{16})]} \tag{5.2}$$

$\hat{I}$ is the AC peak output current, ψ is the phase angle, and m is the modulation index. It is observed that the similar capacitor current expression is achieved:

$$I_{Crms} \approx \frac{\hat{I}}{2} \approx 0.7I_{out,rms} \tag{5.3}$$

It gives an proximate current rating of the capacitor 35 A. By adding margin of the current ripple from the diode rectifier, around 50 A RMS current rating was finalized. In the

designed board, 5 10 μF Vishy MKP1848 DC-link capacitors with rated current 9 A, voltage 900 V and 10 $m\Omega$ ESR are selected. The capacitor power losses can be grossly calculated according to Equation (5.4):

$$P_{in,cap} = \frac{ESR}{5} I^2_{cap,rms} \tag{5.4}$$

The maximum power losses is given by the largest ripple current 50 A, it is around 5 W.

5.3 Power MOSEFET Snubber Circuit

Snubber circuits are commonly used in power electronics. Its operational functions includes [1, 39]:

- Reduce or eliminate voltage (turn-ff) or current spikes (turn-on)
- Limit $\frac{di}{dt}$ at device turn-on and $\frac{dv}{dt}$ at turn-off
- Shape the device switching trajectory within the safe operating area (SOA)
- transfer power dissipation from switch to snubber resistor or a useful load
- Reducing EMI by damping our current and voltage ringing
- Reduce total switching power losses

Figure 5.1 depicts a simple RC turn-off snubber circuit for MOSFET, which can be used to prevent voltage spikes and voltage oscillations during MOSFET turn-off. MOSFET has a large peak current handling capability, and its switching speed (i.e. $\frac{di}{dt}$) can be easily controlled by the gate current. Therefore, there is commonly no need for a turn-on snubber, a RC turn-off snubber is enough in most cases.

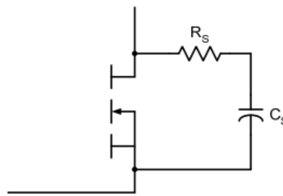


Figure 5.1: MOSFET RC Snubber

The goals of a SiC MOSFET turn-off snubber are to provide a zero voltage across the transistor while the current turns off and control the overvoltage in an acceptable range. Zero voltage while current decreasing is to achieve a lower voltage across the device while the current decreasing to zero, which will give a low turn-off power loss. By reducing the overvoltage level, the MOSFET electrical stress will be controlled to a reasonable level.

Voltage Zero Crossing

To realize zero voltage across the MOSFET, an ideal condition is first assumed, i.e no parasitic inductance is taken into account. To give an easier way to analyze the transient condition of the voltage and current waveforms, an RCD snubber network is first applied [1], see Figure 5.2.

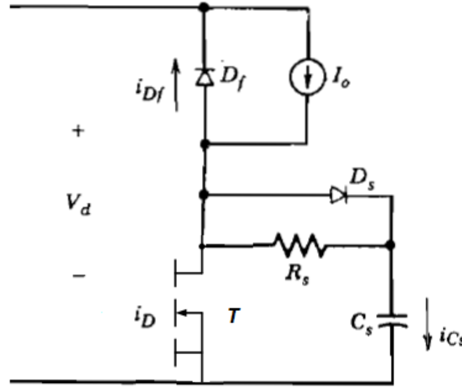


Figure 5.2: Turn-off Snubber Circuit

Prior to turn-off, the current I_o goes through MOSFET transistor T, voltage across MOSFET is essentially zero. At turn-off, the transistor current I_D commutates with snubber circuit diode D_s and C_s. I_D decreases with a constant $\frac{di}{dt}$, $I_o - I_D$ flows into C_s, which is charged with the constant $\frac{di}{dt}$. Therefore, for a current fall time t_{fi}, the capacitor current within time t_{fi} is derived as:

$$i_{cs} = I_o \frac{t}{t_{fi}} \tag{5.5}$$

The instantaneous capacitor voltage can be derived as.

$$v_{cs} = v_{DS} = \frac{1}{C_s} \int_0^t i_{cs} \mathrm{d}t = \frac{I_o t^2}{2 C_s t_{fi}} \tag{5.6}$$

When the snubber capacitor charges to V_d, the i_{cs} becomes to zero, and the freewheeling diode conducts current I_o, the details are also depicted in Figure 5.3 [1].

The middle waveform In Figure 5.3 depicts the condition in which the current falling time t_{fi} is right the time of snubber capacitor voltage charging. C_{s1} is the reference value for capacitor selection. Derives from Equation 5.6, which gives:

$$C_{s1} = \frac{I_o t_{fi}}{2 V_d} \tag{5.7}$$

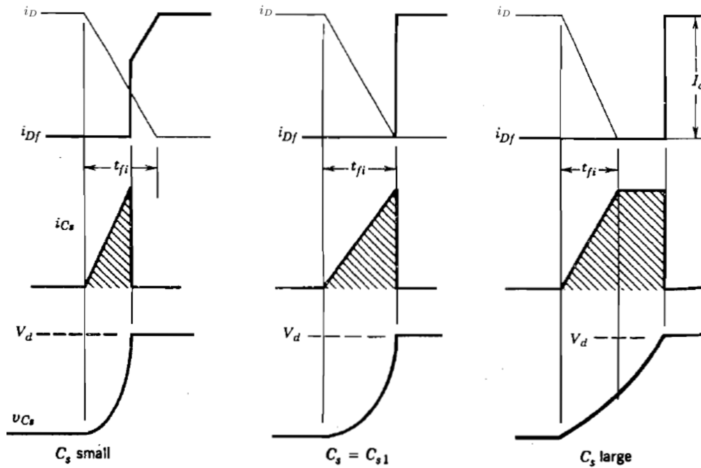


Figure 5.3: Turn-off Transient Waveforms with Different Snubber Capacitors

Figure 5.3 also demonstrated the relationship between snubber capacitor charing time and the transistor current fall time. It obvious that the bigger the C_s is, the smaller, slower increasing current is kept during the current falling. According to Equation (5.8) which results in a lower MOSFET power dissipation. The stored energy of the snubber capacitor will dissipate through the snubber resistor when MOSFET is conducing.

The turn-off MOSFET power dissipation is:

$$\triangle W_T = \int_0^{t_{fi}} i_D v_{DS} \mathrm{d}x \tag{5.8}$$

Snubber circuit power loss is:

$$W_{R_s} = \frac{C_s {V_d}^2}{2} \tag{5.9}$$

The snubber circuit should be chosen which makes sure the peak discharge current of C_s through the turn on MOSFET is smaller than reverse recovery current I_{rr} of the freewheeling diode. For SiC diodes which normally has a profitable zero reverse recovery current. It is assuming to limit the peak discharging current to $0.2I_o$. therefore, the expression for designing a snubber resistance is therefore written as:

$$R_s = \frac{V_d}{0.2I_o} \tag{5.10}$$

To summarize, Equation (5.7) and Equation (5.10) give the basic values of snubber capacitor and resistor. Equation (5.8) and Equation (5.9) give the criteria to compromise the trade-off between turn-off MOSFET power loss and snubber power loss. In [1], which has demonstrated a relationship of the snubber capacitor and the corresponding losses, and suggested a less MOSFET power loss, since the snubber heat dissipation is relatively easier to remove.

Overvoltage Regulation

This section deals with the overvoltage which is induced by the stray inductance. The snubber circuit is used to prevent or eliminate overvoltage. An analyzed circuit was redrew for overvoltage elimination study, see Figure 5.4 [1].

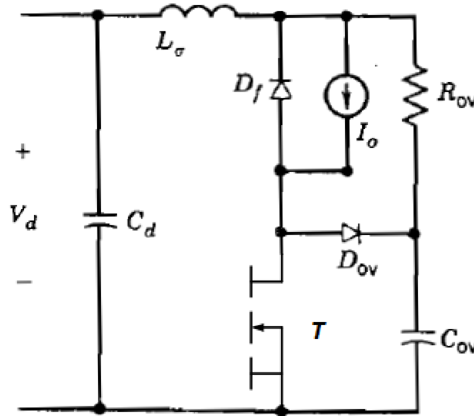


Figure 5.4: Overvoltage Snubber

L_σ stands for the lumped stray inductance. The value depends on the length stray conductor and the PCB layout. Usually it is assumed as 10 nF/cm of the conductor. In SmartMotor SiC power module design, a snubber circuit locates close to the MOSFET power module, the stray inductance influence to MOSFET will be greatly reduced. L_σ is assumed as $10nF$ in the corresponding design.

Prior to turn-off, I_o is going through the stray inductance and stores energy. Voltage across the overvoltage snubber capacitor is input DC voltage V_d. At turn-off, the MOSFET commutation with freewheeling diode is much more fast than the L_σ response time, i.e. when the MOSFET current goes to zero, the current through the freewheeling diode is essentially I_o. The stored energy in the stray inductance transfers to the snubber capacitor, through the output current loop and snubber diode. According to the energy conservation law and $\triangle V_{DS} = \triangle V_{C,OV}$, it has:

$$\frac{C_{OV} \triangle V_{C,OV}^2}{2} = \frac{L_\sigma I_o^2}{2} \tag{5.11}$$

Set the overvoltage to $0.1V_d$, and the maximum output current as $70A$, which will give an capacitance of $8nF$, a $8.2nF$ capacitor was selected for the initial test. To damp out the voltage ringing, set the critical damp factor as 1, which gives:

$$R = \frac{1}{2d}\sqrt{\frac{L_\sigma}{C_{OV}}} = 2.5\Omega \tag{5.12}$$

The power losses of the snubber can be equivalently calculated from the charging and

discharging procedure:

$$P_{C_{OV}} = 2 * \frac{1}{2} C_{OV} (0.1V_d)^2 f_{sw} = 0.9225W \tag{5.13}$$

A $2W$ carbon composition resistor can be used for snubber resistor, because this type resistor has low self-inductance.

To finalize the snubber circuit, a series lab tests should be done to verify the overall effects.

5.4 Power Losses and Heat Sink

Transistor Power losses are the main factor to dimension the heat sink, which contains two parts: switching power loss and conduction power loss. Under the inverter configuration, the MOSFET conduction power loss and its corresponding freewheeling diode power loss can be calculated according to following equations:
Freewheeling diode power loss:

$$P_D = \frac{U_{F,D} \hat{I}_N}{2} (\frac{1}{\pi} + \frac{m}{4} cos\varphi) + r_D \hat{I}_N^2 (\frac{1}{8} + \frac{m}{3\pi} cos\varphi) \tag{5.14}$$

$U_{F,D}$ is the diode forward voltage drop, r_D is the diode conduction resistance. m is the modulation index $\hat{I}_N$ is the peak output current.

MOSFET power loss:

$$P_T = R_{on} \hat{I}_N^2 (\frac{1}{8} - \frac{M}{3\pi} cos\varphi) \tag{5.15}$$

R_{on} is the MOSFET conduction resistance.

The heat sink dimension should be done under the the worst scenario. According to the datasheet at the maximum temperature, $U_{F,D}$ is 2.3 V and R_{on} 88 $m\Omega$. By substituting the corresponding parameters into Equation (5.14) and Equation (5.15), a power loss of 321 W was calculated for non-parallel SiC MOSFET configuration. For two SiC MOSFET parallel condition, the power loss will be 160 W and $107W$ for 3 paralleled SiC MOSFETs, respectively.

The switching power losses for a sinusoidal PWM modulation inverter is difficult to estimate. An easy way to estimate the switching power losses is linearized from a tested switching power loss. According to its datasheet, the switching power loss is $36W$ at $600V$, $50A$ at $10KHz$, for $750V$ blocking voltage, same current rating and $20KHz$ operating, the switching power losses are calculated to be $45W$. And it will keep the same dissipation level for parallel configurations, due to the current sharing properties.

The relationship between the ambient temperature and power module junction temperature are:

$$T_j = (R_{jc} + R_{hs})P_d + T_{amb} \tag{5.16}$$

R_x stands for the thermal resistance, such as junction to case R_{jc}, and case to heat sink R_{hs}. In the power module, the two parallel thermal resistance of R_{jcM} and R_{jcD} result an effective R_{jc} as $0.1967\,°\mathrm{C}/W$. T_{amb} and T_j stand for the ambient and junction temperature, which are $25\,°\mathrm{C}$ and $150\,°\mathrm{C}$ separately. The thermal resistance requirements for different MOSFET configurations were listed in Table 5.1. "$n\times$" means the numbers of MOSFETs which are in parallel.

To avoid the spreading thermal resistance [40], the heat sink is suppose to be the same size as the SiC power circuit board, which has an area of 300 $\times$ 150 mm^2 as listed in Table 5.1. If a rectangular heat sink with 8 fins along the width direction is selected, and free air convection method is applied, the transferred heat dissipation can be derived according to Newton's Law of Cooling.

$$P = h_c A dT \tag{5.17}$$

P - power transferred in W
A - heat transfer area of the surface in m^2
dT is temperature difference between the ambient and the junction
h_c - convection heat transfer coefficient in $W - m^{-2}(\,°\mathrm{C})^{-1}$, in normal room temperature, the range of air movement in a building is between 0.1 to 2.0 m/s, and normally less than $0.5 m/s$ [41]. It gives an air-heat transfer coefficient of 22 - 25 $W - m^{-2}(\,°\mathrm{C})^{-1}$ [42].

For above selected heat sink, let the height be h, which has a surface area of:

$$A = 2 \times 0.3h + 8 \times 2 \times \times 0.15h = 3h \tag{5.18}$$

Combined with Equation (5.17), the heights of the heat sink are achieved for different SiC MOSFET configurations, see in table 5.1 H_{hs} column.

The size of the heat sink and the total converter are all listed in Table 5.1. The power board has a net height of 50 mm without external heat sink. It is obvious that the parallel MOSFET configuration does not only perform a less power loss but also lead to reduced heat sink size.

Table 5.1: Power Losses and Heat Sink Dimensions

Configuration	P_{cond}	P_{sw}	P_{tot}	R_{hs}	A_{hs}/A_{Conv}	H_{hs}	V_{hs}	V_{Conv}
Unit	W	W	W	$°\mathrm{C}/W$	$mm \times mm$	mm	dm^3	dm^3
MOSFET 1 $\times$	321	45	366	0.1178	300 $\times$ 150	44.4	1.998	4.248
MOSFET 2 $\times$	160	45	205	0.4131	300 $\times$ 150	24.8	1.116	3.366
MOSFET 3 $\times$	107	45	152	0.6257	300 $\times$ 150	18.4	0.828	3.078

5.5 PCB Layout of SiC Power Board

Figure 5.5 and Figure 5.6 are demonstrated the corresponding power circuit board EAGLE schematic and printed circuit board layout. This is used for demonstration purpose. The original designed board is confidential to SmartMotor AS.

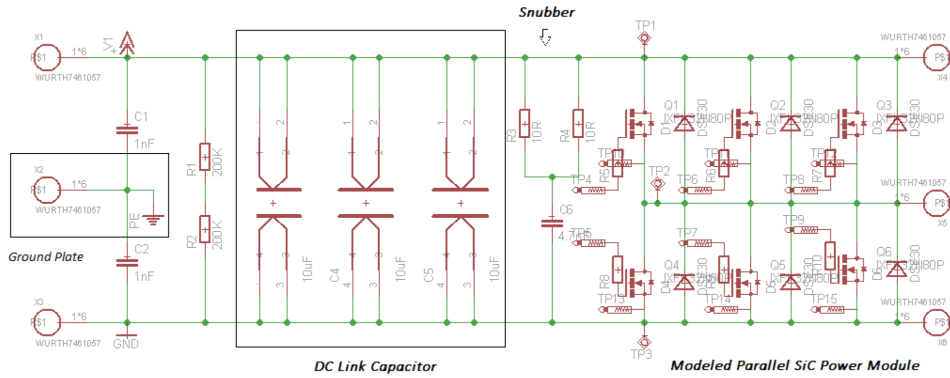


Figure 5.5: Schematics of Demonstrated SiC Board

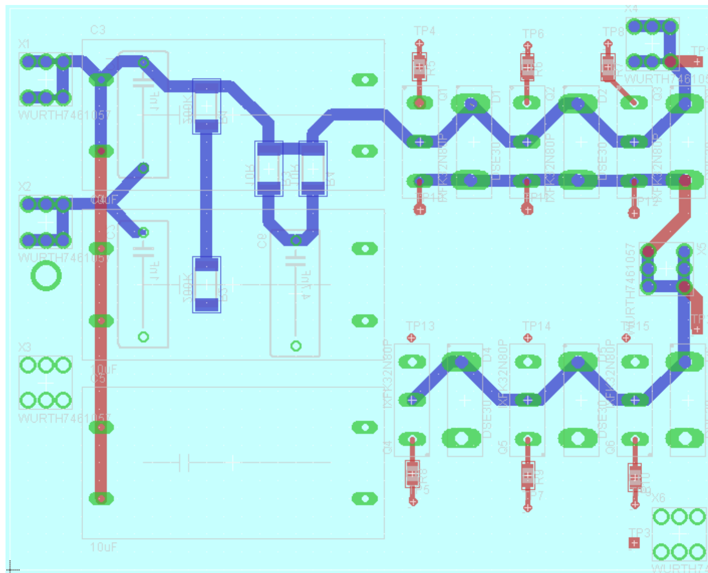


Figure 5.6: PCB Layout of Demonstrated SiC Board

Chapter 6

Laboratory Work Description

Due to the time limitation, the laboratory test has to be specified to the Dual Pulse Test (DPT). The corresponding laboratory preparation work has been documented in this chapter.

6.1 Laboratory Setup

The systematic setup parts for DPTs include:

- Rectified DC Power Supply
- Gate Driver - auxiliary circuit to the main power board
- SiC power circuit Board
- Measurement equipment

Figure 6.1 depicts an overview of the systematic laboratory setup.

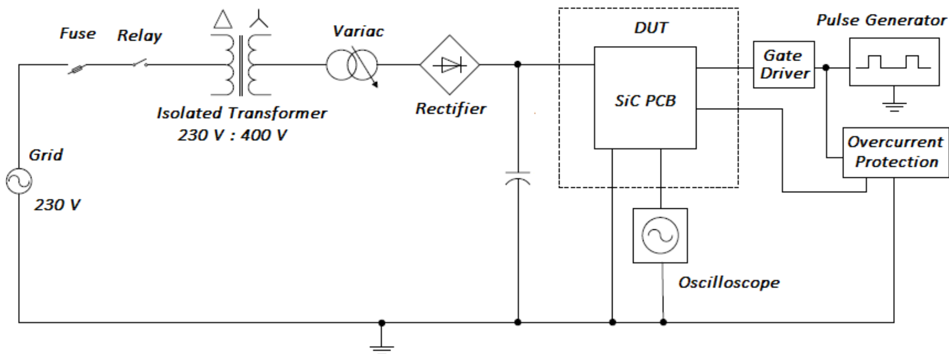


Figure 6.1: Laboratory Setup

6.2 Test Principles of DPT

DPT is commonly applied to study the transistor switching properties. the contents include the switching time and the switching power losses.

A dual pulse signal, in this thesis work which is generated by the Wavetek model 187 pulse generator, is applied to the UTD (Under Test Device). when the first high control signal turns on the UTD, the inductor current linearly rises. The pulse width Δt can be adjusted to reach the target load current (See Equation (6.1)).

$$I_L = \frac{V_{dc}}{L}\Delta t \tag{6.1}$$

Therefore, at the first low level signal the MOSFET is switched off with the desired current. Due to the inductor constitutive law, the current slight drops in the short off period, which can be taken as a constant current. Consequently, the MOSFET turns on with the desired current. By this way, the inductive switching at the desired current and voltage level is realized. Figure 6.2 demonstrates the DPT principle waveforms.

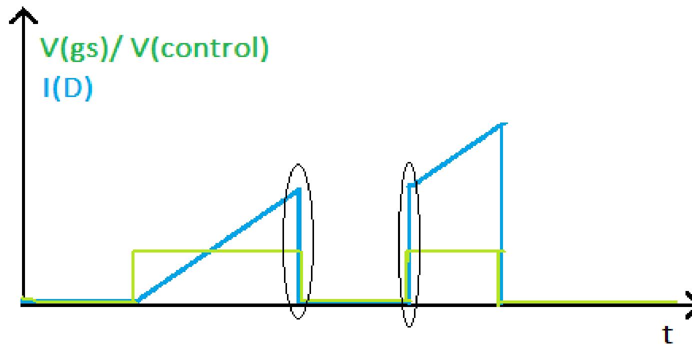


Figure 6.2: DPT Test Principle Waveforms

Switching Energies

Figure 6.3 [1] shows a general transistor switching waveforms and the instantaneous switching power losses. It gives a switching power loss as:

$$P_s = f_s(W_{e(on)} + W_{e(off)}) = \frac{1}{2} f_s V_d I_o (t_{on} + t_{off}) \tag{6.2}$$

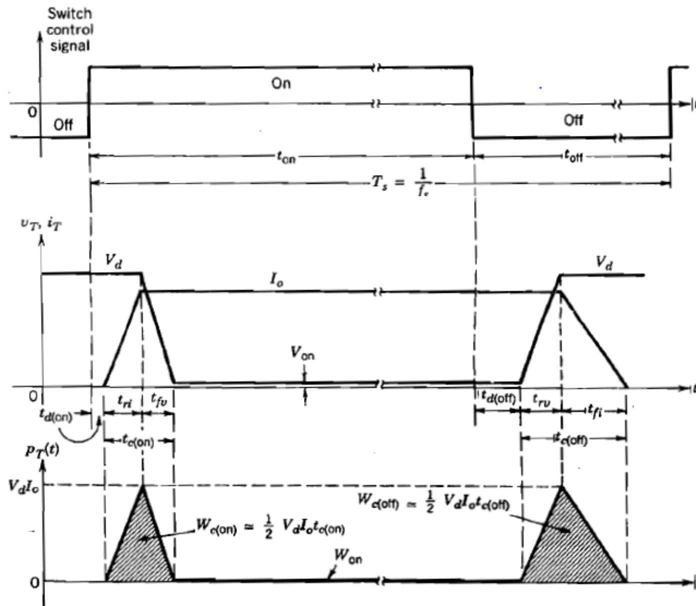


Figure 6.3: Generic Switching Power Loss Characteristics

Switching Times

In [1] the generic switching times are defined as depicted in Figure 6.3. IEC 60747-8 standard has specially defined the MOSFET switching times, as shown in Figure 6.4 [43].

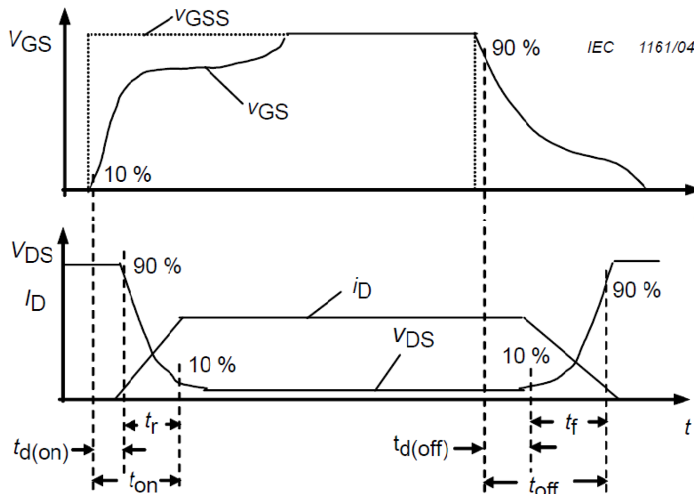


Figure 6.4: Definition of Switching Times

To be practical in the lab test, in this project work, the turn-on time interval has been defined by current rising from 10% to 90% of its final value, or the voltage drop from 90% to 10% of its rated value. In the same manner, the turn-off time it has been measured by current falling from 90% to 10% of its desired switching current or voltage increasing from 10% to 90% of its final value.

6.2.1 Methods of Measurement

1. To avoid the longer measurement ground loop between the gate driver and main power circuit which forms through the oscilloscope, two different systems signals normally are not measured at the same time.

2. The schematic diagram of measurement for three parallel MOSFETs and single device are depicted in Figure 6.5 and Figure 6.6.

   In both test circuits, the inductor current will be recorded by current measurement instrument A1. In Three parallel MOSFET test configuration, A2 was applied to the power module output pins 23 and 24. Theoretically, A2 should be 1/3 of the A1 by the load current sharing property. Therefore, it has been also used to verify the balanced current distribution.

   In the single MOSFET test condition, the MOSFET drain current has been measured through pin 27 and 28. The details of the current waveform can be observed.

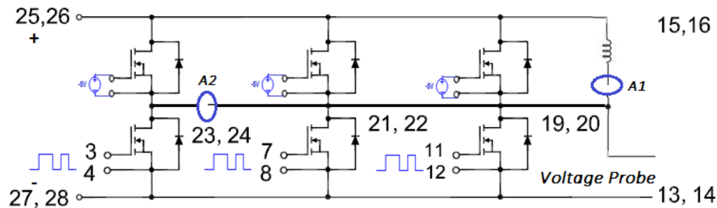


Figure 6.5: Measurement Schematic of Parallel MOSFETs DPTs

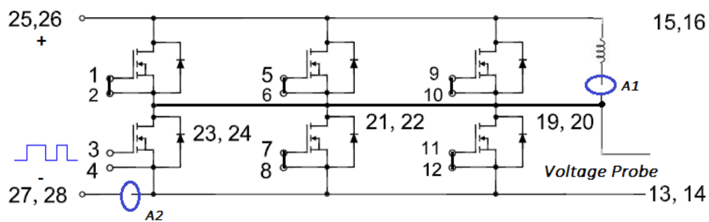


Figure 6.6: Measurement Schematic of Single MOSFET DPTs

6.2.2 Measurement Equipment

1. Oscilloscope
   In this thesis work, Tektronix MSO 2024 oscilloscope was mainly used. It provides advanced debug features, and contains 4 analog and 16 digital channels, with high sample rate up to 1 GS/s. The bandwidth is 200 MHz.

2. Voltage Measurement
   There are two types of voltage need to be measured, the gate SiC MOSFET voltage.

   (a) Single-Ended 10X Passive Probes
   Tekronix TPP0201 and P2220 10X voltage probes are used for the gate voltage measurements. For 10X attenuation both of the probe types have a bandwidth of 200 MHz with input impedance of 10 $M\Omega$, capacitance 16 pF for P2220 and less than 12 pF for TPP0201.

   (b) High-Voltage Differential Probe P5200A
   P5200A active differential probe has two attenuation alternatives as 50X/500X, with the available differential voltage ranges of $\pm 130\ V$ and $\pm 1300\ V$ separately. The differential input impedance is 10 $M\Omega$ and 2 pF. The common mode voltage range is 1300 V with input impedance 5 $M\Omega$ and 4 pF. The bandwidth is 50 MHz.
   It can be used with any oscilloscope and able to be measured under floating circuits with the connected oscilloscope grounded which converters the floating signals to low-voltage ground-referenced signals.

3. Current Measurement
   In this thesis work, Rogowiski coil CWT 06B current traducer from Power Electronics Measurement Ltd. was selected for current measurement. It is a state of the art wide-bandwidth as current probe, which is ideal for power electronics development work since is combines an easy to use thin, flexible, clip-around coil with an ability to accurately replicate fast switching current waveforms.

   The key features include: 300 mA to 300 kA measurement range with lower than 2 mV DC offset over the whole operating temperature range; typical bandwidth from 0.1 Hz to 16 MHz ; the coil voltage isolation is 1 kV and tolerates a peak isolation voltage up to 10 kV.

   However, comparing to the wider bandwidth 200 MHz oscilloscope and 50 MHz voltage probe, $16MHz$ bandwidth will be the limitation factor for measurement system. Coaxial shunts or split core AC/DC current probes with wide bandwidth should be applied capably with the voltage probe and oscilloscope. However, due to the measurable space limitation and the equipment availability, Rogowski coil had to be selected for most of the thesis work. In the same time, its bandwidth is 3 orders higher than the rated 20 kHz bandwidth is also acceptable.

6.2.3 Equipment Calibration

To verify the measurement accuracy, the calibrations have been done with Fluke 5500A calibrator at NUNT-Elkraft service lab. It verified all the measurement equipment errors were in the reasonable range.

6.2.4 Delay of Rogowski Coil Transducer

It is commonly recognized all current measuring techniques have certain time delay comparing to the voltage measurement, which makes the phase shift between measured voltage and current. To improve the accuracy of losses calculation, delay time of the current measurement has to be compensated. In this thesis work, which was realized in a simple circuit as depicted in Figure 6.7 [44].

The test circuit has been constructed with minimum stray inductance. As short as possible wires, metalized polypropylene capacitor and carbon film resistor were applied to limit the parasitic inductance.

As Figure 6.8 demonstrated, the average current delayed response time are 11.8 ns and 13.8 ns for Rogowski SM12-023 and SM12-024, respectively.

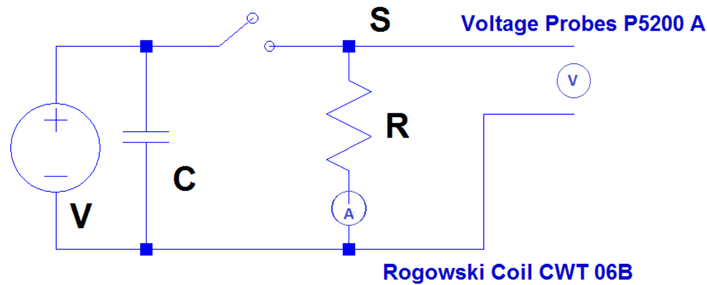


Figure 6.7: Time Delay Calibration Setup

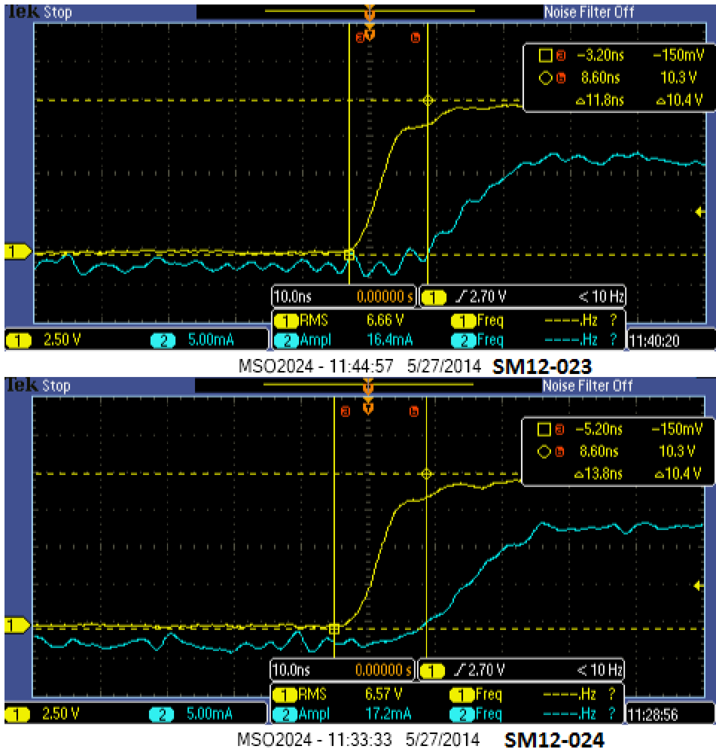


Figure 6.8: Test Results of Time Delay

Chapter 7

LTspice Simulation

LTspice IV is provided by Linear Technology, it is a high performance SPICE simulator, schematic capture and waveform viewer with enhancement models for easing the simulation of switching regulators. It suits for electronics and power electronics circuit. The LTspice SiC power MOSFET and diode models were supplied by Subhadra Tiwari from Wastslia AS and by Richard Lund from SmartMotor AS.

7.1 DPT Simulation

As mentioned in DPT section, the purpose of dual pulse test is to dimension the SiC MOSFET switching properties. The simulation with/without parasitic elements and snubber circuit cases were studied with LTspice simulation.

7.1.1 Ideal DPT Simulation

An ideal DPT case has been first simulated, no parasitic inductance or capacitance are included (See Figure 7.1). Correspondingly, the snubber circuit has not been considered. Applied voltage was set to 600 V and current set to around $10A$ at the first turn-off and second turn-on switching periods. The simulation results see Figure 7.2.

Figure 7.3 shows the details of first turn-off (Up)and second turn-on (Low). By calculation it gave E_{off} 0.23 mJ and E_{on} 0.18 mJ with turn-on around 89.25 ns and turn-off time 68 ns. The switching power losses of a 20 kHz system will be 8.2 W.

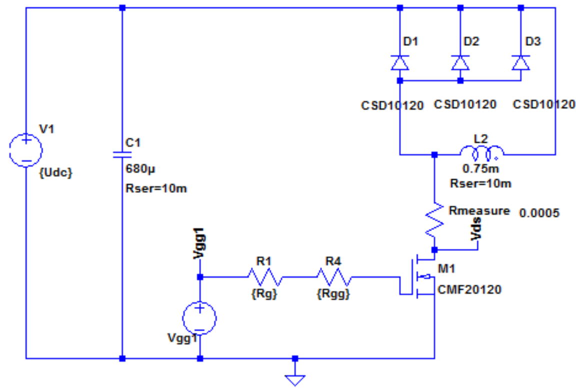


Figure 7.1: Ideal DPT Simulation Schematic

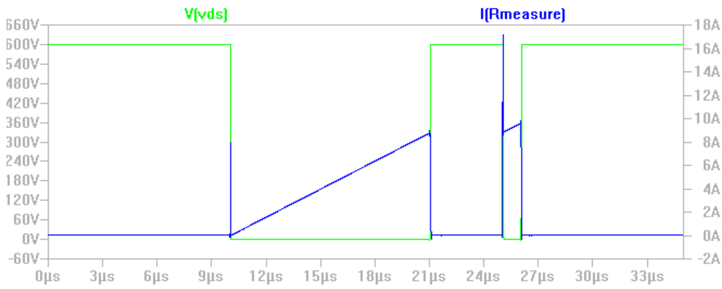


Figure 7.2: Simulation Results of Ideal DPT

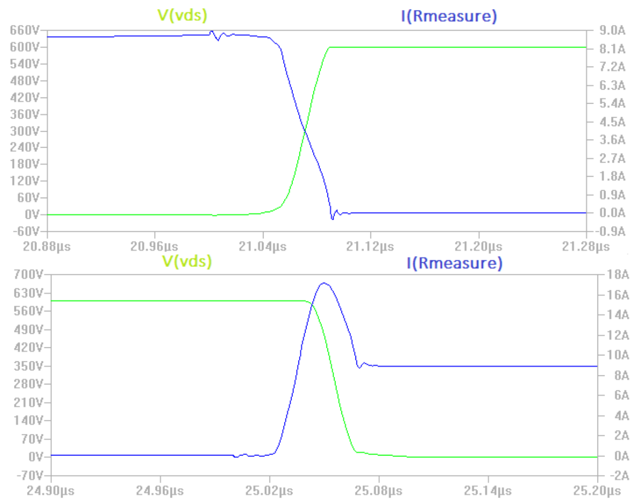


Figure 7.3: SiC MOSFET Switching Waveforms of Ideal DPT Simulation

7.1.2 Parasitic Inductance Included Simulation

No Snubber Included

First the snubber circuit is not included. Due to the presenting of the energy storage inductance, significant voltage and current oscillations are observed (See Figure 7.4). The effect of a proper snubber circuit is simulated in next section.

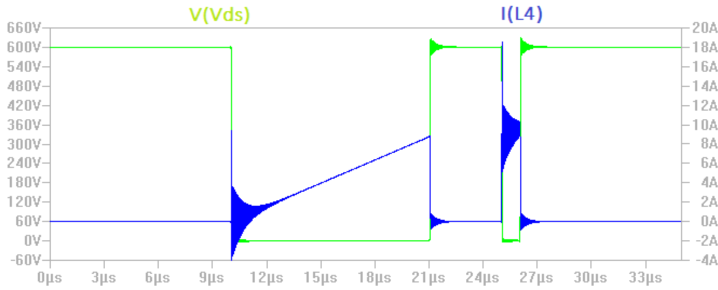


Figure 7.4: DPT Simulation Result with Parasitic Inductance

Parasitic Inductance Included

Figure 7.5 gives the assumed stray inductance distribution. Two RC snubber circuits with 10 nF, 10 Ω and 4.7 nF, 10 Ω are simulated. Their simulation results have been listed in Table 7.1. The switching waveform for 4.7 nF, 10 Ω snubber circuit has been documented in Figure 7.6. The detailed first turn-off and second turn-on waveform see Figure 7.7.

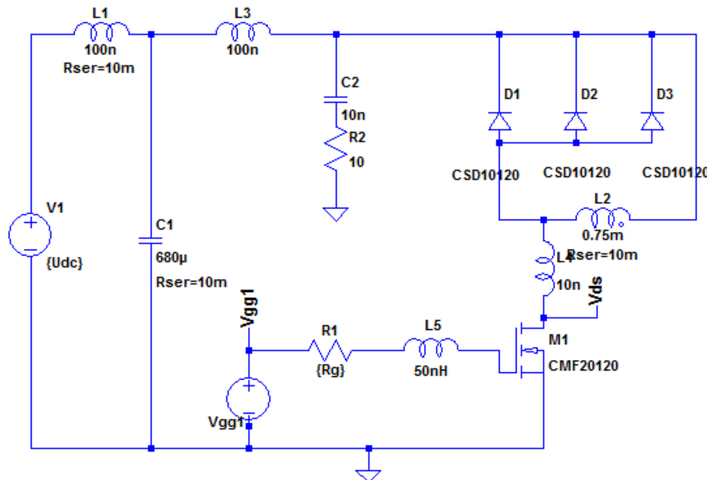


Figure 7.5: Stray Inductance Distribution in DPT Circuit

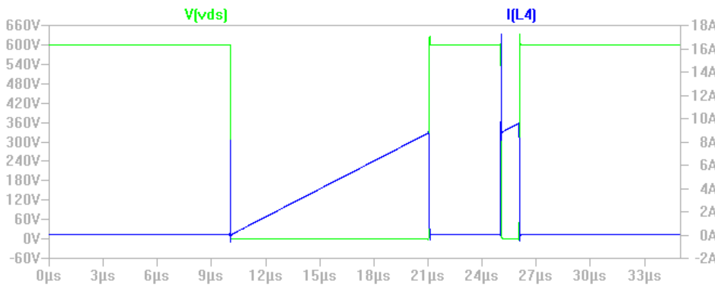


Figure 7.6: DPT Simulation Results with Snubber Circuit

By studying the different simulation cases and their corresponding results, it can be concluded:

1. When taking the parasitic inductance into simulation, the snubber circuit has to be applied. The oscillation induced by the stray inductance can be eliminated with a proper RC snubber.

2. The overvoltage is observed when the stray inductance is taken into account. The larger snubber capacitor results in a smaller overvoltage. Whereas, the corresponding snubber power losses are increased, see Table 7.1. Therefore, overvoltage and power losses have to be compromised as a trade-off pair before the implementation of snubber circuit.

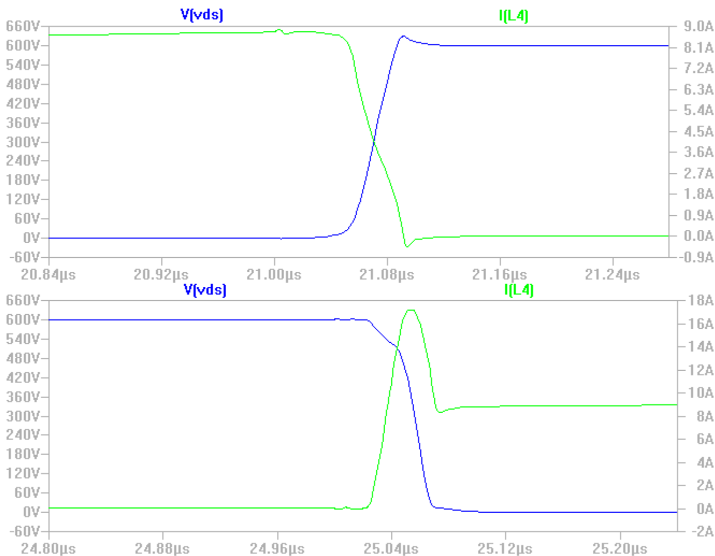


Figure 7.7: Turn-off and Turn-on Switching Waveforms with Snubber Circuit

3. Comparing to the ideal simulation case, extra SiC MOSFET switching power losses are induced. Overvoltage increases turn-off power loss. The snubber capacitor

discharge current during the MOSFET on period increses the MOSFET current. Consequently, turn-on power losses increases. Therefore, a proper PCB layout with minimized parasitic elements is benefit for the power converters.

Table 7.1: Overvoltage and Power Losses of DPT Simulation

$C_s(nF)$	ΔV (V)	$\Delta V\%$	$P_{on}(W)$	$P_{off}(W)$	$P_s(W)$	$P_{tot}(W)$
0	0	0	3.60	4.60	0	8.20
4.7	31.95	5.33	3.82	4.74	0.096	8.656
10	28.63	4.77	3.84	4.75	0.164	8.754

7.2 Gate Configurations and DPTs

In previous section, the simulation gate was constructed by a 11.7 Ω gate resistor. A few different gate configurations will be simulated in this section. Such as a smaller 6.8 Ω gate resistor, and a RC combinations. The aim is to investigate the relationship of the SiC MOSFET switching properties and the gate configurations. The simulation results is performed in Table 7.2. The corresponding simulation schematics can been found in Appendix C.

The simulation have been done under the stray inductance and snubber circuit included condition. The snubber circuit is selected the 4.7 Ω and 10 Ω RC combination. The system operational frequency is 20 kHz, the same as in the previous section.

Table 7.2: SiC MOSFET Power Losses with Different Gate Configurations

Gate	$t_{off}(ns)$	$t_{on}(ns)$	$P_{off}(W)$	$P_{on}(W)$	P_{tot} (W)
R 11.7 Ω	84.74	72.00	4.74	3.82	8.56
R 6.8 Ω	72.00	55.43	3.99	2.93	6.92
R 6.8 Ω // (C 22 nF + R 2 Ω)	54.59	44.04	3.00	2.31	5.31

According to Table 7.2 the switching time reduced by using a smaller value gate resistor, the same as the switching on/off power losses. These properties are even improved by the speed up capacitor combinations.

In the other way, the $\frac{dv}{dt}$ and $\frac{di}{dt}$ rates are increased correspondingly. During the lab work this must be controlled into a reasonable condition to avoid the converter malfunction.

7.3 Overcurrent Protection

One potential problem of the DPT is overcurrent fault, since the DPT circuit is very inductive, there is not enough resistance to fast damp down the inductor current in each switching period.

According to constitutive law, when a constant voltage across inductor, the current will be:

$$i = \int_{t_1}^{t_2} \frac{V}{L} dt + i_0 = \frac{V}{L}(t_2 - t_1) + i_0 \tag{7.1}$$

An ideal inductor carries a constant current when no voltage across it. The freewheeling diode has low forward conduction resistance. Therefore, the inductor current slightly drops, which can be closely taken as constant. In the other words, it takes quiet long time to finally damp out the inductor current. Otherwise, the current will keep building up (See simulation Results in Figure 7.8). The high current operation may lead to overheat of power module which causes a permanent damage or performance variations. It is suggested that for high current test, the DPT should be repeated in an hour period to avoid overcurrent. Whereas the hourly repeated dual pulse test is impossible to realize in the thesis work, since the minimum frequency available on WaveTek is 0.004 Hz namely which repeats around every 4.2 minutes.

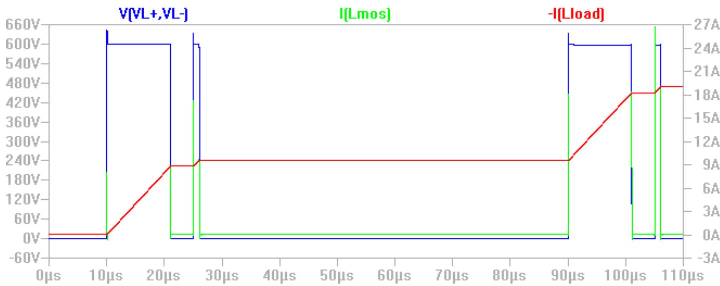


Figure 7.8: Current Build Up in DPT

7.3.1 Current Protection Principle

As depicted in Figure 7.8, the current through load and MOSFET only build up when MOSFET M1 is conducting. During its off time, the current keeps to the prior turn-off values and slowly damps out. The constant off(different from turning off during switching operation) conditions can be realized as the following cases:

1. External circuit loop open
2. MOSFETs off

With these two equivalent condition in mind, the over current protection can be realized by imitating the two conditions.

7.3.2 External Circuit Open Protection

This is an external protection system, which can be easily realized by cutting off the circulating current loop. The implementation can be achieved by adding the protection products into the circuit, such fuses and relays .

Whereas, the long response time limits to use such kinds of protection. For example, Fast-Acting (also named as "Normal-opening") fuses has typical opening times at 500% of the fuse rating range from 0.05 s to approximately 2 s [45]. For instantaneous turn-off relay, the time between applying a command signal to the control circuit and the output circuit turning on is typically 20 microseconds. As demonstrated in Equation (7.1), if the applied turn-on voltage on a 100 μH inductor is 600 V, the current increasing rate will be 6 $A/\mu s$. For an DPT with pulse width as 10 μs, more than 60 A will build up before the fuse or the relay acts to open the circuit. In this way the external current protection is not sufficient.

7.3.3 MOSFET Off Protection

The MOSFET switch-on and switch-off are controlled with electronics based gate driver, the response time compares to mechanical protection will be much faster.

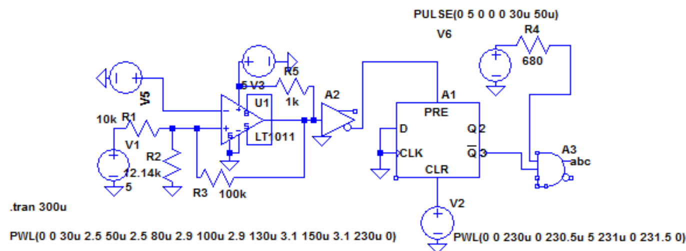


Figure 7.9: Overcurrent Protection Schematic

In Figure 7.9, the principle and schematic of current protection was depicted. The voltage source V5 is used to simulated the ASC758 current sensor output, which has 2.5 V offset voltage, with current sensitivity 20 mv/A. Hysteresis comparator model LT1011 was set with V_{thH} of 2.84 V and V_{thL} at 2.59 V. The responding high threshold current is $17A$ and low threshold 3 A.

When the sensed output current is less than 17 A, $V5$ is less than V_{thH} the nor gate A2 gives a low signal, which is inactive for D flip flop A1, and results in a high $\bar{Q}$. A true $\bar{Q}$ and the control signal from pulse generator operate through the add gates A3 with will gives the value of the control signal. Consequently, under the normal operation, the SiC MOSFET is controlled by the pulse generator signal.

When current exceeds the high threshold level, $V5$ is higher than V_{thH}, the $\bar{Q}$ outputs a low signal. $\bar{Q}$ compares with control signal through A3 will give a constant low which controls SiC MOSFET off.

The reset of the D flip flop A1 only available when both the sensed current is smaller than low threshold current and an external CLR high is applied. It avoids a second turn on before the current totally dies out. The corresponding function table is given in Table 7.3 and the simulation results see Figure 7.10.

Table 7.3: Function Table of Overcurrent Protection

Function	State	PRE	CLR	$\bar{Q}$	CTR	Result
Normal	$V5 < V_{thH}$	0	0	1	0	0
Normal	$V5 < V_{thH}$	0	0	1	1	1
Faults	$V5 > V_{thH}$	1	0	0	0	0
Faults	$V5 > V_{thH}$	1	0	0	1	1
Fault CLR	$V5 < V_{thL}$	0	1	1	-	-
Fault CLR	$V5 < V_{thL}$	0	1	1	-	-

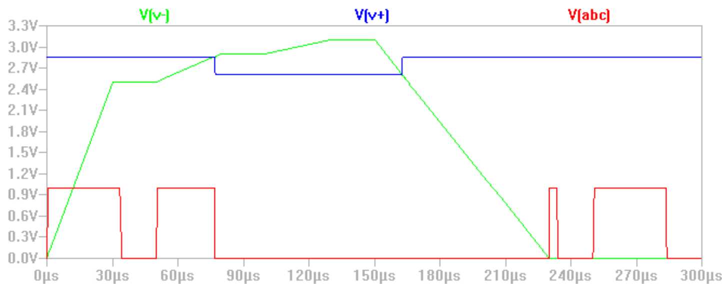


Figure 7.10: Simulation Results

In this way an overcurrent protection is realized. The response time is significantly improved, the analog ACS758 has 4 μs response time. The digital circuit in Figure 7.9 has a response time less than 300 ns. In this way the theoretically maximum current goes through the MOSFET is 43 A. Compared to the 50 A rating current, the overcurrent protection is reasonable.

Chapter 8

Laboratory Test and Measurement

8.1 Initial Measurement

The initial DPT test was done on the three parallel SiC MOSFETs configuration, as depicted in Chapter 6 Figure 6.5. A 1 mH inductor load was connected in. Lower SiC MOSFETs were the UTDs (Under Test Devices). The same gate driver signal were applied to the UTDs through each smaller series damp resistor. The corresponding gate configuration see Figure 8.1.

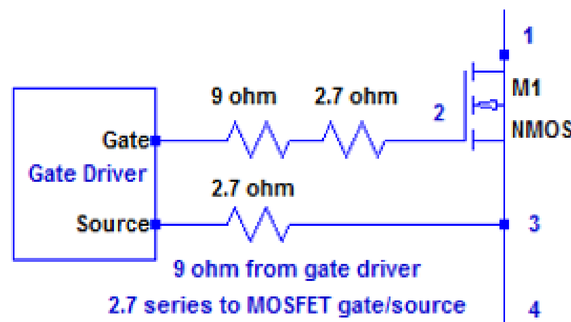


Figure 8.1: Initial DPT Test Gate Configuration

The voltage probe positive was clipped on the output plate which is on the same plate as power module pin 23 and 24. The negative probe clipped on the DC voltage input negative terminal on SiC power board. Two Rogowski coils were connected to the output pins 23 and 24. This arrangement aims at detecting the load current sharing property. The switching time could be recorded by the MOSFET voltage rising and falling.

Figure 8.2 and Figure 8.3 depicted one of the initial lab test results, with a low DC voltage 40 V and a low inductive switching current 3.2 A. The yellow waveform was the voltage

across under test MOSFETs, the dual pulse time interval can be indicated from voltage waveforms. The green was the inductor load current. The blue was the current through the SiC MOSFETs with output ports 23 and 24 in the power module.

By analyzing the recorded switching waveforms, the common issues were found as the severe oscillation and ringing issues during the switching period. For some special waveforms, the unbalanced load current sharing has been detected.

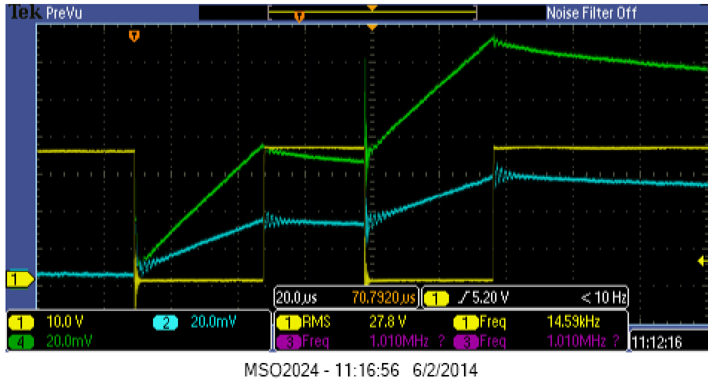


Figure 8.2: Initial Measurement Results

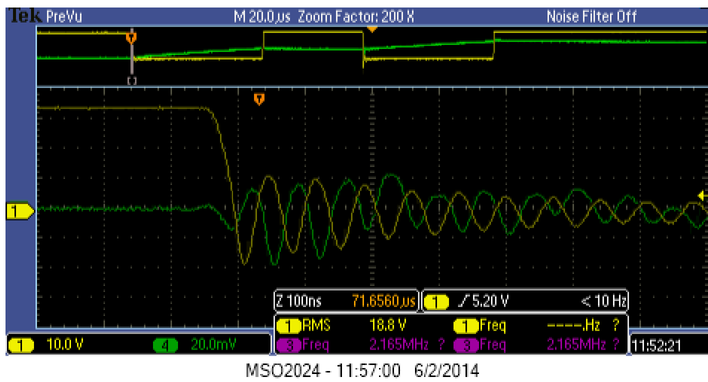


Figure 8.3: Voltage and Current Oscillations

8.2 Analyzing of Oscillation Issues

The possible reasons of the oscillations has been analyzed, which include the measurement instrument, the corresponding external supporting system and SiC power circuit board.

8.2.1 Measurement Instruments

The bandwidth limitation, the instrument impedance and induced measurement impedance due to placement are all the possible reasons of the oscillation.

Bandwidth Limitation

As introduced in Chapter 6.2, all the individual measurement equipment has a wide enough bandwidth compared to the rated 20 kHz system frequency. Whereas the system bandwidth will be derated due to the cascaded connection of probe and oscilloscope. The effective measurement bandwidth has to be recalculated according Equation (8.1) [46].

$$BW_{sys} = \frac{1}{\sqrt{\frac{1}{BW_{osc}^2} + \frac{1}{BW_{probe}^2}}} \tag{8.1}$$

Therefore, the equipment systematic bandwidths become:

- Single-ended 10X passive probe: 141 MHz
- Differential voltage probe P5200A: 48.5 MHz
- Rogowski current transducer: 15.95 MHz

The measured electrical signal accuracies of amplitude and phase depend on the bandwidth. As a common rule, the precision of phase measurement demands a higher bandwidth than amplitude. Normally, 10 times to the highest equivalent frequency [46] bandwidth is required. Theoretically, the 15.95 MHz is enough for a 20 KHz switching frequency system.

Induced Measurement Impedance

First, the connection of an external measurement equipment will somehow influence the original circuits, due to the paralleled instrument impedance. Besides the instrument impedance, the measurement parasitic elements have to been taken into account, such as the stray inductance due to the probe wires, the stray capacitance due to the clip connection.

Second, when more than one oscilloscope analog channel are used into test, the interactive common ground might be formed, which results the unpredictable ground impedance for different measurement systems and the under test circuit.

8.2.2 The Supporting System

The supporting system include the external DC voltage supply and gate driver.

Voltage Supply

The DC voltage was rectified from an isolated voltage transformer. The copper coil within the isolated transformer has formed a capacitive connection to ground. The voltage is then

supplied to the converter input terminals through conductors, which is a source of induced inductance. Therefore, a LC oscillation loop is formed before the power transfers to next section. If the DC-link capacitor is not sufficient enough, the corresponding oscillation will influence the followed switching system.

To eliminated the power side oscillation influence, the supplied voltage was tested at the power converter input terminal, a clean and stable waveform was observed (See Figure 8.4). Thereby, voltage supply is not the source of oscillation.

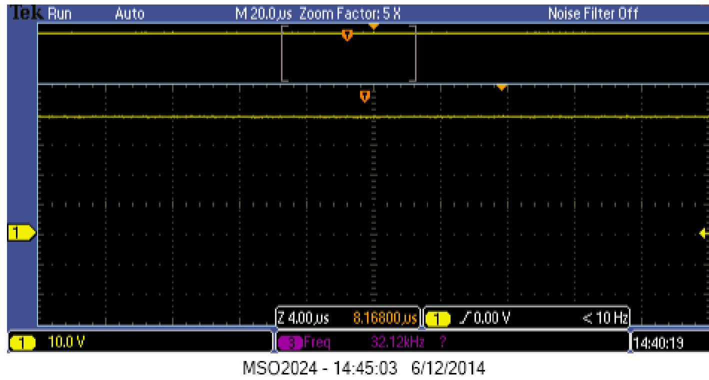


Figure 8.4: Input Voltage Waveform

Gate Driver

Gate driver is one of the suspects of oscillation. The test of charing and discharging a 28 nF metalized polypropylene capacitor has been done to verify its influence. The detail gate voltage and current waveform see Figure 8.5 and Figure 8.6.

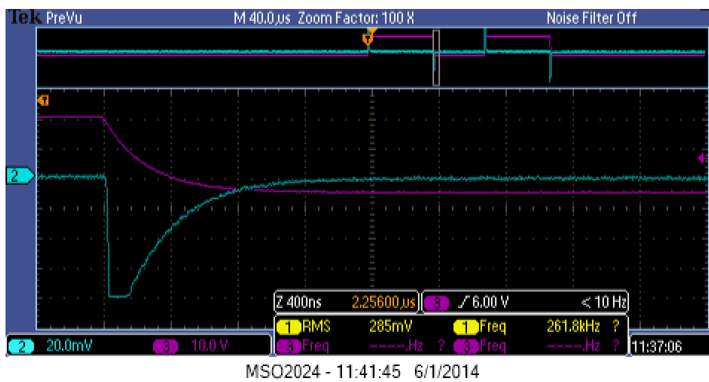


Figure 8.5: Gate Voltage Waveform with a Capacitor Load - Discharging

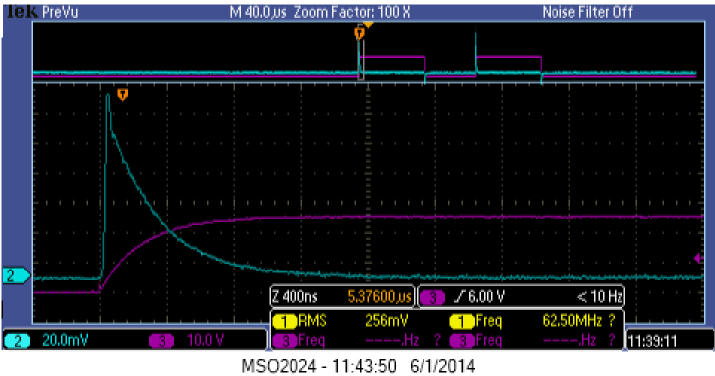


Figure 8.6: Gate Voltage Waveform with a Capacitor Load - Charging

There are no oscillation have been observed from the gate driver terminal. Therefore, the suspicion of gate driver has been eliminated.

8.2.3 PCB Layout of SiC Power Board

Parasitic Inductance

The PCB layout will influence the parasitic parameters. The induced inductance and capacitance may trigger oscillations and ringing. Therefore, in an optimized design, the PCB layout should be done carefully to minimize the parasitic elements.

Whereas, due to the wrong dimension of the SiC Power Circuit Board (PCB), the parasitic inductance was not optimized. The main problems are the mounting of the SiC power module and gate driver placement. Figure 8.7 shows that the power module was mounted through extended power pins. The length is approximately 2 cm. In this case the induced inductance mainly distributed on the gate-source and drain-source.

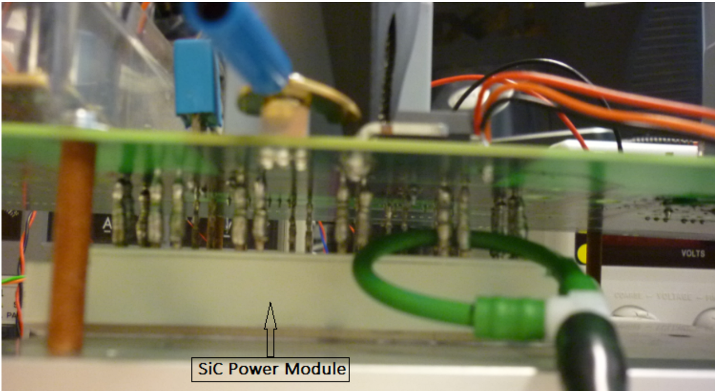


Figure 8.7: Mounting illustration of SiC Power Module

Furthermore, the pitch dimension on the SiC power board does not match with the CREE's commercial SiC MOSFET gate driver. In addition, due to the hand soldering limitation a bridge leg gate driver is impossible to be realized on the power board. The external designed bridge leg gate driver has to be used. However, it is connected through about 5 cm twisted wires. It will adds on the gate-source stray inductance.

Parasitic Capacitance

The mounted parasitic capacitance, stray capacitance and the SiC power module inherent capacitive properties are all the possible oscillation element. The three paralleled upper capacitance with opened drain and source terminal will triple the drain-source capacitance, this is the case for three lower parasitic capacitance during their off intervals.

Besides the LC oscillations, the drain-source capacitance might slow down the MOSFET turn-off speed. An even obvious slow down effect might be observed at the low current condition.

Simulation of Parasitic Elements

Taking these factors into account, a simulation with possible parasitic gate-source inductance and drain-source capacitance had been simulated. Obvious oscillations and slow turn-off time had been observed.

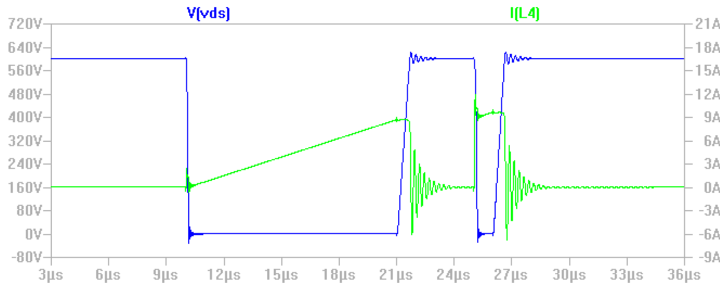


Figure 8.8: Simulation Results with Parasitic Elements

8.3 Load Current Sharing Issues

As discussed previously, in some captured waveforms, the currents through three parallel MOSFETs do not fulfill the 1/3 relationship. More repetitive tests have been done and it has been studied that the measured current is directly influenced by the relative position of the under measured conductor and the surrounded Rogowiski coil. By fixing the conductor into the middle of the coil and repeating the test. The exactly 1/3 current division as Figure 8.9 has been measured.

Thereby, the load current balanced sharing capability has be verified. In addtion, the influence of the Rogowski coil measurement has been eliminated by properly dealing with their relative positions.

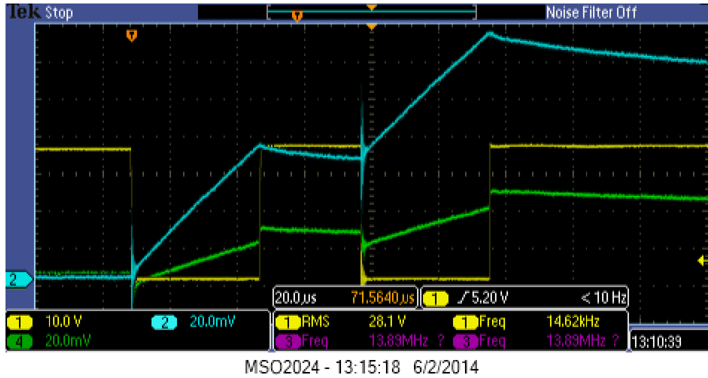


Figure 8.9: Balanced Load Current Sharing Capability

8.4 Problem Diagnosis and Corresponding Solutions

According to previous discussion, it can be diagnose the problem of power converter oscillations are due to the parasitic elements. In addition, the measurement equipment might induce the measured oscillation. For these reasons, the corresponding solutions were proposed.

8.4.1 Improvement of Measurement Equipment

To eliminate the measurement errors, some equipment have be replaced. Tektronix DPO 4104 1 GHz bandwidth oscilloscope and TCP0030A 120 MHz current probe had been applied for the rest laboratory work. The two types voltage probes kept the same.

Due to the limited space, only the inductor current was available to measure. In addition, it has to discard the Rogowski coil measurement, since obvious oscillations has been induced when it was applied to a verified no oscillation circuit.

The corresponding system bandwidths became:

- Single-ended 10X passive probe: 196.12 MHz
- Differential voltage probe P5200A: 49.94 MHz
- Tektronix current probes: 119.15 MHz which is about 8 times of the previous Rogowski Coil traducer system.

8.4.2 Improved of Gate Configuration

To eliminate the oscillations which induced by parasitic inductance and capacitance, a 100 Ω gate resistor has been applied on the purpose of damping down the oscillations. An anti-parallel diode had arranged across the gate resistor to finalize a fast turn-off operation. The corresponding gate configuration is depicted in Figure 8.10.

Due to the verified current balance sharing capability, the DPT was arranged to a single MOSFET configuration, the test schematics has been demonstrated as Figure 6.6. Current probe A1 and voltage probe were attached to the power circuit board. The gate voltage was detected on the gate source pins on the SiC power module.

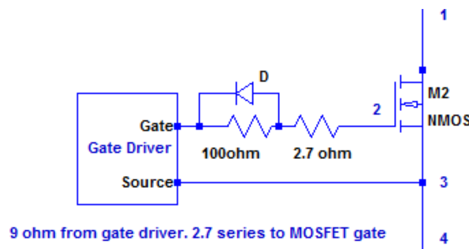


Figure 8.10: Improved Gate Drive Configuration

8.4.3 Oscillation Free Waveforms

One of the improved measurement results with 500 V DC voltage and 10 A inductive switching current was demonstrated in Figure 8.11, Figure 8.12 and Figure 8.13 depict the details of first tun-off and second turn-on waveforms.

The upper purple is the gate-source voltage waveform. The blue waveform despites the voltage across the under test SiC MOSFET. The green is the measured inductor current. The current through the SiC MOSFET at turn-off and turn-on interval can be indirectly read through the inductor current.

It proves, with the new gate configuration and improved measurement instruments, the voltage and current oscillations were effectively eliminated. The overvoltage has not be observed which is due to the 10 Ω and 4.7 nF RC snubber circuit. Nevertheless, the fast switching had not been realized. A turn-off 163 ns and turn-on 100 ns were recorded.

The slow turn-off speed is due to the parasitic drain-source capacitances. In a paralleled SiC MOSFET configuration, the capacitance will be three times higher, which results a even slower switching properties. The other types of induced capacitance might also enforce this effect.

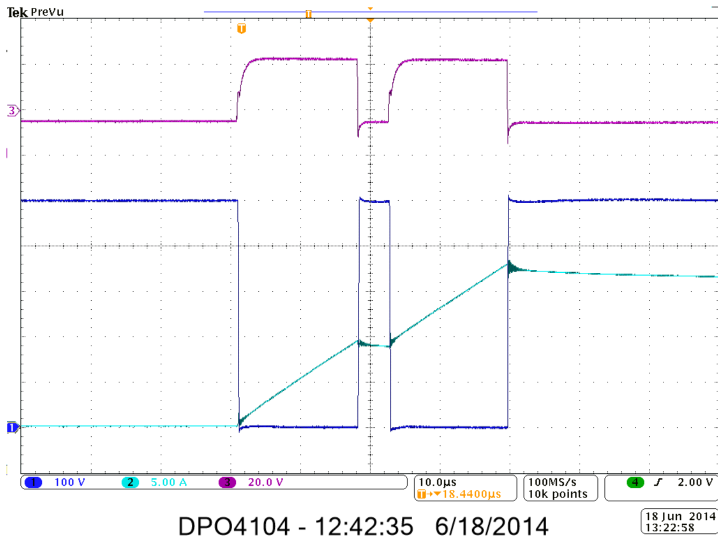


Figure 8.11: SiC MOSFET DPT Waveforms

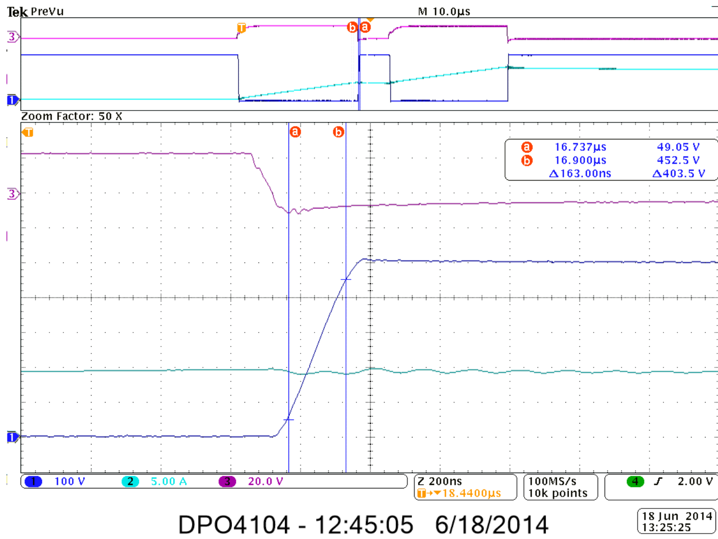


Figure 8.12: SiC MOSFET DPT First Turn-Off Waveforms

A fast turn-on was expected to be realized by changing the un-optimized larger gate resistor. Whereas, the oscillations will arise when the resistor is smaller than 100 Ω.

To finalize the switching performance of the power converter, a systematic optimized PCB layout has to be first arranged. The components and PCB board should be verified to match

each others dimension. A better solution for the gate driver will be achieved by compacting it to the power circuit board with the shortest stray length.

Due to the limited time, this is impossible to be done at this stage. Therefore, the results of switching energy losses in next section has been documented according to the un-optimized power converter configuration.

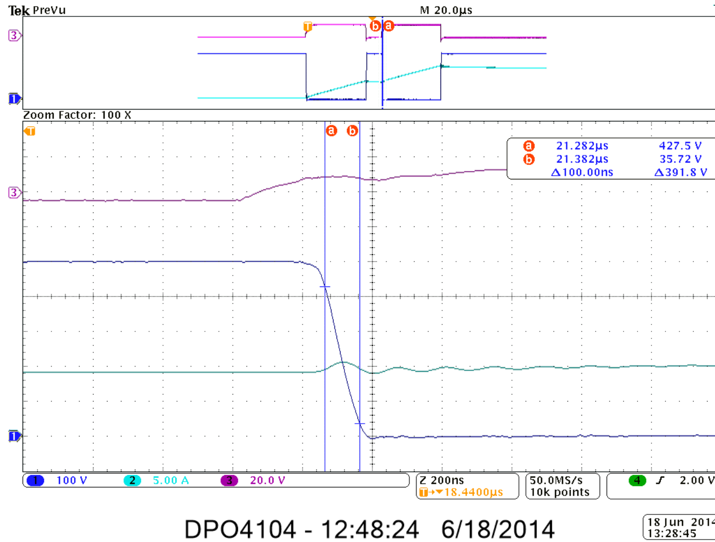


Figure 8.13: SiC MOSFET DPT Second Turn-On Waveforms

8.4.4 DPT results

The DPT results of switching time and switching energies had be documented in this section. Three different voltage levels: 40 V, 300 V and 500 V with different current level tests had be implemented. To match a reasonable operational voltage and current rating, the 300 V and 500 V voltage level tests had be recorded in this thesis work.

300 V Voltage Test Results

Table 8.1: Switching Properties under 300 V Voltage Test

Current (A)	T_{off} (μs)	E_{off} (μJ)	T_{on} (μs)	E_{on} (μJ)	E_{tot} (μJ)
3	369.8	166.4	81.8	36.8	203.2
6	201.0	180.9	80.0	72.0	252.9
9	139.0	187.7	80.0	108.0	295.7
12	97.0	174.6	79.0	142.2	316.8

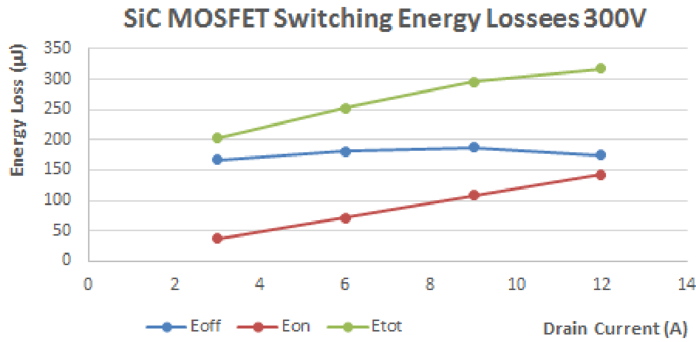


Figure 8.14: Energy Losses under 300 V Voltage Test

500 V Voltage Test Results

Table 8.2: Switching Properties under 500 V Voltage Test

Current (A)	T_{off} (μs)	E_{off} (μJ)	T_{on} (μs)	E_{on} (μJ)	E_{tot} (μJ)
3	490.9	368.2	99.9	74.9	443.1
6	250.0	375.0	103.0	154.5	529.5
9	163.0	366.8	100.0	225.0	591.8
12	124.0	372.0	100.0	300.0	672.0

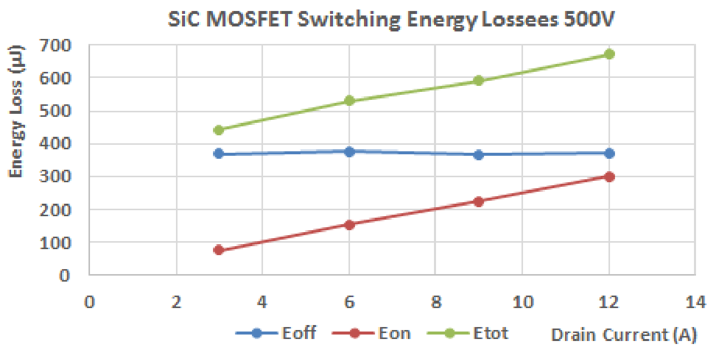


Figure 8.15: Energy Losses under 500 V Voltage Test

From Table 8.1, 8.2 and Figure 8.14, 8.15, following conclusions can be concluded:

The turn-off times are reducing with the increasing grain current. Therefore, the turn-off power losses keep the same or slightly decrease. The turn-on times keep almost the same.

Correspondingly, the turn-on power losses increase linearly with the drain currents. The overall power losses increase following the tendency of turn-on energy losses.

The increased drain current will charge the parasitic drain-source capacitance faster. Therefore, the turn-off slow-effective is be reduced. This leads to the same or even slightly decreased turn-off power loss with increased current.

Chapter 9

Conclusion and Future Work

9.1 Conclusion

This study produced a review of a commercially available SiC MOSFET power module. This is done through theoretical review of the topic, and through simulation and laboratory tests of a designed power circuit board.

LTspice, a power electronics design software has been used for the gate driver design and Dual Pulse Test (DPT) simulation. Additionally, CadSoft EAGLE PCB (Printed Circuit Board) Design Software had be studied to implement the gate diver board.

A bridge leg gate driver with 700 ns dead time and 20 V/-5 V on/off gate-source voltage was designed and manufactured via printed circuit board technology. Thereafter, the switching properties of three paralleled SiC MOSFET and single transistor were investigated in detail. Additionally, a digital overcurrent protection card was implemented to protect the power module for the DPT.

The target gate driver was reliable for on and off gate-source voltage supply. The capacitor load test of gate driver verified it can charge and discharge the tested capacitor in various speed. Fast sourcing and sinking capabilities can be realized by various gate configurations. An optimal combination to realize fast charging and discharging is small gate resistor with in parallel speedup capacitor which is serially connected with a small current limited resistor. In addition, a low forward voltage drop, anti-parallel diode helps to fast discharge.

Components layout is the most important factor for switching power devices. Parasitic inductance and capacitance should be minimized. An un-optimized layout will induce larger parasitic elements, which causes excessive voltage and current oscillations and ringing and maybe significantly limited the fast switching capability of SiC MOSFET. This was the case during the study. The stray inductance was induced due to the relatively long conductors which connected two separated SiC power circuit board and gate driver board.

Besides, the unmatched module pins and PCB holes leaded to extended pin length. Parallel SiC MOSFET configuration induced stray capacitance between the drain and source, which slowed down the MOSFET turn-off speed, which was even slower with smaller drain current.

In order to reduce the oscillations and ringing of the converter, a 100 ohm gate resistor was applied with an anti-parallel Schottky diode. However, there was no way to improve the switching speed with a required 100 ohm gate resistor and inherent stray capacitance.

In addition, high bandwidth measurement instruments were required to capture accurate measurement results. High bandwidth current probes should be used for current measurement. Rogowski current transducer would induce systematical measurement oscillations.

9.2 Future Work

Due to the short amount of time allotted for the laboratory work, plenty of work can still be done. The following tasks can be done for further work:

1. Reconstruct the gate driver and power circuit board. The optimal placement of the gate driver should be taken into account. The gate driver should be located as close as possible to the gate and source pins of power module.
2. Improve the dimension of the holes of the power circuit board to fit the SiC MOSFET power module.

When tasks 1 and 2 are completed, the following tests and/or measurements can be performed on the laboratory setup:

3. DPTs with different voltage and current level and also with different ambient/junction temperatures.

4. On state power losses measurement.

5. Power converter prototype tests.

6. Replace the standard devices to high temperature tolerant components, finalize the high temperature power converter.

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Appendix A

CREE's Isolated Gate Driver

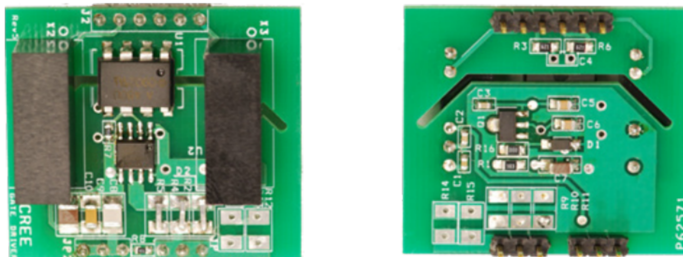

Figure A.1: CRD-001 Top and Bottom View

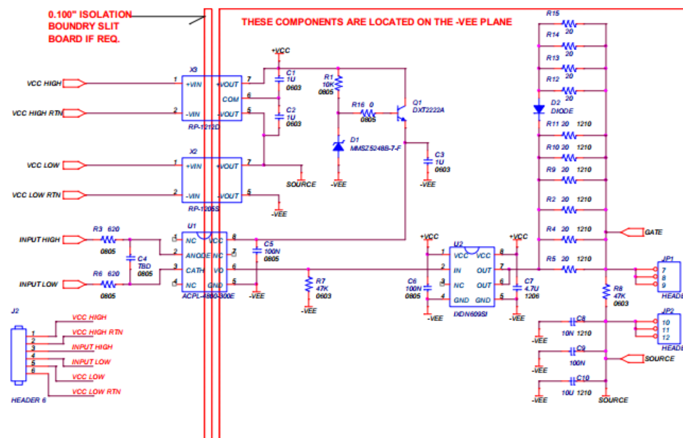

Figure A.2: Isolated Gate Driver Schematic

Appendix B

Isolated Power Rating

This Appendix includes the theoretical calculation and lab tested power requirement of isolated power supply based on the isolated gate driver configuration(See Figure 4.3), which discussed in Chapter 4. Both the lab test and the theoretical calculation are introduces in 10 kV, 20 kV and 40 kV frequencies.

- Theoretical Calculation
  1. Power losses calculation by Zener diode regulator
  According to Figure 4.7, power consumption of the Zener diode regulator, including the series resistor, Zener Diode and load can be equivalently calculated by V_{in} and I_s.

$$V_{in} = 24V constant \tag{B.1}$$

$$I_s = \frac{V_{in} - V_z}{R_s} \tag{B.2}$$

$$P = V_{in} I_s \tag{B.3}$$

  The corresponding power consumption of 20 V and $5V$ voltage regulators are 64 mW and 38 mW , separately.
  2. Pull up resistance power losses
  There are two 47 $k\Omega$ pull up resistors at the outputs of opto-coupler R_{10} and IXDN609CI gate drive R_{20}. The Simulation waveforms across R_{10} and R_{20} see Figure B.1 and Figure B.2). Note in the simulation, the gate drive IXDN609CI was not available. An alternative IXDD409 was used, which has an maximum at $V_{cc} =$ 20 V. So the simulation system voltage is limited to $20V$. An assumption has made where it is replaced by applied $V_{cc} = 25$ V to IXDN609CI, the voltage edge will be $25V$ for high voltage level and 0 for low voltage state for the R_{10}. The same as for R_{20}: 20 V positive and - 5 V negative bias voltage with same patterns in Figure B.1 and Figure B.2. The simulation has done at its average duty ratio $D = 0.5$. The power consumption is also calculated at the average duty cycle with $D = 0.5$:

For R_{10}

$$P_{res} = \frac{25^2 + 0^2}{47k} 0.5 \quad \text{(B.4)}$$

For R_{20}

$$P_{res} = \frac{20^2 + 5^2}{47k} 0.5 \quad \text{(B.5)}$$

Which give $6.64mW$ and $4.52mW$ respectively, in total it will be $11.17mW$.

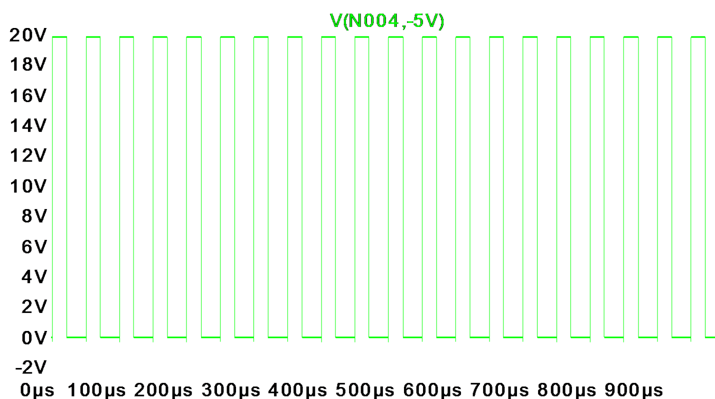

Figure B.1: Voltage Waveform Across Pull-up Resistors after Opto-Coupler

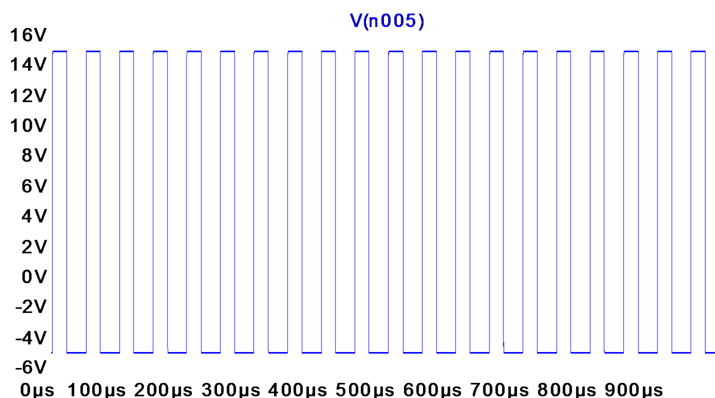

Figure B.2: Voltage Waveform Across Pull-up Resistors at GD Output

3. IXDN609CI Power Consumption
Studied from the datasheet of IXDN609CI, the maximum supply current to the IC is $10\ \mu A$. Therefore grossly $24V * 10\mu A = 0.24mW$ can be assumed.
4. The ESR Power Losses of Stabilizer Capacitors
Most of the capacitors are used as voltage stabilizer, they are not frequently charging and discharging. The main loss will be the ESR power losses, It will be very small

due to the surface mounted configuration.
5. Gate Charge Power Requirement
Different from previously calculated parameters, gate charge power are highly frequency related. The charging and discharging energy is dissipated through gate resistors, which can be calculated by capacitor energy transformation.

$$P = \frac{1}{2}CU^2 * 2f_s \tag{B.6}$$

In the datasheet, the gate capacitor is given in the charge Q forms. Further more three internal MOSFETs will connected in parallel, which is corresponding to 22.5 nF capacitors at 24 V gate source voltage. To make sure enough power supply, a larger capacitor with 45 nF is calculated and tested in lab. Therefore, it gives the following results with $45nF$ capacitors:
at 10 kHz, $P = 270mW$
at 20 kHz, $P = 540mW$
at 40 kHz, $P = 1080mW$
For the maximum total power consumption at 40 kHz is 1.432 W including 20% power margin. Finally, Recom R12P212D 2 W, 6.4 kV, 1.5 $\sim$ 10 pF low isolation capacitance DC/DC power supply with efficiency 70 $\sim$ 75% has be selected.To confirm with the power rating, lab test was realized.

- Lab Test Results
  To simplify the power consumption test, power input to the DC/DC isolated power supply has been done with parallel voltage meters and serious current meter. The maximum power required was tested at 40 kHz with 45 nF capacitor, the measured results are: voltage 11.99 V, current 0.159 A, with the power efficiency 75%, which gives an similar result as 1.429 W.

Appendix C

Gate Driver LTspice Simulation

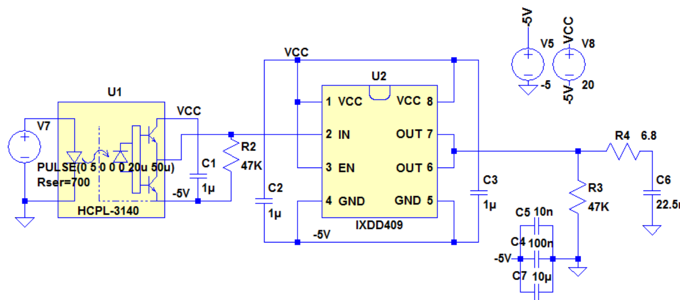

Figure C.1: IXDN409 Gate Driver Simulation Circuit

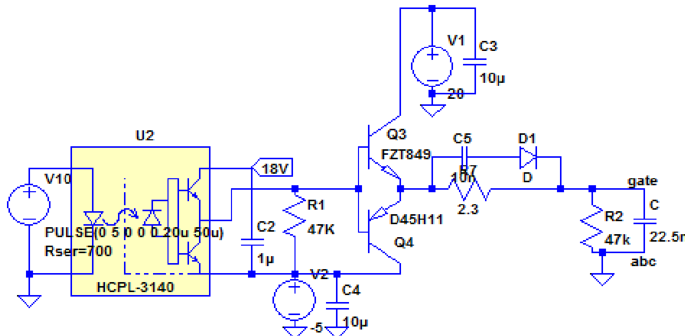

Figure C.2: Schematic of Totempole Gate Drive

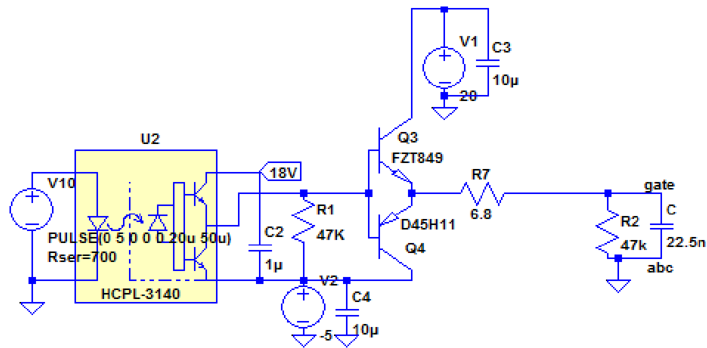

Figure C.3: Resistor Gate Driver - Recommended 6.8Ω

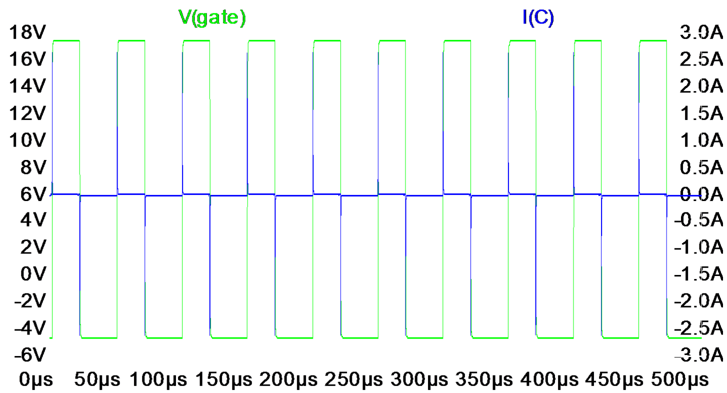

Figure C.4: Simulation Results of Figure C.3

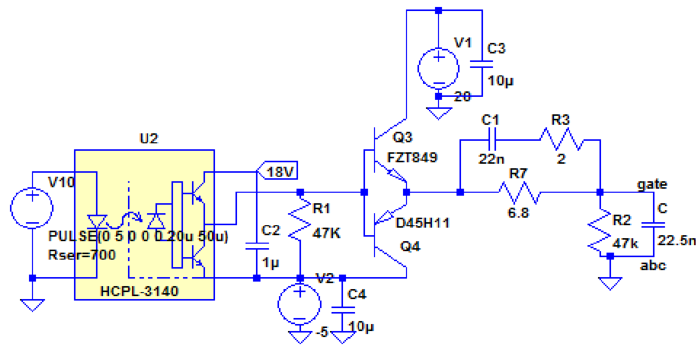

Figure C.5: Capacitor and Resistor Combined Gate

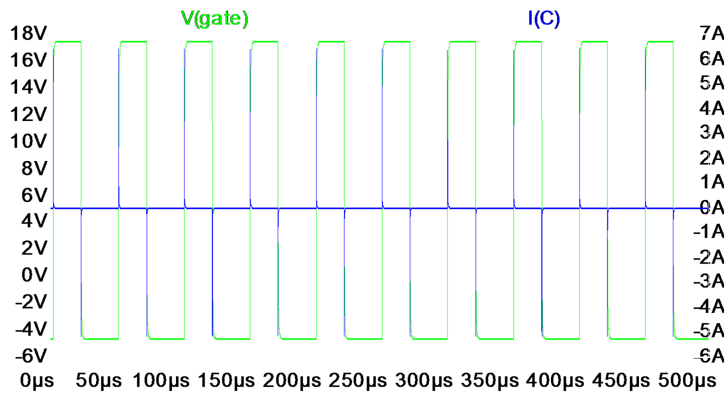

Figure C.6: Simulation Results of Figure C.5