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Protection of capacitor banks

Nuisance tripping of overcurrent relays; causes and possible remedies

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Preface

This master thesis concludes my master of science within energy and environmental engineering at The Norwegian University of Science and Technology, NTNU in Trondheim. The thesis was performed at the Department of Electric Power Engineering during my 10th semester in the spring of 2013. The thesis proposal came from Statnett. It was performed at NTNU under the supervision of Professor Hans Kristian Høidalen, and co- supervised by Ragnar Mangelrød at Statnett in Oslo.

I would like to thank both my supervisors, Hans Kristian and Ragnar for answering all my questions throughout the year. In addition Professor Bruce A. Mork of Michigan Technological University deserves a large thanks for spending time helping me whenever he was on campus. Helge Seljeseth at SINTEF has been invaluable in my search for real life data, and providing explanations when needed.

On a more personal note I would like to express my gratitude to my fellow students Kristian, and Torbjørn for every lunch, dinner, and numerous fruit breaks we have spent together during this semester. And finally Maren and my family for being supportive.

Trondheim, 12. June 2013

Christopher Gebs

Abstract

The origin of this master thesis is Statnett having problems with nuisance tripping of capacitor banks. Their own measurements are said to indicate that harmonics are confusing the overcurrent relays. Disconnecting a large capacitor bank from the transmission system can have large consequences for the stability of the system. Consequently any nuisance tripping such as Statnett has experienced should not be allowed to happen again. Measures must be taken to increase the security of the protection system.

The aim of this thesis is to investigate the overloading of capacitor banks and operation of numerical relays in harmonic rich environments. Investigate why Statnett have experienced nuisance tripping of overcurrent relays, and introduce possible mitigation measures. The definition of nuisance tripping has been broadened to also include correct tripping because of unwanted resonance.

Initially a literature study was conducted to acquire information on the prevailing limits that dictate threshold in relays. Limits have been found in IEC60871-1, and IEEE Std 1036-2010, and IEEE Std. C37.99-2000. In addition a number of books, standards and other publications have been used to understand how capacitors, relays and the general protection systems are influenced by harmonics and possible remedies when overloading becomes an issue. Together with the limits found in standards and regulations measurements from PQSCADA was used as an overview of what can be considered normal operation.

A model was created in ATPDraw based on the datasheet and a relay plan of a 420kV capacitor bank. The system is constructed for this simulation and does not represent one particular real life system. Further on it was used to test the difference between an unfiltered, single-tuned, and a c-type filtered capacitor bank. Simulations with both injection of harmonic current from the inductive load and simulations with a voltage source at the grid side dimensioned according to the regulation limits were conducted.

It was shown that a system with multiple capacitive and inductive components will have multiple resonance frequencies. As the short-circuit power varies these will fluctuate and might occur at a characteristic harmonic. The consequent amplification of the current will in many instances be large enough to overload the capacitor bank. A single-tuned filter solution will lower the resonance frequency but it is dependent on the short-circuit impedance and will thus vary. Using a c-type filter is more complex than a single-tuned but it results in a filter that is independent of the short-circuit impedance. The amplification of currents at the resonance frequency is also smaller with the c-type filter.

Aliasing of high harmonics can possibly cause nuisance tripping of the over current protection if they are not filtered out. It is therefore important to know what harmonics will be present and specify a relay that can handle such harmonics. Although applying a filter is normally intended to avoid actual overloading it can also be applied to lower the loading and making it easier for the relay to separate the particular situations where faults have occurred.

Sammendrag

Utgangspunktet for oppgaven kom fra statnett. De har erfart at overlast vernet av kondensatorbatterier har koblet ut utilsiktet i forbindelse med harmoniske og antagelig resonans. Hvis et stort kondensatorbatteri fjernes fra en tungt belastet linje vil dette kunne skape stabilitetsproblemer. Dersom denne utkoblingen ikke egentlig var nødvendig, men heller en konsekvens av et uegnet eller feil innstilt vern er det lite heldig. Tiltak burde iverksettes slik at dette ikke skjer igjen hverken ved det aktuelle kondensatorbatteriet eller framtidige installasjoner. Målsettingen for denne oppgaven er å undersøke hvordan kondensatorer og numeriske releer blir påvirket av å arbeid i nett med en høy andel harmoniske. Let etter en eller flere bakenforliggende mulige årsaker til at releene koblet ut utilsiktet. Finn mulige tiltak som kan minske sannsynligheten for at slike utfall oppstår.

Først ble standarder fra IEC og IEEE som omhandlet kondensatorbatterier og vern av dem saumfart etter grenseverdier. Disse ble i all hoved sak funnet i IEC 60871-1, IEEE Std. 1036-2010, og IEEE Std. C37.99-2000. Andre bøker og litteratur ble også brukt i søken etter informasjon om hvordan kondensatorer, relevern og andre vern systemer blir påvirket av harmoniske, samt hvordan disse utfordringene kan overkommes. For å ha et sammenligningsgrunnlag til de gitte grenseverdiene fra standarder og statlige forskrifter ble PQSCADA brukt til å hente ut måledata fra det norske høyspentnettet. Sammen utgjorde de normale driftsforhold.

En modell av at tenkt system ble designet i ATPDraw. Dataen for kondensatorbatteriet var reell mens, mens andre deler av systemet ble tilpasset, og det er i så måte ikke et virkelig system. Simuleringer ble kjørt med ulike tiltak for begrensning av resonans ved harmoniske. Installasjoner uten filter, en reaktor tunet til en frekvens og et c-type filter ble utprøvd i to systemer. Et med injeksjon av harmoniske strømmer fra den den industrielle likeretteren og en hvor kilden flere spenningskilder som sammen utgjorde FoL kravet for 420kV opp til den 13. harmoniske.

Det ble vist at et system med flere kapasitive og induktive elementer vil ha flere resonansfrekvenser. Når kortslutningsytelsen endres vil resonansfrekvensene endres. Hvis resonansfrekvensen inntreffer ved en karakteristisk harmonisk vil denne bli betydelig forsterket. Sammen med den fundamentale komponenten kan denne strømmen føre til overbelastning av kondensator batteriet. Et filter som tuner kondensatorbatteriet til en spesifikk serie resonans vil ikke være uavhengig av kortslutningsytelsen og vil fortsatt variere med kortslutningsytelsen. Hvis det derimot brukes et c-type filter vil den nye frekvensresponsen være uavhengig av endringer i kortslutningsytelsen. Et slikt filter er mer komplekst og krever mer av vern systemet enn det enklere filteret. Forsterkningen av harmoniske er generelt lavere når c-type filteret blir brukt.

Feilaktig måling av strømmen som følge av for lave sampling frekvens kan føre til feilaktig utkobling hvis de aktuelle harmoniske ikke blir filtrert ut før samplingen blir foretatt. Det er derfor viktig at de harmoniske strømmene er kjent slik at vernet kan spesifiseres etter disse. I tilfeller hvor vernet filtrerer bort de høyeste harmoniske kan dette føre til at vernet ikke kobler ut selv under en overlast. Selv om filtre normalt blir brukt for å hindre overbelastning pga. resonans vil de også hjelpe i tilfeller hvor kondensator batteriet er nær overlast. Filteret vil kunne gi vernet større marginer mellom den målte lasten og overlast.

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1 Abbreviations

PQSCADA - Power Quality Supervisory Control And Data Acquisition. Software suite from Elspec.
ATP - Alternative Transient Program
EMTP - Electromagnetic Transient Program
ATPDraw - Graphical pre-processor to ATP-EMTP
CT - Current Transformer
VT - Voltage Transformer
A/D - Analog to Digital converter
S/H - Sample and Hold
LPF - Low Pass Filter
MUX - Multiplexor
HMI - Human machine interface
ESR - Equivalent series resistance

2 Introduction

Capacitor banks are used both as a part of filters, and to compensate for inductive losses. The focus of this document is the protection of capacitor banks and in particular units intended to compensate the inductive losses and boosting the voltage. The basic concept is to utilize the 180° phase shift between a capacitive and an inductive load. Adding a source of capacitive reactive power will equal out a similar amount of inductive reactive power. If the capacitor is connected in series with the line, the voltage will be compensated, while a parallel capacitor bank will compensate the inductive current. A parallel connected capacitor bank is often called a shunt capacitor bank. Reducing the inductive component of the current will decrease the line losses, or potentially allow for more active power to be transported. The effect of a adding a shunt capacitor bank is a lower power factor. A graphical presentation of the compensation is given in Figure 1. Note that the shut capacitor bank also helps boosting the voltage.

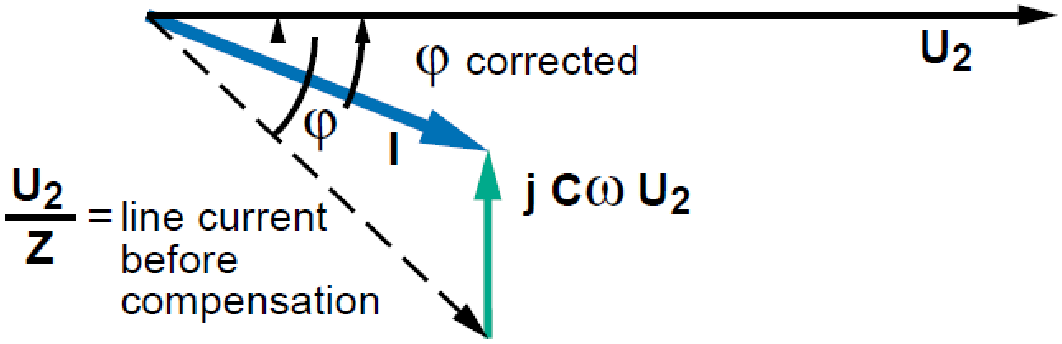


Figure 1: Line current compensation with a shunt capacitor bank[1].

The cost of adding a capacitor bank is relatively low compared to the alternative cost of network expansion. As a result, they are increasingly being installed in the power system. Statnett have observed some of their units being tripped when not supposed to. In systems where power can easily be rerouted this is not a very large problem and can be an acceptable consequence of having a high dependability in the protection system. However in the transmission system the consequence of an unnecessary tripping is more severe, and should be avoided. If it is not possible to avoid tripping, it should occur as fast as possible to limit the damage inflicted. To be able to minimize the probability of unnecessary tripping without new problems can be a difficult task. Successfully minimizing false tripping is dependent on having a thorough knowledge of both the surrounding power system, and the capacitor bank. The aim of this task is to provide an understanding of what should be obtained and how to interpret and use this information.

The first part investigates regulations and standards concerning capacitor banks and their protection. Important limits both regarding the capacitor bank and the grid of which is it connected. Further on the effect of adding a capacitor bank is discussed. To get an understanding of why harmonics are potentially harmful to a capacitor bank the resonance phenomenon and harmonics are introduced. In particular the overloading of capacitor banks originating from excessive harmonic currents are investigated. In addition possible mitigating measures are introduced.

To evaluate how relays can be affected by excessive harmonic currents the typical protection system is introduced. From Statnett the issues are assumed to originate with the overcurrent protection. Therefore this relay is discussed further, the unbalance protection is also discussed briefly as it is affected by the overcurrent protection. To understand how the relay is affected by harmonics the internals and how a numerical relay works is investigated on a general basis. Special attention is put on sampling and aliasing.

PQSCADA measurements are used as a basis for comparison between the regulations, standards and reality. In addition it shows that the predominant harmonics being injected are the characteristic harmonics. The frequency response of a couple of simple systems with capacitor banks with and without resonance mitigating measures are investigated.

3 Terms and definitions

3.1 Harmonics

Any current or voltage component with a frequency that is equal to an integer multiplied with the fundamental frequency.

3.2 Harmonic impedance, Z_h

The harmonic impedance of a system is the systems impedance at a specific harmonic.

Equation 1: Harmonic impedance of an inductor

$$X_{L,h} = 2\pi * 50h * L$$

Equation 2: Harmonic reactance of a capacitor

$$X_{C,h} = \frac{1}{2\pi * 50h * C}$$

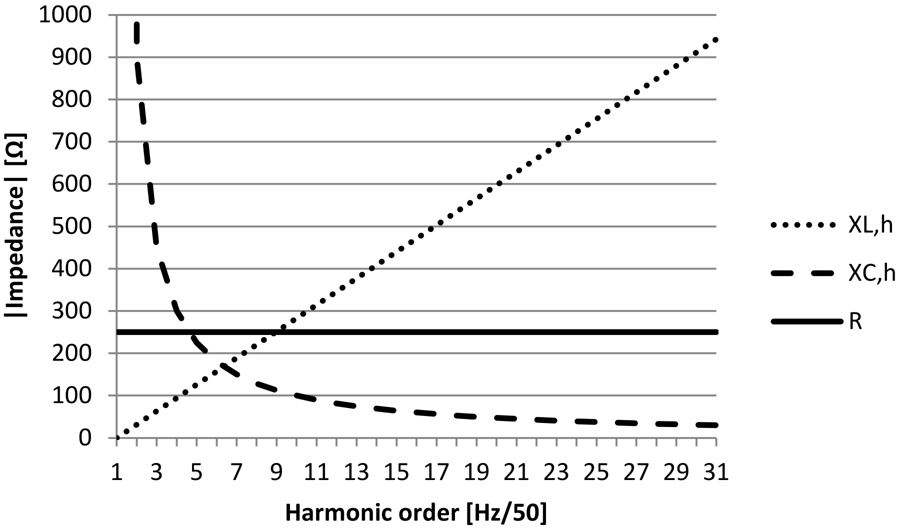


Figure 2: Frequency response of the impedance components. (L=100mH, C = 3.54µF, R =250Ω (large to be visible)

Figure 2 Is only an example. The resistance is quite large, and it is assumed to be constant. In reality the resistance will probably be affected by the skin effect at higher frequencies, and the dielectric hysteresis losses will increase with increasing frequency. IEC 09871-1[2] states that the tanδ of a capacitor bank should be supplied by the manufacturer, but it was not present in any of my data.

$$tan\delta(h) = \frac{ESR(h)}{X_{C,h}}$$

ESR - is equivalent series resistance

3.3 Harmonic order, h

The harmonic order is the harmonic divided with the fundamental. In this text it will be denoted h.

Equation 3: Harmonic order

$$h = \frac{f_h}{f_1}$$

Where :

h - is the harmonic order

f_h - is the frequency of the harmonic

f_1 – is the fundamental. f_h with h=1 is the fundamental frequency.

3.4 Characteristic harmonics

Harmonics with a harmonic order equal to:

$$h = 6n \pm 1 \qquad \text{n = 1,2,3,...}$$

Where 6n is the number of pulses of the rectifier

These harmonics are the product of an ideal balanced 6n pulse rectifier. One of these harmonics will normally be the predominant one in the grid.

3.5 Interharmonics

Interharmonics are current or voltage components with a frequency between harmonics.

3.6 Total Harmonic Distortion, THD

Total harmonic distortion is the ratio of the rms value of the sum of all the harmonic components up to the specified harmonic order to the rms value of the fundamental component.

Equation 4: Current total harmonic distortion

$$I_{THD\%} = \frac{\sum_{h=2}^{n} I_{h,rms}}{I_{1,rms}}$$

Equation 5: Voltage total harmonic distortion

$$V_{THD\%} = \frac{\sum_{h=2}^{n} V_{h,rms}}{V_{1,rms}}$$

Where

$I_{THD\%}$ *- is the harmonic distortion on the current.*

$V_{THD\%}$ *- is the harmonic distortion on the Voltage.*

n – is the highest harmonic order included in the calculations. FoL states that n should be 40 [3]

3.7 Resonance

Because of the opposite frequency dependence of the inductive reactance and the capacitive reactance, any system that include an inductor and a capacitor will have a frequency where the reactance is zero or approaches infinity. The state is called resonance and the frequency is called the resonance frequency.

There are two kinds of resonance

3.8 Parallel resonance

Parallel resonance occurs when an inductance and a capacitor is connected in parallel and the impedance in the parallel paths are equal but of opposite polarity. The harmonic impedance through the circuit will approach infinity only limited by the circuits resistive elements.

Equation 6: Harmonic reactance for parallel connected inductance and capacitance

$$X_h = \frac{X_{C,h} * X_{L,h}}{X_{C,h} - X_{L,h}}$$

3.9 Series resonance

Series resonance occurs when the harmonic reactance is zero through an inductor and a capacitor connected in series.

Equation 7: Harmonic reactance for series connected inductance and capacitance

$$X_h = X_{L,h} - X_{C,h}$$

Equation 8: Resonance frequency

$$h_{res} = \frac{1}{\omega\sqrt{LC}}$$

Equation 9: Resonance frequency based on the short-circuit power of the connected system.

$$h = \sqrt{\frac{S_{SC}}{Q_C}}$$

3.10 The Sampling Theorem

The samping theorem is the basis of the Nyquist rate. If the highest frequency contained in an analog signal x(t) is f_h and the signal is sampled at a frequency larger than twice f_h then x(t) can be exactly recovered from its sample values [4].

To get a proper reading of the signal the sampling theorem states that.

$$f_s \geq 2f_h$$

Where

f_s *– is the sampling frequency*

f_h *– Is the frequency of the highest order harmonic.*

3.11 The Nyquist rate

The Nyquist rate is defined as twice the frequency of the highest frequency present in the sampled signal. [4] This is the smallest sampling frequency that will give a unique digital interpretation of the signal.

3.12 The Nyquist frequency

The Nyquist frequency is equal to half the Nyquist rate. In other words it is the highest frequency that can be unambiguously reproduced when sampling at the corresponding Nyquist rate.

3.13 Normal operation

Any state of operation that is caused by connected equipment operating as intended. It is the basis for what connected equipment has to tolerate and what the protection system has to permit.

3.14 RMS current

Equation 10: The rms current of a pure sine-wave

$$I_{RMS,h} = \frac{I_{PEAK,h}}{\sqrt{2}}$$

Equation 11: The total rms current of N harmonic components including the fundamental

$$I_{RMS} = \sqrt{\sum_{h=1}^{N} I_{RMS,h}^2}$$

Where

I_{RMS} - *is the total rms-current*

$I_{RMS,h}$ – *is the rms-current of the* h^{th}*-harmonic component.*

Equation 12: The total rms current of a sampled current

$$I_{RMS} = \sqrt{\frac{1}{N}\sum_{s=1}^{N}|I(\Delta t * s)|^2}$$

Where

I_{RMS} - *is the total rms-current*

I - *is the measured current*

N - *is number of samples per period*

Δt - *is the period divided with the number of samples*

3.15 Crest factor

The crest factor is the relationship between the signal peak and the signal rms value. It can be a god indication on the level of distortion in the system.

$$Crest\ factor = \frac{Peak}{RMS}$$

3.16 Short-circuit power, S_{SC}

The short-circuit power is a synthetic parameter for the robustness of the electric network. [5]It is a measure of how much power would be available to a potential short-circuit. It is limited upwards by the impedance through transformers and lines. From the short-circuit power the short-circuit current I_{SC}, and short-circuit impedance Z_{SC} can be found. It is usual to represent the utility source by its short-circuit impedance[6].

According to Statnett [7] it is the system operators responsibility to provide S_{SC}.

Equation 13: Short-circuit power

$$S_{SC} = \sqrt{3} * U_{L-L} * I_{SC}$$

Equation 14: Short-circuit impedance

$$Z_{SC} = \frac{U_{L-L}^2}{S_{SC}}$$

Equation 15: Short-circuit current

$$Isc = \frac{Ssc}{\sqrt{3} * U_{L-L}}$$

Where

S_{SC} *– is the short-circuit power*

I_{SC} *– is the short-circuit current*

Z_{SC} *– is the short-circuit power*

$U_{L\text{-}L}$ *– is the phase to phase voltage*

S_{SC} is an important source of information. Both when establishing thresholds for a protection system and when estimating for instance the resonance frequency at a capacitor bank. A robust network would have a large short-circuit power. Consequently the short-circuit impedance would be low, and the voltage distortion caused by a given harmonic current would be lower than in a less robust network. If S_{SC} is large the short-circuit current will be large and faults are easier to differ from normal operation. When S_{SC} is given a simple thevenin equivalent of the connected grid can be created. This equivalent is very useful when a simulation model of any system is to be created. Unfortunately calculating S_{Sc} is a challenging task[8]. It may vary significantly with time, both within what is regarded as normal operation, and as a consequence of future modifications to the grid.

3.17 X/R Ratio

The X/R ratio is the ratio between the reactance and the resistance in the impedance. High voltage systems will have larger X/R ratios than low voltage systems. The total impedance will also be smaller in high voltage systems and thus harmonics will propagate much longer[6]

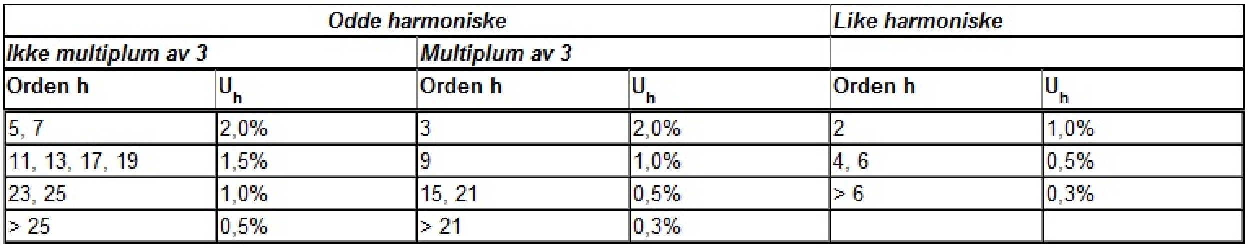
4 Background and theory

4.1 Regulations and standards

Regulations and standards are based on experience and create the framework for what has to be taken in to account when designing new installations. This section explores relevant Norwegian legislation and international standards from IEC and IEEE.

4.1.1 The Norwegian power quality code (FoL)

With regards to voltage harmonics the Norwegian power quality code states the limits given in Figure 3 for Voltage levels above 245kV. These values are a good measure of what should be regarded as normal operation with regards to harmonics. The industry cannot disregard these limits without special permission from the utility. The harmonic currents imposed by industrial rectifiers therefore has to be limited so they do not voltages outside these limits when the go through the harmonic impedance of the grid.



Odde harmoniske				*Like harmoniske*	
Ikke multiplum av 3		*Multiplum av 3*			
Orden h	U_h	Orden h	U_h	Orden h	U_h
5, 7	2,0%	3	2,0%	2	1,0%
11, 13, 17, 19	1,5%	9	1,0%	4, 6	0,5%
23, 25	1,0%	15, 21	0,5%	> 6	0,3%
> 25	0,5%	> 21	0,3%		

Figure 3: Limits regarding harmonic voltages as stated in FoL[9]

4.1.2 Statnett FIKS. Guidelines on system responsibility code

With respect to capacitor bank installations Statnett [7] have certain requirements. The most prominent with regards to harmonics and capacitor banks are listed below.

- Capacitor banks connected to solidly grounded networks must have phase synchronised coupling. Phase synchronised decoupling is not required. Whether or not it is necessary should be investigated for each installation.
- If multiple capacitor banks are connected in parallel. Dampening reactors shall be installed to attenuate large inrush currents
- Isolated neutral when installed in high impedance grounded systems, and solidly grounded neutral when installed in a directly grounded system.
- The protection system for HV equipment shall consist of two independent protection systems
- The protection system shall not trip because of stationary or transient conditions caused by normal operation. For instance switching operations, normal clearing of faults, energizing currents
- The protection system shall have a flat frequency characteristic up to 500hz for the over loading and over voltage protection.

4.1.3 IEC and IEEE standards

IEEE and IEC have quite similar limits, and both focus on their limits as a good tool to maximize the expected lifetime. Previous standards had less strict limits for over voltages and overloading but over time experience with reduced life of capacitor units have continued to push these limits lower with new editions. The over voltage limits from [2] IEC are given in

Table 1: Admissible voltage and current limits from IEC 60871-1 [2]

Type	Voltage, Current (rms)	Maximum duration	Observation
Power frequency	1.0	Continuous	Highest average value over time. Exceptions apply as indicated below
Power frequency	1.1	12 hours in every 24 hours	System voltage regulation and fluctuations
Power frequency	1.15	30 min in every 24 hours	System voltage regulation and fluctuations
Power frequency	1.2	5 min	Voltage rise at light load
Power frequency	1.3	1 min	
Power frequency + harmonics, excluding transients	$1.3I_N$ @ $1.0C_N$ $1.43I_N$ @ $1.1C_N$	Continuous operation Exceptions for short periods (<5min) during light loads in conjunction with voltage limits above.	Combined effect of harmonics and fundamental. C_N is the rated capacitance of a capacitor

In addition IEEE [10] specify that during continuous operation.

- The rms current should not exceed 135% of the rated rms current based upon rated reactive power Q and rated voltage, including fundamental and harmonics.
- The reactive power output should not exceed 135% of rated including harmonics, and the effect of manufacturing tolerances (0 to +5% rated power).

$$Q \leq 1.35 = \sum_{h=1}^{h=h_{MAX}} (V_h I_h)$$

- The crest voltage should not be larger than 1.2 *√2 times the rated rms voltage including harmonics and excluding transients.

$$V_{crest} \leq 1.2\sqrt{2} * \sum_{h=1}^{h=h_{MAX}} (V_h)$$

Capacitor banks can operate above these limits but at a significant cost to the expected lifetime. Over voltages above $1.15U_N$ is not expected to occur more than 200 times in the expected lifetime. In some cases the operator can allow short periods outside the limits if the consequences of disconnecting the capacitor bank are more critical than the ageing. This also applies if the capacitor bank is rarely exposed to conditions close to its limits and thus is normally less stressed. It is the combined stresses that will eventually cause some elements to fail, not one short overloading slightly larger than the given limits.

The momentary overvoltages allowed by IEEE according to figure 4 in section 5 of [10] reproduced in Figure 4. It shows the finite limit of short time overvoltage at 2.2 times the rated rms voltage and the decreasing capabilities when the duration increases. Note that the short time overvoltage limits stated here are quite a lot stricter than those stated by IEC in Table 1.

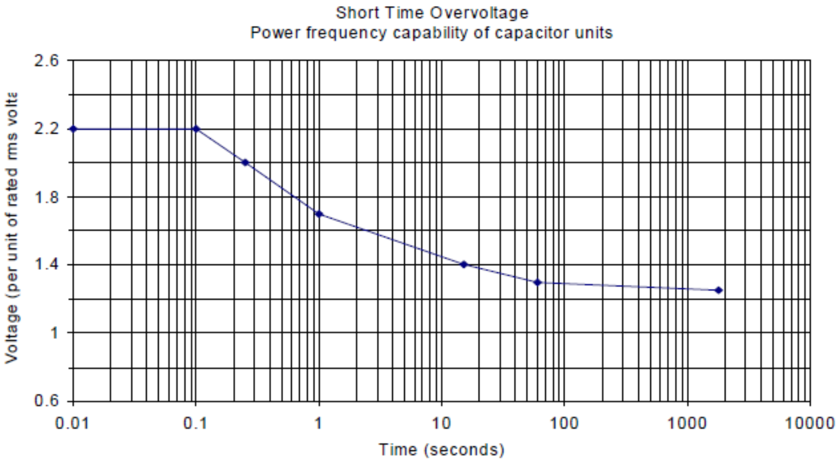


Figure 4: Short time overvoltage power frequency capability of capacitor units. Figure 4 section 5 in [10]

4.2 The effect of adding a Capacitor bank

As seen in Figure 5 adding a capacitor bank will help the grid supply reactive power to the consumer. This will lower the voltage loss across the transmission line by limiting the amount of current flowing through it. [2]Unlike most other electrical components an energized capacitor bank will operate continuously at full load at rated voltage and frequency. Excessive stressing of the capacitor either from voltages larger than rated or harmonic content will shorten the life of capacitor elements. The heating effect of the loading is an important part of the ageing process, it is therefore also important that the ambient temperature is taken in to account. This has often caused unbalance problems if a relay is unable to separate the changing capacitance from uneven heating from failing elements. The effect from the temperature is a gradual change opposed to the abrupt change from a fuse operation. However with many elements the change from one failed element is small. This among other things is why the unbalance relay needs to be very sensitive. The effect of installing a capacitor bank is among others increased voltage at the connection point. When the system is under light loads the voltage will increase and can cause overloading of capacitor elements at the fundamental frequency.

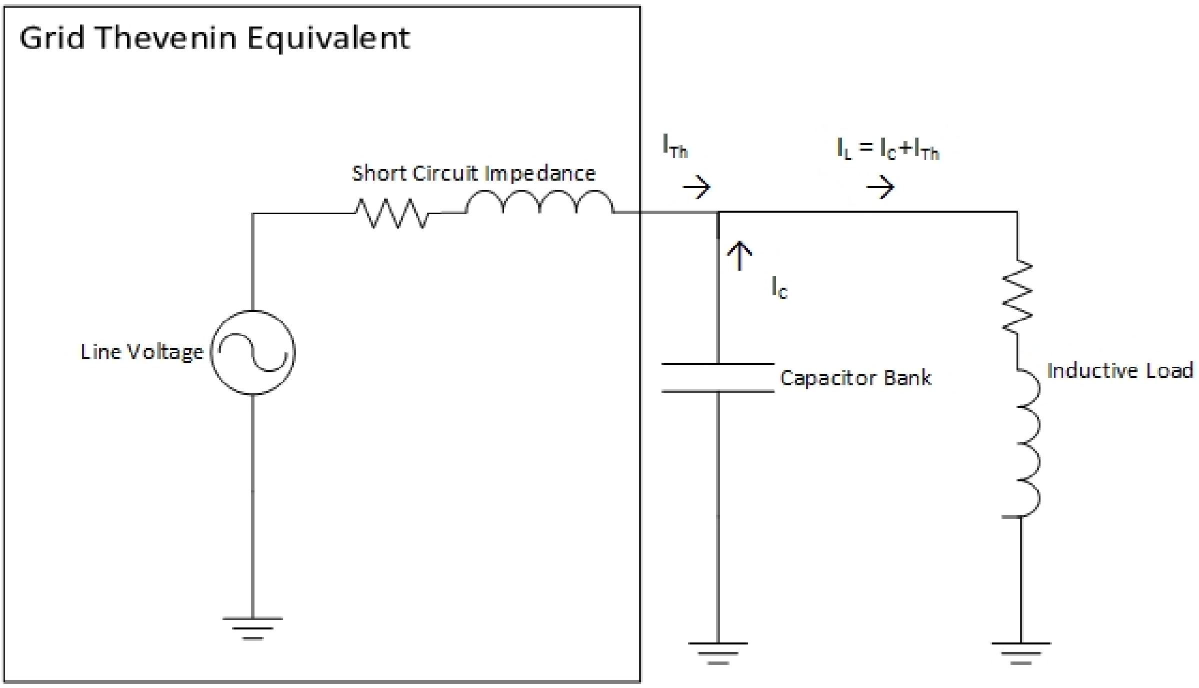


Figure 5: Capacitor bank supplying the reactive power for an induction machine

4.2.1 The effect of adding a reactor in series with a capacitor bank

- Increased voltage level across the capacitor bank
- The inductor will lower the capacitor banks impedance at the fundamental frequency
- The inductor will increase the capacitor banks impedance at the high frequencies. Frequencies above the resonance frequency.
- Prevents the capacitor bank from being a very low impedance path to ground for high frequency components. Such harmonics could potentially be harmful
- Limit inrush and outrush currents from coupling of the capacitor bank, common to have a resistor in parallel with the inductance to "burn of" the high frequency components of the transients.

4.3 Overloading a capacitor bank

Capacitor banks should not be operated continuously above the permissible values stated in paragraph 4.1.3. Which limit is used should be based on what standard has been used during manufacturing and testing of the capacitors. If it is unknown, the most conservative estimate of 1.3 times the rated rms current stated by IEC[2] should be used. Overloading currents will arise from either excessive voltages at the fundamental frequency, harmonics or both. In cases where harmonics cause the overloading, there will normally be one predominant harmonic current originating from a resonance. One source of large voltages at the fundamental frequency is light loading situations in the grid. Such conditions can also cause saturation of transformer cores resulting in large harmonics. It is therefore normal to disconnect capacitor banks from lightly loaded systems, both to protect the external system and to protect the capacitor bank. The most prominent transient overcurrents are normally caused by the inrush currents from coupling capacitor banks. Because these conditions are necessary to operate the capacitor bank means of attenuating them are installed when necessary and installations are constructed to handle quite large transients.

4.3.1 Losses in a capacitor

Losses cause heating and consequently ageing, and possible breakdown of the dielectric. The losses in a capacitor are caused by two phenomena: conduction losses, and dielectric hysteresis losses. [11] They are approximately proportional to the rms current, but at high frequencies the dielectric losses will increase

Conductive losses are caused by the resistance in the conductor between capacitors, through fuses, and electrodes. Skin effect will cause the resistance to increase at high frequencies. The effect is not large in the electrodes, but could cause heating other places in the installation.

Dielectric losses are caused by the small leakage current through the dielectric between the electrodes. In addition heat is created when the dipoles inside the dielectric turn with the voltage polarity. This loss is proportional to the frequency, and therefore the loss that is most affected by harmonics. [12] It is called dielectric hysteresis losses.

Together these losses increase the temperature of the capacitors and accelerate the ageing process of the dielectric. Because of this IEC 60781-1 states that the rms current including harmonics should not exceed 1.3*I_N when operating at rated voltage. The limit is supposed to reflect a loading of the capacitor that does not inflict unnecessary ageing and increased probability of capacitor element failure.

Equation 16: Heat loss

$$P_{LOSS} = R * I_{RMS}^2 * t$$

$$P_{LOSS} = \sum_{h=1}^{N} R(h) * I_{RMS,h}^2 * t$$

This is correct if the resistance is assumed to be constant. The resistance is assumed to be constant for the conductive losses in the capacitor bank. Note that dielectric losses will be larger for harmonics, and thus R will not be constant, especially with high order harmonics passing through the capacitor bank. It has not been found a lot of information about the actual frequency dependence of the capacitor elements in general. However IEC [2] states that upon request the manufacturer should supply a frequency dependent tan(δ) value that would show this. Because it is not much focus on the frequency dependence of resistive losses in the literature and that the data sheet only supply a constant resistive loss the resistance is assumed to be constant.

4.3.2 The consequence of overloading a capacitor bank

Statnett use internally fused units in new installations therefore this is the only technology being discussed.

Appendix B gives an introduction to the structure of the capacitor bank. In addition some possible connections are shown. A capacitor bank is built up of thousands of capacitor elements. The limit for continuous operation is given as 1.1 times the rated voltage in Table 1. If on element fails because it is overloaded and is properly disconnected by its fuse, the consequences are small. The stress level across other parallel elements will increase, and additional failures can cause a cascade failure of elements. IEC 60871-1[2] states that all units should be able to operate with one failed element without causing excessive stressing of the remaining elements.

Disconnection of a capacitor bank during high load, can cause overheating of lines, and upstream components such as transformers because of the increased demand for reactive power and hence increased current amplitude. In most cases high loading of the surrounding system will indicate that the loading of the capacitor bank is reasonably low because of the increased voltage drop. The only exception would be if the increased load is caused by large harmonics.

Cascading failures can occur in cases where fuses inside a capacitor bank do not operate as intended, or the unbalance protection does not remove an overloaded capacitor bank. These events are rare but can cause the units to explode as a consequence of overheating. This was more common in older installations where the electrodes did not weld together when they fails, but rather had an arc burning between them. The paper dielectric also produced more gasses during such faults to further accelerate the process.

4.3.3 Means of mitigation

Depending on what is causing the overloading a number of different solutions are available.

1. The rated voltage of elements can be increased to allow for more elements being disconnected before the unbalance protection trips. Each element would also be able to stay sound for longer.
2. In case of resonance problems the installation can be moved to another location or divided up in to smaller ratings, moving it away from resonance by changing the amount of connected capacitance.
3. Single tuned harmonic filter. Installing a reactor in series with the capacitor to tune the resonance frequency
4. Install harmonic filters at the source to avoid propagating harmonics at the resonance frequency.
5. C-type filter

4.3.3.1 Filtering

In most cases moving the capacitor bank is not really a viable option, and increasing the voltage rating will only prolong the life expectancy, not remove the problem. Asking the polluter to remove more of certain harmonics is probably not going to happen unless the utility pay for it, and very often there are multiple sources. Filtering of the capacitor bank is very often the only option.

Single-tuned harmonic filters

Connecting a reactor in series with each phase will lower the resonance frequency. The reactor is sized to create a de tuned filter with a resonance frequency lower than the harmonic causing trouble. Normally the 3rd harmonic. This rather simple filter will only be tuned for one specific short-circuit impedance, and is thus not very effective. As the short-circuit impedance varies a new resonance might occur. In other words the filter will only move the problem. Additionally tuning a system down to a low order resonance frequency will introduce large losses at the fundamental frequency and thus limit the supplied reactive power.

C-type harmonic filters

The construction is more complex than the single tuned filter, and it will require more of the protection system. Therefore it is a more expensive option, but unlike single tuned filters it is not susceptible to changes in the system impedance which is of particular concern in networked high voltage systems[13]. Another advantage over the single tuned filter is that ideally the C-type filter inflicts no losses at the fundamental frequency. The construction of a C-type filter is shown in Figure 6. C1 is the capacitance of the original capacitor bank. R is a dampening resistor. L and C are tuned to have a series resonance at the fundamental frequency. Because of this there is ideally no additional losses in a C-type filtered capacitor bank at the fundamental frequency. At other frequencies than the fundamental the dampening resistor and the impedance will limit the harmonic coming through the capacitor bank.

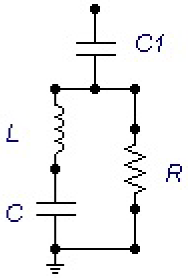


Figure 6: C-type tuned filter

4.4 Capacitor bank protection

The protection systems have to protect the capacitor bank from states where excessive damage is expected. These states can be divided in to three main groups. Blackburn and Domin [14]

1. States where internal faults might cause cascading failures
2. Protect the capacitor bank from power system conditions that is expected to damage the capacitor bank
3. Protect the power system from stress caused by the capacitor bank.

4.4.1.1 Important concepts in power system relaying

The following subsection is based on [15] and[16]. It is intended to give a brief introduction to some important concepts in power system relaying.

4.4.2 Power system relaying

The intention of relaying is to remove problematic situations when they occur, and in doing so minimizing the consequences of a problem. These problems are very often caused by failures but can also be of other origins. An example would be if the load connected to a compensated distribution system is decreasing. The system voltage would increase, and at some point the capacitor is no longer needed. It is actually causing an additional increase in the system voltage, posing a risk both to itself and the connected loads. Therefore it should be disconnected.

4.4.2.1 Measuring transformers

It is important to give the relays accurate measurements. If the transmitted measurements are not correct, the reliability and selectivity of the protection system will decrease. Choosing a suitable measuring transformer is therefore essential to ensuring reliability and selectivity in the protection system. Two notable characteristics of measurement transformers are the frequency dependence, and the danger of saturating the iron core. When an increasing current does no longer increase the flux density in the core it is said to be saturated. If saturation occurs the current will no longer be transmitted as the magnetic field is constant. Consequently a saturated current transformer will result in a discontinuous current measurement, unfaithful of the true current. Possible causes for saturation can be large over currents and dc components in the fault current[15]. In[17] it is shown that the frequency dependence of capacitive voltage transformers can have a large impact on the measured harmonics. The measured frequency response was far from linear and could cause incorrect tripping of the protection system. Based on these results, the frequency response of installed measuring transformers must be known, and corrected for in the relays. Long lines from the measuring transformers to the relay can also cause inaccuracies in the measurements. The significance if the above discussion is that the measurements from a measurement transformer will not necessarily be correct. Both saturation and frequency dependence must be taken into account when designing a relaying system. Choosing a sufficiently large iron core will prevent saturation in the expected scenarios. Similarly to the inherent unbalance the frequency dependence of the measuring transformers should be controlled prior to adjusting the relays.

4.4.2.2 Important concepts in power system relaying

The following subsection is based on [15] and[18], and is intended to give a brief introduction to some important concepts in power system relaying.

4.4.2.2.1 Selectivity

All relays are intended to protect an area of a system. Selectivity is a measure of how well defined the limits of the protected area is. If there is a fault in a system with high selectivity there will be no confusion regarding which relay is to operate, and the sequence in which the backup relays are to react. In other words, selectivity is a measure of how good the protection system is to disconnect as small a part of the system as possible to clear a failure.

4.4.2.2.2 Reliability (dependability, security)

The reliability of a protection system is a measure of the certainty that a protection system will perform as intended. The concept is divided into the two opposing parameters of dependability and security. Dependability is the probability of a relay operating correctly when it encounters the faults it was designed for. Security is defined as the measure of certainty that a relay do not operate incorrectly for any fault. Dependability is most important in power systems where power can be rerouted. Hence the loss of a small section is not critical. When the dependability increase the security will tend to decrease. At the transmission level of a power system the security of the supply become more important than in systems at lower voltage levels. If a part of the transmission systems is disconnected, it can cause stability problems, and even the need for power shedding in high load situations. Because of this the mentality regarding the protection systems reliability tends towards increased security.

Actions that would increase the reliability of a system could be to utilize multiple sources of information or two different relays. Which measure of certainty is increased depend on how the extra information is utilized. To increase the dependability a 1 out of 2 mentality would be used. This would reduce the probability of a fault going undetected. To further increase the dependability the two relays should come from different manufacturers minimizing the probability of common cause errors. If the desired outcome of adding information is to increase the security, a 2 out of 2 mentality would be implemented. Requiring that both relays should operate will limit spurious tripping, but at the same time decreasing the probability of always reacting when detecting a failure.

4.4.2.2.3 Speed

The rapid clearing of a fault is often essential to minimize the consequences of the fault. How fast a relay can react depends on three factors. The first is the time it takes to detect a problem. The second is the other protection systems it has to collaborate and coordinate its actions with, and finally the limitations of the circuit breaker. A relay will in most situations be allowed to observe a failure for some time before deciding whether to send a trigger signal. A consequence of reducing the observation time is that the reliability will also decrease. Coordination with other systems will enforce both an upper and a lower trigger time. For instance the overcurrent relay in a capacitor bank should not operate before the fuse is expected to disconnect a failed element. This can be achieved by tuning the relay to the inverse current time characteristic of the fuse. In addition some safety margin should also be introduced.

4.4.2.2.4 Primary and backup protection

To ensure a dependable protection system, all possible faults should covered by multiple relays and or functions in a multifunctional relay. As discussed in Reliability section some protection systems incorporate the additional redundancy of a duplicate protection system. Protection systems for large capacitor banks and other critical components are such systems. To get a truly duplicated protection system the two relays must be completely independent. Whether or not this is economically feasible depend on the consequences of having to use a less selective protection system if for instance a common circuit breaker fails. The two relays would be the primary protection system, clearing the fault as fast as possible by removing the smallest possible section. Backup protection can either be local or remote. It is responsible for removing the fault if the primary protection fails. It might or might not be more selective, but less selectivity would yield a larger dependability. In most cases additionally protection with less selectivity will be available further out in the system, but the large time delay required will allow the fault to cause substantial damages.

4.4.3 Typical armament

The typical armament of a capacitor bank consists of: Over voltage and under voltage protection. Ground fault protection if grounded. Over current protection and unbalance protection. In modern multifunction numerical relays all or most of these functions are included. However it is normal to use multiple relays to both have redundancy in that they will probably not all fail at the same time. Different algorithms from different manufacturers also provide security. Statnett also require duplication of the protection relays contributing further to the security of detecting a dangerous state. In this text the focus is on the overcurrent relay as this is the one Statnett has experienced nuisance tripping. The unbalance protection is also included in the following discussion as it is affected by the overcurrent relay not working as intended.

4.4.4 Overload protection

The protection sequence is given in [19]. It states that the protection shall operate selectively, the first step is the internal fuses of each element. The second step is the relay protection of the bank, either the overcurrent or the unbalance protection. The third step is the network or the plant protection. When a capacitor element fails the fuse will disconnect it from the circuit instantaneously because of the large discharge current from the parallel elements. It is therefore not necessary to use inverse time characteristics in the overcurrent relay to coordinate the two protection systems. In addition it is not necessary to disconnect an overcurrent at once as the possible damage is slow to evolve. Common with about 3-6 seconds delay. This time delay will ensure selectivity between the fuses and the overcurrent relay. The setting for transient overloading must be smaller than the smallest imaginable short-circuit current, but larger than the largest currents expected from normal operation. Inrush, out rush, or coupling of other capacitor banks nearby. It is all about balancing the need to ensure tripping for a fault, but at the same time avoiding nuisance tripping. Safety versus availability the continuous overcurrent limits are given in Table 1 and just below it.

4.4.5 Unbalance protection

The unbalance protection in an H-coupled capacitor bank is based on measuring the current in the H-bridge. A current will flow in the H-bridge when there is difference in the capacitance on each side. Because the prevailing standards such as [2] accept that the capacitor units can vary with as much as -5% to +10% there will often be a significant inherent unbalance in the capacitance. The resulting current has to be removed from the measurements to achieve the necessary sensitivity. All new relays intended for unbalance protection will have this capability. Capacitor elements are manufactured operate at or below the rated voltage, and can be operated continuously when the voltage is less than 110% of the rated voltage. The unbalance relay should trip when the unbalance current is above the threshold given by the manufacturer. For large capacitor banks it will often sound an alarm when it has detected about half of the allowed failed elements.[20] section 8.4.5 in [20] describe how the unbalance currents can be calculated. Appendix E shows the calculations for the capacitor bank applied in this text

The unbalance current from one failed elements in different locations will have different polarity. Thus the total unbalance current is not a safe measure of the number of failed elements. It is important that the relay is sensitive enough to detect one failed element. Counting the number of failed elements will prevent the relay from being confused by

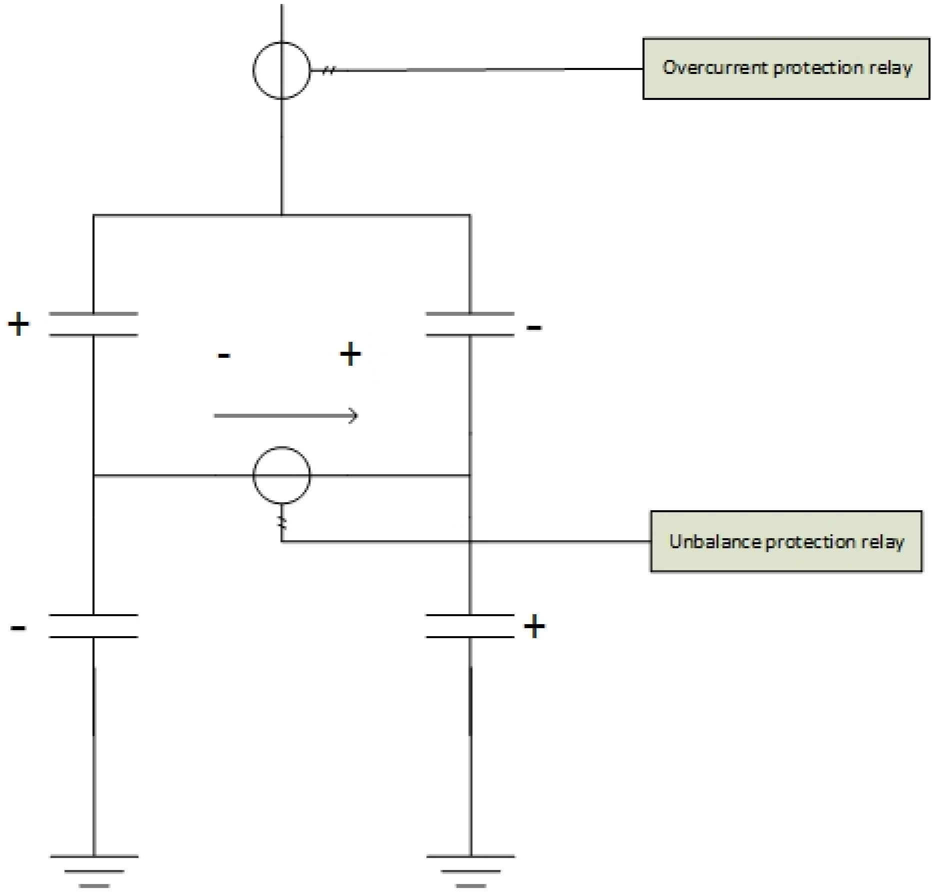


Figure 7: One phase of an H-coupled capacitor bank with overcurrent and unbalance protection CTs indicated. +/- indicates the polarisation of the unbalance current resulting from failed elements in capacitor units depending on their position with regards to the location of the H-bridge.

4.4.6 Numerical Relays

Remember chapter 9 [14]in new microprocessor relays can incorporate a lot more logic, and hence respond correctly to more conditions. (Boolean algebra)

The introduction of numerical relays has given the relay engineer a very flexible programmable relay. It can monitor multiple parameters and detect undesirable states by comparing these. Because it is a computer its functions are not hardwired and can in theory easily be changed and modified. The numerical relay is the latest in relay technology. It utilizes the large advances in computing power made available in the last decades. Previous solution like electromechanical relays evaluated the continuous analog signal. Numerical relays evaluate the signal based on a number of sampled instantaneous values. This limits the amount of available data compared to analysing the analog signal directly. But unlike the older analog relays the numerical relays can easily process and compare different measurements, in addition the digital signals are easily stored and communicated[21]. Experience demonstrate that the benefits of microprocessor based protection, control and communication systems far outweigh the disadvantages [22]. The intention of this section is to bring about a better understanding of the advantages, limitations and possible pitfalls of the numerical relay. First the different building blocks are introduced. Secondly there will be sections on digital sampling and aliasing. Finally the section is rounded up with a summary of the advantages and disadvantages of the numerical relay.

The task of any protection relay is to limit the consequences of a fault, and if possible to protect components from damaging states. This is achieved with measuring transformers supplying relays with analog measurements. This input is sampled and processed and compared to defined thresholds. A tripping signal or other actions will be undertaken if thresholds are breached. The relay control one or more circuit breakers to fulfil required actions. It is possible for the relay to communicate with other relays, or operators, and take in multiple signals. There can be interlocking of relays, prohibiting certain states from occurring, or alarms signalling a serious problem that is not jet critical. A flow chart of the relays task is seen in Figure 8.

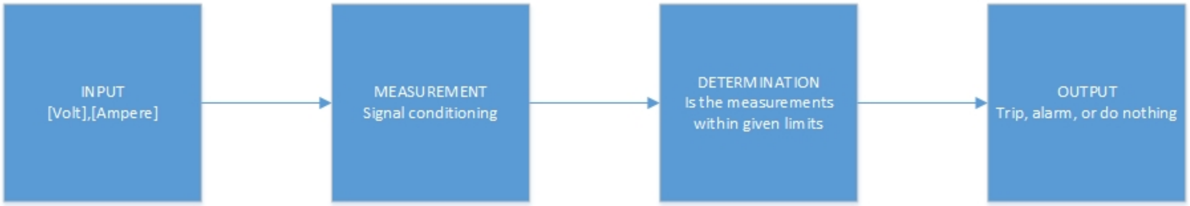


Figure 8: Protection system flowchart

Signal conditioning from the CT to a digital signal.

Figure 9 show the basic building block of a modern numerical relay. The figure is based on figure 6-1 in[21]. Similarly the following section is based on [4, 21, 22]. Before the analog input signal from a CT or a VT can be processed by the microprocessor it has to be turned in to a digital signal. To ensure that the digital signal become as accurate as the relay allows it is conditioned through a series of analog elements. The first step is an isolation transformer. Its main objective is to protect the more fragile components later in the system by entering saturation before the current can damage components behind it. After the isolation transformer sits a LPF, it removes any components with a frequency outside the bandwidth of the A/D converter. The importance of this component will be further explored in section 4.4.6.1. on aliasing. Because the microprocessor can only work with one signal at the time the MUX is used to switch between the different inputs. All of the S/H components will take a sample at the same time and hold it until it has been transferred to the microprocessor. There are two reasons for doing this. Number one is that the microprocessor has to compare signals taken at the same instant. It is possible to extrapolate based on the frequency at which the MUX switch between the signals, but this would increase the work load on the microprocessor and slow down the possible sampling frequency, and also the reaction time of the relay. In addition, extrapolating will introduce another possible error in the measurements. Secondly the A/D converter needs a constant signal to create a staircase approximation of the signal that can be quantized to a valid value and coded in to a digital signal. What is a valid number, is determined by the number of bits in the binary sequence produced by the coder.

Microprocessor with auxiliaries and output

This digital interpretation of the analog signal is transferred to the microprocessor. Initially the signal is compared against any limits concerning that signal on its own. If the signal is used in any other algorithm, it will be stored in memory until all the necessary signals for the algorithm is present. It is possible to store all the measurements, but storing all measurements will generate very large amounts of data. Therefore it is more common to only store abnormal situations permanently. There are different kinds of memory modules for different uses. Permanent storage such as that used for thresholds will normally be some sort of non-volatile memory. Hard disk drives can be used for larger quantities of data such as measurements, and volatile memory is used for temporary storage of measurements. The real time clock is important when measurements are to be compared with measurements from other relays. All communication with the relay happens through either the onsite HMI or through a communication card. Automated communication such as blocking signals from other interlocked relays will come through the contact input isolation block. If a signal is breaching any thresholds the relay will put out the signal specified through the output relay. It can be either a trip signal, an alarm, or possibly a blocking signal to other relays.

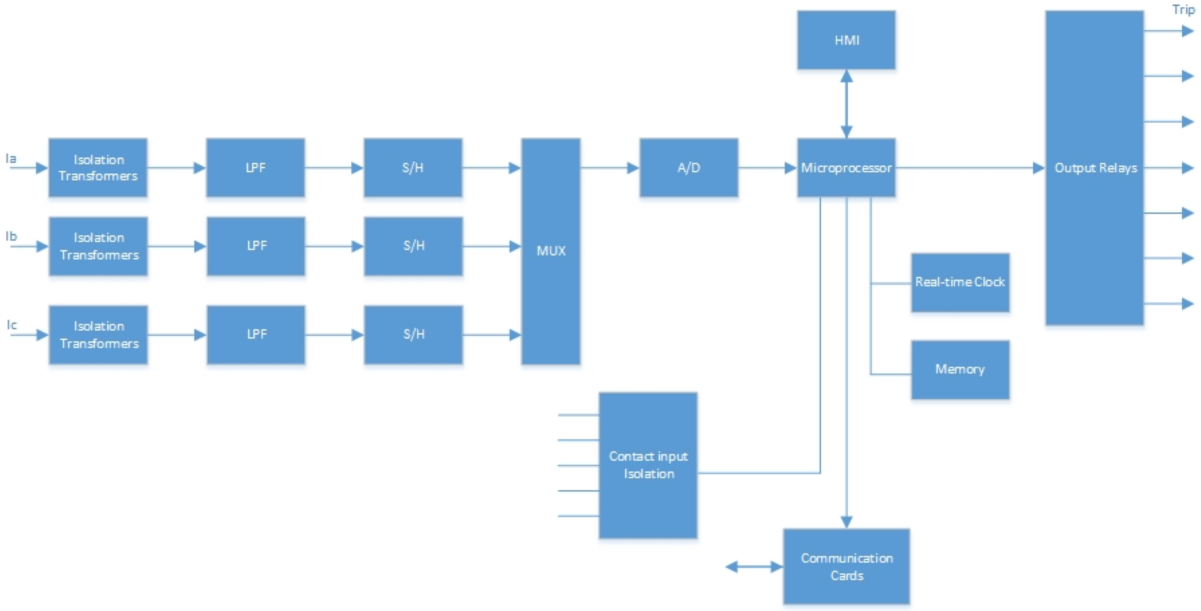


Figure 9: Numerical relay schematic Walter [21]

4.4.6.1 Sampling problems

Because of the limited amount of information gathered through instantaneous samples, the signal perceived by the relay can look very different from the actual analog signal. If the harmonic content is not known when the specifications of the relay are determined, inadequate sampling can cause false measurements. The sampling theorem states that to unambiguously reproduce a sampled signal the sampling frequency must be at least twice that of the highest order harmonic. This limit is often called the Nyquist rate. In most cases it will be necessary to sample at an even higher rate than the Nyquist rate to ensure a correct measurement. If for instance a sample contains components with a frequency equal to half the sampling rate it is possible that all the samples are taken at the zero-crossing for the harmonic at half the Nyquist rate. An example is shown in Figure 10 with the small circles being a sampled value. The signal perceived by the relay has lost the entire harmonic component.

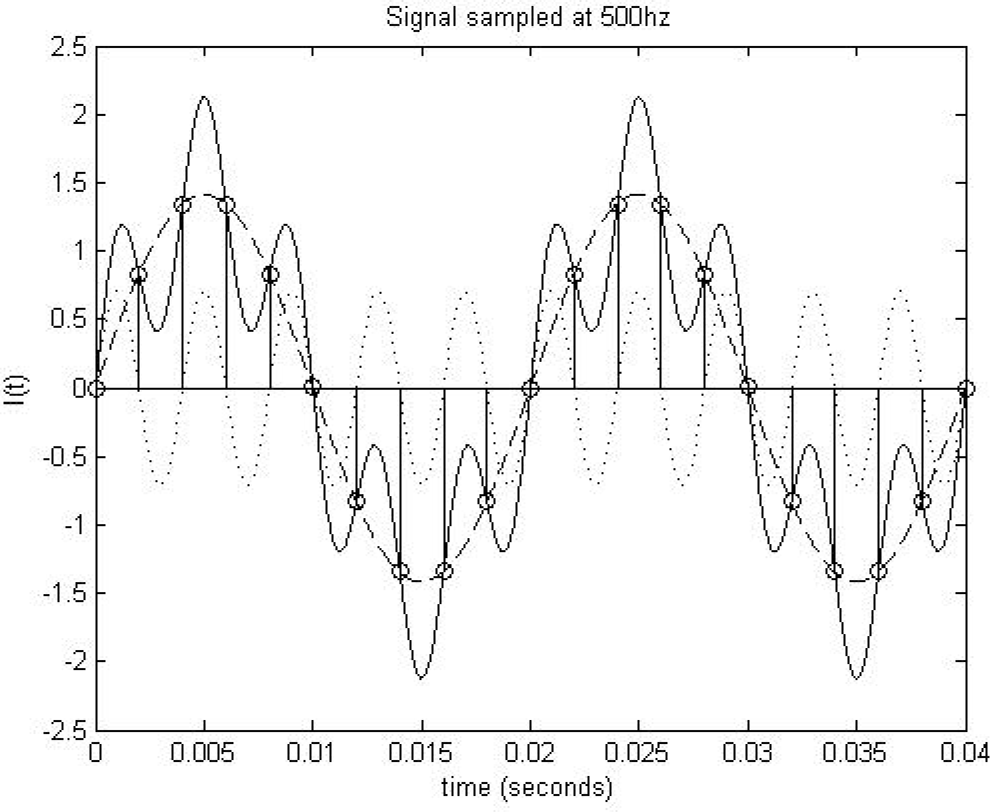


Figure 10: Sampling at zero crossing. Fundamental + 5th harmonic

4.4.6.1.1 ALIASING

If the sampling frequency is lower than the Nyquist rate, all the harmonics above the Nyquist frequency will be observed as a frequency inside the bandwidth the sampling frequency creates. Aliasing is one of the most severe pitfalls with numerical relays concerning the presence of harmonics. The aliases are super positioned on top of the actual harmonic present in the signal. In addition to Figure 10 examples of aliasing can be found in Figure 41 through to Figure 43. It is impossible to remove aliasing from the digital signal through post processing. Avoiding aliasing is therefore critical. Possible consequences of the relay measuring inaccurate values are either tripping when the signal is actually within the thresholds, or oppositely not tripping when the signal is actually outside the limits specified. The Low pas filter is used to remove components outside the available bandwidth of the relay.

Discrete-time sinusoidal whose frequencies are separated by an integer multiple 2π are identical. [4] This means that any harmonic larger than ½ the sampling frequency will be interpreted as one of the harmonics inside the bandwidth.

$$x(n) = A * \cos(2\pi f n + \theta), \quad -\infty < \mathrm{n} < \infty$$

Where:
x(n) – is the sampled instantaneous value.
n – is the sample number.
f – is the frequency with the dimension cycles per sample.
A – is the amplitude.
Θ – is the phase shift

How the harmonics outside the bandwidth will be aliased can be found from a simple diagram. For every harmonic smaller or equal to the Nyquist frequency the harmonics will be correctly detected at the initial rising line segment. An example for a signal sampled at 400hz is given in Figure 11. After the Nyquist frequency at the 4th harmonic order the consecutive harmonics will be aliased as the harmonic given on the y axis. When the line is rising the alias will have the same polarity as the harmonic it is aliasing, if the line is falling the alias will have the opposite polarity and thus make the detected harmonic smaller if any harmonic is present. The sampling frequency is normally equal to a power of two because of the FFT.

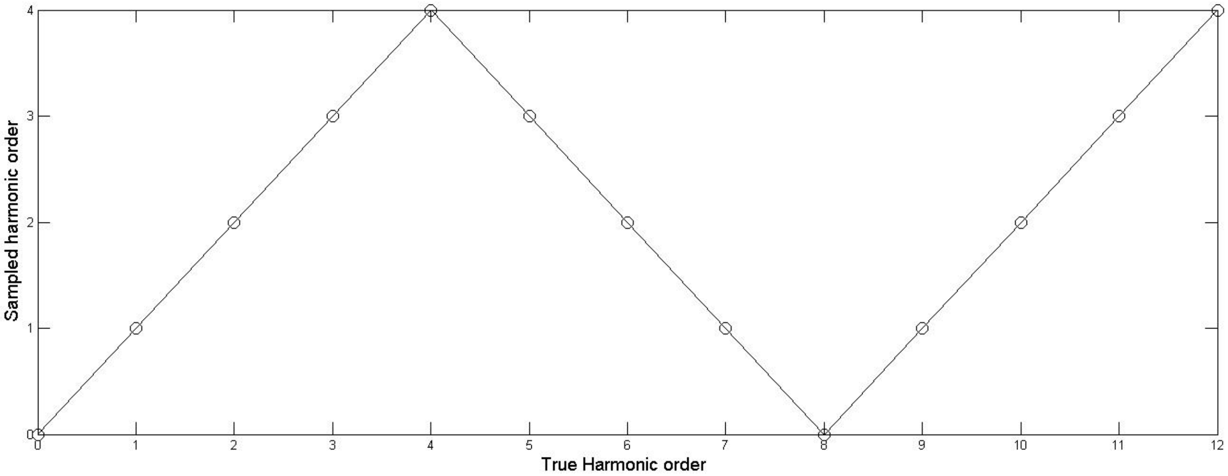


Figure 11: Diagram for finding how a harmonic will be aliased when the signal is sampled at 400hz

4.4.7 Nuisance tripping

Nuisance tripping is when a relay trip for a state that is not truly outside its thresholds. An example would be if the signal is interpreted inaccurately by the relay or by the CT. This definition has been expanded in this text to also include not tripping when supposed to and consequently causing unnecessary damage and tripping of unbalance protection. Finally conditions where overloading caused by resonance could have been avoided is also defined as nuisance tripping. Failing to detect a harmful state will eventually cause a more severe problem and consequently another relay will trip. An example would be if for instance the overcurrent relay is unable to detect high order harmonics. If such harmonics are present they will increase the loading of the capacitor bank completely unnoticed until capacitor elements start to fail, and the unbalance protection trips. Even though the actual tripping happens in another relay, the underlying cause is the overcurrent protection. Therefore reasons for underestimating the current are also included as a nuisance tripping.

Previous generations of relays such as electromechanical and solid state relays were prone to nuisance tripping when harmonic were present. Especially schemes that tripped based on peak values could be inaccurate when the crest factor is large. [23] and [24]. New numerical relays can separate each frequency component and is not tricked by one large peak in the total wave shape. If the digital relay is supplied with digital signal free of aliasing it should be able to evaluate the signal correctly. However the digital filtering or in other words the processing of signals in a numerical relay is not always perfect.

"Digital relays may be influenced by harmonic distortion if the predominant orders of harmonic oscillations are not predicted. The digital band-pass filter response provided in a relay may have a low attenuation factor at a given harmonic frequency and cause undesired tripping of the filter banks." IEEE [20]

A numerical relay can cause nuisance tripping in two different ways. With respect to harmonics the largest problem is the bandwidth of the A/D converter. Other possible problems is under dimensioned CTs leading to saturation and estimating a too low value. Both of these issues will probably lead to the relay not detecting the entire load current. This will cause the relay to not trip for overloading close to the limit. It is also possible that the thresholds have been erroneously implemented in the relay. Either from the manufacturer or the relay engineer.

The advantages of numerical relays include but are not limited to

- Very low burden for the CT
- Self-checking capability
- Digital signals
    - Easily storable,
    - Communication
    - Signal processing
        - It is much easier to apply sophisticated algorithms on digital signals than the equivalent analog signal. Analog signals are often not even feasible to process [4]

The disadvantages of numerical relays include but are not limited to.

- Not a continuous signal. Some information will be disregarded.
- Many functions, larger possibility for human error during set-up
- Sampling frequency limits what the relay can observe.
    - Danger of aliasing (LPF trouble)
    - Danger of not detecting a dangerous harmonic.
        - Consequently overloading the capacitor elements and causing nuisance tripping of the unbalance protection.
- The microprocessor can only look at one signal at the time

- If it is impossible to achieve a sampling frequency that secures a correct digital interpretation of the analog signal, the analog signal should be evaluated directly.

5 PQSCADA

PQSCADA is a data base program used to collect measurements from the grid through the SCADA interface. The following measurements are collected from SINTFs database. All of the signals are from HV installations between 132 and 420 kV. Only one measurement point is located close to an industrial rectifier. Other measurements give an overview of typical system conditions and form a foundation for comparison with the limits given in standards and regulations. It was observed that the only instances where the THD was ever outside the steady state limits from FoL [9] was during transients. All of the observed transients were dampened out after at most a couple of periods. The system returned to being well within the FoL limits. Based this it is not expected that the harmonic distortion of the voltage is very close to the FoL limits. These limits are therefore a good worst case scenario. From the measurements close to the industrial rectifier it is found that the characteristic harmonics truly are the predominant injected currents. Even if an unbalanced rectifier will inject other harmonics and Interharmonics this was not a problem at the measurement point. Figure 12 shows the large impact the disconnection of another line can have on the line current. At this instance the power flow was reversed and nearly doubled. The second harmonic dominates during the transient. This could indicate transformers entering saturation. With regards to any nearby capacitor banks the voltage level does not change significantly even though the current is nearly doubled. Figure 13 present another transient from switching operations in the grid. The most important observation from the transients is that they are very short lived, and that the system quickly settles at a low THD. Because the capacitors can handle overloading up to 5 minutes at 1.3 times the rated current. The resonance must be very large. Since the harmonic currents propagate only upwards in the grid, the most important factor with regards to capacitor banks are the voltage harmonics. They will propagate throughout the grid in all directions until they are dampened out.

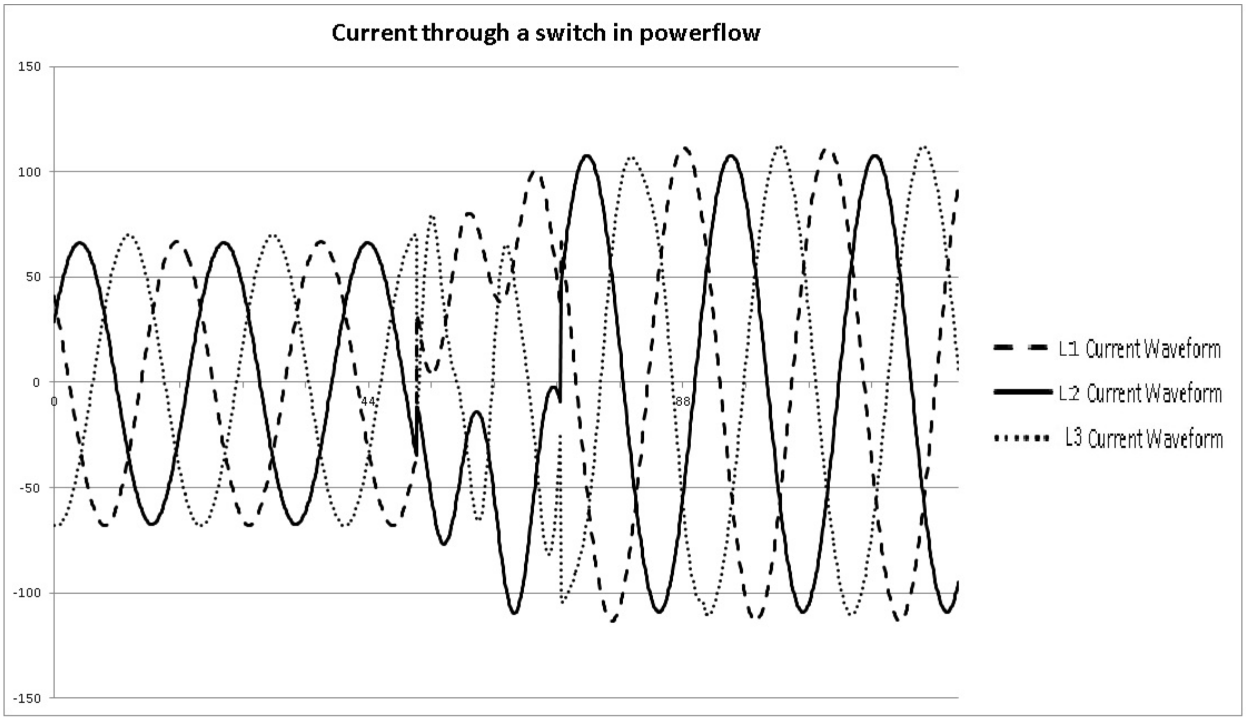


Figure 12: Measurement from a 132kV station. shows the transient that followed a disconnection that reversed the power flow. It went from +10 to -15MW, and 0 MVAr to -2MVAr. The transient current is dominated by the 2nd harmonic.

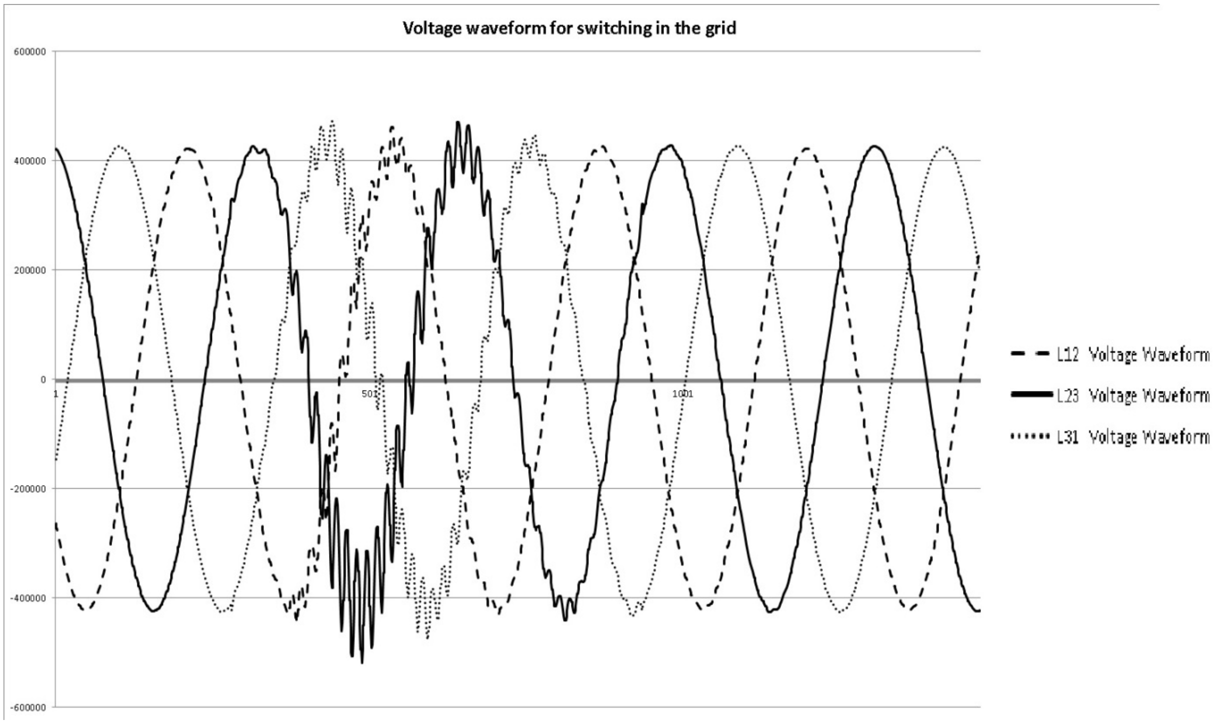


Figure 13: Switching transient in a 400kV station, no change in voltage level

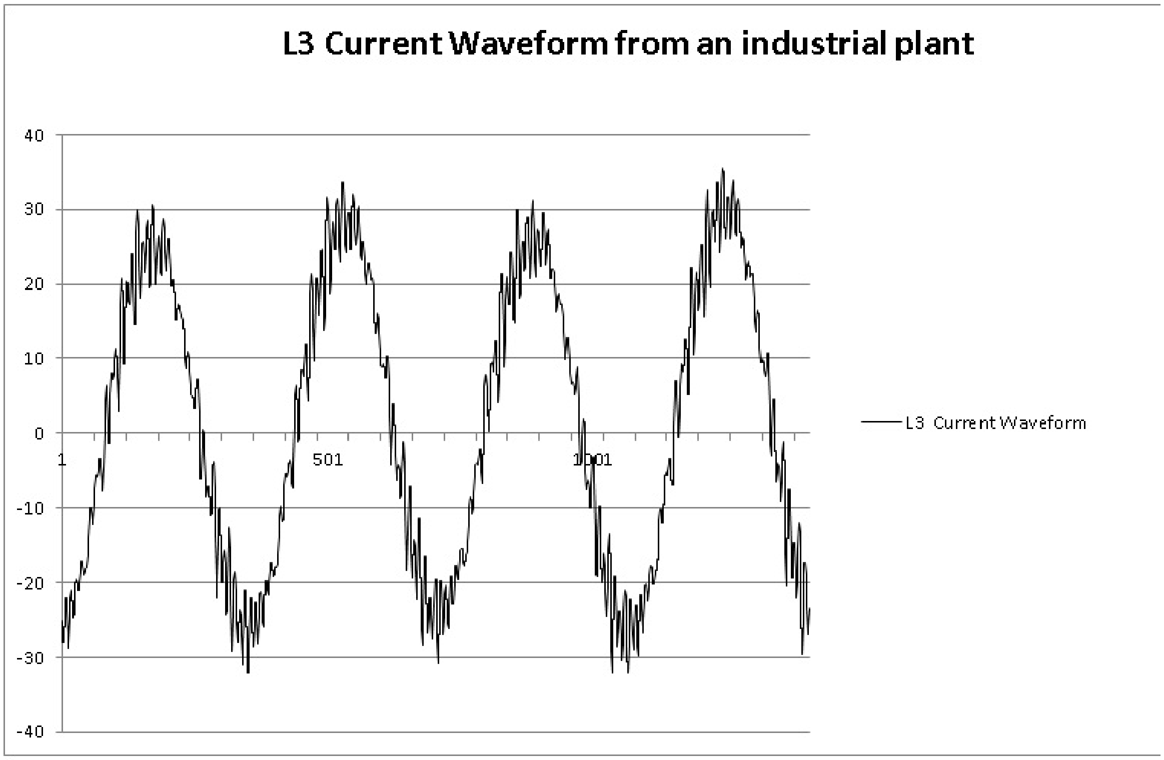


Figure 14 : One phase current from one connection point inside the industrial plant. The most predominant harmonic is the 37th THD is close to 30%.

Figure 14 shows the current measured at an industrial plant. The voltage distortion is only about 0.9%. while the THD in the current is close to 20%. This measurement is not the loads full load current but rather a measurement from one of multiple connection points. At 420kV line to line voltage this current only contributes with approx. 4,3MVA of loading. The very low THD of the voltage at the terminals to the plant indicates that it is either a small part of the load in a strong grid, or there are other loads inside the plant that contributes with far less harmonics. It is also possible that the voltage measurement is taken after a filter that removes harmonics to maintain a THD within the FoL [9]limits.

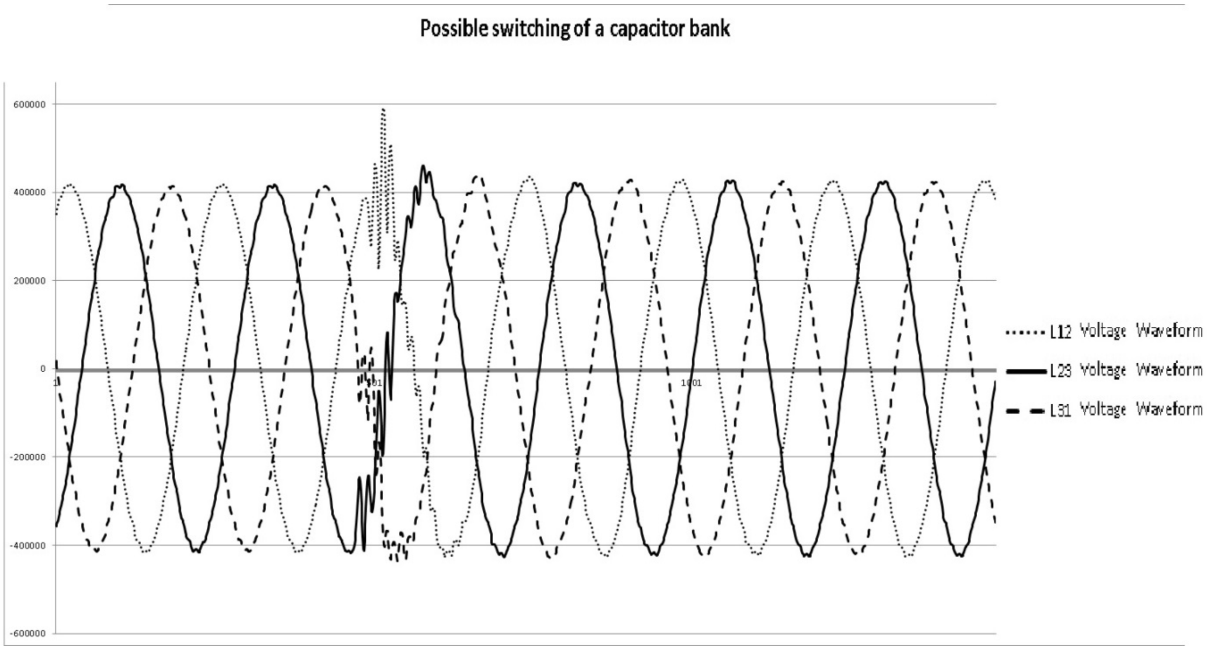


Figure 15: Possible switching of a capacitor bank. Measured at the terminal to the industrial plant

Figure 15 show the transient following after a coupling is made in the grid. The fact that the voltage level is larger after the transient points to this being caused by a capacitor bank being coupled in.

5.1.1 PQSCADA measurements

The measured period with high harmonic content from PQSCADA was repeated and combined to multiple periods with Matlab script 1 given in Appendix F. Then it was analysed with the FFT function in matlab and printed with Matlab script 2 in Appendix F. The results of this FFT analysis are shown in Figure 16. It is observed that the significant harmonics are the 23rd, 25th, 35th and the 37th. As observed in Figure 26 through Figure 29 and Figure 33 there are known resonance frequencies at the 23rd and the 25th. These will be amplified in a similar manner as the 5th and 3rd harmonic is amplified in Figure 35 Figure 37.

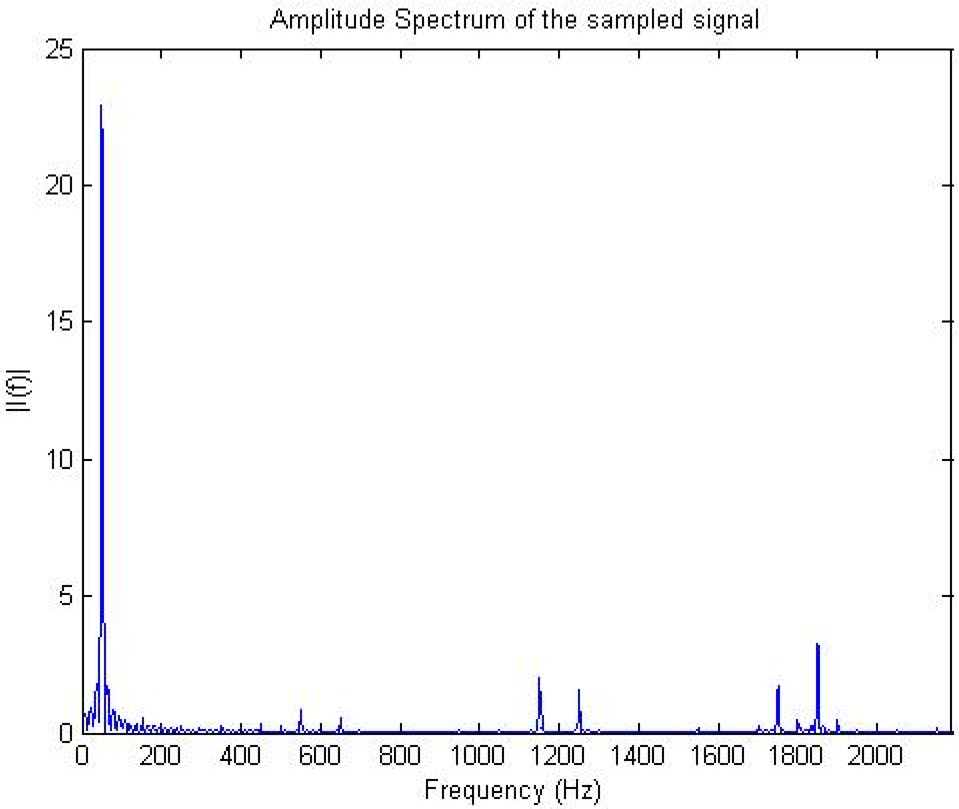


Figure 16: Results from matlab FFT analysis

Simulation with the empirical values from PQSCADA will not provide more information than applying ideal sources at the characteristic harmonics. It is included to show that the predominant harmonics are normally characteristic harmonics close to a rectifier.

6 ATPDraw simulations and results

6.1 Model

The impedance seen from any point in any grid can be calculated by making an equivalent model of the system seen from the desired point. The equivalent impedance contribution from a component can be found using the formulas in [25]. After calculating all impedances including the supply grids short-circuit impedance and replacing the converter with an ideal current source the equivalent circuit is obtained. An example is shown in

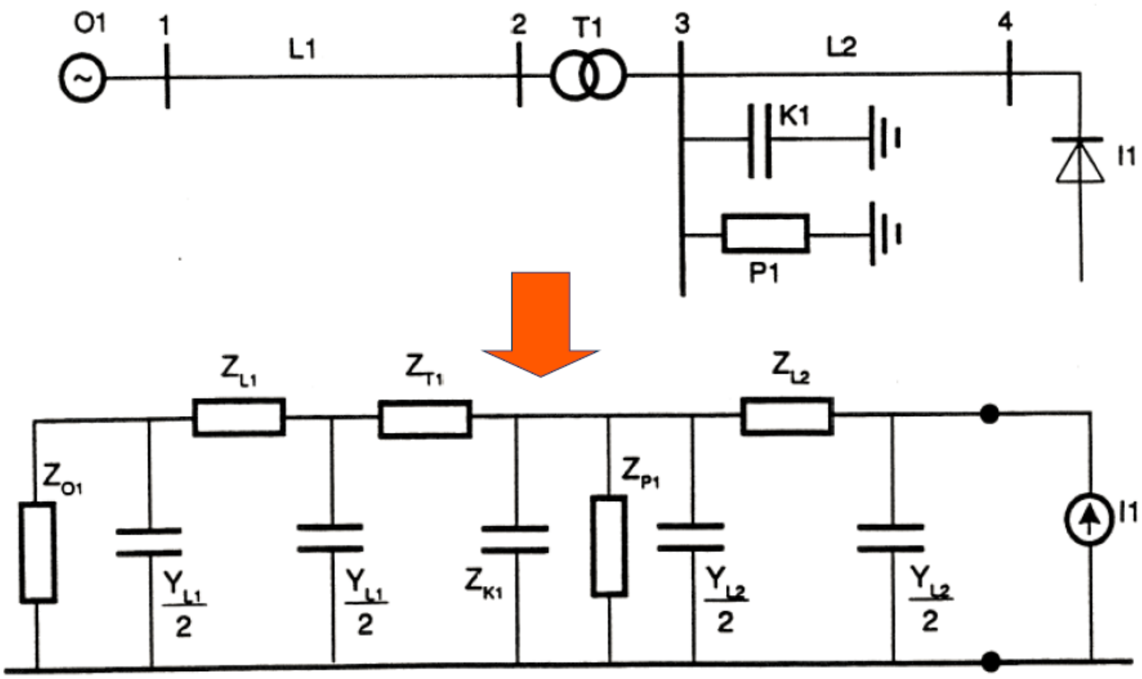


Figure 17: Equivalent circuit for calculating the harmonic impedance from the connection point of the rectifier. Reproduced from [25]

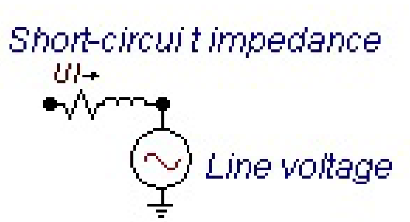


Figure 18: Thevenin equivalent

Since it was impossible to acquire data from an actual nuisance tripping, a more general approach modelling a typical installation has been used. The model is based on data given in the relay plan and data sheets for a typical new capacitor bank installation in Norway [26, 27]. There is no data indicating that this exact capacitor bank has experienced problems with harmonics, but it shows a typical set up of a new capacitor bank installation. Relevant data for the capacitor bank is given in Table 2.

The only available data for the connected grid is the short-circuit power and the voltage level. From Equation 14 the short-circuit impedance can be found. It gives rise to a very simple approximation of the connected grid as a thevenin equivalent see Figure 19. Together with the information given about the capacitor bank the resonance frequency can be found from Equation 8 and Equation 9. The non-linear load is represented as an ideal current source for each of the harmonics present.

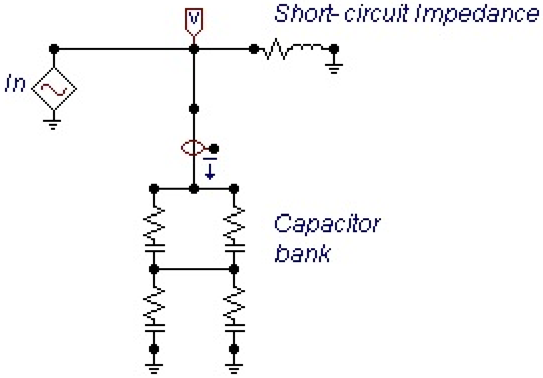


Figure 19: Simple approximation of the system with an unfiltered capacitor bank

J.C.Das [6] states that the short-circuit impedance is a good approximation for the distant power system. However when the harmonic response in a system is evaluated it is essential that the local parts of the system are modelled in detail. Parallel system with capacitances will give rise to other resonance frequencies. The system in Figure 19 will thus only provide parts of the challenge. Even if the resonance frequency found with Equation 9 is avoided, other unknown resonance frequencies can cause problems. To illustrate the effect of local partly capacitive elements such as pi-equivalent of a line, the system in Figure 20 will be evaluated. The line is based on a 420 kV Simplex overhead line in [28].

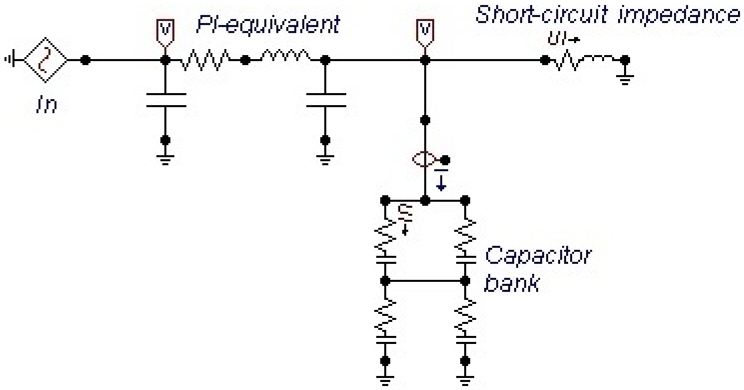


Figure 20: Pi-equivalent added to Figure 19 to illustrate multiple resonance frequencies with an unfiltered capacitor bank

If a real system is to be evaluated the local network should be included as detailed as possible in the simulation. All components in reasonable vicinity of the point where the resonance frequency is to be calculated should be included. Cigré [29] states that at least 2 nodes out from the connection point should be included in the local network. The system outside the defined local network in included in as a lumped short-circuit impedance. Because of the general scope, and lack of one specific system being analysed such a simulation as discussed above will not be attempted. Further reading, and examples can be found in [29] and [6].

The effect of installing an inductor to tune the capacitor bank to a certain resonance frequency is investigated. In addition the more complicated C-type filter is considered. See Figure 21, and . Through testing the system with different short-circuit powers the effect of moving the capacitor bank is also explored. The values used in the simulations can be found in Appendix C.

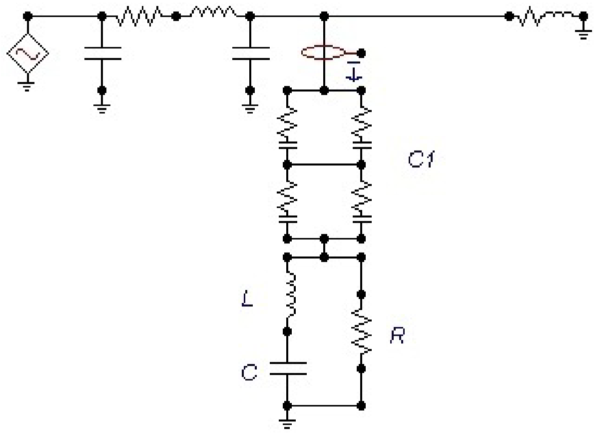


Figure 21: Figure 20 with C-type filter

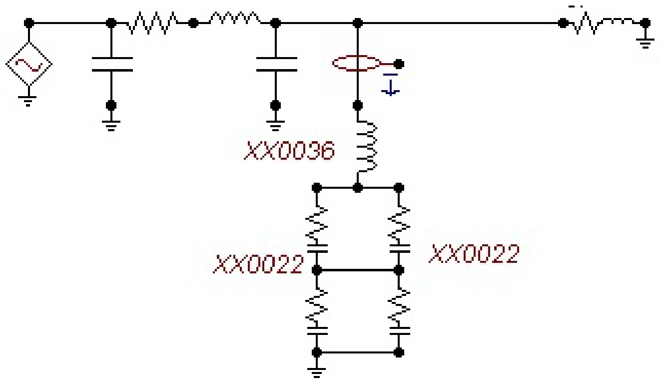


Figure 22: Figure 20 with single-tuned harmonic filter

6.1.1 ATPDraw simulation types

There are three different simulation types; Time domain, Frequency scan, and Harmonic (HFS). Time domain is used when simulating in the time domain to find how the voltages and currents vary with time. Frequency scan and HFS is used to find the systems response to different frequencies. When Frequency scan is selected the user selects the frequency spectrum that is to be analysed and at what intervals. With HFS the user specifies each interval. Frequency scan will be used when the frequency response is analysed in this report. The main reason for using frequency scan is that it is possible to investigate a larger range of frequencies at the same time without large intervals. This is important since small intervals give valuable insight in to the sensitivity of the result. Other than the data given in Table 2, the simulations are based on the parameters given in Appendix C.

Table 2: Capacitor bank datasheet outtakes

Voltage level	**420 [kV]**
Capacitance/phase	2,53 [µF]
Resistance	0.5403 [Ω]
Rated current I_N	192.4 [A]
Short-circuit power	1500-6500 [MVAR]
Reactive power	140 [MVAR]

The Voltage source model in Figure 23 is used to get a better overview since the simulations with harmonic current injection does not load the capacitor bank fully. It only gives the isolated effect of the injected harmonic currents. The voltage sources are equal to the limits given in the FoL[9]. The load is 50MVAr and 50MW. The parameters of the inductive load are given in Table 3. It is slightly larger than the reactive power supplied by one phase of the capacitor bank. Note that the currents injected in the previous examples are much lower than those emerging from these voltages. It is because the load was quite small in the first example.

Table 3: Inductive load 50MW + 50MVAR at 420kV

420 kV Inductive load parameters		
	L [H]	R [Ω]
Inductive load 50MVAr + 50MW	3.743	1176

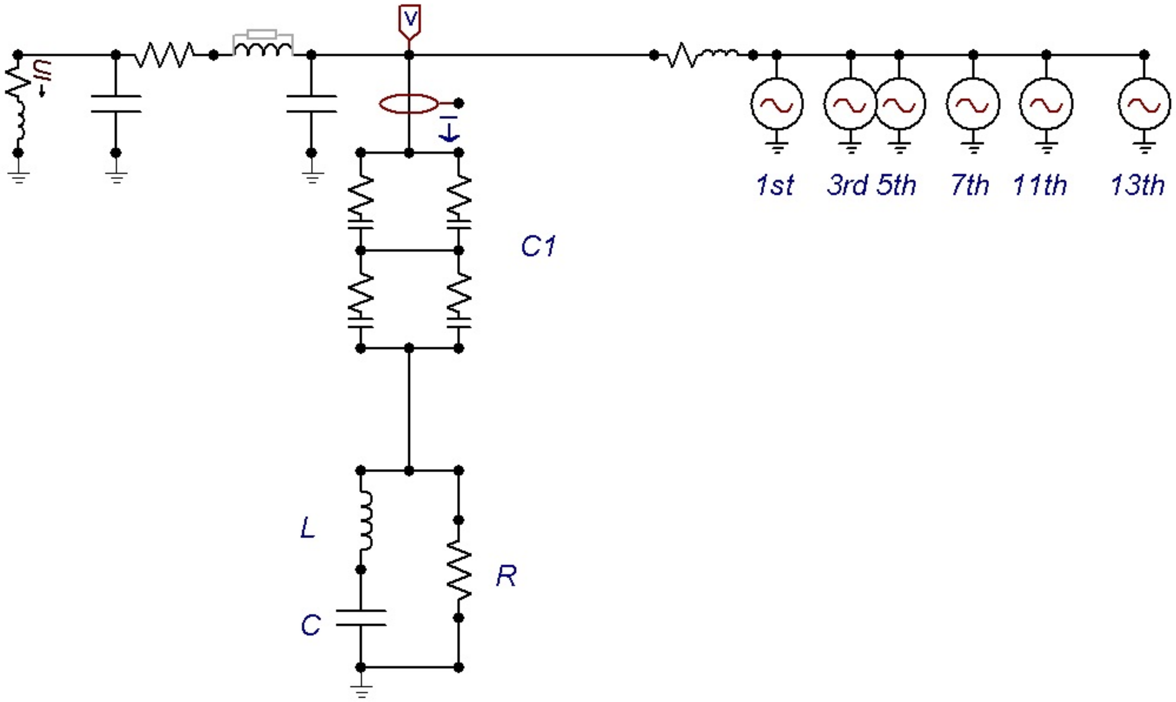


Figure 23: Example of voltage source system in ATPDraw. C-type filtered capacitor bank with short-circuit impedance Pi-equivalent and Inductive load

6.2 Results

6.2.1 Reactive power, frequency scan

The unfiltered capacitor bank will always be capacitive while the filtered capacitor banks become inductive after the tuning frequency. Unlike the Single-tuned filter which becomes purely inductive the C-type filtered capacitor bank become inductive but approaches unity as the frequency increase. The reactive power delivered at the fundamental frequency is reduced by 11% with the single-tuned filter. The C-type filter does not affect the delivered reactive power at the fundamental frequency.

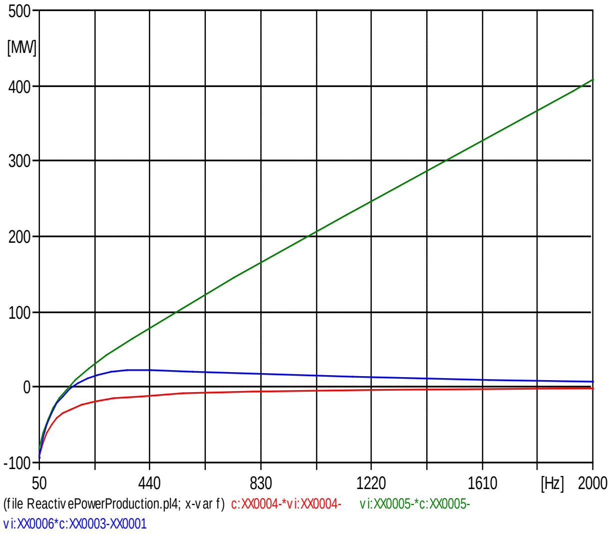


Figure 24: Reactive power production 50-2000 Hz, with Ih = 192.4 A. single-tuned filter (3rd harmonic tuned, green), C-type filter (3rd harmonic tuned, blue), unfiltered (red)

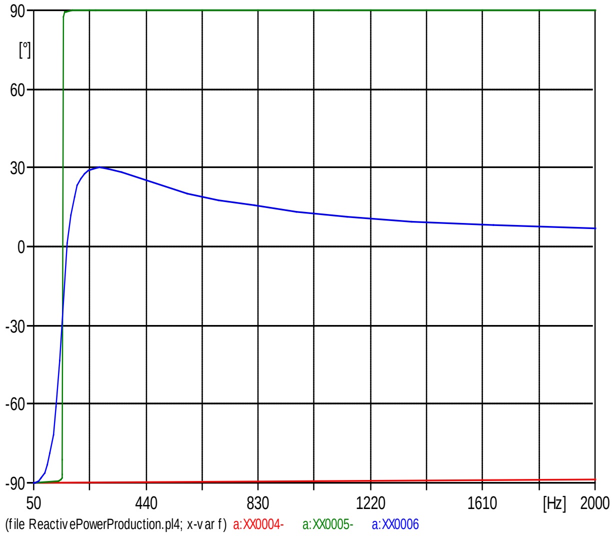


Figure 25: Angle of the reactive power in Figure 24

Table 4: Reactive power supplied at different frequencies

Reactive power						
Harmonic [Hz]	50	150	250	350	550	650
Unfiltered						
Reactive power [MVA]	93,15	31,05	18,63	13,31	8,47	7,17
Angle	-89,975	-89,926	-89,877	-89,828	-89,729	-89,68
Single-tuned						
Reactive power [MVA]	82,89	0,26	32,68	58,52	104,41	126,23
Angle	-89,975	-81,413	89,93	89,961	89,978	89,982
C-type filter						
Reactive power [MVA]	93,15	5,08	15,5	21,37	21,08	19,56
Angle	-89,975	-23,708	29,548	28,311	21,41	18,757

6.2.2 Frequency response of the unfiltered, single-tuned, and C-type filtered capacitor bank

The frequency response of the four systems in Figure 19 through Figure 22 is shown in Figure 26 through Figure 29. In the simplest system there is only observed one resonance frequency. It is between 168 hz and 349hz, depending on the short-circuit power of the grid. Increasing resonance frequency is observed for increasing the short-circuit power. See Table 15 for more details.

When the Pi-equivalent is added to the initial model in Figure 19 an additional resonance frequency appears between 778 and 785 Hz, increasing with increasing short-circuit power. The original resonance frequency is moved to between 149 and 307 Hz.

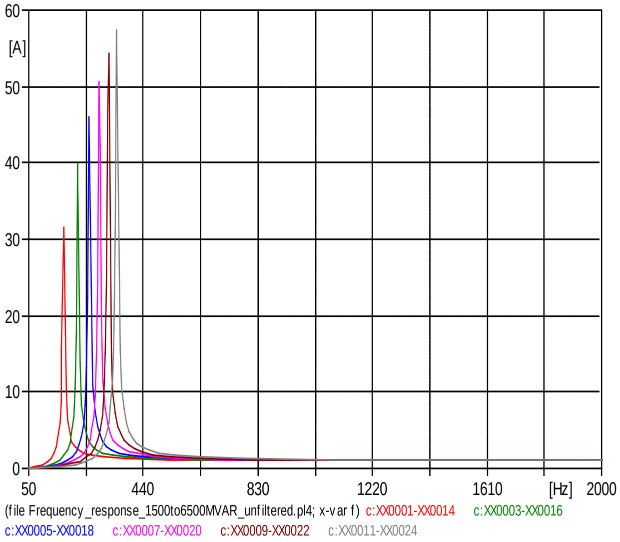


Figure 26: Frequency response of the simple model Figure 19. 1A from the load.

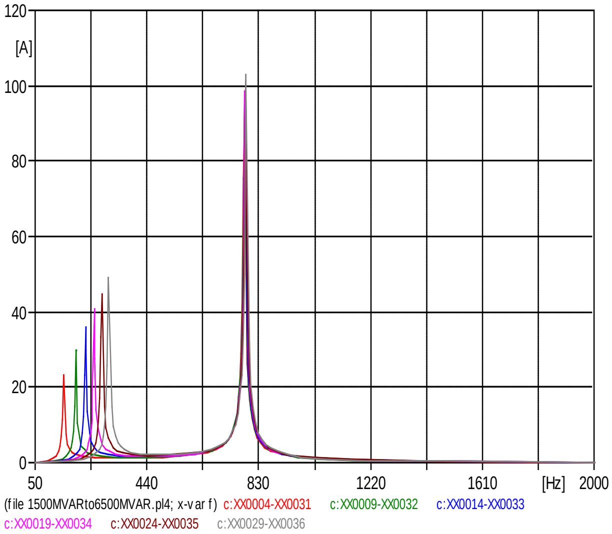


Figure 27: Frequency response for an unfiltered capacitor bank with Pi-equivalent, and short-circuit impedance

With the single tuned capacitor bank the two previous resonance frequencies are lowered further to respectively 93-117 Hz, and 405-564 Hz. A new resonance frequency appears between 1143 and 1360 Hz. Note that both the second and the third resonance frequency has declining amplitude with increasing short-circuit power. This is the opposite of what was observed in the two simulations without the tuned filter.

The C-type filter has a frequency response that is independent of the short-circuit power. It is observed that changing the quality factor Q will change the frequency response. A higher Q will lower the amplitude and cause a slightly higher resonance frequency.

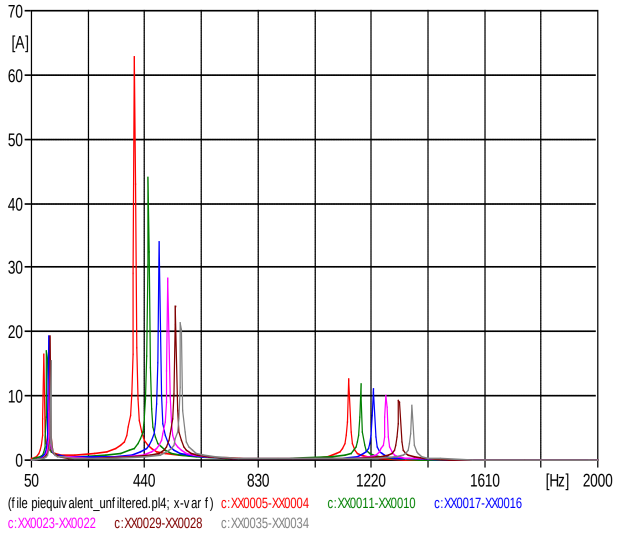


Figure 28: Frequency response single-tuned filtered capacitor bank with pi-equivalent, and short-circuit impedance

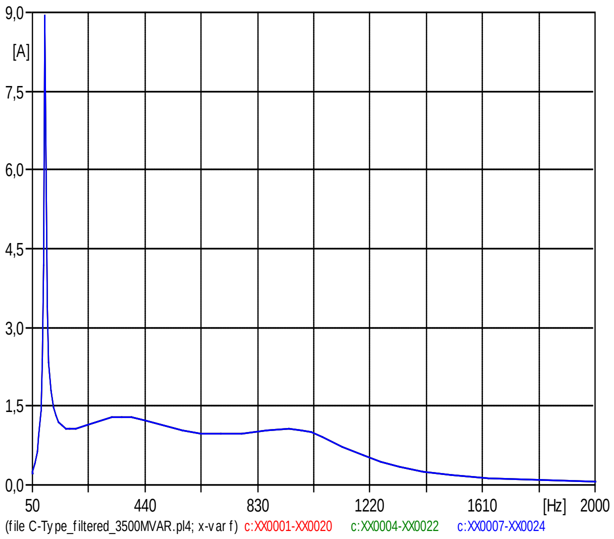


Figure 29: Frequency response C-type filtered capacitor bank with pi-equivalent, and short-circuit impedance

6.2.3 Fourier transform of the unfiltered, single-tuned, and c-type filtered capacitor banks

The unfiltered capacitor bank has a resonance frequency close to the fifth harmonic. A large amplification of the harmonic current is observed in Figure 30. Adding the single-tuned filter removes the resonance frequency from the 5th harmonic, but introduces a resonance frequency close to the 3rd harmonics which is observed to be amplified in Figure 31. The amplification is however not as large as that observed for the unfiltered bank. In Figure 32 where the C-type filter is applied none of the applied harmonics are significant amplified. If the 5th harmonic is disregarding the amplitude of the observed simulations are very similar to those from the unfiltered capacitor bank. Adding the contribution from the harmonics introduced to the normal full loading of the capacitor bank yields that only the unfiltered capacitor bank is overloaded. The rms current through the capacitor bank is calculated from the peak values in Table 19 with Equation 11 and can be seen in Table 5. From Table 5 it can be found that the unfiltered bank is loaded at 1.32 times the rated current.

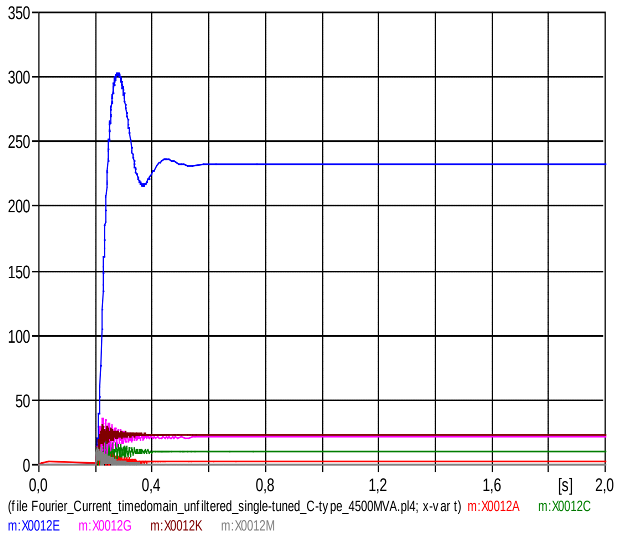


Figure 30: Unfiltered capacitor bank with Pi-equivalent and short-circuit impedance

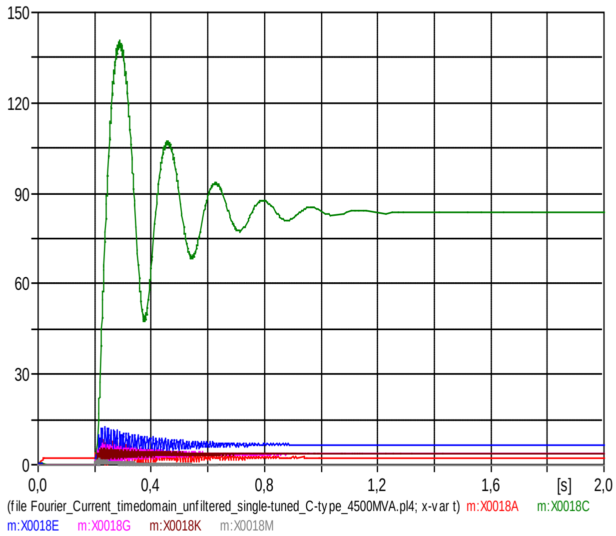


Figure 31: Single-tuned capacitor bank with Pi-equivalent and short-circuit impedance

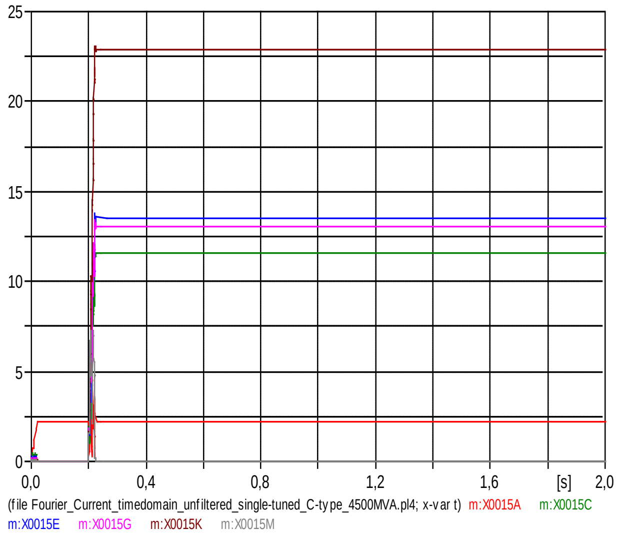


Figure 32: C-type filtered capacitor bank with Pi-equivalent and short-circuit impedance

Table 5: Resulting rms currents through the capacitor bank

Resulting capacitor bank rms current steady state				
	Input	**Unfiltered**	**Single-tuned**	**C-type filter**
I_1 [A]	50,0	1,556	1,697	1,556
I_3 [A]	16,7	7,071	59,185	8,202
I_5 [A]	10,0	164,261	4,738	9,567
I_7 [A]	7,1	14,920	2,546	9,192
I_{11} [A]	4,5	16,405	2,616	16,193
I_{13} [A]	3,8	0,001	0,001	0,001
$I_{RMS,total}$ [A]	**54,4**	**165,9**	**59,5**	**22,5**
$I_{RMS,total}$ [A] with I_N	**193,6**	**254,0**	**201,4**	**193,7**
$I_{RMS,total}$ [p.u] with I_N	1,01	1,32	1,05	1,01

6.2.4 Voltage source with FoL limits on the 3rd to 13th characteristic harmonics

Initially the system was tested with a frequency scan. The input parameters are given in Appendix C. It is observed that the amplification at the resonance frequencies are large for both the unfiltered and the single-tuned capacitor bank. The amplification at the resonance frequencies of the c-type filtered bank is significantly smaller. Only the first is included as the others were approximately zero.

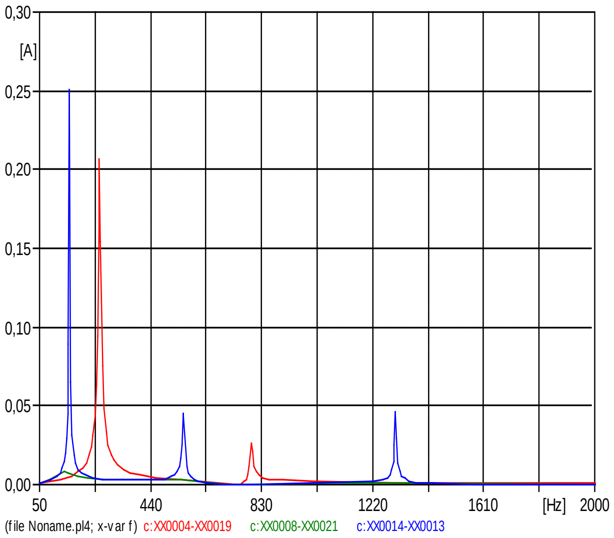


Figure 33: Frequency response of the unfiltered (red), single-tuned (blue), and c-type (green) filtered capacitor bank systems with Pi-equivalent and Short-circuit impedance

Table 6: Results of frequency scan of the voltage source systems

PI-equivalent and short-circuit impedance 4500MVA			
	Unfiltered	**Single-tuned**	**C-Type filter**
1st. resonance frequency [hz]	261	157	137
Peak current [A]	0,207	0,25	0,009
Closest harmonic h [hz]	250	150	150
Peak current at h [A]	0,063	0,039	0,008
Resonance frequency [hz]	794	554	-
Peak current [A]	0,026	0,045	-
Closest harmonic h [hz]	800	550	-
Peak current at h [A]	0,015	0,029	-
Resonance frequency [hz]	-	1301	-
Peak current [A]	-	0,046	-
Closest harmonic h [hz]	-	1300	-
Peak current at h [A]	-	0,043	-

6.2.5 Steady state current waveform and Fourier transform from voltage source model

The current through the unfiltered capacitor bank and the single tuned capacitor bank are both highly distorted. See Figure 34 through Figure 37. The single tuned capacitor bank has a resonance frequency both at the 3rd and the 11th harmonic. In addition it has a resonance frequency at the 26th harmonic. This result in a severe overloading of the capacitor (Table 8) bank with 1.66 times the rated current. In the unfiltered capacitor bank the overloading is caused by a resonance with the 5th harmonic. In total the rms value of the current through the unfiltered capacitor bank is 1.54 times the rated current. As was observed in the current source simulation earlier the c-type filtered capacitor bank is not at risk of being overloaded with the total rms current being 1.04 times the rated value. The actual steady state current is seen in Figure 37 and Figure 38.

Table 7: Resulting peak current from voltage source simulation

Resulting capacitor bank peak current steady state			
	Unfiltered	**Single-tuned**	**C-type filter**
I_1 [A]	278,12	300,76	278,11
I_3 [A]	23,676	264,05	27,552
I_5 [A]	307,15	19,097	29,811
I_7 [A]	44,842	12,635	25,616
I_{11} [A]	22,426	208,03	22,224
I_{13} [A]	0,0026	0,0028	0,0026

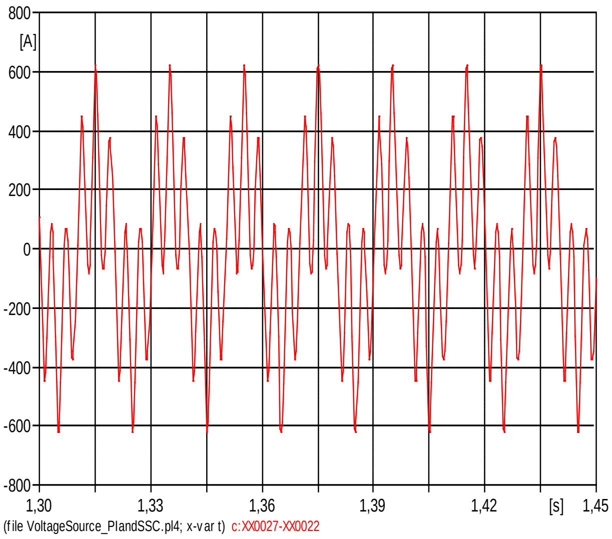


Figure 34: Current through the unfiltered capacitor bank

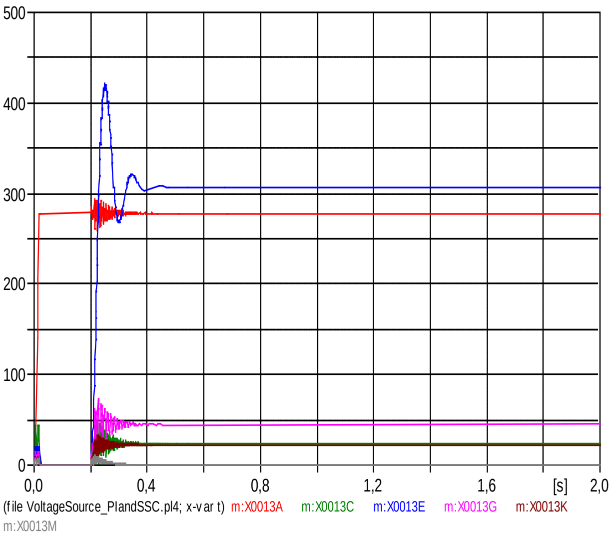


Figure 35: Amplitude of the current components in the unfiltered capacitor bank

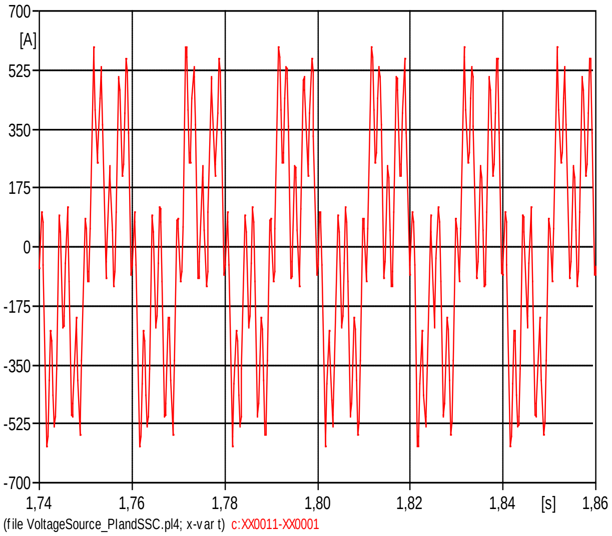


Figure 36: Current through the single-tuned capacitor bank

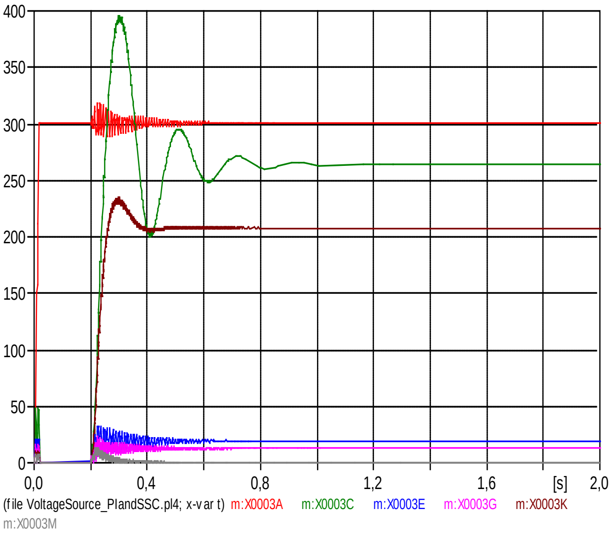


Figure 37: Amplitude of the current components in the single-tuned capacitor bank

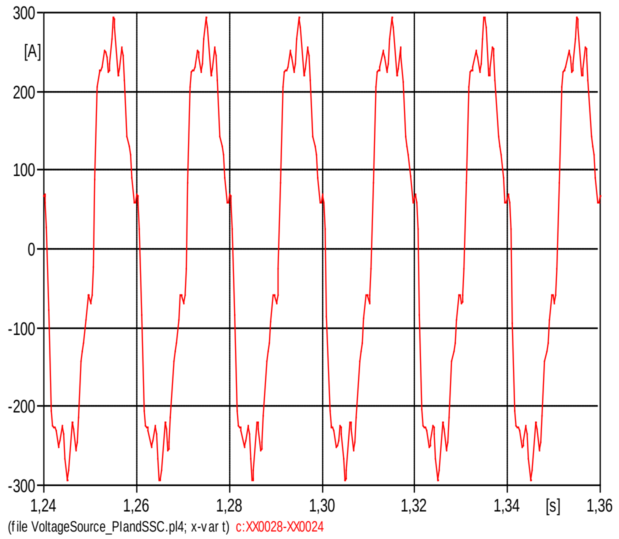


Figure 38: Current through the c-type filtered capacitor bank

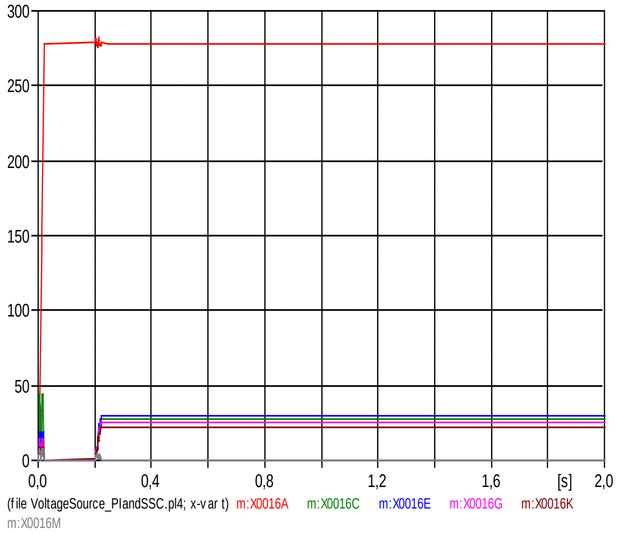


Figure 39: Amplitude of the current components in the c-type filtered capacitor bank

Table 8: Resulting capacitor bank rms current for the voltage source simulations

Resulting capacitor bank rms current steady state			
	Unfiltered	**Single-tuned**	**C-type filter**
I_1 [A]	196,66	212,67	196,65
I_3 [A]	16,74	186,71	19,48
I_5 [A]	217,19	13,50	21,08
I_7 [A]	31,71	8,93	18,11
I_{11} [A]	15,86	147,10	15,71
I_{13} [A]	0,00	0,00	0,00
$I_{RMS,total}$ [A]	**295,61**	**319,36**	**200,18**
$I_{RMS,total}$ [p.u]	1,54	1,66	1,04

7 Discussion

Throughout this text, possible reasons for unwanted tripping of the overcurrent relay, or its failure to detect an overloading and the consequent tripping of the unbalance relay has been discussed. It has been a natural focus around the resonance phenomenon and how excessive harmonic distortion can affect both the capacitors and the relays. The theory has been presented and discussed in section 3 and 4. A summary of these discussions are given before the results from the simulations are investigated.

7.1 Harmonics and resonance

Adding a capacitance to an inductive system will introduce a resonance frequency. Components present at the resonance frequencies will be significantly amplified. Although Interharmonics can be present it is normally the characteristic harmonics that are significant in steady state. Measures should be made to avoid having a resonance frequency at any characteristic harmonic. Even if the closest loads have high pulse numbers and does not emit low order characteristic harmonics they might be present in the applied voltage. Both are capable of causing resonance. The power quality code in Norway [9] states limits for the total harmonic distortion of the voltage. Nonlinear loads inject harmonic currents in to the system. Depending on the harmonic impedance of the system harmonic voltages are induced. A high short-circuit power will yield smaller harmonic distortion than a lower short-circuit power. The harmonic voltages are seen by the rest of the system while the harmonic currents are dampened out quicker and will only be visible upwards in the grid. Lower harmonics are dampened out slower than higher order harmonics. The only parameter that limits the current during a resonance condition is the resistive elements.

7.2 About numerical relays

The LPF which is present at the analog side of all new numerical relays should ideally limit the bandwidth of the analog signal being put through to the A/D converter to well within the limits of its sampling frequency. Removing frequencies outside the relays bandwidth will ensure that the measured values of all components within the bandwidth are without superimposed aliases. If the relay is dimensioned for the harmonics that will be present aliasing should not present any problems. Note that it is impossible to remove aliasing from the digital signal if it is allowed to occur. None the less, all parts of the signal that is outside the bandwidth will not be measured. This can cause the relay to not operate at actual overloading conditions. After a few capacitor elements have failed the unbalance protection will trip, or sound an alarm. The capacitor bank is protected, but it is not the most favourable outcome as at least one capacitor unit probably has to be replaced. It is therefore seen as a sort of nuisance tripping even though it is slightly outside the definition of a nuisance tripping. In general this text regards all conditions that cause unwanted disconnection as nuisance tripping. Resonance causing over loading is thus a nuisance tripping as the capacitor bank should have been designed to avoid that frequency or somehow attenuate the resonance.

Considering that Statnett always use a duplicated relay system on high voltage capacitor banks the probability of a fault going unnoticed by both relays because of manufacturing faults are unlikely. But since the system is put up with focus on the systems security and thus is working on a 1 out of 2 principle false tripping is not reduced by this measure.

Conditions that can cause inaccurate measurements in the relay such as CT saturation, and aliasing will very often cause under estimation of the current. Aliasing can also cause the relay to measure larger measurements than the actual signal. The digital processing algorithms can be wrong for certain special conditions. The only source of information on the impact harmonics have on overcurrent relays was [23] from 1993. It states that microprocessor relays are better than previous technologies, but the microprocessor relays have been improved for 20 years.

7.3 Capacitor bank overloading and resonance

Because of the low impact small amplitude harmonics have on the total rms-current (Equation 11) it is expected that any overloading caused primarily by harmonics originates from a resonance. However light load conditions can cause larger fundamental voltages and consequently larger fundamental currents. This increase has a much larger impact on the total loading of the capacitor bank. It should be removed by the protection system.

IEC [2], IEEE [20], give limits to the manufacturers on what their components are expected to withstand. For the overcurrent protection the limit is 1.3, or 1.35 timed the rated current depending on the standard. In most cases the nuisance tripping is caused by a condition that is truly damaging. Therefore the focus when specifying the capacitor bank should be towards possible remedies for resonance conditions. A large part is to evaluate what harmonics will be present, and to identify the parallel resonances of the connected system. In networked systems with unfiltered capacitor banks there can be a large number of resonance frequencies. See especially [13].

The resonant frequency will swing around depending upon the changes in the system impedance, e.g., switching, operation at reduced load and so on. Similarly an expansion or reorganization of the distribution system may bring out a resonant condition where none existed before.
Even if the capacitor bank in a system is sized to escape current resonance conditions, immunity from future resonance conditions cannot be guaranteed owing to system changes.
One predominant harmonic caused by a resonance is likely to be the cause of an overloading than a more general increase in all harmonics. Equation 11 show that the total rms current and hence the loading of the capacitor bank is proportional to the sum of the squared currents.

7.4 Mitigation of harmonics

It is known that high order harmonics will have a low impedance path to ground through the capacitor bank. The total resistance through the capacitor bank will be larger for high order harmonics because of the increased dielectric losses. However this effect is negligible compared to the reduction in impedance caused by the frequency dependency of the capacitive element. Introducing a reactor, even only a dampening reactor with a low inductance will cause a significant increase in impedance at high frequencies. This will limit the high order harmonic currents going through the capacitor bank. If a larger reactor is installed it can be sized to tune the series resonance of the capacitor bank. A tuned capacitor bank is also called a single-tuned capacitor bank because it is tuned to on frequency. It is important to note that such a filter will only be tuned at one specific short-circuit impedance. The short-circuit impedance will vary over time [6], and the resonance frequency will change. In other words a single tuned capacitor bank only moves the problem to another frequency that might cause resonance at another short-circuit impedance. Another filter is the c-type filter. It is not susceptible to changes in the short-circuit impedance, and introduced no additional losses at the fundamental frequency [13]. It introduces more components that will increase the costs. In addition it must be protected. Whether or not it is necessary depends on the system. But in networked systems with many resonance frequencies it is much more effective than a single-tuned capacitor bank at reducing the resonance problems. At its resonance frequencies the amplitude is significantly attenuated when a c-type filtered capacitor bank is applied.

Other possible solutions are to change the rating of the capacitor bank, or moving the installation to change the short-circuit impedance. If the harmonic emissions from an industrial plant is larger than specified in [9] the utility can insist that they take measures such as installing filters or change to ha rectifier with a larger pulse number. A higher pulse rectifier will significantly reduce the emitted harmonics by removing lower order harmonics.

7.5 Discussion of the results from ATPDraw

In Figure 24 and Figure 25 with details in Table 4 show that the reactive power supplied by the capacitor bank is shown to be unaffected by the c-type filter. If a single tuned capacitor bank is applied the supplied reactive power is reduced with a factor equal to that of the tuning of the filter. When the filter is applied, the circuit becomes inductive at the resonance frequency.

The frequency response of the four systems in Figure 19 through Figure 22 is shown in Figure 26 through Figure 29. It is evident that the addition of a capacitive element adds additional resonance frequencies to the system. This coincide well with [13] and [6] and it is reasonable to assume that a large interconnected system will have many parallel resonances. Therefore only using the short-circuit impedance when planning a capacitor bank installation is insufficient in most cases. Basing the system harmonics only on the injected harmonic currents from one source will only give a part of the problem. It will in most cases not be the only source of harmonics. Because the harmonic voltages in a system is dependent on what is injected in the entire system it is a better source of information. It will also take in to account possible phase shifts in different harmonics. If the harmonic voltages from injected harmonic currents at one point are super positioned on top of the known harmonic voltage it is important to take possible phase shift in to account.

The frequency response of the singe-tuned filter is shown in Figure 28. It is evident that resonance frequencies are reduced. The 3rd harmonic is close to a resonance frequency and is significantly amplified in the appurtenant FFT response in Figure 31. It is however smaller than that of the 5th harmonic without the filter. In addition the 3rd harmonic is very often not present in high voltage systems. Mainly because it is a product of single phase loads, but also because delta wye transformers will not transmit the 3rd harmonic. The single tuned filter is thus sufficient for the system if the harmonics are no higher than the 13th harmonic and the 3rd harmonic is disregarded.

When the c-type filter is applied the amplification of currents becomes much smaller at resonance frequencies. The c-type filter attenuates the harmonics to acceptable levels well within the limits for overloading. From the frequency response in Figure 29 it is evident that the c-type filter will provide a much more consistent means of mitigating resonance problems than the single-tuned filter. The same is observed when the system is altered to consist of a load at the rectifier, and supplied by a voltage source at the far side of the short-circuit impedance. The source is at the limits of characteristic harmonics in FoL [9] up to the 13th harmonic at 420kV including the rated fundamental voltage. The current through the capacitor bank is observed in Figure 33 through Figure 36 to be highly distorted for both the unfiltered and the single-tuned capacitor bank. As in the simulation with injected currents the distortion of the single-tuned capacitor bank originates from the 3rd harmonic and can be disregarded in most high voltage systems operated at steady state. However in this system there are also resonance frequencies at the 11th and the 26th harmonic. Of these two it is only the 11th harmonic that is present, but it is significantly amplified to 147.1 A. Even without the 3rd harmonic the battery will be overloaded with the rms current being 1.35 times the rated current. The current through the c-type filtered capacitor bank can be seen in Figure 37 and Figure 38. It is observed to be much less distorted than the other two solutions. It is similar to the harmonics observed other than the 5th in the unfiltered capacitor bank.

8 Conclusion and further work

Nuisance tripping of overcurrent relays has been defined as tripping when not supposed to. Not tripping when supposed to and consequently causing unnecessary damage and tripping of unbalance protection. Finally conditions where overloading caused by resonance could have been avoided is also defined as nuisance tripping. It is found that to achieve overloading when the fundamental current is at its rated value resonance conditions are necessary. Increasing voltage at the fundamental frequency will quite easily cause overloading during light loads. It is therefore important to disconnect the capacitor bank during light load conditions.

The numerical relay should be setup according to the limits in IEEE and IEC standards according to what standard was used for designing and testing the relays. It is imperative that the relay is specified to measure the highest order harmonic known to be present. If this requirement is not fulfilled harmonics above the Nyquist frequency will be disregarded, and thus the relay might not detect a possible overload. Even though it is highly unlikely that the low pass filter is not working as intended it is noted that this will allow for aliasing and incorrect measurements both larger and smaller than the true rms. In addition Statnetts requirement to always use duplicated protection systems in HV installations will reduce the probability of not detecting an overcurrent.

The accuracy level of the CTs is very low, and saturation should be easily avoided at the relatively low currents measured. Thus it is assumed that the CTs will supply a sufficiently accurate reproduction of the current. A numerical relay can never be more accurate than the supplied signal but in this case the CTs should not be a problem.

Resonance occurs when the resonance frequency is equal to a harmonic present in the system. The particular harmonic will be significantly amplified and is likely to overload the capacitor bank. If resonance occurs the overcurrent relay should trip. It can be argued that this condition should have been avoided in the design phase. Therefore it is also considered as a nuisance tripping. The short-circuit power in a grid is constantly varying and harmonics are rarely confined to the characteristic harmonics. As a result it is impossible to completely remove the possibility of resonance. However, through getting a good overview of the harmonic currents and harmonic impedance will provide a good basis of which to design the capacitor bank. Possible measures to modify the resonance frequency are.

- Moving the capacitor bank.
- Detuning the capacitor bank with a reactor (single-tuned).
- Filtering with a c-type filter
- Dividing the capacitor bank in to smaller units.
- Increasing the rating of the capacitor elements.

Detuning the capacitor bank is very favourable when trying to avoid high order harmonics. In most systems the resonance frequency will be quite low, and while introducing a reactor can move the resonance frequency very low, the losses at the fundamental frequency will become unfavourable. If possible other measures should be evaluated. The single-tuned filter is susceptible to changes in the short-circuit impedance. Thus it will only move the problem to another frequency which is possibly at a characteristic harmonic at some possible short-circuit impedance.

The c-type filter is more complex, but will provide a more general protection against resonance problems. A networked system will have many resonance frequencies, thus a c-type filter is very favourable over a single-tuned or unfiltered capacitor bank. Another advantage is that it will contribute less to additional parallel resonances in the system. On the other hand unfiltered capacitor banks should be avoided to limit the amount of parallel resonances in a networked system.

With regards to avoiding nuisance tripping the most important action is to make sure the overcurrent relay is capable of detecting all harmonics that are present. This will remove the possibility of aliasing. The thresholds should be controlled to check that they are in accordance with the standard of which the capacitor bank is based. Applying means of mitigating resonance conditions where harmonics are significantly amplified will reduce the number of disconnections. Both because of actual overloading, and because of nuisance tripping. It will keep the harmonic loading lower overall to give the relays an easier task. At least that is at the conditions that generated nuisance tripping before. In systems with varying short-circuit power and many parallel resonances the c-type filtered capacitor bank should be the preferred unit.

8.1 Further work

- Conduct a similar test as that conducted by Walter Elmore in [23] on newer overcurrent relays. Preferably both those intended for operation in harmonic rich environments, and those who are not.
- Conduct tests on a real system
- Use a more correct approach to model the connected grid more accurately. For instance as is used in [13] and [6]

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Appendix A: Examples of Aliasing

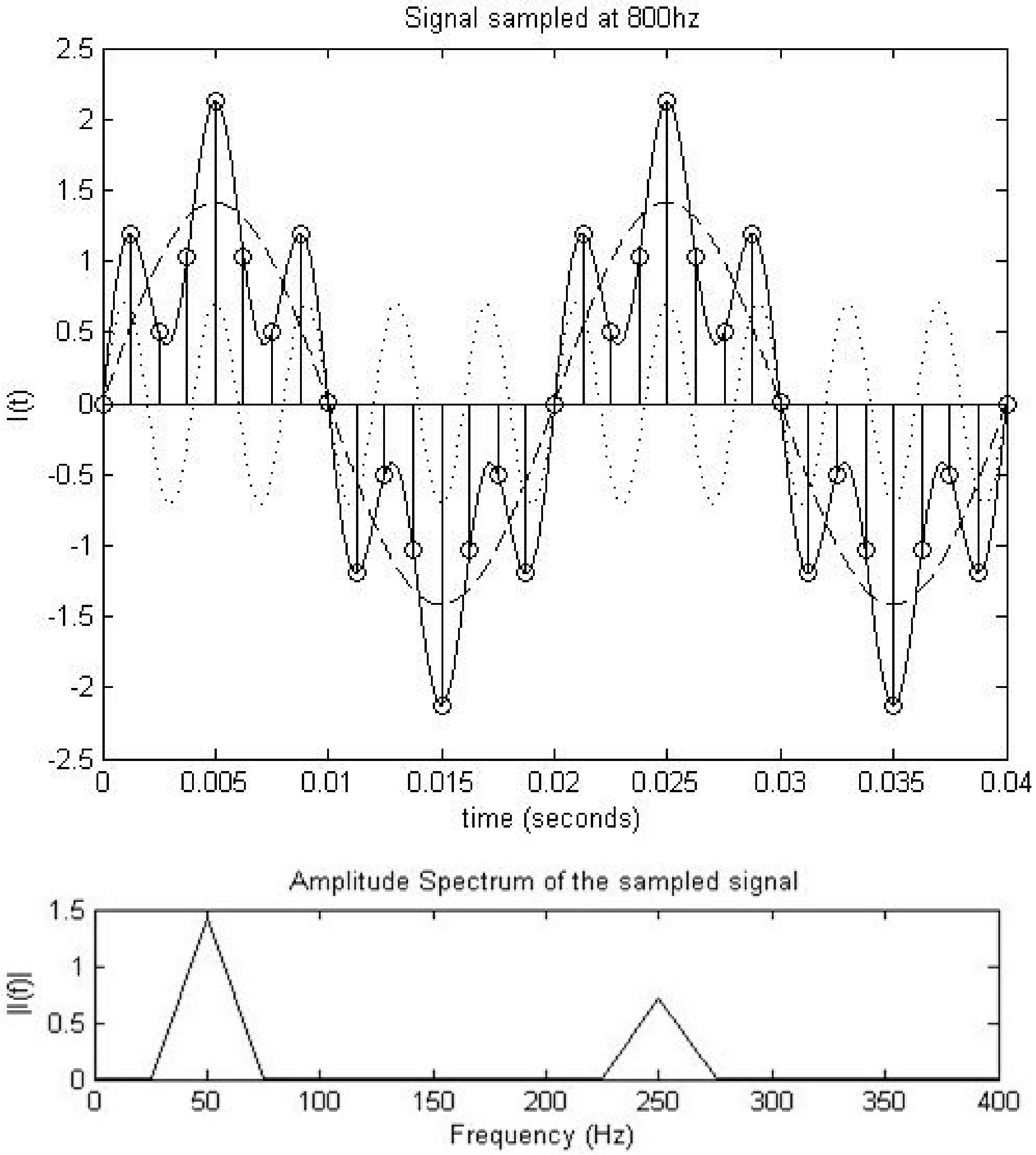


Figure 40: Example of sampling at 800hz, fundamental + 5th harmonic.

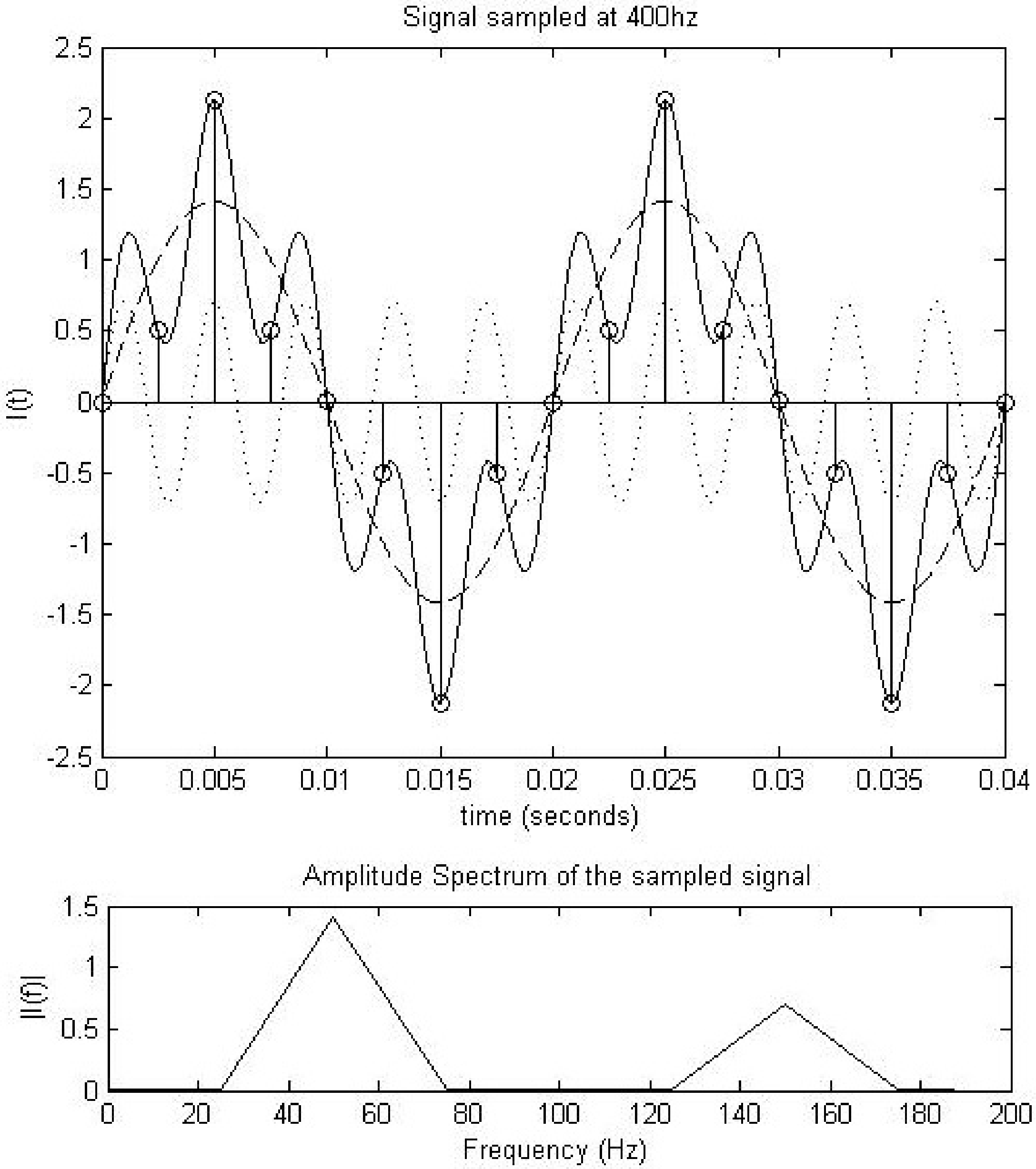


Figure 41: Example of sampling at 400hz, fundamental + 5th harmonic.

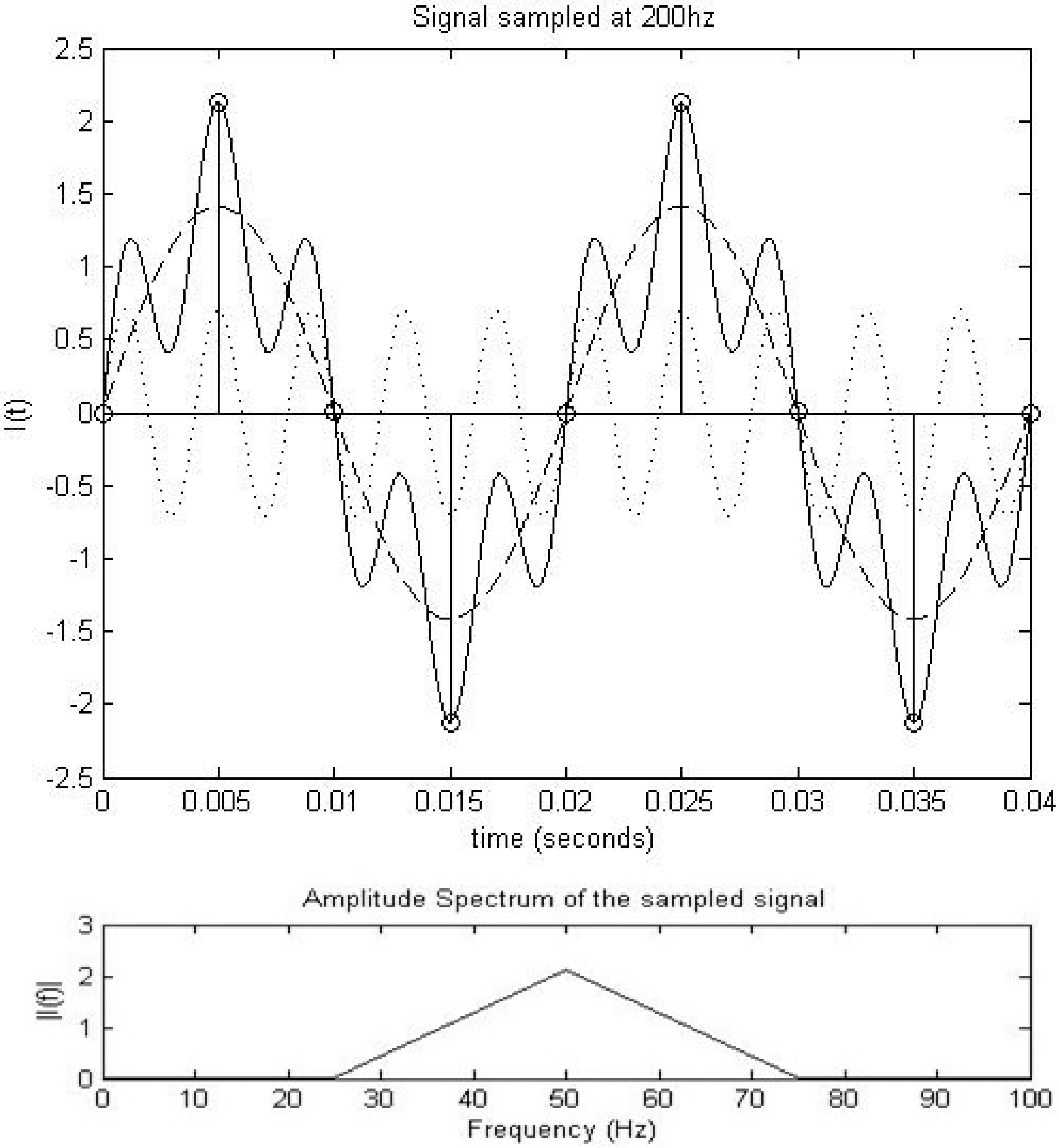


Figure 42: Example of sampling at 200hz, fundamental + 5th harmonic.

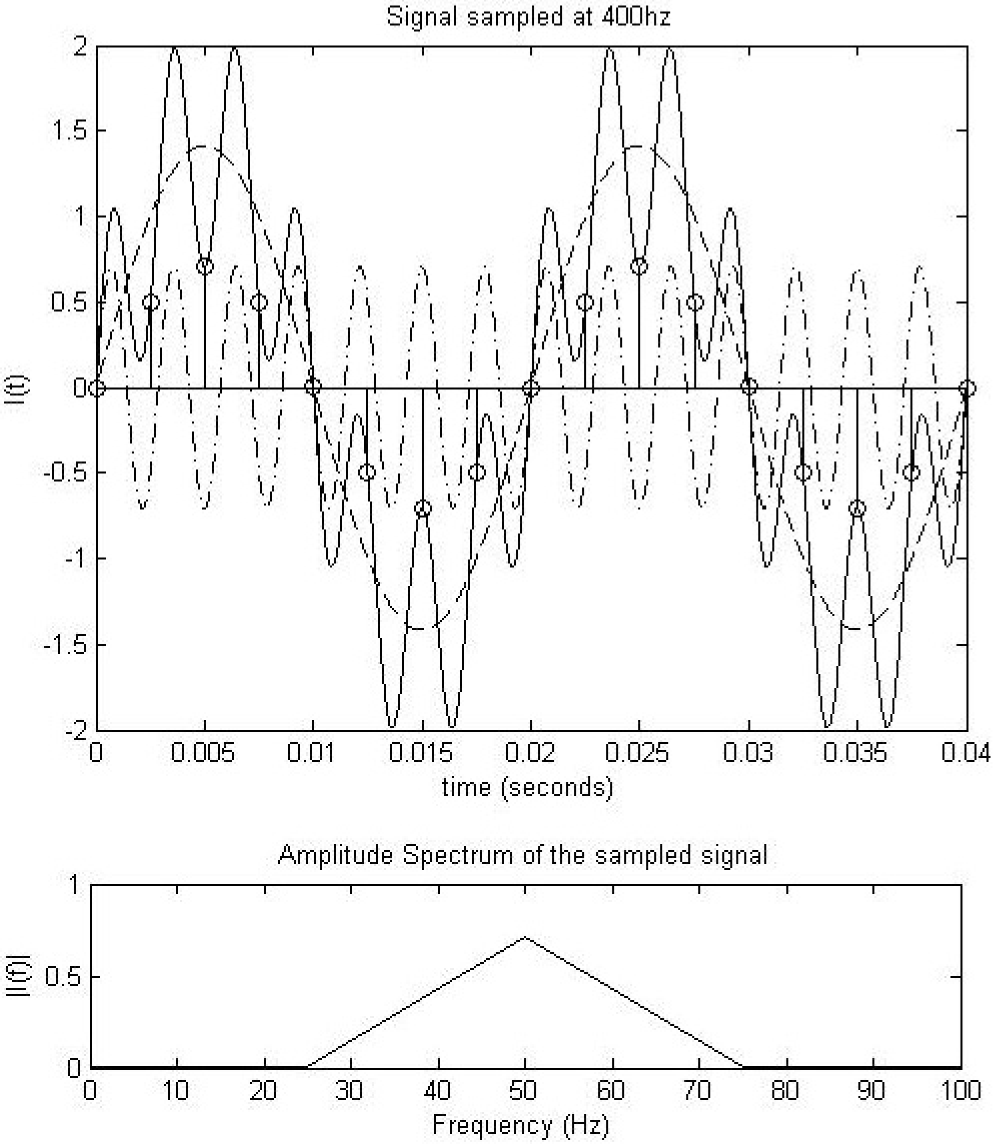


Figure 43: Example of sampling at 800hz, fundamental + 7th harmonic.

Appendix B: The structure of a capacitor bank and its building blocks

This section will explain the structure that is the internally fused capacitor bank. The building blocks of all capacitor banks are the capacitor units. A sketch of a typical capacitor unit can be seen in Figure 44 below. It consists of a number of stacked capacitor elements, each made up of two aluminum foils acting as the electrode separated by a plastic film and rolled to a practical size. Fuses are integrated in the foil.

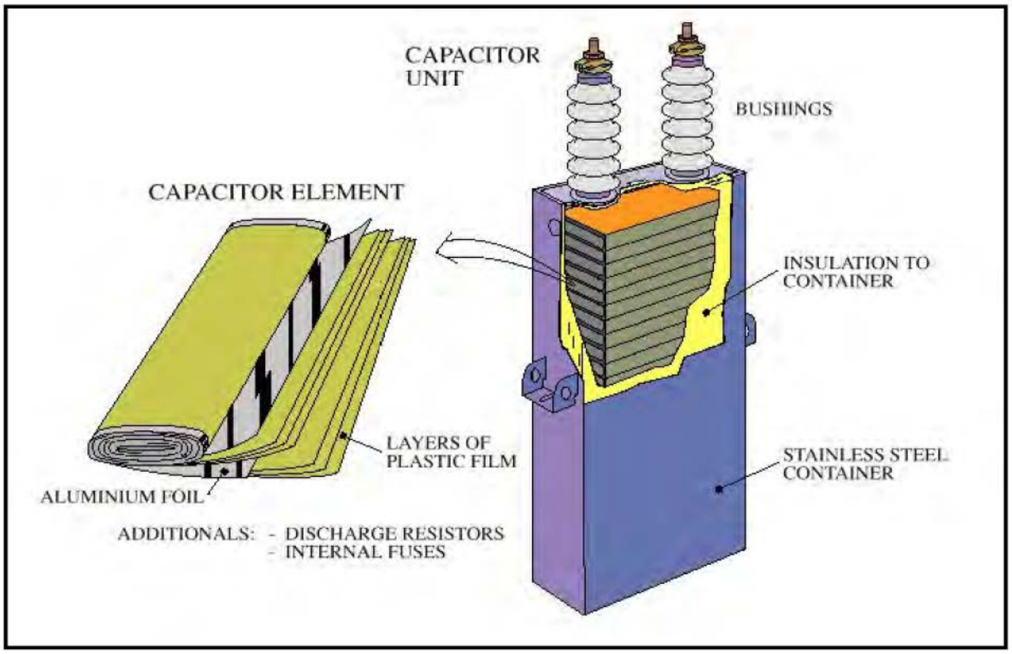


Figure 44: Structure of a capacitor unit [7]

Inside the capacitor unit the capacitor elements are coupled in series and parallel groups to achieve the desired ratings. Internally fused units will have a large number of parallel elements to ensure the voltage levels across elements are less than $1.1U_N$ even after a parallel element has failed and been disconnected by its fuse. From Equation 17, Equation 18, Equation 19, and Equation 20 it is evident that, Parallel elements add to the rated reactive power. Series elements reduce the delivered reactive power but help divide the voltage stresses and thus increase the rated voltage of a unit. How the elements are coupled in a typical unit is shown in Figure 45. Additionally the different components are marked and named.

When a capacitor bank is constructed the capacitor units are coupled in series and parallel groups. The effect is the same as with the elements inside the units. Internally fused units have a large reactive power rating and thus need few parallels. One decisive factor when designing a capacitor bank is to allow for a sensitive detection of the unbalance current arising from failed elements. In large banks it is common to compare either couple the neutrals of a double wye coupled bank, or to measure the unbalance current in an H-bridge for each phase. Both couplings are very favourable in that they remove the influence of any unbalances in the grid. The H-bridge is more sensitive but also more expensive as it requires two more CTs. Because of it sensitivity it is preferred in larger banks where the unbalance current are smaller and the budgets are larger. Simplified examples of each coupling are given in Figure 46 and Figure 47. Both can be installed as grounded and ungrounded systems.

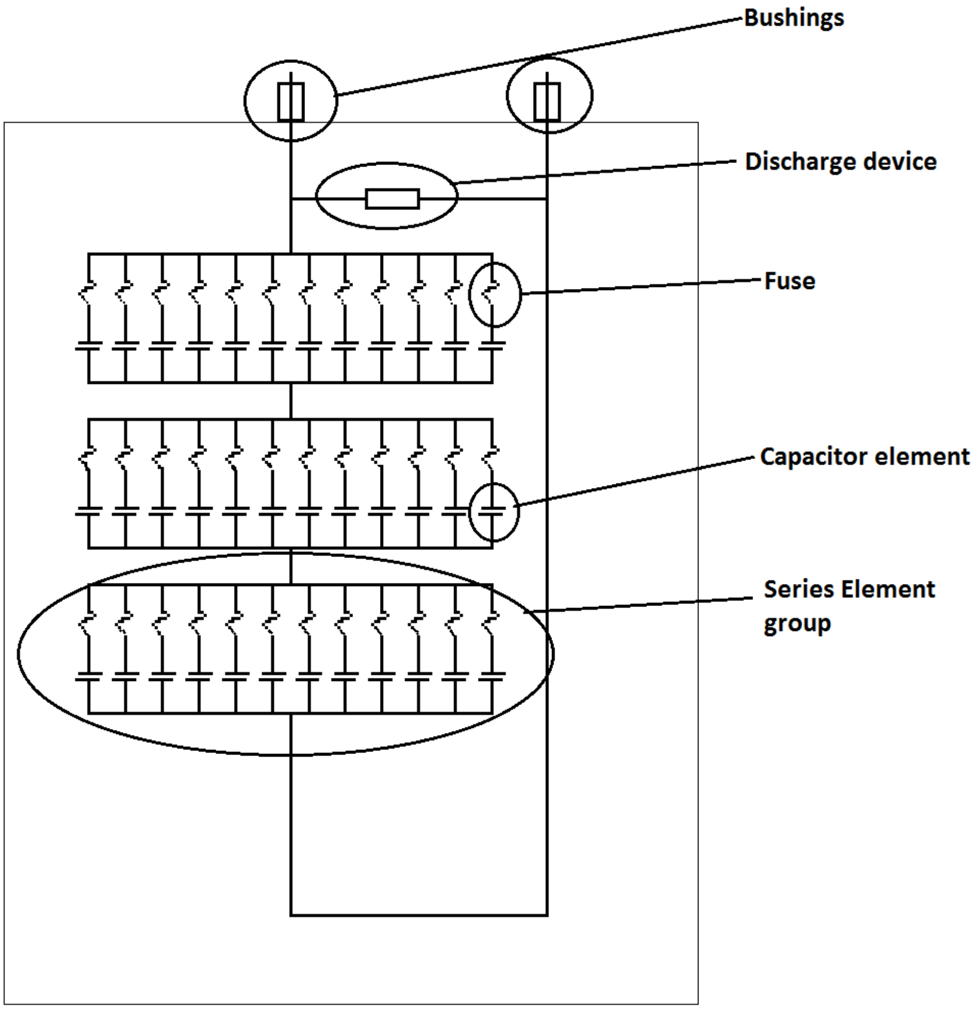


Figure 45: Internally fused capacitor unit

Equation 17: The reactance of a capacitor

$$X_C = \frac{1}{j2\pi f C}$$

Equation 18: The reactive power rating of a capacitor bank per phase

$$S = \frac{U_{L-L}^2}{3X_C}$$

Equation 19: The equivalent capacitance of two capacitances in series

$$C_{eq,s} = \frac{C_1 * C_2}{C_1 + C_2}$$

Equation 20: The equivalent capacitance of two capacitances in parallel

$$C_{eq,p} = C_1 + C_2$$

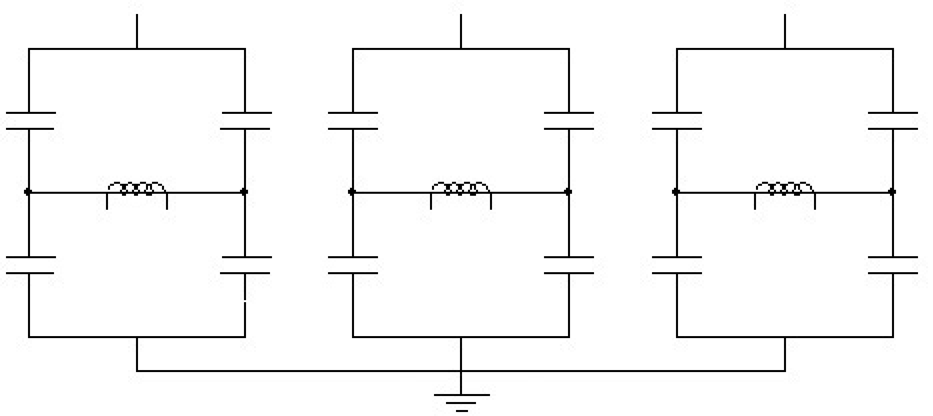


Figure 46: H-coupled capacitor bank. Each capacitor is the equivalent of the series connected units on each side of the H-bridge

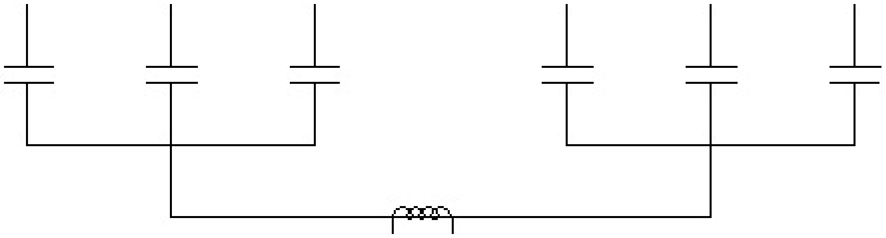


Figure 47: Double wye coupled capacitor bank. The capacitors are the equivalent capacitance of all the units in series and parallel in each phase

Appendix C: Simulation data

Table 9: Short-circuit impedance based on the shot circuit power given in the relay plan for the 140MVAr capacitor bank. Found from S_{SC} using Equation 14. The harmonic order of the resonance frequency is also calculated based on the short-circuit power and Equation 9. The X/R ratio is assumed to be 10. X and R are given at the fundamental frequency.

420 kV					
S_{SC} [MVA]	Z[Ω]	X[Ω]	R[Ω]	L[mH]	h
1500	117,60	112,13	11,21	356,91	3,27
2000	88,20	84,10	8,41	267,68	3,78
2500	70,56	67,28	6,73	214,15	4,23
3000	58,80	56,06	5,61	178,46	4,63
3500	50,40	48,05	4,81	152,96	5,00
4000	44,10	42,05	4,20	133,84	5,35
4500	39,20	37,38	3,74	118,97	5,67
5000	35,28	33,64	3,36	107,07	5,98
5500	32,07	30,58	3,06	97,34	6,27
6000	29,40	28,03	2,80	89,23	6,55
6500	27,14	25,88	2,59	82,36	6,81

Table 10: 100km 420kV simplex Pi-equivalent based on[28]

Pi-equivalent 100 km		
C[µF]	L[mH]	R[Ω]
0,3365	139,4	5,5

Table 11: Single tuned harmonic filter calculations

Single tuned harmonic filter			
X_L =%*X_C	5 %	7 %	11 %
L [mH]	200,54	280,75	441,18
f_{res} [hz]	223,6	189,0	150,8

Table 12: C-type filter calculations based on [13]

Given data		C-Type filter parameters			
S_r [MVAR]	140	Q	1/3	1/2	2/3
f_0 [hz]	50	C1 [µF]	2,53	2,53	2,53
f_n [hz]	150	C [µF]	20,21	20,21	20,21
U_{L-L} [kV]	420	L [mH]	501,3	501,3	501,3
h_n [hz/f_0]	3	R [Ω]	1417,5	945	708,8

Table 13: Input parameters current frequency scan

Input	value
I_{L-G} [A]	1
df [hz]	1
F_{max} [hz]	2000

Table 14: Input parameters voltage frequency scan

Input	value
I_{L-G} [A]	1
df [hz]	1
F_{max} [hz]	2000

Appendix D: Result details

Frequency response

Table 15: Results for the unfiltered capacitor bank with only the short-circuit power. See Figure 19

Only short-circuit power						
Short-circuit power	**1500MVA (red)**	**2500 MVA (green)**	**3500MVA (blue)**	**4500MVA (purple)**	**5500MVA (brown)**	**6500MVA (grey)**
Resonance frequency [hz]	168	216	256	290	321	349
Peak current [A]	31,439	39,89	45,897	50,655	54,277	57,339
Closest harmonic h [hz]	150	200	250	300	300	350
Peak current at h [A]	4,02	5,86	19,23	14,73	6,94	52,92

Table 16: Results for unfiltered capacitor bank, short-circuit power and Pi-equivalent. See Figure 20

Short-circuit power + 100km pi-equivalent						
Short-circuit power	**1500MVA (red)**	**2500 MVA (green)**	**3500MVA (blue)**	**4500MVA (purple)**	**5500MVA (brown)**	**6500MVA (grey)**
First resonance frequency						
Resonance frequency [hz]	149	191	226	256	283	307
Peak current [A]	23,2	29,94	35,95	40,93	44,69	48,86
Closest harmonic h [hz]	150	200	250	250	300	300
Peak current at h [A]	20,6	9,54	4,75	16,42	7,91	18,98
Second resonance frequency						
Resonance frequency [hz]	778	780	781	782	784	785
Peak current [A]	92,52	95,1	97,3	98,69	101,1	102,86
Closest harmonic h [hz]	800	800	800	800	800	800
Peak current at h [A]	16,62	15,58	17	18,7	20,78	23,36

Table 17: Results for single-tuned capacitor bank with Pi-equivalent and short-circuit power. See Figure 21

Short-circuit power + 100km pi-equivalent + single-tuned filter tuned to 3rd harmonic						
Short-circuit power	**1500MVA (red)**	**2500 MVA (green)**	**3500MVA (blue)**	**4500MVA (purple)**	**5500MVA (brown)**	**6500MVA (grey)**
First resonance frequency						
Resonance frequency [hz]	93	103	109	113	115	117
Peak current [A]	16,55	17,05	19,23	15,66	19,22	15,47
Closest harmonic h [hz]	100	100	100	100	100	100
Peak current at h [A]	3,29	4,74	1,41	0,83	0,58	0,45
Second resonance frequency						
Resonance frequency [hz]	405	453	491	520	544	564
Peak current [A]	62,76	43,98	33,96	28,21	23,98	21,24
Closest harmonic h [hz]	400	450	500	500	550	550
Peak current at h [A]	19,29	24,02	8,04	3,39	10,15	3,88
Third resonance frequency						
Resonance frequency [hz]	1143	1184	1228	1272	1315	1360
Peak current [A]	12,32	11,88	10,64	9,68	9,15	8,44
Closest harmonic h [hz]	1150	1200	1250	1250	1300	1350
Peak current at h [A]	4,26	1,96	1,24	1,34	1,62	2,26

Table 18: Results for C-type filtered capacitor bank with Pi-equivalent and short-circuit power. See Figure 22

Short-circuit power + 100km pi-equivalent + C-type filter tuned to 3rd harmonic						
Short-circuit power	**1500MVA (red)**	**2500 MVA (green)**	**3500MVA (blue)**	**4500MVA (purple)**	**5500MVA (brown)**	**6500MVA (grey)**
First resonance frequency						
Resonance frequency [hz]	92	92	92	92	92	92
Peak current [A]	8,93	8,93	8,93	8,93	8,93	8,93
Closest harmonic h [hz]	100	100	100	100	100	100
Peak current at h [A]	3,72	3,72	3,72	3,72	3,72	3,72

Table 19: Resulting peak currents through the capacitor bank

Resulting capacitor bank peak current steady state				
	Input $I_{L-G,rms}$	Unfiltered	Single-tuned	C-type filter
I_1 [A]	50,0	2,2	2,4	2,2
I_3 [A]	16,7	10	83,7	11,6
I_5 [A]	10,0	232,3	6,7	13,53
I_7 [A]	7,1	21,1	3,6	13
I_{11} [A]	4,5	23,2	3,7	22,9
I_{13} [A]	3,8	0,001	0,001	0,001

Appendix E: YOH capacitor bank Unbalance calculations according to IEEE [20]

Table 20: Capacitor bank and capacitor unit construction data from [27]

Capacitor bank construction		
Abbreviation	**Value**	**Description**
S	28	Series groups - total
St	14	Series groups - tap point to neutral
Pt	2	Parallel units per phase
Pa	1	Parallel units on "left" side of string
P	1	Parallel units in affected string
G	0	Grounded
	Capacitor unit construction	
Su	5	Series groups
N	13	Parallel elements in a group

Table 21: Unbalance calculations based on the data in Table 1 and section 8.4.5 in IEEE Std C37.99-2000 [20]

Blown fuses f	Affected capacitor per unit capacitance Cu	Capacitance "H-bridge" to "neutral" Chn	Affected phase capacitance Cp	Affected phase voltage Vln	"H" leg voltage per unit of Vln Vh	"H" current, per unit of total phase current Ih	Voltage on affected capacitor unit Vcu	Voltage on affected element group Ve	Current through affected capacitor Iu
0	1,000	0,143	0,0714	1,000	0,5000	0	1,000	1,000	1,00
1	0,984	0,143	0,0714	1,000	0,5001	0,00030	1,016	1,082	1,00
2	**0,965**	**0,143**	**0,0714**	**1,000**	**0,5003**	**0,00065**	**1,034**	**1,180**	**1,00**
3	0,943	0,143	0,0714	1,000	0,5005	0,00107	1,057	1,296	1,00
4	0,918	0,142	0,0713	1,000	0,5008	0,00158	1,084	1,438	1,00
5	0,889	0,142	0,0713	1,000	0,5011	0,00222	1,118	1,614	0,99
6	0,854	0,142	0,0712	1,000	0,5015	0,00303	1,161	1,840	0,99
7	0,811	0,142	0,0711	1,000	0,5021	0,00412	1,218	2,140	0,99
8	0,758	0,141	0,0710	1,000	0,5028	0,00562	1,298	2,556	0,98
9	0,690	0,141	0,0709	1,000	0,5039	0,00785	1,416	3,173	0,98
10	0,600	0,140	0,0706	1,000	0,5057	0,01149	1,609	4,184	0,97

Appendix F: Matlab scripts

```
11/06/13 20:43  M:\dokument\Masteroppgave 2...\I lengde.m    1 of 1

function IL=I_lengde(b,a);
% b er # perioder, minimum 2
% a er onsket forsterkning av signalet
I1=xlsread('typisk1.xlsx','1 periode','H2:H1397'); %import of excel
                                                   %printout from for
                                                   %instance PQSCADA
I = Ireadx2(I1);
s = 1396; %samples

Iabc = zeros(b*s,3);
Ia=zeros(b*s,1);
Ib=zeros(b*s,1);
Ic=zeros(b*s,1);
for n = 0:(b-1)
    for i = 1:s
        Ia(i+n*s) = I(i);
    end
end

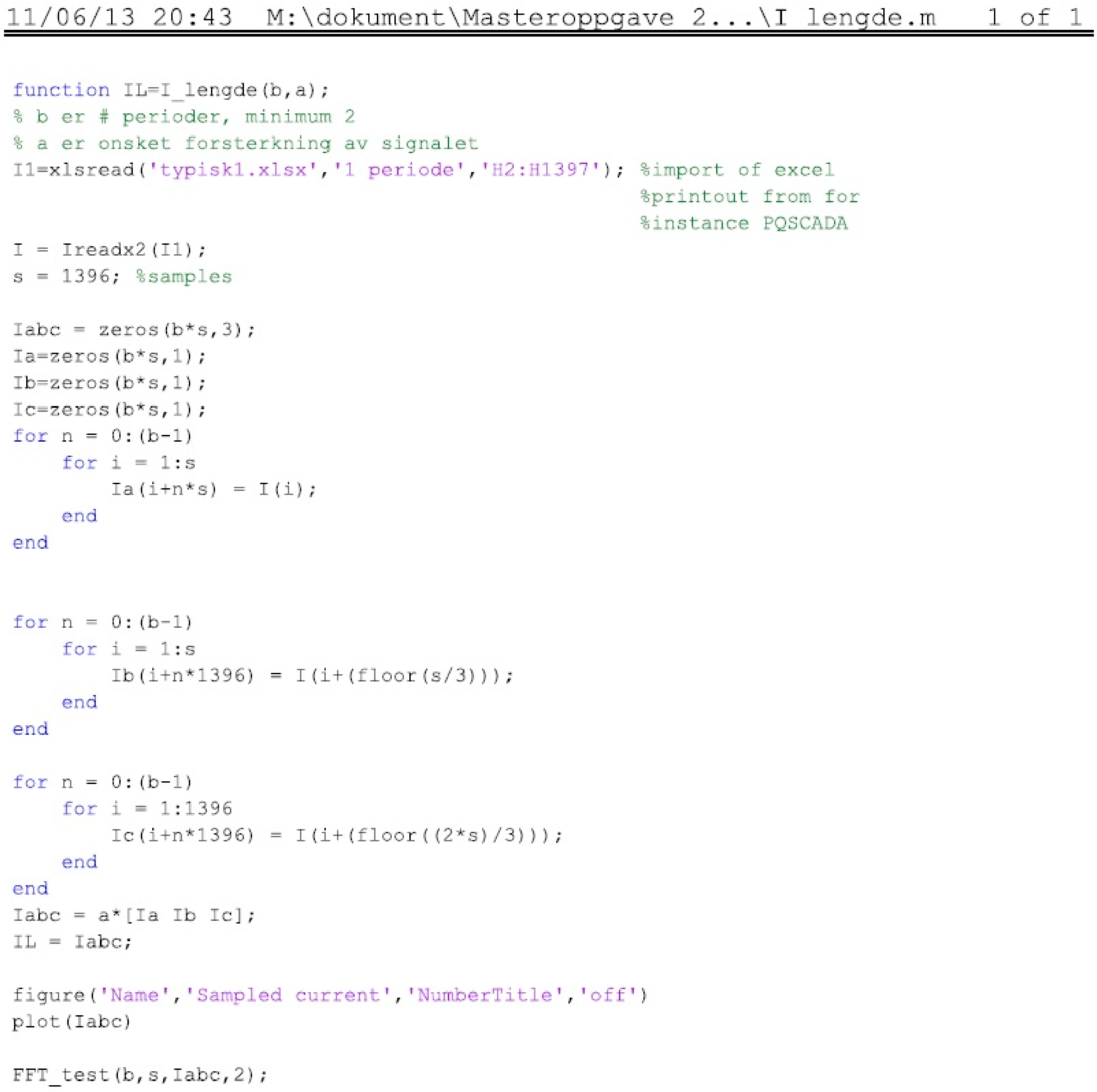

for n = 0:(b-1)
    for i = 1:s
        Ib(i+n*1396) = I(i+(floor(s/3)));
    end
end

for n = 0:(b-1)
    for i = 1:1396
        Ic(i+n*1396) = I(i+(floor((2*s)/3)));
    end
end
Iabc = a*[Ia Ib Ic];
IL = Iabc;

figure('Name','Sampled current','NumberTitle','off')
plot(Iabc)

FFT_test(b,s,Iabc,2);
```

Matlab script 1: Duplicating and combining a measured periode from an excel file



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11/06/13 20:43   M:\dokument\Masteroppgave 2...\I lengde.m    1 of 1

function IL=I_lengde(b,a);
% b er # perioder, minimum 2
% a er onsket forsterkning av signalet
I1=xlsread('typisk1.xlsx','1 periode','H2:H1397'); %import of excel
                                                    %printout from for
                                                    %instance PQSCADA

I = Ireadx2(I1);
s = 1396; %samples

Iabc = zeros(b*s,3);
Ia=zeros(b*s,1);
Ib=zeros(b*s,1);
Ic=zeros(b*s,1);
for n = 0:(b-1)
    for i = 1:s
        Ia(i+n*s) = I(i);
    end
end


for n = 0:(b-1)
    for i = 1:s
        Ib(i+n*1396) = I(i+(floor(s/3)));
    end
end

for n = 0:(b-1)
    for i = 1:1396
        Ic(i+n*1396) = I(i+(floor((2*s)/3)));
    end
end
Iabc = a*[Ia Ib Ic];
IL = Iabc;

figure('Name','Sampled current','NumberTitle','off')
plot(Iabc)

FFT_test(b,s,Iabc,2);
```

Matlab script 2: Running an FFT analysis and plotting the results