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Laboratory Testing of Multi-terminal VSC-HVDC

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Preface

This report presents a summary of the laboratory work conducted during spring 2013 as my master thesis at Norwegian University of Science and Technology. The work has been carried out at the Department of Electric Power Engineering in cooperation with Sintef Energi AS. Laboratory work was done as a continuation of my specialization project written in fall 2012.

I would like to thank my supervisors Kjetil Uhlen and Kjell Ljøkelsøy for their great amount of assistance during the semester. It was pleasure working with Kjell Ljøkelsøy who provided me with needed knowledge about planned configurations in the laboratory as well as theoretical background about the components used in the work. His never-ending enthusiasm over the subject is catching and motivates everyone around him. Kjetil Uhlen helped me to define the general outcome of the dissertation by supporting me with relevant theoretical aid and literature. His clear vision upon the project made it easy to focus on the final outcome.

Georg Kluge gave me a great deal of help during the practical part of the laboratory work. I have learned a lot by working with him on different tasks and his somewhat altruistic helpfulness had a huge impact on receiving the goals in time.

There are several persons on the behalf of Sintef Energi AS whom I need to thank for their friendly advices and helpfulness upon different matters. Salvadore D'Arco and Atle Rygg Årdal assisted me on several urgent problems, saving me valuable amount of time.

Kalle Teearu

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Summary

This report documents laboratory testing of multi-terminal HVDC system in down-scaled model. Testing will be conducted using theory from [1]. First, analytical method for solving DC power flow is introduced and explained. Power flow equations are set up and implemented by means of admittance matrix and Newtons method. Second, laboratory test set-up is presented. Necessary components for steady state tests are described and control and monitoring system is developed. Third, steady state test results are presented and compared with analytical solution of DC power flow. Finally, conclusions on the results and further work are discussed.

Analytical method consists of simple DC power flow equations. Newtons method is explained and Matlab code for finding the solution using iterations is presented. Some simplifications for lower number of power flow equations are made and justification for them is given.

Laboratory test set-up consists of existing and new equipment. Existing equipment will be described briefly and references to relevant documents are given in the following chapters. Missing components in the system were ordered, custom-made or created in conjunction with the two. New equipment is introduced and any further improvements in making the model more realistic are suggested.

Control system for the laboratory test set-up is presented. Existing components in the control system are described together with the description of the signal processing methodology. The structure of controlling the system, as used in the laboratory, is presented and user interface for controlling and monitoring the system is shown. A user interface program is described and code is given.

Testing was conducted in organized manner adding the complexity to the test set-up gradually. Tests are presented so that every next test scenario would have something in common with the one before making the change in outcome easier to observe. Comments on the expected and laboratory values are given, whereas possible reasons for inconsistencies in the results are discussed.

Work on building up a laboratory test system for studying dynamic changes in MTDC systems was started. Results are presented in the second part of the report. Further work for setting up mode true-to-real model of MTDC system is discussed. Any improvements on the existing hardware and software are brought out.

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1 Introduction

1.1 Motivation

In the recent years, attention to renewable energy resources has been increasing due to the ever-growing energy demand and decreasing reserves of fossil fuels. The interest in renewable energy has increased particularly in Europe, where geopolitical situation and the lack of conventional energy resources have led the area to invest in sustainable and local sources of energy.

Among renewable energy resources, wind power has been considered as a sustainable and efficient way of covering a great share of Europe's energy demand. For decades, a number of onshore and coastline wind power facilities have been established, resulting in growing share of wind energy in Europe's energy portfolio. European Council has targeted generating 20% of its energy from renewable resources by 2020 as a part of the energy policy. Incentives are created to motivate research and industry continuing their work towards developments in the sector. All that shows the general direction of Europe's energy policy, regardless of whether the goals set by 2020 are feasible or not. Furthermore, by the year 2050 European Commission has targeted reducing energy related CO_2 emissions back to 1990 level resulting in 85 % decrease [3].

Onshore wind energy has, however, come to limits with rather densely populated areas having a great deal of opposition to nearby wind farms. In addition, more stable and higher velocity of offshore wind entice research and industry focusing to offshore developments. Wind farms, that are relatively close to shore (50 km) are connected to mainland via AC transmission systems. For longer distances, AC systems become economically inefficient due to reactive current compensation in the transmission line. Subsea AC lines longer than 70-100 km HVDC systems become economically less feasible [4], limiting the distance between generation and mainland.

Multi-terminal HVDC systems could improve the overall cost, reliability and functionality even further [5]. An advanced MTDC grid would enable connecting different areas

over long distances with relatively low losses in the transmission lines, resulting in better utilization of renewable energy resources. Combination of North seas wind energy, Southern-Europe's solar power and hydro power in Mid-Europe and Norway enhances the efficiency of renewable energy utilization.

1.2 Voltage source converter

Multi-terminal HVDC grids could, in theory, be based on current source converters (CSC) or voltage source converters (VSC). CSCs, also referred as line-commutated converters (LCC), have existed for decades and their operation is well-known. Control of LCC relies on the AC side voltage. The fact that only turn on of the switching elements in the converter can be controlled, limits the functionality of the technology. VSCs, on the other hand, have better controllability, but come with larger losses in the conversion. Therefore, MTDC system based on VSCs is considered as preferred technology for pan-European super grid [6].

There are a number of different transistors in the market today. There is a great variety of semiconductors differing from function, properties and price. Off-the-shelf products are usually designed so that only some of the parameters are optimized while giving other parameters less attention. This is caused by the cost-effective mass production where, in order to be competitive, producers need to have optimization between cost and performance. Therefore it is very important that customers are aware of the restrictions before they order a specific component such as semiconductor, for example.

Bipolar junction transistors (BJT) and metal-oxide-semiconductor field effect transistors (MOSFET) are two types of semiconductors that have existed for decades and are therefore very well-known. Some of their advantages make them still used today in some applications. BJTs have lower on-state voltage drop and therefore less power dissipation than MOSFETs. Moreover, they have higher available current ratings than its counterpart device. Therefore BJTs are more used in applications where switching speeds are not very high. Power MOSFETs, on the other hand, are much faster devices since there is no charge to be removed or injected. Many of the applications that use BJTs are turning to its newer counterpart due to the need for higher switching frequencies [7].

VSC implement Insulated-Gate Bipolar Transistors (IGBT). IGBTs are fully controllable semiconductors. Turn on and turn off can be controlled by modifying the gate voltage of the semiconductor. IGBTs are relatively new power switches and combine advantages

of both BJTs and MOSFETs. Like MOSFET, IGBT is voltage controlled switch and its switching requirements are very similar to it. In short, lower on-state losses in IGBTs are achieved by the use of additional pn-junction in the structure of the semiconductor device resulting in larger amount of charge carriers. The phenomena is called conduction modulation and is discussed more detailed in [7].

The discussion above leads to the conclusion that the current between collector and emitter of the device can be turned on and off regardless of voltages that are applied to each terminal. That is why VSCs are often referred as self-commutated voltage source converters. Voltage source converter station is able to commutate even when AC grid is weak or unable to support reactive power to converter′s AC terminal allowing to control both active and reactive power independently from one another. This makes it possible, for example, to provide energy via HVDC link to a system performing a black start.

All of the aforementioned makes it clear that VSC is more practical for offshore applications. Wind farms, for example, have unstable power output caused by the variable wind speeds, thus the flexibility of the operation in the DC grid becomes very important.

Majority of point-to-point HVDC connections today are based on LCC technology. The number of VSC-based point-to-point connections is closing to 15, whereas first multi-terminal VSC HVDC connection is expected to be finished in Sweden in 2019 [8]. Existing or planned VSC point-to-point connections can possibly be included into the MTDC network in the future.

1.3   Outline of the report

The body of this thesis is separated into three parts. Chapter 2 introduces the DC network configuration that is of interest in this report. Analytical solution for computing active power flow is developed and explained. Relations between resistances, active powers, DC voltages and DC voltage droops are illustrated. MATLAB code implementing Newtons method was developed and is showed the chapter.

Practical work on setting up laboratory MTDC model is described in Chapter 3. The most important components are brought out and relations between the components are denoted. Software for controlling and monitoring of the test system was developed. A short description of the code of the software is given in this chapter. Laboratory test results are presented and compared to analytical model. Reasoning to any unwanted errors in the laboratory test results is given.

Chapter 4 focuses on DC breaker testing. Current state of technology on DC breakers is given and estimations upon possible future developments are denoted. Tests on resonant DC breaker were conducted and are illustrated and commented in this chapter. Further work on developing a DC breaker for laboratory use is suggested in the end of the chapter.

Further work on the topic is described in Chapter 5. Suggestions for possible improvements in the laboratory are given. In addition, needed improvements for dynamic studies are mentioned. Chapter 6 concludes the laboratory testing of multi-terminal VSC-HVDC. Overall performance of laboratory test set-up is assessed.

2 Analytical solution

In order to evaluate the accuracy of the test results, a mathematical model would have to be created. This chapter introduces the method as well as its association to the test set-up. Approach of handling the network configuration in simplified manner is discussed in the following subsection. This is followed by setting up power flow equations and finally MATLAB code, implementing the equations, is introduced.

2.1 Admittance matrix

Admittance matrix of the DC network is an essential part of power flow equations in analytical calculations. The focus of the experiments is to observe the power flow in MTDC network consisting of three VSCs. At this stage the system is defined as a three-terminal star-connected network with VSC at each end of the line. In order to simplify the power flow equations, $Y - \Delta$ transformation was done as illustrated in Figure 2.1. This reduces the number of nodes in the system resulting in three nodes instead of four.
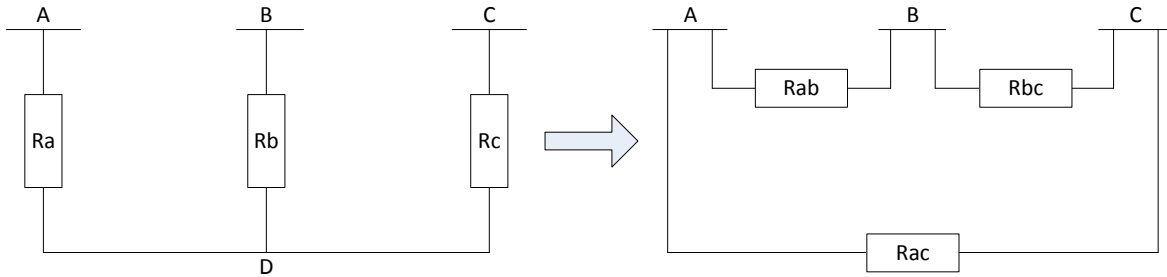
Figure 2.1: $Y - \Delta$ transformation

R_a, R_b and R_c are the resistances between converters and the star point in the DC network. Chapter 3 introduces the laboratory test system in detail. Resistances in the star-connected DC network will be defined and explained. Because of the $Y - \Delta$

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transformation a new relation between line resistances and admittance matrix had to be derived. Equation 2.1 illustrates the general form of an admittance matrix for multi-terminal network.

$$\mathbf{Y} = \begin{bmatrix} Y_{11} & Y_{12} & \cdots & Y_{1n} \\ Y_{21} & Y_{22} & \cdots & Y_{2n} \\ \vdots & \vdots & \ddots & \vdots \\ Y_{m1} & Y_{m2} & \cdots & Y_{mn} \end{bmatrix}, \quad \begin{aligned} Y_{ii} &= \sum_{j=1, j \neq i}^{m} y_{ij}, \\ Y_{ij} &= -y_{ij} \end{aligned} \tag{2.1}$$

Diagonal elements are the sum of admittances to its neighbouring nodes. Off-diagonal elements have negative values of the admittances between the nodes. Admittance matrix can then be re-written for the three-terminal Δ-connected network subsequently:

$$\mathbf{Y} = \begin{bmatrix} Y_{11} & Y_{12} & Y_{13} \\ Y_{21} & Y_{22} & Y_{23} \\ Y_{31} & Y_{32} & Y_{33} \end{bmatrix} \tag{2.2}$$

As discussed above, network configuration illustrated on the right side of Figure 2.1 is used to set up the matrix. Admittance matrix with respect to R_{ab}, R_{bc} and R_{ac} is illustrated in Equation 2.3:

$$\mathbf{Y} = \begin{bmatrix} \frac{1}{R_{ab}} + \frac{1}{R_{ac}} & -\frac{1}{R_{ab}} & -\frac{1}{R_{ac}} \\ -\frac{1}{R_{ab}} & \frac{1}{R_{ab}} + \frac{1}{R_{bc}} & -\frac{1}{R_{bc}} \\ -\frac{1}{R_{ac}} & -\frac{1}{R_{bc}} & \frac{1}{R_{ac}} + \frac{1}{R_{bc}} \end{bmatrix} \tag{2.3}$$

This admittance matrix includes resistances that are not existent in the practical network. In order to express the admittance matrix using resistances from the initial $Y-$connected DC network, $Y - \Delta$ transformation has to be performed. Following equation illustrates the very same matrix with substitute values:

$$\mathbf{Y} = \begin{bmatrix} \frac{R_b + R_c}{R_{Pro}} & -\frac{R_c}{R_{Pro}} & -\frac{R_b}{R_{Pro}} \\ -\frac{R_c}{R_{Pro}} & \frac{R_a + R_c}{R_{Pro}} & -\frac{R_a}{R_{Pro}} \\ -\frac{R_b}{R_{Pro}} & -\frac{R_a}{R_{Pro}} & \frac{R_a + R_b}{R_{Pro}} \end{bmatrix} \tag{2.4}$$

where $R_{Pro} = R_a R_b + R_a R_c + R_b R_c$. This form of admittance matrix is used to set up power flow equations discussed in following section.

2.2 Power flow equations

Power flow equations are set up using substitute network as illustrated in Figure 2.2 and explained in the previous section. Power flow equations are derived using active power, DC voltage, DC droop constant and admittance matrix. Elements in the admittance matrix are calculated using relations from the previous section. General form of DC power flow equations is show in Equation 2.5.
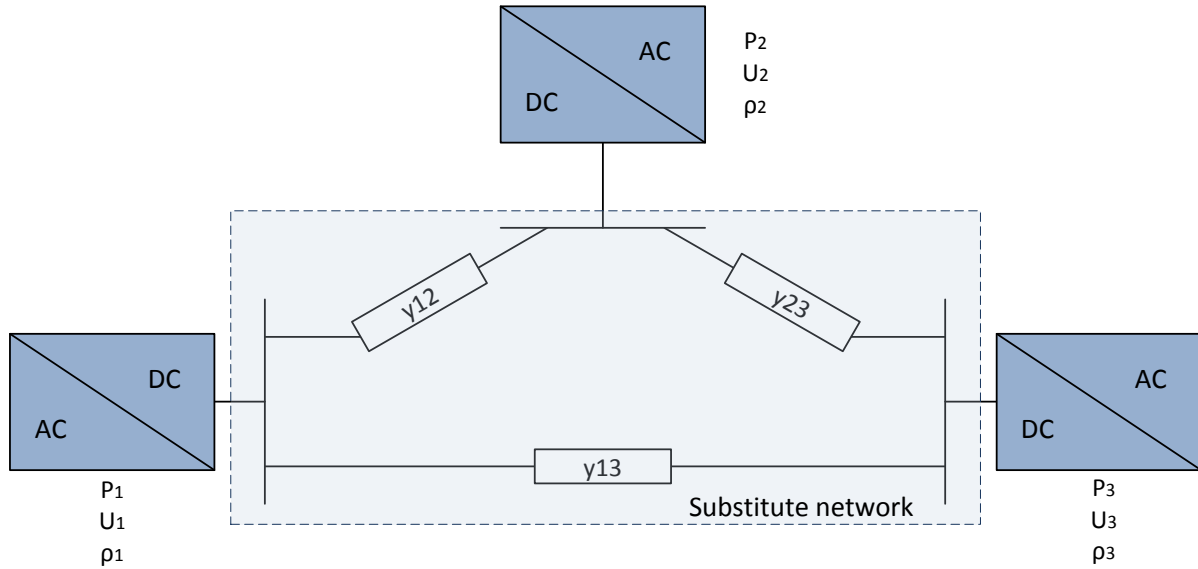
Figure 2.2: Three-terminal DC network with substitute arrangement

$$
\begin{bmatrix} P_1 \\ P_2 \\ \vdots \\ P_m \end{bmatrix} = \begin{bmatrix} U_1 & & & \\ & U_2 & & \\ & & \ddots & \\ & & & U_m \end{bmatrix} \begin{bmatrix} Y_{11} & Y_{12} & \cdots & Y_{1n} \\ Y_{21} & Y_{22} & \cdots & Y_{2n} \\ \vdots & \vdots & \ddots & \vdots \\ Y_{m1} & Y_{m2} & \cdots & Y_{mn} \end{bmatrix} \begin{bmatrix} U_1 \\ U_2 \\ \vdots \\ U_m \end{bmatrix} \tag{2.5}
$$

For the substitute three-terminal DC grid, the load flow equation is as illustrated in Equation 2.6.

$$\begin{bmatrix} P_1 \\ P_2 \\ P_3 \end{bmatrix} = \begin{bmatrix} U_1 & & \\ & U_2 & \\ & & U_3 \end{bmatrix} \begin{bmatrix} Y_{11} & Y_{12} & Y_{13} \\ Y_{21} & Y_{22} & Y_{23} \\ Y_{31} & Y_{32} & Y_{33} \end{bmatrix} \begin{bmatrix} U_1 \\ U_2 \\ U_3 \end{bmatrix} \tag{2.6}$$

All the three VSCs are controlled by DC voltage droop. DC voltage droop is achieved by combining active power and DC voltage controllers. Relation between active power, active power reference, DC voltage, DC voltage reference and DC voltage droop constant is illustrated in Equation 2.7.

$$\begin{bmatrix} P_1 \\ P_2 \\ P_3 \end{bmatrix} = \begin{bmatrix} P_{1ref} \\ P_{2ref} \\ P_{3ref} \end{bmatrix} - \begin{bmatrix} \frac{1}{\rho_1}(U_1 - U_{1ref}) \\ \frac{2}{\rho_2}(U_2 - U_{2ref}) \\ \frac{3}{\rho_3}(U_3 - U_{3ref}) \end{bmatrix} \tag{2.7}$$

Due to the inaccessibility of active power references in the laboratory setup, P_{nref}-s are excluded from the equations. Thus active power inputs into the DC grid are only dependant on DC voltage references resulting in relation illustrated in Equation 2.8.

$$\begin{bmatrix} P_1 \\ P_2 \\ P_3 \end{bmatrix} = - \begin{bmatrix} \frac{1}{\rho_1}(U_1 - U_{1ref}) \\ \frac{2}{\rho_2}(U_2 - U_{2ref}) \\ \frac{3}{\rho_3}(U_3 - U_{3ref}) \end{bmatrix} \tag{2.8}$$

2.3 Newtons method

Newtons method is used for solving non-linear algebraic equations. This method uses iterations, first assuming initial value of the variable being searched, then during the next iteration, using adjusted value based of the derivative $\frac{\partial f}{\partial x}$ [9]. Iterations are repeated until selected convergence criterion ε reaches a low value, meaning that enough accuracy is achieved.

In the given problem, active powers and DC voltages at all three nodes are to be found. DC droop constants and DC voltage references are determined resulting in 6 variables and three equations. Using power flow equations expressed by 2.6, following convergence criteria are obtained (Equation 2.9).

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$$\varepsilon_i = U_i(U_1 Y_{i1} + U_2 Y_{i2} + U_3 Y_{i3}) + \frac{1}{\rho_i}(U_i - U_{iref}) \tag{2.9}$$

Jacobian matrix consisting partial derivatives of convergence criteria with respect to node voltages is illustrated in the following equation:

$$\mathbf{J} = \begin{bmatrix} \frac{\partial \varepsilon_1}{\partial U_1} & \frac{\partial \varepsilon_1}{\partial U_2} & \frac{\partial \varepsilon_1}{\partial U_3} \\[2mm] \frac{\partial \varepsilon_2}{\partial U_1} & \frac{\partial \varepsilon_2}{\partial U_2} & \frac{\partial \varepsilon_2}{\partial U_3} \\[2mm] \frac{\partial \varepsilon_3}{\partial U_1} & \frac{\partial \varepsilon_3}{\partial U_2} & \frac{\partial \varepsilon_3}{\partial U_3} \end{bmatrix} \tag{2.10}$$

Voltage values for the next iteration are found as illustrated in Equation 2.11. Convergence function is multiplied with inverse of Jacobian matrix and then the product is subtracted from previous iteration voltage vector:

$$\mathbf{U_{n+1}} = \mathbf{U_n} - \mathbf{J^{-1}} * \varepsilon \tag{2.11}$$

Examples for calculating partial derivatives in the Jacobian matrix are given in Equations 2.12 and 2.13.

$$\frac{\partial \varepsilon_1}{\partial U_1} = 2U_1 Y_{11} + U_2 Y_{12} + U_3 Y_{13} + \frac{1}{\rho_1} \tag{2.12}$$

$$\frac{\partial \varepsilon_1}{\partial U_2} = U_1 Y_{12} \tag{2.13}$$

Matlab code was created to implement the method discussed above. Figure 2.3 illustrates the procedure in the program. Droop constants, admittance matrix and reference voltages are inserted into the operation and they remain unchanged during the execution of the program. Initial values for DC voltages are 600 V. Based on the con-
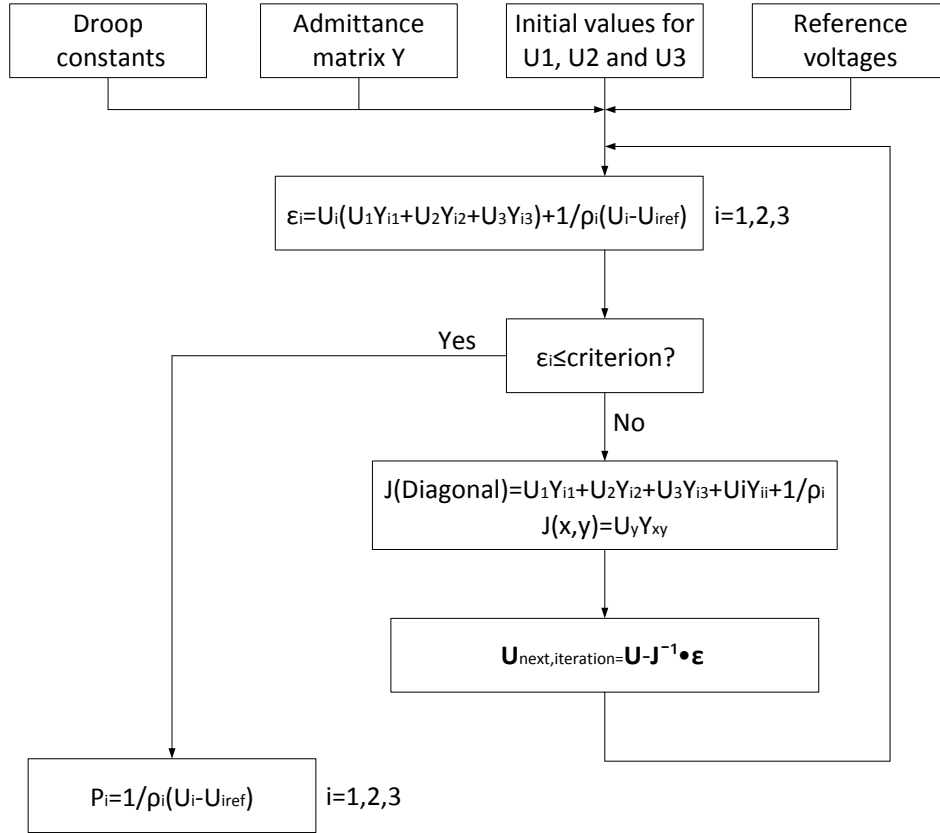
Figure 2.3: Newtons method for solving three-terminal DC network

vergence criterion it is decided whether another iteration is needed or not, or in other words, whether the result is close to real value or not. If ε satisfies the specified criterion, then active power is calculated and no more iterations are conducted. If not then elements in the Jacobian matrix are adjusted for next iteration using analogy from Equation 2.12 for diagonal elements and Equation 2.13 for off-diagonal elements.

Matlab code, implementing the method, is illustrated in Appendix D.

3 Steady state testing

3.1 Laboratory set-up

This section describes the laboratory test system. All parts of the DC network are brought out here and values for the components are calculated or given on the basis of experimentally found values. Some components were custom-made just for the project, while others have been developed over the years in collaboration with ongoing projects that Sintef Energi AS and NTNU have had.

In the laboratory testing, a number of simplifications are made, among them using lower voltages. Down-scaling of the system was handled and discussed in [10] where preferred values for different measures were calculated. These values, however, can be adjusted in the following argumentation, whereas the change in these values is brought about by additional information obtained during the set up.

Effects of the simplifications are discussed after the testing together with the results.

3.1.1 Description of laboratory VSC

Parhaps the most important components in testing multi-terminal DC grid are voltage source converters (VSC). This section introduces the VSC that was used in the laboratory set-up. More detailed information about the VSC is given in memo [11]. The memo includes specific information about the VSC and it various applications, properties and parameters.

The VSC used in the laboratory is designed for low voltage applications. Acceptable AC voltage level is up to 400V whereas DC voltage can be 750 V at its maximum. Rated power for the converter is 60 kVA and it is designed for various applications. All these applications are not handled here and only relevant data is given.
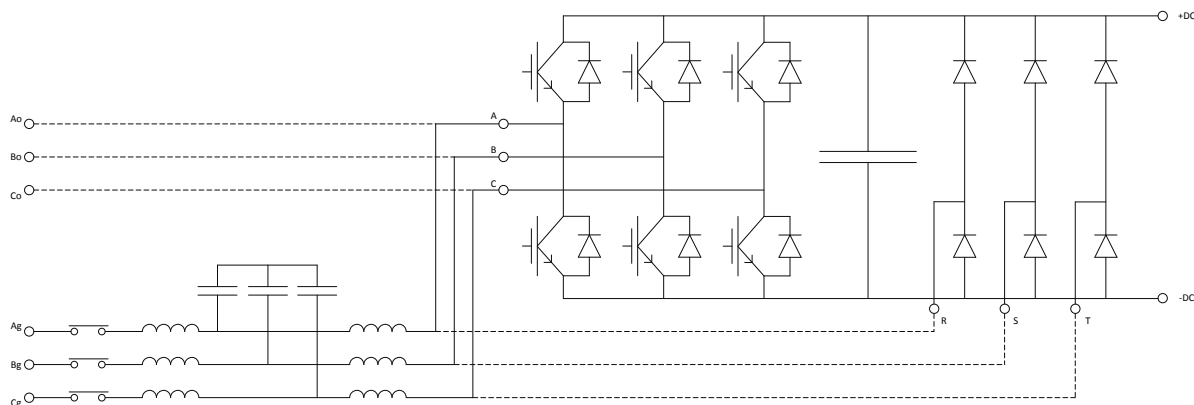
Figure 3.1: Principal layout of laboratory VSC

Figure 3.1 illustrates the general construction of the laboratory VSC. Inverter module and filters are the main parts of the converter. On the left hand side of the figure LCL filter is shown. Converter is connected to the grid via the filter for protecting converter from sudden current and voltage transients. The rest of the figure represents a pre-made inverter module consisting of IGBT bridges, DC-link capacitor and rectifier. Dotted lines are not used in the normal operation of the converter as they become important for motordrive application, which is not handled in this report.

Inverter module

This part of the VSC is the fundamental component. It consists of 6 IGBT modules, 1 capacitor bank, three-phase input rectifier and a driver board. IGBT modules are designed for 400A at 1200V. Capacitance between IGBT bridges and three-phase rectifier is 14 mH. There are two three-phase rectifiers in the laboratory VSC. One of them is a part of the inverter module and is not used in the current application. The second diode rectifier is also connected to the DC-terminal with the duty of charging the DC-link. It is important to have DC-link charged before the connection to avoid a huge inrush current to the capacitor.

Table 3.1: Inverter module parameters and purpose

6 IGBT modules:	400A and 1200V, perform PWM
Capacitor bank:	14 mF, Stable DC voltage
Three-phase diode rectifier:	Charging DC-link
Driver board:	Power supply to gate drivers, protection functions, allowing maximum switching frequency of 6kHz

Filters

The filter that is used in the VSC has two inductors on both side of the capacitors. Parameters are given in Table 3.2. There are several reasons to have LCL filter in the VSC. Having LCL filter ensures that high frequency pulse-width modulated voltage and current wafeforms could not enter the AC grid. It is also critical to have inductance on the AC side of the capacitor when running multiple converters in parallel. Otherwise two capacitors from different converters would be short circuited causing high currents in the AC cables between them.

Table 3.2: VSC filter parameters

Converter side filter inductor L1:	500 uH
Capacitor C:	50 uF
Grid side filter inductor L2:	200 uH

Main contactor and measuring

Main contactor is a three-phase AC switch which is located between AC grid and LCL filter on Figure 3.1. There are several safety functions regarding the operation of the switch. If there are some failures in the system, then main contactor (also named as supply contactor) becomes blocked [2, 11]. After engaging the main contactor, charging circuit is turned on via another set of contactors between AC circuit and charging diode rectifier. When desired DC voltage level is reached, this circuit turnes off again and drivers for the IGBTs become unblocked.

Measurements are done in three different locations on the converter. First, current measurement on the AC side uses three current transducers, one for each phase. They are located between LCL filter and IGBT bridges. Second, AC voltage measurements

are carried out by LEM trafoshunts which are positioned right at the same point as the previously mentioned current transducers. Finally, voltage transducers measure the voltage at the DC side of the converter.

FPGA control board

Vital part of the laboratory VSC is its control system. Physically the control system consists of multiple microcontrollers communicating with each other without any processor. For time-restricted components FPGA module is used. A LCD display and buttons are used as user interface for adjusting settings of the converter. User can change parameters and adjust references depending on the desired operation. The converter control system is also equipped with CAN interface which enables controlling references remotely, instead of using aforementioned LCD display and buttons. Software part of the FPGA board is handled in the following chapter whereas detailed information can be found in [2].
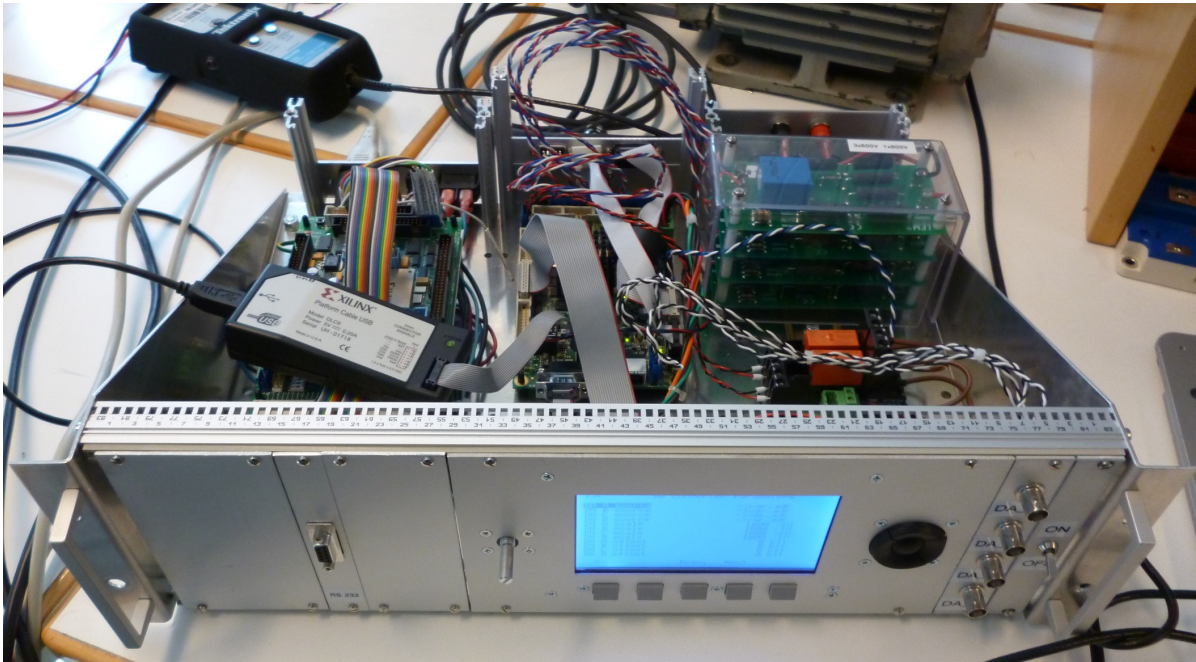

Figure 3.2: FPGA converter controller board

3.1.2   DC Busbars

In order to connect multiple DC lines at one connection point, custom-made terminals are used. The purpose of these components is to have well-organized DC terminals allowing safe and clear overview of the DC grid connections. Each of the busbars have 5 terminals, whereas three of them are equipped with two measuring instruments; one operates in common mode and the other in differential mode. Using common and differential mode helps determining the fault type in the DC network. Busbar is illustrated in Figure 3.3. Busbar plates are equipped with ground connection. Figure A.2 shows an image of the DC busbars.
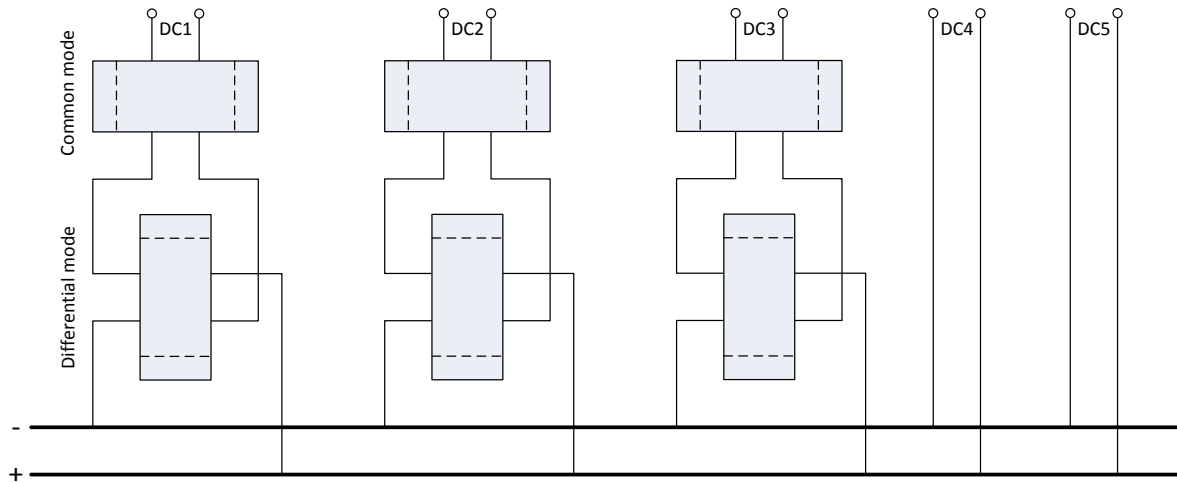
Figure 3.3: Principal scheme of DC busbars

3.1.3   DC line models

In a complete representation of VSC HVDC grid, DC lines ought to consist of resistances, series inductances and parallel capacitances forming π-equivalent for receiving the most accurate behaviour of the DC grid in transient process. In essence, DC grids are more vulnerable to short circuits due to less inductance in the DC lines. In this report, however, transients are not of interest and thus series inductances and parallel capacitances do not have a huge effect on the results. Therefore setting up a DC line model with only resistances is prioritized.

Resistive DC line models consist of three resistor units that are series connected and have parallel set of switches enabling to short any one of them. The values of the resistors are 50m, 100m and 200m, enabling tuning between 0m and 350m with 50m steps. DPST (double pole, single throw) switches were used to bypass each of the three steps. The model is illustrated in Figure 3.4. Due to its robust layout the switches should only be operated under no load conditions.
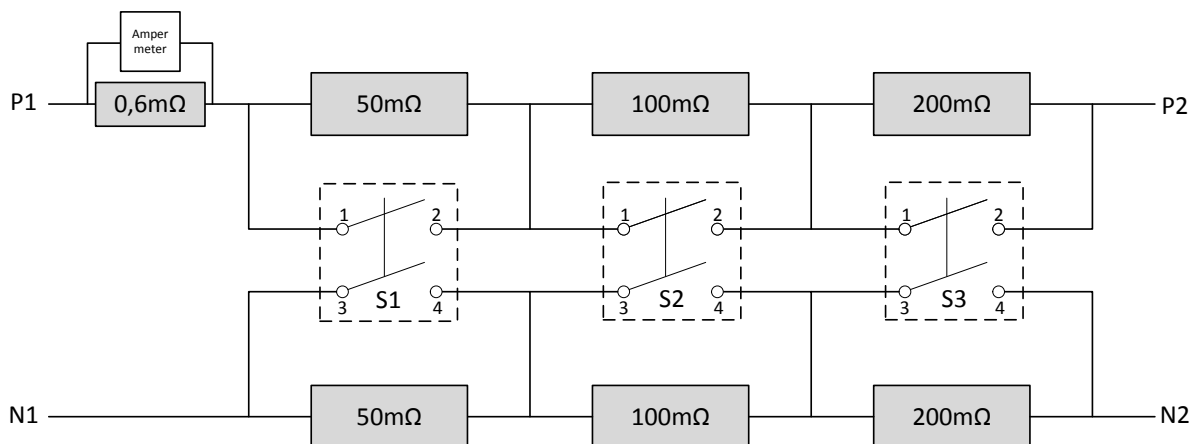
Figure 3.4: Resistive DC line model

Resistive units were ordered without casing. Casings were made so that resistor units could be mounted in standard-sized cabinet. Bypass connections in the resistor units were made using $35mm^2$ copper cables with higher insulation temperature withstand capability. This is vital for long term testing due to the significant amount of dissipated energy. Resistor banks were designed for currents up to 100A thus in full resistance (in two pole system) the power $P = 700m\Omega * (100A)^2 = 7kW$. As seen from Figure 3.5 DC resistors have no top or bottom side of casing which allows stacking multiple DC line resistors on top of each other and forcing hot air out of the roof of the cabinet. A fan was added to the bottom of the cabinet so that hot air in the cabinet could be blown out. The fan is controlled by the speed regulator [11] that uses temperature readings from the temperature sensor mounted in ceiling of the cabinet.

Figure 3.5: DC line equivalent resistor: Wiring process

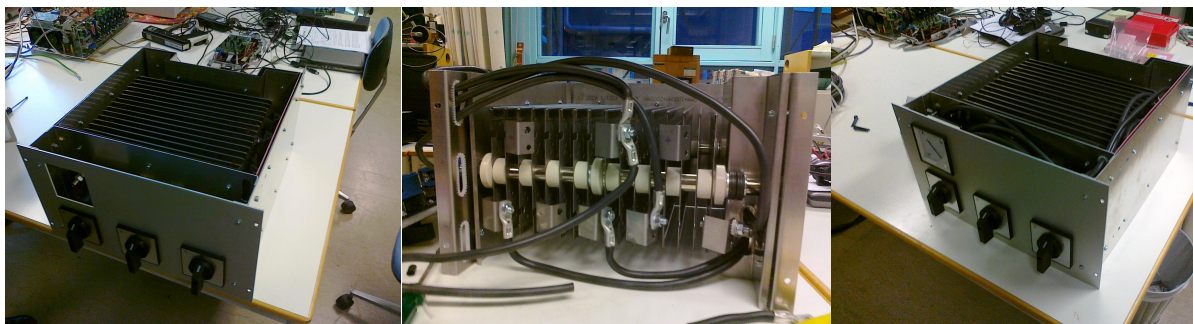In addition to the three resistor units, there are four DC busbars in the cabinet. Laboratory converters were connected in star using $35mm^2$ copper cables between converters, busbars and resistor banks. Copper cables between the converters and resistor banks add extra resistance into the DC network. In order to have as accurate assessment of the system as possible, resistances in the path between converters and DC network star point were measured. Table 3.3 illustrates the resistance in the path between converter and star-point of DC grid.

Table 3.3: Measured resistance between converter and star-point

	R_a	R_b	R_c
0 $m\Omega$ Case	92 $m\Omega$	74 $m\Omega$	50 $m\Omega$
50 $m\Omega$ Case	142 $m\Omega$	130 $m\Omega$	98 $m\Omega$
100 $m\Omega$ Case	188 $m\Omega$	172 $m\Omega$	145 $m\Omega$
150 $m\Omega$ Case	234 $m\Omega$	217 $m\Omega$	189 $m\Omega$
200 $m\Omega$ Case	281 $m\Omega$	265 $m\Omega$	237 $m\Omega$
250 $m\Omega$ Case	330 $m\Omega$	314 $m\Omega$	286 $m\Omega$
300 $m\Omega$ Case	372 $m\Omega$	356 $m\Omega$	330 $m\Omega$
350 $m\Omega$ Case	417 $m\Omega$	401 $m\Omega$	374 $m\Omega$

3.1.4 AC grid connection

Converters were connected to 230/400 V AC grid. Two VSCs were connected to the system via three-phase transformers. These transformers have equal number of windings on primary and secondary side resulting in no change in voltage. Transformer data is shown in Table 3.4.

Table 3.4: Transformer data

Transformer T1	
Power: 70kVA	Frequency: 50-60 Hz
Primary: 380V and 108A	
Secondary: 380V and 105A	
Cooling: AN	Group: YNyn0

Transformer T2	
Power: 80kVA	Frequency: 47-63 Hz
Primary: 400 and 118A	
Secondary: 400 and 115A	
Cooling: AN	Group: YNyn0

Local grid 1 and local grid 2 were connected to the laboratory supply grid via two $1mH$ inductors with rated current of 863 A. Connections between components is illustrated in Figure 3.6.
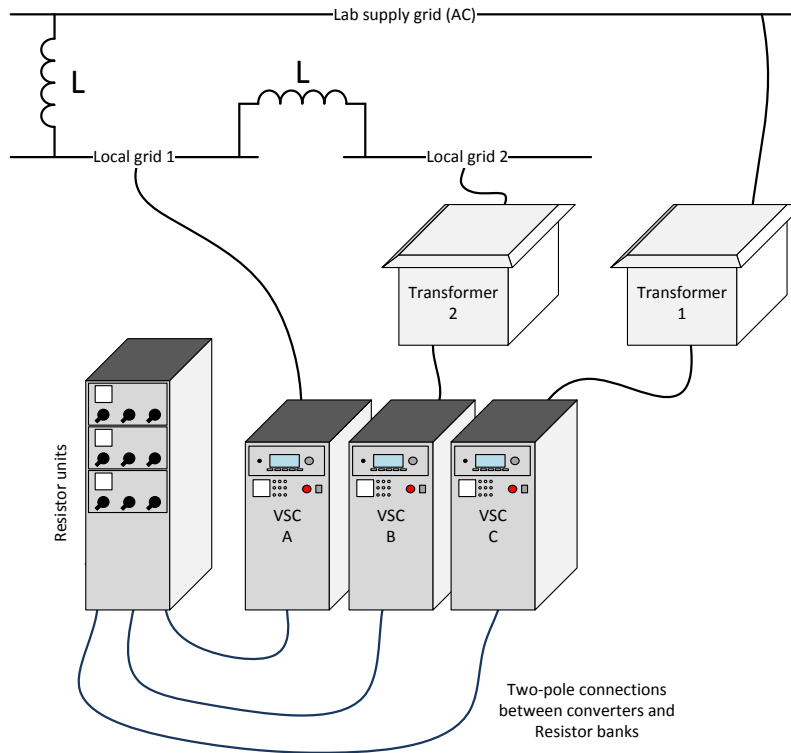

Figure 3.6: Laboratory testing set-up illustration

3.2   Control and monitoring

This section gives an overview of control system of the laboratory test system. Hardware as well as developed software is introduced here. The most relevant control theory is also presented as a part of created software.

3.2.1   Converter control system

Messages

In the previous chapter VSCs were introduced and as a part of these converters FPGA boards play important role in connecting user interface to converters' IGBTs in a specified way. As the converter itself, the FPGA is versatile and could be used in several different applications [2]. Even tough the converter could fully be controlled using the LCD display on the front panel, it is desired to remotely send desired references to the converter. Figure 3.7 illustrates how parameters and references can be inserted to the control system.
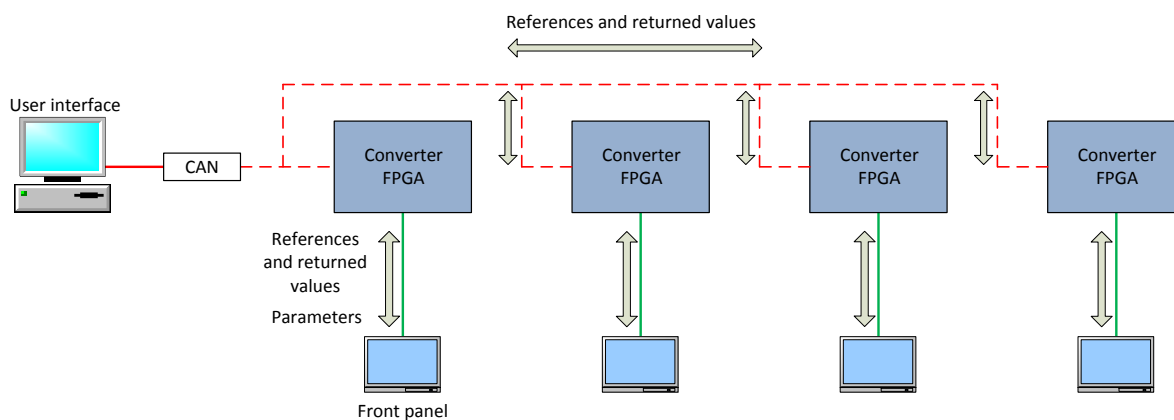
Figure 3.7: Control strategy of laboratory set-up

Parameters are can only be changed from the front panel as these measures need to be adjusted when converter is not under operation. These values represent conditions in which testing is conducted. References, on the other hand, can be sent to the system when it is under operation. These values are variables in the system and depending on which control strategy is used, they define the dynamic operation of the converter.

Table 3.5: Relevant parameters and references

Relevant parameters	Active control mode, reactive control mode, control source, Ireact/Iact ratio, Limit value coupling, rated reg current, I dq meas filt t, I reg Kp, I reg Ti, UDC reg Kp, UDC reg Ti, UDC reg droop, CAN bus enable, CAN bitrate, CAN control signal ID, CAN status signal ID, CAN message valid time, I meas, full scale, I trip level
Relevant references	Active reference, active limits, reactive limits, Converter Status, Reactive current, Active current, U DC-link, U AC RMS, PLL frequency

Table 3.5 illustrates the relevant parameters and references inserted from the front panel and sent via the CAN bus respectively. Information regarding the references is documented in [2], the purpose of each parameter is described in the LCD display menu.

Controller

Outer current controller, as an essential part of DC droop control, is discussed in the given subsection. The most typical way of implementing DC droop control is illustrated in Figure 3.8. This controller is a combination of constant voltage controller and constant power controller. i_{dref} is achieved when active power error and modified DC voltage error are added and put through PI controller. ρ represents a DC voltage droop, whereas when the value is set to 0, the controller acts as constant voltage controller. Infinitely large value of DC voltage droop results in constant power controller.
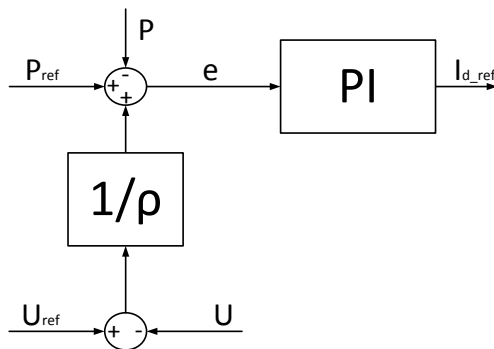

Figure 3.8: Common DC droop controller

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Laboratory outer current controller is somewhat different from the one discussed above. PI regulator is divided into proportional and integral part. Signal from the integral part is fed back to the input of PI regulator. This creates an offset in the error resulting in a droop between DC voltage and active power. In other words, the gain in the controller becomes finite. Outer current controller used in the laboratory is illustrated in Figure 3.9.
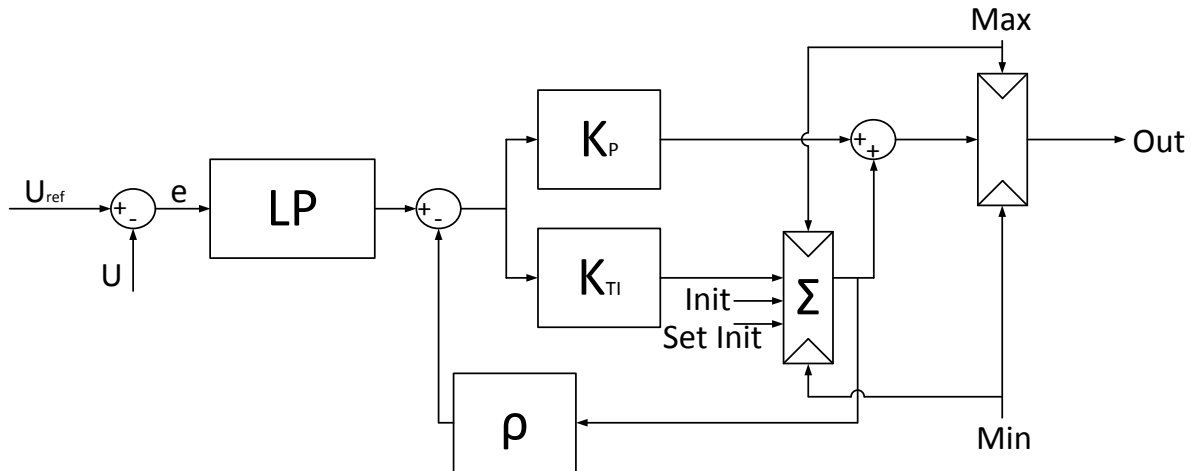

Figure 3.9: Laboratory DC droop controller [2]

3.2.2   CAN bus

CAN Bus was first introduced in the second half of 1980-s in automotive industry. Cars had become more equipped with electronic devices and thus in order to reduce the amount of wiring a communication system with less parallel lines was desired. A system as illustrated in 3.7 is an example of CAN Bus implementation. Components in the system are connected via single or dual-wired scheme and components in the network are taking turns in sending and receiving messages using CAN protocol [12]. Messages are sent and received with the certain rate and the speed of communication measures up to 1Mbit/s enabling fast connection between the modules. In addition, messages sent over the CAN Bus have ID numbers, whereas lower ID number refers to higher priority in the protocol.

The FPGA board used in this project [2] is controllable via the CAN bus. This micro-controller and FPGA device is programmed to receive and send messages to the CAN

bus interface. Each reference has its own message id code which has to be sent to the CAN bus together with the desired value. National Instruments USB-8473 device was used to interconnect PC and VSCs.
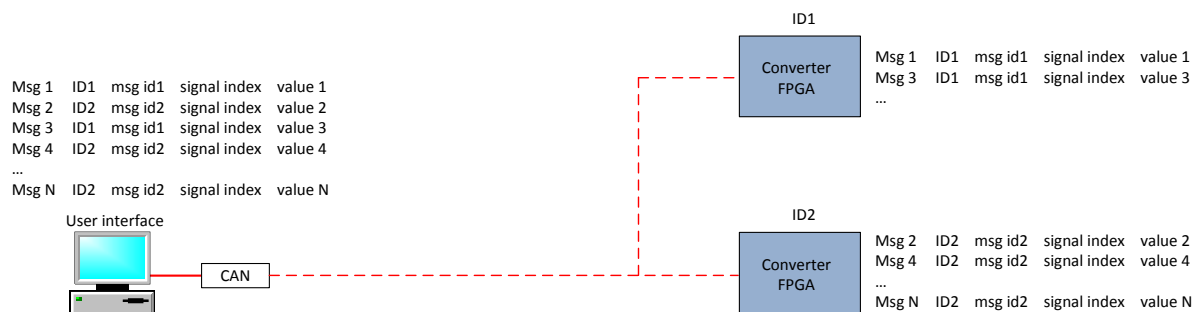

Figure 3.10: Principle of sending CAN messages to the converter

Figure 3.10 illustrates how messages from the user interface are sent to the CAN interface. Each converter only recognizes messages that have the same ID code and message ID as the FPGA board is programmed to receive. Signal index determines which reference in the FPGA board becomes overwritten with the correspondent new value.

3.2.3   LabVIEW code

National Instruments LabVIEW program was used to create an interface for sending and receiving messages to the FPGA boards. As described above, this interface had to bundle messages into 8-byte data before sending them into the CAN bus. In receiving process the program had to do vice versa, namely unbundle 8-byte messages into 8 8-bit messages. Moreover, the program had to be developed so that it would be easily adjustable for the future applications. In order to avoid long and complex codes, similar tasks were gathered into common subordinate codes (subVI-s) so that any future development of the code would be easy to new users. This section gives an overview of the developed software, whereas some proposes for future developments are brought out if further work chapter.

The starting point of developing the program was FPGA board's message protocol. In order to send correct references to the FPGA board as well as receive true values from it, it was needed to reconcile their protocol. In other words, the program had to be designed to understand messages from the board as well as send messages to the board

in an intelligible way. References to the converter are sent one by one and main part of the process is located in a WHILE loop. Figure 3.11 shows the main structure of developed code.
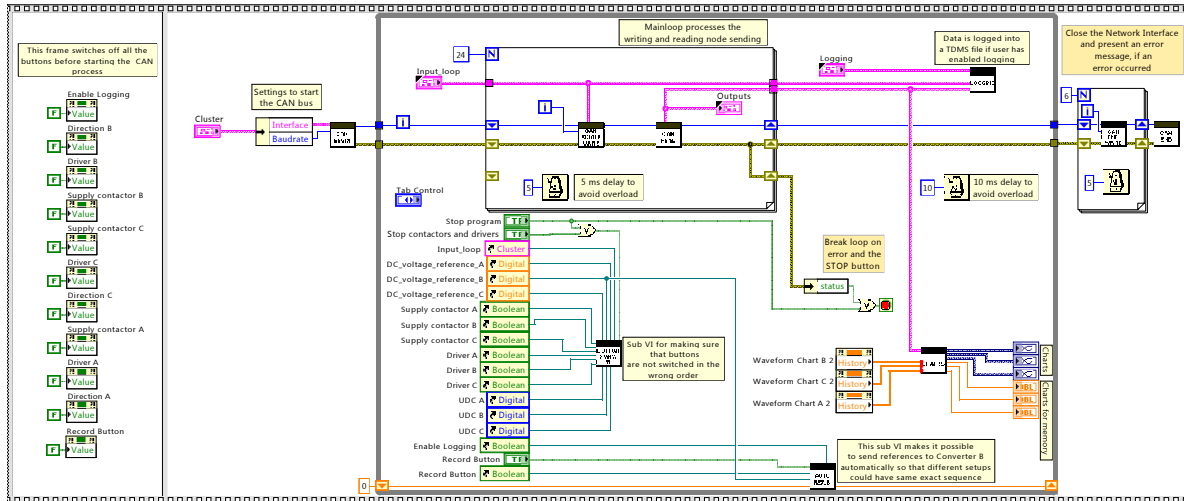

Figure 3.11: Main structure of the LabVIEW program

In addition to the WHILE loop, there is one sequence structure and two FOR loops. Sequence structure is used for enabling the right state of controls in the start-up of the program. Thus it is a part of safety functions in the program. FOR loops ensure that all the messages to the CAN bus are sent during one cycle in the WHILE loop. As stated before, there can only be one message on the CAN bus at the time. Therefore the number of iterations in the FOR loop is determined by how many references need to be sent to converter units. For complex control and bulky test systems, this part of the program could potentially become a bottleneck as some references need to be adjusted more often than possible with the current set-up. However, if there are only few time-critical references, then sending the critical-reference multiple times during one WHILE loop would decrease the severity of the problem.

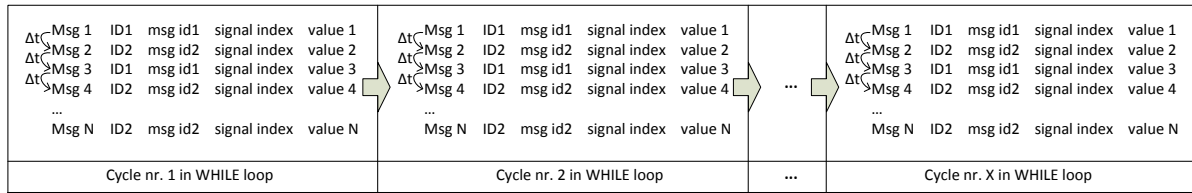|	Msg 1	ID1	msg id1	signal index	value 1		Msg 1	ID1	msg id1	signal index	value 1			Msg 1	ID1	msg id1	signal index	value 1

Figure 3.12: Message sending order and time delay in the program

Figure 3.12 illustrates the sequence of the messages sent to the CAN bus. When the number of messages (N) gets too high, then there is a possibility that $N * \Delta t$ becomes greater than the critical time for some of the parameters in the system. In a complex system, where some references are critical for controlling the operation, these cumulative delays could result in system loosing its stability.

User interface for the LabVIEW program is illustrated in Figure C.1. The program was designed to control the active reference (in this case DC voltage reference) of three different VSCs via the CAN bus. On the upper-left corner of Figure C.1 general controls were designed. Determining CAN interface and message sending rate (baudrate) are first steps of defining the operation of the software. Message sending rate, for example, has to be synchronized between the program and the FPGA board by simply assigning similar values to the two.

Input information on the user interface was divided into clusters for better organization of reference signals in the program code. This avoided having multiple parallel lines between the segments (SubVI-s) of the main structure illustrated in Figure C.2.

CAN BEGIN

CAN Begin SubVI is designed to open and configure CAN interface before any transmission of data is initialised. Figure C.3 illustrates the blocks used in this SubVI. CAN interface is named and primary settings are assigned. Blue blocks in this (CConfig and COpen) and following SubVI-s are predefined in National Instruments LabVIEW CAN package.

CAN SINGLE WRITE

Figure C.4 illustrates the CAN Single Write SubVI. This is the most fundamental part of the program as values for the references and identification codes for the desired measurements are sent to the FPGA board via the CAN bus. Identification code of the converter, message id, signal index and two status id-s of each CAN message are inserted in the blue array on the left. Last column of the array is left empty and becomes overwritten with the values from the input cluster as FOR loop iterations renew each of the value once in the outer WHILE loop. 24 Different rows in the array ensure that all the relevant values for this particular application become sent to the FPGA boards. Thus FOR loop needs to have 24 iterations as one iteration uses one row from the table at the time.

The number of needed sending messages for each converter is 6 resulting in 18 messages in total (three converters). The total number of desired measurements from the converter is 9. Two status messages can be acquired in one CAN message whereas one of them is always used receiving the status bitfield state.

Table 3.6: Messages sent and measurements received

Message Direction In CAN	Message/Measurement
TO CONVERTER	00 - command bit field, 01 - active reference, 04 - positive active limit, 05 - negative active limit, 06 - positive reactive limit, 07 - negative reactive limit
FROM CONVERTER	0 - Converter Status, 1 - status bitfield, 9 - Reactive current, 10 - Active current, 11 - RMS current, 13 - U DC-link, 15 - U AC RMS, 17 - PLL Frequency, 18 - PLL arctan angle

Other 8 measurements from the converter have to share the second slot (4th column in the array). Thus the length of one WHILE loop is 24 FOR loop iterations. Table 3.6 illustrates the messages and measurements used in the program. Signal indexes for each message/measurement are included in the table.

All the data from each row is combined into single message according to the FPGA protocol. Checksum is performed ensuring that any irrelevant data will not get sent to the CAN bus (CWrite).

CAN READ

This SubVI is designed to receive the values from the converter (CRead). The program has to read the message from the CAN bus and identify which value is sent using the FPGA board protocol. Outer case structure is used to distinguish between converters while inner case structure identifies and routes each value for the converter. "Unbundle by Name" and "Bundle by Name" elements together with feedback nodes are used ensuring that all the values from other cases are being preserved while new messages enter the user interface.

CAN END

After stop message from the user, the program exits the main WHILE loop and CAN bus has to be closed (CClose). Messages from the program are no longer recognized and sent to the CAN bus.

OTHER

Rest of the SubVI-s in the program are designed to protect the converters from undesired sequences as well as make using the program more convenient. Needed information is logged into an external file for further processing. All the SubVI-s are illustrated in Appendix C.

3.3 Laboratory test results

3.3.1 General

In order to have comparable test results, a specified sequence of sending messages was created. Active reference (DC voltage reference) for converter B was changed after every 5 seconds, while references in converter A and C were kept constant. Table 3.7 illustrates the steps used in majority of tests. Having sequences, however, does not attempt to show dynamic behaviour of the system, but instead illustrates the difference between cases when parameters are adjusted.

Table 3.7: Active reference sequence in testing: Sequence S1

	0 s	5 s	10 s	15 s	20 s	25 s	30 s	35 s	40 s	45 s	50 s	55 s	60 s
Converter B	600	610	620	630	640	620	600	590	580	570	560	580	600
Converter A	600	600	600	600	600	600	600	600	600	600	600	600	600
Converter C	600	600	600	600	600	600	600	600	600	600	600	600	600

3.3.2 Results and comparison

Comparable lower resistance and droop constant of 6%

DC network with comparable resistance in the lines was tested. Comparable resistance implies that values on the resistor banks is set to equal. As discussed before, there is asymmetry in paths between converters and star point of the DC network. Values illustrated from Table 3.3 are used to compute expected power flow in the DC network.

All the following tables and figures include measured resistances, DC droop constants and references for each of the converter in the three-terminal star-connected DC network. In addition, tables show results from laboratory tests at the time instance t=12.5s, that is when $U_{b,ref} = 620V$.

DC droop constants were set to 6 % for all three VSCs. Resistances are indicated in the tables and figures below. Results at time instance $t = 12.5s$ are illustrated in Table 3.8. Full test is shown in Figure 3.13.

Table 3.8: Comparable lower resistance test

$\rho_a = 6\%$	$R_a = 284m\Omega$			
$\rho_b = 6\%$	$R_b = 260m\Omega$		RESULTS at t=12.5s	
$\rho_c = 6\%$	$R_c = 196m\Omega$		Laboratory	Power flow
Converter A	$P_{a,ref} = 0kW$	Power	6.13 kW	6.04 kW
	$U_{a,ref} = 600V$	Voltage	602.8 V	603.6 V
Converter B	$P_{b,ref} = 0kW$	Power	-15.5 kW	-13.2 kW
	$U_{b,ref} = 620V$	Voltage	608.7 V	612.1 V
Converter C	$P_{c,ref} = 0kW$	Power	8.96 kW	6.99 kW
	$U_{c,ref} = 600V$	Voltage	604.8 V	604.2 V

There is 10-20 % difference between calculated and tested power contributions. DC-link voltages are very similar to the expected ones, expect converter B DC-link voltage, which differs from the expected value by 3.4 volts.
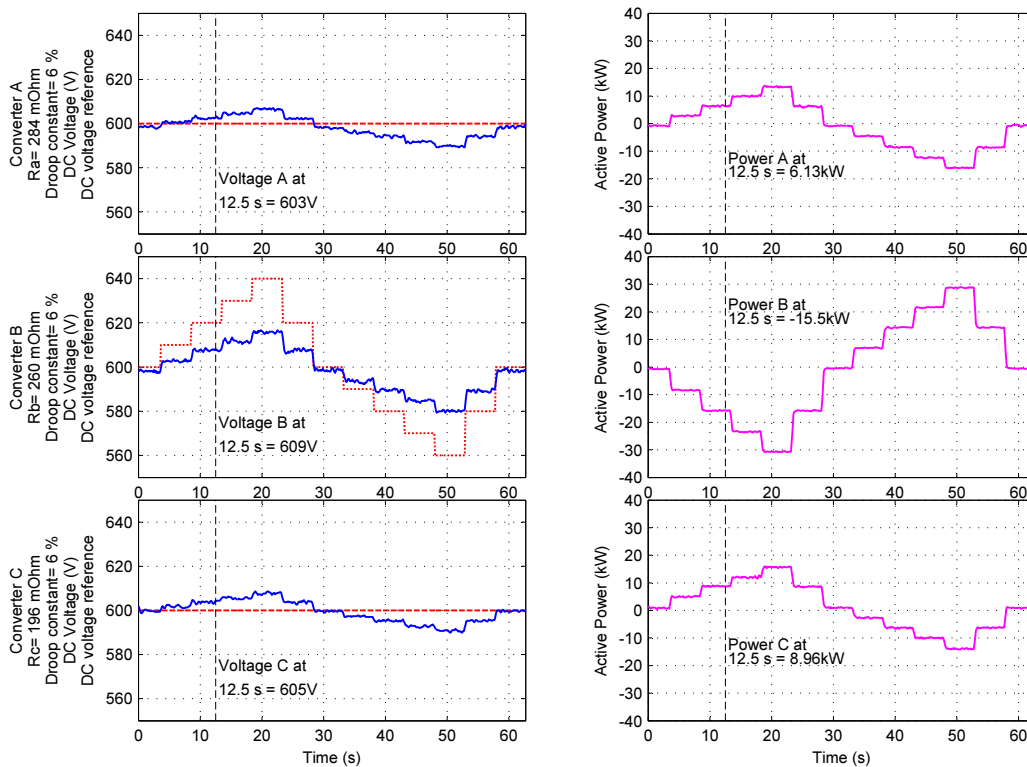

Figure 3.13: Comparable lower resistance and equal DC droop constant of 6%

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It is clearly observed that the relation between DC voltage and power flow is linear over the different points in the test, converter A and C share the consumption unequally. This is due to unequal resistances in converter A path and converter C path.

Comparable higher resistance and droop constant of 6%

Another test with equal 6 % DC voltage droop was conducted. This time, DC line resistances were set to higher values than these of the previous test. Again, it was attempted to have as equal line resistance in the DC lines as possible. Still some disparity in the resistances remained. Table 3.9 and Figure 3.14 illustrate the results.

Table 3.9: Comparable higher resistance test

$\rho_a = 6\%$	$R_a = 562m\Omega$			
$\rho_b = 6\%$	$R_b = 530m\Omega$		RESULTS at t=12.5s	
$\rho_c = 6\%$	$R_c = 474m\Omega$		Laboratory	Power flow
Converter A	$P_{a,ref} = 0kW$	Power	4.25 kW	4.28 kW
	$U_{a,ref} = 600V$	Voltage	601.2 V	602.6 V
Converter B	$P_{b,ref} = 0kW$	Power	-10.7 kW	-9.19 kW
	$U_{b,ref} = 620V$	Voltage	612.3 V	614.5 V
Converter C	$P_{c,ref} = 0kW$	Power	4.72 kW	4.73 kW
	$U_{c,ref} = 600V$	Voltage	601.8 V	602.8 V

This time the difference between analytical and laboratory values was somewhat less, resulting in less discrepancy in active powers. Furthermore, the difference in DC-link voltages were not as high as during the test before. As expected, Converter A consumed less power than Converter C.

When comparing the second test with the one above, it can be observed that power flow is somewhat smaller. This was also expected since additional resistance in the DC line affects the admittance matrix (and thus active power flow equations) in negative way:

$$P_i \downarrow = U_i(U_1 Y_{i1} \downarrow + U_2 Y_{i2} \downarrow + U_3 Y_{i3} \downarrow) \tag{3.1}$$
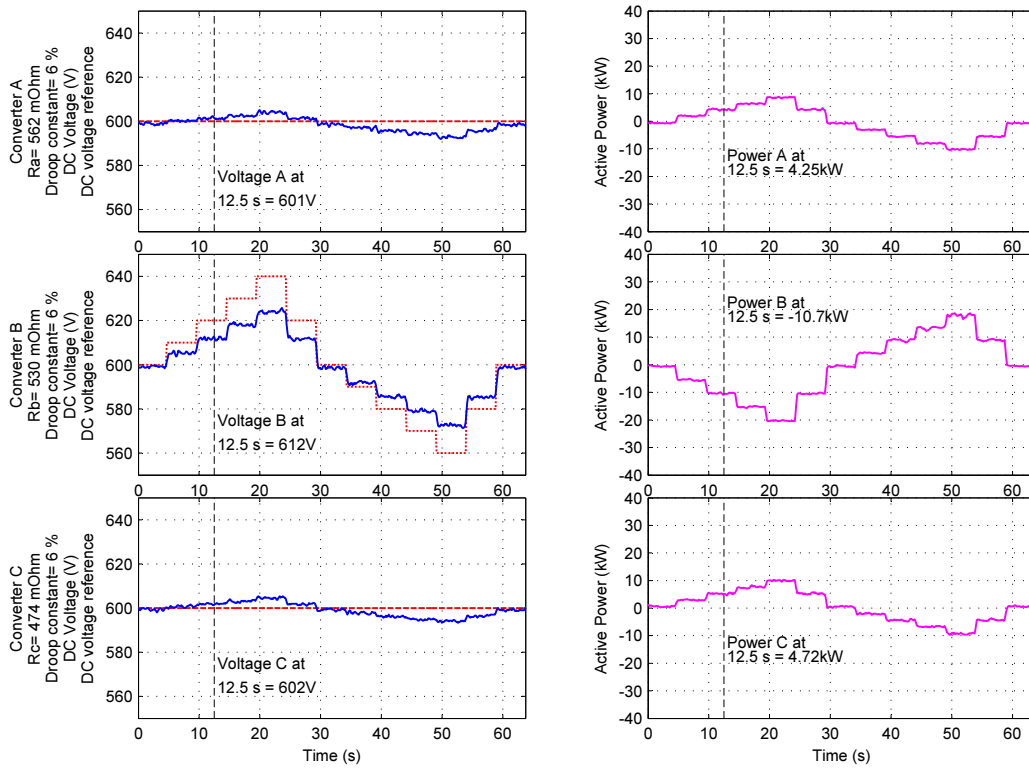
Figure 3.14: Comparable higher resistance and equal DC droop constant of 6%

Comparable higher resistance and droop constant of 10%

Table 3.10 and Figure 3.15 illustrate analogous test to the one above with higher values of DC voltage droop constants. Higher values of ρ_a, ρ_b and ρ_c were expected to decrease the power flow even further compared to the previous test. DC voltage droop constant, which stands for the voltage change in percentage resulting active power change of 1 pu, was increased from 6 % to 10 %. Resistances were kept the same exact values to the ones above.

$$\Delta P_i^{pu} \downarrow = -\frac{1}{\rho_i \uparrow}(U_i^{pu} - U_{i,ref}^{pu}) \tag{3.2}$$

30

Table 3.10: Comparable higher resistance test (higher droop constant)

$\rho_a = 10\%$	$R_a = 562m\Omega$			
$\rho_b = 10\%$	$R_b = 530m\Omega$		RESULTS at t=12.5s	
$\rho_c = 10\%$	$R_c = 474m\Omega$		Laboratory	Power flow
Converter A	$P_{a,ref} = 0kW$	Power	2.92 kW	3.41 kW
	$U_{a,ref} = 600V$	Voltage	602 V	603.4 V
Converter B	$P_{b,ref} = 0kW$	Power	-8.04 kW	-7.2 kW
	$U_{b,ref} = 620V$	Voltage	610.2 V	612.8 V
Converter C	$P_{c,ref} = 0kW$	Power	3.51 kW	3.68 kW
	$U_{c,ref} = 600V$	Voltage	602.8 V	603.7 V

Results at the time instance t=12.5s confirm the theory showing significant decrease in active power measurements. For instance, power injection by converter B decreased from 10.7 kW to 8.04 kW.
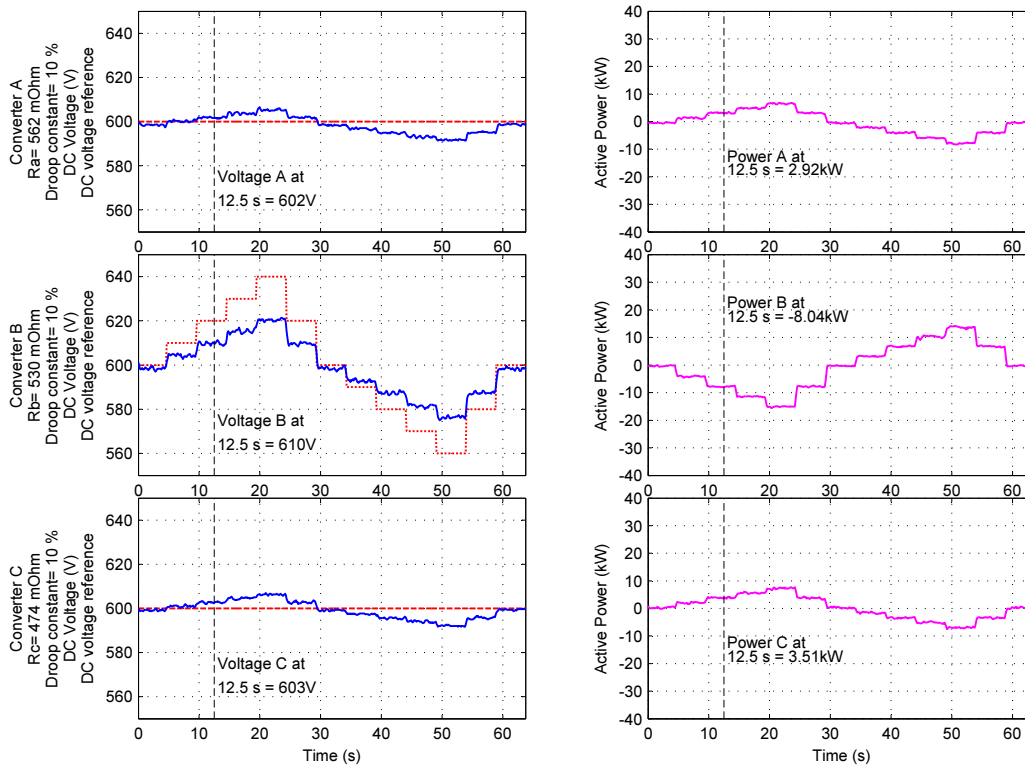
Figure 3.15: Comparable higher resistance and equal DC droop constant of 10%

Again, active power measurements were relatively close to expected values. Power consumption via converter A was slightly less than via converter C. This was expected, because less resistance in converter C DC line, results in higher power measurement in that point. Small values are more prone to any measurement offset errors. A possible measurement offset or an offset in sending active reference could be the cause of the error.

Variable resistance and droop constant of 6%

In the following test, illustrated in Table 3.11 and Figure 3.16, DC line resistances were set to unequal values. Again, values from the admittance matrix help to understand which of the consuming converters is expected to take larger share in the power flow.

Table 3.11: Variable resistance test

$\rho_a = 6\%$	$R_a = 376m\Omega$			
$\rho_b = 6\%$	$R_b = 530m\Omega$			RESULTS at t=12.5s
$\rho_c = 6\%$	$R_c = 660m\Omega$		Laboratory	Power flow
Converter A	$P_{a,ref} = 0kW$	Power	5.76 kW	5.28 kW
	$U_{a,ref} = 600V$	Voltage	601.2 V	603.2 V
Converter B	$P_{b,ref} = 0kW$	Power	-10.6 kW	-9.26 kW
	$U_{b,ref} = 620V$	Voltage	611.7 V	614.4 V
Converter C	$P_{c,ref} = 0kW$	Power	4.18 kW	3.81 kW
	$U_{c,ref} = 600V$	Voltage	601.2 V	602.3 V

Table above shows that according to the analytical model, the power consumption in converter A should be slightly larger than that of converter C. Test results confirm that active power consumption in converter C is indeed larger. DC voltages are also close to the expected values.

Reasoning for why the difference in the measured and analytical values exists, can be found by investigating multiple errors in the system. First, even taking into account that resistor banks were measured in Section 3.1.3, there is still some uncertainty on the real values of the DC resistance due to internal resistance of Converter. Each connection can have slightly different condition, resulting in variance in the resistance. Moreover, cables shorting the three resistor units in one resistor bank are not equal in length, resulting in small offset. Further discussion on the inaccuracy in the resistance is given in the conclusion.
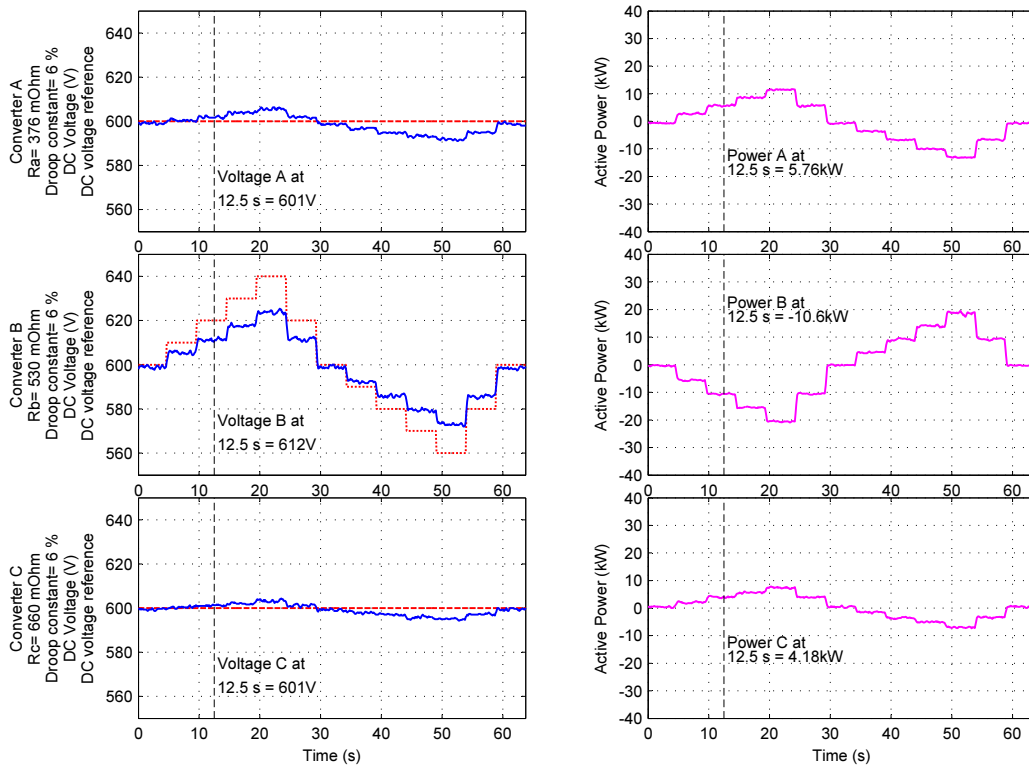
Figure 3.16: Unequal resistance and equal DC droop constant of 6%

Comparable resistance, droop constants of 6%, 10% **and** 14%

Unequal but comparable resistance test with different DC droop constants is illustrated in Figure 3.17. Similarly to the tests above, Table 3.12 shows the values of voltages and active powers at time instance t=12.5s. Again, relying on the Equation 3.2, it was expected that power consumption via converter C would be less than that of converter A. Laboratory test meets the expectations as can be observed in the table below.

Laboratory test results are again relatively close to analytical power flow. As mentioned earlier, results with relatively low values are more prone to measurement errors. This configuration of test set-up results in relatively low power flow, thus the error in the measurement has greater share in the total value. Nevertheless the test can be considered as a success in proving the theory.
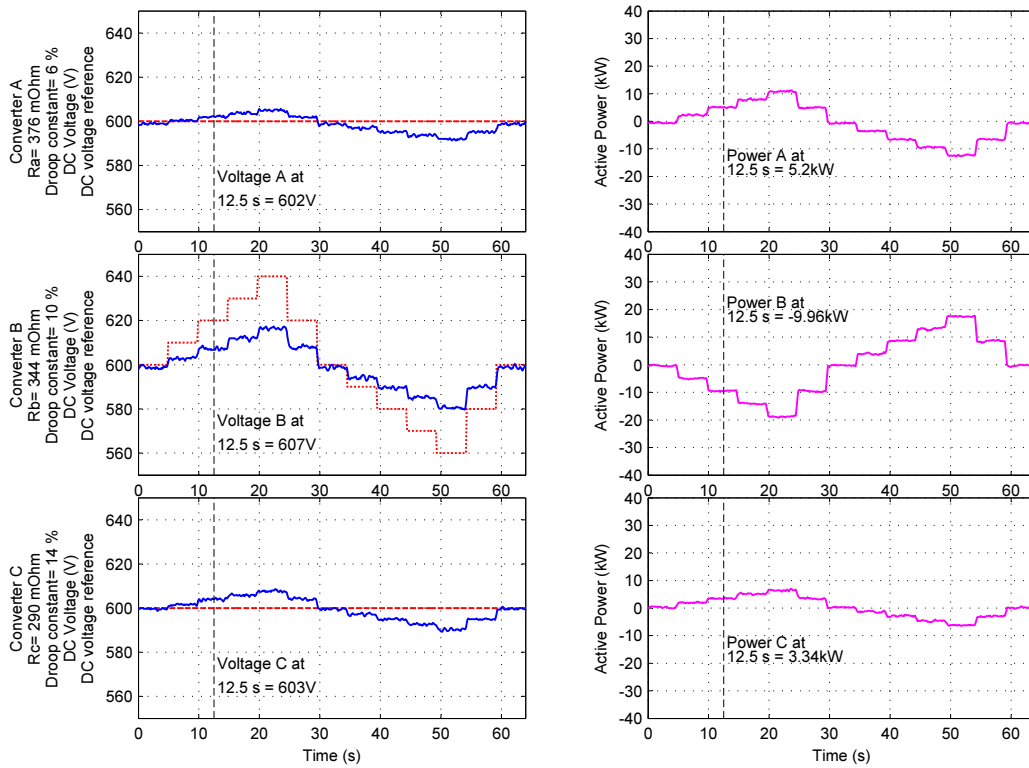
Figure 3.17: Unequal resistance and unequal DC droop constant of 6%, 10% and 14%

Table 3.12: Unequal resistance and different DC droop constants

$\rho_a = 6\%$	$R_a = 376m\Omega$			
$\rho_b = 10\%$	$R_b = 344m\Omega$		RESULTS at t=12.5s	
$\rho_c = 14\%$	$R_c = 290m\Omega$		Laboratory	Power flow
Converter A	$P_{a,ref} = 0kW$	Power	5.2 kW	5.21 kW
	$U_{a,ref} = 600V$	Voltage	602 V	603.1 V
Converter B	$P_{b,ref} = 0kW$	Power	-9.96 kW	-8.72 kW
	$U_{b,ref} = 620V$	Voltage	607 V	611.3 V
Converter C	$P_{c,ref} = 0kW$	Power	3.34 kW	3.39 kW
	$U_{c,ref} = 600V$	Voltage	603.2 V	604.8 V

3.3.3   Summary

All the 5 cases discussed above were relatively close to the expected values. Analytical and tested results differ from each other due to several reasons. First, resistances in the DC line models, that is along the path between the VSC terminals, were not determined accurately. DC resistor banks consist of three resistor units, which are shorted via DPST switches. Cables used to connect resistor units with switches are not equal in length.

There is a great deal of measurement error involved, whereas noise in the measurement is not proportional to measured value. By studying the raw data from the log file, it was observed that regardless of the magnitude of active power measurement, the fluctuations are up to 1 kW. This means that tests with smaller power flow are more prone to these errors.

Active power was obtained on the AC side of the converters using I_q and $U_{AC,RMS}$. This means that converter losses are included in the laboratory test results. Losses in the laboratory VSCs are in the range of 2-5 % meaning that actual DC power flow was actually closer to the expected values.

4 DC breakers

In the second part of the report, work towards dynamic testing is begun. DC breakers for laboratory use were studied and attempt of creating one for testing purposes is reported.

Breaking DC circuits presents multiple challenges to the design of high voltage DC circuit breakers (DCCB). Mature and cost-effective technology of DCCB is not available due to too little interest from the industry over the last decade [13]. In the last few decades, the subject has been investigated to some degree, but with the lack of wide market for the product, it has simply not been profitable enough for manufacturers to make large-scale investments for developing the product. Recently, however, the interest in DCCBs has increased and several improvements concerning technological challenges have been made. Existing high voltage solutions are considered too expensive with regards to high building costs as well as relatively large operational costs caused by the losses.

This chapter will give an overview of the challenges in the current technology and presents an attempt to create a robust DC breaker for the laboratory setup. Conclusions on the work and ideas for further improvement will be addressed at the end of the chapter.

4.1 State of technology and challenges in HVDC breakers

AC breaker principle uses natural zero-crossing of the current waveform to interrupt circuit. An insulating medium is designed to guarantee that electric arc between contacts does not reignite after the zero-crossing. Since there is no natural zero-crossing in DC current, a need for bringing down the current to zero is achieved by other means which will be described below.

Requirements for a DC switch vary greatly depending on which of the HVDC technologies is used. CSC technology presents fewer challenges to interrupting DC current due to less capacitance on the DC side of the converter. VSC technology, on the other hand, relies

hugely on high capacitance on the DC side meaning that in a case of a fault a lot of the energy stored in the capacitance has to be dissipated in the circuit breaker. This leads to higher currents and smaller time constants making speed and efficiency of the breaker even more vital.

Resonant DC breakers

Resonant circuit breakers are using series R and L in parallel with normal AC circuit breaker for creating an oscillation for an artificial zero crossing. These two components in series will cause natural oscillation resulting in arc extinguishing when the amplitude of oscillation becomes large enough. Depending on whether the capacitor is precharged or not, these breakers can be classified into two types, namely passive and active resonant DC breakers. In the case of active mode, another switch has to be added to the commutation path of the DC breaker preventing discharging of the capacitor.
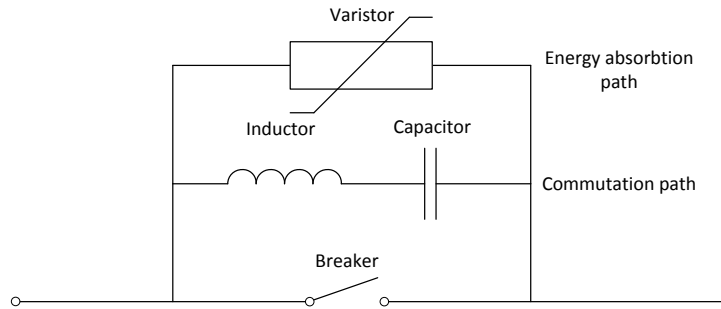
Figure 4.1: Resonant DC breaker

There can be a significant amount of energy stored in the system and for successful interruption this energy has to be absorbed. Another parallel path is included into the design of DCCB with non-linear resistive element purposed become much more conductive when higher voltages are applied, much like diodes. These elements are called varistors or voltage dependent resistors (VDR) and their task is to protect the equipment they are in parallel with.

When the arc in the main switch is being extinguished, the current starts to flow into the capacitor resulting in high voltage over the element. Varistor therefore senses the voltage and at specified point becomes more conductive. Voltage rise is stopped by the varistor bank taking most of the current in the circuit and after absorbing the energy

in the system, the voltage lowers once again resulting in the rise of the resistance in the varistor [13]. Figure 4.1 illustrates a passive resonant DC breaker with absorbtion and commutation paths.

Available ratings of the technology reach up to 4kA in current at 500kVA with the interruption time of 40 to 80 ms [14]. Thus the current and interruption time ratings are not practically suitable for multi-terminal HVDC systems where fault currents have higher ratings over the shorter periods of time. The limitation in the design is set by arc chamber properties of AC breakers.

Solid-state DC breakers

Solid-state DC breakers consist essentially of two components, a semiconductor device and a varistor bank. Semiconductor switches include a number of power electronic switches, such as IGBTs or silicon controlled rectifiers (SCRs). Semiconductor devices are easily controllable and perform well in interrupting DC circuits. Varistor in the solid-state DC breaker acts much the same as that of the previously discussed resonant DC breaker. It protects the semiconductor device by limiting the voltage over the semiconductor device and dissipates the excessive energy.

High on-state conduction losses are the main drawback of the technology. Losses in the semiconductors are considerably larger than in a conventional AC breaker. The development of silicon carbide (SiC) could diminish this problem resulting in smaller losses in power electronic switch. Smaller losses are result of silicon carbides higher electric field tolerance leading to thinner layers and smaller resistance [15]. Another disadvantage of the technology is the price of semiconductor devices resulting in high installation costs in addition to the costly operation.
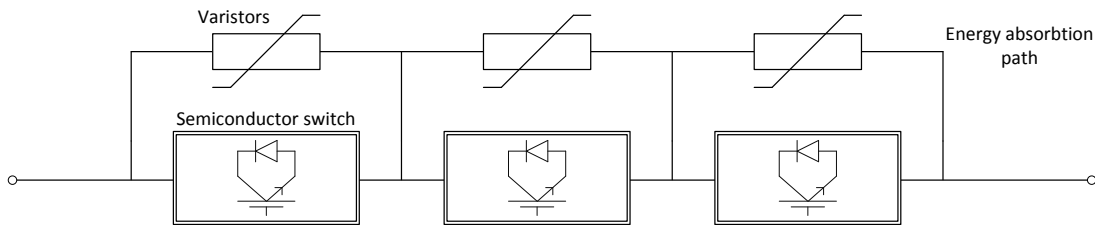

Figure 4.2: Solid-state DC braker

Hybrid DC breakers

Recent developments in DC breaker designing have led to hybrid solution of mechanical and solid-state breakers [16]. Hybrid DC breaker consists of solid-state DC breaker as described in the previous section. In addition to the normal solid-state path, low-conduction path is included. Low-conduction path consists of fast disconnector and small solid-state switch [17].

When a fault occurs, the solid-state switch on the low-conduction path turns off and fault current is rerouted to the main path. Fast switch on the low-conduction path then opens and fault clearance on the main path can begin. Varistor banks make sure that voltage over each segment of the main path does not exceed the breakdown value of the power electronic switches. Inductive energy is dissipated and current will be interrupted. After that, another mechanical switch opens to protect varistor banks from thermal overload [17]. Figure 4.3 illustrates the DC breaker discussed above.
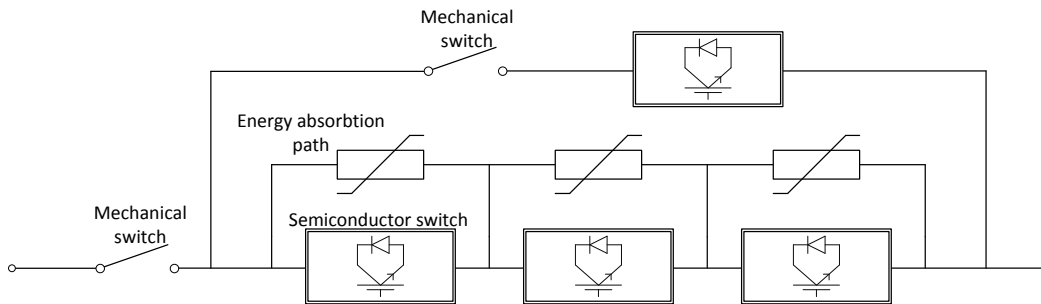
Figure 4.3: Concept of ABB's DC breaker

4.2 Developing a DC breaker

A description of an attempt to develop a DC breaker for laboratory use is described in this chapter. Test breakers are set up and tested whereas conclusions and areas of improvement are stated at the end of each testing. Future developments are discussed at the end of the section.

First series of tests

The first test breaker was built up as a resonant DC breaker. Aim for the DC breaker was set to being able to interrupt 100 A at 800 V. Testing circuit for the DC breaker is illustrated in Figure 4.4. It consists of power supply, DC-DC converter, series inductor and oscilloscope. The power of the testing was intended to increase gradually, thus having power supply at 30 V was considered to be sufficient.
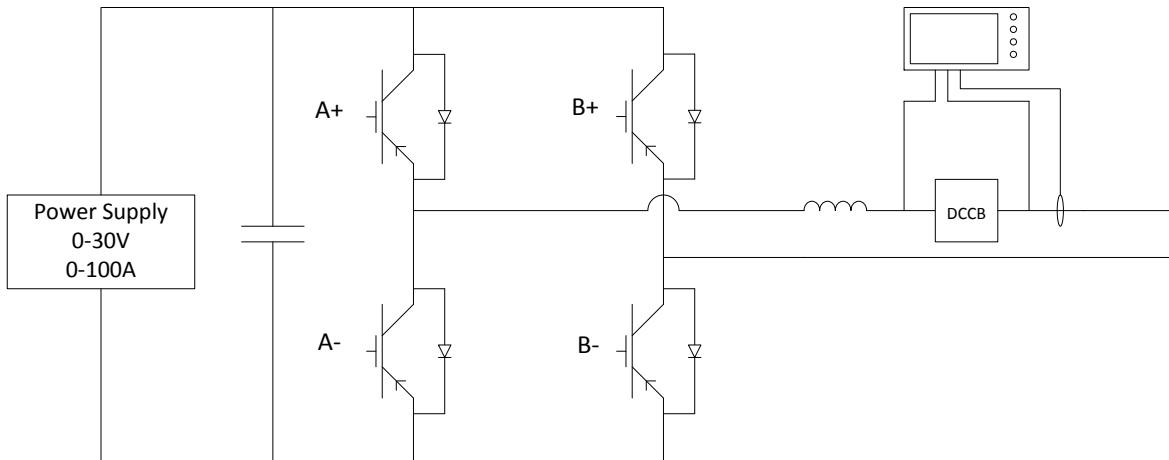

Figure 4.4: First test setup

The purpose of the DC-DC converter in the test setup was to ensure interruption in case test subject failed. In this setup the converter acts much like solid-state DC breaker. Series inductance is added to act as a DC line inductance during the fault. A relay with the time delay is added to the test setup so that after 70ms the IGBTs would become blocked regardless whether the test DC breaker has interrupted or not.

The values for the tests are indicative. The purpose of the three tests is to realize the severity of challenges in the design of DC breaker. As mentioned above, the first set of tests is conducted with the use of low voltage power supply. This power supply is able to provide 100 A at 30 V as seen on Figure 4.4.

First setup for the test DC breaker is shown in Figure 4.5. A regular 3-phase ACCB is used as a main switch, whereas only one of the chambers is being used. Connections between chambers are make further testing setups in mind. It is possible to connect all the three chambers in series and analyse if it benefits the performance of the DC breaker.
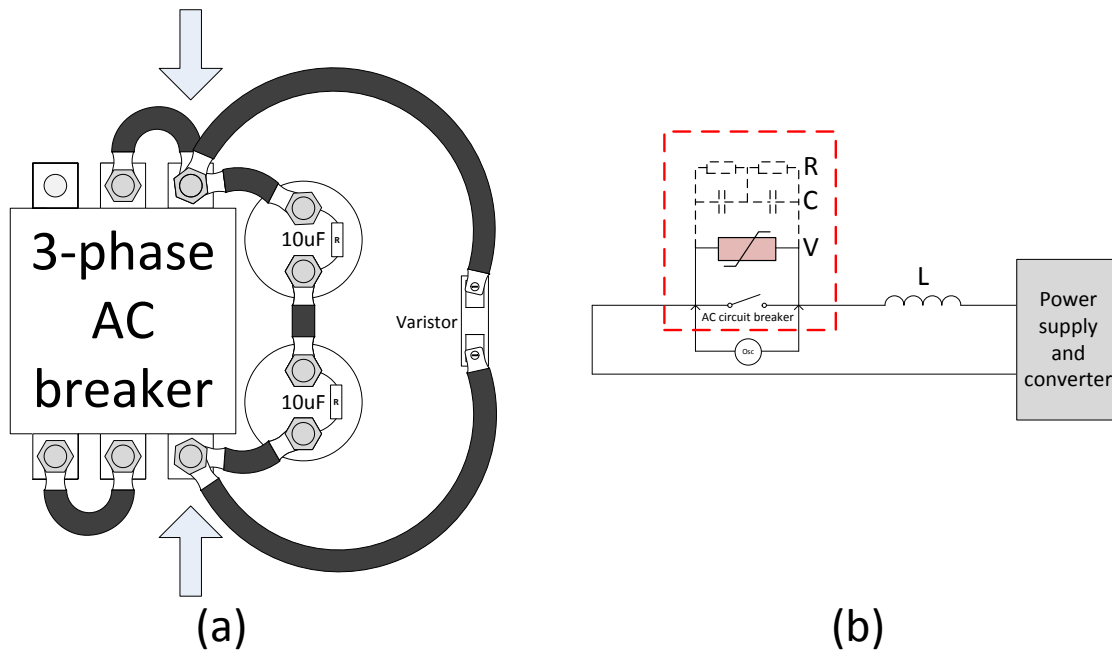
Figure 4.5: First test DC breaker

Figure 4.5 (a) shows the physical layout for the first test DCCB. It consists of ACCB, two capacitors, parallel resistors and a varistor. The two capacitors were equipped with parallel high ohmic resistors so that the person reconfiguring the breaker would be protected against any charge stored in the capacitors.

For higher voltage ratings and thus higher potential overvoltage, circuit breakers need to be equipped with varistors to clamp the voltage by dissipating the inductive energy as discussed in the previous chapters. As seen in Figure 4.5 (a) and (b) varistor is placed in parallel with other components. Since the testing voltage was only 30, then the effect of varistor was not registered in the first series of testing. Connections were manufactured using copper cables with cross sectional area of $35mm^2$ and respective cable shoes. The ACCB was connected with a remote push button enabling safer switching operation. An image of the test setup is illustrated in Figure A.5.

Figure 4.6 illustrates the curves of current and voltage over the contacts of the test DC breaker, that is over the contacts of ACCB in the setup. Reference case has only ACCB to see whether the naked breaker is able to interrupt the current. ACCB contacts are opened at 0 and voltage takes two steps. The two steps are caused by the design of the

ACCB contacts consisting of more than contactor inside the chamber.
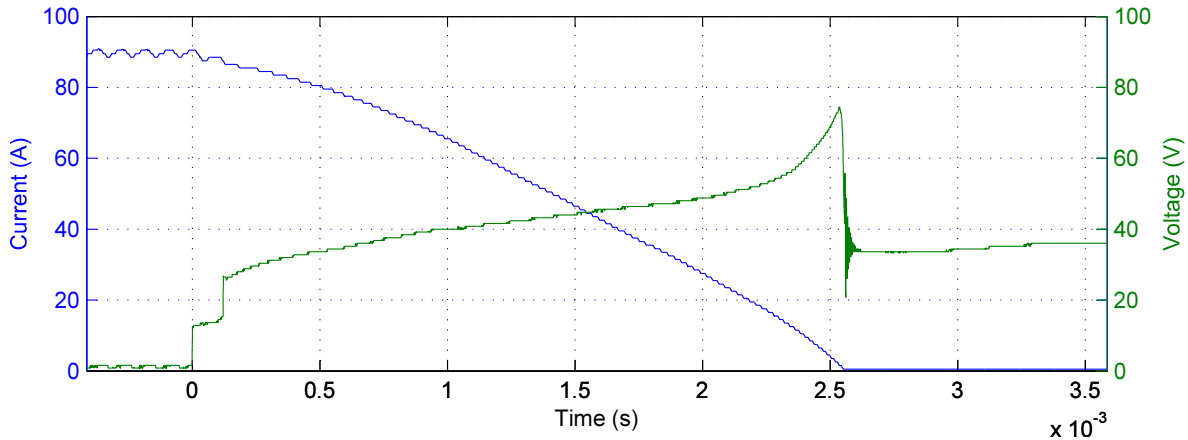
Figure 4.6: First series of tests: interrupting 90 amperes at 35 volts (no capacitor)

After the physical disconnection, the arc is formed and voltage over the contacts rises until the arc is being extinguished and current becomes zero. Subsequently the voltage across the contacts becomes equal to the source voltage (35 V). It takes about 2.5 ms for current to decline to zero, thus interruption of relatively high current at low voltages is manageable with ACCB. Same test results with lower currents are illustrated in Figure B.1 and Figure B.2.

It can be observed that voltage peak of the 90 A testing was lower and interruption time longer than for the other two tests. This is most likely caused by the design of the ACCB. In case of higher currents, the arc is pushed away from the contacts, resulting in better extinguishing conditions.

More severe oscillations were registered when capacitors were added to the configuration. The energy stored in the capacitors prior the interruption became to flow between capacitor and inductance until all of it was dissipated in the resistance. Rogowski coil was included for measuring the current entering the ACCB contacts. Rogowski coil measures the current flowing from capacitor into the arc. Line current, on the other hand, does not include the fast oscillations between the arc and parallel part of the breaker. Position of the coil is marked with red in Figure 4.7.
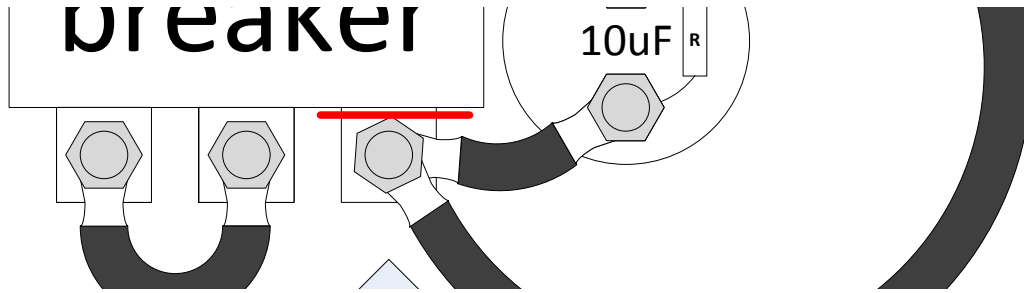
Figure 4.7: Position of Rogowski coil

Figure 4.8 illustrates current and voltage waveforms when capacitors were connected to the setup. Current being ahead of voltage waveform 90 degrees, indicates the capacitive nature of interruption. Oscillation is being damped out when energy in the capacitor becomes dissipated in the resistance in the current path.
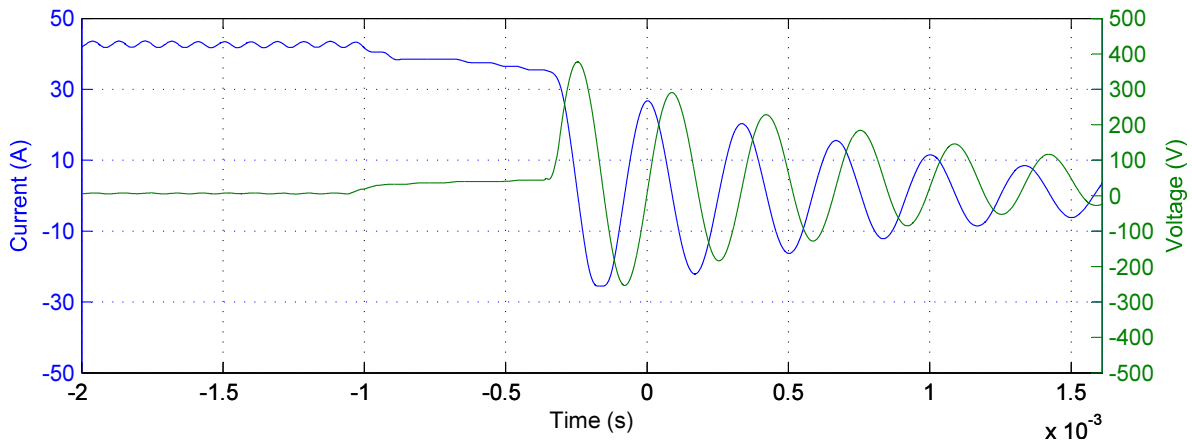

Figure 4.8: First series of tests: interrupting 41 amperes at 35 volts (capacitor included)

Additional coil illustrated in Figure 4.7 allows to decide whether current in the breaker has been interrupted or not. Figure 4.9 and Figure B.3 illustrate the current into the ACCB and shows that the arc in the main path does not reignite after being interrupted. Current spike, however, illustrates why it is desired to have an inductor in series with the capacitance. Inductance in the would limit the inrush current from the capacitor. Large inrush current can potentially become fatal to the capacitor.
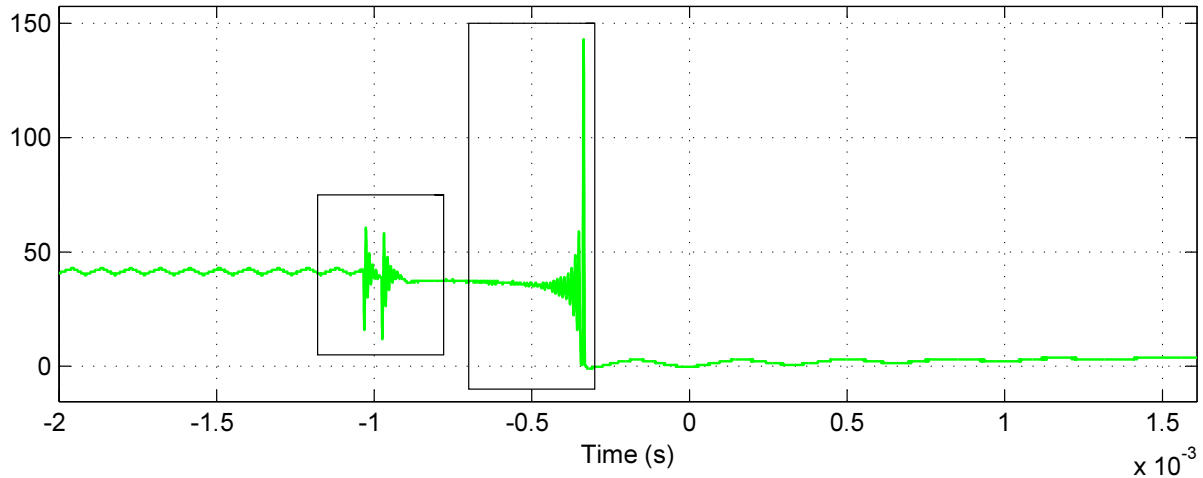
Figure 4.9: First series of tests: interrupting 41 amperes at 35 volts (capacitor included) additional probe

Although this test DC breaker was able to interrupt current at low voltage, it was early to conclude it as suitable device. In order to use the breaker as a part of test setup, it had to be tested in higher voltages. A suitable DC breaker should be able to interrupt ip to 150 amperes at 800 voltages. Thus higher voltage source had to be used.

Second series of tests

Modifications in the design of second DC breaker are illustrated in Figure 4.10 and Figure A.6. The aim of these tests was to perform similar set of experiments with modified values in the parallel circuit. Instead of two 10 F capacitors resulting in total capacitance of 5 F, a twin set of 50 F capacitors were used. This resulted in the total capacitance of 25 F in parallel with the ACCB. Cable connections between ACCB and capacitors were replaced by small copper bars resulting smaller inductance in the path.
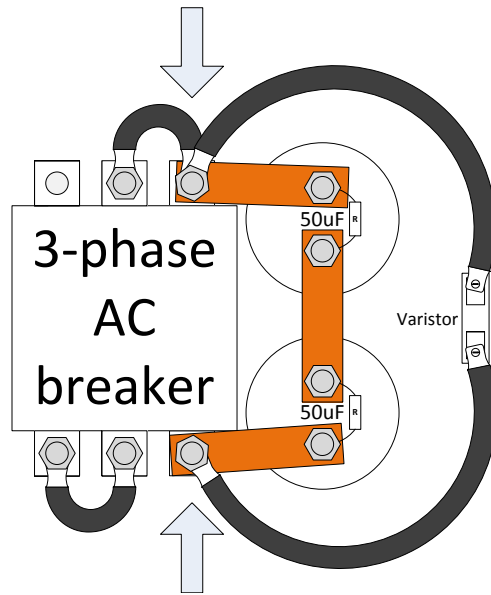
Figure 4.10: Second test DC breaker

Again, bare ACCB was tested before connecting parallel circuit of the test DC breaker. Current and voltage was increased gradually and each test was repeated several times. Additional probe was not used in this series of tests due to the absence of parallel circuit. Results of these tests are illustrated in Figure 4.11.
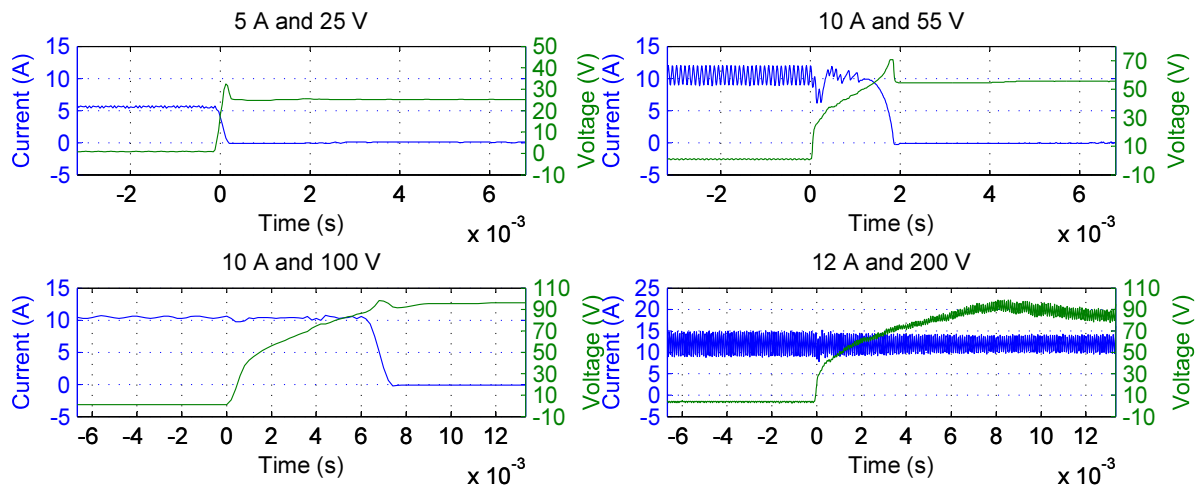
Figure 4.11: Test results from ACCB testing

In tests below 100 volts, the ACCB managed interrupting the DC circuit. However, even with relatively low currents, the ACCB could not break the circuit at 200V. Tests were repeated multiple times and 8 times out of 10, the breaker failed. Current did not decrease to zero and voltage readings over the arc are unstable and noisy (see Figure 4.11).

Parallel circuit was added to the test breaker. With the parallel circuit the breaker was able to interrupt higher currents. Each test was again repeated multiple times and the performance of the test DC breaker varied greatly from test to test. Test results at higher current and voltage ratings were inconsistent; test DC breaker was not able to interrupt the current within 70 ms 6 or 7 times out of 10 tests. When the test DC breaker was, however, able to interrupt the current, then the amount of time it took, was inconsistent. Some of the successful tests of second resonant DC breaker are illustrated in Figure 4.12.
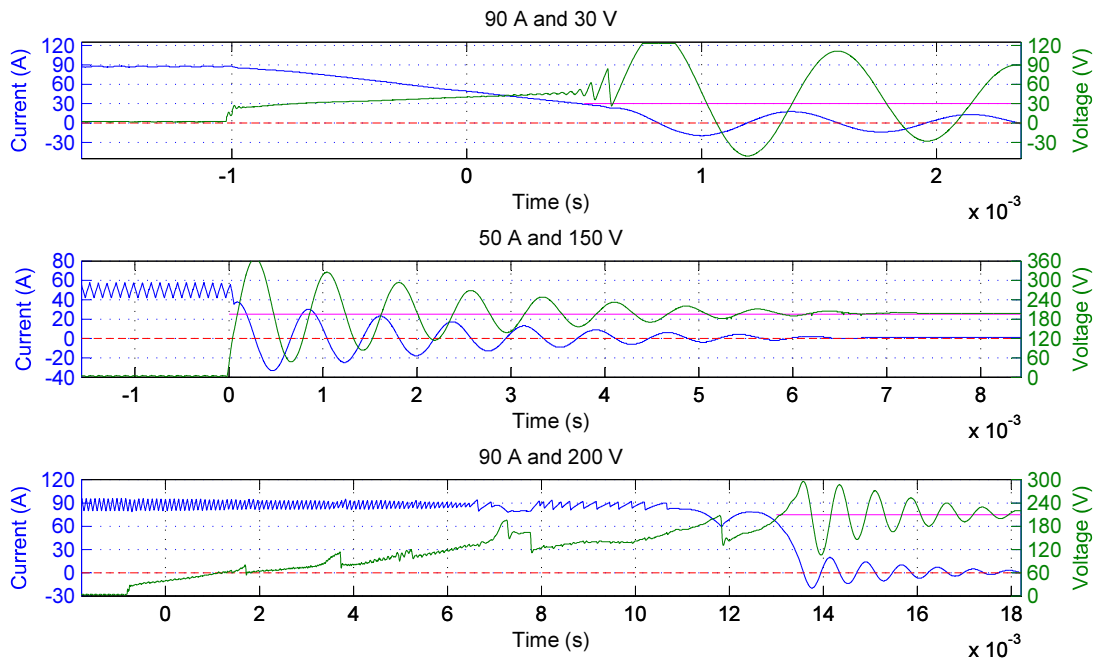
Figure 4.12: Test results from ACCB testing

Critical value of voltage rating occurs was 200 V. 6-7 tests out of 10 were not successful and the ones that did succeeded to interrupt, had a lot of current and voltage spikes on the waveform. 90 A and 200 V DC breaker test, for example, resulted in visible sparks in

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the AC contacts. A modest example of unstable behaviour in the AC breaker chamber is illustrated in the bottom figure showing one of the successful tests of resonant DC breaker interrupting 90 A at 200 V.

4.3   Conclusion and further work on circuit breakers

Due to unsatisfying results of the DC breaker tests, it was decided that solid-state DC breakers will be developed and used for the laboratory purpose. These breakers could be equipped with parallel circuits consisting of normal AC breakers and smaller solid state interrupter, should one desire to create a hybrid DC breaker for laboratory use.

Work on developing a laboratory DC breaker, intended to create interruptions in the DC grid, was ended with drawings on the solid state DC breaker. Four IGBTs would be connected in series and gates of these semiconductor devices will be controlled by gate driver described in [18].
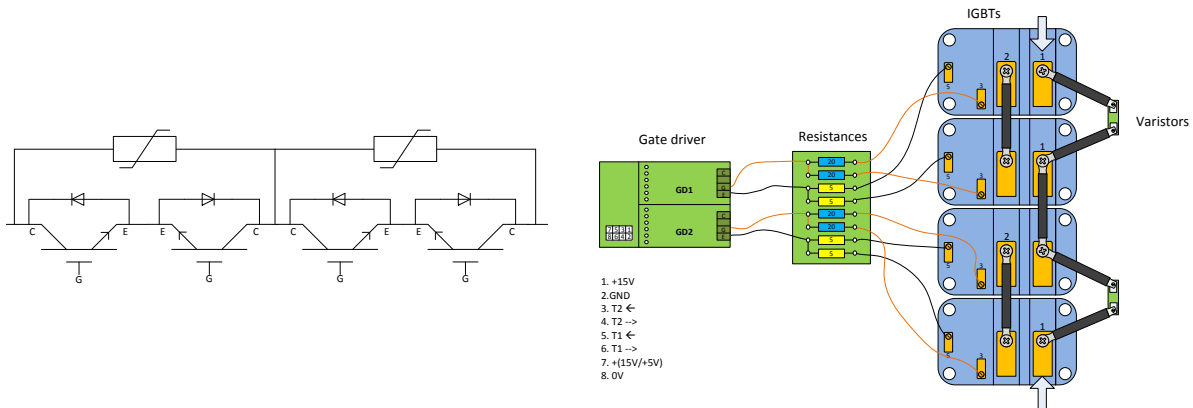
Figure 4.13: Test results from ACCB testing

Four IGBTs need to be mounted on heat sink so that losses from switching operations could be extracted from the devices.

5 Further work

There are several possibilities to improve test setup for further work. This chapter focuses on the most obvious future developments regarding physical system, software and methodology.

5.1 DC line models

Inductance

Inductances in the DC network have significant effect on the behaviour of the system in dynamic mode. Precise modelling of inductance in DC lines is essential when short circuit sequences in the DC network become of interest. Accurate line parameters from cable manufacturers help setting up correct down-scaled model of the HVDC grid. Effort should be made on finding these values.

Inductive element in the DC line model should be adjustable for different lengths of the represented down-scaled network. Care should be taken in calculating the accurate values for the laboratory inductors. In addition, inductance in the system ought to be adjustable with the same steps as existing resistor banks. This ensures the constant relation between resistance and inductance in the DC line models. It could be desirable to conduct sensitivity analysis on the DC lines with respect to different cable types, changing the relation between resistance and inductance in the cable models. Thus, changing the inductance of the DC line model in small steps should be made possible. Implementation of variable inductors would meet all the aforementioned criteria.

Capacitance

Much like modelling inductance in the DC line, capacitance needs to be added for accurate dynamic behaviour of the HVDC model. Variable capacitance should be added

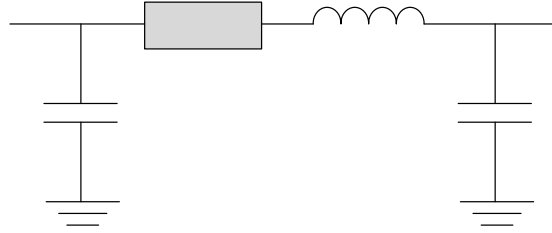into π-equivalent representation of the DC line as shown in Figure 5.1.

Figure 5.1: π-equivalent of line model

Resistor banks and connector cables

Adjustments in the design of the resistor banks could be considered for improved accuracy of resistances. In order to avoid replacing the bypassing switches, each resistor bank could be measured under the load for mode accurate values.

Resistance in the connection cables and internal connections of VSCs could be measured and if possible adjusted so that the values between each converter would correspond. By any feasible measure, this resistances should be minimized so that the range of usable resistance could be maximized.

5.2 Software improvements

Outer current controller

Existing LabVIEW code sends active references into the FPGA boards without implementing any current controllers. It could be of interest to bypass the internal FPGA board outer current controller and implement it in the LabVIEW program instead. Figure 5.2 illustrates the aforementioned idea.
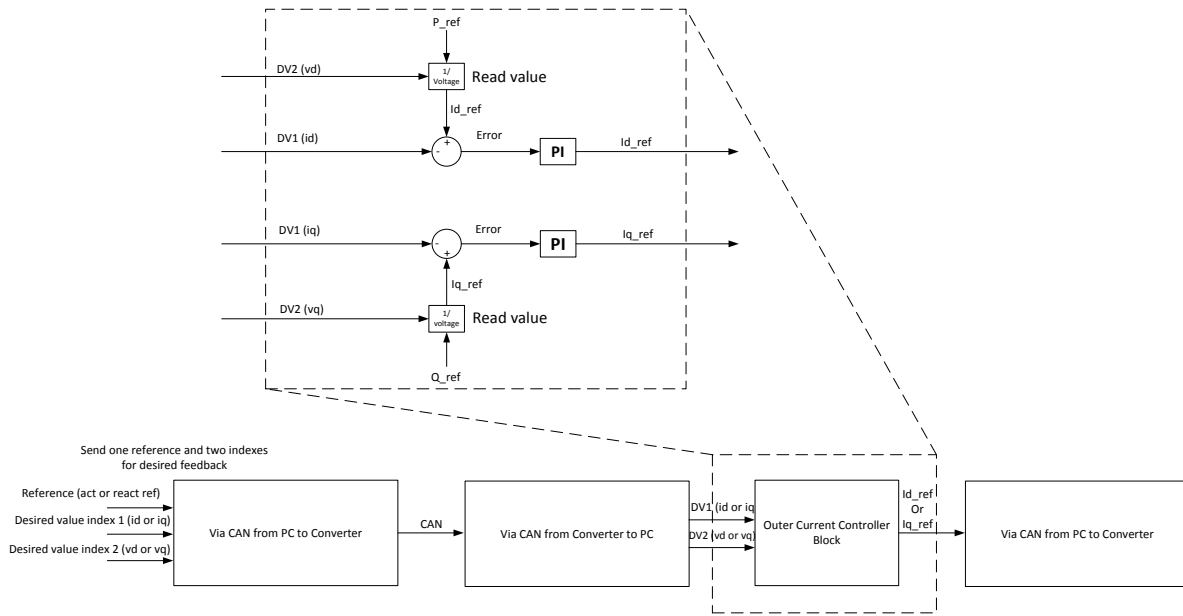
Figure 5.2: Advanced control of converters

Precise power control

Having outer current controller outside the FPGA boards would enable implementing more sophisticated control strategies. Conventional DC droop control, being very similar to frequency droop control in AC systems, does not however take into account the losses in the DC network resulting in inaccurate power flow [19]. Access to active power references of the converters allows implementing precise power control as discussed in [1].

6 Conclusion

Minimal requirements for setting up laboratory test system for studying DC voltage droop in multi-terminal DC grid were fulfilled. It was assumed that DC line models consisting of only resistances is sufficient for steady state analysis. Three VSCs were added to star-connected DC network and DC voltage references were used to implement DC droop control. User interface for controlling and monitoring the operation of three VSCs was developed.

DC droop control was tested and reported in 5 different configurations. These 5 configurations differed from one another with respect to DC grid arrangement and values of DC droop constants. Laboratory test results were compared to analytical solution. Comparison showed that there is a strong relation between laboratory and expected test results. In all of the reported cases, active power measurements had the same relation between the converters. In other words, converter that was expected to have largest impact to the DC power flow, always met those expectations and vice versa.

DC voltage measurements were very close to the expected ones having mostly no more than 1-2 V difference between laboratory test results and analytical solution. Measurements were relatively prone to fluctuation errors so from time to time there was more deviation, between laboratory test result and analytical solution, than expected. DC voltage measurements based on average value over longer period could have eliminated this problem.

More accuracy in measuring the resistance of the DC line model would have resulted in better match between expected and tested results. Resistances were measured from the terminals of VSCs' cabinet, thus the resistances inside the cabinets were not determined. This additional resistance would in turn have affected analytical results and would possibly have resulted in better match between expected and tested results. Using measurements from the DC side of the converter would have excluded losses in the VSCs making results closer to the expected ones.

Study and development towards laboratory DC breaker led to a conclusion that simplest and most effective laboratory DC breaker should consist of solid state switches. Although

the work towards laboratory DC breaker could not be finished due to limited time frame, it can be concluded that laboratory DC breaker based on solid state switches is more feasible and further work should be put into developing one.

For dynamic studies more advances model of DC lines should be used. DC line equivalent based on only resistances is not sufficient. Accurate information from subsea DC cable manufacturers would help to set up as true-to-life model as possible.

Appendix A: Additional pictures

Figure A.1: DC resistor cabinet and voltage source converters
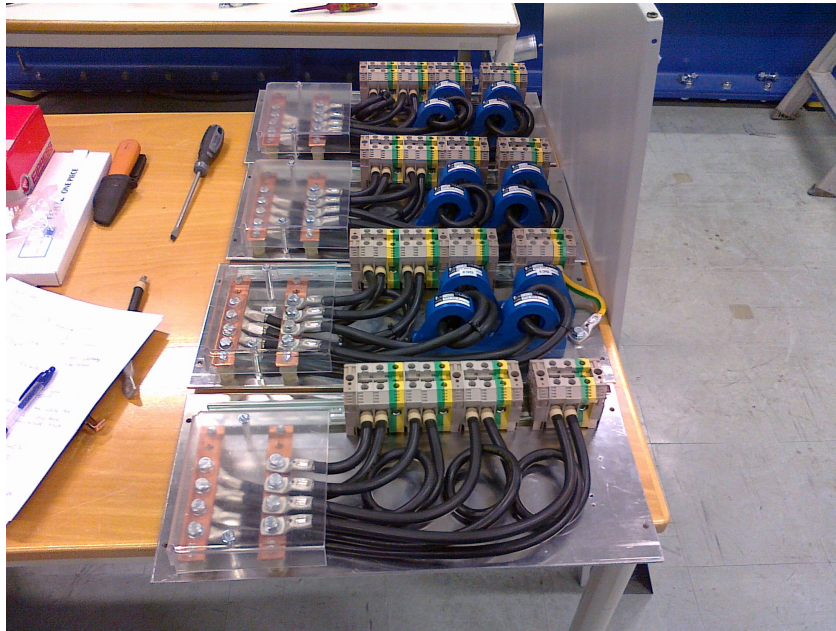
Figure A.2: DC busbars

Figure A.3: DC resistors in the cabinet

Figure A.4: Busbars and cooling fan in the cabinet
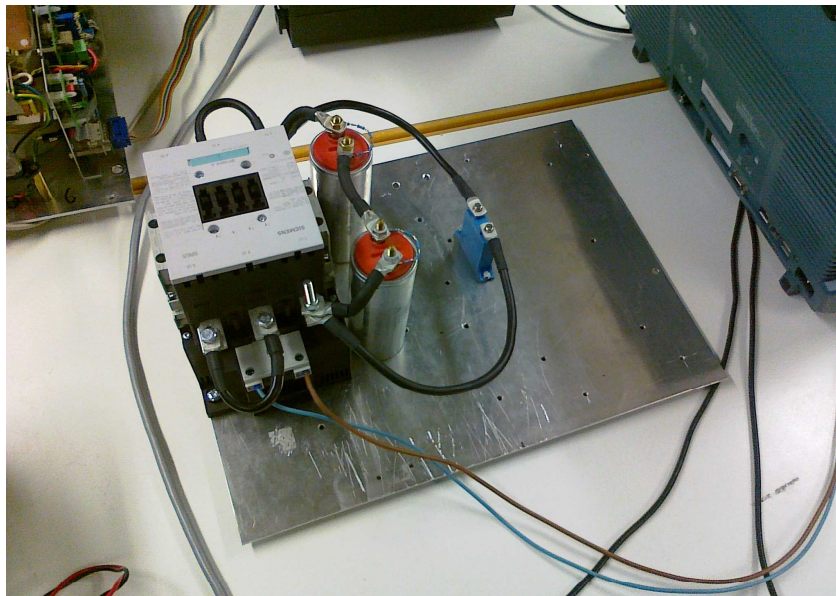
Figure A.5: First test DC breaker
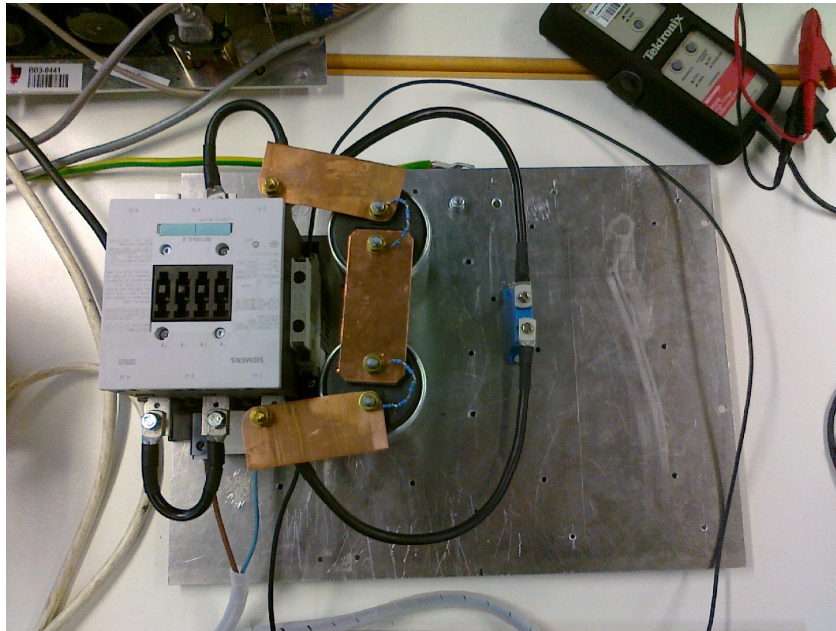
Figure A.6: Second test DC breaker

Appendix B: Additional figures
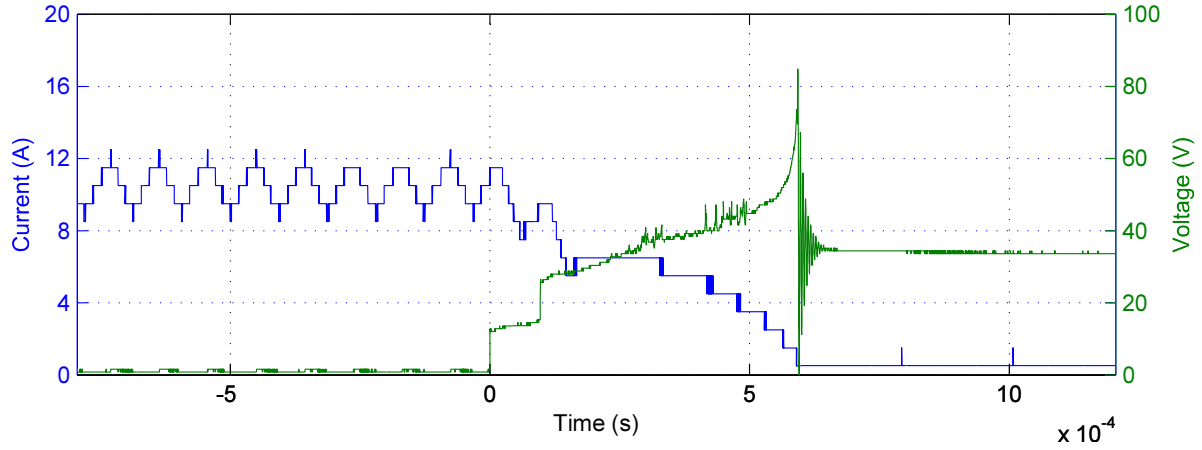
Figure B.1: Reference DC breaker tests: interrupting 10 amperes at 35 volts (no capacitor)
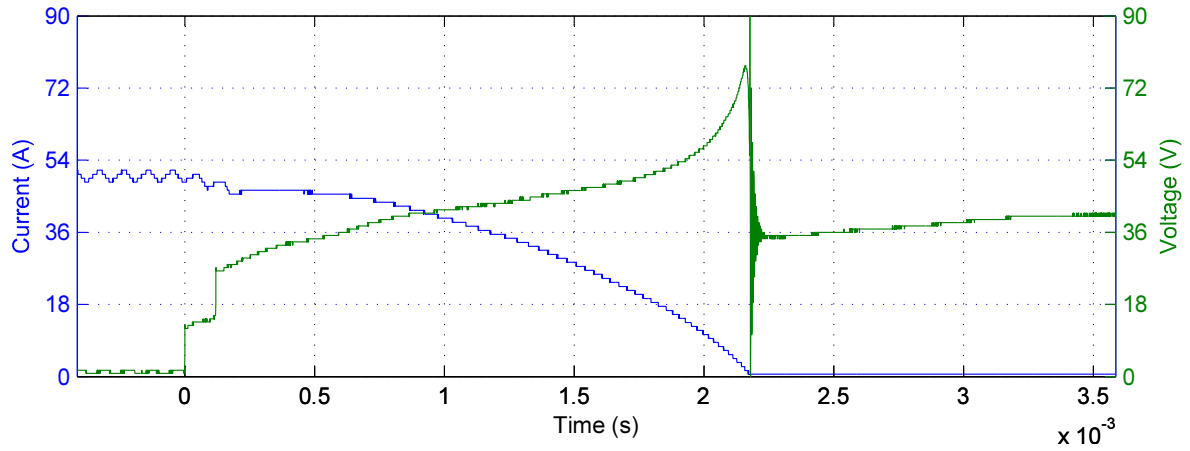
Figure B.2: Reference DC breaker tests: interrupting 50 amperes at 40 volts (no capacitor)

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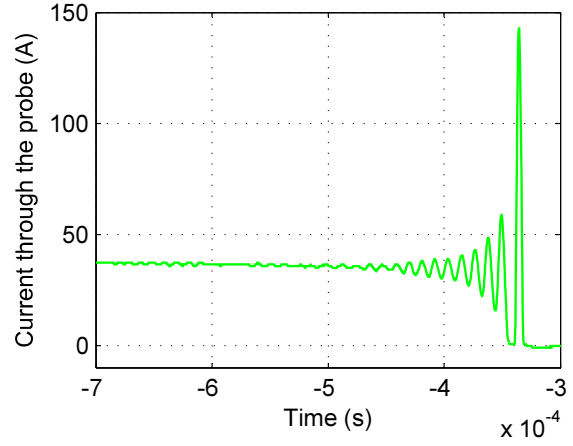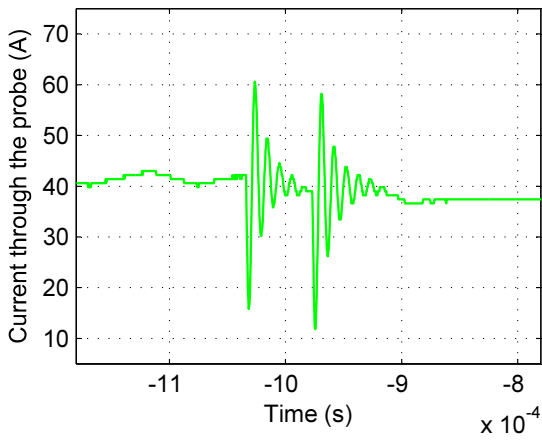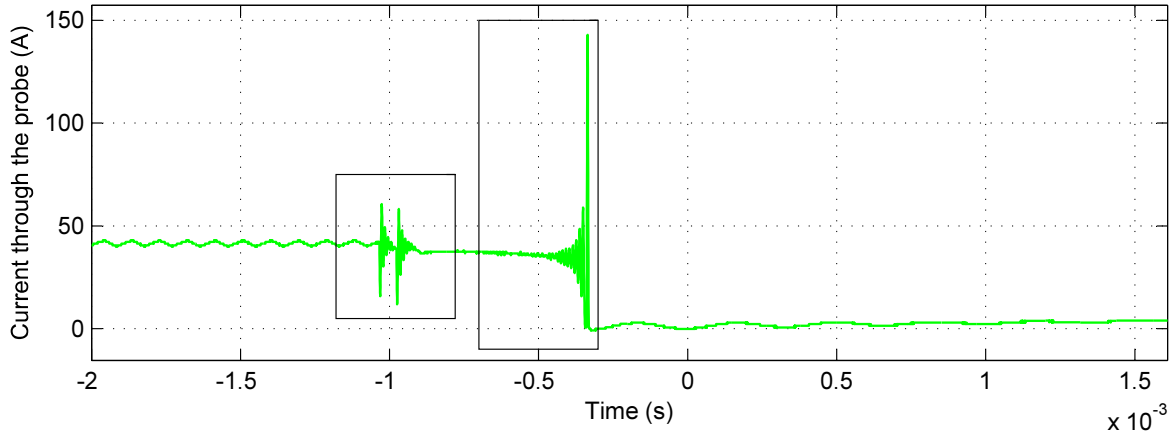
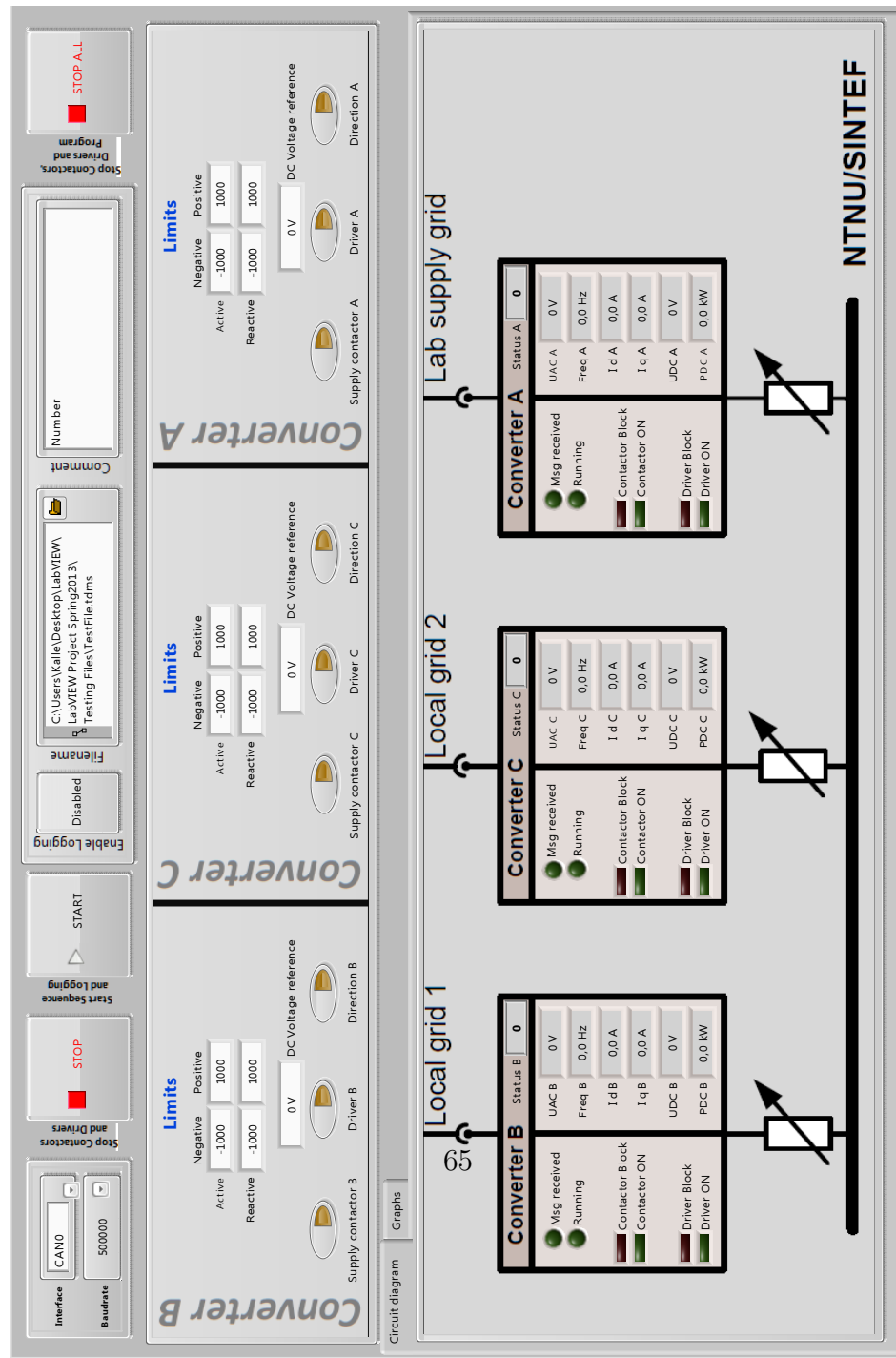Figure B.3: First series of tests: interrupting 41 amperes at 35 volts (capacitor included) additional probe

Appendix C: LabVIEW program

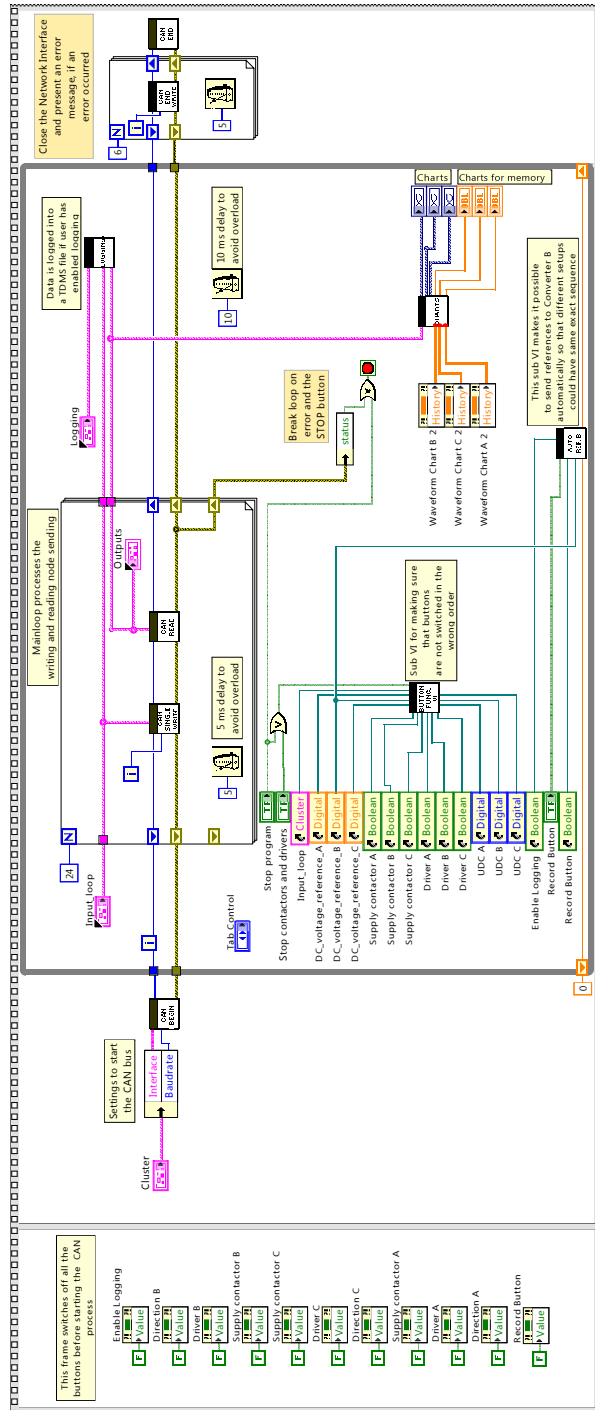Figure C.1: User interface front panel of the LabVIEW program
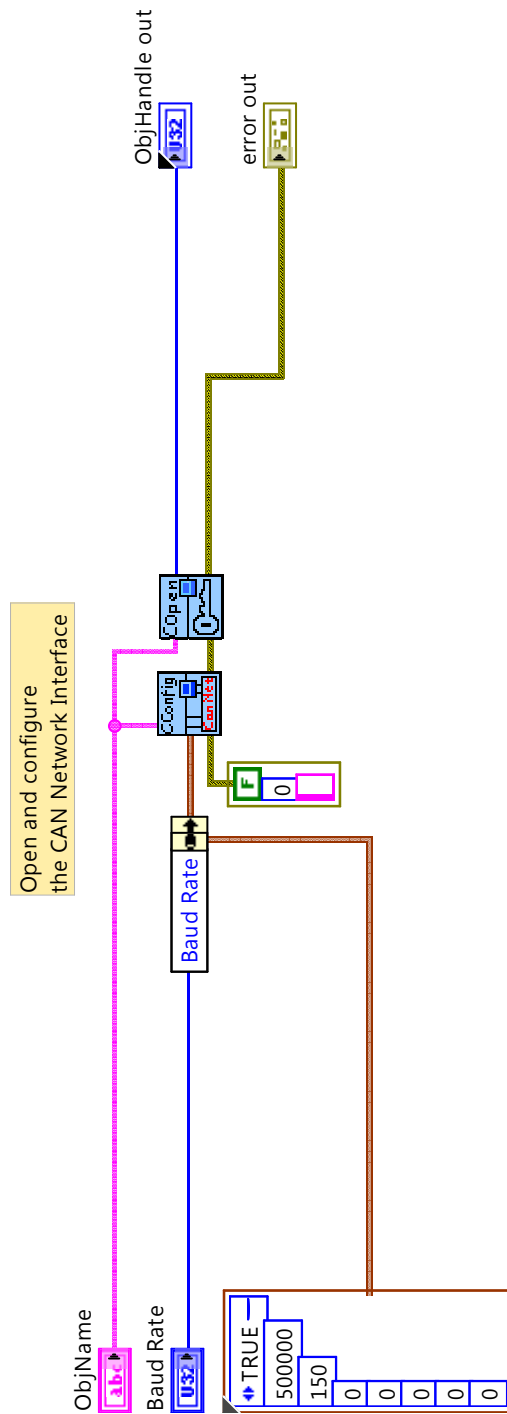
Figure C.2: Main block diagram
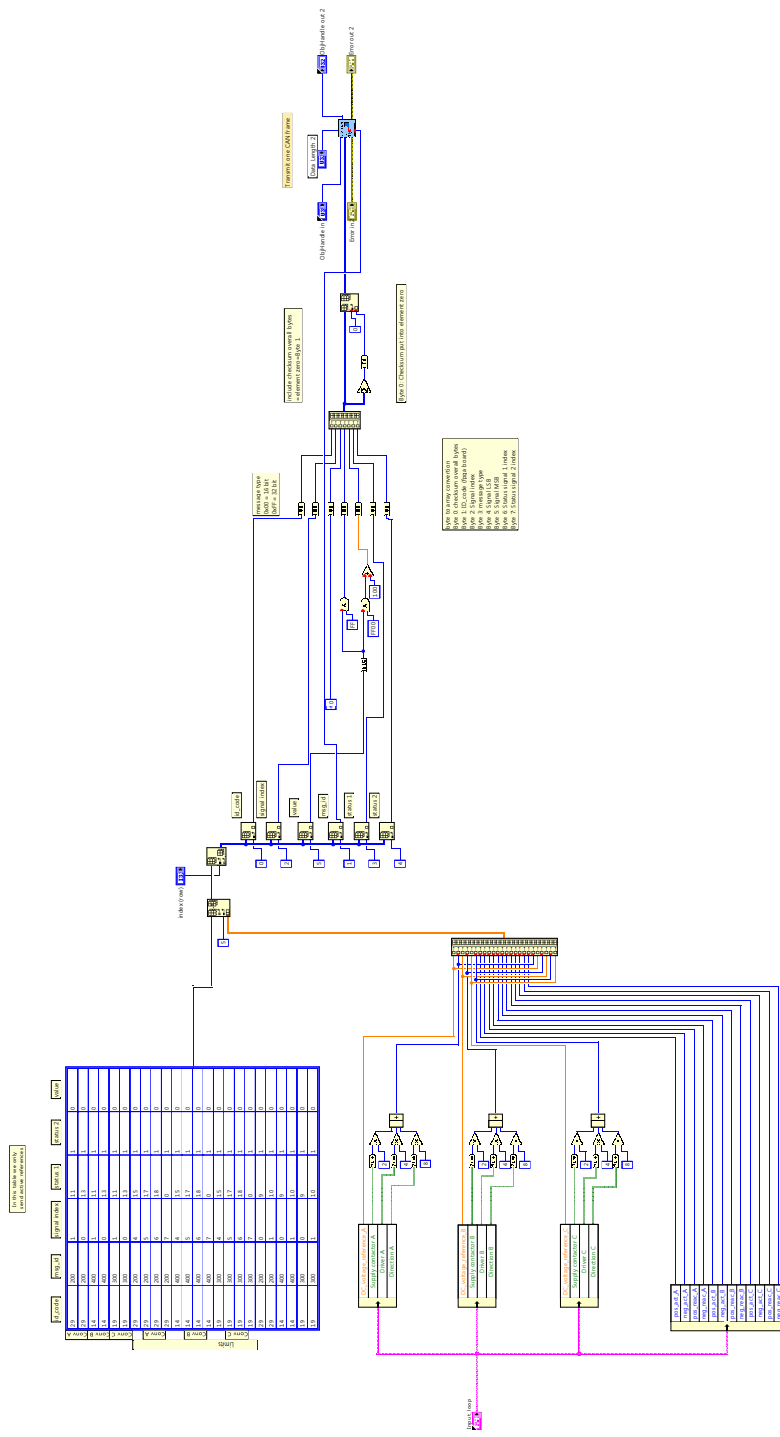
Figure C.3: Block diagram of CAN BEGIN SubVI

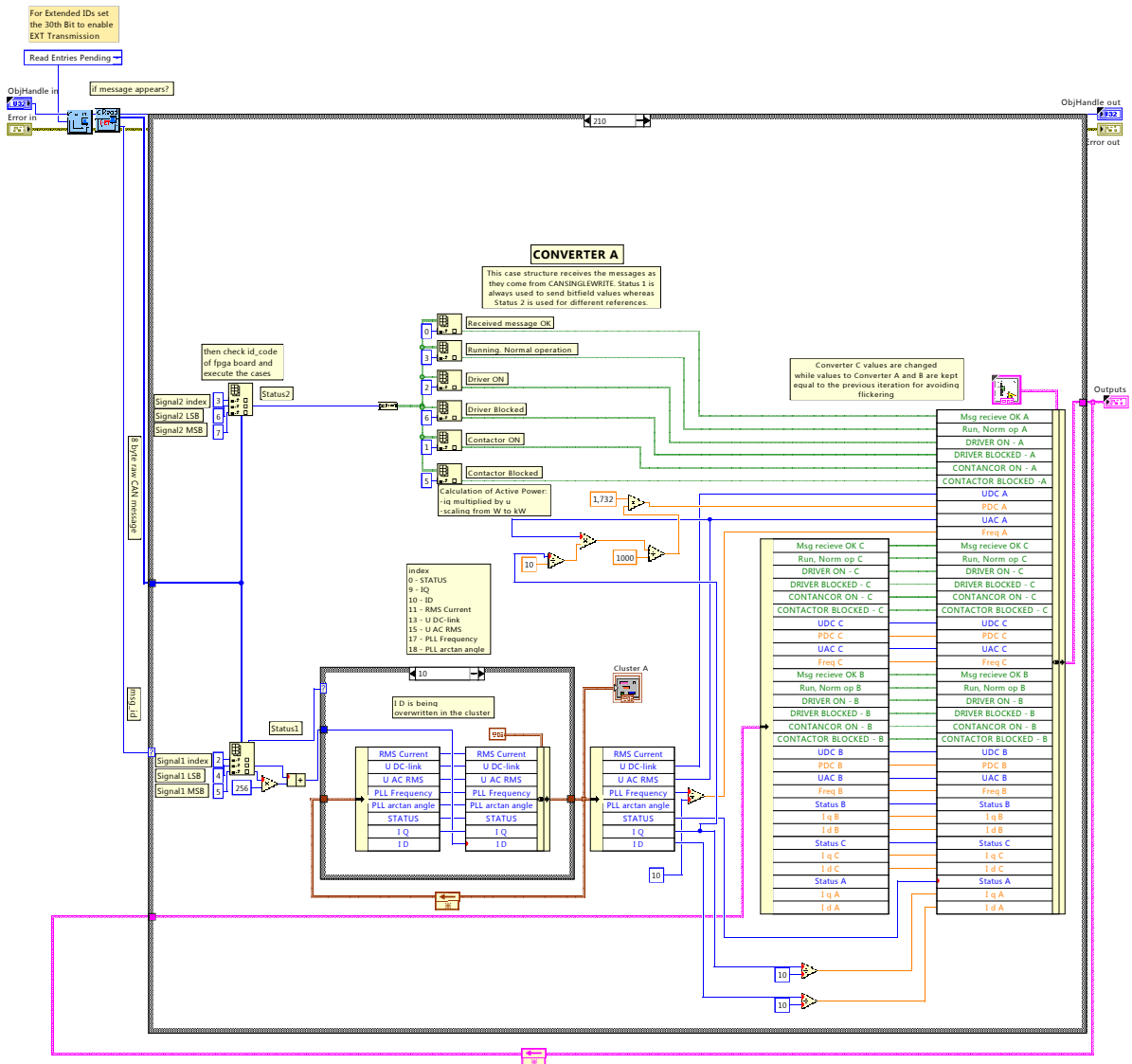67

Figure C.4: CAN single write SubVI
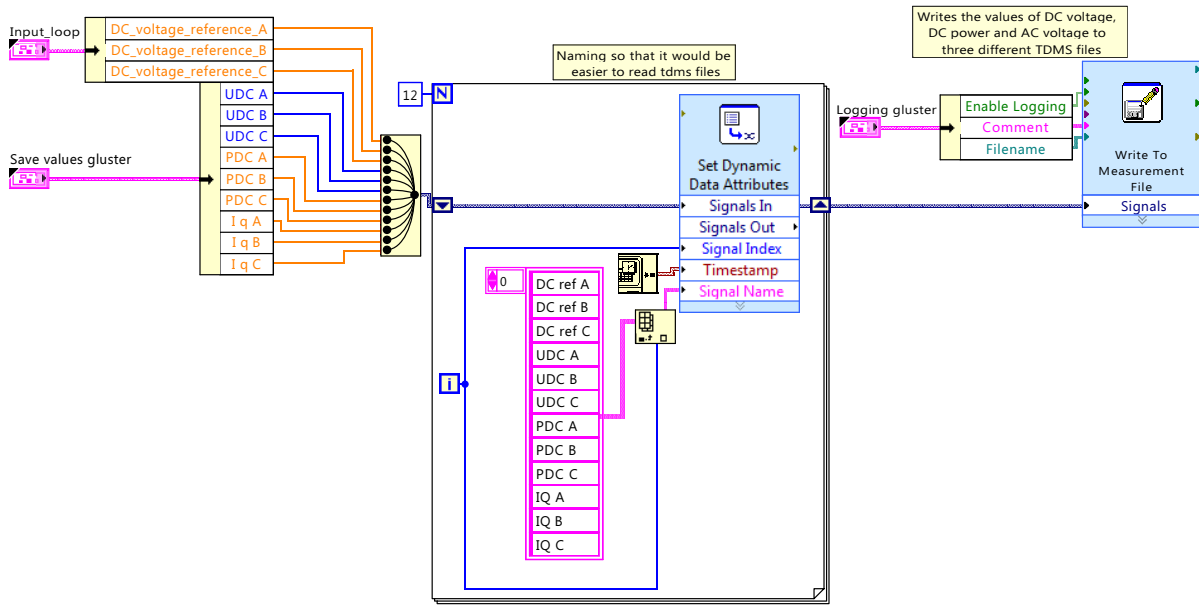
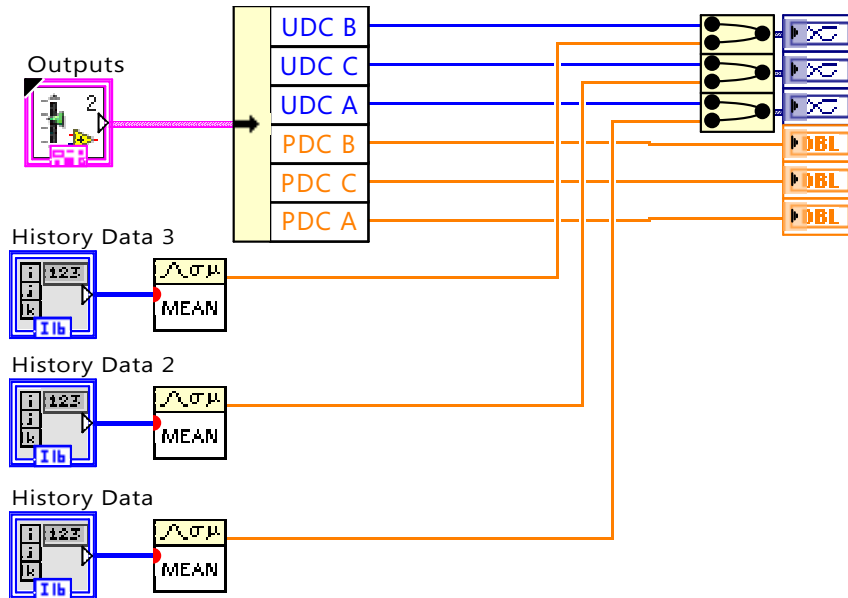Figure C.5: CAN read SubVI

Figure C.6: Data logging SubVI

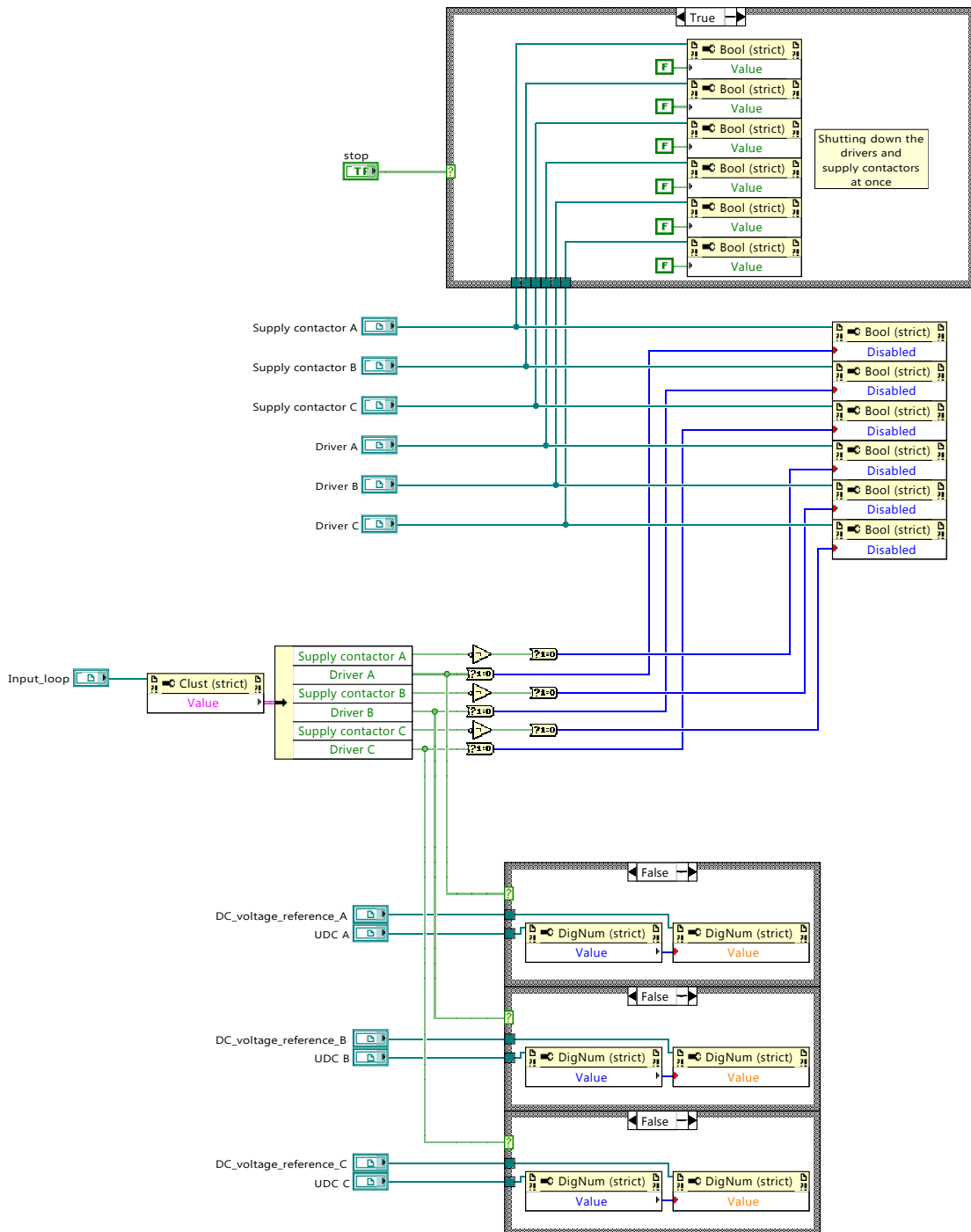Figure C.7: SubVI for charts in the front panel
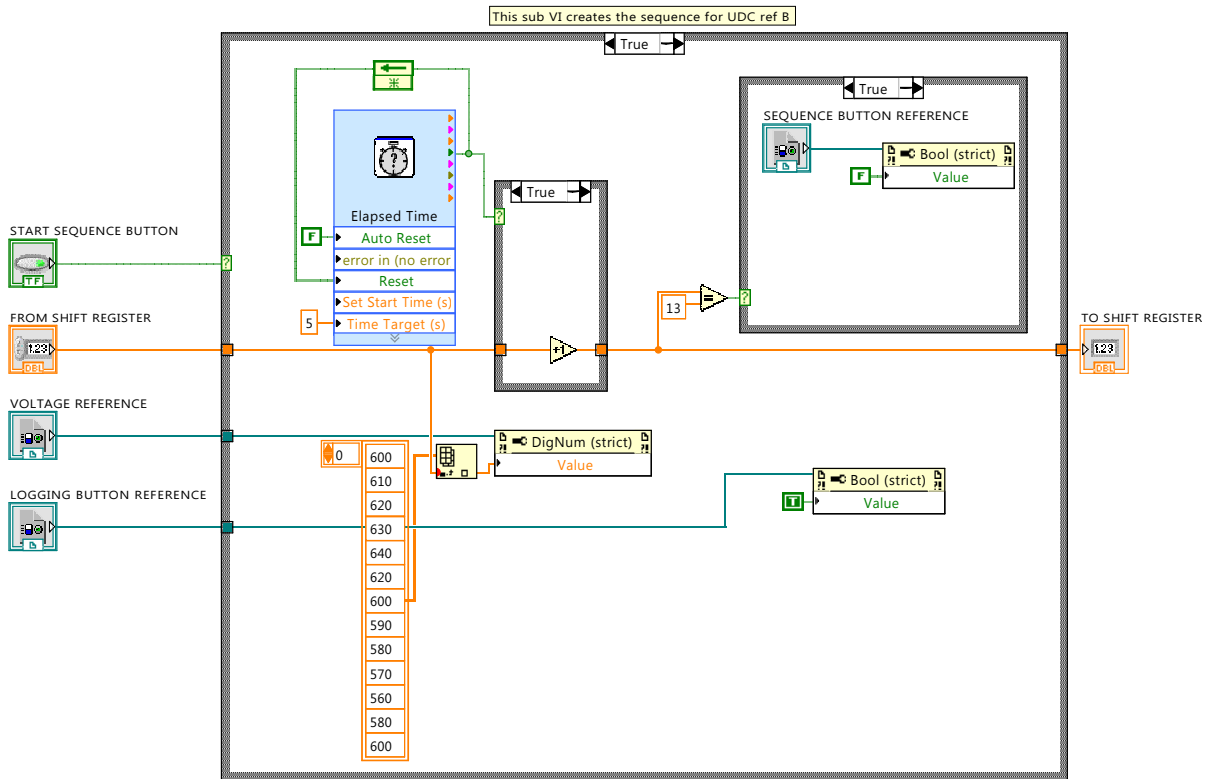
Figure C.8: Safety function for order of button switching
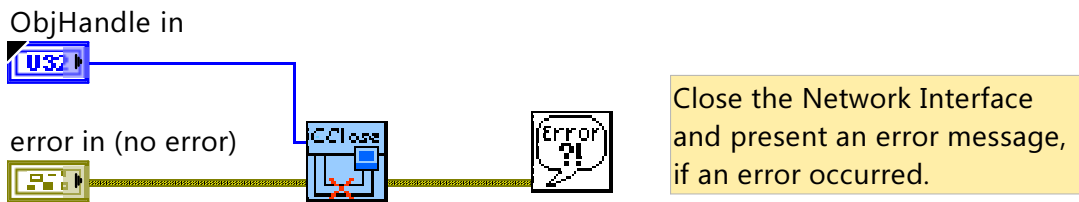
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Figure C.9: SubVI for defined testing sequence
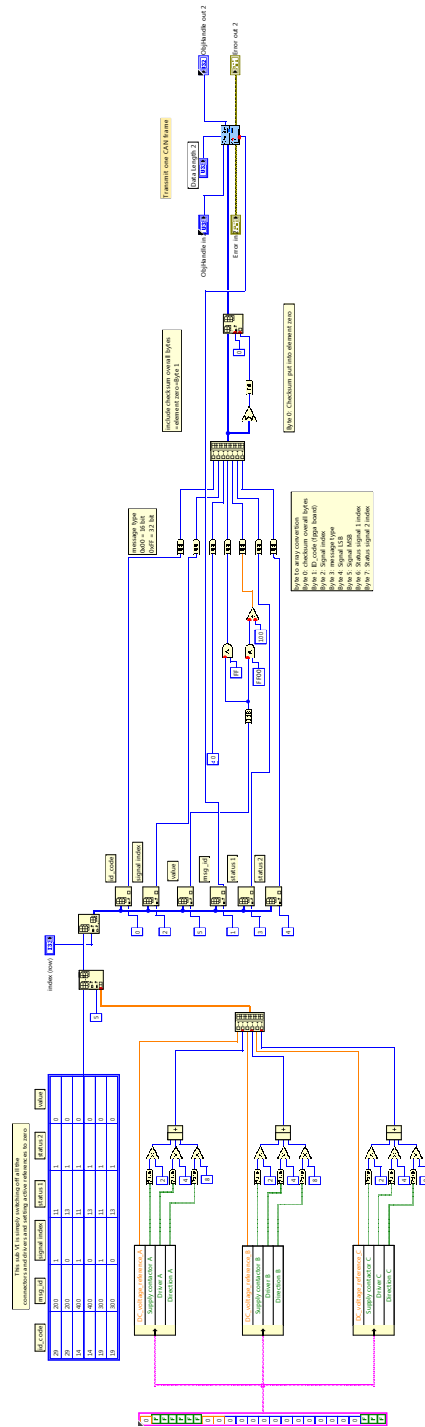

Figure C.10: CAN End SubVI

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Figure C.11: CAN Single End SubVI

Appendix D: Matlab code

```matlab
%% General

u=1;     %linewidth
clc
%*****Choose case nr!*****
n=input('Please select the case number (between 1-36):');
%************************

f = figure;

outputString = sprintf('Number%d', n);

DATA=xlsread('Test020513.xlsx',outputString);

TIME=DATA(:,1)/514*65;   %Time for all cases

DC_ref_B=DATA(:,3);      %Converter B reference voltage data
UDC_B=DATA(:,6);         %Converter B DC voltage data
PDC_B=DATA(:,9);         %Converter B power data

DC_ref_A=DATA(:,2);      %Converter A reference voltage data
UDC_A=DATA(:,5);         %Converter A DC voltage data
PDC_A=DATA(:,8);         %Converter A power data

DC_ref_C=DATA(:,4);      %Converter C reference voltage data
UDC_C=DATA(:,7);         %Converter C DC voltage data
PDC_C=DATA(:,10);        %Converter C power data

%% Computation

% reference powers are zero

clc

Pref = [0 0 0]';

% droops are read from the file

delta=[DATA(1,14)/100 DATA(1,15)/100 DATA(1,16)/100]';

Ra_bank = 2*DATA(2,17);    %mOhm
Rb_bank = 2*DATA(2,18);    %mOhm
Rc_bank = 2*DATA(2,19);    %mOhm

Ra=(Ra_bank)/(1000*6);   %resistance on converter A branch in pu
Rb=(Rb_bank)/(1000*6);   %resistance on converter B branch in pu
Rc=(Rc_bank)/(1000*6);   %resistance on converter C branch in pu

Rpro=Ra*Rb+Rb*Rc+Ra*Rc;

Y(1,1)=(Rb+Rc)/Rpro;     Y(1,2)=-Rc/Rpro;        Y(1,3)=-Rb/Rpro;
Y(2,1)=-Rc/Rpro;         Y(2,2)=(Ra+Rc)/Rpro;    Y(2,3)=-Ra/Rpro;
Y(3,1)=-Rb/Rpro;         Y(3,2)=-Ra/Rpro;        Y(3,3)=(Ra+Rb)/Rpro;

% U reference
```

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```matlab
Uref=[interp1(TIME, DC_ref_A, 12.5)/600 interp1(TIME, DC_ref_B, 12.5)/600 interp1(TIME,↙
DC_ref_C, 12.5)/600]';

% U

U=[1 1 1]';

 funk=[0 0 0]';

for iteration=1:6

    for l=1:3
        temp=0.0;
        for c=1:3
            temp=temp+U(c)*Y(l,c);
        end
        funk(l)=U(l)*temp+1/delta(l)*(U(l)-Uref(l))-Pref(l);
    end
    for l=1:3
        for c=1:3
            if l==c
                 temp=0.0;
                for i=1:3
                    temp=temp+Y(l,i)*U(i);
                end
                Jac(l,l)=temp+Y(l,l)*U(l)+1/delta(l);
            else
                Jac(l,c)=Y(l,c)*U(l);
            end
        end
    end

    for i=1:3
        P(i)=Pref(i)-1/delta(i)*(U(i)-Uref(i));
    end

U=U-inv(Jac)*funk;
funk;
end


p_a = interp1(TIME, PDC_A, 12.5);
u_a = interp1(TIME, UDC_A, 12.5);
p_b = interp1(TIME, PDC_B, 12.5);
u_b = interp1(TIME, UDC_B, 12.5);
p_c = interp1(TIME, PDC_C, 12.5);
u_c = interp1(TIME, UDC_C, 12.5);

POW = ['       ',num2str(p_a,3),' kW                 ', num2str(p_b,3),' kW              ',↙
num2str(p_c,3),' kW    '];
VOL = ['        ',num2str(u_a,4),' V                ', num2str(u_b,4),' V              ',↙
num2str(u_c,4),' V    '];

POW1 = ['        ',num2str((-1)*P(1)*60,3),' kW                 ', num2str((-1)*P(2)*60,3),'↙
```

```
kW               ',num2str((-1)*P(3)*60,3),' kW    '];
VOL1 = ['        ',num2str(U(1)*600,4),' V                ', num2str(U(2)*600,4),' V↙
',num2str(U(3)*600,4),' V    '];

DEL1= ['delta_a=',num2str(delta(1)),'              Ra=',num2str(Ra*(1000*6)),' mOhm↙
Uref_a=',num2str(interp1(TIME, DC_ref_A, 12.5)),' V'];
DEL2= ['delta_b=',num2str(delta(2)),'              Rb=',num2str(Rb*(1000*6)),' mOhm↙
Uref_b=',num2str(interp1(TIME, DC_ref_B, 12.5)),' V'];
DEL3= ['delta_c=',num2str(delta(3)),'              Rc=',num2str(Rc*(1000*6)),' mOhm↙
Uref_c=',num2str(interp1(TIME, DC_ref_C, 12.5)),' V'];

disp    ('_____')
disp(DEL1)
disp(DEL2)
disp(DEL3)
disp    ('_____')
disp    ('*************Laboratory test results (t=12.5s)*************')
disp    ('_____')
disp    ('       Pa               Pb               Pc       ')
disp(POW)
disp    ('_____')
disp    ('       Ua               Ub               Uc       ')
disp(VOL)
disp    ('_____')
disp    ('_____')
disp    ('***************Power flow results (t=12.5s)**************')
disp    ('_____')
disp    ('       Pa               Pb               Pc       ')
disp(POW1)
disp    ('_____')
disp    ('       Ua               Ub               Uc       ')
disp(VOL1)
disp    ('_____')
```

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