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Control of Voltage Source Converters for Power System Applications

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PROBLEM DESCRIPTION

Nowadays, the energy demand is growing rapidly and the renewable energy sources represent a reliable and cost effective alternative to the old-fashioned methods (burning of fossil-fuels, uranium etc). Among other renewable energy sources, wind represents one of the best developed and researched sectors. Even though the onshore wind power industry is more developed than the offshore sector the tendency is to go offshore. Basically due to the increase of size, noise, visual pollution and with regards to higher values of wind speed, the offshore wind applications are dominating over the onshore wind farms. The installation of wind farms offshore rises many engineering challenges related to construction, installation and nevertheless the power transmission. The latter requires great effort in order to make the offshore wind farm viable, especially for power transmission over long distances between the wind farm and the shore. HVDC transmission systems are capable of overcoming these problems offering lower transmission losses compared to traditional HVAC transmission. The VSC-HVDC transmission system incorporates advanced power electronics technology used in electric power systems and has the capability of transmitting large amount of power over long distances. In addition, it allows fast and decoupled active and reactive power control [1]. The weak point of VSC-based HVDC system is the bulky dimensions of dc-link capacitors, which is the main lifetime limiting factor of the entire system. By reducing the dc-link capacitor size a reduction in cost and volume of the inverter can be achieved. However, a small dc-link capacitance leads to large fluctuation in the dc-link voltage, and hence can cause semiconductor switch breakdown. The proposed algorithm in this work involves the control of inverter dynamics. The idea is to control the exact amount of required current in the inverter with the knowledge of rectifier current, to force the power balance. In other words, the voltage control is obtained by controlling the energy that flows in and out of the dc-link capacitor. Hence, the dc-link voltage does not fluctuate even though a fairly small capacitance is utilized due to the fact that no current flows into the dc-link capacitor.

ABSTRACT

The research work is aimed on the investigation of possible modeling and control schemes for the dc-link of VSC, with the purpose of identifying the impact of such modeling and control on the dynamics of the conversion system. A system consisting of back-to-back converters with equivalent grid interconnection and source representation is designed in the software PSCAD/EMTDC using a detailed switching model of the inverter and rectifier components. The control technique based on the well-established concept of vector control is implemented. The main task of the master thesis is oriented towards the achievement of more reliable dc-link dynamics with smaller required capacitance. The control algorithm is based on balancing the power between inverter and rectifier through the dc-link with the minimum dc voltage variations. Dc-link voltage regulation is achieved by implementing a control based on the energy stored in the dc-link capacitor. Alignment to a dq synchronous reference frame orientation with PI regulators is used in the control philosophy for decoupling purposes.

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1. MOTIVATION AND PROBLEM DEFINITION

1.1. Motivation for research

Renewable energy sources are constantly gaining popularity in terms of increasing world energy consumption and *CO-2* reduction research activities. Among them, wind power has reached a considerable growth during recent years. It is projected that significant part of wind installations will be offshore, therefore special attention must be paid to the generated power transmission methods. Figure 1.1 shows the trend of constant wind energy production increase in EU region.

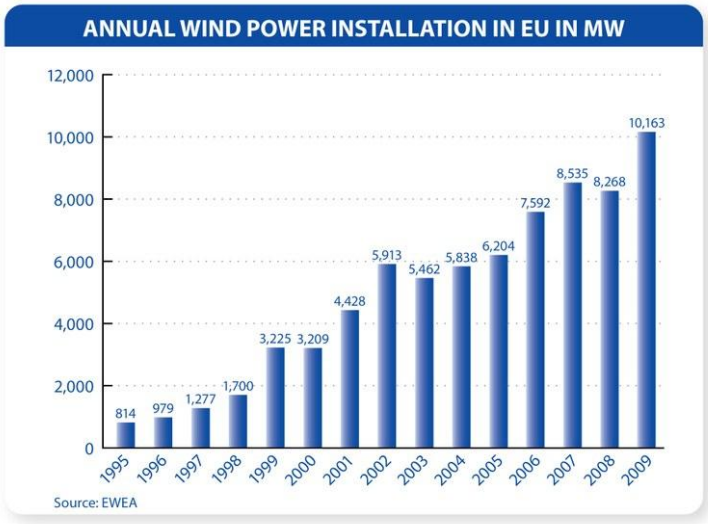


Figure 1.1. Annual wind power installations in EU *(MW)* [2]

According to Figure 1.1 the growth of the wind energy sector is observed every year with a total installed power in the EU reaching 10,163 MW in 2009.

The fast growth in wind power is possible due to several facts, such as inhibition on fossil fuel usage, as well as rapid development of power electronics. Until recently, the offshore wind farm sites were installed close to the shore in relatively small water depths, which encountered several aspects that concerned the use of such sites. Among them, the near-shore area is often used for recreational activities, fishing and maritime traffic. Moreover, the placement of a wind farms close to the shore results in negative environmental impact concerning noise disturbances and visibility pollution. The trend is to increase the distance from the wind farm to the shore. Consequently, the generated power in offshore wind farms has to be transported over long distances to be delivered to the supply grid on the shore. A reasonable solution is the use of

High-Voltage Direct Current (HVDC) transmission. Two different alternatives of HVDC are possible, namely classic HVDC using line-commutated thyristors (LCC-HVDC) and Voltage Source Converter HVDC using self-commutated IGBTs (VSC-HVDC).

1.2. Objectives

The objectives of the research work consist of the investigation of possible modeling and control schemes for the dc-link of VSC, with the purpose of identifying the impact of such modeling and control on the dynamics of the conversion system.

The main goals of the thesis are summarized below:

- good understanding of the VSC-based HVDC transmission system concept and its behavior;
- modeling of the VSC-based HVDC transmission system using PSCAD/EMTDC software;
- implementation of two dc-link control strategies for the VSC-based HVDC transmission system, i.e. using dc-link voltage as variable and dc-link energy as variable;
- analysis of the developed system behavior.

1.3. Structure of the thesis

This thesis studies the control of voltage source converter based HVDC power transmission and the report is structured in four chapters.

The main subject of the master thesis is the dc-link capacitor in back-to-back converters. But the main part of the work is the design of control for power conversion using energy as a variable. The objective is to get instantaneous input/output power balance, using small energy storage in the dc-link, provided by the control.

Chapter 1 provides an introduction to the studied subject, containing motivation for research, the problem formulation and the objectives of the work.

Chapter 2 presents an overview of VSC-based HVDC transmission system. A comparison between conventional HVDC transmission and VSC-based HVDC transmission is made. The applications and the configuration of HVDC system and VSC- HVDC are briefly described.

Chapter 3 deals with the control of the system. This chapter also contains the design of the current controller, the dc voltage controller, the active and reactive power controllers and the

ac voltage controller. The tuning process of these controllers was realized according to well-established tuning criteria.

Chapter 4 describes the design and analysis of a VSC-based dc-link model that utilizes PWM technique and IGBT semiconductors and is implemented into PSCAD/EMTDC simulation software.

Chapter 5 concludes the most important facts of the thesis and presents ideas for the future research work.

2. HIGH-VOLTAGE DIRECT CURRENT TRANSMISSION

2.1. Introduction

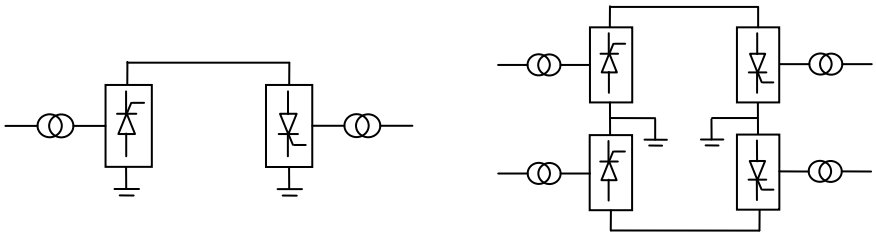
The HVDC transmission is advantageous for power delivery over long distances and asynchronous interconnections by using overhead lines or underground cables. One of the most important aspects of HVDC systems is its fast and stable controllability. It is a well-established technology and since its first commercial introduction in 1954 in Sweden more than 50 projects have been realized [3].

Until recently, the classic HVDC transmission based on thyristors was used for power conversion from ac to dc and vice versa. Appearance of Voltage Source Converter (VSC) makes use of more advanced semiconductor technology instead of thyristors. The VSC-based HVDC installations has several advantages compared to classic HVDC transmission such as independent control of active and reactive power and separate power systems interconnection.

VSC-HVDC is also used to reverse the power flow direction without changing the polarity of dc voltage (in multi-terminal dc systems) and there are no requirements of fast communication between the two converter stations [4].

2.2. HVDC converter arrangements

HVDC converter bridges and cables can be arranged into a number of configurations for effective utilization [5]. Converter bridges may be arranged either monopolar or bipolar as shown in Figure 2.1.



(a) (b)

Figure 2.1. Monopolar (a) and bipolar (b) connection of HVDC converter bridges

Monopolar HVDC system is presented in Figure 2.1 (a). In this configuration, two converters are used which are separated by a single pole line and a positive or a negative dc voltage is used [6]**.** The main properties of monopolar HVDC system are:

- single high-voltage conductor;
- current return through the ground;
- relatively low costs.

Many existing subsea cable transmissions use monopolar system.

Bipolar HVDC system is represented in Figure 2.1 (b). This is the most commonly used configuration of HVDC system in applications where overhead lines are used to transmit power. In fact, the bipolar system consists of two monopolar systems [6]**.**

The bipolar Current Source Converter (CSC) system is represented in Figure 2.1 (b).

The main properties of bipolar HVDC system are:

- two conductors, positive and negative polarity;
- mid-point connected to ground;
- the connection between the two sets of converters is grounded either at one or at both ends;
- one of the poles can continue to transmit power in case the other one is out of service.

Multi-terminal HVDC system. In the configuration of Figure 2.2 there are more than two sets of converters like in the bipolar case. Thus, converters one and three can operate as rectifiers while converter two operates as an inverter. Operating in the opposite order, converter two can operate as a rectifier and converters one and three as inverters [6]**.**

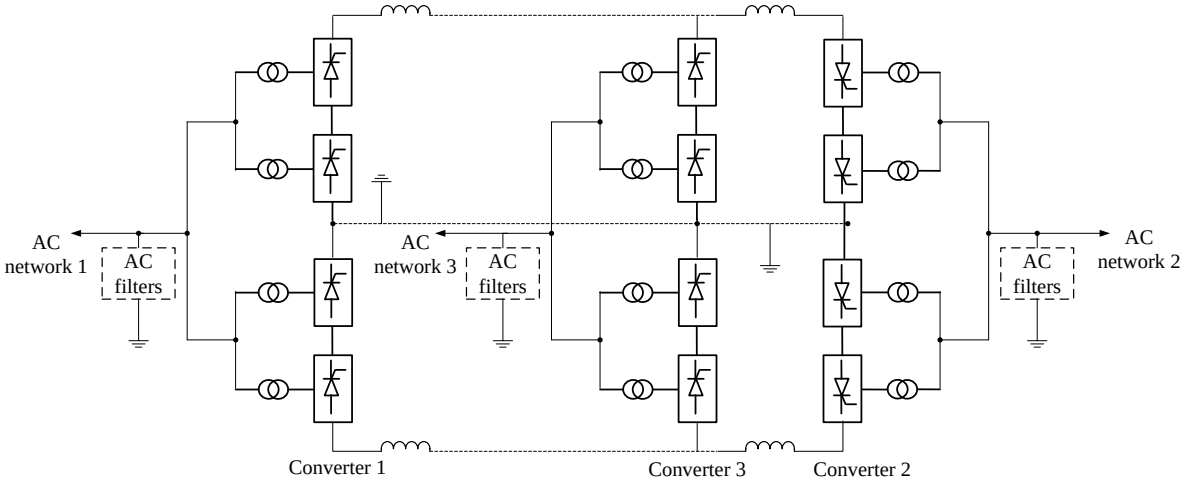


Figure 2.2. Multiterminal HVDC system

Back-to-back HVDC system. In the case of Figure 2.3 the two converter stations are located at the same site and no transmission line or cable is required between the converter bridges. The connection may be monopolar or bipolar. The two interconnected ac systems may have the same or different rated frequency, i.e. 50Hz or 60Hz. This way of connection can also be used to stabilize the ac system.

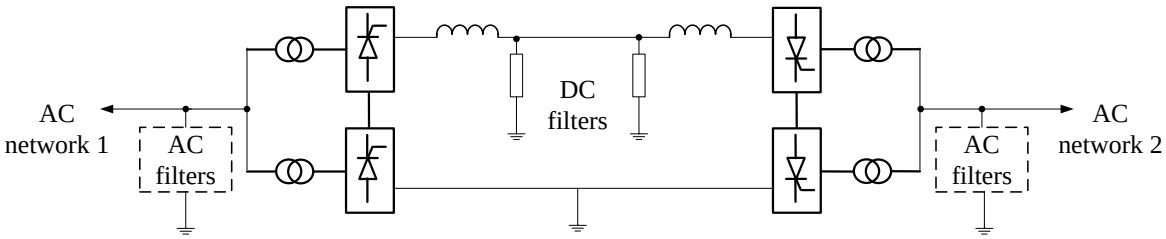


Figure 2.3. Back-to-back converter system

The back-to-back converter consists of a rectifier and an inverter connected with a common dc-link. The properties of this combination are [7]:

- the dc-link voltage must be higher than the peak line operating voltage;
- the dc-link voltage is regulated by controlling the power flow to the ac grid;
- the possibility of fast control of the power flow.

2.3. Classic HVDC transmission

A classic HVDC system in Figure 2.4 consists of ac filters, shunt capacitor banks or other reactive-compensation equipment, converter transformers, converters, dc reactors, dc filters, and dc lines or cables [8].

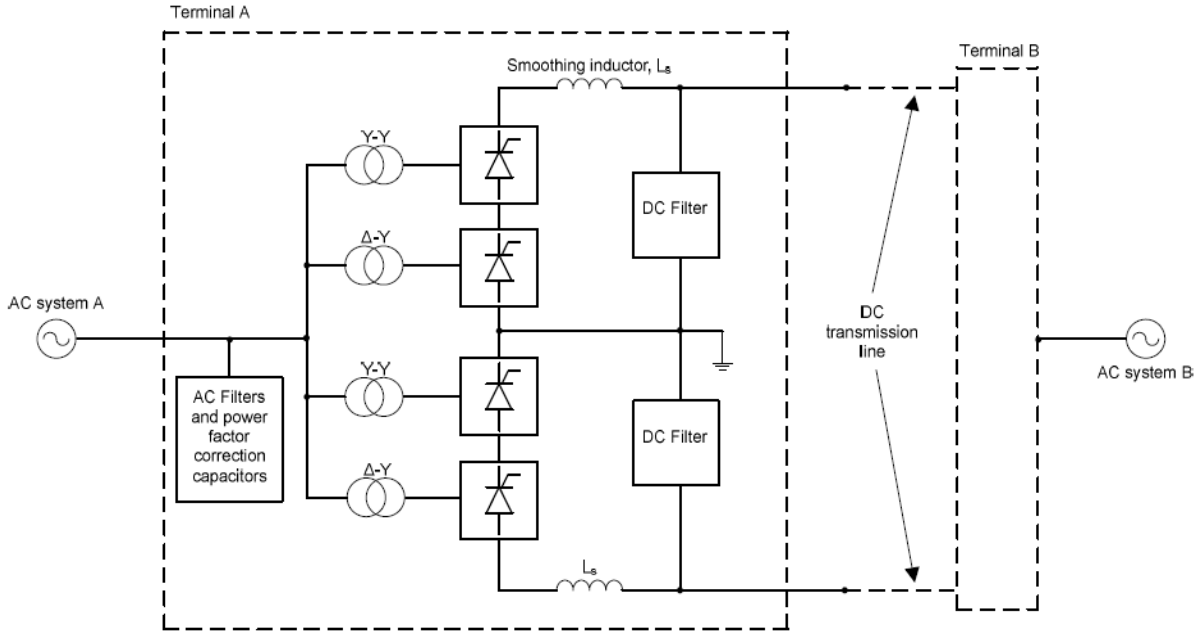


Figure 2.4. A basic configuration for a classic HVDC system [9]

The dominant valve type in classic HVDC converter is a thyristor. Thyristors are able to conduct high currents, in a range of several kilo-amps, and can block high voltages [10]**.** The 6-pulse bridge of Figure 2.4, as the basic converter unit of classic HVDC, can be used both as a rectifier or inverter. A 12-pulse converter bridge can be built by connecting two 6-pulse bridges in parallel or in series. Each bridge consists of defined amount of series connected thyristors. The bridges are connected separately to the ac system by dint of converter transformers, one with Y-Y winding structure and another with Y-Δ winding structure. In this way the 5th and 7th harmonic currents through the two transformers are in opposite phase that helps to reduce the distortion in the ac system [9]**.**

The HVDC converters are HVDC system's most vital part. They implement the conversion from ac to dc at rectifier side and from dc to ac at inverter side. HVDC converters are connected to the ac system by dint of converter transformers. As already mentioned before, CSCs are used in classic HVDC transmission. On the ac side of the converter CSC acts as a constant voltage source. It requires a capacitor as energy storage device, large ac filters for harmonic elimination and a reactive power supply for power factor correction. On the dc side of the converter CSC acts as a constant current source. In this case, CSC requires an inductor as its energy storage device and dc filters that provide appropriate fault current limiting features. The main benefit of CSC is relatively low switching losses.

2.4. VSC-based HVDC system

VSCs utilize self-commutating switches, e.g. gate turn-off thyristors (GTOs) or insulated-gate bipolar transistors (IGBTs), which can be turned on or off in a controlled manner. VSCs operate at high switching frequency utilizing Pulse-Width Modulation (PWM) technique.

Generally, the new transmission technology has the following advantages compared to classic thyristor-based HVDC [11]:

- Possibility to control the reactive power independent of the active power (to or from the converter) without any needs for extra compensating equipment;
- Little risk of commutation failures in the converter;
- Possibility to connect the VSC-HVDC system to a "weak" ac grid or even to one where no generation source is available and naturally the short-circuit level is very low [6]**;**
- Faster dynamic response due to higher switching frequency operation (phase-controlled), which further results in reduced need for filtering and hence smaller filter size [6]**;**
- Minimal environmental impact.

Table 2.1. Comparison of classic and VSC-HVDC systems [available at www.abb.com]

Function	Classic HVDC	VSC- HVDC
Converter valves	Thyristor	IGBT
Connection valve - ac grid	Converter transformer	Series reactor (+ transformer)
Filtering and reactive compensation	50% in filters and shunt capacitors	Only small filter
Dc current smoothing	Smoothing reactor + dc filter	Dc capacitor
Telecom between converter station controls	Needed	Not needed

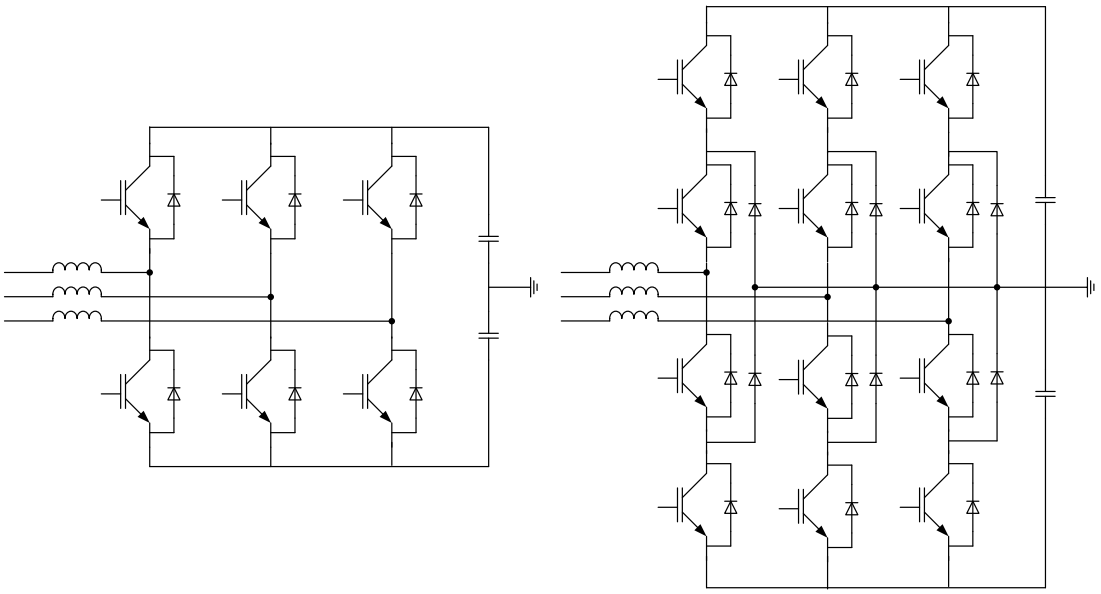
However, VSC transmission has some disadvantages, which include potentially high switching power losses and high capital costs compared to classic HVDC, though the technology continues to evolve.

2.4.1. Configuration of VSC-HVDC

The two VSCs may be seen as the core of VSC-HVDC transmission system topology. One of the VSCs operates as a rectifier, while the other one as an inverter. Both converters

utilize IGBT power semiconductors as switches. The two VSC stations are connected via a dc transmission line.

Mainly, two basic configurations of VSCs are used in HVDC transmission system. These are the two-level VSC converter, presented in Figure 2.5 (a), and the three-level VSC converter, which is presented in Figure 2.5 (b).



(a) (b)

Figure 2.5. The topology of the VSC, (a) two-level VSC, (b) three-level VSC[12]

Typical configuration of VSC-based HVDC transmission system is presented in Figure 2.6.

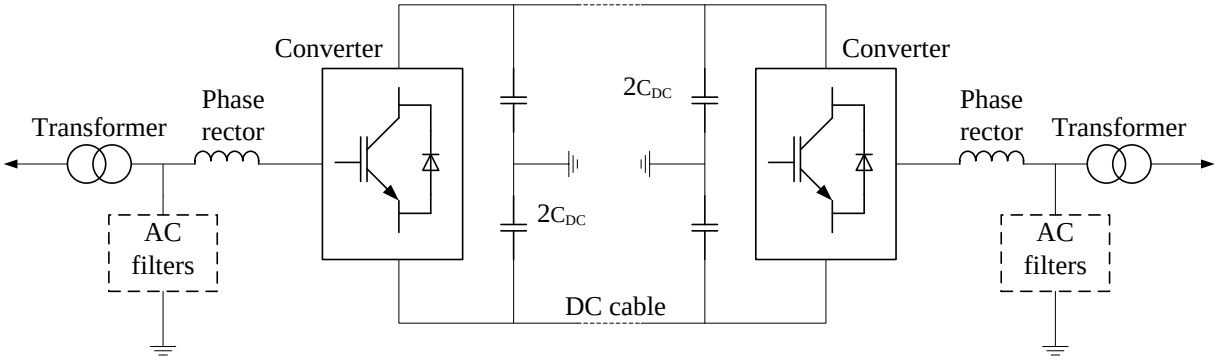


Figure 2.6. Typical VSC-HVDC system [13]

VSC-based HVDC transmission system consists of two VSCs, transformers, phase reactors, ac filters, dc-link capacitors and dc cables.

The sending end and receiving end of VSC-HVDC have the similar configuration, one operating as a rectifier and another as an inverter. In this work the two converters are connected back-to-back. Normally, converters are connected to the ac system by means of transformers. The most important function of transformers is to transform the ac voltage level to the dc voltage level. Usually, they are single-phase three-winding type, but depending on the transportation requirements and the rated power, they can be arranged in other ways [14]**.** The phase reactors are used for controlling active and reactive power flow by regulating currents through them. The reactors also serve as ac filters and therefore reduce the high frequency harmonic contents of the ac currents which are caused by the switching operation of the IGBTs. The dc side contains two equally-sized capacitors. The size of these capacitors depends on the required dc voltage. The primary objective of the dc capacitor is to provide a low inductive path for the turned-off current [15] and energy storage to be able to control the power flow. The capacitor also reduces the voltage ripple on the dc side. Ac filters prevent the voltage harmonics entering the ac system. New type of dc cables is used in VSC-HVDC applications, where the insulation is made of an extruded polymer that is particularly resistant to dc voltage. Polymeric cables are the preferred choice for HVDC, mainly because of their mechanical strength, flexibility, and low weight [2]**.**

VSC on the ac side acts as a constant current source and therefore requires an inductor as its energy storage device. A small ac filter for harmonics elimination is also required on the ac side. On the dc side VSC acts as a constant voltage source and it requires a capacitor as its energy storage device. Energy storage capacitor here provides dc filtering capability. When compared to classic HVDC that are based on CSC, VSC-based HVDC has relatively high switching losses, but by using a soft-switching commutation scheme, the switching losses are considerably reduced [8]**.**

The transfer of power in the case of VSC-based HVDC transmission systems is controlled in the same way as in the case of classic HVDC transmission. The inverter side controls the active power, while the rectifier side controls the dc voltage [16]**.** The control system of the VSC-based HVDC is realized by using a fast inner current control loop and several outer control loops, depending on the application [17]**.**

The control system of VSC-HVDC has at its base level a fast inner current control loop that controls the ac currents. The ac current references are provided by the outer controllers [17]**.** The slower outer controllers include the dc voltage controller, the ac voltage controller, the active power controller, the reactive power controller and the frequency controller. Thus, the reference of the active current can be obtained from the dc voltage controller, from the active

power controller or from the frequency controller. On the other hand, the reference of the reactive current can be derived from the reactive power controller or from the ac voltage controller [15].

The most relevant components of the HVDC system are the following:

- The thyristor or IGBT valves that realize the conversion from ac to dc and thus are the main components of any HVDC converter;
- The converter transformers transform the voltage level of the ac busbar to the required entry voltage level of the converter;
- The smoothing reactor, which has the main functions of prevention of the discontinuous current, limitation of the dc fault currents and prevention of resonance in the dc circuits;
- The ac harmonic filters, which absorb harmonic currents generated by the HVDC converter and supply reactive power;
- Dc transmission circuit consisting of dc transmission line, cable, dc switches and earth electrode.

2.5. Capacitor configuration

Since the master thesis is oriented on the reduction of dc-link capacitance, basic capacitor theory will be briefly described.

Capacitors are one of the standard components in electronic circuits and are widely used in many ac and dc power system applications. Capacitors store energy by stockpiling positive and negative charges on plates that are separated by an insulating dielectric.

With two factors the application of energy storage technology can be characterized. First of all, the amount of energy that can be stored in the device. Secondly, the speed rate at which the energy can be transferred into or out of the storage device. This depends mainly on the peak power rating of the power conversion unit [18].

As shown in equation (2.1) the capacitance *C* in capacitor represents the relationship between stored charge *(q)* and the voltage between the plates (*V)*. The capacitance depends on the permittivity of the dielectric *(ε)*, the area of the plates *(A)* and the distance between the plates *(d)*, equation (2.2).

$$q = CV \tag{2.1}$$

$$C = \frac{\varepsilon A}{d} \tag{2.2}$$

Equation (2.3) shows that the energy stored in the capacitor depends on the square of the voltage and the capacitance [18].

$$W = \frac{1}{2} C V^2 \tag{2.3}$$

$$dV = i \cdot \frac{dt}{C_{tot}} + i \cdot R_{tot} \tag{2.4}$$

The amount of energy that a capacitor is capable to store can be increased by increasing the capacitance or the peak voltage rating of the capacitor.

The total voltage change when charging or discharging capacitors is shown in equation (2.4). It is important that C_{tot} and R_{tot} are the result from a combined series/parallel configuration of capacitor cells to increase the total capacitance and the voltage level [18]**.** The C_{tot} R_{tot} defines the response time of the capacitor for charging or discharging.

2.6. Dc-link configuration

During disturbances in the ac system large power oscillations may occur between the ac and the dc side. This will lead to oscillations in the dc voltage and dc over-voltages that may stress the IGBT valves.

The capacitor is a major factor limiting the lifetime of the inverter. Though, it is possible to reduce the costs and volume of the inverter by reducing the total dc-link capacitance. On the other hand, small capacitance leads to large voltage fluctuations in the dc-link voltage and consequently can cause semiconductor switch breakdown [18].

2.6.1. Dc-link model

The model of the dc-link can be characterized by equation (2.5):

$$\frac{C U_{dc}}{dt} = i_{dc} - i_L \tag{2.5}$$

where i_{dc} is dc-link current and $i_L = \frac{U_{dc}}{R_L}$ where R_L is load resistance.

The equivalent dc-link model is shown in Figure 2.7.

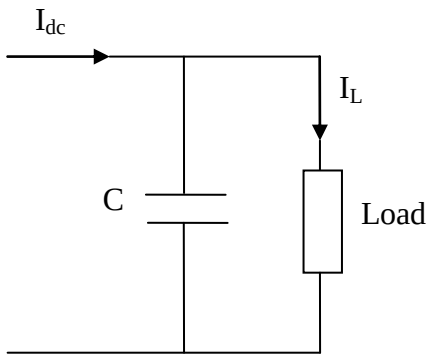


Figure 2.7. Dc-link model

According to figure 2.6 it is observed that the dc-link is connected across the load. As was already presented in Figure 2.6, two capacitors of the same power rating appear on the dc side. The VSC that is also shown in Figure 2.6 operates as a rectifier where the power flows to the dc-link. During the operation, dc-link voltage regulation is achieved by means of controlling the energy stored in the dc-link capacitor.

3. CONTROL STRATEGY OF VSC-HVDC

3.1. Introduction

In the case of VSC-based HVDC transmission systems the transfer of power is controlled in the same way as in the case of a classic HVDC transmission. The inverter side controls the active power, while the rectifier side controls the dc voltage [8]. With classic HVDC the reactive power cannot be controlled independently of the active power. VSC-HVDC makes it possible to control the reactive power and the active power independently. The reactive power flow can be controlled separately in each converter by the ac voltage that is requested or set manually without changing the dc voltage. The active power flow can be controlled by dc voltage on the dc side or the variation of frequency of ac side, or set manually. Thus, the active power flow, the reactive power flow, the ac voltage, the dc voltage and the frequency can be controlled when using VSC-HVDC. Figure 3.1 represents the overall control structure of the VSC-HVDC transmission system.

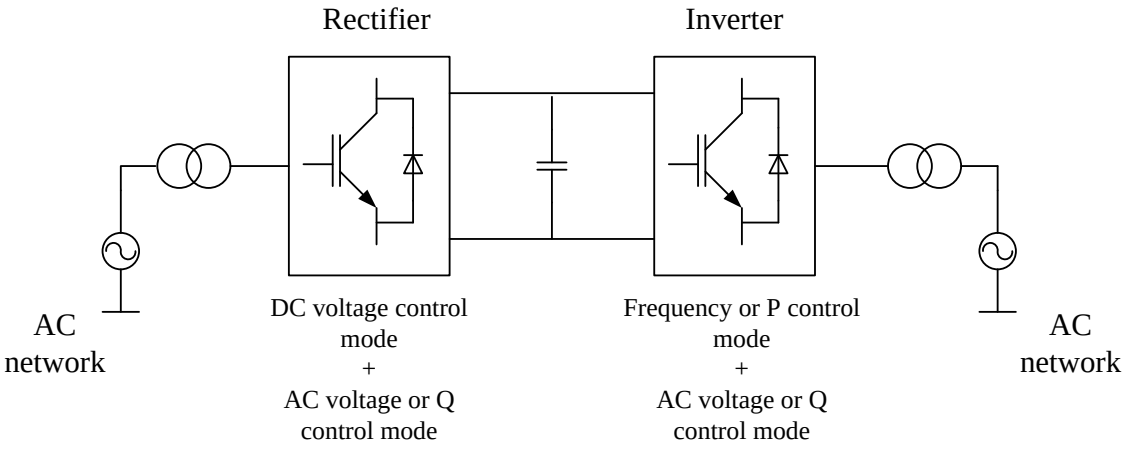


Figure 3.1. Overall control structure of the VSC-HVDC transmission system

3.2. Operation of VSC-HVDC

The VSC-HVDC system is based on self-commutated PWM technique. PWM generates pulse-width modulated signal by comparing the instantaneous magnitude of a triangular waveform with sinusoidal input reference. This is shown in Figure 3.2.

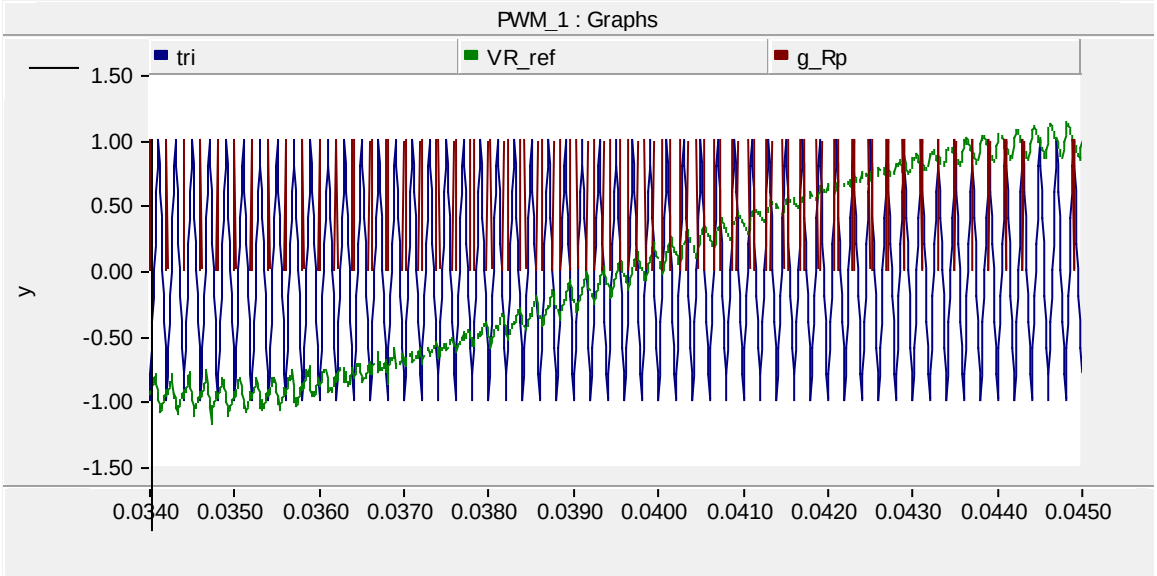


Figure 3.2. Sinusoidal PWM technique

Thus, the VSC can produce its own voltage waveform independent of the ac system. PWM controls the average output voltage during a very short period, which is called switching period. PWM technique uses a sinusoidal reference signal and produces the desired output voltage. The independent control of active and reactive power can be achieved by means of PWM template that can be changed almost instantly. Changing the fundamental frequency voltage phase angle across the series reactor controls the power, whereas changing the fundamental frequency voltage magnitude across the series reactor controls the reactive power [1]. Two VSC converters are connected together in back-to back configuration forming a transmission link is shown in Figure 3.3.

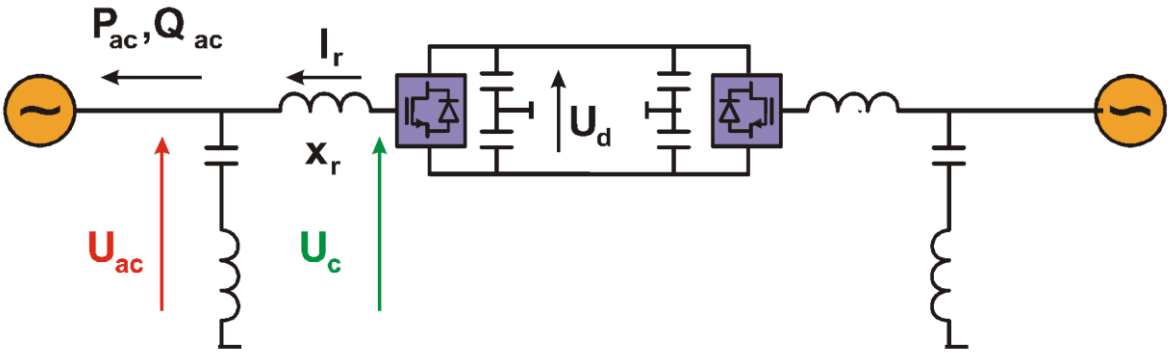


Figure 3.3. Single line diagram for VSC-HVDC link [1]

By implementing the PWM technique each converter can be controlled in all four quadrants of Figure 3.4 while the constant dc voltage is maintained. Reactive power on every

terminal can be controlled by regulating ac voltage independently of transmission power level or voltage rating of the converters [1].

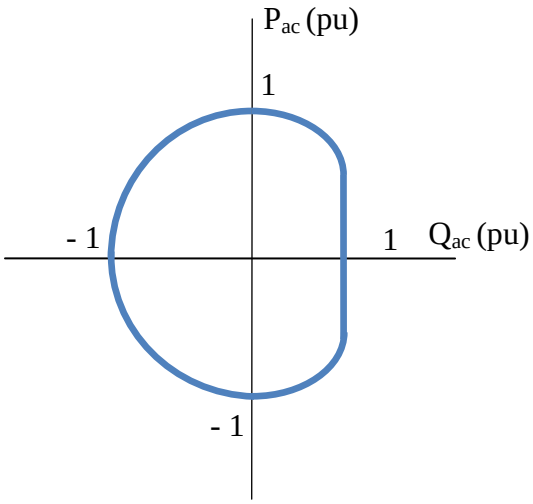


Figure 3.4. Typical P-Q diagram of VSC-HVDC transmission

Different control strategies of VSC-HVDC are known. One way to control VSC-based HVDC converters is power-angle control, which is also called voltage-angle control. It is perhaps the most straightforward controller for grid-connected VSCs [19], another widely used method of VSC-HVDC control is vector control.

3.2.1. The principle of power-angle control

The principle of power-angle control is based on the equations:

$$P = \frac{U_1 U_2 \sin\theta}{X} \qquad (3.1)$$

$$Q = \frac{U_1^2 - U_1 U_2 \cos\theta}{X}$$

where P and Q is the active and reactive power in the ac system with voltage magnitudes U_1 and U_2 between two electrical nodes. The variables θ and X are the phase-angle difference and line reactance between the two nodes respectively [19]. Following equation (3.1) it is straightforward that the active power is mainly associated with the phase angle θ, while the reactive power is more associated with the voltage-magnitude difference. The provided mathematical relationships are the base of power-angle control. Thus, the active power is controlled by adjusting the voltage

phase angle of the VSC. Similarly, the reactive power is controlled by varying the voltage magnitude of the VSC. Despite the fact that power-angle control seems to be simple and beneficial, it has never been used in any existing VSC-HVDC systems since it has several severe drawbacks:

- The controller bandwidth is seriously limited;
- The control system is not able to limit the valve current of the converter.

The latter is a severe problem, since the VSC-HVDC converters usually do not provide an over-current protection feature. Thus, it is vital for the control system to be able to limit the valve current in order to prevent the converters from being tripped during perturbations [19].

3.3. Vector control principle

Vector current control is the most popular control method used for VSC-based HVDCs. The basic principle of the vector current controlled VSC is to control instantaneous active and reactive grid currents independent of each other [20]**.** The vector control scheme is shown in Figure 3.5.

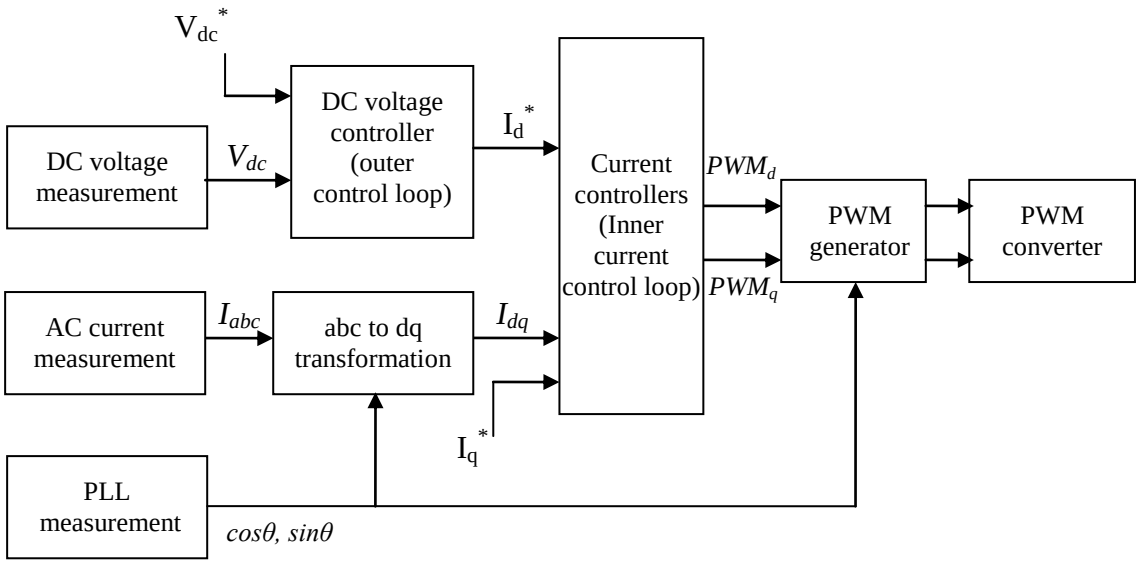


Figure 3.5. Vector control principle[21]

By utilizing synchronously rotating *dq* reference frame independent active and reactive power control is possible. Initially, system currents and voltages are described as vectors in a stationary $\alpha\beta$ reference frame, then they are transformed to the rotating *dq* coordinate system.

The transformation to *dq* coordinates is done as follows. Three-phase components *xa(t), xb(t)* and *xc(t)* are first described as two vectors in the *αβ* reference frame Figure 3.6 using Clark transformation:

$$\begin{bmatrix} x_\alpha(t) \\ x_\beta(t) \end{bmatrix} = \begin{bmatrix} \sqrt{\frac{2}{3}} & -\frac{1}{\sqrt{6}} & -\frac{1}{\sqrt{6}} \\ 0 & \frac{1}{\sqrt{2}} & -\frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} x_a(t) \\ x_b(t) \\ x_c(t) \end{bmatrix} \tag{3.2}$$

where k is a constant koeficient.

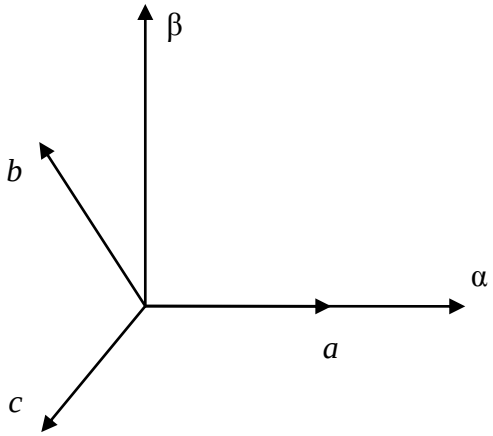


Figure 3.6. Stationary *abc* and αβ reference frames

Using a Park transformation, the transformation from *αβ* frame to *dq* can be written as:

$$X_{dq} = X_{\alpha\beta} e^{-j\theta} \tag{3.3}$$

The vectors *xα*(*t*) and *xβ*(*t*) are rotating with the angular frequency *ω*(*t*), which is the angular frequency of the grid voltage in rad/s. Let *θ*(*t*) be the angle defined by integrating *ω*(*t*) [10]. Then the expanded matrix form of Park transformation is obtained as:

$$\begin{bmatrix} x_d(t) \\ x_q(t) \end{bmatrix} = \begin{bmatrix} \cos(\theta(t)) & \sin(\theta(t)) \\ -\sin(\theta(t)) & \cos(\theta(t)) \end{bmatrix} \begin{bmatrix} x_\alpha(t) \\ x_\beta(t) \end{bmatrix}. \tag{3.4}$$

Vectors *xd*(*t*) and *xq*(*t*) represent currents, where *xd*(*t*) is the current which gives required power to the dc bus and *xq*(*t*) is the current which defines the reactive power condition. This transformation gives excellent controlling possibilities. A correct transformation requires an exact value of the angle $\theta(t)$ to decouple the components for independent power control. The angle θ is given as:

$$\theta = \tan^{-1}\left(\frac{v_\beta}{v_\alpha}\right) \tag{3.5}$$

where $v\alpha$ and $v\beta$ are voltage components in the $\alpha\beta$ reference frame. The value of the angle θ is computed by using a synchronization technique, namely, phase-locked loop (PLL) [22]. The phase-locked loop is used to synchronize the turning on/off of the power devices, calculate and control the flow of active/reactive power by transforming the feedback variables to a reference frame suitable for control purposes [21].

The fundamental current and voltage components become dc variables and PI controllers are needed to reduce the steady-state errors [20]**.** The reference voltage components from the PI controller are transformed back to 3-phase values and used as inputs to the PWM. The vector control system is based on inner and outer control loops. The inner loop controls the power between the dc-link and the grid, while the outer loop controls the dc voltage of the load.

3.4. Dynamic model of VSC-HVDC

Schematic representation of the system is shown in Figure 3.7.

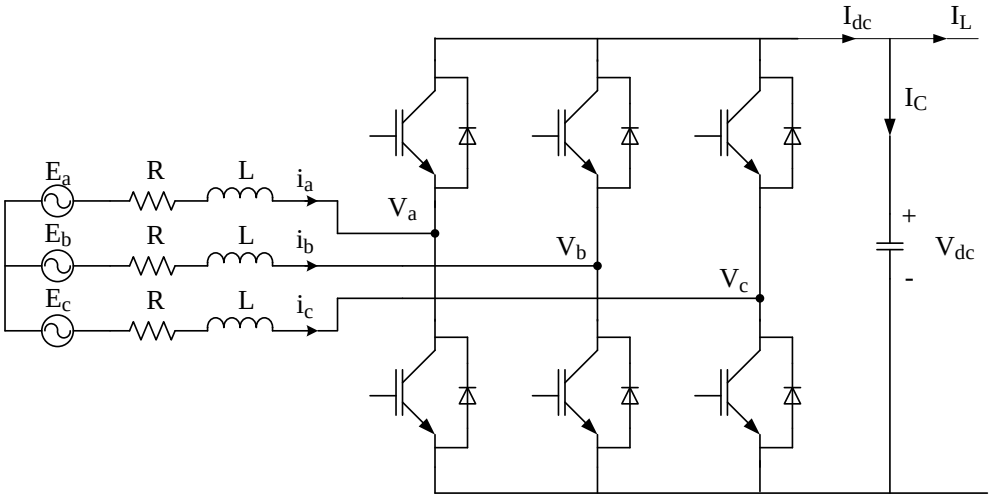


Figure 3.7. Schematic representation of the VSC-HVDC system

To analyze the system connected to the grid in Figure 3.7, standard Kirchoff's voltage law is used, thus the voltage at the grid side of the converter can be described as:

$$E_{abc} = L\frac{d}{dt}i_{abc} + v_{abc} + Ri_{abc} \tag{3.6}$$

where v_{abc} are converter input voltages, while i_{abc} are grid currents, E_{abc} are grid voltages, R and L are resistance and inductance respectively between the converter and the grid.

Three-phase currents and voltages are transformed in *dq* reference frame by means of *abc* to *dq* transformation, where ω is the system frequency in rad/s.

$$\begin{vmatrix} E_d \\ E_q \end{vmatrix} = L\frac{d}{dt}\begin{vmatrix} i_d \\ i_q \end{vmatrix} + \omega L \begin{vmatrix} 0 & -1 \\ -1 & 0 \end{vmatrix}\begin{vmatrix} i_d \\ i_q \end{vmatrix} + R\begin{vmatrix} i_d \\ i_q \end{vmatrix} + \begin{vmatrix} v_d \\ v_q \end{vmatrix} \tag{3.7}$$

After the transformation in *dq* reference frame, the voltage equations are

$$\begin{aligned} E_d &= L\frac{d}{dt}i_d - \omega L i_q + v_d + Ri_d \\ E_q &= L\frac{d}{dt}i_q + \omega L i_d + v_q + Ri_q \end{aligned} \tag{3.8}$$

It can be observed that the d- and q-axes are decupled, they are only related to each other by means of $\omega L i_q$ and $\omega L i_d$ terms.

The power exchange in *dq* reference frame is given by

$$P_{dq} = \frac{3}{2}(v_d i_d + v_q i_q) \tag{3.9}$$

During a steady-state operation the power exchange at the dc side will be equal to the power at the ac side. From equation (3.9):

$$P_{dq} = P_{dc} = V_{dc} \cdot I_{dc} \tag{3.10}$$

Following the previous equation (3.10), the dc current in steady-state is:

$$I_{dc} = \frac{P_{dq}}{V_{dc}} = \frac{3(v_d i_d + v_q i_q)}{2V_{dc}} \tag{3.11}$$

3.5. Per-unit representation

The per-unit system simplifies the analysis of complex power systems by choosing a common set of base parameters. It is also ideal for computer simulations and design of controllers of the VSC-HVDC.

The per-unit system is based on nameplate rated values for power, phase current and voltage [23]. The determination of any quantity in the per-unit system is

$$Quantity\ (per\ unit) = \frac{Quantity\ (normal\ units)}{Base\ value\ of\ quantity\ (normal\ units)}$$

The base quantities used for per-unit conversion are given below.

$$\begin{aligned}
&V_{d,b} = V_{q,b} = \sqrt{\frac{3}{2}} V_n \\
&I_{d,b} = I_{q,b} = \sqrt{2} \cdot I_n \\
&Z_{d,b} = \frac{V_{d,b}}{I_{d,b}} = \frac{V_n}{\sqrt{3} \cdot I_n} = Z_n \\
&S_{d,b} = \frac{2}{3} S_n \\
&S_{DC} = S_n = \sqrt{3} V_n I_n = \frac{3}{2} V_{d,b} I_{d,b} \\
&I_{DC} = \frac{S_{DC}}{V_{DC,b}} = \frac{3}{4} I_{d,b} = \frac{3\sqrt{2}}{4} I_n \\
&Z_{DC,b} = \frac{V_{DC,b}}{I_{DC,b}} = \frac{8}{3} Z_{d,b} = \frac{8}{3} Z_n ,
\end{aligned} \tag{3.12}$$

where

$V_{d,b}$ and $V_{q,b}$ are representation of voltages in the *dq* coordinates;

$I_{d,b}$ and $I_{q,b}$ are representation of currents in the *dq* coordinates;

V_n, I_n, Z_n and S_n are rated voltage, current, impedance and apparent power respectively;

S_{DC}, I_{DC}, V_{DC} and Z_{DC} are apparent power, current, voltage and impedance of the dc side respectively.

3.6. Phase-locked loop

A very important and necessary feature of grid side converter control is the grid synchronization. The synchronization algorithm is able to detect the phase angle of grid voltage in order to synchronize the delivered power. The purpose of this method is to synchronize the inverter output current with the grid voltage, in order to obtain a unity power factor.

The inputs of the PLL model are the three phase voltages measured on the grid side and the output is the tracked phase angle. The PLL model is implemented in synchronous *dq* reference frame, where a Park transformation is used. The phase-locking of the system is realized by adjusting the q-axis voltage to zero. A PI controller is used for this purpose. By integrating the sum between the PI output and the reference frequency the phase angle is obtained.

3.6.1. Inner control loop

The inner controller or current controller as input takes the error between the reference current and measured current. This error is carried through the PI regulator and the decoupling terms from (3.8) are compensated by feed-forward. As a result the desired converter voltage in dq reference frame is obtained.

The feed-forward is used to minimize disadvantage of slow dynamic response of cascade control. As the reference values of the inner loop variables are often available, these are fed forward for a faster and safer operation.

The structure of the inner current controller is presented in Figure 3.8.

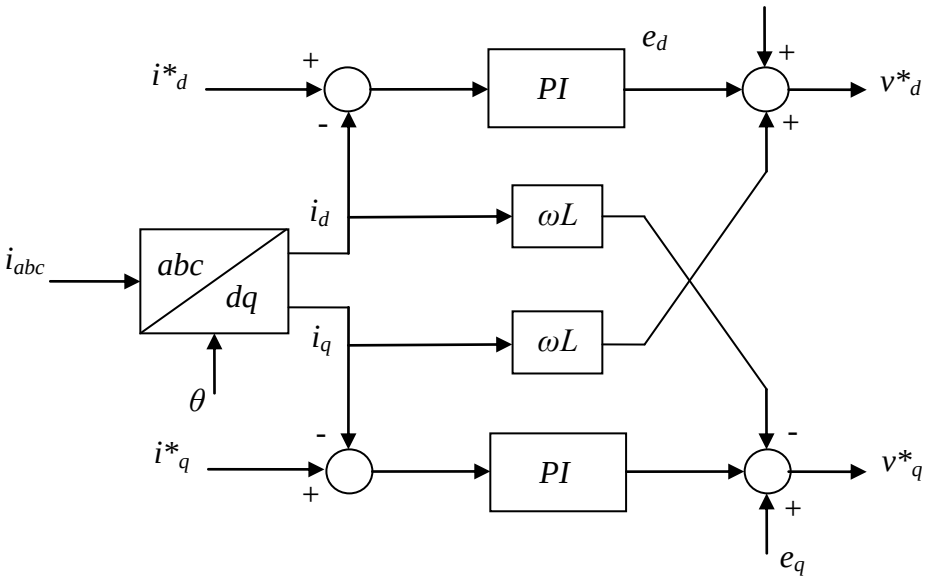


Figure 3.8. The structure of the inner current controller

The controller in Figure 3.8 consists of two PI regulators, for *q* and *d* axis respectively.

3.7. The outer controller

Common objectives for the outer loop active power through the converter, reactive power at each side and dc-link voltage. Active current (i_d) is used to control active power flow or dc voltage level. Similarly, reactive current (i_q) is used to control reactive power flow into stiff grid connection. The outer controller block diagram is shown in Figure 3.11.

3.8. Dc voltage control using classic control algorithm

Dimensioning of the dc-link voltage controller is determined by the transfer function between the defined current reference value and the dc-link voltage.

From power balance of the VSC-HVDC terminal

$$P_{ac} + P_{dc} + P_{cap} = 0 \tag{3.13}$$

$$\frac{3}{2} V_d i_d + V_{dc} I_{dc} + V_{dc} i_{cap} = 0 \tag{3.14}$$

where I_{dc} and i_{cap} are the dc bus current and the capacitor current respectively, and 3/2 factor comes from the Park's transformation.
From (3.14) the current through the capacitor is

$$i_{cap} = -\left(\frac{3V_d i_d}{2V_{dc}} + I_{dc}\right). \tag{3.15}$$

And the same current in terms of voltage across the capacitor is given by

$$i_{cap} = C\frac{dV_{dc}}{dt}. \tag{3.16}$$

From equations (3.15) and (3.16) the differential equation for the dc voltage becomes

$$\frac{dV_{dc}}{dt} = -\frac{3V_d i_d}{2CV_{dc}}\left(i_d + \frac{2V_{dc}I_{dc}}{3V_d}\right). \quad (3.17)$$

Equation (3.17) shows that dc voltage is regulated by controlling the active current i_d. The I_{dc} term from the equation (3.17) is compensated by feed-forward in the dc voltage controller. The dc voltage control block diagram is presented below.

From equation (3.16) the following block diagram seen in Figure 3.9 is obtained.

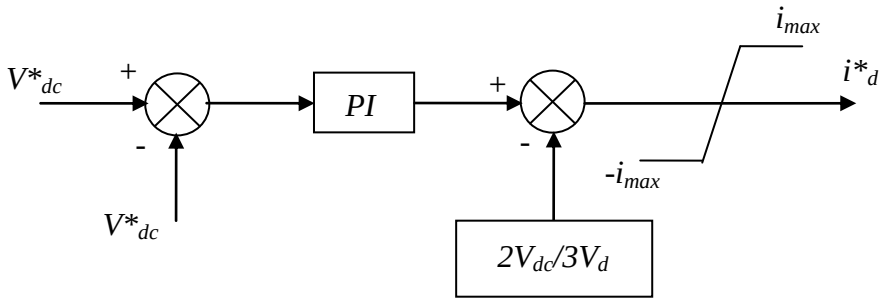


Figure 3.9. Dc voltage regulator block diagram

3.9. Active and reactive power controllers

The per-unit representation of active and reactive power of the system in *dq* transformation can be written as

$$p_{pu} = v_{d\,pu} i_{d\,pu} \quad (3.17)$$
$$q_{pu} = -v_{q\,pu} i_{q\,pu}.$$

More accurate active and reactive power control is achieved if using PI controllers a feedback loop is employed. Active and reactive power control loops are shown in Figure 3.10.

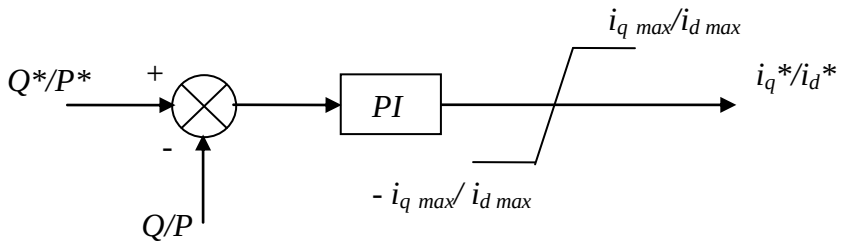


Figure 3.10. Block diagram of active power control in per-unit

3.10. Control loop transfer functions

Initially, the open loop transfer functions of each control scheme must be determined prior to specifying the parameters of PI controllers. In order to realize this, the equivalent Laplace transformation of the physical systems must be identified. Linearized differential equation of the respective state variable is used to derive the transfer function of the system.

With respect to outer control loop, the total time delay of an inner loop is approximately the sum of all the particular delays in the inner loop.

3.10.1. Transfer function of inner current loop

After eliminating the feed-forward elements the open loop transfer function of the inner current loop is as follows

$$G_{O.L.} = K_p\left(\frac{1+T_i s}{T_i s}\right)\left(\frac{1}{1+T_{eq}s}\right)\cdot\frac{1}{r}\left(\frac{1}{1+\tau s}\right), \tag{3.18}$$

where $\tau = L/r$.

Figure 3.13 presents the inner current loop block diagram in *dq* reference frame.

3.10.2. Transfer function of dc voltage control loop

The block diagram of the dc voltage control loop using conventional control method is shown in Figure 3.11.

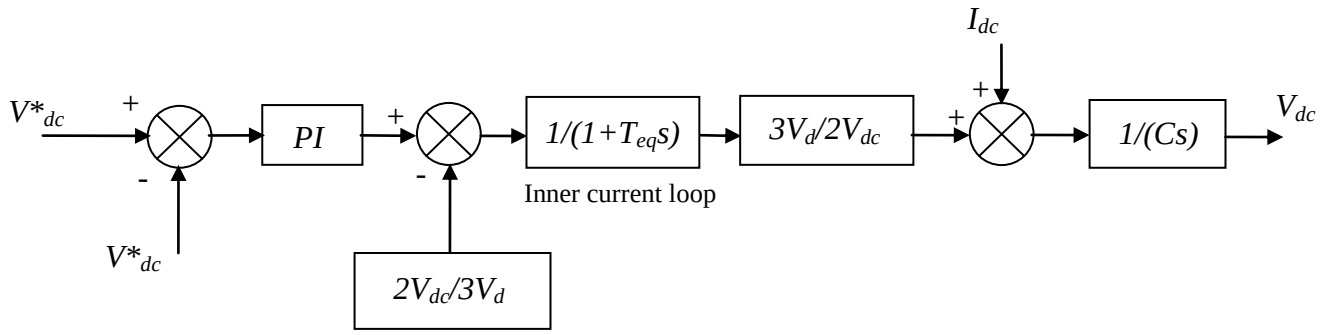


Figure 3.11. Closed loop control diagram of dc voltage controller

Initially, constant disturbances are neglected and the open loop transfer function thus becomes

$$G_{O.L.} = K_p\left(\frac{1+T_i s}{T_i s}\right)\left(\frac{1}{1+T_{eq}s}\right)\cdot\frac{3v_d}{2V_{dc}}\cdot\frac{1}{Cs}\ , \qquad (3.19)$$

where T_{eq} is the time delay in the current control loop.

3.11. Tuning of PI controllers

In order to achieve the optimal performance of the control loops the PI controllers must be properly tuned. The fundamental objectives of PI tuning are as follows:

- fast response of the system by means of increasing the cut-off frequency as high as possible;
- small overshoot and good damping of oscillations.

To optimize the speed of response and system stability, modulus optimum and symmetrical optimum techniques are applied depending on the form of the open loop transfer function of the control loop [24].

If the system contains plants with low order (< 3) transfer functions then modulus optimum technique is used. The objective is to make the cut-off frequency as high as possible. Hence, when there is one dominant and another minor pole in the transfer function, the integral time constant of the PI controller is chosen to cancel out the dominant pole. When one pole of the open loop transfer function is near origin or at the origin itself, the modulus optimum criterion is not suitable. Instead, symmetrical optimum criterion is used for tuning the PI controllers. This method has an advantage of enhanced phase margin [24].

3.11.1. **Tuning of current controller using Modulus Optimum**

The modulus optimum criterion is applied in the tuning process of the inner controller. It is tuned using the theory in Appendix A and [21].

The results from modulus optimum criterion for the inner controller give

$$K_p = \frac{\tau_{pu} r_{pu}}{2T_a} \tag{3.20}$$

$$T_i = \frac{L_{pu}}{\omega_b r_{pu}} \tag{3.21}$$

where T_i and K_p is the integration time and the proportional gain of the PI regulator, L_{pu} and r_{pu} are the per-unit inductance and resistance between the converter and grid Figure 3.7, τ is a time constant of 5 ms, base frequency ω_b= 314.16 and T_a is the first order time delay converter

$$T_a = \frac{1}{2f_s} \tag{3.22}$$

where f_s is the switching frequency of PWM.

After utilizing all elements, the control parameters are

$$K_p = 4$$

$$T_i = 0.013$$

Figure 3.12 presents the inner current loop block diagram in *dq* reference frame.

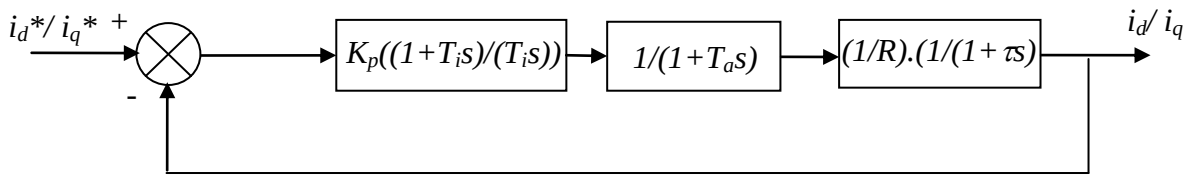


Figure 3.12. Inner current loop control block diagram in *dq* coordinates

3.11.2. Tuning of classic dc voltage controller using Symmetrical Optimum

The dc- link controller is tuned by using the symmetrical optimum tuning criteria applied in Appendix B and [21]. This gives the following values for the gain and integration constants

$$T_v = a^2 T_{eq} \tag{3.23}$$

$$K_v = \frac{T_c}{aK \cdot T_{eq}} \tag{3.24}$$

where the subscript '*v*' means the voltage controller.

T_{eq} is the first order time constant of the inner (current) control loop, $T_c=1/\omega_b C_{pu}$, K is $V_{d,pu}/V_{dc,pu}$ and is equal to *1 pu* during the normal operation, and a is a degree of freedom in the controller, recommended value of a is between 2 and 4 in literature [25], here $a = 3$ is used.

The control parameters are

$$T_v = 0.0018$$

$$K_v = 10.67$$

Closed loop control diagram of dc voltage controller is shown in Figure 3.12.

3.12. Dc-link voltage control using power balance principle

3.12.1. Introduction

The most important ability of the back-to-back converter is to enable fast control of the power flow. The fluctuations in the dc-link power can be avoided if the rectifier side dc-link power and the inverter side dc-link power in a PWM rectifier-inverter system are equalized [26]. As a consequence the current at the inverter input will not be distorted. But replacing the large dc-link capacitor with a small one introduces a drawback of the inverter output current distortion by low order harmonics. The avoidance of the large energy storage element in the VSC increases the risk of dc voltage fluctuation with a frequency six times of the supply voltage. In addition, the ripple in the dc-link voltage might increase if the supply voltage is distorted by low order harmonics or unbalance. The standard solution for power system is to install the aluminum electrolytic capacitors as the energy storage element. In some high power or high voltage motor drives applications electrolytic capacitors are considered as poor and inappropriate solution due to size, weight, cost and reliability [10]. The latter is probably the most important issue among others mentioned above. Due to continuous out-gassing, the properties of the electrolytic capacitors deteriorate gradually with time. Hence, the capacitor is the major weakness point

limiting the lifetime of inverter systems. The reliability of the VSC may increase though if the film capacitors are used instead of electrolytic [27].

By reducing the dc-link capacitor size a reduction in cost and volume of the inverter can be achieved. However, as already mentioned previously a small dc-link capacitance leads to a large voltage fluctuation in the dc-link voltage, and hence can cause semiconductor switch breakdown. The conventional dc-link voltage control algorithm was already introduced in the previous chapters. The drawback of this method is that the inverter power dynamics are not considered directly and as a result large dc-link voltage variations occur, especially in the case when the system is connected to the weak grid. The vital point of the proposed algorithm is to involve the inverter dynamics in the rectifier control. Since the rectifier operates with the knowledge of inverter operating status this method has the potential of faster response. Consequently, it is possible to control the rectifier current so that the inverter is supplied with exact amount of required current. Hence, the dc-link voltage does not fluctuate even though a fairly small capacitance is utilized due to the fact that no current flows into the dc-link capacitor.

3.12.2. Power dynamics of inverter

The equations appearing in this section are derived analytically. Only the basic equations were available prior to beginning this section. A schematic representation of the inverter side with the single capacitor bank is shown in Figure 3.13. If the power balance between inverter and rectifier $P_{rect} = P_{inv}$ is achieved, then the stored energy in the dc-link will not vary.

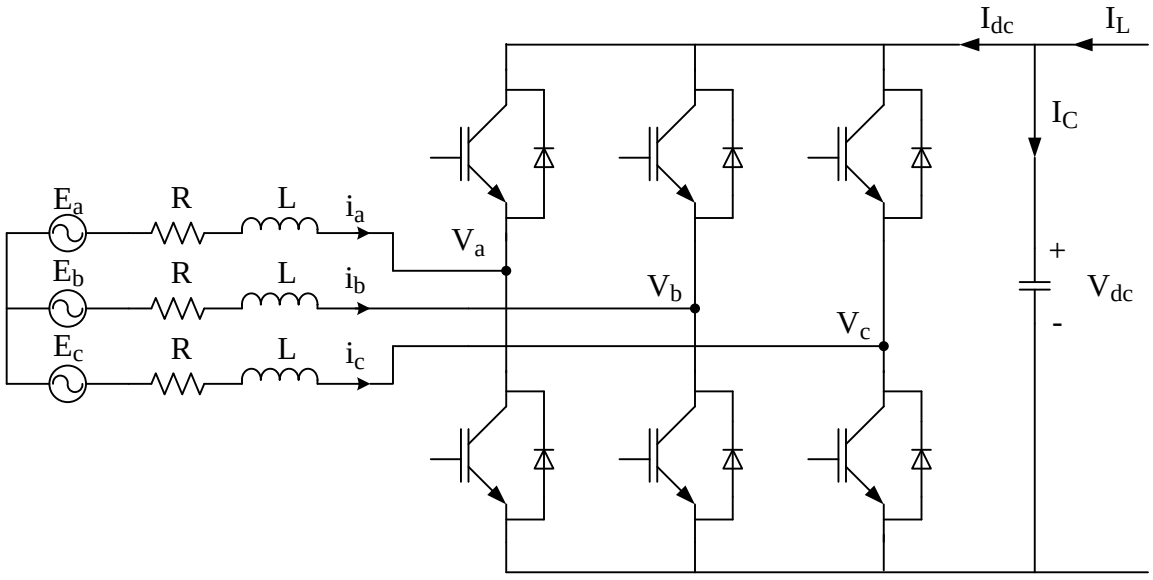


Figure 3.13. Schematic representation of the inverter side

To analyze inverter side behavior connected to the grid in Figure 3.13, the voltage at the grid side of the inverter can be described as

$$E_{abc} = -L\frac{d}{dt}i_{abc} + v_{abc} - Ri_{abc} \tag{3.25}$$

where $E_{abc} = [E_a, E_b, E_c]^T$ are the grid voltages, $i_{abc} = [i_a, i_b, i_c]^T$ are the source currents, L and R are inductance and resistance between converter and grid respectively, v_{abc} are converter input voltages.

After the transformation in *dq* reference frame, the voltage equations are

$$\begin{aligned} v_d &= L\frac{d}{dt}i_d - \omega L i_q + E_d + Ri_d \\ v_q &= L\frac{d}{dt}i_q + \omega L i_d + E_q + Ri_q \end{aligned} \tag{3.26}$$

Using inverter side voltage and current variables (Figure 3.13), the time derivatives of the inverter power and the power dynamics of the inverter are derived.

The derivative of d and q axes line currents

$$\frac{d}{dt}i_d = -\frac{R}{L}i_d + \omega i_q + \frac{V_d}{L} - \frac{E_d}{L} \tag{3.27}$$

$$\frac{d}{dt}i_q = -\frac{R}{L}i_d - \omega i_q - \frac{V_d}{L} + \frac{E_d}{L} \tag{3.28}$$

The *d* and *q* axes inverter terminal voltages,

$$\begin{aligned} v_d &= E_d - \omega i_q + K_p(i_d^* - i_d) + T_i\int_0^t e_d\,dt \\ v_q &= E_q + \omega i_q + K_p\left(i_q^* - i_q\right) + T_i\int_0^t e_q\,dt \end{aligned} \tag{3.29}$$

where K_p and T_i are proportional gain and integral time coefficients of the PI regulator respectively; $e_d = i_d^* - i_d$ and $e_q = i_q^* - i_q$ are dq axes current errors; i_d^* and i_q^* are current reference values.

The power from the dc-link to inverter is given by,

$$P_{inv} \equiv \frac{3}{2}\left(i_d v_d + i_q v_q\right), \tag{3.30}$$

where $i_d v_d$ and $i_q v_q$ are currents and voltages in dq coordinates.

From (3.27) – (3.30), the dynamics of the inverter are obtained as follows,

$$\frac{d}{dt}P_{inv} = \frac{3}{2}\left(\frac{d}{dt}i_d v_d + \frac{d}{dt}i_q v_q + i_d\frac{d}{dt}v_d + i_q\frac{d}{dt}v_q\right). \tag{3.31}$$

After implementing equations from (3.50) to (3.52)

$$\frac{d}{dt}P_{inv} = \frac{3}{2}\left(\frac{d}{dt}i_d v_d + \frac{d}{dt}i_q v_q + i_d\frac{d}{dt}v_d + i_q\frac{d}{dt}v_q\right)$$

$$= \frac{3}{2}\left[v_d\left(-\frac{R}{L}i_d + \omega i_q + \frac{v_d}{L} - \frac{E_d}{L}\right) + v_q\left(-\frac{R}{L}i_q - \omega i_d + \frac{v_q}{L} - \frac{E_q}{L}\right)\right.$$

$$\left. + i_d\left(-\omega\frac{d}{dt}i_q + T_i e_d + K_p\frac{d}{dt}i_d\right) + i_q\left(\omega\frac{d}{dt}i_d + T_i e_q + K_p\frac{d}{dt}i_q\right)\right]$$

$$= \frac{3}{2}\left[v_d\left(-\frac{R}{L}i_d + \omega i_q + \frac{v_d}{L} - \frac{E_d}{L}\right) + v_q\left(-\frac{R}{L}i_q - \omega i_d + \frac{v_q}{L} - \frac{E_q}{L}\right)\right.$$

$$+ i_d\left(-\omega\left(-\frac{R}{L}i_q - \omega i_d + \frac{v_q}{L} - \frac{E_q}{L}\right) + T_i e_d + K_p\left(-\frac{R}{L}i_d + \omega i_q + \frac{v_d}{L} - \frac{E_d}{L}\right)\right)$$

$$\left. + i_q\left(\omega\left(-\frac{R}{L}i_d + \omega i_q + \frac{v_d}{L} - \frac{E_d}{L}\right) + T_i e_q + K_p\left(-\frac{R}{L}i_q - \omega i_d + \frac{v_q}{L} - \frac{E_q}{L}\right)\right)\right];$$

After simplification the dynamics of the inverter are

$$\frac{d}{dt}P_{inv} = -\frac{R}{L}P_{inv} + \mu \tag{3.32}$$

where

$$\mu = \frac{3}{2}\left[\frac{v_d^2 + v_q^2}{L} + \left(\frac{-E_d v_d - E_q v_q}{L}\right)\right.$$
$$+ \omega\left(\left(i_q v_d - i_d v_q\right) + \omega\left(i_d^2 + i_q^2\right) - \frac{v_q i_d + v_d i_q}{L} + \frac{E_q i_d - E_d i_q}{L}\right)$$
$$\left. + T_i\left(e_d i_d + e_q i_q\right) + K_p\left(\frac{R}{L}\left(-i_d^2 - i_q^2\right) + \frac{v_d i_d + v_q i_q}{L}\right) + \left(\frac{-E_d i_d - E_q i_q}{L}\right)\right]$$

μ is a variable that is a part of the inverter dynamics. This variable is implemented in inverter side of the system and is used to provide the rectifier with updated inverter operating status to get the close communication between the rectifier and inverter. The inverter dynamics are used for the rectifier current control so that the stored energy in the dc-link capacitor can be kept constant.

3.12.3. **Rectifier power dynamics**

Choosing the dc-link voltage and line currents as a state vector, one can describe the dynamics of the rectifier

$$C\frac{d}{dt}V_{dc} = i_C \tag{3.33}$$

$$L\frac{d}{dt}i_d = \omega L i_q + E_d - v_d \tag{3.34}$$

$$L\frac{d}{dt}i_q = -\omega L i_d + E_q - v_q\ , \tag{3.35}$$

where V_{dc} and i_C denote the dc-link voltage and capacitor current respectively, E_d and E_q the d and q axes source voltages, v_d and v_q the d and q axes rectifier terminal voltages, i_d , i_q the d and q axes line currents, ω denotes the angular frequency of the source voltage and C is the capacitance of the dc-link.

Aligning the reference frame to the d axis of the source voltage $E_q = 0$ is obtained. Then the power from the source to the rectifier is given by

$$P_{rect} \equiv \frac{3}{2}\left(i_d E_d + i_q E_q\right) = \frac{3}{2} i_d E_d\ . \tag{3.36}$$

From (3.34) and (3.36) it is obtained that

$$\frac{d}{dt}P_{rect} = \frac{3}{2}i_d E_d = \frac{3}{2}\frac{E_d}{L}(E_d - v_d). \tag{3.37}$$

3.12.4. Transfer functions for power balancing

The master-slave control principle [26] is applied with the inverter power dynamics considered as a master system and the rectifier power dynamics as a slave system. It should be noted that the rectifier must exactly track the inverter power dynamics.

By utilizing (3.32) and (3.37) the inverter dynamics $G_1(s)$ and the rectifier dynamics $G2(s)$ are obtained as,

$$G_1(s) = \frac{1}{s + \left({}^{R}/_{L}\right)} \tag{3.38}$$

$$G_2(s) = \left(\frac{3E_d}{2L}\right)\frac{1}{S}. \tag{3.39}$$

Then

$$v_d(s) = E_d - \frac{2L}{3E_d}G_1(s)\mu - K(s)(P_{inv} - P_{rect}) \tag{3.40}$$

where K(s) is proportional coefficient.

The equation (3.40) implementation is a part of the control system that is shown in Figure 3.17.

3.12.5. Dc-link voltage control using the capacitor energy as a variable

A controller for the dc-link voltage regulation is developed utilizing the energy stored in the capacitor as a variable. The voltage control is obtained by controlling the energy that flows in and out of the dc-link capacitor. The energy equation is as follows

$$W = \frac{1}{2}CV_{dc}^2 \tag{3.41}$$

and consequently the power equation is

$$P_c = V_{dc}i_C \tag{3.42}$$

Then it follows that

$$\frac{dW}{dt} = C\dot{V_{dc}}V_{dc} = V_{dc}i_C = P_c \tag{3.43}$$

Using equation (3.43) Figure 3.15 is obtained.

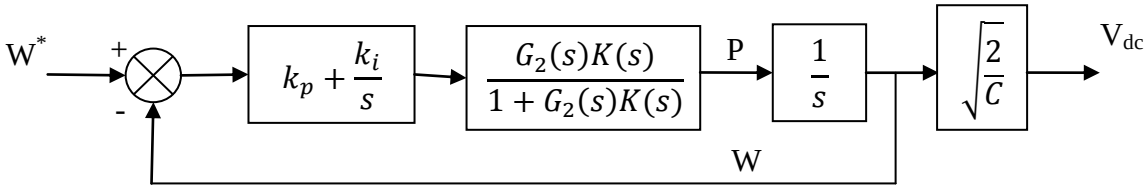


Figure 3.14. Control block diagram for dc-link voltage regulation that utilizes energy as a variable

In order to get the error between the energy and energy reference, closed loop system must be obtained

$$\frac{W(s)}{W^*(s)} = \frac{G_2(s)K(s)\left(k_p + {k_i}/{s}\right)}{[1 + G_2(s)K(s)] + G_2(s)K(s)\left(k_p + {k_i}/{s}\right)} \tag{3.44}$$

Figure 3.15 represents the block diagram for proposed converter control scheme that incorporates the inverter dynamics and utilizes the capacitor energy as a variable for the dc-link voltage regulation.

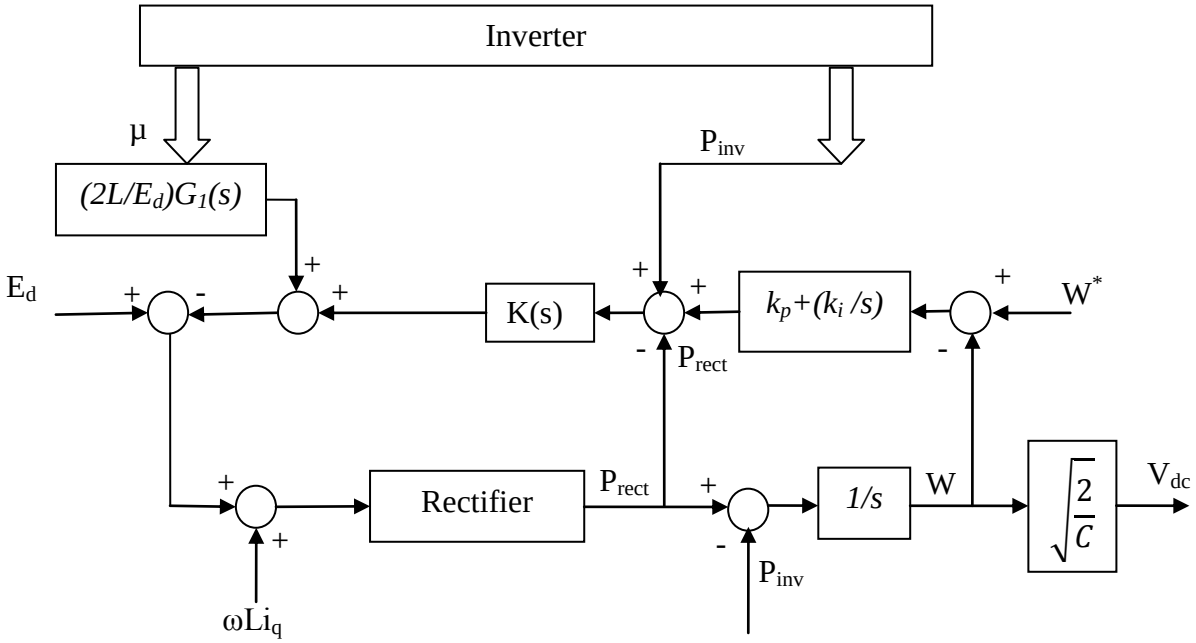


Figure 3.15. Detiled block diagram for proposed converter control scheme

Converter control block diagram is shown in Figure 3.15. The energy reference is first set and is fed into PI regulator. The output then directed to the addition/summation block. There, the rectifier power P_{rect} is substracted from the inverter power P_{inv} with the output of the PI taken into account. Later blocks represent the influence of the inverter dynamics on control system. On the block diagram, *Ed* is *d* axes source voltage and ωLi_q is the decoupling term. In order to provide the feedback of energy the rectifier power has to be first substracted from the inverter power and then dragged through the integrator block. Thus, the closed loop function is now complete.

As was previously mentioned before, the main idea of this control method is to assume constant dc-link voltage and to integrate the instantaneous power flowing into the voltage source during transitions between different power levels.

3.12.6. Reason for using the new control method

Figure 3.16 shows the block diagrams of a widely used dc-link voltage control scheme that was discussed in section 3.9.

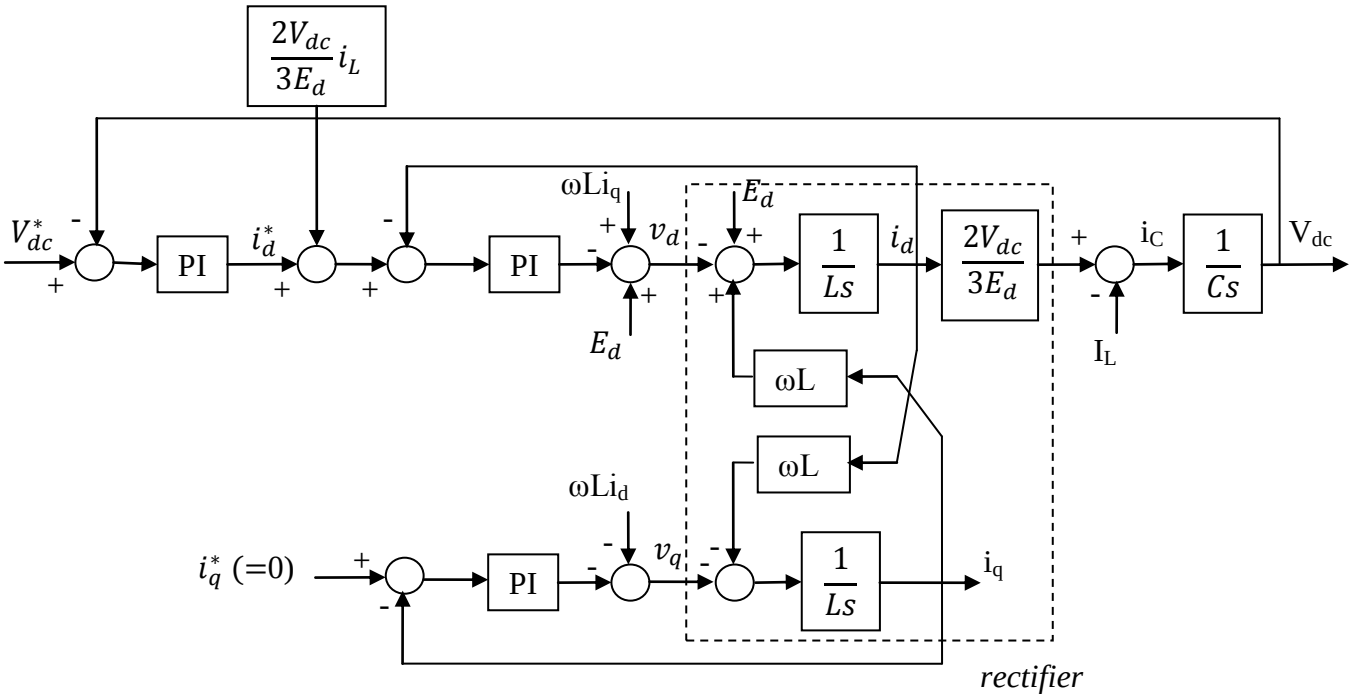


Figure 3.16. Control block diagram for the conventional dc- link control

In the conventional control algorithm, the load current compensation is obtained by injecting the feed-forward voltage term $(2V_{dc}/3E_d)i_L$ after the voltage PI regulator. Based on the power balance condition between the source and the dc-link side the compensation term can be calculated. It is worth mentioning that the dynamics of the load current i_L are not reflected in the conventional control scheme. The proposed scheme uses both $P_{inv}(t)$ and $P_{rect}(t)$ and also the derivative $\frac{d}{dt}P_{inv}(t) = G_1(s)\mu$. In other words, the inverter dynamics is utilized for the rectifier current control so that the stored energy W in the dc-link capacitor can be kept constant.

4. SIMULATIONS AND RESULTS

4.1. Introduction

This chapter is based on simulation studies of the VSC-HVDC control structures. The PSCAD/EMTDC electromagnetic transient simulation software was used for modeling of VSC-HVDC. Simulation results are expected to validate the required characteristics of the controllers discussed in the previous chapter.

4.2. Specification of the VSC

The system considered in this work is given in Figure 4.1. The HVDC system consists of two VSCs connected via a dc-link.

To study the control of dc voltage using energy as a reference two terminal VSC-HVDC was used. The control of converter VSC1 is done by using dc voltage control and reactive power control while the control of converter VSC2 is done by active and reactive power control.

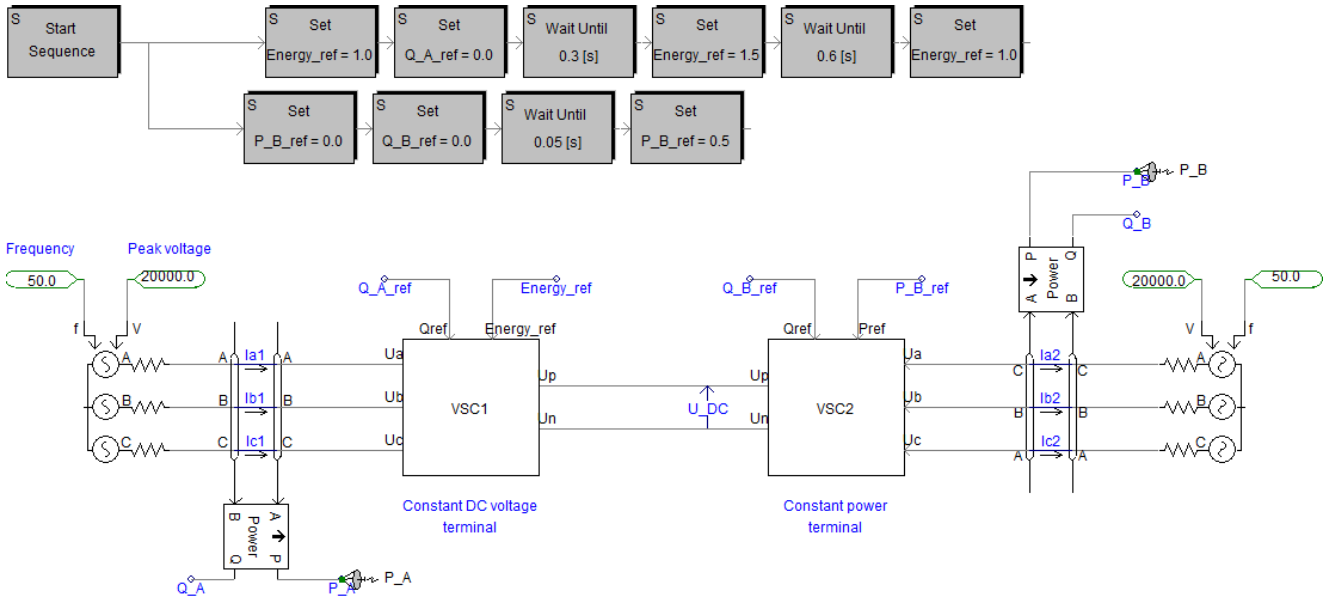


Figure 4.1. The considered test system in PSCAD/EMTDC

For simulating the transients in dc voltage, the operating energy reference was first set to 1 pu. At t = 0.3 s the dc voltage reference is increased to 1.5 pu and again reduced back to 1 pu at t = 0.6 s. All the elements are implemented in PSCAD software are used in per-unit values. A complete specification list can be observed in Table 4.1.

Table 4.1. Specifications of VSC used in the simulation

Parameters	Rating
Rated Power (S_n)	100 *MVA*
DC Voltage (U_{DC})	50 *kV*
AC Voltage (V_n)	24.5 *kVrms*
Frequency (f)	50 *Hz*
Peak voltage	20 *kV*
L-filter impedance *(r + jωL)*	(0.01+j0.25)*p.u.*
Base frequency, ω_b	314.1592 *rad/sec*

The switching frequency of the converter is defined as 5 kHz. Hence the average time delay of the converter is:

$$T_a = \frac{1}{2 \cdot f_{switch}} = 100\ \mu s\ ,$$

where f_s is switching frequency.

The dc-link capacitance is

$$C = \frac{2\tau S_n}{U_{DC}^2}. \tag{4.1}$$

Using a time constant τ = 5ms and using the specifications from the table 4.1:

$$C = \frac{2\tau S_n}{U_{DC}^2} = \frac{(2)(0.005)100 \cdot 10^6}{(50 \cdot 10^3)^2} = 400\ \mu F \tag{4.2}$$

This matches the total capacitance of the dc-link. In the model this equivalent capacitance comes from two capacitors connected in series and grounded at their junction node. Two series connected capacitors of 800μF are used in the VSC-HVDC models.

4.3. The main per-unit values

Base quantities for *dq* reference frame are

$$S_b = V_{db} I_{db} = \frac{2\sqrt{3}}{3} V_n I_n = \frac{2}{3} S_n = \frac{2 \cdot 100}{3} = 66.67\ MVA$$

$$V_{db} = V_{qb} = \sqrt{\frac{2}{3}} V_n = \sqrt{\frac{2}{3}} \cdot 24.5 = 20\ KV$$

$$I_{db} = I_{qb} = \sqrt{2} I_n = \frac{S_b}{V_{db}} = \frac{66.67\ MVA}{20\ KV} = 3.33\ KA$$

$$Z_{db} = Z_{qb} = \frac{V_{db}}{I_{db}} = \frac{20\ KV}{3.33\ KA} = 6\Omega$$

$$L_b = Z_{db} = 6\Omega$$

$$C_b = \frac{1}{Z_{db}} = \frac{1}{6\Omega}$$

The base quantities for the dc side of the VSC-HVDC are calculated as shown below.

Rated power

$$S_{DC,b} = S_n = \frac{3}{2} S_{db} = 100\ MVA$$

Dc voltage

$$U_{DC,b} = 2V_{d,b} = 40\ KV$$

Dc current

$$I_{DC,b} = \frac{S_{DC}}{U_{DC,b}} = 2.5\ KA$$

Impedance

$$Z_{DC} = \frac{U_{DC,b}}{I_{DC,b}} = \frac{40\ KV}{2.5\ KA} = 16\Omega$$

Physical quantities of inductance, resistance and capacitance

$$L = \frac{0.25pu \cdot 6\Omega}{100\pi\ rad/s} = 0.0048\ H$$

$$r = 0.01pu \cdot 6\Omega = 0.06\Omega$$

$$C = 400\ \mu F$$

The per-unit quantities will are found as follows

$$L_{pu} = \frac{L}{L_b} = \frac{0.0048}{6} = 0.0008pu \cdot s/rad$$

$$r_{pu} = \frac{r}{Z_{db}} = \frac{0.06}{6} = 0.01pu$$

$$C_{pu} = \frac{C}{C_b} = \frac{400}{1/6} = 2400pu \cdot rad/s$$

The VSC-HVDC model with the specified component ratings is shown in Figure 4.2 below.

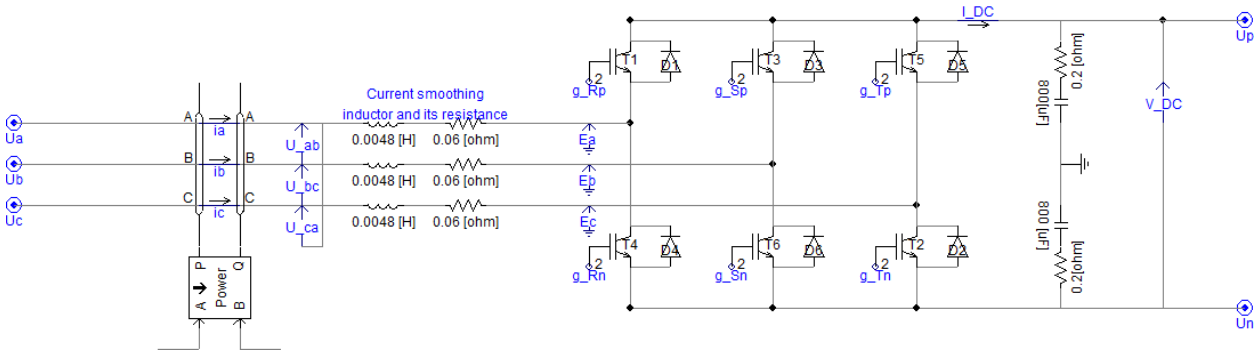


Figure 4.2. VSC-HVDC model in PSCAD software

As can be observed in Figure 4.2, the dc-link appears on the right while the grid is on the left side. The power measurement is made by measuring the line currents and voltages and applying mathematical equations. This is done in the "Power" block in Figure 4.2. The current smoothing inductors with their respective resistances of the line are also presented. The dc-link consists of two series connected capacitors which yield a total dc-link capacitance of 400 uF. The gate signals for the IGBTs are generated in a separate block and the PWM signal generation circuit is seen in Figure 4.3.

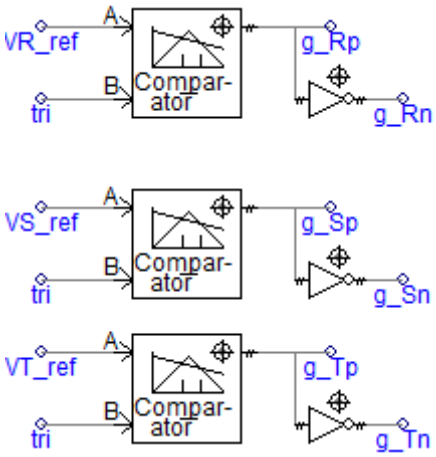


Figure 4.3. Gate signals for IGBT

Here, a triangular signal is fed into comparator and is compared with each phase's ac voltage. The output is the PWM signal which depends on both the level of ac voltage and triangular signal at particular time moment. This signal is inverted in order to make the signals for one leg complementary. The gate signal generation for two other legs is similar.

The line-to-line voltage measurements are used to calculate the phase voltages. The phase voltages are calculated as:

$$V_a = \frac{V_{ab} - V_{ca}}{3}$$
$$V_b = \frac{V_{bc} - V_{ab}}{3} \qquad (4.3)$$
$$V_c = \frac{V_{ca} - V_{bc}}{3}$$

In PSCAD this is implemented as shown in Figure 4.4.

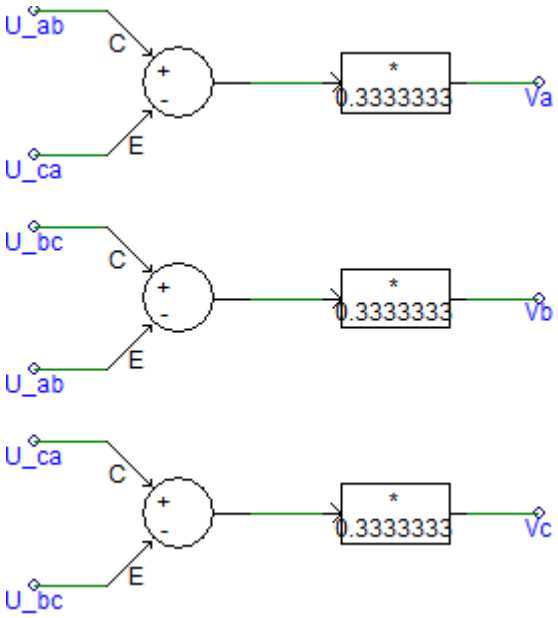


Figure 4.4. Phase voltage calculations from line voltage measurements

Calculating the phase voltages in the way that is shown in Figure 4.4 will avoid the zero sequence voltages.

Phase lock loop was built in PSCAD and used in the model as shown in Figure 4.5.

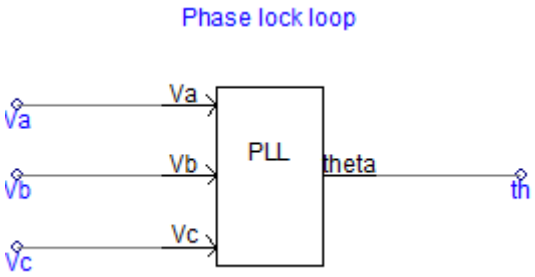


Figure 4.5. Built in PLL used for generation of synchronizing angle (θ)

The *abc to dq* transformations, *rms* measurements and *pu* conversions in *dq* reference frame are shown in Figure 4.6 below. The angle *th* in Figure 4.5 is the transformation angle generated by the PLL and is used in *abc* to *dq* transformation in Figure 4.6.

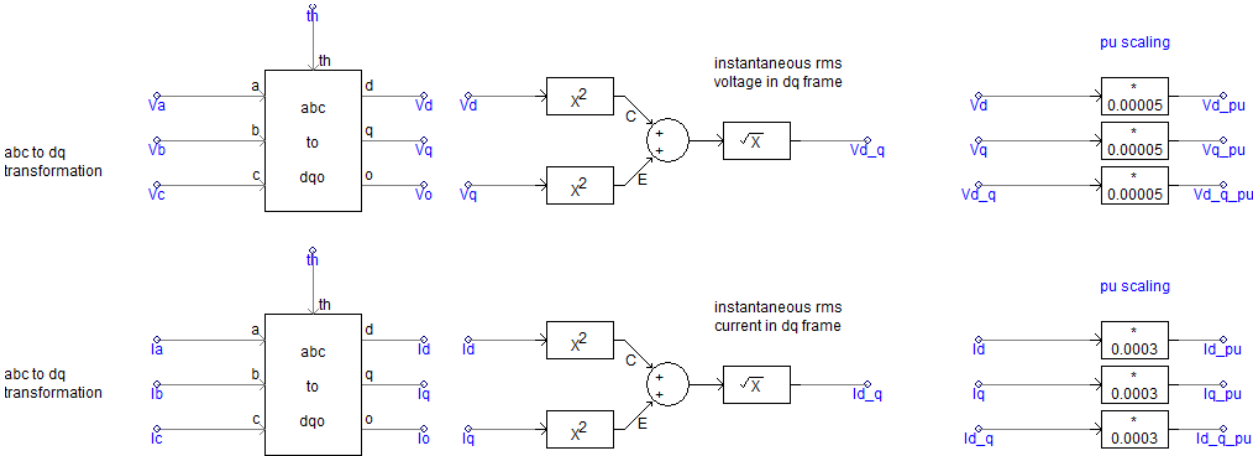


Figure 4.6. *abc to dq* transformations, *pu* transformations and *rms* measurements

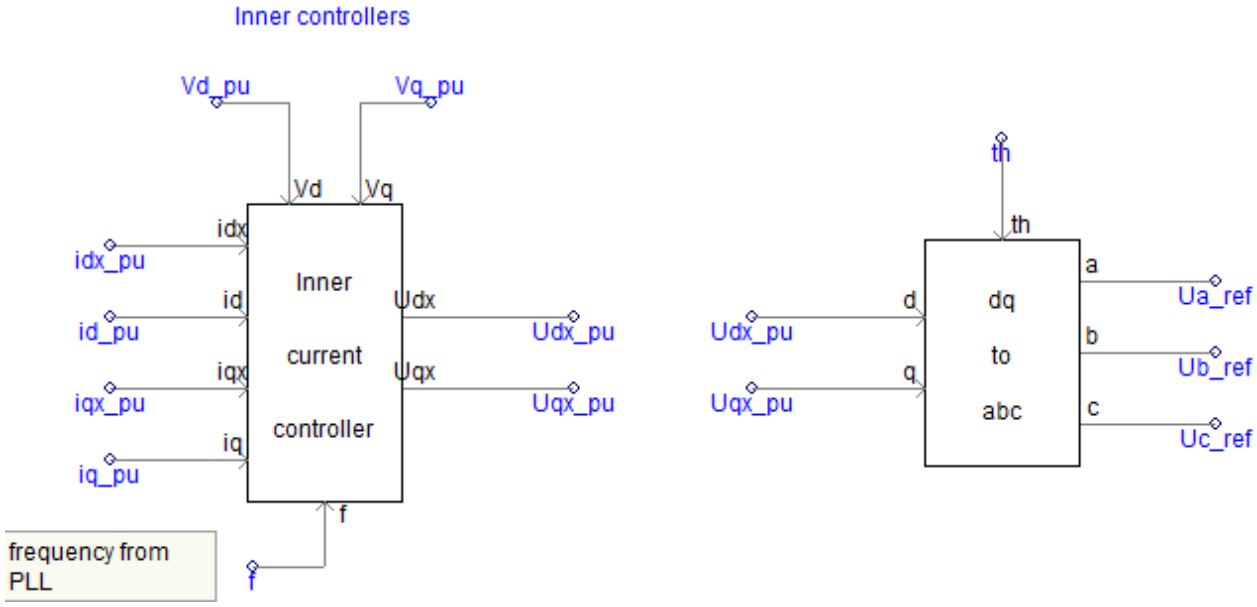


Figure 4.7. Inner current controller block diagram

idx_pu and *iqx_pu* shown in Figure 4.7 are reference currents for the active and reactive current controllers respectively.

4.4. Simulation of inner current loop

The inner current controller loop in PSCAD is shown in Figure 4.8.

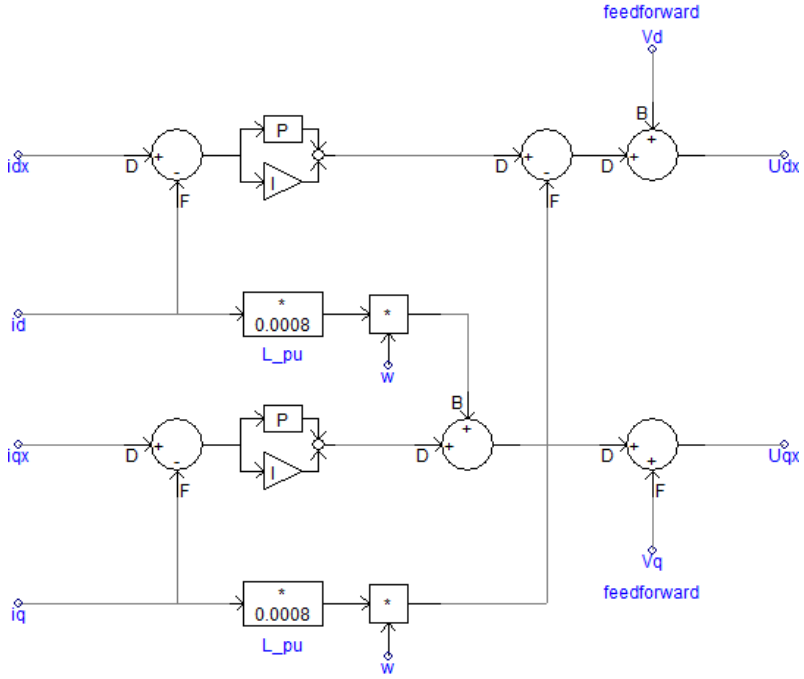


Figure 4.8. Inner current loop implemented in PSCAD

The PI controllers for the inner current loop are defined by modulus optimum criterion described in section 3.12.1.

Hence the time constant T_i is given by

$$T_i = \tau = \frac{L_{pu}}{r_{pu}} = \frac{0.0008}{0.06} = 0.013\ s$$

A cut-off frequency was selected $\omega_c = 5000/2 = 2500Hz$.

And the proportional gain becomes

$$K_P = \omega_c T_i r (1 + T_a^2 \omega_c^2)^{1/2} \qquad (4.4)$$

where

$\omega_c = 5000\pi$ rad/s,

$T_i = 0.013$ s,

r=0.01 pu,

$T_a = 10^{-4}$ s

Substituting the values into equation (4.4) we get

$$K_P = 5000\pi \cdot 0.013 \cdot 0.01(1 + (10^{-4})^2 \cdot 5000\pi^2)^{1/2} \approx 4$$

The control structure consisting of rectifier control scheme in PSCAD that incorporates the inverter dynamics and utilizes the capacitor energy as a variable is shown in Figure 4.9.

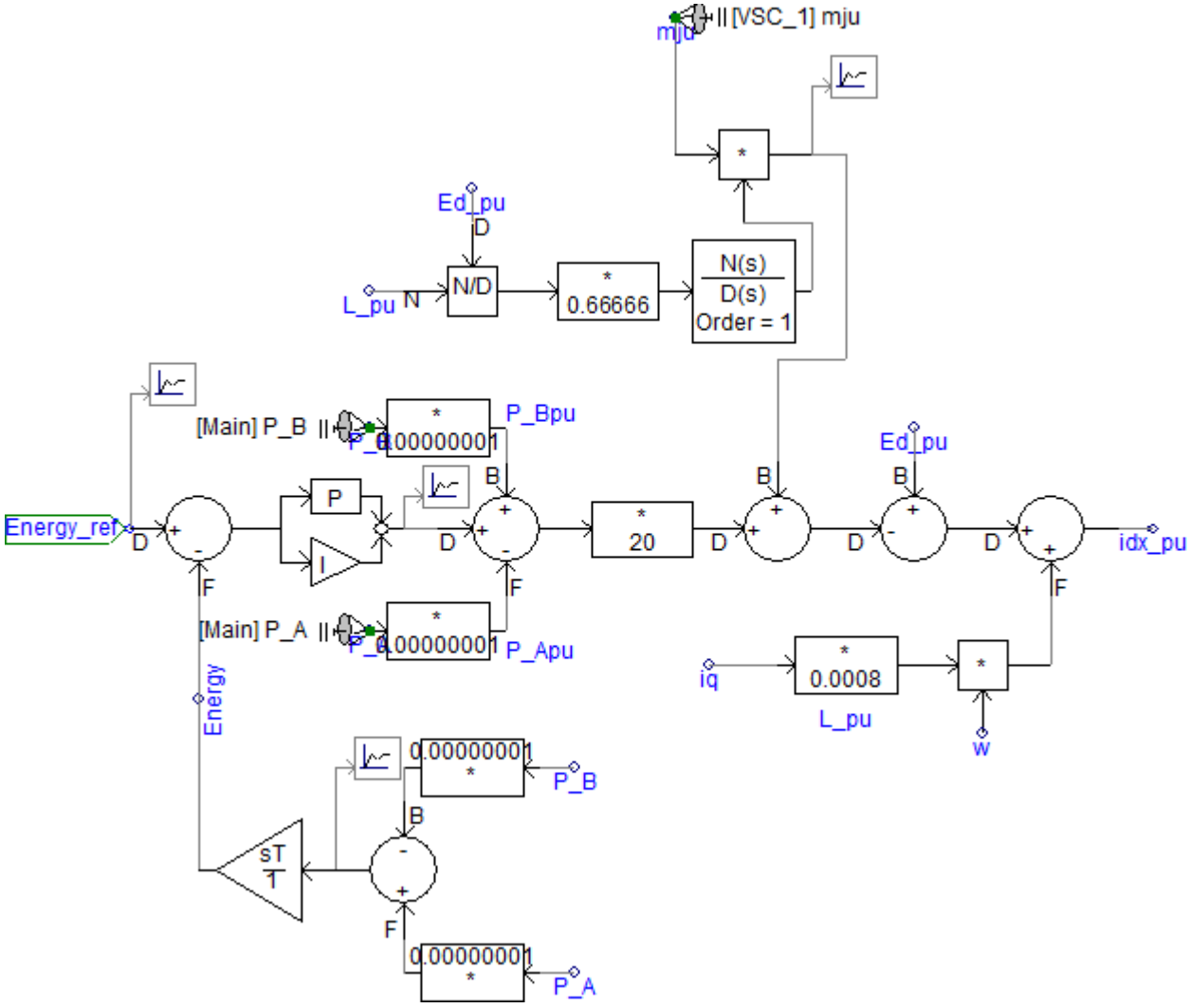


Figure 4.9. Rectifier control scheme that incorporates the inverter dynamics implemented in PSCAD

Based on the mathematical model and the block diagram, the proposed dc-link power balancing scheme for rectifier-inverter side was implemented in PSCAD software to prove the analytical derivation of equations. The model takes into account all the disturbances and influences of the system.

At some point of the systems design process the system showed quite good response. In this case the system responded to the reference values (Figure 4.10), but rather slow response was observed. As presented in the Figure 4.10 a very stressful start-up occurs with the dc-link voltage reaching almost 90 kV (2.25 pu). Some measures need to be provided to reduce this

peak, e.g. by means of optimizing the control system. The response of the dc-link voltage on the control systems reference is slow and with some visible oscillations. This might be due to the inaccurate tuning of PI regulators. The slow response introduces a benefit of lower voltage overshoot. This is highly appreciated since it reduces the stress on the dc-link capacitors and power semiconductors and therefore increases the lifetime of the system.

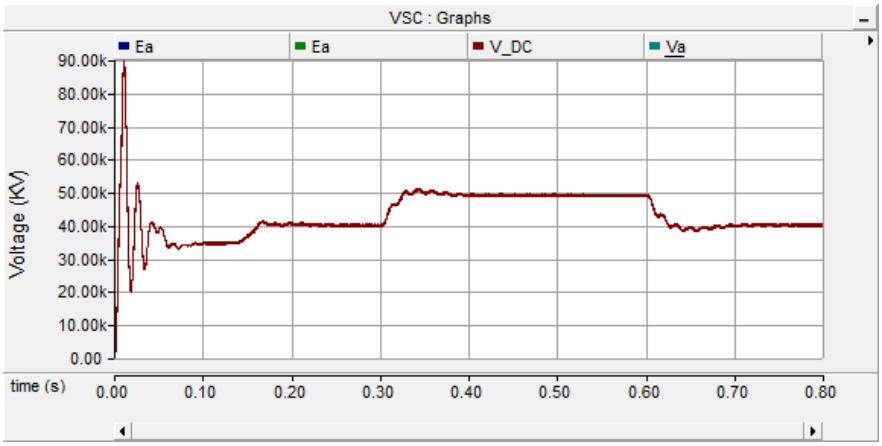


Figure 4.10. Dc-link voltage transient response for new control method

It should be noted that at that point the system was not complete and some vital parts of the system were missing or incomplete. For example, the energy feedback was incorrect, which according to the theory should not give any response, but in fact the system functioned well. For comparison the waveform in Figure 4.11 presents the result of the conventional properly tuned control system.

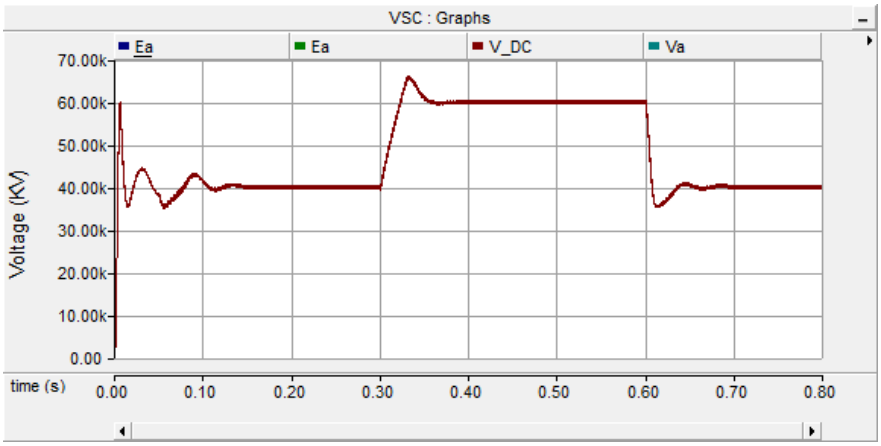


Figure 4.11. Dc-link voltage transient response for conventional control method [21]

The system response using conventional dc-link voltage control is fast and clear, but with obvious voltage over/undershoots.

5. CONCLUSIONS AND SUGGESTED FURTHER WORK

5.1. Conclusions

In this work two methods of dc-link voltage control were discussed, voltage control by using voltage reference and voltage control by utilizing energy of the dc-link capacitor as a reference. Tuning methods of the system were also discussed. The more interesting scheme of voltage control utilizing energy is implemented in PSCAD/EMTDC software after all mathematical derivations were carried out. The tuning of the PI controller was not realized in new proposed converter control scheme for a rectifier – inverter system, due to fact that the system is not responding to the input references and some errors need to be found and solved in order to continue the tuning of this control method. Some error correction proposals were suggested in the last stages of the thesis. Possible errors in the control circuitry can be, for instance, mathematical errors due to complexity of the given derivations, e.g. inverter dynamic equation derivation. Another possible reason is the practical implementation of block diagrams in the PSCAD environment.

Tuning methods for the conventional converter controllers have been established and tested by means of simulations. Method of modulus optimum is used to derive parameters of the inner current controller and symmetrical optimum to derive parameters of outer dc voltage controller. General guidelines for tuning the controllers are presented under simulations in PSCAD.

Further investigations of the control strategy and tuning rules are necessary for improvements in the controller performance.

5.2. Suggested further work

A good understanding of control system and strategies, their advantages and disadvantages in general operating conditions is necessary to derive the most relevant option for control of any system.

Possible errors in the control circuitry are as follows:

- Incorrect per-unit scaling of measured values;
- Possible mathematical errors due to complexity of the given derivations, e.g. inverter dynamic equation derivation;
- The practical implementation of block diagrams in the PSCAD environment;
- Improper tuning of PI regulators in the control system influences the overall systems performance.

Some of the possible further work proposals could be listed as follows.

- Existing errors must be corrected in order to make the further optimization of the control system;
- Frequency control should be evaluated;
- Study of the tuning rules for other types of outer controllers (active power, reactive power and ac voltage controllers);
- Study the case with VSC-HVDC connected to weak ac grid.

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APPENDIX

Appendix A

Modulus Optimum criterion

The open loop transfer function is given by

$$G_{O.L.} = K_p\left(\frac{1+T_iS}{T_iS}\right)\left(\frac{1}{1+T_wS}\right)\cdot\frac{1}{r}\left(\frac{1}{1+\tau S}\right) \quad ,\tau \gg T_w \tag{5.1}$$

The time constant T_i of the PI controller is defined so that $T_i = \tau$.

The chosen crossover frequency ω_c is one or two orders of magnitude smaller than *1/Tw* in order to avoid interference from the switching frequency components.

Following the requirement of unity gain at ω_c,

$$|G_{O.L.}| = \left|\left(\frac{K_p}{T_iS}\right)\left(\frac{1}{1+T_wS}\right)\cdot\frac{1}{r}\right|_{s=j\omega_c} \tag{5.2}$$

Reorganizing equation (3.21), proportional gain of the PI controller is determined as:

$$K_p = \omega_c T_i r|1+j\omega_c T_w| \tag{5.3}$$

Appendix B

Symmetrical Optimum criterion

Given the transfer function

$$G_{O.L.} = K_p\left(\frac{1+T_iS}{T_iS}\right)\left(\frac{1}{1+T_{eq}S}\right)\cdot\frac{3v_d}{2V_{DC}}\cdot\frac{1}{C_s} \tag{5.4}$$

The phase angle for $S=j\omega$ will be:

$$\begin{aligned}\angle G_{O.L.} &= \tan^{-1}(T_i\omega S) - 90° - \tan^{-1}\left(T_{eq}\omega S\right) - 90° \\ &= \tan^{-1}(T_i\omega S) - \tan^{-1}(T_i\omega S) - 180° \\ &= \phi_m - 180°\end{aligned} \tag{5.6}$$

where Φ_m is the phase margin.

Differentiating Φ_m with respect to cut-off frequency ω_c,

$$\frac{d\phi_m}{d\omega_c} = \frac{T_i}{1+(T_i\omega_c)^2} - \frac{T_{eq}}{1+\left(T_{eq}\omega_c\right)^2} = 0 \tag{5.7}$$

Solving equation (3.25):

$$\omega_c = \frac{1}{\sqrt{T_iT_{eq}}} \tag{5.8}$$

Substituting equation (3.25) in (3.26)

$$\angle\phi_m = \tan^{-1}\sqrt{\frac{T_i}{T_{eq}}} - \tan^{-1}\sqrt{\frac{T_{eq}}{T_i}}\,. \tag{5.9}$$

Let

$$\tan^{-1}\sqrt{\frac{T_i}{T_{eq}}} = \theta \;\rightarrow \tag{5.10}$$

$$\rightarrow \tan^{-1}\sqrt{\frac{T_{eq}}{T_i}} = 90° - \theta\,. \tag{5.11}$$

Φ_m in terms of θ becomes,

$$\phi_m = \theta - (90° - \theta) = 2\theta - 90° \tag{5.12}$$

and

$$\sin\phi_m = \sin(2\theta - 90°) = -\cos 2\theta\ . \tag{5.13}$$

From half-angle trigonometric equations

$$\begin{aligned} \sin\theta &= \sqrt{\frac{1-\cos 2\theta}{2}} \\ \cos\theta &= \sqrt{\frac{1+\cos 2\theta}{2}} \\ \tan\theta &= \sqrt{\frac{1-\cos 2\theta}{1+\cos 2\theta}}. \end{aligned} \tag{5.14}$$

Combining equations (5.10), (5.13) and (5.14),

$$\sqrt{\frac{T_i}{T_{eq}}} = \tan\theta = \sqrt{\frac{1-\cos 2\theta}{1+\cos 2\theta}} = \sqrt{\frac{1+\sin\phi_m}{1-\sin\phi_m}}. \tag{5.15}$$

Equation (5.15) gives integral time constant of

$$T_i = T_{eq}\left(\frac{1+\sin\phi_m}{1-\sin\phi_m}\right) = a^2 T_{eq}\ . \tag{5.16}$$

where *a* is constant. The higher the values of *a*, the higher the phase margin and consequently the overshoot decreases. On the other hand, the system response becomes slower. According to literature [25], the recommended value of *a* lies in a range between 2 and 4. For this particular work, the tuning is realized by choosing *a* = 3.

From the unity gain requirement at cut-off frequency,

$$|G_{O.L.}| = \left| K_p \left(\frac{1 + j\omega_c T_i}{j\omega_c T_i} \right) \left(\frac{1}{1 + j\omega_c T_{eq}} \right) \cdot \frac{3V_d}{2V_{DC}} \right| \cdot \frac{1}{j\omega_c} \tag{5.17}$$

$$= K_p \frac{3V_d}{2V_{DC}} \cdot \frac{1}{j\omega_c C} = 1 \, .$$

From equation (5.17) the proportional constant becomes

$$K_P = \frac{2V_{DC}}{3V_d} \omega_c C \, . \tag{5.18}$$