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Silicon Carbide Technologies for High Temperature Motor Drives

Øyvind Holm Snefjellå

Master of Science in Energy and Environment
Submission date: June 2011
Supervisor: Tore Marvin Undeland, ELKRAFT
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Problem description

Down-hole motor drive systems can be important in future oil gas installations for exploitation of existing oil wells. Huge values are related to increased exploitation of the oil fields. It is expected that technology development in this area will be a large driving force for development of power electronics for high temperatures and pressure. SmartMotor has initiated a 5 years research project on development of motor drives for subsea and down-hole operation. The project is in cooperation with the Norwegian research council (NFR). Silicon Carbide (SiC) is the most promising material for making semiconductors for high temperature operation. A comparison of the material properties of Silicon Carbide and Silicon is therefore of large interest.

The performance of two different SiC transistors should be verified. The switching speed of the transistors should be adjusted to study how the switching behavior will be affected. The intrinsic properties of SiC transistors make the devices extremely fast. At high switching speeds the influence of parasitic circuit elements becomes more important. The fast switching can easily lead to oscillations and ringings. Hence, the influence of parastics on the switching behavior should be studied. Finally a converter using Silicone Carbide transistor should be built and tested. The maximum operating temperature of the converter is dictated by the transistor housing and the devices used in the control and drive circuits. It is not the task of the thesis to find the maximum operation temperature. However, the operation of the converters with SiC transistors should be verified.

Assignment given: 17. January 2011

Supervisor: Tore Marvin Undeland, ELKRAFT

Preface

This master thesis documents the spring work during the fifth and final year of my master degree study in Energy and Environment at the Norwegian University of Science and Technology (NTNU). Working on this project has been challenging, nevertheless it has been very interesting and I have learned allot. Especially during the late hours I have spent in the laboratory, searching for errors and trying to find explanations for strange results. The fact that the research topic is quite new has created many challenges. Finding measuring equipment suitable for measuring the fast switching transients has proved to be very difficult and also time consuming.

During my work with the thesis there are a number of peoples I will like to address a great thank to, and whom I would not been able to finish the work without. First off all I would like to thank my supervisor Prof. Tore M. Undeland for giving me the opportunity to work on such an interesting topic. He has always encouraged me and supplied me with good ideas. And then Ibrahim Abuishmais, a PhD-student at the department, for helping me analyzing the measurements and for proof reading parts of my thesis. I would also like to thank Richard Lund from SmartMotor for helping throughout the whole project. He has always replied my mails and been willing to share his practical experience.

Bard Almås from the service lab at NTNU deserves an extra acknowledgement. He has spent numerous hours helping me with the lab equipment and showing me how to make printed circuit boards.

In the end, I would like to thank my fellow students, contributing to a nice and friendly working atmosphere. Without you it would not have been the same.

Øyvind Holm Snefjellå

Trondheim, June 2009

Summary

Many applications benefit from using converters which can operate at high temperatures among them; down-hole drilling, hybrid vehicles and space craft. The theoretical performance of transistors made of Silicon Carbide (SiC) is investigated in this work. It is shown that their properties at high temperatures are superior compared to Silicon (Si) devices. Two half-bridge converters, using SiC normally-off Junction Field Effect Transistors (JFET) and SiC Bipolar Junction Transistors (BJT), are designed and tested to verify the performance of SiC devices. The challenges which arise when replacing slow switching Si devices with extremely fast SiC transistors are thoroughly discussed.

To fully utilize the properties of SiC transistors, the converter designer must pay extra attention to the Printed Circuit Board (PCB) layout and component selection. For best device performance, all parasitics should be kept at a minimum. A high value of the Schottky diode capacitance results in voltage and current ringings, thus more ElectroMagnetic Interference (EMI) and switching energy loss. It is recommended selecting a Schottky diode with low junction capacitance as the freewheeling diode of the converter. Simulations and measurements show that the SiC transistors require special gate driving circuits to perform at their best. It is recommended to use a two-stage driver with high capability of charging and sinking gate/base currents. The JFET driver should also have a bipolar output to provide high noise immunity. The JFET is classified as a unipolar device; however the nature of the gate-source structure, which is a pn-junction, gives the device some bipolar characteristics. The gate structure is similar to BJT. To obtain a low on-state resistance some continuous gate current has to be provided. This is more pronounced at high temperatures.

An analog control board, for operating the half-bridge as a step down converter, is designed and implemented. The controller uses current mode control to obtain a constant output voltage. Slope compensation is included to ensure stable operation at high duty-cycles. This makes the converter able to operate stably for a wide range of input voltages. The step down converter shows excellent performance during stationary operations and the ripple voltage is within its limit.

When operating at high ambient temperatures it is important to have small transistor losses to minimize the self-heating of devices. The losses of a three phase inverter are calculated based on the measured conduction and switching losses of the SiC transistors. The calculations show that both inverters, based on BJTs and JFETs, are able to operate with very high efficiency even at high temperatures. High temperature characterization of the devices shows that their dynamic behavior, i.e. switching losses and switching times, are almost unaffected by temperature changes. The transistors, tested in this work, are suited to operate at ambient temperatures up to 150 ˚C. This is imposed by the conventional device packaging. Higher operating temperatures are achievable by using different packaging technologies, i.e. metal packaging advanced soldering methods.

Sammendrag

Mange applikasjoner drar nytte av å bruke omformer som kan driftes ved høye temperaturer. Blant disse applikasjonene finner en ned-i-hulls boring, hybrid biler og romfart industri. I dette arbeidet er den teoretiske ytelsen, til transistorer laget av Silisium Karbid (SiC), kartlagt. Egenskapene ved høye temperaturer er langt bedre enn for Silisium transistorer (Si). To halv-broer er designet og testet for å kartlegge ytelsen til to utvalgte SiC transistorer. De valgte transistorene er en ”Junction Field Effect Transistor” (JFET) og en ”Bipolar Junction Transistor” (BJT). JFETen er normalt av og leder kun når en positiv gatespenning påtrykkes. Når sakte svitsjende Silisium transistorer blir erstattet av ekstremt raske SiC transistorer oppstår det en rekke problemer. Disse problemene er studert grundig i denne rapporten.

Fo å utnytte egenskapene til SiC transistorene til det full, så må omformerdesigneren være ekstra nøye når kretskortlayouten skal tegnes. Komponenter må også velges med omhu. Den beste ytelsen oppnås hvis alle parasittiske komponenter blir minimert. En høy Schottkydiode-kapasitans resulterer i oscillasjoner i både strøm og spenning. Oscillasjonene bidrar til økt ElektroMagnetisk Interferens (EMI) og økte svitsjetap. Når en velger friløpsdiode er det derfor anbefalt å velge en Schottkydiode med lav kapasitans. Simuleringer og målinger viser at SiC transistorene er avhengig av å benytte spesielle gatedrivere for å driftes optimalt. Det er anbefalt å bruke en totrins driver som kan levere og trekke høye transiente gate/base-strømmer. Driveren for JFETen burde også ha en bipolar utgangsspenning for å øke immuniteten mot støy. JFETene viser noen av de samme egenskapene som bipolare transistorer, selv om de klassifisert som unipolare transistorer. ”Gate-source” strukturen til JFETene er en pn-overgang og ligner på den for BJTer. En kontinuerlig gatestrøm må påtrykkes for å oppnå en lav ledemotstand. Størrelsen på strømmen må økes med stigende temperatur.

En analog styrekrets for halv-broen er designet og test. Kontrolleren styrer halv-broen som en Buck omformer. Kontrolleren benytter strøm modus styring for å opprettholde en konstant utspenning. Strømstigningskompensering er benyttet for å dempe underharmoniske oscillasjoner som oppstår ved høye arbeidssykluser. Buck omformeren kan derfor driftes for et bredt spekter av innspenninger. Omformeren fungerer utmerket under stasjonær drift og rippelspenningen er innenfor grensene.

Under høytemperturdrift er det viktig at transistortapene er små slik at oppvarmingen av transistorene blir minst mulig. Tapene i en tre fase vekselretter er beregnet, basert på de målte svitsje- og ledetapene for BJTene og JFETene. Beregning viser at begge vekselretterne kan driftes med høy virkningsgrad selv ved høye temperaturer. Karakteriseringen av transistorenes dynamiske egenskaper ved høy temperaturer, viser at svitsjetidene og svitsjetapene er nesten uavhengig av temperatur. De testede transistorene kan benyttes for omgivelses temperaturer opp til 150 ˚C. Temperaturgrensen settes av begrensninger ved de konvensjonelle transistorkapslingene. Høyere temperaturer kan oppnås ved å benytte andre kapslingsteknologier. Metall kapslinger, hvor avanserte lodde teknikker er benyttet, er et eksempel på en type høytemperaturkapsling.

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Abbreviation

Parameter	Explanation
SBC	Synchronous Buck Converter
SPWM	Sinusoidal Pulse Width Modulation
PWM	Pulse Width Modulation
LED	Light Emitting Diode
BOM	Bill of Materials
CTE	Coefficient of Thermal Expansion
JFET	Junction Field Effect Transistor
BJT	Bipolar Junction Transistor
PCB	Printed Circuit Board
DR	Design Rules
CCM	Continuous Conduction Mode
DCM	Discontinuous Conduction Mode
DPT	Double Pulse Test
DUT	Device Under Test
DDCC	Direct Duty Cycle Control
SiC	Silicon Carbide

1 Introduction

1.1 Problem background and motivation

Large parts of the "easy" accessible oil and gas reserves are already discovered and exploited. To discover and access future reservoirs in a profitable manner, new technology is required. Electrification of down-hole applications have proven to be very promising, especially for exploitation of deep offshore reservoirs. Many of the processes which have been mechanically or hydraulically powered in the past are now starting to be electrified. Some of these applications are drilling motors, subsurface valves, progressive cavity pumps, intervention tools, etc. Figure 1-1 shows an overview of a possible down-hole system.

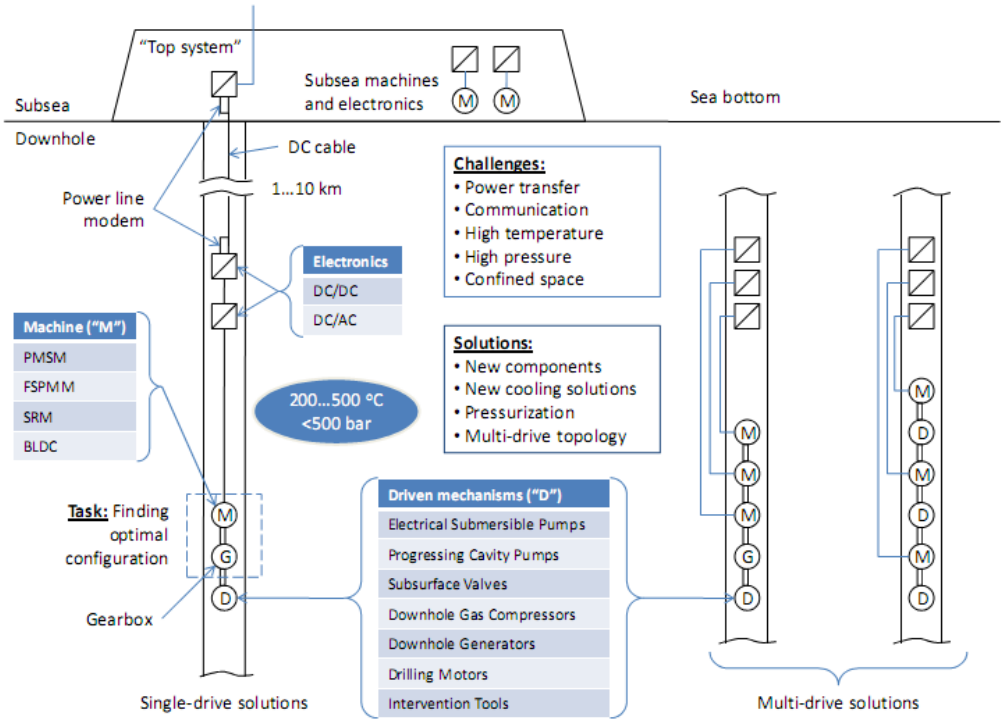

Figure 1-1 Oil and gas recovery system

The harsh environment for the power electronics with both high pressure and high temperatures demands new technologies for both control electronics and power stages. Depths of several kilometers into the sea bed are often experienced for such equipment. Temperatures increase by 15-30 ˚C/km, and the ambient temperature for the most extreme environments exceeds 200 ˚C. For down-hole operation to be successful one need to have motor drives which can operate reliably at these elevated temperatures.

Hybrid vehicles are another promising application area for high temperature motor drives. The performance and required motor size of a car are closely related to the cars size and weight. Hence, it is beneficial to reduce the weight. The cooling system for the semiconductors contributes to increased costs and weight. Converters for today's hybrid motor are based on IGBTs. Due to the high temperature on the cooling liquid of the combustion engine, the semiconductors need a separate cooling system. By introducing

Silicon Carbide (SiC) transistors and high temperature motor drives, the converters can use the same cooling system as the combustion engine [1]. This will greatly reduce both the cost and the weight of future hybrid vehicles.

Space craft and military industries have been a driving force for development of Silicon Carbide materials and high temperature electronics [2]. The fact that SiC can operate at higher temperatures and higher switching frequencies than Si [3, 4] gives a large reduction of heat sinks and passive components. Reduced size means reduced weight, and weight is one the most crucial factors when it comes to space travelling. Hence, NASA and other space explorers will benefit from the development of high temperature SiC converters.

This work is a preliminary study of Silicon Carbide converters for high temperature operation. Commercial available enhancement mode SiC transistors have been studied and two different transistors have been implemented in converters in. Inverters for high temperature operations are presented in [5, 6]. In [5] the main focus is on the packaging and the selected transistors are normally-on JFETs. [6] presents a 4kW Multi Chip Power Module (MCPM) which can operate at temperatures up to 300 ˚C. Large parts of the research on this topic is based on custom made packaging and non commercial transistors. In this work the focus is more directed against what can be made by using the available discrete SiC devices.

1.2 System description and scope of work

SmartMotor is working in cooperation with Badger Explorer to develop a motor drive for down-hole drilling. The concept of Badger Explorer is given in their web page: “The Badger Explorer, a new formation and reservoir evaluation tool which drills into the underground without the risks, cost and complexity of drilling an exploration well with a rig.” So the idea is to replace costly drilling rigs with an autonomous drilling machine which is powered with a DC cable. The drilling tool seals the hole behind it as it travels into the sea bed, and when the job is done the cable is cut and the tool is left buried. More information of the system can be found at [7].

The required specifications of the drive are given in Table 1-1. The drilling motor, which the drive is controlling, is a three phase permanent magnet radial flux machine. For the desired voltage and current levels the best selection of converter topology is a three phase full-bridge inverter, see figure Figure 1-2. Motors are much more robust than the power electronics, when concerning high temperatures. Hence, the largest challenge is to design the power stage of the converter and its drive circuitry.

High temperature drive specification	
V_{dc}	500 V
I_1	5-10 A
f_{sw}	15 kHz
T_{amb}	175 ˚C
Where	V_{dc} is the DC-link voltage I_1 is the rms value of the fundamental output current f_{sw} is the switching frequency T_{amb} is the down-hole ambient temperature

Table 1-1 Drive specification

One of the first steps when designing converters for high temperature is to find appropriate power transistors. Due to the limitations at high temperatures for regular

Silicon [8] it was decided to look into the new Silicon Carbide technology. A three-phase inverter is basically three bridge legs, also called half-bridge converters, connected in parallel. It is therefore a good start to first design a successful bridge leg, before building the complete inverter.

The goal of this thesis is to design and test two half-bridge converter using two different types of SiC transistor. The converters should meet the electrical specification given in Table 1-1. It is both difficult and expensive to get hold on ICs, small signal transistors and capacitors for high temperature operation. Hence, the gate drivers and control electronics used in this work are designed for normal operation temperatures (80 ˚C). Nowadays, all motor drives are implemented with digital control. Programming of DSP and FPGA controllers are both challenging and time consuming. This work focus on the hardware and analog control will be used for controlling the half-bridge. The half-bridge will be operated either as a step down converter or as a Synchronous Buck Converter (SBC).

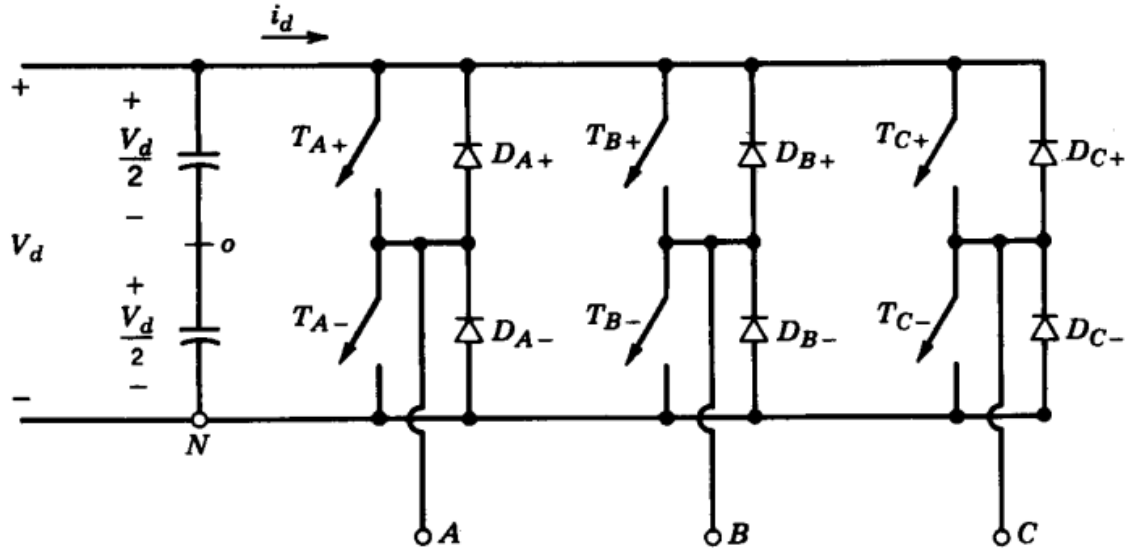

Figure 1-2 Three-phase inverter [9].

Most focus has been put on converter design considerations, both for bridge configurations in general and for SiC transistors in spesific. The new SiC transistors have different driving requirements than the well-known Silicon IGBT, which is used in most motor drives. Also, the dynamic behavior is very different form the one seen in IGBTs. This work treats the challenges which arise when replacing Si IGBTs or MOSFETs with SiC transistors. Especially, the influence of parasitic will be investigated closely. The work focuses on the application of semiconductor devices. However, and understanding of the semiconductor physics is necessary for an optimal design. From a control point of view normally-off transistors are preferred over normally-on devices. Hence, only enhancement mode SiC transistors will be considered in the thesis.

SiC devices have both lower on-state voltage and lower switching losses than comparable Si devices. It is therefore of interest to investigate what could be achieved by replacing Si transistors with SiC transistors. A theoretical comparison of the inverter losses for the two technologies will therefore be performed.

1.3 Report outline

This chapter has presented the motivation for looking into converters for high temperature motor drives. The scope of work and the system description have also been presented. Chapter 2 presents most of the theory which the report is based on. The theoretical properties of SiC are described in chapter 3. A theoretical loss comparison between a state-of-the-art IGBT and available SiC transistors are also performed. Chapter 4 describes the half-bridge converters designed, including layout consideration and driver selection. The design and tuning of an analog controller, for the half-bridge, is presented in the last sections of this chapter. The laboratory setup and the measuring equipment used for testing the converters are presented in chapter 5. A description of the experimental standard and principles are also given. Some initial measurements are given at the end of the chapter. These measurements are analyzed in chapter 6 by the use of the simulations program LTspice. The simulation program is also used to identify the influence of parasitic circuit elements on transistor switching waveforms. The results from the double pulse testing and from the on-state voltage measurements are presented in chapter 7. This chapter also includes verification of the performance of the step down converter. A brief conclusion followed by topics for further research is presented in chapter 8.

Matlab codes for calculation of switching losses and inverter losses are provided in appendixes. The PCB layouts and full Bill of Materials (BOM) for the converters are provided in appendix D and E respectively. The appendixes also include the simulation models and some additional measurements from the converter testing. Finally, some pictures of the laboratory setup and the converters are given.

Parts of the theory presented here is based on the background study performed in the specialization project [10]. To achieve complete substance of the thesis, some of the work from the specialization project is repeated. It is remarkable how fast the Silicon Carbide industry is developing. Some statements, from specialization project, regarding the production of SiC devices are no longer valid and large parts of chapter 3 had to rewritten before it could be presented.

2 Background and Theory

This chapter gives a short introduction of the convert topologies which are used in this work. Some useful equations which are used for design consideration and efficiency calculations are also presented. The challenges which arise at elevated temperatures are presented in the last section as an introduction to the Silicon Carbide chapter.

2.1 Step down converter

A step down converter, also called Buck converter, is a basic DC to DC converter, which produces an output voltage which is lower than the input voltage. Figure 2-1 shows the principal schematic of the converter. The reverse diode voltage is shown in Figure 2-2. The output filter of the converter acts as a low pass filter and filters out the ripple components of the switching voltage. This makes it possible to produce a DC output voltage.

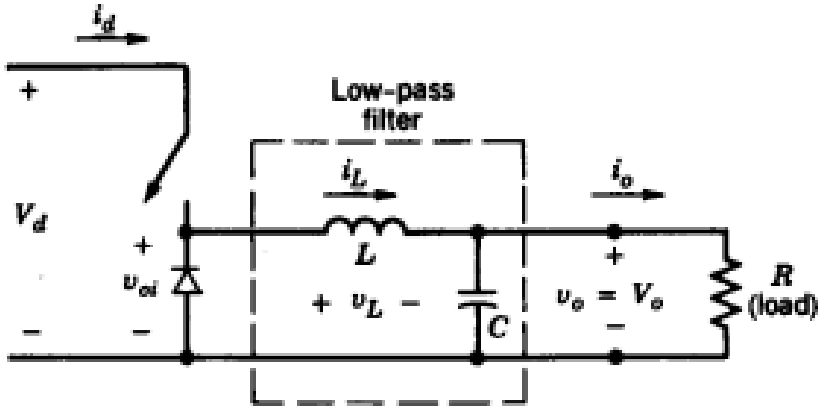

Figure 2-1 Step down converter with resistive load [9]

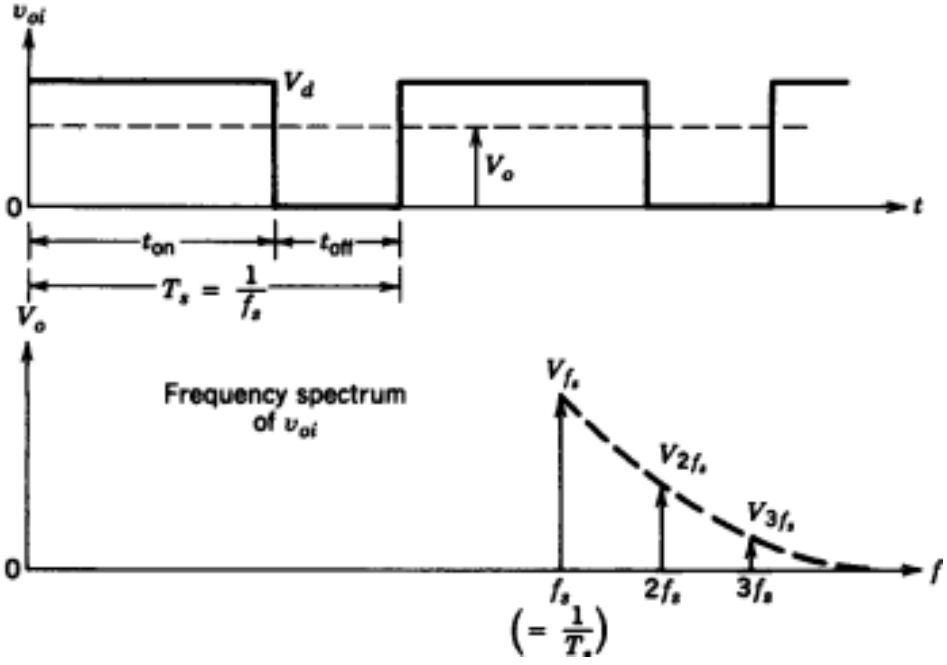

Figure 2-2 Output waveforms of Buck converter [9]

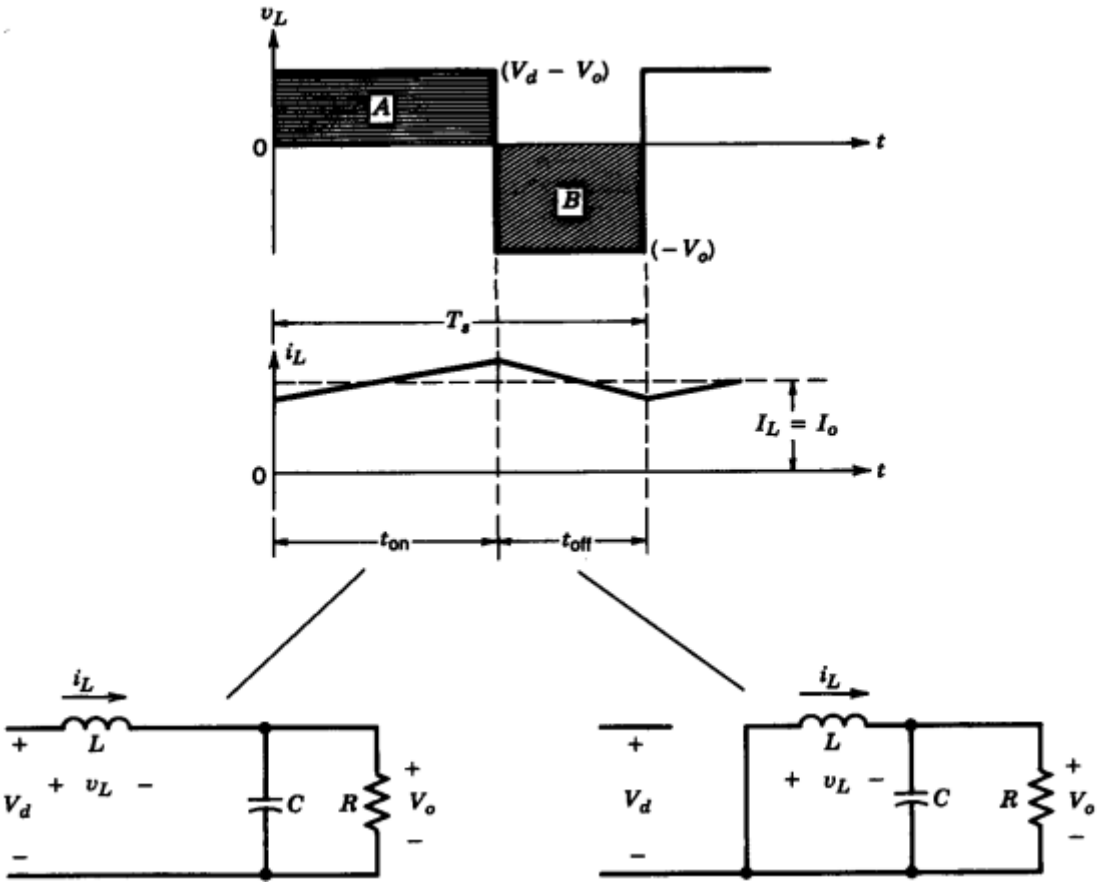

Figure 2-3 Inductor voltage and current assuming continuous current [9]

The relationship between the input and output voltage of the converter can be derived by considering the inductor voltage shown in Figure 2-3. In stationary operation, the integral of the inductor current needs to be zero. This can be showed by equation (2.1), since the inductor current has the same magnitude at the start and the end of each switching period.

$$v_L = L\frac{di}{dt} \tag{2.1}$$

By performing the integration, of the inductor voltage over one switching period, the relationship between input voltage (V_i), output voltage (V_o) and the duty cycle (D) can be found. When operating in continuous current mode the equation becomes:

$$V_o = V_i D \tag{2.2}$$

Where D is defined as the ratio between the on-time of the switch and the length of the switching period, $D=t_{on}/T_s$.

If the load gradually decrease the boundary between continuous- and discontinuous current is found at a boundary current I_{LB}. At the boundary the inductor current reaches zero amps at the end of the switching period. The value of the boundary current is therefore given by:

$$I_{LB} = \frac{1}{2} i_{L,peak} \tag{2.3}$$

An expression for $i_{L,peak}$ can be found by integrating both sides of equation (2.1) from zero to t_{on}. If the output voltage is kept constant, then the boundary current is given by:

$$I_{LB} = \frac{V_o T_s}{2L}(1 - D) \tag{2.4}$$

The boundary current is increasing with decreasing duty cycle, hence the lowest duty cycle will be dimensioning for the output inductor.

2.2 Half bridge converter

Figure 2-4 shows a principal drawing of a half-bridge converter. It consists of two transistors and two freewheeling diodes. The converter can operate as a single phase inverter by means of Sinusoidal Pulse Width Modulation (SPWM) or it can operate as a DC to DC converter. A description of the SPWM operation is given in section 2.4.2. If one of the transistors is kept off and the other is switching, then the setup can be used as a step-down converter by connecting a low pass filter across the diode which is opposite of the switching transistor. A half-bridge can also be operated as a synchronous Buck converter, which is an improved version of the Buck converter. A SBC uses a transistor instead of the freewheeling diode. By selecting an appropriate transistor, the freewheeling conduction losses can be greatly reduced. To operate the half-bridge in Figure 2-4 as a SBC; the low pass filter and the load is connected across D2. Q1 acts as the main transistor and Q2 as the freewheeling transistor. The converter controller must have a complementary output signal, which means that Q1 conducts when Q2 is off and opposite. The freewheeling diode D2 does only conduct during the short blanking time when both transistors are off. D1 will conduct if the inductor current goes negative. A description on how to generate the blanking time and how to obtain complementary control outputs are given in the next subchapter.

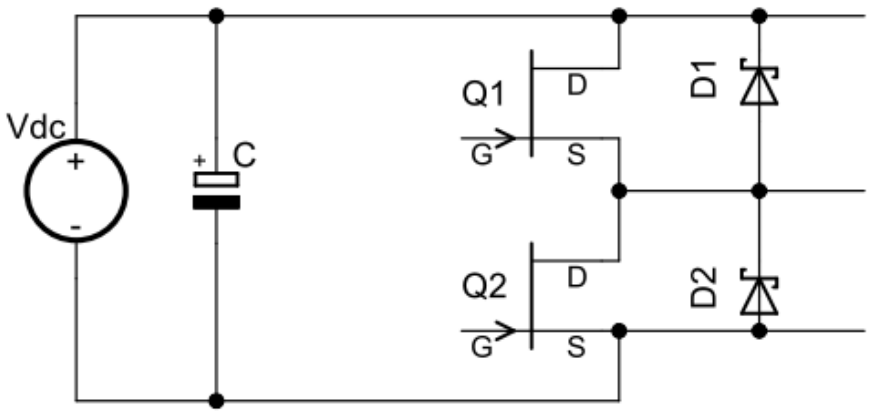

Figure 2-4 Half bridge converter

2.3 Gate drivers for bridge applications

When designing gate drivers for bridge configurations extra care must be taken, due to floating potentials and the risk of shorting the DC-link. It is common to refer the logic level control signals to ground. If the drivers are floating it is therefore required to use

signal isolation to avoid connecting together nodes with different potential. The output voltage of gate drivers are usually referred to the source potential of the transistors they are controlling. In bridge configuration the source voltage of the upper transistor jumps in potential when the lower is switching, thus signal isolation is required. If the DC-link voltage is generated by a rectifier and the negative potential of the DC-link is not grounded, then also the lower driver can be floating. The above arguments are also valid for the power supplies of the drivers, and the supply of the upper transistor must be isolated from ground. In general, all control circuits are electrically isolated from the drive circuit to prevent the high voltage of the power stage to enter the control circuit [11]. If both the upper and the lower transistor in a bridge leg is on at the same time, then the DC-link is shorted and an excessive current will flow. This phenomenon is called a shoot trough and a logic circuit must be added in the controller to prevent it. A shoot through can also occur if one of the transistors is turned on by noise. Hence, the gate drivers should be designed to provide high noise immunity.

2.3.1 Signal and power isolation

There are basically three ways of obtaining signal isolation, either by optocouplers, fiber optics or transformers [9]. Optocouplers and fiber optics transfer the signal by means of light produced by a Light Emitting Diode (LED). Fiber optics are more noise immune than optocoupler and they can provide very high isolation voltage and large creepage distances [9]. The advantage of opto-isolators is that they can transmit pulses of any duty cycle. On the other hand, they always require a power supply on the output side and they are somehow slower than isolation transformers. If the circuit is designed properly, isolation transformers can be used to transfer both signal and power. This is a major advantage over optocouplers. As a standalone component pulse transformers have a maximum duty cycle around 0.5, due to the requirement that the volt-seconds across the windings must balance. The duty cycle limitation can be overcome by using a high frequency square wave carrier to modulate the drive signal [11]. Figure 2-5 shows an example of such circuit; here the signal is restored by rectifying the pulses on the secondary side of the transformer.

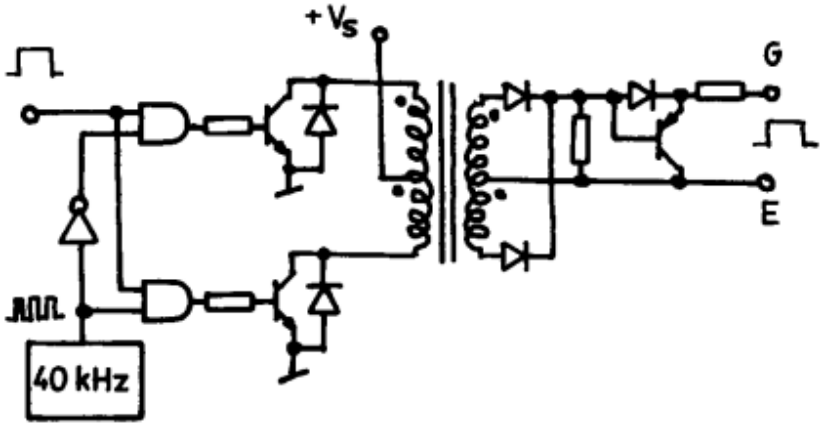

Figure 2-5 Carrier modulated transformer isolated drive circuit [11]

As described, all optical coupled and some transformer coupled drivers require a DC-supply on the output side. For the upper driver these have to be isolated. The two most popular ways of generating the DC voltage, are by use of auxiliary supplies or bootstrap supplies. The auxiliary supplies can be made by connecting a transformer, with several secondary windings, to the mains and rectifying the outputs. Isolated high frequency DC/DC converters can also be used. They can be made much more compact, since the

transformers are designed for high frequencies. A bootstrap supply can be used if the power required by the driver is very small. Figure 2-6 shows a simple circuit where the upper driver has an isolated bootstrap supply and the lower is supplied by an auxiliary DC source. The diode and the resistor act as a charge pump, and every time the lower transistor turns on, current flows from the lower supply charging the upper capacitor. When the upper transistor is on, the capacitor supplies the driver with the required energy, until the next time the lower transistor turns on, and the capacitor recharges.

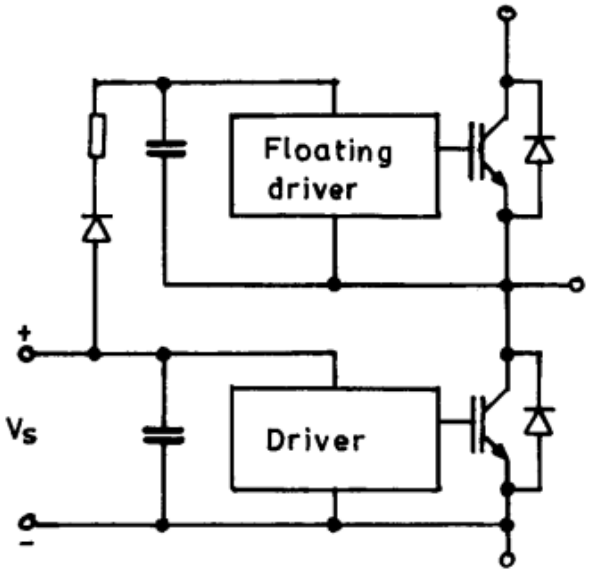

Figure 2-6 Bootstrap auxiliary supply [11]

2.3.2 Dead time calculation

The turn-off time of a transistor is usually different form the turn-on time. There are also differences in the propagation delay, of a gate driver, for turn-on and turn-off. Hence, the turn-on signal to one driver cannot be given at same time as the turn-off signal is given to the other. To avoid shoot through in a bridge configuration some "dead time" has to be added in the controller. The "dead time" is defined as the time from one of the gate drivers gets the turn off signal to the other gets the turn on signal. There are basically two types of dead time, one which is implemented in the controller as described above and one effective dead time where both of the transistors is off. The effective dead time is also called the blanking time. The blanking time is often a large fraction of the dead time since the controller dead time is calculated based on worst case considerations. During the blanking time, the output voltage is determined by the direction of the output current and not by the control signal. This introduces nonlinear effects and can case instability in some cases if the blanking time is too long.

The control dead time should be selected such that the blanking time always is positive, but not unnecessarily long. The controller dead time can be calculated from the following equation [12]:

$$t_{dead} = \left[\left(t_{off,max} - t_{on,\min}\right) + \left(t_{pdd,max} - t_{pdd,min}\right)\right] \cdot 1.2 \qquad (2.5)$$

Where, $t_{off,max}$ and $t_{on,min}$ are the respective maximum turn-off and turn-on time of the transistors for any possible operating condition. $t_{pdd,max}$ is the maximum propagation delay of the driver at turn-off and $t_{pdd,min}$ is the minimum propagation delay of the driver at turn-on. The factor of 1.2 is added to have some additional safety margin. A procedure for measuring the switching times is described in section 5.1.

Figure 2-7 shows an example of analog dead time generation for a half-bridge. The control signal is applied to A1 which is a buffer with complementary outputs. Complementary outputs means that one of the terminals has an inverting output while the other has a non inverting output. In a bridge configuration, A2 is connected to the upper gate driver and A3 to the lower. Assume that A3 initially is on and that the lower transistor is conducting, and then a positive signal is applied to the input terminal of A1. This results in a logic high voltage at the upper non inverting terminal and a logic low at the inverting terminal. The capacitor C5, which is charged initially, will quickly discharge through the diode D1 and A3 turns off when voltage over the capacitor is reduced under the threshold voltage.

For the upper branch, the voltage over the capacitor C2 is initially zero. When a positive voltage is applied the capacitor starts to charge through the resistor R4. After some time the voltage over the C2 reaches the threshold of A2 and the upper gate driver gets its on signal. The controller dead time is basically the charging time of the capacitor from zero voltage up to the threshold of A2.

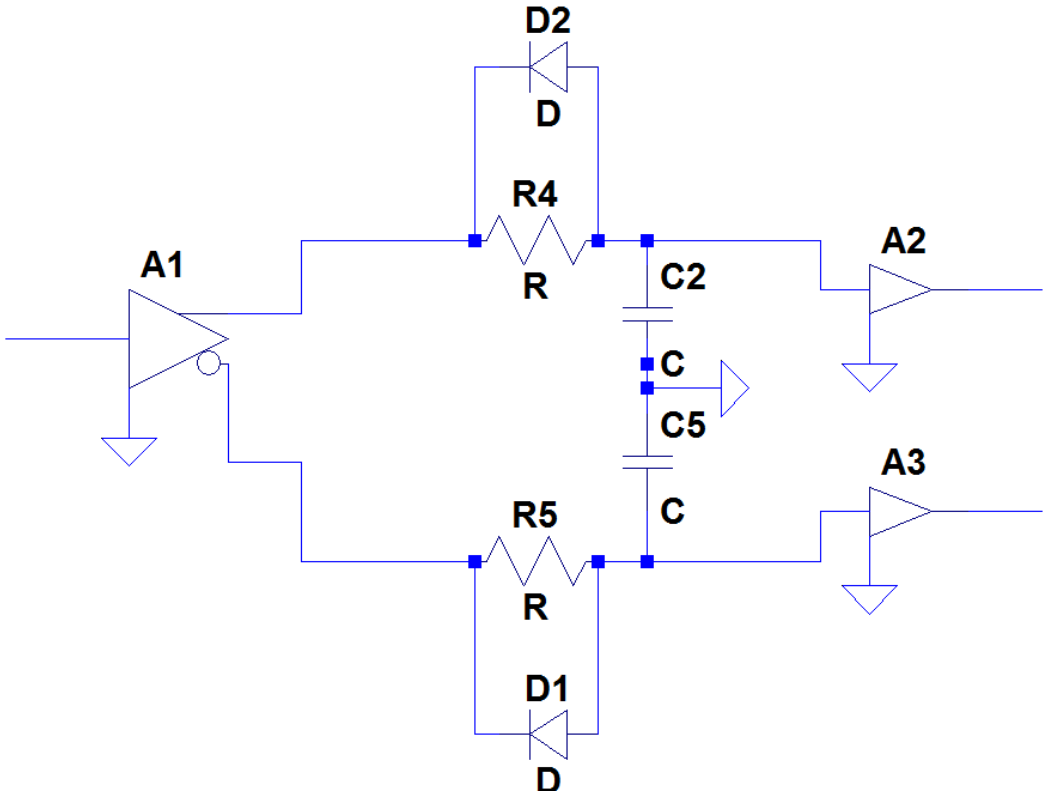

Figure 2-7 Dead time generation circuit

If one assumes that the output voltage of A1 is a step response with amplitude equal to V_o and the capacitor voltage is denoted by V_{cap}, then the dynamic equation describing the circuit can be written as:

$$V_o = CR\frac{dV_{cap}}{dt} + V_{cap} \tag{2.6}$$

By using laplace transform followed by partial fraction decomposition and inverse laplace the time response can be found.

$$V_{cap}(t) = V_o(1 - e^{-\frac{t}{RC}}) \quad (2.7)$$

The required time constant, τ=RC, is found by setting $V_{cap}(t_{dead})=V_{threshold}$, where $V_{threshold}$ is the threshold voltage of A2 and A3.

2.4 Inverter losses

The losses in a inverter consists of driving power for the transistors, conduction and switching losses of transistors and diodes, losses in the output filter and ESR losses in the DC-link capacitor. This section focus on semiconductor related losses, and an analytical expression of the losses in a three phase inverter is presented.

2.4.1 Driver losses and required driver power

When calculating converter losses, also driving losses should be included. To be able to dimension the power supplies of driver circuits, the required output power and driver losses must be known. Figure 2-8 shows the principle connection of a driver. The internal resistance of the driver, R_{int}, often changes when the output changes from on to off.

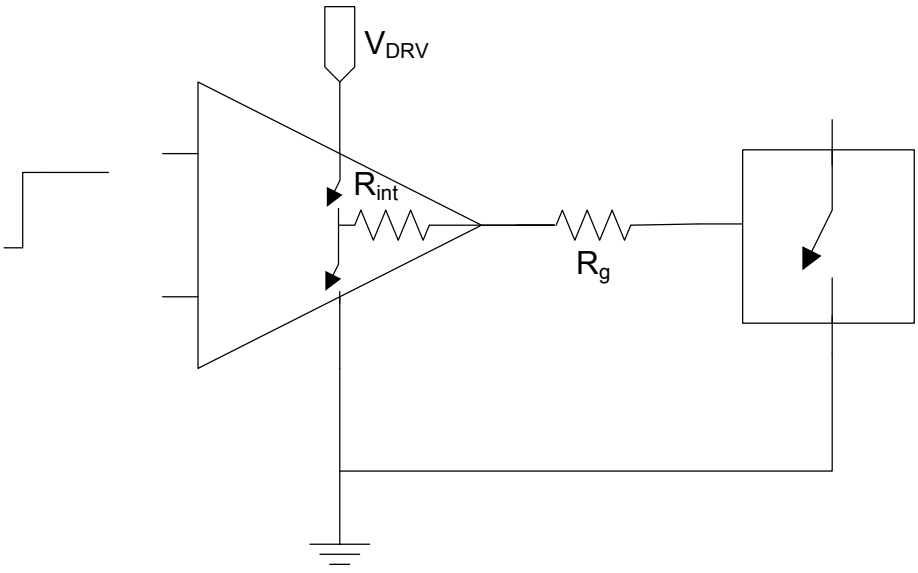

Figure 2-8 Principle driver connection

The power supplied by a driver circuit can be divided in two parts; power for charging the input capacitors and power for supplying a continuous base/gate current. The charging power is given by [13]:

$$P_{charge} = V_{DRV} Q_G f_{DRV} \quad (2.8)$$

Where V_{DRV} is the amplitude of the applied gate drive voltage, f_{DRV} is the frequency of the drive signal and Q_G is the charge required to charge the input capacitance, C_{ISS}, of the device. Q_G is the integral of the gate current during turn-on or turn-off of the transistor.

Q_G is a function of the applied gate voltage and it is also slightly dependent on DC-link voltage. The value of Q_G can usually be found by reading from the gate charge characteristic in the data sheet of the transistor. If the curve is omitted, the value of Q_G

can be estimated by using the input capacitance of the transistor. Equation (2.9) from [14] gives a good estimation.

$$Q_G = k_c C_{ISS}\left(V_{G(on)} - V_{G(off)}\right)$$
$$k_c = \frac{Q_{G(ds)}}{C_{ISS,ds}\left(V_{G(on,ds)} - V_{G(off,ds)}\right)} \tag{2.9}$$

$Q_{G(ds)}$ is the value specified in the data sheet and $V_{G(on,ds)}$ and $V_{G(off,ds)}$ are the applied gate voltages to obtain $Q_{G(ds)}$.

The most popular transistors of today, which are MOSFET and IGBT, do not require a continuous gate current. Among the SiC transistors, both normally-off JFETs and BJTs needs a continuous base/gate current. Both devices have a pn-junction between the gate and the source/emitter. The required on-state power is therefore equal to product of the base current (I_b) and the forward voltage drop of the pn-junction (V_{fb}) multiplied with the duty cycle.

$$P_{onstate} = I_b V_{fb} D \tag{2.10}$$

In motor drives the driver has to operate at duty cycles up to 100%. The driver supply usually can operate with some overload for a short period. It is therefore common to dimension the supplies for a duty cycle of 0.95. When calculating the inverter losses the average driver duty cycle must be used. The control signals to the transistors in a bridge leg are usually complementary. Hence, the average driver duty cycle over one fundamental period is equal to 0.5, when the effect of the dead time is neglected. The required power to drive a transistor is therefore given by:

$$P_{drive} = P_{onstate} + P_{charge} = V_{DRV} Q_G f_{DRV} + I_b V_{fb} \cdot 0.95 \tag{2.11}$$

The conduction losses in the gate driver can easily be calculated by the following equation.

$$P_{cond} = I_b^2 (R_g + R_{int}) D \tag{2.12}$$

The driver losses are the sum of the charging power and the conduction losses. By summing P_{drive}(D=0.95) and P_{cond}(D=0.95) the size of the driver power supply can be found.

$$P_{drive,supply} = V_{DRV} Q_G f_{DRV} + 0.95[I_b V_{fb} + I_b^2 (R_g + R_{int})] \tag{2.13}$$

The required average power is found by changing the duty cycle from 0.95 to 0.5 in the equations above.

2.4.2 Analytical expression of power losses in a voltage source converter with sinusoidal currents

All derivations in this section assume sinusoidal pulse-width modulation. Figure 2-9 shows an ideal single phase inverter operating under SPWM.

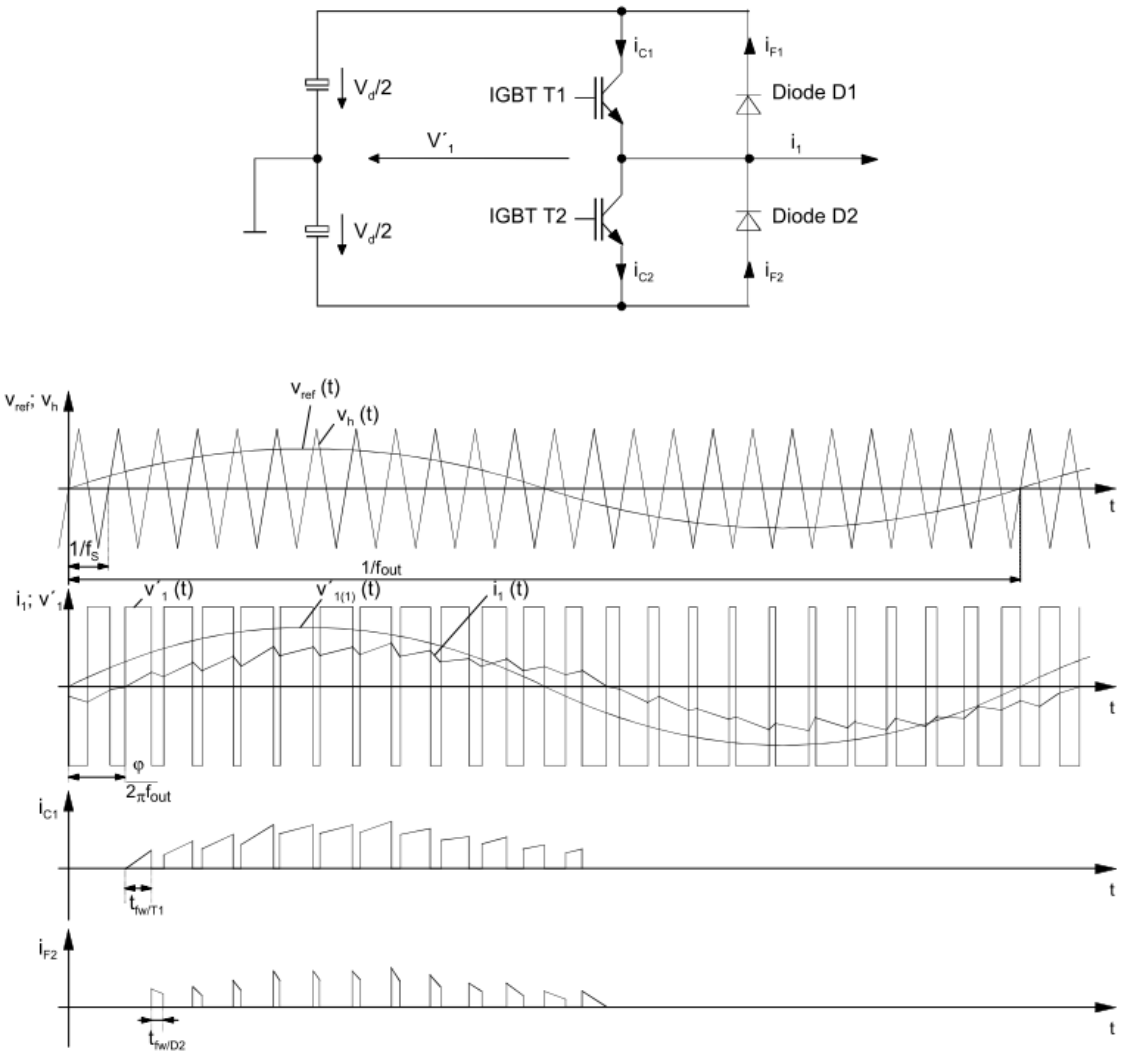

Figure 2-9 A single converter phase with sinusoidal pulse-width modulation [15]

The pulse pattern in sinusoidal pulse-width modulation is generated by comparing a sinusoidal reference voltage, $v_{ref}(t)$, with a triangular waveform, $v_{tri}(t)$. The upper switch in the bridge leg is on when the magnitude of the reference voltage is higher than the magnitude of the triangular waveform. The switching frequency is equal to the frequency of the triangular waveform and the amplitude of the sinusoidal output voltage of the convert is controlled by the amplitude of $v_{ref}(t)$. In normal converters it is not possible to access the midpoint of the DC-link, thus the output of a single half-bridge has a DC offset. When the load is connected between the midpoints of two half-bridge converters, operating under SPWM, the DC-bias is cancelled and only the AC component is left across the load. To obtain a three phase output one need three half-bridge modules and three separate reference signals to control them. The reference signals are obtained by sampling sinusoidal phase modulation functions.

$$\begin{aligned} m_R(\omega t) &= M\cos(\omega t) \\ m_S(\omega t) &= M\cos\left(\omega t - \frac{2\pi}{3}\right) \\ m_T(\omega t) &= M\cos\left(\omega t + \frac{2\pi}{3}\right) \end{aligned} \tag{2.14}$$

M is the modulation index and is given bellow

$$M = \frac{2\widehat{U_{(1)}}}{U_{dc}} \quad M \in [0,1] \tag{2.15}$$

Where $\widehat{U}_{(1)}$ is the amplitude of the output fundamental phase voltage and U_{dc} is the value of the DC-link voltage. If M is smaller or equal to 1, this is called linear modulation mode of the inverter. All transistor and diode pairs in the inverter will have the same losses, due to symmetry. Therefore, it is sufficient to consider the losses in one transistor and one diode and then multiply the losses with six to get the full three phase inverter losses. The transistor T1 and diode D2 are considered in the following derivation. Depending on the required accuracy and the available data different analytical loss models can be used.

Two loss models presented in [15] are given in the following sections.

2.4.2.1 *Simplified linear approach*

The first loss model is a simplified linear approach. This model is based on the following assumptions:

- Transistor and diode switching times as well as switching interlocking times are neglected
- The junction temperature is temporally constant
- Linear modulation of the converter
- The switching ripple in the output AC current is neglected
- The switching frequency is much larger than the AC output frequency.

The inverter losses are divided in on-state forward losses and switching losses.

Conduction losses:

By assuming a linear characterization of the on-state voltage of the diode, $v_F(t)$, and the transistor, $v_{CEsat}(t)$, their forward voltage can be expressed as:

$$v_{CEsat}(t) = V_{CE0} + r_{CE} \cdot \hat{\imath}_1 \sin(\omega t) \tag{2.16}$$

$$v_F(t) = V_{F0} + r_F \cdot \hat{\imath}_1 \sin(\omega t) \tag{2.17}$$

Where V_{CE0} and r_{CE} are the threshold voltage and the on-state resistance of the transistor respectively. V_{F0} and r_F are the threshold voltage and the on-state resistance of the diode. $\hat{\imath}_1$ is the peak value of the fundamental component of the output current. The value of V_{CE0} for unipolar transistors such as MOSFETs and JFETs is equal to zero. The on-state losses of the transistor T1 can be calculated according to

$$P_{fw,T1} = \frac{1}{2}\left(\frac{V_{CE0}}{\pi} \cdot \hat{\imath}_1 + \frac{r_{CE}}{4} \cdot \hat{\imath}_1^2\right) + M \cdot \cos(\varphi) \cdot \left(\frac{V_{CE0}}{8} \cdot \hat{\imath}_1 + \frac{r_{CE}}{3\pi} \cdot \hat{\imath}_1^2\right) \tag{2.18}$$

Where φ is the phase angle between the fundamental component of the output voltage and current. The diode, D2, forward losses are given by:

$$P_{fw,D2} = \frac{1}{2}\left(\frac{V_{F0}}{\pi} \cdot \hat{\imath}_1 + \frac{r_F}{4} \cdot \hat{\imath}_1^2\right) - M \cdot \cos(\varphi) \cdot \left(\frac{V_{F0}}{8} \cdot \hat{\imath}_1 + \frac{r_F}{3\pi} \cdot \hat{\imath}_1^2\right) \tag{2.19}$$

From equation (2.17) and (2.18) one can see that conduction losses are dependent of the phase angle of the current. As the phase angle increases the diode losses increase and the transistor losses reduce. The reason is that the relative conduction time of the diode increases with reduced power factor. If φ is increased beyond 90 °, the converter operates as a rectifier.

Switching losses:

The switching losses are sum of turn-on and turn-off losses of the transistors and the diodes. The turn-on losses of diodes are very small compared to the other losses, thus they can be neglected. By assuming that the switching losses are linearly dependent on the transistor/diode current they can be calculated from

$$P_{on+off,T1} = \frac{1}{\pi} f_s \left[E_{on,T}(\hat{\imath}_1) + E_{off,T}(\hat{\imath}_1) \right] \tag{2.20}$$

$$P_{off,D2} = \frac{1}{\pi} f_s \cdot E_{off,D}(\hat{\imath}_1) \tag{2.21}$$

Where $E_{off}(\hat{\imath})$ and $E_{on}(\hat{\imath})$ are the switching energies which can be found from a data sheet or measured in the lab. A procedure on how to measure the energies is given in section 5.1.1. The losses increase approximately linearly with increasing DC-link voltage.

If $E(\hat{\imath},V_{dc})$ is not given in the data sheet, the switching losses can be estimated with (2.22) from [16].

$$P_{sv} = \frac{1}{\pi} f_s \left[E_{on,T} + E_{off,T} + E_{off,D} \right] \frac{V_{dc} \hat{\imath}_1}{V_{ref} \hat{\imath}_{ref}} \tag{2.22}$$

The switching energies in the equation are measured at a current equal to $\hat{\imath}_{ref}$ and a DC-link voltage equal to V_{ref}. This equation can only be used for small deviations from the reference values since the rise and fall times are dependent on the magnitude of the current and voltage magnitudes.

2.4.2.2 *Approximation of component characteristics by polynomial equations*

This model is based on the same assumptions as the previous model except that the effect of the dead time is included.

Conduction losses:

By approximating the forward characteristic of the transistor and the diode according to y = A+Bx , one gets the following equations:

$$P_{fw,T1} = \left(\frac{1}{2} - \frac{T_{dead}}{T_s}\right)\left(\frac{A_{fw,T}}{\pi} \cdot \hat{\imath}_1 + \frac{B_{fw,T}}{4} \cdot \hat{\imath}_1^2\right) + M \cdot \cos(\varphi) \cdot \left(\frac{A_{fw,T}}{8} \cdot \hat{\imath}_1 + \frac{B_{fw,T}}{3\pi} \cdot \hat{\imath}_1^2\right) \tag{2.23}$$

$$P_{fw,D2} = \left(\frac{1}{2} + \frac{T_{dead}}{T_s}\right)\left(\frac{A_{fw,D}}{\pi} \cdot \hat{\imath}_1 + \frac{B_{fw,D}}{4} \cdot \hat{\imath}_1^2\right) - M \cdot \cos(\varphi) \cdot \left(\frac{A_{fw,D}}{8} \cdot \hat{\imath}_1 + \frac{B_{fw,D}}{3\pi} \cdot \hat{\imath}_1^2\right) \tag{2.24}$$

Switching losses:

By approximating the switching losses dependency on current according to $y = Bx+Cx^2$ the losses can be calculated with:

$$P_{on+off,T1} = f_s \cdot \hat{\imath}_1 \left(\frac{B_{on+off,T}}{\pi} + \frac{C_{on+off,T}}{4} \hat{\imath}_1 \right) \tag{2.25}$$

$$P_{off,D2} = f_s \cdot \hat{\imath}_1 \left(\frac{B_{off,D}}{\pi} + \frac{C_{off,D}}{4} \hat{\imath}_1 \right) \tag{2.26}$$

2.4.3 Total converter losses

The total semiconductor related losses of a three phase inverter are the sum of the switching losses, the conduction losses and the driving losses. By combining (2.8), (2.12), (2.18), (2.19), (2.20) and (2.21) the losses can be written as:

$$P_{loss} = 6(P_{charge} + P_{cond} + P_{fw,T1} + P_{fw,D2} + P_{on+off,T1} + P_{off,D2}) \tag{2.27}$$

The output power of a sinusoidal three phase inverter is given by [9]

$$P_{3-phase} = \sqrt{3} V_{LL} I cos(\varphi) = \frac{3\hat{U}_1 \hat{\imath}_1}{2} cos(\varphi) \tag{2.28}$$

and the efficiency can then be written as

$$\eta = \frac{P_{3-phase}}{P_{loss} + P_{3-phase}} \tag{2.29}$$

where V_{LL} is the line-to-line voltage.

2.5 Challenges at high temperature

To be able to design a converter for elevated temperatures it is important to understand the challenges and problems related to high temperature operation. There are different problems related to different types of components. A converter consists mainly of semiconductor power devices, control electronics, capacitors and inductors/transformers.

Some of the problems related to semiconductors are increased leakage current and reduced breakdown voltage. The life time of an electrolytic capacitor decreases with increasing temperature. The reasons for this are evaporation of the electrolyte and degradation of the dielectric films [17]. It can be showed that the life time of an electrolytic capacitor varies according to equation (2.30) [18]. The equation is based on the Arrhenius equation which is valid for all capacitor types.

$$L = L_B M_V 2^{\left[\frac{(T_R - T_C)}{10}\right]} \tag{2.30}$$

L_B is the lifetime at rated voltage and rated temperature in hours, T_R is rated temperature, T_C is the actual core temperature and M_V is the DC voltage multiplier.

$$M_V = 4.3 - 3.3\frac{V_A}{V_R} \tag{2.31}$$

V_A is the applied voltage. The value of ceramic capacitors tends to decrease for increasing temperatures [17]. Hence, it is hard to find large enough capacitance values at elevated temperatures.

At elevated temperatures, >150 ºC, optocouplers have excessive leakage currents, thus they can no longer be used. Hence, transformers must be used to provide signal isolation. When choosing transformers, special materials with low losses at elevated temperatures and with high Curie temperature has to be used. If the temperature in an iron core exceeds the Curie temperature it loses its magnetic properties.

This work concentrates on semiconductor devices and the proceeding sections goes more in detail on semiconductor related issues.

2.5.1 Semiconductors at elevated temperatures

The table below lists the main problems concerning semiconductors which are operating at elevated temperatures [8]. Some of the problems in the list are discussed below.

Physical effects that make it difficult to build semiconducting devices and circuits that will operate reliably for long times at high temperatures
1. Increasing intrinsic carrier density with temperature
2. Increasing junction leakage current with temperature
3. Variations in device parameters with temperature
4. Availability of adequate wide-temperature-range device models for circuit simulators
The following degradation mechanisms accelerate with increasing temperature:
5. Increased electromigration of conductors
6. Increased chemical reactivity, especially of ohmic contacts
7. Increased diffusion of dopants and ohmic contacts
8. Decreased dielectric breakdown strengths
9. Mechanical stresses due to expansion mismatches and thermal cycling
10. Reliability assurance and evaluation
Other issues which concerns technological infrastructure and manufacturability:
11. Availability of low defect density wafers
12. Availability of doping techniques
13. Availability of wet (chemical) and dry (plasma) etching techniques

Table 2-1 Problems regarding construction of semiconductors for high temperatures

The intrinsic carrier density, n_i, of a semiconductor depends on the temperature and of the band gap of the material. The relationship is descibed by the following equation [8]:

$$n_i = \left(\frac{2\pi kT}{h^2}\right)^{\frac{3}{2}} (m_{dh}m_{de})^{\frac{3}{4}} e^{-\frac{E_g}{2kT}} \tag{2.32}$$

Where k and h are Plank's and Boltzmann's constants, T is the absolute temperature, m_{de} and m_{dh} are the electron and hole effective masses, and E_g is the bandgap. The formula shows that the carrier density increases with increasing temperature. If n_i reaches the dopant density then this junction is "washed out" and cannot withstand a reverse voltage. To counteract the increasing n_i, the doping density can be increased. Unfortunately this will result in reduced breakdown voltage. The I-V characteristic of a pn junction is given equation (2.33) [9].

$$J = qn_i^2 \left[\frac{L_n}{N_a \tau_n} + \frac{L_p}{N_d \tau_p} \right] [e^{\frac{qV}{kT}} - 1] \quad (2.33)$$

N_d and N_a are ionized donor and acceptor densities respectively, q is the magnitude of the electron charge, J is the current density, V is the voltage over the junction, L_n is the minority carrier diffusion length, L_p is the majority carrier diffusion length, and τ_n and τ_p are minority and majority carrier lifetimes respectively. The term before the last square brackets can be recognized as the reverse saturation current of a pn-junction, and it is proportional to n_i^2. Hence thermal generations of carriers inside the junction increase the leakage current as the temperature increases.

Many high temperature components have to operate at a wide specter of temperatures. To design an electric circuit for high temperatures it is necessary to have good models of the devices performances. Hence, it necessary to know how the device parameters change with temperature

It is difficult to estimate the life time of high temperature components. The normal way of testing the reliability of a device is to expose it to temperatures and voltages beyond its ratings. This is called accelerated testing. For the test to be valid it is important that the failure mechanisms are the same in the accelerated test as under normal operation. This is not always the case for high temperature components. One of the reasons is that chemical reactions become more dominant at high temperatures.

2.5.2 Packaging

Reliable packages are required to operate successfully at high temperature. As the temperature increases, so does the stress on the package. Some important packaging issues are listed below.

First the materials have to sustain the high temperature. It is also very important that Coefficient of Thermal Expansion (CTE) of the substrate and the die are almost the same. Any mismatch can lead to cracking in the die [19] .

Electromigration in conductors is another important problem at high temperatures[8]. Electromigration is the transport of material caused by the gradual movement of the ions in a conductor due to the momentum transfer between conducting electrons and diffusing metal atoms. Eventually this can lead to open circuit.

Interdiffusion of different metals at the die bond pad can result in failure of the electrical interconnections [19]. There are also problems with soldering at elevated temperatures.

3 Silicon Carbide Technology

Before using a new material it is important to study its theoretical performance. The following sections describe the properties of Silicon Carbide and give an overview of the development of SiC power devices. A theoretical comparison between available SiC devices and a state-of-the-art IGBT is also performed.

3.1 Material properties of SiC

Silicon Carbide is a new and promising semiconductor for power electronic devices. SiC is a wide band gap material, which gives it many advantages over Silicone. A wide band gap means that the crystal bonds are stronger than in Si, i.e. it requires more energy to break an electron out of the bond. The increased band gap leads to a lower value of the intrinsic carrier concentration. Another important property of SiC is the high electrical field it can withstand. The critical electric field can be typically 10 times higher in SiC than in Si. Table 3-1 shows the most important properties of some wide band materials which can be used in power devices.

Parameter		**Silicon**	**4H-SiC**	**GaN**	**Diamond**
Band-gap E_g	eV	1.12	3.26	3.39	5.47
Intrinsic Conc. n_i	cm^{-3}	$1.4 \cdot 10^{10}$	$8.2 \cdot 10^{-9}$	$1.9 \cdot 10^{-10}$	$1 \cdot 10^{-22}$
Critical Field E_c	MV/cm	0.23	2.2	3.3	5.6
Electron Mobility μ_n	$cm^2/V \cdot s$	1400	950	1500	1800
Permittivity ε_r	-	11.8	9.7	9.0	5.7
Thermal Cond. λ	W/cm·K	1.5	3.8	1.3	20
BFoM: $\varepsilon_r \cdot \mu_n \cdot E_c^3$	rel. to Si	1	500	2400	9000

Table 3-1 Wide bandgap material properties in comparision with silicon [20]

It is important to mention that the electron mobility and the breakdown electric field are depending on the doping level. The table shows the properties for some standard values. The SiC substrates can be made in different polytypes i.a. 3C-SiC, 4H-SiC and 6H-SiC. The ones which are most used are 4H-SiC and 6H-SiC [4]. 4H-SiC is best for electronic applications due to its higher carrier mobility and wider band gap.

From equation (2.32) one can see that the intrinsic carrier density is exponentially decreasing with increasing bandgap. This means that SiC will have a much lower intrinsic carrier density than Si at a given temperature. The breakdown voltage of a 4H-SiC junction decreases only by 8% when the temperature changes from room temperature to 623 ˚C [4]. It follows from equation (2.33) that the diffusion current in a pn-junction is varying with the square of the intrinsic carrier density. Hence, a Silicon Carbide pn-junction has many orders of magnitude lower leakage current than a corresponding Silicon junction at elevated temperatures.

The theoretical advantages of using Silicon Carbide over Silicon are many. Different devices utilize the material properties in different manners. The proceeding sections discus how the material properties in Table 3-1 is related to the performance of devices. It is practical to divide the devices in two groups, unipolar devices which are majority carriers and bipolar devices which are minority carriers.

3.1.1 Unipolar devices

The main contribution to on-state losses in a unipolar device is the on-state resistance of the drift region. Thus a good way to compare SiC and Si is to compare the specific resistance $R_{on,sp}$. Assuming an abrupt, one-dimensional, non punch trough junction fabricated in a uniformly doped semiconductor layer the specific on-resistance can be expressed as [3]:

$$R_{on,sp} = \frac{4V_B^2}{\varepsilon_r \mu_n E_c^3} \tag{3.1}$$

V_B is the breakdown voltage (V), μ_n is the electron mobility ($cm^2/V \cdot s$), ε is the permittivity ($C/V \cdot cm$) and E_C is the critical electric field (V/cm). When two devices are compared it is reasonable to choose devices with the same breakdown voltage. Equation (3.1) shows that the resistance decrease with the third power of the critical electrical field and with increasing electron mobility. This equation can give an approximation of the ratio between the theoretical resistance in Si and SiC. Silicon Carbide has one order of magnitude higher value of the critical field than Silicon, thus the on-state resistance will be much smaller in SiC. To perform a more accurate calculation it is necessary to consider the mobility's and the breakdown electric fields dependency on the doping level N_B. This calculation has been done in [21] based on the material properties in

Table 3-2 . The result is shown in Table 3-3.

	Si	**6H-SiC**	**3C-SiC**
E_g(eV)	1,11	2,86	2,2
μ_n($cm^2/V \cdot s$)	1350	≈500	≈1000
V_{sat}(cm/s)	1×10^7	2×10^7	$2{,}5 \times 10^7$
E_c(V/cm)	2×10^5	~4×10^{6} [a)]	~3×10^{6} [a)]
ε	11,8	9,7	9,66
λ(W/cm· ˚C)	1,5	4,9	4,9
where	μ_n is the electron mobility E_c is the breakdown electric field strength ε is the dielectric constant λ is the thermal conductivity at 300K E_g is the bandgap V_{sat} is the saturation drift velocity		

[a)]For doping level of 4,8 X 10^{16} cm^{-3}

Table 3-2 Comparison of some of the electrical and material properties of Si, 6H-SiC, and 3C-SiC for power device applications

	$R_{on,sp(SI)}/R_{on,sp(SiC)}$			
	50V	200V	1000V	5000V
6H-SiC	92,9	198,2	305,7	355,9
3C-SiC	49,3	88,8	177,4	229,8

Table 3-3 Ratio between specific drift region resistance

The table shows that SiC has theoretically over two orders of magnitude lower specific on-resistance than silicon. Hence, SiC JFETs and MOSFETs can be made with considerable lower conduction losses than their Si counterpart. It can also be shown [3]

that the switching losses of a FET device decreases with increasing critical electric field, which gives SiC a further advantage over Si. Thus SiC can operate at higher switching frequencies. The losses in a FET power device can theoretically be reduced by 73 percent by replacing Si with SiC [3].

The most popular unipolar device of today is the MOSFET. Up to recently there has been none commercial available SiC MOSFETs due problems related to the inversion channel and the gate oxide layer. UMOSFET made of SiC can suffer from breakdown of the field oxide at the trench corners of the gate [22]. Since the critical electric field in SiC is ten time higher than in Si, the peak surface field in the semiconductor can reach values of 2-3 MV/cm without initiating breakdown. By Gauss' low it can be showed that the electric field in the gate oxide is up to 2.5 times higher than in the adjacent SiC. This gives a field in the oxide of 5-7 MV/cm, which is very close to the breakdown field of the oxide. In the corners of the gate structure there can be a field enhancement of up to 3 times the surrounding field strength. Hence, oxide breakdown becomes a limiting factor for high voltage UMOSFET made of Silicon Carbide. The largest problem with SiC MOSFET has been the low inversion channel mobility [22]. The inversion channel mobility in Silicon MOSFETs typically varies between 750 to 500 $cm^2/V{\cdot}s$ when the device is biased from weak inversion to strong inversion. In SIC MOSFETs the inversion channel motilities have been measured in single digits up to recently. New annealing techniques have result in higher mobility, 26 $cm^2/V{\cdot}s$ for NO-annealed MOSFETs and 89 $cm^2/V{\cdot}s$ for $POCI_3$-anneald MOSFETs [23], and January 2011 Cree lanched industry's first commercial SiC power MOSFET.

Schottky diodes have, unlike pn diodes, no reverse recovery behavior because they do not have minority carriers. However, they still have some reverse recovery effects due to parasitic capacitance in the devices. This capacitance creates oscillations due to parasitic inductances in the circuit. It also introduces some reverse recovery current, but it is much smaller than the one in a pn diode [24]. The low reverse recovery current reduces the losses in switching transistor, this have made the Schottky diodes very popular. The switching losses in Schottky diodes are very small and only the turn-off recovery needs to be considered. If one assume that diodes recovers at a constant reverse voltage, then the turn-off loss can be expressed as [25]:

$$E_{off,D} = Q_c V_R f_s \tag{3.2}$$

Where Q_c is the total diode junction charge at a specified reverse voltage V_R. The problem with Si Schottky diodes is the high leakage current due to the low barrier heights between Silicon and common metals, i.e. less than 0.5. By using Silicone Carbide a barrier height of approximately 1.5 eV is obtained between the SiC and the metal. The barrier height depends on which metals that are used. A high barrier height gives a high on-state voltage. Due to the fact that reverse leakage current is exponentially dependent on the barrier height, SiC schottky diodes have many orders lower leakage current than those made of Si, and they can therefore be used at higher voltage levels [22]. As general rule the reverse current density should be kept below 1 (mA/cm^2). There are demonstrated SiC Schottky diodes for blocking voltages up to 4 kV in [26].

3.1.2 Bipolar devices

The high bandgap of Silicon Carbide has also some drawbacks. To achieve the same value of the current density in SiC pn-junction, as in a Si, the forward voltage must be much higher. By combining equation (2.32) and (2.33) and make some simplifications

the forward voltage drop of pn-junction can be estimated by the following relations [20]:

$$U_f = \frac{E_g}{q} - \frac{kT}{q}\ln\left(\frac{J_{ref}}{J_f}\right) \tag{3.3}$$

Where J_f is the forward current density and J_{ref} is a factor that is slightly material and temperature dependent. Due to the high bandgap of Silicon Carbide the threshold voltage of a pn-junction becomes almost 3V. Hence, SiC pin diodes are only suitable for high voltage levels where the value of the drift region resistance dominates the on-state voltage.

The high threshold voltage is a big disadvantage for devices with an odd number pn-junction. This is one of the major drawbacks of SiC IGBTs and one of the reasons that IGBT not has been a competitive SiC device.

BJTs have an even number of junctions, thus the high threshold voltage of the pn-junction is somehow cancelled out. One of the problems with Silicon BJT is "second breakdown" which can lead to destruction of the device. The electron concentration in the collector drift region will exceed the background doping level for a critical value of the current density. When this happens there will be established a positive feedback in the thermal system and the transistor will become unstable, thus thermal runaway will occur [27]. For a high voltage device where the electrons reach their saturation velocity the critical collector current density is given by [27]:

$$J_{C,crit} = qnv_s = qN_D v_s \tag{3.4}$$

N_D is the drift region doping level. The doping level of the drift region for a given breakdown voltage is given below [9]:

$$N_D = \frac{\epsilon E_c^2}{2qV_B} \tag{3.5}$$

Silicon Carbide has 10 times higher critical filed than Silicon, thus the doping level and the critical current can be 2 orders of magnitude higher. In practice this means that second breakdown is not a problem in SiC BJTs. Due to the high critical field both collector and base can be made narrower in SiC than in silicon. The result is a higher current gain.

The high critical field in SiC allows for a much shorter drift region. Hence, the carrier lifetime in the devices can be greatly reduced. The result of this is reduced switching time. Hence, minority carrier devices in SiC will be much faster than their silicon counterpart [9].

Degradation is one of the major drawbacks related to bipolar SiC transistors. The presence of electron-hole-plasma can lead to crystal degradation and reduces the device performance over time [20]. Stacking fault is the main reason for these problems. Fortunately the production process has improved a lot the last decade and some of the producers now claim that the problem is solved.

3.2 State of the art of SiC devices

There has been a remarkable progress in the development of SiC power devices the last years. Currents in excess of 100 A and blocking voltages in excess of 19 000 V has been demonstrated [22]. Several discrete SiC transistors are now available from different manufacturers. The first available SiC transistor was the normally-on JFET, which was followed by the noramally-off JFET. During the last few months two new transistors have become available, namely the BJT and the MOSFET. The most successful SiC device so far is the Schottky diode, which contributes to greatly reducing switching losses in transistors due to their lack of reverse recovery current. The largest application of Schottky diodes are in Power Factor Correction (PFC) and in solar inverters. IGBT modules with SiC Schottky diodes are available from [28]. The long-term market forecast for SiC devices are very promising. It is expected that market size will grow from 53M$ in 2010 to 1B$ in 2020 [29].

Gallium Nitride (GaN) is also a very promising wide band gap semiconductor. It has higher Band-gap and higher critical electrical breakdown field than SiC, see Table 2-1. This makes it a good material for making fast switching high efficiency semiconductor devices. The production technology for GaN is quite immature at the moment, but there is expected a large growth in the nearest future [30]. Gallium Nitride has much lower thermal conductivity than Silicon Carbide. This is a drawback for high temperature operation and it is therefore expected that SiC will be the preferred material in high temperature devices [29]. Figure 3-1 shows a figure-of-merit comparing the material properties SiC, GaN and Si.

Implementation of SiC transistors in different applications has shown great results both regarding high efficiency and high temperature operation. By using SiC transistors, the efficiency of a converter can be increased, due to lower switching and on-state losses than their Silicon counterpart. Drop in replacement in inverters, where Silicon IGBTs are replaced with SiC transistors, have shown an increase in the efficiency of 1-3% [23, 31-33]. A SiC three phase 20 kVA inverter has been demonstrated with an efficiency of more than 99.5 % [34]. To fully utilize the high temperature properties of SiC both high temperature gate drivers and package are required. There is no use in a 600 ˚C device if there are no available packages. From the summer of 2011 a gate driver ICs, which can operate at temperatures up to 225 ˚C and sink/source currents of ±4A, will be available from [35]. There will also be available signal isolation, isolated DC/DC converters and controllers with fault detection, all which can operate at 225 ˚C. A complete SiC three phase 5kW inverter, including gate drivers and controller, which can operate at junction temperatures up to 200 ˚C has been presented in [36]. The inverter operates at switching frequency of 50kHz and the efficiency is 95,92% at T_j=200 ˚C. Due to the high junction temperature and the high switching frequency the heat sink and output filter can be made very small. Hence, the inverter is seven times smaller than a commercial Si inverter.

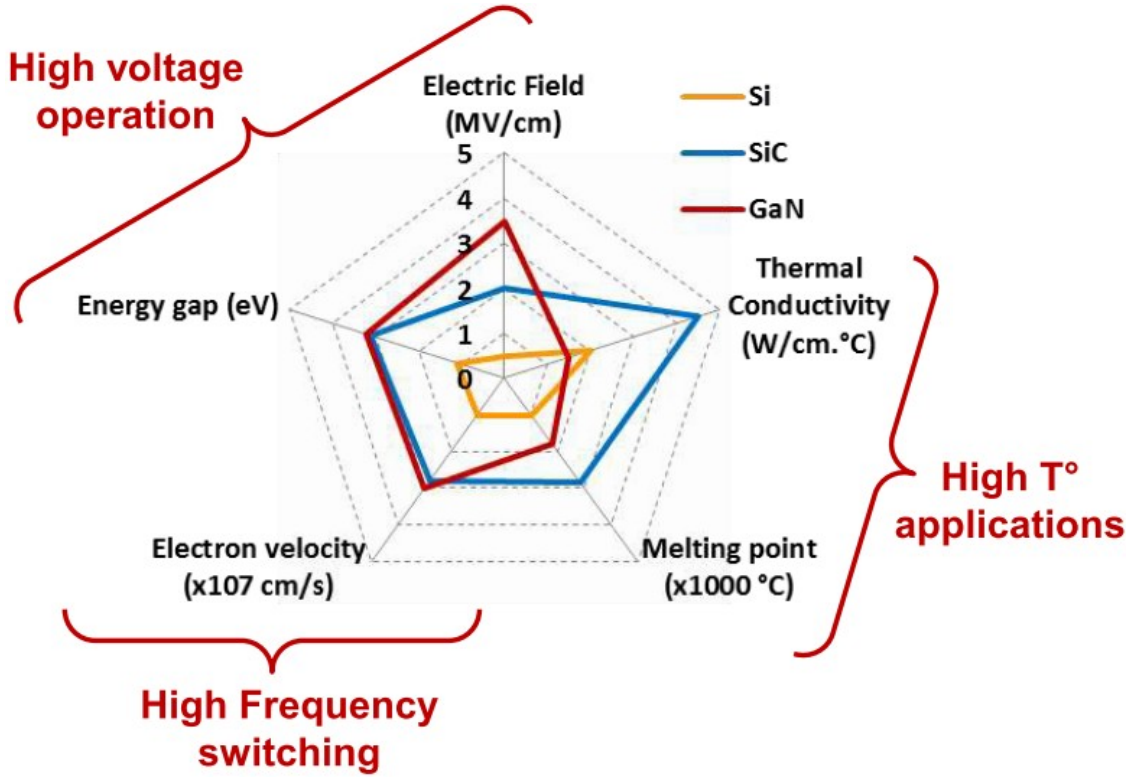

Figure 3-1 GaN vs. SiC vs. Si Figure-of-merit [29]

Micro pipes have been the largest problem with commercial SiC wafers. This has limited the size of available dies. In 2011 the first 6" SiC wafers will be produced [29], thus the substrate cost will greatly reduced. The future looks very promising for Silicon Carbide.

3.3 Available enhancement mode SiC transistors

It is important to understand the physics of a device before using it in a converter. The first available SiC transistors were normally-on devices, which is a drawback from a safety point of view. Most controll systems requires enhancement mode, such that the systems is shut down in case of failure in the controll power supply. It was therefore decided to look more closely into 3 of the available enhancement mode transistors, JEFETs from Semisouth, BJTs from TranSiC and MOSFETs from CREE. All the selected devices have a brake-down voltage of 1200V and a continuous current rating of approximately 20A. Based on the availability of samples one JFET and one BJT were selected for lab testing. The BJT sample was unfortunately only a 6 amps device. The following sections explain the operation of the different devices and show calculations of the required driving powers. All calculations are based on values from the data sheets of the devices and the operation conditions are V_{dc}=600V, I=20A and f_s=15kHz. The calculated driver power is the power required for driving the device, when the gate driver power supplies are dimensioned also the efficiency of the driver must be accounted for.

3.3.1 JFET

The JFET form Semisouth is of the type SJEP120R063, data sheet is available at [37]. The transistor can block forward voltages up to 1200 V. The maximum continuous drain current is 30 A when the junction temperature is 125 ˚C. Maximum junction temperature (T_j) is 175 ˚C, but the limitation is due to the packaging of the device.

3.3.1.1 ***Device structure***

Figure 3-2 and Figure 3-3 shows the cross-section of the transistor.

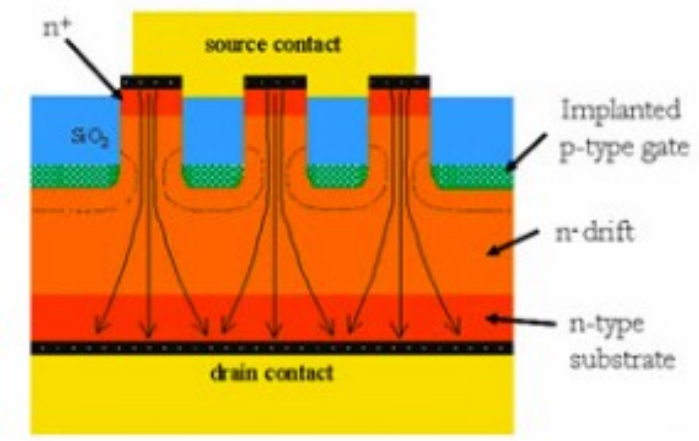

Figure 3-2 Cross-section of a enhancement mode SiC J-FET [38]

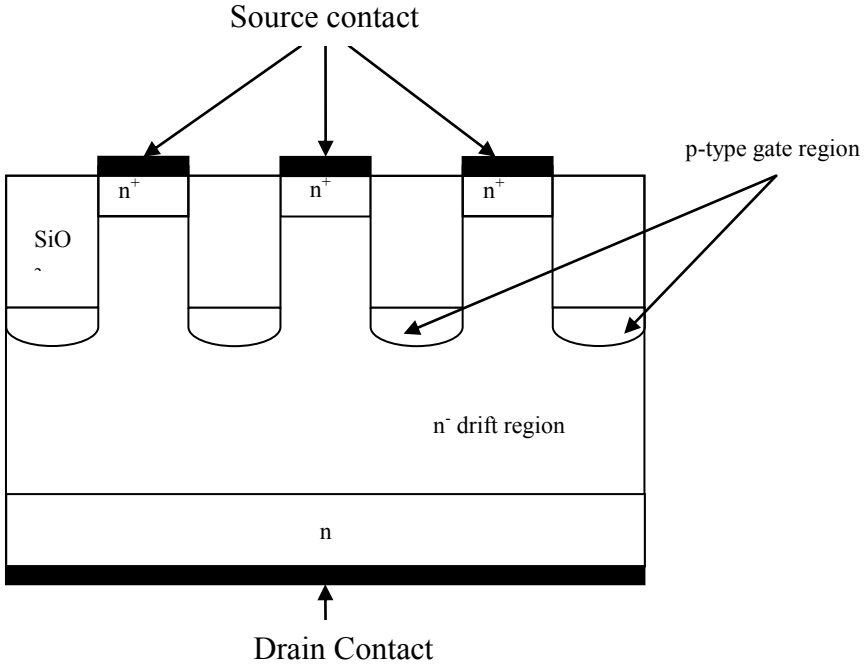

Figure 3-3 Cross-section of a enhancement mode SiC J-FET

In contrast to normally-on devices, which usual have a lateral structure, the enhancement mode J-FET from Semisouth has a vertical channel. The finger width is made so small that the depletion layer, of the pn-junction between gate and source, pinches off the channel when no voltage is applied at the gate i.e. V_{GS}=0. When a positive voltage, V_{GS}, is applied and the input capacitance is charged the junction becomes forward biased and the depletion region is removed. When the depletion region is removed the drain and source are connected through the n-channel. Hence, the device starts to conduct when a positive voltages is applied between drain and source, V_{DS}. If a continuous gate-source voltage is increased far beyond 3V the pn-junction will

start to conduct a high current and there will flow an excessive gate current, which will eventually destroy the gate. The JFET has a highly integrated gate structure in contrast to MOSFETs and IGBTs. This complicates switching due to the coupling between the gate source capacitance and the voltage dependent gate drain capacitance. Figure 3-4 shows the Schokley equivalent schematic of the device. This model does not describe vertical JFETs very accurately, but is gives some approximations.

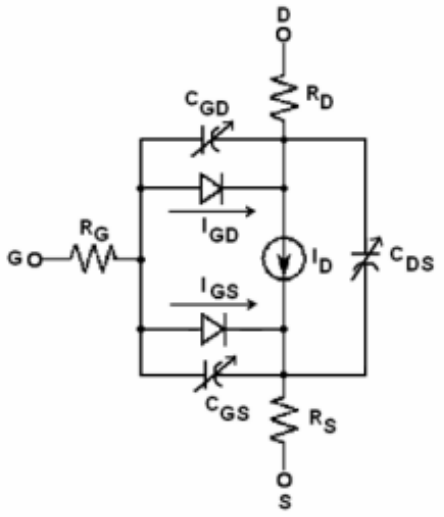

Figure 3-4 Schematic representation of the SiC JFET [39]

The capacitances of the JFET vary with voltage; this is the same as for MOSFETs and IGBTs. The SiC JFET has much lower intrinsic capacitances than comparable Si MOSFETs [39] and is therefore able to switch much faster. Extra care must be taken when the JFET is used in a bridge configuration due to the low threshold voltage of approximately 1V.

3.3.1.2 *Required driving power*

Due to the low threshold voltage, the application note suggests that a driver with a bipolar output is used. It is also recommended to use a clamping capacitor between gate and source to stabilize the gate voltage. The calculations below are based on a driver which has an output of 2.5V and -15V.

Even though the JFET is classified as an unipolar Field Effect Transistor it has some bipolar characteristics. The gate structure of the device is a pn-diode and is somehow similar as for BJTs. To obtain a low on-state resistance, at high temperatures, some continuous gate current has to be applied. This is different from other FET transistors like the MOSFET and the IGBT. The required driving power is therefore the sum of the charging power for charging C_{GD} and C_{GS} and power for supplying the continuous current.

If a gate voltage of 2.5 V is applied then the gate-source current is less than 0.01A at a junction temperature of 25 ˚C and 0.35A at 150 ˚C. The maximum drain current at150 ˚C and V_{GS} = 2.5V is approximately18A. The on-state driving losses can be calculated from equation (2.10). This gives $P_{onstae}(T_j = 25) = 0.025 \cdot D$ [W] and $P_{onstae}(T_j = 150) = 0.875 \cdot D$ [W]. To operate with 20A at 150 ˚C a gate voltage of 3V is required. The resulting gate current is 1.56 A.

The gate charge curve from the data sheet is shown in Figure 3-5. No data is given for gate voltages lower than zero volts. Hence, the required charge for lifting the voltage from minus 15 to 0 must be calculated. The gate source capacitance (C_{GS}) is a junction space charge capacitor, which means the capacitance is dependent on the width of the depletion layer. By assuming that it behaves as a parallel plate capacitor the capacitance can be expressed as [9]:

$$C_{SC}(V) = \frac{\varepsilon}{W(V)} \tag{3.6}$$

Where ε is the relative permeability and W(V) is width of the depletion layer expressed by:

$$W(V) = W_o \sqrt{1 - \frac{V}{\Phi_C}} \tag{3.7}$$

W_o is the depletion layer at zero voltage bias, ϕ_c is the contact potential of the junction and V is the applied voltage. By combining the two equations above and using the value of C_{GS} at zero gate voltage (C_o) to eliminate ε and W_o the additional charge can be expressed as

$$Q_{-15} = C_o \int_{-15}^{0} \frac{1}{\sqrt{1 - \frac{V}{\Phi_C}}} dV \tag{3.8}$$

The contact potential depends on the doping level and the temperature, ϕ_c was set to 3V to get an estimation of the charge. By performing the integration the charge was calculated to 12.6nC. The effect of charging the gate drain capacitance in the period where the driver voltage goes from -15 to 0 can be neglected due to the low value of the capacitance at high reverse voltages. This gives a total charge of 12.6nC + 60nC = 72.6nC. If an external clamping capacitor is connected between the gate and the source, this also requires addition charge from the driver. The suggested capacitor of 4.7nF requires 4.7nF·(2.5+15)V = 82.25nC. The charge supplied by the driver is then equal to 154.85nC. At a switching frequency of 15kHz equation (2.8) gives a charging power of 0.041W.

The total required driving power at T_j =25 ˚C and T_j =150 ˚C are 0.065W and 0.872W respectively and the average driving power during inverter operation are (D=0.5) 0.054W and 0.479W. Table 3-4 summarizes the calculated values.

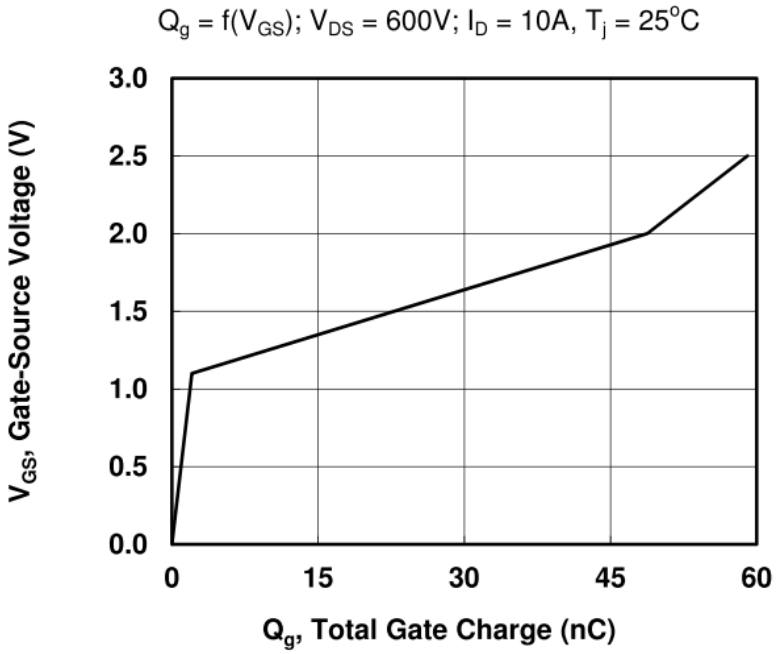

Figure 3-5 Gate charge curve [37]

Driving requirements for SJEP120R063		
T_j	**25 ˚C**	**150 ˚C**
Q_G	154.9 nC	154.9 nC
I_g	10mA	350mA
V_{DRV}	2.5V, -15V	2.5V, -15V
P_{charge}	41mW	41mW
$P_{onstate}$(D=0.95)	24mW	831mW
$P_{onstate}$(D=0.5)	13mW	438mW
P_{drive}	65mW	872mW
$P_{average,drive}$	54mW	479mW

Table 3-4 Driving requirements for SJEP120R063 T_j=25 ˚C and T_j=150 ˚C

3.3.2 BJT

The BJT from TranSiC is the BT1220AC, the data sheet can be obtained by sending a request to [40]. The BJT can withstand a forward voltage of 1200V and has a rated current of 20A at T_j = 150 ˚C. Maximum operating junction temperature is 175 ˚C, as for the JFET this is limited by the packaging. A High temperature version of the device is also available. The calculations for the BT1206AC are also performed.

3.3.2.1 *Device structure*

There are no available descriptions of the device structure, so the description is based on understanding of the switching waveforms shown in the data sheet and in other publications. The high value of the critical electrical field in SiC makes it possible to produce very thin devices. When making the devices thinner the carrier life time can be reduced. From the switching waveforms and data sheet characteristics one can see that the BJTs have no quasi saturation region. One can also see that the devices have no tail current at turn on. These observations confirm that the injected carrier life is very short. As a result, the operation of the SiC BJT is very similar to that of a unipolar device.

3.3.2.2 *Required driving power*

Neither the base charge curve nor the total base charge at a certain voltage is given in the data sheet. The base charge is therefore estimated as the sum of the base-collector

and base-emitter charge. This is a valid approximation since the driving power is totally dominated by the continuous base current for normal operation frequencies. Table 3-5 gives the driving requirements for the two devices. The calculations are based on formulas in section 2.4.1.

Driving requirements for BJTs		
Device	**BT1220AC**	**BT1206AC**
Q_G	222 nC	53.5nC
I_b	700mA	300mA
$V_{DRV} = U_{BE(sat)}$	3.2V, 0V	3.2V, 0V
P_{charge}	10.7mW	2.6mW
$P_{onstate}(D=0.95)$	2.128W	0.912W
$P_{onstate}(D=0.5)$	1.12W	0.48W
P_{drive}	2.139W	0.923W
$P_{average,drive}$	1.131W	0.483W

Table 3-5 Driving requirements for BT1220AC and BT1206AC

The required gate charges presented in the tables are unrealistic low. To be able to switch the devices at desired speeds an extra speed-up/bypass capacitor has to be used. This capacitor needs to be charged and discharged every switching cycle and this contribution can be significantly larger than the Q_G calculated from the data sheet. A two-stage DC coupled driver can be used instead of the speed up capacitor to improve the efficiency.

3.3.3 MOSFET

The MOSFET CMF20120D is produced by CREE and data sheet can be found at [41]. The device can withstand a forward voltage of 1200V and has a rated current of 33A at $T_j = 25$ ˚C.

3.3.3.1 *Device structure*

CREE has not published papers on the structure of the device. As stated in 3.1.1, the channel mobility in SiC is much lower than in Si. To obtain a low on-state resistance of the MOSFET the channel must be made as short as possible. By using a UMOS structure several short channels are connected in parallel. A qualified guess would therefore be that the CREE MOSFET has an UMOS structure.

3.3.3.2 *Required driving power*

It is recommended to use a bipolar driving voltage with V_{GS} equal to 20V and -2V. The MOSFET has no continuous gate current, thus the total drive power is equal to the charging power, P_{charge}. One major difference between the MOSFET and the two other devices is that the MOSFET has an internal freewheeling diode. The forward voltage of the diode is typically between 3 and 3.5V at 10A, but varies with the gate-source voltage. The more negative V_{GS} is the higher the forward voltage becomes. The table below shows the drive requirements of the MOSFET.

Driving requirements for CMF20120D	
Q_G	90.8 nC
I_g	0A
$V_{DRV} = V_{GS}$	20V, -2V
P_{charge}	30mW

Table 3-6 Driving requirements for CMF20120D

The gate charge, Q_G, is given for V_{DC} equal to 800V so the gate charge at 600V should be somehow smaller. The input capacitor is almost constant when the voltage changes from to 600 to 800, thus the error when using Q_G(800V) is small.

3.4 Theoretical efficiency comparison between available SiC transistors and a state-of-the-art Si IGBT

This section presents a theoretical inverter efficiency comparison between three available SiC transistors and a state of the art IGBT. In addition to the requirements given section 2.4, it was decided that the device packages should be of the type TO-247. The selected IGBT was the IKW15T120 and the data sheet can be found at [28].

Driving requirements for IKW15T120	
Q_G	85 nC
I_g	0A
$V_{DRV} = V_{GS}$	15V, 0V
P_{charge}	19 mW

Table 3-7 Driving requirements for IKW15T120

The data sheet of the CREE MOSFET gives only data for junction temperatures up to 125 ˚C. It was therefore decided to compare the devices at 25 ˚C and 100 ˚C. In the comparison the peak fundamental output current is set 20A, the DC-link voltage to 600V and the modulation index to 1. This gives a line-to-line output voltage of approximately 367.4V and an output power of 9kW at unity power factor. The selected freewheeling diode was a SiC Schottky diode from Infineon, IDH15S120. Even though both the MOSFET and the IGBT has freewheeling diodes, inside their package, the IDH15S120 is used to make the comparison as fair as possible. The tables in appendix B show the estimated parameters from the data sheets. There are some uncertainties regarding these values that the reader should know about. Some of the values are found by interpolation between nonlinear graphs. The IGBT switching losses includes the losses due reverse recovery in the internal diode, this overestimates the switching losses. For the devices were the switching losses was given at another voltage level than the one selected here equation (2.22) was used to make an estimation. When calculating the driving power the efficiency of the driver and the driver power supply should be included. The largest uncertainties are related to the selected switching speeds of the devices. By changing gate resistors and speed up capacitors the switching speed can be adjusted, and therefore also the switching losses. Increased switching speed gives lower losses but also more oscillations, higher dV/dt and more EMI. This means that a conservative manufacturer, which tolerates only small oscillations, will give high switching losses relatively to other manufacturer. The performed comparison must therefore only be used as estimation.

PM machines are usually designed for power factors in the range of 0.90-0.95 at rated conditions [42]. It was therefore decided to compare the transistors when the power factor of the inverter was set to 0.95. This gives a converter output power of 8.55kW. A Matlab script based on the formulas in section 2.4, see appendix A1, was used to calculate the theoretical inverter losses and the inverter efficiency. The calculations were based on the simplified linear approach. Figure 3-6 and Figure 3-7 shows the total inverter losses, and also how the losses are dived, for T_j=25 ˚C and T_j=100 ˚C respectively. Table 3-8 shows a summary of the total inverter losses and efficiencies.

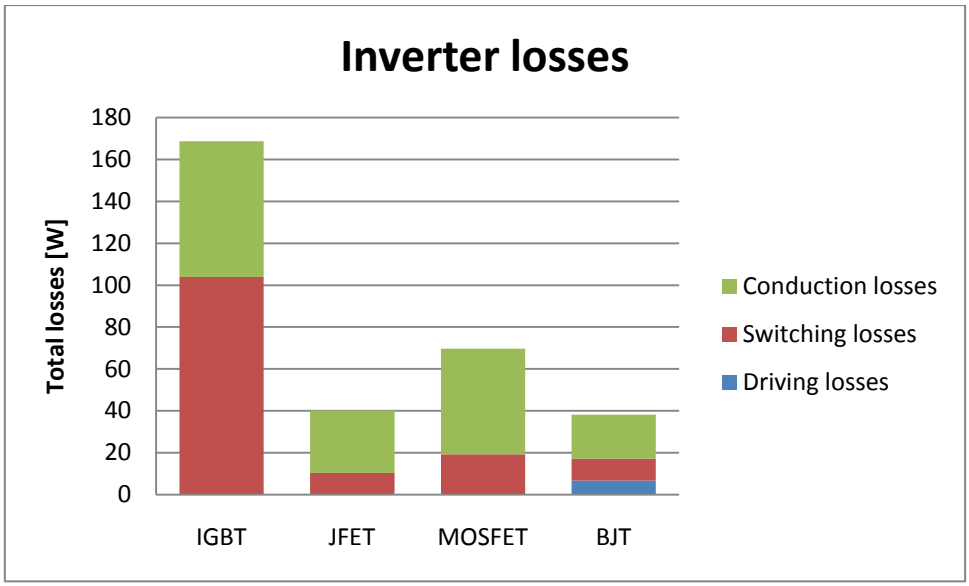

Figure 3-6 Inverter losses at T_j=25 ˚C

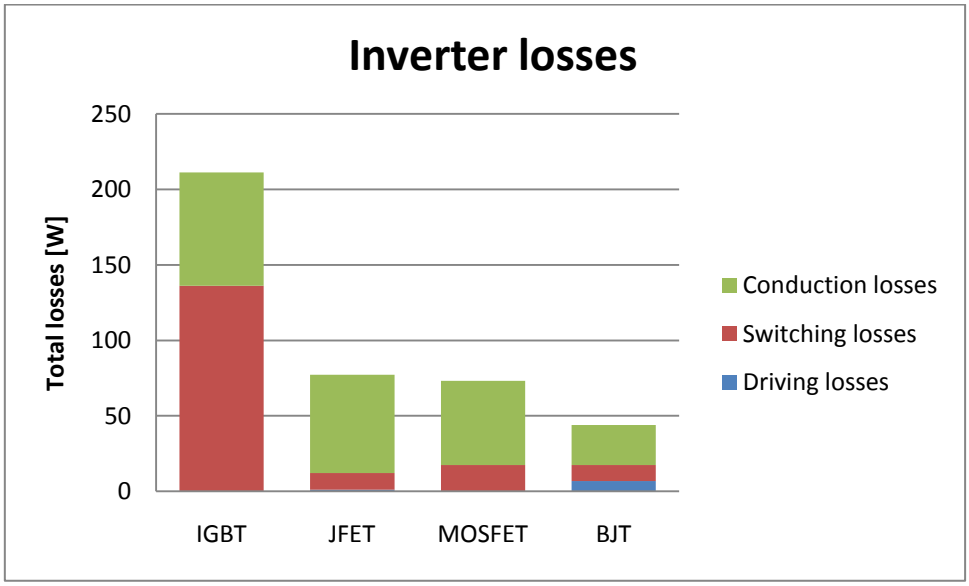

Figure 3-7 Inverter losses at T_j=100 ˚C

	T_j=25 ˚C			**T_j=100 ˚C**		
	Driving	Total	Efficiency	Driving	Total	Efficiency
IGBT	0.11 W	168.7 W	98.06 %	0.11 W	211.3 W	97.59 %
JFET	0.32 W	40.2 W	99.53 %	1.00 W	77.2 W	99.11 %
MOSFET	0.18 W	69.7 W	99.19 %	0.18 W	73.2 W	99.15 %
BJT	6.79 W	38.3 W	99.55 %	6.79 W	43.8 W	99.49 %

Table 3-8 Total inverter losses and efficiencies

The conduction and switching losses of the freewheeling diode are included in the figures. From the results one can see that BJT based inverter has the lowest losses. The MOSFETs and the JFETs have almost equal losses at T_j=100 ˚C. The JFETs have higher efficiency at low temperatures while the MOSFETs have slightly higher efficiency at high temperature. If the temperature is further increased the MOSFETs will outperform the JFETs. The on-resistance in an unipolar device has a high positive

thermal coefficient. This is the reason why the conduction losses in the JFETs have a dramatic increase when the temperature is increasing. For the MOSFETs, there are two factors contributing to the on-resistance. These are the resistance of the drift region and the channel resistance. As stated earlier, the channel mobility in SiC is much lower than for Si. Luckily, the channel mobility increases with increasing temperature, and lowers the channel resistance. This effect counteracts the high positive thermal coefficient of the drift region and gives the MOSFETs a rather low thermal coefficient for the on-resistance. The driving requirements of the JFETs increase when the temperature increases. All the SiC based inverters have more than 1% higher efficiency than the Si IGBT at T_j=25 ˚C, and more than 1.5% higher at T_j=100 ˚C. From the loss distribution, one can see that the switching frequency is too high for the IGBT.

4 Design of Converters and Control Circuits

This chapter explains how the two half-bridge converters were designed, including PCB layout, driver design and selection of isolated power supplies. To be able to test the converters under continuous operation, a control circuit has to be made. The selection of controller depends on the converter topology and the mode of operation. To produce a three phase output, which is required in most motor drives, one needs three bridge legs. Due to the time limitation of this work it was not possible to build all three legs and implement motor control. Hence, it was decided to test the half-bridges as synchronous buck converters or as a step down converter. Section 4.5 and 4.6 present the design of output filter and of the control circuit.

The control circuits are principally the same for both transistor types, but the required controller gain becomes different due different current ratings of devices. The BJTs and JFETs have different gate drivers, and therefore also different propagation delay from input to output. Hence, the controller dead time is different for the two converters. It was therefore decided to only design a controller for the JFET half-bridge.

4.1 Half-bridge converter specifications

One of the main objectives in this work was to design and test two half-bridge converters based on two different SiC transistors. The criteria for selecting the transistors were that; they should be normally-off devices, their voltage class should be 1200V and their rated current should be higher than 10A. When this work was initiated there were only two available SiC transistors which could meet these criteria, namely the SJEP120R063 JFET from Semisouth and the BT1220AC BJT from TranSiC. Due to long delivery times on the BT1220AC the device was replaced with the BT1206AC, which is a 6 Amps device. Both transistors are delivered in TO-247 packages.

It was decided to make the converters on a Printed Circuit Board (PCB) to have a compact design. Before making the layout of the board some Design Rules (DR), like the clearing distance and the trace width, must be calculated. The DR are depending on the current and voltage ratings of the converter. Even though the current ratings of the devices are different it was decided to use the same DR, based on the required converter ratings presented in section 1.2, for both half-bridges. The trace width is dimensioned for a load current of 10A, and the clearing distance is calculated for 1000V. The maximum voltage is set two times higher than DC-link voltage, V_{dc}=500V, to be sure that no flashovers occur during the switching transients. The selected board is two sided and has 70 μm of copper. An extract of the project work [10], which describes how the DR were calculated, is given in appendix C. The result of the calculation gave a clearing distance of 3mm and a minimum trace width of the power traces of 3mm.

Due to their fast switching and their lack of reverse recovery current it was decided to use SiC Schottky barrier diodes as freewheeling diodes. Two different diodes were selected; SDP30S120 from Semisouth and IDH10S120 from Infineon, both can block reverse voltages of 1200V. The SDP30S120 has a rated forward current of 30A and IDH15S120 has a rated forward current of 15A.

To be able to test the SiC devices at elevated temperatures, the design shown in Figure 4-1 was used. The green plate is the PCB, the yellow layer is thermal insulation. The transistors and the freewheeling diodes are screwed down on the large heat sink.

Figure 4-1 Heat sink layout

By using external heating the temperature of the heat sink, and thus also the casing of the SiC devices, can be adjusted. The heating is performed by placing the heat sink on a cook plate. The heat sink is over dimensioned and has a lower thermal resistance than what is necessary for normal operation of the converters. Thermal isolation is required to protect the rest of the circuit against excessive heating.

4.2 PCB layout considerations

As stated earlier, SiC transistors can switch much faster than their Si counterpart. The low switching times can cause large problems in form of high dV/dt and high di/dt. Hence the layout of the circuit is very important. Bad layout can easily lead to large oscillation and over voltages. None of the selected SiC transistors have the tail current phenomena which are observed in silicon IGBTs. The lack of tail current reduces the switching losses at turn-off, but it also reduces the damping of oscillations since tail current losses introduce a parasitic damping

To reduce the over voltages at turn-off it is important to minimize the stray inductances of the paths where the current changes quickly. The induced overvoltage is proportional to the value of the inductances and the rate at which the current changes, see equation (2.1). The most critical loop is the one consisting of the DC capacitor, the transistors and the freewheeling diodes. Figure 4-2 shows the stray inductances in this loop. The real inductance is distributed along the traces but they are showed as lumped inductances for illustrative purpose. Initially Q1 is conducting and the current has the direction shown in the figure. Due to the inductance, which is present in most loads, the current can be modeled as constant current source when looking at one switching period. When Q1 is turned off the load current commutates to the diode D2. This leads to high di/dt in the stray inductances L2, L3, L6, L4 and in the parasitic inductance of the capacitor. Hence the path including C, Q1 and D2 should be minimized. The same arguments are valid for the path C, Q2 and D1.

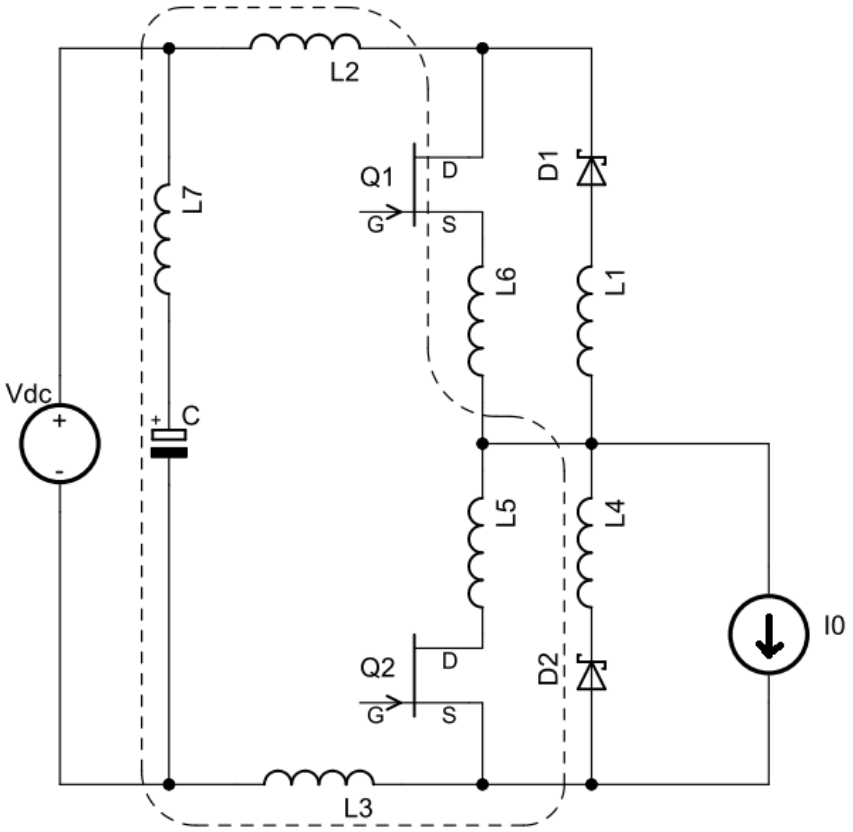

Figure 4-2 Stray inductance in power loop

The inductance of a rectangular loop can be calculated from the following formula [43]:

$$L = \frac{\mu_0}{\pi}\left[l \cdot \ln\frac{2d-w}{w} + d \cdot \ln\frac{2l-w}{w}\right] \quad (4.1)$$

Where l and d are respective length and width of the rectangle, w is the trace width of the conductor and μ_0 is permeability of air. The inductance increases with increasing area and decreases with increasing trace width. This means that the area of the loop should be minimize and the trace width should be made as large as possible. Table 4-1 shows an example of how the inductance in 8 cm long loop changes for different parameters.

Self inductance in a 8 cm long loop given in nH				
	Distance between the traces (d):			
Trace width (w):	5 mm	10 mm	30 mm	50 mm
1 mm	20.1	28.6	47.8	62.1
3 mm	8.8	17.8	35.4	47.6
4 mm	5.1	14.8	32.1	43.7

Table 4-1 Self inductance of a 8 cm long loop

The mutual inductance of two loops is depending on the distance between the loops and on how large their common area is. Close loops have high mutual inductance.

The leads connecting the DC-link to the PCB introduce a relatively large inductance. To reduce this inductance it is common to place a decoupling capacitor on the PCB. The capacitor then decouples the inductance of DC-link connection, and thus reducing the

effective area of current loop drawn in Figure 4-2. The decoupling capacitor also contributes to stabilize the DC voltage during switching. The half bridge PCB was therefore designed with two 4.7 µF capacitors in parallel.

Another way to reduce the inductance is to use earth planes and strip line connections. It is called a strip line connection when the current trace is right on top of the return path, see Figure 4-3.

Figure 4-3 Strip line connection, the copper traces are white while the insulating PCB is green

This gives a very low area of the loop since the width is only the thickness of the PCB. To keep the inductances as low as possible the boards were designed with two power planes. The downside was connected to the negative DC voltage, which is grounded, and the upper plane to the positive DC voltage.

To fully understand the switching behavior of the transistors the stray capacitances should also be included in Figure 4-2. Figure 4-4 shows a redrawing of the half-bridge circuit where a RLC load is connected between the mid-point and ground, and the converter is operating as SBC. The capacitances C1-C4 represent the stray capacitances of the semiconductor devices, while C5 is stray capacitance of the filter inductor LF. The device capacitances are very voltage dependent. In combination with the stray inductances these capacitances create both current and voltage oscillations. During turn-on, the device capacitances will discharge/charge trough the transistor which is switching. This gives a current overshoot which is only limited by the switching speed and the stray inductances in the current path. The inductor capacitor, C5, introduces a current spike every time Q1 is turned on. Unlike the stray inductances, the stray capacitances cannot be changed by changing the layout. The only way to reduce C1-C4 is to select new devices with smaller intrinsic capacitances. C5 is depending of coil selection. The stray capacitance of a winding increases with decreasing distance between the turns and also with increasing potential differences between neighbor turns. Hence, the focus for PCB designer must be to minimize the stray inductances and to adjust the switching speed such that switching waveforms are acceptable. There are also some inductances that cannot be changed; these are the inductances of device packages. Figure 4-5 shows typical package inductances for the BitSiC1206.

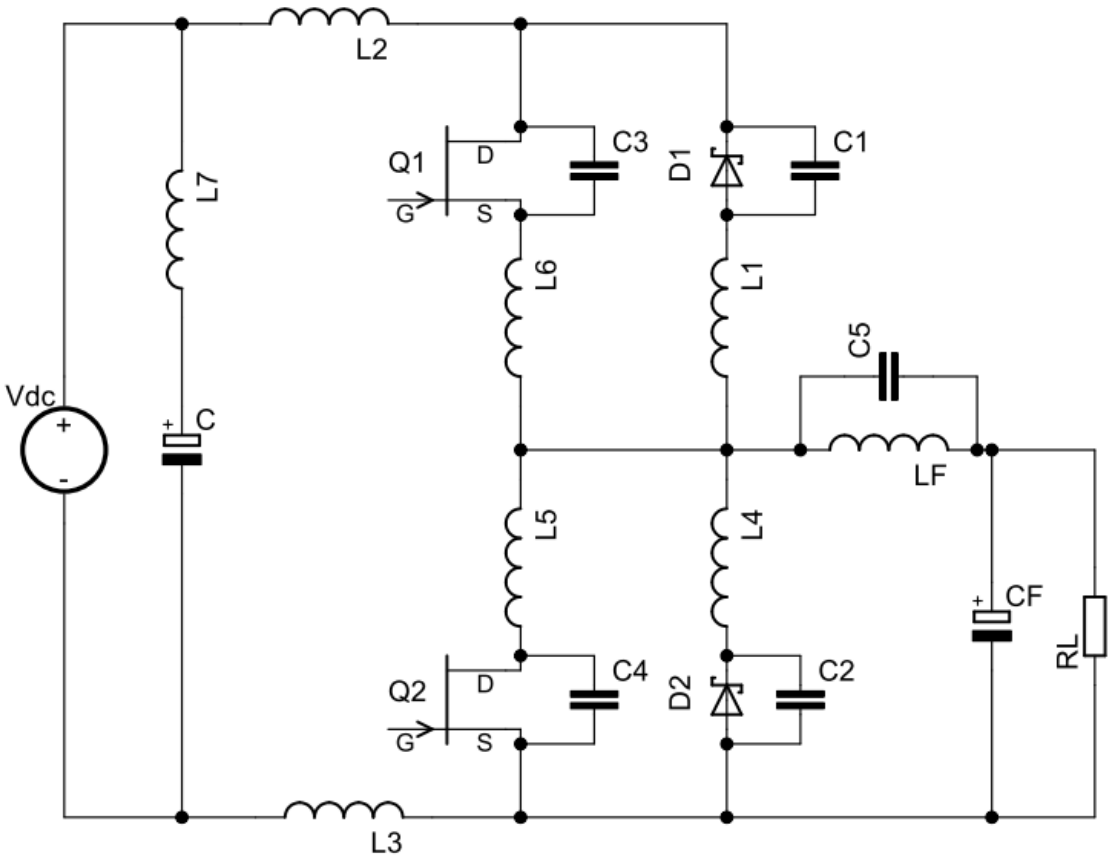

Figure 4-4 Stray capacitances in half-bridge circuit

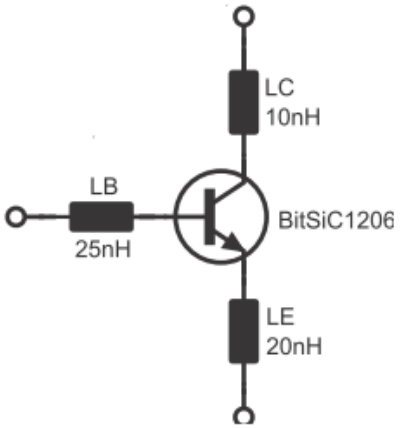

Figure 4-5 Package inductance of BitSiC1206 TO-258/To-247 [44]

A smart connection of the drive circuits is important to obtain good switching results without oscillation. The conductors connecting the transistor to the driver should be as short as possible. There should be no common conductor where both the load and driver currents flow. A common conductor can induce voltages which will slow down the turn off and can also be a source of oscillations [9]. It is smart to look at the transistor as a four terminal device where the driver has its own source contact. The length of the conductors and area of loop connecting the driver to the transistor should be minimized to reduce the inductance and also to reduce the coupling with the power circuit.

4.3 Gate/base driver design and selection

Different transistors have different driving requirements. It is important to use a driver which meets these requirements to fully utilize the different devices. The following sections describe the driver design and selection for the JFET and the BJT.

4.3.1 JFET gate driver

In previous work [10] it has been shown that, in a bridge configuration, the turn-on of one JFET can lead to transiently turn-on of the other, due to the Miller effect. This is called a shoot trough and the result is high currents and excessive losses in both transistors. The Miller capacitance is the capacitor between the gate and the drain. When the JFET is exposed for high dv/dt, e.g. when the other transistor in the bridge leg is switching, there will flow a charging current through the Miller capacitance. The current will flow according to $C \cdot dV/dt$. It is therefore important to have a gate driver with low impedance which can sink this current. The current flowing through C_{GD} creates a voltage drop across the internal gate resistance of the device and the gate resistance of the gate driver. This voltage charges the C_{GS} capacitor, and the JFET will turn on if the voltage over the gate-source capacitance reaches the threshold level. For very fast voltage transients it can be showed that there will be a capacitive voltage distribution between C_{GD} and C_{GS} [45]. The derivation in [45] was made for a MOSFET model, but the result should be valid also for JFETs.

The low threshold voltage of the device makes it very sensitive to false triggering. By connecting an external capacitor between the gate and the source of the JFET the voltage rise due to charging current is decreased [39] . The capacitor will stabilize the gate voltage but probably slow down the switching, since more charge needs to be supplied by the gate driver at turn-on. The application note of the device suggests using a capacitor with a value between 1-5nF. It was decided to be conservative and use a 4.7nF capacitor.

A gate driver from Semisouth, SGDR600P1 , was selected to drive the JFETs. The gate driver has a two stage output. During the first 100 ns of the turn-on the gate source voltage is boosted to 5V before it drops down to its stationary on-value of 3V. This leads to greatly reduced turn-on times. The gate driver output voltage is plotted in Figure 4-6.

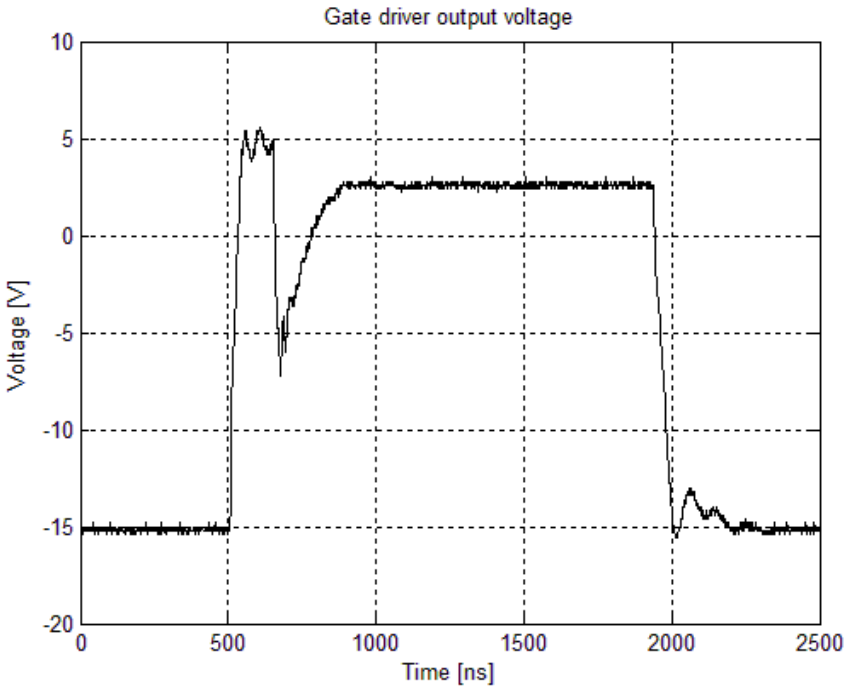

Figure 4-6 Gate driver output waveforms

When the transistor is off, the gate driver supplies a negative voltage of minus 15 V. By applying the negative voltage, the noise immunity is increased and the probability for uncontrolled turn-on is reduced.

If the high switching speeds results in excessive EMI or ringing the switching speed should be reduced. This can be done by adding a series resistor between the output of the gate driver and the gate contact of the J-FET. The selected resistor should have no inductance to avoid oscillations and induced voltages. Tuning of the gate resistance is shown in chapter 7.1.

From the driver data sheet, which can be found at [37], one can find the required driver supply power. When operating, the SJEP120R063, at a duty cycle of 100% and a switching frequency of 50kHz, the required power is 2.4W. The SGDR600P1 requires an input supply voltage of ±15V. As describe in section 2.3.1, the supplies of the two drivers must be isolated from each other and the supply voltage of the upper transistor must be isolated from ground. To meet these requirements and to obtain galvanic isolation on the PCB, two Traco DC to DC converters where selected. If the input voltage is in the range of 9-18V the Traco will supply the gate driver with ±15 V. The maximum supplied power is 5W.

4.3.2 BJT base driver

The BJT is a current controlled device, which means that the operation region of the device is decided by the amount of current injected into the base. The maximum collector current is given by the product of the base current and current gain. To obtain a low on-state voltage and keep the transistor in the saturated operation region, it is recommend to overdrive the base current with 50% [44]. The current gain is increasing with increasing collector current and decreasing with increasing temperature. There are basically to ways to drive the device, either by applying a base current which is proportional to collector current or by applying a constant base current. The latter solution is least complex and was therefore selected. The current gain at T_j=175 ˚C and

I_c=6A is approximately equal to 30. By using 50% overdrive the required base current is 0.3A. A MOSFET driver IC, TC4421AVPA from Microchip, with high peak current capability was selected for driving the BJT. The input voltage of the IC should be in the range 4.5-18V and the output resistance (R_{out}) is 1.25 Ohms. It was decided to supply the IC with 15V. The size of external gate resistance must be selected such that DC output current becomes 0.3A. An expression for the gate resistance is given below.

$$R_g = \frac{(15 - V_{BE})}{I_b} - R_{out} \tag{4.2}$$

V_{BE} is the forward voltage drop of the base emitter diode and is approximately 3V for Silicon Carbide and I_b is the required base current. This gives a gate resistance of 38.75Ω. A 39Ω resistor was used in the final design.

Current controlled devices are generally more noise immune than voltage controlled devices since they require an injected current to turn on. However, when the BJTs are exposed to high dV/dt a capacitive current is injected into the base through the base-emitter capacitance. This can occur in a bridge leg when one transistor is switching and the other is off. The gate driver should therefore be able to sink the injected base current.

SiC BJTs stores very little charge during forward conduction compared to silicon bipolar transistor. However, a significantly base current peak is required to quickly charge the parasitic capacitances between the base and the collector, the Miller capacitance. The same current peak will also rapidly charge the base emitter capacitance and therefore minimizing the turn-on delay. The same current peak, but in negative direction is required to obtain a fast turn-off. The value of the required charge is very voltage dependent and can be found in the data sheet of the device. A speed up capacitor with a series resistor, connected in parallel with the gate resistor, can be used to supply the charge. A larger capacitor value gives a higher current peak and therefore faster switching. Based on the recommended values in the data sheet, and some simulations in LTspice, it was decided to use a 22nF capacitor with a one Ohm series resistor. An optocoupler was selected for signal isolation. The driver schematic is shown in Figure 4-7. Both the optocoupler and the driver IC have inverting outputs, and the pull-up resistor R1 is used to keep the input to the IC high, when the control signal to optocoupler is low. Two Traco 6W isolated DC/DC converters were selected to supply the drivers. Figure 4-8 shows the output waveforms of the driver.

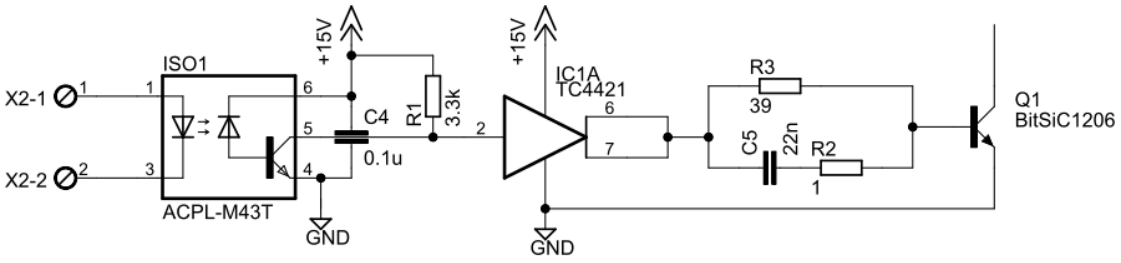

Figure 4-7 BJT driver schematic

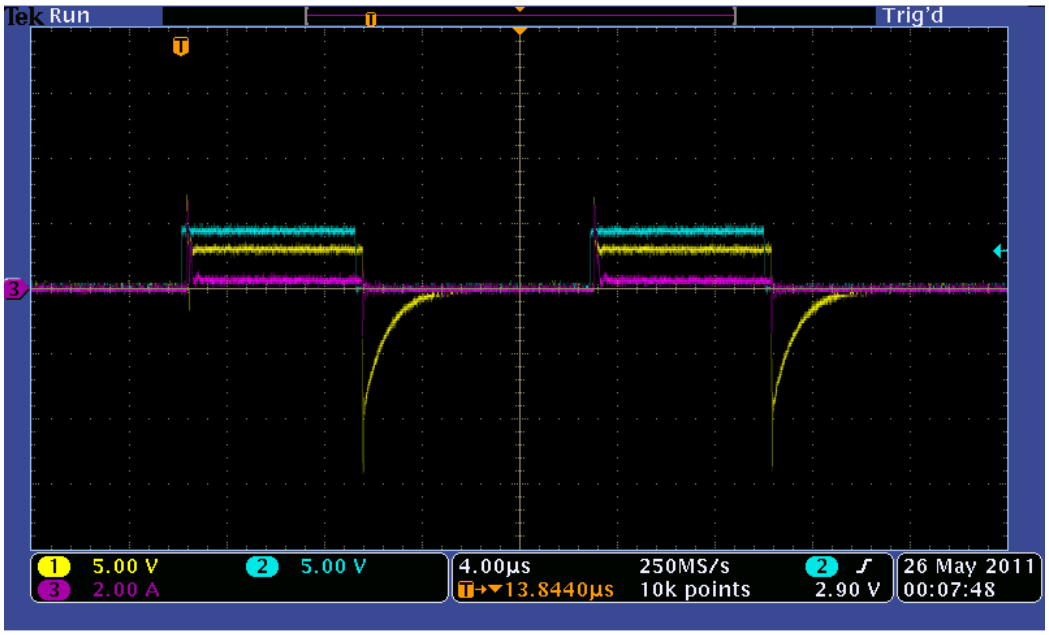

Figure 4-8 BJT driver operation, the input voltage to the optocoupler is turquoise, the output voltage is yellow and base current is purple

4.4 Converter schematic and PCB layout

The Eagle software was used to draw the converter schematics and to design the PCB layouts. The boards were design according to the design rules and layout consideration presented in the previous sections.

4.4.1 JFET schematic and layout

Figure 4-9 shows the schematic of the half-bridge converter based on the JFETs. The schematic of the gate driver and DC/DC converters can be found in appendix D1. VG1, VS1, VG2 and VS2 in the figure are the connection to the drivers.

In the figure the Xes are connectors, TP are test points, D3, D4, D7 and D8 are zener diodes. The zener diodes are included to protect the gates from over voltages. Maximum gate voltage of the JFETs is ±15V. R1 and C6 create a voltage snubber which damps the voltage oscillations. The gate resistances R3 and R4 are mounted in a socket such that easily can be changed. The gate drivers, IC3 and IC4, are also mounted in a socket to make it possible to place them on top of the transistors.

The layout of the board is shown in Figure 4-11. The dotted lines show the boarders of the power planes. Separate layout of the top and bottom layer can be found in appendix D2.

Figure 4-10 shows a picture of the final converter. A full Bill Of Material (BOM) can be found in appendix E1.

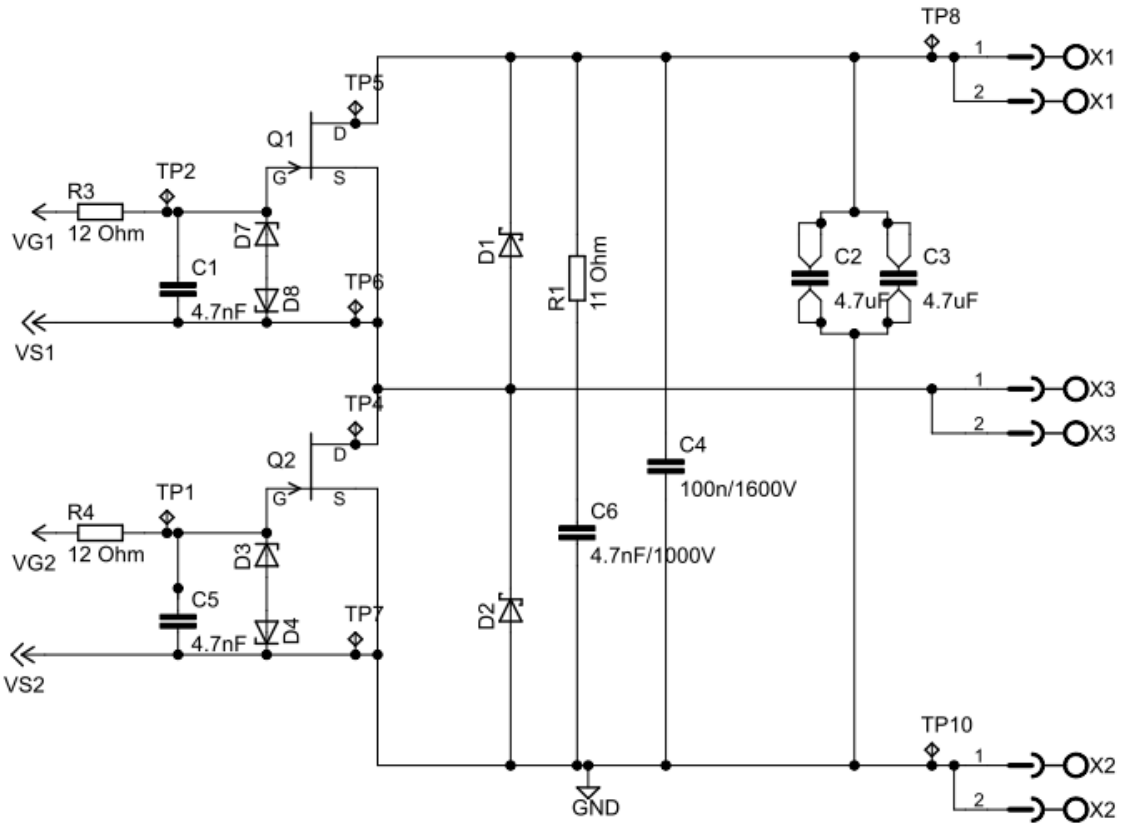

Figure 4-9 JFET half-bridge schematic

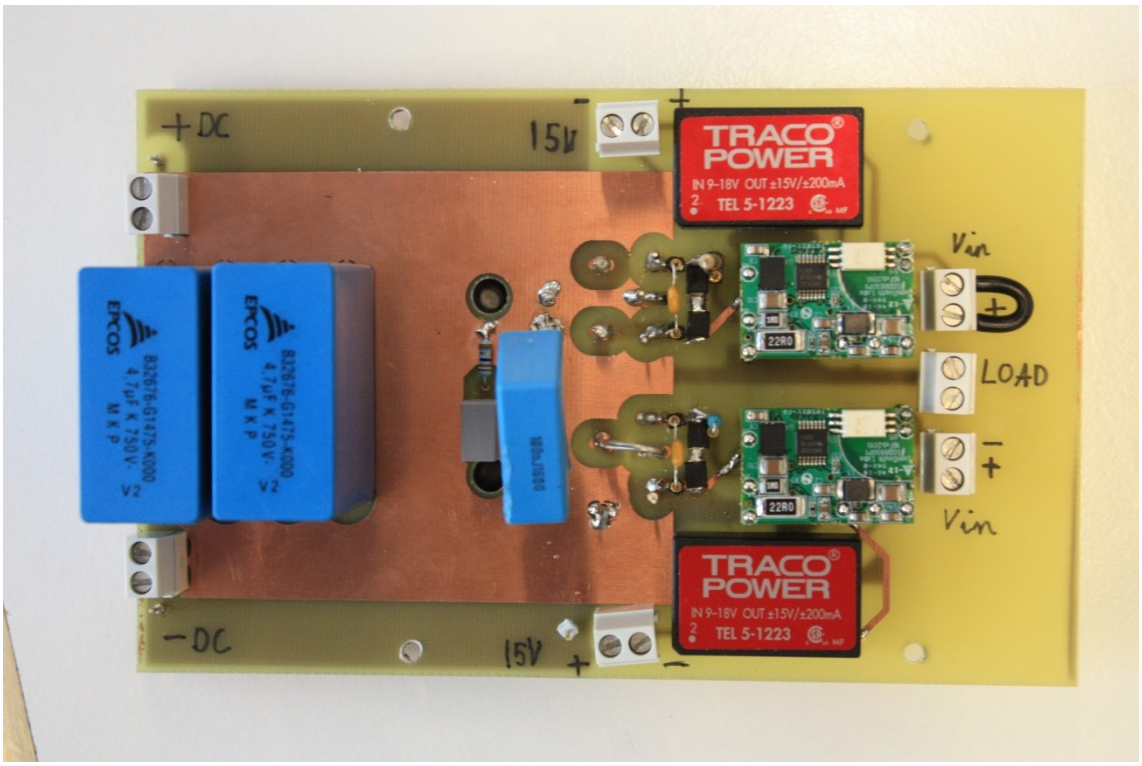

Figure 4-10 Picture of JFET half bridge

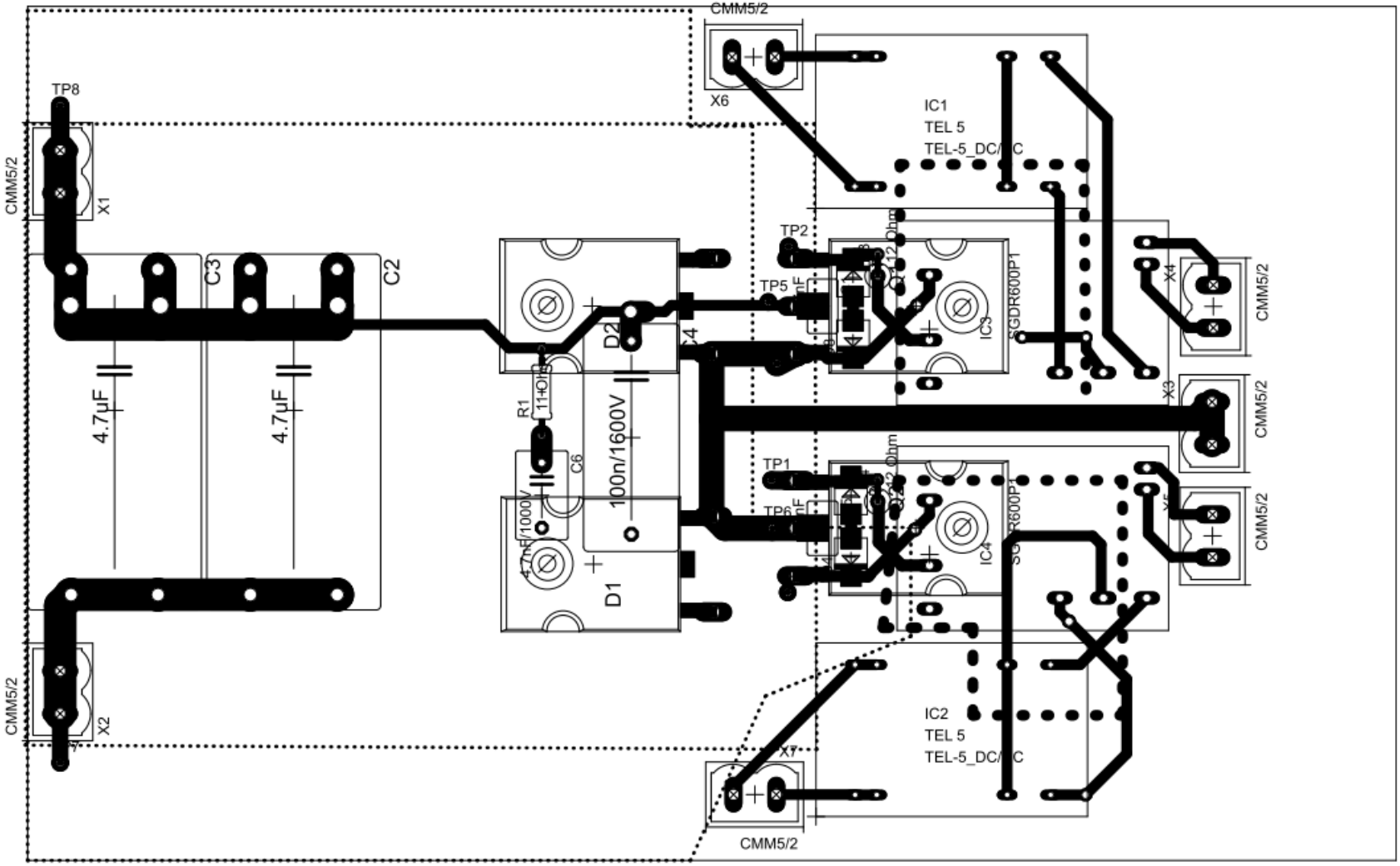

Figure 4-11 JFET half-bridge PCB layout

4.4.2 BJT schematic and layout

Figure 4-12 shows the schematic of the power stage of the half-bridge converter based on the BJTs. The schematic of the drivers and the isolated power supplies are shown in Figure 4-13 and Figure 4-14 respectively. The resistors R14 and R15 are added to limit the input current of the optocouplers to 10mA for a control voltage of 15V. VG1 and VS1 connect the upper transistor to the driver and VG2 and VS2 connects the lower transistor to the driver. VS2 is also connected to ground. R9 is a shunt resistor used for sensing the load current.

The layout of the board is shown in Figure 4-16. Separate layout of the top and bottom layer can be found in appendix D3. Figure 4-15 shows a picture of the final converter. A full BOM can be found in appendix E2.

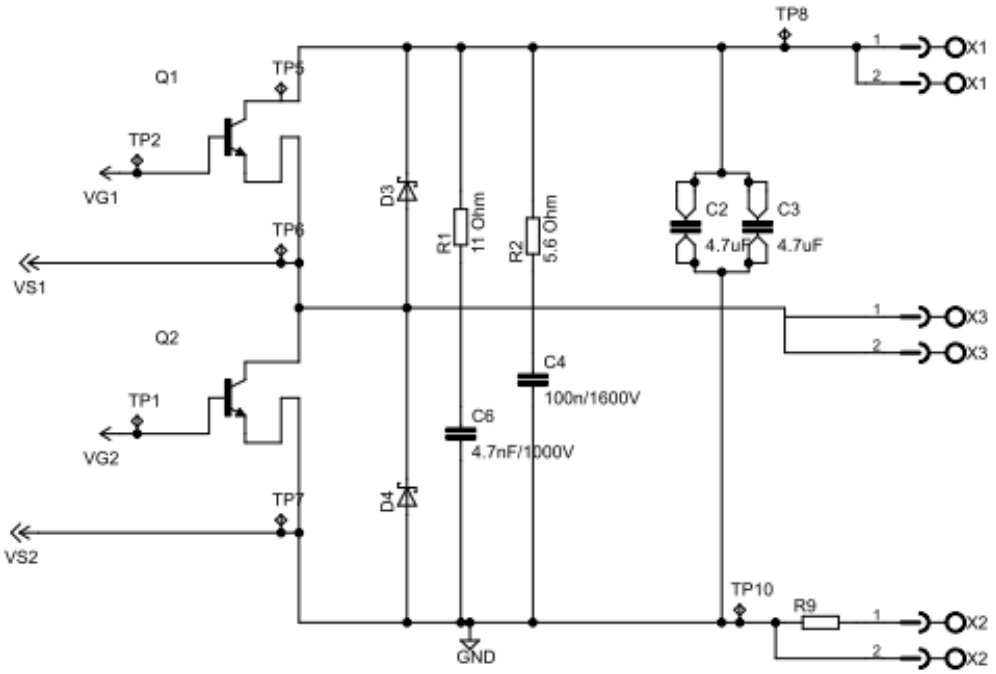

Figure 4-12 BJT half-bridge schematic

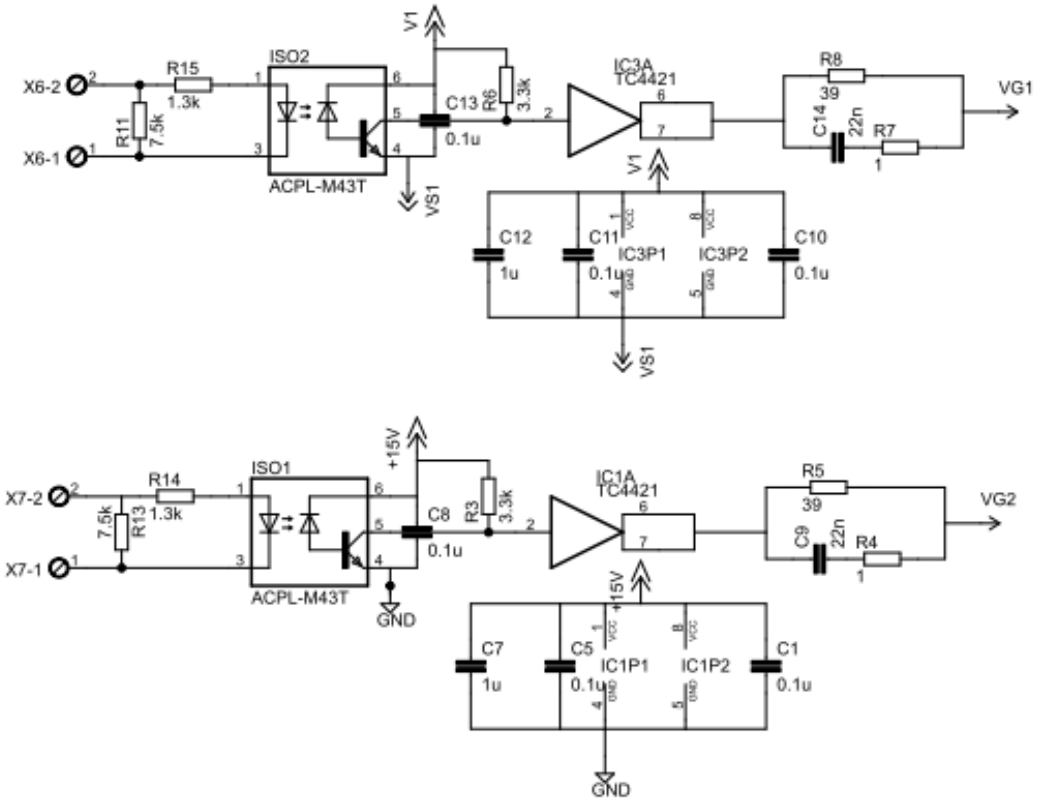

Figure 4-13 BJT drivers schematic

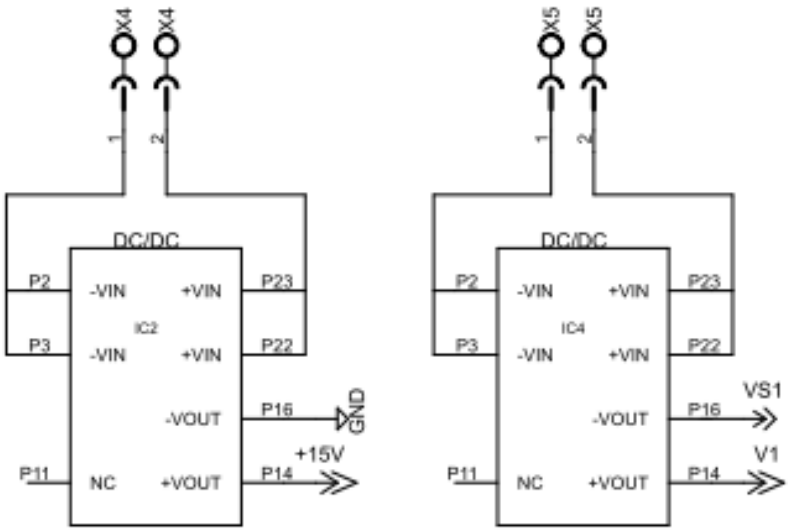

Figure 4-14 Isolated gate driver supply

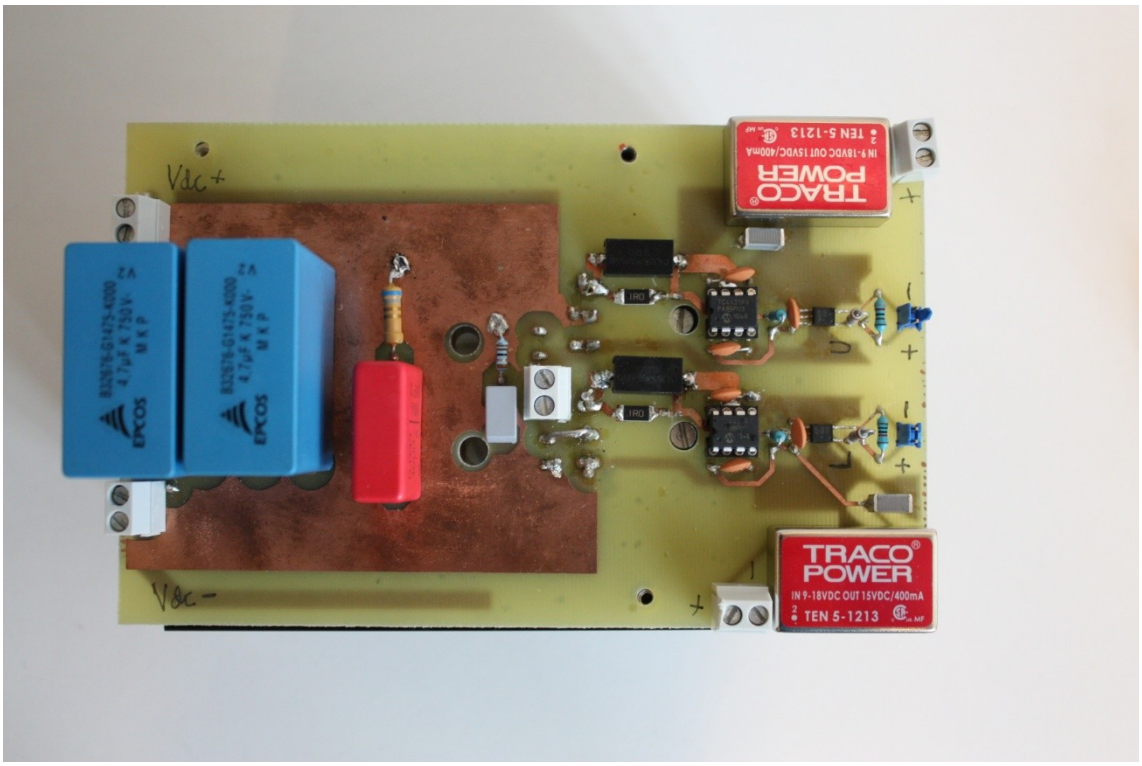

Figure 4-15 Picture of BJT half-bridge

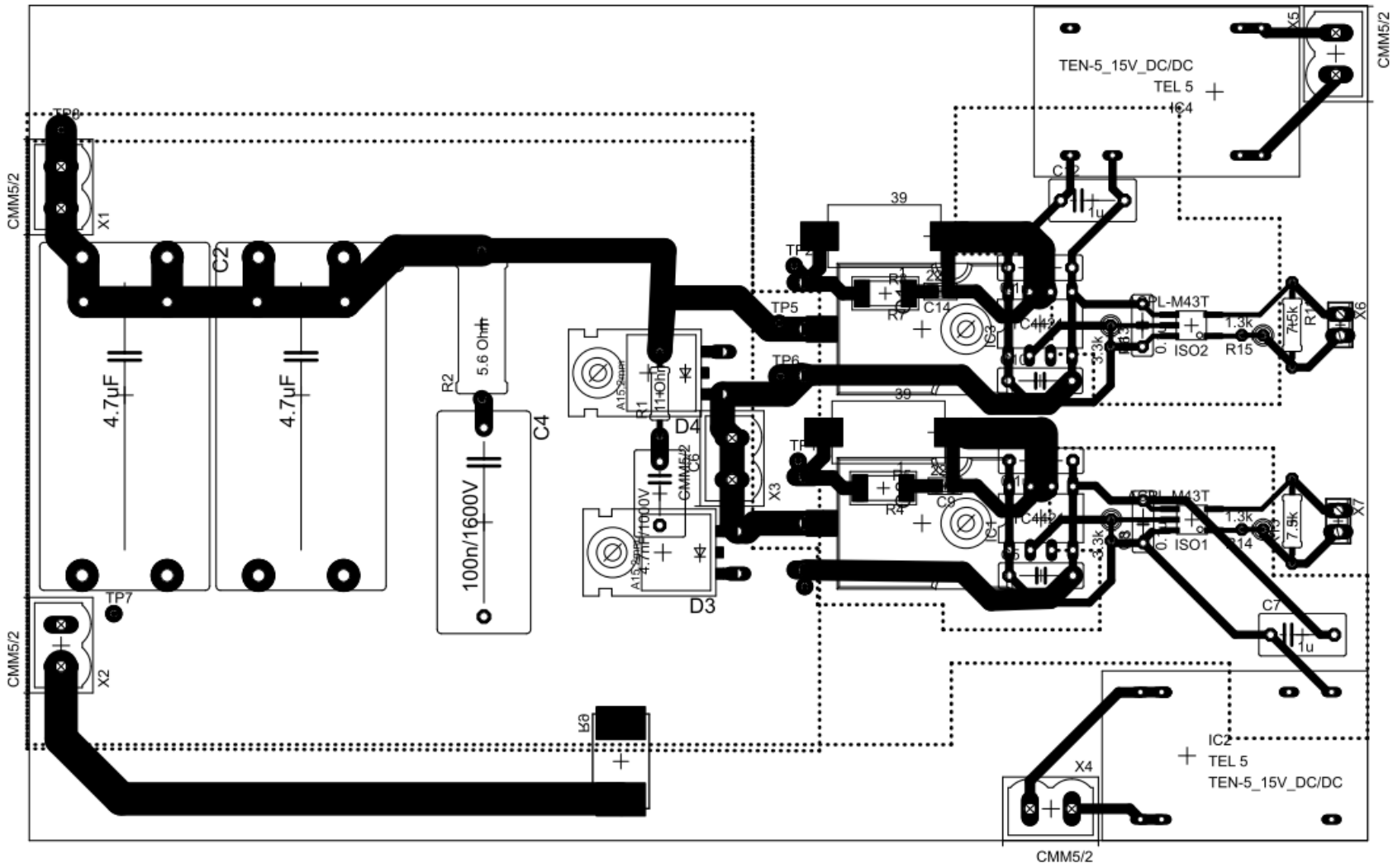

Figure 4-16 BJT half-bridge PCB layout

4.5 Types of control and modes of operation of Buck converters

When selecting a control strategy and an appropriate compensation network for the controller of the step down converter, one need to know if the converter is going to operate in Continuous Conduction Mode (CCM) or Discontinuous Conduction Mode (DCM). A controller designed for operating in continuous current mode is also stable for discontinuous operation [46]. On the other hand, if the control loop is designed for discontinuous operation, it often goes unstable in the continuous mode. The reason for this is the LC-filter at output of the converter. In continuous mode the filter introduces a resonance double pole which gives a phase lag of 180 ˚. Hence, the control loop for a continuous mode converter needs an extra phase lifting zero. A controller designed for continuous current mode is therefore more robust than one designed for discontinuous mode.

The most common way to control DC/DC converters are with Pulse Width Modulation, PWM. In PWM a constant switching frequency is used, and the output voltage is controlled by adjusting the duration of which the switch is on. Variable frequency switching is only used in special applications.

There are advantages and disadvantages with both continuous and discontinuous modes of operation. The main disadvantage with discontinuous mode is the high peak current through the transistor, diode and output filter capacitor [47]. The advantage is fast response when correcting disturbances that results from large steps in load current and input voltage. The inductor current starts at zero each period, which means that any load level can be reached in on cycle. For Buck converters operating in continuous mode the output voltage is completely independent of the load. This gives the continuous Buck excellent open loop load regulation [47]. One of the drawbacks of continuous current converters is that the required inductor size is quite large. Buck converters have best over-all performance when operating in continuous current mode. It was therefore decided to design the converter for continuous operation.

4.5.1 Filter dimensioning

The range of operation condition for the step down converter is shown in Table 4-2.

Operation condition		
Input voltage	V_{in}	250-500V
Output voltage	V_o	200V
Load current	I_o	2-10A
Switching frequency	f_s	15kHz
Load Resistor	R_o	20-100Ω
Maximum overload current/ short circuit current	I_{sc}	20A

Table 4-2 Converter ratings and operation conditions

The output voltage range gives a duty cycle which varies between 0.4 and 0.8. The maximum current ripple, ΔI_L, is two times the minimum load current, 4A. To be sure that the converter operates in continuous conduction mode the output inductor needs to be dimensioned according to:

$$L \geq \frac{V_o t_{off}}{\Delta I_L} = 200V \cdot \frac{40\mu s}{4A} = 2mH \qquad (4.3)$$

The duty cycle is set to 0.4 in the calculations. This means that the filter inductor needs to be larger than 2mH. A normal voltage requirement is that the peak-to-peak ripple voltage, ΔV_o, should be less than 1% of the output voltage, thus the ripple voltage must to be smaller than 2V.

To meet the ripple requirements, two factors needs to be considered. If one assumes that the ripple component of I_L flows through the capacitor and the average current flows through the load resistor, then the capacitor delivers some additional charge, ΔQ, when the inductor current is lower than the average load current. During this period the output voltage of the converter drops. The peak-to-peak output ripple voltage can be calculated from [9]:

$$\Delta V_o = \frac{\Delta Q}{C} = \frac{\Delta I_L T_s}{8C} \tag{4.4}$$

Where ΔI_L is given by:

$$\Delta I_L = \frac{V_o}{L}(1 - D)T_s \tag{4.5}$$

By combining (4.4) and (4.5) one can obtain an expression for the ripple voltage in percentage of the output voltage:

$$\frac{\Delta V_o}{V_o} = \frac{1}{8}\frac{T_s^2(1 - D)}{LC} \tag{4.6}$$

Hence, the ripple voltage is largest in percentage for small duty cycles. From equation (4.6), setting L=2mH and ΔV_o=2V, the minimum value of the capacitor must be 16.67μF.

The other contribution to the ripple voltage is the voltage drop across the capacitors equivalent series resistor, ESR.

$$ESR \leq \frac{\Delta V_{o,max}}{\Delta I_L} \tag{4.7}$$

Hence, the ESR of the selected capacitor needs to be smaller than 500mΩ. Table 4-3 summarizes the filter requirements.

Filter requirements		
Inductance value	L	≥2mH
Capacitance value	C	≥16.67μF
Equivalent series resistance	ESR	≤500mΩ

Table 4-3 Filter requirements

It was decided to use an electrolytic capacitor with C=470uF and an ESR of 194mΩ. An inductor with L=2.3mH was selected.

4.5.2 Voltage mode

The oldest control strategy for DC/DC converters is Direct Duty Cycle Control, DDCC. Figure 4-17 and Figure 4-18 shows the operation principle. The error between the measured output voltage and reference is amplified and compared with a repetitive sawtooth waveform. The repetitive waveform is internally generated in the controller IC. When the control signal (V_c), which is the output of the error amplifier, is larger than the triangular waveform the switch is turned on. Hence, the duty cycle is directly

proportional to the deviation between the actual output voltage and the reference, and also proportional to the control voltage.

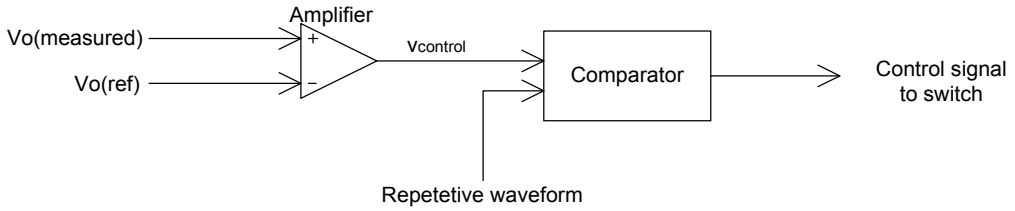

Figure 4-17 PWM control block diagram

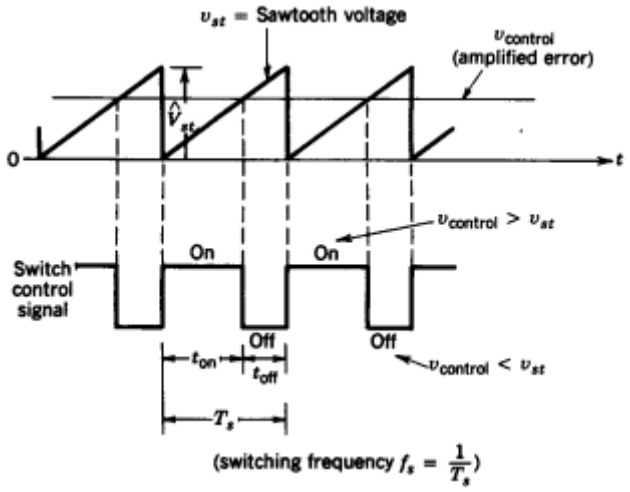

Figure 4-18 Comparator signal [9]

4.5.3 Current mode

In contrast to voltage mode control, where the repetitive sawtooth waveform is internally generated, the repetitive waveform in current mode control is obtained by sensing the converter inductor current. Hence, the inductor current is compared with the control voltage, forming an inner current control loop. The control voltage is obtained the same way as in voltage mode control. This means that the control voltage now sets the inductor current instead of controlling the duty cycle directly. The figure below shows an example of current mode control.

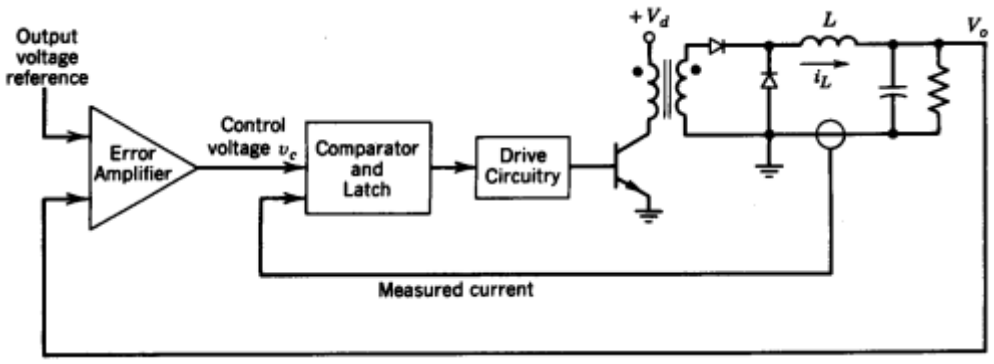

Figure 4-19 Current mode control [9]

Since the inductor is included in the inner loop, the double pole of the output filter is reduced to a single pole which is much easier to compensate for [48]. There are also some problems with current mode control. The most important problems are instability above 50% duty cycle, subharmonic oscillations, non-ideal loop response and an increased sensitivity to noise [49]. The instability above 50% duty cycle can be solved by adding slope compensation. By adding a compensating ramp with 50% of the downslope of the output inductor current, as seen from the control circuit, the converter can operate at 100% duty cycle [49]. The ramp should be added to the sensed current or to the control voltage. If the ripple component of the current is small compared to the DC component, which is the case for many continuous operating converters, empirical results show that the slope compensation should be made larger than 50% of the inductor down slope. By increasing the compensation slope the damping of system increases and the subharmonic oscillations are reduced. When the compensation slope is equal to the inductor slope, all subharmonic oscillations are removed. As the compensation slope is increased beyond 50% of the inductor current, the converter starts to act more like a voltage mode converter and less like a current mode converter.

4.6 Implementation of controller IC

A UC3843BN PWM controller from STmicroelectronics was selected to control the converter. The IC can operate with both current mode control and voltage mode control. It was decided to use current mode control..

When modeling the controller all nonlinearities, which are introduced by blanking time, rise times and fall times, are neglected. It is assumed that the inductor current is directly proportional to the control signal during current mode control. The derivations in the following sections are based on [50, 51]. DC values are given in capital letters while time varying expressions are given in small letters.

4.6.1 Brief control theory

Knowledge to some basic control theory is required to design a controller which gives a stable non-oscillating output voltage.

Bode-Nyquist stability criteria says that [52]; the system is stable if the gain of the open loop transfer function, h_0, drops below one before the phase angle of the transfer function has reached -180 °. The phase margin, ψ, is defined as 180 ° plus the phase angle of h_0 at the crossover frequency, f_c. The crossover frequency is the frequency where gain of the system crosses the 0-dB line. A properly damped system should have phase margin which is larger than 45 °.

The sampling theorem say that to be able to reproduce a continuous signal correctly all frequency components in the signal must be smaller than $f_s/2$ [52], where f_s is the sampling frequency. In a switch mode power supply the sampling frequency is equivalent to the switching frequency. The crossover frequency of the converter is often set to 25% of the switching frequency [48].

4.6.2 Modeling of converter

Ideally the average inductor current is proportional to the control signal. Hence the inductor current can be expressed as:

$$I_L = KV_c \tag{4.8}$$

Where K is the ratio between the maximum inductor current and the maximum control voltage.

$$K = \frac{\max I_L}{\max V_c} \tag{4.9}$$

V_c is limited internally to 5V by the selected controller and the maximum inductor current is given by I_{sc}. This gives K=4.

It is good approximation to say that the DC part of the inductor current flows through the load resistor and that the ripple part flows through the filter capacitor. This gives the following "DC Relationship":

$$V_o = I_L R_o = K V_c R_o \tag{4.10}$$

By rewriting (4.10) the amplitude of the control voltage can be expressed as:

$$V_c = \frac{V_o}{K R_o} \tag{4.11}$$

The "Control to Output Gain" is given by (4.12).

$$\frac{v_o}{v_c} = K R_o H_e(s) \tag{4.12}$$

$$H_e(s) = \frac{1 + s \cdot ESR \cdot C}{1 + s \cdot R_o \cdot C} \tag{4.13}$$

Where $H_e(s)$ is the combined transfer function of the load and the output filter. The control to output transfer function has one pole and one zero. The respective corner frequencies are:

$$f_{p,f} = \frac{1}{2\pi R_o C} \tag{4.14}$$

$$f_{z,f} = \frac{1}{2\pi ESR \cdot C} \tag{4.15}$$

At maximum load; $f_{p,f}$=16.9Hz and $f_{z,f}$=1745.5Hz.

The "Low Frequency Gain" is found by setting "s" equal to zero in (4.12):

$$\frac{V_o}{V_c} = K R_o \tag{4.16}$$

The equation shows that the low frequency gain decreases with increased loading of the converter. The low frequency gain varies from 80 (38dB) to 400 (52dB) for the given load conditions.

4.6.3 Design of compensation network

The crossover frequency was set to ¼ of the switching frequency. The resulting crossover frequency is 3.75kHz. This criterion is used when calculating the required gain of the compensating network. At the crossover frequency $\omega \cdot R_o \cdot C >> 1$. Hence, the uncompensated system gain at f_c is approximately expressed by:

$$Gain_{openloop@f_c} = K \frac{\sqrt{1 + (2\pi f_c \cdot ESR \cdot C)^2}}{2\pi f_c \cdot C} \tag{4.17}$$

The open loop gain at the crossover frequency is 0.866 (-1.35dB)

This means that the gain required from the Error Amplifier (E/A) compensation network at the cross over frequency is 1.35dB.

To stabilize the converter the compensation network shown in Figure 4-20 was used.

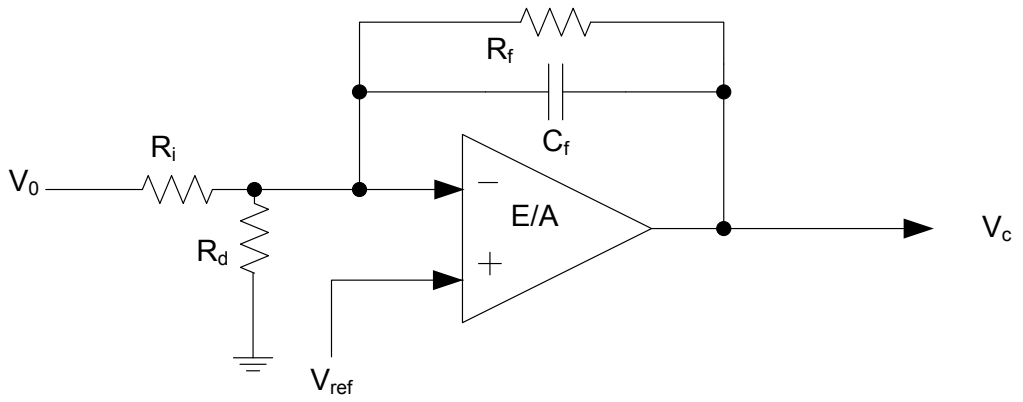

Figure 4-20 Compensation network

It can be shown that the transfer function of the compensation network can be written as:

$$\frac{v_c}{v_{o,scaled}} = \frac{R_f}{R_i}\frac{1}{1 + R_f C_f s} \tag{4.18}$$

Where $v_{o,sacled}$ is given by:

$$v_{o,scaled} = \frac{v_o R_d}{R_d + R_i} \tag{4.19}$$

The gain is independent on R_d. R_d is therefore is used to set the reference value of the output voltage. The selected controller IC has an internal reference voltage of 2.5V. This means that R_d has to be selected such that the desired output voltage is scaled down to 2.5V.

$$R_d = \frac{2.5}{V_o - 2.5} R_i \tag{4.20}$$

The ESR zero, $f_{z,f}$, is cancelled by the compensation network pole, $f_{p,c}$, at $f_z/8$=218.1Hz. The offset between the poles increases the low frequency gain but reduces the phase margin. The required E/A gain at frequencies bellow $f_{p,c}$ is:

$$Gain\ bellow\ f_{p,c} = -Gain_{openloop@f_c} + 20\log f_c - 20\log f_{p,c} \tag{4.21}$$

Where $f_{c,p}=1/(2\pi R_f C_f)$. This gives a required gain at low frequencies of 26dB (20).

From equation (4.18) one can see that the E/A gain at low frequencies is equal to R_f/R_i. R_f must be kept over a certain value to avoid overloading the operational amplifier. It was therefore decided to set R_f = 1.58MΩ. This gives C_f=461.9pF and R_i equal to 79kΩ. If the desired output voltage changes, R_d has to be varied according to equation (4.20) to set the new reference. With an output voltage of 200V R_d must be equal to 1kΩ.

The open lop transfer function of the system is given in equation (4.23).

$$h_o = KR_o \frac{R_f}{R_i} \cdot \frac{1 + s \cdot ESR \cdot C}{1 + s \cdot R_o \cdot C} \frac{1}{1 + R_f C_f s} \tag{4.22}$$

Figure 4-21 shows the Bode diagram of h_o. The phase margin is 68.5 ˚, and it should be more than sufficient to provide stable operation.

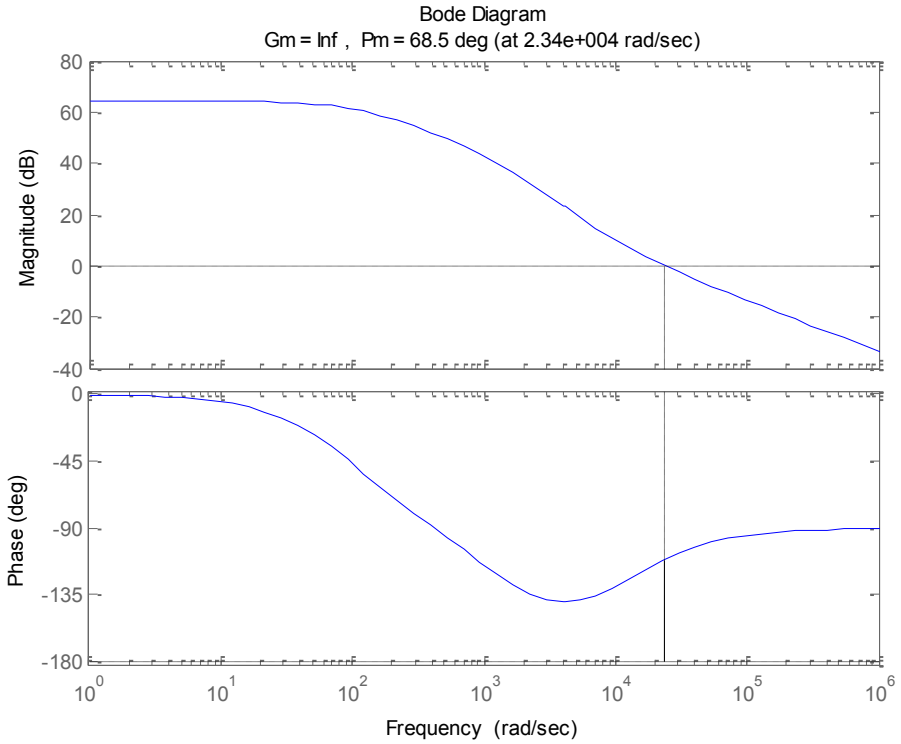

Figure 4-21 Bode diagram of open-loop transfer fuction

The IC PWM controller has integrated over current protection. When the voltage at the current sensing pin exceeds 1V, the switching pulse is terminated independently of the control voltage. Thus, the current sensing resistor, R_s, needs to be dimensioned such that the voltage over it reaches 1V at the maximum allowed current. This gives R_s=0.05Ω. Switching noise and stray capacitance in the inductor can introduce current spikes which lead to premature pulse termination. A low pass RC filter needs to be added to the current measurement to filter out these transients [53].

The corner frequency of the low pass filter must be higher than the switching frequency to avoid damping the measured inductor current ramp. It was decided to use a corner frequency which is at least one order of magnitude larger than the switching frequency. By using R_{fs}=5kΩ and C_{fs}=200pF the corner frequency becomes 159.1kHz. Figure 4-22 shows the connections of the components.

As stated above, to operate the converter stably at duty cycles in excess of 50% slope compensation needs to be added. The compensating slope should be adjusted according to the down slope of the inductor current. The down slope of the inductor current is proportional to the output voltage of the converter.

$$\frac{\Delta i_L}{\Delta t} = \frac{V_o}{L} \tag{4.23}$$

With an output voltage of 200V and an inductance of 2.3mH the current down slope becomes 86.957kA/s, which is equal to 5.80A/66.67µs. This means that the maximum peak-to-peak input at the current sense pin is equal to $5.80 \cdot R_s$. It was decided to set the compensation slope equal to 1.1 times the inductor slope to be sure that the subharmonic oscillations are damped out fast. The amplitude of the compensation slope then becomes $5.80 \cdot 0.05 \cdot 1.1 = 0.32V$.

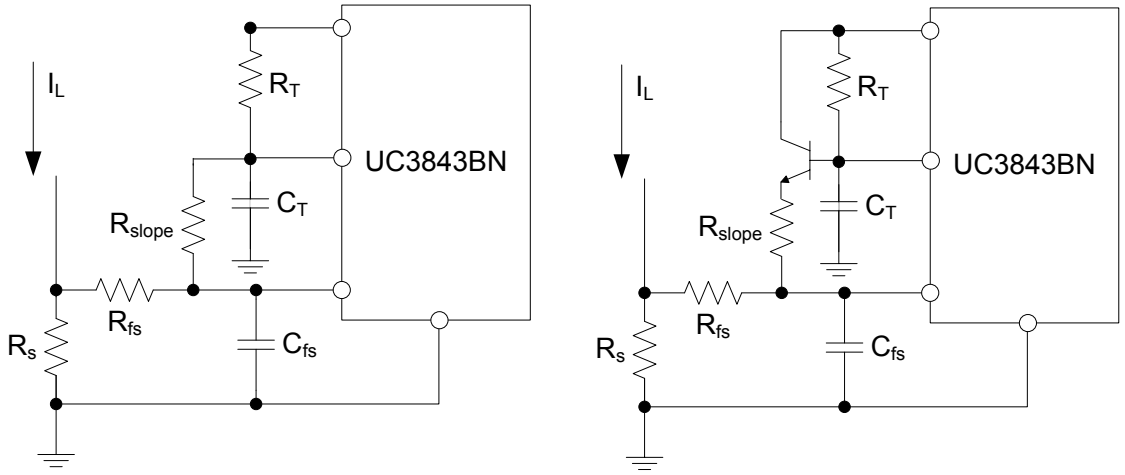

Figure 4-22 Connection of current sensing and slop compensation

The figure above shows two possible connections of the slope compensation. By using a transistor, as shown in the figure to the right, the loading of the oscillator becomes lower. It was decided to use the solution to the right and an NPN 2n2222 transistor was selected. The peak to peak output voltage at the emitter of NPN transistor is equal to 1.5V. Hence, the ratio between R_{slope} and R_{fs} must be equal to 3.69. This gives $R_{slope}=18.44k\Omega$.

It is not possible to find components with the exact same values as calculated. When selecting components the one which is closest is selected. This will give some deviations from the calculated performance, but the error should be minimal.

4.6.4 Generation of dead time and complementary outputs

The circuit shown in Figure 2-7 was used to generate the dead time and to create complementary outputs. The data sheets of all components were closely studied and the information regarding propagation delays were put into equation (2.5). The measured switching times were also put into the equation. The required dead time was calculated to be 518ns. From equation (2.7) the time constant was calculated to be 3.266µs. A resistor of 12kΩ and a capacitor of 270pF were selected.

4.6.5 Control board schematic and layout

The schematic of the control board is shown in Figure 4-23 and the PCB layout of the board is presented in Figure 4-24. A picture of the control board is shown in Figure 4-25. The full BOM can be found in appendix E3.

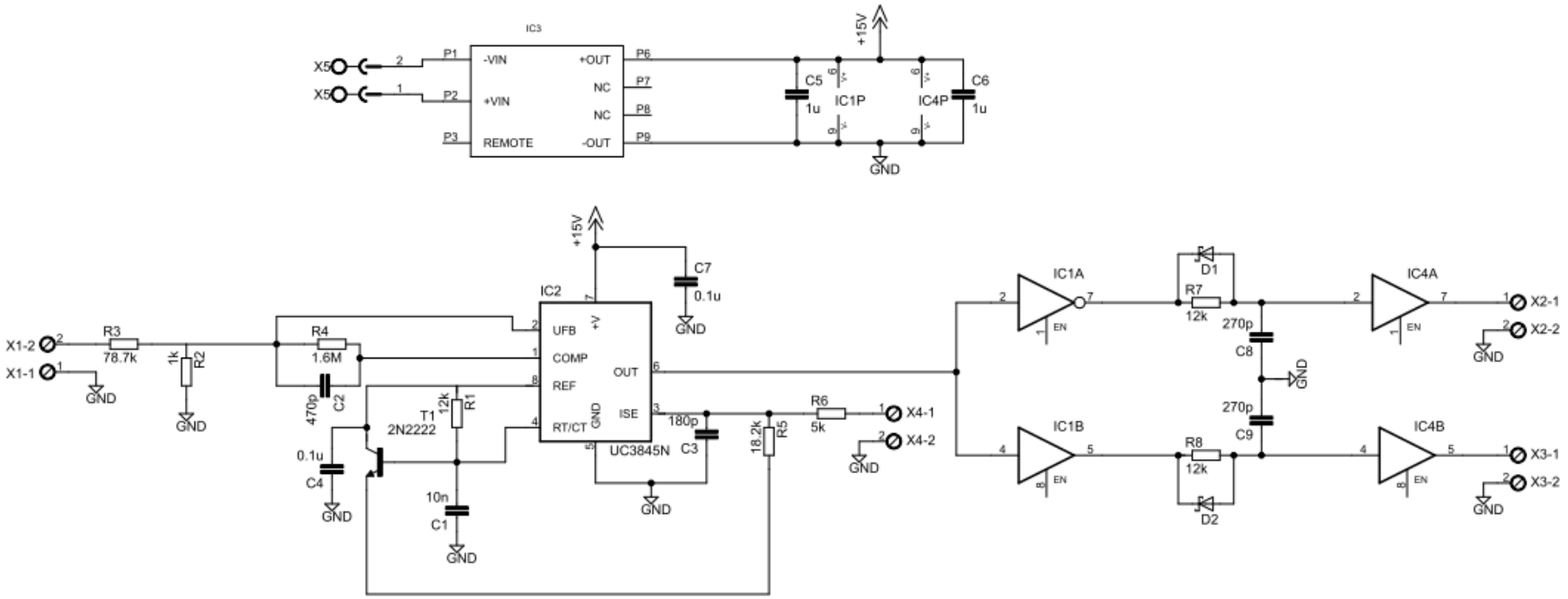

Figure 4-23 Schematic of PWM controller and dead time generation

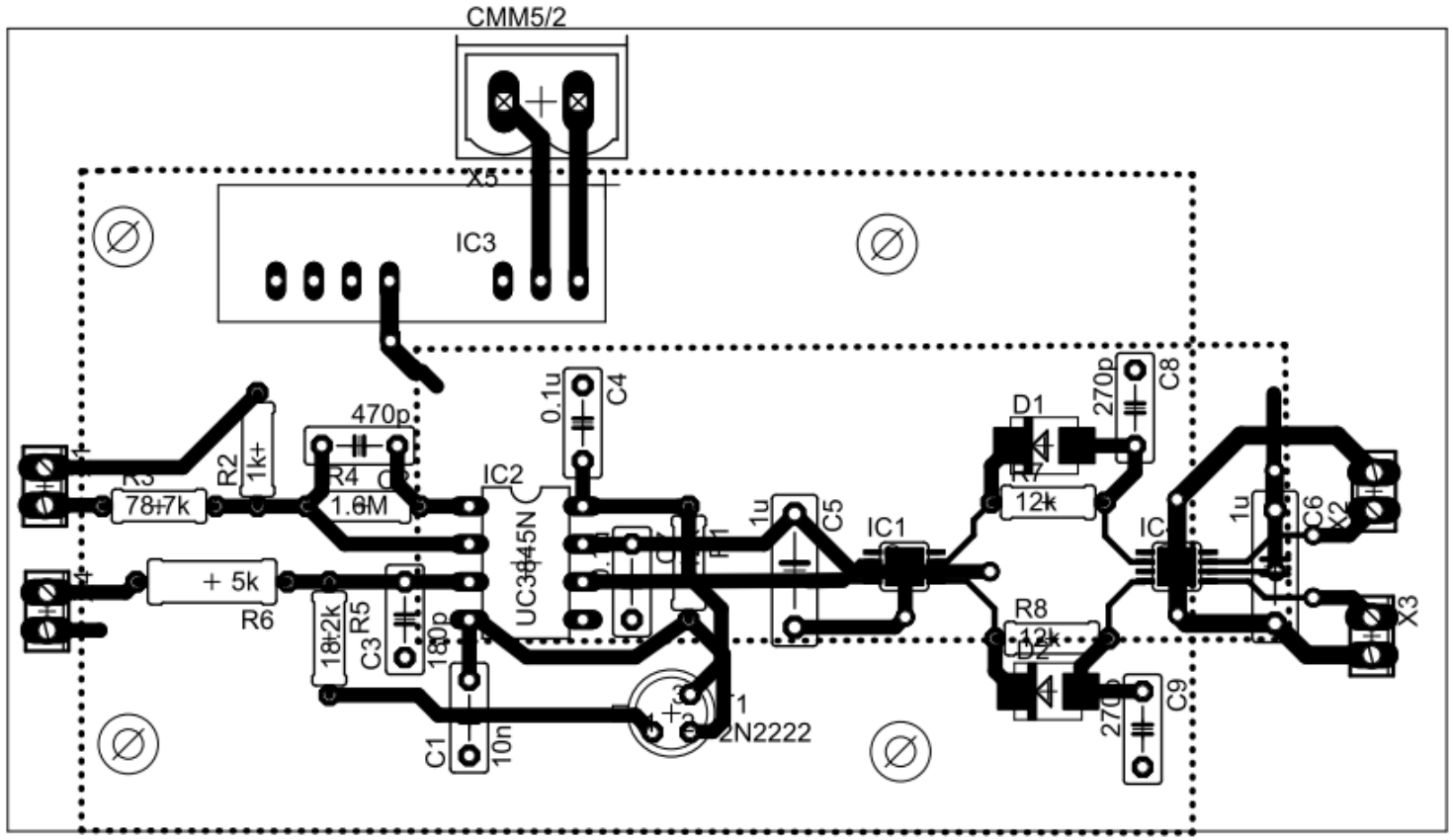

Figure 4-24 Board layout of PWM controller and dead time generation

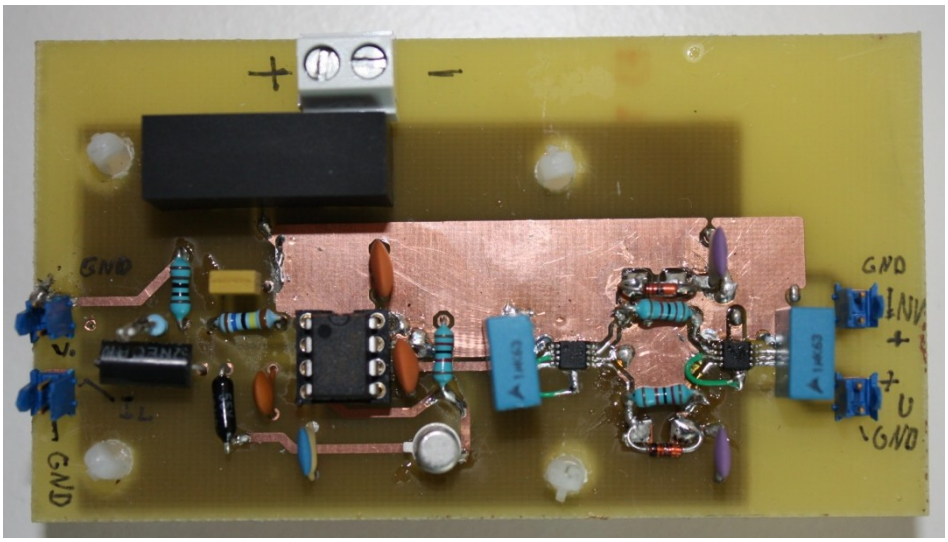

Figure 4-25 Picture of control board

5 Laboratory Setup and Measurement Description

This section describes the laboratory setup and the measuring equipment which has been used. A description of the experimental standard and principles are also given. At the end some initial measurements are presented.

5.1 Experimental standards and test principles

To characterize the dynamic performance of the SiC transistors it is necessary to define certain parameters and test principles. The switching behavior of JFETs and MOSFETs are somehow similar. The IEC 60747-8 standard [54] for MOSFETs is therefore used to define the switching times and the switching energies for the JFETs. IEC 60747-7 is the standard for BJTs [55].

5.1.1 Switching times and energies

The difference between the switching times definition for JFETs and BJTs is that the BJT has the base current, I_b, as the input signal while the JFET has the gate voltage. The explanation below is given for JFETs, but is also valid for BJTs if the term gate voltage is replaced with base current.

The turn-on time t_{on} is the sum of turn on delay $t_{d(on)}$ and the current rise time t_r. Where $t_{d(on)}$ is defined as time from the gate voltage reaches 10 % of its maximum value to the drain current has risen to 10 % of its final value. The time duration when the current, through the transistor, increases from 10 % to 90 % of its on-value is defined as the current rise time. Hence the turn-on time is the time from the gate voltage reaches 10 % of its final value to the time where the current reaches 90 % if is on value.

The turn-off time is the sum of the turn-off delay $t_{d(off)}$ and the current fall time t_f. $t_{d(off)}$ is defined as the time from gate voltage is reduced to 90 % of its value to the point where the current has dropped to 90 % of its initial value. The current fall time is defined as the time it takes for the current to drop from 90 % to 10 %. Figure 5-1 shows an illustration of the switching times. The figure in the standard in standard shows the waveforms for resistive switching. This is unrealistic since almost all loads are inductive, hence the figure can be misleading.

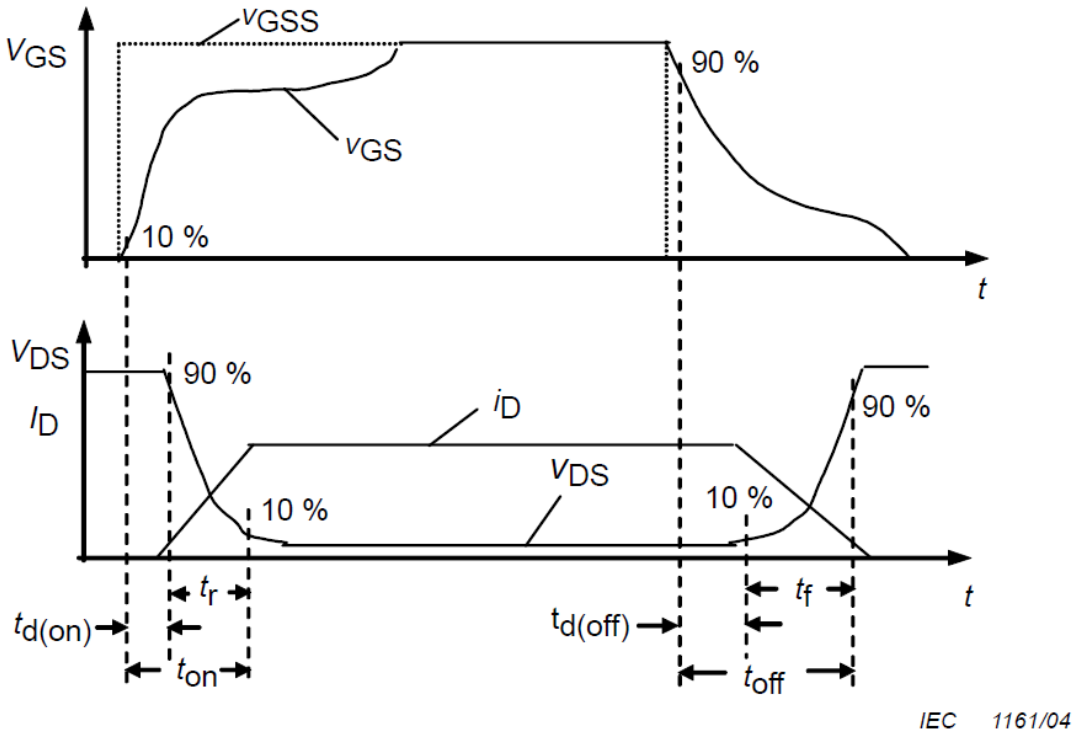

Figure 5-1 Waveforms for turn on and turn off of a transistor [54]

Since the standard is developed for a MOSFET using a one-stage driver output, it is not 100 % appropriate to use when testing the JFET with a two-stage driver. The start of the $t_{d(on)}$ interval is defined as the time V_{GS} reaches 10 % of the first stage voltage i.e. when the gate voltage has reached 0.5 V. While the start of the $t_{d(off)}$ interval is defined as the time V_{GS} decreased to 90 % of the second stage voltage i.e. 2.7 V.

It is very difficult to accurately measure the transient base current of the BJTs during switching. The induced noise in the measuring equipment could be of the same magnitude as measured base current. Hence, to measure the delay times becomes very difficult. The start of the turn-on/turn-off is therefore defined, in this work, as the point where the base voltage/current starts to change.

The instantaneous power dissipation is given by:

$$p(t) = u(t)i(t) \tag{5.1}$$

Where u(t) is the voltage over the transistor and i(t) is the current flowing through the device. The dissipated energy is the integral of the power over time. The turn-on energy E_{on} and turn-off energy E_{off} are the energies dissipated in the transistors during turn-on and turn-off respectively. Figure 5-2 shows the time periods for the energy calculations. The on-period is defined from the point where the current reaches 10 % of its stationary value to the point where voltage is reduced to 10 % of its starting value. The off-period is defined opposite. By using the definitions from the figure, the switching energies can be calculated as:

$$E_{on} = \int_0^{t_1} u(t)i(t)dt \tag{5.2}$$

$$E_{off} = \int_{t_2}^{t_3} u(t)i(t)dt \tag{5.3}$$

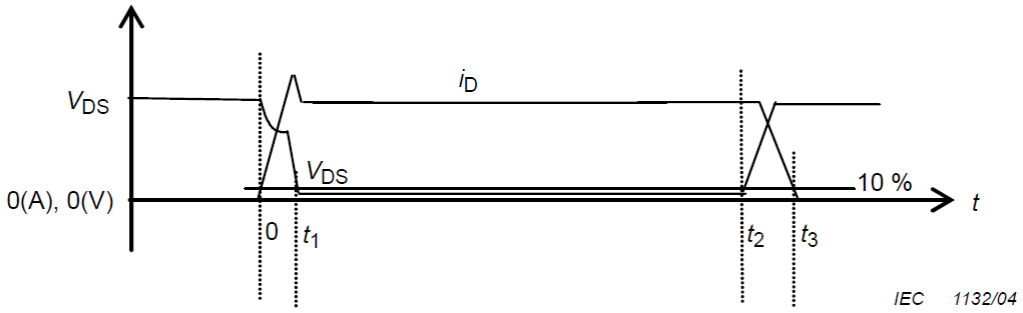

Figure 5-2 Definition of switching losses [54]

If there are any tail currents at turn-off this should be added to the switching energies. The power dissipated due tail currents can be significant even for low current values since the voltage is at its blocking value.

The integration to obtain the switching energies is performed numerical in Matlab. Appendix A2 shows the Matlab code used to perform the integration. After the energies are calculated the switching losses can be found by multiplying the sum of E_{on} and E_{off} with the switching frequency f_s.

$$P_s = f_s(E_{on} + E_{off}) \tag{5.4}$$

5.1.2 Test principles

To measure the switching times and switching energies the well known double pulse test (DPT) was used. The test circuit is shown in Figure 5-3. The lower transistor Q2 is the Device Under Test (DUT) and the upper transistor is kept off. The test is performed by applying two pulses on the lower gate driver. During the first pulse the current rises in the inductor. When Q2 turns off the current commutates to the upper diode. The second pulse is then applied before the current in the inductor has had a noticeable decrease. This makes it possible to investigate turn on and turn off at a desired load current by adjusting the duration of the first pulse. Figure 5-4 shows the principle waveforms.

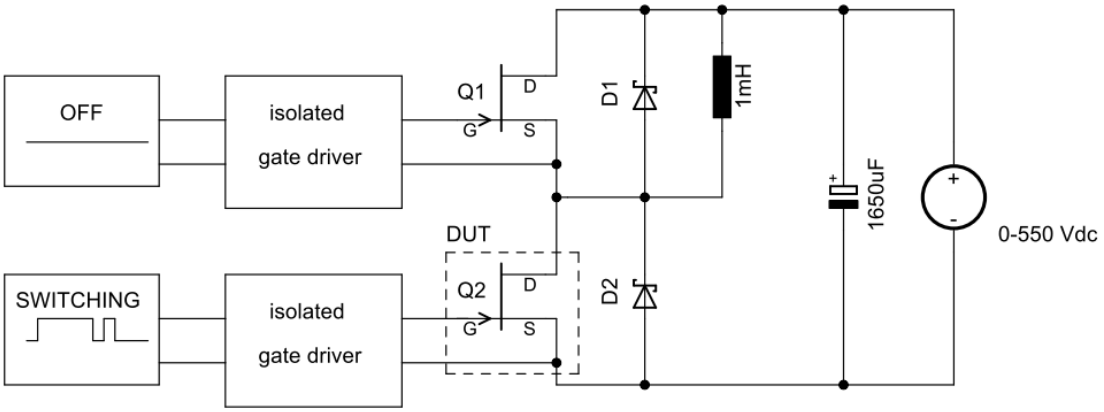

Figure 5-3 Double pulse setup

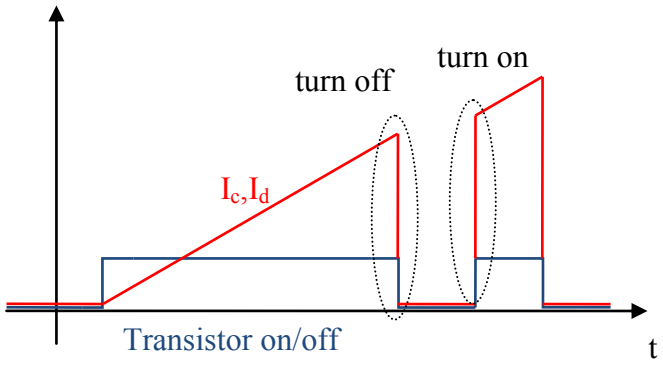

Figure 5-4 Double pulse test principle

The on-state voltage of a transistor is found by measuring the voltage over the device terminals when it is conducting a known current at known junction temperature. By repeating the measurements, for several currents and several temperatures, the static characteristics of the transistors are obtained. NTNU has no available equipment for measuring the on-state voltage of the devices, thus a homemade measuring setup was made. The inductor in Figure 5-3 was changed with a power resistor. The value of the resistor was selected quite high such that variations in the transistor on-state voltage not would affect the current. By adjusting the DC-link voltage the current through the power resistor can be set to the desired value. No automatic measuring equipment were used, thus all readings had to be performed manually. The problem with manual readings is that it takes some seconds from the transistor turns on until the measured values are logged. The transistor will therefore have some self-heating and the junction temperature will be higher than measured heat sink temperature. How much the device would heat is depending on the thermal capacitance (C_T) of the device and the thermal resistance from junction to heat sink ($R_{\theta js}$). The thermal time constant, T_{th}, can be estimated by the product of C_T and $R_{\theta js}$. If the duration of the applied current is substantial longer than the device time constant, then the junction temperature can be described by the steady state equation given bellow [9]:

$$T_j = P\left(R_{\theta jc} + R_{\theta cs}\right) + T_s \tag{5.5}$$

Where $R_{\theta jc}$ is the thermal resistance between the junction and the case, $R_{\theta cs}$ is the thermal resistance between the case and the heat sink and is equal to the resistance of the thermal pads which are used in between, T_s is the heat sink temperature. The selected heat sinks were over dimensioned and their time constants are in the range of a couple of minutes. Hence, the heat sink temperature is approximately constant if the duration of the current conduction is limited to some few tens of seconds. Neither Semisouth nor TranSiC gives data regarding the thermal impedance or the heat capacity of the devices. To get an approximation it was decided to use the thermal characteristics given data sheet of the SiC MOSFET from Cree which also has a TO-247 package. The thermal impedance from junction to case reaches a stationary value after 0.5s. To be sure that the steady state equation can be used, the duration of the applied current pulse should be at least 10 times larger than the time constant.

Based on the above discussion; the duration of the current pulse was set to 10s and the measured on-state voltage and conducted current were read at the end of this period. The heat sink temperature was measured with a data logger using a T-thermocoupler and the junction temperature was then estimated by equation (5.5). The thermal resistance form junction to heat sink, including the resistance of the thermal pads, is 1.16 ˚C/W for the JFETs and 1.66 ˚C/W for the BJTs. There are some uncertainties related to the calculated junction temperature, especially when dissipated power in the transistor is high.

To test the performance of the SBC both stationary and dynamic behavior should be investigated. The parameters which influence the operation are the load resistance and the input voltage. The converter should therefore be tested with different loads and with different input voltages. A step load is added under stationary operation to test the dynamics of the converter.

5.2 Measuring equipment

5.2.1 Oscilloscope

All the waveforms for the DPT are captured by an oscilloscope from Tecktronix, MSO3014. The oscilloscope has a bandwidth of 100MHz. During some of tests the voltage was higher than the ratings of the standard probes. A high voltage probe, P5100, from Tecktronix was therefore used. The maximum voltage of the P5100 is 2500V and the bandwidth is 250MHz. After some tests it was discovered that the P5100 has a 6.5ns time delay compared to the standard probes. Hence, in some of the oscilloscope figures the drain/collector voltage should be shifted 6.5ns. The time delay was compensated when switching energies and switching times were calculated. The scope pictures which are affected by the time shift will be marked with: "*Voltage shifted 6.5ns*". The currents were measured with Rogowski coils; section 5.2.5 gives a closer description of the current measuring. A pulse generator was used to generate the controls signal to the gate drivers.

5.2.2 On-state characteristics

A Fluke 89 IV True RMS multimeter was used to measure the on-state voltage of the transistors. The transistor current was measured with a Metrix PX120 Power Meter and the gate voltage of the JFETs was measured with a Fluke 117 True RMS multimeter. All the equipment was calibrated with a Fluke 5500A calibrator. The accuracy is shown in the table below.

Measuring equipment accuracy	
Fluke 89 True RMS Mulitmeter	0.1mV for the range 0-3V 1mV 1mV for the range 3V-
Fluke 117 True RMS Multimeter	1mV for the range 0-6V
Metrix PX120	1mA for the range 0-2A 10mA for the range 2-10A

Table 5-1 Measuring equipment accuracy

5.2.3 SBC operation

The oscilloscope was used to capture the switching waveforms of the synchronous Buck converter and a Metrix PX120 Power Meter was used to measure the load current and the output power. The input current to the converter is 15kHz DC with large distortion due to current oscillations between the bulk capacitor and the PCB decoupling capacitor. It is therefore very challenging to measure the average DC current and the input power to the converter. The input power was measured with two different power meters, Metrix PX120 and Yokogawa 2533E DC/AC, but both gave very unreliable readings. As a last attempt, the input power to the bulk capacitor was measured by connecting a power meter between the rectifier and DC-link. Also these measurements were very unreliable. The efficiency of converter could therefore not be calculated.

5.2.4 Complete list of lab equipment

The table below shows a list of all the laboratory equipment that has been used during this work. The column to the left explains the application of the equipment, the mid column gives the name of the equipment and the right most column shows manufacturer and product number.

Instrument archive		
Application/measurement	Equipment	Product number
Gate voltage	Multimeter	Fluke 117 True RMS
Gate current (shunt)	Multimeter	Fluke 112 True RMS
Signal generation	Pulse generator	Wavetek model 187
Driver supply	DC supply	GSC M.1301
DPT waveforms	Oscilloscope	Tektronix MSO3014
Data storage	Lab PC	DELL latitude D505
Heating	Kook plate	Sasco 500W
Load current and power	Power meter	Metrix PX120 Power Meter
Heatsink temperature	Data logger	HP 34970A
Voltage regulation	Variac	Lübecke Variac 3R54-220-H
Galvanic isolation	Isolation transformer	Delta-Y
Drain/collector current	Rogowski coil	Athena Energy 840HiBW
Base current	Rogowski coil	PEM CWT 3R
SBC input/output current	LEM current sensor	LEM LA55-P
LEM supply	DC supply	Mascot Type 719
SBC input power	Digital power meter	Yokogawa 2533E DC/AC
Rectifier	Bridge rectifier	Vishay 36MT160 35A 1600V
Drain/collector voltage	High voltage probe	Tektronix P5100

Table 5-2 Instrument archive

5.2.5 Current measuring

There are many challenges when measuring fast current transients and it is very expensive to buy equipment with both high bandwidth and high current ratings. As the switching times decreases the influence of measuring delays becomes more decisive. It is therefore important to know the equipment that is being used.

5.2.5.1 *Rogowski coils*

The drain/collector current was measured with a Rogowski coil from Athena Energy Corp, 840HiBW, and the base current of the BJT was measured by a Rogowski form Electronic Measurements (PEM) Ltd, CWT3. A Rogowski coil consists of a helical coil of wire, which is wrapped around the current carrying conductor. The current in the conductor induces a voltage in the Rogowski coil according to equation (2.1).

This means that the coil needs to be connected to an integrator circuit in order to provide an output which is proportional to the current. Integrator circuits can be either active by using op-amps or it be made by a passive circuit. Passive integrators has droop for low frequencies. The Rogowski coil used in this work has an active integrator circuit. The coil has no iron core, thus it cannot saturate and is therefore linear even for high currents. A drawback by using a Rogowski with an active integrator is that a step response becomes oscillatory if the rise-time is sufficiently fast [56]. Since the tested SiC transistors have very short current rise times the measurements can be exposed to oscillatory noise which is not real. The band width of the CTW3 and the 840HiBW are actually too low to give very accurate results. Surfaces with high dV/dt close to the measuring coil can induce noise in the measurements [57]. Since the coil is connected between the legs of the transistor some noise should be expected.

5.2.5.2 *Current measuring delay*

Basically all current measuring techniques have a certain time delay. The length of the delay varies for different topologies and also increases with the cable length of the measuring coil. When calculating the switching losses it is very important to shift the current measurement such that voltage and current are in phase. Hence, the time delay has to be measured. The test setup used to find this delay is shown in Figure 5-5. The capacitor is made of metalized polypropylene and the resistor is of carbon film to obtain a low inductance. First the capacitor is charged by the DC source. When switch operates the capacitor is shorted over resistor. By measuring the voltage and the current the relative time shift can be found.

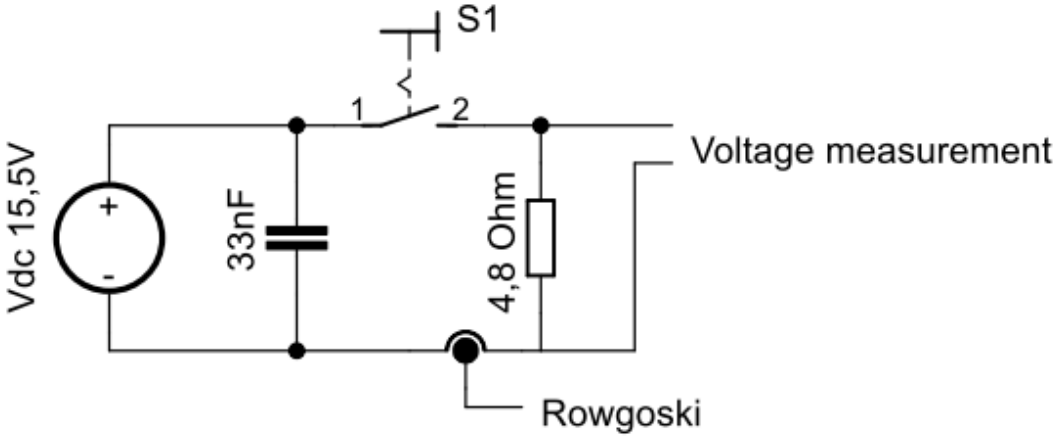

Figure 5-5 Measurement of current time delay

Current and voltage waveforms where captured with the oscilloscope. One of the resulting waveforms is given in the figure below.

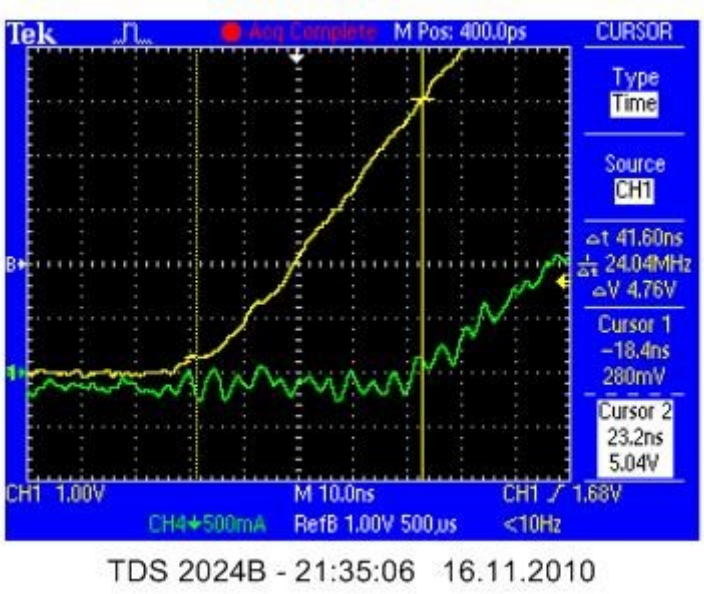

Figure 5-6 Measurement of time delay for CWT

The measurement was repeated many times and the relative time delay was found to be approximately 43 ns for the CWT and 50ns for the 840HiBW. Half way through the DPT measurements something strange happened, the time delay of the 840HiBW suddenly changed from 50ns to 40ns. Hence, the current should be shifted 10ns in some of the oscilloscope pictures. The scope pictures which are affected by the time shift will be marked with: "*Current shifted 10ns*". It is corrected for the phase when calculating switching losses in chapter 7.

5.2.5.3 ***Shunt measurements***

The uncertainty of the Rogowskies introduced a need for new current measuring equipment. A shunt resistor was designed to try to meet these requirements. The shunt was made of resistance wire and had a resistance 0.143Ω. The wire was of the type Kanthal D and has very constant resistance for a wide temperature range. A coaxial cable was used to connect the shunt to the oscilloscope. Figure 5-7 shows the connection of the shunt on the PCB and Figure 5-8 and Figure 5-9 show the measured current. The yellow curve is the shunt current, the purple is the PEM Rogowski and green is the 840HiBW Rogowski. Unfortunately, the induced switching noise is so high that measurements cannot be used. Anyhow, the shunts waveforms show that time delays of the Rogowskies are correctly adjusted. The shunt was removed before the rest of the measurements were performed.

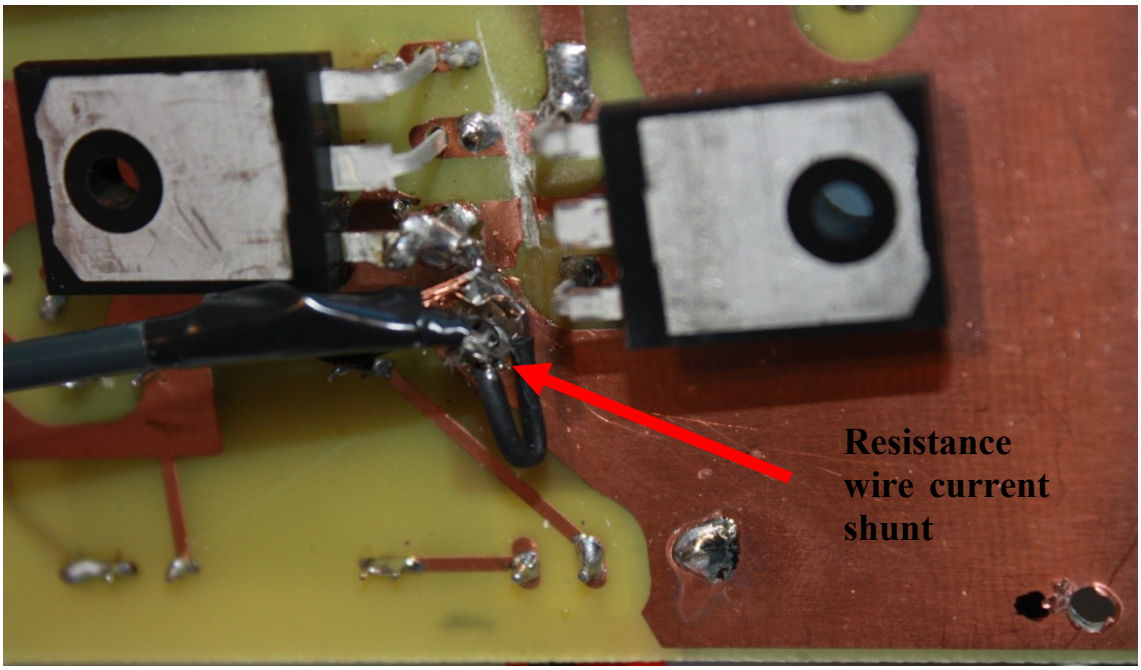

Figure 5-7 Picture of current shunt

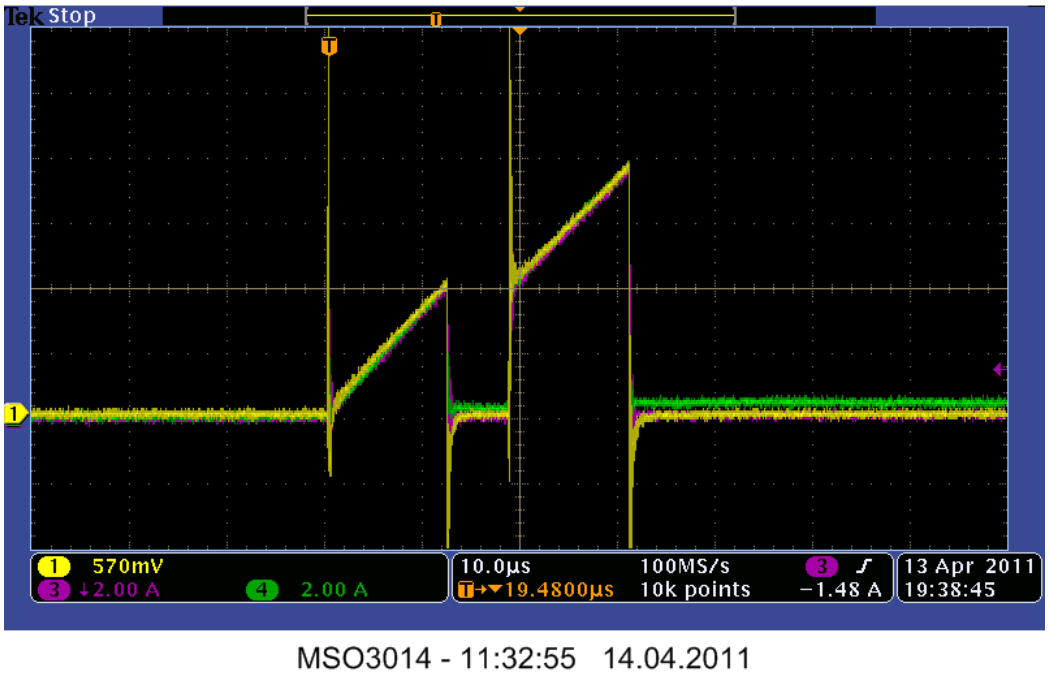

Figure 5-8 DPT current waveforms measured by current shunt

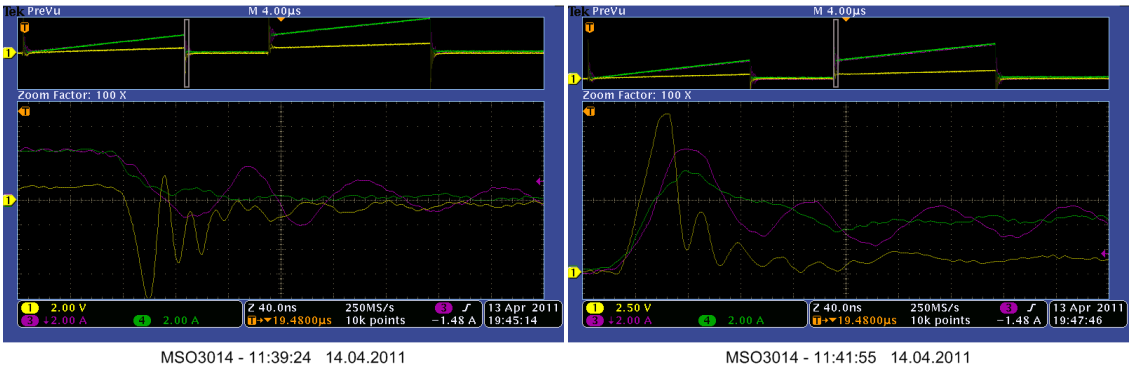

Figure 5-9 Comparison between Rogowski coils and current shunt, turn-off to the left and turn-on to the right

5.3 Laboratory setup

An overview of the lab setup is shown in Figure 5-10. The regulating transformer is connected to the grid. There is an isolating transformer connected between the variac and the rectifier. The gate drivers are supplied by a separate DC source and all measurements are performed with an oscilloscope. The control signals are either generated by a pulse generator or by control board designed in chapter 4.6. Figure 5-11 shows the principal connection of SBC. A picture of the laboratory setup is given in appendix I.

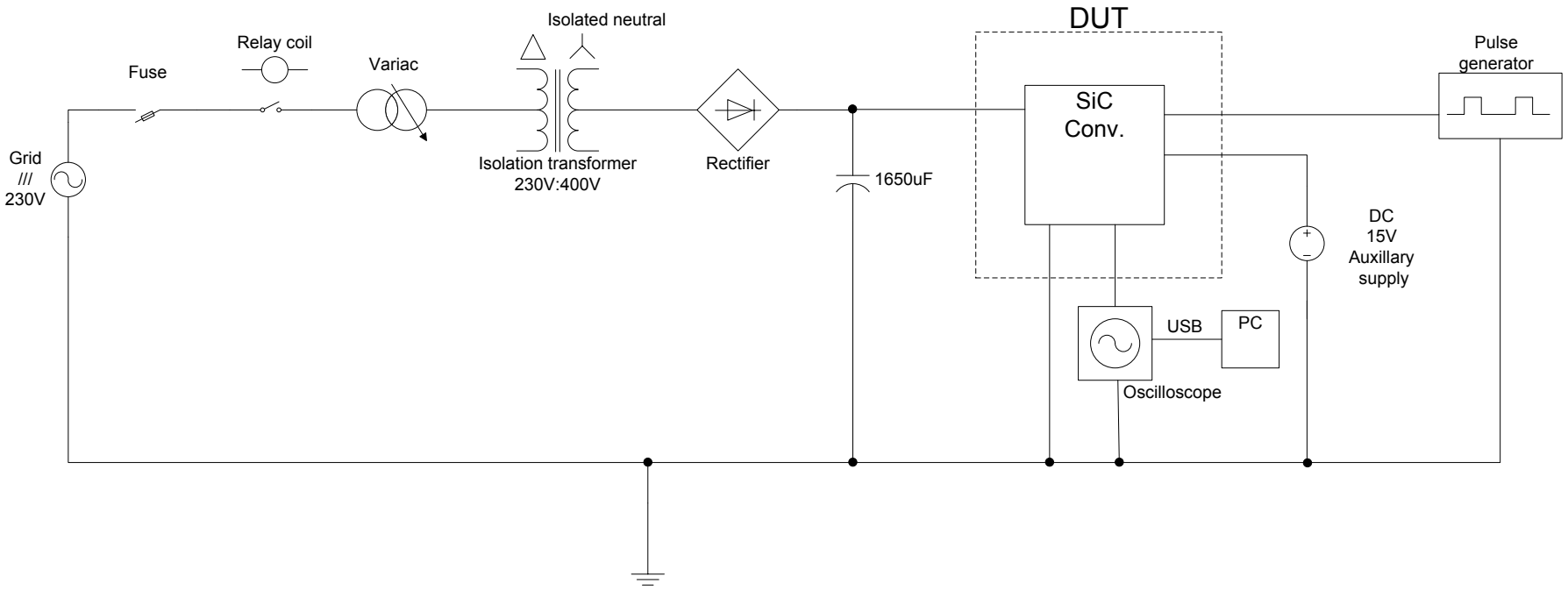

Figure 5-10 Laboratory setup

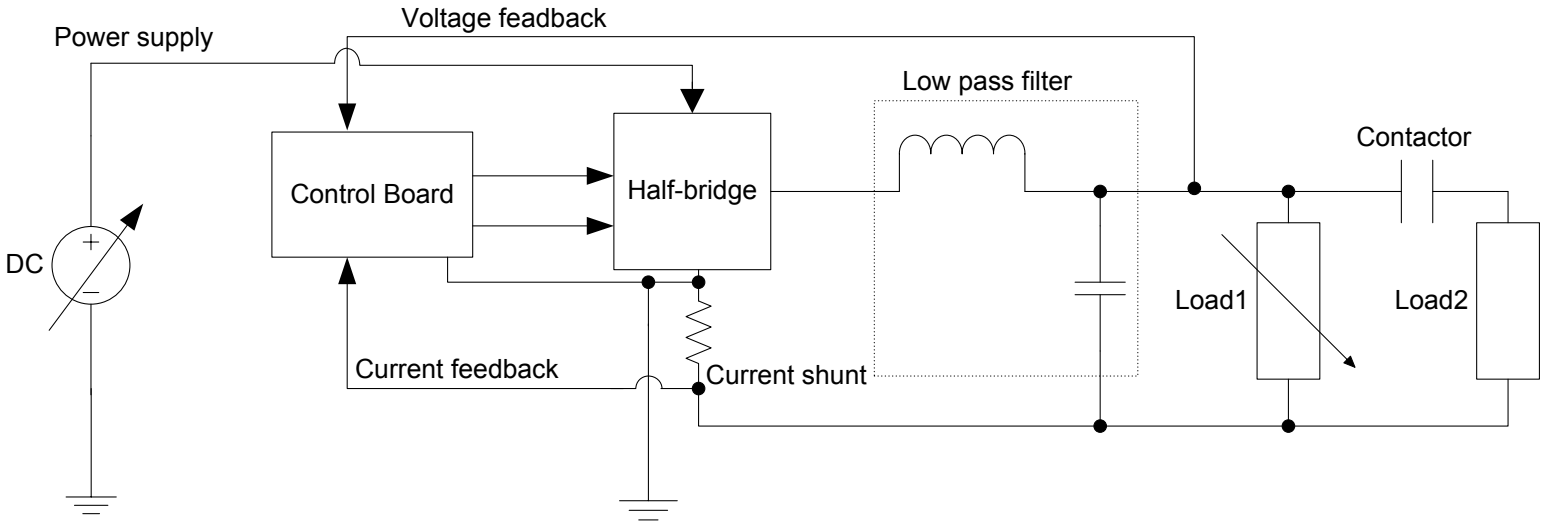

Figure 5-11 Principal connection of the SBC

5.4 Initial measurements

This section presents the initial measurements that were performed before the final results were logged. The purpose is to analyze the measurements and detect potential errors. The JFET half-bridge was investigated during both DPT and Buck operation and the BJT half-bridge was investigated during DPT.

5.4.1 DPT JFET half-bridge

The external gate resistor, Rg, is set to 12 Ω for all switching waveforms unless other values are given in the figure capitation. Figure 5-12 shows the DPT waveforms for a drain current of 10A and DC-link voltage equal to 500V. The specific turn-on and turn-off waveforms are given in Figure 5-13. From the figures one can see that there is a large current overshoot at turn-on. The overshoot is caused by discharging of the parasitic capacitances of the circuit. The overshoot will therefore increase with increasing voltage and with increased switching speed. This can be seen by Figure F-1 and Figure F-2 in appendix F.

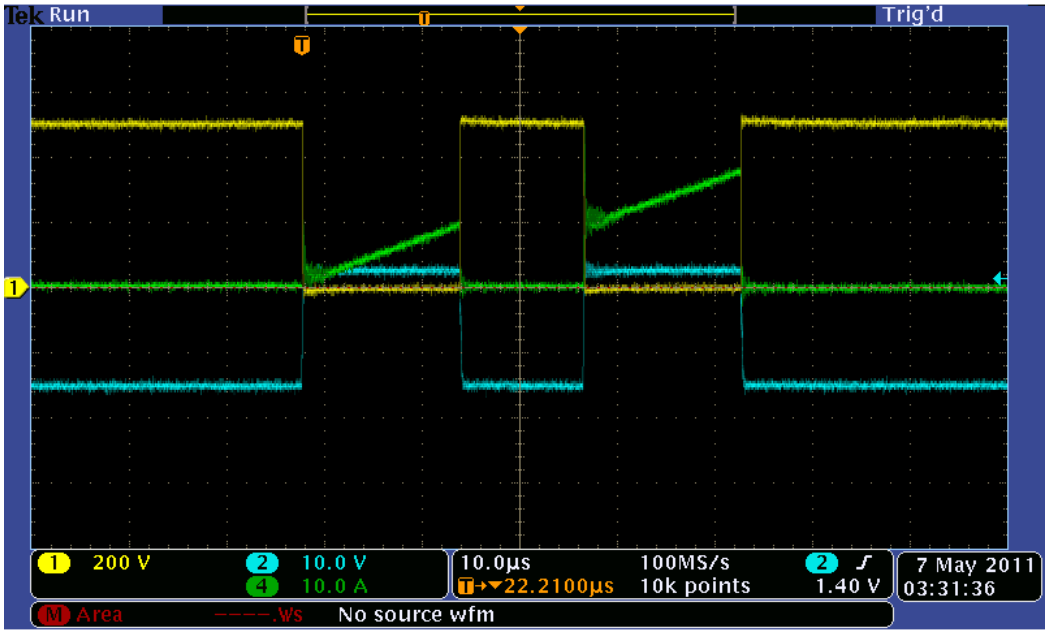

Figure 5-12 DPT JFET with I_d=10A and V_{dc}=500V, I_d is green and V_{DS} is yellow. *"Voltage shifted 6.5ns"*

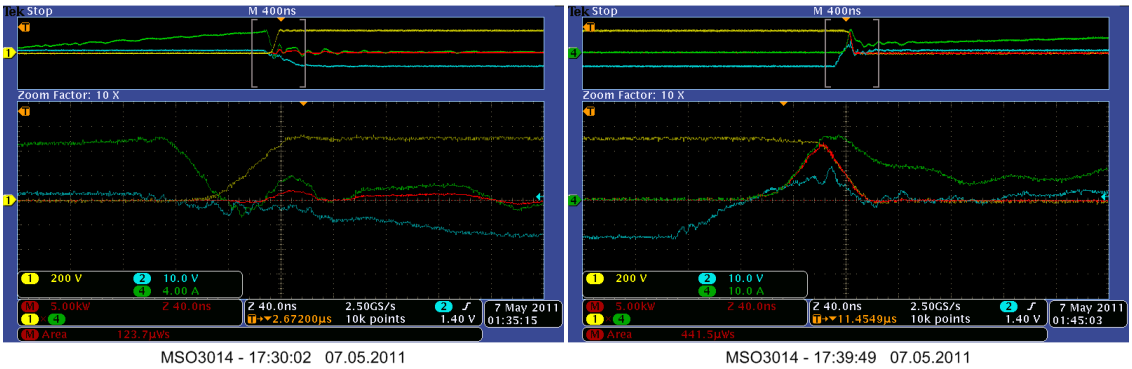

Figure 5-13 DPT JFET turn-off to the left and turn-on to the right. The red curve shows the dissipated power. *"Voltage shifted 6.5ns"*

The figure below shows how the turn-on changes when the switching speed is changed. It is easy to see that there is a strong correlation between the current overshoot and the switching speed. By increasing the gate resistor from 0 to 67.7Ω the current peak was reduced from 25A to 13.6A. Figure 5-15 shows the turn-off for the same gate resistances. Generally, all oscillations and ringings become smaller when the switching speed is reduced. On the other hand, reduced switching speed leads to increased switching losses. Hence, a proper trade-off between low switching losses and small oscillations has to be made. Chapter 7.1 deals with this issue.

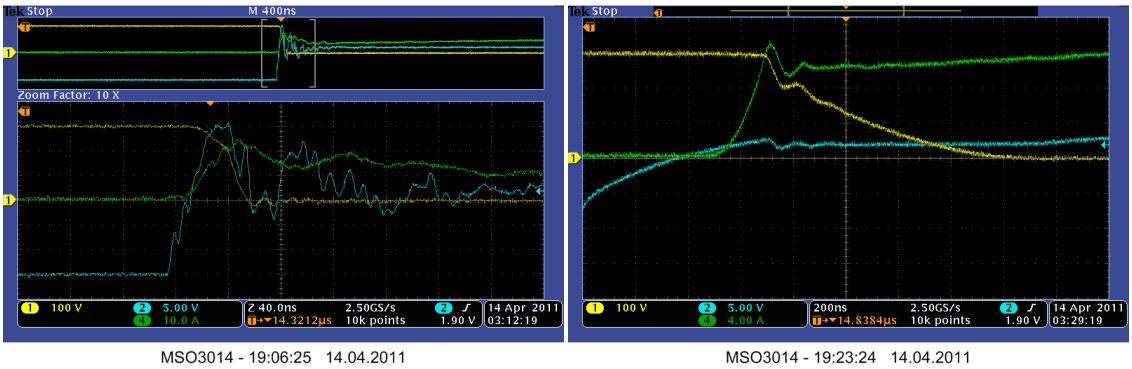

Figure 5-14 Turn-on with I_d=10A and V_{dc}=300V, R_g=0Ω in the figure to the left and 67.6Ω in the one to the right

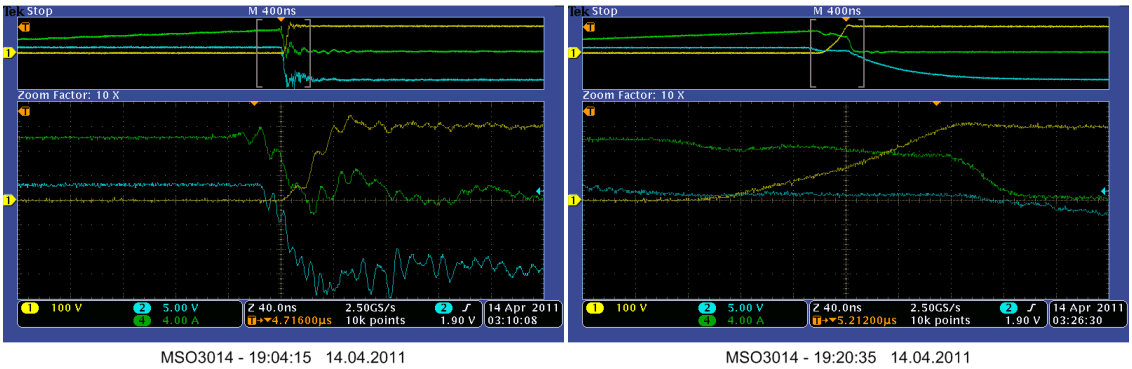

Figure 5-15 Turn-off with I_d=10A and V_{dc}=300V, R_g=0Ω in the figure to the left and 67.6Ω in the one to the right

If the turn-off waveforms to the left in Figure 5-13 and Figure 5-15 are studied, one can see that they are somehow unexpected. The drain current reaches almost zero before the voltage starts to rise. It looks like soft switching created by a turn-off snubber. Theoretically one would expect that drain-source voltage has to reach the DC voltage before the freewheeling diode gets forward biased and starts to conduct. Hence, the school book picture would be; first an increase in the drain-source voltage followed by a decrease in the drain current when the current commutates from the transistor to the diode. Section 6.1.1 gives an explanation of this phenomenon by use of simulations.

As discussed earlier, the JFETs require a clamping capacitor, between gate and source, to stabilize the gate voltage. The selection of this capacitor will also affect the switching behavior. Figure 5-16 and Figure 5-17 show turn-on for two different values of the capacitor. When increasing the capacitance, the current rises slower at the beginning of the turn-on. This can be seen by the inductance plateau which is longer in time, but smaller in value, for the 10nF case. The turn on delay increases for increasing capacitance value. This makes sense since the gate driver must supply more charge to reach the threshold. The drain current is measured with two different Rogowski coils in the figures. The green curves are from the Athena coil and purple curves are from the PEM coil. From the measurements one can see that PEM coil has much higher oscillations than Athena coil. These oscillations are most probably a result of the low bandwidth of the coil. The bandwidth of the PEM coil is only 20MHz while the Athena has 70MHz. Hence, the Athena is the preferred choice of these two.

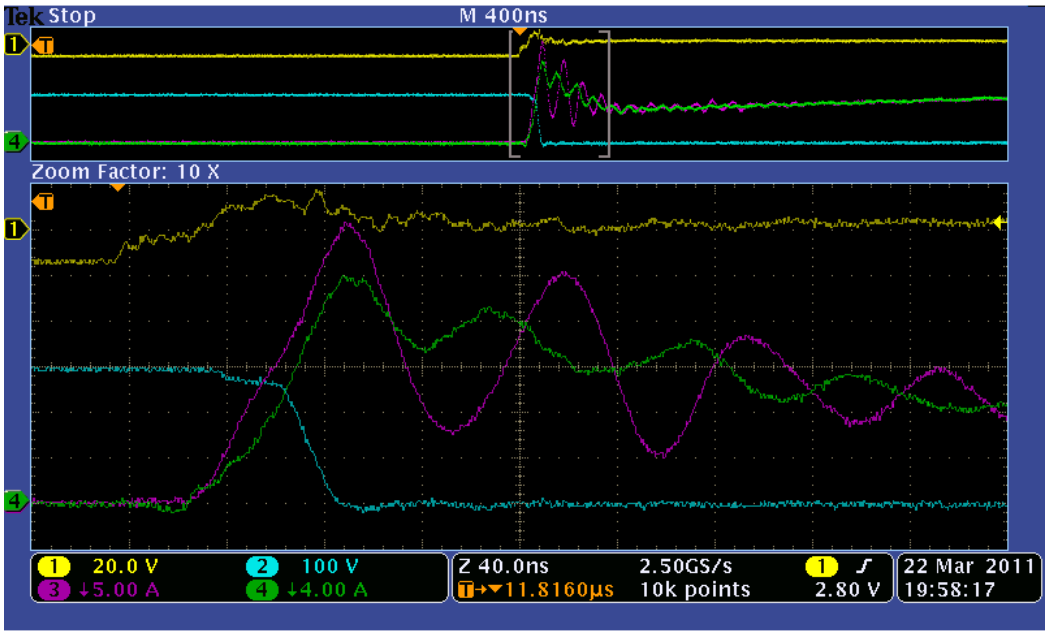

Figure 5-16 Turn-on JFET I_d=10A V_{dc}=300V C_g=10nF R_g=1.8

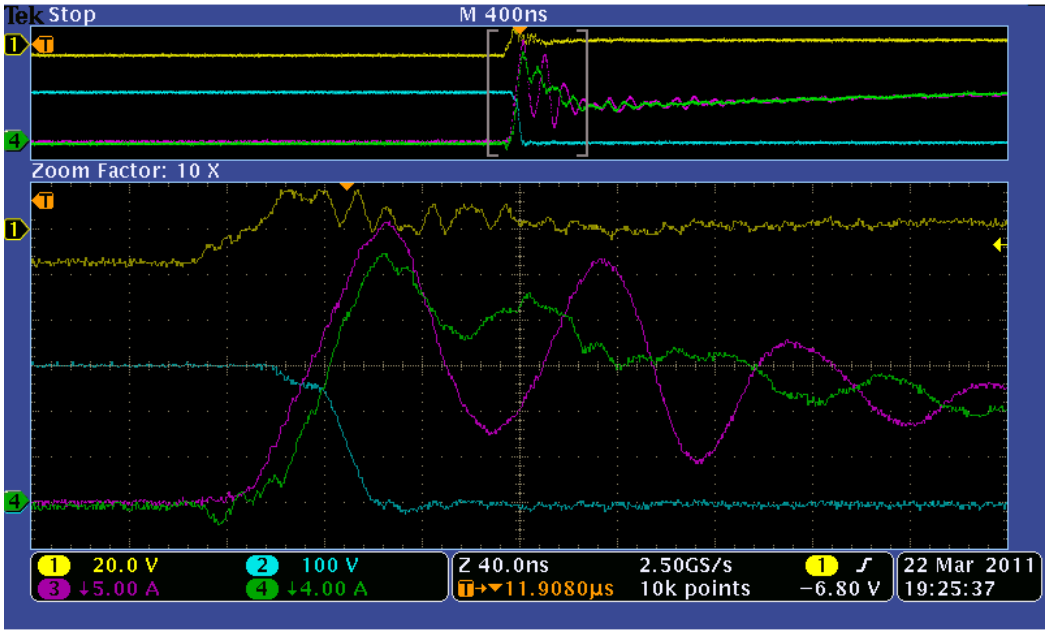

Figure 5-17 Turn-on JFET I_d=10A V_{dc}=300 C_g=4.7nF R_g=1.8

An interesting observation is that the voltage rise time decreases for increasing currents. The voltage rise time at six ampere is actually twice as long as in the 20 ampere case. Also the ripple and the overshoot in the drain source voltage increases with increasing turn-off current. This can be seen by Figure F-3 in appendix F. As described in the

"layout consideration" section, the selection of inductor type can influence the switching behavior. Two different inductors were tested to investigate this, one 150µH air coil and one 1mH coil with iron core. Figure F-4 from appendix F shows the turn-on waveforms for both coils. The turn-on with the iron coil has more oscillations in the current. This could be due higher parasitic capacitance in the iron coil. The iron core coil has higher inductance than the air coil and oscillations could also be created by a resonance between the coil and some stray capacitances in the circuit. The turn-off waveforms were almost unchanged.

For safety reasons the heat sink has been grounded during all measurements. For the room temperature testing the heat sink was electrically connected to the ground plane of the PCB. During the high temperature testing a thermal, but also electrical, isolation was used between the heat sink and the PCB to prevent excessive heating of the components. The change in the ground connection dramatically changed the turn-off waveforms of the JFETs. Figure 5-18 shows the turn-off when they are electrically connected and Figure 5-19 shows the waveforms when the isolation is introduced. In the latter case the current oscillations are increased with a factor 2.5. This could be due to changes in capacitance towards ground.

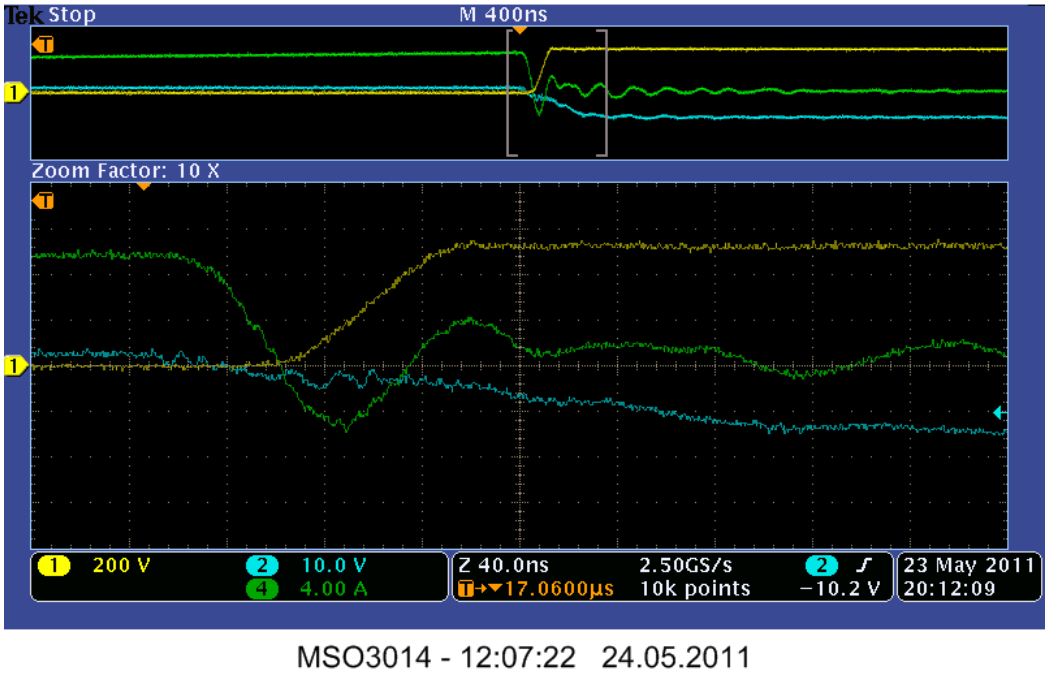

Figure 5-18 Turn-off JFET I_d=10A V_{dc}=500V, heat sink ground connected to the PCB ground plane. *"Voltage shifted 6.5ns"* and *"Current shifted 10ns"*

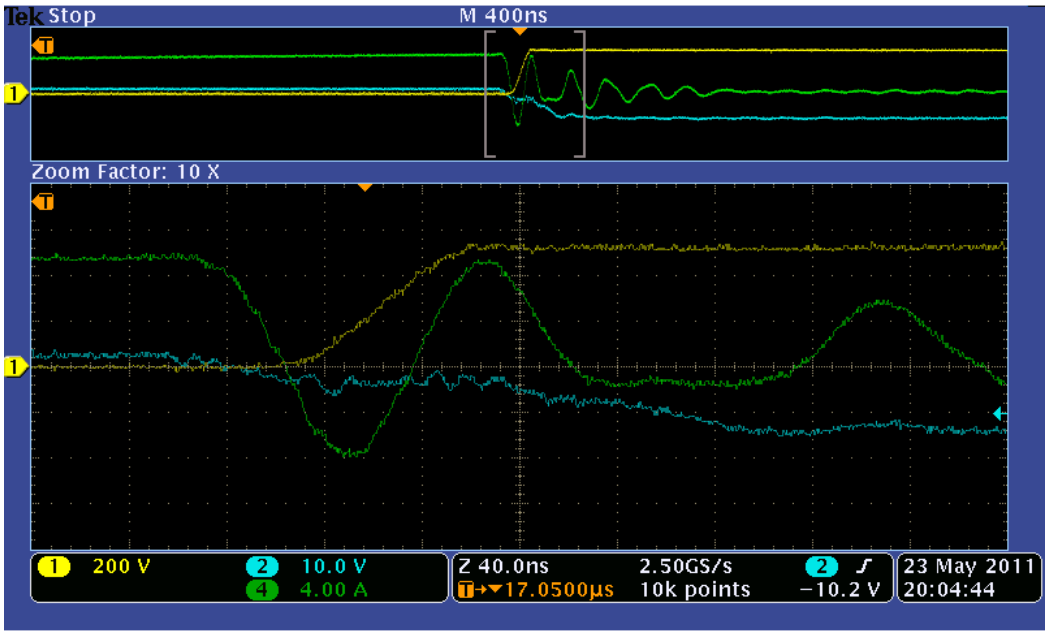

Figure 5-19 Turn-off JFET I_d=10A V_{dc}=500V, heat sink ground not connected to the PCB ground plane. *"Voltage shifted 6.5ns"* and *"Current shifted 10ns"*

5.4.2 DPT BJT half-bridge

Most of the discussions performed in the JFET section are also valid for the BJTs. Hence, only the BJT figures and some extra comments are presented in this section.

The figure below shows the DPT for BJTs for a DC voltage of 300V and a drain current of 6A. The turn-on and turn-off waveforms can be seen in Figure 5-21 and Figure 5-22 respectively. Figure 5-23 shows the same waveforms for 500V. When comparing the BJT and the JFET waveforms there is one noticeable difference in the turn-off. The BJTs do not have the same degree of soft switching as observed for the JFETs. The Schottky diodes used in the BJT half-bridge have only one fourth of the junction capacitance as the ones used in the JFET half-bridge. Hence, the junction capacitance of the freewheeling diodes acts as a turn-off snubber.

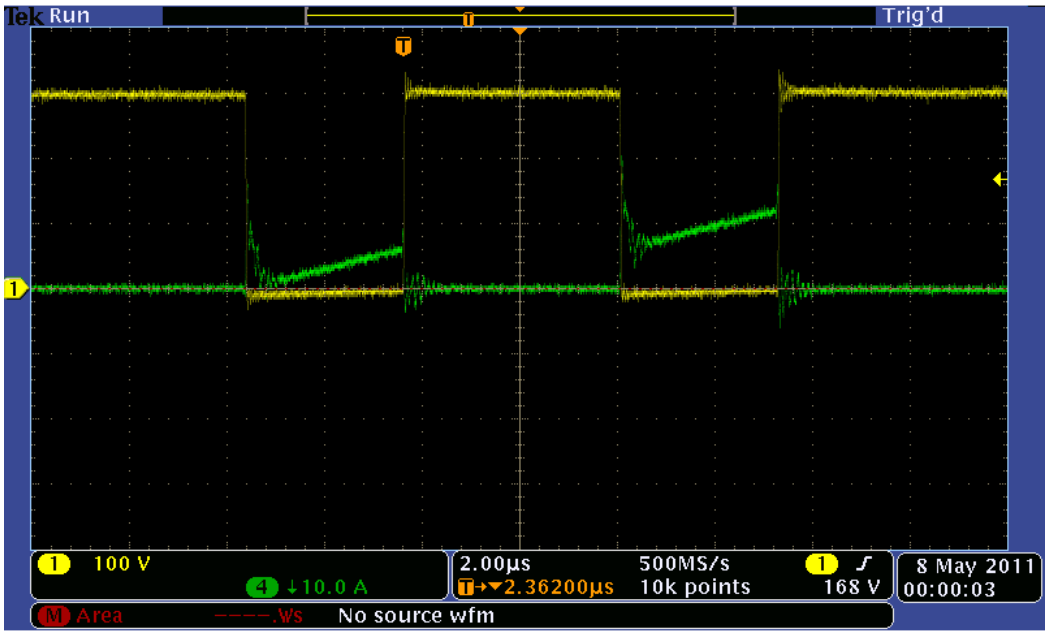

Figure 5-20 DPT BJT with I_d=6A and V_{dc}=300V, I_d is green and V_{DS} is yellow. *"Voltage shifted 6.5ns"*

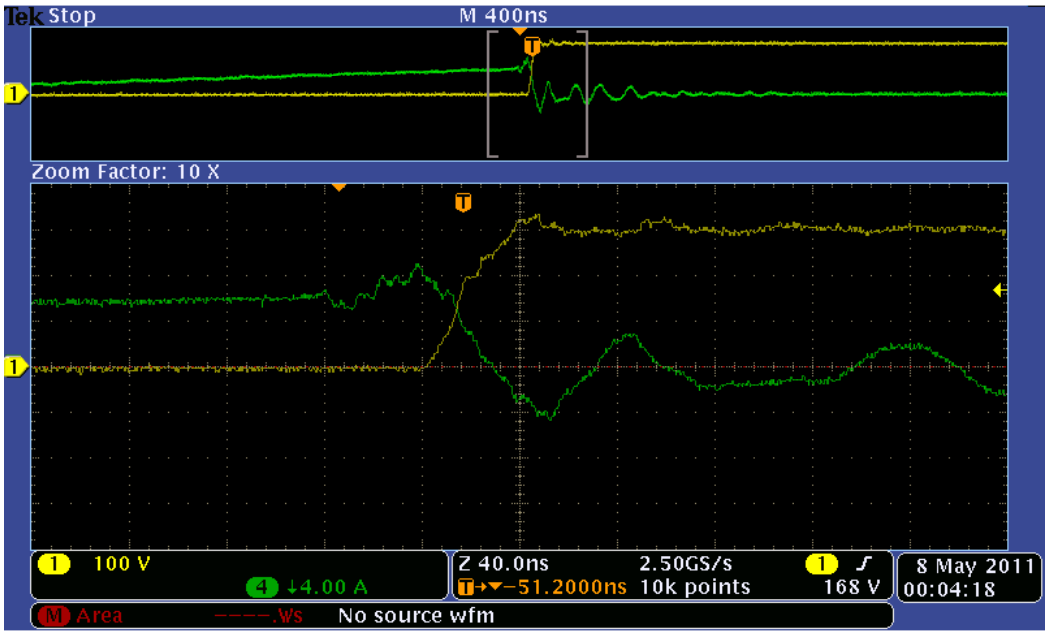

Figure 5-21 Turn-on with I_d=6A and V_{dc}=300V, I_d is green and V_{DS} is yellow. *"Voltage shifted 6.5ns"*

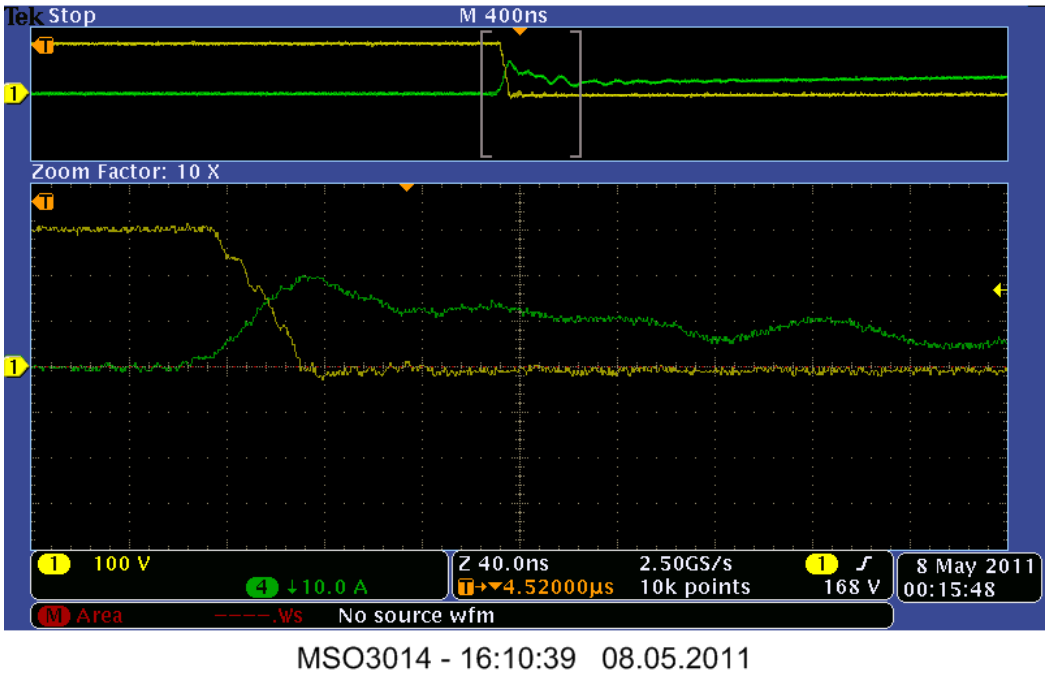

Figure 5-22 Turn-off with I_d=6A and V_{dc}=300V, I_d is green and V_{DS} is yellow. *"Voltage shifted 6.5ns"*

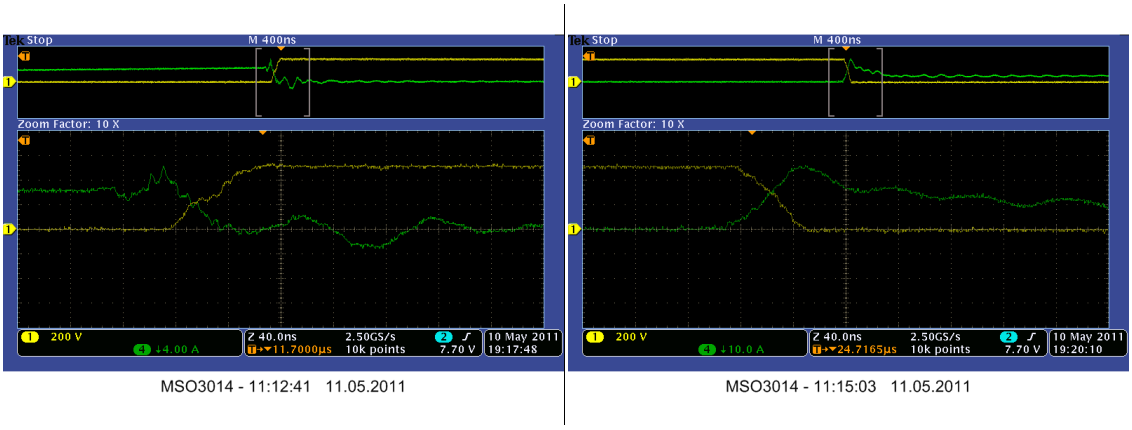

Figure 5-23 DPT BJT with I_d=6A and V_{dc}=500V, turn-off to the left and turn-on to the right. *"Voltage shifted 6.5ns"*

5.4.3 Buck converter operation

Before testing a converter it is important to know that the control circuit operates correctly. It was therefore decided to check the output of the control board before connecting it to the converter. The control board has two complementary output signals which should have a 0.5µs delay between them. In the first measurement, see Figure 5-24, there was no delay. If these signals had been applied to the converter it would have resulted in a shoot through.

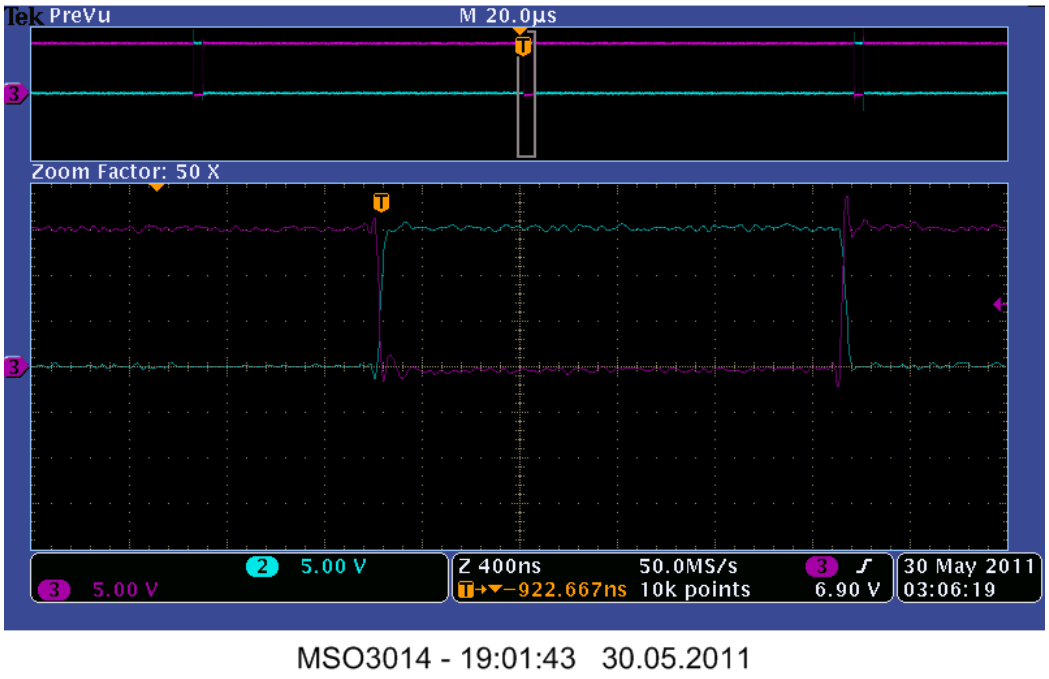

Figure 5-24 Initial control board output

Figure 5-25 shows the exponential ramp which should create the time delay. The step at beginning of the ramp triggers the output buffer momentarily. The voltage step indicates that the capacitance of the diodes D1 and D2 in Figure 4-23 is too large and therefore bypasses a current which is large enough to raise the voltage to buffer threshold. By changing the diodes, to 1N4148 small signal pin diodes, this problem was solved. Section 6.1.2 presents simulations of the dead time generation circuit.

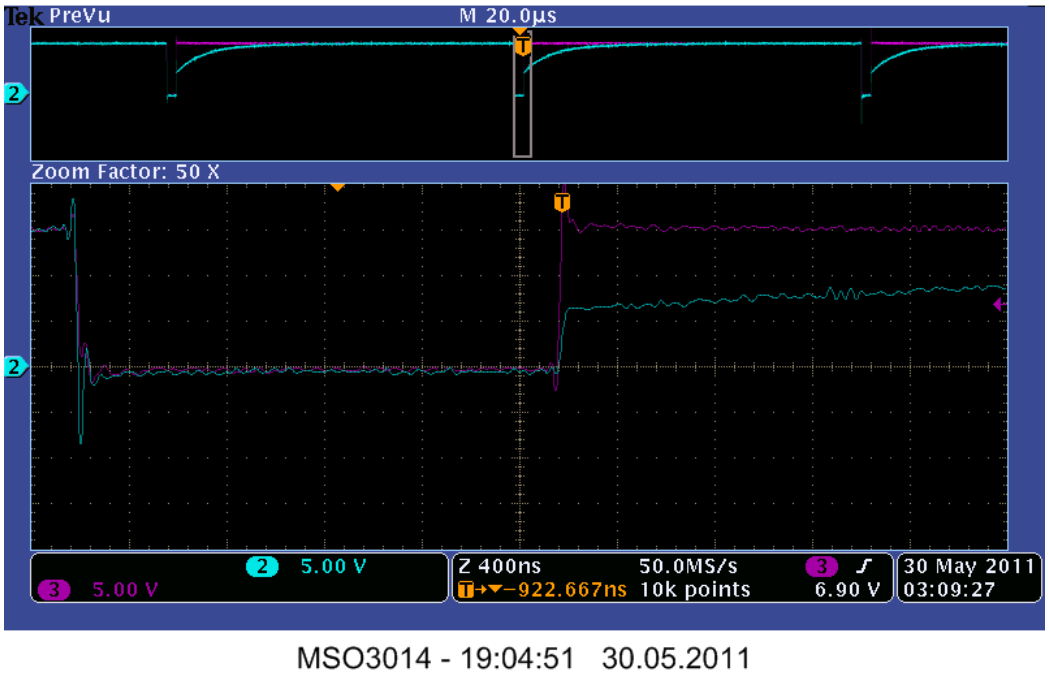

Figure 5-25 Step in voltage due to the capacitance of the Schottky diode

After the controller was up-and-running it was connected to the half-bridge. When the synchronous buck was powered up it was not able to reach a stationary operation point. The inductor current suffered from large subharmonic oscillations and the ripple in output voltage was several volts. Figure 5-26 shows the converter operation. From the figure one can see that the inductor current goes negative during the subharmonic oscillations. Regular buck converters can only have positive inductor current. The freewheeling transistor in a SBC allows the inductor current to change direction and therefore go negative. This is one of the major differences between buck converters and synchronous buck converters. During the blanking time of the SBC the output voltage is dependent of the direction of the current [9]. This introduces nonlinearity in the relationship between the controller output and the output voltage. The controller was designed for a regular buck converter without dead time and current dependent output voltage. The assumption to neglect these effects has proved to be unrealistic, and the controller is not able to damp subharmonic oscillations which are created at start-up of the convert.

To ease the task of the controller the output signal to the freewheeling transistor was removed and the transistor was kept permanently off. After the change the current is now longer able to go negative and the half-bridge will operate as step down converter with 0.5µs delay in the on-signal. This reduces the miss-match between the model of the converter, which the controller is tuned for, and the real converter. The change turned out to be sufficient to stabilize the converter. Figure 5-27 shows the stable operation of the Buck converter. The output ripple voltage is very low and the output current shows no sign of subharmonic oscillations. In the result chapter the half bridge is therefore operated as a Step down converter instead of a SBC.

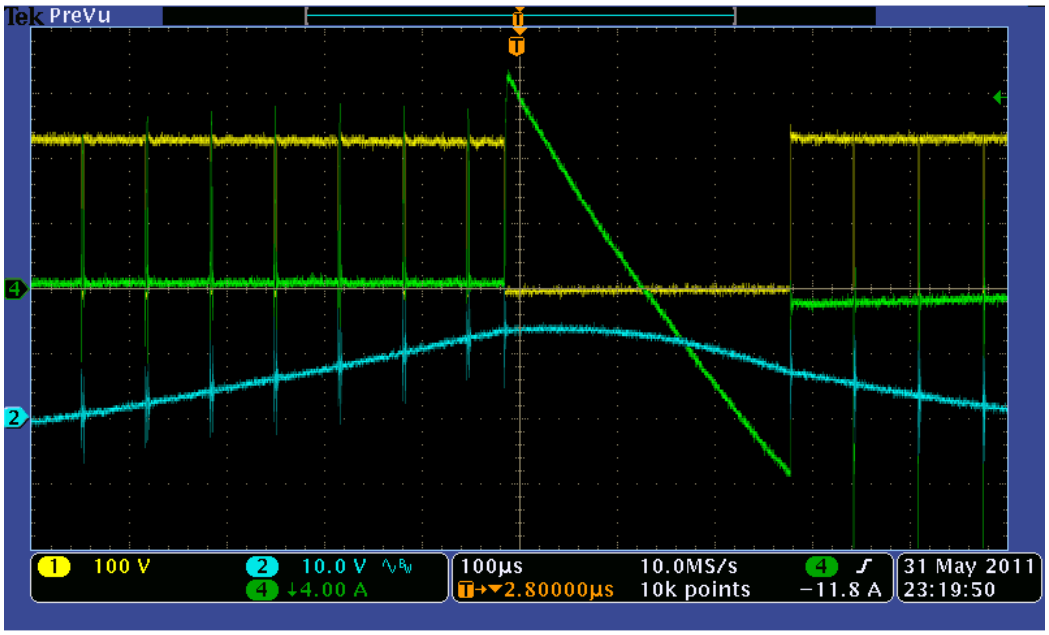

Figure 5-26 Output waveforms SBC, the input voltage to output filter is yellow, the ripple component of the output voltage is blue and current through the lower/freewheeling transistor is green.

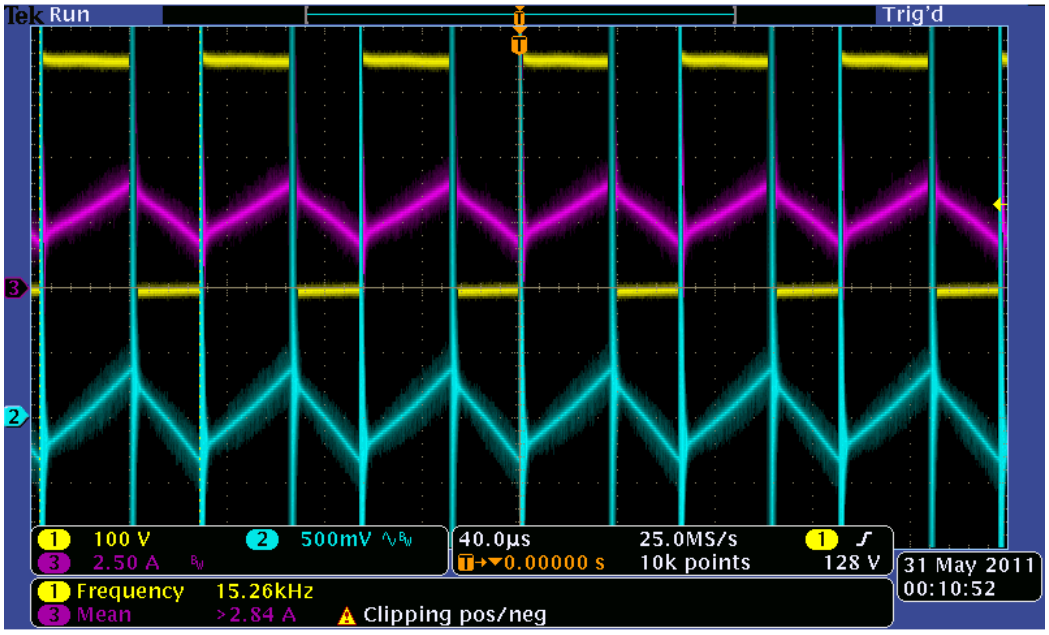

Figure 5-27 Stable operation of Buck converter, the input voltage to output filter is yellow, the ripple component of the output voltage is blue and the inductor current is purple.

6 Simulations in LTspice

All simulations are performed with the LTspice software. LTspice is a spice based simulation platform and it available for free from the producer. The software is well suited for simulations of both electronic and power electronic circuits. The purpose of using the simulation tool is to obtain a deeper understanding of the converter dynamics. It can also be used to identify the influence of parasitic circuit elements and to understand the transistor switching waveforms.

6.1 Influence of parasitic

6.1.1 Soft switching due to parasitic capacitances

It was decided to use a well known transistor to investigate the soft switching behavior of the JFETs. A standard MOSFET model was selected from LTspice component library. The MOSFET was tuned to have approximately the same switching speed as the JFETs. The simulation model can be found in appendix G1. First, the DPT was performed with ideal diodes and an ideal inductor. The result is presented in the figures below. In the turn-off waveforms the voltage reaches the DC-link value before the current starts to fall. There is no overshoot in the current at turn-on. These results are as expected for the ideal case.

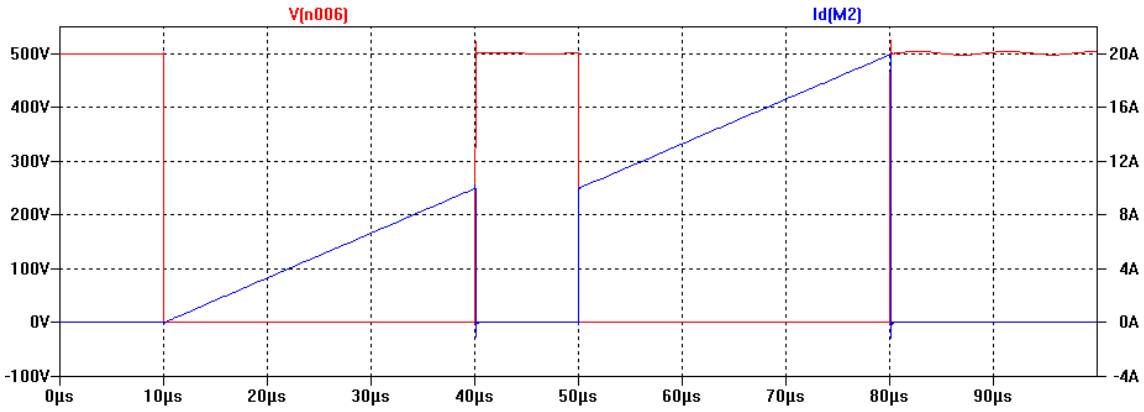

Figure 6-1 DPT MOSFET with ideal diodes

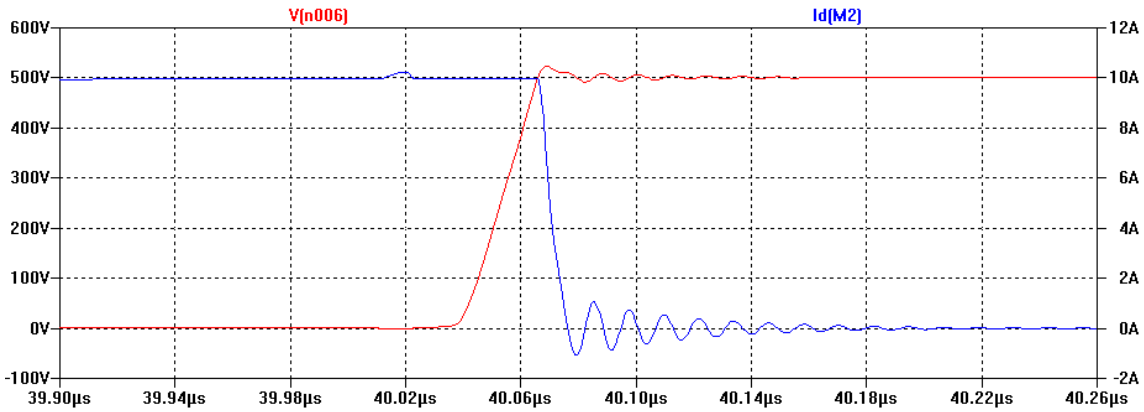

Figure 6-2 Turn-off with ideal diodes

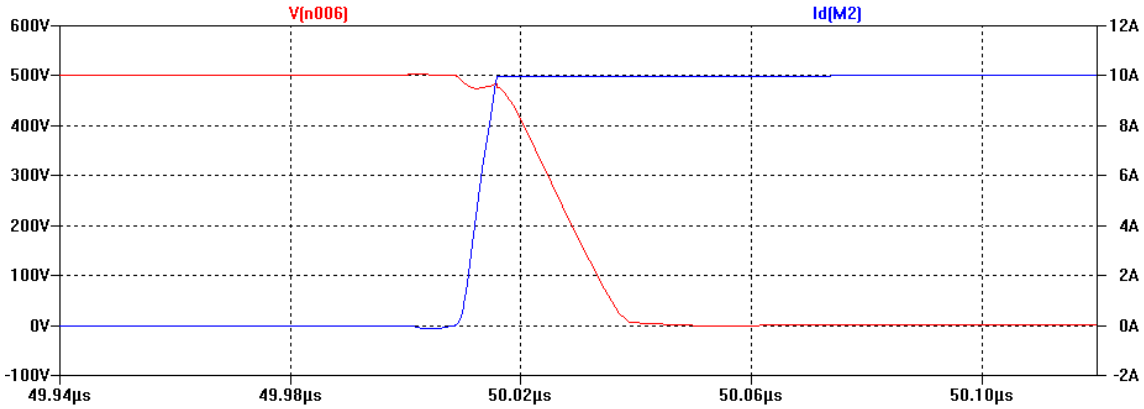

Figure 6-3 Turn-on ideal diode

The simulations were repeated with new diodes and with a non ideal inductor. The new diodes are a model of the SDP30S120, which are the ones used in the actual test. The model was created by [58]. From the data sheet of the SDP30S120 one can see that the junction capacitance (C_j) is 3.7nF at 1V reverse bias. Junction capacitances have strong voltage dependence and the capacitance of the SDP30S120 is reduced to 0.1n at a reverse voltage of 600V. A 150pF capacitor was connected in parallel with the inductor to model its parasitic capacitance. The results are presented in Figure 6-4, Figure 6-5 and Figure 6-6. Figure 6-5 shows that the turn-off losses are greatly reduced compared to the ideal case. Figure 6-7 is used to explain the turn-off waveforms. Initially, the voltage over Q2 is approximately zero and the DC voltage lay over the inductor L1. At the beginning of the turn-off, the transistor voltage is clamped by capacitor C2 and the load current is shared between C2 and Q2. As the voltage starts to rise C2 decreases quickly and can no longer clamp the voltage over Q2. This marks the start of the second stage of the turn-off and it is indicated as the break in current waveform. As the voltage over the inductor starts to fall the capacitors C1, C3 and C5 starts to discharge and the inductor current is shared between the capacitances and Q2. This keeps the transistor current low during the rest of the voltage rise time. If the capacitances are large enough the turn-off losses can be reduced to a neglect able value. During turn-on, all the capacitors charges/discharges through the transistor. This is the explanation behind the high current peak. One can say that the parasitic capacitances move the switching losses from the turn-off to the turn-on. Unfortunately, the total switching losses will be higher when the capacitances are included [9]. The switching losses were estimated for the two cases. In the ideal case the transistor switching energy is equal to 155.85µJ, divided between E_{off}=89.25µJ and E_{on}=69.6µJ. For the real case the switching energy is equal to 188.4µJ, divided between E_{off}=18.4µJ and E_{on}=170µJ. Hence, the total switching energy is more than 20% larger.

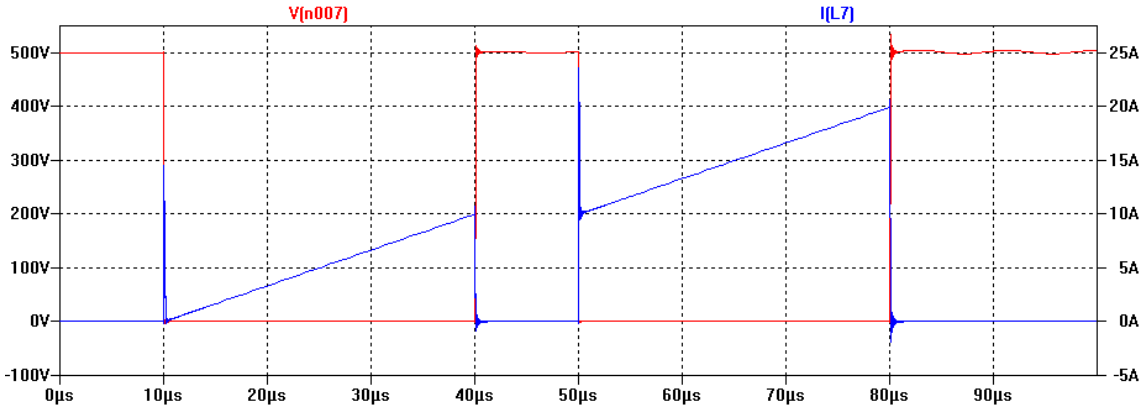

Figure 6-4 DPT MOSFET with real diodes and non ideal inductor

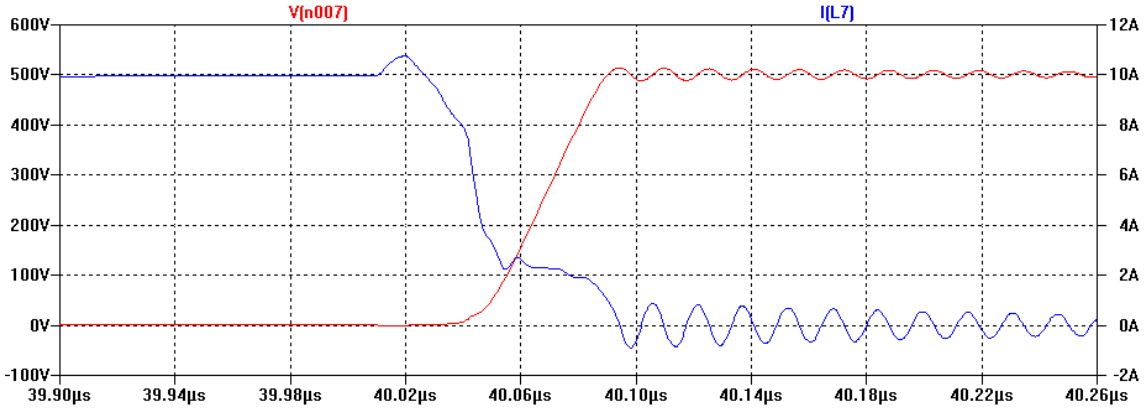

Figure 6-5 Turn-off with real diodes and non ideal inductor, C_j=3.7nF

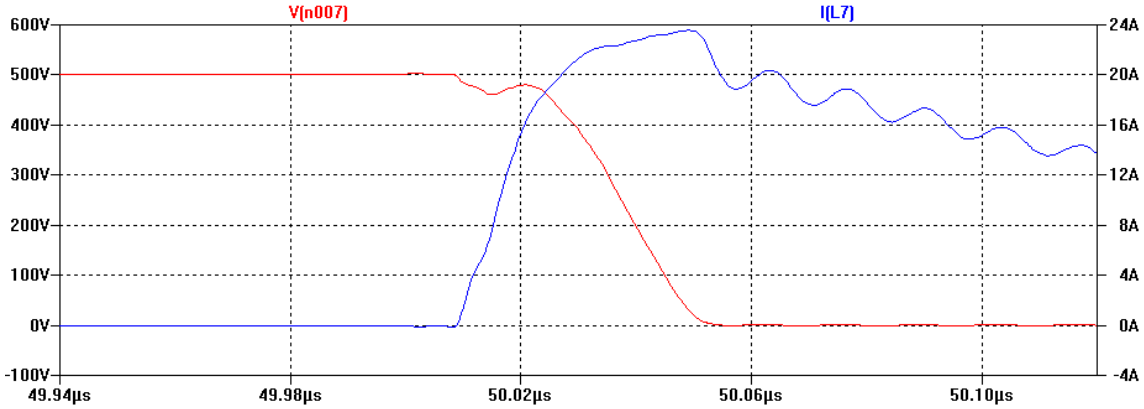

Figure 6-6 Turn-on with real diodes and non ideal inductor, C_j=3.7nF

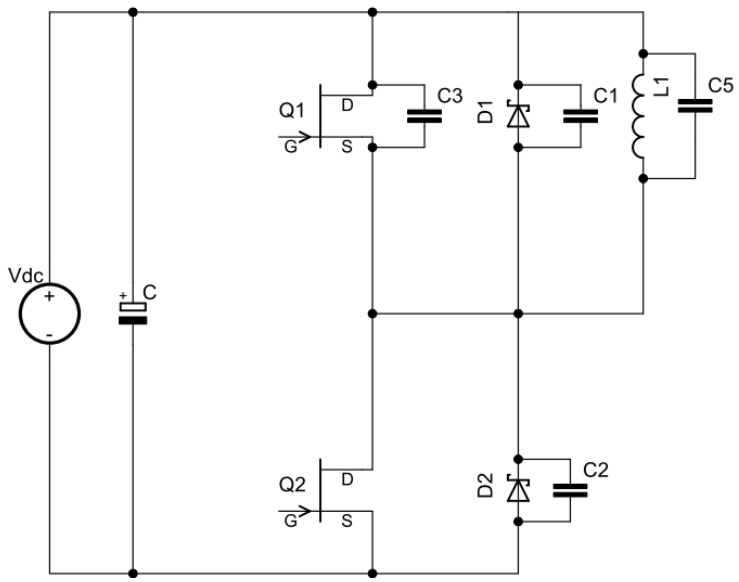

Figure 6-7 Explanation of soft switching

The simulations were also performed for a lower value of the junction capacitance. Figure 6-8 and Figure 6-9 show the switching for a junction capacitance of 750pF at a reverse voltage of 1V. This is the same value as in the IDH15S120.

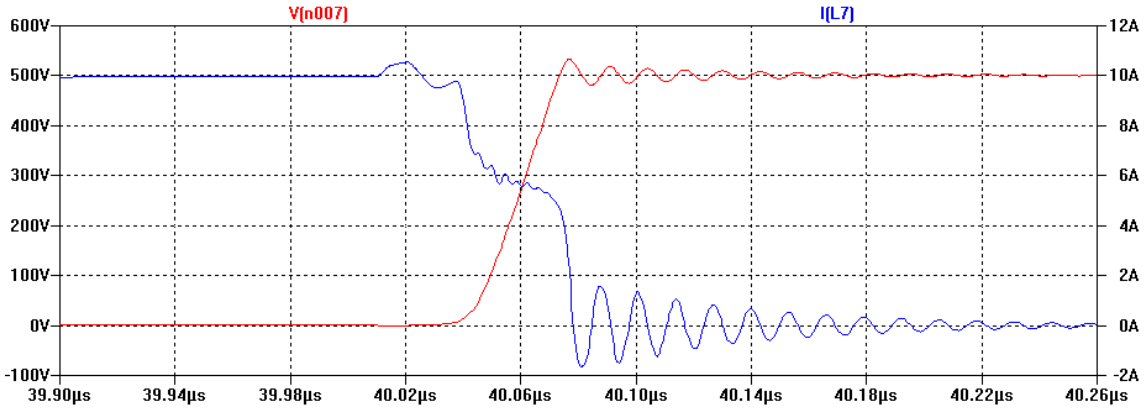

Figure 6-8 Turn-off with real diodes and non ideal inductor, C_j=750pF

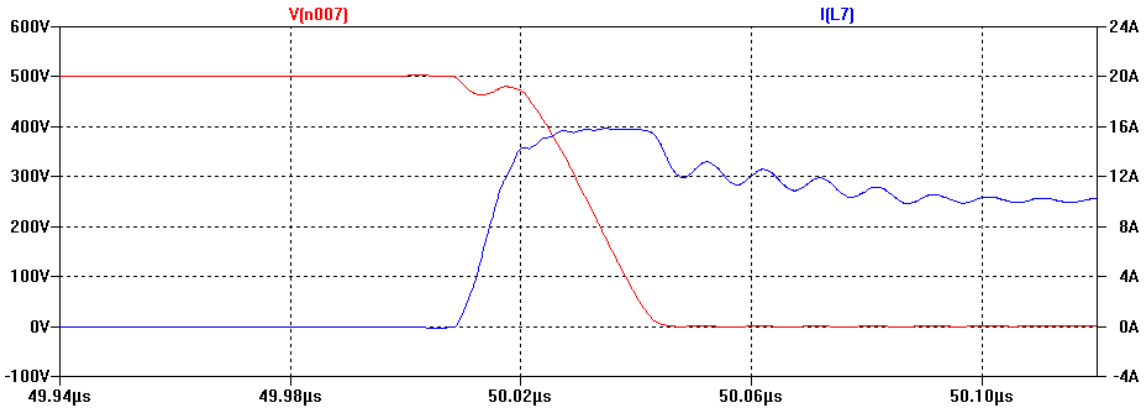

Figure 6-9 Turn-on with real diodes and non ideal inductor, C_j=750pF

6.1.2 Problems with dead time generation

The original Schottky diodes, D1 and D2 in Figure 4-23, had a junction capacitance of 550pF at 1V reverse bias. An equivalent Schottky diode was found in the LTspice library. The circuit for simulations of the dead time generation can be found in appendix G2. Figure 6-10 shows the resulting waveforms. The threshold voltage of the output buffer is 2.4V, thus the voltage step is more than large enough to trigger the output.

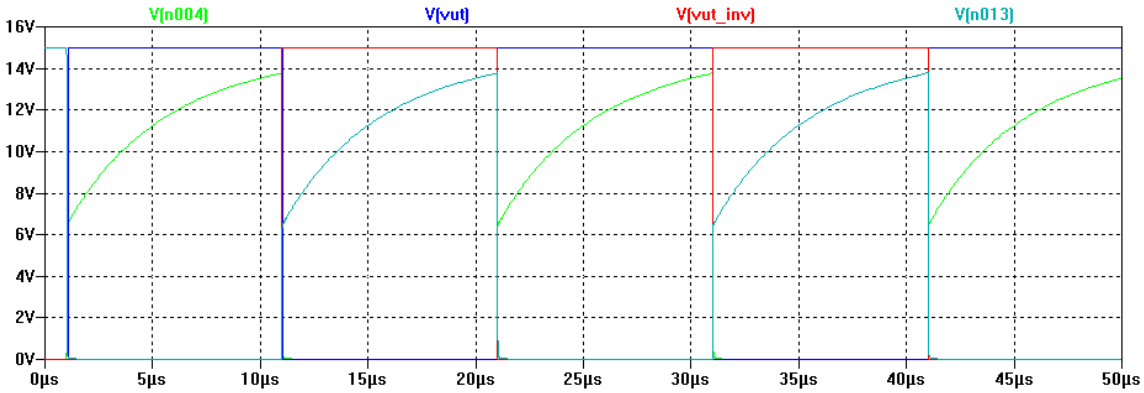

Figure 6-10 Control output with the original diode

It was decided to replace the Schottky diode with a small signal pn-diode. A standard 1N4148 diode was selected. Figure 6-11 shows the new result and one can see that dead time generation is working.

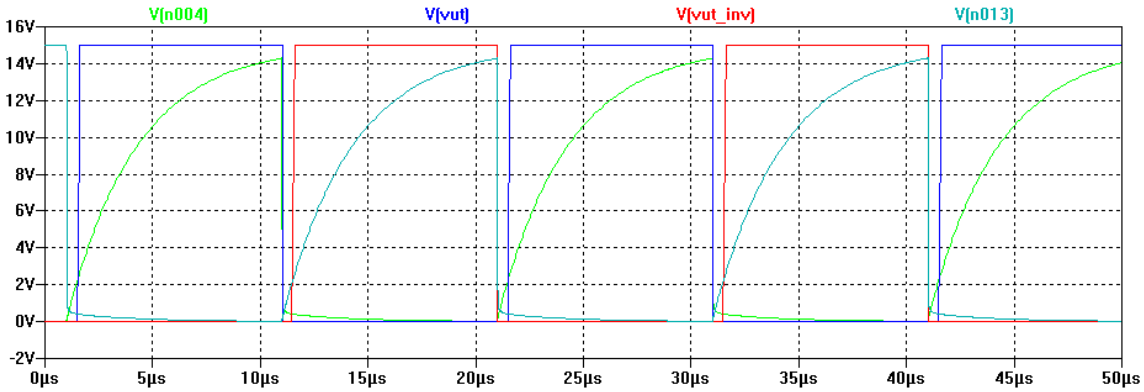

Figure 6-11 Control output with 1N4148 diode

6.2 BJT double pulse test

TranSiC, the manufacturer of the BT1206A, has created a quite accurate spice model of the device. This model can be used to reproduce the BJT switching waveforms presented in section 5.4.2. The largest challenge when reproducing the switching is to include the correct parasitics. A simulation model was created based on physical understanding and the earlier discussions. The final model, including all parasitics, is shown in Figure 6-12. The values of the parasitics were tuned by comparing the simulation results with the real measurements. The junction capacitance of the diodes was set to 750pF to match the IDH15S120. Figure 6-13 shows the model of the base drive circuit.

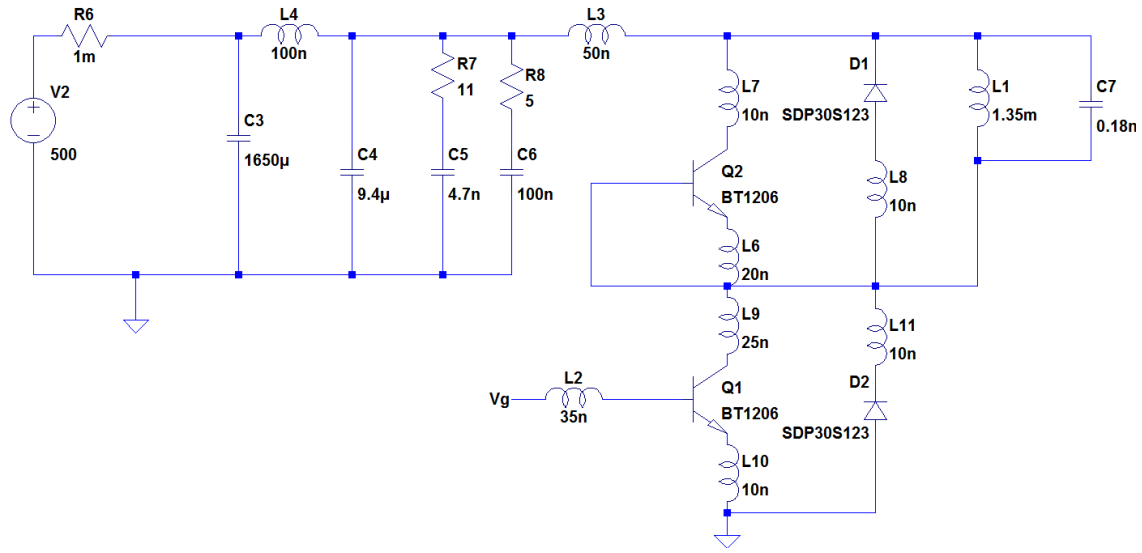

Figure 6-12 BJT simulation model including parasitic components

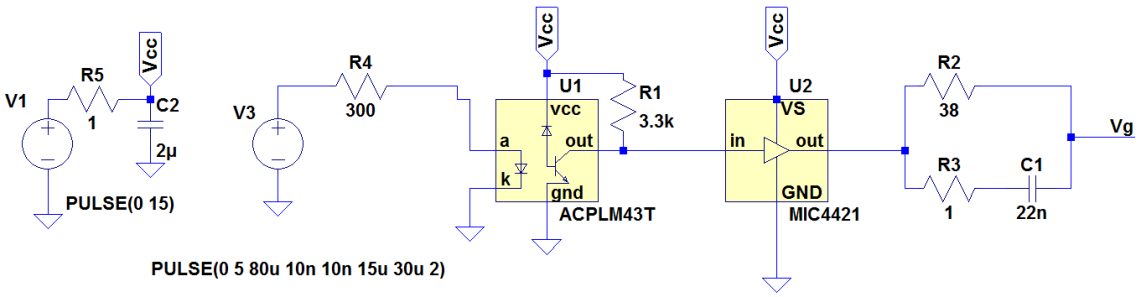

Figure 6-13 Base drive circuit for the BJTs

The simulation results are presented in Figure 6-14 – 6-16. The turn-on looks much the same as the measurements. From Figure 6-15 one can see that there still are some phenomena which need to be modeled before the turn-off waveforms can be fully understood. The mismatch could be due to weaknesses in transistor and diode models or it could be parasitic effects which not are included in the model.

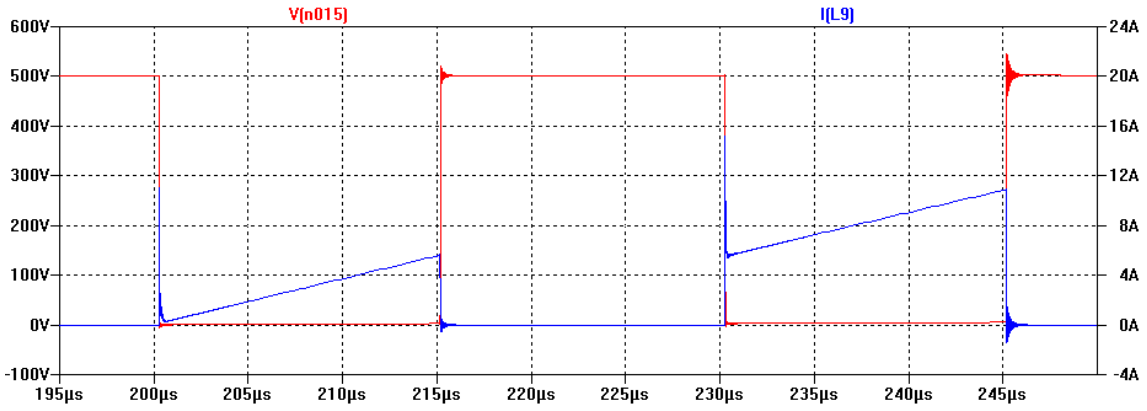

Figure 6-14 Simulated DPT

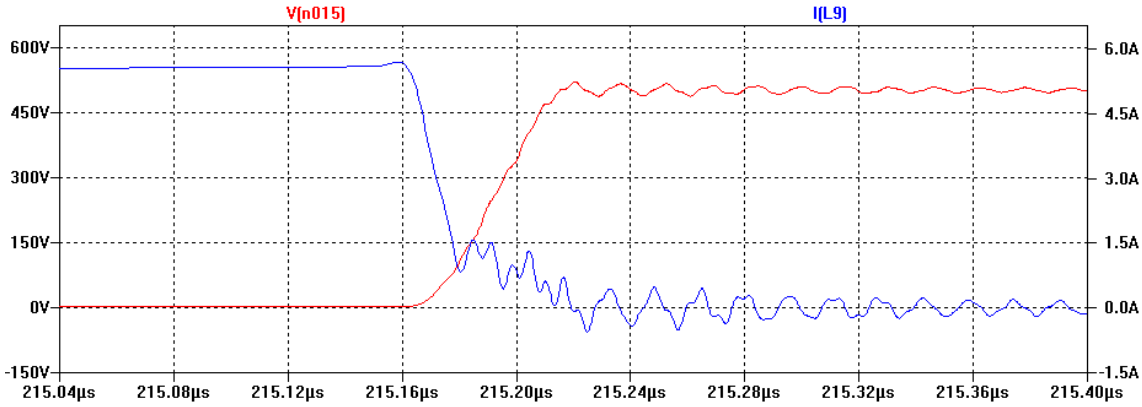

Figure 6-15 Simulated turn-off waveforms

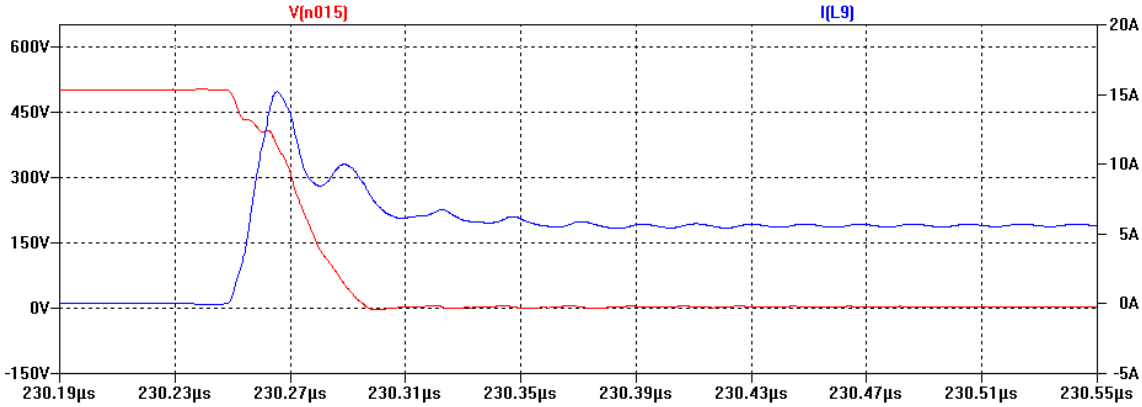

Figure 6-16 Simulated turn-on waveforms

6.3 PWM controller for Buck converter

The simulation models of the Buck and synchronous Buck converters are placed in appendix G3. Figure 6-17 shows the unstable operation of the SBC. The subharmonic current oscillations create large oscillations in the out voltage. One can see that the inductor current goes negative during each oscillation.

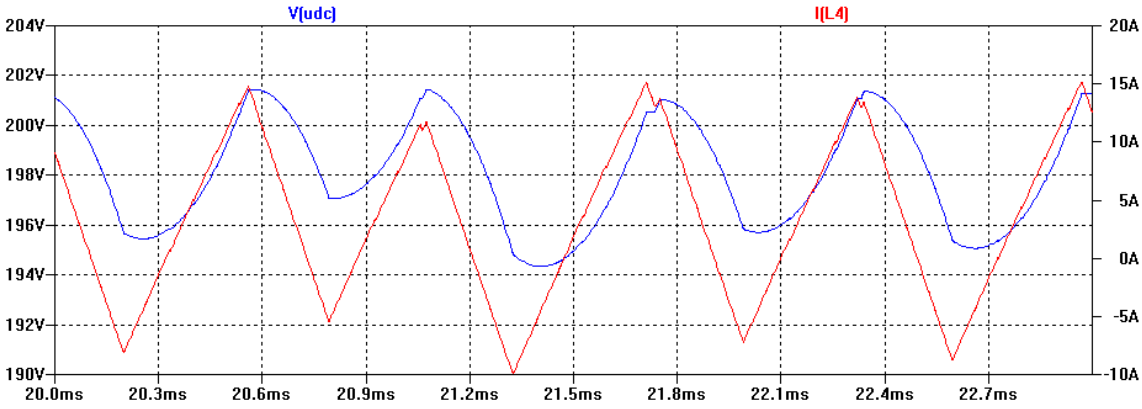

Figure 6-17 Subharmonic oscillations in SBC with V_{in}=400V and R_o=59Ω

Figure 6-18 shows the stationary operation of the Buck converter. The input voltage and the load are the same as for the SBC. By comparing the output ripple of the two

converters one can see that ripple in the Buck is approximately one tenth of the ripple in the SBC. The peak-to-peak value of the ripple voltage, in the Buck, is only 0.375% of the output voltage.

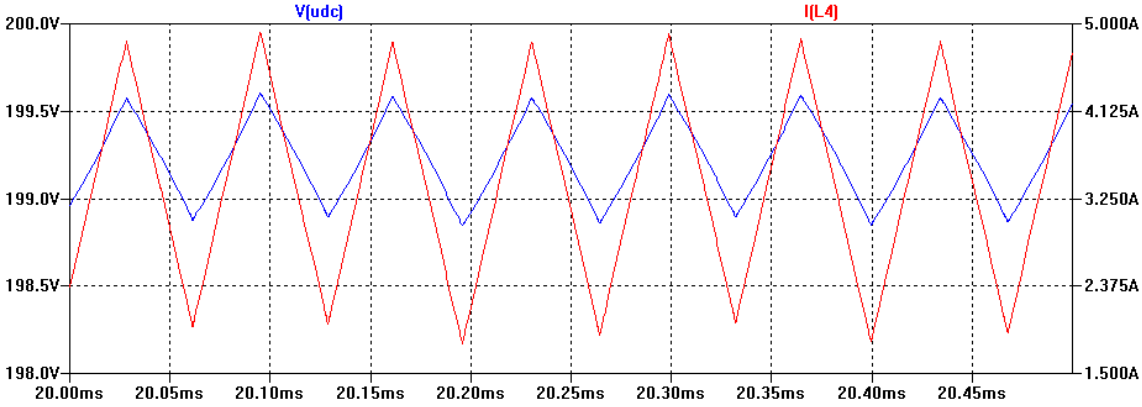

Figure 6-18 Operation of Buck converter with V_{in}=400V and R_o=59Ω

A step in load, from 59Ω to 29.5Ω, was simulated for the Buck converter. The response is shown in the figure below. There are almost no disturbances in output voltage during step load and a new stationary operation point is reached in less than 0.5ms.

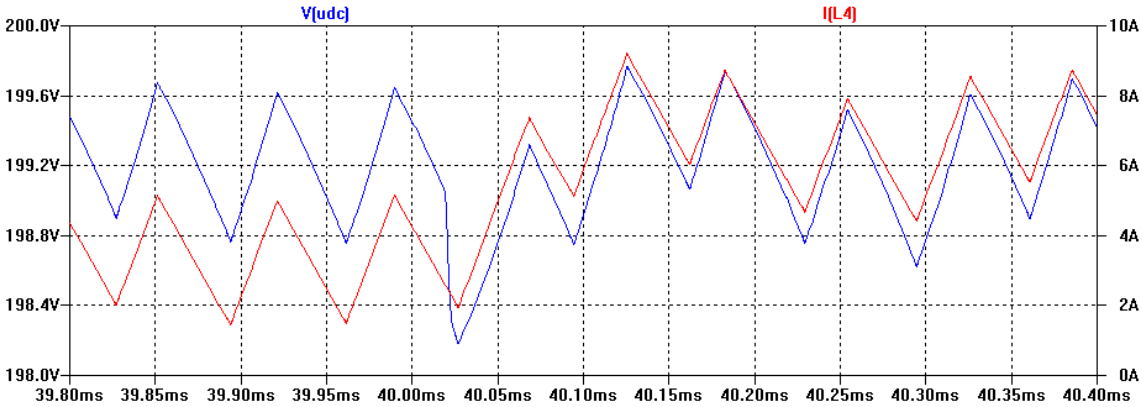

Figure 6-19 Step load for Buck converter with V_{in}=500V. The load changes from 59Ω to 29.5Ω

The start-up of the Buck converter is shown in Figure 6-20 and Figure 6-21. The controller IC limits the maximum current to 20A to protect the transistors. The voltage overshoot, when output voltage reaches its reference value, is less than 1%.

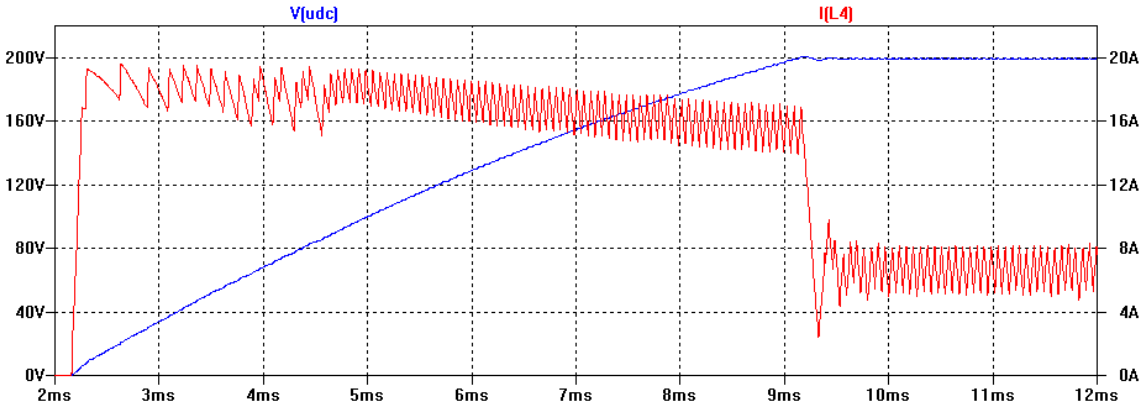

Figure 6-20 Start-up of Buck converter with V_{in}=400 and R_o=30Ω

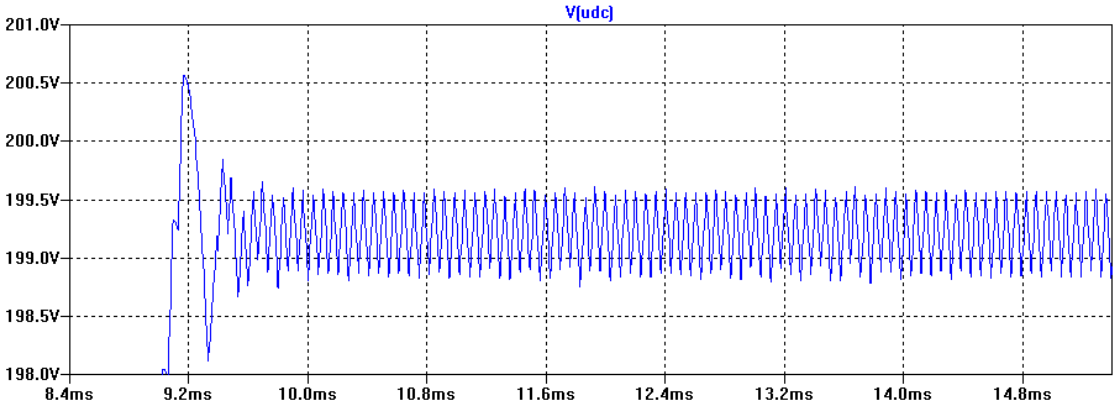

Figure 6-21 Voltage overshoot at turn-on of the Buck converter

7 Results and Discussion

The results of the double pulse testing and of the on-state voltage measurements are presented in this chapter. The performance of the step down converter is verified by laboratory measurements. A general discussion follows in the last subchapter.

7.1 Selection of gate resistance

This section presents the tuning of the gate resistor for the JFET driver. The switching losses are very much dependent on the switching speed, which again is tuned by the external gate resistor. The selection of gate resistor is a tradeoff between low losses and low EMI. A series of DPT, for different values of R_g, were performed to have a basis of comparison when making the selection. A DC-link voltage of 300V and a switching current of 10A were selected as the operation conditions. From Figure 7-1 and Figure 7-2 one can see that a gate resistance of 1.6 Ω gives the minimum switching losses. Selection of such a low value would result in excessive oscillations, thus a higher value should be selected. The turn-off losses and the turn-off time start to increase dramatically when the resistance exceeds 12Ω. Hence, a gate resistance of 12Ω seems to give the best overall performance. For the rest of the measurements R_g is equal to 12Ω.

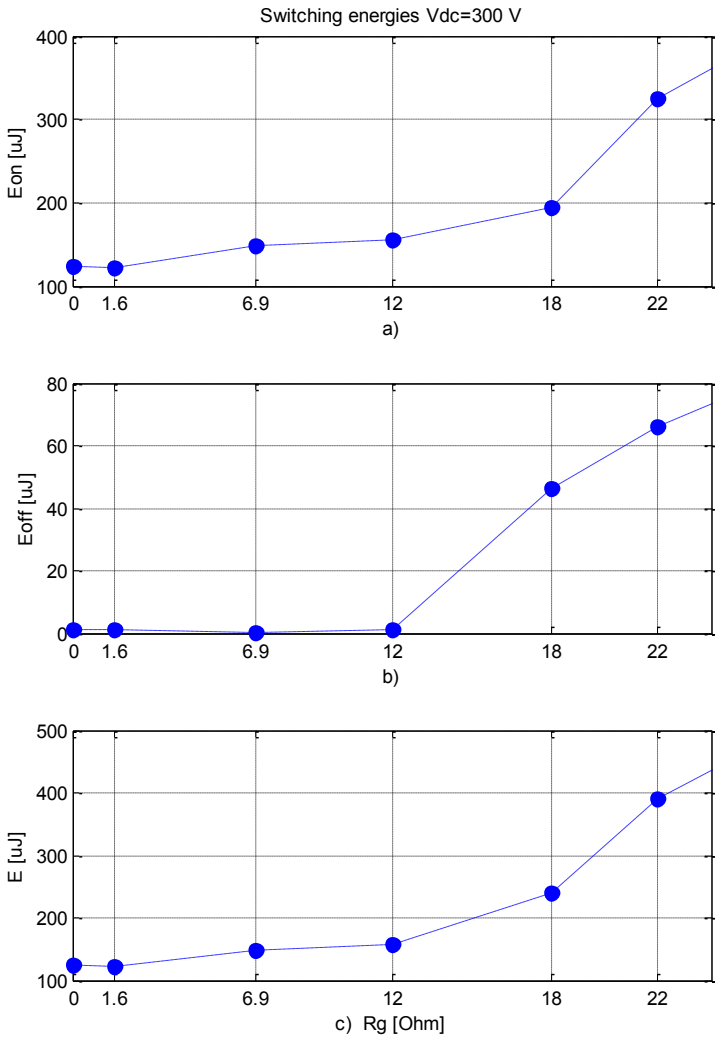

Figure 7-1 Switching losses as a function of R_g, R_g is an external gate resistance. I_d is 10A

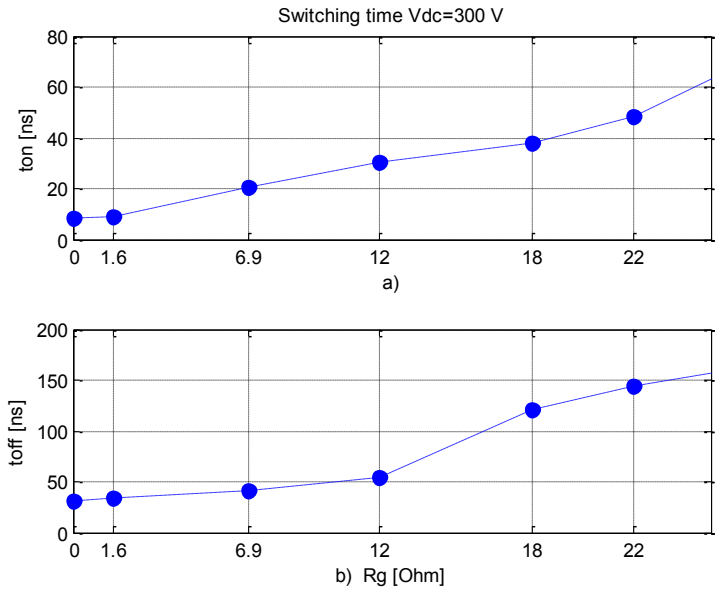

Figure 7-2 Switching times as a function of R_g, I_d=10A

7.2 Dynamic characterization

Before using a transistor in a real application the dynamic behavior of the device should thoroughly investigated. It is interesting to know how the switching waveforms changes for different operation conditions. In this section the switching losses and switching times are calculated for different currents, voltages and temperatures.

7.2.1 Switching characteristics of SiC JFET

Figure 7-3 shows how the switching energies changes for varying current. The total losses increase more than linear with increasing current. As the current increases, both the peak value of the dissipated power and the duration of the loss period are increased. When the current is increased beyond the snubbering capability of the parasitic snubber, the turn-off losses starts to elevate. Figure 7-4 shows the relationship between current and switching time. When the current increases also the current fall and rise times increase, thus the switching time increases.

Figure 7-5 and Figure 7-6 show the switching energies and the switching times dependency of the DC-voltage. One can see that the turn-on and turn-off times are almost independent of the voltage, while the energies show a dramatic increase for increasing voltage. The increase in the energies can be explained by three factors. First, the peak dissipation increases with increasing voltage. Secondly, a higher voltage gives longer rise and fall times for the drain-source voltage. The current peak at turn-on is a significant contribution to the turn-on losses. It was showed that the value of the peak is closely related to the applied voltage. This explains the large correlation between increased voltage and increased turn-on losses.

The dynamic behaviors for varying temperatures are presented in Figure 7-7 and Figure 7-8. Both the switching energies and times are almost independent of the junction temperature. The variations in the figures are so small that they could be created by random variation in the measuring equipment and by random oscillations. This is good news for the converter designer which can use the same parameters independently of operation temperature.

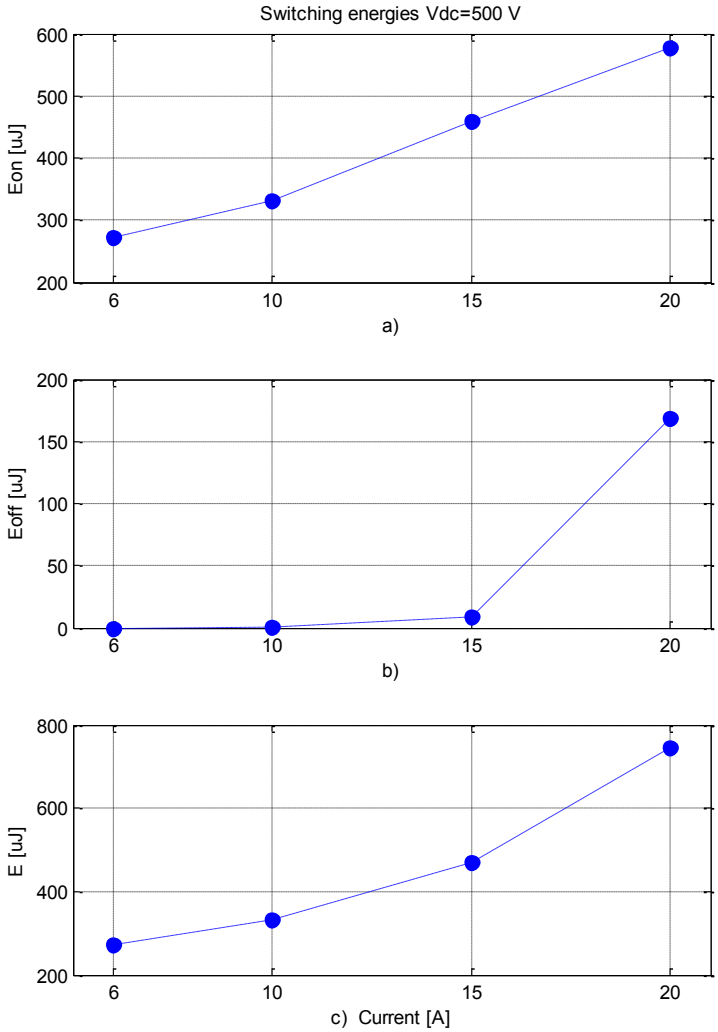

Figure 7-3 Switching energies as function of current for V_{dc}=500V

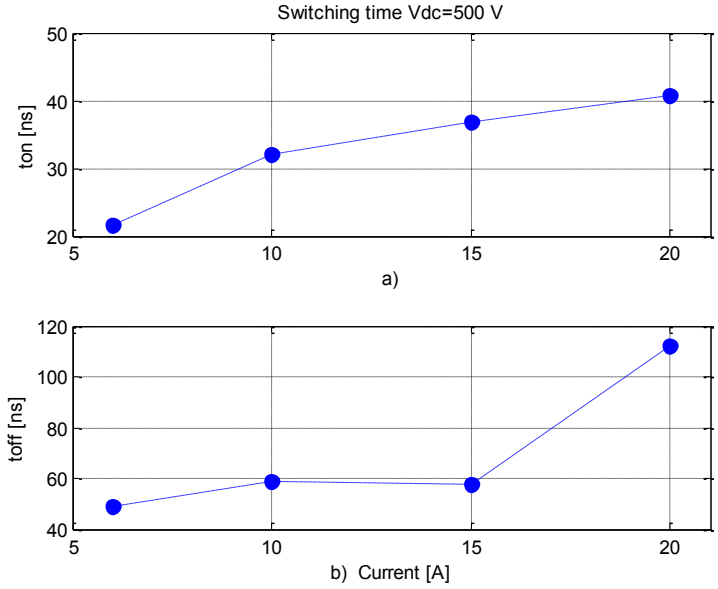

Figure 7-4 Switching times as function of current for V_{dc}=500V

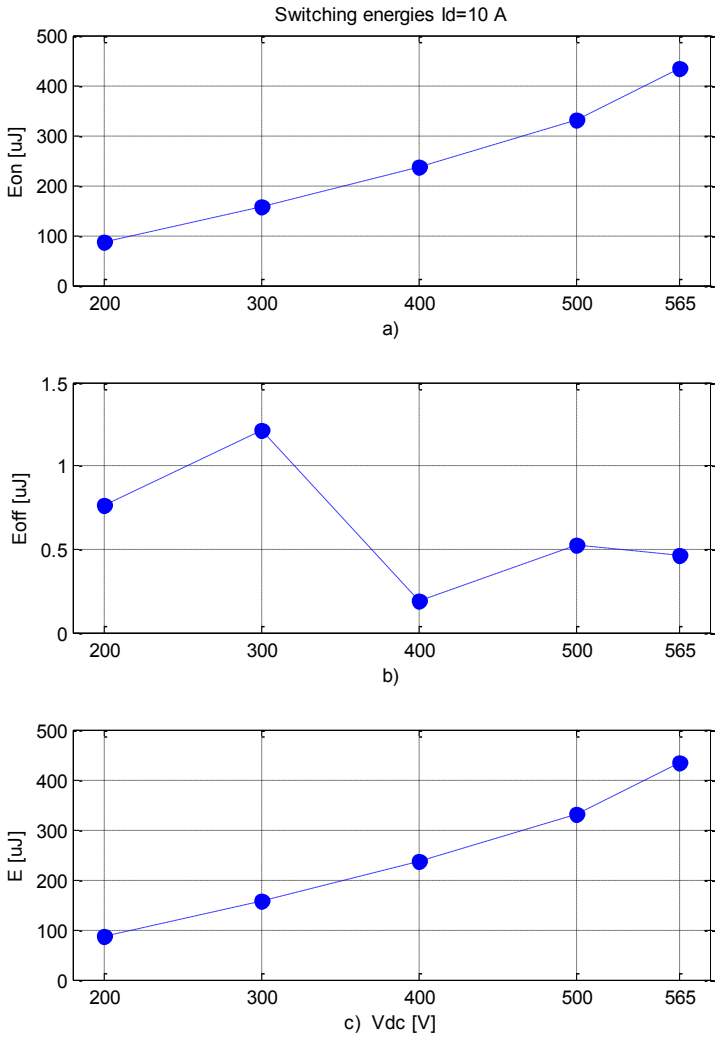

Figure 7-5 Switching energies as function of voltage for I_d=10A

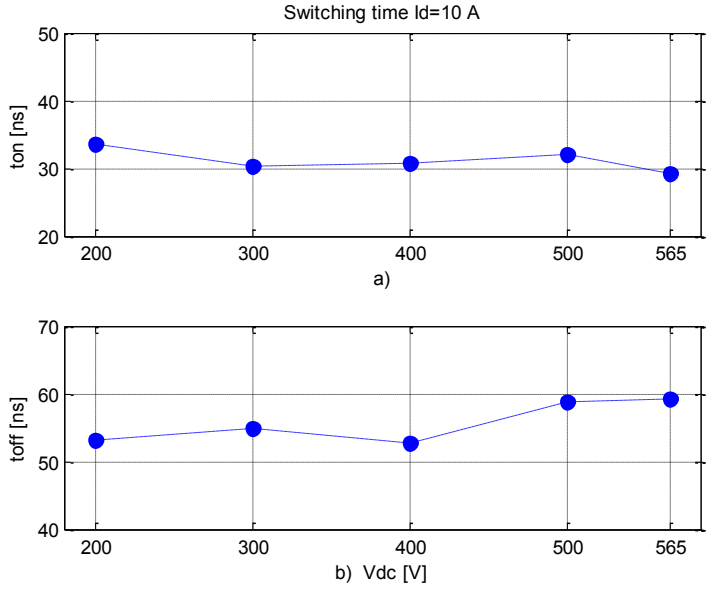

Figure 7-6 Switching times as function of voltage for I_d=10A

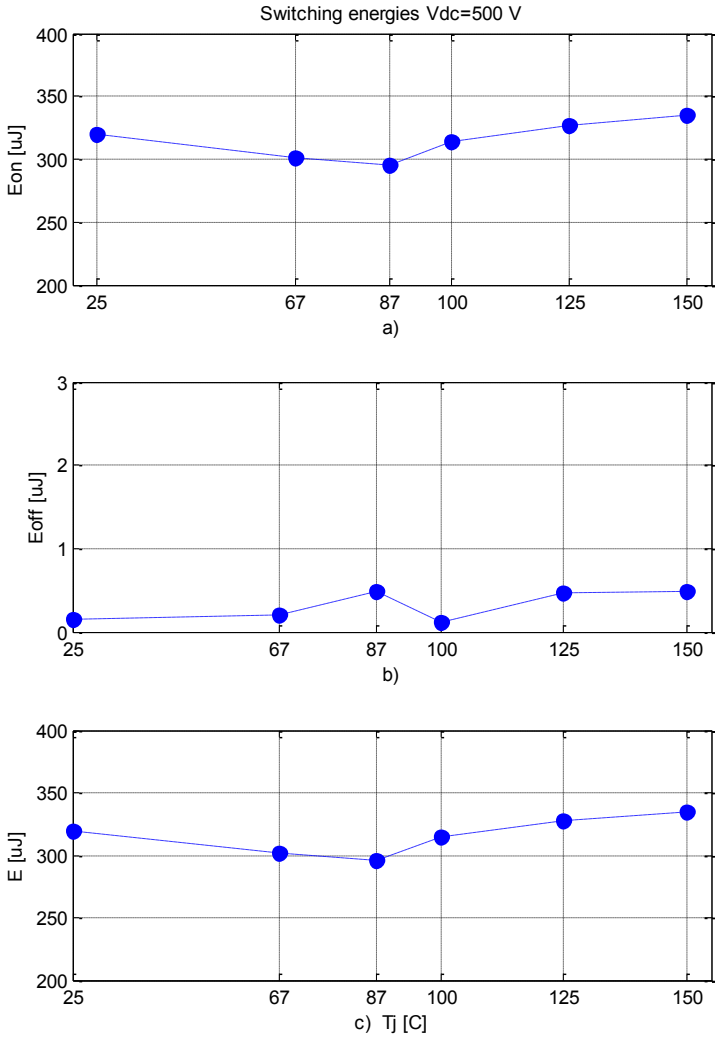

Figure 7-7 Switching energies as function of junction temperature for I_d=10A and V_{dc}=500V

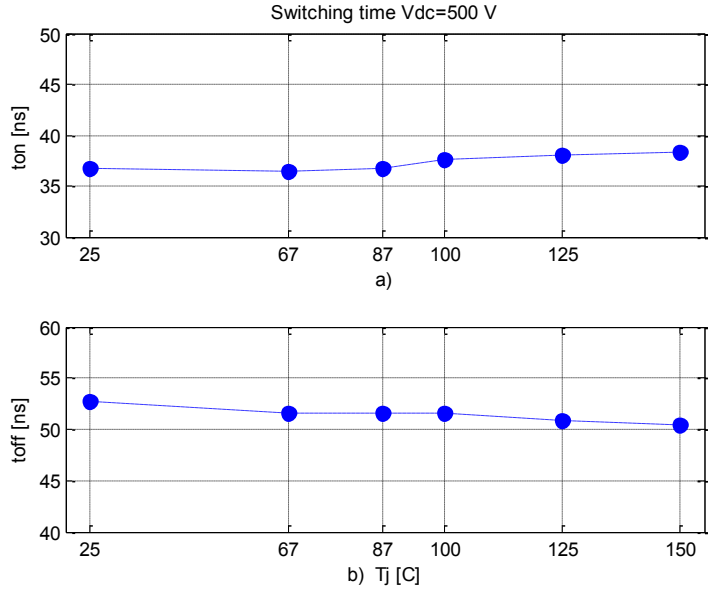

Figure 7-8 Switching times as function of junction temperature for I_d=10A and V_{dc}=500V

7.2.2 Switching characteristics of SiC BJT

The switching energies and the switching times for the BJT transistors are shown in Figure 7-9 – 7-12. As for the JFETs, both the energies and times increase with increasing. Generally, the turn-off losses contribute to a larger part of the total losses than for the JFETs.

Figure 7-11 and Figure 7-12 show how the energies and the times changes for varying temperatures. One can see that the dynamic properties are practically independent of the junction temperature.

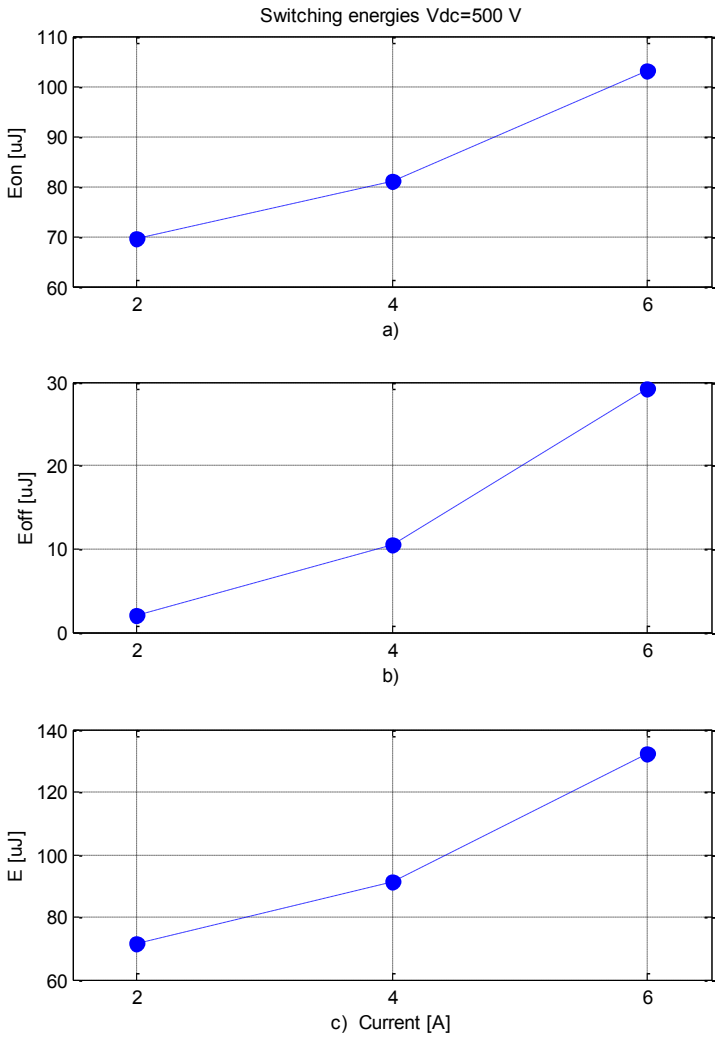

Figure 7-9 Switching energies as function of collector current for V_{dc}=500V

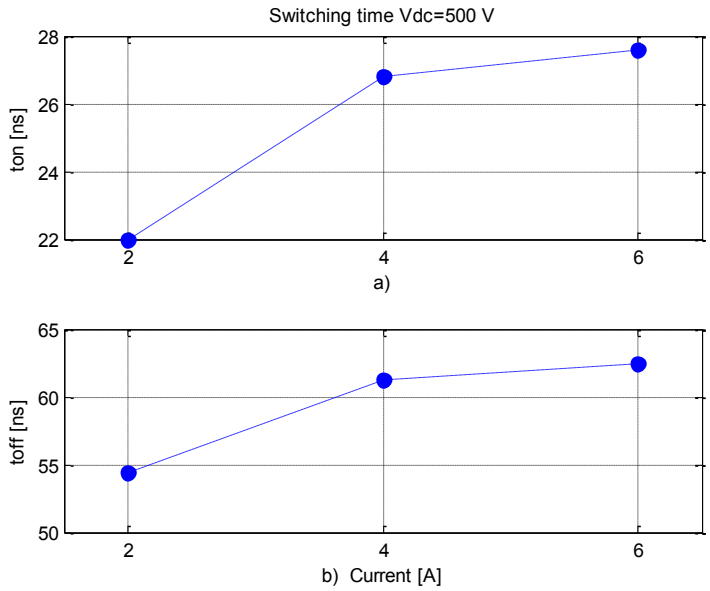

Figure 7-10 Switching times as function of collector current for V_{dc}=500V

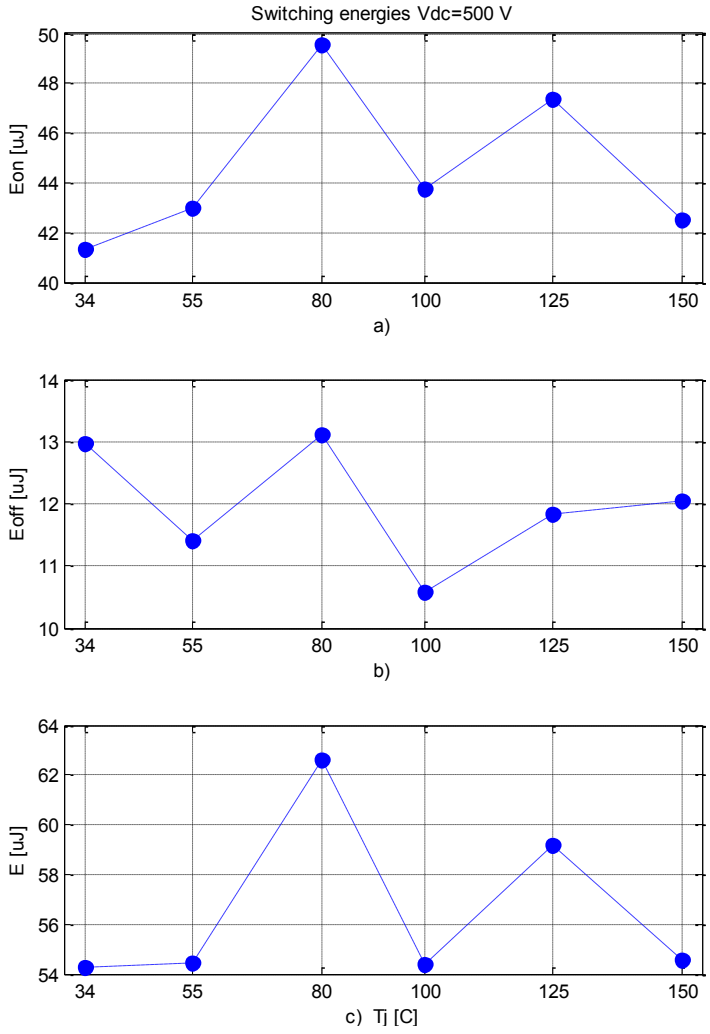

Figure 7-11 Switching energies as function of junction temperature for I_c=6A and V_{dc}=500V

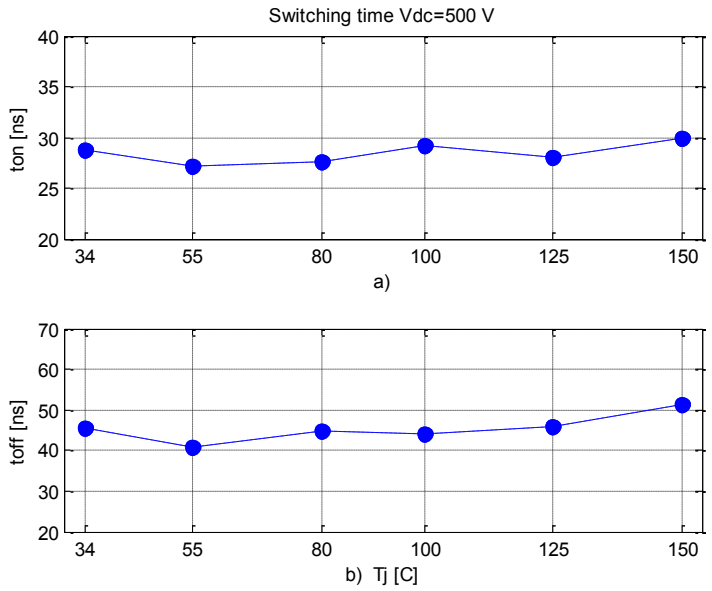

Figure 7-12 Switching times as function of junction temperature for I_c=6A and V_{dc}=500V

7.3 On-state losses

The on-state losses of a transistor are basically the product of the on-state voltage and the conducted current. The on-state voltage of a given devices is a function of the conducted current, the junction temperature and the gate-voltage/base-current. Measurements of the on-state voltage of the JFETs and the BJTs are presented below.

JFET

The on-state voltage of a minority carrier device is dominated by the resistance of the drift region. The drift region resistance is given by the structure of the device and of the specific resistance. The specific resistance in both Si and SiC has a large positive temperature coefficient, thus it is expected that on-state voltage will increase for increasing temperatures. From the data sheet of the device one can see that the on-state voltage is almost independent of the gate voltage as long as the current is below 10A and the gate voltage is kept above 2.5V. Unfortunately, as the temperature increases the gate current increases and the gate voltage drops. Figure 7-13 shows a plot of the gate voltage versus junction temperature. When the temperature passes 120 ˚C the gate voltage drops below 2.5V and the on-state voltage will start to increase at higher rate, especially for high currents.

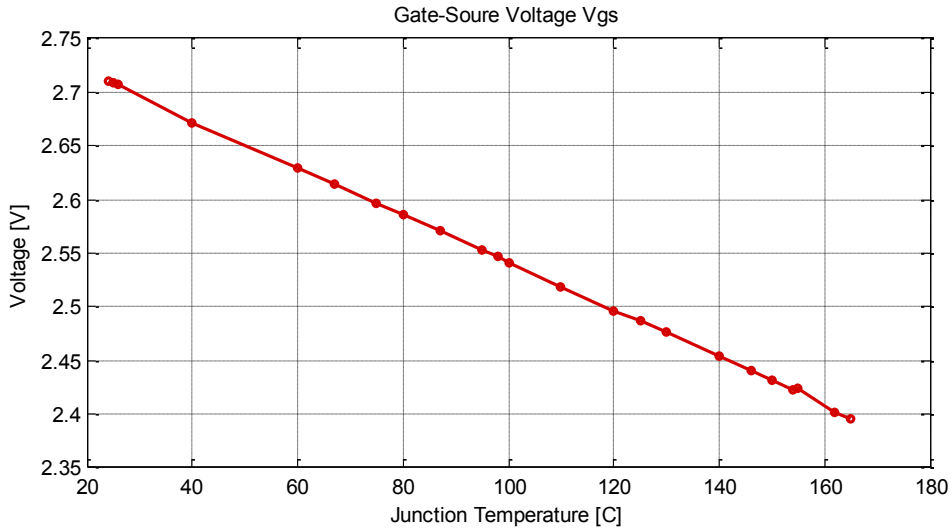

Figure 7-13 Gate voltage as a function of temperature

Figure 7-14 shows the on-resistance of the device for two different current levels. When the temperature increases from 25 ˚C to 120 ˚C the on-resistance is increased by 208%. An equation describing the relationship between the on-resistance and the junction temperature was generated by using the curve fitting tool, CFTOOL, in Matlab. The resistance temperature dependency had a very good match with a second degree polynomial.

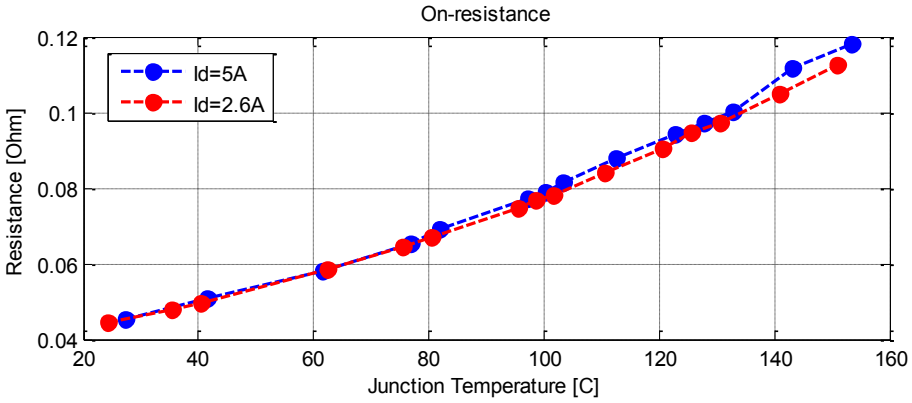

Figure 7-14 On-resistance as function of temperature

$$R_{I_d=5A}(T_j) = 0.03895 + 0.00018T_j + 2.208 \cdot 10^{-6}T_j^2\ [Ohm]$$
$$V_{ds,I_d=5A} = 0.19475 + 0.0009T_j + 1.104 \cdot 10^{-5}T_j^2\ [V] \quad (7.1)$$

Two I-V characteristics were generated, one at a case temperature of 24 ˚C and the other at 150 ˚C. The junction temperature becomes somehow higher than the casing temperature due to self heating of the device. For the 24 ˚C case the junction temp reaches 30 ˚C for a drain current of 10A, hence if the junction temperature is said to be 27 ˚C only a small error is made. Figure 7-15 shows the resulting characteristics.

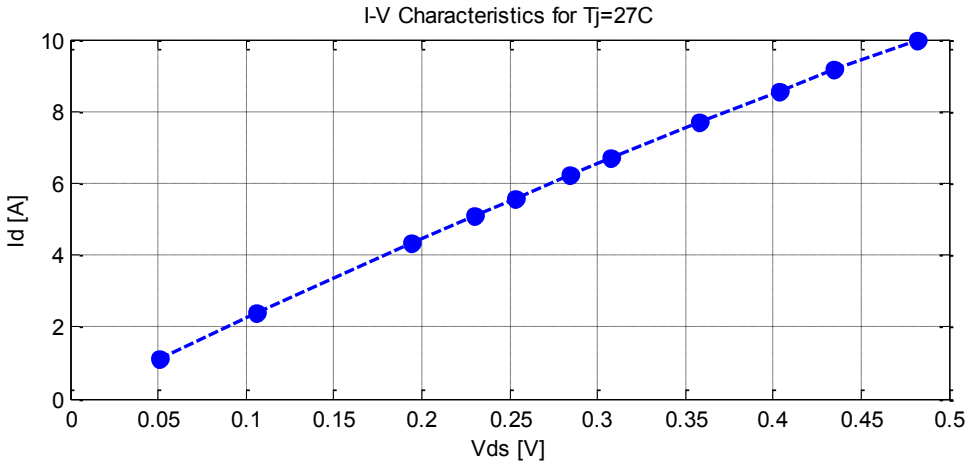

Figure 7-15 I-V Characteristics for T_j=27 ˚C and V_{GS}=2.7V

As the junction temperature increases the on-state voltage increase and the dissipated power increases. Hence, the variations in junction temperature become much larger when making I-V characteristics for higher temperatures and it is longer possible to assume constant junction temperature. The three dimensional plot shown in Figure 7-16 was created to present the measurements. At a junction temperature of approximately 195 ˚C thermal runaway occurred and the gate-source structure of the device got shorted internally. The explanation of the thermal runaway can be found by considering the gate voltage. As the temperature increases the gate current increases and gate voltage drops. A lower gate voltage gives a higher on-state voltage, thus the losses becomes higher. Finally, increased losses lead to increased junction temperature and the cycle continuous.

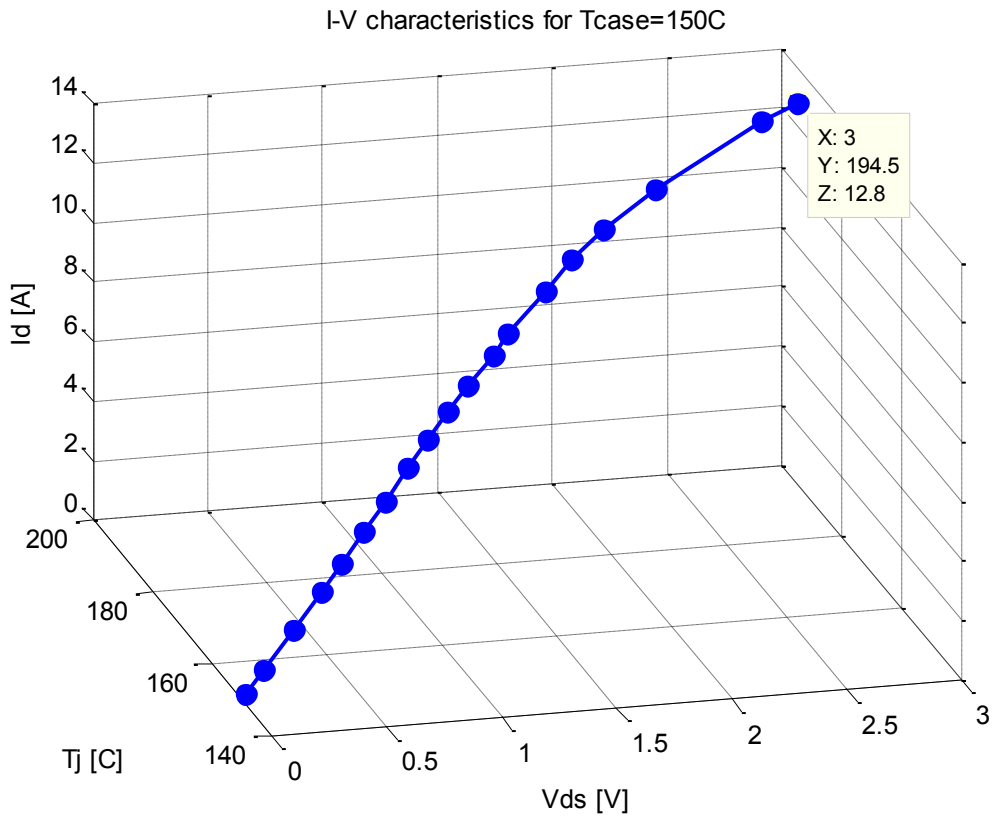

Figure 7-16 I-V characteristics for T_{case}=150 ˚C

BJT

A base current of 0.3A was applied for all conduction measurements. Bipolar transistors usually have a lower temperature dependency of the on-state voltage than unipolar devices due to the conductivity modulation. Figure 7-17 shows the on-state voltage for different temperatures. The temperature dependency can be modeled by a second order polynomial. Equation (7.2) was created with the CFTOOL in Matlab. The on-state voltage has a rather large positive thermal coefficient, but it is considerable smaller than the one for JFETs. The on-state voltage for I_c=4.05A increases with 144% when the junction temperature increases from 25 ˚C to 120 ˚C.

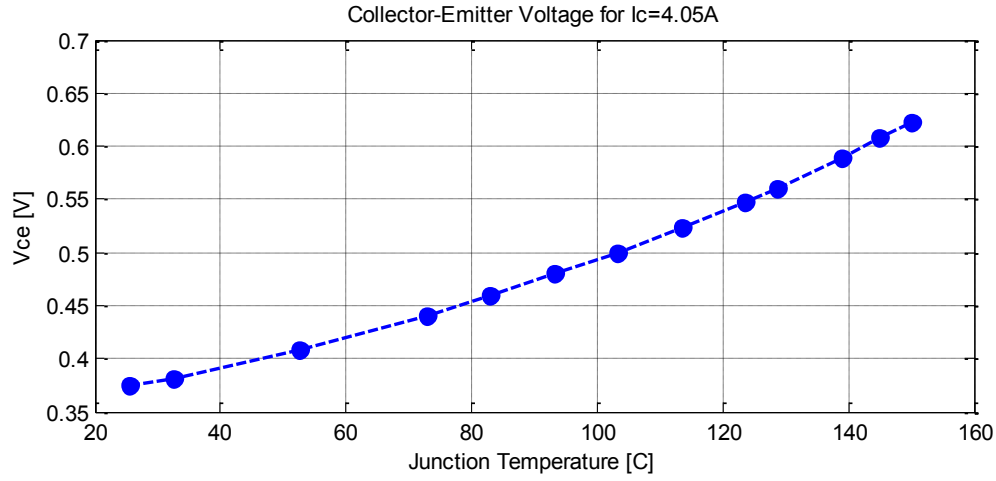

Figure 7-17 On-state voltage as function of temperature for I_c=4.05A

$$V_{ce,I_c=4.05A}(T_j) = 0.3533 + 0.0006372T_j + 7.637 \cdot 10^{-6}T_j^2[V] \qquad (7.2)$$

The BJTs have lower current rating than the JFETs and their on-state value is less dependent on the junction temperature as well. The self-heating will therefore be smaller. Three measuring series were performed to create a I-V characteristic of the device. During these series the junction temperature increases 10 ˚C above the heat sink temperature. By assuming T_j to be 5 degrees higher than T_{case} the maximum deviation from the real value is limited to 5 ˚C. The figure below shows the resulting I-V characteristics. Table 7-1 gives the threshold voltages of the device.

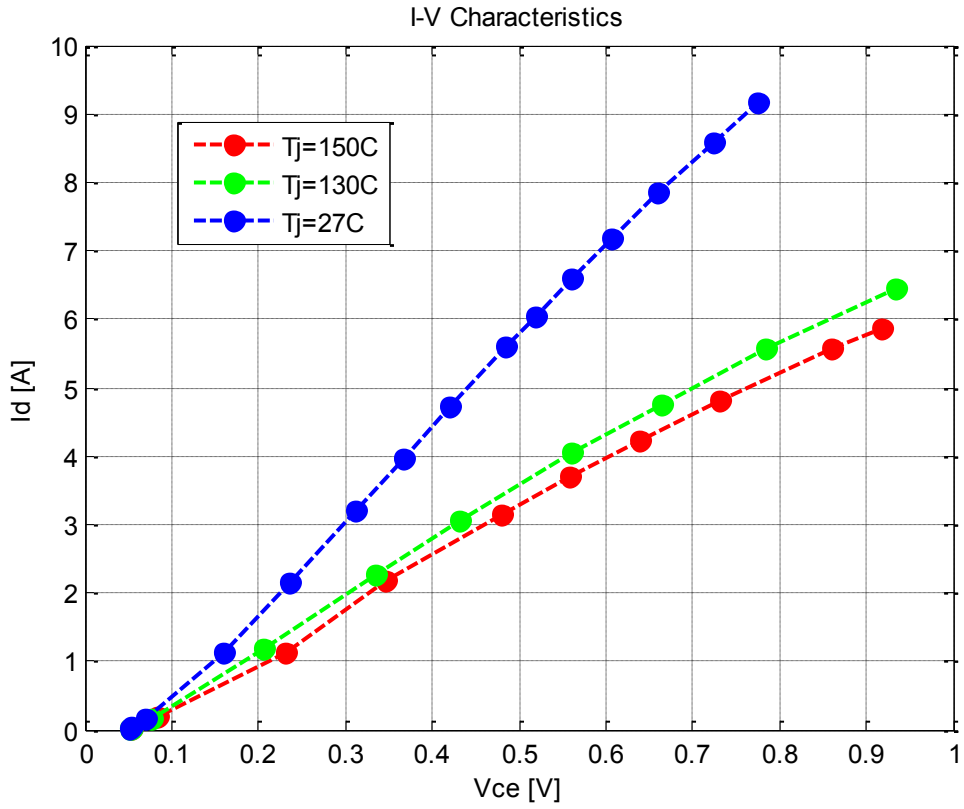

Figure 7-18 BJT I-V characteristics

BJT threshold voltage versus temperature	
T_j	V_{CE0}
22 ˚C	51.2mV
125 ˚C	52.0mV
145 ˚C	53.3mV

Table 7-1 BJT threshold voltage

7.4 Loss comparison and inverter efficiency

Based on the measurements presented in the previous sections the inverter efficiency can be calculated. For the calculations the junction temperature of the JFET and BJT are T_j=140 ˚C and T_j=150 ˚C, respectively. The temperatures were selected based on the availability of measurements.

The relevant parameters for the calculations are presented in the table below.

Parameters for loss calculations		
Parameters	**JFET**	**BJT**
T_j	140 ˚C	150 ˚C
$\hat{\imath}_1$	10A	6A
r_{CE}	0.1184Ω	0.1477Ω
V_{CE0}	0V	0.053V
E_{on}	332µJ	103µJ
E_{off}	5µJ	29µJ
$P_{average,drive}$	0.421W	2.68W
$P_{average,drive,theoretical}$	0.169W	0.483W
V_{dc}	500V	500V
Cos(ϕ)	0.95	0.95

Table 7-2 Parameters for calculations of inverter losses

Due to the uncertainties related to the current measurements of the high temperature testing of the BJTs it was decided to use the switching losses from the room temperature testing. However, the error by using the room temperature values should be minimal since the switching losses are almost independent of temperature. The switching losses for the JFET were obtained by linear interpolation between the points in Figure 7-7. The driving power, $P_{average,drive}$, includes the losses in the DC/DC converters supplying the drivers. $P_{average,drive,theoretical}$ is minimum theoretical power which is required for driving the devices. The freewheeling diode used for the calculations is the IDH15S120. Table 7-3 shows the results of the calculations.

Inverter parameters		
Losses and efficiency	**JFET**	**BJT**
Output power	3.563kW	2.138kW
Driving	2.53W	16.08W
Conduction	19.37W	9.42W
Switching	10.58W	4.71W
Total losses	32.48W	30.21W
Driver η	40.1%	18.0%
Inverter η	99.1%	98.6%

Table 7-3 Calculated inverter efficiencies

From the results one can see that driving losses of the BJTs are remarkable high compared to the switching and conduction losses.

7.5 Verification of the step down converter performance

To be sure that the converter performance is satisfactory it should tested at its boundary conditions. To check if the selected filter inductor is large enough to keep the converter in continuous conduction mode, the converter should be operated at its maximum input voltage with the minimum load. Figure 7-19 shows the operation under these conditions. The inductor current is the purple waveform; the ripple component of the output voltage is given by the turquoise waveform and the converter output voltage is yellow. This is the same for all the figures, unless other is stated. The current waveforms are measured with a LEM module. The oscilloscope did not have a gain which matched the sensitivity of the module, thus the waveforms should be multiplied with 6/5. One can see from the figure that the current is continuous. Hence, the inductor is large enough. The peak-to-peak ripple voltage is well below 1%, thus the requirements related to output voltage quality are fulfilled. Figure 7-20 shows that the converter is stable also for discontinuous conduction mode of operation.

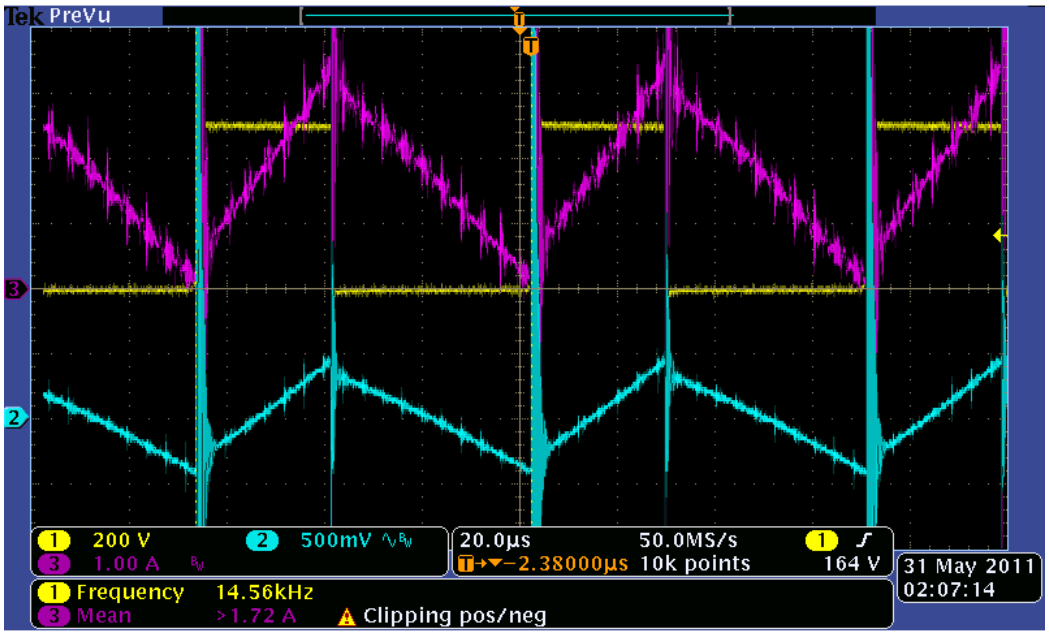

Figure 7-19 CCM boundary check V_{in}=500V R_o=97Ω

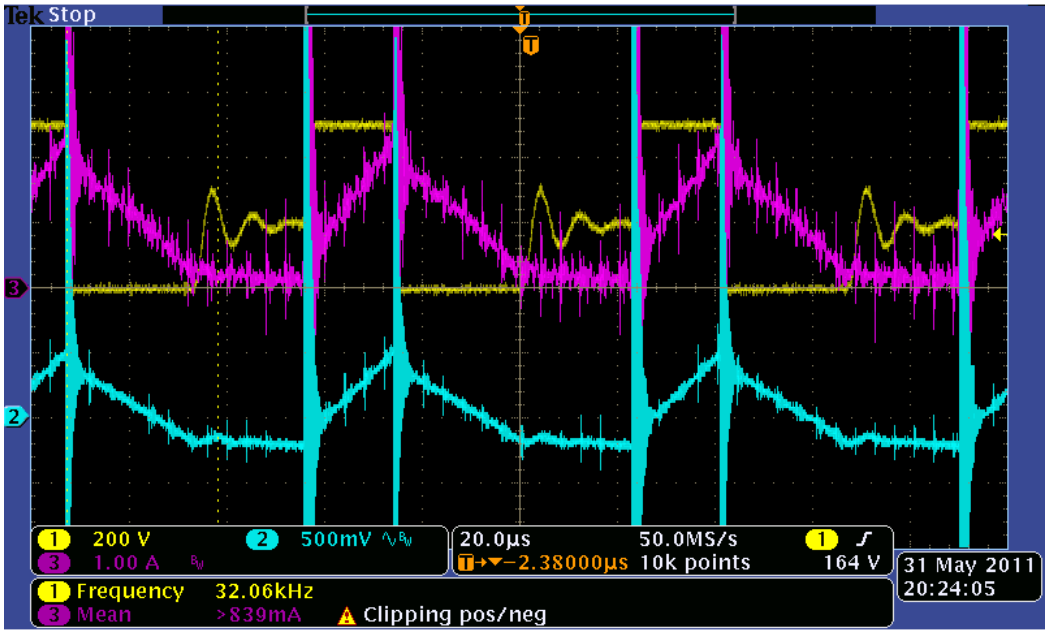

Figure 7-20 DCM V_{in}=500 R_o=217Ω

The most critical operation point from a stability point of view is at high loads and high duty cycles. The likelihood of having subharmonic oscillations gets higher as the duty cycle increases. Figure 7-21 shows that converter can operate stably when the input voltage is 250V and the load is 29.5Ω.

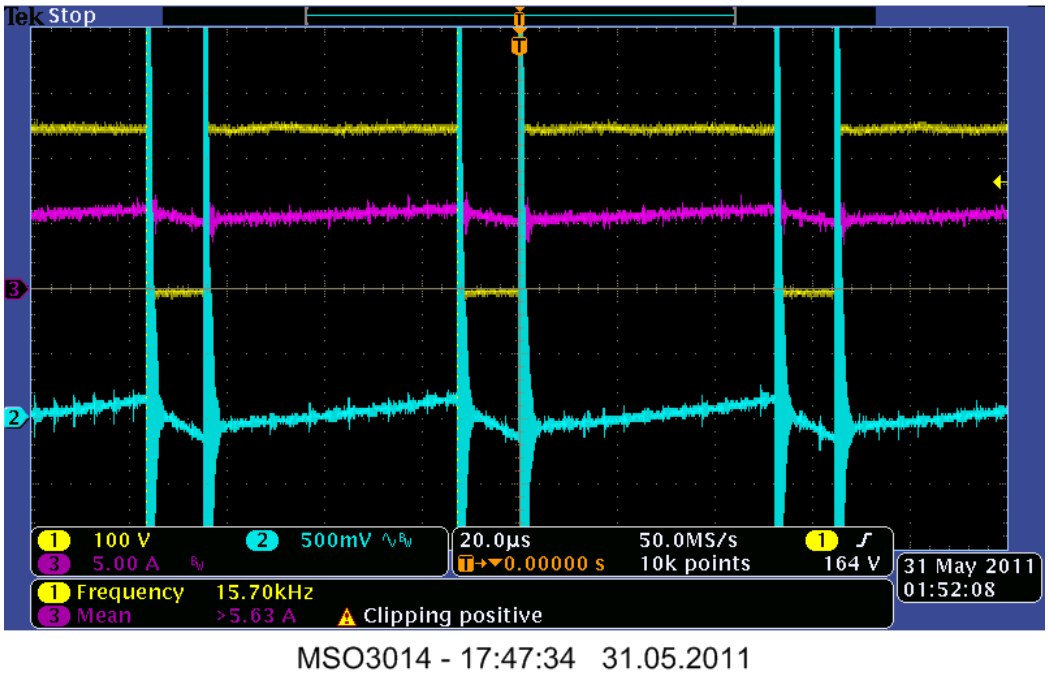

Figure 7-21 Stability check, V_{in}=250V R_o=29.5Ω

To test the dynamic performance of the converter, it was exposed to a step in the load, followed by a drop in the load some seconds later. Since the converter is most robust at low duty cycles it was decided to start the test with V_{in}=500V. The initial load was set to 678W and the load after the step was set to 1333W. Figure 7-22 shows the resulting waveforms. The converter oscillates for 800ms after the load step. During this period, the peak-to-peak value of the output voltage is increased to approximately 5V. This is acceptable for a short time period. There are no signs of oscillations when load is disconnected. Afterwards the test was repeated for an input voltage of 400V. This time the converter was not able to stabilize the current and the subharmonic oscillations were not damped. The results of the test can be found in appendix H2.

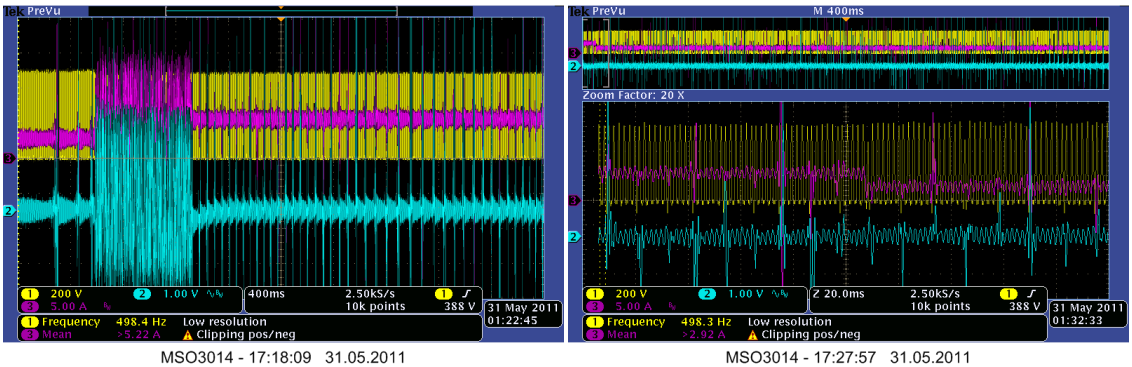

Figure 7-22 Step in load to the left and drop in load to the right, V_{in}=500V $R_0$0=59Ω $R_0$1=30Ω

Table 7-4 gives the peak-to-peak voltage ripple for different operation condition. The ripple is well below its limit for all conditions. The oscilloscope readings which the

table is based on can be found in appendix H1. The efficiency of the converter should also have been included, but it was not possible due to the measuring problems which are described earlier. Figure 7-23 shows the oscillations in the input current of the converter.

Vin	Vout	Rload	ΔVpp	$\Delta V/V_0$	Continuous
251.2V	199.6V	59Ω	0.3V	0.15%	Yes
351V	199.6V	59 Ω	0.66V	0.33%	Yes
401V	199.6V	59 Ω	0.74V	0.37%	Yes
450.4V	199.6V	59 Ω	0.85V	0.425%	Yes
501.8V	199.1V	29.5 Ω	0.9V	0.45%	Yes
500.9V	199.6V	59 Ω	0.9V	0.45%	Yes
500.4V	199.8V	97 Ω	0.82V	0.41%	Yes
501.6V	200V	217 Ω	0.69V	0.345%	No

Table 7-4 The table shows the measured peak-to-peak voltage ripple for different operation conditions

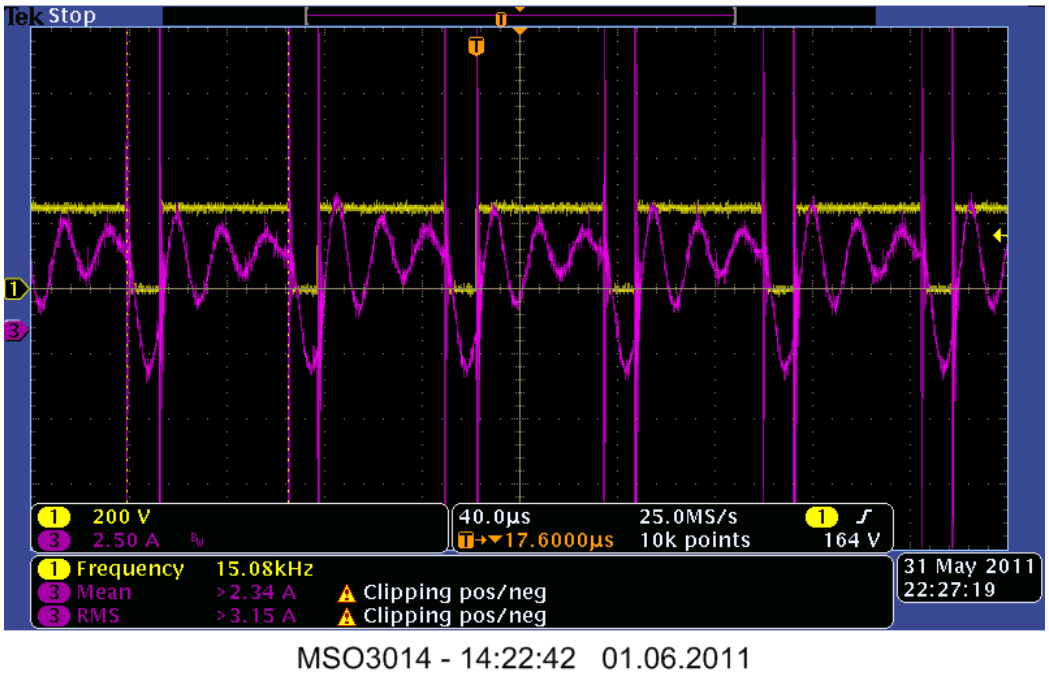

Figure 7-23 Converter input current V_{in}=250 R_o=59

7.6 General discussion and summary

Chapter 3 presented the theoretical potential of SiC transistors. The low intrinsic capacitances make them able to switch extremely fast. The fast switching makes the converters very sensitive to parasitic capacitance. Even small capacitances results in high current peaks at turn-on and soft switching at turn-off. Large Schottky diode capacitance results in voltage and current ringings, thus more EMI and switching energy

loss. Simulations confirmed this conclusion despite for the fact that the turn-off losses are reduced. Schottky diodes with low junction capacitance are recommended.

The tuning of the JFETs switching speed was performed by changing the external gate resistance. When changing the gate resistor also the conduction characteristics are affected. The optimal value from a switching point of view turned out to be somehow too high when considering the on-state voltage at high temperatures. The measurements showed that the gate voltage fell below 2.5V when the temperature reached 120 ˚C. This problem can be solved by modifying the SGDR600P1 driver board. The board has two separate internal gate resistors, one small for charging and discharging the capacitances at switching and one for supplying the gate voltage and current during the on-period. By only changing the switching resistor the switching speed can be reduced without increasing the on-state voltage at high temperatures.

The design of the BJT driver is very simple. The cost of the simple design is paid in forms of very low efficiency. The output voltage of the driver is 15V while the base-emitter forward voltage is around 3V. Hence, approximately 80% of the driver power is dissipated in the gate resistor. So instead of having a 1W power supply the driver requires at least 5W. A new two-stage DC-coupled driver similar to the one used for the JFET should therefore be designed. A further increase in the efficiency can be obtained by making an adaptive driver which changes the base current in proportion to the collector current.

The dynamic behavior of both the JFET and the BJT are almost independent of the temperature. Both switching times and switching energies are relatively constant. The changes are so small that they can be due to random oscillations and measuring uncertainty.

The on-state voltage of the devices shows a high positive thermal coefficient. This is as expected for the JFETs, but the BJTs have a higher temperature dependency than what is normal for bipolar devices. The BJT on-state voltage can be described by the following equation [9].

$$V_{CE(sat)} = V_{BE(on)} - V_{BC(sat)} + V_d + I_c(R_e + R_c) \qquad (7.3)$$

Where $V_{BE(on)}$ and $V_{BC(sat)}$ are the voltages across the forward biased B-E and C-B junctions, respectively. V_d is the voltage across the drift region and R_e and R_c are the ohmic resistance of the emitter and collector regions respectively. It was shown that the BJT threshold voltage, which is the difference between $V_{BE(on)}$ and $V_{BC(sat)}$, is almost independent of the temperature. Hence, the voltage increase is across the drift region and the ohmic regions. There were no signs of tail currents in the switching waveforms of the BJTs. This indicates that the carrier life-time of the device is very short. As a result the conductivity modulation becomes less dominant and the BJT behaves almost as a unipolar device. This explains the high temperature dependency of the on-state voltage.

There are some uncertainties related to the current measurements. To measure the current waveforms accurately have proved to be one of the largest challenges of this work. It is difficult to find measuring equipment which has sufficient bandwidth and at same time is small enough to be connected in the circuit without introducing to high stray inductance. The bandwidth of the Athena Rogowski should have been 2-3 times higher to be sure that the measured waveforms are correct. The calculated losses should therefore only be used as an approximation. To find the exact losses a calorimetric

measurement should be performed. The fact that the time delay of the Rogowski changed at the end of the testing, introduces extra uncertainty in the measurements of the high temperature switching. If the switching energies of the BJT from Figure 7-9 and Figure 7-11 are compared, one can see that energies in Figure 7-9 are two times larger. It is most likely that Figure 7-11 is incorrect, but the trends shown in figure should still be valid.

The transistors tested in this work do not meet the requirements for high temperature operation, where the ambient temperature is higher than 150 ˚C. The limitations are mainly related to the packaging technology. The JFETs showed signs of degradation during the high temperature testing when the thermal runaway occurred. From the tests performed in this work it can look like the BJT is better suited for high temperature operation. However, the transistors are suited for operation at intermediate temperatures levels where T_{amb}<150 ˚C. The calculations based on the measured conduction and switching losses showed promising results. The calculated efficiency of the JFET-based inverter, when operating at T_j=140 ˚C and delivering 3.56kW, was 99.1%. For the BJT the efficiency was calculated to 98.6%, when operating at T_j=150 ˚C and supplying 2.14kW. The main reason for the lower efficiency of the BJT is the high driving losses. If the efficiency of the BJT driver had been increased to 40%, which is equal to the efficiency of the JFET driver, then the total converter efficiency will be 99%. However, the calculated efficiencies should only be used as an approximation. There are inaccuracies in both the switching losses and in the mathematical model used for calculating the losses. To find the real efficiency, a complete three phase inverter should be built and the input and output power should be measured.

The stationary operation of the buck converter is satisfactory, and all the requirements are fulfilled. However, its dynamic behavior shows subharmonic oscillations that should be improved. The response of the converter is quite fast and there are almost no overshoot in the output voltage at turn-on. Reducing the crossover frequency and increasing the added slope compensation can improve the converter stability. The performance of the converter with the suggested improvements could be tested by simulation. If the SBC still is unstable a new controller which accounts for the differences between the Buck and the SBC should be designed.

The most important property of a converter for down-hole drilling is the ability to operate at high temperatures. However, as the ambient temperature increases the maximum allowed internal device heating dissipation decreases. When pushing the limits it is therefore important to use transistor with minimal losses. SiC transistors in general have both the desired properties, and thus should be ideal for down-hole applications. TranSiC has recently released the first SiC transistor with high temperature packaging. With this new package, the BJT can operate at junction temperatures above 250 ˚C. This will probably be sufficient to meet the requirements of the down-hole drilling converter described in the introduction of the thesis.

8 Conclusion and Scope of Further Work

8.1 Conclusion

This report presents the superior properties of SiC transistors. Two commercial available enhancement mode SiC transistors, BJTs from TranSiC and JFETs from Semisouth, have been investigated in detail. To fully utilize the properties of SiC the converter designer must pay extra attention to the PCB layout and to the selection of components. For best device performance, all parasitic components should be kept at minimum. This prevents excessive oscillations and ringings in voltage and current waveforms. Extra attention should be paid to the design of gate driver circuits to ensure full utilization of the SiC devices. Driver circuits with improved dynamic performance such as DC coupled two-stage drivers are highly recommended to drive the two aforementioned devices. This driver circuit is able to charge and sink a gate/base current with considerably fast speed. It is also capable of maintaining a gate/base current during intended on-state period. With bipolar output voltage of this driver, higher immunity at gate/base could be achieved. This is crucial for SiC devices as threshold voltage tends to be relatively low e.g. SiC JFET. In addition, a clamping capacitor should also be placed between the gate and source of the JFET to stabilize the gate voltage.

Two half-bridge converters were successfully designed and implemented. Measurements on the converters showed switching times in the range of some few tens of nano seconds for both the BJTs and the JFETs. The dynamic behavior of the transistors is almost independent of temperature. Based on the measured switching and conduction losses the efficiency of a three phase inverter was calculated, where driving power and the efficiency of the isolated power supplies were included in the calculations. The calculated efficiency of the JFET based inverter, when operating at T_j=140 ˚C and delivering 3.56kW, was 99.1%. For the BJT the efficiency was calculated to 98.6%, when operating at T_j=150 ˚C and supplying 2.14kW. The driving losses in the BJT inverter contribute to over 50% of the total losses. This is unacceptably high; therefore a new optimized driver should be designed.

The junction capacitance of the Schottky diodes introduces a high current peak at turn-on. It also acts as turn-off snubber during turn-off transition. Hence, the capacitance moves the switching losses from the turn-off to the turn-on. By simulations it was shown that the total losses increase for increasing junction capacitances.

An analog controller, for operating the half-bridge as a step down converter, was designed. The step down converter showed an excellent performance in stationary operation. The maximum output voltage ripple was below 0.5% for all operating condition, with the selected filter. Simulations showed that voltage overshoot at start-up is less than 1% of the output voltage. The dynamic performance of the converter exhibit subharmonic oscillations especially at high duty cycles.

8.2 Scope of further work

Throughout this work the difficulties related to measurements of steep current waveforms have been experienced. To measure the switching losses accurately a calometric loss measurement should be performed. Both the tested transistors have a

maximum operating junction temperature of 175 ˚C mostly due packaging limitations. The high temperature and high current version of the BJT should therefore be tested to find out if it is suitable for use in high temperature motor drives.

The next step in designing a converter for high temperatures is to build a gate driver which can operate at elevated temperatures. The gate driver should be based on the high temperature ICs and small signal transistors from [35] which can operate at temperatures up to 225 ˚C. Finally, a three phase inverter with all high temperature components should be built and tested.

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Appendixes

A Matlab codes

A1 Code for calculating inverter losses

```
%Loss calculations
%---------------------------

%Input parameters
%---------------------------
Udc=600;              %DC-link voltage [V]
i1=20;                %Amplitude of sinusoidal output current [A]
M=1;                  %Modulation index
phi=0.318;            %Phase [rad]
fs=15e3;              %Switxhing frequency [Hz]
Pdrive_av=19e-3;      %Average driving power [W]
%Transistor parameters
Vce0=0.85;
rce=54.4e-3;
Eon=1.73e-3;
Eoff_T=1.86e-3;
%Diode parameters
Vf0=0.905;
rf=45.2e-3;
Eoff_D=32.4e-6;

%Calculations
%---------------------------
U1=M*Udc/2;           %Peak phase voltage [V]
Pfw_T=0.5*(Vce0/pi*i1+rce/4*i1^2)+M*cos(phi)*(Vce0/8*i1+rce/(3*pi)*i1^
2);
Pfw_D=0.5*(Vf0/pi*i1+rf/4*i1^2)-M*cos(phi)*(Vf0/8*i1+rf/(3*pi)*i1^2);
Psv=fs/pi*(Eon+Eoff_T+Eoff_D)
Ploss=6*(Psv+Pfw_T+Pfw_D+Pdrive_av)
Pout=3*U1*i1/2*cos(phi)
Pin=Pout+Ploss
n=Pout./Pin
```

A2 Code for calculating switching energies

```
A=importdata('Tap.xlsx'); %Title of import file

% 10A-------------------------------------
%Turn on with Id=10A
t10on1=A.data.i10on(1,5);
t10on2=A.data.i10on(2,5);
samp10on=A.data.i10on(3,5); %Sampling time
vds10on=A.data.i10on(t10on1:t10on2,3);
id10on=A.data.i10on(t10on1:t10on2,4);
p10on=vds10on.*id10on;

E10on=samp10on*trapz(p10on)
```

```
%Turn off with Id=10A
t10off1=A.data.i10off(1,5);
t10off2=A.data.i10off(2,5);
samp10off=A.data.i10off(3,5); %Sampling time
vds10off=A.data.i10off(t10off1:t10off2,3);
id10off=A.data.i10off(t10off1:t10off2,4);
p10off=vds10off.*id10off;

E10off=samp10off*trapz(p10off)

E10=E10on+E10off
```

B Estimated data sheet values

SJEP120R063	**T=25 ˚C**	**T=100 ˚C**
r_{DS}	41.9 mΩ	102.9 mΩ
E_{on}	132.5 µJ	153.3 µJ
E_{off}	189.4 µJ	203.3 µJ
$P_{average,drive}$	54 mW	166 mW

Table B-1 Parameters for SJEP120R063

CMF20120D	**T=25 ˚C**	**T=100 ˚C**
r_{DS}	80 mΩ	85.7 mΩ
E_{on}	397 µJ	330 µJ
E_{off}	240 µJ	242 µJ
$P_{average,drive}$	30 mW	30 mW

Table B-2 Parameters for CMF20120D

IDH15S120	**T=25 ˚C**	**T=100 ˚C**
R_F	45.2 mΩ	90.5 mΩ
V_{F0}	0.905 V	0.833 V
E_{off}	32.4 µJ	32.4 µJ

Table B-3 Parameters for IDH15S120

BT1220AC	**T=25 ˚C**	**T=100 ˚C**
r_{CE}	21 mΩ	26 mΩ
V_{CE0}	0.08 V	0.09 V
E_{on}	229 µJ	229 µJ
E_{off}	110 µJ	110 µJ
$P_{average,drive}$	1.131 W	1.131 W

Table B-4 Parameters for BT1220AC

IKW15T120	**T=25 ˚C**	**T=100 ˚C**
r_{CE}	54.4 mΩ	72 mΩ
V_{CE0}	0.85 V	0.8 V
E_{on}	1.73 mJ	2.32 mJ
E_{off}	1.86 mJ	2.40 mJ
$P_{average,drive}$	19 mW	19 mW

Table B-5 Parameters for IKW15T120

C PCB Design Rules

C1 Electrical clearing

To avoid flashover between trace on the PCB there has to be some clearing between them. The electrical clearing is calculated in accordance with the IPC-2221 standard [59]. The board which is used is a two sided board with 70 µm of copper. This means that all traces are external. The conductors will not be coated and they will be used in an altitude between sea level and 3050 meter above. Thus the clearing class A6 has to be used when the spacing between the trace is calculated. From Table C-1 we get the following expression for the clearing distance, d_c:

$$d_c = (V_{max} - 500)[V]0{,}005\left[\frac{mm}{V}\right] + 2{,}5[mm] \qquad \text{(C.1)}$$

Where V_{max} is the maximum voltage that can appear between two traces. The value of V_{max} is the sum of the DC-link voltage and the induced overvoltage due to switching. The DC-link voltage will never be higher than 700V. It was decided to dimension for 1000, which gives a minimum clearing of 3mm. The reason for selecting a relative large clearing distance is to prevent flashover due to creepage currents. Dust and pollutions on the PCB decreases the creepage resistance.

Voltage Between Conductors (DC or AC Peaks)	Minimum Spacing						
	Bare Board				Assembly		
	B1	B2	B3	B4	A5	A6	A7
0-15	0.05 mm	0.1 mm	0.1 mm	0.05 mm	0.13 mm	0.13 mm	0.13 mm
16-30	0.05 mm	0.1 mm	0.1 mm	0.05 mm	0.13 mm	0.25 mm	0.13 mm
31-50	0.1 mm	0.6 mm	0.6 mm	0.13 mm	0.13 mm	0.4 mm	0.13 mm
51-100	0.1 mm	0.6 mm	1.5 mm	0.13 mm	0.13 mm	0.5 mm	0.13 mm
101-150	0.2 mm	0.6 mm	3.2 mm	0.4 mm	0.4 mm	0.8 mm	0.4 mm
151-170	0.2 mm	1.25 mm	3.2 mm	0.4 mm	0.4 mm	0.8 mm	0.4 mm
171-250	0.2 mm	1.25 mm	6.4 mm	0.4 mm	0.4 mm	0.8 mm	0.4 mm
251-300	0.2 mm	1.25 mm	12.5 mm	0.4 mm	0.4 mm	0.8 mm	0.8 mm
301-500	0.25 mm	2.5 mm	12.5 mm	0.8 mm	0.8 mm	1.5 mm	0.8 mm
> 500 See para. 6.3 for calc.	0.0025 mm /volt	0.005 mm /volt	0.025 mm /volt	0.00305 mm /volt	0.00305 mm /volt	0.00305 mm /volt	0.00305 mm /volt

B1 - Internal Conductors
B2 - External Conductors, uncoated, sea level to 3050 m
B3 - External Conductors, uncoated, over 3050 m
B4 - External Conductors, with permanent polymer coating (any elevation)
A5 - External Conductors, with conformal coating over assembly (any elevation)
A6 - External Component lead/termination, uncoated
A7 - External Component lead termination, with conformal coating (any elevation)

Table C-1 Minimum spacing between traces, IPC 2221 standad

C2 Trace width and skin depth

a) Skin depth

The skin depth is a measurement of the field penetration in a conductor. When working with high frequencies it is important to take the skin depth in to account when dimensioning conductors. The skin depth is given by the following equation [60]:

$$\delta = \frac{1}{\sqrt{\pi f \mu \sigma}} \qquad \text{(C.2)}$$

f is frequency of the applied voltage, μ is the permeability of the material and σ is the electrical conductivity. The skin dept will decease with one over the square root of the frequency. For copper the permeability is equal to $4\pi x10^{-7}$ (H/m) while the conductivity is $5{,}8x10^{7}$ $(\Omega\ m)^{-1}$. This gives a skin dept of 0.3 mm at 50 kHz.

b) Trace width

The current carrying capacity (CCC) of a PCB trace is defined as the maximum current that can be applied before the maximum allowed temperature rise in the trace is reached. The IPC 2221 standard is used to calculate the required trace width. Figure C-1 shows the relation between CCC, temperature rise and cross section are.

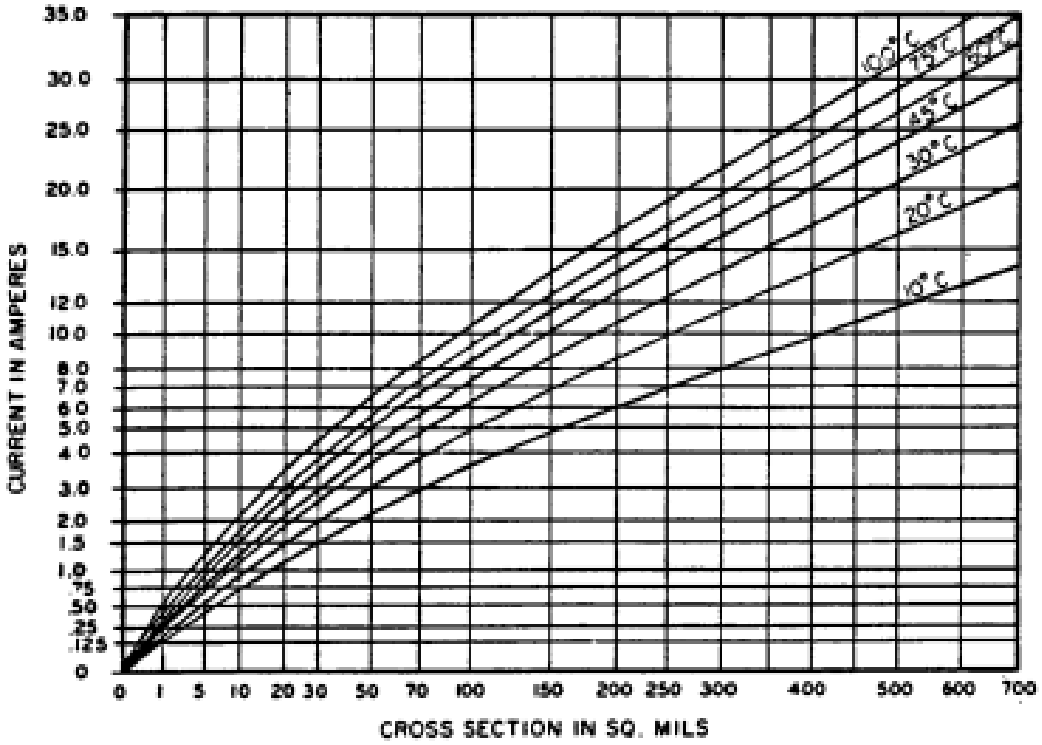

Figure C-1 Relationship between current magnitude and cross section [59]

The thickness of the cupper trace on the selected board is 70 μm and the load current is about 10 A. Since the thickness of the trace is much smaller than the skin dept at 15kHz the whole trace cross section can be utilized. The allowed temperature rise is set to 20 ˚C. From the figure we get a cross section area of approximately 250 square mils which is equal to 0,161 mm^2. This gives a trace width of 2,30mm. The resulting current density is 62.1 (A/mm^2). It should be mentioned that the IPC 2221 standard is conservative and inaccurate. They are based on measurements done in the 50s. One of the drawbacks is that the temperature rise is independently related to the cross-section area of the trace and hence, the varying convection effect due to different trace surface is neglected [61].

The traces of a PCB can be made in different ways e.g. etching and milling. For this project it was decided to use etching. When the PCB is delivered from the manufacturer it is covered by a protection film which is resistant to acids. The traces on the board are

made by removing the protection film around the traces and then submerge the board into an acid. The acid dissolves the unprotected copper. During this etching process the acid will etch about the same length in the vertical and the horizontal direction at the edge of the traces. Thus, when calculating the required trace width this should be taken into considerations, especially when the copper layer is thick. For a 70µm board there should be added approximately 2·70µm=0,14mm to the trace width to be safe.

This gives a trace width, for the load current carrying traces, of 2.44 mm. It is important to distinguish between the different kinds of traces. The traces for signals and gate driver supplies can be much thinner than the power traces. Since some of the components on the PCB are going to be heated when the converter is tested, it was decided to choose an even more conservative trace width. The PCB was built with a minimum trace width of 3 mm.

D Schematics and Board Layouts

D1 Gate driver and DC/DC converter connections for JFET half-bridge

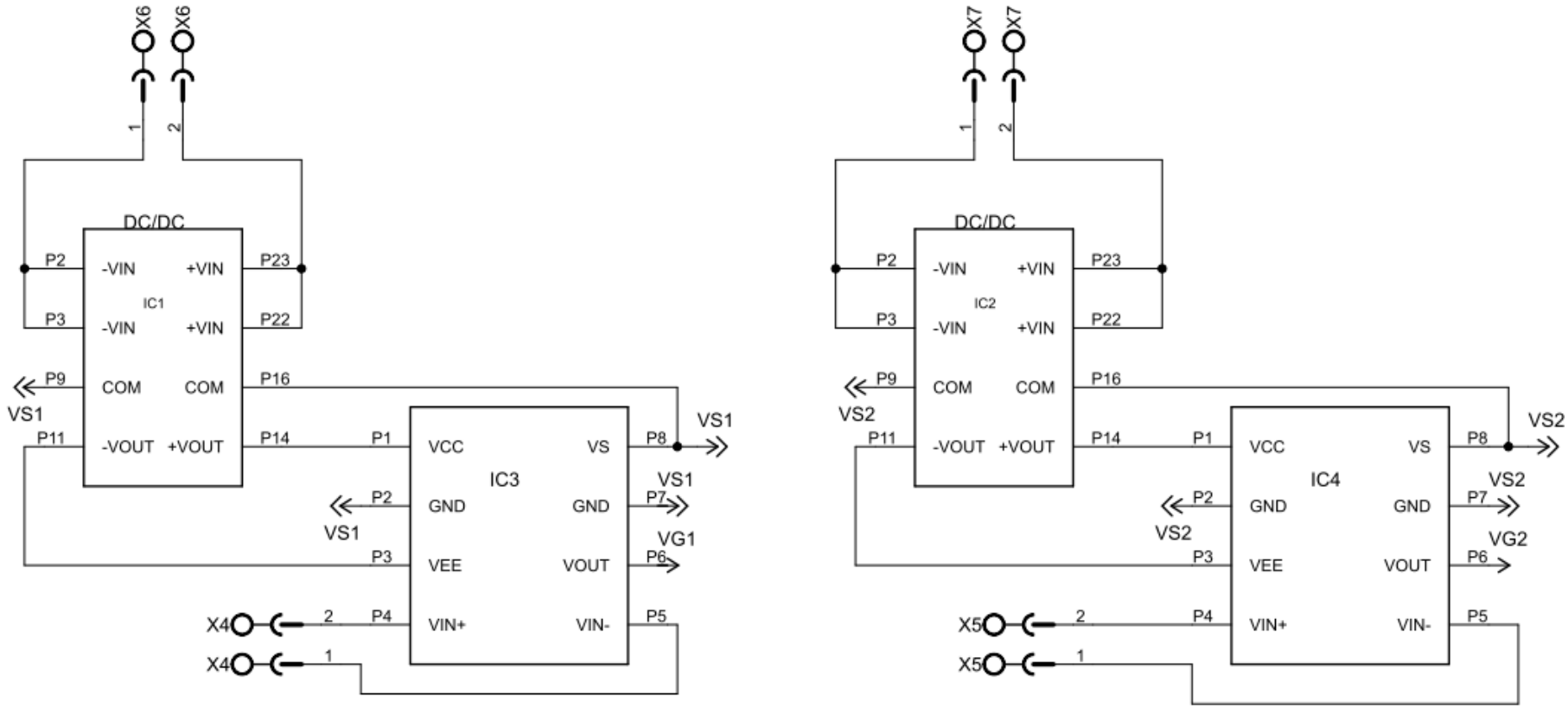

Figure D-1 Gate driver and DC/DC converter connections for JFET half bridge

D2 PCB layout for the JFET half-bridge

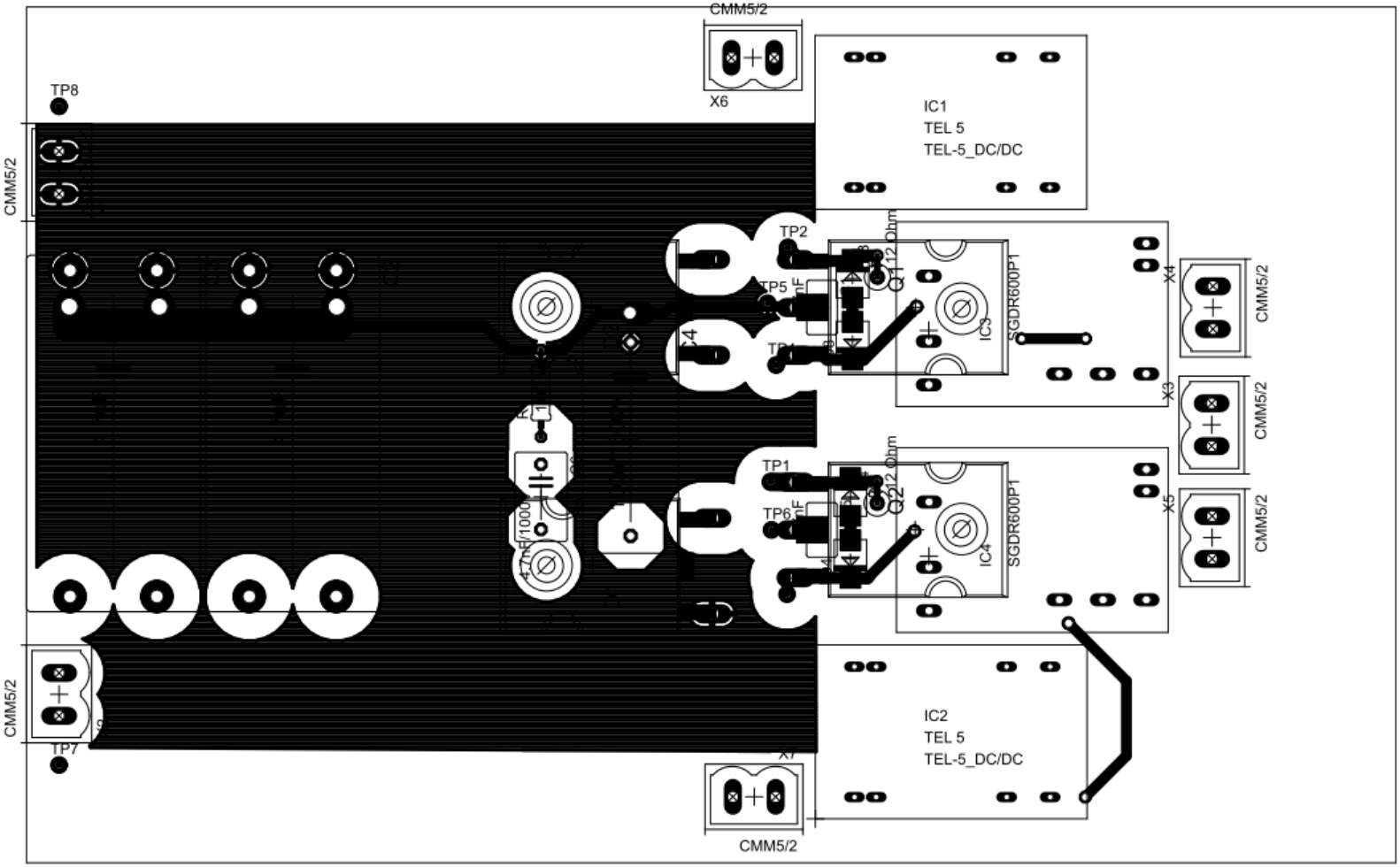

Figure D-2 JFET PCB top layer

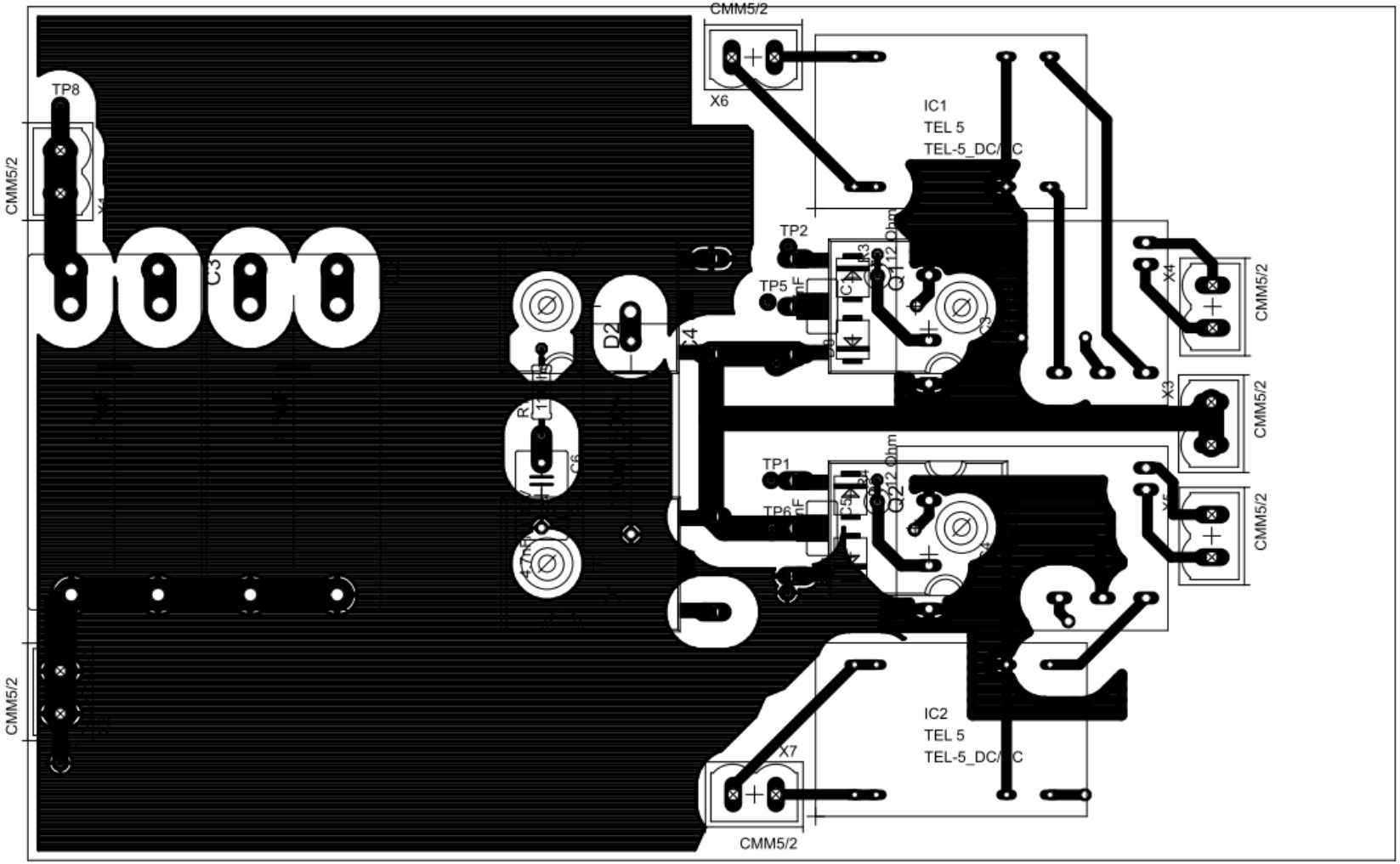

Figure D-3 JFET PCB bottom layer

D3 PCB layout for the BJT half-bridge

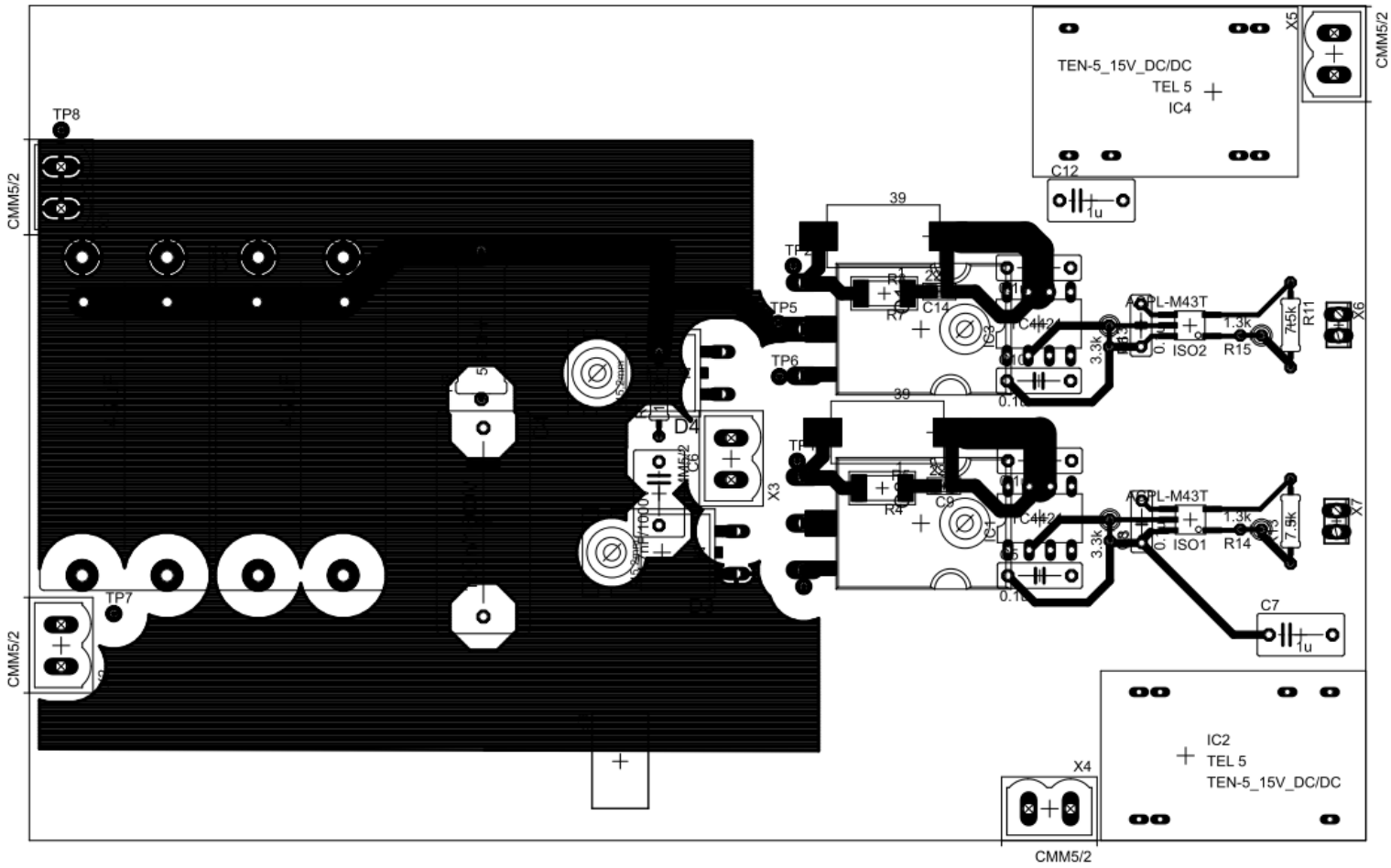

Figure D-4 BJT PCB top layer

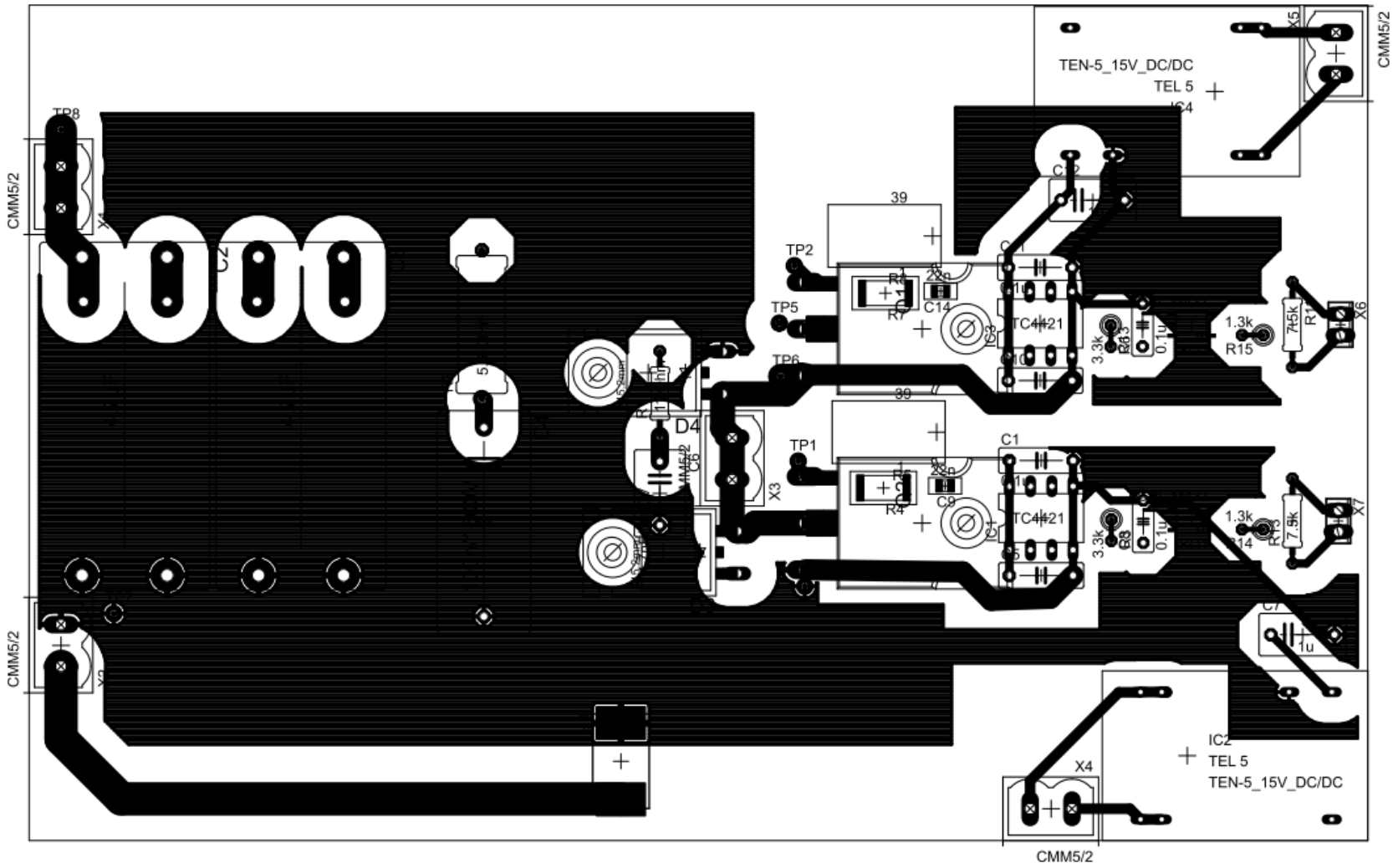

Figure D-5 BJT PCB bottom layer

D4 Control card PCB layout

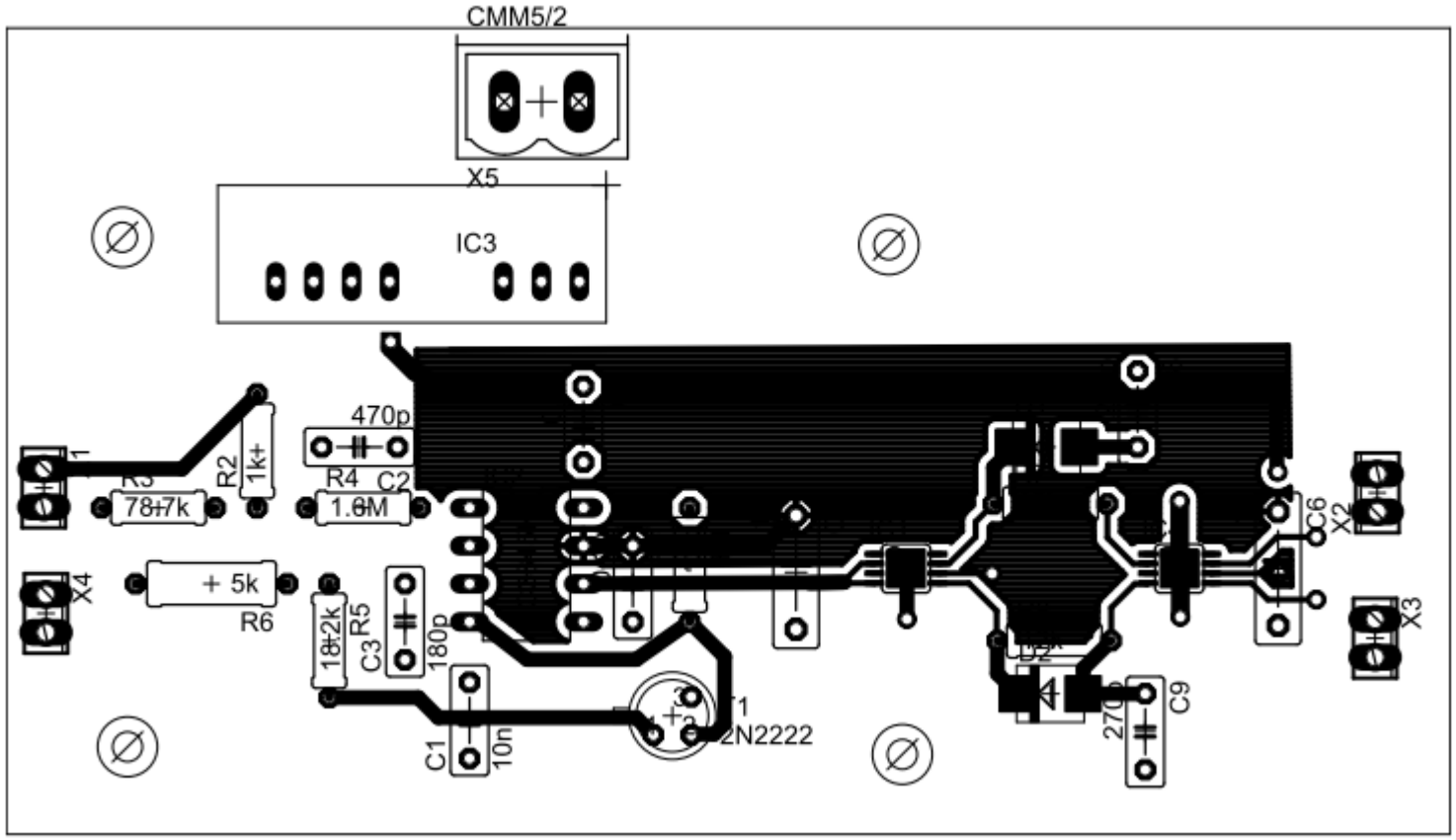

Figure D-6 Topp layer

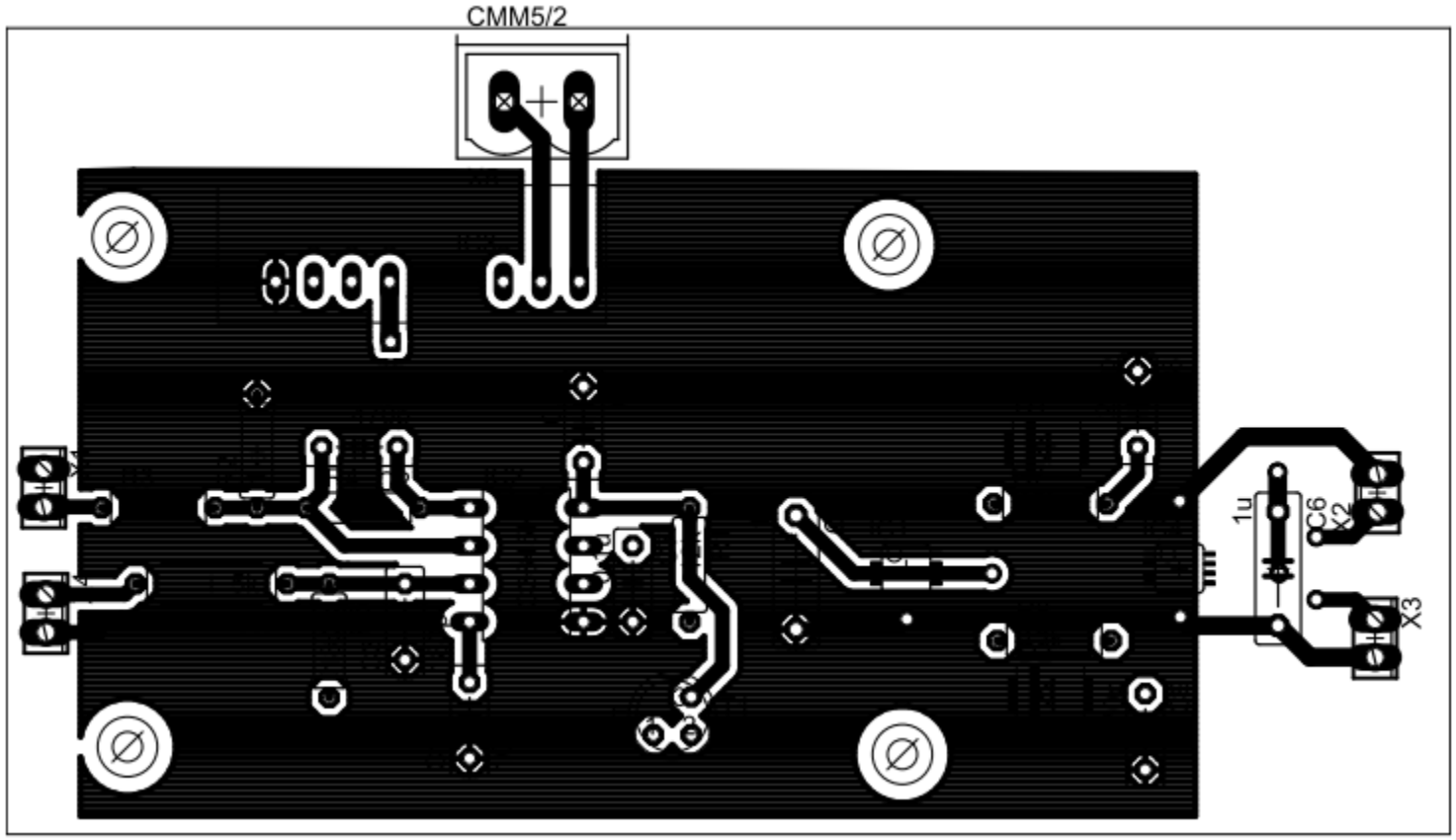

Figure D-7 Bottom layer

E Bill of Materials

E1 BOM JFET half-bridge

Component type	Count	Name/symbol	Values	Rating		Name/device	Manufacturer
DC/DC converter	2	IC1,IC2	P=5W			TEL 5-1223	Traco power
Hylse liste	1	NA(IC3,IC4)		1.5A	125V	BL 1/36 G	Fischer
JFET	2	Q1,Q2		BVds=1200V	Id(Tj=125)=30A	SJEP120R063	Semisouth
Schottky	2	D1,D2		Vdc=1200V	If=30A	SDP30S120	Semisouth
Capacitor	2	C2,C3	4.7uF	Vdc=750V	ESR=3.8mOhm	871-B32676G1475K	EPCOS
Test Pins	8	TP(1,2,4-8, 10)				SN/040/LT/BA	OXLEY
Capacitor	1	C4	100nF	Vdc=1600V	Vac=650V	PHE450RD6100JR06L2	Evox Rifa
Gatedriver	2	IC3,IC4				SGDR600P1	Semisouth
PCB	1	NA	70um				Scankemi
Thermal pads	4	NA	R=0.56C/W			K10-104	Bergquist
Contact	7	X1-7		V=250V	I=24A	CMM 5/2	Stelvio
Zener	2	D3,D7		Vbr=6.2V		1SMB5920BT3G	ON Semi
Zener	2	D4,D8		Vbr=16V		1SMB5930BT3G	ON Semi
Resistor	1	R1	11 Ohm				
Capacitor	2	C6	4.7nF	1kV			
Resistor	2	R3,R4	12 Ohm				
Capacitor	2	C1,C5	4.7nF	50V			

Table E-1 BOM for JFET half-bridge

E2 BOM BJT half-bridge

Component type	Count	Name/symbol	Value	Rating		Name/device	Manufacturer
Capacitor	2	C2,C3	4,7uF	Vdc=750V	ESR=3,8mOhm	871-B32676G1475K	EPCOS
Schottky	2	D3,D4		Vb=1200V	If=15A	IDH15S120	Infineon
Test Pins	5	TP(5-8,10)				SN/040/LT/BA	OXLEY
PCB	1	NA	70um				Scankemi
Thermal pads	1	NA	R=0,56C/W			K10-104	Bergquist
Capacitor	1	C4	100nF				
Resistor	1	R1	11 Ohm				
Resistor	1	R2	5.6 Ohm				
BJT	2	Q1,Q2		Vb=1200V	If=6A		TranSiC
Contact	5	X1-5		V=250V	I=24A	CMM 5/2	Stelvio
Contact	2	X6,X7					Berg
DC/DC	2	IC2,IC4		P=6W	Vut=15V	TEN 5-1213	Traco power
MOSFET driver	2	IC1,IC3		Ip=10A		TC4421	MICROCHIP
Capacitor	2	C7,C12	1u	Vdc=63V			EPCOS
Capacitor	6	C1,C5,C10,C11	0.1u	V=50V			Multicomp
Resistor	2	R3,R6	3.3k				
Capacitor	2	C9,C14	22n	V=50V			AVX
Resistor	2	R4,R7	1 Ohm				TYCO
Resistor	2	R5,R8	39 Ohm				TyCO
Opto coupler	2	ISO1,ISO2				ACPL-M43T	Avago
Resistor	2	R14,R15	1.3k	P=0.6W			
Resistor	2	R11,R13	7.5k	P=0.6W			

Table E-2 BOM for BJT half-bridge

E3 BOM control board

Component type	Count	Name/symbol	Value	Rating		Name/device	Manufacturer
Complementary gate driver	1	IC1				Mic4225ymme	Micrel
Non inverting driver	1	IC4				Mic4224ymme	Micrel
PWM controller	1	IC2				UC3843BN	Stmicro
Filter capacitor	1	NA	470uF	Irip(10kHz)=6.5A	Vdc=500V	ALS30A471KE500	BHC
Current sensing resistor	1	NA	0.05 Ohm	P=5W		WSR5R0500FEA	Vishay
Signal transistor	1	T1		Vbr=30V	Ic=800mA	2N2222	Multicomp
Capacitor	2	C4, C7	0.1u	V=50V			Multicomp
Dead time diode	2	D1,D2		Iav=2A	Vbr=40V	STPS2L40U	Stmicro
DC/DC omformer	1	IC3		Vut=15V	Vin=9-36V	IM2415SA	XP Power
Resistor Time delay	2	R7,R8	12k Ohm				
Capacitor	2	C5,C6	1uF	Vdc=50V	Vac=30V		
Capacitor	2	C8,C9	270pF				
Contact	4	X1,X2,X3,X4					Berghus
Contact	1	X5				CMM 5/2	Stelvio
Capacitor	1	C2	470pF	Vdc=100V			
Resistor	1	R4	1.6M Ohm	P=0.6W			
Resistor	1	R2	1k Ohm	P=0.6mW			
Resistor	1	R3	78.7k Ohm	P=0.6W			
Resistor	1	R5	18.2k Ohm	P=0.25W			
Resistor	1	R6	5k Ohm	P=0.25W			
Resistor	1	R1	12k Ohm				
Capacitor	1	C1	10nF	Vdc=100V			
Capacitor	1	C3	180pF	Vdc=100V			

Table E-3 BOM for control board

F DPT measurements with JFET half-bridge

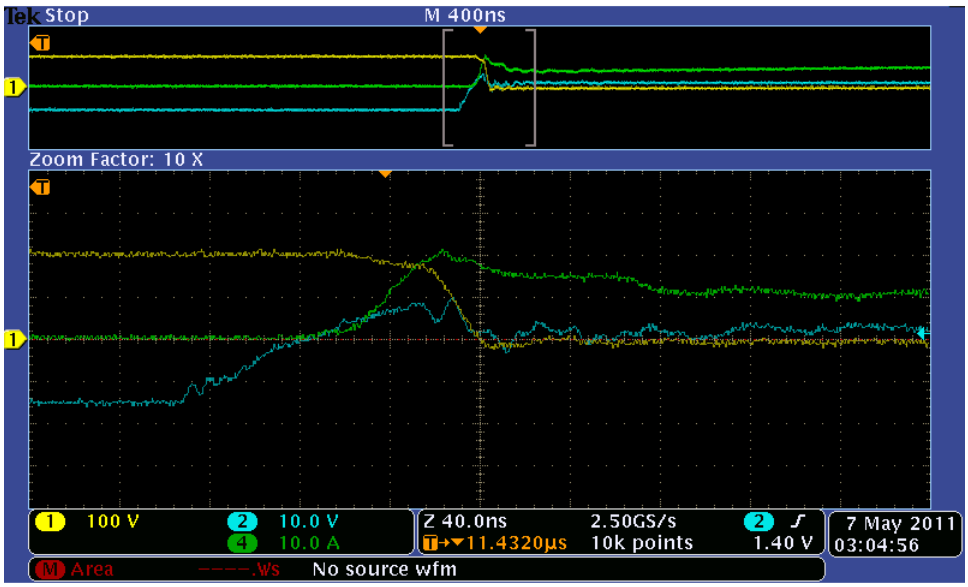

Figure F-1 Turn-on JFET with I_d=10A and V_{dc}=200V, I_d is green and V_{DS} is yellow. Peak current is equal to 21A *"Voltage shifted 6.5ns"*

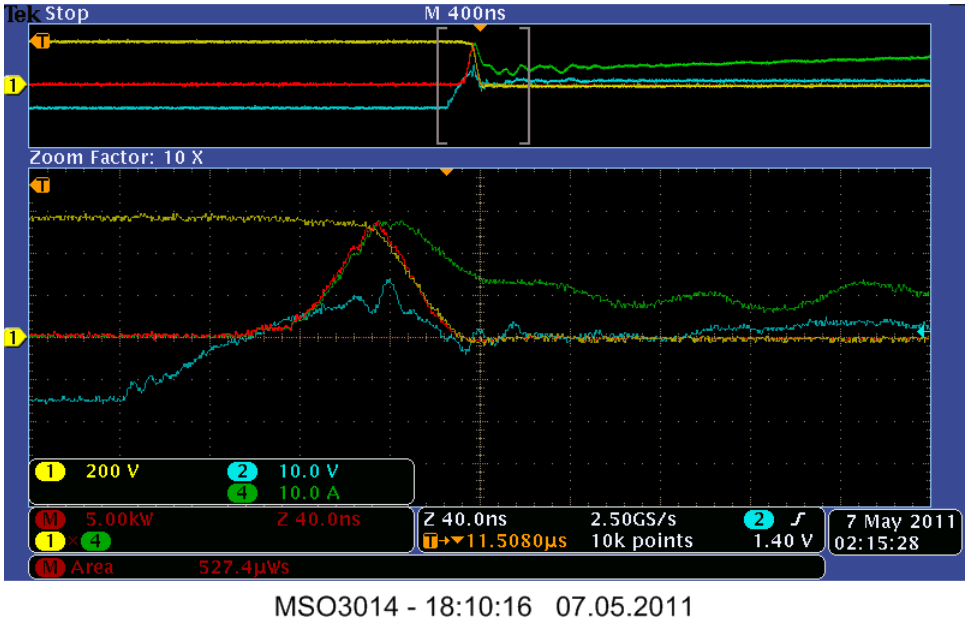

Figure F-2 Turn-on JFET with I_d=10A and V_{dc}=565V, I_d is green and V_{DS} is yellow. Peak current is equal to 28A *"Voltage shifted 6.5ns"*

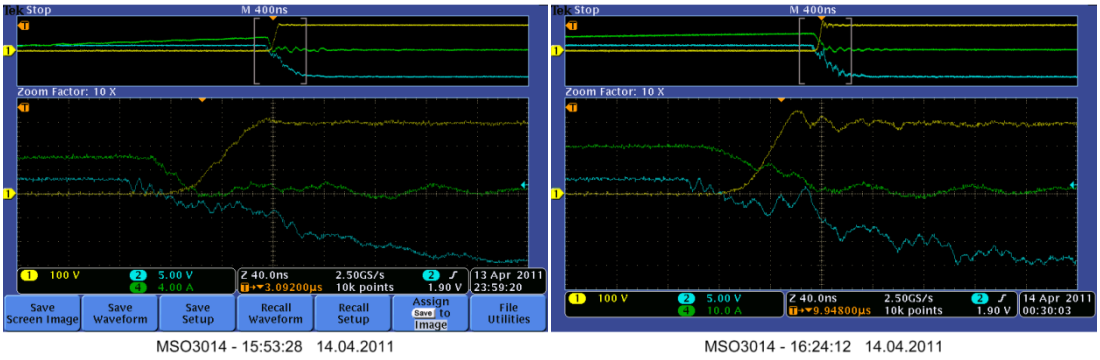

Figure F-3 JFET turn-off with DC voltage of 300V, I_d=6A to the left and 20A to the right.

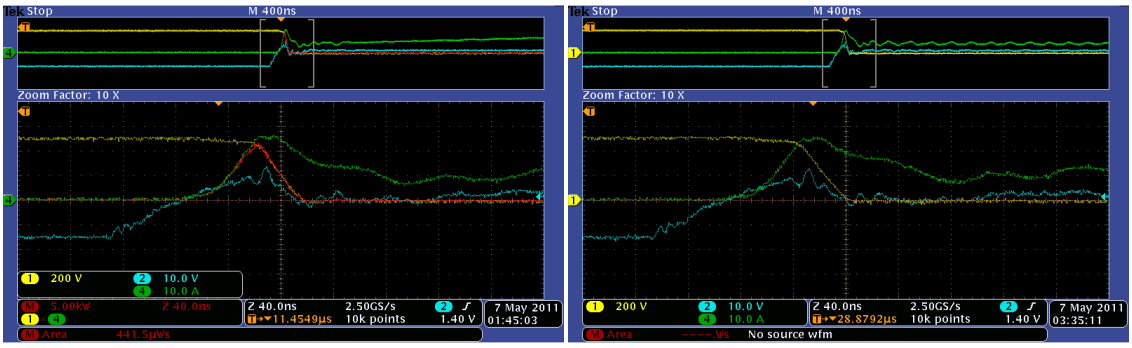

Figure F-4 JFET turn-off with DC voltage of 500V, 150µH air coil to the left and 1mH coil with iron core to the right. *"Voltage shifted 6.5ns"*

G Simulation models in LTspice

G1 Investigation of soft switching

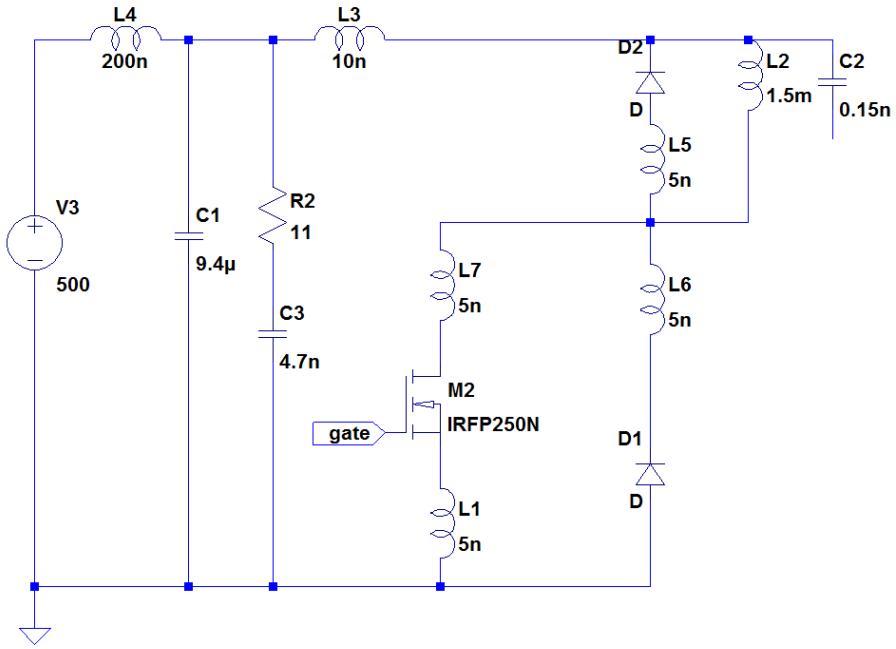

Figure G-1 Model for investigation of soft switching

G2 Dead time generation model

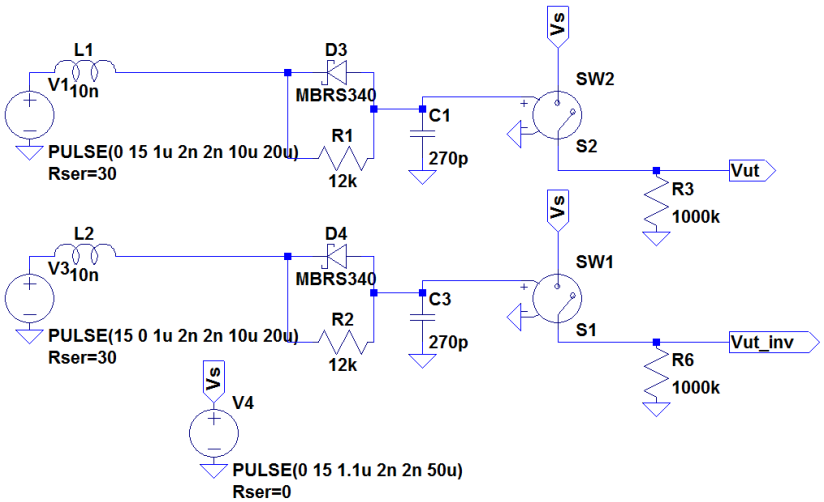

Figure G-2 Model for investigation of the dead time generation.

G3 Model of step down converter and SBC

The controller circuit in Figure G-3 is common for both the Buck and the synchronous Buck converter.

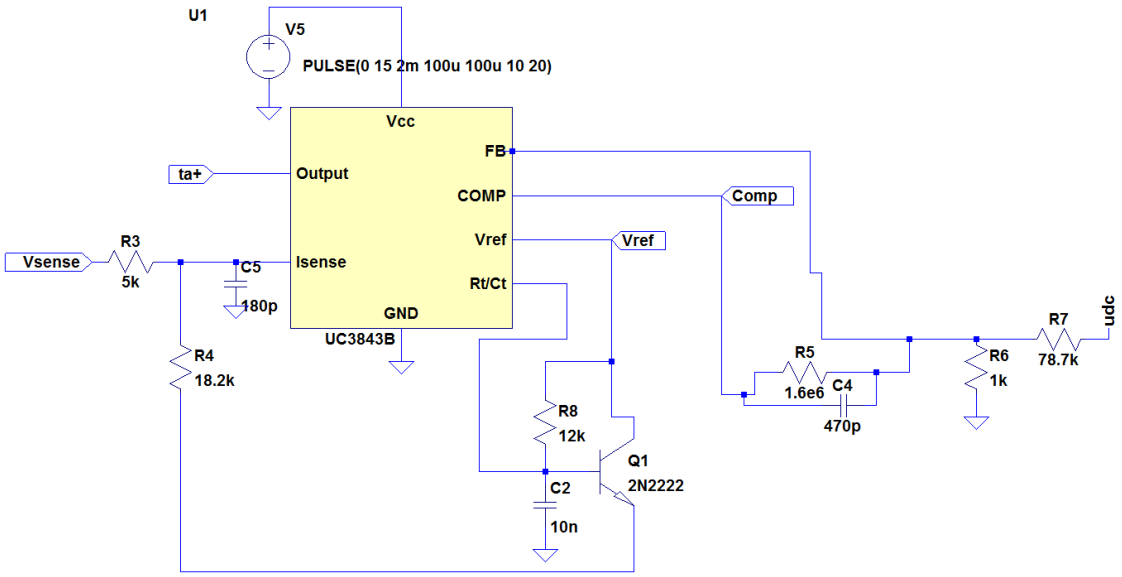

Figure G-3 Controller circuit

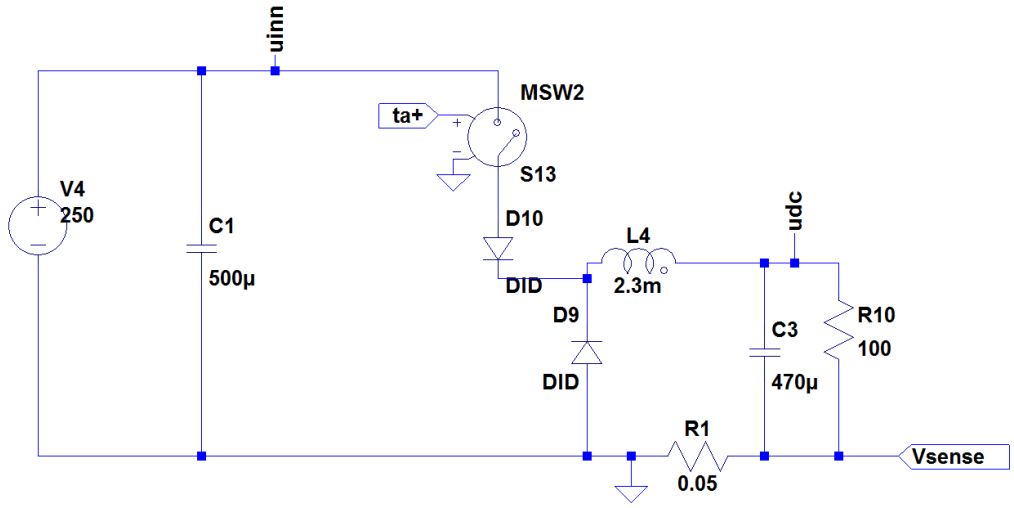

Figure G-4 Model of Buck converter

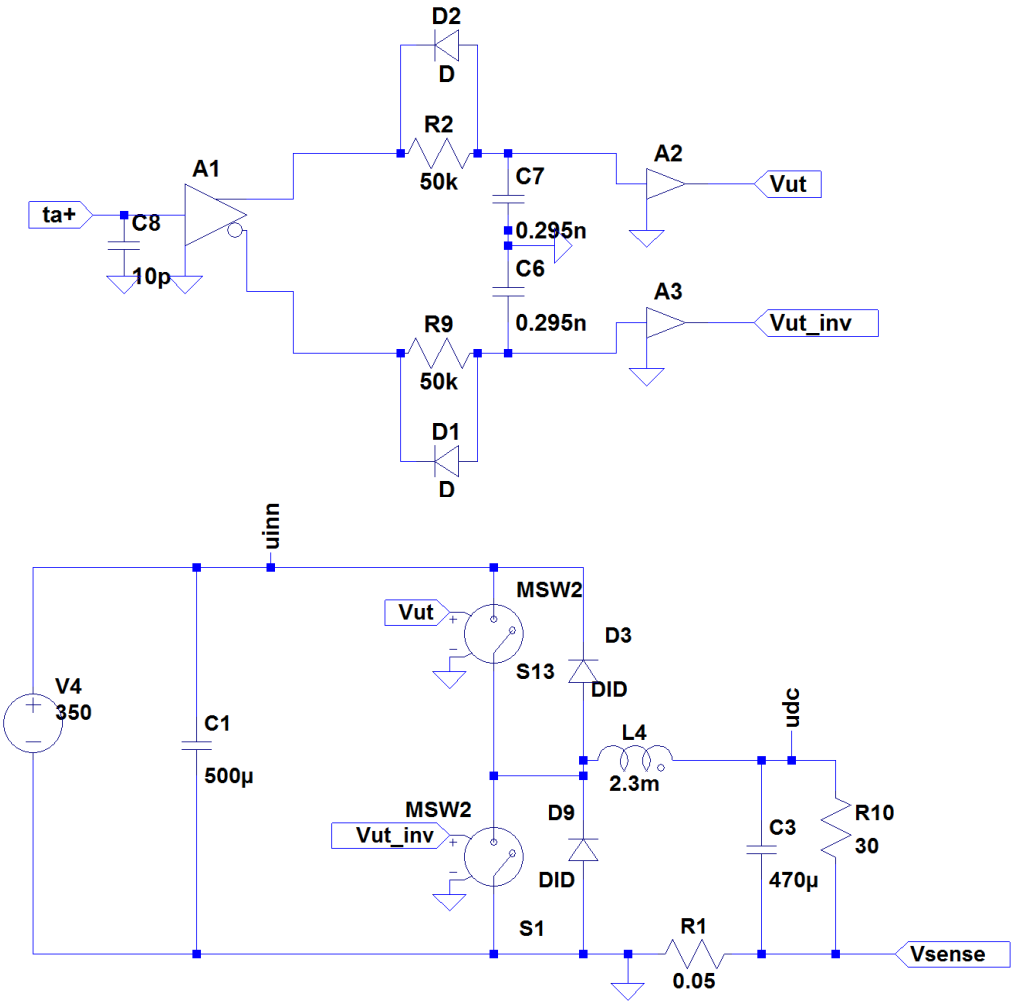

Figure G-5 Model of SBC, the upper circuit generates the complementary outputs

H Measurements of step down converter

This appendix presents measurements from the step down converter. The yellow curves are input voltage to output filter, the purple curves are the inductor current and turquoise curves are the ripple component of the output voltage.

H1 Output waveforms for a 59Ω load

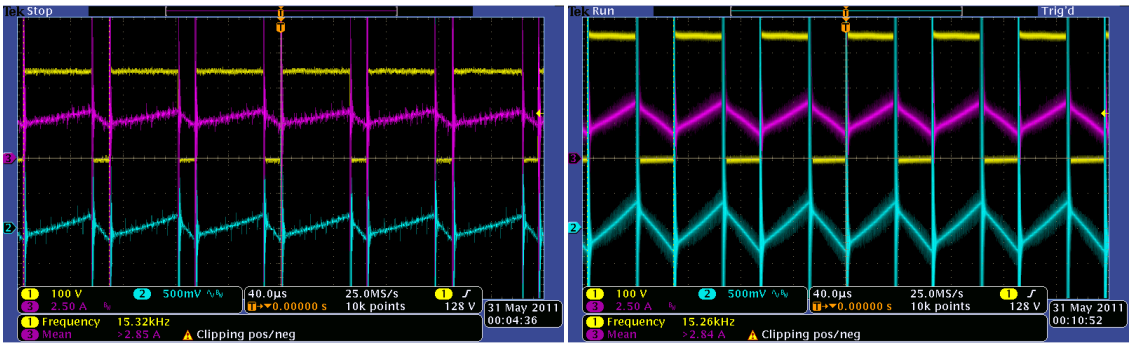

Figure H-1 Vin=250V to the left and Vin=350V to the right

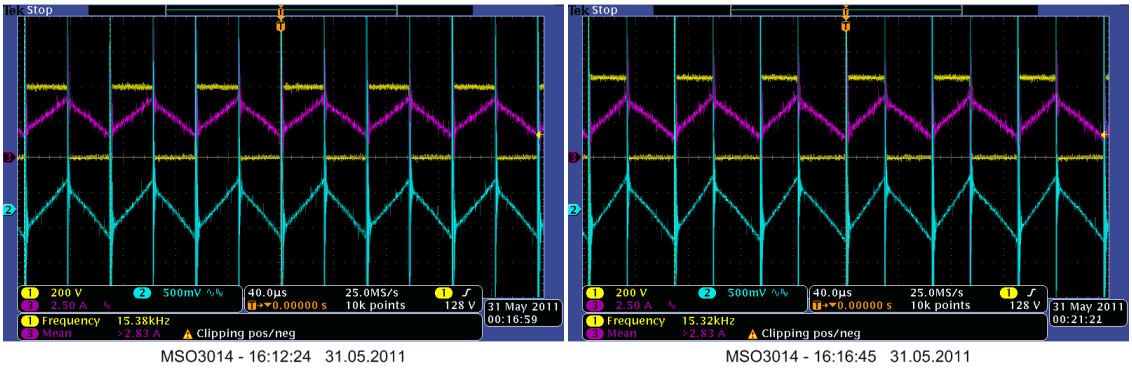

Figure H-2 V_{in}=400V to the left and V_{in}=450V to the right

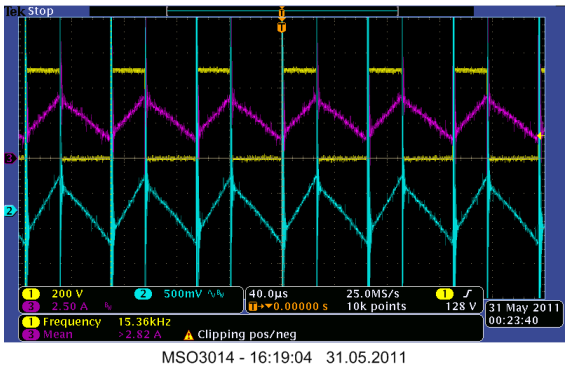

Figure H-3 V_{in}=500V

H2 Step load from 59Ω to 30Ω for a input voltage of 400V

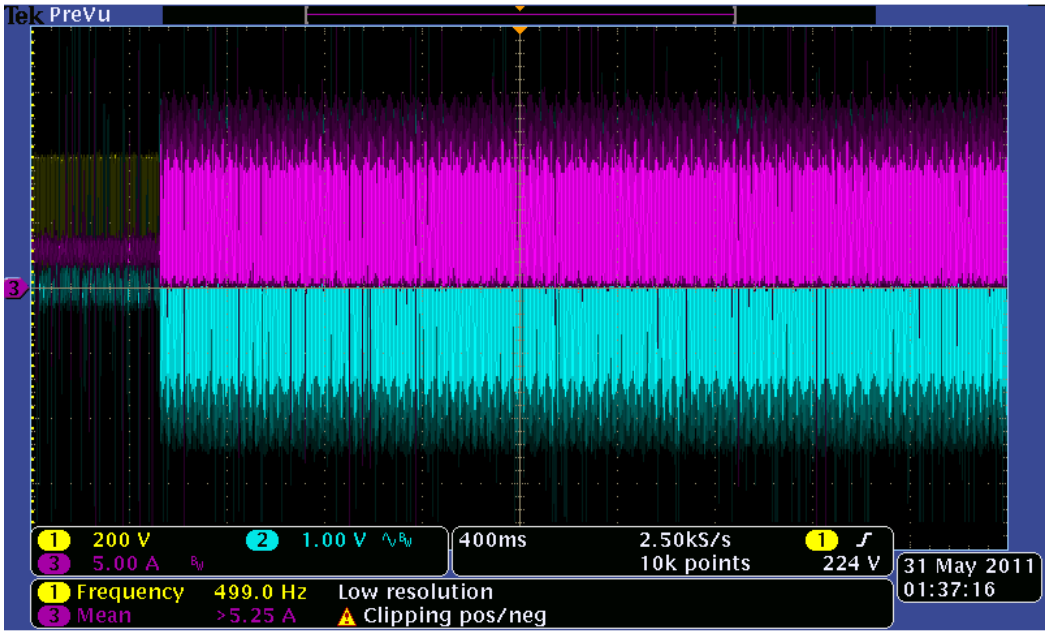

Figure H-4 Step load response

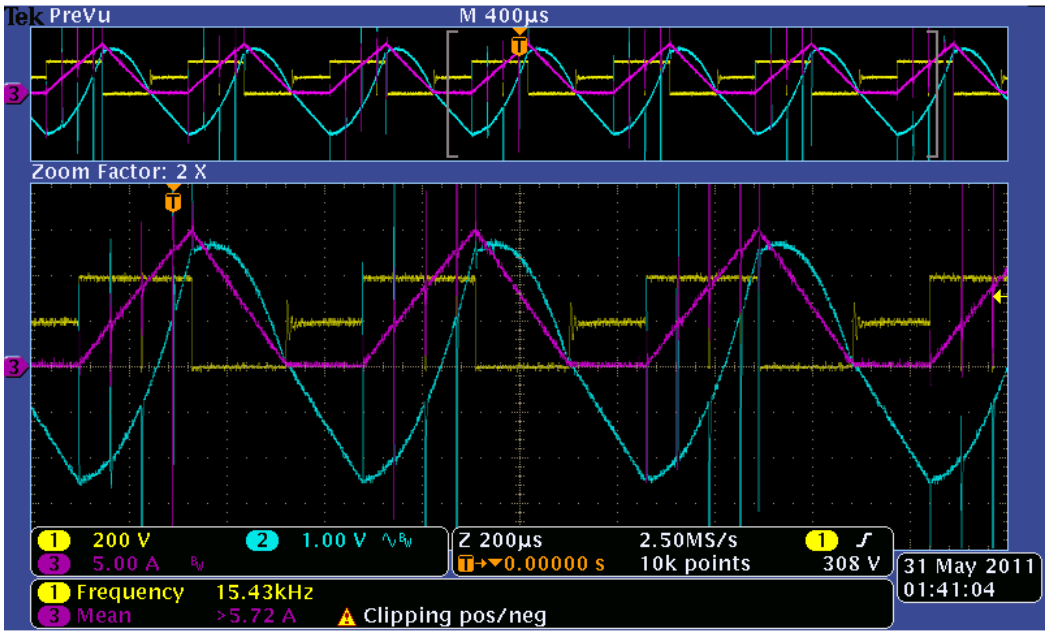

Figure H-5 Output waveforms after the step load

I Pictures from the laboratory

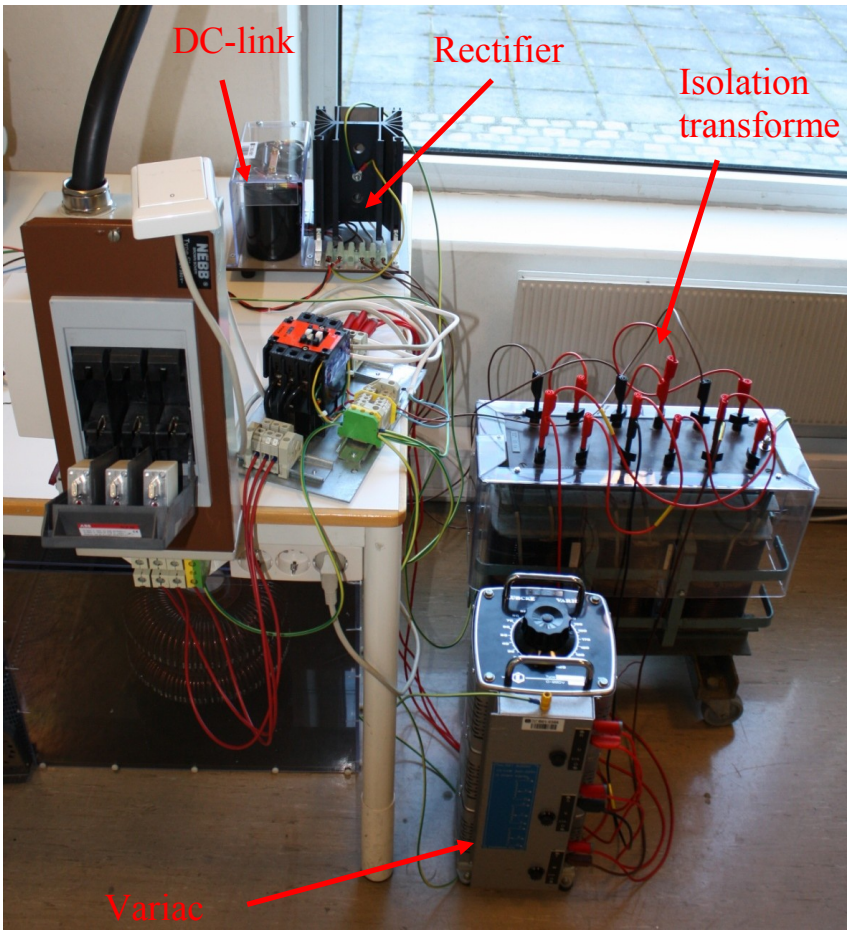

Figure I-1 Picture of lab setup

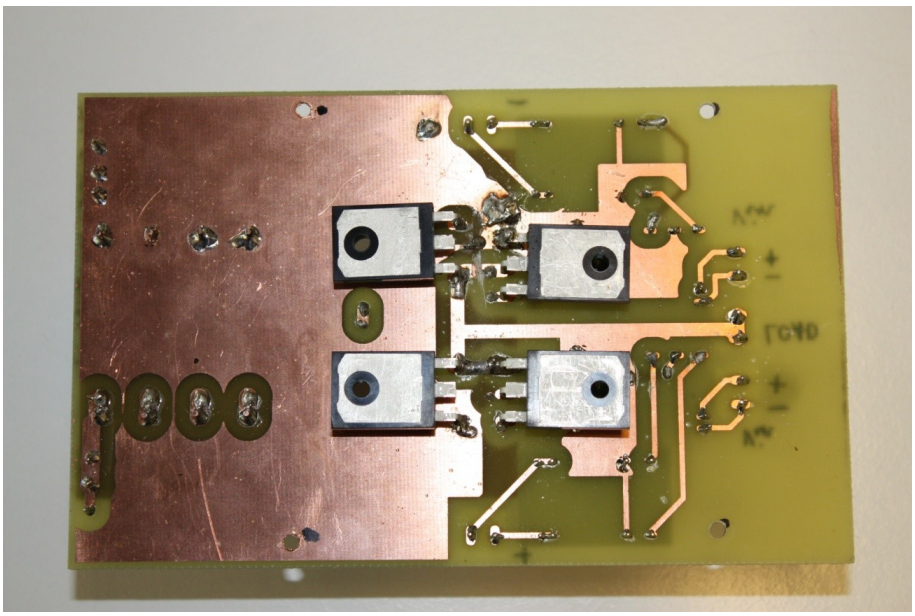

Figure I-2 Bottom side of JFET PCB

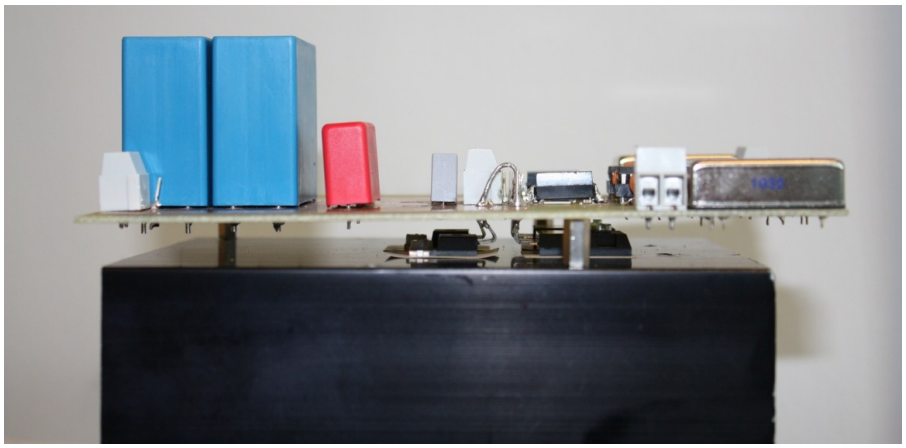

Figure I-3 Side view of BJT PCB

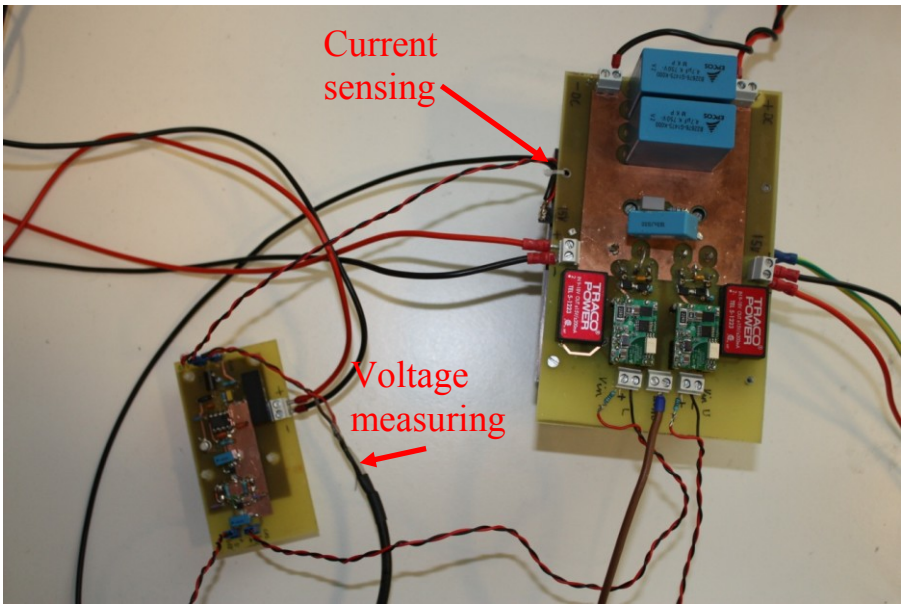

Figure I-4 Connection of control board

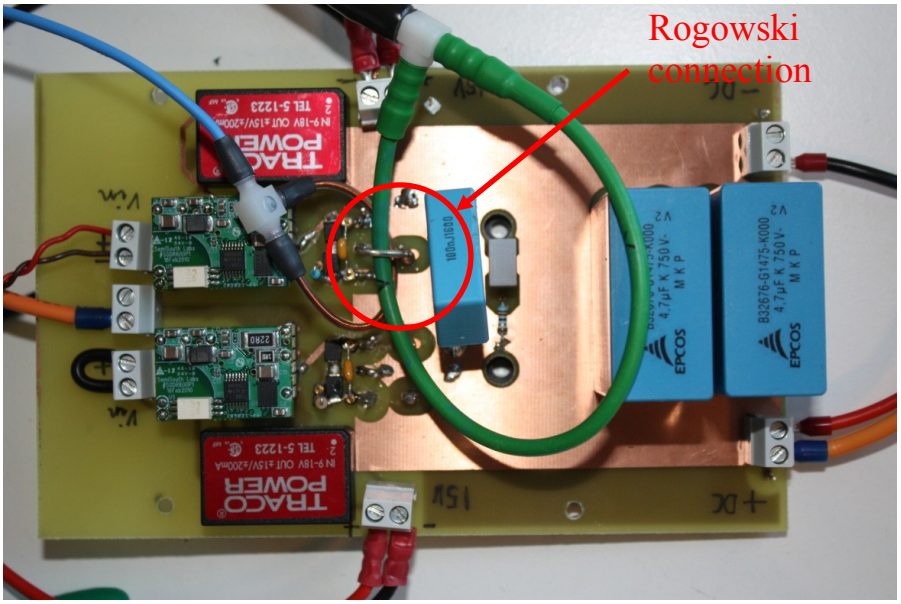

Figure I-5 Connection of Rogowski coils