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A 10 dBm 2.4 GHz CMOS PA

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Master of Science in Electronics
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Problem Description

Background:
In addition to the sensitivity of the receiver, the output power of the transmitter is a decisive factor for the transmission range in wireless communication systems. The typical output power in the recent commercial 2.4 GHz band systems has been 0 dBm. In some cases, the ETSI/FCC standards allow higher output power, and taking advantage of this would be desirable. This assignment consists of assessment and design of a 10 dBm 2.4 GHz Power Amplifier.

Assignment:
- The student should choose a suitable architecture based on the given specifications. The theoretical limitations of the chosen architecture and the considerations leading to the choice should be reported.
- The Power Amplifier should be designed (schematics and layout) in a typical 0.18 um CMOS process according to the specifications. It should be robust against the temperature, supply voltage and process variations.
- The assignment also includes the evaluation and requirement specification of an antenna matching circuit if applicable.

Typical tasks in the course of this work are modelling, schematic and layout design, and extraction of the parasitics from the layout.

Assignment given: 16. January 2006
Supervisor: Jukka Tapio Typpø, IET

Abstract

This report describes the assessment and design of a 10 dBm 2.4 GHz CMOS PA including driver stage. The PA is designed in a 0.18 μm CMOS technology.

A three stage PA has been designed due to the high voltage gain needed. Class F has been chosen for the output stage. An output filter short-circuiting the second harmonic frequency and reflecting the third harmonic frequency is used to obtain the near-square drain voltage that is characteristic to class F.

A lowered supply voltage of 0.9 V is used to avoid exceeding the transistor break-down voltage of 2 V.

The typical output power achieved is 10.2 dBm. The drain efficiency of the output stage is 47.7 %, and the *PAE* of the entire PA is 30.5 %. The final layout excluding bonding pads consumes an area of 0.66 mm^2, including four internal inductors consuming a total of 0.59 mm^2.

The *PAE* obtained is higher than those of a selection of recently published PAs that are comparable in technology, frequency and output power.

Acknowledgements

This master thesis has been written in the 10th and last semester of a Master of Science in Electronics degree at the Department of Electronics and Telecommunications, NTNU.

The work has been carried out at Texas Instruments Norway in Oslo, a company with high expertise in RF transceiver design. I am grateful for the opportunity to complete my studies in a professional environment.

My best thanks to Tor-Inge Kvaksrud and Øyvind Birkenes, my supervisors at Texas Instruments Norway, for continuous guidance and support throughout the project. Thanks also to Roger Johnsen at Texas Instruments Norway for valuable RF design tips.

Oslo, June 2006

Torjus Selvén Kallerud

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1 Introduction

The Power Amplifier (PA) is a crucial component in any radio transmitter. Its key performance metrics are output power, efficiency and linearity. The output power is one of the deciding factors of transmission range, and is obviously valuable. The efficiency is a measure of the amount of energy transmitted compared to the total amount of energy consumed by the amplifier. A high efficiency is vital for long battery life, and in some appliances to avoid excessive heating. The linearity of the amplifier is very important when information is contained in the amplitude of the signal. When amplifying constant envelope signals, as in this project, the resulting distortion due to non-linear behaviour is the main concern.

TABLE 1.1 PA SPECIFICATION

	Minimum	Typical	Maximum	
Global supply voltage V_{glob}	1.7	1.8	1.9	**V**
PA supply voltage V_{dd}	0.85	0.9	0.95	**V**
Temperature T	-40	27	125	**deg C**
Frequency f_0	2.4		2.4835	**GHz**
Differential input signal V_{in}		400		**mV (peak-to-peak)**
Input capacitance C_{in}		100		**fF**
Output power P_{out}		10		**dBm**

The specifications of the PA are given in Table 1.1. The typical values are those expected in normal operation, while the minimum and maximum shows the deviation that must be tolerated. The supply voltage, temperature, frequency band and input signal amplitude are parameters that will be used when designing the PA. The input capacitance and output power will be goals to achieve. The PA will be optimised for high efficiency, while keeping in mind that the area consumed is important for the production cost. No minimum and maximum values are given for the input capacitance and the output power. The deviation should still be kept to a minimum.

The report includes some general PA background, leading to a choice of class. The theoretical limitations of the PA are reported, and also the limitations imposed by the available process and external components. A chapter on schematic design explains the considerations leading to an initial PA, before a revision of the PA due to instability is described. A section on the layout of the PA and its performance and reliability follows, before the design is concluded.

The complete schematics of this PA with dimensions are only available in the appendix. The distribution of the appendix is restricted, and it is therefore printed separately.

2 Background

Some general PA background is needed to understand this work. Some common performance metrics will first be introduced. A short introduction to modulation formats used in radio communication is given next, with their relation to PA design. The final section explains some theory on stability and its application on PA design.

2.1 Power Amplifier performance metrics

The performance of a PA is a combination of several metrics [1]. Most important is the output power in the frequency band of interest. The frequency band is often characterised by bandwidth *BW* around a centre frequency f_0. The centre frequency is often reported as an angular frequency ω_0 where

$$\omega_0 = 2\pi \cdot f_0 . \tag{2.1}$$

Power is generally reported in W, while the output power P_{out} of a PA is typically reported in dBm. dBm is a logarithmic scale where 0 dBm corresponds to 1 mW. Conversion is done by

$$P_{out}\left[\text{dBm}\right] = 10 \cdot \log\left(\frac{P_{out}\left[\text{mW}\right]}{1\,\text{mW}}\right). \tag{2.2}$$

This PA will be designed to have an output power of 10 dBm across the 2.4 GHz Industrial-Scientific-Medical (ISM) band, ranging from 2.4000 GHz to 2.4835 GHz.

Another key measure is the efficiency. The drain efficiency η of a PA is the ratio of power delivered to the load P_{out} to the power P_{DC} drawn from the power supply,

$$\eta = \frac{P_{out}}{P_{DC}} . \tag{2.3}$$

High efficiency can be obtained by trading power gain. The Power Added Efficiency (*PAE*) is therefore a better measure that takes the power gain into account by subtracting the input power P_{in}. The *PAE* is given by

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} . \tag{2.4}$$

The *PAE* will be used as the key performance metric in this design, meaning that the design will be optimised for the highest possible *PAE*.

The normalised power output capability *PN* is the ratio of the output power to the product of the maximum drain current Id_{max} and the maximum drain voltage Vd_{max},

$$PN = \frac{P_{out}}{Vd_{\max} \cdot Id_{\max}}. \qquad (2.5)$$

A low *PN* means that the device is stressed with a large drain current or a large drain voltage compared to the output power. In integrated CMOS, the voltage across any two nodes of a transistor is limited due to various break-down phenomena. The normalised power output capability can therefore be an indication on ability of integration.

2.2 Modulation formats

Radio Frequency (RF) systems transmit information by modulation of a carrier wave. Modulation means an alteration of the carrier wave that can be detected by the receiver and translated back to the original information. Three basic properties of a carrier wave can be alternated; amplitude, frequency and phase. This gives rise to amplitude modulation (AM), frequency modulation (FM) and phase modulation (PM). AM and FM are well known for their use in radio broadcasting.

Most modern wireless systems[1] transmit digital signals. Modulation of a stream of digital bits is called keying, where 0 and 1 are converted into a change of a carrier wave property. The three basic formats are amplitude shift keying (ASK), frequency shift keying (FSK) and phase shift keying (PSK). More advanced modulation formats such as Quadrature Amplitude Modulation (QAM) use a combination of these to increase the bit rate by transmitting more bits per symbol.

For the PA design, there are two important aspects of the modulation format. These are the bandwidth of the resulting signal and the use of amplitude modulation. Modulation and keying introduce sidebands to the carrier wave. The bandwidth of the resulting signal depends on the modulation format, and will have to be narrower than the bandwidth of the PA.

[1] And also the first systems created

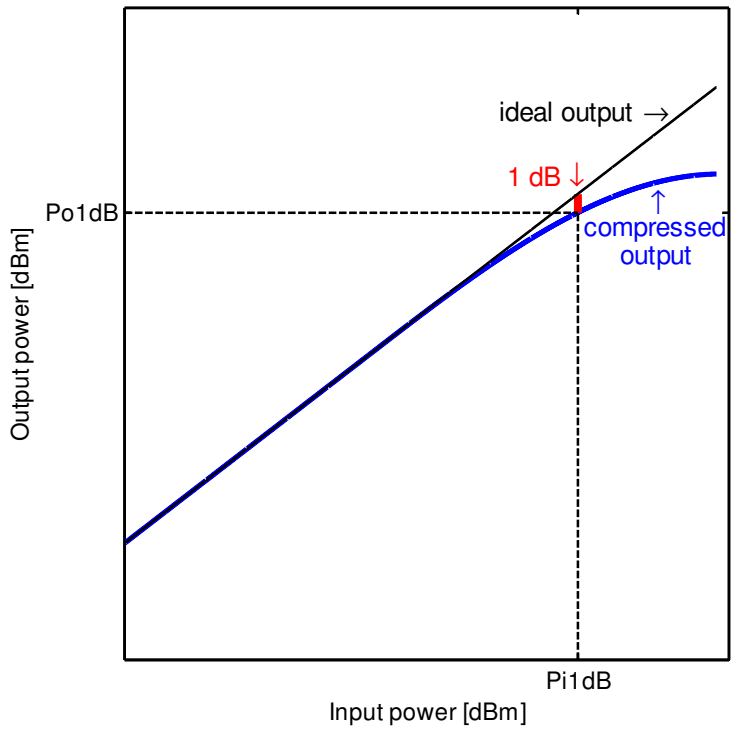


FIGURE 2.1 COMPRESSION IN A PA

Correct amplification of an amplitude modulated signal requires the use of a linear PA, meaning that the gain of the PA is equal over a range of different input amplitudes. All amplifiers will experience compression, which is a reduction of gain at high input amplitudes, as illustrated in Figure 2.1. The output amplitude will thus be lower than expected. The point where the output power is 1 dB lower than anticipated from the gain in the linear region is called the 1-dB compression point. It can be related to the input power, i.e. Pi_{1dB}, or the output power, i.e. Po_{1dB}.

This compression will not equally affect the entire waveform, only the parts where the voltage level approaches the supply voltage. The resulting output waveform will thus be different than the input. Assuming a sinusoid input signal, the result will be a “flattened sinusoid” as shown in Figure 2.2. This alteration will add a certain signal power at harmonic frequencies of the input signal.

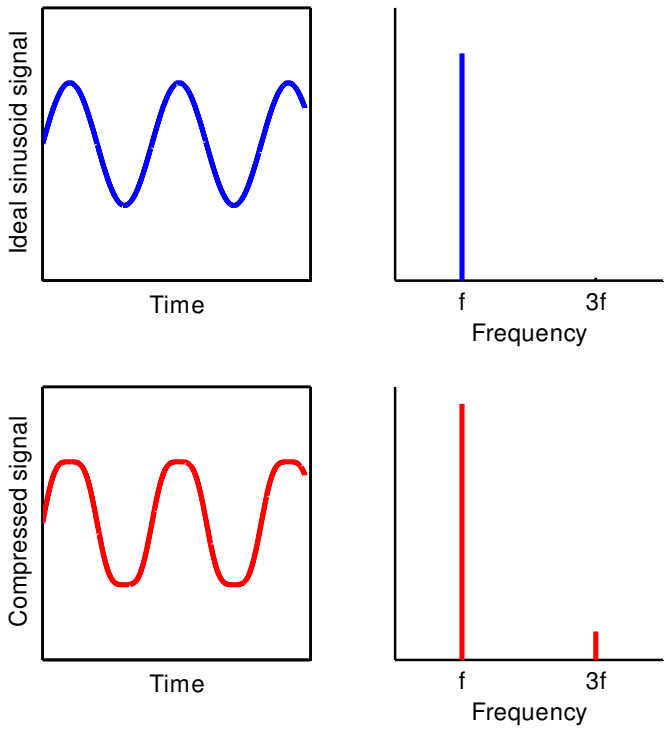


FIGURE 2.2 EXAMPLE OF AN IDEAL SINUSOID AND A FLATTENED SIGNAL DUE TO COMPRESSION

A common solution to compression problems is back-off. The PA is simply limited to the linear region, i.e. amplifying signals that do not drive the PA into compression. As all amplifiers are most efficient with a large output signal swing, back-off seriously reduces efficiency. For example, a PA amplifying signals for use in WLAN[2] might need a back-off of 8-10 dB to keep the error rate reasonably low. This typically reduces the *PAE* of a linear PA to about 5 % [2].

When amplifying a signal with constant envelope, the alteration of amplitude is not a problem. The input amplitude is constant, and the output amplitude is also constant. The harmonic power radiated from the antenna is regulated, so additional filtering may be necessary if compression introduces a larger harmonic power than the regulations allow.

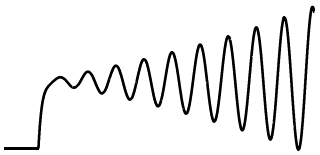
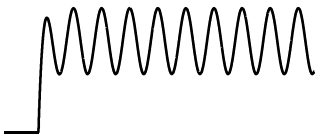
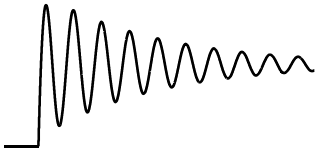
2.3 Stability

Stability is an important issue in all amplifiers. One method of identifying instability is by an investigation of the step response of the PA. A step inserts energy at all frequencies into the PA and is likely to trigger instability sources.

[2] The 802.11a Wireless Local Area Network (WLAN) standard uses 64-QAM modulation, where a combination of phase and amplitude modulation enables a transmission of 64 bits per symbol.

Considering the PA as a second-order resonant circuit, the step response can be understood by the theory of simple harmonic motion [3]. The possible cases are listed in Table 2.1.

TABLE 2.1 POSSIBLE CASES FOR SIMPLE HARMONIC MOTION

Case	Oscillations	Example step response	Consideration
Positive feedback	Growing		Unstable
Undamped	Constant		Unstable
Underdamped	Decaying		Marginally stable
Critically damped	None		Stable
Overdamped	None		Stable

Critical damping would be desirable for this PA. This would ensure a rapid, stable response at the supply voltage turn-on. An overdamped system would be equally stable, but would require a longer time before attaining the anticipated steady state. The underdamped system is common in PA design, and is also considered stable as the oscillations disappear over time.

Small variations can turn an underdamped system into an unstable system. An underdamped system therefore has a low stability margin. When subject to an RF input signal, a PA with an unstable step response will experience a similar instability on the envelope of the RF output signal.

3 Choice of class

PAs are divided into different groups called classes, which are described in this chapter. The main usable classes for radio frequencies range from class A to class F. The conventional classes A, AB, B and C use the amplifying transistor as a controlled current source. The switching classes D, E and F use the transistor as a switch in order to increase efficiency. Only a summary of the most relevant properties is presented here. A more thorough review is given in [1]. The chapter will conclude with a choice of class for this PA.

3.1 Conventional classes

Class A, AB, B and C are called conventional for their history of being the first available PAs, and also for their currently widespread use. A class A PA, as shown in Figure 3.1, consists of a simple common-source amplifying transistor. It is biased such that the transistor stays in the active region [1], as in a small-signal amplifier. A large DC-blocking capacitor prevents DC dissipation in the load, and a resonant filter ideally short-circuits any harmonic power. The class A PA is, as a small-signal amplifier, characterised by nearly linear operation but also high power consumption compared to the power delivered to the load.

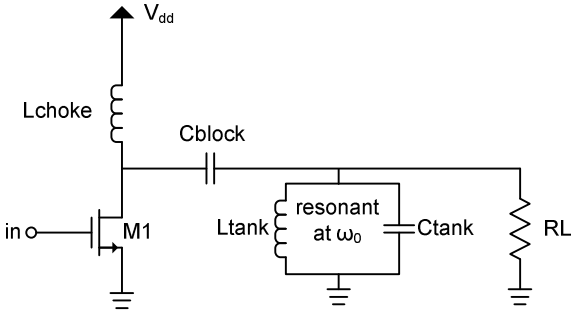


FIGURE 3.1 CLASS A PA EXAMPLE CIRCUIT

The concept of the following classes AB, B and C can be understood from the same circuit diagram as the class A, with the main difference being biasing. The bias current in the transistor is lowered so the transistor is conducting for only a part of the RF cycle. This increases efficiency while reducing linearity and gain, ranging from the quasi-linear class A to the non-linear class C with a maximum theoretical drain efficiency of 100 % [1]. However, as the drain efficiency approaches 100 %, the power gain approaches zero. The maximum efficiency will thus be limited by the required gain.

High gain, quite linear amplification and limited distortion have made the conventional classes attractive for integration in CMOS. However, the final PAE obtained is often very low and far from the theoretical maximum. This has a negative impact on the battery life of handheld devices, and can also lead to problems related to heat dissipation. The search for higher efficiencies has lead to the use of the transistor as a switch.

3.2 Switching classes

Classes D, E and F are named switching classes, as the amplifying transistor is used as a switch. An ideal switch does not dissipate any power, as the voltage across it is zero when switched on, and the current through it is zero when switched off. The maximum theoretical efficiency of these classes is therefore 100 %, but various issues limit their practical PAE and their use in integrated CMOS.

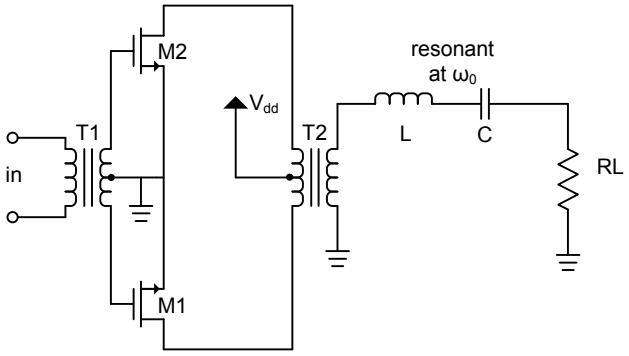


FIGURE 3.2 CLASS D PA EXAMPLE CIRCUIT

The class D PA is believed to have been introduced by Baxandall [4]. The concept is to switch a current between two transistors, so that each transistor only conducts current when the voltage across it is zero. This can be achieved as shown in Figure 3.2 by means of transformers, but the operation relies on switches that are considerably faster that the period of the signal. If the switching time T_{sw} corresponds to a considerable portion of the RF period T_{RF}, the non-zero product of voltage and current during switching will lead to a decrease of efficiency. For that reason, the class D PA is often used in audio systems, and can also be found in low RF PAs. However, with the available process and in the 2.4 GHz band, the switching times will be considerable.

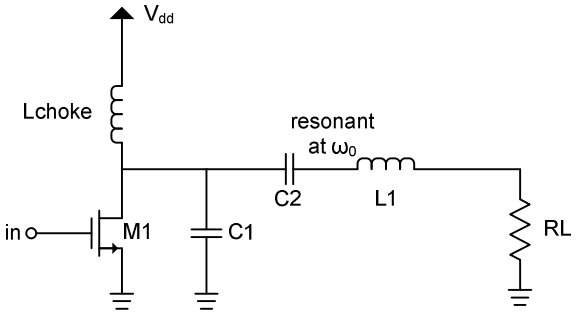


FIGURE 3.3 CLASS E PA EXAMPLE CIRCUIT

The class E PA was invented in 1975 in an attempt to increase the efficiency of switching PAs operating at high frequencies [5]. Instead of relying solely on fast switching to separate the voltage and the current, it uses a load network to shape the voltage waveform. The goal is a voltage waveform with zero amplitude and zero slope at the switching points. By adding a shunt capacitor between drain and source to the load network, as shown in Figure 3.3, this is obtained at the switch

turn-on. However, the current is nearly at a maximum when the switch turns off, leading to a considerable loss of efficiency when using non-ideal switches at high frequency. It also introduces a large stress on the switching transistor, with a maximum voltage of 3.6 times the supply voltage V_{dd} at the drain [1].

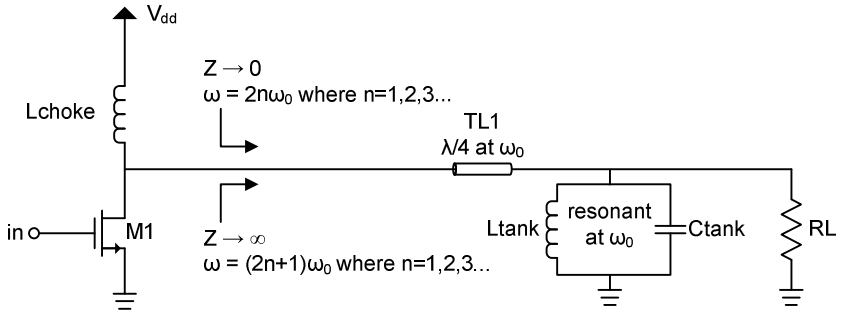


FIGURE 3.4 CLASS F PA EXAMPLE CIRCUIT

The class F PA shown in Figure 3.4 is often traced to Tyler [6]. Similarly to class E, the concept is using an output filter to shape a voltage waveform at the drain of the output transistor so that it has zero amplitude when the switch is on. Unlike class E, the output filter of a class F PA is used to terminate the harmonic frequencies (harmonics) of the output voltage signal with specific impedances, so that it approaches a square wave. The concept of flattening drain voltages to increase efficiency was well-known, but Tyler is recognised as the inventor of a working class F PA.

In ideal class F operation, all odd harmonics are terminated in an open circuit, and all even harmonics are terminated in a short circuit. This results in a voltage wave at the drain of the output transistor that contains only odd harmonics, which is a square wave. The drain current is also shaped by the output network, resulting in a half-sinusoid current waveform containing only even harmonics.

3.3 Concluding the choice of class

The main performance criteria of the different classes are recapitulated in Table 3.1, with the main challenge of each class marked in orange.

TABLE 3.1 EVALUATION OF PA CLASSES (NUMBERS FROM [1])

	Maximum theoretical efficiency η	Normalised power output capability *PN*	Peak drain voltage Vd_{max}	Special requirements
Class A	50 %	0.125	2 V_{dd}	
Class AB, B	78.5 %	0.125	2 V_{dd}	
Class C	→ 100 %	→ 0	2 V_{dd}	
Class D	100 %	0.32	2 V_{dd}	$T_{RF} >> T_{sw}$
Class E	100 %	0.098	3.6 V_{dd}	
Class F	100 %	0.16	2 V_{dd}	

The main drawback of the linear classes A, AB and B is the inherent limitation on efficiency. Even though most PAs at 2.4 GHz will operate far from its maximum theoretical efficiency, published class A, AB or B RF PAs report lower efficiencies than other classes [7],[8]. Class C can theoretically be highly efficient, but with a gain that can be lower than that of the switching classes. Its low normalised power output capability requires the use of larger devices than the other classes.

The three switching classes are equally able to provide high efficiency, and there are examples of functioning implementations of each class [9]-[11]. The result in this work will depend on the success of integration, i.e. obtaining the behaviour described above in a robust solution with the given specification and process.

The main objection to class D is the requirement of very fast devices, as the square waveform generation relies on short switching times compared to the RF period. Class E suffers from a larger peak drain voltage than the other classes, leading to an additional challenge with regards to the break-down voltage limit of 2 V across any two nodes of a transistor. Class F relies on square waveforms generated by appropriate filtering. This is feasible in the 2.4 GHz band, although area consuming. The peak drain voltage can pose problems in class F as in any other class, but less than in class E.

The class F architecture is therefore considered the most suitable for this specific task.

4 Ideal class F operation

An overview of the operation and theoretical limitations of an ideal class F PA is given below. The ideal behaviour of a class F PA with a limited number of reflected harmonics is also described.

4.1 Ideal solution

An example class F PA circuit is shown in Figure 3.4. A parallel LC-filter resonant at the fundamental frequency will have high impedance at the fundamental frequency. When connected between the drain node and ground, this filter will allow the energy of the fundamental frequency to reach the resistive load. At frequencies below and above the fundamental frequency the impedance will ideally be zero, short-circuiting the harmonics to ground. This is the desired operation for even harmonics, while an open circuit is required for the odd harmonics.

A lossless transmission line connected to a load Z_L will have an input impedance Z_{in} dependent on the length l [12], with Z_{in} given by

$$Z_{in} = R_0 \cdot \left(\frac{Z_L + jR_0 \tan(\beta l)}{R_0 + jZ_L \tan(\beta l)} \right) \tag{4.1}$$

where β is the phase constant of the medium and R_0 is the characteristic impedance of the transmission line.

A transmission line with a length equal to a quarter of the signal wavelength λ, known as a quarter-wave transformer, has an input impedance

$$Z_{in} = R_0 \cdot \left(\frac{Z_L + jR_0 \tan\left(\beta \frac{\lambda}{4}\right)}{R_0 + jZ_L \tan\left(\beta \frac{\lambda}{4}\right)} \right). \tag{4.2}$$

The signal wavelength λ in the medium is given by the ratio of the phase speed u_p and the frequency f_0,

$$\lambda = \frac{u_p}{f_0}. \tag{4.3}$$

Using that and

$$u_p = \frac{\omega_0}{\beta}, \tag{4.4}$$

it is found that

$$\lambda = \frac{u_p}{f_0} = \frac{u_p 2\pi}{\omega_0} = \frac{2\pi}{\beta}. \tag{4.5}$$

The input impedance is thus

$$Z_{in} = R_0 \cdot \left(\frac{Z_L + jR_0 \tan\left(\frac{\pi}{2}\right)}{R_0 + jZ_L \tan\left(\frac{\pi}{2}\right)} \right). \tag{4.6}$$

$\tan\left(\frac{\pi}{2}\right)$ is not defined, but the limit value can be found to be

$$Z_{in} = \frac{R_0^2}{Z_L}. \tag{4.7}$$

This result shows that the impedance seen into a quarter-wave transformer Z_{in} will be a short circuit if the load impedance Z_L is an open circuit, and vice versa. This is known as impedance inversion.

A quarter-wave transformer at the fundamental frequency will appear as half a wavelength at the second harmonic. This will invert the impedance twice, resulting in the original impedance. The second harmonic will thus see a short circuit. The third harmonic will see a short circuit inverted three times, which is an open circuit. Higher harmonics will ideally be correspondingly terminated, even harmonics will see open circuits and odd harmonics will see short circuits.

The resulting drain voltage will contain only odd harmonics, and thus ideally be a square wave as shown in Figure 4.1. As no DC voltage drop can exist across an inductor, it will have an average value of V_{dd}. When assuming a perfect switch with zero on-resistance and infinite off-resistance, the drain voltage will be 0 V when the switch is on and $2 \cdot V_{dd}$ when the switch is off. The drain voltage amplitude is thus V_{dd}.

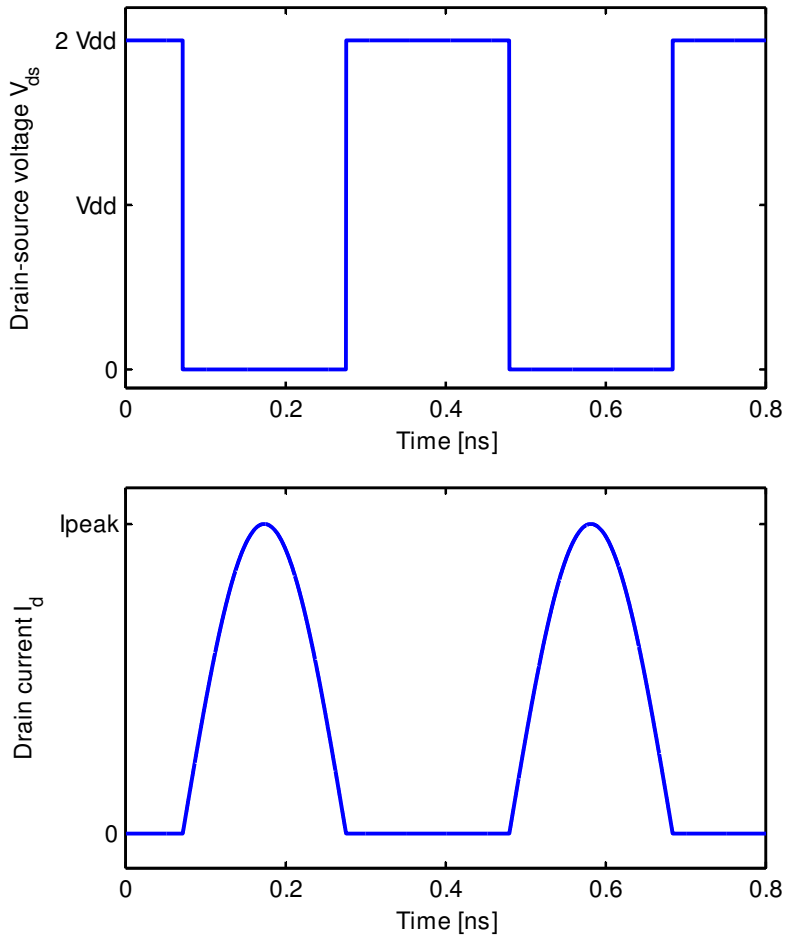


FIGURE 4.1 IDEAL CLASS F VOLTAGE AND CURRENT WAVEFORMS

Using Fourier transformation [3], the fundamental coefficient of a square wave is found to be $\frac{4}{\pi}$. The fundamental voltage amplitude is thus

$$V_{fund} = \frac{4}{\pi} \cdot V_{dd} \,. \tag{4.8}$$

As only the fundamental component of the drain voltage reaches the load, the output power is

$$P_{out} = \frac{V_{fund}^2}{2R} = \frac{\left(\frac{4}{\pi} \cdot V_{dd}\right)^2}{2R}, \tag{4.9}$$

where R is the impedance seen from the drain. The peak drain current [1] is

$$I_{peak} = \frac{2 \cdot \frac{4}{\pi} \cdot V_{dd}}{R}. \qquad (4.10)$$

The load impedance of the output filter also ensures that the drain current is sinusoid for the half period that the switch is conducting. This results in the half-sinusoid current waveform shown in Figure 4.1.

4.2 Discrete solution

An ideal termination of all harmonics may not be feasible. A number of resonant filters may replace the transmission line [6], each filter reflecting one harmonic (a discrete solution). A discrete solution with a single filter reflecting the third harmonic is shown in Figure 4.2.

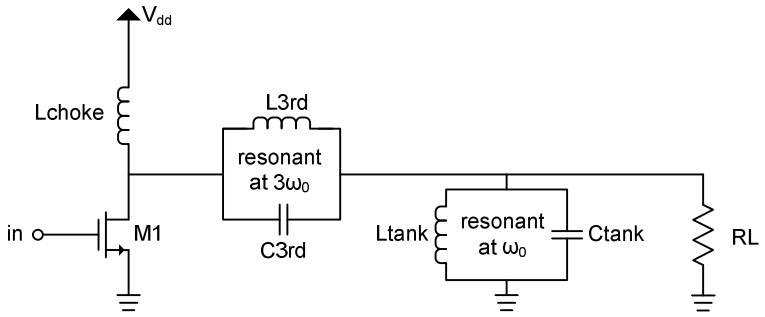


FIGURE 4.2 CLASS F PA WITH DISCRETE 3RD HARMONIC FILTER

Adding odd harmonics in the drain voltage will approach the signal to a square wave. By minimising the time of simultaneous current through and voltage across the transistor, this helps increase efficiency.

TABLE 4.1 OPTIMAL FOURIER COEFFICIENTS AND MAXIMUM THEORETICAL EFFICIENCIES OF CLASS F PAS WITH IDEAL DISCRETE FILTERS

	V_{fund}	V_3	V_5	Max theoretical efficiency η
No harmonics present	1			78.5 %
3rd harmonic present	1.1547	0.1667		90.7 %
3rd and 5th harmonics present	1.2071	0.2323	0.0607	94.8 %

The optimal Fourier coefficients and the maximum theoretical efficiencies calculated in [13] for two discrete filter solutions are presented in Table 4.1. A PA with no reflecting filter is listed for reference. A half-sinusoid drain current is assumed. The corresponding waveforms are shown in Figure 4.3.

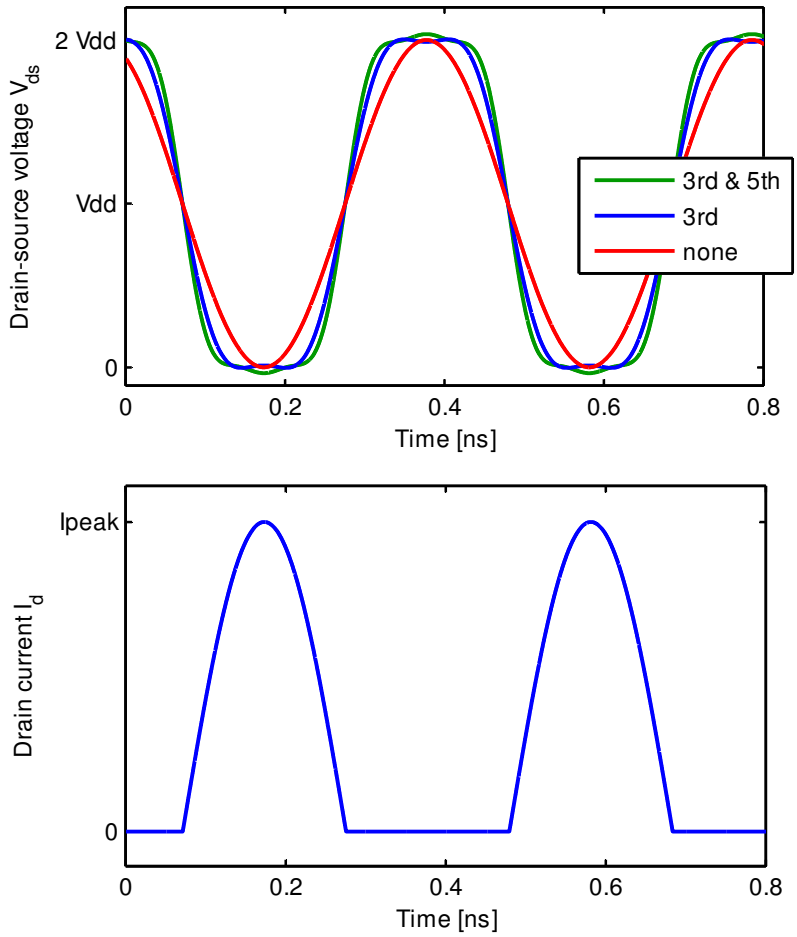


FIGURE 4.3 DRAIN VOLTAGE AND CURRENT WAVEFORMS CONTAINING VARIOUS NUMBERS OF ODD HARMONICS

It is seen that a class F PA with only the fundamental frequency present has the same theoretical efficiency as a class B PA [1], as no shaping of the drain voltage is done. The addition of a filter reflecting the fifth harmonic increases the theoretical efficiency by 4.1 % points compared to only reflecting the third harmonic. As all practical filters have a small loss outside the stop-band, the fundamental frequency will be increasingly attenuated with the addition of resonant filters. This limits the optimal number of filters [1].

5 Implementation challenges and limitations

When attempting to integrate a class F PA in CMOS, several challenges occur. Some are related to feasibility, while others are related to cost. The main limitations and the measures taken to overcome the challenges are described below.

5.1 Break-down voltage

One of the most severe limitations in integrated CMOS is the break-down voltage. If the voltage across any two nodes of a transistor exceeds the limit, a destructive break-down may occur. In the 0.18 μm process used in this design, the limit is 2 V. In ideal class F operation, with a circuit as shown in Figure 3.4, the drain voltage has a peak value of two times the supply voltage V_{dd}. This is due to the inductive load, which ensures a DC-level of V_{dd} at the drain. Using the global supply voltage V_{glob} of 1.8 V and connecting the source to ground, the peak drain voltage of 3.6 V will exceed the break-down limit. Three popular solutions to this problem are discussed below; the use of a high voltage transistor, the cascode topology and a lowered supply voltage.

5.1.1 High voltage transistor

A high voltage transistor is available in the process. It has a thicker gate oxide layer, and the minimum length is 0.35 μm. This raises the break-down limit to 3.6 V. It also increases the switching time of the transistor, which is important in any switching amplifier. The gain is also lower than for a low voltage transistor. High gain is needed in this PA, so the use of high voltage transistors is not seen as a good solution to the break-down problem in this PA.

5.1.2 Cascode topology

A telescopic cascode topology is shown in Figure 5.1. It consists of two stacked transistors, and is able to accommodate a full theoretical voltage swing from 0 V to $2 \cdot V_{dd}$ with a large V_{dd} without breaking down. The DC voltage at the source of the top transistor is largely set by the voltage at the gate of the same transistor. The RF swing at this node is limited by the low load impedance seen by the bottom transistor.

Assuming a constant bias voltage equal to V_{dd} at the gate of the top transistor, the source voltage will be approximately constant at this level minus an offset. This offset is ideally equal to the threshold voltage of the transistor, giving a source voltage of $V_{dd} - V_{th}$. The maximum voltage across two terminals of the transistor is thus

$$V_{\max} = 2 \cdot V_{dd} - \left(V_{dd} - V_{th}\right) = V_{dd} + V_{th} \tag{5.1}$$

The supply voltage is therefore limited to 2 V – V_{th} ≈ 1.5 V.

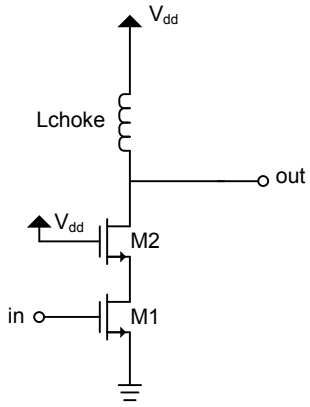


FIGURE 5.1 TELESCOPIC CASCODE TOPOLOGY

The drain node of the bottom transistor will be at the same level as the source of the top transistor. No voltage will thus exceed 2 V across the bottom transistor. The bulk nodes of each transistor are assumed to be connected to the source nodes. The top transistor would have to be placed in a p-well in a deep n-well to allow another bulk potential than ground.

5.1.3 Lowered supply voltage

The cascode topology is a complicating factor in the design. A less complicated way of avoiding the problem of break-down is to lower the supply voltage until no voltage exceeds the limit. This will not affect the achievable efficiency, as it depends on the voltage and current waveforms and not their peak values. However, a loss of efficiency due to the conversion from the global supply voltage V_{glob} of 1.8 V has to be considered.

The supply voltage V_{dd} used for the amplifier stages is in this design set to 0.9 V. This is half the global supply voltage V_{glob} of 1.8 V. This gives a reasonable margin between the theoretical peak voltage and the break-down limit. A simple resistive conversion would mean that half the energy drawn from the global power supply is lost in conversion. Conversion loss can be limited at a cost increase, by using a switching regulator. An example is the Texas Instruments TPS62001 regulator that converts any voltage between 2 V and 5.5 V to 0.9 V with up to 95 % efficiency [15]. The use of a lowered supply voltage would then only reduce the total *PAE* of the system by 5 %.

A switching regulator can introduce additional noise into the circuit. If the switching frequency is constant, this can add a spurious frequency to the output signal. The noise from the regulator can be reduced by spreading the switching frequency or with other techniques trading efficiency.

Lowering the supply voltage is considered the best solution to avoiding break-down in this PA design.

5.2 Output filter

The load network can be implemented either internally or externally on a Printed Circuit Board (PCB). An internal filter can be more easily interfaced with the amplifier output. However, integrated passive components are sensitive to process variations and a may introduce additional uncertainty. An external filter is easier to revise. It can thus be designed to match the actual Integrated Circuit (IC) after production, and to some extent be tuned to absorb unpredicted effects on the IC due to inaccurate models or design errors. The output filter is therefore realised externally in this design.

All physical passive components have a Self-Resonant Frequency (*SRF*), above which the component no longer operates as expected. For an inductor, this will occur when the reactance of the parasitic capacitance of the package is comparable to the reactance of the inductor. The inductor will then act as an LCR-circuit where the inductance L cannot be considered alone. Most suppliers of passive components do not provide models or scattering parameter (s-parameter) files that are valid at or above the *SRF*.

High impedance termination of the third harmonic and low impedance termination of the second harmonic are the two most vital properties of the output filter to ensure class F operation. Well-defined operation at frequencies at least up to the third harmonic frequency $f_3 \approx 7.5$ GHz is therefore required for components used in the output filter providing these impedances.

Surface-mounted components can be found with $SRF > 7.5$ GHz in certain low values and in very small packages. However, a layout using surface-mounted components at this frequency will be highly susceptible to variations in placement, soldering etc.

A microstrip filter is a filter made solely by metal strips separated from a ground plane by a dielectric medium. It is defined by its structure, and therefore has a well-defined and predictable frequency response up to very high frequencies. It consumes more PCB area, but costs less than a filter realised by surface-mounted components. It is therefore used in this design. If the area is more critical than cost, a substrate with higher relative dielectric constant ε_r can be used. The microstrip filter dimensions will then be reduced.

5.3 Reference current

Bias currents are quite easily regenerated and multiplied in CMOS, using a combination of PMOS and NMOS current mirrors. The challenge is creating a stable bias current that is independent of temperature and supply voltage. One possibility is to use a parasitic bipolar transistor to generate a bandgap voltage reference that depends mostly on physical constants [1]. This is considered outside the scope of this work, so a constant bias current of 10 μA is in the following assumed to be available.

5.4 Modelling of physical properties

All real circuit components in CMOS have some non-ideal parasitic properties. These properties have to be taken into account when designing, by creating appropriate models that can be simulated. The accuracy of these models is vital to the successful design of RF integrated circuits. The exact model values are often company confidential, as they are found by experience and represent a competition advantage.

5.4.1 RF transistors

The RF transistor models provided by the foundry are used. These are spice models generated to fit results that have been measured on produced devices. Process variations are modelled through the use of corner simulations. All process variations are combined to create two extreme cases for the transistors; fast and slow. Combinations of fast NMOS and slow PMOS and vice versa are also available. In addition to the two extreme cases, a typical model representing the expected behaviour is available.

5.4.2 Integrated passive components

Resistors, capacitors and inductors are also modelled by the foundry. The validity of the models depends on the layout of the components, which is therefore done as described in the documents provided by the foundry. As for the transistors, the passive components can be described by a typical, fast or slow model.

5.4.3 Package

A Quad Flat No-lead (QFN) package is assumed. The connections are realised by a bond wire connecting an on-chip bonding pad to a pin in the package. The bond wires are mainly inductive, while the bonding pads are mainly capacitive. The model used for the package is shown in Figure 5.2.

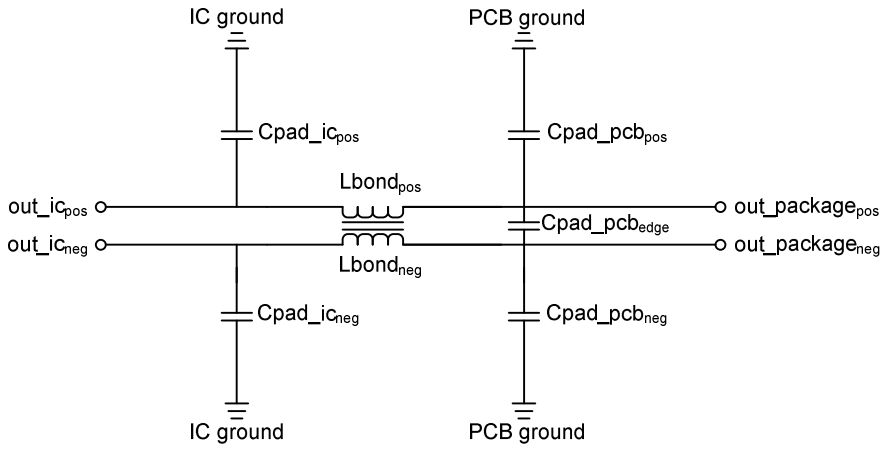


FIGURE 5.2 PACKAGE MODEL

The on-chip bonding pads are modelled as ideal capacitors to IC ground. The bond wires are modelled as ideal inductors. The package pins are modelled as ideal capacitors to PCB ground. To model the proximity of the two RF outputs, a mutual inductance and a capacitor are added between the two paths. The proximity of bond wires for power and ground is not modelled, as this depends on the placement of the other modules on the chip.

5.4.4 PCB

The PCB material used for external components such as the microstrip filter is FR4. The important parameters are the physical dimensions, the dielectric constant and the loss tangent. The parameters used are shown in Table 5.1.

TABLE 5.1 PCB PARAMETERS

Dielectric thickness *h*	800 µm
Copper thickness *t*	35 µm
Relative dielectric constant ε_r	4.25
Loss tangent *Tand*	0.025

There are no models for variations in fabrication or resistance against moist, aging etc.

5.4.5 Load

The PA is designed to match a differential antenna with an input impedance of 50 Ω. The load model used in simulations is shown in Figure 5.3.

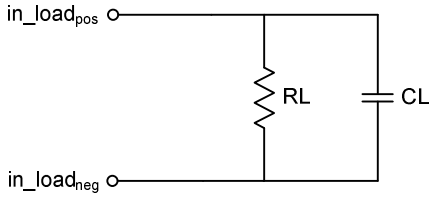


FIGURE 5.3 LOAD MODEL

The capacitance in parallel with the resistor accounts for the capacitive effect of the antenna at frequencies above the fundamental frequency. As it is small, its reactance does not have a large effect at the fundamental frequency.

6 Schematic design

A class F PA can be divided into three main blocks, as shown in Figure 6.1. The main amplifier converts DC power from the power supply to RF power with high efficiency. The main amplifier does however rely on a driver supplying sufficient input amplitude to drive the transistor as a switch. The third block is the output filter, which is the load seen by the main amplifier. It transfers the output power from the IC to the antenna. Without the appropriate load at the drain of the output transistor, the PA will not be in class F operation. The concurrent design of these three blocks is therefore vital to achieve the anticipated behaviour.

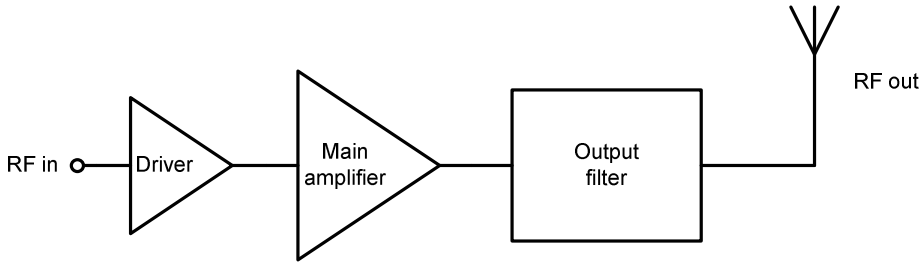


FIGURE 6.1 CLASS F PA BLOCK SCHEMATIC

In addition to the three blocks of the RF signal path, a fourth block is needed to provide an appropriate bias to each amplifier stage.

The design has been optimized for *PAE*, while always complying with the specifications. The main goal is an output power of 10 dBm with a *PAE* as high as possible. Parasitics and other non-ideal behaviour are known to lower the final output power. The PA is therefore initially designed for an output power of 13 dBm. This gives a reasonable margin to allow for reduction of output power due to added parasitics and modifications to ensure stability.

A differential architecture has been used in order to reduce even-order distortion, such as noise on the power supply or ground nodes. The virtual ground node shared by the two parts of a differential amplifier also reduces the effects of a non-ideal ground when in normal operation.

6.1 Driver

The only function of the driver is to provide a voltage that is sufficient to drive the output stage transistor as a switch. The specified differential input voltage is 400 mV peak-to-peak. This corresponds to 100 mV amplitude on each input. The typical input capacitance is specified to 100 fF on each input.

The driver can be seen as a separate PA, so the driver stage efficiency can be increased by the use of a switching class. This would however require an internal filter or extra pins to interface a second external filter. As the power consumed by the driver is small compared to the total PA power consumption, only a small

increase of total PA efficiency is attainable. The considerable increase of complexity and cost can therefore not be justified.

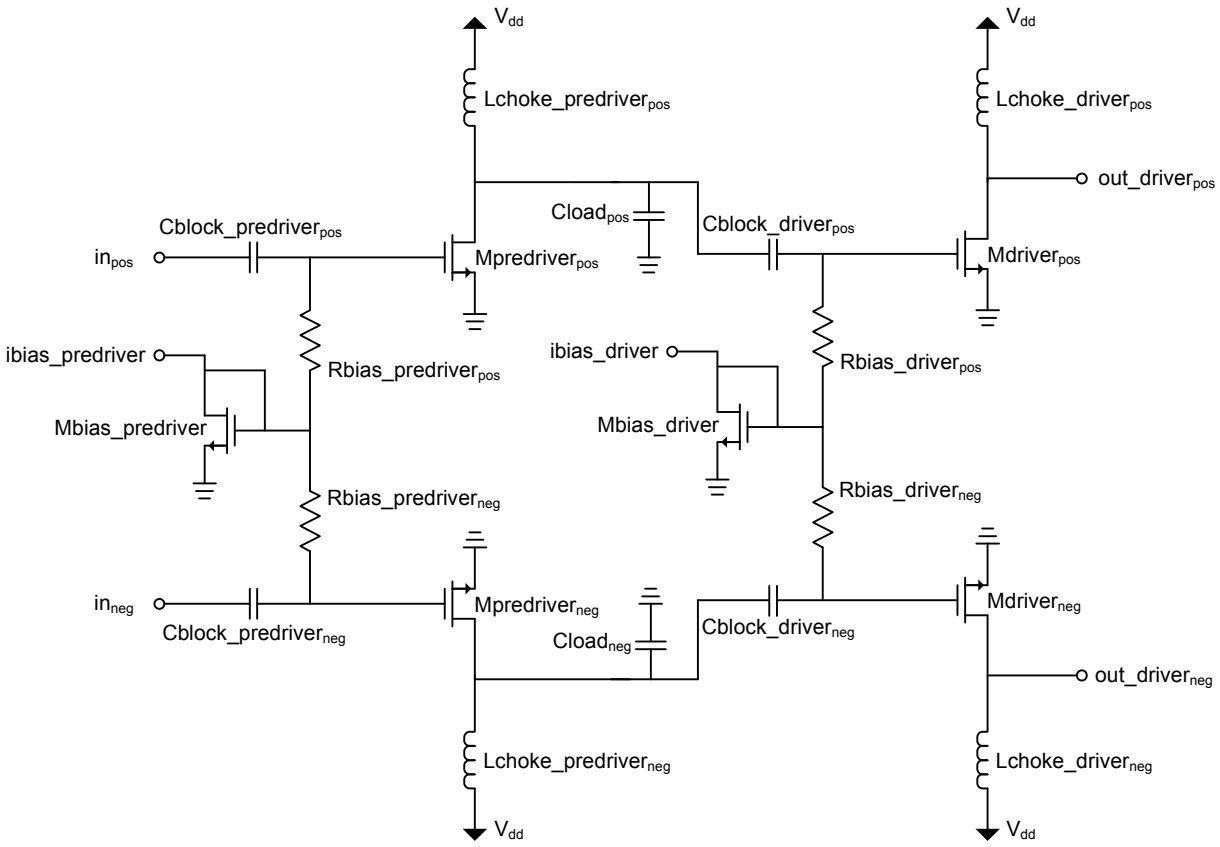


FIGURE 6.2 DRIVER STAGES SCHEMATIC

To drive the output stage as a switch, the output amplitude from the driver should be as large as possible, limited only by the break-down voltage. This need for high voltage gain has led to the design of a driver divided into two stages. The driver architecture is shown in Figure 6.2.

6.1.1 Inductive load

To maximize the voltage gain, an inductive load is used on both stages. An inductive load allows higher output signal amplitude than other loads, which makes the driver better suited for driving the output stage as a switch. The size of the inductors is chosen such that the LC-circuit consisting of the inductor and the total capacitance of the connected drain node has a resonant frequency corresponding to the fundamental frequency f_0 = 2.45 GHz.

The capacitance of the drain node consists mainly of the gate capacitance of the next stage in series with the DC-blocking capacitor connecting two stages. The DC-blocking capacitor is made large enough to avoid a large voltage drop across it due to voltage division, so the total capacitance is approximately equal to the gate capacitance of the next stage.

As shown in Figure 6.3, there exist both differential and single-ended inductors. The single-ended inductor has two inputs only. The differential inductor has, in addition to the two inputs, a centre tap for a common connection. The differential inductor is therefore well suited to the use in this PA, where the two drains of a differential amplifier stage should be connected to a common node, i.e. V_{dd}. A large area reduction is obtained by the use of one inductor per stage instead of two.

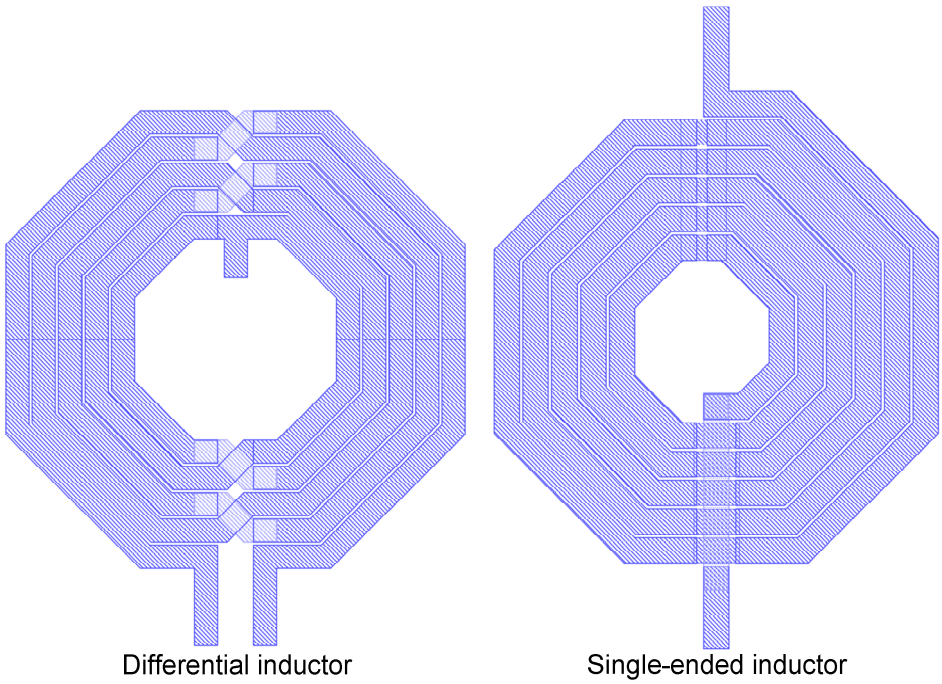


FIGURE 6.3 DIFFERENTIAL AND SINGLE-ENDED INDUCTOR IMPLEMENTATIONS

Simulations show, however, that the needed inductance of a differential inductor is much larger than that of the single-ended, to obtain the same performance. The decreased performance is due to a large capacitive coupling between the two input nodes. This results from the parallel routing of the two signals, where, in fact, the two neighbouring paths have the largest possible voltage difference.

This reduction of performance requires the use of a much larger inductance when using differential inductors than when using single-ended inductors. The resulting area difference between one differential inductor and two single-ended inductors is small, but in favour of single-ended inductors.

The drain node of the driver stage has been found to have a total capacitance *Cdrain_driver* = 680 fF. The required inductance for resonance at f_0 = 2.45 GHz can be found from the equation

$$f_o = \frac{1}{2\pi \cdot \sqrt{L \cdot C}}. \qquad (6.1)$$

Rearranging for *L* gives

$$Lchoke\_driver = \frac{1}{Cdrain\_driver \cdot (2\pi \cdot f_0)^2} = 6.2\,\text{nH}\,. \qquad (6.2)$$

In the case of the pre-driver stage, the gate capacitance of the next stage is quite small, leading to a total drain node capacitance *Cdrain_predriver* = 390 fF. Resonance at the fundamental frequency would require an inductor of 10.8 nH, occupying a large area. The required inductance has therefore been decreased by adding an additional capacitor *Cload* between the drain node and ground.

An inductance of 5.2 nH has been used. The required extra capacitance can then be found using (6.1) where *C* is replaced by *Cdrain_predriver* + *Cload*, so that

$$Cload = \frac{1}{Lchoke\_predriver \cdot (2\pi \cdot f_0)^2} - Cdrain\_predriver = 420\,\text{fF}\,. \qquad (6.3)$$

This area of this capacitor is considerably smaller than the reduction of inductor area, so the total cost is lowered.

6.1.2 Dimensions

The length *L* is set to the minimum of 0.18 µm in all transistors. The aim of the two driver stages is to provide the required gain with the lowest possible current consumption. The width *W* of the first driver stage is therefore set as large as possible. Provided that the transistor stays in the active region, the width is limited by the specified input capacitance.

A starting point for dimensioning the width *W* is found from the basic relation of the drain current I_d of a transistor to its gate-source voltage V_{gs} [14]. In its most basic form it depends on the dimensions and some process parameters, and is given by

$$I_d = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{gs} - V_{th})^2, \qquad (6.4)$$

where μ_n is the electron mobility in the channel, C_{ox} is the gate capacitance per unit area and V_{th} is the threshold voltage of the transistor. For a given DC operating point, i.e. a bias current and a DC gate-source voltage, the required width can thus be found.

A large second stage gives a large gain, but is also a heavy load for the first stage. A reasonable distribution of voltage gain between the two stages is also important. If the gain of the first stage is too large, the second stage can be driven into heavy compression resulting in an unnecessary increase in distortion. The width of the second driver stage is thus determined as a compromise between these factors, with an aim of low total current consumption.

6.1.3 Bias

The bias current of the RF transistors is set by means of a current mirror. Using the architecture in Figure 6.4, the gate voltage of the bias transistor *Mbias* will be what is required to accommodate the drain current imposed through the input *ibias*. This voltage is copied to the gate of the RF transistor through the bias resistor *Rbias*. The resistance has to be much larger that the input impedance of the amplifying transistor, such that only a negligible part of the RF current is lost to the bias network. RF distortion in the bias network can also be a source of instability.

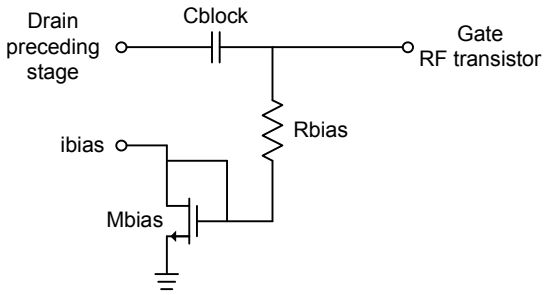


FIGURE 6.4 BIASING OF A PA STAGE

Assuming equal sizes and keeping both transistors in the active region, the drain currents of the two transistors will ideally be equal. A difference in size will result in a difference of current, where the current ratio equals the size ratio. The bias current will vary little with process variations, as the same variations will apply to both transistors in the mirror.

A DC blocking capacitor separates the DC voltage of the drain of the preceding stage from the bias voltage, allowing a DC voltage difference. The current *ibias* feeding the bias transistor of each stage is generated from the global 10 μA reference current.

The current mirror providing the bias voltage is shared between the positive and the negative parts. This saves area, and also ensures equal bias voltage for both transistors. To ensure good matching, the width is set equal to that of the amplifying transistors and the number of fingers is set to 2. The bias current of the amplifying transistors is thus that of the bias transistor multiplied by a factor equal to half the number of fingers of the amplifying transistors.

The bias current controls the gain of each driver stage. This can be used to compensate loss, and if small variations of output power are of interest.

6.2 Main amplifier

The output stage of the PA is realised as shown in Figure 6.5. The circuit is equal to one driver stage, but the output stage is directly connected to the external output filter through the package model described in chapter 5.

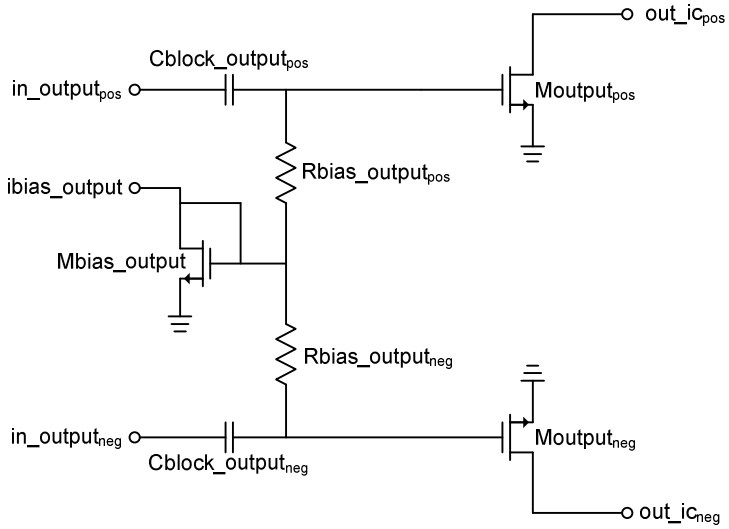


FIGURE 6.5 OUTPUT STAGE SCHEMATIC

The DC voltage level at the drain of the RF transistors is set by an external power supply V_{dd_ext} through the output filter. This enables a different supply voltage than that of the driver stages. The supply voltage should be adjusted so that the drain voltage is at its most effective, i.e. with a peak value somewhat below the break-down voltage.

6.2.1 Dimensions

Minimum length transistors are used to achieve steep edges. The width is found as a compromise between low gate capacitance for the preceding stage and low on-resistance for the switch. Low on-resistance increases the *PAE*, as the voltage across the transistor when conducting is lowered.

6.2.2 Bias

Biasing circuitry is provided as for the driver stages.

The bias voltage is set such that the current pulses have a width of 50 % of the period. For an ideal transistor used as a switch, the optimal bias voltage is equal to the threshold voltage of the transistor. However, as the conductivity of the switching transistor is low when it starts conducting, the desired current pulse width is obtained with a higher bias.

A bias current of 5 mA has been found to yield a current pulse of approximately 50 % width and the highest *PAE*.

6.3 Output filter

The microstrip filter connected to each of the RF outputs consists of four pieces of microstrip transmission line as shown in Figure 6.6. Two of them connect the RF output to the load, while the other two are perpendicular to the first two ending in open circuits. One of them is long and thin acting as an inductor to ground, while the other is short and wide acting as a capacitor to ground [16]. These two lines constitute an LC-filter resonant at the fundamental frequency f_0. To match the desired drain impedance to the antenna impedance, a tapered line is used. A tapered line has a wider end than start, so that the impedance seen at the start is higher than the impedance seen at the end.

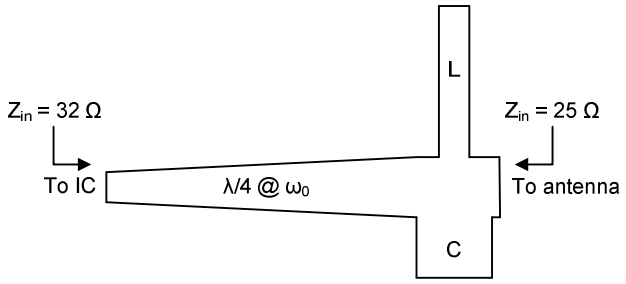


FIGURE 6.6 CONCEPTUAL MICROSTRIP FILTER LAYOUT

The microstrip filter is designed and optimised in Microwave Office. The software package includes empirical models of microstrip lines. Lines that are terminated in open circuits have models that incorporate the end effect. A cross model is used at the intersection of the different lines. A short line is placed between the filter and the output port to ensure that the cross is matched to the correct line width. The complete circuit schematic from Microwave Office can be found in appendix A.

6.3.1 Optimal drain impedance

As the antenna is modelled as a differential load of 50 Ω, the load seen by each output is 25 Ω. To minimize the loss of energy, the impedance of the end of the microstrip filter is matched to 25 Ω. Using the Microwave Office tool TXLine and the PCB parameters reported in chapter 5, this translates to a metal width of 4238 μm.

The optimal drain impedance seen by the transistor at the fundamental frequency can be found from the required output power of the PA by using (4.9).

The available peak-to-peak voltage swing of the drain voltage is assumed to range from 0.2 V to 1.6 V. It does not range from 0 to $2 \cdot V_{dd}$ because of the non-ideal switch with non-zero on-resistance and non-infinite off-resistance. The drain voltage amplitude V_{drain} is thus 0.7 V. The positive and negative parts of the output stage are to deliver an output power of 10 mW each to combine to 13 dBm. 13 dBm gives a reasonable margin to the target output power of 10 dBm, as described above.

Using the optimal amplitude of the fundamental component of the drain voltage from Table 4.1, the optimal drain impedance is found as

$$R = \frac{(1.1547 \cdot V_{drain})^2}{2 \cdot P_{out}} = \frac{(1.1547 \cdot 0.7)^2}{2 \cdot 0.010} = 32\,\Omega\,. \tag{6.5}$$

The output filter will thus be designed to provide a drain impedance of 32 Ω.

6.3.2 Reflection coefficients at harmonic frequencies

The length of the transmission line is set to correspond to a quarter of a wavelength at 2.45 GHz. In theory this should reflect all odd harmonics. In practice it is found to be impossible. Dispersion and loss in the transmission line alters the behaviour such that the length that is seen as three quarters of a wavelength at the third harmonic is not seen as five quarters of a wavelength at the fifth harmonic. Therefore, only one harmonic can be efficiently reflected. Low harmonics are most effective [17], so the filter is designed to reflect the third harmonic and short-circuit the second harmonic.

This behaviour corresponds to the discrete solution in Figure 4.2. However, as a series inductor is not easily implemented in microstrip, a quarter-wave line solution as shown in Figure 3.4 is used. For the reasons explained above, it is optimised for reflecting the third harmonic only, and not for reflecting all odd harmonics.

Two different views of the output filter is used; one for optimisation and tuning, and the other for extraction of s-parameters. The difference is that when optimising the output filter, the package model is included in the simulations. Port 1 corresponds to the inside of the package model, at the drain of the output transistor. Port 2 is the connection to the load. When extracting s-parameters, only the microstrip filter is included. Port 1 is then on the input of the microstrip filter, while port 2 is still the connection to the load.

The s-parameter S_{11} visualised in a Smith chart is the main view used for optimisation. S_{11} relates the reflected voltage wave at port 1 V_1^- to the incident voltage wave at the same port V_1^+, when all other ports are terminated in their characteristic frequency [18]. S_{11} is defined as

$$S_{11} = \frac{V_1^-}{V_1^+}\,. \tag{6.6}$$

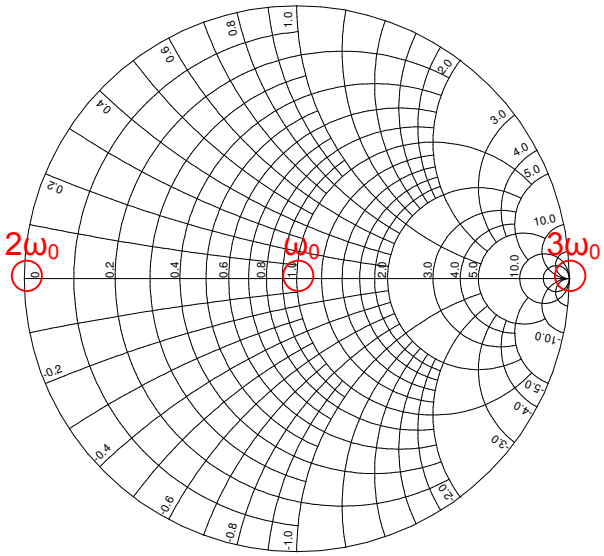


FIGURE 6.7 IDEAL OUTPUT FILTER REFLECTION AT THE DRAIN (REF 32 Ω)

The goal is to approach the points for ideal operation shown in Figure 6.7. Good match ($S_{11} \approx 0$) at the fundamental frequency, high impedance ($S_{11} \rightarrow 1$) at the third harmonic and low impedance ($S_{11} \rightarrow -1$) at the second harmonic are three equally important goals. The reference impedance for the Smith chart is set to 32 Ω. A perfect match in the Smith chart then means that the drain sees the desired impedance of 32 Ω, and the package model is neutralised as much as possible. The four free parameters that can be tuned to achieve this load impedance are the lengths of the three main microstrip lines and the start width of the quarter-wave line. The obtained reflection coefficients visualised in a Smith chart is found in appendix C.

6.3.3 Differential output filter

The output filter described above is duplicated to form the differential output filter connected to the PA. There is also a connection to the external power supply V_{dd_ext} through two inductors. The inductors are large enough not to noticeably alter the match at the fundamental frequency and above, and with an *SRF* higher than the third harmonic.

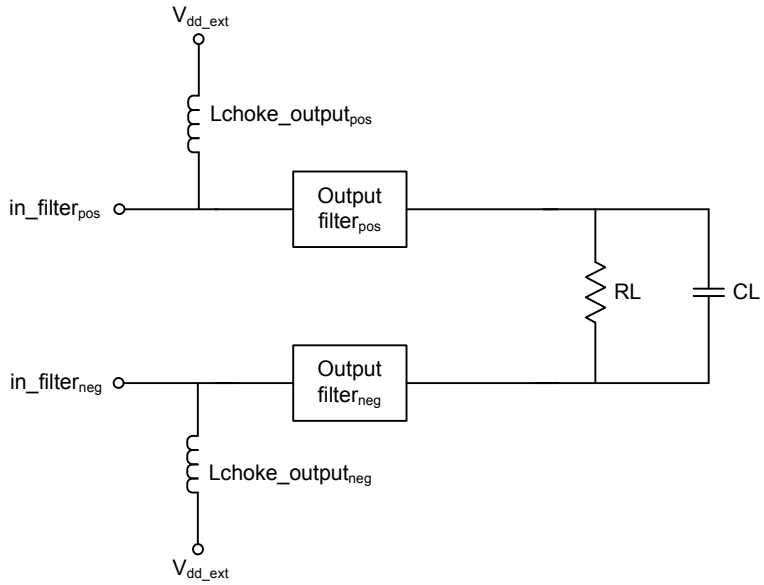


FIGURE 6.8 DIFFERENTIAL OUTPUT FILTER CONNECTION

The connection used is shown in Figure 6.8. In contrast to the ideal class F PA circuit described in chapter 3, this output stage does not have a DC-blocking capacitor. As a differential architecture with two identical parts is used, the DC voltage level on each side of the differential load resistor will be equal. The lack of a DC-blocking capacitor results in a DC level of V_{dd_ext} on both sides of the load. As no DC current traverses the load, no DC power is dissipated in the load.

6.4 Bias current generation

The global bias current is fed into an NMOS current mirror to permit regeneration and multiplication. To increase the available range of current multiplication factors, a PMOS current mirror is added. It is connected between the input current mirror and the current mirror biasing each stage, as shown in Figure 6.9.

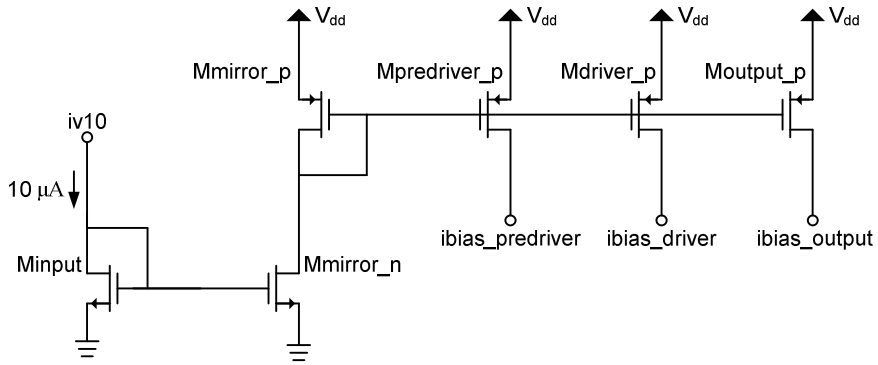


FIGURE 6.9 BIAS CURRENT GENERATION

The final bias current of the RF transistors is determined by the product of the different width ratios. As an example, the bias current $Ibias_{Moutput}$ of the output stage is found as

$$Ibias_{Moutput} = \frac{NF_{Mmirror\_n}}{NF_{Minput}} \cdot \frac{NF_{Moutput\_p}}{NF_{Mmirror\_p}} \cdot \frac{NF_{Moutput}}{NF_{Mbias\_output}} \cdot 10\,\mu A\,, \qquad (6.7)$$

where $NF_{Mmirror\_n}$ is the number of fingers of transistor *Mmirror_n* etc. The width of each finger is equal in both transistors in a mirror. Some deviation from the ideal output current is seen due to different drain-source voltage V_{ds}. To minimize the power dissipation, the currents should be kept to a minimum in the early stages. The width ratio of the first mirror will therefore be low.

6.4.1 Bias block supply voltage

The connection of the bias block to the output stage is shown in Figure 6.10. An NMOS current mirror is fed with a current provided by the PMOS in the bias block. The lowered supply voltage V_{dd} may be troublesome for this connection.

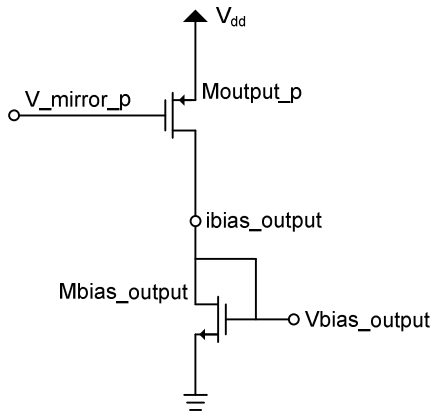


FIGURE 6.10 CONNECTION OF THE BIAS BLOCK TO THE OUTPUT STAGE

The drain and gate voltages of the NMOS transistor are equal, and decided by the combination of drain current and transistor width. For the bias currents of interest, the gate voltage *Vbias_output* has been found to vary between the threshold voltage $V_{th} \approx 0.5$ V and approximately 0.8 V. The drain-source voltage of the PMOS transistor Vds_p is

$$Vds_p = Vbias\_output - V_{dd} \qquad (6.8)$$

With a supply voltage $V_{dd} = 0.9$ V, the PMOS drain-source voltage is limited to a range of -0.1 V to -0.4 V. If it raises above the effective gate-source voltage V_{eff} defined by

$$V_{eff} = V_{gs} - V_{th}\,, \qquad (6.9)$$

the transistor exits the active region and enters the linear region [14]. As a current mirror relies on all transistors operating in the active region, this change of region

introduces an error in the multiplication of currents. The PA performance will then largely depend on small voltage variations in the bias block.

To counteract this varying behaviour, the bias block uses the global supply voltage V_{glob} of 1.8 V. This will ensure that the transistors are kept in the active region for the currents of interest, but will not noticeably influence the typical output currents of the block.

6.5 A note on simulations

The circuit schematic drawn in Design Architect is exported to an Eldo netlist for simulation. Two main simulation algorithms are available. The transient analysis is the traditional approach. First, a DC operating point is found using the DC sources in the netlist. Then the time is incremented by a small value, before recalculating the voltage of all nodes. The calculations are faster if the deviation from the DC operating point is small.

The transient simulation is useful for an investigation of the response over time of a circuit. However, the performance of an RF module such as a PA is defined by the operation after start-up when subject to a stable periodic input, called its steady state. The steady state is reached when all node voltages are periodic. Long start-up times before reaching the steady state and small time steps required to improve accuracy and resolution of the result waveforms lead to long and heavy simulations.

An alternative to the transient simulation is the steady-state simulation, provided by the Eldo RF option. It uses a different algorithm based on identifying a distribution of power in the steady state. The power is distributed between the different frequency components resulting from a Fourier analysis of the periodic node voltages. In an RF system, there is typically a carrier wave frequency chosen as the fundamental frequency of the steady-state simulation. The harmonic power can be considerable, but is normally limited to the lower harmonics. The higher harmonics are attenuated by the inherent filtering of the circuit elements.

The accuracy of a steady-state simulation depends on the number of harmonics simulated. In a linear amplifier where the node voltages are mostly sinusoidal, a low number of harmonics is needed to yield accurate results. When simulating more non-linear circuits such as a class F PA, there is considerable power in the harmonic frequencies. If too few harmonics are calculated in the simulation, the result may be inaccurate. It is also possible that the simulation engine is unable to converge, i.e. finding a steady state.

Including more harmonics in a steady-state simulation is like decreasing the maximum time step in transient simulation. The accuracy is increased, but also the simulation time. To determine the needed number of harmonics, simulations using an increasing number of harmonics should be compared. When the addition of harmonics only has a minor effect of the results, the increased simulation time cannot be justified. This investigation of required number of harmonics should be

done repeatedly during the design, as the required number could change when the circuit is expanded or otherwise altered.

6.5.1 Use of s-parameter files

When simulating the entire PA, the output filter has been modelled by an s-parameter file generated by Microwave Office. An s-parameter file defines the frequency response of any passive component, by use of the scattering parameters. Eldo accepts use of blocks defined by s-parameters.

The s-parameter file is defined for a range of frequency points. For frequencies outside this range Eldo extrapolates the curve defined by the points in the file. This is not always correct, and an extrapolation error at DC can result in serious errors. To ensure correct behaviour by the simulator, a DC biasing network is added around the s-parameter block. The setup for the output filter is shown in Figure 6.11.

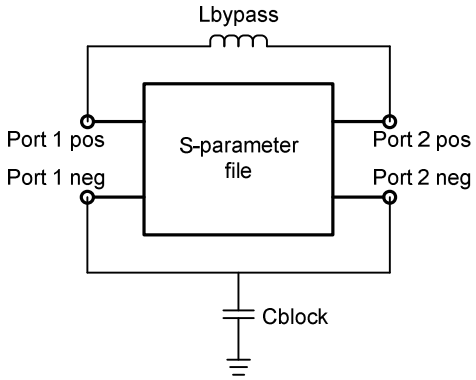


FIGURE 6.11 SIMULATION SETUP OF S-PARAMETER FILES

The inductor *Lbypass* ensures that the correct behaviour of the output filter, i.e. short circuit, is used for DC calculations. It is set large enough not to alter the circuit behaviour at higher frequencies. Similarly, the negative ports that correspond to the ground plane of the PCB are connected to ground through a large capacitor. This prevents any DC current from flowing between the positive ports and ground through the s-parameter block, and corresponds to the true DC properties of a microstrip filter above a ground plane.

7 Stabilisation

The PA initially designed was found to be unstable. Several approaches exist for stabilising an unstable amplifier. Some approaches and their use in this design are discussed below.

Instability occurs when there is a loop with a loop gain larger than 1, also known as positive feedback. The instability source can be intentional loops with larger gain or another phase delay than anticipated or non-intentional loops created by parasitic effects. An example of a non-intentional loop can be feedback from one amplifier stage to another through the non-ideal power or ground connection.

The main source of feedback in this amplifier has been found to be the parasitic gate-drain capacitance C_{gd} of the output stage. This capacitance couples any oscillation on the drain to the gate. This oscillation is then amplified back to the drain, creating a loop.

7.1 Reduction of parasitics

The size of the gate-drain capacitance strongly depends on the dimensions of the transistor. The width of the output transistor was initially optimised for efficiency. Increasing the width lowers the channel resistance, which leads to a lower voltage across the transistor when it is conducting. The output power and the *PAE* as a function of transistor width (schematic simulation) are shown in Figure 7.1. An increase in width does however also increase the gate-drain coupling which has shown to destabilise the PA.

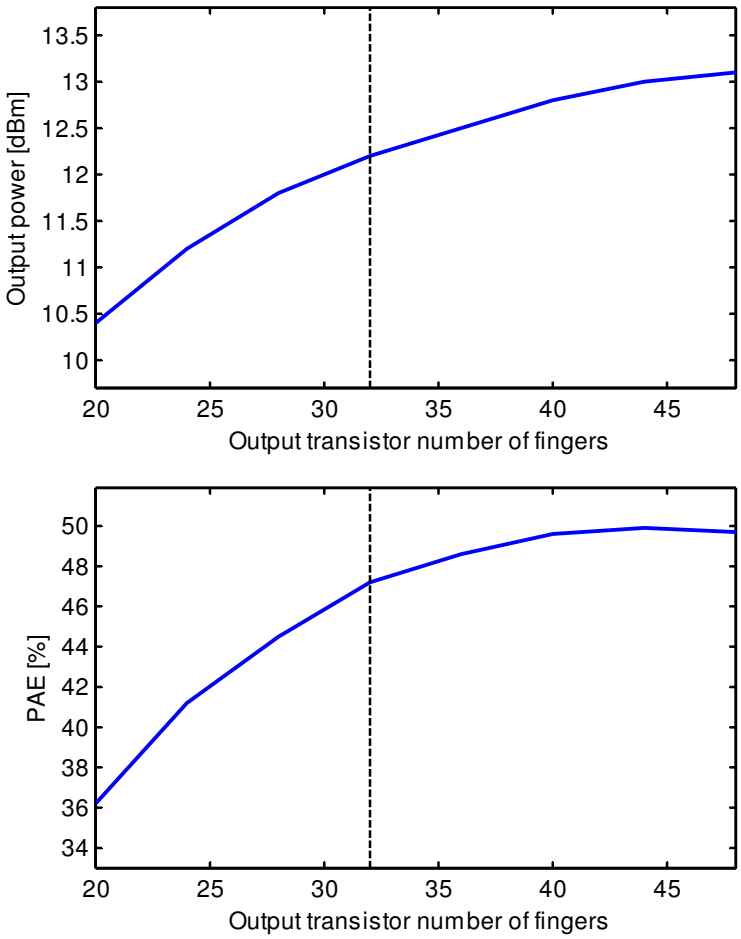


FIGURE 7.1 OUTPUT POWER AND PAE AS A FUNCTION OF OUTPUT TRANSISTOR NUMBER OF FINGERS

It is seen from Figure 7.1 that both the output power and the PAE drop more rapidly below a critical width of 32 fingers. The final number of fingers is therefore set to 32, and further stabilisation is done by other means. The exact transistor dimensions can be found in appendix A.

7.2 Negative resistance

Oscillations in a PA may be due to an input impedance with a negative resistive component [1]. The oscillations can therefore be reduced or even removed by introducing additional resistive impedance at the input. A resistance in series with the gate helps keeping the resistive part of the input impedance positive. Oscillations are thus damped instead of amplified. This resistance will also dissipate some of the input power, so a compromise has to be found between stability margin and reduction of performance.

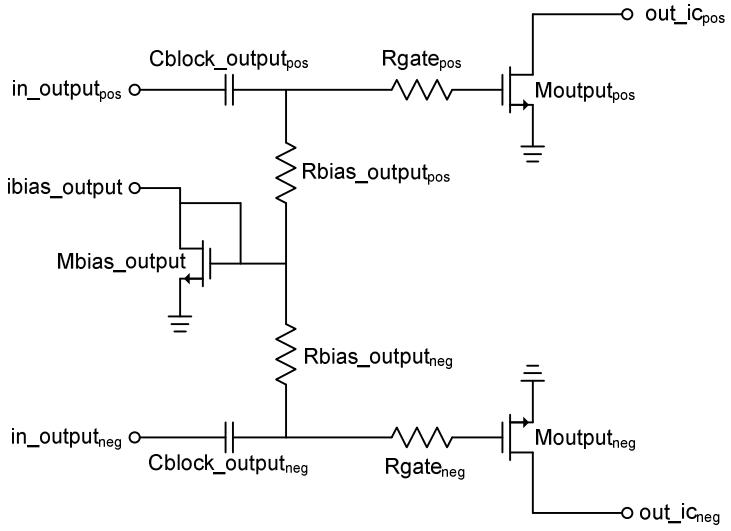


FIGURE 7.2 REVISED OUTPUT STAGE WITH ADDED GATE RESISTORS

This technique has been used to stabilise the output stage. A resistor R_{gate} in series with the gate of the output transistors as shown in Figure 7.2 has been found to increase stability with a limited impact on the output power. The cost is mainly a reduction of *PAE*.

7.3 Reduction of gain

The bias current of a conventional amplifying transistor is determined by the need of gain. Increasing the bias current increases the gain. However, in a class F output stage, the voltage gain is a function mostly of input voltage and output load. The bias current determines the width of the current pulse, but has limited effect on the voltage gain. It does however have a large effect on stability, as it impacts the gain of the feedback loop.

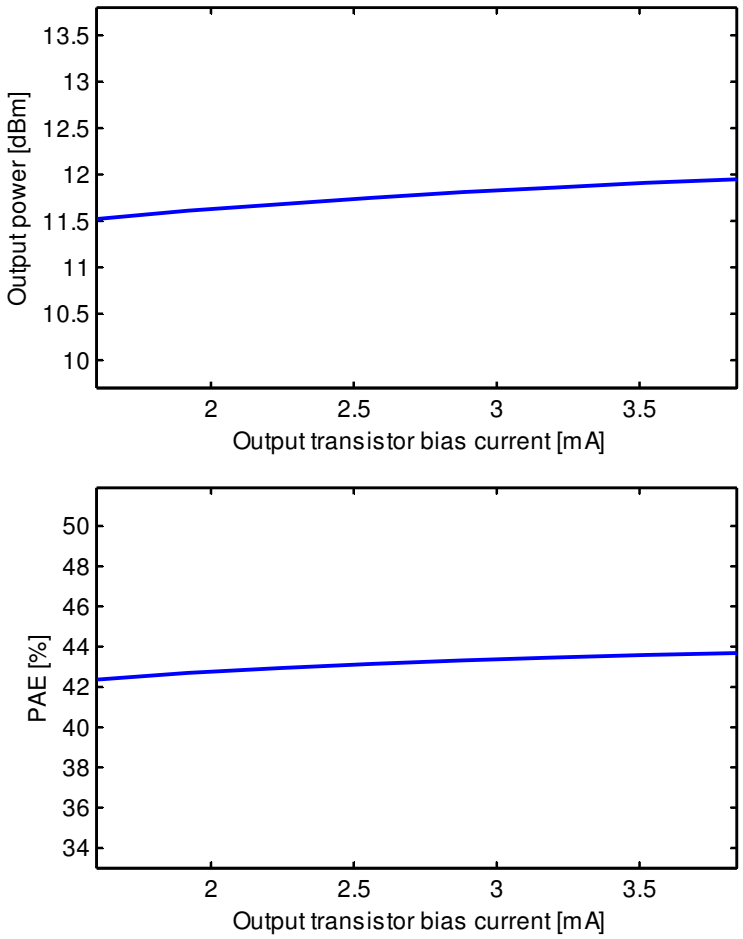


FIGURE 7.3 OUTPUT POWER AND PAE AS A FUNCTION OF OUTPUT TRANSISTOR BIAS CURRENT

The bias current of the output transistors was initially optimised for *PAE*, but has been greatly reduced to obtain stability. As seen in Figure 7.3 (schematic simulation), no critical bias is found as for the output transistor width discussed in section 7.1. The bias current has therefore been reduced as much as necessary to obtain stability.

7.4 Unilateralisation

Unilateralisation is an attempt to reduce feedback from the output of an amplifier stage to its input, while not reducing its amplifying capabilities [1]. Cascode topology is a good example, where the input is well isolated from the output (see Figure 5.1). However, this topology was eliminated in chapter 5, and a stabilisation of the existing topology is considered more appropriate than a change of topology. The stabilising nature of the cascode topology should be kept in mind in future designs, as it might ensure stability at a low cost of performance.

7.5 Neutralisation

Neutralisation is a way of reducing the effective feedback by introducing another feedback loop [1]. If the two feedback loops are equal in amplitude and opposite in phase, the net feedback will be zero. When the feedback is due to the gate-drain capacitance, neutralisation can in theory be obtained by connecting a capacitor between the gate and an opposite signal of that of the drain. This signal can be created in different ways, but in a differential amplifier it is available on the drain of the other transistor.

An important factor of success is that the two capacitors have to be equal in size. This is also the main limiting factor, as the gate-drain capacitance is voltage dependent. In a small-signal amplifier, an approximation may be useable. In a switching PA, however, the transistor is operated from cut-off to saturation each cycle and the gate-drain capacitance varies considerably. A neutralising capacitor is therefore not used in this design.

7.6 Idealisation of power and ground

The bond wires connecting the internal power and ground nodes to the external power supply and ground, separate the internal potentials from the external potentials. The external nodes are considered to be ideal, with a constant potential. The bond wire therefore allows RF distortion on the internal power and ground nodes. The extraction of layout parasitics also includes the distribution of potential from the bonding pads to the transistors.

RF distortion on the power and ground nodes can lead to instability. The source of each amplifying transistor is connected to ground. Therefore, any signal on ground can lead to a variation in the gate-source voltage of the transistor, with a consequent amplified signal on the drain of the same transistor.

This effect can be reduced by increasing the number of bond wires connecting the internal node with the external. Several bond wires in parallel will have a lower inductance than one alone, meaning that the internal power and ground nodes will have a potential closer to the ideal external potential.

In this design, the ground node is shared among all amplifying transistors by means of the substrate potential. The power, however, is separated in two nodes. One is for the bias block and has a typical value of 1.8 V. The other supplies the two driver stages through the on-chip inductors and has a typical value of 0.9 V. This separation also increases the PA stability, by increasing the isolation between the power in the bias block and the power at the drain nodes of the driver transistors.

TABLE 7.1 NUMBER OF BOND WIRES USED

Connection	No. of bond wires	Resulting Inductance [nH]
RF out positive	1	0.500
RF out negative	1	0.500
Power for bias block	3	0.167
Power for driver stages	3	0.167
Ground	12	0.042

The required number of bond wires needed to ensure stability is presented in Table 7.1. The large number of bond wires can constitute a considerable increase of packaging cost. This can be eliminated by using connection methods with low connection inductance, such as a flip-chip package. As described in [19], connection inductances as low as 0.015 nH per connection can be expected using a flip-chip package.

7.7 Consequences of stabilisation

The initial PA design was unstable, and started oscillating whenever the power was on. The introduction of a series gate resistance, the reduction of output stage transistor width, the reduction of output stage bias current and the use of additional bond wires have stabilised the PA. The typical output power has been decreased, but kept above 10 dBm according to the specifications. The total cost in efficiency has been a considerable reduction of *PAE* from 44 % to 30.5 %.

8 Layout

While layout can be automated in digital design, it is at present an important manual phase in RF design. At radio frequencies, the parasitics introduced by non-optimal design can considerably lower the performance compared to a simulation of the circuit schematic. With the schematic, only the different components are simulated, while a simulation of extracted parasitics from the layout will take routing and proximity effects into account. In a PA this will often result in a loss of both output power and *PAE*, and can sometimes introduce instability.

8.1 RF layout basics

To reduce the difference between the schematic and extracted simulations, there are two important issues to keep in mind. One is symmetry and the other is spacing. Space between two signals reduces the parasitic coupling between the signals. This will reduce the potential for loops that may lead to instability. Symmetry is obviously important in a differential PA. The differential architecture is used to lower the even harmonic content in the output power, based on destructive interference. If the two amplifiers are not exactly equal, this cancellation will not be as effective. It can even result in constructive interference.

Additionally, as much of the RF routing as possible should be done in the top metal, as it has lower capacitance to ground and lower series resistance than the other metals. 90 degree corners should be divided into two 45 degree corners to avoid wave reflection. A 90 degree corner can also increase coupling to the neighbouring signals.

The power and ground routing should be as wide as possible. This lowers the resistance, and keeps the potential more constant across the module. In this PA, a bottom metal ground plane is placed wherever possible without short-circuiting any connections.

Signals that are sensitive to RF distortion can be routed in a slit in the ground plane. This provides shielding that lowers the coupling to neighbouring RF paths. The bias currents have been routed using this technique.

A guard ring surrounds all transistors. This provides a good substrate connection, ensuring that all parts of the transistor have approximately the same bulk potential.

8.2 Layout floor plan

The PA has been laid out as shown in Figure 8.1. The squares marked *pd*, *d* and *o* are the pre-driver, driver and output stages respectively. The signal path goes from the left to the right, and the layout is symmetrical around a horizontal line dividing the positive and the negative parts of the differential PA.

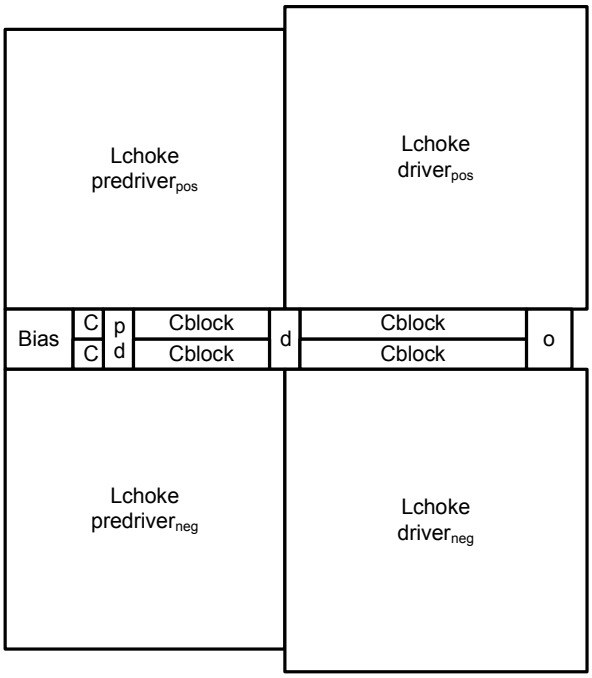


FIGURE 8.1 PA LAYOUT FLOOR PLAN

The final layout occupies an area of 0.66 mm^2 excluding connection pads. Most of the area is occupied by the inductors, with a total area of 0.59 mm^2. A screenshot of the layout can be found in appendix B.

8.3 Layout verification

There are two tools that are used to check the layout. The Design Rule Check (DRC) reports if any design rules are violated, such as metal wires that are narrower than the minimum width. Some rules are reported to be violated in this design, but they are all rules that can only be considered once the entire chip top-level layout is assembled. The PA module is therefore considered not to violate any design rules.

The other tool is Layout Versus Schematic (LVS) which reports any difference in properties or connections of the devices in the layout compared to the schematic. In this design the entire circuit except the inductors has been verified to match the schematic. The inductors have been manually measured to match the dimensions given in the schematic model.

8.4 Extraction of parasitics

The parasitic extraction of the layout has been performed by Calibre on the entire layout except the inductors. The result is a netlist containing a large number of circuit elements, each with a connection to the neighbouring circuit elements. This can be imported to the schematic editor Design Architect, so that simulations can be alternately performed on the schematic and on the extracted netlist. The inductor models have been added in the test bench.

The simulation on the extracted netlist is the best available approximation to the actual circuit. A circuit that shows the expected behaviour over a set of corner simulations of the extracted netlist is considered ready for tape-out[3].

[3] Tape-out is the point where the circuit design is sent to production. The name has survived from the days when magnetic tapes were used to transfer the data to the foundry.

9 Discussion

The results obtained are discussed below with respect to reliability, performance and stability. Suggestions to work that could be done in the future are also given.

9.1 Reliability

The PA is specified to operate over a bandwidth ranging from 2.4 GHz to 2.4835 GHz with an operating temperature ranging from -40 to 125 degrees Celsius. The supply voltage is also somewhat variable. The variation is set to ± 0.1 V, which is believed to be larger than the actual variation of the regulated voltage. The production of the circuit also introduces an uncertainty due to variable dimensions and material parameters. These variations are modelled by the foundry and implemented as a choice of typical, fast or slow devices as explained in section 5.4.

All these variations are simulated in a set of corners believed to cover all potential worst case scenarios with regards to performance. The results are used to find minimum and maximum values of key performance metrics, and also to verify that the operation is stable and otherwise as predicted. The exact corner sequence is confidential, so only three resulting cases will be shown. These are labelled typical corner, best corner and worst corner. The best corner is that with the highest output power, and the worst corner is that with the lowest output power.

There are other variations that are not covered in the corner simulations. These are various off-chip parameters that may also influence the PA performance. The metal and dielectric PCB dimensions may vary from board to board. The relative dielectric constant may vary depending on the type and amount of glue that is used. The loss tangent of the dielectric can vary over time due to temperature variations and moist absorption of the PCB. In addition, the antenna input impedance varies with the surroundings. The impact of these variations have not been simulated or calculated. As the PCB manufacturer does not provide any tolerance figures, the results would not be trustworthy.

Further investigation into the reliability of off-chip components is considered outside the scope of this work. It is assumed that a filter can be constructed with a frequency response comparable to or better than that of the Microwave Office model. It is also assumed that even though some variations are unavoidable, the filter can be made robust enough not to alter the reliability of the PA considerably. A successful example of a class F PA at 2.4 GHz loaded by a microstrip filter can be found in [20].

9.2 Performance

The final PA performance results have been extracted from a corner simulation performed on the circuit extracted from the final layout. The results obtained are

recapitulated in Table 9.1. In addition to the lowest output power, the worst corner also has the lowest *PAE* of all the corners simulated. Similarly, the best corner has the highest values. The results obtained when using typical values for all parameters is labelled the typical corner. An average circuit at room temperature with normal supply voltage is believed to perform as indicated in the typical corner.

TABLE 9.1 PA PERFORMANCE

	PAE	P_{in} [dBm]	P_{out} [dBm]	C_{in} [fF]
Worst corner	6.7 %	-18.6	1.0	92
Typical corner	30.5 %	-18.0	10.2	105
Best corner	42.4 %	-17.4	12.8	119

Both transient analysis and steady-state analysis have been performed, and the difference in performance is negligible. The reported performance numbers are extracted from the steady-state analysis. Harmonic power in the output signal can be found in appendix C.

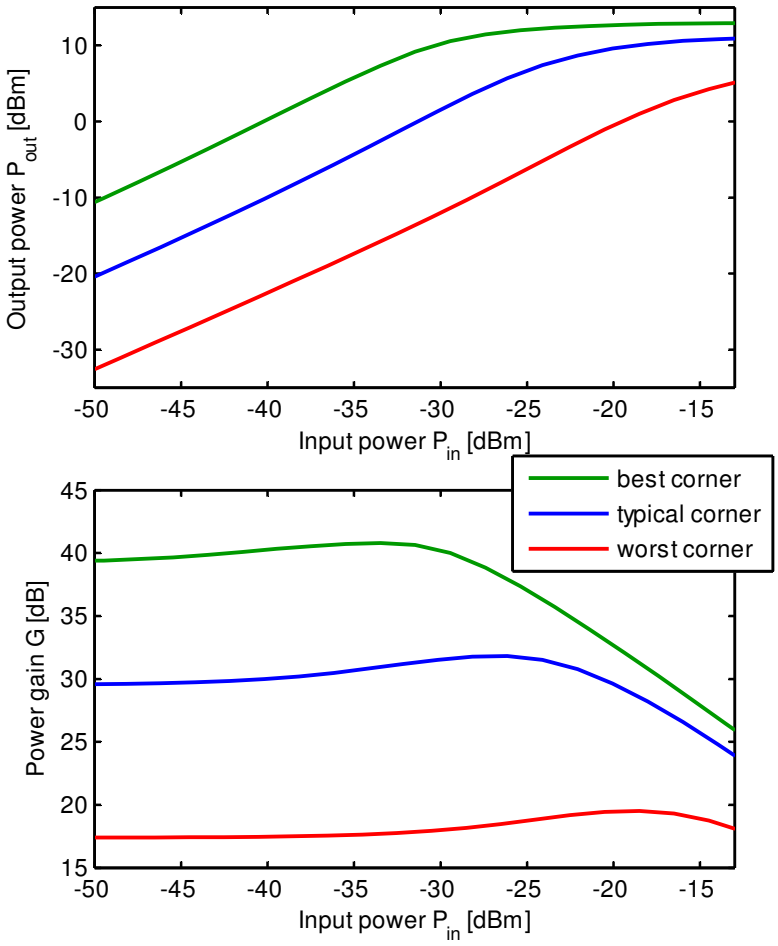


FIGURE 9.1 OUTPUT POWER AND POWER GAIN AS A FUNCTION OF INPUT POWER. THE TYPICAL, WORST AND BEST CORNERS ARE SHOWN.

As shown in Figure 9.1, the power gain varies considerably over the different corners. As the input power is approximately constant, this leads to varying output power.

The total current drawn at the typical corner is 37.2 mA. Of this, 24.3 mA is drawn by the output stage. This corresponds to a drain efficiency η = 47.7 % for the output stage.

If the 0.9 V supply voltage is converted from 1.8 V with 95 % efficiency, the current drawn by the PA would be 20 mA. If converted from 3 V, it would be 12 mA.

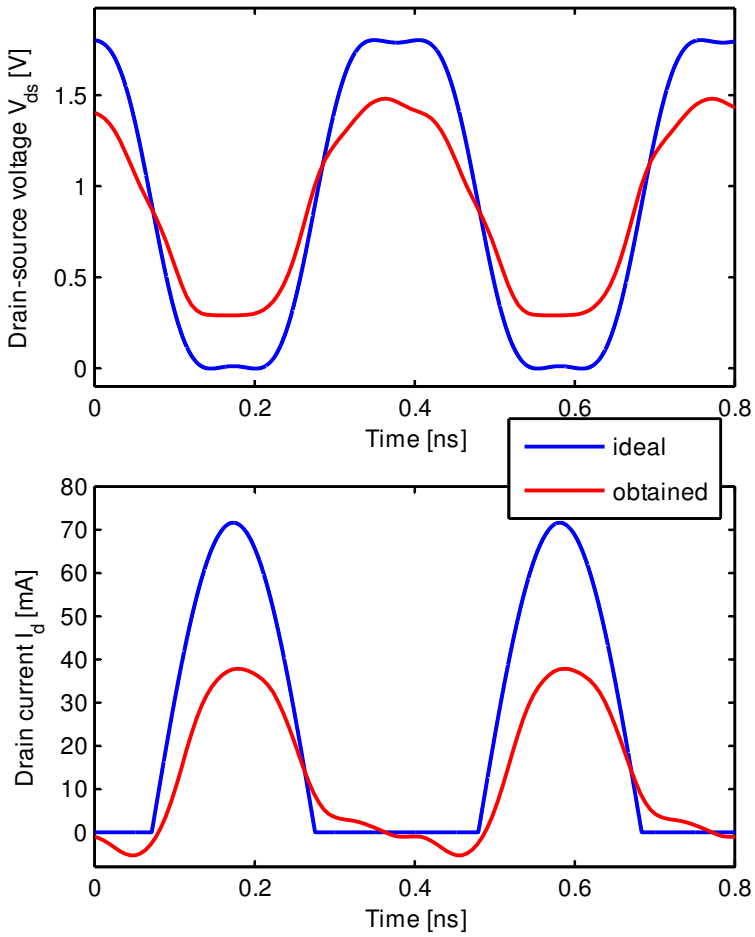


FIGURE 9.2 IDEAL AND OBTAINED DRAIN-SOURCE VOLTAGE V_{DS} AND DRAIN CURRENT I_D OF THE OUTPUT STAGE

The drain voltage V_{ds} and drain current I_d of the output stage in the typical corner is shown in Figure 9.2. The ideal case is shown as reference. It is seen that the drain-source voltage approximates a square wave, confirming that a certain amount of odd harmonics is present. As expected, the swing is not fully from 0 to $2 \cdot V_{dd}$ as in the ideal case. The drain current is largest where the drain-source voltage is lowest, also as expected.

TABLE 9.2 PERFORMANCE COMPARISON TO RECENTLY PUBLISHED PAS

	Class	Frequency	Technology	P_{out}	V_{dd}	PAE
[7]	AB	2.4 GHz	0.18 µm CMOS	9.0 dBm	1.8 V	16%
[8]	AB	2.4 GHz	0.18 µm CMOS	3.5 dBm	1.8 V	9%
[21]	Unknown	2.4 GHz	0.18 µm CMOS	1.5 dBm	3 V	3.3 %[4]
[22]	Unknown	2.4 GHz	0.18 µm CMOS	0 dBm	3 V	2.9 %[5]
This work	F	2.4 GHz	0.18 µm CMOS	10.2 dBm	0.9 V	30.5%

The PA is compared to a selection of recently published PAs in Table 9.2. Compared to this selection, this work performs very well in terms of *PAE*. The data sheets of the two transceivers from Texas Instruments [21] and Nordic Semiconductor [22] do not report PA *PAE*. The drain efficiencies η are approximated using the reported current consumption during transmission. To increase accuracy, the current consumed by the module when in transmit mode but not in transmission, i.e. mainly the frequency synthesizer current consumption, has been subtracted where available. Power lost in supply voltage conversion has not been subtracted due to lack of data.

There are numerous PAs that have higher *PAE* than those listed above. The list has been limited to reported PAs that have been realised in the same technology and at the same frequency as this work. A PA designer is not often free to choose frequency band and technology. The results obtained at other frequencies and in other technologies are therefore not of great interest. Reported PAs at 2.4 GHz in 0.18 µm CMOS with considerably higher output power than 10 dBm have also been excluded from the list, for the same reason.

9.3 Stability

Although stabilising measures as described in chapter 7 have been taken, some oscillations at supply voltage turn-on are still seen.

This could have been because the feedback loop needed some energy at a certain frequency to start oscillating. This was tested by injecting a current pulse into the drain of the output stage. A narrow pulse contains all frequencies of interest, and only a small amount of energy is needed to trigger the oscillations if the loop gain is greater than one. The oscillations that were triggered by this pulse quickly decayed. The conclusion that can be drawn from this result is that the oscillations at start-up are not caused by the steep slope of the power turn-on.

Instead, it was found that the problem lies in the biasing of the output stage. When the PA is turned on, the drain of the driver stage is charged to a voltage of almost 0.9 V through the inductor *Lchoke_driver*. The capacitor *Cblock_output* that initially had a voltage of approximately 0 V on each side now has nearly 0.9 V on one side. Due to charge preservation, the other plate will also initially have the

[4] Drain efficiency η calculated using transmit current reported in datasheet minus current consumption in transmit mode when not transmitting.
[5] Drain efficiency η calculated using transmit current reported in datasheet. No current consumption in transmit mode when not transmitting is reported.

same potential of nearly 0.9 V. The capacitor will then have to be charged with a charge ΔQ allowing a voltage difference ΔV between the two capacitor plates, where

$$\Delta Q = C \cdot \Delta V \,. \tag{9.1}$$

The current charging the capacitor needs a path from the supply power through the capacitor to ground, and the only available path is through the bias resistance *Rbias_output*. The capacitor is large to ensure that most of the RF voltage is seen across the gate-source capacitance of the output transistor. The bias resistance is large to ensure that a negligible portion of the RF current reaches the bias transistor. This results in a time constant τ in the RC-circuit given by

$$\tau = Rbias\_output \cdot Cblock\_output \approx 21\,\mathrm{k\Omega} \cdot 9\,\mathrm{pF} \approx 190\,\mathrm{ns} \tag{9.2}$$

This large time constant, which corresponds to approximately 460 RF periods, means that the capacitor charges slowly. During that time the gate voltage of the output transistors is higher than predicted. This gives the transistors a higher gain than at normal operation. This leads to oscillations that do not occur in simulations where the starting operating point is calculated with the power already on.

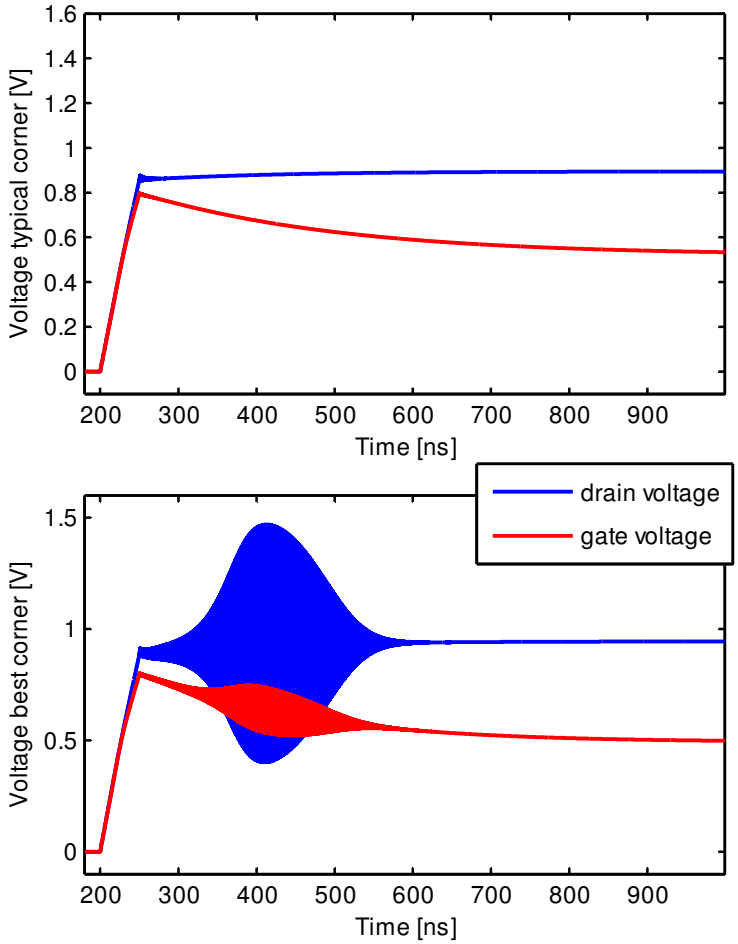


FIGURE 9.3 DRAIN AND GATE VOLTAGE OF THE OUTPUT TRANSISITOR DURING START-UP. THE TYPICAL AND BEST CORNERS ARE SHOWN.

As seen by comparing the top and bottom of Figure 9.3, these oscillations are only seen in the process corner known as “best corner” where the gain is highest. This is obviously the worst corner regarding oscillations. It is seen that these start-up oscillations start decaying when the gate voltage has fallen to a level where the loop gain is no longer higher than one.

To avoid this excessive the gate voltage, additional circuitry consisting of a low impedance path to ground and a delay element can be used to keep the gate node at ground during start-up. When the fixed delay has passed, the gate node will be slowly charged from ground to its final value. The loop gain will thus never be larger than at normal operation, so this oscillation source is removed.

Alternatively, to avoid that the start-up oscillations reach the output, the output pins can be clamped to ground for the first microsecond after power supply turn-on. The need for these measures depends on the application of the PA, so they are not implemented in this work.

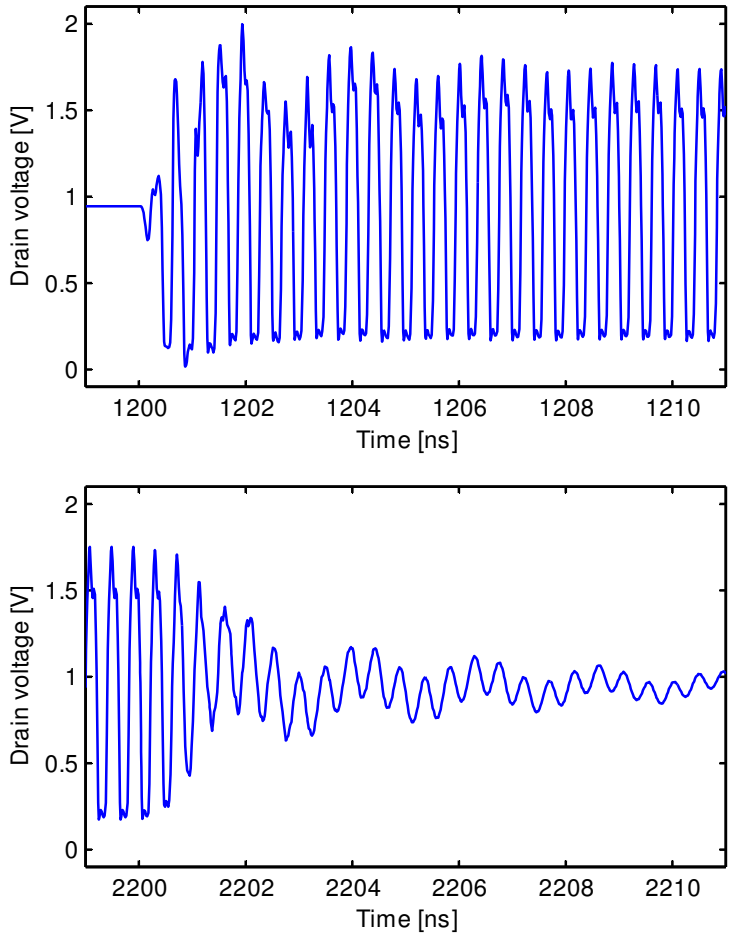


FIGURE 9.4 DRAIN VOLTAGE OF THE OUTPUT TRANSISTOR AT RF INPUT TURN-ON AND TURN-OFF. ONLY THE BEST CORNER IS SHOWN.

Transient simulations of RF turn-on and turn-off have also been performed. As seen in Figure 9.4, the envelope of the drain of the output transistor shows an

underdamped behaviour. As the oscillations are damped at supply voltage turn-on, at RF input turn-on and at RF input turn-off across all potentially worst case scenarios, the PA is considered stable. A larger stability margin would be desirable, but will not be further investigated in this work.

9.4 Future work

There are some aspects of a PA design that have become evident during the work but not been thoroughly explored. These aspects could be interesting topics for future research.

It should be verified that an output filter as outlined above is able to produce the required frequency response. An electro-magnetic simulation (EM-simulation) performed on the microstrip structure will give a reliability comparable to that of the extraction of layout parasitics from the integrated circuit design. Other microstrip structures and other substrates could also be evaluated to find an optimal compromise of production cost and performance.

A better methodology for further identification and elimination of instability sources would be a valuable tool for PA design. The main instability source, the feedback from drain to gate in the output transistors, has been greatly reduced. The stability margin can however be increased by further reduction of that and other instability sources if found. The challenge is to keep the performance at the same level. The need of an output clamp as described above should also be evaluated. It does not reduce instability at internal nodes, but does prevent interference from start-up oscillatons from reaching the antenna.

The possibility to control the output power depending on actual distance to the receiver can be valuable. Digital control of the bias current multiplication is an addition that may be worth considering. So is also the possibility to put the PA in power-down without turning off the supply voltage.

If a new but similar design is to be done, there are some additional aspects that should be considered. The cascode topology should be investigated. It has an inherent isolation between input and output, greatly reducing the parasitic feedback that proved problematic in this design. In addition, a higher supply voltage may be used, possibly eliminating the need for two different power supply voltages. The power conversion loss can probably also be reduced if the applied supply voltage is closer to the globally available supply voltage.

A shared optimisation of area and *PAE* can also be interesting. The reduction of area, for instance by using another load than inductive in one or both driver stages, will reduce both area and *PAE*. A prioritisation of importance is therefore needed to find the best compromise that combines low area with a reasonable *PAE*.

A study of possible integration of the output filter can also be useful, as a class F PA relies heavily on a specific output filter frequency response. Integration would make the PA operation independent of the customer PCB layout.

10 Conclusion

A class F PA capable of delivering 10.2 dBm output power in the 2.4 GHz ISM band has been designed. A switching PA class was chosen in order to maximize *PAE*. Class F was chosen for the combination of lower maximum drain voltage than class E and better high frequency performance than class D.

Some basic challenges and limitations related to implementing the PA in integrated CMOS and the output filter on PCB have been discussed. The resulting models have been used in the design.

Numerous measures to stabilise the initially unstable amplifier have been discussed, and some implemented. The cost of stabilisation was a reduction of *PAE* by 13.5 % points. A stability margin has not been determined.

The simulations performed on the extracted parasitics from the final layout show a typical output power of 10.2 dBm with an output stage η of 47.7 % and a total PA *PAE* of 30.5 %.

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