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IV and CV characterization of 90nm CMOS transistors

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Problem Description

Prototype circuits produced in 90nm CMOS are to be characterized by means of a new probe station and instrumentation for IV and CV measurements. The assignment will consist of measuring the capacitance-voltage and current-voltage transistor characteristics for this 90nm technology.

Assignment given: 16. January 2006
Supervisor: Trond Ytterdal, IET

Abstract

A 90nm CMOS technology has been characterized on the basis of IV and CV measurements. This was feasible by means of a state of the art probe station and measurement instrumentation, capable of measuring current and capacitance in the low fA and fF area respectively. From IV results it was found that the static power consumption is an increasing challenge as the technology is scaled down. The IV measurements also showed the impact from small-channel effects, which was not as prominent as expected. Investigation of literature has resulted in a methodology for accomplishing accurate CV measurements on thin-oxide transistors. By using extraction methods on the capacitance measured, key parameters have been obtained for the CMOS technology. Some of the extracted results suffer however from the choice of test setup.

Preface

This master thesis was accomplished in the spring of 2006 at the Department of Electronics and Telecommunications (IET), The Norwegian University of Science and Technology (NTNU). NTNU was also the proposer of the master thesis.

Academic advisor and supervisor has been professor Trond Ytterdal. He has provided for the superior project guidance, by arranging regular meetings, answering questions and giving me input in numerous discussions. He has also been holding test equipment lessons and providing the test transistors for physical measurements. All of this which I am very thankful for.

In addition I would like to thank the following persons:

- Principal engineer Tore Barlindhaug, for answering questions and preparing the lab instrumentation ready for use.
- Ph.D. student Tajeswar Singh, for giving me practical training on some of the measurement equipment and for useful discussions.
- M.Sc. Anders Lund, for creating small script to split the large size of data from simulations.

Trondheim, 12 June 2006

Håvard Lund

Acronyms and Abbreviations

MOS Metal-Oxide Semiconductor

MOSFET Metal-Oxide Semiconductor Field-Effect Transistor

MOS-C Metal-Oxide Semiconductor Capacitor

CMOS Complementary MOS

NMOS n-channel MOSFET

PMOS p-channel MOSFET

DC Direct Current

AC Alternating Current

IV Current vs. (DC bias) Voltage

CV Capacitance vs. (DC bias) Voltage

DIBL Drain-Induced Barrier Lowering

ISS Impedance Standard Substrate

DUT Device Under Test

ABB Auto-Balancing-Bridge

Nomenclature

V_G	MOSFET externally applied gate voltage $[V]$
V_D	MOSFET externally applied drain voltage $[V]$
V_B	MOSFET externally applied bulk voltage $[V]$
V_S	MOSFET externally applied source voltage $[V]$
V_{GS}	MOSFET externally applied gate-to-source voltage $[V]$
V_{DS}	MOSFET externally applied drain-to-source voltage $[V]$
V_{SB}	MOSFET externally applied source-to-bulk voltage $[V]$
C_{gg}	MOSFET total parasitic gate capacitance $[F]$
C_{gb}	MOSFET parasitic gate-to-bulk capacitance $[F]$
C_{gs}	MOSFET parasitic gate-to-source capacitance $[F]$
C_{gd}	MOSFET parasitic gate-to-drain capacitance $[F]$
C_{bb}	MOSFET total parasitic bulk capacitance $[F]$
C_{bg}	MOSFET parasitic bulk-to-gate capacitance $[F]$
C_{bs}	MOSFET parasitic bulk-to-source capacitance $[F]$
C_{bd}	MOSFET parasitic bulk-to-drain capacitance $[F]$
C_{db}	MOSFET parasitic drain-to-bulk capacitance $[F]$
C_{sb}	MOSFET parasitic source-to-bulk capacitance $[F]$
C_{ol}	MOSFET overlap capacitance between gate-drain or gate-source $[F]$
V_{th}	MOSFET threshold voltage $[V]$
V_{tn}	MOSFET threshold voltage, NMOS specific $[V]$
V_{tp}	MOSFET threshold voltage, PMOS specific $[V]$
V_{FB}	MOSFET flatband voltage $[V]$
V_{eff}	Effective gate voltage $[V]$
W	Effective width of MOSFET gate $[m]$
L	Effective length of MOSFET gate $[m]$
L_{ov}	Overlap between gate and source, or gate and drain $[m]$
I_D	MOSFET drain current $[A]$
I_G	MOSFET gate leakage current $[A]$
I_{sub}	MOSFET drain-to-source subthreshold leakage current $[A]$
g_{ds}	MOSFET drain-source conductance $[A/V]$
r_{ds}	MOSFET drain-source resistance $[\Omega]$
g_m	MOSFET transistor transconductance $[A/V]$
t_{ox}	Thickness of MOSFET gate oxide $[m]$

γ MOSFET body-effect coefficient [$V^{1/2}$]
λ MOSFET channel-length modulation parameter [$1/V$]

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Chapter 1

Project introduction

1.1 Motivation

With the continually decrease in dimensions for the MOSFET, new characteristics come into effect. For this master thesis recently fabricated transistors in a 90nm CMOS process were available for investigation. By investigating the voltage versus current characteristics for the transistors, the impact from this technology downscaling can be investigated. This is achieved through IV measurements. CV measurement is an important method to characterize the semiconductor material ([36, chapter 5-6]). From this numerous key parameters associated with a particular MOSFET process can be investigated. New and more precise measurement equipment for these two methods of IV and CV have become available, opening for a more precise investigation of deep-submicron devices. The results from measurements can finally be used to determine the quality of the models used for simulations.

1.2 Method

First the 90nm CMOS technology is characterized through IV measurements, by using a probe station and additional measurement equipment. Then the semiconductor material is investigated through CV measurements.To verify the results, the same measurements are simulated with the circuit simulator Eldo. The level of the parameters to be measured are typically very small for such deep-submicron devices. This must be taken into account, and requires theoretical input from present literature.

1.3 Structure of the report

The report is organized in the following main chapters:

- **Chapter 2:**
  Here a theoretical foundation necessary for the master thesis is presented.
- **Chapter 3:**
  Here the specifications for what to be accomplished and devices to be investigated throughout the project are introduced.
- **Chapter 4:**
  Here the test plans and test setup used for simulations and physical measurements are presented.
- **Chapter 5:**
  Here the results for DC measurements and simulations at room temperature are given.
- **Chapter 6:**
  Here an accompanying discussion for DC measurements and simulations results at room temperature is given.
- **Chapter 7:**
  Here the results and discussion for AC measurements and simulations at room temperature are given.
- **Chapter 8:**
  Here a conclusion for the project on the basis of results and experience is stated.

Chapter 2

Theory

This chapter will present the fundamental theory necessary for this master thesis. First a basic review of semiconductor physics is given. Then the physical structure of the MOSFET will be examined, along with its dependency on applied bias voltage. Further the various parasitic capacitances associated with the MOSFET is explained, initially by reducing the MOSFET into a basic MOS-C structure. That is, removing the drain and source diffusions. Finally the most important effects from downscaling with respect to the MOSFET phycical geometries are reviewed. This latter topic is important regarding the focus of this master thesis.

Most parts of this chapter have been taken from [18], [22, chapter 1] and [39, chapter 3]. Some sections also list additional references. Note that the concepts *substrate* and *bulk* are used in turns through all sections of this chapter, although they describe mainly the same. In principle the theory reviews the NMOS, that is, a MOSFET built on a p-type bulk semiconductor. But it is applicable to PMOS as well by changing the sign of every voltage and replacing the operator $>$ with the operator $<$ and vice versa.

2.1 Basic semiconductor physics

A pure semiconductor is an elemental material that conducts better than an insulator, but worse than a conductor. This characteristic is because of its 4 electrons in the outer shell, the valence shell. By sharing electrons with four other neighbouring semiconductor atoms, a perfect lattice structure is created as shown in figure 2.1. A pure lattice consisting of only semiconductor atoms is called an **intrinsic semiconductor**. Silicon (symbol Si) is one type of semiconductor that is often used in the electronics industry, and will be used to a large extent in the review to follow as well.

Electrons and **holes** are important when reviewing the theory of semicon-

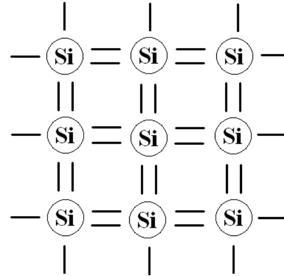

Figure 2.1: Intrinsic semiconductor lattice, created by silicon atoms.

ductors. The term *hole* is here a concept for the absence of electrons. Holes and electrons have basically the same properties, except from the hole representing positive charge while the electron represents negative charge. In an intrinsic semiconductor lattice there will always exist some free electrons that have gained enough kinetic energy to leave the bonds between the semiconductor atoms that they usually are a part of. Since each free electron is also interpreted as a free hole, the number of electrons and holes are thus equal. Because of this the intrinsic semiconductor lattice has an equal number of electrons and holes at a given temperature, and is thus electrically neutral.

By however doping the semiconductor with other impurity materials, this impurity atom will replace a semiconductor atom in the lattice and enter the bonds with other neighbouring semiconductor atoms. The outer shell of the semiconductor atom thus achieves a number of electrons in its valence band according to the desire of the designer. Thus by introducing contamination, the number of free carriers is altered and hence the conductivity of the semiconductor is controlled. It can be doped to have either an excess of free electrons (n-doping, resulting in an excess of negative carriers) or an excess of free holes (p-doping, resulting in an excess of positive carriers). A doped lattice is called an **extrinsic semiconductor**, being different from the intrinsic semiconductor by having a net profit of carriers.

The interesting aspect of this is the combination of p- and n-type materials. Since the material has an excess of either electrons or holes, it is negatively or positively charged respectively. Placed together, these two opposite charged materials will therefore set up an inherent electrical field. An opposite directed electrical field must therefore be applied to achieve current conduction through the combined material. In this way current flow is possible in one direction only, and not the other. This opens for devices with exclusive properties, such as the MOSFET. The MOSFET is designed to be conducting current by the means of only one type of free carriers (holes or electrons), determined by the combination of materials described above.

Materials try to aim for 8 electrons in its outer shell to obtain the structure of a noble gas. This works as the basic rule when designing a p- or n-type material. Two examples are useful to illustrate this process:

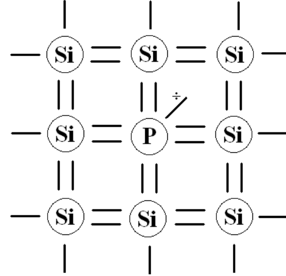

Figure 2.2: Silicon lattice doped with donor phosphorus, resulting in excess of negative electron.

First is when silicon is doped with a donor (5 electrons in the outer shell), e.g. phosphorus (symbol P). This results in an excess of about 1 electron per impurity atom. Hence an n-type material is created, as shown in figure 2.2. The concentration of donor doping (atoms/m^3) is termed N_D.

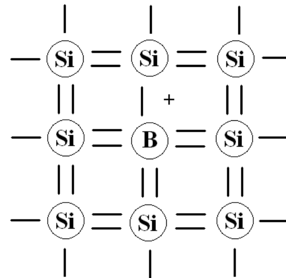

Figure 2.3: Silicon lattice doped with donor phosphorus, resulting in excess of positive hole.

Second is when silicon is doped with an acceptor (3 electrons in the outer shell), e.g. boron. This results in an excess of about 1 hole per impurity atom. Hence a p-type material is created, as shown in figure 2.3. The concentration of acceptor doping (atoms/m^3) is termed N_A.

Two important processes regarding the free carriers in a semiconductor material are that of *generation* and *recombination*. Electrons within the semiconductor lattice are exposed to an ambient temperature, which in turn can be converted to kinetic energy by the electrons in the bonds. At some point the electron have gained sufficient kinetic energy to abandon the covalent

bond and become a free charge carrier, leaving a hole behind. This process is known as generation, while the opposite when the electron enters the bond again is called recombination. These two processes are to a large extent in balance, such that the concentration of free charge carriers n_i in an intrinsic semiconductor is constant at the specific temperature. On the other hand, in an extrinsic semiconductor this is not true since the carrier concentration has been altered through doping. These type of materials therefore have a much larger concentration of holes relative to electrons or vice versa. These concentrations are called *majority carriers* and *minority carriers*, to distinguish between the carriers created by doping and those created by generation.

2.2 The MOSFET

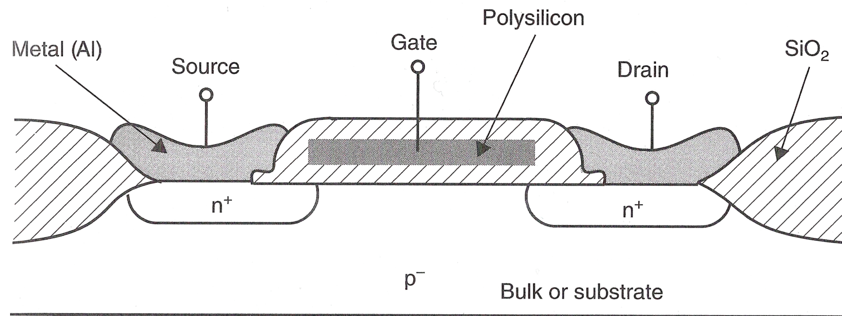

Figure 2.4: Cross-sectional view of NMOS. ([22, figure 1.6]).

The MOSFET is a four-terminal transistor device, based on the above described semiconductor material. The nodes are named *gate, drain, source* and *bulk*. It is created by diffusions of p- or n-type semiconductors placed into a bulk of n- or p-type semiconductor respectively. A cross-section of an NMOS is shown in figure 2.4. The drain and source regions consist of heavily doped n^+ regions[1]. While the substrate or bulk region consists of a lightly doped p^- region[2]. It is obvious that the MOSFET may be viewed as a capacitor, consisting of the gate and the bulk as the two electrodes and the gate oxide as the dielectric in between.

There are several process and design parameters which are of importance for the electrical properties of the MOSFET. The channel length L, channel

[1]The plus sign indicates that this region has a large number of free negative carriers available

[2]The minus sign indicates that this region only has slightly more free positive carriers than free negative carriers available

width W, doping level in diffusions and bulk, and gate oxide thickness t_{ox} are some of those. They all affect the functionality of the MOSFET, in accordance with general theory of electronics but also on the basis of theory from processing. This report will investigate the effect of these parameters in terms of the electrical behavior.

A MOSFET may be used both as a switch and as an amplifier. Gate is the controlling node, by setting up the required electrical field to determine the charge concentration at the bulk-to-oxide interface. In this way it determines whether the device is fully on, in intermediate state or off. Since the gate is electrically isolated from bulk, drain and source by the gate oxide, it does in the most simplistic review not conduct any DC current. According to the charge concentration at the bulk-to-oxide interface, current may or may not flow between drain and source. The MOSFET itself is a symmetrical device, where drain and source are defined on basis of the direction of current flow. When the charge concentration is such that current is allowed to flow, the current flow itself is determined by the drain-to-source voltage V_{GS}. The purpose of the bulk node is to set the source-to-bulk voltage V_{SB}, and hence set the electrical conditions for the substrate. By setting the bulk to a lower potential than the rest of the device nodes, the initial reverse-bias of the two p-n junctions is increased such that the device is not conducting when it is intended to be on.

It has been seen that the controlling voltage parameters of the MOSFET are the gate, drain and bulk potentials with respect to the source node. This will be examined more detailed further in the upcoming sections 2.2.1, 2.2.2 and 2.2.3 respectively. The following review assumes an NMOS (i.e. p-type semiconductor) with a fixed substrate voltage if not otherwise specified.

2.2.1 MOSFET dependency of gate-source voltage V_{GS}

It is of particular interest to investigate the behavior of the MOSFET as a function of the gate bias. The mode of operation as a function of applied V_{GS} is typically divided into three regions. These regions are called *accumulation*, *depletion* and *inversion*. The transitions are however not abrupt. Only the MOS-C principle will be investigated initially, to particularly show the impact V_{GS} has on the charge concentration in bulk.

Accumulation region (device off)

Within the p-type substrate there is an excess of positive, majority carriers. By applying a negative gate voltage, these positive majority carriers are attracted toward the oxide-to-substrate interface. The holes accumulate, and an *accumulation layer* is thus created. Any free negative minority carriers in

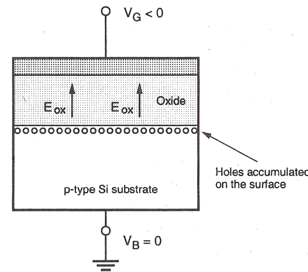

Figure 2.5: p-type MOS-C in accumulation region. ([39, figure 3.5]).

the substrate are on the other hand repelled further away from the junction. Hence the device is OFF, and the resulting electric field in the gate oxide is directed upward against the gate.

Depletion region (device in intermediate state)

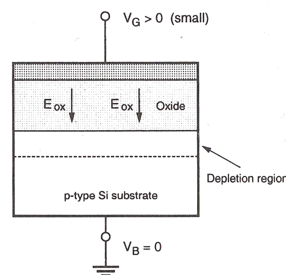

Figure 2.6: p-type MOS-C in depletion region. ([39, figure 3.6]).

If a small, positive gate voltage is applied, the situation turns opposite. Now the positive majority carriers are pushed out of the accumulation layer and deeper into the substrate, leaving ions[3] of negative charge fixed in the silicon lattice ([18, chapter 1.2.1]). The gate bias at which the substrate semiconductor eventually reaches neutrality all over is called the *flatband voltage* V_{FB} ([18, chapter 2.3]). Any increase in gate voltage beyond V_{FB} causes the silicon lattice region near the bulk-to-oxide interface to become depleted from holes. This stand-off between positive gate voltage and negative ion charge near the bulk-to-oxide interface thus creates a *depletion region*, where

[3]Ions are atoms with a net positive or negative charge (i.e. not neutral). If electrons are removed, the atom becomes positively charged. While if electrons are accepted, the atom becomes negatively charged. When holes are pushed into the substrate, this means in practice that the doped silicon atoms in the p-type substrate near the bulk-to-oxide interface accept electrons and hence becomes negatively charged ions.

there are almost no positive majority carriers left. That is, they will balance the charge of each other. This depletion region grows down into the volume of the semiconductor with increasing gate voltage. The resulting electric field in the gate oxide is directed downward against the substrate. At some point the depletion region prevails the gate voltage, and therefore stops increasing in volume. The rest of the p-type substrate is however neutral.

Inversion region (device on)

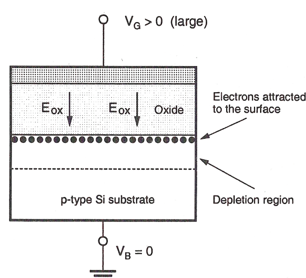

Figure 2.7: p-type MOS-C in inversion region. ([39, figure 3.7]).

If the applied gate voltage is further increased, negative minority carriers from the substrate are attracted toward the bulk-to-oxide interface. These negative minority carriers are a result of the positive majority carriers that were repelled deep into the substrate during depletion, activating the process of *generation* described in section 2.1 as a response. Since the number of positive majority carriers in the p-type substrate increase due to repulsion from the bulk-to-oxide interface, negative minority carriers must be generated to maintain neutrality. Finally a continuous n-type channel region becomes present at the bulk-to-oxide interface under gate, consisting of negative minority carriers that were just created. The semiconductor material near the bulk-to-oxide interface is said to be *inverted*, since it now has a hole-to-electron concentration similar to that of an n-type material. The device is at present thus in *inversion region*. The depleted area below the channel is still present irrespective of the conducting channel, but it does not increase. Instead, the increase in gate voltage is balanced by the increase in attracted negative minority carriers. The gate voltage at which this channel is created is called the *threshold voltage* V_{th}. The actual threshold voltage is determined by the doping profile of the substrate. The resulting electric field is still directed downward against the substrate. It is common to divide this region into the two sub-regions *weak inversion* and *strong inversion*, which refer to the regions before and after V_{th} respectively. Hence the threshold voltage indicates the point at which strong inversion is reached.

By adding n-type drain and source diffusions on each side of the MOS-C structure, the charge concentration at the bulk-to-oxide interface described above determines the condition between these two diffusions. When the device is off, the p-type region between the two diffusions acts as a barrier since it is of opposite polarity. But when the channel is present, the charge concentration at the bulk-to-oxide interface is on the other hand of the same polarity as that of the diffusions. Hence there is a direct path between drain and source where current may flow, since these minority carriers are mobile.

CMOS is a concept for technologies embracing both NMOS and PMOS fabricating, where the latter is created by interchanging the n^+ regions with p^+ and p^- with n^- in figure 2.4. PMOS is therefore on when the gate voltage is negative, while the NMOS is on when the gate voltage is positive. PMOS thus uses holes as minority carriers to conduct current, while the NMOS uses electrons. The current goes from source to drain for the PMOS, and from drain to source for the NMOS.

2.2.2 MOSFET dependency of drain-source voltage V_{DS}

The MOSFET mode of operation as a function of applied drain voltage is typically divided into the three regions *cut-off*, *linear region* and *saturation region*. The two latter regions are visualized in figure 2.8. This dependency assumes that a conducting channel is already present such that the device is in inversion, as already reviewed in section 2.2.1. The drain bias is essential for establishing the current flow I_D between drain and source.

Cut-off

If $V_{DS} = 0V$, then $I_D = 0A$ ideally. Notice from the discussion about gate bias above, that the drain current will be zero also if a conducting channel is not present.

Linear (triode) region $((V_{GS} - V_{th}) > V_{DS})$

This region becomes present if a small V_{DS} is applied, as seen in figure 2.8a. I_D will then be about proportional to V_{DS}, hence a linear curve characteristic is obtained. By adjusting V_{DS} within this region, the behavior of a voltage-controlled resistor is obtained. As V_{DS} is further increased however, the size of the conducting channel starts to decrease at the drain end. At the so-called *pinch-off* voltage (figure 2.8b) the conducting channel reaches only just to about the drain diffusion. Drain current now starts to saturate, because only a depleted version of the original channel is left on the oxide-to-substrate interface near drain.

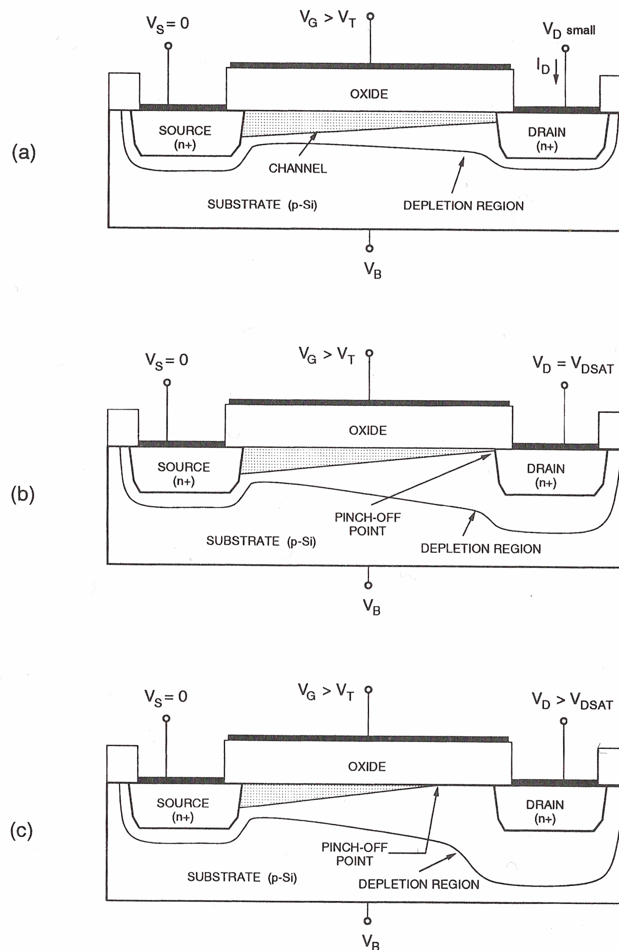

Figure 2.8: MOSFET modes of operation with variable drain potential: a) linear, b) pinch-off and c) saturation ([39, figure 3.14]).

Since the MOSFET characteristics in linear region resemble that of a voltage-controlled resistor, the output resistance of the MOSFET is a very interesting parameter for this specific region. This is modeled by the **transistor drain-to-source resistance,** r_{ds}, or the drain-to-source conductance g_{ds} which is the inverse of r_{ds}. g_{ds} is ideally infinite when the MOSFET is in cut-off.

Saturation (active) region ($(V_{GS} - V_{th}) < V_{DS}$)

As V_{DS} is further increased after pinch-off, the depleted channel gradually replaces the original channel and so the pinch-off point moves closer and closer toward the source diffusion. As a result the drain current becomes more and more saturated because of the decrease in effective channel length (figure 2.8c). As a result the velocity of the minority carriers saturates, and the $V_{DS} - I_D$ curve characteristic flattens. A common exception from this characteristic comes as a consequence from *channel-length modulation*, which arise for short channel devices. That is, since the effective length of the channel is reduced with increasing V_{DS}, the effective r_{ds} is also reduced. This effect results in a small proportional increase in I_D even in this region. Channel-length modulation is expressed by the parameter λ, where $\lambda = 0$ indicates that the slope is zero in saturation region.

The characteristics of the MOSFET in saturation region is very similar to that of a voltage-in-current-out amplifier, commonly named a *transconductor*. Because of this the transconductance gain of the MOSFET is a very interesting parameter for this specific region. This is modeled by the **transistor transconductance,** g_m.

2.2.3 MOSFET dependency of source-bulk voltage V_{SB} (the body effect)

Usually both source and bulk are connected to a common voltage level, which was a prerequisite for the previous review. A different bulk voltage bias compared to the source potential however gives rise to *body effect*. This may implemented due to design issues, or unintentionally. For NMOS this body effect occurs for positive V_{SB}, while for PMOS it occurs for negative V_{SB}. The body effect increases the effective threshold voltage V_{th}, since the potential that the gate voltage must overcome is increased. As a result it also reduces the drain current capabilities of the device. That is, the maximum achievable drain current is reduced.

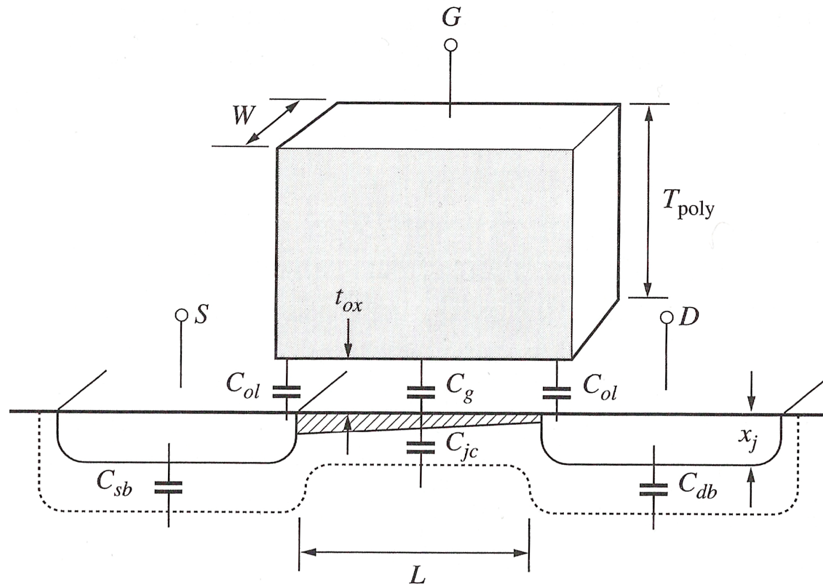

Figure 2.9: MOSFET capacitances ([31, figure 2.17)]).

2.3 MOSFET parasitic capacitances

The parasitic capacitances of the MOSFET make up an important part of the total parasitic capacitance of a specific design in addition to the interconnect delays. Rise- and fall-times are determined by the necessary time to charge and discharge the internal circuit capacitances, in general determined by the time constant $\tau = R \cdot C$. The analysis of MOSFET capacitances is therefore very interesting regarding the speed and power consumption of a circuit.

Analysis of MOSFET parasitic capacitances is also an often-used method for characterizing a specific MOSFET technology. This is done by measuring the MOSFET equivalent capacitance, and from this vital information can be extracted. Among the MOSFET device and process parameters which can be found from CV measurements are gate oxide thickness t_{ox} and threshold voltage V_{th}. A more supplementary list can be found in [18, chapter 1.3.3].

Most parts of this section have been taken from [21], [22, chapter 1.2], [23, chapter 5.10], [28, chapters 20 and 22], [31, chapter 2.8], [32, chapter 9.3] and [39, chapter 3.6]. It will focus on MOSFET-related capacitances and not interconnect capacitances, since the latter is not the focus of this master thesis. It is however interesting to notice that interconnect capacitances begin to dominate MOSFET capacitances as the technology is scaled down toward deep-submicron ([39, chapter 6.5]).

The theory of MOSFET parasitic capacitances is in many ways based upon the general theory about parallel-plate capacitors. Any basic study of this latter topic will not be given, as this is assumed known by the reader. Going directly to the analysis of the MOSFET-specific capacitances is found more appropriate instead.

Capacitances associated with the MOSFET is typically classified into two major groups: *oxide-related capacitances* and *junction capacitances*. The former comes as a consequence of the gate oxide acting as a dielectric between various electrodes of the MOSFET, and will be discussed in section 2.3.2. While the latter is a result of the depletion region formed between the p-n junctions within the semiconductor material, acting as a dielectric between the diffusions and bulk. Junction capacitances will not be studied as part of this master thesis.

First an evaluation of the capacitance associated with the basic two-terminal MOS-C will be given. This device constitute a very important part of the four-terminal MOSFET, and is therefore of interest to create a basic understanding of the MOSFET capacitances.

2.3.1 The MOS capacitor (MOS-C)

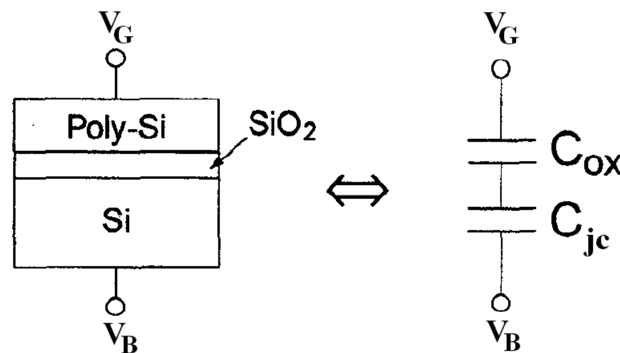

Figure 2.10: Equivalent circuit for the capacitances represented by the MOS-C ([8, figure 2]).

A simplistic drawing of a silicon-based MOS-C is shown in figure 2.10. It consists of doped silicon as the substrate, a gate electrode made of polycrystalline silicon[4], and silicon dioxide (symbol SiO_2) to separate gate from the substrate. The MOS-C actually consists of two different capacitors. These are the gate capacitance per unit area C_{ox} and the channel junction capacitance C_{jc}. The dielectric of C_{ox} is the always existing gate oxide, while the dielectric of C_{jc} is the depleted region created in the semiconductor during

[4] Polysilicon is non-crystalline silicon with a high level of doping ([22, page 17])

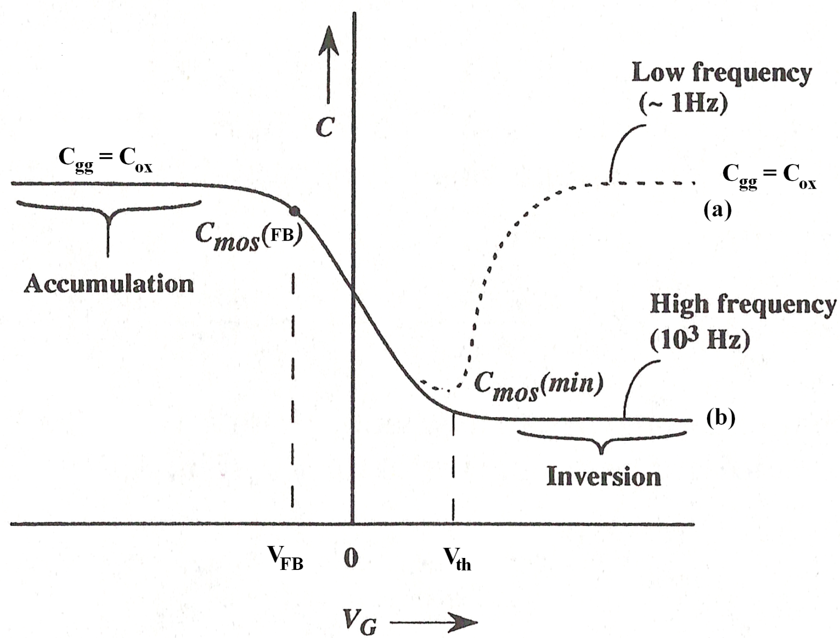

Figure 2.11: Ideal CV curve for p-type unit sized MOS-C structure, at: a) low AC test signal frequency and b) high AC test signal frequency ([32, figure 9.7a]).

depletion. The presence or non-presence of C_{jc} is hence determined by the mode of operation as will be seen, while C_{ox} is constant at all time.

By assuming a unit sized MOS-C, C_{ox} is shared between various electrodes according to the mode of operation for the MOS-C. For the review to come it is appropriate to introduce the total gate capacitance C_{gg}. It is also appropriate to introduce the gate-to-bulk capacitance C_{gb} seen between the two external electrodes V_G and V_B.

An ideal CV plot showing the total gate capacitance C_{gg} of a unit sized MOS-C under external bias is shown in figure 2.11. The three regions accumulation, depletion and inversion discussed in section 2.2.1 are clearly reflected in this plot. In accumulation region the number of positive majority carriers accumulated at the bulk-to-oxide interface is large, hence C_{gg} is on its maximum and equal to C_{ox}. With increasing gate bias in depletion region, the positive majority carriers are pushed away from the bulk-to-oxide interface and the depleted area under gate expands. In this region of operation C_{gg} is therefore reduced, since the number of positive majority carriers at the bulk-to-oxide interface is only decreasing. At V_{th}, C_{gg} reaches a minimum value. This is a result of the gate and bulk semiconductor being separated by the conducting channel. At the same time C_{jc} becomes present, created by the external node V_B and the conducting channel as the electrodes with the depleted region in the middle acting as a dielectric. Up until now C_{gb} has been equal to C_{gg}. But since the path between oxide and bulk from now on is intercepted by the channel, C_{gb} will no longer follow C_{gg}. When V_G is further increased beyond this point and into inversion, the negative minority carriers created in bulk by thermal generation are attracted towards the gate. In this region of operation the total gate capacitance C_{gg} is increasing once again, due to the increasing number of negative minority carriers at the bulk-to-oxide interface. Finally C_{gg} returns back to its maximum value C_{ox} once again, provided that the signal frequency is low enough.

It was seen that C_{gb} was intercepted by the channel when entering inversion. Hence it is appropriate to introduce the gate-to-channel capacitance C_{gc}, where the channel has replaced the electrode functionality of bulk. As C_{gb} was following C_{gg} in accumulation and depletion, C_{gc} follows C_{gg} in inversion.

In addition to the dependency of DC level on applied voltage, the MOS-C is also dependent on the signal frequency of the applied voltage. This dependency exists only in the inversion region. Inversion region is based on the supply of negative minority carriers generated in bulk as a response to the repulsion of holes. The flow of minority carriers through the substrate occurs in two directions: First is the attraction of minority carriers towards the bulk-to-oxide in inversion, while second is the repulsion of minority carriers

back towards deep bulk in accumulation. The former is achieved by means of *drift*, while the latter is achieved by *diffusion*. It has been seen that the actual direction of flow is controlled by the gate voltage. The generation and recombination of these minority carriers require a finite period of time. If these negative minority carriers are not generated or recombine fast enough according to the change in gate signal voltage, the resulting capacitance will not increase again in inversion (see equation 2.9 later in this chapter). The time required for generation is larger than that required for recombination.

Plots for the n-type MOS-C are in principle exactly the same as that for the p-type MOS-C. The major difference is that the p-type uses holes as minority carriers, while the n-type uses electrons as minority carriers. Therefore the n-type MOS-C will have an accumulation region at positive gate biases, while this is opposite for the p-type MOS-C.

2.3.2 Oxide-related capacitances

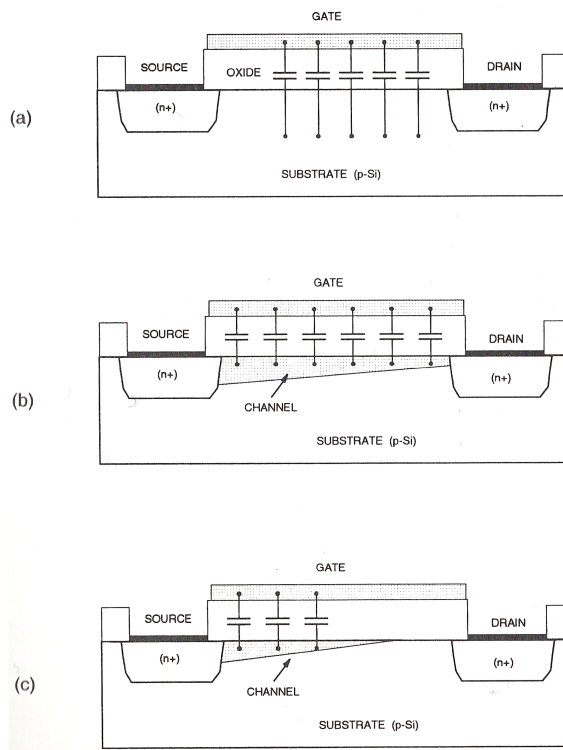

Figure 2.12: MOSFET oxide-related capacitances, dependent on shape of conducting channel according to applied bias voltage. a) cut-off b) linear c) saturation ([39, figure 3.29]).

The MOSFET oxide-related capacitances arise mainly due to a decomposition of the MOS-C total gate capacitance C_{gg} discussed in section 2.3.1, along with some fixed overlap capacitances. The value of the various decompositions depends on the region of operation for the MOSFET, as will be discussed further with reference to figure 2.12.

There are, in the most simplistic review, three locations where electrodes are overlapping each other with a non-conducting dielectric in the middle as seen in figure 2.9. The first one of these is the gate overlapping the bulk, to achieve the fundamental operation of the MOSFET as explained in section 2.2. Second and third are the gate overlapping the drain and source diffusions, respectively. These two overlaps L_{ov} are necessary to guarantee the creation of a continuous channel between the drain and source diffusions. The oxide-related parasitic capacitances associated with the MOS transistor so far thus become the gate-to-bulk C_{gb}, gate-to-drain C_{gd} and gate-to-source C_{gs} capacitance. The gate oxide in the middle acts as the dielectric.

When the MOSFET is in accumulation (equals cut-off region seen in figure 2.12a), there is no conducting channel between source and drain. C_{gd} and C_{gs} are therefore only given by the overlap L_{ov} between gate and each of the drain and source diffusions. Each of these two overlap capacitances are termed C_{ol} in figure 2.9, and are determined by the overlap area and C_{ox}. C_{gb} is however on its maximum, since there is a direct path between the bulk connection and the oxide interface.

When a conducting channel becomes present in inversion, a new situation occurs for the three oxide-related capacitances. As reviewed in section 2.3.1 the channel replaces the electrode functionality of the bulk seen by the gate, and thus effectively shields bulk from gate. Hence C_{gb} becomes zero, after gradually dropping in depletion region due to the change in carrier concentration at the bulk-to-oxide interface. On the other hand, the effective overlap area of gate to both source and drain is increased due to the conducting channel. Hence C_{gd} and C_{gs} is increased, which in sum constitute C_{gc} seen earlier and also the overlap capacitance. Two observations are thus made. First is that C_{gb} consists of a voltage-dependent capacitance component only. While second is that C_{gd} and C_{gs} consist of both a voltage-dependent capacitance component determined by the shape of the conducting channel, and a voltage-independent capacitance component determined by the fixed gate-to-diffusion overlap area. When the channel extends across the MOSFET in linear region (figure 2.12b), the total mobile charge in the conducting channel is shared between drain and source. Hence the gate-to-channel capacitance seen by each of the drain and source nodes is given by approximately half of the total mobile charge, such that the total gate-to-channel capacitance is simply split equally between drain and source. But when saturation region is entered (figure 2.12c), drain is pinched off. Hence the

gate-to-channel capacitance seen by drain is negligible, while the effective gate-to-channel capacitance seen by source is further increased. [39, chapter 3.6] approximates C_{gs} to be of around $\frac{2}{3} \cdot C_{gg}$ in this region, in addition to the two voltage-independent overlap capacitances C_{ol}.

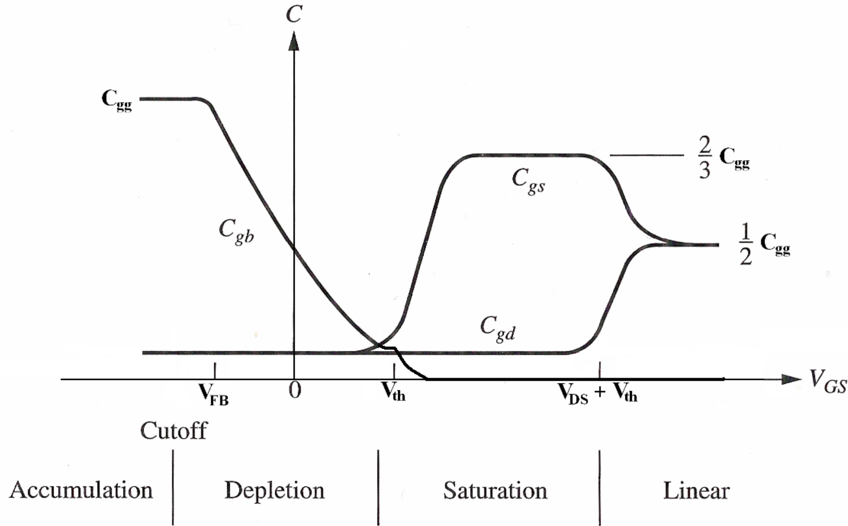

Figure 2.13: Plot of oxide-related capacitances for NMOS ([31, figure 2.18)]).

A plot showing the oxide-related capacitances for an NMOS is given in figure 2.13. It was in the introduction to this section stated that the oxide-related capacitances C_{gb}, C_{gd} and C_{gs} comprised the total MOS capacitance C_{gg} from section 2.3.1. Hence by summing these three decompositions, C_{gg} is approximately achieved. From figure 2.13 it is seen how C_{gb} is almost equal to the total MOS capacitance C_{gg} when the device is in cut-off. Further is is shown that C_{gb} drops to zero when the device enters inversion, while C_{gd} and C_{gs} share C_{gc} according to the shape of the channel.

The frequency dependency is present for the oxide-related capacitances as well, but in a rather different way than that for the basic MOS-C. Since the structure consists of drain and source diffusions in addition to the MOS-C itself, the rate of generation of minority carriers in inversion is not so crucial. Instead the device has a quick supply of these carriers from drain or source, according to whether it is an NMOS or PMOS. Hence the upper frequency of operation for the MOSFET is limited by the cut-off frequency of the MOSFET itself rather than the rate of generation and recombination. Since this cut-off frequency usually is in the GHz area, it will not represent any challenge. However, CV measurement of thin-oxide devices will dictate requirements for the signal frequency as will be seen.

2.4 Effects on the MOSFET from downscaling in CMOS process technology

There are two important aspects from downscaling in the technology geometries which are interesting specifically for this master thesis. Most parts of this section have been found in [16] and [25].

- With decreasing dimensions the parasitic capacitances associated with the MOSFET also decrease.
- As the processing technology is scaled down, the leakage currents increase.

2.4.1 Decrease in MOSFET parasitic capacitances

Parasitic capacitances associated with the MOSFET decreases with decreasing dimensions of the MOSFET. The first reason for this is the reduction in area, seen from equation 2.11 in the forthcoming section 2.5. Besides, the thickness t_{ox} of the gate oxide is scaled according to the overall technology scaling, which decreases the gate capacitance per unit area as seen from equation 2.12 in section 2.5. As an example the voltage-independent gate-to-source overlap capacitance $C_{gs_{ov}}$ can be studied, given as

$$C_{gs_{ov}} = W \cdot L_{ov} \cdot C_{ox} \tag{2.1}$$

where W is the gate width, L_{ov} is the length of overlap between gate and source, and C_{ox} is the gate capacitance per unit area. It is clear from the formula that when the dimensions and C_{ox} are decreasing, the capacitance will also decrease.

An advantage with this decrease is reduced capacitive load in the circuits, and hence reduction in charging time and power consumption. A challenge is however that this reduction in capacitance sets stronger demands to instrumentation, test setup and accomplishment of the measurements to be able to measure the small quantities.

2.4.2 Increase in leakage currents

According to [25, section II], there are three main sources for leakage current in MOSFETs:

1. Reverse-bias leakage I_{RB} in the p-n junctions when the device is reverse-biased.

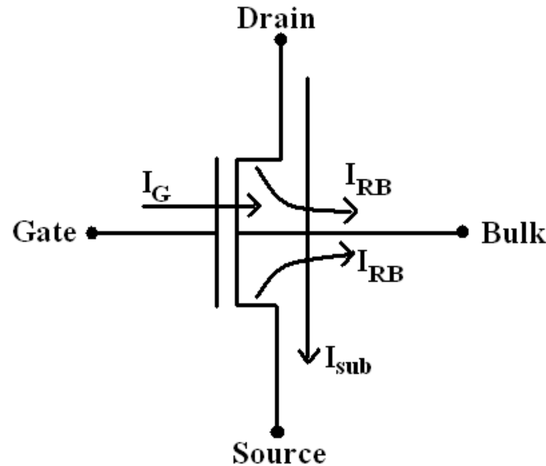

Figure 2.14: Leakage sources associated with MOSFETs, here represented by an NMOS ([25, figure 3]).

2. Subthreshold leakage current I_{sub} between drain and source when the device is reverse-biased, i.e. intended to be off.

3. Gate leakage current I_G between gate and bulk

The focus when investigating older technologies has traditionally been on the two former sources, while the latter is especially of interest regarding deep-submicron technologies. However, both source number 2 and 3 are within the scope of this master thesis.

The subthreshold leakage current I_{sub} refers to the current flowing between drain and source before V_{th} is reached. I_{sub} is caused by minority carriers flowing between drain and source already before a conducting channel is present. Hence there is a small current flow already before V_{GS} has reached the inherent V_{th} of the device. This leakage is further enhanced by the effect called DIBL[5]. With increasing V_{DS} towards inversion, substrate region at the bulk-to-oxide interface becomes partly depleted although the device is intented to be off. This makes it possible for electrons to flow. As a result, the effective V_{th} decreases and I_{sub} increases. This effect strengthens with decreasing process geometries, since the distance between drain and source typically decreases accordingly. With decreasing distance some electrons actually may become able to travel directly between the drain and source diffusions. This is called *punchthrough*, and creates a permanent on-state for the device which is not wanted.

[5]Drain-Induced Barrier Lowering

As the process geometry is reduced, the oxide thickness t_{ox} is reduced accordingly. This decrease in oxide thickness consequently brings along an increase in gate leakage I_G between gate and bulk. Gate leakage current is caused by impurities in the dielectric material, making it possible for some electrons to move through the dielectric. This is sometimes referred to a the *tunneling effect* ([18, chapter 5.10]). When t_{ox} becomes thinner, the percentage share of impurities in the oxide becomes larger. In this way the gate leakage increases with decreasing gate oxide thickness. For deep-submicron technologies I_G is becoming equal to and even larger than I_{sub}. According to [25, section II], I_G is actually more than two times that of I_{sub} for some present technologies.

This static leakage current consisting of I_G and I_{sub} may be small for a single device, but for a complete design the leakage accumulates and hence becomes a challenge regarding power consumption. One of the advantages with traditional CMOS technologies used in digital design was that power consumption was mainly dynamic, that is, power was consumed only during charging and discharging of the MOSFET parasitic capacitances during switching. With the ever increasing gate leakage however, the effect of static power consumption must be taken into account as well. And where dynamic power consumption is dependent on switching activity, the static power consumption is rather dependent on what mode of operation the device is in, the total number of transistors and what type of transistors the design consists of. This overall increase in power consumption leads to an increase in circuit temperature, and also a decrease in battery lifetime when batteries are used. The former could further increase the possibility of circuit failure, and would set higher demands to additional cooling systems. New circuit techniques for dealing with and reducing these high leakage currents is also necessary (see [25, sections III, IV and V] for an overview), but this is beyond the scope of this master thesis.

CV measurements involving MOSFET oxide-related capacitances become more complicated with increasing gate leakage. This is because more and more of the AC test signal current will flow directly through the oxide. New methods is therefore necessary to make possible measurements on thin-oxide technologies.

2.5 Mathematical foundation

2.5.1 MOSFET first-hand model equations

The following equations are taken from [22, chapter 1.5] unless otherwise specified, and describe the behavior of the n-channel MOSFET in the various regions of operation. The equations are intended for first-hand modeling,

and are thus not suitable for use in the transition between two different regions.

Effective gate voltage

$$V_{eff} = V_{GS} - V_{tn} \qquad [V] \tag{2.2}$$

Threshold voltage

The effective threshold voltage V_{th} of the technology, when taking the substrate bias (body effect, V_{SB}) into account, is given as ([22, equation 1.73])

$$V_{tn}(V_{SB}) = V_{tn0} + \gamma \cdot \left(\sqrt{V_{SB} + |2\phi_F|} - \sqrt{|2\phi_F|} \right) \qquad [V] \tag{2.3}$$

V_{tn0} = threshold voltage specifically at $V_{SB} = 0$ [V]
γ = body-effect coefficient $[V^{1/2}]$
ϕ_F = Fermi potential [V] (not specified any further, but set to -0.35V for NMOS and 0.35 for PMOS according to [22, page 70])

MOSFET in cut-off

The drain current is ideally given by

$$I_D = 0 \qquad [A] \tag{2.4}$$

In reality there will flow a small drain current in this subthreshold region as well, according to section 2.4.

MOSFET in linear (triode) region

The drain current in saturation region is given by ([22, equation 1.65])

$$I_D = \mu_n C_{ox} \left(\frac{W}{L} \right) \left[(V_{GS} - V_{tn}) V_{DS} - \frac{V_{DS}^2}{2} \right] \qquad [A] \tag{2.5}$$

where the last fraction $\frac{V_{DS}^2}{2}$ is usually ignored for the purely linear region.

Further the definition for the MOSFET drain-source conductance g_{ds} in linear region is given as ([22, equation 1.89])

$$g_{ds} \equiv \left. \frac{\partial I_D}{\partial V_{DS}} \right|_{V_{GS}=const.} \qquad [A/V] \tag{2.6}$$

MOSFET in saturation (active) region

The drain current in saturation region is given by ([22, equation 1.71])

$$I_D = \frac{\mu_n C_{ox}}{2} \left(\frac{W}{L} \right) (V_{GS} - V_{tn})^2 \left[1 + \lambda (V_{DS} - V_{eff}) \right] \qquad [A] \tag{2.7}$$

where the last term $[1 + \gamma(V_{DS} - V_{eff})]$ models the channel-length modulation, and can usually be omitted for first-hand calculations.

λ = channel-length modulation parameter [1/V]

Further the definition for the MOSFET transistor transconductance g_m in saturation region is given as ([22, equation 1.75])

$$g_m \equiv \left. \frac{\partial I_D}{\partial V_{GS}} \right|_{V_{DS}=const.} \qquad [A/V] \tag{2.8}$$

2.5.2 Definition of capacitance

The capacitance is a measure of how much electrical charge a capacitor is capable of storing, and is defined as ([6, equation 8.1])

$$C \equiv \frac{Q}{V} \qquad [F] \tag{2.9}$$

Q = charge [C]
V = potential of the body of the capacitor [V]

The intrinsic capacitance over terminals x and y of a MOSFET will be written as

$$C_{xy} = \left. \frac{\partial Q_x}{\partial V_{xy}} \right|_{V_{other}=const.} \qquad [F] \tag{2.10}$$

Capacitances associated with MOSFETs are in many ways similar to the shape of a parallel-plate capacitor. This is possible by viewing only smaller

sections of the overall MOSFET capacitance. The capacitance for a parallel-plate capacitor may be expressed as ([6, equation 8.8])

$$C = \epsilon \frac{A}{d} \qquad [F] \tag{2.11}$$

A = area of plate electrodes [m^2]
d = distance between plate electrodes [m]
ϵ = permittivity for the dielectric between the electrodes [F/m])

2.5.3 MOSFET gate capacitance

C_{ox} represents the gate capacitance per unit area for a MOSFET transistor, and is given by ([22, equation 1.56])

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{K_{ox} \cdot \epsilon_0}{t_{ox}} \qquad [F/m^2] \tag{2.12}$$

ϵ_{ox} = permittivity of gate oxide SiO_2 [F/m]
K_{ox} = relative permittivity of gate oxide SiO_2 (approximately 3.9 [dimensionless])
ϵ_0 = permittivity of vacuum ($8.854 \cdot 10^{-12}$ [F/m])
t_{ox} = thickness of gate oxide [m] (process dependent)

2.5.4 Summary of MOSFET oxide-related parasitic capacitances

Table 2.1 summarizes the oxide-related MOSFET capacitances resulting from the discussion in section 2.3.2.

Capacitance	**Accumulation**	**Depletion**	**Inversion (Linear)**	**Inversion (Saturation)**
C_{gs}	$C_{ox} \cdot W \cdot L_{ov}$	$C_{ox} \cdot W \cdot L_{ov}$	$\frac{1}{2} \cdot C_{ox} \cdot W \cdot L + C_{ox} \cdot W \cdot L_{ov}$	$\frac{2}{3} \cdot C_{ox} \cdot W \cdot L + C_{ox} \cdot W \cdot L_{ov}$
C_{gd}	$C_{ox} \cdot W \cdot L_{ov}$	$C_{ox} \cdot W \cdot L_{ov}$	$\frac{1}{2} \cdot C_{ox} \cdot W \cdot L + C_{ox} \cdot W \cdot L_{ov}$	$C_{ox} \cdot W \cdot L_{ov}$
C_{gb}	$C_{ox} \cdot W \cdot L$	Decreasing	0	0
C_{gc}	$C_{gs}+C_{gd}$	$C_{gs}+C_{gd}$	$C_{gs}+C_{gd}$	$C_{gs}+C_{gd}$
C_{gg}	$C_{gb} + C_{gc}$	$C_{gb} + C_{gc}$	$C_{gb} + C_{gc}$	$C_{gb} + C_{gc}$

Table 2.1: Formulas for calculating the MOSFET oxide-related parasitic capacitances, including both voltage-independent and -dependent components. ([39, table 3.6])

W = width [m]
L = length [m]
L_{ov} = overlap distance between the gate and each of two drain and source diffusions [m]
C_{ox} = gate capacitance per unit area [F/m]

2.5.5 Impedance

A short review of basic impedance parameters is appropriate. The following has been found in [36, chapter 1-1].

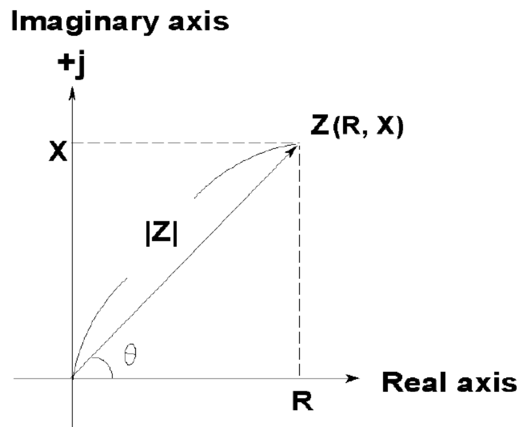

Figure 2.15: The impedance vector. ([36, figure 1-1]).

Impedance is the frequency-dependent opposition of a device. It is a complex value, consisting of a real and an imaginary part. The vector representing this complex quantity is shown in figure 2.15.

On rectangular form the impedance is given by

$$Z = R + jX \qquad [\Omega] \tag{2.13}$$

Z = impedance (complex)
j = imaginary unit
R = resistance (real)
X = reactance (imaginary)

The reactance associated with capacitance is given by

$$X_C = \frac{1}{\omega C} = \frac{1}{2\pi f C} \qquad [\Omega] \tag{2.14}$$

X_C = capacitive reactance [Ω]
C = capacitance [F]
ω = angular frequency [rad/s]
f = frequency [Hz]

while the reactance associated with inductance is given by

$$X_L = \omega L = 2\pi f L \qquad [\Omega] \tag{2.15}$$

X_L = inductive reactance [Ω]
L = inductance [H]
ω = angular frequency [rad/s]
f = frequency [Hz]

The dissipation factor D describes the loss of energy in a reactive component, and is for a capacitor specifically given as

$$D = \frac{1}{Q} = -\frac{R}{X_C} \qquad [dimensionless] \tag{2.16}$$

D = dissipation factor [dimensionless]
Q = quality factor [dimensionless]
X_C = capacitive reactance [Ω]
R = Resistance [Ω]

Chapter 3

Specifications

This chapter will introduce the specifications necessary as a framework for the measurements to be investigated. These are set according to the project text [14], the transistor specification document [38], and after consulting academic advisor. IV characterization is accomplished by applying DC voltage, while CV characterization is accomplished by applying an AC test signal superimposed on a DC voltage as will be seen in section 4.3. Because of this the former is sometimes categorized as DC measurements while the latter is sometimes categorized as AC measurements in this report.

3.1 What to be measured

Single 90nm CMOS transistors located on 90nm prototype dies shown in figure 3.1 are to be characterized. These prototype dies have most recently been delivered by the semiconductor fabrication facility, situated on a die-level. The fabrication of these prototype dies was initiated by IET NTNU.

3.2 DC measurements

The DC characteristics of the 90nm transistors are to be investigated at room temperature. Generally the IV-characteristics for I_D as a function of both V_{GS}, V_{DS} and V_{SB} are of interest. More specifically the leakage-currents IG and I_{sub} are important parameters to be investigated, and also the influence of body effect and channel-length modulation.

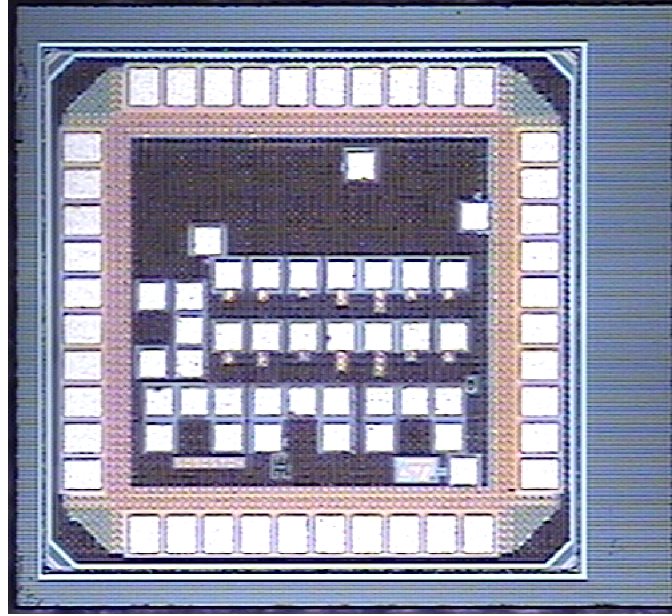

Figure 3.1: 90nm prototype die.

3.3 AC measurements

Regarding AC measurements, this master thesis will include work on finding a suitable CV measurement methodology for the characterization of deep-submicron devices with very thin gate oxides. Further, measurement of MOSFET capacitance with respect to the 90nm transistors is to be accomplished, by carrying out the methodology found. More specifically the oxide-related capacitances are of interest. The work should also include in a discussion about the layout of the prototype dies regarding suitability for CV measurements.

3.4 Dimensions for 90nm transistors

The 90nm physical devices on the 90nm prototype dies to be investigated have dimensions as specified in table 3.1 ([38]), where all are of SVT[1]. The four NMOS transistors share common gate, source and bulk. This is also the case for the four PMOS transistors. Parameter m is a device multiplier, indicating that each superior device consists of 10 transistors in parallel with the given dimensions. W, and hence the gate area must therefore be multiplied with 10 to find the total geometry for each device.

[1]Standard threshold voltage.

Device	**Width** W [μm]	**Length** L [μm]	**M**
`nmos0`	1.2	0.1	10
`nmos1`	1.0	0.2	10
`nmos2`	4.0	0.5	10
`nmos3`	4.0	1.0	10
`pmos0`	3.0	0.1	10
`pmos1`	1.0	0.2	10
`pmos2`	8.0	0.5	10
`pmos3`	8.0	1.0	10

Table 3.1: Dimensions for 90nm transistors

There are a total of 15 dies available, all containing the same eight MOSFETs. These dies are identified by type-number SO9C57D4 and run-number SO9C5-7.

Chapter 4

Test setup

This chapter will present the overall test plans both for simulations and physical measurements, along with the setup of test equipment and instrumentation to accomplish the measurements.

A complete equipment list for instrumentation used in the physical measurements can be found in appendix A.

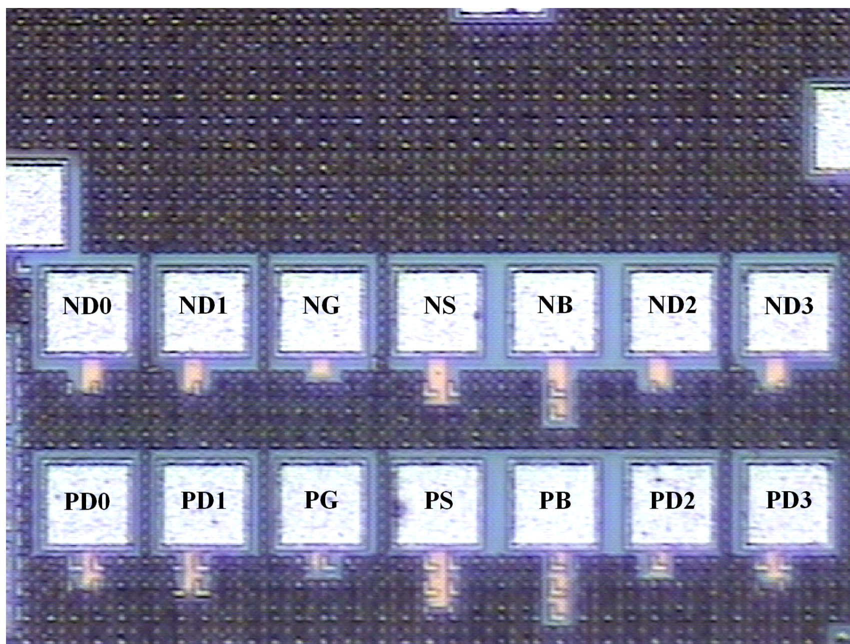

Figure 4.1: Test pads on 90nm prototype dies.

The actual test pads to be used when accomplishing measurements on the 90nm prototype dies are shown in figure 4.1. Here D, G, S and B indi-

cates drain, gate, source and bulk respectively, N and P indicates nmos and pmos, while the drain numbering refers to the device number. Each pad is approximately $100\mu m$ on each side.

4.1 DC measurements for 90nm transistors

For DC measurements on the 90nm transistors there are 6 different tests of interest. These are

- Threshold voltage V_{th}
- Subthreshold leakage current I_{sub}
- V_{DS}-I_D in forward-bias, and from this extracting g_{ds}
- V_{GS}-I_D in forward-bias, and from this extracting g_m
- Gate leakage current I_G, both in reverse- and forward-bias
- Influence of body effect

Sweep combinations consisting of the following are to be used for NMOS devices:

- V_{GS} swept from 0V to 1V in 0.05V steps (from -0.5V for subthreshold calculations)
- V_{DS} swept from 0V to 1V in 0.05V steps
- V_{SB} swept from 0V to 0.2V in 0.1V steps

While the sweep combinations to be used for PMOS devices are:

- V_{GS} swept from 0V to -1V in -0.05V steps (from 0.5V for subthreshold calculations)
- V_{DS} swept from 0V to -1V in -0.05V steps
- V_{SB} swept from 0V to -0.2V in -0.1V steps

All physical DC measurements will be achieved by using the SUMMIT 11561B probe station from Cascade Microtech in combination with the SCS-4200 Semiconductor Characterization System from Keithley. The DC analyzer includes a Microsoft Windows-based integrated test program environment called KITE[1], providing the necessary setup and control facilities for the analyzer. [20] presents the use for this DC analyzer and how to achieve the desirable IV characteristics. An introduction to the use of the probe station has been found in [33].

[1] Keithley Interactive Test Environment

4.2 AC measurements for 90nm transistors

For AC measurements the following tests are of interest

- Gate-to-bulk capacitance C_{gb} (oxide-related capacitance)
- Gate-to-channel capacitance C_{gc} (oxide-related capacitance)
- Total gate capacitance C_{gg} (oxide-related capacitance)

All physical AC measurements will be achieved by using the SUMMIT 11561B probe station from Cascade Microtech in combination with the 4294A Precision Impedance Analyzer from Agilent. [1] has been used as a reference for learning how to operate this instrument. In addition, [3] and [4] presents the use of the AC analyzer in combination with the Cascade Microtech probe station and measurement of very thin gate oxides. For measurements depending on external DC bias in addition to that provided by the 4294A, the Keithley 4200-SCS will be used.

4.3 Measurement methodology for CV characterization

According to the specifications in chapter 3, it was of special interest to find a proper test procedure for the preparation and execution of CV measurements for the oxide-related capacitances. This procedure is necessary for obtaining accurate CV results. Information about this has been found in [2], [5], [10], [11], [18], [19, appendix K], [21], [26], [27] and [36]. A guide on accomplishing basic CV measurements with the Agilent 4294A is given in appendix B.

4.3.1 Instrumentation setup and choice of measurement method

The *Auto-Balancing Bridge method* (ABB) is chosen as the measuring method, as this is suitable for impedance measurement over a wide test signal frequency range ([36, sections 2.1 and 2.3]). The Agilent 4294A is based on this method, and covers test signal frequencies from 40Hz to 110MHz. This fits very well for general measurements on a variety of devices, including the MOSFET parasitic capacitances. This 4294A is a necessity for measuring low parasitic capacitance precisely and with sufficient resolution. One limitation of the ABB method however is that it is not capable of accomplishing measurements at very high frequencies (RF), but this is not of interest for this master thesis.

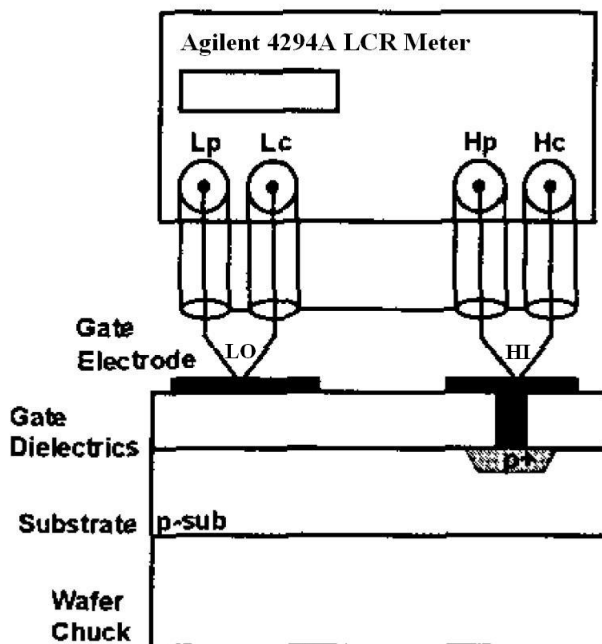

Figure 4.2: Basic setup for CV measurements ([26, figure 2]).

The terminal configuration to be used is the 4TP[2] with a 1 meter direct BNC[3]-to-SSMC[4] coaxial cable. A length of 1 meter is preferred over the 2 meter, since it has better high-frequency properties. The length of this cable and the terminal configuration must be specified in the setup of the 4294A before any measurement takes place, and is part of the cable compensation. This is necessary so that the Agilent 4294A becomes able to compensate for the propagation delay and internal capacitance through the extension cable. In general for 4TP configuration the user must always provide for that the length of the cable is kept safely below the wavelength of the applied measurement signal, as reviewed in [36, chapter 3-2]. The Agilent 4294A is however capable of operating with test frequencies much higher than that limited by this general rule, by matching its test circuit impedance with the characteristic impedance of the coaxial 4TP cables at high frequencies ([36, page 3-5]).

The probe station, chuck, chamber, probes and test cables are specially de-

[2] *Four-Terminal Pair.* The purpose of the 4TP concept is to reduce errors introduced by the test cables at high frequencies, and hence make measurements more accurate. This is achieved by having the voltage sensing lines and the current conducting lines separated, hence reducing the lead impedance ([36, pages 3-1 and 3-2]).

[3] Bayonet Nut Connector.

[4] (Screw-on mating) microminiature coaxial connector.

signed to allow for measurements of very small quantities, excluding the parasitic effects of the test system itself. Thus the use of this special equipment ensures high accuracy on the measurements. Probes used for the CV measurements are of a guarded, coaxial type. The enclosing chamber acts as a Faraday cage, by reducing the external electromagnetic and electrostatic noise from entering the DUT. The only openings into the chamber are those allowing access for the probes and microscope. Coaxial cables delivered by Cascade Microtech and approved by Agilent are used for accomplishing the 4TP connection setup, and is connected directly between the 4294A and the probes. With coaxial cables the influence of external electromagnetic fields is reduced to a great extent. These cables are specially built for high frequencies. Characteristic impedance of the coaxial cables is 50Ω, to match the 4294A. The alternative to using the direct 4TP SSMC-to-BNC coaxial test cables would be to use the existing triaxial setup of the probe station, with coaxial-to-triaxial adapters between the 4294A and the probe station. Practical experiments have however shown that this gives less accurate results than that of the direct connection method ([34]).

Finally the so-called *AttoGuard* system provided by Cascade should be used. This is an additional plate placed over the DUT in the microchamber, which reduces the effective aperture opening for the probes to the DUT. Hence the chamber becomes more unaffected of external influence, by providing DUT and chuck better shielding from probes and other external sources.

4.3.2 Connecting the DUT to measurement instruments

The HI and LO terminal side of the Agilent 4294A impedance analyzer are to be connected to each side of the capacitor structure of interest, as introductory illustrated in figure 4.2. Only the coaxial probes are used for measuring the capacitance itself, while the two additional probes are available for external DC bias purposes via the Keithley 4200-SCS. If a bulk contact pad is not available on the top of the wafer, probing of bulk must be accomplished through the chuck. This is however not a recommended method, since it reduces the test signal frequency range available ([4, chapter 5]). The 90nm prototype dies available have however dedicated test pads for bulk on top of the wafers as seen before.

The choice of connection between the probe station, instrumentation and DUT depends on the parameters to be measured, and is therefore not necessarily as simple as that shown in figure 4.2. Much of the literature investigated use the two-terminal MOS-C for illustrative purposes but also as the device to be measured, excluding many of the practical challenges associated with capacitance measurements on four-terminal MOSFETs. Some articles also use special test structures particularly designed according to the parameter to be measured. More practical examples of measurements

on four-terminal MOSFETs in particular have been found in [17], [35, chapter 3.2] and [36, chapter 5-5].

Gate-to-source capacitance C_{gs}

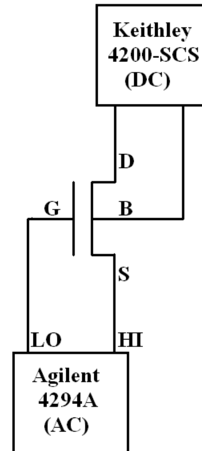

Figure 4.3: Hardware connection for measuring C_{gs}.

C_{gs} is found by connecting source to HI and LO to gate, while drain and bulk are connected to the 4200-SCS (figure 4.3). Here the HI on source will provide for sweeping V_{SG} during the CV measurement, since gate is at virtual ground. Since a V_{SG} is applied, the result must therefore be mirror imaged to achieve V_{GS}. In this setup the bulk voltage may be changed before each CV sweep to investigate the influence of body effect, while the DC bias on drain is used to set the initial V_{DS}. These bias settings are made according to figure 2.13, where it is seen that C_{gs} is a function of V_{GS} and V_{DS}. The measured C_{gs} will include the voltage-independent overlap capacitance of the source diffusion.

Gate-to-drain capacitance C_{gd}

Measurement of C_{gd} is found by connecting HI to drain and LO to gate, while source and bulk are connected to the 4200-SCS for DC bias purposes (figure 4.4). Overlap capacitance for the drain diffusion will be included in the measured value as well. The actual sweeping of V_{GS} is here accomplished by stepping the DC bias on source initially before each CV measurement, since gate is at virtual ground. During the CV measurement, V_{DS} is swept since drain is connected to the HI node. So the setting of V_{DS} and V_{GS} when measuring C_{gd} is quite opposite of that when measuring C_{gs}. As for

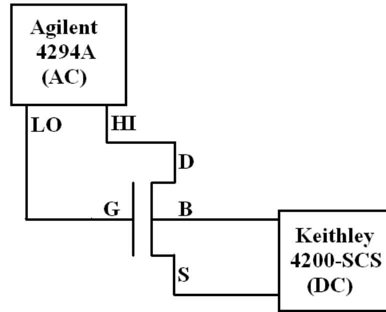

Figure 4.4: Hardware connection for measuring C_{gd}.

C_{gs}, the DC bias on bulk may be used to investigate the body effect. All of these bias settings for C_{gd} are made according to figure 2.13 in the same way as was seen with C_{gs}.

Gate-to-bulk capacitance C_{gb}

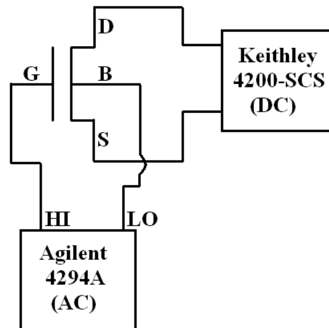

Figure 4.5: Hardware connection for measuring C_{gb}.

The first method of measuring C_{gb} is to connect HI to gate and LO to bulk, while at the same time using the Keithley SCS-4200 to bias both drain and source to a common voltage (figure 4.5). In this way there will be no effective potential difference between drain and source, but rather between these nodes relative to bulk. Drain and source will function as external sources of minority carriers when the device enters inversion. Measuring C_{gb} in accumulation and depletion is in practice the same as measuring C_{gg} in accumulation and depletion.

According to [36, chapter 5-6] and [21] it is preferred to actually make the opposite connection. That is, connect bulk to the HI terminal and gate to LO. The reason for this is that the large chuck area will function as a pickup

for external noise. Since the LO terminal is very sensitive to noise due to properties of the ABB method, this will therefore affect the measurement to a large extent when this noise is transferred from chuck to bulk via the backside of the die. In addition the chuck itself represents an additional increase in parasitic capacitance, which would have to be accounted for.

The second method is to let drain and source be floating, and make the measurement connection between bulk and gate similar to that in the first method. HI then goes to the gate pad, while LO goes to the bulk pad. The capacitance will be very similar to that measured with the first method, except from that it has no external supply of minority carriers from drain or source at the transition from depletion to inversion since these are floating and hence not electrically in contact with the conducting channel. This means that these minority carriers must be generated by thermal generation in bulk. Since this process of generation needs a specific time, it can not cope with the high frequency of the test signal. Therefore the curve does not drop toward $C_{gb} = 0F$ at V_{th} in inversion, but rather settles at a finite value.

Gate-to-channel capacitance C_{gc}

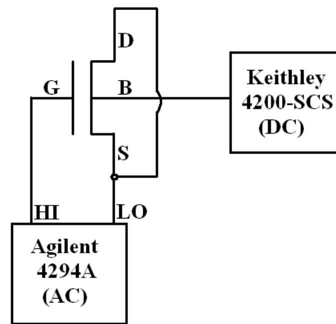

Figure 4.6: Hardware connection for measuring C_{gc}.

The gate-to-channel capacitance C_{gc} is measured by connecting both drain and source to the LO node, while gate is connected to the HI node (figure 4.6). Bulk is connected to the 4200-SCS, to set the level of V_{SB}. In this way the capacitance between gate and the electrode consisting of the inverted channel is effectively measured, since drain and source are at virtual ground. Measuring C_{gc} in inversion is the same as measuring C_{gg} in inversion. It is obvious that C_{gc} will include the voltage-independent overlap capacitances of drain and source in accumulation, depletion and inversion.

Total gate capacitance C_{gg}

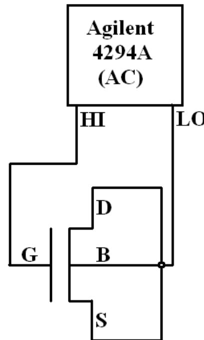

Figure 4.7: Hardware connection for measuring C_{gg}.

For measuring C_{gg} it is necessary to create a two-terminal MOS-C out of the four-terminal MOSFET. This is achieved by connecting drain, source and bulk together while leaving gate separate. Hence $V_{SB} = V_{DB} = 0V$. Further the HI node of the 4294A is connected to gate, while LO goes to the common drain-source-bulk node (figure 4.7). It is obvious that the measurement of C_{gg} consists of only one sweep. As indicated previously and also reviewed in the theory, C_{gg} is composed by C_{gb} in accumulation and depletion and C_{gc} in inversion. Similar, the voltage-independent overlap capacitances of drain and source are included in C_{gg} in all of these three regions.

Some parts of the literature advise that this arrangement of creating the MOS-C structure should be accomplished already at the layout stage, letting drain, bulk and source share one common test pad while gate has a separate test pad. The advantage with this layout is that it will not require the connection of drain, bulk and source to be accomplished manually by connecting three probes in a daisy-chain configuration. This latter could perhaps complicate the compensation procedure, and introduce additional parasitic capacitances. The drawback however is that this test-structure will limit the measurements to C_{gg} only, since the layout is fixed to a two-terminal MOS-C structure.

Two-probe method versus four-probe method

In accordance with the discussion above, it is for some capacitance measurements possible to choose between using the two-probe method (figure 4.8a)) and the four-probe method (figure 4.8b)). The four-probe method is dependent on an external DC source in addition to the CV meter itself, while only the CV meter is sufficient for the two-probe method. The two-probe method offers the most simple setup of the two. This utilizes the two

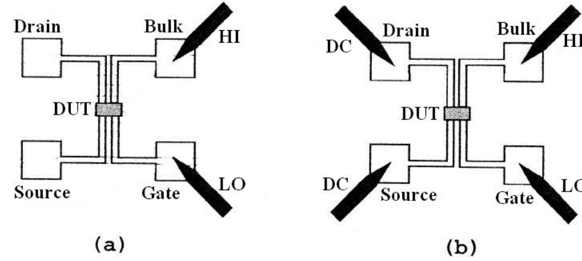

Figure 4.8: CV measurements, using a) Two-probe method b) Four-probe method ([5, figure 1]).

coaxial probes for the capacitance to be measured, while the two additional pads are left floating. It is suitable for measurements where there is no need for additional DC biasing in addition to that provided by the CV meter. A major disadvantage with the two-probe method is however that it does not resemble the normal connection of a MOSFET, since it leaves some nodes floating. All capacitances in parallel with the capacitance under test will as a result be included in the measurement ([35, chapter 3.2, page 8]), and hence the resulting capacitance measured becomes slightly larger than expected. This is an important argument for why this method in general should be avoided.

With the four-probe method it is required to ensure that the 4200-SCS is using the same ground level as the 4294A. The ABB method of the 4294A creates a *virtual ground* on its LO-node. That is, it is held at a constant voltage referred to the HI node. This means that it is not a genuine earth ground, but instead a ground that is actively enforced by the 4294A. Therefore the ground level of the 4200-SCS must also be utilized such that it is capable of dynamically follow this virtual ground. This is obtained by removing the metal link between chassis GND and COMMON on the back of the 4200-SCS, and then connecting the virtual ground of the 4294A to this COMMON terminal of the 4200-SCS. According to the ABB structure, this virtual ground is connected to the shielding (guard) of the HI and LO ports ([36, chapter 2-4-7] and [35, chapter 3.2, page 3]). Now the 4200-SCS will dynamically adjust its COMMON level according to the virtual ground, and hence be capable of creating a well defined voltage between its outputs and the LO node of the 4294A. The four-probe method may now be used to measure the capacitances where there is need for additional DC bias. Note that for capacitance measurements where only the two-probe method is strictly necessary, it is still favourable to bias the two additional nodes to zero volts. In this way these nodes are connected to the COMMON level of the ABB, and the additional parallel capacitances are not included

in the measurements. In between the two- and four-probe method is the three-probe method, which can be used for measurements where it is found sufficient to apply external DC bias to only one additional node.

4.3.3 Compensation and calibration

Calibration, which defines the reference plane with a specified accuracy for the Agilent 4294A, is assumed performed regularly by those responsible for the laboratory. Therefore this is not necessary to perform before using the 4294A. According to [36, table 2-2], the basic measurement accuracy of the 4294A is 0.08% of the reading. However, before any measurements, phase and fixture **compensation** for the 4294A is required. This compensation is also necessary in all cases where the test conditions has changed since a previous compensation (e.g. change in distance between measuring cables, or change in relative distance between probes). The compensation eliminates, or at best reduces, the effect of stray capacitance in the test setup due to the 4294A itself, test cables and probes. In this way any parasitics introduced between the reference plane of 4294A and the probe tips are taken into account. The accuracy of the measurement will however still suffer from the additional parasitics caused by additional on-die structures other than the DUT itself. Fixture compensation is achieved by using the ISS[5] provided by Cascade Microtech. The result of the compensation is most easily verified by measuring the reference capacitors on the ISS. It is very important to set the 4294A to maximum accuracy before accomplishing compensation. Once the test cables between the 4294A and the probe station have been connected and compensation is complete, the positioning of these cables and the probes relative to each other is not allowed to be disturbed. Otherwise compensation must be accomplished all over again.

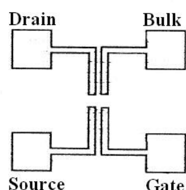

Figure 4.9: Dummy-structure for excluding on-die parasitics ([5, figure 1]).

To additionally take the parasitic effects of the on-die DUT electrodes into account (e.g. pad capacitance, wire capacitance, contact resistance), it is recommended that a dummy-structure is included on the die layout ([5, section

[5]Impedance Standard Substrate.

I]). The dummy will include everything except from the DUT itself. This is shown in figure 4.9. Any capacitance represented by this structure can then be measured, and hence subtracted from the capacitance value measured for the device of actual interest. This elimination is very valuable sine an exact, known value for the additional on-die capacitances are found. These on-die capacitances increase the overall level of the capacitances measured for the DUT.

4.3.4 Accomplishment of measurements

The CV measurement itself is accomplished by applying an AC signal superimposed on a DC voltage over the device to be characterized, and then reading off the resulting AC current. This AC test signal on DC level is applied by the HI terminal of the 4294A, while the resulting AC current flow is sensed at the LO terminal ([40, page 152]). From this the impedanze Z is given as the total frequency-dependent opposition of the specific device, according to equation 2.13. For DC bias dependent devices the maximum DC voltage range over which the capacitance can be measured is determined by the safe operating voltage for the oxide. Exceeding this limit does not automatically mean that the oxide is damaged, but the oxide will at least accumulate defects more rapidly. At a given breakdown voltage however the oxide will eventually be destroyed. From this it is obvious that there exist intermediate breakdown states, from which the device is capable of recovering as long as the accumulation of defects have not become large enough ([29, page 46]). For the 90nm technology investigated in this master thesis a maximum of 1V over any two nodes was allowed, hence the voltage was generally swept between -1V and +1V.

When performing the CV measurements, it is preferable to sweep from inversion to accumulation ([21, pp. 3-4]). Assuming that a fixed voltage bias is initially applied before sweeping takes place and looking at C_{gb}, C_{gb} starts in depletion and moves toward inversion. Eventually C_{gb} stabilizes in inversion, at equilibrium conditions for the semiconductor. Now the C_{gb} is ready for having the bias voltage swept. As the sweeping takes place, the dependency of sweep rate is not so prominent since the recombination rate for the minority carriers in bulk is quite fast. However, when sweeping in the opposite direction (from accumulation to inversion), the dependency of sweep rate is more prominent. The reason for this is that the generation rate for minority carriers in bulk to create the conducting channel when entering inversion region is much slower than that for the recombination rate. Hence sweeping from inversion to accumulation may utilize a faster sweep rate, and thus also ensures a more correct measurement irrespective of sweep rate. To ensure that C_{gb} initially enters inversion, a light-pulse may be applied before sweeping takes place to force it to generate minority carriers.

Another important setup when performing the actual measurements is to allow for enough hold time at a given bias. This is necessary since capacitances associated with the MOSFET need a given time to become fully charged. Setup of this is specified by using the bandwidth functionality of the 4294A. In addition the averaging functionality of the 4294A should be used to suppress random irregularities during the measurements. The choice of precision is a trade-off between speed and accuracy of the measurements. Finally, the overall precision of the measurement should be set for the x-axis of the 4294A. This is accomplished through the settings of start voltage, stop voltage and total number of points. These settings are compromises between precision and speed as well.

The setting of AC test signal frequency and AC test signal amplitude is also of importance for the measurement results. Since the operation of the MOSFET itself in principle is not dependent on AC test signal level, it is preferable to use a low-level signal ranging from a few mV rms to approximately 100mV rms. Main reason for this is to avoid altering the effective DC bias level applied. The test signal frequency must be chosen on the basis of having to measure very thin gate oxides. According to [7], this is achieved by increasing the test frequency above that usually used for thicker gate oxides. The reason for this is that the thin gate oxide has a very low inherent capacitance, and also a lot of leakage current. A low capacitance consequently results in a very high impedance, as seen from the mathematical relations in section 2.5.5. In addition, the leaky oxide is more resistive than capacitive for low frequencies when a high voltage bias is applied. This means that much of the test signal will flow as leakage current, resulting in an additional decrease in capacitance. Both of these two aspects complicates the CV measurements of very thin gate oxides. The result is an unwanted lowering in the capacitance level in accumulation ([15]). The Agilent 4294A is in general optimized for measuring impedance levels around 50Ω, and by referring to equation 2.15 it is seen that the test signal frequency therefore should be high for low capacitances. By increasing the test signal frequency, the impedance level to be measured is lowered toward that optimum for the 4294A. Secondly the effect of the gate leakage is suppressed, by making the capacitive part of the oxide more prominent than the resistive part. [36, chapter 5-6] states that the frequency should be set to 1MHz or higher for thin-oxide technologies, which is much more than that used for thicker gate oxides. A more complete review of component dependency factors for various devices can be found in [36, chapter 1-5].

For making capacitance measurements of thin-oxide devices, it is favorable to employ a large MOSFET. In this way larger the parasitic capacitances to be measured becomes larger and hence more measurable. It also reduces the impact from short-transistor effects and overlap effects. Alternatively a large MOSFET can be made out of smaller sub-devices in parallel, if the

test transistors are originally meant to be used for other test purposes as well.

Finally, it is of importance to notice that repeated measurements executed with the same test setup may still generate different results. [36, chapter 4-7] lists ambient temperature variations, change in contact conditions between DUT and probes, change in conditions when performing compensation, and electromagnetic coupling with various external conductors near DUT as some of the important factors that may cause these differences. These variations may occur despite all the precautions that have been stated in this measurement methodology.

4.3.5 Extraction of capacitance from measured impedance

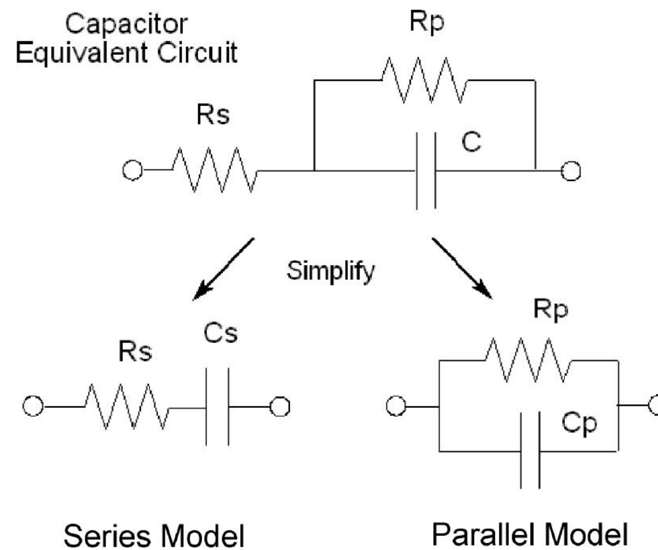

Figure 4.10: Two-parameter equivalent circuits modeling the capacitor ([2, figure 3-1]).

An important aspect with impedance measurement instruments in general is how they actually perform the measurement of for example capacitance of a MOSFET. As the name implies, they do not measure the capacitance directly. Instead the complex impedance Z of the device is measured, according to the relations in section 2.5.5. The physical structure of the capacitor is usually modeled by a three- or higher-parameter equivalent circuit, since there are no devices that are purely resistive, capacitive or inductive. The typical three-parameter equivalent for a capacitor is shown at the top in figure 4.10. For simplification purposes it is necessary to reduce this more realistic three-parameter model into one of two two-parameter models shown

at the bottom of figure 4.10. The first equivalent is a capacitor C_p in parallel with a resistor R_p, while the second one is a capacitor C_s in series with a resistor R_s. Here R_s represents the parasitics associated with the wiring and capacitor electrodes, while R_p represents the leaky dielectric ([36, chapter 5-1]). Based on one of these two-parameter equivalent circuits, the capacitance is then derived from the measured impedance. These two both have their advantages and disadvantages when it comes to modeling the capacitance of the MOSFET in a correct manner, according to what kind of additional parasitic effect R_s or R_p is to be emphasized. [36] gives a more in-depth review on this topic. The Agilent 4294A is equipped with both of these two basic two-parameter equivalent circuits.

A choice must be made between using the series and the parallel equivalent circuit to obtain a set of calculated capacitance values. Since this master thesis involve CV measurements of ultra-thin oxides, it is preferable to use the parallel equivalent because of the leaky oxide modeled by R_p. The 4294A also has a built-in Equivalent Circuit Analysis Function for investigating the results with a three- or four-terminal model directly ([1, pp. 249-253]), specially included for the analysis of ultra-thin dielectrics. This opportunity is however not investigated in this report.

It has been an interesting discussion in recent years about how to model the MOSFET capacitance of deep-submircon devices most correctly. The discussion in general concludes with that this challenge calls for at least a three-parameter equivalent circuit instead of the simplistic two-parameter equivalent. This to take the increase in gate leakage better into account. [7] gives a very good overview of the evolution in this discussion.

4.4 Simulation setup

4.4.1 90nm transistors

All simulations will be accomplished by using the SPICE model cards provided by the supplier of the actual 90nm CMOS technology. These files model the 90nm MOSFETs at the Berkeley SPICE BSIM3v3.2.4[6] level (Eldo level 53). It is important to accomplish simulations with a setup as close as possible to that used for physical measurements. This is mainly obtained by using the same device sizes as that specified in chapter 3 and the same device connections as that on the prototype dies.

The following simulation corners are of interest for investigating the measurement results:

- TT - NMOS typical, PMOS typical

[6]Berkeley Short-channel IGFET Model, version 3.2.4

- FF - NMOS fast, PMOS fast
- SS - NMOS slow, PMOS slow
- SSA - NMOS slow, PMOS slow, analog corners included

SSA represents here the absolute minimum that the measurements ideally should not go below.

All files used for DC and AC simulations are given in appendix C. Since the same files have been used for all types of sweeps and connections scenarios, each file listing only represent one of these scenarios.

The setup for the DC simulations will follow the sweep plan given in 4.1. For AC simulations the setup will be dictated by the experience achieved through chapter 7. The most important aspect when accomplishing AC measurements is to leave any nodes that are floating in the measurements also floating in the simulations. Any additional information about the DC and AC simulations will be given as the results are presented.

Chapter 5

Results for DC measurements at room temperature

The following presents the plots for all DC measurements (solid line), along with TT corner simulations (dotted line, in the middle), SS corner simulations (dashdot line, least extreme value), FF corner simulations (dashed line, most extreme value) and SSA corner simulations (big black dots, a little less extreme than SS) - at room temperature 27°.

Die 1, 2, 4 and 5 were investigated. In this way, any abnormal individual result could be compared and hence detected. The same sweep and step method was used for all of the different MOSFETs. All DC measurements have been accomplished in total darkness.

To take typical deep-submicron leakage into account in the simulations, a model-card named *nsvt_leak* was used for all simulations.

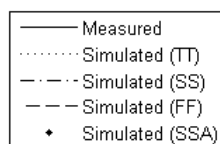

Figure 5.1: Legend for all DC plots.

The following devices are plotted:

- die2_nmos0
- die2_nmos1

- die1_nmos2
- die1_nmos3
- die5_pmos0
- die5_pmos1
- die2_pmos2
- die2_pmos3

For the evaluation of the g_{ds} and g_m, these parameters were calculated manually by using the values of I_D, V_{GS} and V_{DS}. Hence, to make the comparison between simulated and measured values, the values of g_{ds} and g_m automatically generated by Eldo were not used.

Since the nmos and pmos devices on the dies were separately sharing drain, source and bulk, the gate leakage I_G measured was with respect to all these 4 devices acting as one device. It was further necessary to find the gate leakage for each individual device. This was achieved by multiplying the total gate leakage with the ratio of the specific device gate area to the total device gate area of all four devices ($63.2\mu m^2$ for NMOS and $125.0\mu m^2$ for PMOS). Simulations were accomplished with this test setup as well, such that the prerequisites for simulations were as close to that of the physical measurements ([37]).

Contents is as follows:

1. V_{DS} - I_D at $V_{SB} = 0.0V$
2. V_{DS} - g_{ds} at $V_{SB} = 0.0V$
3. V_{GS} - I_D at $V_{SB} = 0.0V$
4. V_{GS} - g_m at $V_{SB} = 0.0V$
5. Subthreshold leakage current at $V_{DS} = 0.1V$ and $V_{DS} = 0.5V$ for nmos devices, and $V_{DS} = -0.1V$ and $V_{DS} = -0.5V$ for pmos devices, both at $V_{SB} = 0.0V$
6. Gate-leakage I_G at $V_{DS} = 0.0V$, $V_{SB} = 0.0V$
7. Body-effect by comparing $V_{SB} = 0.0V$ with $V_{SB} = 0.2V$ for nmos devices, and $V_{SB} = 0.0V$ with $V_{SB} = -0.2V$ for pmos devices, at $V_{DS} = 0.5V$ for nmos and $V_{DS} = -0.5V$ for pmos.

Three measurement-series per plot are included for the general IV-measurements.

5.1 nmos0

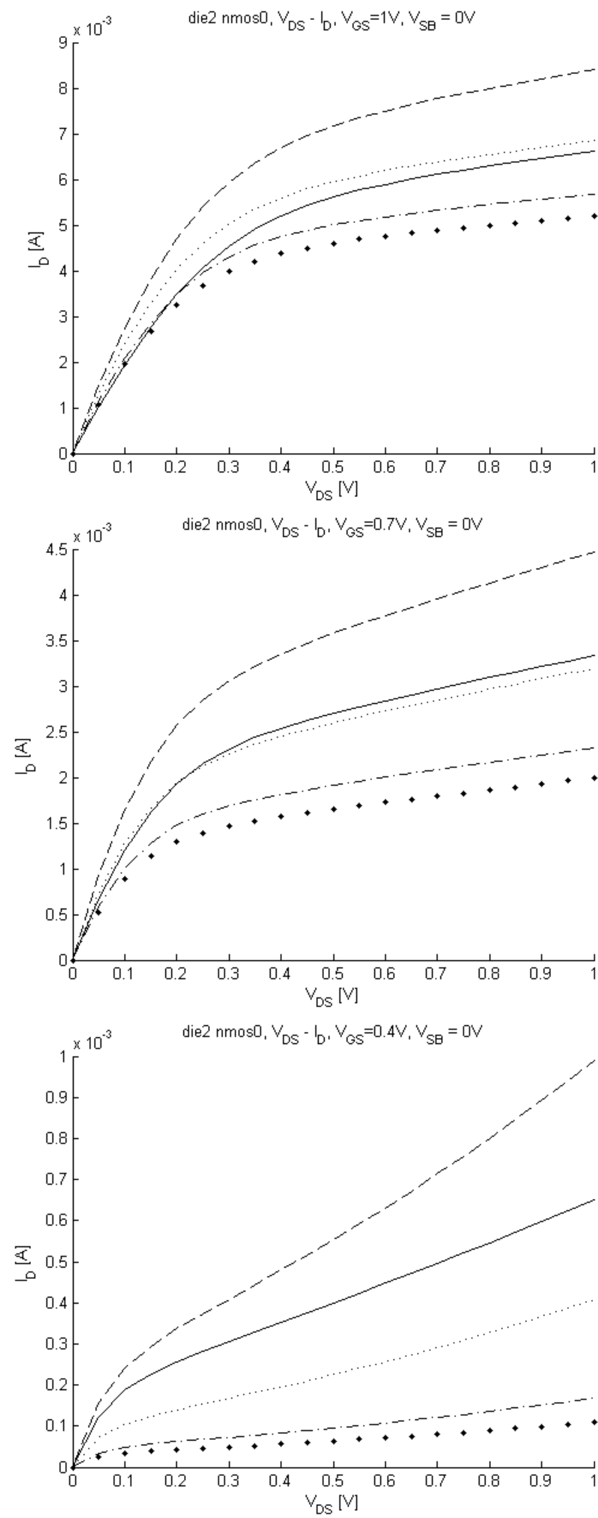

Figure 5.2: die2_nmos0 $V_{DS} - I_D$.

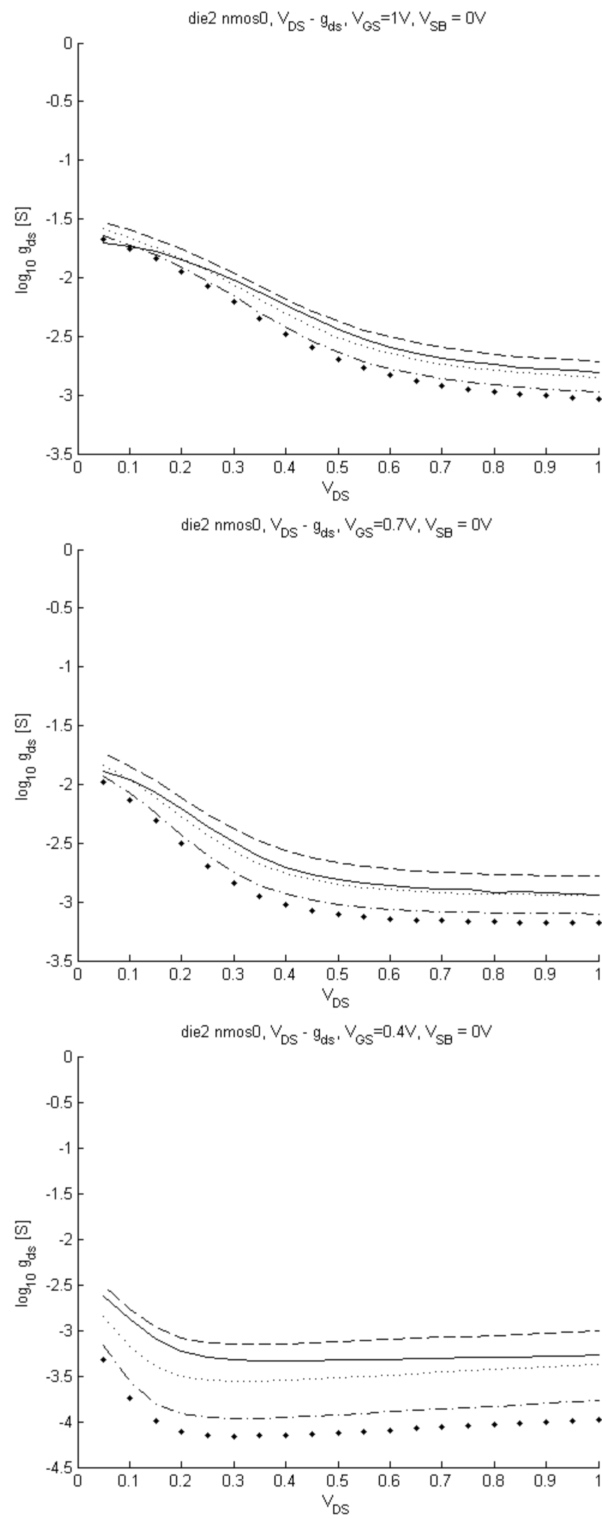

Figure 5.3: die2_nmos0 drain-source conductance g_{ds}.

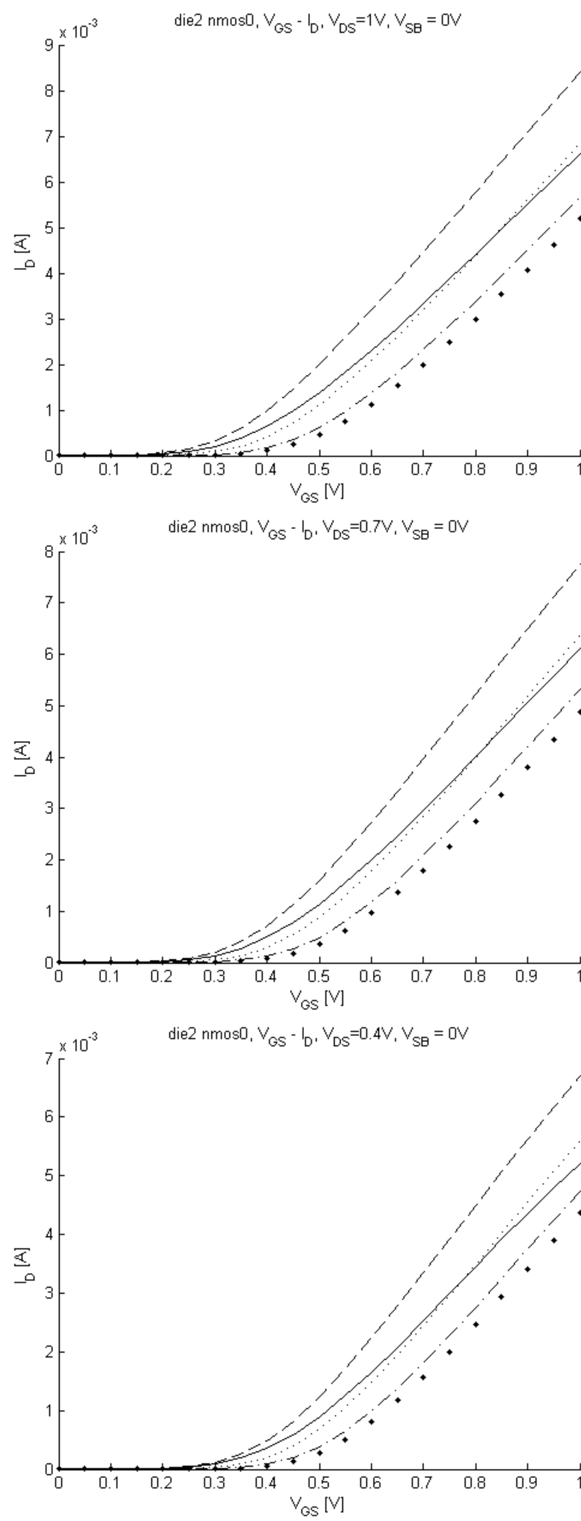

Figure 5.4: die2_nmos0 $V_{GS} - I_D$.

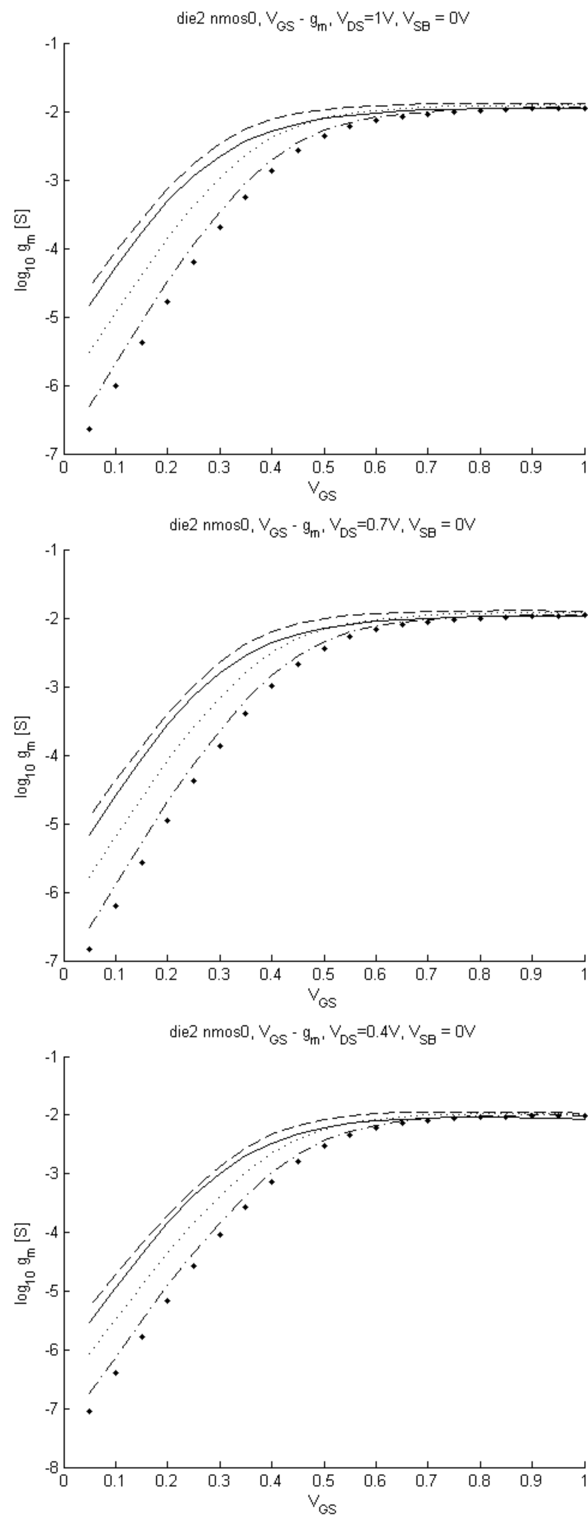

Figure 5.5: die2_nmos0 transconductance g_m.

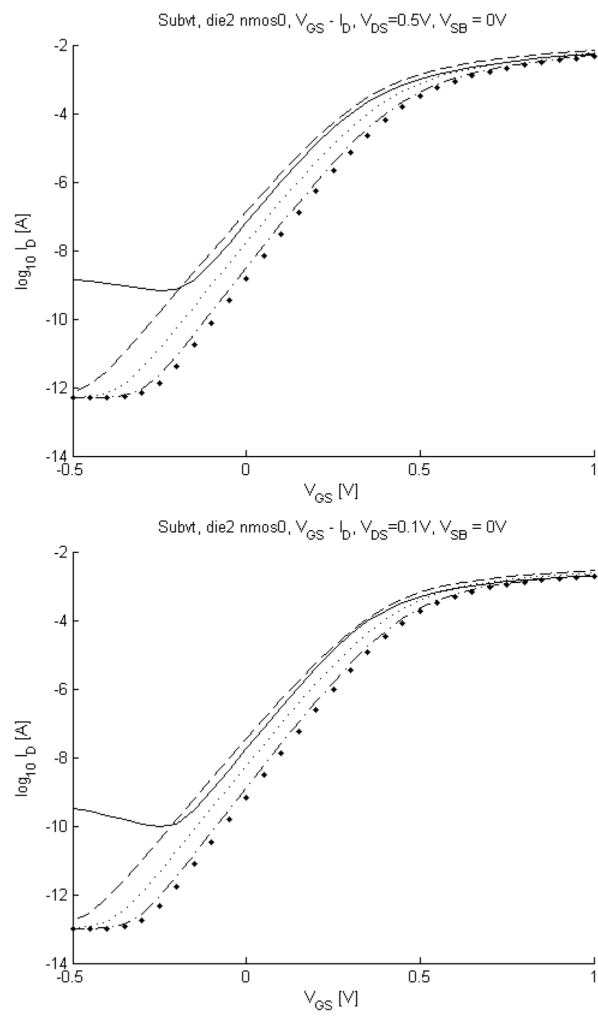

Figure 5.6: die2_nmos0 subthreshold conduction.

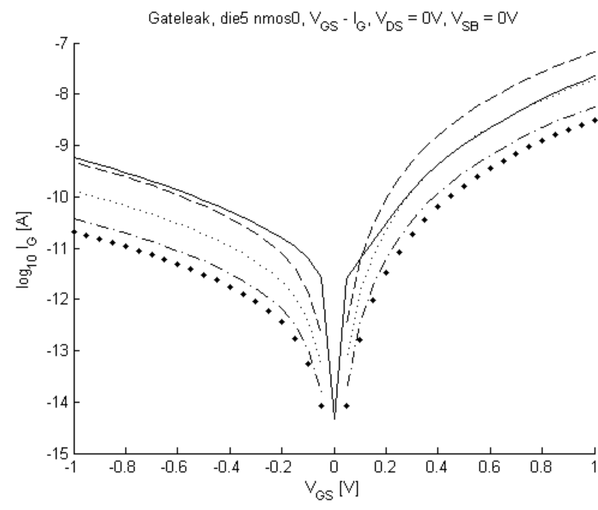

Figure 5.7: die5_nmos0 gate-leakage.

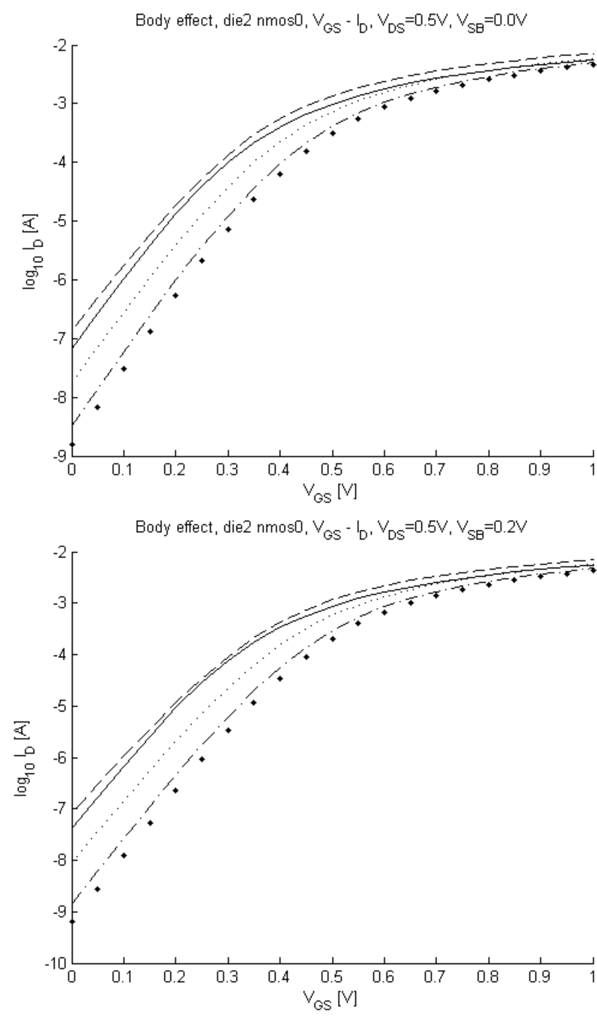

Figure 5.8: die2_nmos0 body-effect.

5.2 nmos1

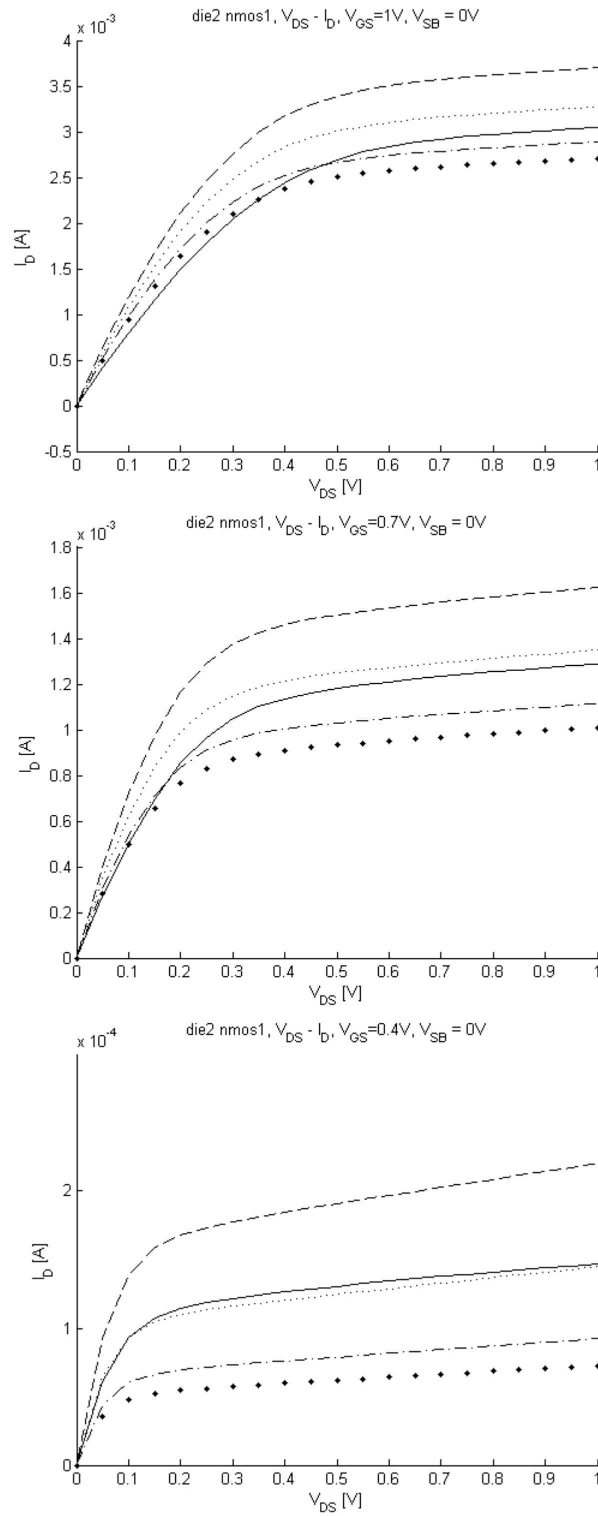

Figure 5.9: die2_nmos1 $V_{DS} - I_D$.

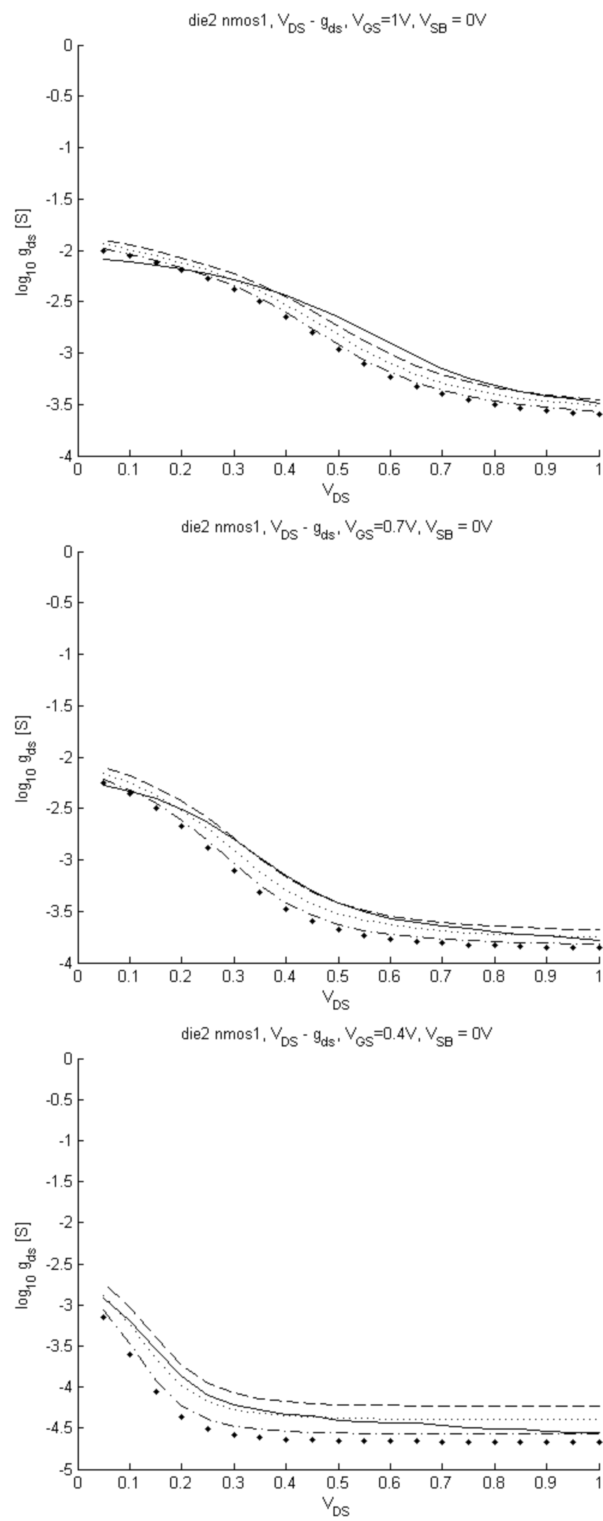

Figure 5.10: die2_nmos1 drain-source conductance g_{ds}.

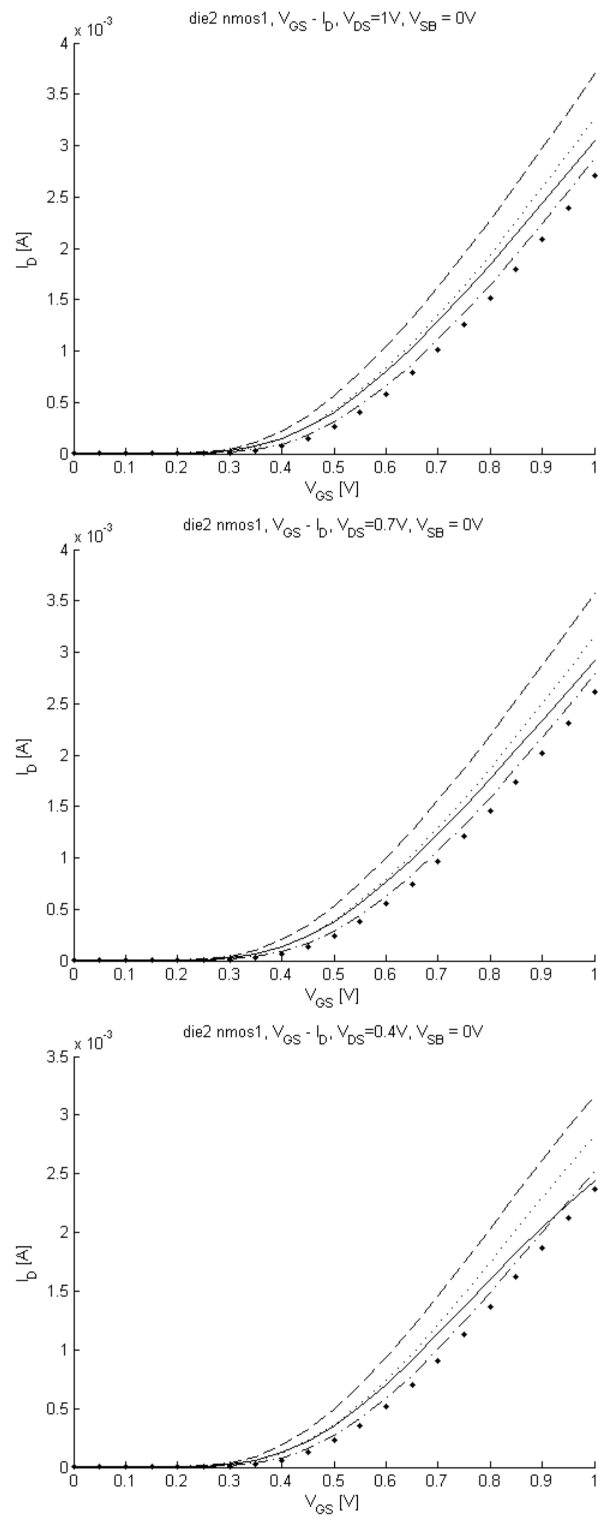

Figure 5.11: die2_nmos1 $V_{GS} - I_D$.

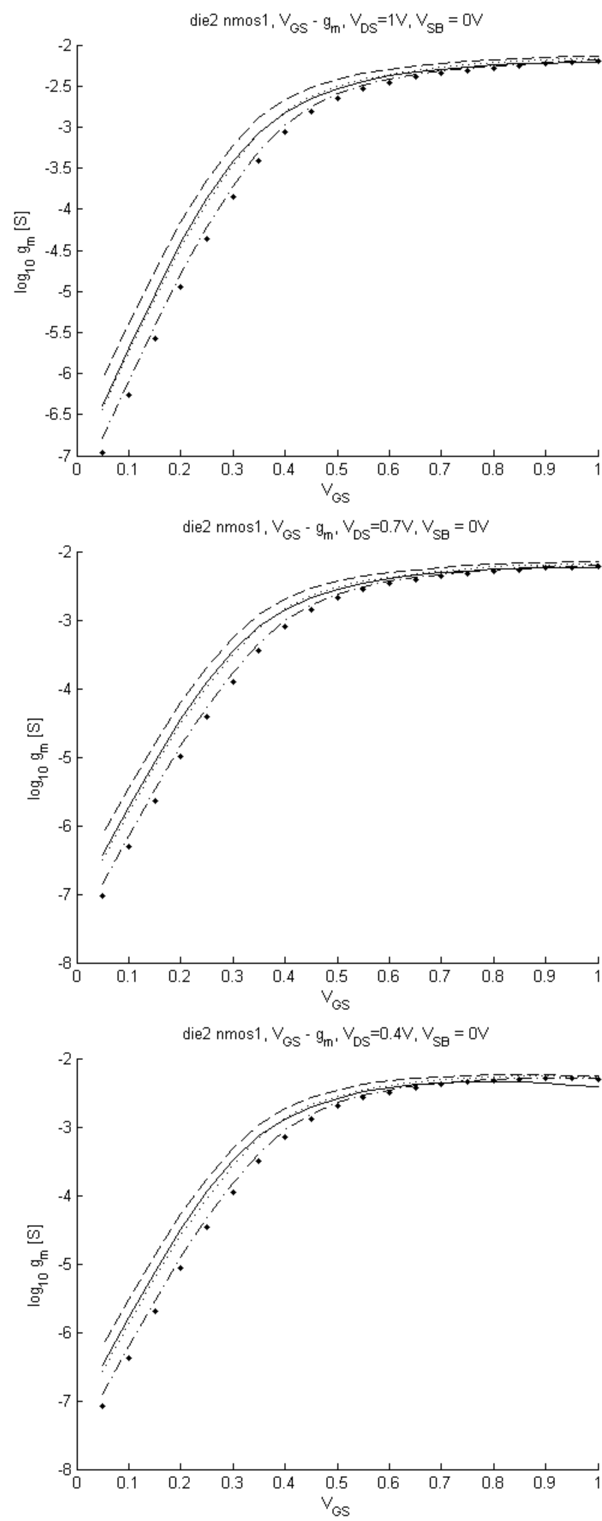

Figure 5.12: die2_nmos1 transconductance g_m.

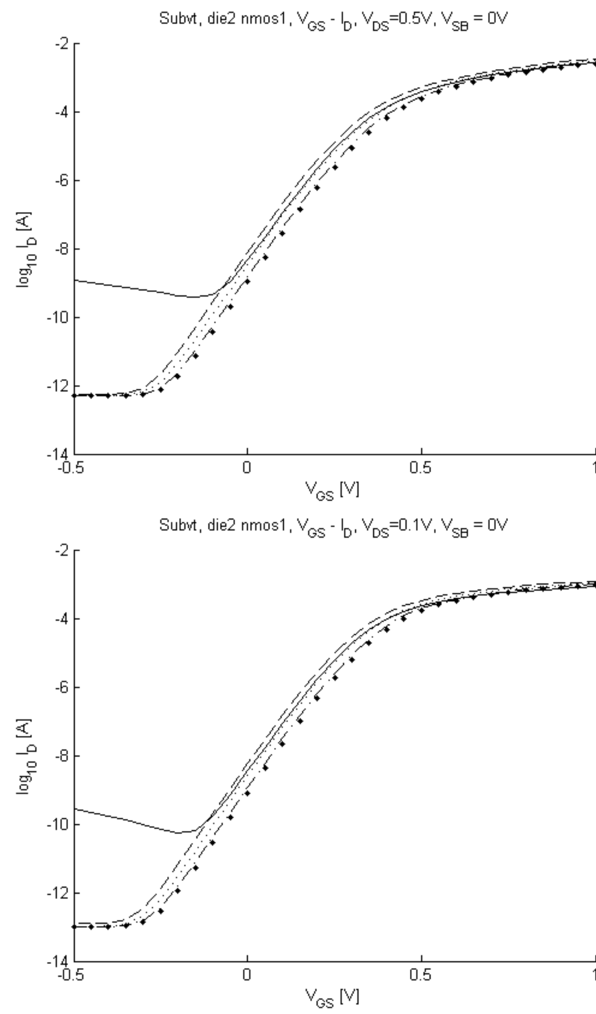

Figure 5.13: die2_nmos1 subthreshold conduction.

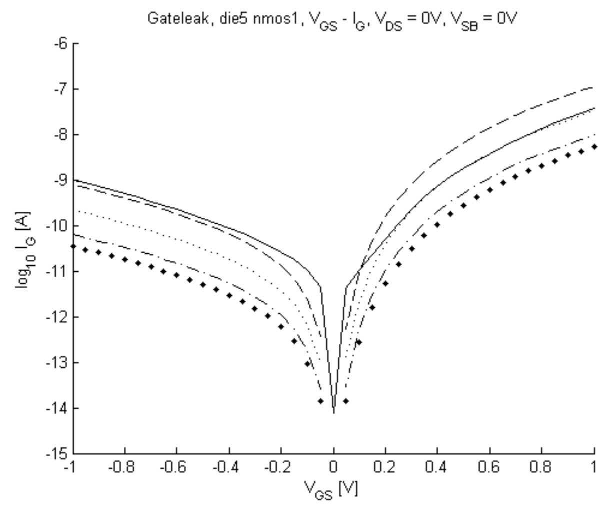

Figure 5.14: die5_nmos1 gate-leakage.

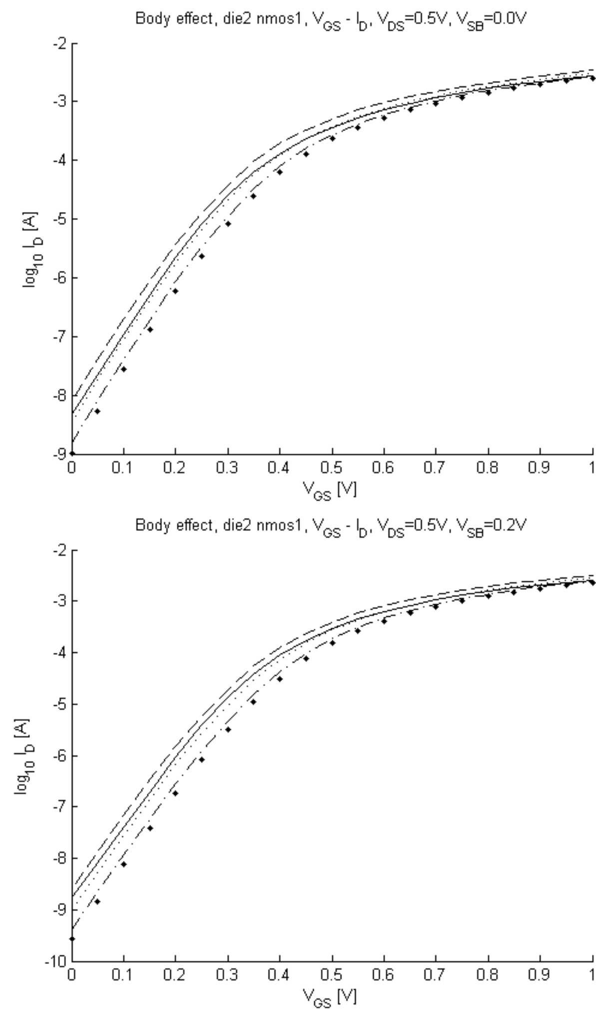

Figure 5.15: die2_nmos1 body-effect.

5.3 nmos2

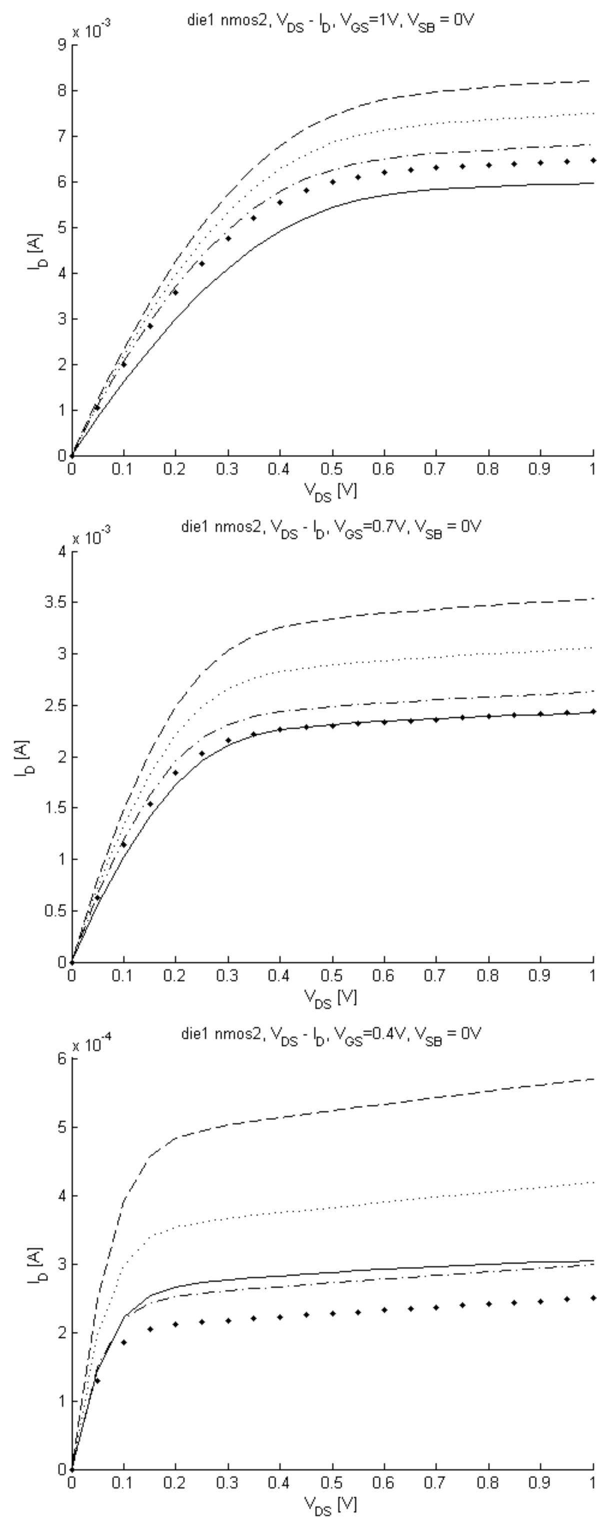

Figure 5.16: die1_nmos2 $V_{DS} - I_D$.

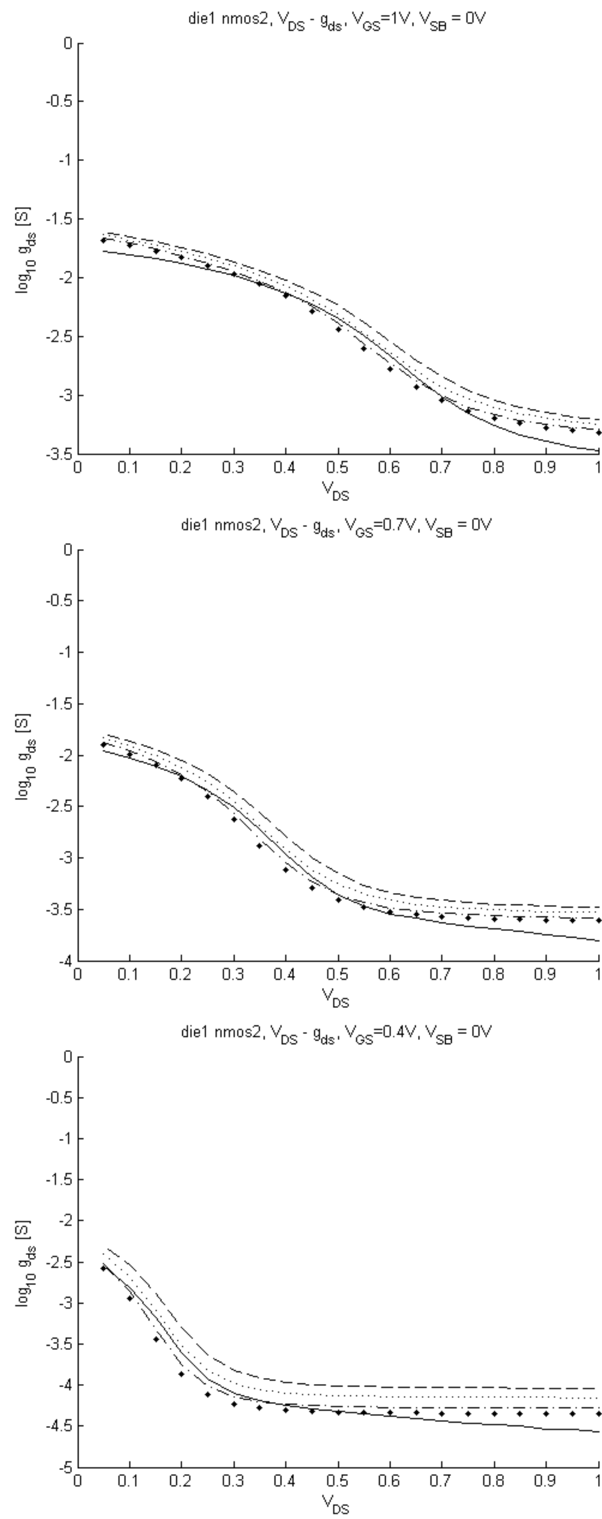

Figure 5.17: die1_nmos2 drain-source conductance g_{ds}.

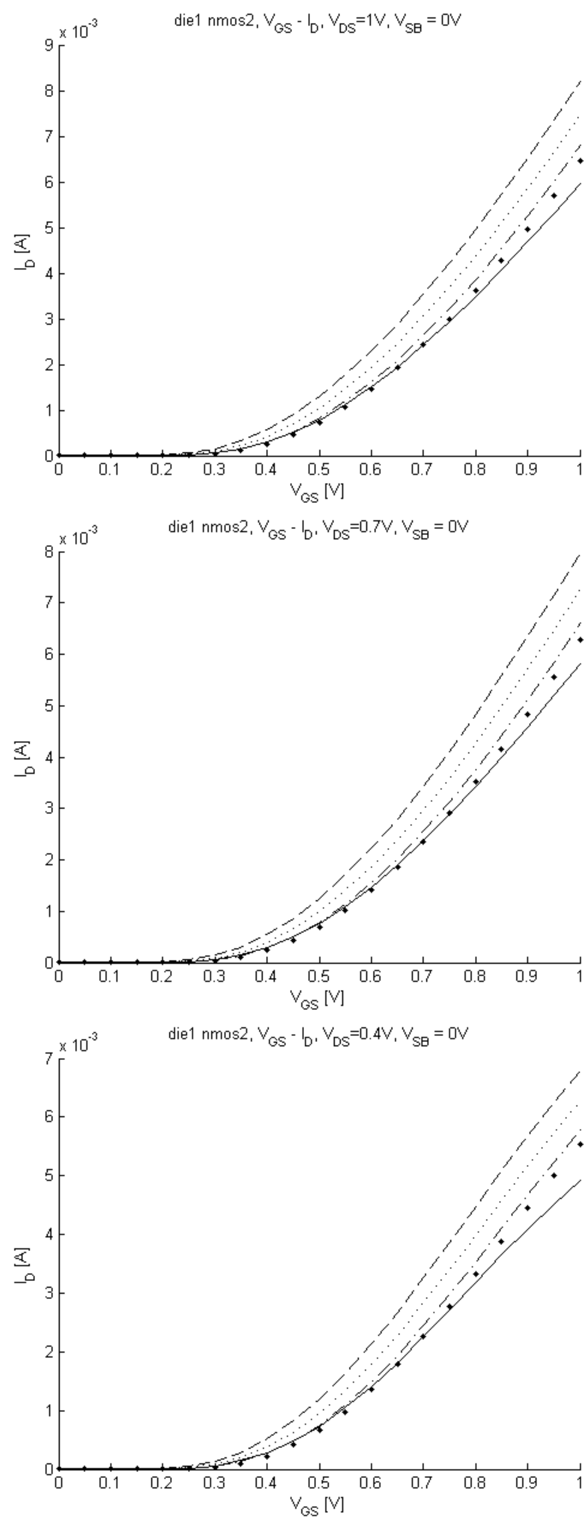

Figure 5.18: die1_nmos2 $V_{GS} - I_D$.

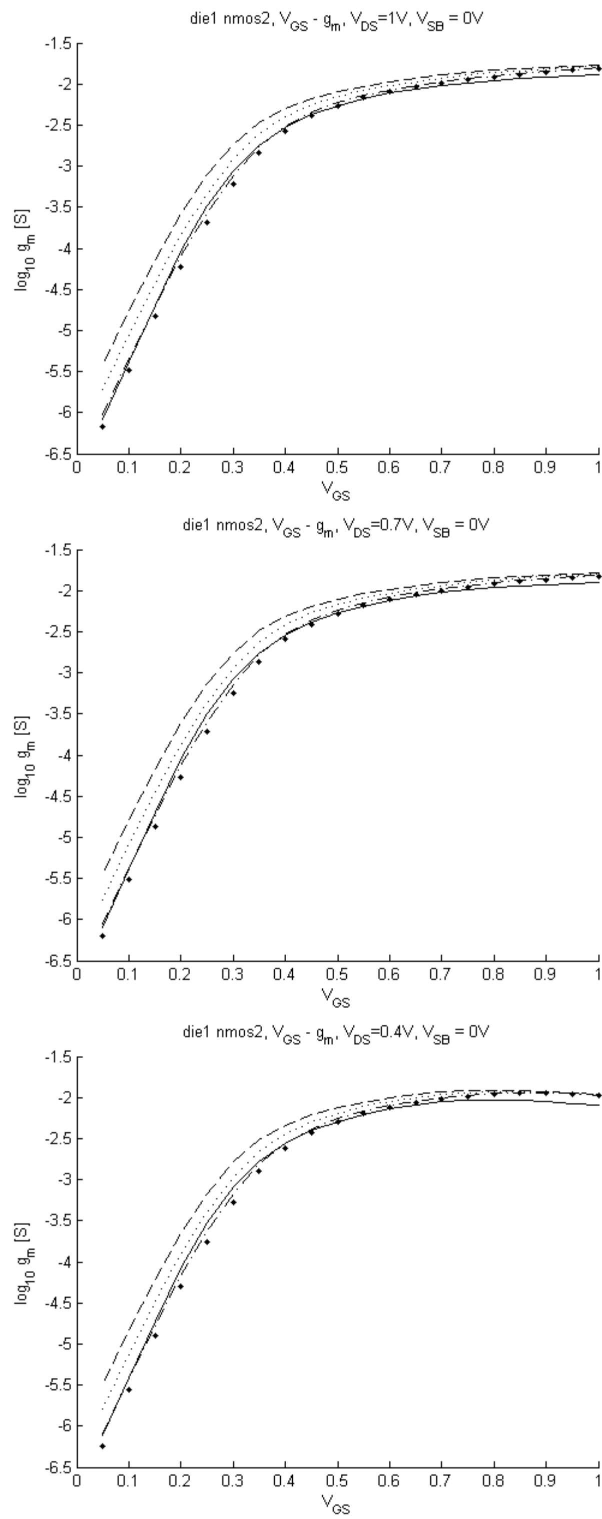

Figure 5.19: die1_nmos2 transconductance g_m.

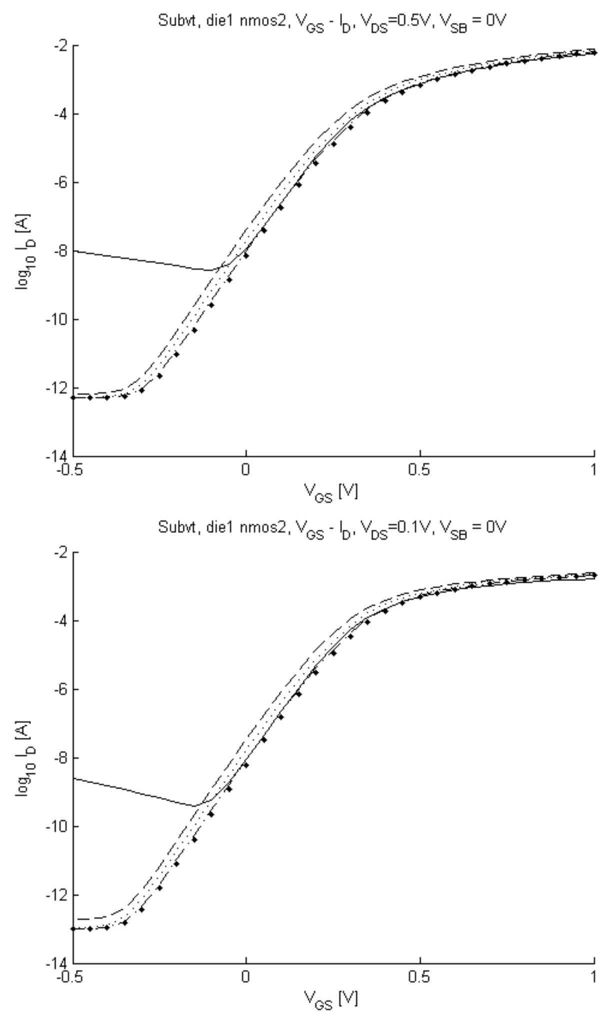

Figure 5.20: die1_nmos2 subthreshold conduction.

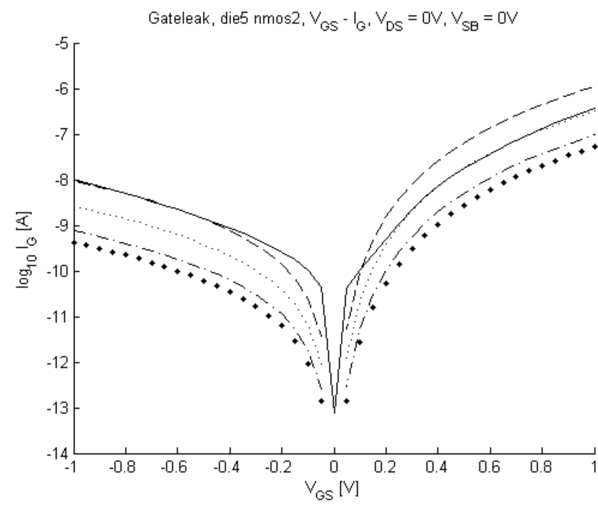

Figure 5.21: die5_nmos2 gate-leakage.

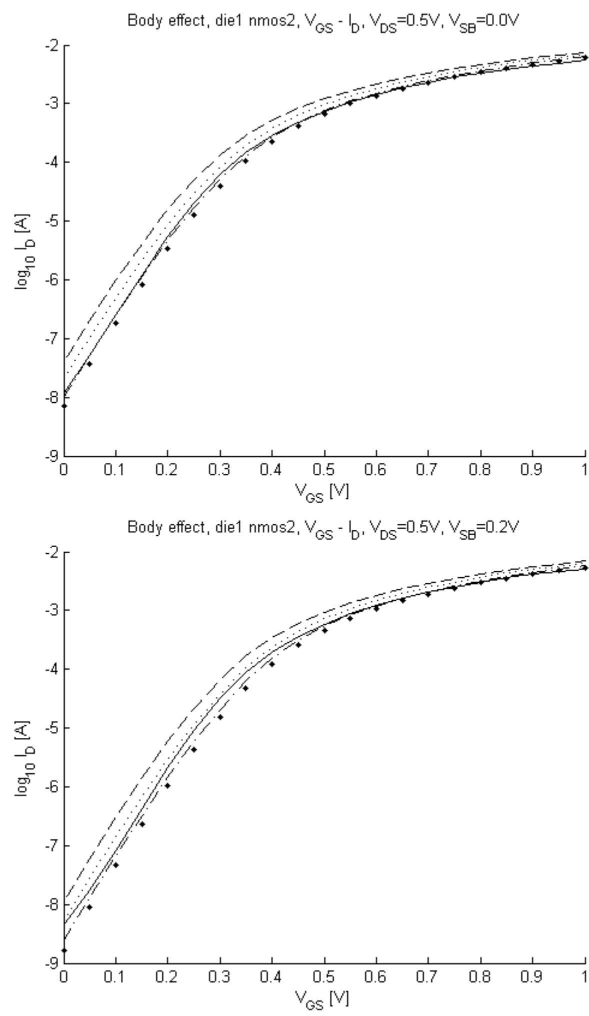

Figure 5.22: die1_nmos2 body-effect.

5.4 nmos3

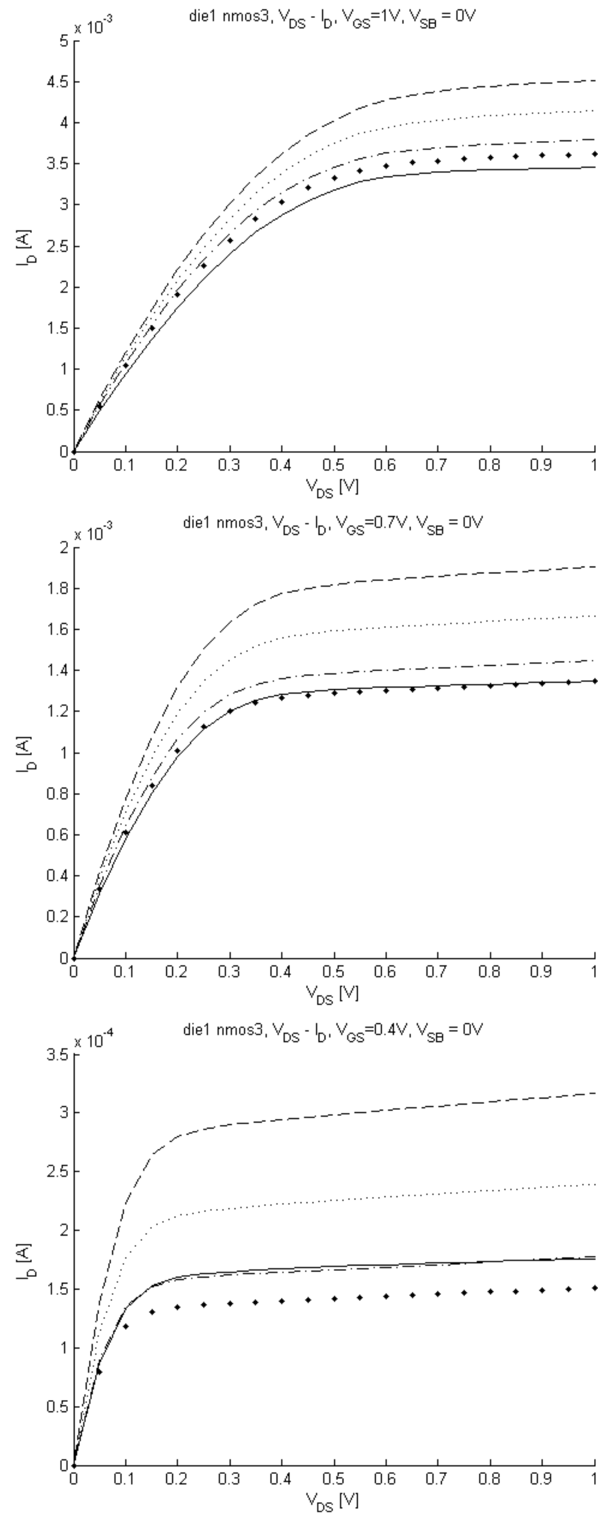

Figure 5.23: die1_nmos3 $V_{DS} - I_D$.

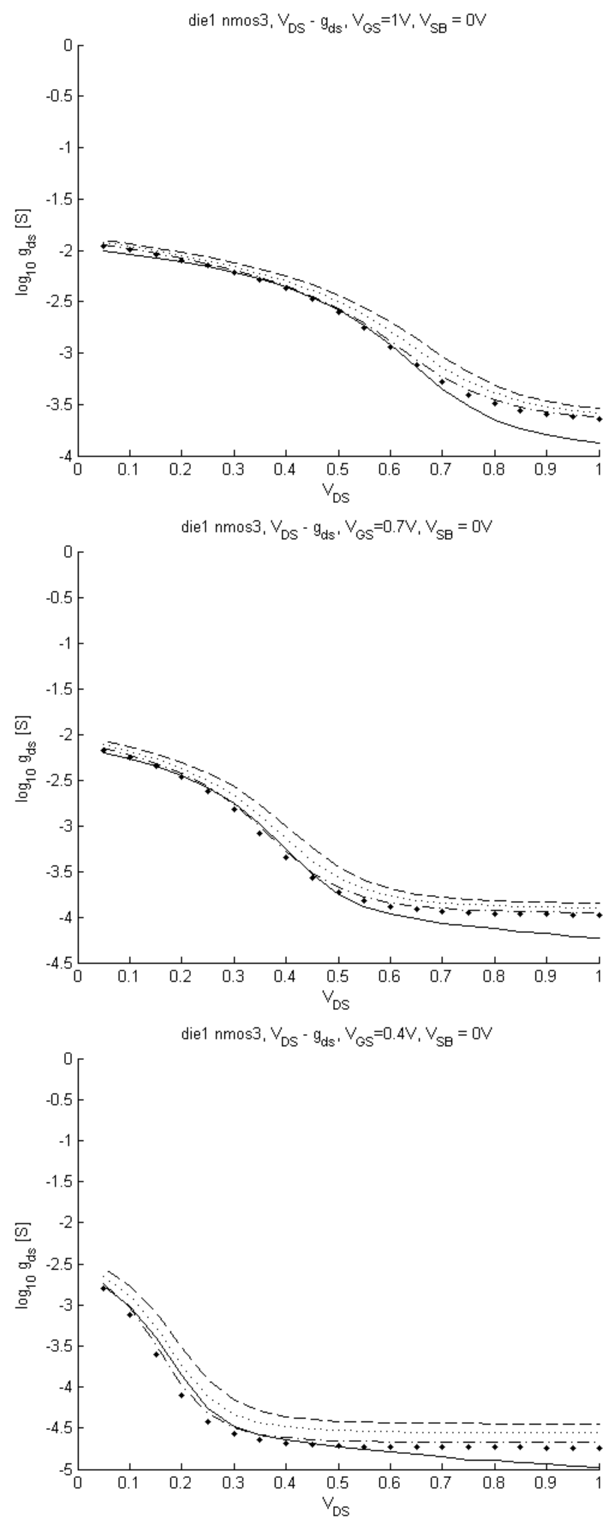

Figure 5.24: die1_nmos3 drain-source conductance g_{ds}.

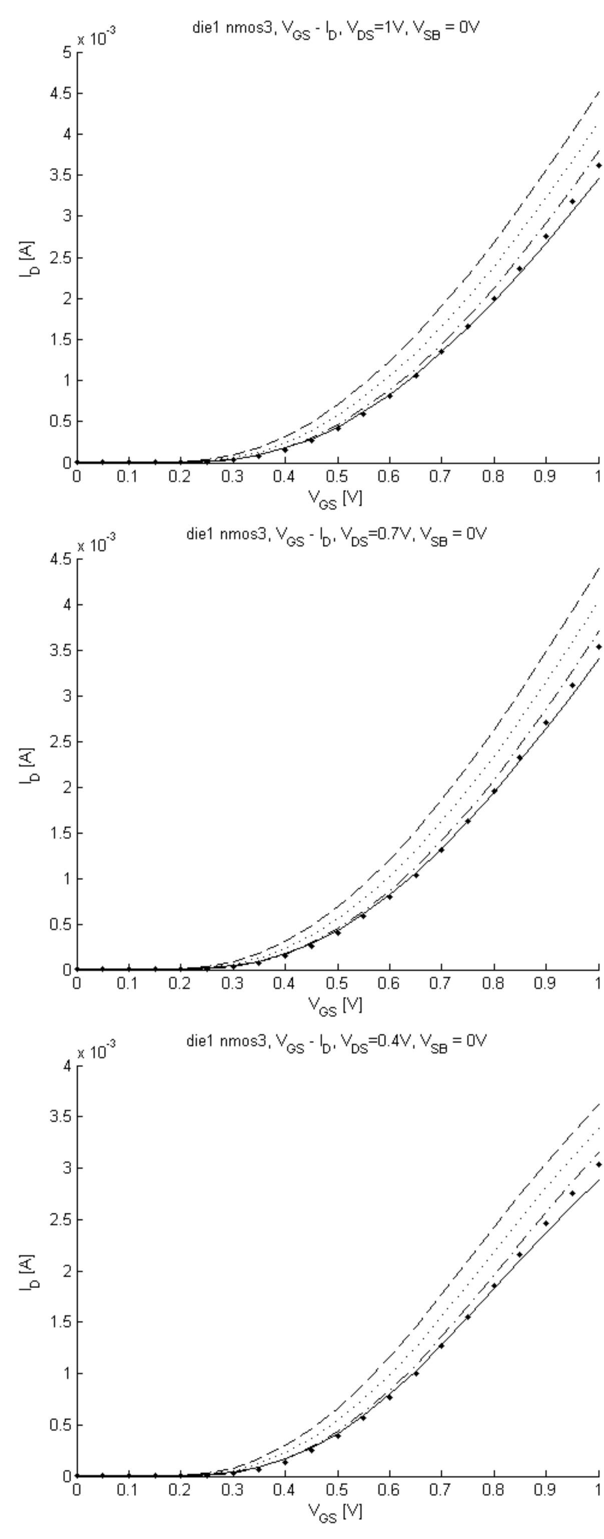

Figure 5.25: die1_nmos3 $V_{GS} - I_D$.

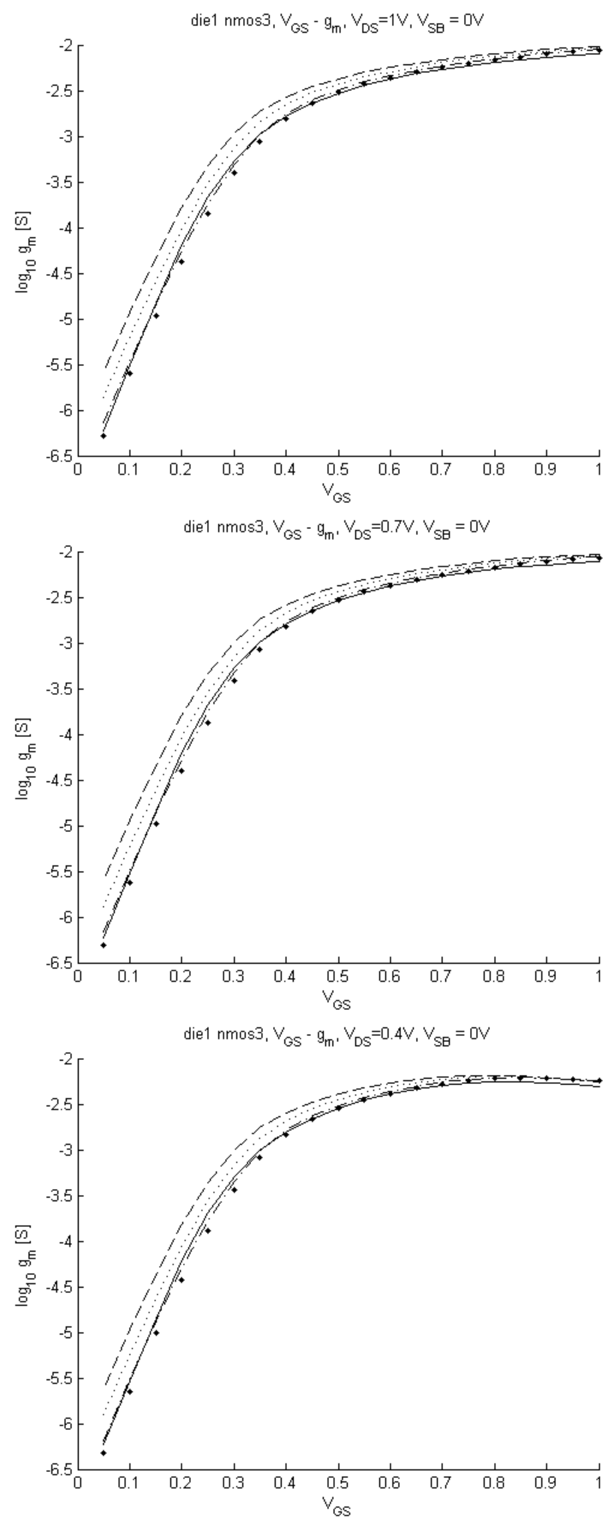

Figure 5.26: die1_nmos3 transconductance g_m.

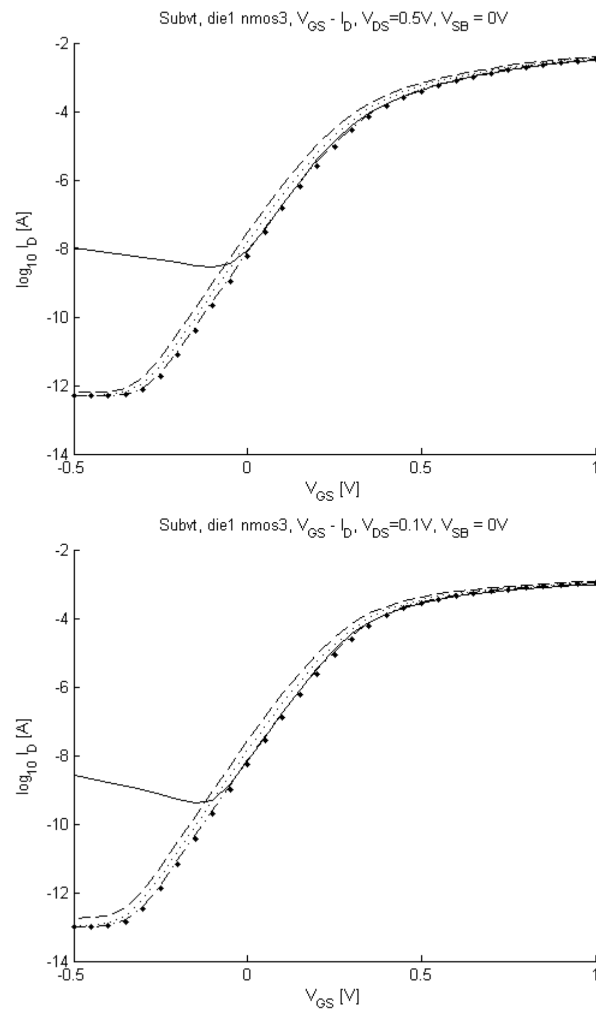

Figure 5.27: die1_nmos3 subthreshold conduction.

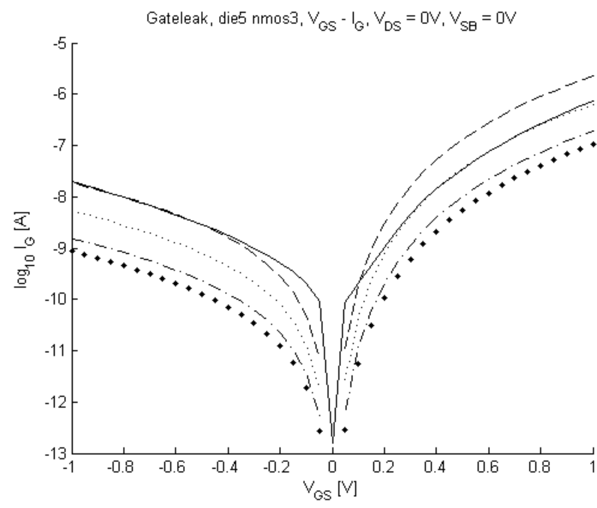

Figure 5.28: die5_nmos3 gate-leakage.

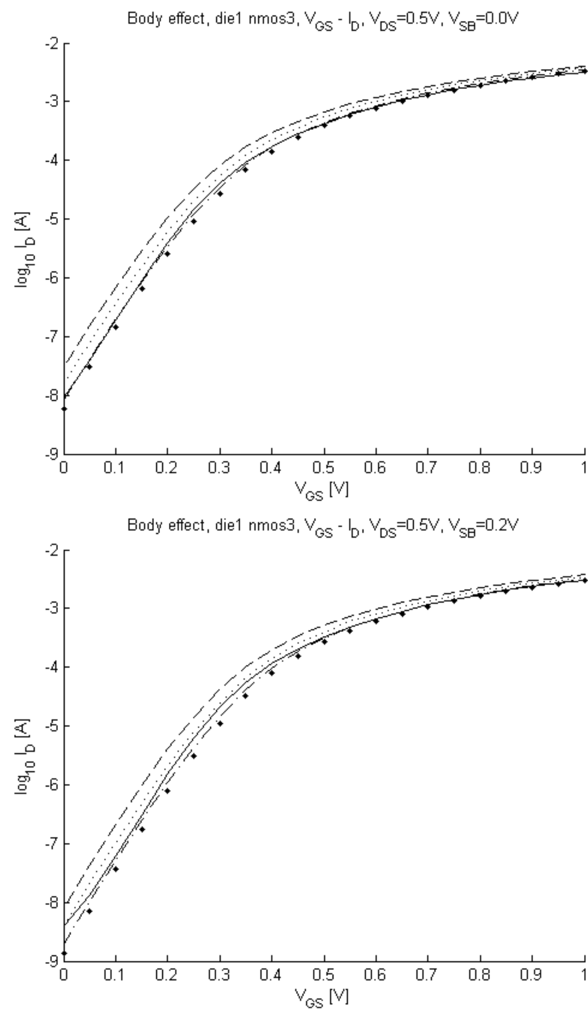

Figure 5.29: die1_nmos3 body-effect.

5.5 pmos0

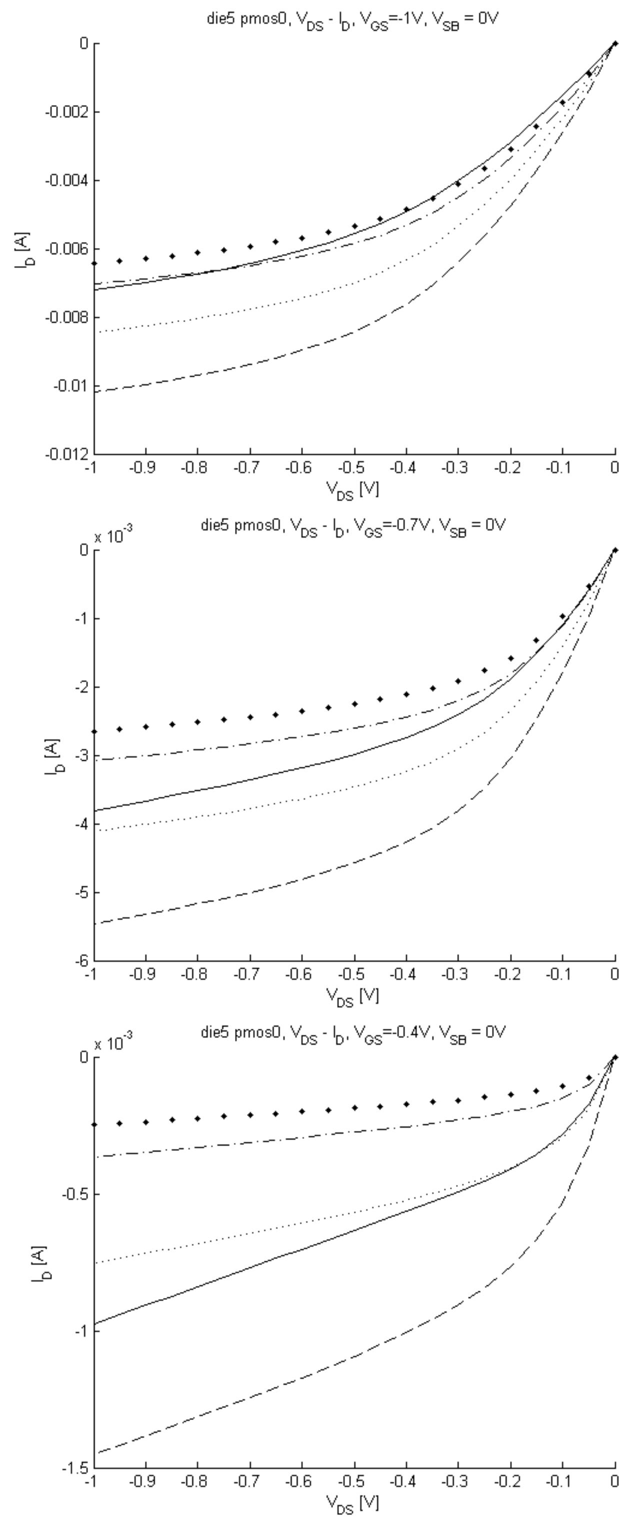

Figure 5.30: die5_pmos0 $V_{DS} - I_D$.

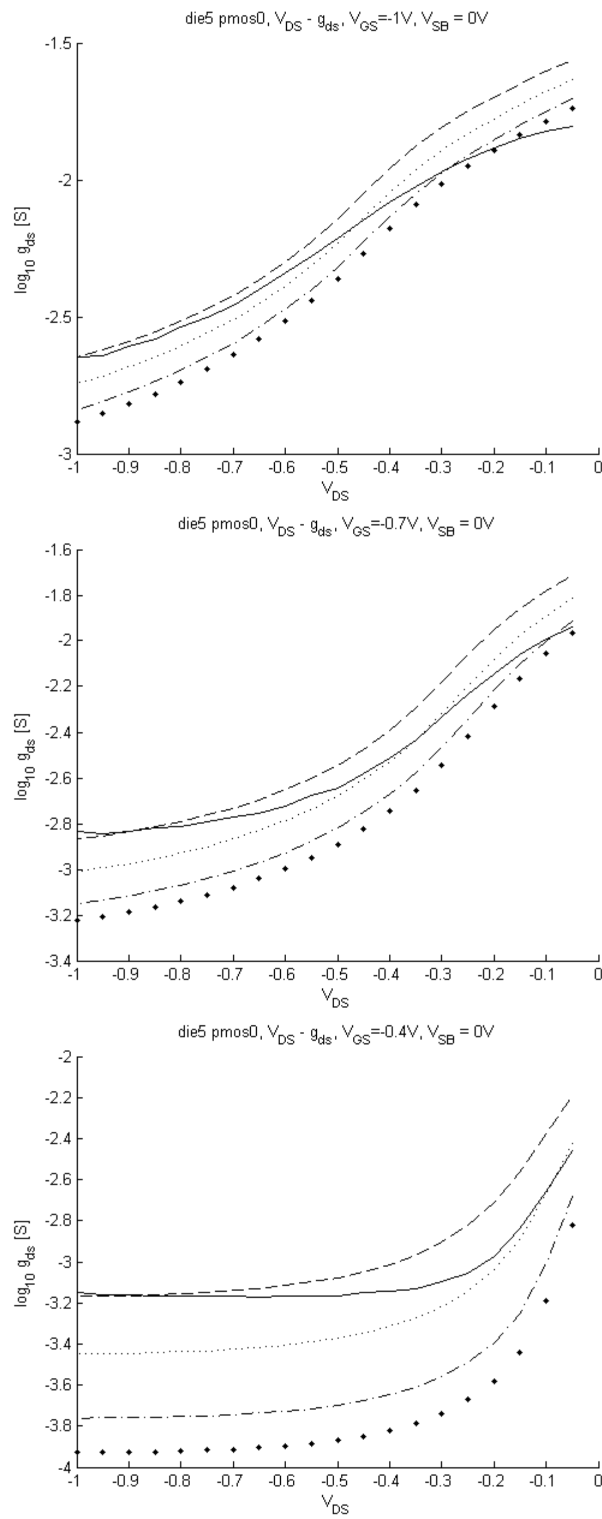

Figure 5.31: die5_pmos0 drain-source conductance g_{ds}.

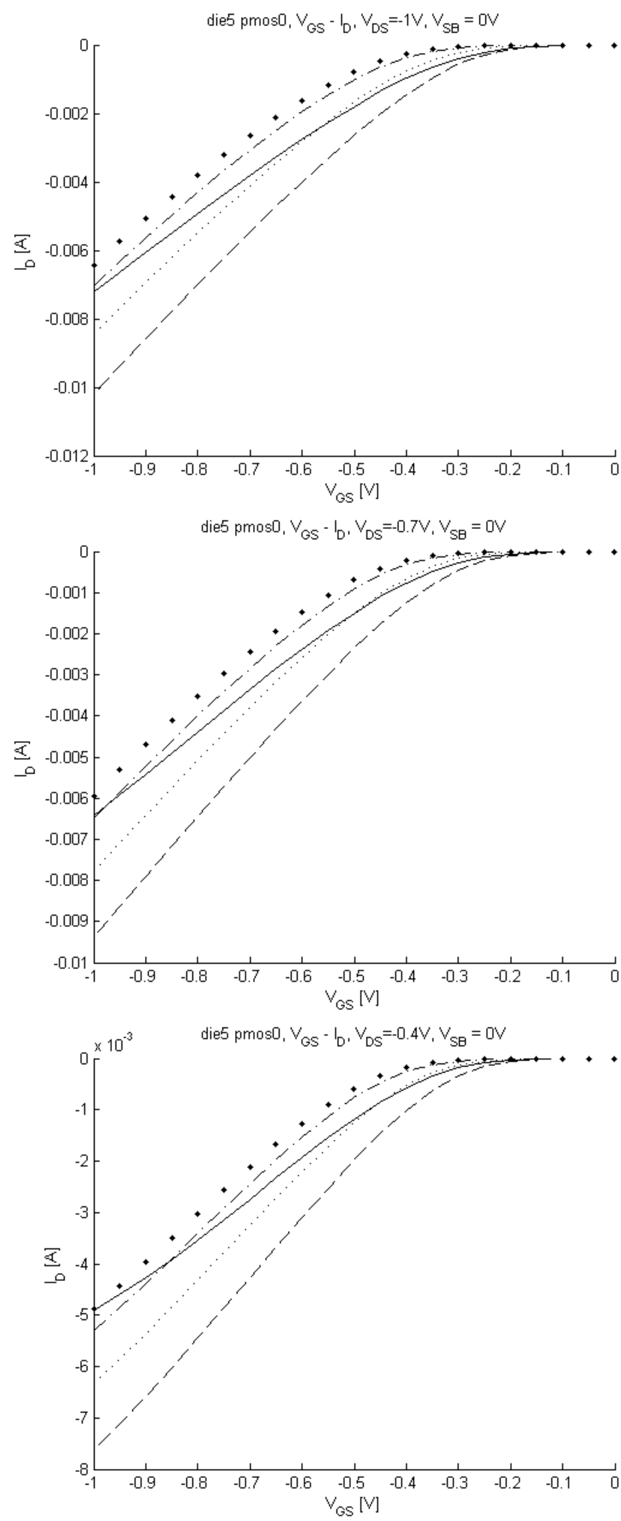

Figure 5.32: die5_pmos0 $V_{GS} - I_D$.

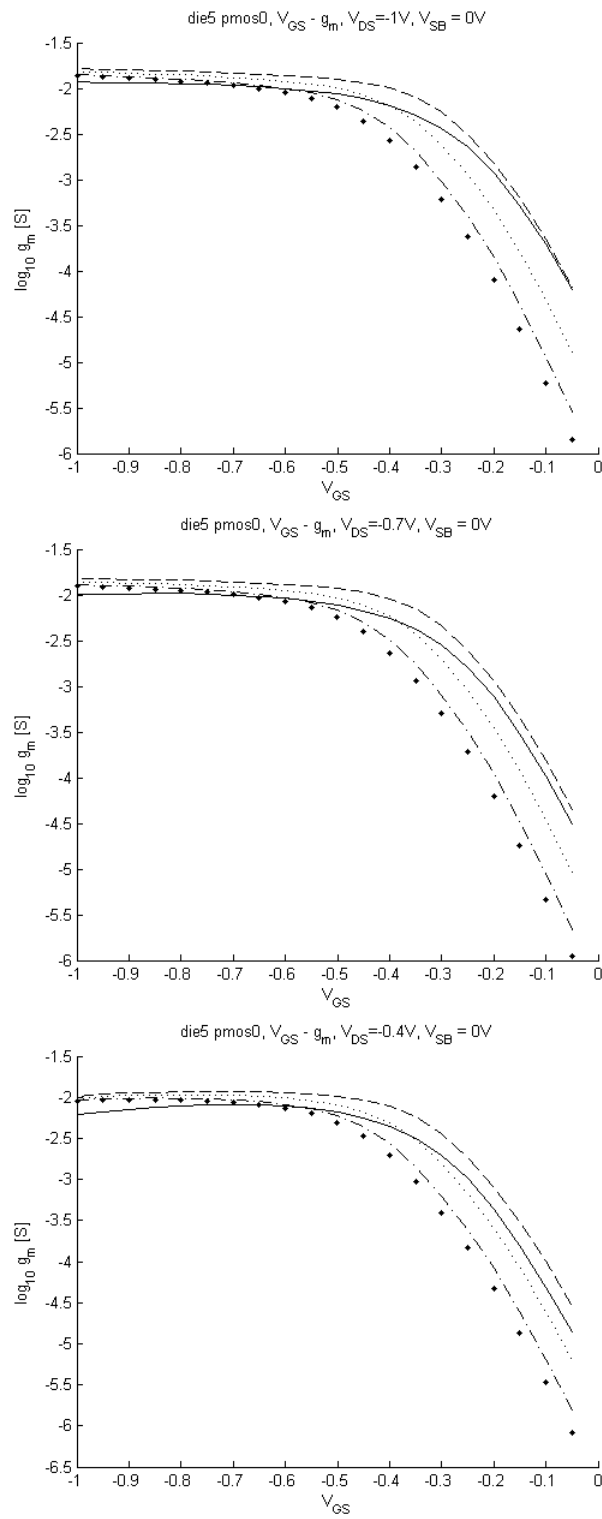

Figure 5.33: die5_pmos0 transconductance g_m.

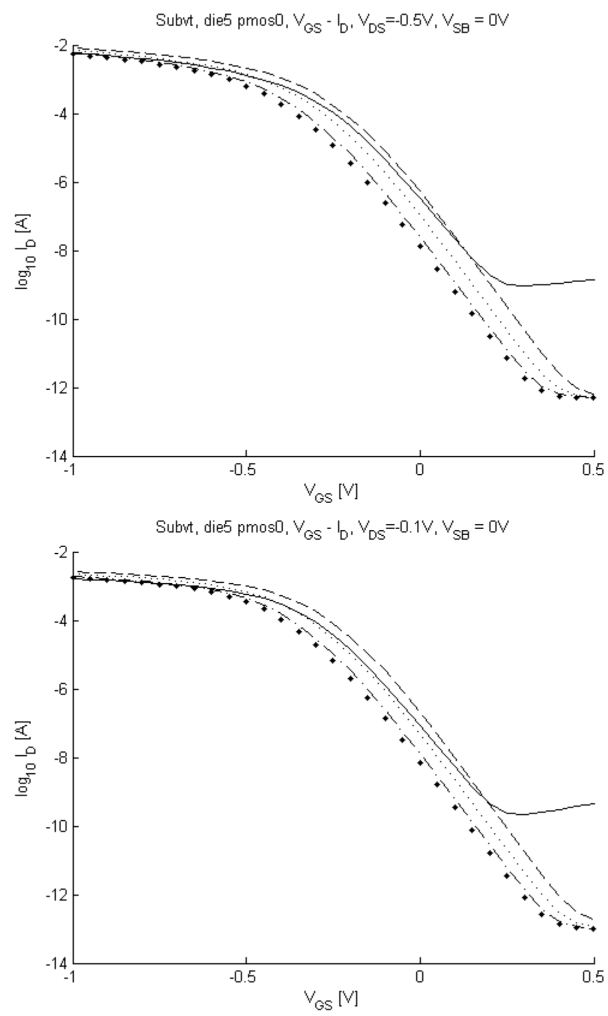

Figure 5.34: die5_pmos0 subthreshold conduction.

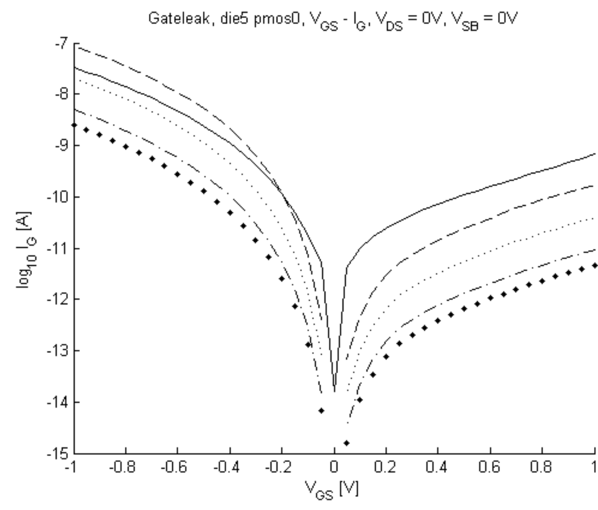

Figure 5.35: die5_pmos0 gate-leakage.

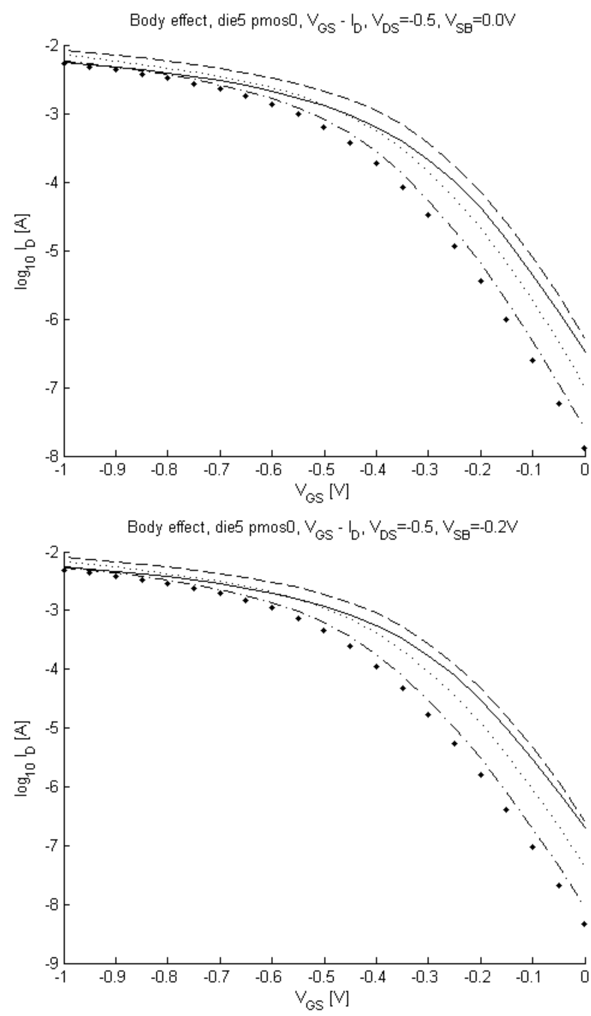

Figure 5.36: die5_pmos0 body-effect.

5.6 pmos1

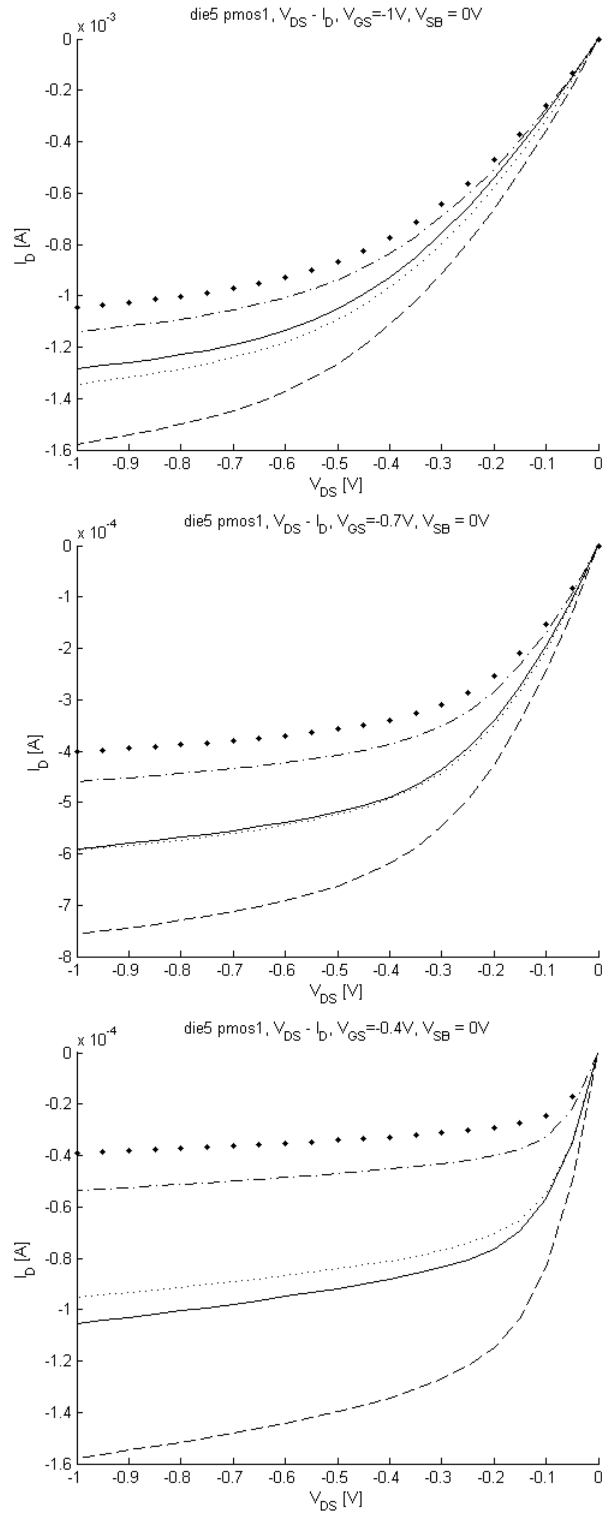

Figure 5.37: die5_pmos1 $V_{DS} - I_D$.

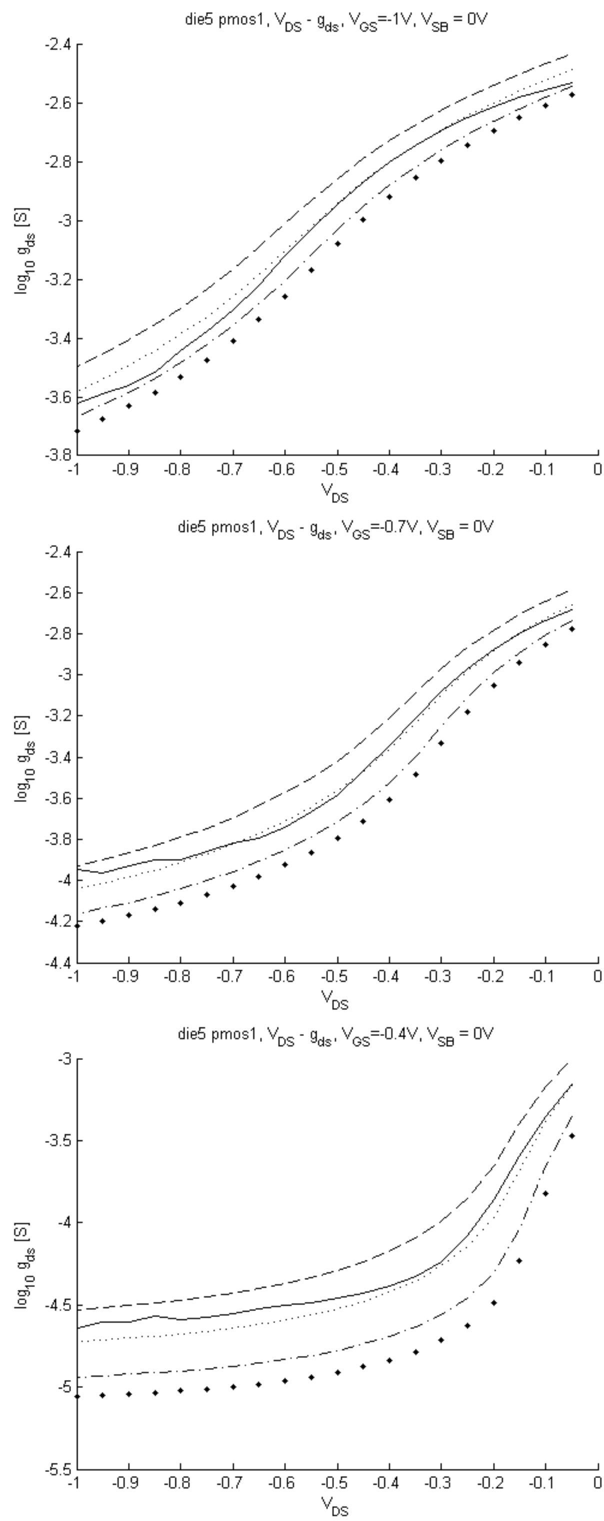

Figure 5.38: die5_pmos1 drain-source conductance g_{ds}.

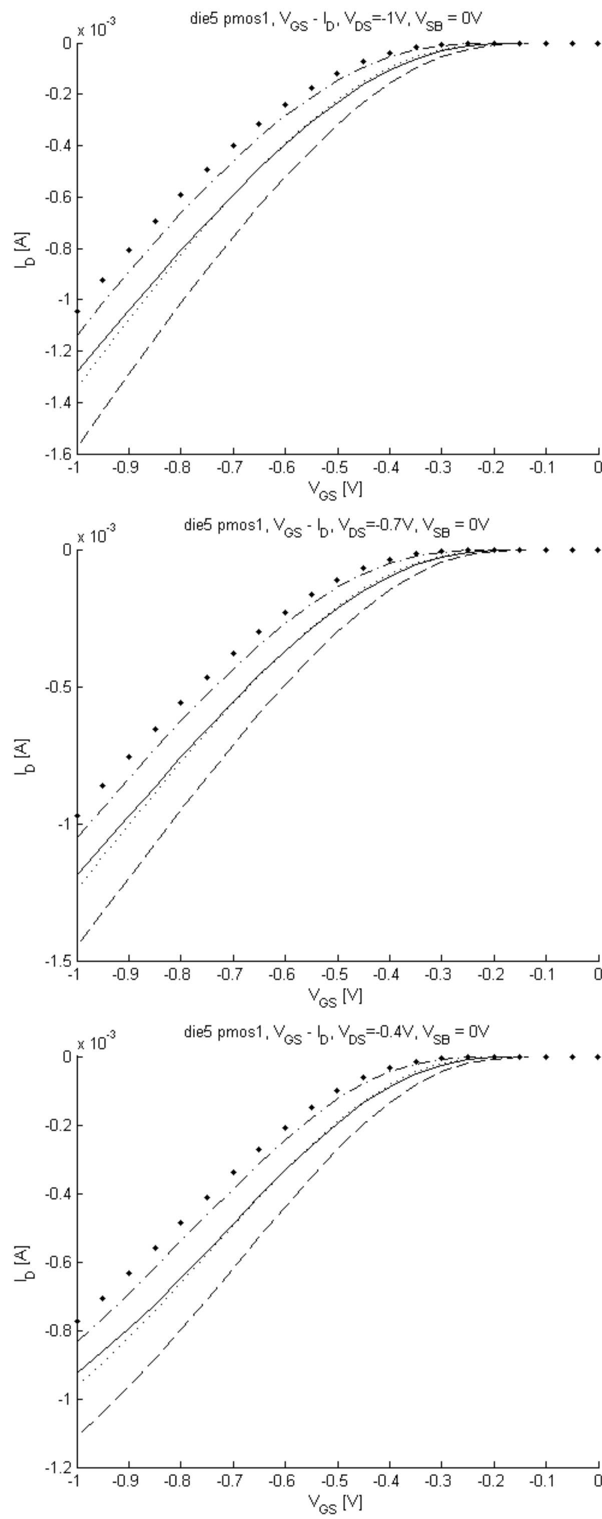

Figure 5.39: die5_pmos1 $V_{GS} - I_D$.

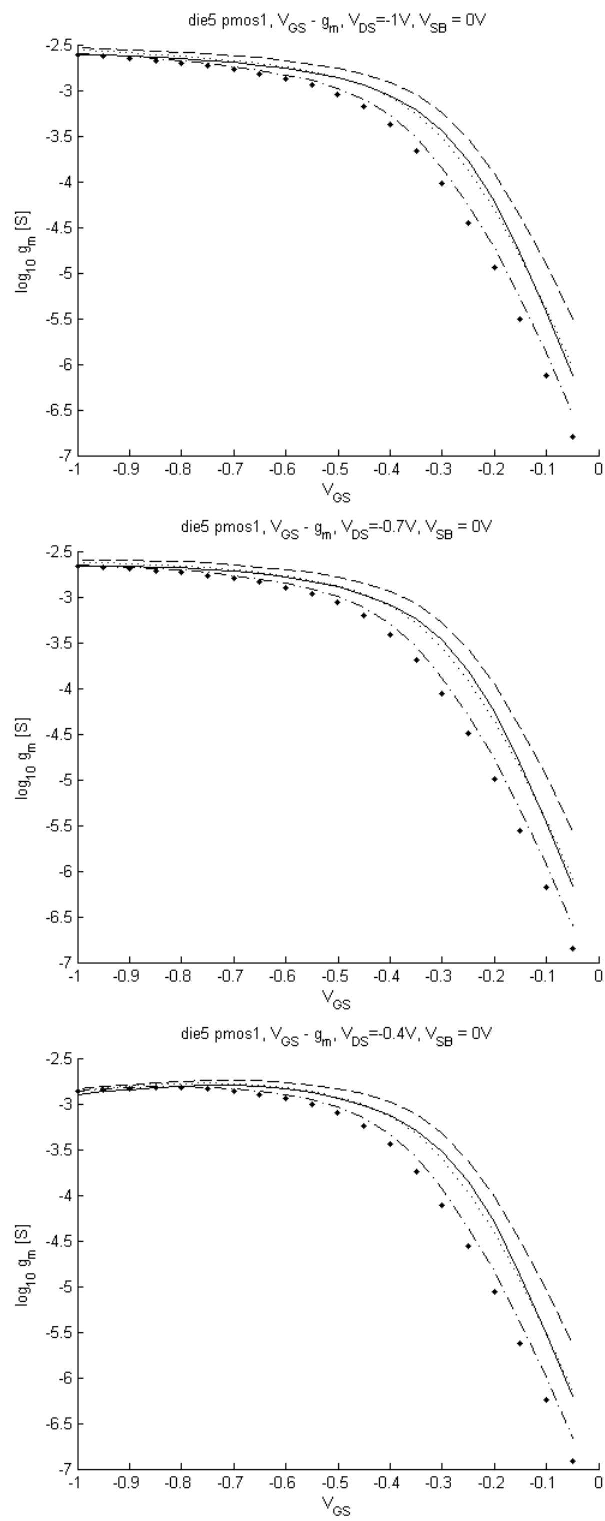

Figure 5.40: die5_pmos1 transconductance g_m.

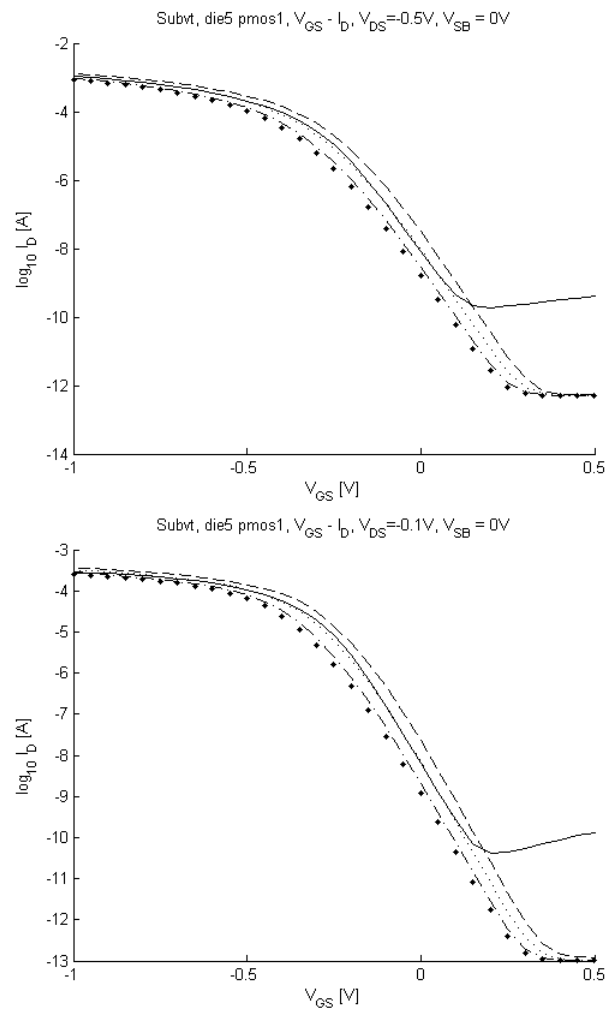

Figure 5.41: die5_pmos1 subthreshold conduction.

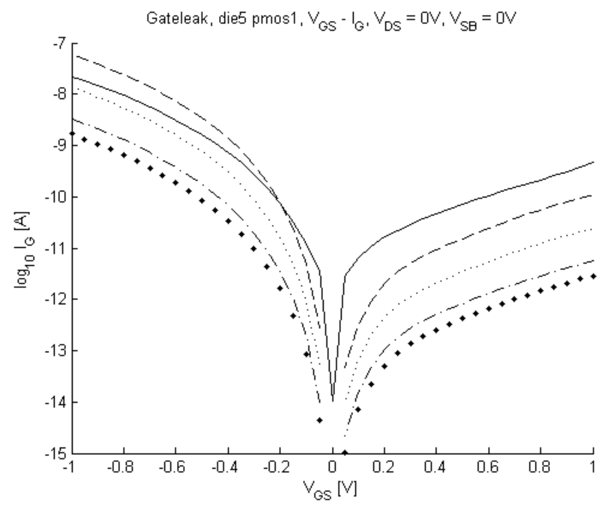

Figure 5.42: die5_pmos1 gate-leakage.

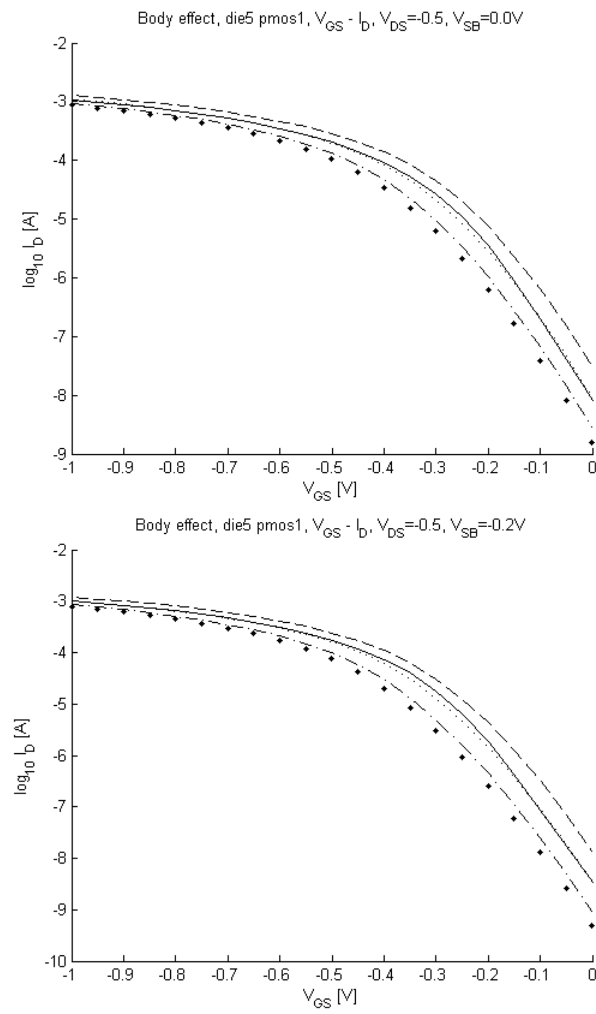

Figure 5.43: die5_pmos1 body-effect.

5.7 pmos2

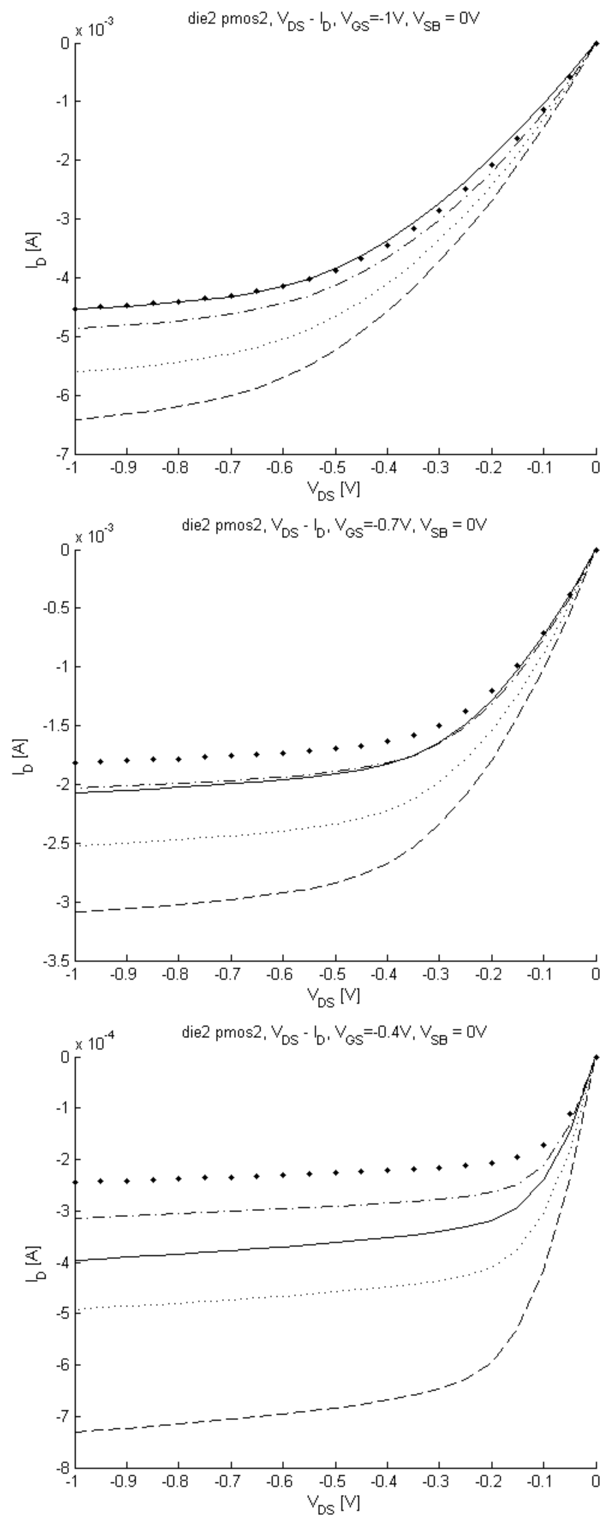

Figure 5.44: die2_pmos2 $V_{DS} - I_D$.

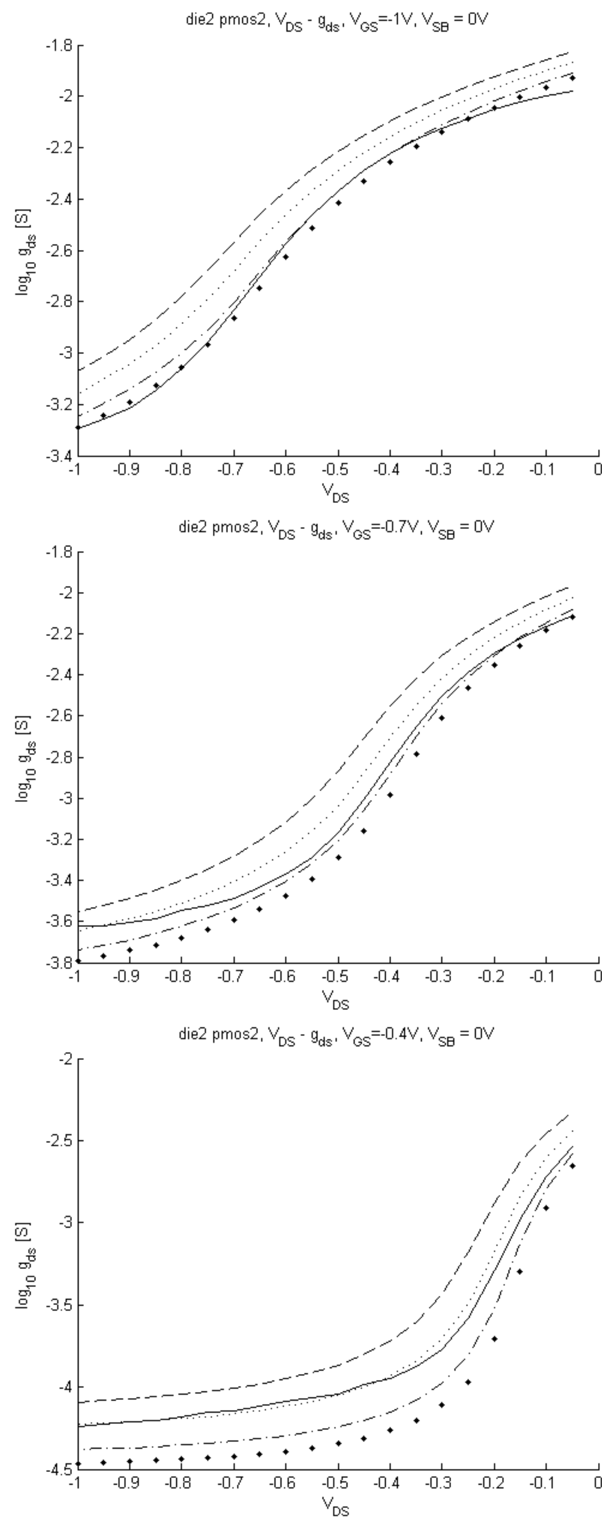

Figure 5.45: die2_pmos2 drain-source conductance g_{ds}.

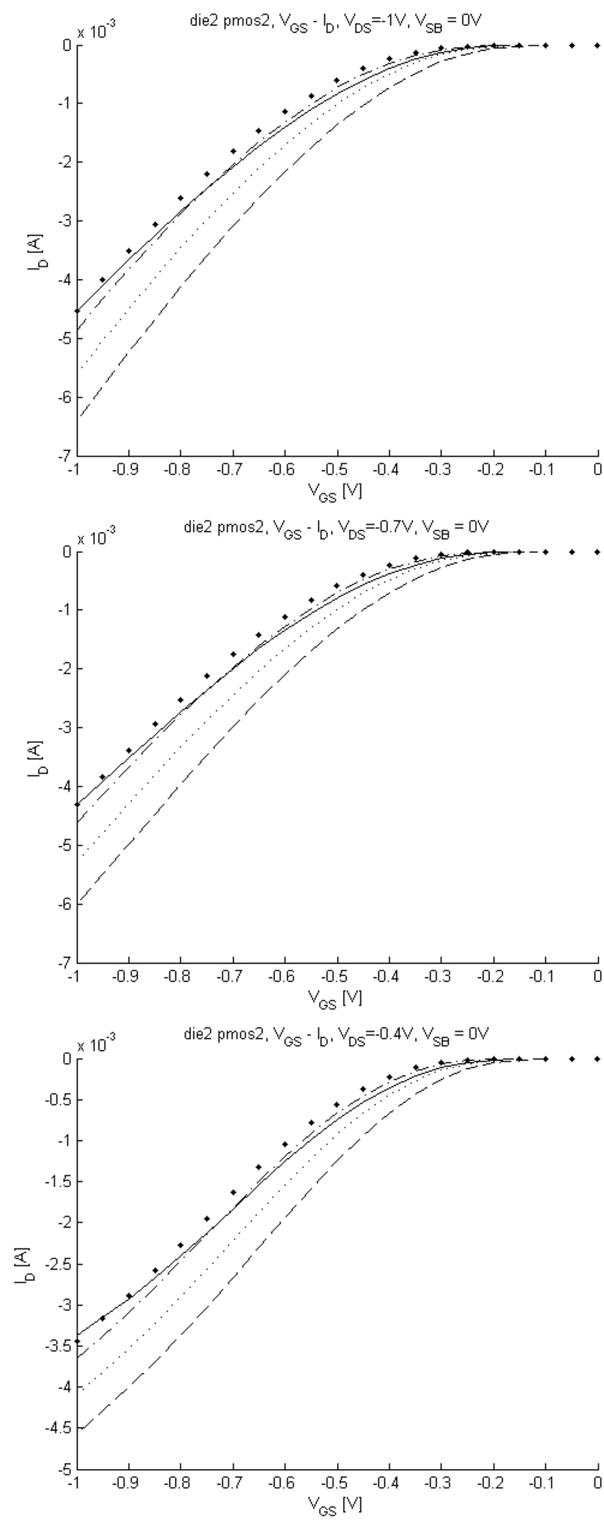

Figure 5.46: die2_pmos2 $V_{GS} - I_D$.

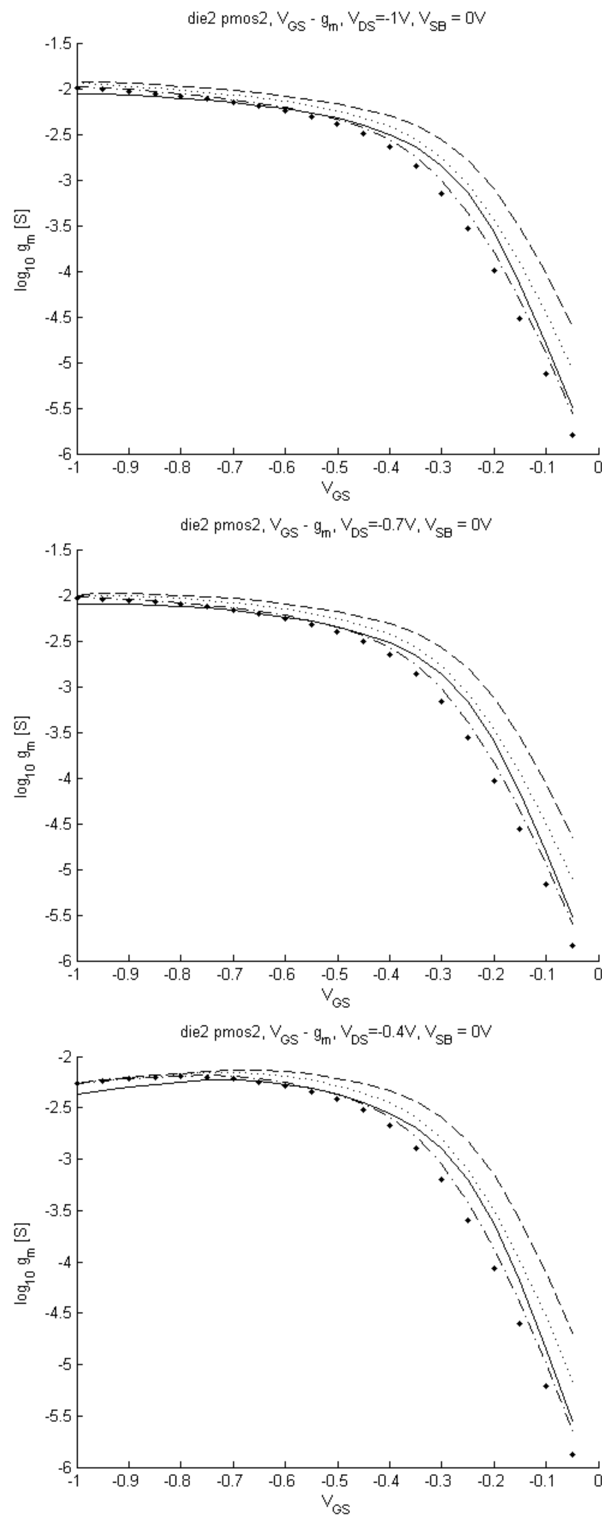

Figure 5.47: die2_pmos2 transconductance g_m.

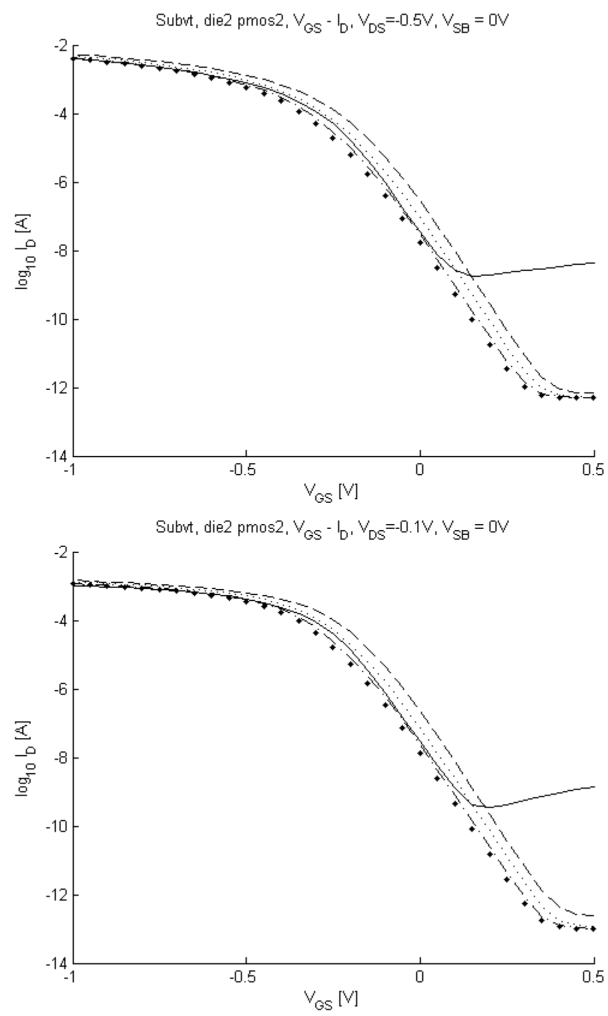

Figure 5.48: die2_pmos2 subthreshold conduction.

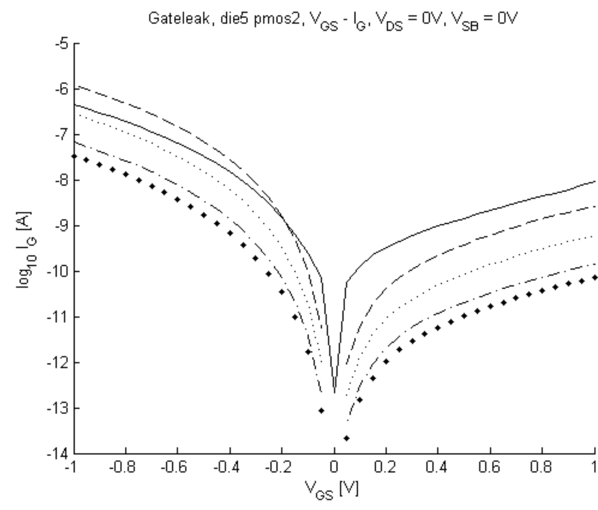

Figure 5.49: die5_pmos2 gate-leakage.

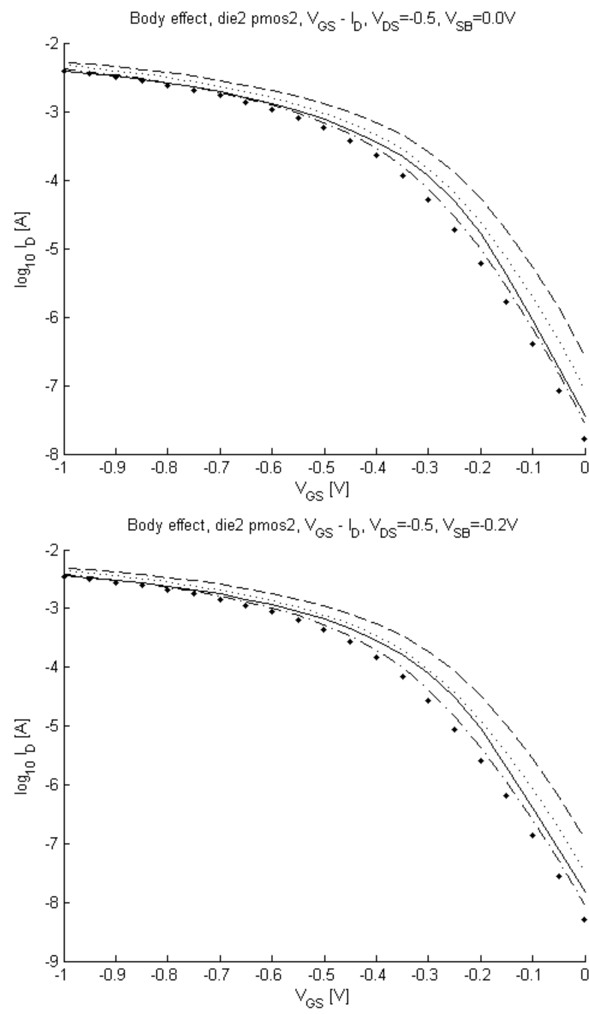

Figure 5.50: die2_pmos2 body-effect.

5.8 pmos3

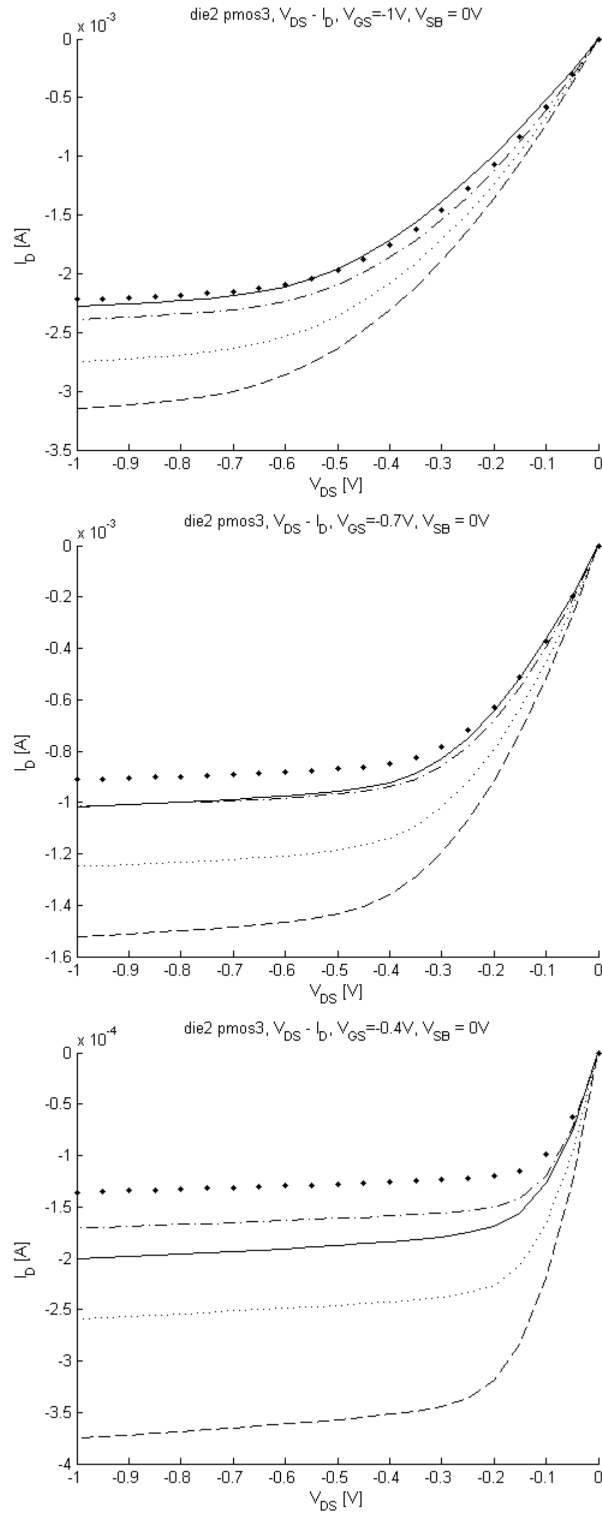

Figure 5.51: die2_pmos3 $V_{DS} - I_D$.

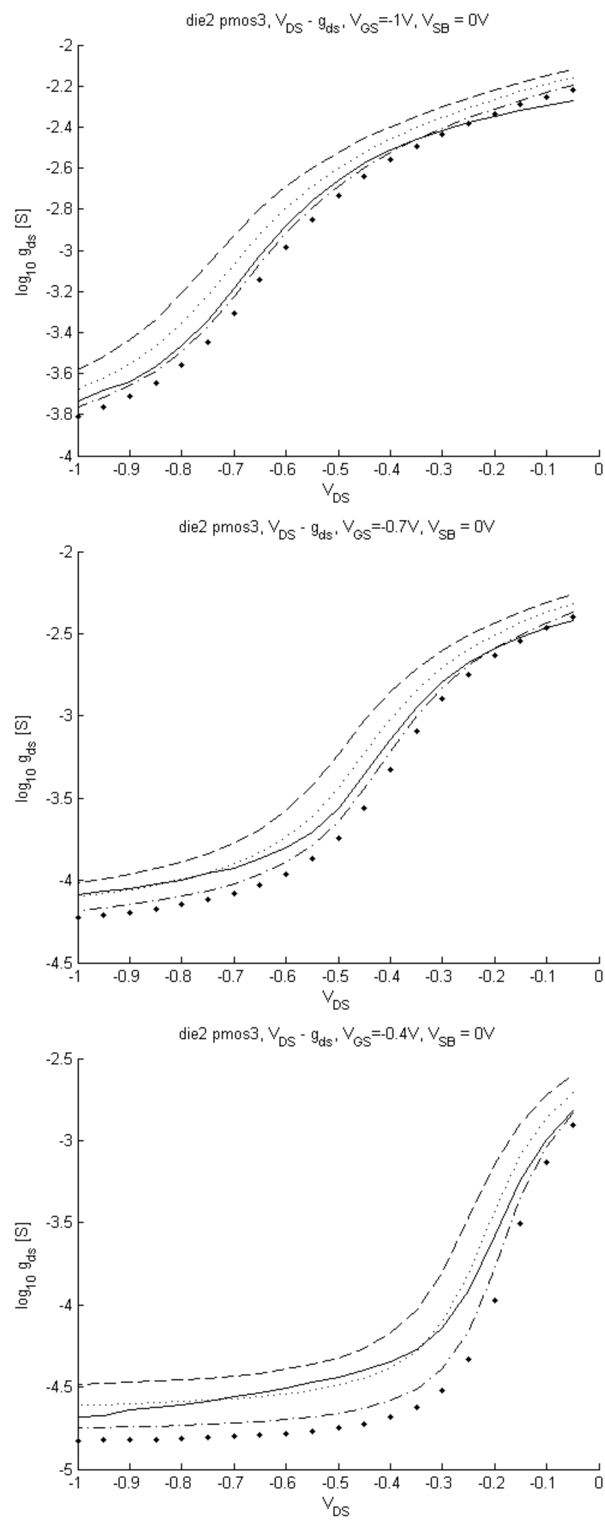

Figure 5.52: die2_pmos3 drain-source conductance g_{ds}.

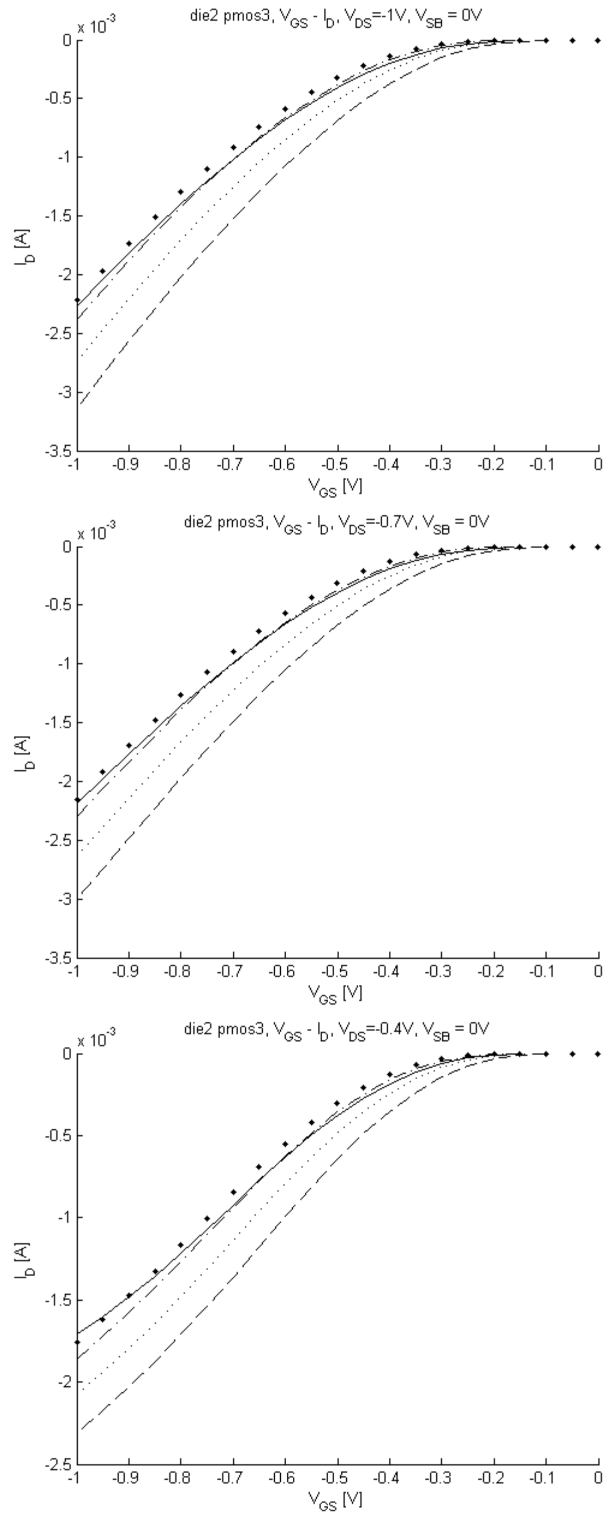

Figure 5.53: die2_pmos3 $V_{GS} - I_D$.

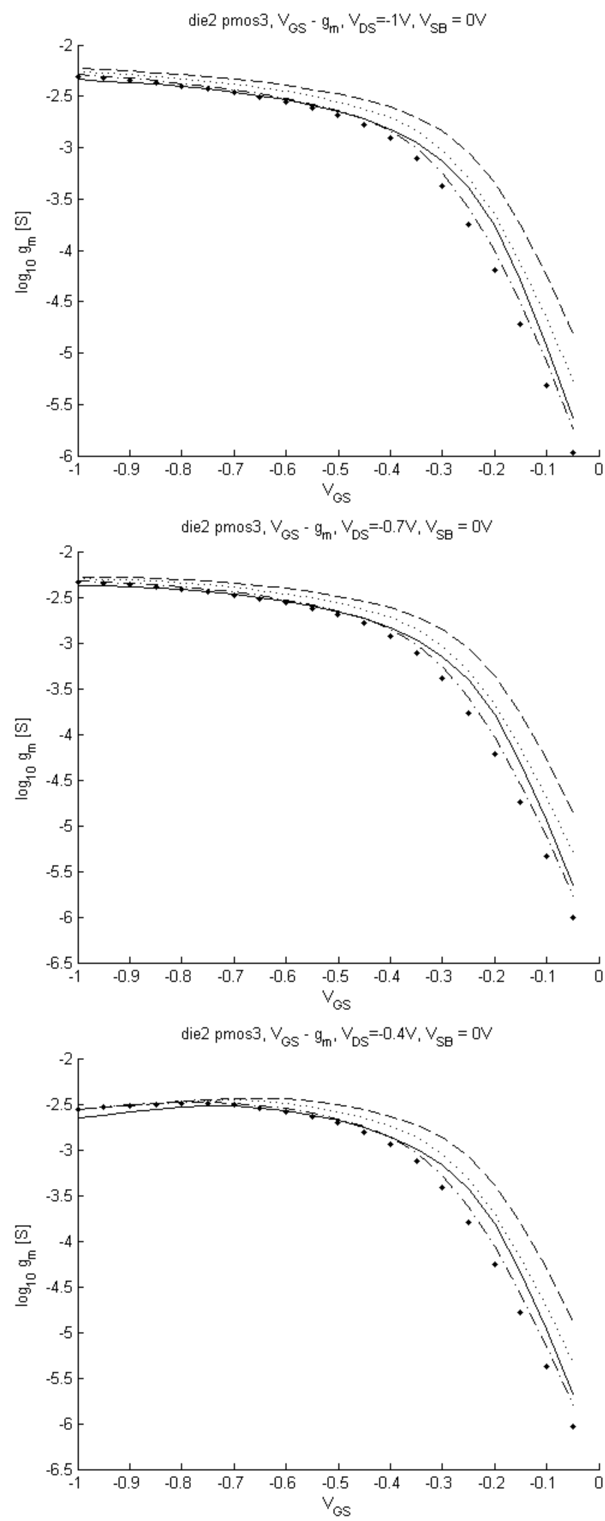

Figure 5.54: die2_pmos3 transconductance g_m.

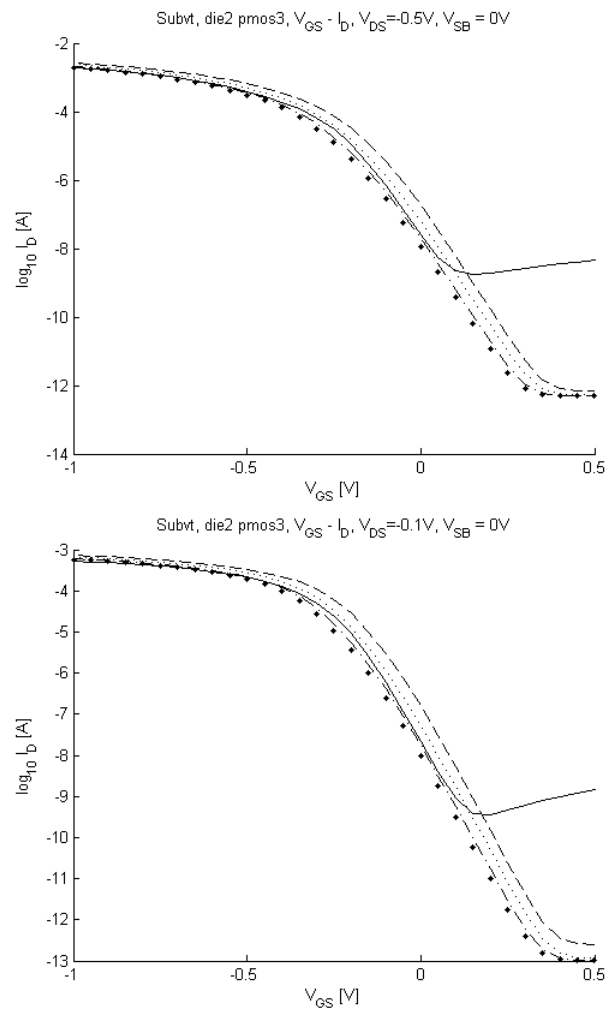

Figure 5.55: die2_pmos3 subthreshold conduction.

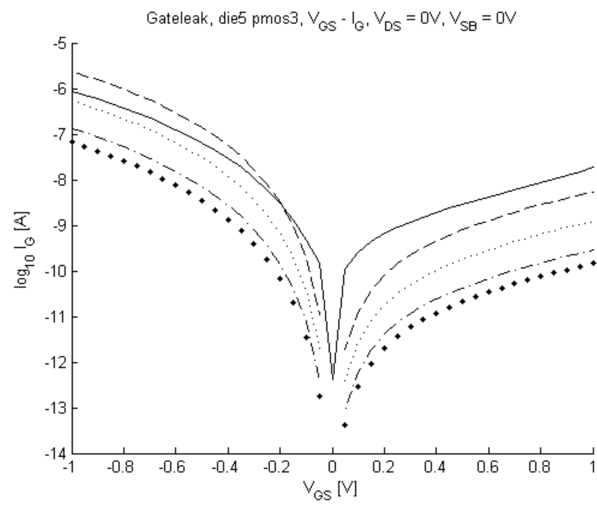

Figure 5.56: die5_pmos3 gate-leakage.

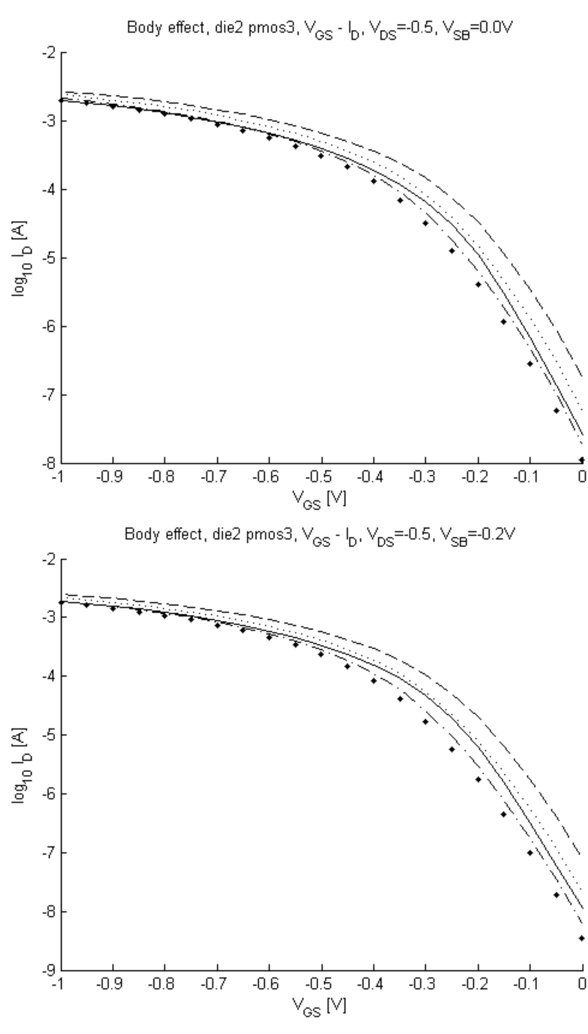

Figure 5.57: die2_pmos3 body-effect.

Chapter 6

Discussion for DC measurements at room temperature

In this chapter the DC measurement results and simulations are discussed. All plots were given in chapter 5.

6.1 Experience gained when accomplishing measurements

When performing the first IV measurements, the main criteria for approving the results was that the curves were quite similar to that of a typical MOSFET curve. Any unevenness in the curves were interperated as an outcome from bad contact between the probe tip and the test pad, and the probe tip would then be adjusted until a reasonable curve was achieved. The overall trend is that most of the final measurement results do not lie between the best-case and worst-case corner boundaries at all time.

When performing repeated measurements on die4 and die5 however, it was experienced that the placement of the probe on the test pad also influenced the level of the curves itself. This meant that it was possible to achieve i.e. a higher drain-current for a given drain-source voltage, by making very small adjustments with the probe after the first reasonable curve already had been achieved. This dependency on the probe contact with the pad showed to be very sensitive, and also not fully intuitive. The various devices did also not seem to suffer in the same degree to this dependency. One problem with this knowledge was that by repeatedly adjusting the probe softly, the pad would at some time be damaged. When this happened, the drain current

level of the device was reduced to a non-acceptable minimum.

The IV results has been achieved by balancing between obtaining the maximum performance of the various devices and not damaging the test pads. Investigations has shown that the final obtained measurements do not in any particular way suffer from pad contact resistance or routing series resistance.

It has been experienced that measurement time is strongly dependent on resolution and device type. With the chosen resolution given in chapter 4.1, the time consumption has ranged from 20 minutes to two hours for one sweep of a device.

6.2 Conformity between die1, die2, die4 and die5

Altogether the measurement results from die1, die2, die4 and die5 were quite the same. The choice between the similar devices from dissimilar dies to be plotted was made by using the maximum achieved drain current, smoothness of the curves and similarity to simulations as the basic criterias. Is has hence been assumed that is is allowed to choose devices from all the various die data available.

The gate-leakage data has however only been taken from the die5 results. The reason for this was that die5 was the only die where V_{GS} was swept from -1V to +1V. Die1, die2 and die4 was only swept from 0V when gate-leakage was investigated.

On basis of this the devices to be plotted were chosen, as already shown in chapter 5

6.3 V_{DS}-I_D (IV) characteristic

All V_{DS}-I_D physical measurements have in general much resemblance with the simulations, but has however a slight reduction in slope and maximum drain current compared with typical corner simulations. This deviation is in general larger in the linear region than in the saturation region. Calculations have shown that the reduction in drain current is not caused by series resistance from the metal conductors and pads on the die, hence it has not been necessary to take series resistance into account when accomplishing simulations.

The MOSFET drain-source conductance g_{ds} is also found from this data material, by using the definition from equation 2.6. The deviation between measured and simulated is naturally a consequence of the deviation in measured I_D It is seen that g_{ds} in general increases with reducing W/L.

6.3.1 Channel-length modulation

Device	$\lambda[1/V]$ measured	$\lambda[1/V]$ simulated, typical
die2_nmos0	1.733e-3	1.567e-3
die2_nmos1	0.433e-3	0.367e-3
die1_nmos2	0.467e-3	0.700e-3
die1_nmos3	0.193e-3	0.350e-3
die5_pmos0	2.633e-3	2.200e-3
die5_pmos1	0.300e-3	0.367e-3
die2_pmos2	0.733e-3	1.067e-3
die2_pmos3	0.267e-3	0.353e-3

Table 6.1: Extraction of channel-length modulation parameter λ from DC measurements and typical (TT) simulations, at $V_{GS} = 1V$ for NMOS and $V_{GS} = -1V$ for PMOS.

The plots also show that the drain current in saturation region slightly increases linearly with increasing V_{DS}. This is the *channel-length modulation*, and was expected on beforehand because of the short channel lengths. By investigating the slope of the curve in saturation, the channel-length modulation paramerer λ is found. The results are given in table 6.1. It is seen from the plots that this effect is more prominent for short devices than for the longer devices. It is somewhat surprising that λ for nmos2 and pmos2 is larger than for nmos1 and pmos1, even though the two latter have shorter gate lengths. The small discrepancies between measured and simulated λ is caused by issues that were discussed about the accomplishment of the measurements.

6.4 V_{GS}-I_D (IV) characteristic

These plots are just another way of investigating the V_{DS}-I_D, and hence course and maximum value of physical measurements is slightly reduced when comparing with typical simulations.

The MOSFET transconductance g_m is also found from this data material, by using the definition from equation 2.8. In general it is seen from the plots that g_m increases with increasing W/L. A trend for most devices is that g_m is situated outside the corners in strong inversion. More specifically, g_m is lower than the SS and SSA corners. The 90nm CMOS technology is capable of achieving higher gain in saturation than that of older technologies. This is because of the increase in I_D with decreasing gate length L, as seen in equation 2.5.

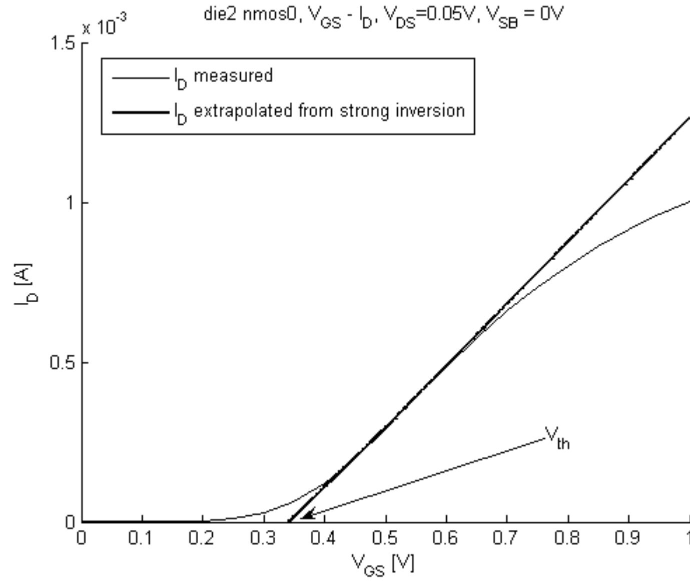

Figure 6.1: Showing principle of extracting V_{th} from DC measurements of nmos0.

6.4.1 Threshold voltage V_{th}

From the $V_{GS} - I_D$ characteristic the threshold voltage V_{th} can be found. To reduce the effect of DIBL but at the same time ensuring that the investigated device eventually reaches inversion, a small value of V_{DS} is preferable [40, chapter A]. Since this means that $V_{DS} < V_{eff}$, the device operates in linear region. By assuming a purely linear region, equation 2.5 can be written as

$$I_D = \mu_n C_{ox} \left(\frac{W}{L} \right) (V_{GS} - V_{tn}) V_{DS} \tag{6.1}$$

From this equation it is seen that by plotting $V_{GS} - I_D$ and linearly extrapolating the almost linear curve in strong inversion, V_{th} is found at the point where the extrapolated line intersects the x-axis. This is shown in figure 6.1. This method of extraction is however not ideal. First is that DIBL caused by V_{DS} may still influence V_{th}, even though it is small. For extracting V_{th}, $V_{DS} = 0.05V$ was used for NMOS and $V_{DS} = -0.05V$ for PMOS. Second influence is that of the small channel length L. Both of these two effects were reviewed in section 2.4. Using the saturation method instead, which means to ensure that the device is in saturation all the time and using equation 2.7, would only worsen the impact from DIBL and is therefore not of interest to be used.

The results are shown in table 6.2. All measured values of V_{th} are within

Device	$V_{th}[V]$ **measured**	$V_{th}[V]$ **simulated TT**	$V_{th}[V]$ **simulated FF**	$V_{th}[V]$ **simulated SS**	$V_{th}[V]$ **simulated SSA**
die2_nmos0	0.341	0.397	0.349	0.437	0.449
die2_nmos1	0.321	0.343	0.316	0.369	0.381
die1_nmos2	0.302	0.297	0.273	0.319	0.331
die1_nmos3	0.292	0.279	0.258	0.300	0.313
die5_pmos0	-0.270	-0.310	-0.266	-0.355	-0.373
die5_pmos1	-0.252	-0.266	-0.234	-0.312	-0.333
die2_pmos2	-0.239	-0.229	-0.187	-0.260	-0.282
die2_pmos3	-0.225	-0.214	-0.172	-0.251	-0.265

Table 6.2: Extraction of threshold voltage V_{th} from DC measurements and all simulations corners for $V_{SB} = 0.0V$, at $V_{DS} = 0.05V$ for NMOS and $V_{DS} = -0.05V$ for PMOS.

the simulation corners, except that of nmos0. More specifically, V_{th} for nmos2, nmos3, pmos2 and pmos3 tend to swing towards the slow corner while V_{th} for nmos0, nmos1, pmos0 and pmos1 tend to swing towards the fast corner. It was on beforehand expected that V_{th} would suffer more from small-channel effects for the devices with the smallest channel lengths. These effects spread out the flux lines of the electric field, and thus gate does not have the same control of the channel operation as it otherwise would have. With decreasing gate length L the threshold voltage V_{th} should decrease ([39, pp. 119-125]), and with decreasing gate width V_{th} should increase ([39, pp. 125-126]). The first is a *short-channel effect*, while the latter is a *narrow-channel effect*. However, it was on beforehand assumed that the narrow-channel effect would occur at widths smaller than that used for the 90nm transistors available. Because of this it is reasonable to expect that V_{th} would decrease for the smallest gate lengths L. The results in table 6.2 on the other hand do not support this expectation. Instead the results allege that the narrow-channel effect suppresses the short-channel effect. Since both the channel length L and width W varies for most of the the different MOSFETs, it is not appropriate to plot V_{th} as a function of either L or W.

It is however of importance to emphasize that there are many uncertainties associated with this method for investigating V_{th}. First is that of how the tangential line is drawn. It should be taken from the point at which the derivate of I_D is on its maximum. This can be interpreted as the point at which the line is most linear. It is seen that the MOSFET conducts current already before V_{th}, which is the subthreshold region. This is because the transition from cut-off to linear region is not abrupt. It is however reasonable to assume that the extraction method results in an overestimation of V_{th}. But the results in table 6.2 should give an indication of V_{th} for the various devices relative to each other and to simulations. Second disadvantage with this method is the impact from DIBL. V_{DS} is small, but it is still is not zero. Because of these two effects the V_{th} found with this linear

extrapolating method is more a device-specific V_{th}. The impact of these two effects increases as the technology is scaled down, and hence the results show the difficulties of investigating deep-submicron technologies with traditional methods. As will be seen in chapter 7 a technology-specific V_{th} can in theory be extracted from CV measurements without the influence of DIBL, provided a correct test setup.

6.5 Subthreshold leakage current I_{sub}

From the sub-threshold voltage curves it is obvious that the increase in drain current I_D starts already in the subthreshold region. This is in accordance with the simulations, except from that the initial I_{sub} in general is larger in physical measurements compared to the values from simulations. It has already been described how DIBL contributes to the subthreshold current leakage I_{sub} to a large extent. The plots supports this theory by showing that I_{sub} increases with increasing V_{DS} in the subthreshold region.

Device	**Subthreshold slope, measured** $[mV/decade]$ $V_{DS_{nmos}} = 0.1V$ $V_{DS_{pmos}} = -0.1V$	**Subthreshold slope, measured** $[mV/decade]$ $V_{DS_{nmos}} = 0.5V$ $V_{DS_{pmos}} = -0.5V$
die2_nmos0	83.3827	85.6480
die2_nmos1	73.6466	73.4501
die1_nmos2	72.3010	72.5594
die1_nmos3	72.3154	72.8371
die5_pmos0	87.9800	91.3511
die5_pmos1	73.4087	73.2934
die2_pmos2	72.2328	72.0530
die2_pmos3	72.2372	72.1071

Table 6.3: Extraction of subthreshold slope from linear part of logarithmic subthreshold plots at $V_{SB} = 0.0V$.

Table shows the results from calculating the subthreshold slope at the two different V_{DS} values plotted. The subthreshold slope indicates how fast I_{sub} increases with increasing V_{GS}. A fast slope means that V_{th} is is reached faster, hence a low V_{th} for the device. The most characteristic trend is that the devices with the smallest gate lengths L (nmos0 and pmos0) have a clear increase in slope with increasing V_{DS}. This is caused by the DIBL effect. The rest of the devices are in general less influenced by change in V_{DS}, and hence less influenced by DIBL. Some devices actually have a less steep slope when V_{DS} is increased. These results are more in accordance with the theory than that experienced when reviewing the extraction of V_{th} from DC measurements earlier.

The subthreshold plots give a rough indication of the point at which V_{th} occurs, in addition to the general $V_{GS} - I_D$ plots. Although the plots do not

use the same V_{DS} as that used when V_{th} was found by linear extrapolation, the subthreshold plots do however indicate the same trend of which corners V_{th} tends to swing towards. I_{sub}, and hence V_{th} is seen to reside within the simulated corners for all devices, including nmos0. When the curve begins to stabilize, a conducting channel is present and the device is on. The current seen in this region is the on-current of the transistor.

6.6 Gate leakage-current $I_G - V_{GS}$

As reviewed in section 2.4, the gate leakage current also becomes more noticeable with decreasing oxide thickness. This is therefore a very interesting parameter with respect to the 90nm CMOS technology investigated.

Plots show that the measured physical gate leakage for all devices is a little higher than that from typical corner simulations. It is obvious that I_G is quite large. For comparison a $0.35\mu m$ technology can have a gate leakage lower than the approximately 10fA noise floor of the measurement system. The plots also show that the gate leakage is not symmetrical when comparing a forward-biased device with a reverse-biased device. Instead the gate leakage is much smaller when the MOSFET is reverse-biased. This is because the reverse-biased device does not have a conducting channel present which can supply the gate with the same amount of electrons as that of the forward-biased device. Besides, the gate-leakage for the reverse-biased device is situated further away from the typical corner compared to that for the forward-biased device. Although I_G is lower at reverse-bias than at forward-bias, it is still prominent.

One very interesting result is the value of I_G relative to I_{sub} at reverse bias. It is seen that most of the devices have a gate leakage current I_G just slightly below or almost equal to the drain-to-source subthreshold leakage current I_{sub} at a low V_{DS}. Nmos3 and pmos3 actually have an I_G that is larger than I_{sub} at reverse-bias. I_G is necessarily several orders of magnitude lower than the drain-to-source current in inversion region. These observations supports the expectations to deep-submicron technologies reviewed in section 2.4.

6.7 Influence of body effect

It is seen that the subthreshold leakage current I_{sub} decreases slightly with increasing V_{SB}. This is because of the increase in V_{th} with increasing V_{SB}, and is in accordance with the theory from section 2.4. Since $_{sub}$ decreases, it takes a longer time before the theoretical maximum current capacity I_D is reached and hence V_{th} is shifted toward a higher level. This is known as the body effect. The measured drop at V_{GS} is given in table 6.4, where it

Device	Drop in I_{sub} at $V_{GS} = 0V$ [A]
die2_nmos0	24.04e-9
die2_nmos1	2.92e-9
die1_nmos2	5.46e-9
die1_nmos3	4.25e-9
die5_pmos0	121.38e-9
die5_pmos1	4.66e-9
die2_pmos2	20.01e-9
die2_pmos3	14.06e-9

Table 6.4: Drop in I_{sub} av V_{GS}, when changing V_{SB} from 0.0V to 0.2V for nmos devices and from 0.0V to -0.2V for pmos devices.

is seen that the drop in general is large for devices with large W/L. This drop must be seen in accordance with the maximum current capability of the device when it is fully on.

It was previously found that the extraction of V_{th} from DC measurements of deep-submicron technologies most possibly suffer from inaccuracies and additional effects. The CV characterization in chapter 7 has therefore been found more applicable for specifically extracting the body-effect coefficient γ.

6.8 Future improvements for test-structure layout of 90nm prototype dies regarding DC measurements

It has been found that the layout structure itself present at the 90nm prototype dies is fully applicable for DC measurements. The sharing of gate, source and bulk test pads for each set of four nmos and pmos transistors does not result in any limitations for the accomplishment of the measurement itself. However it could be of interest to have a set of transistors with either fixed W and varying L or vice versa, to be able to investigate the small-channel effects in more confident way.

Chapter 7

Results and discussion for AC measurements at room temperature

This chapter will present the accomplishment of AC measurements, along with accompanying discussion to relate the results up against the theory. Thereafter various practical methods found in the literature for extracting the parameters V_{FB}, C_{ox}, t_{ox} and V_{th} are investigated. It has been found that CV characterization of devices with very thin oxide thickness complicates this extraction process, but that the instrumentation available helped on this to a great extent. The most important papers regarding parameter extraction from CV characteristics especially concerning ultra-thin gate dielectrics have been found to be [8] and [12].

The effect of chuck noise discussed in section 4.3 was only experienced for frequencies lower than that required by the ultra-thin oxide measurements. That is, lower than 1MHz. Therefore the standard C_{gb} with gate to HI and bulk to LO have been used instead of the opposite connection that was recommended is section 4.3.2. The advantage of this is that the plots become more directly comparable with the theory, otherwise they would be mirror imaged. Except from this, the preparations and actual measurements have been accomplished in accordance with the discussion in chapter 4.3.

The AC measurements and simulations in this chapter treat the four NMOS devices as one large device, and the four PMOS devices as another large device. Thus the focus is on these large devices rather than investigating each separate transistor. This method makes the results more accurate since the capacitance levels to be measured become larger. In addition it is just as good for parameter extraction as that of investigating each device separately. The choice of this method comes naturally due to the layout of connections

between the test pads and the transistors. Therefore all plots of capacitance in this chapter shows the total capacitance of all four nmos or pmos device, and not device-specific capacitances. Hence the focus is on the technology itself. To emphasize this through this chapter, the names NMOS and PMOS are used without any numbering.

All measurements have been accomplished with an AC test signal level of 20mV_{rms}. Initial measurements showed that reducing the test signal amplitude to e.g. 5mV_{rms} resulted in a more uneven slope, while increasing the test signal amplitude to e.g. 30mV_{rms} resulted in a slight decrease in the measured capacitance level in depletion. 20mV_{rms} was therefore found to be optimal.

The so-called *two-frequency technique* was used to achieve reasonable results specifically for the ultra-thin oxide technology. According to [4, chapter 7.1], this method makes if possible to extract the capacitance C for a three-parameter equivalent circuit based on results obtained from extractions with a two-parameter equivalent. Hence the simplification showed in figure 4.10 is reversed. It aims at measuring C_p at two different frequencies, with a spacing such that the difference in measured C_p is quite large. Then the capacitance of the ultra-thin oxide is calculated according to the following equation ([4, chapter 7.1]):

$$C = \frac{f_1^2 C_{p1}(1 + D_1^2) - f_2^2 C_{p2}(1 + D_2^2)}{f_1^2 - f_2^2} \tag{7.1}$$

where
f_1, f_2 = the two frequency points
D_1, D_2 = dissipation at the two frequency points (see equation 2.16 in section 2.5.5)
C_{p1}, C_{p2} = capacitance at the two frequency points

This method has been used for all plots and results given. By measuring the impedance at these two frequencies f_1, f_2, C_p and D have been extracted with the built-in parallel two-parameter equivalent circuit of the 4294A. Then the final results have been calculated manually. Tests showed that it was necessary with a test signal frequency of at least 10MHz for this thin-oxide technology to achieve the required accuracy. Two sets of frequencies have been used: 80MHz together with 20MHz, and 100MHz together with 40MHz. The parallel two-parameter equivalent model was chosen to extract results from the impedance measurements itself, since this in theory should model the capacitance of ultra-thin oxides best possibly.

It has not been possible to extract the on-die parasitics caused by structures other than the DUT itself. The reason for this was that there was no dummy-

structure available on the prototype dies. Hence all plots shown include these additional parasitic capacitances. It is however possible to extract much information from the measured capacitance, since this is a constant capacitance that increases the overall level of the measurement. As will be seen the level of additional capacitance can be estimated for some of the plots, and hence be subtracted before parameter extraction. Since no dummy-structure is available, it is difficult to investigate the quantity of the small overlap capacitance C_{ol}. The investigation of the results will therefore not take this capacitance into account.

7.1 Experience gained when accomplishing measurements

The procedure of performing compensation for each time the relative probe spacing was changed was very time consuming, but absolutely required. At least after initially powering up the instrument. The frequencies used in the measurements were mainly chosen such that the results at two different frequencies had large variations relative to each other, but also in accordance with the verification measurements after compensation. When connecting the COMMON level of the Keithley 4200-SCS to the virtual ground of the Agilent 4294A (see section 4.3.2), a standard coaxial Y-adapter was utilized at the front of the 4294A to create an extra output line. This method of branching demonstrated to worsen the results from compensation, resulting in less frequencies that fulfilled the demands of both precision and high frequency. Because of this it was necessary with the two sets of frequencies as already specified.

The constant repetition of landing the probes, measuring, changing relative probe spacing, performing new compensation and landing the probes again resulted in a high number of landings on the test pads that were common for most of the measurements. This was especially true for the gate pads, and so carefully planning was necessary to exploit the whole area of the gate pad such that it was not destroyed. It was experienced that each pad could handle a maximum of approximately 6 landings. However, this number was reduced according to the angle from which the probe was coming from. Since each test usually required a specific setup of the probes relative to each other, the number of maximum probe landings was therefore usually lower.

As for the IV-plots, the CV measurements also showed to be dependent on good contact between probe and test pad. However, this dependency was not as prominent as that experienced with the IV measurements. Instead a sufficient contact between probe and pad was either achieved or not achieved, with mainly no intermediate situations. Nevertheless this did not

make the CV measurements easy to accomplish. The main reason for this was the challenge of interpreting whether unexpected results actually were caused by the measurement setup, oxide damage or deep-submicron effects. To illustrate this, the NMOS devices of two prototype dies were measured, resulting in very unexpected results. By using the exactly same test setup and instrumentation on a third prototype die, results pursuant to that expected from the theory was achieved. The problem of knowing whether a device actually has any damage could have been solved by investigating the same device with IV measurements afterward. This would however require a change in test setup, and also an unacceptable increase in the total number of pad landings.

7.2 Presentation of AC measurement results

The following presents the plots for all AC measurements (solid line), along with TT corner simulations (dotted line), SS corner simulations (dashdot line) and FF corner simulations (dashed line) - at room temperature 27° and in total darkness. Any exceptions from this in later sections will be pointed out. However, first an evaluation of possible measurements with the test equipment available is necessary.

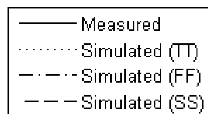

Figure 7.1: Legend for all AC plots.

7.2.1 Evaluation of possible CV measurement methods

It is on beforehand of interest to evaluate to what extent the CV measurement methods described in section 4.3.2 are possible to actually be accomplished. Because of the fixed layout of the 90nm prototype dies, it is obvious that not all tests are feasible. In general all tests where either HI or LO is connected to more than one node can not be directly carried out. If this was to be accomplished, layout must have been changed specifically for that test or probes must have been physically interconnected. Neither of these two methods were possible, which excluded the direct measurement of C_{gg} and C_{gc}. However, the latter can be measured with bulk and either drain or source floating in a two-probe configuration.

The measurement of C_{gd} would require stepping the source DC bias with the Keithley 4200-SCS to provide for a V_{GS}, since the potential between HI

and LO nodes of the Agilent 4294A is only defining the V_{DS}. In addition there are a total of 8 different transistors with separate drain connections. In sum this would result in a very large amount of data, and hence it would be favourable to have a pre-assembled program package for the Keithley 4200-SCS to accomplish this setup and data acquisition. This is one reason for not measuring C_{gd}. But the main reason is that each change in probe setup from one drain pad to another would require repeatedly compensation, which further would result in an unacceptable number of probe landings on those pads common for all measurements.

Finally the measurement of C_{gb} and C_{gs} must be accomplished in a three-probe configuration. This is because gate, source and bulk are common for all transistors while only drain have separate pads. Hence it is not possible to bias all four drain pads with only one probe available, and so drain must be floating. As a consequence of this, C_{gs} will not drop at $V_{DS} + V_{th}$ as shown in figure 2.13, but instead include C_{gd} over the whole sweep. The measurement of C_{gs} with drain floating will therefore achieve approximately the same results as when measuring C_{gc} with either drain or source floating. For C_{gb} the drop at V_{th} as discussed in section 4.3.2 will be present, since source is providing for the external supply of minority carriers when the device enters inversion.

By combining the information obtained from measurements of C_{gc} and C_{gb} in a three-probe configuration, the overall C_{gg} is found. C_{gc} and C_{gb} will therefore be investigated further. The measurements that will be shown have been taken from measurements on die3, die5, die6 and die7.

7.2.2 Gate-to-bulk capacitance C_{gb} with drain and source floating

The measurement of C_{gb} is interesting for investigating the accumulation and depletion region of the total C_{gg}. Plots for C_{gb} with drain and source floating for both NMOS and PMOS are shown in figure 7.2. The purpose of measuring C_{gb} with drain and source floating is to show the effect of not having an external supply of minority carriers when the device enters inversion. Because of this, C_{gb} does not drop towards zero at V_{th} as seen in figure 2.13 but rather settles at a higher capacitance value. This is in accordance with the discussion in section 4.3.2.

The measurement of C_{gb} with drain and source floating are very interesting for initial investigation of the additional on-die parasitic capacitances that arise from other sources than the DUT. It is seen from the plots that this additional capacitance is larger when measuring the NMOS structure compared to that for the PMOS structure. The level of the additional capacitance can however not be estimated, since there is no known zero-level.

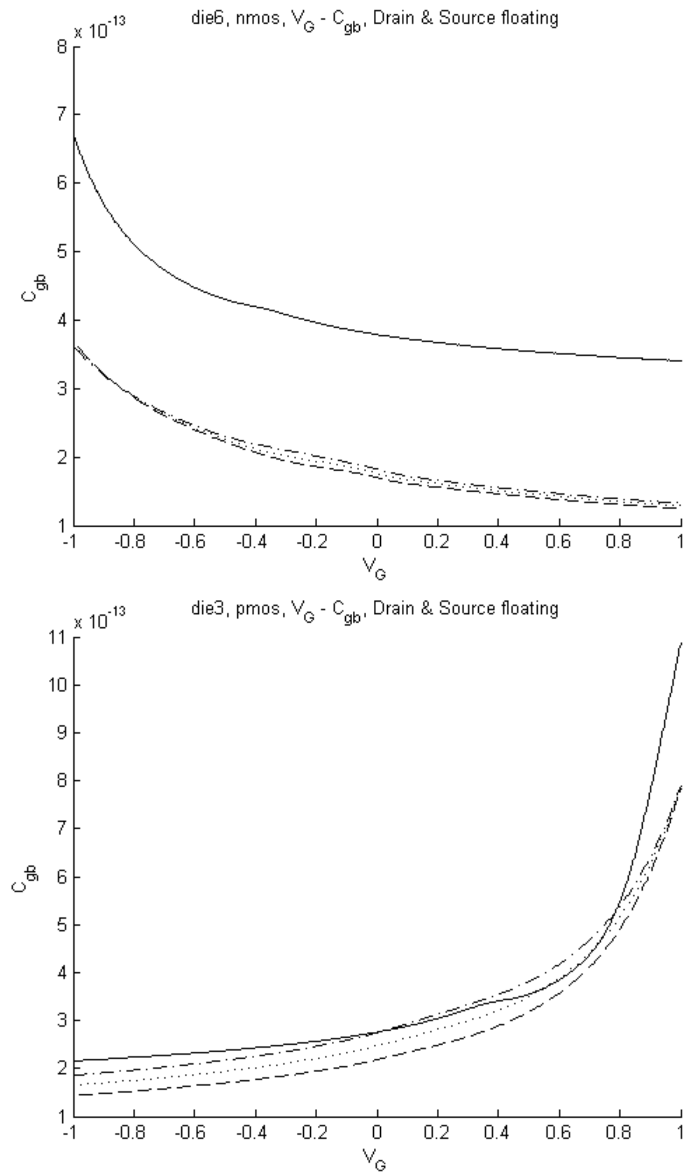

Figure 7.2: Measured and simulated C_{gb} for nmos and pmos with all drain nodes and source floating.

7.2.3 Gate-to-bulk capacitance C_{gb} with drain floating and source connected to external DC bias

Plots for C_{gb} with source connected to external DC bias and all drain nodes floating for NMOS and PMOS are shown in figures 7.3 and 7.4 respectively. Now C_{gb} has an additional drop at V_{th} as expected. The maximum capacitance in depletion for PMOS is slightly higher than that found in figure 7.2. Main reason for this is that the two measurements were accomplished at different times during the project, and illustrates that repeated CV measurements on deep-submircon devices still may generate different results.

These plots give a better view of on-die additional capacitances compared to C_{gb} with drain and source floating. It is reasonable to assume that this capacitance can be seen as a constant capacitance that is equal to the minimum value of C_{gb} in inversion. The actual C_{gb} is then superimposed on this constant capacitance, increasing the overall capacitance level. This trend is seen in depletion as well. But since the ideal value in inversion is not known except from that found by simulations, it is not preferable to extract the additional on-die capacitance from this region. In inversion however, C_{gb} should ideally drop to approximately zero after V_{th} has been reached. This leads to an additional capacitance of approximately 290fF for NMOS and 115fF for PMOS for C_{gb} from figures 7.3 and 7.4 respectively.

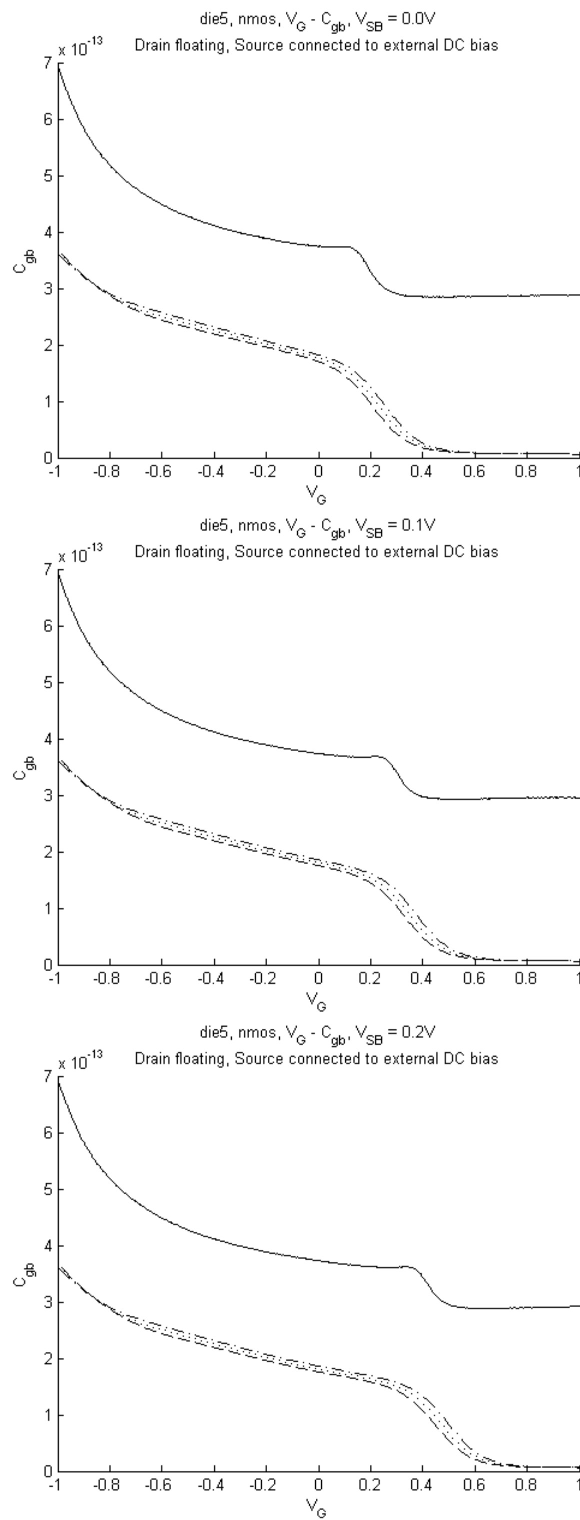

Figure 7.3: Measured and simulated C_{gb} for nmos with all drain nodes floating and source connected to external DC bias..

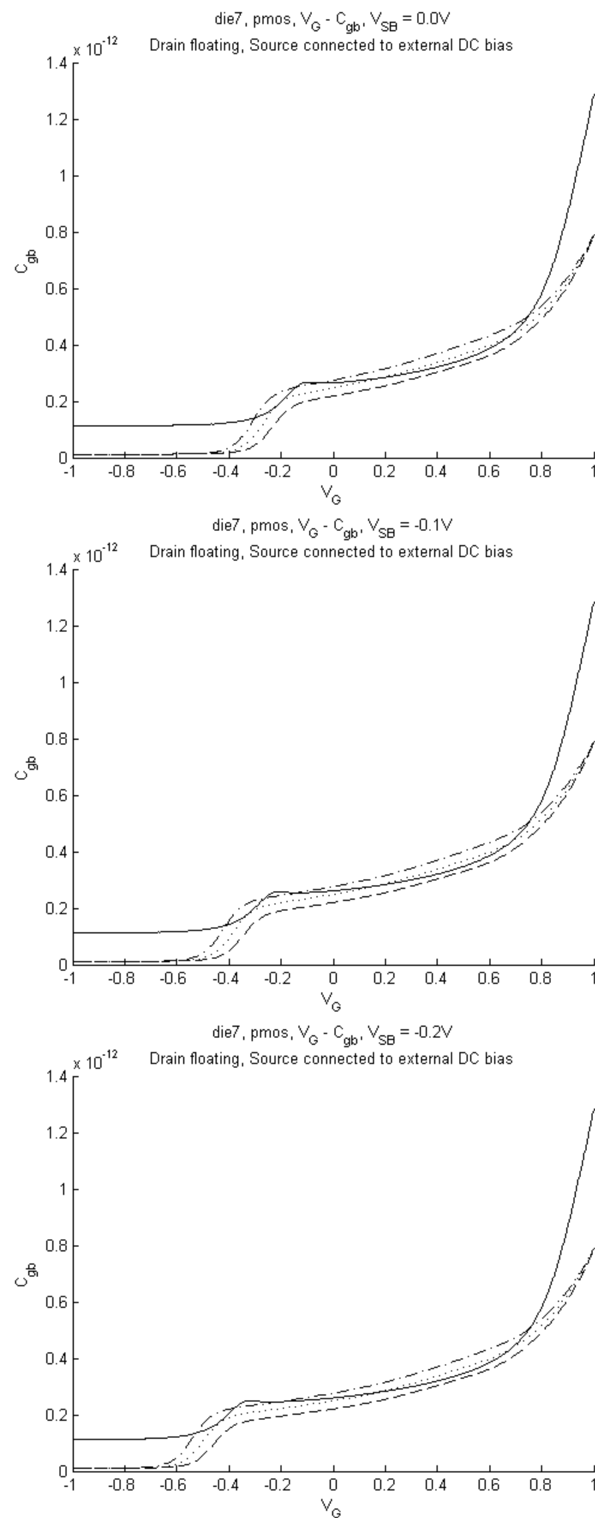

Figure 7.4: Measured and simulated C_{gb} for pmos with all drain nodes floating and source connected to external DC bias.

7.2.4 Gate-to-channel capacitance C_{gc} with bulk and either drain or source floating

By plotting C_{gc} the inversion region of the total C_{gg} can be investigated. To measure C_{gc} it was necessary to simplify the measurement setup reviewed in section 4.3.2. Since it was not possible to tie drain and source together because of the layout and instrumentation available, only either drain or source was connected to the LO node. In this way the capacitance seen over these two nodes, e.g. between gate and source when drain is floating, would represent the total C_{gc}. This because the unconnected node is floating and hence not in contact with the conducting channel in linear region.

The circuit simulator is not capable of calculating C_{gc} directly. Therefore the simulated capacitance C_{gc} has been found by assuming that C_{gc} is equally shared between drain and source in linear region since drain is floating. The justification for this approximation was reviewed in section 2.3.2. By simulating C_{gs} or C_{gd}, half of the total C_{gc} is thus found. Finally the total C_{gc} is calculated by adding together these two capacitances.

Plots of C_{gc} for NMOS and PMOS are shown in figures 7.5 and 7.6 respectively. When measuring C_{gc}, all drain nodes have been successively connected as well as the source node. The measurement of C_{gc} for PMOS seem to suffer from an additional effect, creating large peaks in inversion. The unconnected nodes that are left floating may be the cause of these effects. However, all plots finally stabilizes in strong inversion. It has previously been stated that the measurement of C_{gs} with drain floating is effectively the same measurement as the method used for C_{gc}, only with HI and LO of the impedance meter interchanged. Separate measurements of C_{gs} have been carried out as well, but since this does not result in any new information relative to the C_{gc} found it will not be presented here.

Any estimation of additional on-die capacitance caused by other structures than the DUT is difficult for the C_{gc} results. This is because a zero-level point is not known in the same way as it was for C_{gb} with source connected to external DC bias.

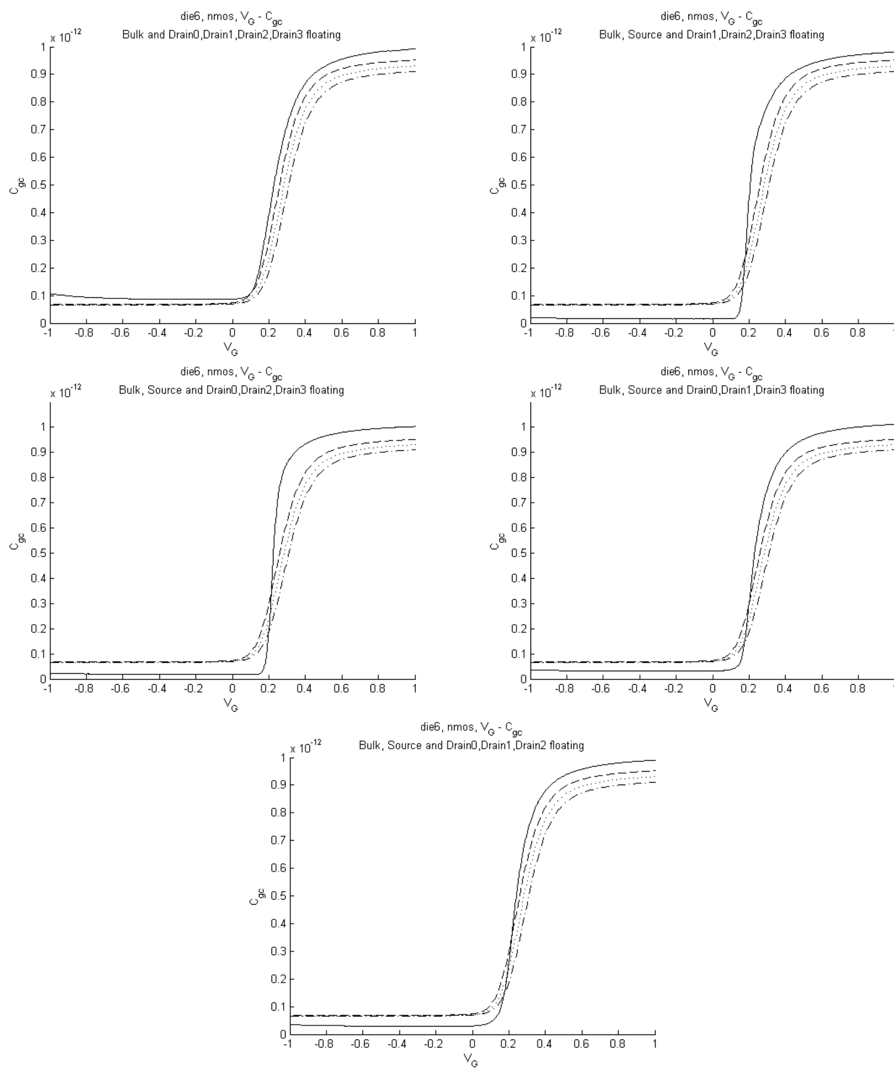

Figure 7.5: Measured and simulated C_{gc} for nmos with bulk and either drain or source floating.

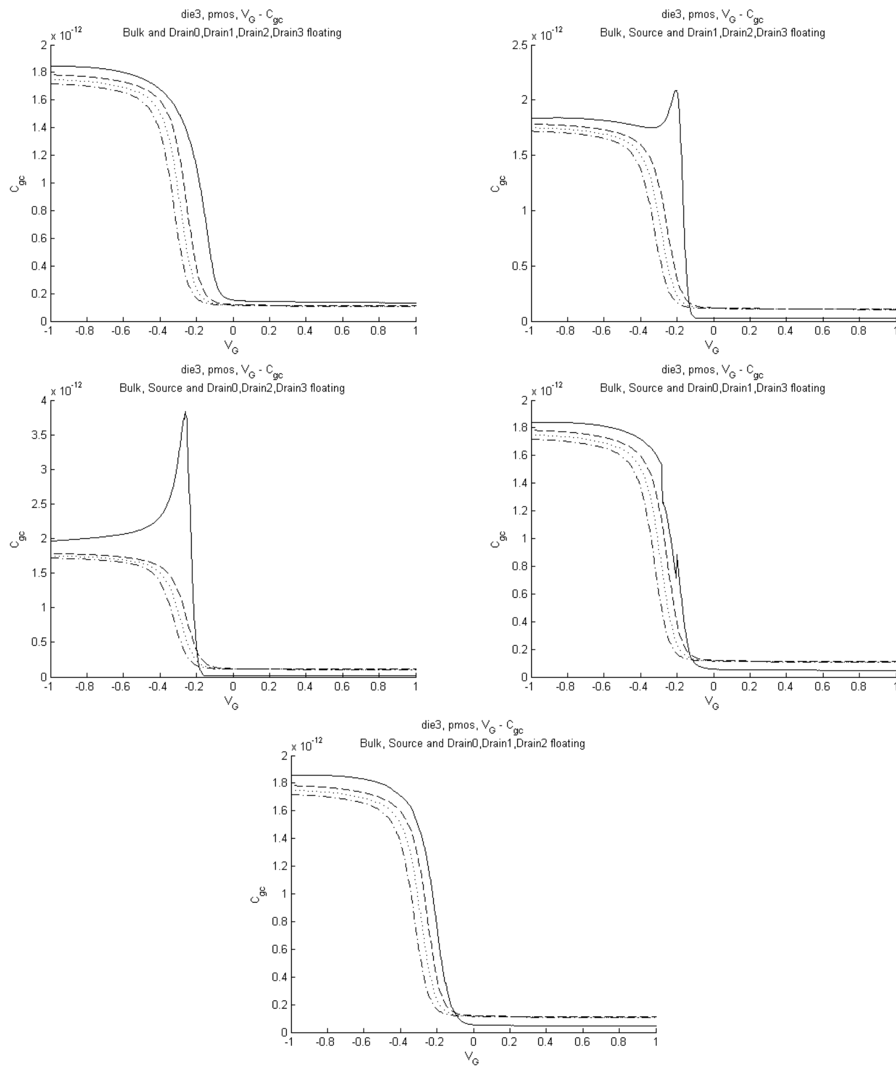

Figure 7.6: Measured and simulated C_{gc} for pmos with bulk and either drain or source floating.

7.3 Extraction of threshold voltage V_{th}

The CV measurement results are very useful for extracting the threshold voltage V_{th} in a simple and exact way. According to [40, chapter A], [41] and chapter 2, V_{th} is found by searching in the transition between depletion and inversion for the measured C_{gb} with source and drain grounded by using equation 7.2:

$$V_{th} = MAX\left(\frac{dC_{bg}}{dV_B}\right) \tag{7.2}$$

This is because of the rapid change in bulk charge when the device enters strong inversion, when the conducting channel becomes present (see figure 2.13. It is interesting to notice that the method is not influenced by the overall measured level of the capacitance, but rather the point at which this transition appears. Hence it should not suffer from any increase in measured capacitance level due to additional on-die constant parasitics.

The advantages with this method compared to the method used in chapter 6 is that it does not suffer from drain and source resistance, since there is no current flowing between these two diffusions. It will not be affected by the DIBL effect either, since drain and source are at equal potential.

For accomplishing this extraction, C_{gb} from figures 7.3 and 7.4 was used for NMOS and PMOS respectively. Source then provided for the external supply of charge carriers necessary when the device entered inversion at V_{th}. The results after applying equation 7.2 is shown in figures 7.7 and 7.8, where the measured V_{th} and typical corner V_{th} are pointed out. The curve in figure 7.7 is more uneven because it was necessary to increase the DC bias level of the impedance meter, which reduces the measurement precision.

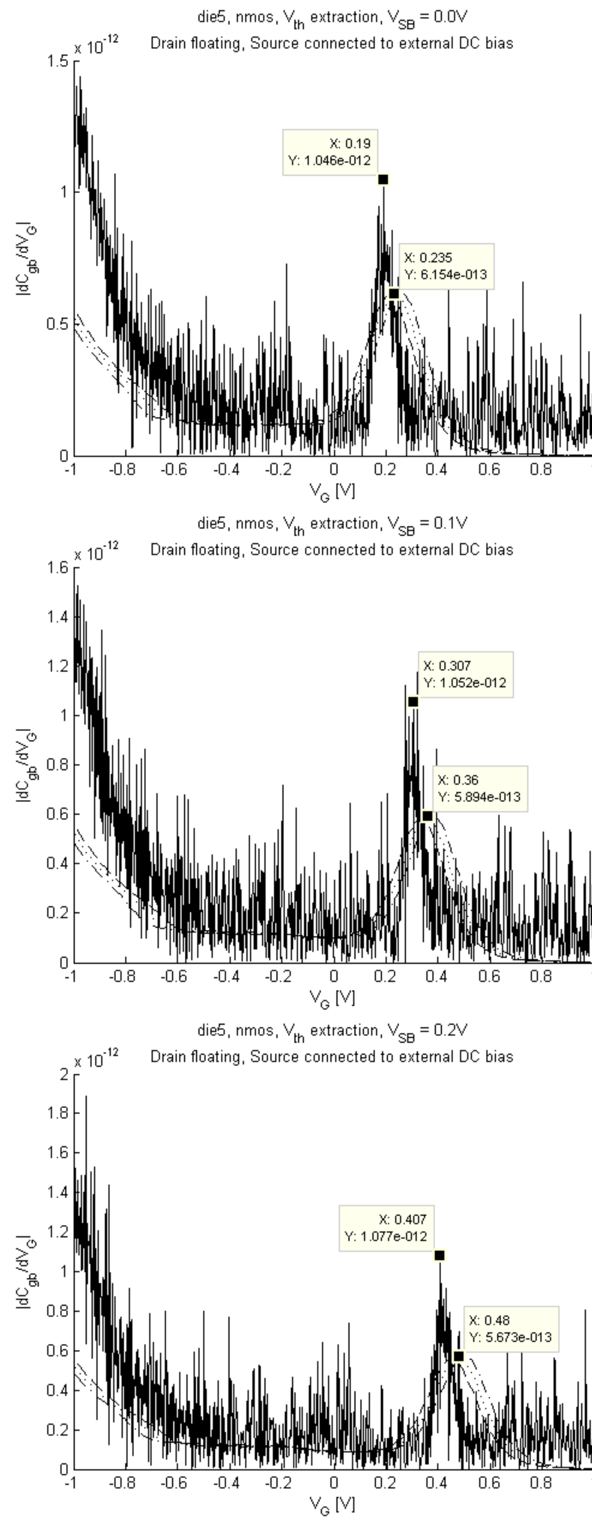

Figure 7.7: Extraction of V_{tn} at different V_{SB} from C_{gb} with drain floating and source connected to external DC bias.

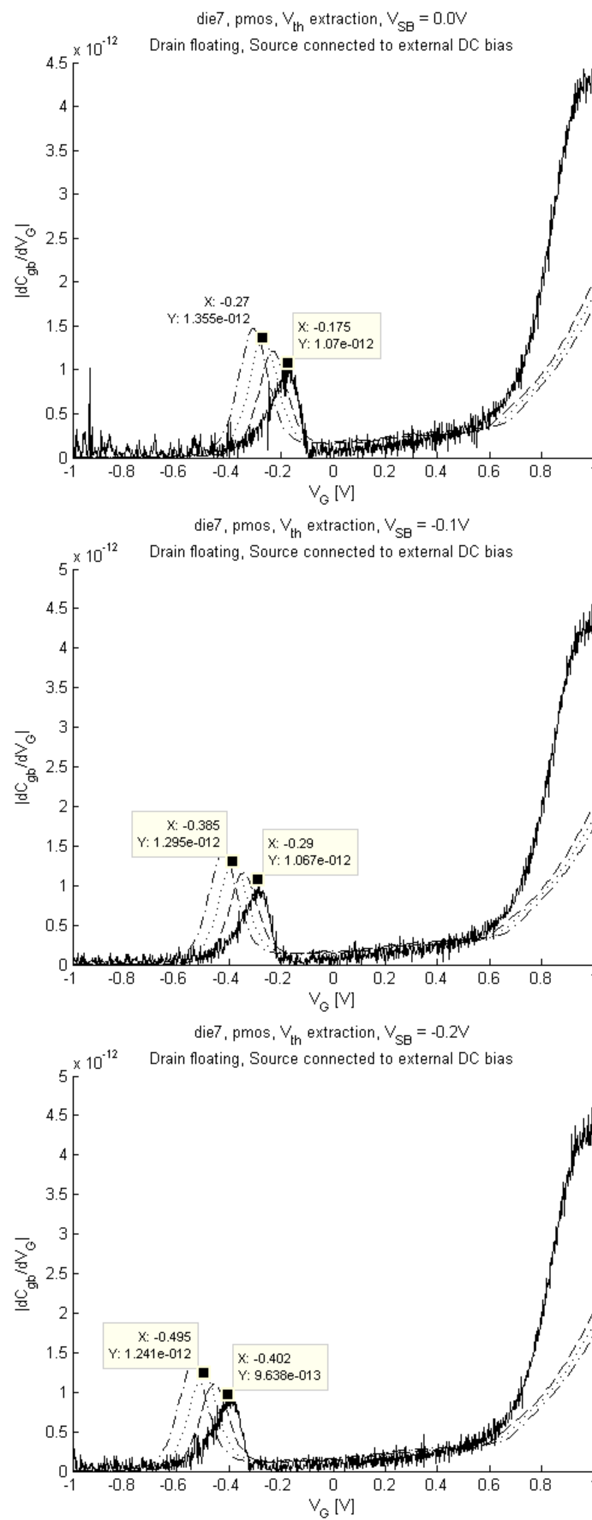

Figure 7.8: Extraction of V_{tp} at different V_{SB} from C_{gb} with drain floating and source connected to external DC bias.

Device	$V_{th}[V]$ **at** $\lvert V_{SB}\rvert = 0.0V$	$V_{th}[V]$ **at** $\lvert V_{SB}\rvert = 0.1V$	$V_{th}[V]$ **at** $\lvert V_{SB}\rvert = 0.2V$
`NMOS (measured)`	0.190	0.370	0.407
`NMOS (simulated TT)`	0.235	0.360	0.480
`NMOS (simulated SS)`	0.260	0.380	0.500
`NMOS (simulated FF)`	0.215	0.335	0.450
`PMOS (measured)`	-0.175	-0.290	-0.402
`PMOS (simulated TT)`	-0.270	-0.385	-0.495
`PMOS (simulated SS)`	-0.305	-0.420	-0.535
`PMOS (simulated FF)`	-0.230	-0.345	-0.455

Table 7.1: Extraction of V_{th} from measurements and simulations.

From the plots in figure 7.7 and 7.8, V_{th} at the three different values of V_{SB} is found and can be compared to values of V_{th} found simulations obtained with the same method. This is summarized in table 7.1.

The DC biasing of source only should be sufficient for providing the external supply of minority carriers when the device enters inversion region, leaving drain floating. But ideally the measurement of C_{gb} should be accomplished with both drain and source biased to zero volts, hence not leaving the drain nodes floating. It is seen from the plots in figures 7.3 and 7.4 that the drop in capacitance at V_{th} is slightly smaller when compared to the simulations. According to the review in section 4.3.2, any floating drain nodes would introduce additional parallel capacitance in the measurement. Measurement of C_{gb} with each drain pad successively connected in addition to the source pad is shown in figure 7.9. It is seen from the figure that the subtraction of these additional parallel capacitances caused by the floating drain nodes does not result in any particular increase in drop at the transition from depletion to inversion. Any constant increase in overall capacitance from floating nodes would still not affect the extraction of V_{th}, since this method only depends on the point at which the drop itself occurs rather than the capacitance level.

It is seen that the extracted V_{th} in all cases are outside the simulation corners, and tend to represent very fast devices. It was from the DC measurements found that V_{th} for all devices was situated within the corners, from which these AC results therefore differ. This difference is actually quite drastic for the PMOS devices.

Although it was found that the floating drain nodes did not introduce any major additional capacitance in the measurement, the connection setup does still not resemble that of a MOSFET under normal operation. A prerequisite

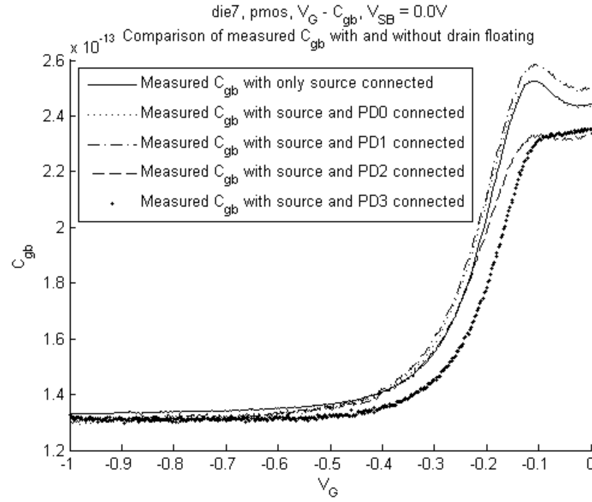

Figure 7.9: Investigation of effect on C_{gb} measurement when connecting drain nodes in addition to source.

for this method to be able to prevent the influence of DIBL was precisely that of having drain and source at equal potential. But since drain now is floating, potential V_{DS} between drain and source is not actually known exactly. Hence the device may be suffering from DIBL, which lowers V_{th}. A verification of this can be found by investigating the measured C_{gc}. From the review in section 2.3.2 it was seen that C_{gc} starts to increase approximately at V_{th}. However, from the plots of C_{gc} in figures 7.5 and 7.6 it is found that the point at which this increase occurs varies depending on the connection setup. The difference is not so large for the NMOS, but it is obvious that the transition takes place slightly earlier when drain is floating compared to when source is floating. For the PMOS this difference is much more prominent. This observation explains the results found from the plots in figures 7.7 and 7.8, where V_{th} occurs earlier than that found from simulations when the drain nodes are floating. This change in point at which transition between depletion and inversion occurs was on the other hand not experienced with the circuit simulator. On the background of this discussion, both drain and source should have been biased to zero volts to ensure a known V_{DS}.

7.4 Extraction of flatband voltage V_{FB}

The $1/C_{gb}^2$ versus V_G method can be used for finding the flatband voltage V_{FB}. This is a classical method, also used in [12, figure 2]. By plotting $1/C_{gb}^2$ versus V_G for the depletion region, V_{FB} is found by extrapolating the straight line found in depletion until it intercepts the x-axis. This interception point

is then equal to V_{FB}. The behavior of this method is quite intuitive: When sweeping through depletion toward accumulation, the $1/C_{gb}^2$ is very straight due to its approximately constant slope. But as V_{FB} is reached, the slope starts to decrease until finally settling at a more constant value. This decrease does not take place abruptly, and so extrapolating these last points in depletion with a straight line would give a somewhat satisfactory value of V_{FB}.

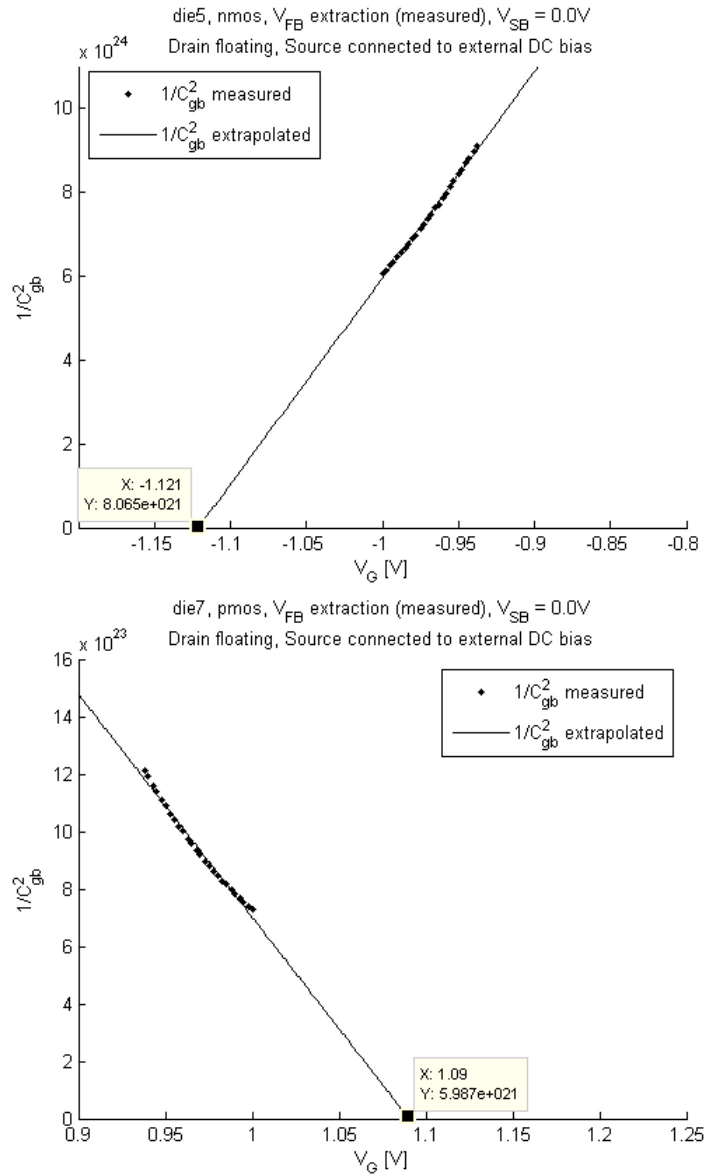

Figure 7.10: Extraction of V_{FB} from C_{gb} measurements.

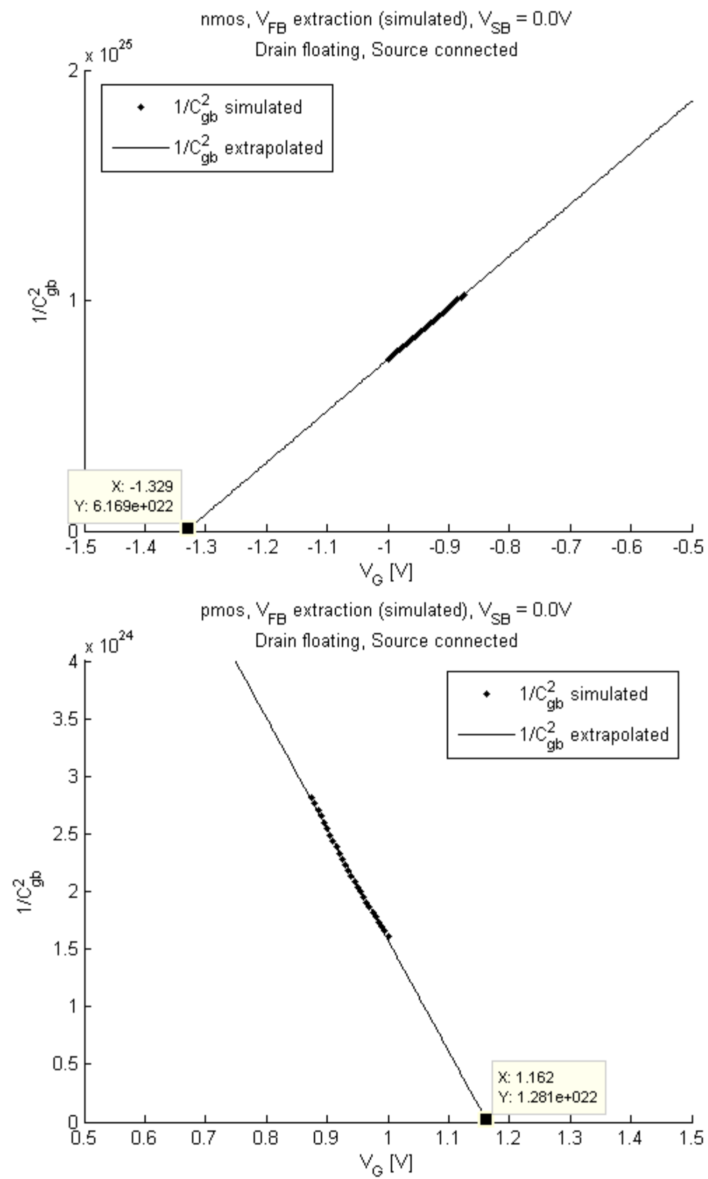

Figure 7.11: Extraction of V_{FB} from C_{gb} simulations.

Device	$V_{FB}[F]$
NMOS (measured)	-1.121
NMOS (simulated TT)	-1.329
PMOS (measured)	1.090
PMOS (simulated TT)	1.162

Table 7.2: Extraction of V_{FB} from measurements and typical corner simulations.

The method described above was used on the data from figures 7.3 and 7.4. Expected increase in overall capacitance level caused by other additional on-die parasitics was on beforehand subtracted, since this affects the extraction process. Plots showing the extraction method used on the measured and simulated C_{gb} are given in figures 7.10 and 7.11 respectively. The results from the extraction for both measurement and typical corner simulations are given in table 7.2. It is seen that V_{FB} extracted from measurements is smaller than V_{FB} found from typical corner simulations. A reasonable explanation for this is that the C_{gb} slope at the end of the measured depletion region is higher for the measured data than for the simulated data, even though the additional on-die capacitance has been subtracted. Hence the measured data is closer to V_{FB} than the typical corner simulations.

7.5 Extraction of gate capacitance C_{ox} and gate oxide thickness t_{ox}

From the CV measurement results, C_{ox} can be found as the maximum C_{gg} of the MOSFET. This can further be used for extracting t_{ox}. Since C_{gg} tend to be symmetrical, both accumulation and inversion can in principle be used for extracting C_{ox} and further t_{ox}.

7.5.1 Finding C_{ox} and t_{ox} from accumulation region

The traditional way of finding t_{ox} is to bias the device into strong accumulation, and then read out the maximum capacitance $C_{max} \approx C_{ox}$ in this region. From this, t_{ox} can be calculated by using equation 2.12. This method works well for thick-oxide technologies. For thin-oxide technologies like the 90nm investigated in this master thesis however, the maximum voltage rating to avoid oxide breakdown is a limiting factor. It has been shown that the flat-band voltage V_{FB} of the technology was not reached within the maximum voltage limit $\pm 1V$. Hence the resulting sweep did not reach a saturated accumulation, only covering inversion and partly depletion. If the maximum

capacitance value obtained within this voltage limit was used, the extracted t_{ox} would clearly be larger than the actual t_{ox}.

This problem of unsaturated accumulation is described in [8, p. 106]. The same article propose a method (the Vincent method) for extracting t_{ox} from measurements where saturated accumulation is not achieved, by basically extrapolating the increasing depletion curve until strong accumulation is obtained. V_{FB} is used as the point where strong accumulation appears. By plotting $1/C_{gb}$ versus $\frac{1}{(V_G - V_{FB})^{1/n}}$, C_{ox} can then be found at the point at which the curve intercepts the y-axis when the x-axis is equal to zero. This method basically shifts the curve according to V_{FB} that was found previously, and assumes that the last points of the depletion can be extrapolated until $VG = V_{FB}$ and accumulation is obtained. The parameter n is determined by the type of statistics assumed for the distribution of the charge carriers within the semiconductor in accumulation, where Boltzmann statistics, quantum statistics and degenerate metallic statistics are listed. [12] refines this method, by finding the optimal value of n according to the expected t_{ox} of the technology. In this master thesis the results from [12, table 2] has been interpolated to achieve $n = 1.0535$ for a oxide thickness of 1.95nm, assuming an actual oxide thickness of 2nm for the 90nm technology.

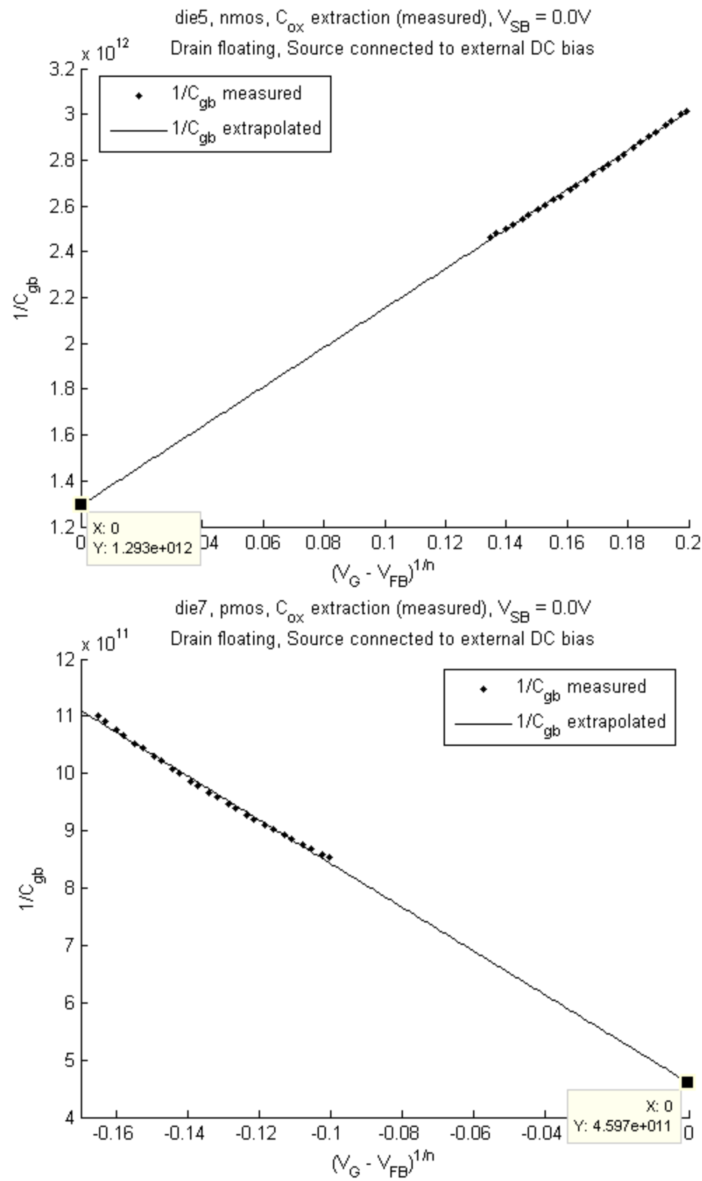

Figure 7.12: Extraction of C_{ox} from measurements.

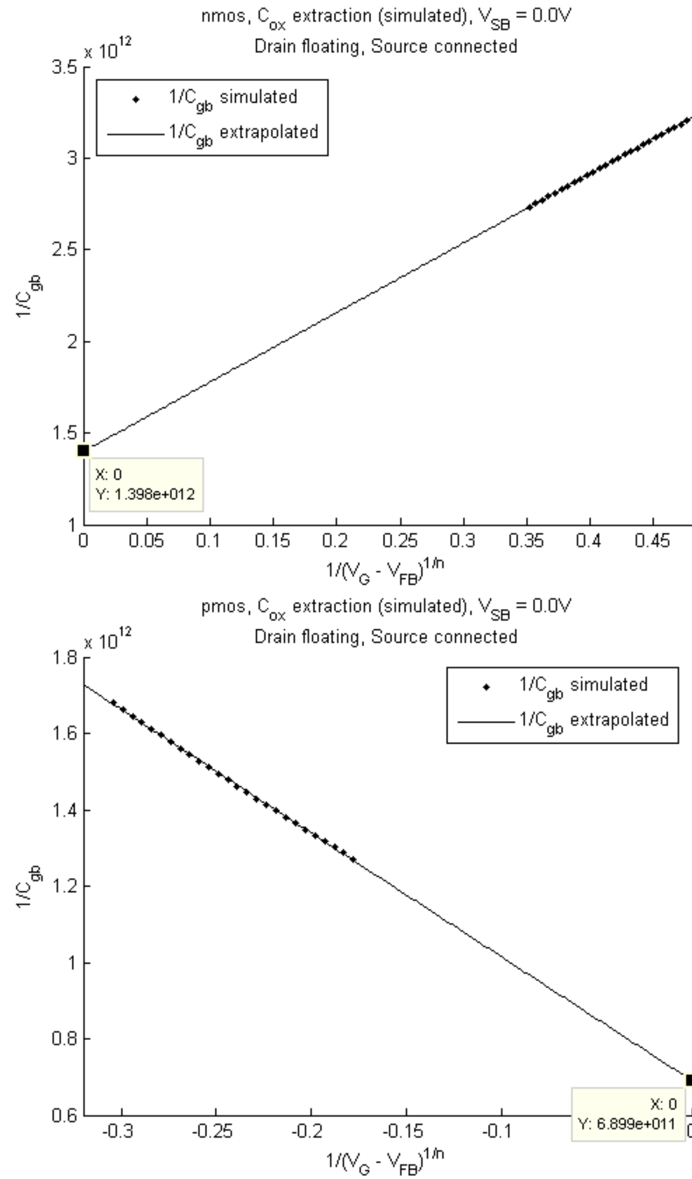

Figure 7.13: Extraction of C_{ox} from simulations.

Data from figures 7.3 and 7.4 was on beforehand adjusted to eliminate the additional on-die capacitances investigated earlier. It was also found necessary to plot $1/C_{gb}$ versus $(V_g - V_{FB})^{1/n}$ instead of $1/C_{gb}$ versus $\frac{1}{(V_G - V_{FB})^{1/n}}$, to shift the x-axis the correct way. The resulting plots after using this method on the C_{gb} data in depletion are shown in figures 7.12 and 7.13 for measurements and typical corner simulations respectively.

Device	$C_{gb_{max}}[F]$	$A_{tot}[\mu m^2]$	$C_{ox}[F/m^2]$	$t_{ox}[m]$
NMOS (measured)	7.733e-13	63.2	0.01224	2.8217e-9
NMOS (simulated TT)	7.153e-13	63.2	0.01132	3.0509e-9
PMOS (measured)	2.175e-12	125.0	0.01741	1.9843e-9
PMOS (simulated TT)	1.449e-12	125.0	0.01160	2.9778e-9

Table 7.3: Extraction of C_{ox} from measurements and typical simulations. NMOS and PMOS in unsaturated depletion region.

C_{gb} in figures 7.3 and 7.3 is the total C_{gb} for all NMOS and PMOS devices respectively. C_{ox} is therefore found by dividing the maximum capacitance C_{gb} found from the plots in figures 7.12 and 7.13 with the total gate area A_{tot} for each set of NMOS and PMOS devices. t_{ox} is then found by using equation 2.12. The extracted values are given in table 7.3. No specific trend can be read of of this table, but it is obvious that the extracted t_{ox} except for the measured PMOS is overestimated. Ideally t_{ox} extracted from the typical simulation corners should have been closer to 2nm.

7.5.2 Finding C_{ox} and t_{ox} from inversion region

C_{ox} may also be found from the inversion region, according to figures 2.11 and 2.13. This is because of the almost symmetrical course of C_{gg} in inversion and accumulation. Inversion region was therefore also investigated for finding C_{ox} for this 90nm technology. A problem that was assumed to complicate C_{ox} extraction from inversion region however was that caused by the so-called *polydepletion* effect. Poly-silicon is typically used as gate material for present CMOS technologies, as a replacement for true metal-gates used previously. A depletion layer is created in the polysilicon due to the minority carriers at the bulk-to-oxide interface in strong inversion. This depletion layer is seen to reduce the coupling between gate and channel and causes and additional voltage drop, which in turn decreases the total gate capacitance C_{gg} ([24] and [30, section III]). A plot showing the typical corner simulation of NMOS C_{gg} over a wide V_G for the 90nm technology is shown in figure 7.14. The use of a large V_G clearly shows the effect of polydepletion. It is seen that C_{gg} only partly returns to the maximum achievable capacitance at

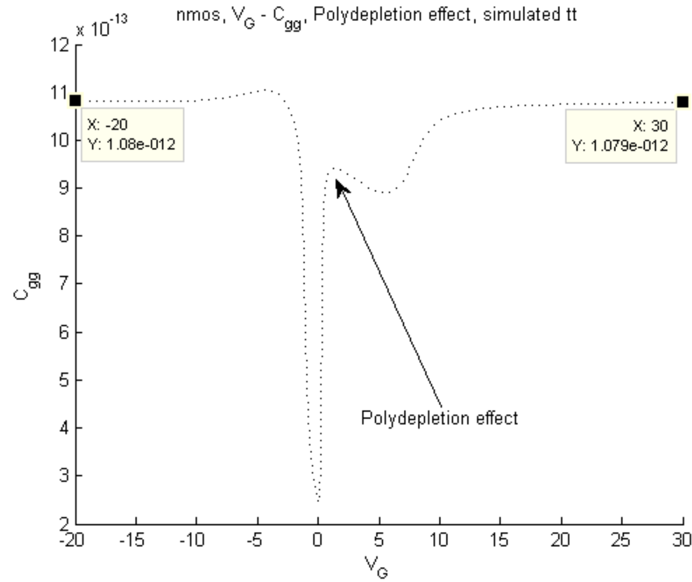

Figure 7.14: Simulated effect of polydepletion on total gate capacitance C_{gg} for NMOS transistors (all four sharing common gate).

$V_G \approx 1.0V$. This is the point at which the polydepletion effect occurs. When V_G is further increased to a critical value however, the device restores from polydepletion and C_{gg} eventually achieves approximately the same value as that seen in accumulation. The effect of polydepletion becomes more severe as the oxide thickness is decreased. This problem of polydepletion effect is amongst others described in [8, p. 106].

Devices	$C_{ox}[F/m^2]$ **Source connected**	$C_{ox}[F/m^2]$ **Drain0 connected**	$C_{ox}[F/m^2]$ **Drain1 connected**	$C_{ox}[F/m^2]$ **Drain2 connected**	$C_{ox}[F/m^2]$ **Drain3 connected**
NMOS (measured)	0.01570	0.01552	0.01587	0.01601	0.01567
NMOS (simulated TT)	0.01472	0.01472	0.01472	0.01472	0.01472
PMOS (measured)	0.01475	0.01466	0.01570	0.01467	0.01484
PMOS (simulated TT)	0.01399	0.01399	0.01399	0.01399	0.01399

Table 7.4: Extraction of C_{ox} from measurements and typical corner simulations. NMOS and PMOS in inversion region, with bulk floating and either drain or source connected.

Devices	$t_{ox}[m]$ **Source connected**	$t_{ox}[m]$ **Drain0 connected**	$t_{ox}[m]$ **Drain1 connected**	$t_{ox}[m]$ **Drain2 connected**	$t_{ox}[m]$ **Drain3 connected**
`NMOS (measured)`	2.1988e-9	2.2244e-9	2.1758e-9	2.1565e-9	2.2037e-9
`NMOS (simulated TT)`	2.3455e-9	2.3455e-9	2.3455e-9	2.3455e-9	2.3455e-9
`PMOS (measured)`	2.3407e-9	2.3548e-9	2.1988e-9	2.3497e-9	2.3269e-9
`PMOS (simulated TT)`	2.4679e-9	2.4679e-9	2.4679e-9	2.4679e-9	2.4679e-9

Table 7.5: Extraction of t_{ox} from measurements and typical corner simulations. NMOS and PMOS in inversion region, with bulk floating and either drain or source connected.

From this observation it is clear that it is not optimal to extract C_{ox} from inversion region within the maximum allowed voltage limit. However, it will still give an indication of the value. This has been achieved by reading out the maximum capacitance in strong inversion from the plots in figures 7.5 and 7.6, and dividing it with the total gate area. The results are given in table 7.4. t_{ox} has been calculated as well as shown in table 7.5.2, according to equation 2.12 in section 2.5.

Since it was not possible to estimate the additional on-die capacitance when measuring C_{gc}, the values of t_{ox} in table are in principle smaller than if it had been possible to take this capacitance increase into account. The impact from polydepletion on the other hand increases the t_{ox} values. The simulated effect of polydepletion is from figure 7.14 seen to represent a drop in C_{gc} of approximately 140fF for NMOS. Hence if the level of capacitance caused by other on-die structers is in the same order, the values of t_{ox} in table 7.5.2 can be thought of as quite representative for the maximum capacitance obtained after the device has restored from polydepletion.

7.6 Influence of body effect on V_{th}

Regardless of the deviation in V_{th} caused by the floating drain nodes, it is still possible to investigate the effect of body effect V_{SB}. This is achieved under the assumption that this deviation is constant for all measurements of C_{gb}. By using equation 2.3 from section 2.5 on the results in table 7.1, the body-effect coefficient γ is found. The results are given in table 7.6. The change from $V_{SB} = 0.0V$ to $V_{SB} = 0.2V$ for NMOS and from $V_{SB} = 0.0V$ to $V_{SB} = -0.2V$ for PMOS has been investigated. It has been seen that the simulated V_{th} increases almost linearly with the applied bulk voltage, which is according to the expectations from [25, section II] for small changes in V_{SB}. For the measurements this is true for PMOS as well, while the results

Device	$\gamma[V^{1/2}]$
NMOS (measured)	1.9371
NMOS (simulated TT)	2.1870
NMOS (simulated SS)	2.1424
NMOS (simulated FF)	2.0978
PMOS (measured)	-2.0264
PMOS (simulated TT)	-2.0085
PMOS (simulated SS)	-2.0531
PMOS (simulated FF)	-2.0085

Table 7.6: Extraction of body-effect coefficient γ from measurements and simulations.

for NMOS are not found to be perfectly linear. This is reflected in table 7.6, where it is seen that the value of γ is slightly lower than that found from simulations. Hence the measured V_{th} deviates more from the simulations but at the same time linear dependency on V_{SB} is quite good, while the opposite observations are true for NMOS.

7.7 Evaluation of methods

It is of importance to evaluate the accuracy of the methods used for extracting V_{FB}, C_{ox} and V_{th}. The first issue is that the accuracy of extracting C_{ox} is actually dependent on the accuracy obtained when extracting V_{FB}. Tests have shown that small variations in the extracted V_{FB} could lead to major deviations in C_{ox}. This is a direct consequence of the deep-submicron technology, where small voltage shifts have large impact on the mode of operation. This is especially seen in depletion, where the slope is quite high. It has been found that the choice of data points to be included as a reference for the extrapolation can have a great impact on the result. It is important to choose those points such that only the straight part at the very end of depletion is included. Also, the same data segment used when extracting V_{FB} should be used when extracting C_{ox}. It is obvious that different extrapolating methods will have a large impact on the resulting values extracted. In this chapter an automated linear extrapolating function from Matlab has been used. From the extracted values of t_{ox} it is obvious that there exists an inaccuracy. A $t_o x$ of approximately 2nm for both NMOS and PMOS technology was on beforehand expected, but it was seen that almost all devices

were overestimated.

By investigating the inversion region a more realistic value of t_{ox} was found for both measurements and simulations. The results from this method would have been greatly improved if a dummy-structure was available on the prototype dies. Then the progress of the slope toward maximum C_{gc} after polydepletion could have been predicted by comparing the measured data with simulations.

The results achieved from extracting V_{th} from C_{gb} was found to be suffering from the floating drain nodes. It was on beforehand assumed that it would be best to accomplish the CV characterization of the prototype dies more in a technology perspective rather than a device-specific perspective. Thus only source was connected to external DC bias, to ensure that the devices obtained the supply of minority carriers when entering inversion. Because of this the drain nodes were left floating when measuring C_{gb}, which must have created a non-zero V_{DS}. A better solution would be to measure V_{th} for each transistor with the drain nodes successively connected to external DC bias. One challenge with this is that it would require a new orientation of the probes relative to the test pads than that used when drain was floating.

7.8 Future improvements for test-structure layout of 90nm prototype dies regarding AC measurements

The layout of the 90nm prototype dies was fixed at the time of start-up, and was therefore not possible to change. After accomplishing CV characterization, some experience have been gained regarding the optimal layout for such measurements.

The first important improvement would be to create a dummy-structure, consisting of the exactly same test-structure as that for the DUT except from the DUT itself. In this way any additional on-die parasitic capacitances associated with the test pads and interconnect routing could have been measured, and hence subtracted from the measurement results. It has been seen through the presentation of the results from CV characterization that the lack of this dummy-structure made it necessary to estimate an approximate value for this capacitance, and also to neglect the effect of it in some cases. By combining an accurate subtraction of this capacitance with a four-probe method, it should be possible to achieve very exact results.

The second improvement comes in conjunction with how to actually carry out the practical measurements. This in relation with the layout of the test structure. Much of the literature describe only the measurement setup for two-terminal devices, but through this report a review of the measurement

on four-terminal devices has been given. [13] recommended to make a MOS-C out of the MOSFET already at the layout stage to obtain a two-terminal device, by connecting together drain, source and bulk as one common node. But this would however restrict the measurements available to that of being capable of measuring C_{gg} only.

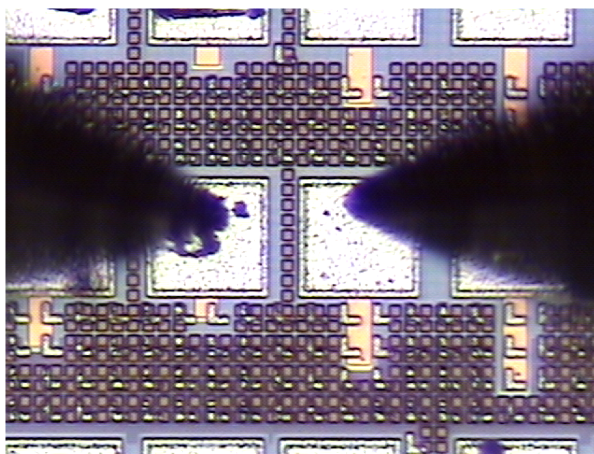

Figure 7.15: Probe size relative to size of micro pad.

A better solution in a technology characterization perspective would be to have a total of one large MOSFET device with separate drain, source, gate and bulk connections. The reason for making this device large is to increase the level of capacitance to be measured, hence reducing the impact from additional parasitics and alternatively small-channel effects. One such transistor would sufficient for characterizing most parts of a specific technology. The main drawback is that it is not so usable for re-use in other types of tests as was the case for the 90nm prototype dies used in this project. By having the common gate, bulk and source nodes and separate drain nodes, this layout was very suitable for the IV measurements. But when accomplishing CV measurements, the arrangement of the probes in the probe station became more fixed due to the system setup. That is, since only two of the probes were coaxial, they had to be connected to the impedance meter. This left the two additional probes in a fixed positioning. Thus if the coaxial probes connected to the impedance meter were positioned along an x-axis, the ordinary probes available for DC bias purposes had to be positioned along a y-axis with the default setup of the probe station. This limited the possible placement of the probes relative to each other, which is complicated additionally by the size of the probes relative to the pad size as seen in figure 7.15. By however only having a total of four pads, laid out according to the setup of the probe station, this would simplify the CV measurements. For reducing the challenges associated with one probe getting in the way for

other probes and also for reducing the possibility of pad damage, it would be advantageous to increase the pad size provided that there is enough space on the die layout.

For being able to measure capacitances where more than one node is connected to either HI or LO of the impedance meter, a specific test structure must be created already at the layout stage as already mentioned. Another method would be to achieve this connection internally in the probe station by using very short SSMC-to-SSMC cables between these three probes in a daisy-chain configuration. The reason for why this is possible is that each probe has a total of two connection screws on top, which are linked together internally in the probe body. By using one of these three configurations it would be possible to measure any capacitance of interest. It is however reasonable to assume that this connection would worsen the accuracy obtained from fixture compensation.

Chapter 8

Conclusion

In this master thesis IV and CV characterization for 90nm transistors on recently fabricated prototype dies have been accomplished and investigated. This was achieved by using a new probe station and instrumentation, capable of measuring current and capacitance in the low fA and fF respectively.

A total of four nmos and four pmos devices were studied by IV measurements. The IV characterization results were for the majority of the devices found to reside within the simulation corners. There was however a prominent tendency for the measurements of slewing towards the slow corners, thus a reduced maximum drain current was obtained for the devices. Repetition of the same tests over various dies proved that the contact condition between probe and micro pad had an influence on this issue. Some devices were however actually outside the slow corners at all time.

From the IV measurements the impact from leakage currents was also investigated. For a reverse-biased device it was found that the gate leakage I_G in general was close to or even at the same level as that of the drain-to-source leakage current I_{sub}. The static power consumption is thus increasing with decreasing technology dimensions. It was also seen that DIBL mostly affected the initial I_{sub} for the reverse-biased devices, but not so much the slope of I_{sub} towards the threshold voltage of the devices.

Before being able to conduct CV measurements, a study of theory and methods appropriate for ultra-thin oxide devices was necessary. This resulted in a general measurement methodology for CV measurements of deep-submicron technologies. Such technologies were in general found to require high test signal frequencies and more extensive capacitance-equivalent circuits to obtain good results. By combining this methodology with the state of the art instrumentation available, it was possible to achieve accurate capacitance measurements in the low fF-range.

When accomplishing CV characterization, the focus was put on the tech-

nology itself rather than at device-specific investigations. The total C_{gb} and C_{gc} was measured to obtain the almost symmetrical C_{gg}. From this various methods found in the literature for extracting V_{FB}, C_{ox} and V_{th} were presented and applied on the results. It was seen that the methods based on extrapolation of the unsaturated depletion region clearly suffered from the somewhat rough estimations that were used. The method that investigated inversion region for extracting C_{ox} was found more accurate, but complicated by the effect of polydepletion. Finally the extraction of threshold voltage was influence by using a three-probe method instead of a four-probe method, which resulted in a V_{th} occurring earlier than expected. The three-probe method was used under the assumption that the connection of drain to the COMMON level would not make any difference, since at least the source node provided for the external supply of minority carriers at V_{th}. This setup proved however not to be ideal.

Although the methods used for extraction from the CV measurements resulted in deviation from the expected values, they represent methods that are common in literature at present time. This is because these deviations were more caused by the practical accomplishment of the measurements used, rather than the methods used. For fully utilization of the CV results a dummy structure should have been available, such that the measurements can be adjusted according to a known capacitance level represented by the additional on-die parasitics. This would ease the extraction of process parameters for the technology, and can be part of a future test layout.

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Appendix A

List of equipment

Unit	**Type/data**	**Manufacturer**	**Laboratory-nr. (serial nr.) [product nr.]**
Probe station, manually operated, 8", with MicroChamber	SUMMIT 11561B	Cascade Microtech	(358940308)
DC Analyzer	SCS-4200	Keithley	-
ThermoChuck	TPO3200A-2300-2	Temptronic	(04050316)
Gas dryer	SA139591	Temptronic	-
Precision Impedance Analyzer	4294A 40Hz-110MHz	Agilent	HJ-3006
Microscope	A-Zoom2, 10X	Thales Optem Inc.	-
Illuminator	LampLink2, with digital controller	Thales Optem Inc.	-
Pneumatic Vibration Isolation System	1VIS95	Standa	-
1 meter BNC to SSMC cable, 4TP (for CV measurements	-	Cascade Microtech	[105-540]
Impedance Substrate Standard (ISS)	S/N 106-683A	Cascade Microtech	832271 899058
DCP to DCP Guard connection strap	-	Cascade Microtech	[123-625]
DCP 100 series (coaxial probes)	50Ω SSMC connection	Cascade Microtech	-
DCP-HTR series (conventional DC probes)	50Ω SSMC connection	Cascade Microtech	-

Table A.1: List of equipment

Appendix B

Reference guide for basic CV measurements with the Agilent 4294A

This reference guide explains how to achieve basic CV measurement by manually operating the 4294A through the front panel. For using the 4294A in co-operation with the Keithley 4200-SCS through GPIB to obtain a four-probe configuration, see the "4200-SCS Semiconductor Characterization System: Reference Manual, Keithley" chapter 8 and appendix M.

Options not discussed in this summary may be left unaltered. It is not necessary to exactly follow the same order. Some exceptions are however pointed out.

1. Turn on the Agilent 4294A. Warm-up time for instrument before compensation or measurements is minimum 30 minutes.

2. Set up the probe station from Cascade in such a way that it is ready for CV-measurements

Notice first that among three different wafer connection methods available with the Cascade probe station, the 4TP method is chosen. Notice second that the 4294A utilizes the Auto-Balancing Bridge Method for accomplishing measurements. Notice third that the applied stimuli in this guide will be DC bias voltage, not current. The necessary setup is as follows:

- Unscrew the originally placed blue Triax-based wires (inside the top-hat) from the two coaxial probe-tips that support BNC-connections (which are those two with the visually longest probe tips / not enclosed within a white ceramic).
- Connect the BNC-to-SSMC 4TP coaxial cables between the 4294A and the two coaxial probes inside the probe station, in the following way: Connect each of the four BNC-to-SSMC cables to the 4294A instrument through the BNC connectors. Then the two screws on the first probe must to be connected to the two LOW-wires (Lpot, Lcurr), while the screws on the second probe must be connected to the two HIGH-wires ((Hpot, Hcurr). It does not matter which of the two screws that goes to which LOW- / HIGH-wire. In practice, this creates a shortcircuit between Lpot and Lcurr withing the probe, and a shortcircuit between Hpot and Hcurr within the second probe. The outer shielding of each of these four coaxial cables becomes connected to the bulk of the coaxial probes, which stretches almost to the tip of these probes.
- Connect the short, black strap between the screws situated nearest the probe tips. This is to minimize the ground return path.

- Now a set of HIGH- and a LOW-terminal pair to the impedance-analyzer has been created. The bias stimuli (AC and DC) is applied through the Hcurr terminal. Voltage measurement is performed between the Hpot and Lpot terminals, while current measurement is performed through the Lcurr terminal. The chuck is electrically floating, such that the test signal applied by the HI node is not driven towards ground. Make sure that the BNC-to-SSMC cables are not twisted, and do not change their positions during or between measurements and calibration. The HIGH terminal is to be connected to the electrode that shall receive the sweeping stimuli (DClevel+ACsignal), while the LOW terminal (virtual, enforced ground) is to be connected to the electrode that shall function as the ground reference for the stimuli.

3. Insert the DUT (die or wafer) on the main chuck.

4. Insert the ISS (Impedance Standard Substrate) into the probing station (in advance equipped with AttoGuard plate for precise measurements), in the upper or lower right corner of the wafer chuck. This is a dedicated place for the ISS (called auxiliary chuck), which is not exposed to the heating and cooling forced by the user during temperature sweeps through the TermoChuck system from Temptronic. Compensation performed at various temperatures is not desirable, since this would disturb the result depending on the applied temperature. So if this thermally isolated placement was not available, it would be necessary to wait for the chuck to cool down / heat up to room temperature before each compensation – which would take a lot of time. The ISS will be situated in this place of the wafer chuck during the whole period of measurements. I.e. it is not supposed to be removed after the first compensation is performed, since several compensations will be required later between measurements as well. Cascade Microtech recommends the 106-683 ISS for the DCP coaxial probes that the probe station at the time being is equipped with.

5. Adjust (and almost land) the probes on the pads according the device (DUT) to be measured, then lift the probes again. Keep these probe positions through the rest of this manual / measurements, and never change the position of the two probes relative to each other again except from in the z-direction. For adjustment of the probes relative to the DUT or ISS

in the future, use therefore the chuck rotators (which move the chuck), and NOT the x- or y-positioners (which move the probes)

The reason for this is to keep the measurement conditions the same over the whole test period, such that the compensation (explained later in this note) is not disturbed by changing the relative probe positions after compensation has performed. In this way, the ISS in the compensation procedure is measured with the same preconditions as the measurement of the DUT itself.

6. Make sure that adapter settings has been set up correctly:

   [Cal] → [Adapter] → [4TP 1M]

The points used for compensation should be those stored in the instrument, and not points specified by the user:

   [Cal] → [Comp point] → [Fixed]

Notice that if the “Adapter” or “Comp point” at any time is changed, previous compensation is destroyed and must be done all over again.

7. Select active trace

   [A] (Selects trace A)

   [B] (Selects trace B)

Only the following settings are valid for the active trace only:

   [Format]

   [Display] → [Def trace]

   [Display] → [Offset]

   [Display] → [more ½] → [Title]

   [Scale ref]

   Keys in the MARKER block

8. It is possible to split the display into two sections, showing both active and inactive trace

   [Display] → [Split]

In this way, if e.g. measurement parameters C_P – Q and sweep parameter frequency f is chosen, the upper plot will show frequency f (x-axis) versus C_P (y-axis) while the lower plot will show frequency f (x-axis) versus Q (y-axis).

9. Give a title to the active trace if desirable. This title will be shown continually on the screen.

[Display] → [more ½] → [Title]

10. Choose desired measurement parameters (i.e. on y-axis)
The instrument have the following built-in two-parameter equivalent circuits relevant for CV measurements:

- A capacitance in parallel (C_P) with a conductor
- A capacitance in series (C_S) with a resistance

[Meas] → [|Z|-θ] or [R-X] or [L_S-R_S] or [L_S-Q] or [C_S-R_S] or [C_S-Q] or [C_S-D]
or [|Y|- θ] or [G-B] or [L_P-G] or [L_P-Q] or [C_P-G] or [C_P-Q] or [C_P-D]
or [COMPLEX Z-Y] or [|Z|-L_S] or [|Z|-C_S] or [|Z|-L_P] or [|Z|-C_P]
or [OTHER] → [|Z|-R_S] or [|Z|-Q] or [|Z|-D] or [L_P-R_P] or [C_P-R_P]

If e.g. C_P-R_P is chosen, C_P will be placed in trace A and R_P in trace B. The plot to be shown on the display can be toggled with the buttons [A] and [B].

Choice of measurement parameters are however not so important if the complex impedance Z is saved. Then any parameter of interest can be extracted manually afterwards with another tool than the 4294A.

11. Choose desired sweep-parameter (i.e. on x-axis)

[Sweep] → [Parameter]

→ [FREQ]
(fixed oscillator voltage level, fixed DC bias, oscillator frequency sweep)
[OSC LEVEL]
(fixed frequency, fixed DC bias, oscillator voltage level sweep)
[DC BIAS]
(fixed frequency, fixed oscillator level, DC bias sweep (voltage or current))

Frequency-sweep: e.g. 40Hz (minimum) to 110MHz (maximum)
Oscillator voltage level sweep: e.g. 5mV (minimum) to 1V (maximum)
DC bias level: e.g. -40V (minimum) to 40V (maximum)

Remember to state the desirable unit for the sweep-parameter (current or voltage)

12. Set up the sweep range for the selected sweep parameter (selected in stage 11)

[Start] → Adjust with knob or numeric keypad for start value
[Stop] → Adjust with knob or numeric keypad for stop value

These values are used for both traces.

13. Set the number of points for the x-axis (i.e. the resolution of the sweep parameter)

[Sweep] → [Number of points] → Number between 2 and 801

14. Select sweep direction

[Sweep] → [Direction]

It is advantageous to sweep MOSFETs from inversion region toward accumulation region.

15. Set up options for the fixed parameters (i.e. those not chosen as sweep parameter):

[Source] →

[Bias Menu] →

[Mode] → Select between voltage, current, constant voltage, constant current.

[Meas range] → Sets the accuracy of the current delivered to DUT, hence sets the accuracy for the impedance measurement. Set this initially to 1mA, and continue to use this as long as the error message "DCBIAS OVERLOAD" is not shown after DC bias is turned on.

[Voltage level] → Set level of DC voltage bias (applies if DC bias has NOT been chosen as sweep parameter, and voltage is chosen as DC bias unit)

[Current level] → Set the level of DC current bias (applies if DC bias has NOT been chosen as sweep parameter, and current is Chosen as DC bias unit)

[Max limit voltage], [Min limit voltage] → sets the maximum and minimum DC voltage. These limits take effect when constant voltage or constant current is chosen (to protect the DUT), otherwise these values are discarded.

[Bias ON/off] → turns dc Bias on/off → USED TO ACTIVATE DC BIAS

[Osc Menu] →

[Frequency] → Sets the frequency of the oscillator (applies if oscillator Frequency has NOT been chosen as sweep parameter)

[Level] → Sets the amplitude level of the sinusoidal oscillator signal (applies independent of which parameter has been chosen as sweep parameter)

[Osc unit] → Choose whether the sinusoidal oscillator signal is to be a voltage or a current (applies independent of which parameter has been chosen as sweep parameter)

The setup for the sweep parameter (stage 11) overrides the setup for the sweep parameter in the [Source] menu.

When performing the SHORT fixture compensation explained later, the oscillator level should be lowered temporarily to below 500mV (if a larger value is intended to be used in the measurements). If not, the 4294A may indicate the errors “REDUCE OSCILLATOR LEVEL” or “BRIDGE UNBALANCED”. See Operation Manual (page 151) for further information.

16. Select which method is intended to start (trigger) the measurement:

[Trigger] → [Continuous] This is the default option. By choosing continuous, the measurement is repeated over and over again an unlimited number of times, without any external triggering mechanism.

17. Set up measurement accuracy, stability and time:

[Bw/Avg] →

Set up the precision of the measurement (1=fast, 5=precise)
[Bandwidth] → [5]

Define the data measured during the continuous sweeps to be averaged
[Averaging] → [ON]

Set up the factor of the averaging (i.e. how many of the latest sweeps which are to be taken into account when performing the averaging)
[Averaging factor] → desired number

“Point averaging” may be used to take a number of measurements at a given point of the sweep parameter during each sweep, and then make an average measurement value based on all of these measurements (not necessary initially, but may be explored afterwards):

[Point avg] → choose whether this functionality is to be used or not
[Point avg factor] → choose the number of measurements per point

The use of point averaging is must be considered in relation with the use of sweep averaging.

18. Calibration and compensation consists of adapter compensation, fixture compensation, user calibration, port extension compensation. Refer to the Impedance Measurement Handbook for the difference between calibration and compensation. Compensation is accomplished by using the ISS.

REMEMBER TO TURN OFF ANY DC BIAS (STAGE 15) BEFORE PERFORMING COMPENSATION / CALIBRATION. THIS IS ESPECIALLY IMPORTANT WHEN THE SHORT COMPENSATION IS PERFORMED – OTHERWISE THE PROBES MAY BE DAMAGED DUE TO THE EXTENSIVE SHORT-CIRCUIT CURRENT.

Adapter compensation
In theory already accomplished and stored by the user who first used a specific adapter. Besides, this is not necessary for the simple 1-meter direct BNC-to-SSMC coaxial cables with the 4TP configuration since this itself is not a adapter from Agilent (would on the other hand be necessary with the 16048G and 16048H adapters).

User calibration
Not required for the 1-m 4TP configuration (cannot be performed)

Port extension compensation
Not required for the 1-m 4TP configuration (cannot be performed)

Fixture compensation (essential!)
Fixture compensation should be accomplished if a new test sequence is to be taken, if the spacing between probes is changed, if cables between 4294A and probes has been disturbed, or if any other setup is changed. This is achieved by using the Short-Open-Load (SOL) compensation technique.

The Open-Short (not Load) technique should be sufficient for standard measurements where the standard 1 meter 4TP cables approved by Agilent is the only extension between the 4294A and the DUT. For more complex test setups (see Impedance Measurement Handbook, chapter 4-2-4) the Open-Short-Load is necessary. In this note the complete Short-Open-Load technique will be examined for completeness, for then to finally verify that the Load compensation is not necessary for most basic setups.

Since the ISS is not light sensitive, it is not necessary to turn off the microscope lights when compensation is performed. The temperature from the lamp will however increase the temperature within the microchamber of the probe-station.

When landing the probes on the ISS, it is sufficient to just slightly hit the test structure to get a good contact.

Before each compensation procedure, the following settings must be applied. This is because some of the instrument settings also affect the precision of the compensation:

- set averaging ON, with high precision ([Bandwidth] = 5). This is really important. Otherwise the checking at the various fixed frequency points will be accomplished too fast, resulting in an imprecise compensation.
- use a high test signal level to increase measurement accuracy (e.g. 500mV)
- choose frequency as the sweep parameter, and a split-window with |Z| and C_P or C_S (not actually necessary to obtaining the required precision, but for verification purposes explained below)
- the choice of test signal frequency does not matter, since the compensation procedure itself is accomplished at specific fixed frequency points

Make sure that the compensation procedure measures at fixed frequency points (i.e. it will check a whole series of frequencies, and then interpolate between them), as should already have been accomplished in stage 6. This means that after compensation is fulfilled, the test signal frequency can be changed to any value of desire without destroying the compensation.

[Cal] → [Comp point] → [Fixed]

Each fixture compensation should be initiated by a phase compensation. Phase compensation must be accomplished with the probes in open-state (i.e. lifted up from the ISS)

[Cal] → [Adapter] → [Setup] → [Phase Comp]

Remember to apply this new phase compensation by pressing [Done] after the phase compensation has finished.
("Load comp" indicated in the same menu as "Phase comp" is not necessary, since this will be accomplished as part of the fixture compensation procedure described below.)

Then the fixture compensation itself continues as follows.

Open compensation

Keep probe tips lifted from the ISS
[Fixture comp] → [OPEN]
Wait until compensation is done (indicated by the uppermost "OPEN ON off" changing colour from blue to white and going from "OFF" to "ON")

Verify afterwards that a valid compensation has been performed, indicated by $|Z| \approx$ MΩ-range (i.e. ∞ Ω)

Short compensation

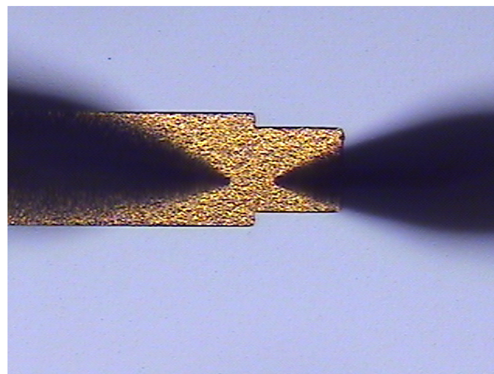

Figure B. 1 Short-structure on ISS

Land probe tips on a proper shorting-strip on the ISS (by using chuck rotators)
[Fixture comp] → [SHORT]
Wait until compensation is done (indicated by the uppermost “SHORT ON off” changing colour from blue to white and going from “OFF” to “ON”)

Verify afterwards the connection between the shorting-strip and probes, indicated by |Z| ≈ Ω-range (i.e. 0 Ω)

Load compensation

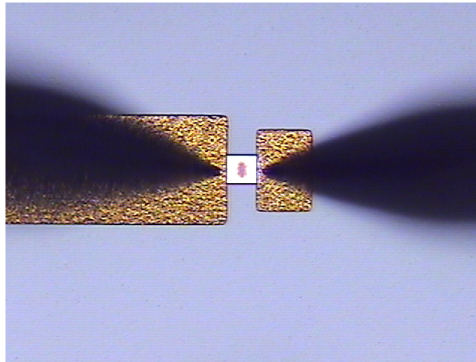

Figure B. 2 50Ohm load-structure on ISS

Land probe tips on a proper load-strip on the ISS (by using chuck rotators)
[Fixture comp] → [LOAD]
Wait until compensation is done (indicated by the uppermost “LOAD ON off” changing colour from blue to white and going from “OFF” to “ON”)

Verify afterwards the connection between the load-strip and probes, indicated by |Z| ≈ 50 Ω

As a final practical test of general measurement compliance, the ISS holds some various reference capacitors which may be measured after compensation (60fF, 440fF, 860fF).

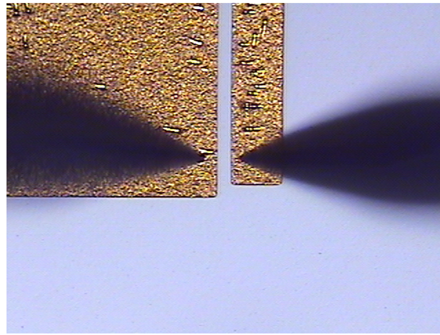

Figure B. 3 60fF reference capacitor on ISS

The capacitor structure next to the shorting- and load-strip is a 60fF reference capacitor. According to Cascade Microtech this should be measured to approximately 63fF over the whole frequency axis.

Follow this procedure to obtain this value:

1) Land the probes on the capacitor structure.
2) Check to see if a value close to 63fF is obtained over the whole frequency-range (x-axis).
3) If the capacitance values at the various frequency points are not close to 63fF at all, turn off the load compensation
4) Check again to see if a value close to 63fF is obtained.
5) If still not close, perform the compensation procedure all over again.
6) There may be some variations in the capacitance value at the various frequency points. It has been experienced that the measured value is slightly higher at frequencies above 80MHz, making these high-frequency values less useful for measurements. See to that at least the value at the frequency planned to be used is close to the ideal 63fF.
7) Compensation is now complete. Change the sweep parameter, AC test signal level, AC test signal frequency and measurement precision back to that required for performing measurements.

19. After compensation is complete, move the probes away from the ISS and land them on the DUT instead.

20. Axis format for the x-axis (the sweep parameter)

[Sweep] → [Type] → linear or logarithmic

Note that the use of logarithmic scale is only applicable for frequency sweep

21. Axis format for the y-axis (the measured parameter)

[Format] → [Lin] or [Log]

Remember on beforehand to select active trace for which the axis format is to be changed.

22. Set up the display of measurement results:

Turn off the inactive trace, such that the display only displays the active trace of interest. This functionality is useful as long as it is not necessary to have a split screen showing both traces at the same time.
[Display] → [Hide inactive ON]

Turn the monitoring of enforced, real-time dc bias level (current or voltage) on. Shown in the lower part of the screen as “VDC”
[Display] → [Bias mon] → [Current] or [Voltage]

Turn the monitoring of enforced, real-time test signal (i.e. oscillator) voltage/current on). This is useful, since the actual signal level applied to DUT may differ from the applied signal level because of electrical loss between each test terminal and the DUT. Shown in the lower part of the screen as “VAC” and “IAC”.
[Display] → [Osc mon] → On

The [Display] menu also has some additional functionality such as OFFSET, EQUIV CIRCUIT, DISPLAY ALLOCATION, MODIFY COLOR. See the operation manual.

Parameters set up through the [Display] menu does not in any way change the data stored, only the visualization of the data on the 4294A monitor.

23. Set up the scale for the y-axis:
Choose the start and stop points for the y-axis, according to the results expected from measurements:

[Scale ref]

→ [Top value] → Knob / numeric keypad

→ [Bottom value] → Knob / numeric keypad

Alternatively the auto-scale functionality may be used for the y-axis

[Scale ref] → [Auto scale]

24. **THIS POINT SHOULD BE THE LAST POINT BEFORE DEFINING MEASURED DATA AS VALID DATA:**
Notice that the instrument starts the measurements immediately after the measurement type and sweep parameter (stage 4,5,6,7 etc.) is set, since the trigger-mechanism is set to "continuous". This means that the measurements taken so far consists of an average value found from measurements taken both before and after compensation, hence the output is not representative. To start measurements from scratch, push

[Bw/Avg] → [Averaging restart]

New output will now be valid after some time (necessary to find the new average values, based on several measurements).

Remember that DC bias must on beforehand have been turned ON (stage 15), for actually accomplishing the measurements.

25. Use the “Marker” section on the instrument to inspect the curves on the screen.

26. Many data types may be saved (3.5” floppy-disk) (se Operator Manual chapter 8)

[Save]

→ [State] (binary)

→ [Data] (ascii, binary) (NB! Remember to specify on beforehand the data to be included.)

→ [Graphics] (tiff)

→ [Touchstone] (.s1p)

Data is not saved before the [Done]-button is pushed (after specifying a name for the file).

27. Hopefully the unlimited repeat of sweeps will result in a distinct, averaged result. It may however in some cases be of interest to at some point stop the continuous sweep

[Trigger] → [Hold]

Note that no further sweeping can be triggered after it has been stopped (a completely new measurement sweep must be initiated).

28. If the Agilent 4294A instrument is turned off, it will go back to default state (applies to all input parameters, such as measurement type, stimulus, sweep range etc.)

For resetting the 4294A to default state when the instrument is already turned on (useful for accomplishing reset without having to turn it off and then on again):

[Preset] (green button)

References:

Operation manual, Agilent 4294A

Impedance Measurement Handbook, Agilent Technologies, December 2003

Configuring a Precision System for On-Wafer Capacitance, Application Note CVMOS-APP-0103, Cascade Microtech

CV Measurement And Calibration Techniques, Franz Sischka

ADDITIONAL NOTES ON THE USE OF FOUR-TERMINAL PAIR (4TP):

- The four-terminal pair (4TP) method consists of splitting a differential pair into 4 dedicated coax-lines out, to separate the bias lines from the sense lines. Each line (voltage_low, voltage_high, current_low, current_high) has its own dedicated shielding, to minimize sensitivity for external noise and also to reduce the radiation to the outside. If the short-circuiting of Hcurr-Lpot or Lcurr-Lpot is done very far away from the DUT, the connection becomes a 2TP (two-terminal pair) instead (destroying the good properties of the 4TP).
- Agilent 16048G is a 4TP adapter with a 1m long cable.
- Agilent 16048H is a 4TP adapter with a 2m long cable.
- Finally there is the 4TP method reviewed in this note, consisting of four single BNC-to-SSMC coax-cables with no adapter, also produced by Agilent. This is preferred since it avoids the necessity of converting from coax (4TP) to triax (probe-station), which would introduce additional error. Instead these single coax-cables are connected directly to the Cascade dual-input coaxial DCP-probes in the probe station (2 coax-cables per probe).
- If a 4TP cable which includes an adapter is to be used, it is necessary to perform a so-called “adapter compensation” (which for the 16048G/16048H includes load and phase compensation). The 100Ω resistor from Agilent (04294-61001) is used as the load in this compensation procedure. Since this is only a one-time necessity for each adapter type, it is usually executed as the 4294A impedance analyzer itself is installed.
- If only the 4TP coax cables without the adapter is to be used, no adapter compensation is required (only phase and fixture compensation).

ADDITIONAL NOTES FROM THE "IMPEDANCE MEASUREMENT HANDBOOK":

- When performing measurements on devices with more than two electrodes (like the MOSFET), it is important to cancel out the effects of additional parasitic capacitances / stray capacitances (referenced to ground) associated by the remaining electrodes which are not connected to the two coaxial probes. In this way only the intended capacitance measured, without the influence of additional capacitances. This is achieved by connecting the remaining node(s) to the outer shielding of the coaxial cables (i.e. the bulk of the coax probes). The described method is important when measuring high impedance (i.e. low capacitance)
- The oscillator level should be low when measuring semiconductor devices.
- The actual applied oscillator level and DC bias level may not be exactly the same as the operator of the Agilent 4294A has setup the instrument to apply, due to the inherent properties of the "Auto-balancing bridge method". In general this must be taken into consideration when measuring high capacitances for AC signal level, and when measuring low resistivity semiconductor for DC bias level (causing a slight measurement error).
- The capability of providing high DC bias currents is limited for the Agilent 4294A. When high currents are necessary, an external DC current bias instrument must be used.

ADDITIONAL NOTE ON COMPENSATION:

The compensation performed by Agilent 4294A on the basis of data measured through the Short-Open-Load compensation technique make use of three equivalent circuit models (for short, open and load) to model the physical setup. These use some default values for the various circuit components in the equivalent circuits (resistor, capacitor, inductor). To summarize, the resistor for the load compensation is 50Ω while all other components have values equal to zero. If so-called ACP-probes (RF-probes) are to be used, the default values must be changed to new values indicated on the box that these probes are shipped in. A demonstration can be found on this site:
http://www.cascademicrotech.com/index.cfm/fuseaction/pg.view/pID/1170

These values can be set by pressing:

[Cal] → [Fixture compen] → [Define value] → open conduct / open cap
short resist / short induct

Do however NOT change these values if standard DCP-probes (i.e. ordinary coaxial probes) are to be used.
See operation manual page 153-154 for more information.

Appendix C

Eldo simulation files

C.1 IV simulations

C.1.1 IV simulations for nmos devices

```
IV CHARACTERISTICS FOR NMOS

.option nowarn=902 !Turn off warning "Model␣parameter␣ignored"
.option aex !Allow for saving extracted values to file
.option noascii !Turn off ascii-based plotting of results in .chi-file
.option jwdb !Create .wdb output
.option nocou !Do not create .cou output
.probe v
.temp 27.0000

.lib /dak/90nm_40b1_eldo/cmos090_tt.mod
*.lib /dak/90nm_40b1_eldo/cmos090_stat.mod
*.lib /dak/90nm_40b1_eldo/cmos090_ff.mod
*.lib /dak/90nm_40b1_eldo/cmos090_ffa.mod
*.lib /dak/90nm_40b1_eldo/cmos090_fs.mod
*.lib /dak/90nm_40b1_eldo/cmos090_fsa.mod
*.lib /dak/90nm_40b1_eldo/cmos090_sf.mod
*.lib /dak/90nm_40b1_eldo/cmos090_sfa.mod
*.lib /dak/90nm_40b1_eldo/cmos090_ss.mod
*.lib /dak/90nm_40b1_eldo/cmos090_ssa.mod



*nmos0 l=0.1 w=1.2
*nmos1 l=0.2 w=1.0
*nmos2 l=0.5 w=4.0
*nmos3 l=1.0 w=4.0


xnmos0 vd_n vg_n vs_n vb_n nsvt_leak       l=0.1 w=1.2 nfing=1 mult=10
xnmos1 vd_float1 vg_n vs_n vb_n nsvt_leak l=0.2 w=1.0 nfing=1 mult=10
xnmos2 vd_float2 vg_n vs_n vb_n nsvt_leak l=0.5 w=4.0 nfing=1 mult=10
xnmos3 vd_float3 vg_n vs_n vb_n nsvt_leak l=1.0 w=4.0 nfing=1 mult=10



vd vd_n 0 dc 1.0
vs vs_n 0 dc 0
vg vg_n 0 dc 1.0
vb vb_n 0 dc 0

.step vb 0 -0.2 -0.1
.step vd 0 1.0 0.05
.dc vg -1.0 1.0 0.05
.plot id(xnmos0.m1)
.plot ib(xnmos0.m1)

*NOTICE: this 90nm model is of level bsim3, hence the gate leakage calculation
*is based on a .subckt --> ig-extraction can not be accomplished as a part of
```

```
*the M1 MOSFET parameters. Instead an amperemeter must be used.
*.plot ig(xnmos0.m1)

.plot i(vg)
.plot gm(xnmos0.m1)
.plot gds(xnmos0.m1)


.extract label=vg file=extracts.txt vg(xnmos0.m1)
.extract label=vd file=extracts.txt vd(xnmos0.m1)
.extract label=vs file=extracts.txt vs(xnmos0.m1)
.extract label=vb file=extracts.txt vb(xnmos0.m1)

.extract label=vth file=extracts.txt vt(xnmos0.m1)
.extract label=gm_max file=extracts.txt max(gm(xnmos0.m1))
.extract label=gm_min file=extracts.txt min(gm(xnmos0.m1))
.extract label=gds_max file=extracts.txt max(gds(xnmos0.m1))
.extract label=gds_min file=extracts.txt min(gds(xnmos0.m1))
*.extract label=ig file=extracts.txt ig(xnmos0.m1)


.end
```

C.1.2 IV simulations for pmos devices

```
IV CHARACTERISTICS FOR PMOS

.option nowarn=902 !Turn off warning "Model␣parameter␣ignored"
.option aex !Allow for saving extracted values to file
.option noascii !Turn off ascii-based plotting of results in .chi-file
.option jwdb !Create .wdb output
.option nocou !Do not create .cou output
.probe v
.temp 27.0000

.lib /dak/90nm_40b1_eldo/cmos090_tt.mod
*.lib /dak/90nm_40b1_eldo/cmos090_stat.mod
*.lib /dak/90nm_40b1_eldo/cmos090_ff.mod
*.lib /dak/90nm_40b1_eldo/cmos090_ffa.mod
*.lib /dak/90nm_40b1_eldo/cmos090_fs.mod
*.lib /dak/90nm_40b1_eldo/cmos090_fsa.mod
*.lib /dak/90nm_40b1_eldo/cmos090_sf.mod
*.lib /dak/90nm_40b1_eldo/cmos090_sfa.mod
*.lib /dak/90nm_40b1_eldo/cmos090_ss.mod
*.lib /dak/90nm_40b1_eldo/cmos090_ssa.mod



*pmos0 l=0.1 w=3.0
*pmos1 l=0.2 w=1.0
*pmos2 l=0.5 w=8.0
*pmos3 l=1.0 w=8.0


xpmos0 vd_n vg_n vs_n vb_n psvt_leak      l=0.1 w=3.0 nfing=1 mult=10
xpmos1 vd_float1 vg_n vs_n vb_n psvt_leak l=0.2 w=1.0 nfing=1 mult=10
xpmos2 vd_float2 vg_n vs_n vb_n psvt_leak l=0.5 w=8.0 nfing=1 mult=10
xpmos3 vd_float3 vg_n vs_n vb_n psvt_leak l=1.0 w=8.0 nfing=1 mult=10



vd vd_n 0 dc -1.0
vs vs_n 0 dc 0
vg vg_n 0 dc -1.0
vb vb_n 0 dc 0

*Notice that vb is stepped also to 0.3V for pmos.
*Investigate the difference between the last vb=0.2block and the last but one vb=0.2block
*(when stepped to only 0.2V) to understand why.
.step vb 0 0.3 0.1
.step vd 0 -1.0 -0.05
.dc vg 1.0 -1.0 -0.05
.plot id(xpmos0.m1)
.plot ib(xpmos0.m1)

*NOTICE: this 90nm model is of level bsim3, hence the gate leakage calculation
*is based on a .subckt --> ig-extraction can not be accomplished as a part of
*the M1 MOSFET parameters. Instead an amperemeter must be used.
*.plot ig(xpmos0.m1)

.plot i(vg)
.plot gm(xpmos0.m1)
.plot gds(xpmos0.m1)


.extract label=vg file=extracts.txt vg(xpmos0.m1)
.extract label=vd file=extracts.txt vd(xpmos0.m1)
.extract label=vs file=extracts.txt vs(xpmos0.m1)
.extract label=vb file=extracts.txt vb(xpmos0.m1)

.extract label=vth file=extracts.txt vt(xpmos0.m1)
.extract label=gm_max file=extracts.txt max(gm(xpmos0.m1))
.extract label=gm_min file=extracts.txt min(gm(xpmos0.m1))
.extract label=gds_max file=extracts.txt max(gds(xpmos0.m1))
.extract label=gds_min file=extracts.txt min(gds(xpmos0.m1))
*.extract label=ig file=extracts.txt ig(xpmos0.m1)


.end
```

C.2 CV simulations

C.2.1 CV simulations for nmos devices

CV CHARACTERISTICS FOR NMOS

```
.option nowarn=902 !Turn off warning "Model parameter ignored"
.option aex !Allow for saving extracted values to file
.option noascii !Turn off acsii-based plotting of results in .chi-file
.option jwdb !Create .wdb output
.option nocou !Do not create .cou output
.probe v
.temp 27.0000

.lib /dak/90nm_40b1_eldo/cmos090_tt.mod
*.lib /dak/90nm_40b1_eldo/cmos090_stat.mod
*.lib /dak/90nm_40b1_eldo/cmos090_ff.mod
*.lib /dak/90nm_40b1_eldo/cmos090_ffa.mod
*.lib /dak/90nm_40b1_eldo/cmos090_fs.mod
*.lib /dak/90nm_40b1_eldo/cmos090_fsa.mod
*.lib /dak/90nm_40b1_eldo/cmos090_sf.mod
*.lib /dak/90nm_40b1_eldo/cmos090_sfa.mod
*.lib /dak/90nm_40b1_eldo/cmos090_ss.mod
*.lib /dak/90nm_40b1_eldo/cmos090_ssa.mod

*nmos0: w=1.2 l=0.1
*nmos1: w=1.0 l=0.2
*nmos2: w=4.0 l=0.5
*nmos3: w=4.0 l=1.0


xnmos0 vd_n vg_n vs_n vb_n nsvt_leak w=1.2 l=0.1 nfing=1 mult=10
xnmos1 vd_n vg_n vs_n vb_n nsvt_leak w=1.0 l=0.2 nfing=1 mult=10
xnmos2 vd_n vg_n vs_n vb_n nsvt_leak w=4.0 l=0.5 nfing=1 mult=10
xnmos3 vd_n vg_n vs_n vb_n nsvt_leak w=4.0 l=1.0 nfing=1 mult=10



vs vs_n 0 dc 0.0
vg vg_n 0 dc 0.0
vd vd_n 0 dc 0.0
vb vb_n 0 dc 0.0



.dc vg -1 1 0.005


.defwave cbb_nmos0_abs=abs(cbb(xnmos0.m1))
.defwave cbd_nmos0_abs=abs(cbd(xnmos0.m1))
.defwave cbs_nmos0_abs=abs(cbs(xnmos0.m1))
.defwave cbg_nmos0_abs=abs(cbg(xnmos0.m1))

.defwave cgg_nmos0_abs=abs(cgg(xnmos0.m1))
.defwave cgb_nmos0_abs=abs(cgb(xnmos0.m1))
.defwave cgs_nmos0_abs=abs(cgs(xnmos0.m1))
.defwave cgd_nmos0_abs=abs(cgd(xnmos0.m1))

.defwave c_g_nmos0_abs=abs(cgb(xnmos0.m1)+cgs(xnmos0.m1)+cgd(xnmos0.m1)) !equals cgg_nmos0_abs
.defwave c_b_nmos0_abs=abs(cbg(xnmos0.m1)+cbs(xnmos0.m1)+cbd(xnmos0.m1)) !equals cbb_nmos0_abs

.defwave cgb_tot_abs=abs(cgb(xnmos0.m1)+cgb(xnmos1.m1)+cgb(xnmos2.m1)+cgb(xnmos3.m1))
.defwave cgs_tot_abs=abs(cgs(xnmos0.m1)+cgs(xnmos1.m1)+cgs(xnmos2.m1)+cgs(xnmos3.m1))
.defwave cgd_tot_abs=abs(cgd(xnmos0.m1)+cgd(xnmos1.m1)+cgd(xnmos2.m1)+cgd(xnmos3.m1))
.defwave cgg_tot_abs=abs(cgg(xnmos0.m1)+cgg(xnmos1.m1)+cgg(xnmos2.m1)+cgg(xnmos3.m1))

.defwave cbg_tot_abs=abs(cbg(xnmos0.m1)+cbg(xnmos1.m1)+cbg(xnmos2.m1)+cbg(xnmos3.m1))
.defwave cbs_tot_abs=abs(cbs(xnmos0.m1)+cbs(xnmos1.m1)+cbs(xnmos2.m1)+cbs(xnmos3.m1))
.defwave cbd_tot_abs=abs(cbd(xnmos0.m1)+cbd(xnmos1.m1)+cbd(xnmos2.m1)+cbd(xnmos3.m1))
.defwave cbb_tot_abs=abs(cbb(xnmos0.m1)+cbb(xnmos1.m1)+cbb(xnmos2.m1)+cbb(xnmos3.m1))

.defwave csg_tot_abs=abs(csg(xnmos0.m1)+csg(xnmos1.m1)+csg(xnmos2.m1)+csg(xnmos3.m1))
.defwave cdg_tot_abs=abs(cdg(xnmos0.m1)+cdg(xnmos1.m1)+cdg(xnmos2.m1)+cdg(xnmos3.m1))


.plot w(cbb_nmos0_abs)
.plot w(cbd_nmos0_abs)
.plot w(cbs_nmos0_abs)
.plot w(cbg_nmos0_abs)
```

```
.plot w(cgg_nmos0_abs)
.plot w(cgb_nmos0_abs)
.plot w(cgs_nmos0_abs)
.plot w(cgd_nmos0_abs)

.plot w(c_g_nmos0_abs)
.plot w(c_b_nmos0_abs)

.plot w(cgb_tot_abs)
.plot w(cgs_tot_abs)
.plot w(cgd_tot_abs)
.plot w(cgg_tot_abs)

.plot w(cbg_tot_abs)
.plot w(cbs_tot_abs)
.plot w(cbd_tot_abs)
.plot w(cbb_tot_abs)

.plot w(csg_tot_abs)
.plot w(cdg_tot_abs)



.end
```

C.2.2 CV simulations for pmos devices

CV CHARACTERISTICS FOR PMOS

```
.option nowarn=902 !Turn off warning "Model␣parameter␣ignored"
.option aex !Allow for saving extracted values to file
.option noascii !Turn off acsii-based plotting of results in .chi-file
.option jwdb !Create .wdb output
.option nocou !Do not creat .cou output
.probe v
.temp 27.0000

.lib /dak/90nm_40b1_eldo/cmos090_tt.mod
*.lib /dak/90nm_40b1_eldo/cmos090_stat.mod
*.lib /dak/90nm_40b1_eldo/cmos090_ff.mod
*.lib /dak/90nm_40b1_eldo/cmos090_ffa.mod
*.lib /dak/90nm_40b1_eldo/cmos090_fs.mod
*.lib /dak/90nm_40b1_eldo/cmos090_fsa.mod
*.lib /dak/90nm_40b1_eldo/cmos090_sf.mod
*.lib /dak/90nm_40b1_eldo/cmos090_sfa.mod
*.lib /dak/90nm_40b1_eldo/cmos090_ss.mod
*.lib /dak/90nm_40b1_eldo/cmos090_ssa.mod

*pmos0: w=3.0 l=0.1
*pmos1: w=1.0 l=0.2
*pmos2: w=8.0 l=0.5
*pmos3: w=8.0 l=1.0



xpmos0 vd_n1 vg_n vs_n vb_n1 psvt_leak w=3.0 l=0.1 nfing=1 mult=10
xpmos1 vd_n2 vg_n vs_n vb_n1 psvt_leak w=1.0 l=0.2 nfing=1 mult=10
xpmos2 vd_n3 vg_n vs_n vb_n1 psvt_leak w=8.0 l=0.5 nfing=1 mult=10
xpmos3 vd_n4 vg_n vs_n vb_n1 psvt_leak w=8.0 l=1.0 nfing=1 mult=10



vs vs_n 0 dc 0.0
vg vg_n 0 dc 0.0
vd vd_n 0 dc 0.0
vb vb_n 0 dc 0.0



.dc vg -1 1 0.005


.defwave cbb_pmos0_abs=abs(cbb(xpmos0.m1))
.defwave cbd_pmos0_abs=abs(cbd(xpmos0.m1))
.defwave cbs_pmos0_abs=abs(cbs(xpmos0.m1))
.defwave cbg_pmos0_abs=abs(cbg(xpmos0.m1))

.defwave cgg_pmos0_abs=abs(cgg(xpmos0.m1))
.defwave cgb_pmos0_abs=abs(cgb(xpmos0.m1))
.defwave cgs_pmos0_abs=abs(cgs(xpmos0.m1))
.defwave cgd_pmos0_abs=abs(cgd(xpmos0.m1))

.defwave c_g_pmos0_abs=abs(cgb(xpmos0.m1)+cgs(xpmos0.m1)+cgd(xpmos0.m1)) !equals cgg_pmos0_abs
.defwave c_b_pmos0_abs=abs(cbg(xpmos0.m1)+cbs(xpmos0.m1)+cbd(xpmos0.m1)) !equals cbb_pmos0_abs

.defwave cgb_tot_abs=abs(cgb(xpmos0.m1)+cgb(xpmos1.m1)+cgb(xpmos2.m1)+cgb(xpmos3.m1))
.defwave cgs_tot_abs=abs(cgs(xpmos0.m1)+cgs(xpmos1.m1)+cgs(xpmos2.m1)+cgs(xpmos3.m1))
.defwave cgd_tot_abs=abs(cgd(xpmos0.m1)+cgd(xpmos1.m1)+cgd(xpmos2.m1)+cgd(xpmos3.m1))
.defwave cgg_tot_abs=abs(cgg(xpmos0.m1)+cgg(xpmos1.m1)+cgg(xpmos2.m1)+cgg(xpmos3.m1))

.defwave cbg_tot_abs=abs(cbg(xpmos0.m1)+cbg(xpmos1.m1)+cbg(xpmos2.m1)+cbg(xpmos3.m1))
.defwave cbs_tot_abs=abs(cbs(xpmos0.m1)+cbs(xpmos1.m1)+cbs(xpmos2.m1)+cbs(xpmos3.m1))
.defwave cbd_tot_abs=abs(cbd(xpmos0.m1)+cbd(xpmos1.m1)+cbd(xpmos2.m1)+cbd(xpmos3.m1))
.defwave cbb_tot_abs=abs(cbb(xpmos0.m1)+cbb(xpmos1.m1)+cbb(xpmos2.m1)+cbb(xpmos3.m1))

.defwave csg_tot_abs=abs(csg(xpmos0.m1)+csg(xpmos1.m1)+csg(xpmos2.m1)+csg(xpmos3.m1))
.defwave cdg_tot_abs=abs(cdg(xpmos0.m1)+cdg(xpmos1.m1)+cdg(xpmos2.m1)+cdg(xpmos3.m1))


.plot w(cbb_pmos0_abs)
.plot w(cbd_pmos0_abs)
.plot w(cbs_pmos0_abs)
.plot w(cbg_pmos0_abs)

.plot w(cgg_pmos0_abs)
.plot w(cgb_pmos0_abs)
.plot w(cgs_pmos0_abs)
.plot w(cgd_pmos0_abs)
```

```
.plot w(c_g_pmos0_abs)
.plot w(c_b_pmos0_abs)

.plot w(cgb_tot_abs)
.plot w(cgs_tot_abs)
.plot w(cgd_tot_abs)
.plot w(cgg_tot_abs)

.plot w(cbg_tot_abs)
.plot w(cbs_tot_abs)
.plot w(cbd_tot_abs)
.plot w(cbb_tot_abs)

.plot w(csg_tot_abs)
.plot w(cdg_tot_abs)



.end
```

Appendix D

Contents of electronic attachment

Attachment\Results\DC
IV measurement and simulation files.
Relevant Matlab plotting script.

Attachment\Results\AC
CV measurement and simulation files.
Relevant Matlab plotting scripts.

Attachment\Eldo
Eldo circuit simulation files.

Attachment\Pictures\DC
Pictures from IV measurements and simulations.

Attachment\Pictures\AC
Pictures from CV measurements and simulations.

Attachment\Pictures\Other
Other pictures.