NTNU

Norwegian University of
Science and Technology

# Gate driver design for normally-off SiC JFET

Silicon Carbide technology for PV inverters

**Aleksejs Grigorjevs**

Master of Science in Electric Power Engineering
Submission date: July 2011
Supervisor: Tore Marvin Undeland, ELKRAFT

Norwegian University of Science and Technology
Department of Electric Power Engineering

# PREFACE

The master thesis was developed in the Department of Electrical Power Engineering at the Norwegian University of Science and Technology (NTNU) in collaboration with Eltek Valere, the power electronics R&D company. The thesis concludes my 1,5 year long exchange period in Norway.

The practical part of the thesis is fulfilled in the laboratory facilities of Eltek Valere in Kristiansand, Norway.

I would like to use the opportunity to thank people that have influenced my work.

Professor Tore Undeland who has been my supervisor and advised me throughout the work.

Kjetil Bøysen and Arkadiusz Kulka who have been my co-supervisors at Eltek Valere for providing valuable information and the opportunity to use the power electronics facilities at Eltek Valere.

Roar Myhre at Eltek Valere for holding the vital discussions on the measurement setup and results.

Special thanks to Øyvind Mjanger at Eltek Valere for helping with the design of the gate driver board. Without this help I might not make it before the deadline.

PhD students at Energy Conversion group Ibrahim Abuishmais and Fritz Schimpf for their help, input and valuable discussions on the way to fulfilment of the thesis.

Vladimir Klubicka and Thor Lohse who helped me out with establishing the laboratory setup in the final stages of the thesis.

All these people did not hesitate to help whenever I came by or contacted them.

Last but not least, I am very lucky to have Tania who has made both the good and the bad days better. My life would not be the same without You.

Trondheim, July 15, 2011

Aleksejs Grigorjevs

# ABSTRACT

In this thesis a research on modern SiC semiconductor devices is made with a bias on the driving methods and requirements. A compact two-stage gate driver circuit for SiC VJFET is developed, the transistor is characterized and its gate requirements are estimated. The performance of developed driver is compared to the commercial SiC VJFET gate driver from SemiSouth. The conclusion is that both drivers behave similarly in switching the device in a half-bridge converter. In addition, the developed gate driver is a rather cheap solution compared to SemiSouth driver which is only available as engineering sample. Though, the optimization and especially shaping of the gate voltage/current waveforms must be done in order to extract the maximum performance of the SiC VJFET and obtain the lowest possible switching and on-state losses.

Simulations are also carried out for validating the design of the board. The simulated circuit shows good correspondence with what was expected and described in scientific papers.

The SiC BJT base driver circuit, which in addition was used to drive SiC MOSFET and SiC VJFET, is also characterized. The AC-coupled SiC BJT base drive circuit (section 3.6.3), which is also developed during the thesis, displayed a relatively good performance taken into account the simple design and cost effective nature of this driver.

A characterization of different SiC transistors, i.e. SiC VJFET, SiC MOSFET and SiC BJT, is made. Two SiC Schottky diodes are also tested as the freewheeling diodes. Extensive experiments are performed on the developed half-bridge converter utilizing various combinations of SiC transistors, SiC diodes and gate/base driver circuits. The obtained results conclude that these new SiC transistors switch extremely fast and with relatively low energy losses, so that they can be used in high-frequency applications. Thus, converters that utilize SiC transistors can be made extremely compact. SiC BJT showed the best result with the highest switching speed and lowest energy losses compared to other two SiC transistors.

# TABLE OF CONTENTS

# LIST OF FIGURES

# LIST OF TABLES

# 1. INTRODUCTION

## 1.1. Motivation for research

Global climate change and depleting fossil fuel reserves are driving society's quest for a sustainable energy infrastructure. The need for a cleaner environment and the continuous increase in energy demand opens new opportunities for decentralized renewable energy production [1]. Distributed Generation (DG) system is the most promising solution to overcome the overloading of distribution grids. DG system usually consists of renewable sources like solar, hydro or wind with the advantage that the power is produced near places where it is consumed. This leads to extinction of transmission losses.

In the last decade solar energy technologies have become less expensive and more efficient making it an ideal replacement for traditional fossil fuels like coal or gas. Figure 1.1 shows the tendency of cost per watt reduction for solar power production.

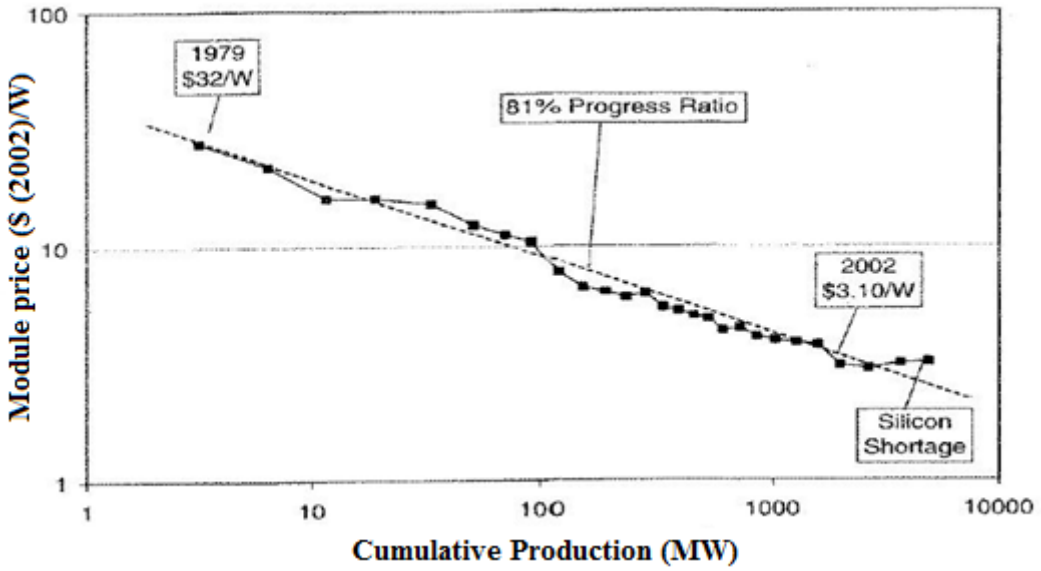



**Figure 1.1. Cumulative production of solar power vs. PV module price (From www.elkem.no)**

Over the past 30 years the PV industry has achieved impressive price decreases. The price of PV modules has reduced by 22% each time the cumulative installed capacity (in MW) has doubled [2].

It can be seen from Figure 1.1 that the price for solar energy has decreased from $32/W in 1979 down to $3.10/W in 2002. Due to lack of pure silicon in the last few years a slight increase in the price can be observed. Nevertheless a PV system is still much more expensive

than traditional power generation systems. The main reason for this is the high manufacturing cost of PV panels, but on the other hand the energy from the sun is infinite, free and will be available to humanity for millions of years. Perhaps most important issue is that solar energy is one solution that offers environmentally friendly power generation.

In addition to the PV module cost, the cost and reliability of PV inverters are basic issues if market competitive PV supply systems are the aim. A reflection of the development of specific cost and production quantity for a PV-inverter of nominal power between 1 and 10kW during the last two decades is seen in Figure 1.2.

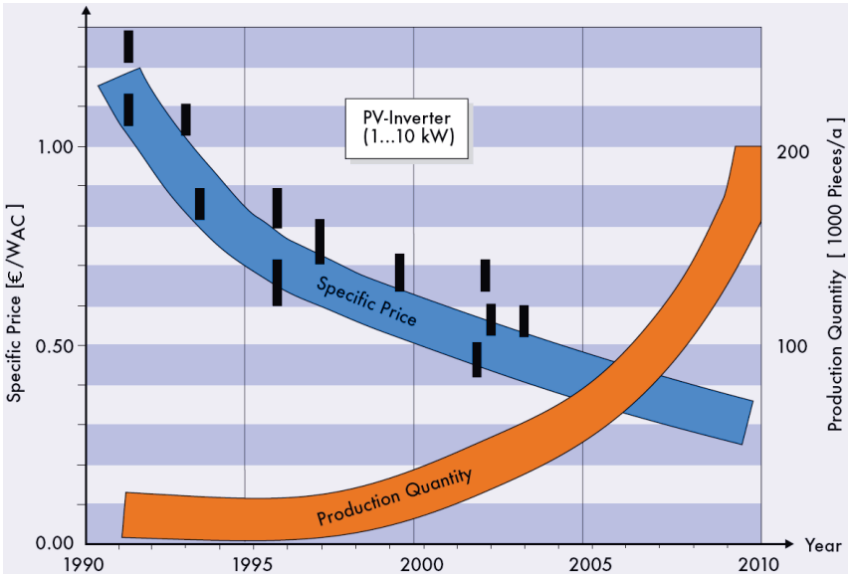



**Figure 1.2. Development and prognoses of specific cost and production quantity for a PV-inverter of nominal power between 1 and 10kW during the last two decades [3]**

The inverter cost share represents about 10-15% of the total investment cost of a grid connected system [3]. In Figure 1.2 the development of the PV inverters specific cost (€/$W_{AC}$) of small to medium power range (1-10 kW) is illustrated. It can be seen that the inverter cost of this power class has decreased by more than 50% during the last decade. The main reasons for this reduction are the increase of the production quantities and the implementation of new system technologies (e.g. string-inverters). The corresponding specific cost was expected to achieve about 0.3 €/$W_{AC}$ by the year 2010.

As mentioned before, decentralized energy production using solar energy could be a solution for covering continuously-increasing energy needs. According to the latest report of IEA

PVPS on installed PV power [4], during 2009 there was a total of 6.2 GW of installed PV systems, of which the majority (90%) are installed in Germany, Spain, USA and Japan.

The growth of installed capacity since 1992 and the split of this capacity between the two primary applications for PV, representing grid connected and stand-alone applications, can be seen in Figure 1.3. Grid connected PV systems have had an enormous increase in their market share over the last decade.

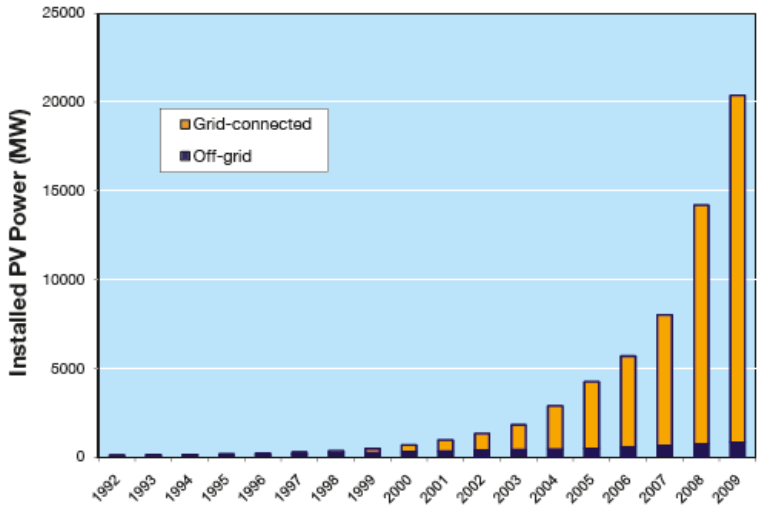



**Figure 1.3. Cumulative installed capacity between 1992 and 2009 in the IEA-PVPS reporting countries [4]**

The annual rate of growth of cumulative installed capacity in the IEA PVPS countries was 44 %, down from the record 77 % recorded in 2008. This European market boom in 2008 is a result of the 2.5 GW of installation in Spain and the 1.5 GW in Germany. For comparison reason Figure 1.4 shows statistics from previous years. Even a quick overview is enough to mention that the installed PV power has increased from approximately 8000 MW in 2007 up to more than 20000 MW in 2009.

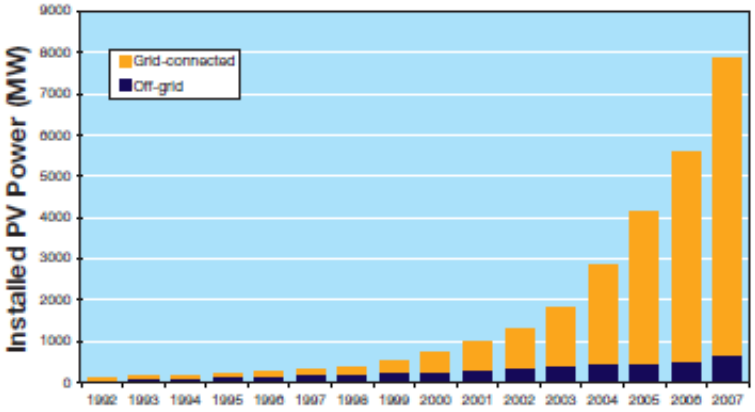



**Figure 1.4. Cumulative installed capacity between 1992 and 2007 in the IEA-PVPS reporting countries[5]**

A world energy consumption scenario by year 2050 [6] can be observed in Figure 1.5.

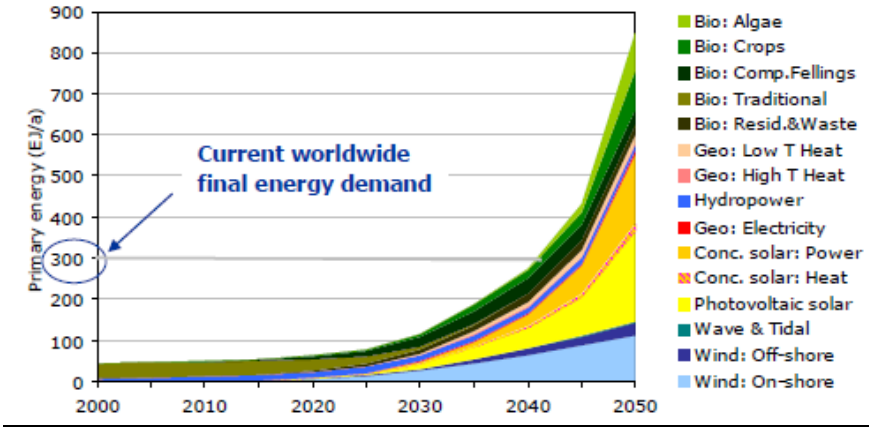



**Figure 1.5. Global deployment potential of various renewable energy sources**

According to Figure 1.5 it is projected that by the year 2050 a major part of the world energy demand will be covered by solar power generation. In order to realize this scenario an ultimate goal is to contribute to the cost reduction of existing solar energy technology and provide investments in research and development of new technologies.

The largest technical potential and *realisable* technical potential for sustainable power and heat generation is from direct solar energy, particularly in regions with a large amount of direct irradiation.

The Energy Scenario includes three different sources of solar energy [6]:

• Solar power from photovoltaics (PV)

• Concentrating solar power (CSP)

• Concentrating solar high-temperature heat for industry (CSH)

The potential adopted for these sources is shown in Figure 1.6.

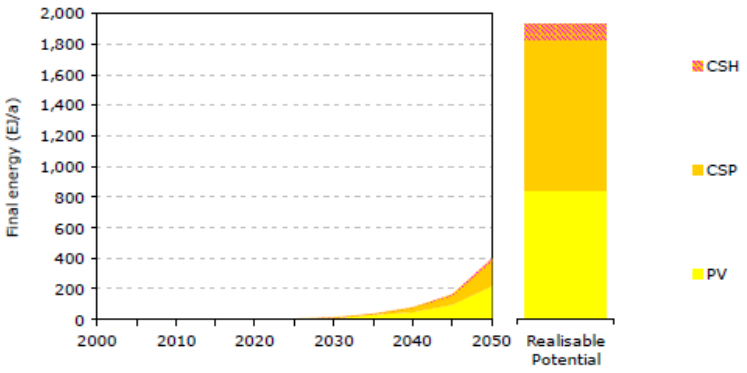



**Figure 1.6. Global deployment potential of solar power and heat (Left: Evolution of deployment potential over time, right: Maximum feasible potential)**

According to Figure 1.6 main power generation is expected from PV and CSP. PV is a well-established source of electric energy with around 21 GW of capacity installed worldwide at the end of 2009 as was already mentioned in Figure 1.3. The Scenario contains a potential for PV based on continuing annual growth rates of 25-30%, including outputs from both building-integrated and large area PV installations.

PV power generation has a number of important characteristics that, depending on the local conditions, enable the shift to a more sustainable energy system. Six primary groups of benefits can be identified [7] and the result is seen in Figure 1.7.

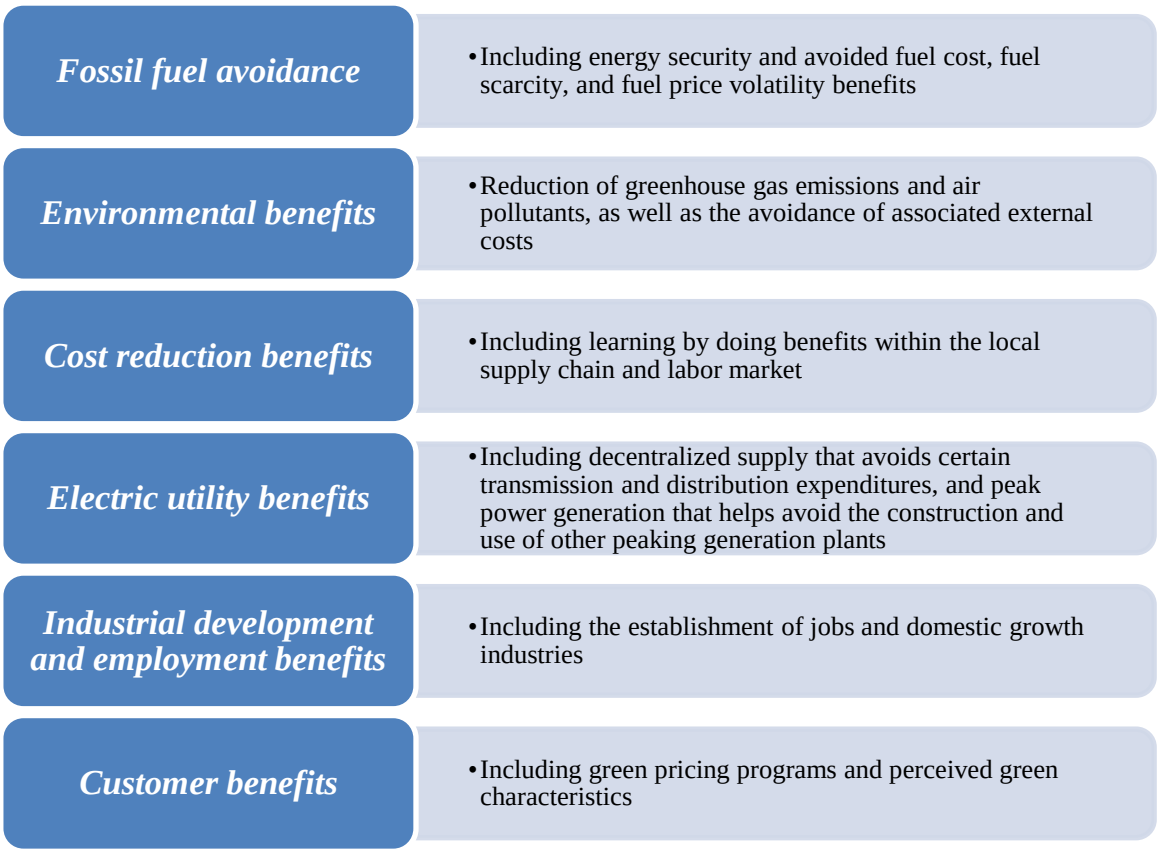



**Figure 1.7. Six primary groups of benefits of PV power generation**

## 1.2. Thesis structure

The thesis is divided into 9 chapters and a brief content review of each chapter is outlined below.

Chapter 1 deals with general considerations on photovoltaic power generation and motivation for research.

Chapter 2 discusses the possibility of PV converter improvements by utilizing Silicon Carbide (SiC) technology. A survey on commercially available SiC transistors is shown. Chapter also presents a comparative analysis of today's PV converters.

Chapter 3 contains general considerations of gate/base drive circuits and describes some topological circuits that govern gate driver circuit design. At the end of the chapter three SiC transistor gate/base driver solutions from different SiC transistor manufacturers are presented.

Chapter 4 contains gate requirement estimation of SiC VJFET as well as a step-by-step gate driver design procedure.

Chapter 5 presents LTspice software simulation results for proposed gate driver circuit.

Chapter 6 contains the description of laboratory setup together with a brief introduction to the test procedure. This chapter also presents the measurement plan for the experiments.

Chapter 7 shows the obtained results from performed experiments.

Chapter 8 provides a detailed analysis of simulation (chapter 5) and measurement (chapter 7) results.

Chapter 9 contains the key findings of the thesis and the scope for future research.

The thesis will thus present many different aspects, from theoretical operation to electronic board conception and will be completed with series of validation tests on the final system.

# 2. SILICON CARBIDE TECHNOLOGY FOR PV INDUSTRY

## 2.1. Introduction

Solar power is still too expensive to compete in free market economies and the reality is that the majority of today's electricity is generated utilizing the burning of fossil fuel. Solar power's success has predominantly come from subsidized markets, mainly Germany, Spain and Japan [4]. PV technology has a great potential to compete on a global energy market, but a reduction in electrical generation cost must be done. One of the most important ways to cut the expenses is to increase the efficiency of the PV inverter that converts dc output of the photovoltaic cells into the ac form needed by the grid [8]. Higher efficiency in the energy conversion stage will directly reduce the pay-back time of a system and increase the profitability. An interesting characteristic of photovoltaic converters is the fact that 100% of the energy needs to be processed by the power electronics stage, while this value is approximately 33% for double fed induction generators in wind turbines and 10% for variable speed generators in small hydraulic plants [9].

Therefore, in order to boost the efficiencies of PV systems of great interest are the newest developments regarding semiconductor materials, as operation with reduced losses even at high blocking voltages are becoming more attractive, leading to some changes not only on the choice of topologies by also on the concept of the whole system.

## 2.2. Today's converter technologies in PV systems

As mentioned above, 100% of the energy in photovoltaic converters needs to be processed by the power electronics stage. This makes energy conversion stage an important part of the total PV system with efficiency regarded as the vital parameter. Since a PV cell produce dc output voltage and current, an inverter is needed to feed the generated power to the grid.

Nowadays, two technologies are mainly used either with the aid of HF-transformer or transformerless topologies with excluded transformer. Transformerless topologies for PV inverters are an upcoming technology [10]. This is due to the fact that transformer operated at grid frequency is bulky, expensive and produce losses and is therefore regarded as a poor component due to increased size, weight, and price. One way to omit the bulky transformer is to operate at higher frequencies. Topologies with HF-transformers are a good solution when

galvanic isolation is necessary. HF-inverters are often realized as resonant topologies with zero-voltage- or zero-current-switching to achieve low losses. Some inverters use a transformer embedded in a high-frequency dc–dc converter or dc–ac inverter as shown in Figure 2.1.

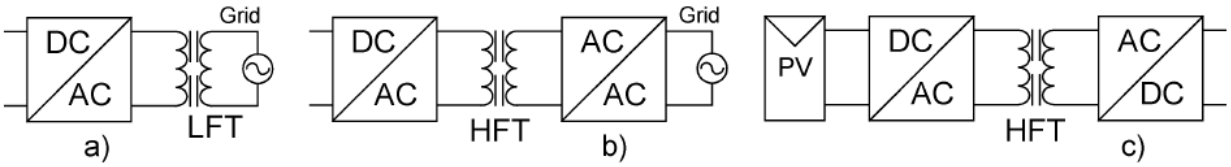



**Figure 2.1. Examples of transformer-included inverter solutions. (a) Line-frequency transformer (LFT) is placed between the grid and the inverter (solves problems with injection of dc currents into the grid). (b) High-frequency transformer (HFT) is embedded in an HF-link grid-connected ac/ac inverter. (c) HFT is embedded in a dc-link PV-module-connected dc–dc converter [11].**

### 2.2.1. HF-transformer converters

One example of topology that employs HF-transformer can be seen in Figure 2.2. A Dual active bridge (DAB) bidirectional DC/DC converter has the advantages of decreased number of devices, soft-switching commutations, low cost, and high efficiency [12].

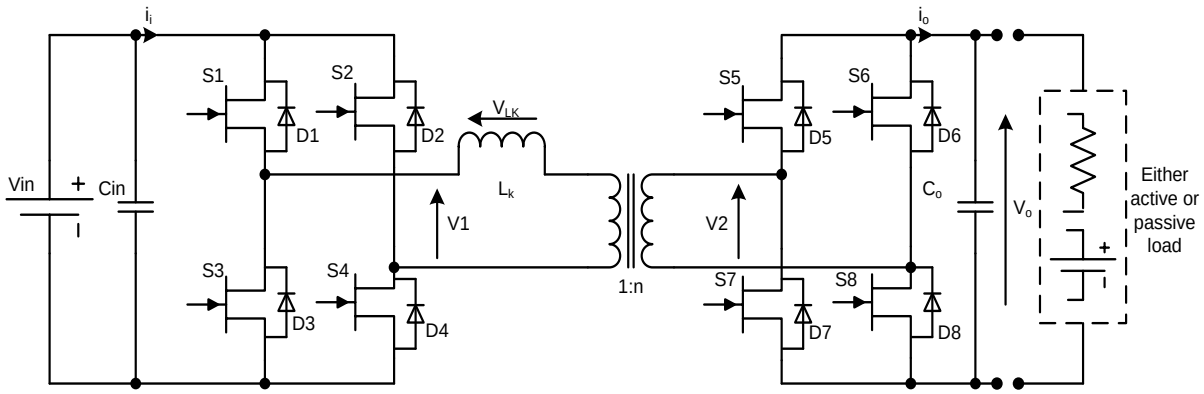



**Figure 2.2. Circuit diagram of single-phase DAB converter**

Both bridges are controlled with constant duty cycle of 50 %. This way a high-frequency square-wave voltage at transformer terminals is generated (±vi, ±vo). Due to the presence of the transformer leakage inductance with a controlled and known value, the power flow can be controlled by appropriate phase shift between two square waves. Controlled phase shift makes the bidirectional power transfer possible. It is worth mentioning that the power is delivered from

the bridge which generates the leading square wave. The switching characteristics of DAB converter are shown in Figure 2.3.

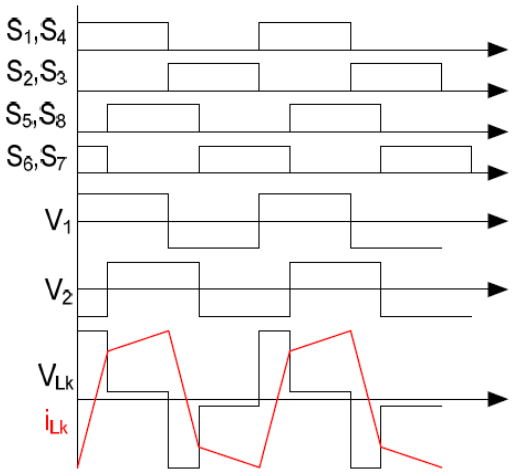



**Figure 2.3. DAB converter main switching waveforms**

The primary bridge is composed by S1, S2, S3 and S4. The gate signals of S1 and S4 are the same. The gate signals of S2 and S3 are also identical. The gate signals of S1 and S2 are complementary 50% duty cycle signals. With this control signals, the voltage V1, with values ±vi, is generated in the primary side of the transformer.

In a similar way, a voltage V2 (with values ±vo) is generated in the secondary side of the transformer, by controlling the switches of the secondary bridge (S5, S6, S7 and S8). All the control signals of the secondary bridge are similar to the signals of the primary, but with a certain phase shift. These two phase shifted signals (V1 and V2) generate a voltage ($V_{Lk}$) in the leakage inductance (Lk) of the transformer and a certain current flows through it. This current is controlled by the phase shift between the primary and secondary voltages of the transformer.

Since the power flow in PV inverters is always in one direction, i.e. from the PV cells, the DAB converter can be modified to suit this requirement. The result of such modification can be observed in Figure 2.4.

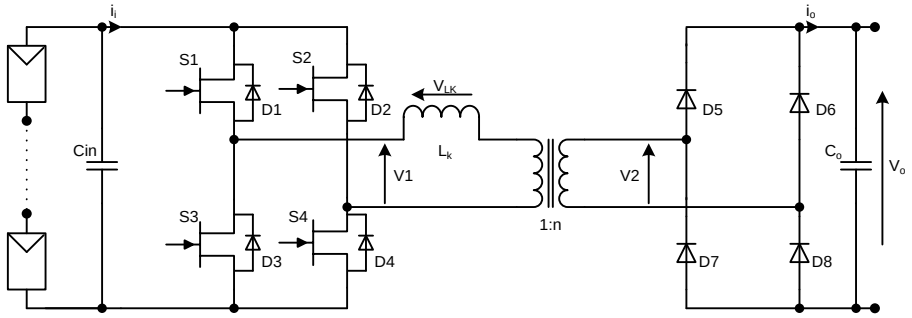



**Figure 2.4. Circuit diagram of single-phase DAB converter suitable for PV inverters**

In this case the dc supply from the PV cells is transformed into high frequency ac and rectified on the secondary side of the transformer by means of a diode rectifier. By removing the transistors from the secondary side the converter cost is decreased together with the decrease of overall losses. The control of the converter in Figure 2.4 is more complicated though than in the case of Figure 2.2 discussed previously.

### 2.2.2. Transformerless PV converters

Transformerless PV converters have a severe drawback of fluctuating potential of the PV-generator. One of the possibilities to prevent this fluctuating potential of the PV-generator is to disconnect to DC-side from the AC-side during the freewheeling periods of the inverter. Two patented topologies use this idea: HERIC (Highly Efficient and Reliable Inverter Concept) [13] and the H5-topology [14]. Both topologies base on the standard full-bridge.

The HERIC-topology, shown in Figure 2.5 introduces a combination of two switches and diodes in parallel to the grid. They are operated at grid-frequency and form a new free-wheeling path. During free-wheeling the switches of the full-bridge can be open, thus disconnecting dc- and ac-side. Switches S1-S4 are operated at high frequency, while S5 and S6 are operated at grid frequency.

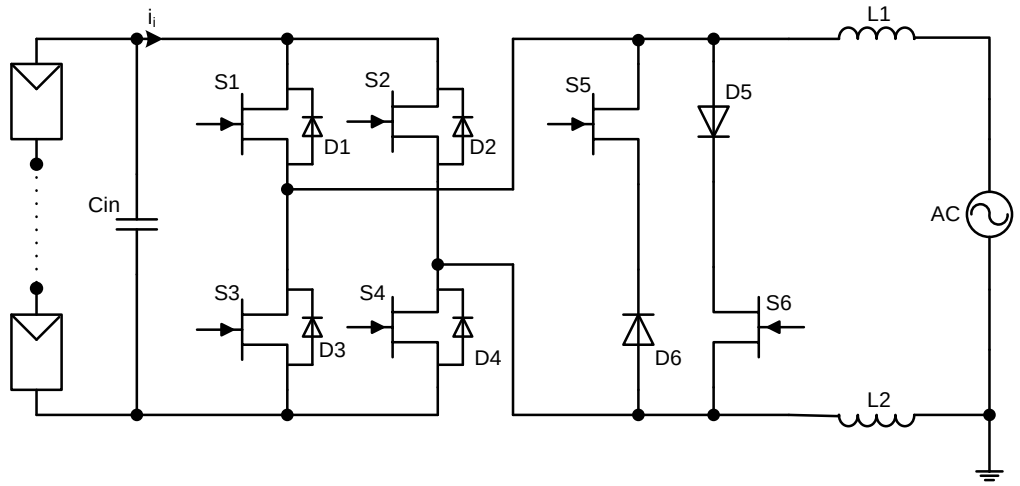



**Figure 2.5. HERIC (Highly Efficient and Reliable Inverter Concept) converter topology**

The H5-Topology shown in Figure 2.6 only needs one more switch compared to the normal full bridge. The switches S5, S2 and S4 are operated at high frequency, S1 and S3 at grid frequency. During free-wheeling S5 is open, disconnecting dc- and ac-side. The free-wheeling-path is closed via S1 and the inverse diode of S3 for positive and S3 and the Diode of S1 for

negative current. Compared to HERIC, H5 has the advantage of using fewer components while HERIC uses less switches in series on the other hand.

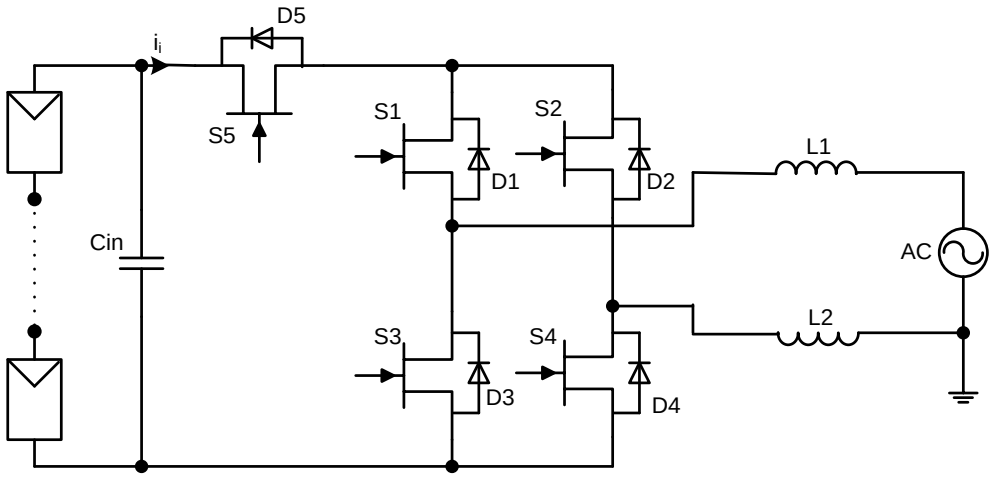



**Figure 2.6. H5 converter topology**

Here, switches S3, S4 and S5 are operated at high frequency, while S1 and S2 are operated at grid frequency. For high frequency switching MOSFETs can be used due to low switching loss. For low frequency switching IGBTs can be employed due to relatively low conduction loss. Combination of MOSFETs with IGBTs within half-bridge configuration can lead to reduction of overall losses.

### 2.2.3. Advantages and disadvantages of transformerless PV converters

The advantages of the transformerless topologies are as follows:

- Reduced weight, size and volume of the PV systems.
- Absence of the transformer means reduced transformer losses and thus improved efficiency of the system by 1-2%.
- No inductive reactance contribution from the transformer, thus improved power factor for light load operation.
- Reduced cost of the PV application since the transformer is eliminated.

The absence of high or low frequency transformer, however, presents other challenges which the different topologies of inverters have to address. Among these are the following:

- The introduction of a leakage current between the output and input due to lack of galvanic isolation.
- The change of voltage amplitude of the input to suit the requirements of the output or grid.

- The surface of the PV array forms a capacitor, with respect to ground, which is the energized by the fluctuating potential. A person connected to ground and touching the PV array may conduct the capacitive current to ground, causing an electrical hazard to the person involved.
- The voltage fluctuations generate electric and magnetic fields around the PV array (electromagnetic interference).

## 2.3. Silicon carbide technology

The most promising materials in the semiconductor industry today are mainly hexagonal crystal structure Silicon Carbide (4H-SiC) and Gallium Nitride (GaN). Characteristics of these materials showing far more superior qualities than Si are reflected in Figure 2.7. GaN is shown for comparison reason and the main research is further focused on SiC.

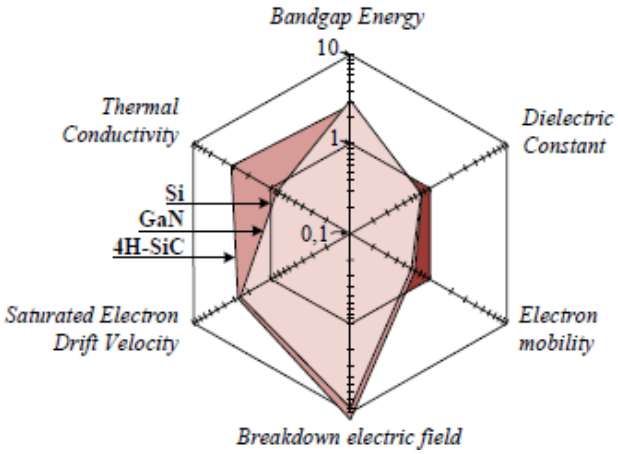



**Figure 2.7. Characteristics of semiconductor materials normalized to the values of Si (logarithmic scale) [9]**

The most important feature of SiC is high electric breakdown field. This allows manufacturing of devices with thinner and shorter drift layer resulting in a fairly low specific on-state resistance even at higher blocking voltages. The superior saturated electron drift velocity allows for fast dynamic behaviour. Due to the larger band gap energy value in relation to Si, SiC is stable operation at higher temperatures which is especially interesting for downhole oil development applications and other harsh environments. The thermal conductivity is far more superior for SiC material compared to both Si and GaN. In other words, devices made of SiC can dissipate larger amounts of heat even at high temperatures, what is especially attractive in applications oriented to high power density or to harsh ambient conditions like military and space. These outstanding features [15] of SiC come nevertheless at a higher cost per chip area,

which is considered as main drawback that still concerns the widespread of SiC devices. For more detailed description of SiC material and SiC semiconductor devices, reader is referred to author's specialization project found in [16].

## 2.4. SiC semiconductor devices

Recently, two classes of SiC power electronic devices are commercially available, namely Schottky diodes and field effect transistors [17]. SiC Schottky diodes are available from several manufacturers, including Infineon, Cree, IXYS, Microsemi, and STMicroelectronics, etc. The high voltage ratings to 1200 V and the near zero reverse recovery time of these devices, make them excellent choices for many other hard switching applications [18]. Similarly one of the most successful and promising device to replace Si-MOSFET and IGBT is the normally-off vertical JFET. SiC controllable switching devices in a variety of voltage and current levels are available as engineering samples such as JFETs from SemiSouth and SiCED, MOSFETs from Cree, and BJTs from Cree and TranSiC.

The important issue of SiC power semiconductor devices is the voltage rating which is typically 1200 V and in some cases reaches 1700 V, e.g. SJEP170R550 SiC JFET from SemiSouth. These high voltage transistors rarely reach high current capabilities though. Today's state-of-the-art Si MOSFETs and IGBTs are mainly rated to 600 V and are widely used in a variety of power electronics applications. Such transistors, for instance, are used in three-phase inverters that are based on multilevel or similar topologies. By utilizing 1200 V SiC transistors new converter topologies can be used that can lead to increase in power density and improvements in converter efficiency.

### 2.4.1. SiC VJFET

Figure 2.8 shows the equivalent schematic model of the normally-off SiC VJFET [17]. The result merges some of the recognizable characteristics of both MOSFETs and BJTs, without the most common negative characteristics of either.

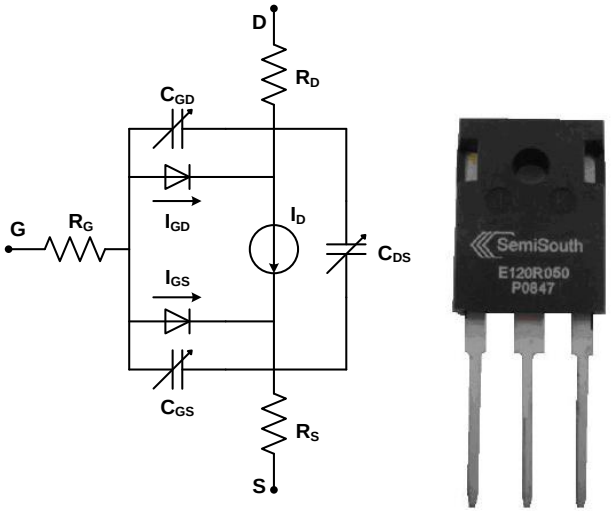



**Figure 2.8. Equivalent schematic model (left) and TO-247 package (right) of the SiC VJFET [17]**

Figure 2.8 reveals that at the gate-source junction, a variable capacitance appears which resembles a classical MOSFET's gate-source capacitance. The value of this capacitance is lower though compared to a MOSFET. Just like in a BJT, a p-n diode also appears at the gate-source junction. This layout sets the basic gate requirement to deliver a dynamic charge to the gate capacitance during the turn-on and rapidly remove this charge to ensure a fast turn-off process [19]. Apart from dynamic charge/discharge requirement another vital gate requirement is the maintenance of the gate-source diode on by keeping it forward biased during the on-state. Due to SiC p-n diode's typical built-in potential of around 3 V at 25 °C the drive voltage must thus be kept at 3 V or higher. The gate driver circuit should also maintain the diode forward current ($I_{GFWD}$) during the on-state. The I-V characteristic of the gate-source diode is shown in Figure 2.9.

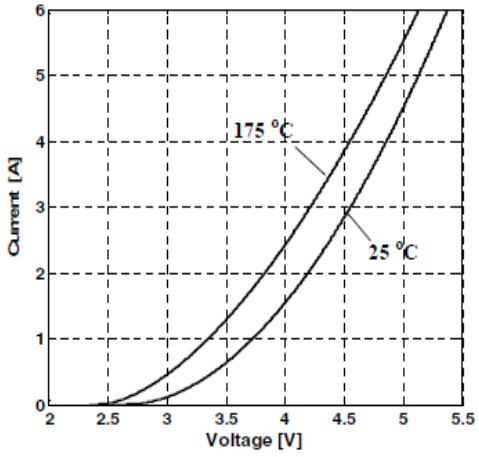



**Figure 2.9. I-V characteristics of the gate-source diode [17]**

A minimum gate current of $I_{GFWD}$ = 100 mA when the junction temperature is 25 °C is to be supplied to the gate while keeping the gate-source voltage of 3 V. This current raises to $I_{GFWD}$ = 500 mA for $T_J$ = 175 °C, revealing the temperature dependent nature of the gate threshold voltage. Therefore, the higher the junction temperature the lower the voltage is needed for the gate-source diode to start conducting.

Since the SiC VJFET is a very fast switching device with very low intrinsic capacitances careful attention should be paid to PCB layout design process using these devices [20]. Like MOSFET, high frequency oscillations between the device's internal capacitances and other circuit parasitics may be observed.

### 2.4.2. SiC MOSFET

The Cree has introduced a 1200 V SiC MOSFET with extremely low on-state resistance Rds(on) of 80 mΩ, thus removing the upper voltage limit of silicon MOSFETs [21]. It should be noted that high voltage (>1000 V) silicon MOSFETs can be manufactured, but due to fairly high Rds(on) their application is considered unpractical. Even though it seems that the physics of the device itself has not gone through many changes, according to manufacturers there are some differences in characteristics when compared to what is usually expected with high voltage silicon MOSFETs. These differences will be addressed later in this chapter.

From general MOSFET theory [22] it is known that MOSFET transistors are relatively simple to drive because their control electrode is isolated from the current conducting silicon, therefore a continuous on-state current is not required. Once the MOSFET transistors are turned-on, their drive current is practically zero. Figure 2.10 shows the switching model of the MOSFET. The most important parasitic components influencing switching performance are also shown in this model.

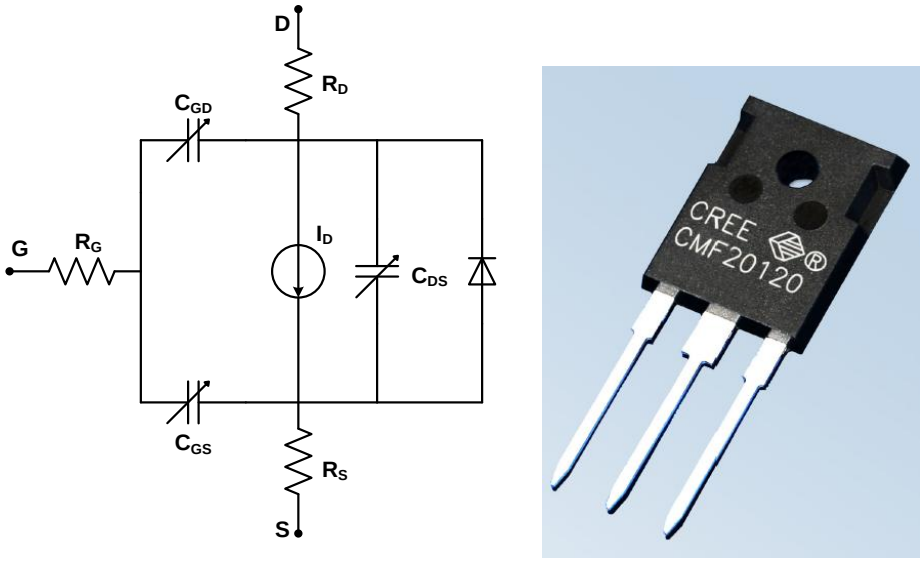



**Figure 2.10. Typical equivalent schematic model (left) and TO-247 package (right) of the SiC MOSFET [22]**

As in the SiC VJFET case, Figure 2.10 reveals that three variable capacitances appear on the MOSFET model. The switching performance of the MOSFET transistor is determined by how quickly the voltages can be changed across these capacitors. Therefore, in high speed switching applications, the most important parameters are the parasitic capacitances of the device. This mean that the analysis provided for the SiC VJFET can partly be addressed here as well. The variable gate capacitances set the gate requirement to deliver a dynamic charge during the turn-on and rapidly remove this charge to ensure a fast turn-off process. Unlike SiC VJFET, there is no requirement of providing the on-state current for the gate of SiC MOSFET, since the gate is isolated as already mentioned before.

As well as any other MOSFETs, SiC MOSFET has a parasitic body diode. Among other parasitics of the device it is worth mentioning the gate mesh resistance $R_{G,I}$ and both source and drain inductances $L_s$ and $L_d$ respectively. $R_{G,I}$ represents the resistance associated with the gate signal distribution within the device. Since it is between the driver and the input capacitor of the device, it directly impedes the switching times and the dv/dt immunity of the MOSFET. According to manufacturer the typical value of this resistance is 5 Ω [23]. All of the above mentioned parasitics have significant effect on switching speeds and consequently on switching losses of the device.

In [21] it is stated that two important characteristics need to be kept in mind when applying the SiC MOSFETs. First of all, modest transconductance requires that the gate-source voltage $V_{GS}$ needs to be 20 V to optimize performance of the device. The transconductance of the MOSFET is its small signal gain in the linear region of operation [22]. The modest

transconductance also affects the transition where the device behaves as a voltage controlled resistance to where it behaves as a voltage controlled current source as a function of $V_{DS}$. The result is that the transition occurs over higher values of $V_{DS}$ than are usually experienced with Si MOSFETs. The transconductance issue also makes it important to properly design the gate driver circuit.

The gate driver should be capable of producing a 25 V (+20 V to -5 V) swing. The recommended on-state $V_{GS}$ is +20 V and the recommended off-state $V_{GS}$ is between -2 V to -5 V.

### 2.4.3. SiC BJT

The explicit description of SiC BJT and the way to drive it will be given in section 3.6.3.

## 2.5. SiC in PV inverters

Well proven benefits of implementation of SiC transistors in PV inverters can be found in [24], [25] and [26]. In [24] development of both single-phase and three-phase inverter is realized utilizing SiC VJFETs. Inverters were designed to meet the requirements for the use of normally-off SiC VJFETs such as a low inductive layout, a bipolar gate driver circuit and output inductances with low parasitic capacitances for high switching frequencies.

Results for a single-phase inverter show a maximum efficiency of above 99 % was reached. This is 1 % to 1.5 % higher than what commercially available single-phase inverters can offer today. In addition, heatsink with forced air convection was used in this inverter. If avoiding the fan, a 2 to 3 kg heatsink would allow keeping the temperature below 80 °C at nominal power. In contrast, a passively cooled 5 kW commercial inverter has a heatsink in the range of 9 to 12 kg. This way, a weight reduction of nearly 80 % is possible with SiC transistors.

The design target for the development of the three-phase inverter was to make it highly compact, i.e. increase the power density and improve the efficiency compared to state-of-the-art inverters. It was therefore optimized for a switching frequency of 48 kHz, whereas traditional inverters operate in a 16 kHz range.

Table 2.1 shows the efficiency measurement results for inverters operated at different frequencies and employing different semiconductor devices.

**Table 2.1. Efficiencies of the three-phase inverter with 16 kHz Si IGBT and 48/144 kHz SiC VJFET**

| Switching frequency | 16 kHz IGBT | 48 kHz JFET | 144 kHz JFET |
|---|---|---|---|
| **Efficiency** | 95.33% | 96.77% | 92.93% |

Analyzing the results in Table 2.1 it can be seen that despite a three times higher switching frequency, the efficiency of inverter employing normally-off SiC VJFETs is 1,5% better than with conventional Si IGBTs operating at 16 kHz. Impressive results are achieved at a switching frequency of 144 kHz, which is 9 times higher than IGBT switching frequency of 16 kHz, showing the efficiency of 93%. Even though the result is relatively low for a PV inverter, a very compact design can be obtained with passive components greatly reduced. The final result from three-phase inverter that utilizes SiC VJFETs shows a power density of 550 W/dm$^3$, which is almost four times than for commercial inverters, and a maximum efficiency of 97.8 % at 48 kHz.

# 3. DRIVER CIRCUITS FOR SiC TRANSISTORS

## 3.1. General considerations

Traditional methods of driving silicon power MOSFETs and BJTs can be easily found in the literature. These methods are mature and widely used in the industrial applications. This is not the case with emerging SiC transistors though. Very few scientific papers on the driving methods for SiC transistors are available. According to manufacturers the intrinsic properties of SiC transistors make them extremely fast. On the other hand fast switching makes these transistors vulnerable to parasitics in the surrounding circuit. This is especially vital in the gate/base circuit. Consequently, the gate/base driver circuit must be carefully designed in order to extract the maximum performance of SiC transistors and make their appearance in the future converter design possible.

## 3.2. Driver circuit background

The primary function of a driver circuit is to turn-on/off a power semiconductor device. The turn-on/off times should be kept as short as possible in order to minimize the time the device spends in the active region where the instantaneous power dissipation is large [27]. During the on-state the driver circuit needs to provide the drive power to keep the device in the on-state with minimum possible losses. For example, the base current is needed to drive the BJT and gate-source voltage to drive the MOSFET. Negative drive power is also favourable since it helps achieving fast turn-off transition and provides a degree of protection by keeping the device off during stray transient signals. Typical gate driver circuit interface is shown in Figure 3.1.

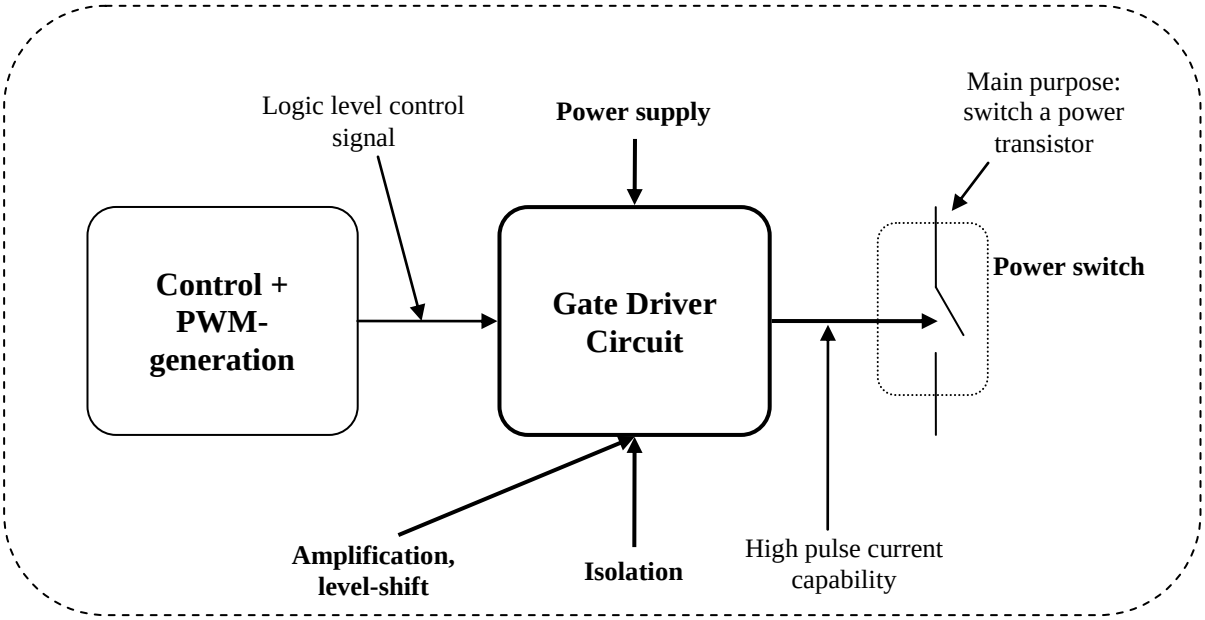



**Figure 3.1. Schematic of the gate driver circuit interface**

It can be seen that the driver circuit is the interface between the control circuit and the power switch. The driver circuit amplifies the control signals to level required to drive the power switch. It should be noted that the driver circuit is referred to the source/emitter of the power switch. If needed, an electrical isolation between the power switch and control circuit is also embedded in the driver circuit. It is worth mentioning that in some cases the driver circuit has significant power capabilities, e.g. in a case of driving the power BJTs which have fairly low beta values.

Topology of the driver circuit is mainly dependent on the application it will be used for. On the other hand, some functional considerations can be classified and are reflected in Figure 3.2.

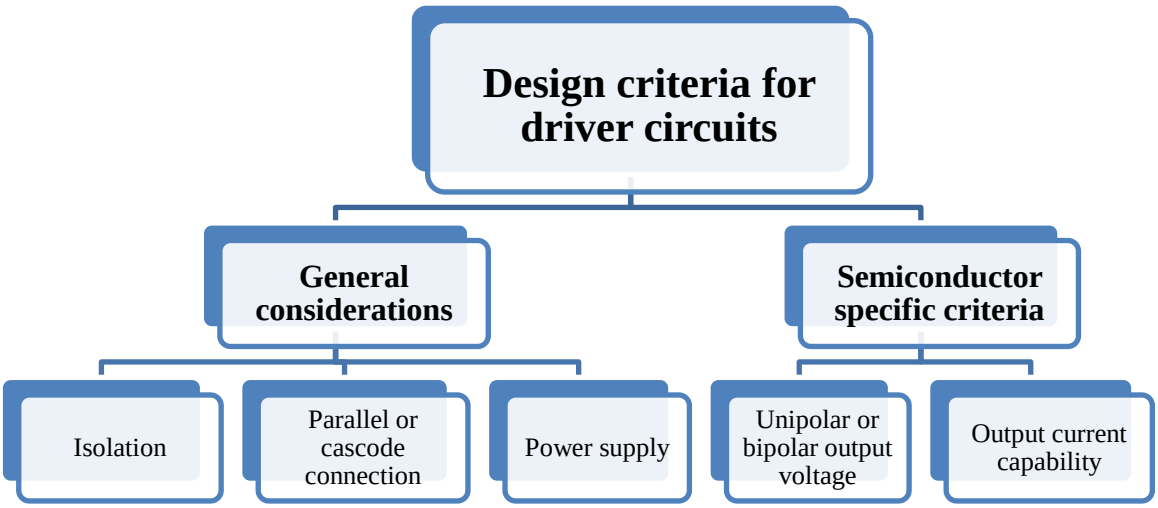



**Figure 3.2. Design criteria for driver circuits**

General design considerations include issues regarding electrical isolation, type of power supply and whether the device is in parallel or in cascode connection with the driver circuit. Care must be taken when designing the power supply for half-bridge driver, especially for the high side since it needs a so called floating power supply. Criteria which are dictated by the semiconductor device itself include the choice of driver output voltage polarity as well as output current capability (Figure 3.2). Unipolar voltages lead to less complex driver circuits. Driver circuits with unipolar output have severe drawback though, since they can only provide fast turn-on of the device. If the fast turn-off of the power switch is also of great importance, bipolar driver circuits should be considered.

Output current capability is fully dictated by the power semiconductor device being driven. Power MOSFETs, for instance, need initial high current pulse in order to turn-on and then only relatively high gate-source voltage at fairly low current needs to be sustained to keep the device in the on-state. Unlike MOSFETs, gate circuit for power BJTs must provide a relatively large output current for the duration of the BJT on-state interval. New SiC transistors have much in common with traditional devices. This mainly refers to SiC MOSFETs and SiC BJTs. One type of transistors which has recently appeared on the market is SiC VJFET. The way such transistors are driven still has some similarities with traditional transistors, but also has its own unique characteristics which make the driver circuit design fairly complex. More detailed analysis on how SiC transistors are to be driven will be given in the next sections.

Further influence on the topological details of the driver circuit can be caused by additional functionalities, e.g. overcurrent protection of power devices with error feedback, blanking times for bridge configuration or driver output wave shaping for gaining improved switching characteristics. Table 3.1 shows the different semiconductor device gate/base requirements.

**Table 3.1. Gate/base current requirements of different power semiconductor devices**

| | IGBT | MOSFET | Thyristor | GTO | IGCT | BJT | JFET |
|---|---|---|---|---|---|---|---|
| Bipolar drive | **Yes/(No)** | **(Yes)/No** | **No** | **Yes** | **Yes** | **Yes/No** | **Yes** |
| Gate/base current | **Pulses for turn on/off** | **Pulses for turn on/off** | **Pulses for turn on** | **Pulses for turn on/off** | **Pulses for turn on/off** | **On-state: cont. current** | **Pulses for turn on/off + on-state cont. current** |
| Gate current amplitude | **Relatively low** | **High** | **High** | **Turn off: high β = 3** | **Very high β = 1** | **High β = 10** | **Relatively high** |

## 3.3. Topologies

As already mentioned before the topology of the driver circuit is strongly dependent on the application it will be used for. Though the designers can still choose from many standard solutions and edit the existing topologies to suit the need of specific application. An example of a simple base driver circuit with unipolar output for converters with a single-switch topology is shown in Figure 3.3.

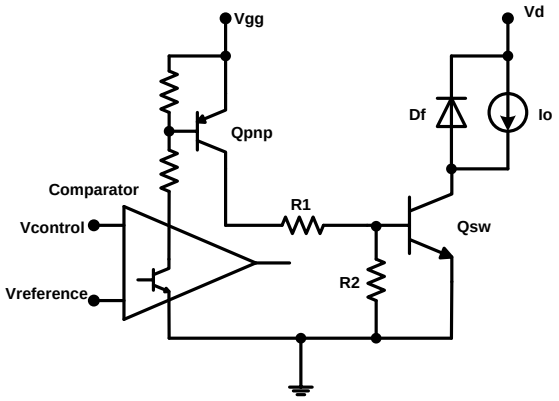



**Figure 3.3. Simple BJT driver circuit with unipolar output [27]**

Circuit operation is mainly dependent on Qpnp which provides the base current for main BJT Qsw. If the Vcontrol is higher than Vreference the comparator puts Qpnp and as a consequence the Qsw in the on-state. If the Vcontrol is lower than Vreference the comparator

puts both Qpnp and Qsw in the off-state. Values of R1 and R2 are chosen according to the desired base current of main BJT Qsw.

A MOSFET gate driver circuit is shown in Figure 3.4. It can be seen that two switches are used in a totem-pole arrangement where the comparator controls NPN-PNP totem-pole stack.

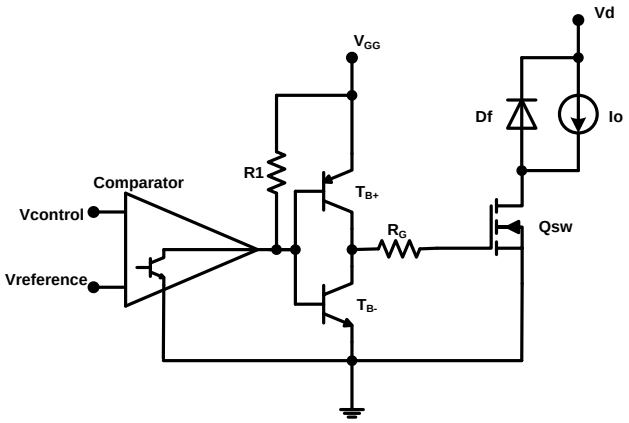



**Figure 3.4. A MOSFET gate driver circuit with a totem-pole configuration [27]**

The operation of this circuit is as follows. When the output transistor of the comparator turns off, the NPN BJT turns on thus providing positive gate voltage to the MOSFET. The gate is shorted to the source via Rg and PNP transistor during the turn-off of the MOSFET. The benefit of this circuit is that no on-state current flows through Rg thus the small value resistor can be chosen. As a result, much faster turn-on/off can be obtained. It is worth mentioning that sometimes rather than using discrete components, a buffer IC can be used instead. Many ICs are available on the market with a variety of input/output capabilities.

Unipolar driver circuits have a severe drawback due to the lack of negative drive power that can provide fast turn-off. In order to operate power semiconductor devices at high switching frequencies, driver circuit must have the ability to turn-off the device as fast as they turn-on. Driver circuits with bipolar output (either positive or negative voltage) are therefore preferred in most applications due to increased functionality and safety. Such driver circuits require negative power supply to be provided together with the positive power supply.

An example of the base driver circuit where both positive and negative voltage supply are used is shown in Figure 3.5. This circuit is capable of providing rapid turn-on and turn-off at the expense of a bit more complex circuitry and the need of negative power supply.

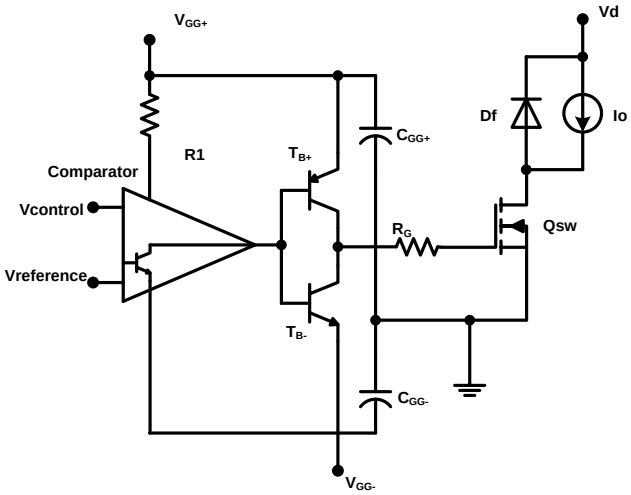



**Figure 3.5. MOSFET gate driver circuit with bipolar output [27]**

The operation of the circuit in Figure 3.5 will not be covered in details since it resembles the procedure mentioned for previous topologies.

## 3.4. Electrical isolation

An electrical isolation is often needed between the control circuit and the driver circuit. This is mainly referred to bridge applications where emitter-potential of upper switches is dependent on state of lower switches, while emitter-potential of lower switches is fixed by the negative DC-rail.

The basic ways to provide electrical isolation are either by use of optocouplers or transformers. In other words, the gate signal can be isolated optically or magnetically. In newer applications fiber optics can be used instead of otpocouplers. A brief comparison of different ways of electrical isolation in driver circuits with highlighted benefits and drawbacks can be found in Figure 3.6.

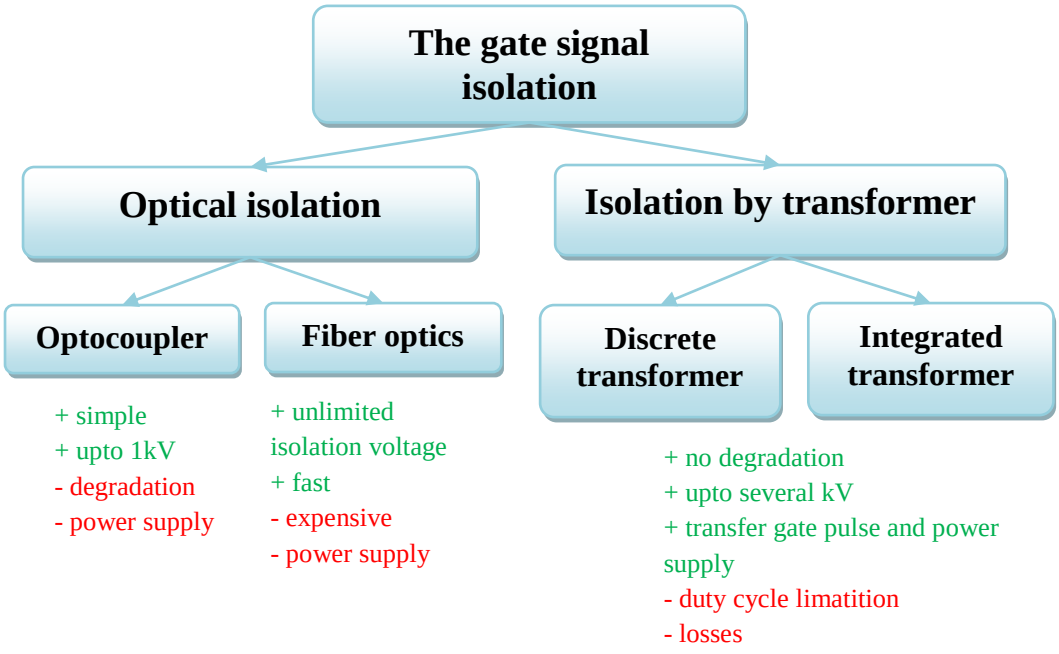



**Figure 3.6. Types of gate signal isolation**

It can be observed that optocouplers represent relatively safe isolation method. As an alternative, fiber optic cables can be used to provide very high electrical isolation and creepage distance [27], but in expense of high cost. The drawback of both isolation methods is the need of power supply.

Figure 3.7 shows a basic construction of optocoupler. It consists of a light-emitting diode (LED), the output photo transistor, and a built-in Schmitt trigger. The output of the Schmitt trigger, which in turn is the output of the optocoupler can be used as the control signal to the driver circuit.

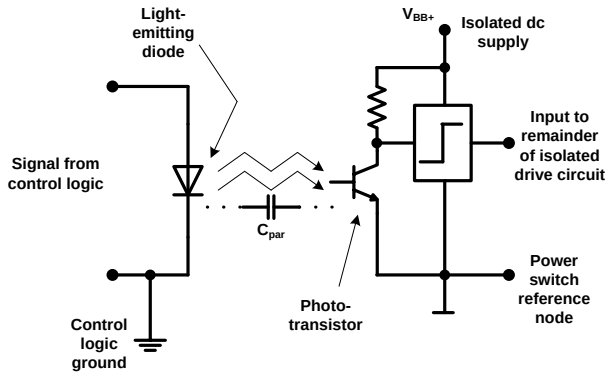



**Figure 3.7. Schematic of an optocoupler used to couple signals to a floating (electrically isolated) driver circuit [27]**

An important aspect of an optocoupler is the parasitic capacitance between the sender light-emitting diode and the photo transistor seen in Figure 3.7. The switching and high change

in voltage (dV/dt) occurs when the photo transistor turns on. This means that the current appears in this capacitance as a negative base current and turn-off the photo transistor. Thus the internal photo transistor is sensitive to be turned off by the current through the parasitic capacitance. This effect can be minimized though by means of special screens that increase the immunity of the optocoupler. An example of the application of optocoupler isolators in the gate driver circuitry is found in Figure 3.8.

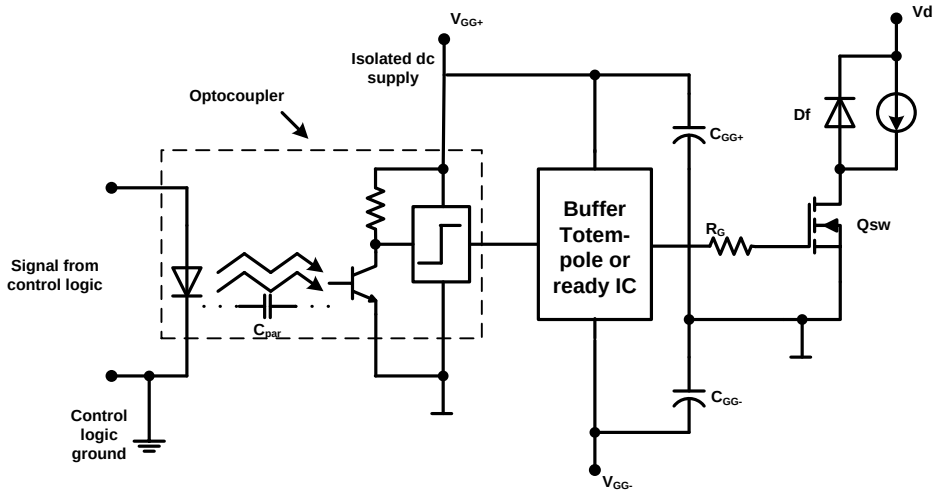



**Figure 3.8. An optocoupler isolated driver circuit for driving power MOSFETs and BJTs.**

The circuit in Figure 3.8 uses a high common-mode noise immunity optocoupler (HCPL-4503) and a high-speed driver (IXDL4425) which has the 3 A output capability [27]. With this configuration the largest power MOSFETs and BJTs can be driven. The gate driver circuit provides a +/- 15 V output voltage for high noise immunity and fast switching of power semiconductor devices.

Transformer isolated driver circuits add more flexibility to the overall design process. A basic schematic of transformer isolated driver is shown in Figure 3.9.

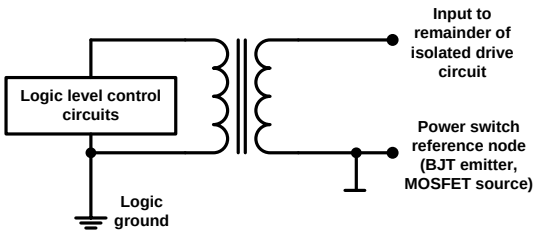



**Figure 3.9. Transformer coupling of control signals from control circuit to electrically isolated driver circuit**

Same transformer used to transfer the control signal can be used to provide the isolated dc power supply. An example of the above said is the circuit shown in Figure 3.10.

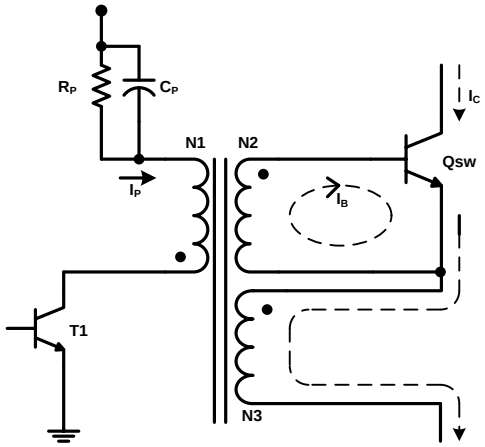



Figure 3.10. Proportional "flyback" BJT base driver [27]

Here, the base current is made to be proportional to the collector current. This way the need for an auxiliary dc power supply with respect to emitter terminal is avoided. Though, these circuits suffer from duty ratio limitations and are rather used in low switching frequency applications.

## 3.5. Power supply

### 3.5.1. Bootstrap

Power supply is a very important part of every driver circuit and should be carefully planned and dimensioned. Perhaps the least complex solution for isolated power supply for use with optocouplers is the "bootstrap-supply" shown in Figure 3.11.

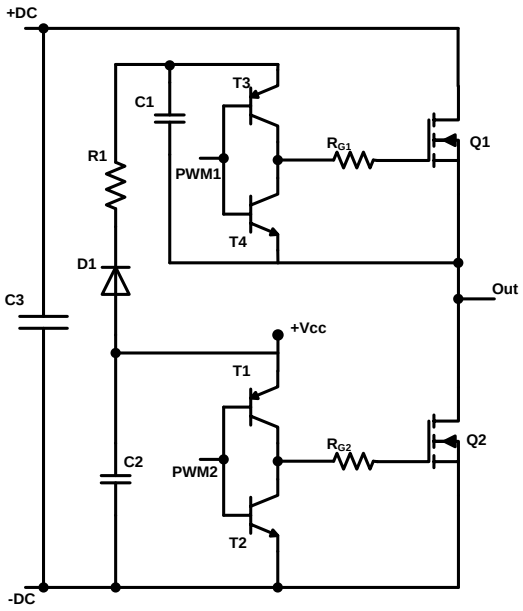



Figure 3.11. An example of isolated power supply for bridge configurations

The bootstrap capacitor, totem-pole driver and the gate resistor are the floating, source-referenced parts of the bootstrap arrangement. The benefit with this configuration is that both the low-side and the high-side can be fed through single power supply. In addition, this is a simple and cheap solution. The drawbacks of this technique are limitation in the duty cycle range as well as that on-time of switches is limited by choice of the buffering capacitors [28].

### 3.5.2. Charge-pump

Figure 3.12 shows how a charge pump creates a higher Vcc to be used for the driver IC for the high-side transistors.

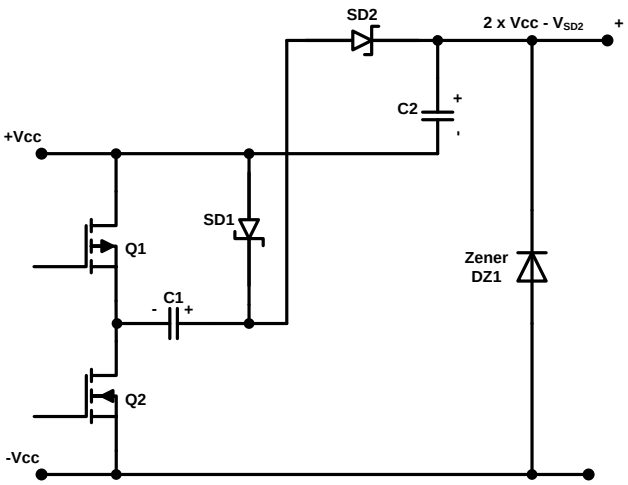



**Figure 3.12. Charge-pump power supply configuration**

Here the pair of N-Channel and P-Channel MOSFETs acts as switches, alternately connecting incoming supply voltage to output through capacitors and Schottky diodes, isolating it and almost doubling it [28].

## 3.6. SemiSouth, CREE and TranSiC driver circuit solutions for SiC transistors

### 3.6.1. SemiSouth isolated SiC VJFET gate driver

The SGDR600P1 gate driver from SemiSouth in Figure 3.13 is a two-stage DC-coupled gate driver optimized for switching SJEP120R050 and SJEP120R063 normally-off SiC VJFETs. Gate driver provides a peak output current of +6/-3 A for fast turn-on/off transients which lead to reduced switching energy losses [29]. A simple schematic of the driver circuit is seen in Figure 3.14. A more detailed schematic of driver circuit can be found in Appendix A.

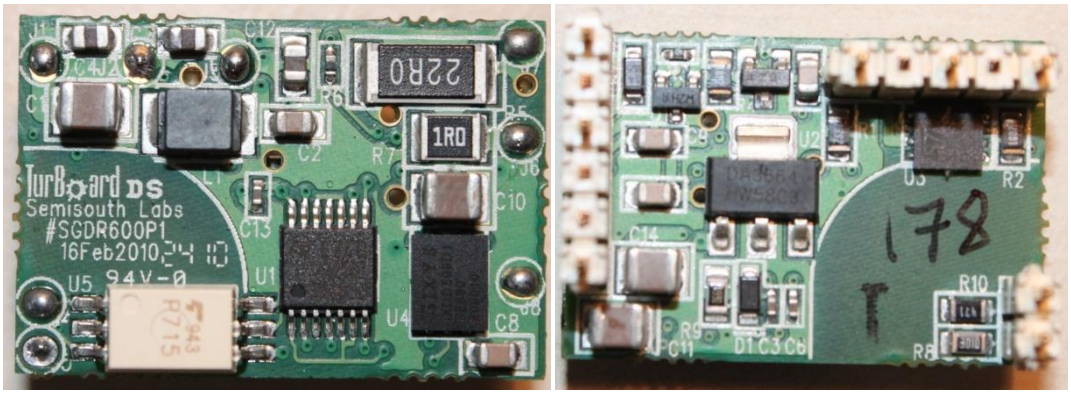



Figure 3.13. SGDR600P1 Gate driver layout. Left: top. Right: bottom [29]

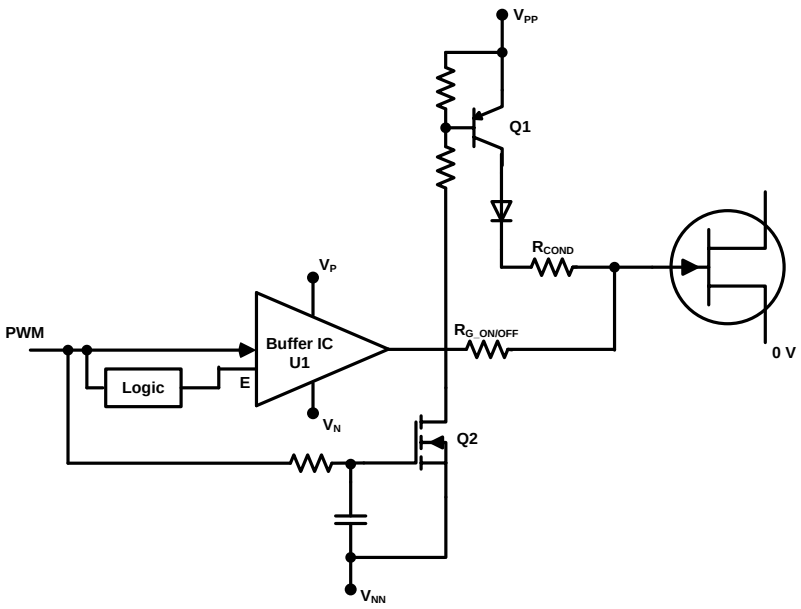



Figure 3.14. Two-stage gate driver circuit schematic

The driver is designed to first apply a high peak current pulse for supplying the required gate charge as quickly as possible for a rapid turn-on. Then secondly maintain the steady state dc

gate voltage/current to sustain low loss conduction [19]. It is recommended to overdrive the gate during the turn-on transient in order to reduce the transition time and as a consequence the losses. The overdrive time must be limited though since excessive power loss will be dissipated by the gate and could result in damage to the gate if this duration lasts longer than 100 ns. With this taken into account, the driver allows for precise control of the overdrive conditions as well as the steady state condition.

The circuit of Figure 3.14 accepts a single PWM control signal and generates a second PWM signal that synchronized with the original control signal but has a much shorter pulse width. The generated pulse is supplied to the "Enable" pin of the driver IC thus activating a first turn-on stage which controls delivery of dynamic gate charge. The original control pulse is applied to the gate of a low power MOSFET Q2, which in turn activates the second turn-on stage via a PNP transistor Q1. Q1 supplies the necessary steady state dc gate current required to maintain conduction. Current limiting resistor $R_{COND}$ is sized to set the desired forward gate current $I_{GFWD}$ while stepping down the voltage from the positive rail voltage to that required by the gate of the VJFET. The turn-off is provided by the driver IC, which has the sinking ability.

This design uses a Toshiba high-speed optocoupler which makes fast operation possible while providing sufficient layout spacing to meet safety precautions. Buffer IC from IXYS is used to achieve high-current turn-on/off pulses through Rg. The low current conduction stage uses 15 V – 6 V step-down dc-dc converter as the power source for Q1 thus gaining a reduction in gate power loss. Q1 is a small PNP transistor dimensioned to provide approximately 140 mA on-state gate current to maintain low $R_{ds(on)}$. Timing logic is specifically set to limit the high turn-on/off current pulses to 100 ns [30]. The gate driver is capable of providing a 30 V gate voltage swing, i.e. from -15 V to +15 V.

Typical gate voltage/current waveforms can be observed in Figure 3.15.

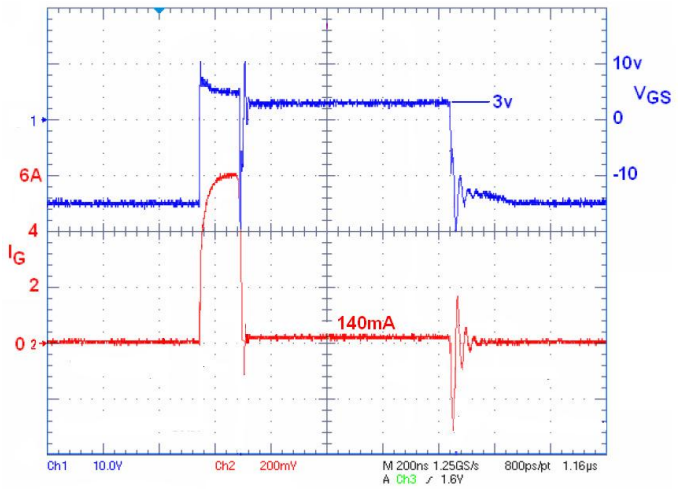



**Figure 3.15. Two-stage gate driver voltage/current output waveforms [29]**

Observing the waveforms in Figure 3.15 one can clearly mention the margin between two stages of the gate driver circuit. First driver stage provides a high current peak (up to 6 A) in order to quickly charge the gate capacitance. The second stage takes over with a fairly low on-state current in a range of 140 mA depending on the gate resistor value. This low current is sustained in order to maintain a low $R_{ds(on)}$ while keeping the gate power loss to a reasonably low level. The on-state gate voltage is kept at 3 V level, but this voltage is increased during the turn-on transient and can reach up to 10 V. It is worth mentioning that the gate of SiC VJFET must be supplied with some portion of current in order to keep the internal gate-source diode forward biased.

This driver approach can be realized in many other ways though. For example, using discrete transistors (Figure 3.16), multiple driver ICs, or a single dual driver IC (Figure 3.17). The method chosen will depend upon the required driver voltages, transition times, and desired peak current capability.

A way to realize the two stage driver circuit without employing driver ICs is shown in Figure 3.16. Three different MOSFETs are used to deliver the proper voltage/current needed by the gate of the SiC VJFET. Here, a common PWM signal is used and a second PWM signal that synchronized with the original control signal is generated. In this case S1 delivers the dynamic charge and S2 provides the on-state conduction current. S3 pulls the gate low through a low ohm pull-down resistor R3 during the turn-off.

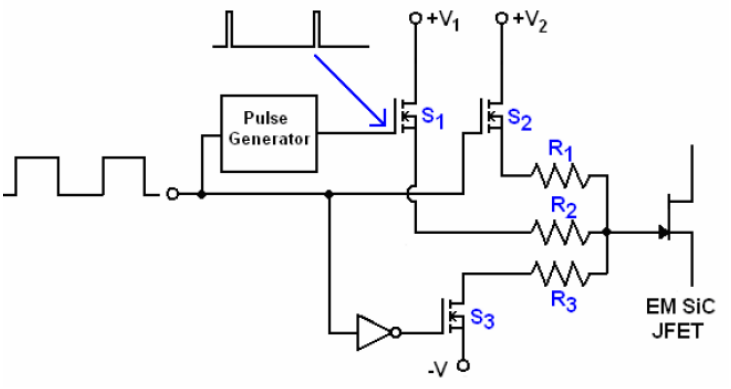



Figure 3.16. DC-coupled, two-stage gate driver for driving SiC VJFETs [19]

Another driver design approach is to use dual driver IC. In the Figure 3.17, IXYS IXDI404 for driving a SJEP120R063 is used. In this circuit driver A controls the dynamic charge delivery conditions while driver B controls the steady state gate conditions. The pulse width should not exceed the turn-on time of the device by more than 100 ns, since the purpose of driver A is to deliver a high peak current for charging the devices input capacitance.

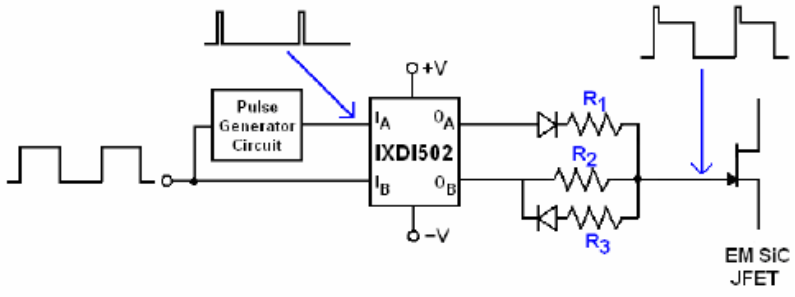



Figure 3.17. A simple, cost effective, two-stage gate driver approach using a single IXDI502 dual driver IC [19]

### 3.6.2. CREE isolated SiC MOSFET gate driver

In this chapter an implementation of an isolated gate driver suitable for testing and evaluating SiC MOSFETs in a variety of applications is described. The particular application is transistor double-pulse test board [31] made by CREE Inc. Paper is a good starting point and can be taken as a background for designing a gate driver capable of driving other SiC transistors, for example SiC VJFETs. Driver layout can be seen in figure Figure 3.18. A detailed schematic of driver circuit and the bill of materials can be found in Appendix B.

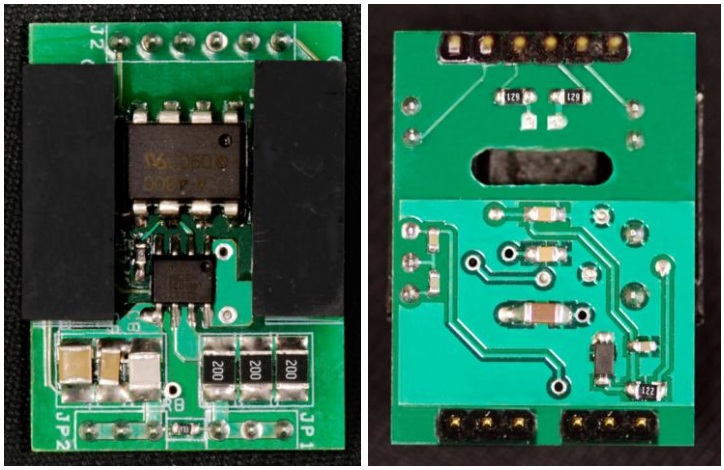


**Figure 3.18. Isolated gate driver top (left) and bottom (right) view [32]**

The circuit consists of two isolated DC-DC converters (X2 and X3), an optocoupler (U1) and the gate driver IC (U2). The IXYS IXDN409SI driver IC can provide up to 9 A of output peak current and capable of withstanding a 35 V output swing. A typical output resistance is approximately 0.8 Ω.

The ACPL-4800-300E optocoupler from Avago Technologies has been chosen due to high common mode transient immunity (30kV/μsec). Power for the circuit is provided by isolated 1W DC-DC converters. The main benefit of these converters is very low isolation capacitance. X2 is a 12V to 5V step-down converter and X3 is a 12V in, +/-12V out converter. $V_{CC}$ determines the gate pulse positive voltage and $-V_{EE}$ determines the negative gate pulse voltage. An important thing to be mentioned is that the $-V_{EE}$ node is used as the ground reference for optocoupler and the gate driver. Stray inductance minimization can be achieved by connecting capacitors C8-C10 close to the source output pin and the gate driver. This provides tight coupling between the source output terminal and the $-V_{EE}$ node.

A brief description of the operation of the gate driver is as follows. The gate terminal goes high as soon as a +10 V to +12 V pulse is applied to the optocoupler [32]. The positive gate voltage is adjusted by changing the voltage between the $V_{CC\ HIGH}$ and $V_{CC\ HIGH\ RTN}$, while the negative voltage is adjusted by varying the voltage between the $V_{CC\ LOW}$ and $V_{CC\ LOW\ RTN}$ pins. ***The voltage difference between the $V_{CC}$ and $-V_{EE}$ nodes must not exceed the maximum ratings of driver IC (U2), which is 35V.***

If a more compact design is needed the circuit can be modified. The direct connection of $V_{CC}$, source, and $-V_{EE}$ directly to external power supplies can be achieved by removing the isolated DC-DC converters. When the DC-DC converters are removed, jumpers and an additional 1k resistor are placed. The result of this change is shown in Figure 3.19.

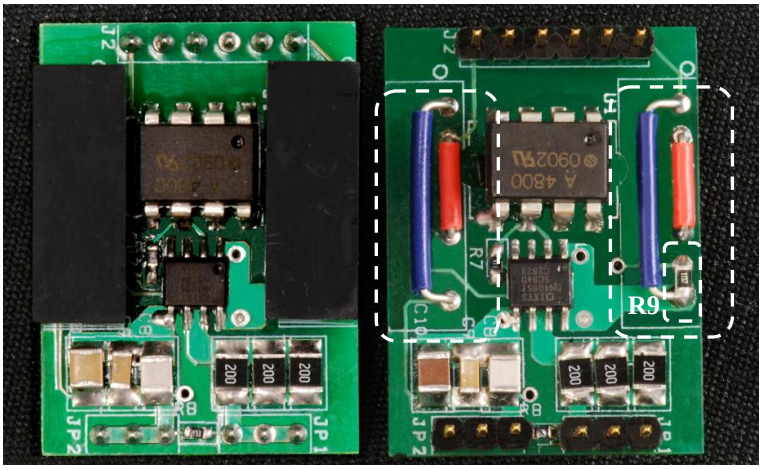



Figure 3.19. Modified (right) isolated gate driver with removed DC-DC converters [32]

### 3.6.3. TranSiC SiC BJT base driver

The AC-coupled (capacitor coupled) driver circuit design for the BitSiC BJT transistors is kept simple due to the fact that SiC BJTs do not go into deep saturation. This way a high base current can be applied, and still short turn-off times can be achieved [33]. Though simple design does not always mean lack of quality. It is still possible to make use of the benefits from fast switching. In the case of SiC BJT, there is no requirement of proportional base drive current, even though it will help improve efficiency. All these characteristics add flexibility to the design of base driver circuit for SiC BJTs. Figure 3.20 shows the schematic of base driver circuit for SiC BJTs.

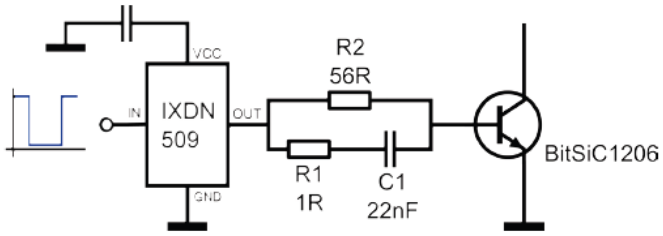



Figure 3.20. **Driver circuit for BitSiC1206 [33]**

The passive network is used in the driver circuit to set both the dc-bias (R2) and dynamic turn-on/off peak (R1 and C1) of base current. This circuit has a severe drawback of having rather low efficiency due to the power dissipation in the dc-bias resistor R2. The driver circuit was tested in a setup seen in Figure 3.21.

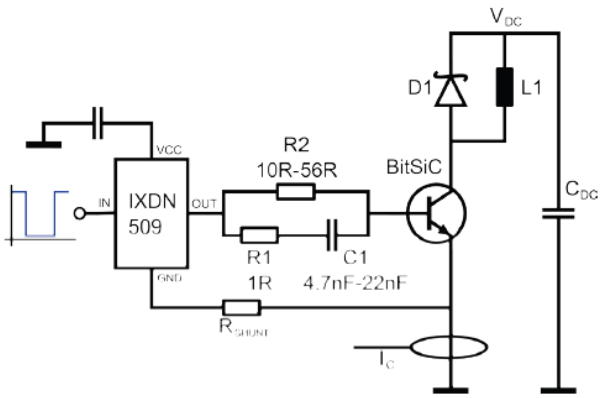



**Figure 3.21. Test setup schematic [33]**

It is a standard double-pulse test setup (or clamped inductive load setup) which helps to acquire switching waveforms of the tested transistors. The operation is as follows. First, the current in the inductance L1 is ramped up to the desired value. The transistor is then turned off, and the current circulates in the inductance and the freewheeling diode. When the transistor is turned on after a short period of time, the turn on waveform, for almost the same current, can be recorded [33]. A photograph of the setup is shown in Figure 3.22 below.

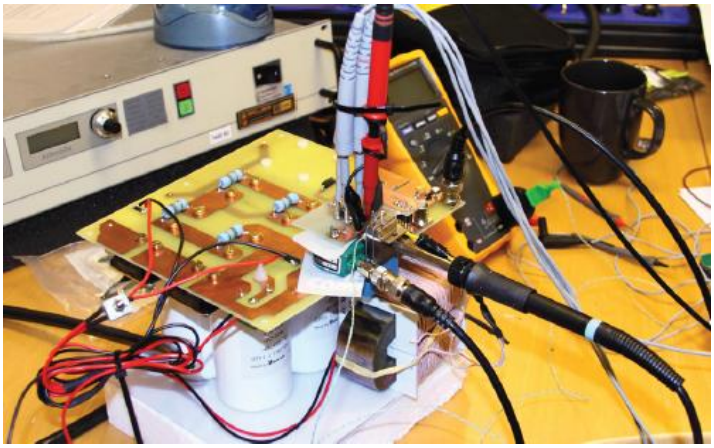


**Figure 3.22. Photograph of test setup [33]**

In order to properly dimension the base driver circuit for SiC BJT one has to take into account the gain of transistor at specific temperature. With 150 °C junction temperature kept in mind, the base current is calculated based on highest collector current and with added 50% margin. This margin is added due to the fact that overdriving the base is recommended in order to keep the transistor in the saturation region. According to the data sheet the dc gain of BitSiC1206 at 6 A and 150 ºC is 33, therefore 270 mA base current would then be needed. 20 V supply voltage to the driver IC and 3 V base collector voltage gives that 17 V will appear over the resistor. A value of 56 Ω is chosen which give roughly 300 mA.

A significant dynamic base current peak is needed during turn-on in order to charge the parasitic Miller capacitance. The current peak will also charge the base-emitter capacitance to the threshold voltage of the PN junction. The simulated waveforms of the turn-on with the driver passive network and the driver network with transistor can be observed in Figure 3.23.

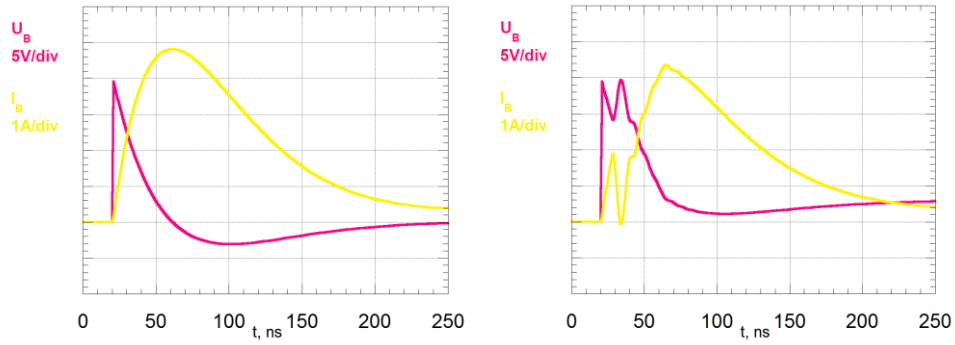



**Figure 3.23. Simulated turn-on waveforms of BitSiC1206 SiC BJT. Left: driver passive network. Right: driver network with transistor [33]**

The amount of current needed is calculated according to the base-collector charge and the voltage fall time needed. As stated in [33], the 1200 V and 6 A rated BitSiC1206 stores about 55 nC when charged to 800 V. If the desired voltage fall is 15 ns then the average current of 3.7 A is needed during the voltage fall transition. The conclusion is that the base driver circuit needs to provide both high voltage in the beginning of the turn-on process and then a relatively high current. It should be mentioned that in Figure 3.23 the output waveforms with the driver circuit connected to the base of transistor are distorted due to parasitic emitter inductance and current through the miller capacitance.

Turn-off process of the SiC BJT basically follows the same procedure. For fast turn-off a relatively high negative current supplied to the base is needed. A negative voltage spike is also beneficial in order to get the base current to rapidly change into negative direction. Fast turn-off transition is achieved if the discharge of the parasitic capacitors between base-collector and base-emitter is done rapidly. The simulated waveforms of the turn-off with the driver passive network and the driver network with transistor can be observed in Figure 3.24.

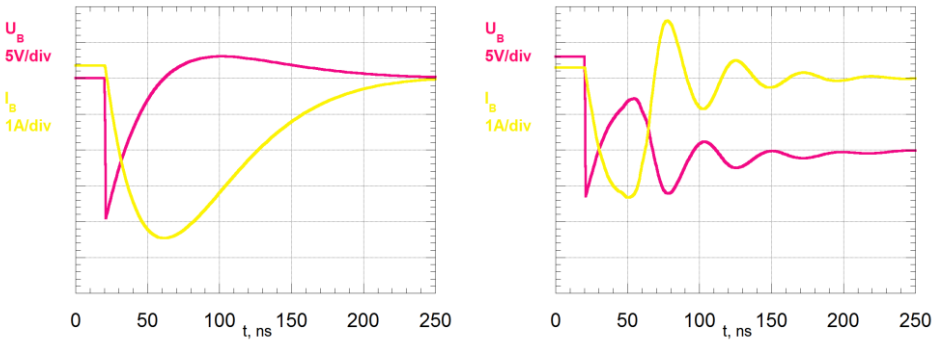



**Figure 3.24. Simulated turn-off waveforms of BitSiC1206 SiC BJT. Left: driver passive network. Right: driver network with transistor [33]**

Again, as with the turn-on case, the waveforms with transistor connected are slightly distorted. The current is dropping to zero level quite rapidly after the collector-emitter voltage has collapsed. The ringings of both the voltage and current due to parasitic circuit inductances can be observed. The full cycle of base driver switching can be observed in Figure 3.25.

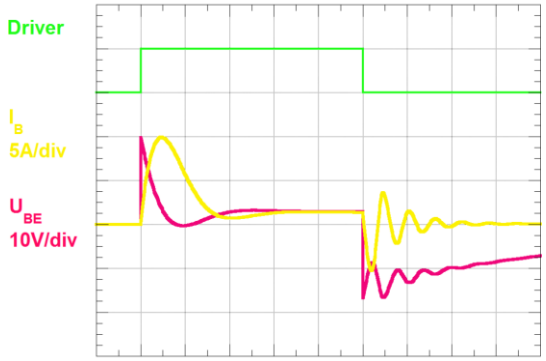



**Figure 3.25. Simulated passive driver network, base voltage and current [34]**

The driver circuit discussed in this chapter can also be used to drive SiC VJFETs. Multiple papers and application notes [35], [20], [36], [37] state that this particular gate driver may not be the most optimal solution for achieving the best possible switching speeds, but it is otherwise an effective, simple, and cost effective technique for initial evaluation of the SiC VJFET. In contrast to a power BJT, the VJFET requires very little continuous gate current during the steady conduction period, but in general all driver design considerations mentioned before are applicable to the SiC VJFET case. On the other hand, the components for the gate driver circuit have to be properly dimensioned to satisfy the specific requirements of the gate of SiC VJFET that will be addressed below. SiC VJFET switching waveforms in a double-pulse test application can be observed in Figure 3.26.

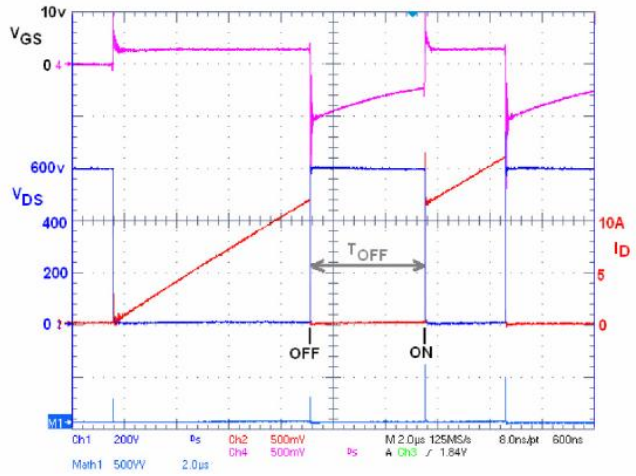



**Figure 3.26. Resulting waveforms for AC-coupled driver in single switch test circuit. VDS = 600V, ID = 12A, Unipolar driver with $R_{CL}$ = 100 Ω and $C_{BP}$ = 47 nF driving a SJEP120R125 [19]**

Here, the properly level shifted gate-source voltage $V_{gs}$ appears on top and fast switching drain-source voltage $V_{ds}$ together with the drain current $I_d$ appear in the bottom part of the Figure 3.26. The bypass capacitor swings the gate negative, making faster turn-off of the VJFET possible due to enhanced current sinking capability.

# 4. GATE DRIVER CIRCUIT DESIGN FOR NORMALLY-OFF SiC VJFET

## 4.1. Gate requirements of SiC VJFET

Manufacturers state that the unique structure of the SiC VJFET requires specific needs from the gate driver circuit if maximum performance is to be achieved [30]. In fact, designing a proper gate driver circuitry is a difficult task, unless the gate requirements and specific characteristics of the device are known. Three main operating modes of SiC VJFET are as follows:

- **On-state conduction**
- **Turn-on**
- **Turn-off**

All three modes will be addressed separately in order to make the design process discrete.

### 4.1.1. On-state requirements

Two precautions should be kept in mind when selecting the required gate voltage for SiC VJFET [30]. Like for all other voltage controlled semiconductor devices the voltage should be high enough to reach adequate channel saturation which yields lower specific on-state resistance Rds(on). On the other hand, the voltage should be limited so that the current flowing into parasitic gate-source diode is not very high that can cause excessive losses and hence destroy the device. According to datasheet [38] the threshold voltage for SJEP120R063 SiC VJFET is 1 V. It should be noted that significant drain current starts to flow only when the gate voltage exceeds this threshold value. The Rds(on) decreases until Vgs reaches 2.5 – 3 V, depending on the temperature. At this point the channel of the device is considered fully saturated and further increase in Vgs yields no Rds(on) reduction. The channel will be close to maximum saturation when the gate current is maintained at 100 mA at both 25 °C and 175 °C. Figure 4.1 shows four most important waveforms pulled out from device datasheet.

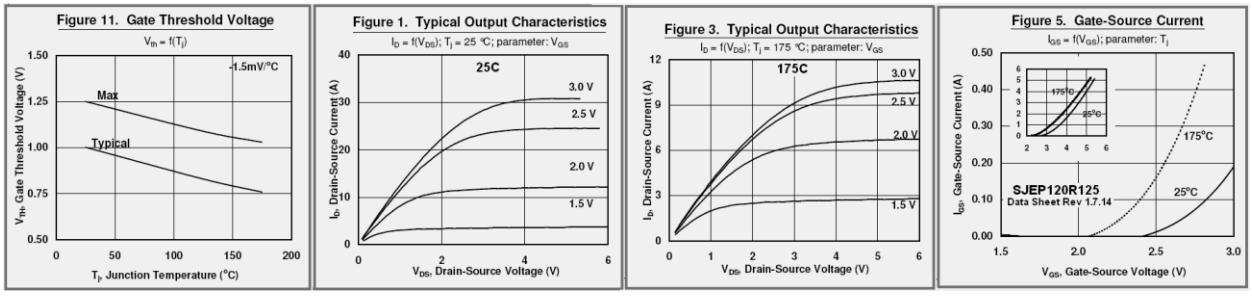



**Figure 4.1. Important SiC VJFET waveforms taken from datasheet [38]**

Two waveforms in the center show typical drain current Id vs. applied drain-source voltage Vds for various gate-source voltages. It can be seen that at 25 °C and 3 V applied at the gate the current reaches 30 A. Due to de-rating of the device this current decreases to approximately 10 A when the junction temperature is increased to 175 °C. Waveform on the left shows gate-source threshold voltage as a function of junction temperature. It can be seen that the threshold voltage decreases with increased junction temperature. Finally, waveform on the right shows the characteristics of the parasitic gate-source diode, i.e. the gate-source forward current Igs as a function of applied gate-source voltage Vgs. In this case the temperature dependence is again straightforward. It can be observed that the diode conduction threshold voltage decreases with increased temperature.

### 4.1.2. Turn-on

The turn-on of SiC VJFET is basically similar to that for MOSFET or BJT. The faster the input capacitances are charged the faster the turn-on of device [30]. Peak gate current value dictates the turn-on speed. The higher the applied gate driver voltage, the higher the gate resistance Rg is required for a given current. It is worth mentioning that the higher the Rg the higher the damping in the gate circuit, which in some applications is critical. The drawback of high Rg values is that higher losses might occur due to power dissipation in the gate resistor which limits the constant gate current needed for on-state conduction. In order to achieve a very fast turn-on, a high amplitude fast rising gate current pulse is required. This can only be possible if the gate leakage inductance Lg is low enough. Minimizing the physical distance between the gate driver and the gate of device is a reasonable solution. ***Due to fairly low gate threshold voltage of SiC VJFET any parasitic ringing in the gate circuit can result in the accidental turn-on of the device. Thus, it is important to keep the ringing in the gate minimized.***

### 4.1.3. Turn-off

The turn-off process is similar to turn-on, but in this case the faster the input capacitances are discharged, the faster the device will turn-off. In the ideal case a negative voltage in the range of -5 to -15 V is required to achieve fast turn-off transient. Low ohm current path should also be provided. The negative voltage is especially important in the bridge configuration where the switching of one transistor can cause an accidental switching of the opposite transistor. And again, the lower the gate leakage inductance the more effective the negative bias can suppress the turn-on glitches.

### 4.1.4. Summary

***Summary of gate requirements for SiC VJFET:***

- Voltage controlled gate – approximately 3 V in the on-state
- Dynamic charge during turn-on
- Removal of charge during turn-off
- Maintenance of the gate-source diode on by keeping it forward biased
- Temperature dependent gate threshold voltage – typically 1.25 V at 25 °C and reducing with increased junction temperature
- Both the gate voltage/current must be sustained to keep the device on

## 4.2. System requirements

The design of the proper gate driver circuit is not limited by only knowing the requirements of the gate of the transistor. Overall system requirements are of great importance. Figure 4.2 shows the schematic of half-bridge configuration without the main power circuit appearing since it is not related to the gate interface.

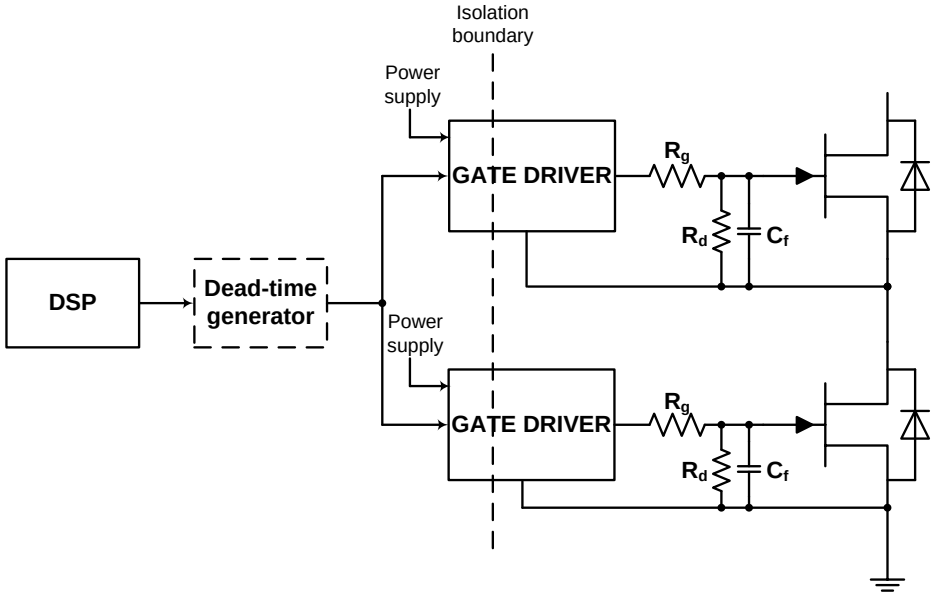



**Figure 4.2. Schematic showing main system requirements of the half-bridge configuration**

It is seen from Figure 4.2 that the dead-time generation stage is required in order to feed both low-side and high-side gate drivers with single channel DSP signal. It should be noted though that in modern power electronic converters this stage is implemented into the DSP and the dead-time is adjusted by changing the program code in the software. Isolation boundary

shows the requirement of isolating the input control signal from the power stage of the gate driver. The need for separate isolated power supplies is also highlighted. A small filter capacitor $C_f$ and damping resistor $R_d$ connected across the gate-source of the transistor in Figure 4.2 are intended to suppress oscillations and the problem of retriggering at the turn-off of the transistor.

## 4.3. Gate driver application

The gate driver circuits are usually designed for specific applications. Depending on these applications the driver has different properties and output characteristics. Gate/base requirements for different semiconductor devices were discussed in section 3.1. As a result, it is obvious that no universal gate driver exists and each driver needs to be properly tuned to fit each specific application.

The proposed two-stage gate driver circuit is designed for high frequency switches employed into PV converters discussed in chapter 2.2. High frequency operation needs significant power and speed capabilities and this has to be taken into account when dimensioning the power supply for the laboratory prototype.

## 4.4. Design implementation

The gate driver design process started with analysis of the possible driver topologies described in section 3.3. The main source of information on SiC transistor driving though is the manufacturer's application notes and manuals since very few academic papers exist so far. It should be mentioned that SiC transistors discussed in section 2.4 have recently appeared on the market and the way to drive them is still not obvious as in the case with ordinary MOSFETs and BJTs. Gate driver circuit from SemiSouth (section3.6.1) was carefully studied and analyzed and as result was taken as the base for the proposed gate driver design. Some ideas were taken from there, but the main source of design ideas came from discussion with engineers at Eltek Valere. The design procedure is split into separate stages in order to make the process of following the design fairly easy. The full schematic can be observed in Appendix E.

### 4.4.1. Power supply

In order to make the gate driver circuit suitable for use in the high-side of the bridge configuration it was decided to use isolated dc-dc converters for delivering the power supply to the board. NMS1215C isolated 2W dual output dc-dc converters were chosen due to high

efficiency and low stray capacitance values resulting in less influence on the driver board. Three sets of dc-dc converters were chosen for testing, i.e. +/- 9 V, +/- 12 V and +/- 15 V.

In order to reduce the losses in the on-state conduction current path of the gate driver the positive supply voltage was reduced to as low as +5 V by means of switch-mode dc-dc converter seen in Figure 4.3.

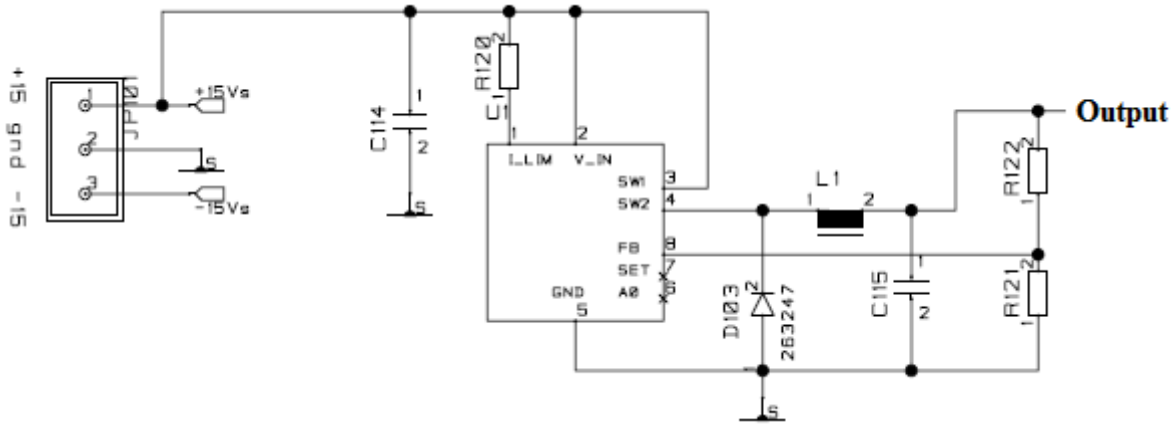



**Figure 4.3. Switch-mode dc-dc converter for power loss reduction in the on-state conduction current path**

The LT1107 from Linear technology is chosen due to relatively high efficiency and flexibility in variation of output voltage. Here, C114 is a decoupling capacitor, R120 is a current limiting resistor, the combination of L1 and C115 serves as the filter and reduces the output current and voltage ripple. LT1107 keeps the $V_{FB}$ at the internal reference voltage of 1.25 V. Resistors R121 and R122 are used to set the desired output voltage using equation (5.1):

$$V_{out} = \left(1 + \frac{R_2}{R_1}\right)(1.25\ V) \qquad (5.1)$$

***Diode D103 turns on when SW2 reaches 0.4 V below ground. D103 must be a Schottky diode, since the voltage at SW2 must never fall below –0.5 V. A silicon diode will allow SW2 to go to < –0.5 V, causing potentially destructive power dissipation inside the LT1107.***

In the early stages of the design process it was decided to take the negative voltage supply of the gate driver as the "ground" reference. As a consequence the supply voltage for the optocoupler and the logic elements was generated internally by deploying the circuit seen in Figure 4.4.

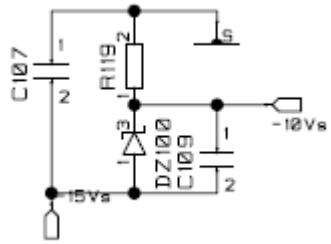



Figure 4.4. Internal discrete 5 V voltage regulator

It is a simple yet robust solution in order to obtain a 5 V supply. The 5.1 V Zener diode DZ100 is used to step down the voltage from -15 V down to -9.9 V. Thus, the difference is used to feed the optocoupler and the logic.

### 4.4.2. Galvanic isolation

It was decided to use the optocoupler to isolate the signal generation circuit from the power circuit. The schematic of the optocoupler connection circuit can be observed Figure 4.5.

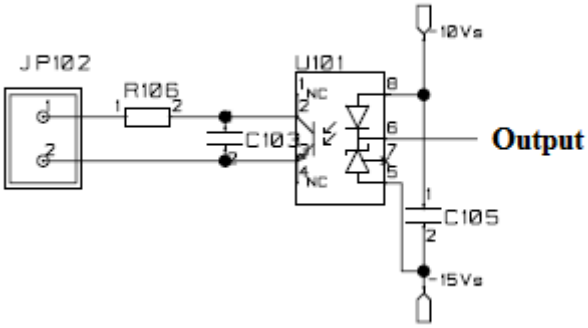



Figure 4.5. Optocoupler connection layout

Si8220 optocoupler from Silicon Labs is chosen due to far more superior qualities over similar components. The most important characteristics are high transient immunity – 30 kV/µs, high isolation voltage – 3.75 $kV_{RMS}$ and high-speed operation due to RF technology. The extended input current range from 5mA to 20 mA adds flexibility in the design process. Resistor R105 is used to match the output of the control electronics to the input needs of the optocoupler. C103 is an optional filter capacitor and C105 is used to stabilize the supply voltage for the optocoupler.

### 4.4.3. Logic circuits

The SN74AHC02 quadruple 2-input positive-NOR gate IC from Texas Instruments is used as main logic component. The logic/timing gates have two functions. Gates U104 B and C

together with some more additional components in Figure 4.6 are used to generate a very short approximately 100 ns pulse. This pulse is synchronized with the optocoupler output signal.

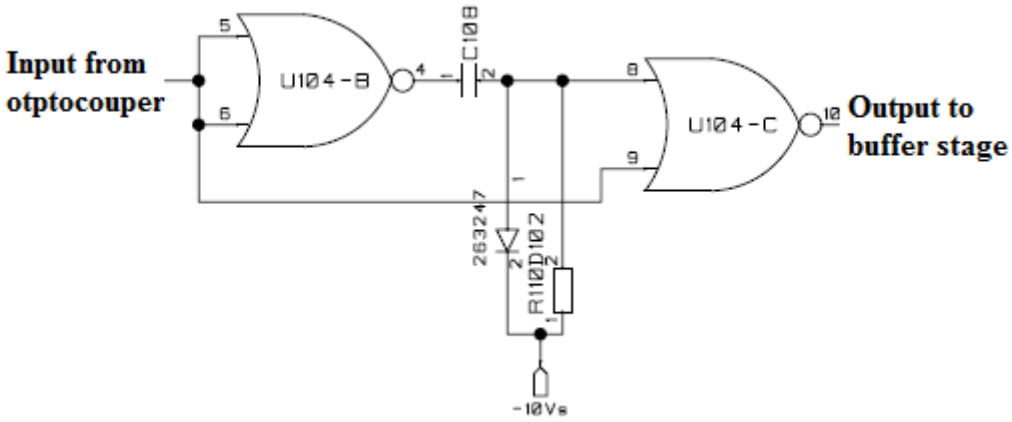



**Figure 4.6. Logic gates used to generate 100 ns turn-on pulse**

Gate U104 - A in Figure 4.7 inverts the output signal of the optocoupler in order to provide the turn-off signal for the SiC VJFET. ***Gate U104 – D is not used. The unused gates should always be connected to ground. Fail to do so might result in unexpected signal distortion.***

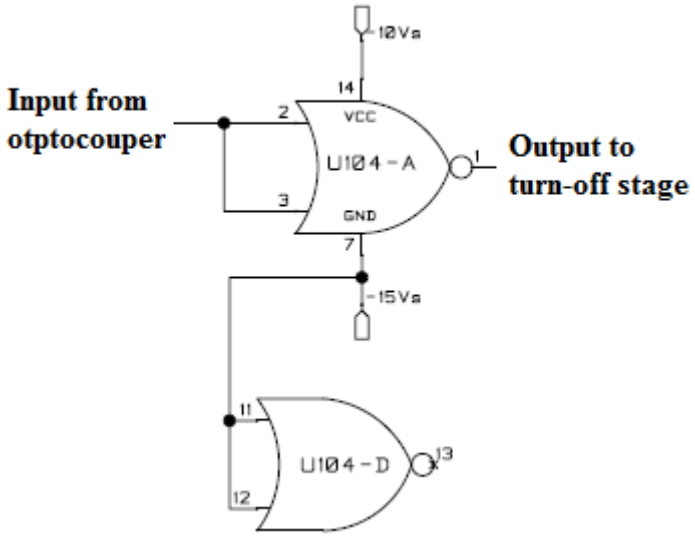



**Figure 4.7. Logic gate used to provide the adequate signal for turn-off stage**

Figure 4.7 also shows the connected voltage supply, which is 5 V.

### 4.4.4. On-state conduction stage

As discussed in section 4.1 SiC VJFET requires the on-state current in order to sustain conduction of drain current. Figure 4.8 shows the proposed solution for achieving low on-state current.

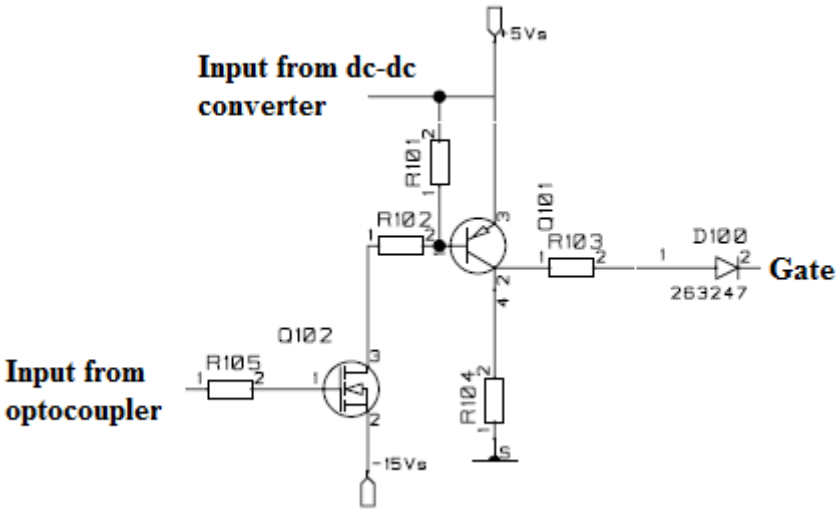



Figure 4.8. A schematic of on-state conduction stage of SiC VJFET

The +5 V voltage supply is delivered from the switch-mode dc-dc converter discussed previously. The operation is as follows. When the output of the optocoupler goes high it provides the gate voltage for small N-channel MOSFET which tends to connect the base of the PNP transistor to -15 V supply. In fact the voltage at the base drops from 5 V supplied at the emitter to approximately 4.5 V which is the main requirement in order to properly bias the PNP transistor. This way low current conduction is sustained. When the output of the optocoupler goes low the MOSFET turns off and the base-emitter voltage difference decreases, and as a consequence the PNP transistor turns off. The diode D100 is used to block the current sinking path during the turn-off of SiC VJFET. R103 is the current limiting resistor used to set the on-state conduction current point. Resistor R104 is optional and is used to pull the collector voltage to ground when the PNP transistor is in the off-state.

### 4.4.5. Buffer stage (IC and discrete components)

Buffer stage selection was one of the main issues of the design process and the first question to answer was whether to use the commercial IC or discrete components. As the trade-off was not found it was decided to make both stages appear on the board with an option of connecting either one or another.

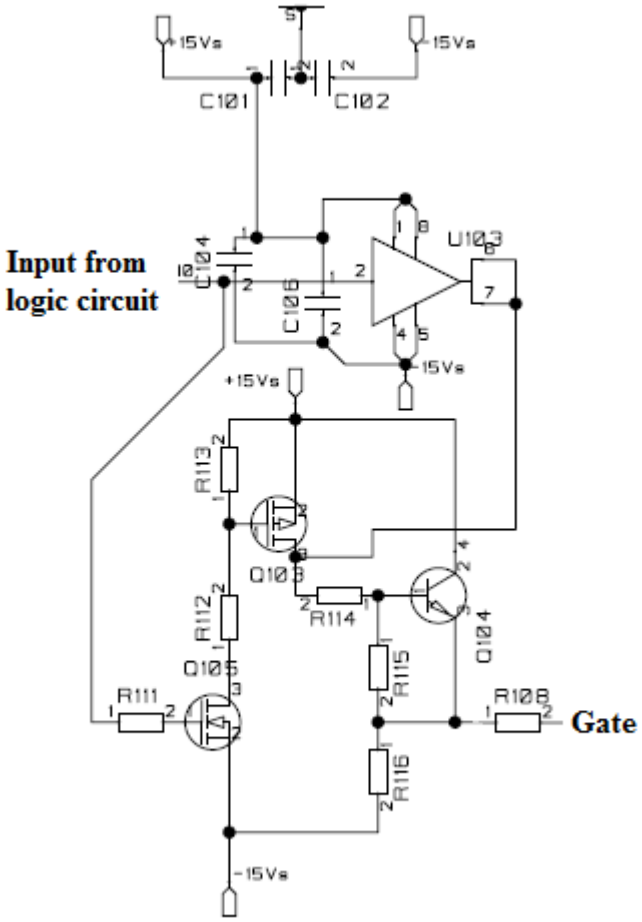



Figure 4.9. Schematic of the buffer stage

The result of such combination is shown in Figure 4.9. Here, U103 is a commercial IC, whereas Q103 and Q105 are used as discrete solution. It should be noted that both stages deliver the base current for NPN transistor Q104 which in turn delivers the dynamic current peak for fast turn-on. R108 is the external gate resistor with the value of 1 Ω since low ohm path is needed for the peak turn-on current. The resistors R111 – R116 are chosen according to the biasing rules for transistors. R114 is the current limiting resistor for the base of NPN transistor Q104. The decoupling capacitors C104 and C106 used across the $+V_P$ and $-V_N$ supply voltages of the driver IC are located close to the driver in order to protect it from overvoltages. ***The gate driver IC or transistors must be rated for more than sum of the positive turn-on voltage and negative turn-off voltage.***

### 4.4.6. Turn-off stage

Since the current sinking capability of the buffer IC is not utilized it was decided to implement a separate circuit that is capable to pull the gate low in order to achieve fast turn-off transition. The schematic can be observed in Figure 4.10.

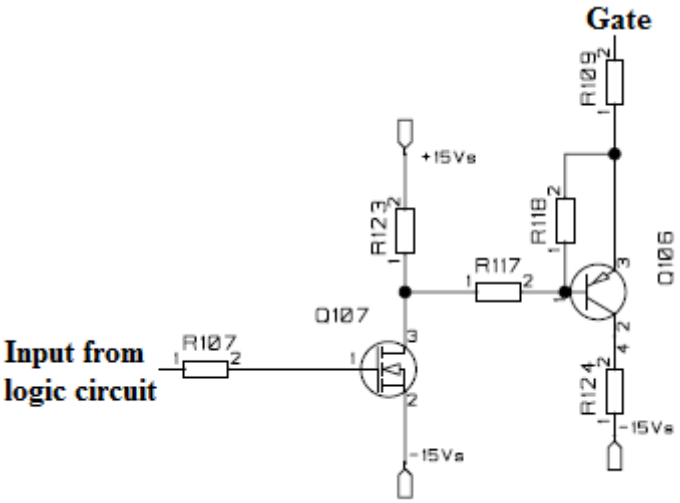



Figure 4.10. Turn-off stage of SiC VJFET

The idea behind this solution resembles the on-state conduction stage with the same combination of low power MOSFET Q107 and PNP BJT transistor Q106. The specific difference of this circuit is that the input to the MOSFET is provided by logic which inverts the optocoupler signal. This means that the turn-on and turn-off signals are complementary. Resistor R123 is optional and is used to speed-up the transition from the turn-off to the turn-on of SiC VJFET.

## 4.5. Gate driver PCB layout

Together with the PCB designer at Eltek Valere the proposed gate driver circuit design procedure was implemented into a board seen in Figure 4.11. And again, many valuable ideas came from discussions held with the colleagues and engineers at Eltek Valere. It is a four layer PCB with inner layers dedicated to different voltage level planes.

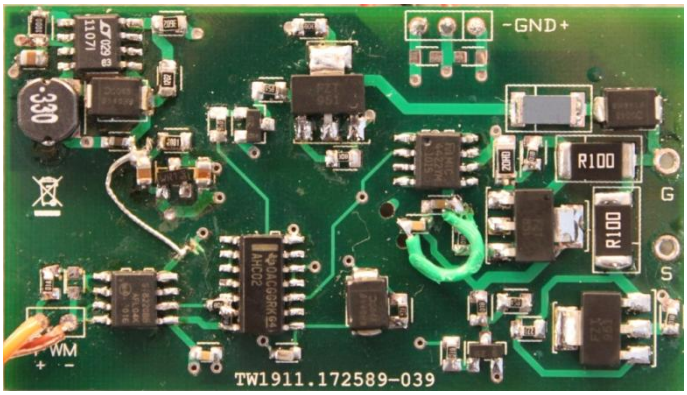



Figure 4.11. Proposed gate driver board photograph

The board shown is a fully assembled gate driver with the components put in places. The component mounting procedure of the gate driver was made step-by-step so that all the errors on the way to a complete circuit could be corrected as soon as they appear. Some modifications during the soldering process were made and these modifications can also be observed in Figure 4.11.

# 5. SIMULATION RESULTS

## 5.1. General information about LTspice

LTspice (Linear Techology Simulation Program with Integrated Circuit Emphasis) is the software used in the master thesis. It is based on Spice 3 platform [39]. LTspice is a free software and can be downloaded from Linear Technology's website [40]. It is released for engineers that develop electronic circuits to assist planning, development and rapid prototyping of new components. The program has a rich component library that mainly consists of Linear Technology's own manufactured components. The library can be extended though by importing the ordinary Spice models that are available on most of the manufacturer's websites. It should be noted that minor changes have to be made in order to adopt the models for LTspice environment. To find extra libraries and simulation files reader is referred to Yahoo group dedicated to LTspice [41].

## 5.2. Planning of simulation

The simulations are based on the case which will further be used for the laboratory prototype. This makes a consistency of the obtained results as well as the simulations will probably enlighten problematic areas of the design that might be worth to know prior to beginning the laboratory testing. The main aim of simulations is to try different ideas and solutions but still stick to the design discussed in section 4.4. Models used in the simulations were partly imported due to specific needs of the gate driver circuit being developed.

A step-by-step simulation process is chosen in order to trace all the problems on the way to the final simulation. In other words, the proposed gate driver circuit will be divided into many functional parts and these parts will be simulated separately to test the overall functionality. Then according to results obtained the parts are to be connected to make a complete circuit.

## 5.3. LTspice simulation results

The power supply for the gate driver circuit was extensively simulated as it is considered as the vital part of the design with relatively high error probability. The switch-mode dc-dc converter seen in Figure 5.1 was the biggest concern since many external components had to be

considered. Following the design procedure in [42] the converter was tuned to provide a fixed 5 V output.

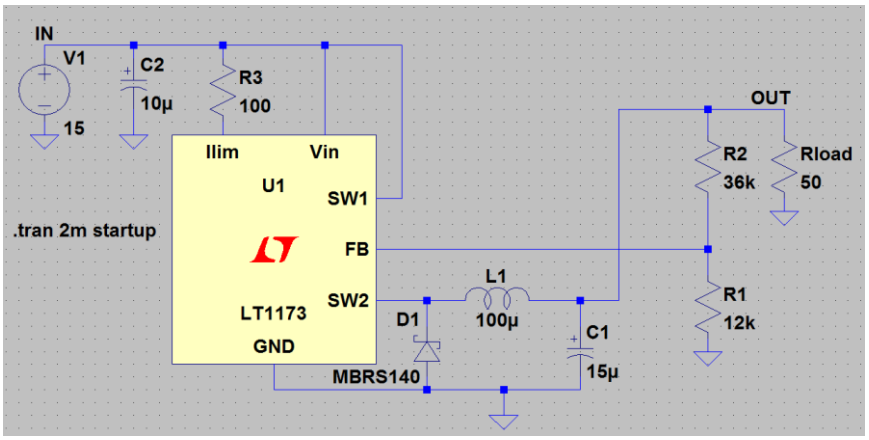



Figure 5.1. Simulated switch-mode dc-dc converter

Results for this converter operating in step-down mode can be observed in Figure 5.2.

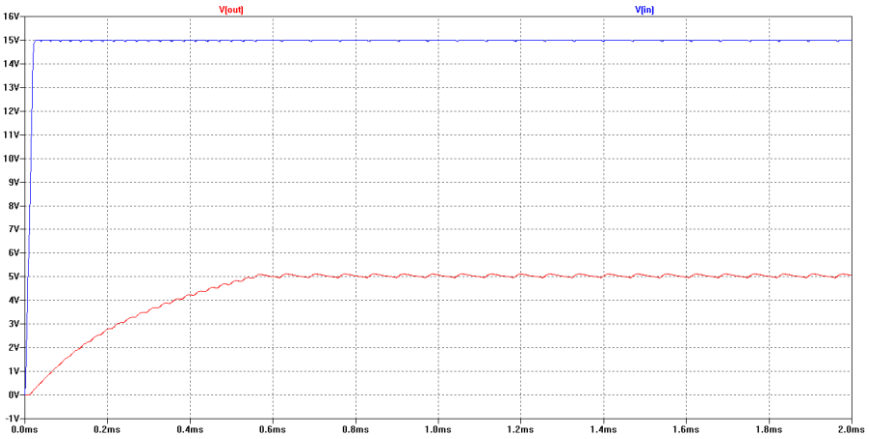



Figure 5.2. Switch-mode dc-dc converter simulated output voltage

It can be seen that the +15 V input is chopped down to form a fixed +5 V output. Selection of proper values for output inductor L1 and capacitor C1 gives relatively low output ripple.

Circuit seen in Figure 5.3 is the discrete 5 V voltage regulator discussed in section 4.4.1. The 5.1 V Zener diode D1 is used to step down the voltage from -15 V to -9.9 V. The difference is used to supply both the optocoupler and the logic.

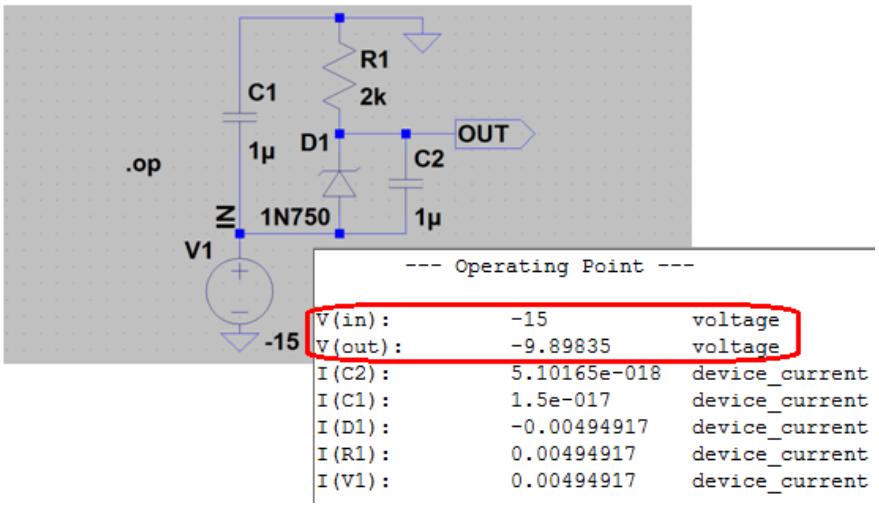



Figure 5.3. Simulated discrete 5 V voltage regulator

The optocoupler interface with the input control signal on the primary side and the output on the secondary side can be observed in Figure 5.4.

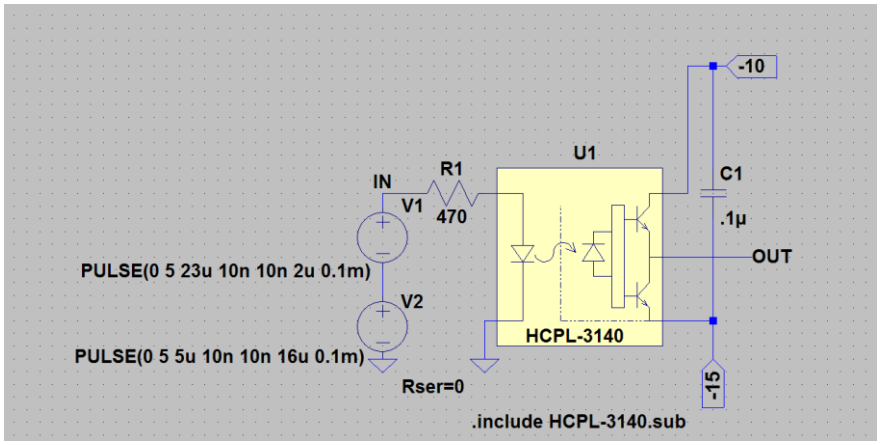



Figure 5.4. Simulated optocoupler with control signal input on the left

Series connected voltage supplies V1 and V2 generate the required control signal. Resistor R1 limits the supply current to the optocoupler to match the allowed input range. ***The model of the optocoupler used is different from the one described in section 4.4 due to unavailability of the required model. It should be noted though that both optocouplers have similar characteristics and only minor difference are present.*** The waveforms of the input/output of the optocoupler are shown in Figure 5.5.

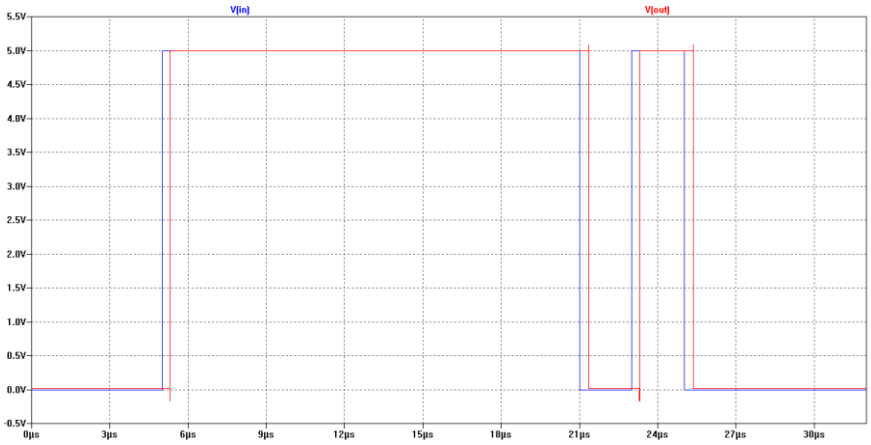



**Figure 5.5. Input vs. output waveforms of the optocoupler**

As expected the output follows the input with a minor time delay. ***All the delays of the system should be taken into account in order to properly bias the gate. Both the buffer stage and the on-state conduction stage should be activated at the same time.***

Figure 5.6 shows the simulated logic elements that provide input signal either for the buffer stage or the turn-off stage of the SiC VJFET. The input signal for both parts is the same and is delivered from the output of the optocoupler.

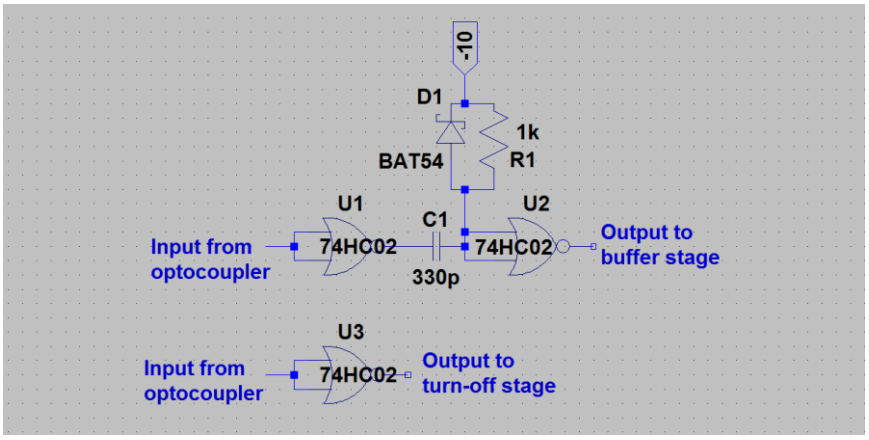



**Figure 5.6. Simulated logic gate circuit**

The logic output waveforms can be observed in Figure 5.7.

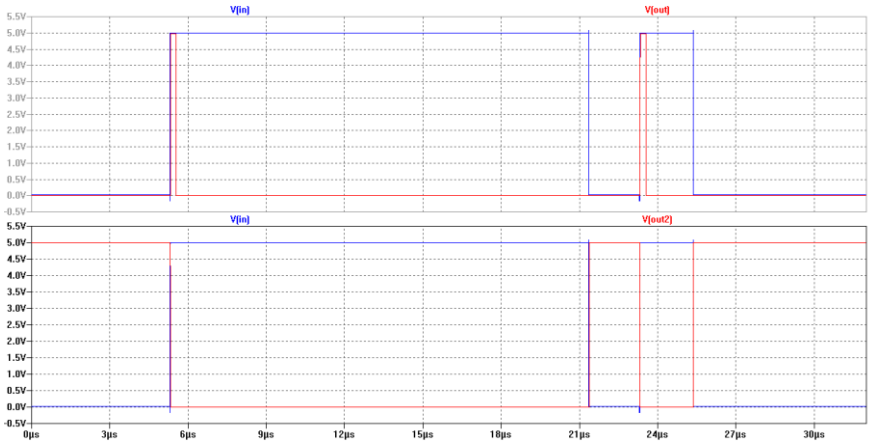



**Figure 5.7. Simulation results for logic circuit**

Here, the upper waveforms show the input/output of the logic related to the buffer stage, while lower waveforms show the input/output of the logic related to the turn-off stage. Analyzing the waveforms reveals that the signal for the buffer stage is synchronized with the input control signal but only stays on for a fraction of the total on-time period, i.e. 100 ns. The logic for the turn-off stage inverts the control signal.

As already discussed in section 4.4 the proposed gate driver circuit consists of two stages, i.e. buffer stage and the on-state conduction stage. In fact three stages can be distinguished adding also the turn-off of the SiC VJFET. The circuit in Figure 5.8 is the simulated on-state stage of the gate driver.

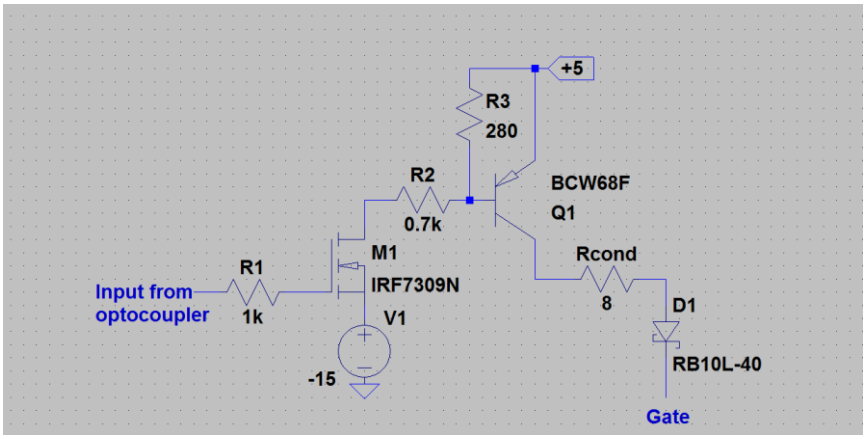



**Figure 5.8. Simulated on-state conduction stage of the SiC VJFET**

The operation will not be covered in this section since it has already been discussed in section 4.4.4. The +5 V are delivered from the switch-mode dc-dc converter to reduce the power losses of this stage. Resistors R2 and R3 were chosen to bias the PNP transistor. The simulation results for this stage can be observed in Figure 5.9.

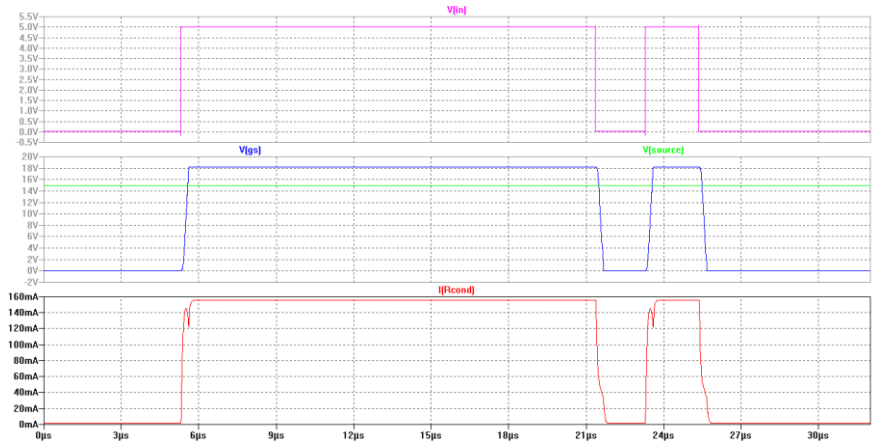



**Figure 5.9. Simulation results for the on-state conduction stage**

The waveforms are (from top to bottom) the control signal, gate-source voltage Vgs and on-state gate current Ig respectively. It is seen that in this case the gate requirements are fulfilled by achieving 3 V and 160 mA at on-state. ***On the Vgs waveform the source potential appears as the green line which represents the "ground" level. Seen from there, the lower level of Vgs (which appears as the 0 V) is actually -15 V. This is done due to limitation of the software that does not allow making the negative voltage appear as the reference.***

Figure 5.10 shows the most important part of the gate driver that is responsible for reducing the switching losses by delivering the required gate charge for fast-turn-on.

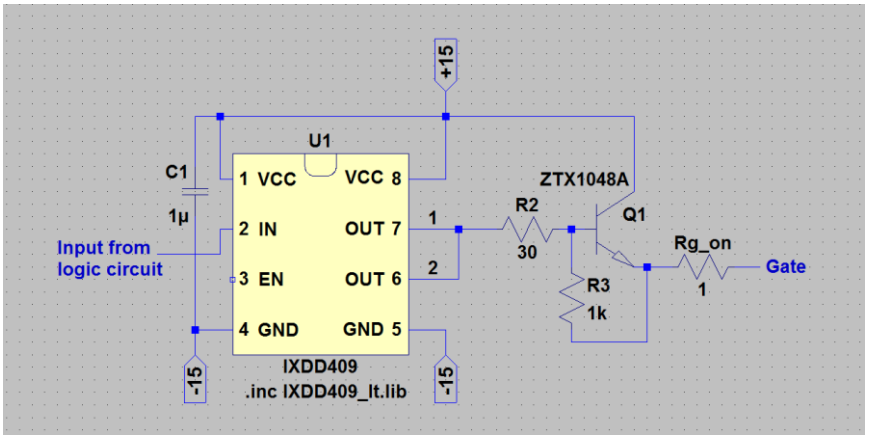



**Figure 5.10. Simulated buffer stage of the SiC VJFET**

Here, the buffer IC delivers the base current for middle power NPN transistor which in turn delivers the required charge for the gate. By placing the transistor between the IC and the gate the sinking capability of the buffer is dismissed. Thus the sinking is provided by a separate circuit that will be discussed in the upcoming section. ***The buffer IC is different from the one***

***used in the design process due to availability and functionality of the current Spice model.*** The output waveforms for the buffer stage can be observed in Figure 5.11.

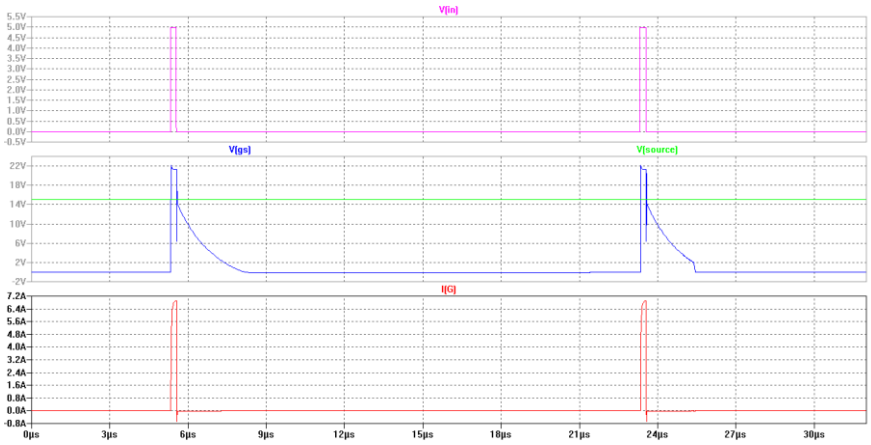



**Figure 5.11. Simulation results for the buffer stage**

The waveforms are (from top to bottom) the control signal, gate-source voltage Vgs and turn-on peak gate current Ig respectively. The gate current waveform shows the peak current reaching more than 6 A and appears only for 100 ns in order to provide rapid turn-on of the SiC VJFET. Vgs is reaching the peak value of 7 V with respect to the source potential. Strange exponential behaviour of Vgs should be noted at the instant when the buffer stage is disconnected. Lastly, Figure 5.12 shows the circuit that is used to pull the gate low during the turn-off process.

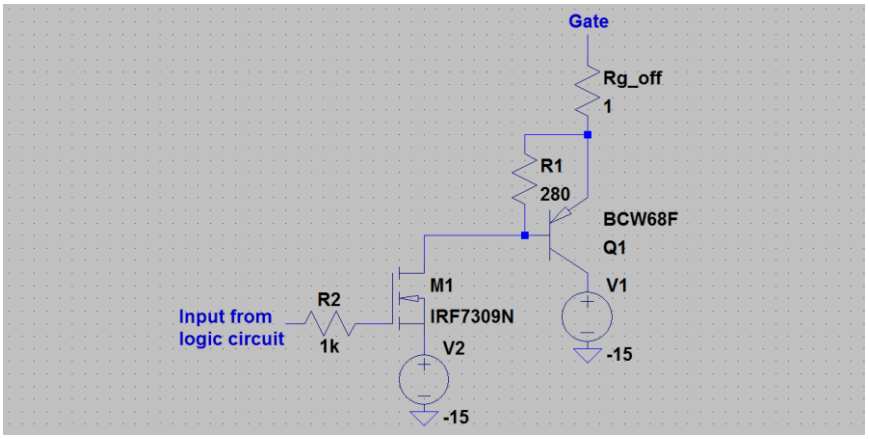



**Figure 5.12. Simulated turn-off stage of the SiC VJFET**

It was not possible to simulate this stage separately from two other stages and consequently the simulation result is not shown. The complete circuit of the gate driver can be found in Appendix C, but the resultant waveforms can be observed in Figure 5.13.

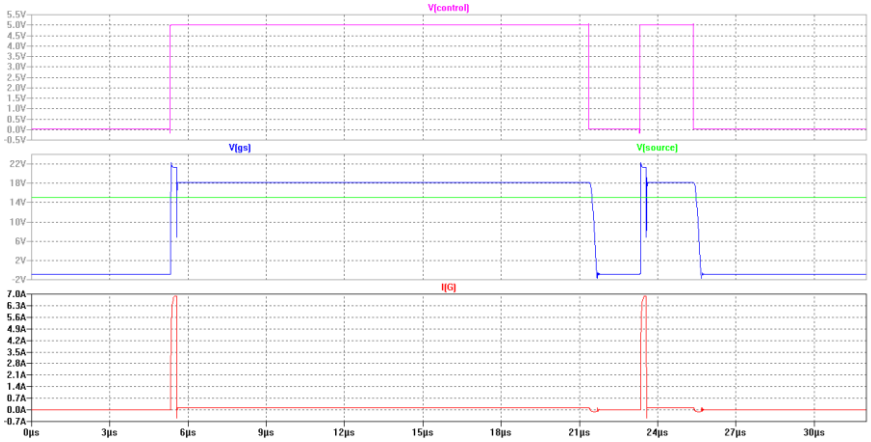



**Figure 5.13. Final simulation results for the proposed gate driver circuit**

The waveforms are (from top to bottom) the control signal, resultant gate-source voltage Vgs and resultant gate current Ig respectively. Analyzing the waveforms in Figure 5.13 one can easily distinguish the margin between the stages and the contribution from each of the stages. It can be seen that the turn-on edge of Vgs is now much steeper resulting in a fast turn-on transition. Both the current and voltage are boosted during the first 100 ns when the buffer stage is active. Then the on-state stage takes over with 3 V and 160 mA to keep the SiC VJFET in the on-state and provide low Rds(on). A rather passive behaviour from the turn-off stage can be observed since the current is not forced to go negative and the turn-off edge of Vgs is relatively slow. This results in a minor increase in the gate driver losses. For comparison Figure 5.14 shows the measured gate current of the commercial gate driver from SemiSouth discussed in section 3.6.1 compared to the proposed gate driver current simulated in LTspice environment.

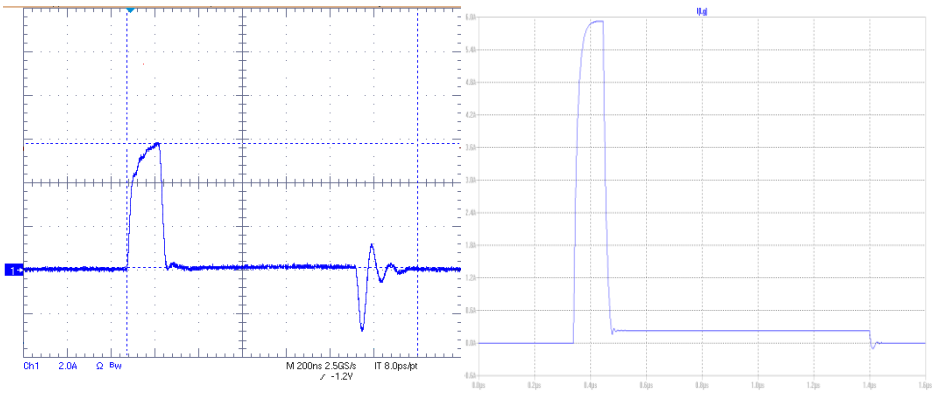


**Figure 5.14. Measured vs. simulated gate current**

It is seen that the shape of the turn-on current is the same and the amplitudes in both cases are close to 6 A. The on-state current is more obvious in the simulated waveform, but this

is mainly due to the scale used. And again the lack of fast turn-off in the simulated waveform is straightforward revealing the imperfection of the designed turn-off circuit. This is to be taken into account when dealing with real laboratory prototype.

# 6. LABORATORY SETUP

## 6.1. Setup description

### 6.1.1. Double-pulse test setup

Switching energy loss is one of the major performance factors used in comparing different semiconductor devices for new designs. Minimizing this number is a priority for high switching frequency applications as this type of loss can become a significant portion of the total device losses [19]. The losses of normally-off SiC VJFET and other SiC transistors are measured according to the same standard as MOSFET/BJTs.

Double-pulse clamped inductive load transistor test [43] as shown in Figure 6.1 is an efficient method to investigate the switching times, energies, turn-on and turn-off power loss and conduction loss of power electronic devices under testing (transistor and freewheeling diode marked with DUT in Figure 6.1) at different current and voltage levels. The photo of laboratory setup can be seen in Figure 6.2.

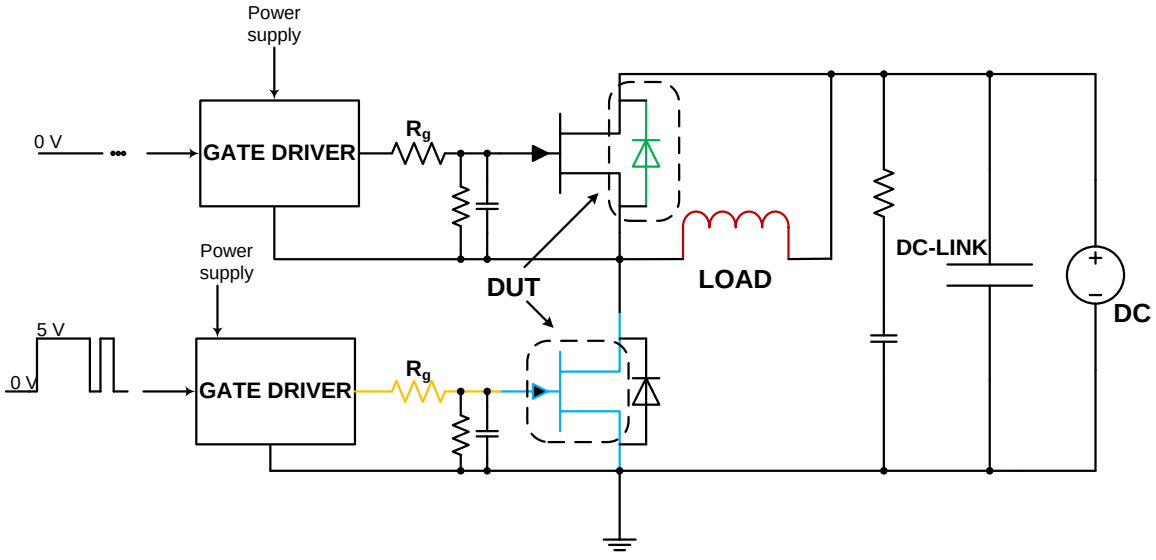



Figure 6.1. Schematic of double-pulse test circuit

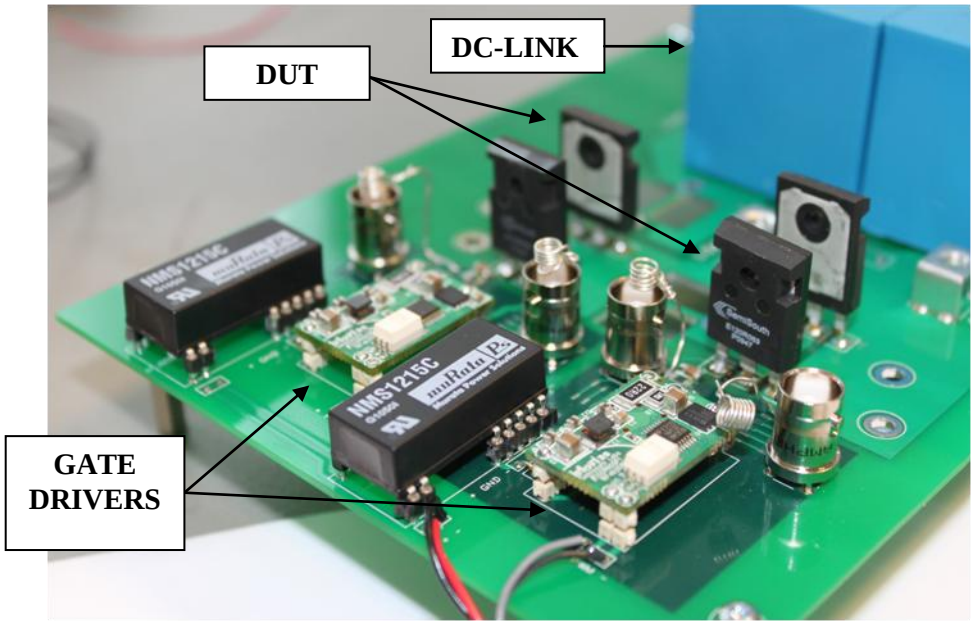



Figure 6.2. Laboratory photograph of double-pulse test board

The gate drive circuit is connected to transistors gate, and a double-pulse is applied. The two pulses are composed by one long pulse followed by a fairly short pulse. This allows stressing the transistor by turning on and turning off at rated current. The typical current and voltage waveforms can be observed in Figure 6.3, the power dissipation and energy loss of transistor can be calculated using equations (6.1) – (6.3). Energy loss is the integral of power dissipation. The power and energy losses waveforms are also shown in Figure 6.3. Since only Schottky diodes were used in the experiment which lack reverse recovery, diode current waveforms were not monitored separately.

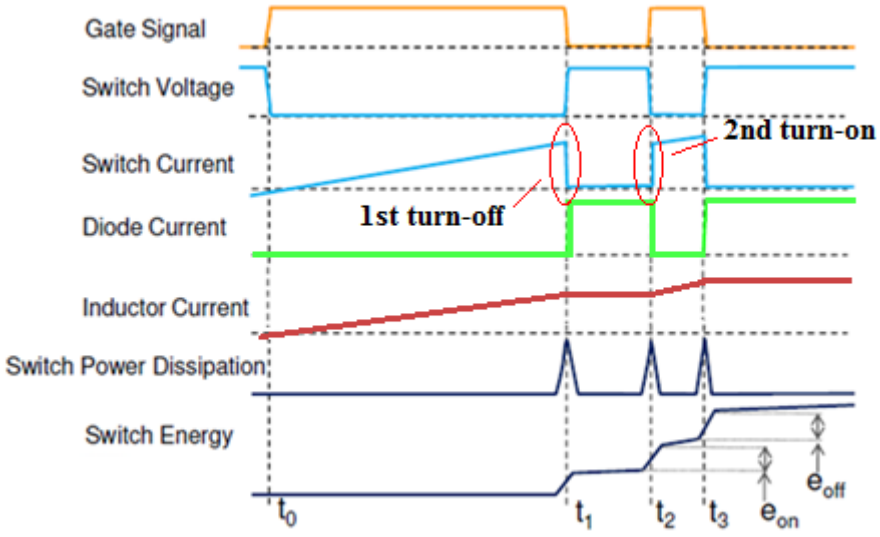



Figure 6.3. Principle waveforms during double-pulse test [44]

Integrated with the oscilloscope power measurement software was used to acquire switch power dissipation and switching energies. An example of software interface showing acquired switching power and energy values is shown in Figure 6.4.

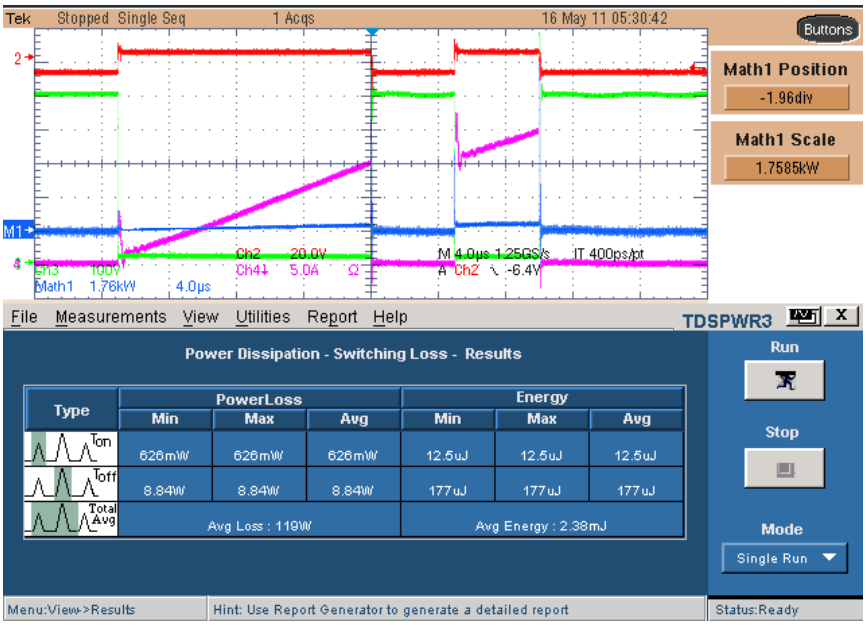



**Figure 6.4. Switching power and energy extraction tool**

The vertical cursors can be set manually to define the region where the values are calculated. It can be either turn-on/turn-off or both at the same time. If the specific on-state resistance $R_{ds(on)}$ of the power transistor is defined then the conduction power losses are also included in the calculation. In this case the average power loss and energy can also be found.

If the previously mentioned software is not available then the power and energy calculation analytical methods should be applied in order to obtain these values [45]. The power can be calculated by using equation (6.1)

$$P = V(t) \cdot I(t) \tag{6.1}$$

where *P – switching power dissipation, W;*

*V(t) – instantaneous transistor voltage, V;*

*I(t) - instantaneous transistor current.*

The turn-on/off energy is the energy dissipated inside the transistor during the turn-on/off of a single drain current pulse which can be calculated by using equation (6.2)

$$E_{on} = \int_{t_{on}} V(t) \cdot I(t) dt \tag{6.2}$$

where $E_{on}$ – *turn-on switching energy, [J]*.

The turn-off energy can be calculated by using the equation (6.3)

$$E_{off} = \int_{t_{off}} V(t) \cdot I(t) dt \tag{6.3}$$

where $E_{off}$ – *turn-off switching energy, [J]*.

### 6.1.2. Half-bridge converter PCB layout

The main power board for the double-pulse test was developed in cooperation with the engineers at Eltek Valere's laboratory facilities. Some ideas were taken from [31] where the design process of the single transistor double-pulse test board is described. The printed circuit board without the components connected can be observed in Figure 6.5. The main schematic of the board developed in CADSTAR software is available in Appendix D.

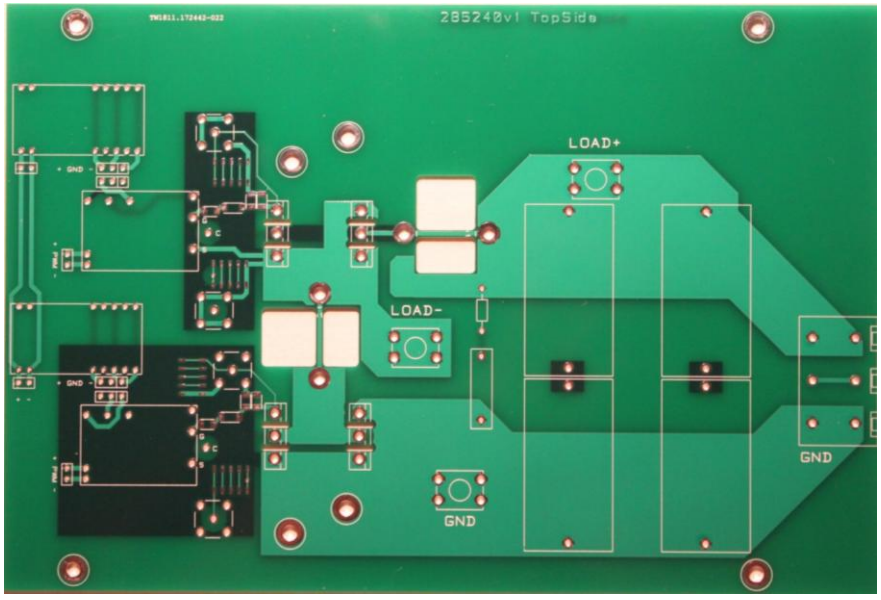



**Figure 6.5. The photograph of the main power test board (top view)**

The board includes footprints for all the required components together with some options for measurements. For instance two different connectors are available for gate-source and drain-

source voltage measurements. Depending on the probe tip used either one or another option can be utilized. A cut-out for the current probe is made in the board to measure the drain current.

### 6.1.3. Load inductor

A ferrite core inductor with a single layer winding which results in a low parasitic capacitance was used in the experiment. The value is chosen to be 535 µH which was the closest available to recommended 850 µH mentioned in [31].

In order to calculate the current that builds up in the inductor during the double-pulse test equation (6.4) was used.

$$V_L = L\frac{di_L}{dt} \tag{6.4}$$

where $V_L$ *– inductor voltage, [V];* $L$ *– inductance, [H];* $i_L$ *– instantaneous inductor current, [A];* $t$ *– instantaneous time moment, [s].*

Defining the desired current value and knowing applied voltage and inductance value time duration of the pulses can be obtained. For this experiment applied voltage was set to 500 V and the value of inductor was fixed to 535 µH. If the desired current during the first pulse is set to 15 A then according to (6.4) the pulse duration should be equal to 16 µs. This value was chosen as a default for most of the measurements. Following same procedure the time periods for 10 A and 5 A are 10 µs and 5 µs respectively.

### 6.1.4. Input control signal generation – DSP card

Input signals to the gate driver were provided by means of a DSP card from Texas Instruments which was specially programmed for this experiment by one of the co-supervisors. A photo of the DSP card can be seen in Figure 6.6.

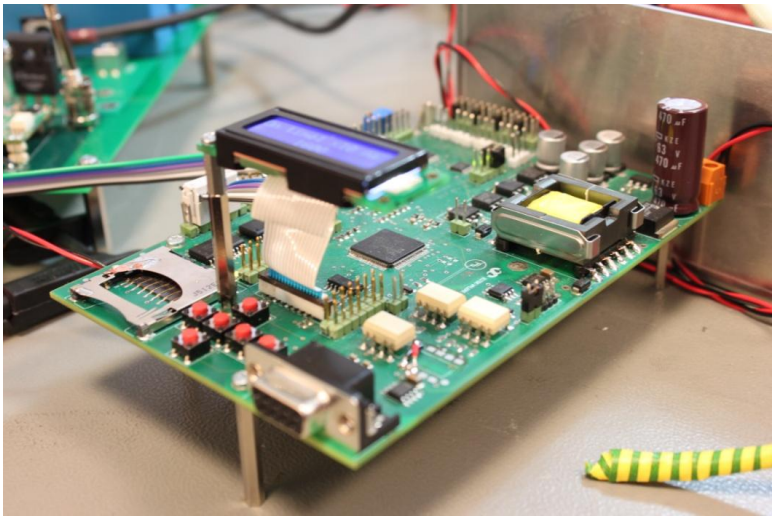


Figure 6.6. Lab photo of connected DSP card

A user friendly interface allowed very quick and precise pulse width adjustment. All four on/off pulses were set separately. It is worth mentioning that the DSP card allowed making modifications in pulse widths in real-time with fully operational and energized circuit. For the sake of simplicity and time saving some default presets of pulses were also programmed, e.g. a set of 16 µs, 6 µs, 6 µs and 0.6 s which stand for 1$^{st}$ on time, 1$^{st}$ off time, 2$^{nd}$ on time and 2$^{nd}$ off time respectively.

## 6.2. Measurement equipment

The measurement equipment available at the laboratory was thoroughly studied and compared. As a result equipment found in Table 6.1 was chosen as the one with best specifications for given experiments.

Table 6.1. List of measurement equipment

| Equipment | Type | Bandwidth |
|---|---|---|
| **Oscilloscope** | Tektronix TDS5054B DPO | 500 MHz, 2.5 Gs/s |
| **Current probe** | Tektronix TCP202 | 100 MHz |
| **Voltage probe** | Tektronix P6139A | 500 MHz |

For accurate measurements, it is very important to de-skew the voltage and current probes to insure that all of the delays are the same. De-skewing the voltage probes can be done by attaching both probes to a pulse generator output and adjusting the channel de-skew on the

oscilloscope so that both pulses are time synchronized [31]. This way, the probes were de-skewed and the results are expected to be trustful enough.

## 6.3. Measurement plan

It was decided to split the measurements into different sections with a brief description appearing prior to each experiment section. In each of the experiments the devices that are used are also highlighted in a separate table. ***Different SiC transistors, freewheeling diodes and gate driver circuits might appear in each particular experiment.*** The gate drivers used are either commercial driver (DC coupled) from SemiSouth discussed in section 3.6.1, the AC coupled driver constructed based on the SiC BJT driver design mentioned in section 3.6.3 or the proposed two-stage gate driver discussed in section 4.4.

Default measurement parameters were set for all captured waveforms in order to enlighten the later comparison process. These parameters can be found in Table 6.2 below.

**Table 6.2. Default measurement parameters**

| Parameter | Value | Scale |
|---|---|---|
| **Drain-source voltage Vds *(Collector-emitter voltage Vce)*** | 500 V | 100 V/decade |
| **Gate-source voltage Vgs** | 15 V | 20 V/decade |
| **Drain current Id *(Collector current Ic)*** | 15 A | 5 A/decade |
| **Gate current Ig** | | 5 A/decade |
| **Time** | | 40 ns/decade |
| **Screen resolution** | | 400 ps/pt |

The most important waveforms during the double-pulse test are the 1$^{st}$ turn-off and the 2$^{nd}$ turn-on. During these periods of time transistor switches at the full load current, which is 15 A according to Table 6.2. During the 1$^{st}$ turn-off the dv/dt of $V_{ds}$ was measured and during the 2$^{nd}$ turn-on the di/dt of $I_d$ was measured. Current and voltage overshoots were also monitored. A full cycle of double-pulse waveform is also captured to make the base for comparison of voltage/current values and switching times.

### 6.3.1. Gate driver circuit measurements

Gate current/voltage measurements were performed with limited bandwidth on the oscilloscope, i.e. 20 MHz. This is done in order to filter unwanted high frequency signal which disturbs the waveforms of interest.

Two methods for gate current measurement were tested in order to estimate the best possible result. The influence of these methods on gate current/voltage measurements was also studied. It is worth mentioning that current measurement in power electronics is quite complicated due to the lack of high quality equipment as a result of high cost.

First method involved use of fairly low ohm resistor with a value of 0.1 Ω. The idea is to measure the voltage drop over the resistor and then simply scale this voltage to get 1:1 ratio with the current flowing through it. In fact a value of 1 Ω is preferable since the scaling process becomes less complicated, but a value of 0.1 Ω provides less influence on the current measurement process and produces less losses. Such resistors are widely used in high frequency applications due to low inductance and are also called current sensing resistors. The experiment revealed obvious drawback of this method which will be briefly described further. First of all a differential probe was needed to perform correct current measurement. The available differential probe was quite massive in size and due to limited space available in the gate interface created a serious constraint. As the further investigation showed this constraint was not the problem. The distortion on the current measurement was so high that this method was excluded and other options were to be found.

Second method was to make a loop of wire in the gate interface and use a current probe to record the desired waveform. Since the current probe size added some difficulties as with the differential probe the loop of wire had to be made big enough. Adding an extra loop in the gate is a risky task which can cause a serious distortion in current measurement due to stray inductance. Since no other option was available it was decided to use this method for recording gate current measurements because the results appeared to be good enough to be documented.

Just to be mentioned, another possible method of gate current measurement is to use a small current transformer. A two-stage current transformer measurement setup is shown in Figure 6.7.

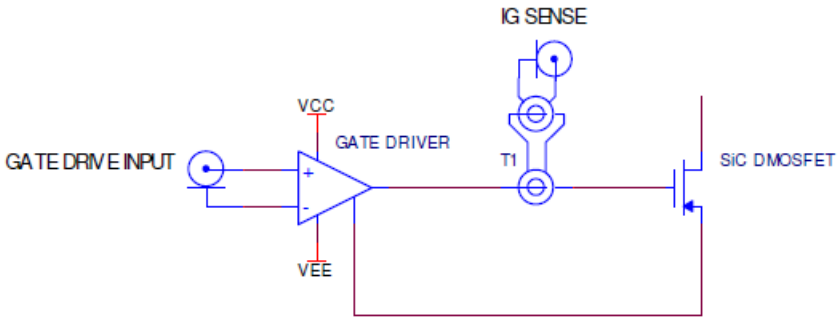



**Figure 6.7. Two-stage current transformer measurement setup**

The first stage consists of 10 turns of wire on a small high permeability core, whereas the second stage is a small wide bandwidth current transformer. ***This measurement method requires a separate source return path for the gate driver. If this is not provided there is a probability that the load di/dt can be fed back into the gate driver circuit, due to stray inductance of the source lead.***

Unlike for gate current measurements, BNC connectors were used for recording the gate-source voltage which appeared to be a reasonable choice during design process. The probes were easily fit to these connectors. To reduce the loop in the probe and improve the quality of measurement a ground wire was disconnected and a fairly short connection to ground point was made. This way gate voltage waveforms of sufficient quality were acquired.

In order to test the behaviour of the gate driver circuits and the influence on the switching of SiC transistors it was decided to vary the gate resistor value as well as the applied gate supply voltages. This way optimized switching behaviour [30] can be achieved and the trade-off between fast speed (low losses) and EMI issues can be obtained. Some other tests of interest include the placement of ferrite bead in the gate to see if the waveforms can be improved. This might come in the expense of slower switching speed though. The small capacitor, typically 2.2 nF has proved to provide extra noise immunity of the gate [19], so it is decided to test this as well.

# 7. MEASUREMENT RESULTS

All measurements were done at comparable conditions and measurements methods of voltages and currents as well as the test circuit. Only the drivers are different since all devices need specific gate/base signals. Unless other stated, the voltage/current levels as well as other important parameters were held at levels according to Table 6.2.

## 7.1. Experiment #1 - Gate measurements

The main objective of this experiment is to study the behaviour of the designed two-stage gate driver for SiC VJFET and compare the performance to commercial SiC VJFET DC-coupled gate driver (section 3.6.1). Among other objectives of interest is to study the behaviour of both the DC-coupled and the AC-coupled (section 3.6.3) gate drivers and test the way they drive SiC transistors.

Gate measurements were performed using method described in section 6.3. The idea behind the gate current measurement is to make a loop of wire in the gate interface and use a current probe to record the desired waveform. Adding an extra loop in the gate is a risky task though which can cause a serious distortion in current measurement due to addition of stray inductance. ***The external gate resistor was not connected due to complexity of gate interface and lack of available space. The gate driver circuit itself contains biasing resistors. Placing an external gate resistor influences both gate driver stages. In the ideal case resistors must be changed on the driver board itself.***

A small 2.2 nF capacitor and a 10 kΩ resistor was also connected close across the gate-source of the device to increase the noise immunity of the gate.

### 7.1.1. DC-coupled gate driver

Table 7.1 shows the devices under test for this particular experiment.

**Table 7.1. Objects under test for gate measurements**

| Switch | Freewheeling diode | Gate Driver |
|---|---|---|
| SemiSouth SiC VJFET SJEP120R063 | CREE C3D20060 SiC Schottky diode | SemiSouth SGDR600P1 |

Figure 7.1 (left) shows the output switching waveforms of the DC-coupled gate driver without the DC bus applied to the power circuit.

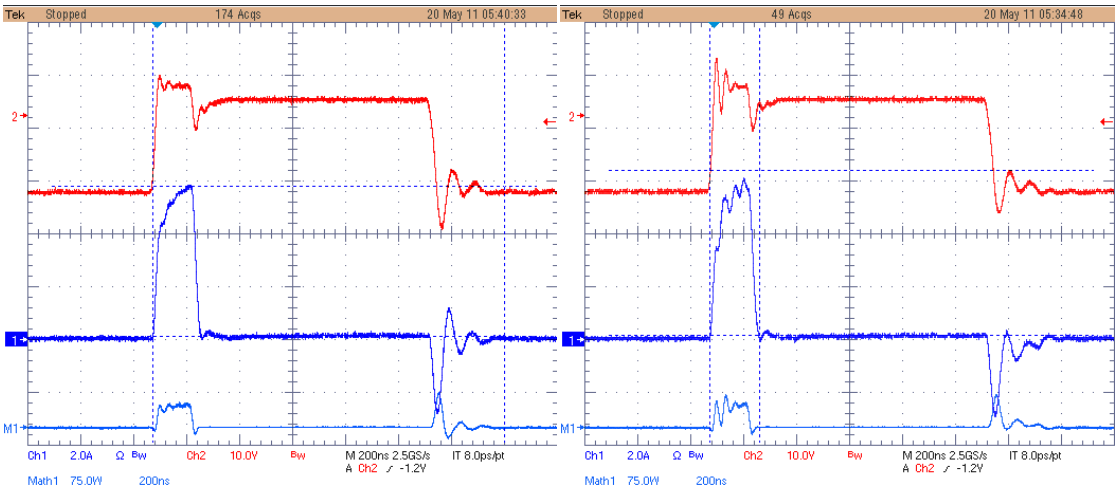



**Figure 7.1. DC-coupled gate driver output waveforms. Left: without Vds. Right: with Vds applied. Ch2 (Red, 10 V/div) - Gate voltage. Ch1 (Blue, 2 A/div) - Gate current. M1 (light blue) - Gate power.**

Analyzing the waveforms on the left in Figure 7.1 it can be observed that both the voltage and current have two stages. When the control electronics provides the turn-on signal the gate voltage builds up to the value as high as 7.6 V. At the same time the current is rising rapidly to the peak value of 5.8 A. It is worth mentioning that the time period of these relatively high voltage and current in Figure 7.1 are limited to approximately 200 ns. In the ideal case [46] this time should be limited to 100 ns since it is enough to charge the gate input capacitances. If the time period is more than 100-200 ns it can cause a severe damage to the gate due to excessive high current flow through the parasitic gate-source diode. The second stage takes over when the current drops to the value as low as 140 mA to sustain the conduction of SiC VJFET. It can also be observed that the voltage stabilizes at the level of 3 V. This coincides well with the main gate requirements of SiC VJFET mentioned in section 4.1. During turn-off the gate capacitances are discharged through the low ohm current path on the gate driver circuit. This appears as the negative current in the Figure 7.1. The mean power for both the turn-on and turn-off is estimated to be 2.33 W.

For comparison reason waveforms on the right in Figure 7.1 show the gate output with the DC bus applied to the power circuit. It can be seen that the waveforms are slightly distorted and more high frequency oscillations occur. This proves that there is influence of the main power circuit on the gate driver circuit due to added stray inductances. These inductances create high frequency oscillation feedback to the gate driver circuit. Hence, the loop area composed of the VJFET + freewheeling diode + dc-link capacitors must be minimized, as well as the physical

distance from the gate driver to the VJFET must also be minimized. The voltage and current peaks has now reached 10.9 V and 6.1 A respectively. The power losses also increased from 2.33 W to 2.7 W compared to the previous case.

Figure 7.2 shows a close-up on the second stage, low current conduction stage, of the DC-coupled gate driver circuit.

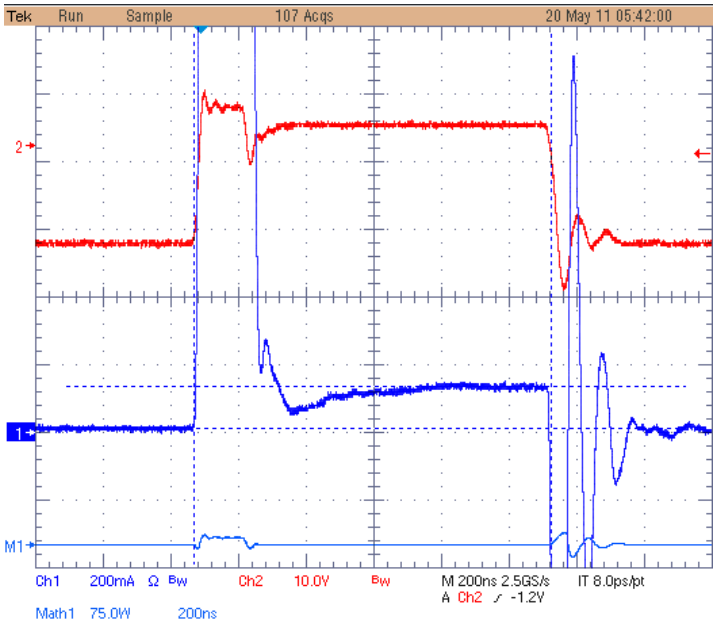



**Figure 7.2. DC-coupled gate driver output waveforms. A close-up on the second stage (140 mA conduction stage) of the DC-coupled gate driver. Ch2 (Red, 10 V/div) - Gate voltage. Ch1 (Blue, 200 mA/div) - Gate current. M1 (light blue) - Gate power.**

Figure 7.2 reveals the second stage of the DC-coupled gate driver circuit showing the 140 mA current needed to sustain the gate-source diode in the on-state and as a consequence the conduction of the SiC VJFET. ***Gate current scale is increased and the peak is not visible.***

### 7.1.2. AC-coupled gate driver

The devices under test for this particular experiment can be observed in Table 7.2.

**Table 7.2. Objects under test for gate measurements with AC-coupled gate driver**

| Switch | Freewheeling diode | Gate Driver |
|---|---|---|
| SemiSouth SiC VJFET SJEP120R063 | CREE C3D20060 SiC Schottky diode | AC-coupled |

The AC-coupled driver circuit used in the previous experiments was optimized to be used with SiC VJFET. The gate resistor Rg was decreased from 56 Ω to 20 Ω. Figure 7.3 (left) shows

the output switching waveforms of the AC-coupled gate driver without the DC bus applied to the power circuit.

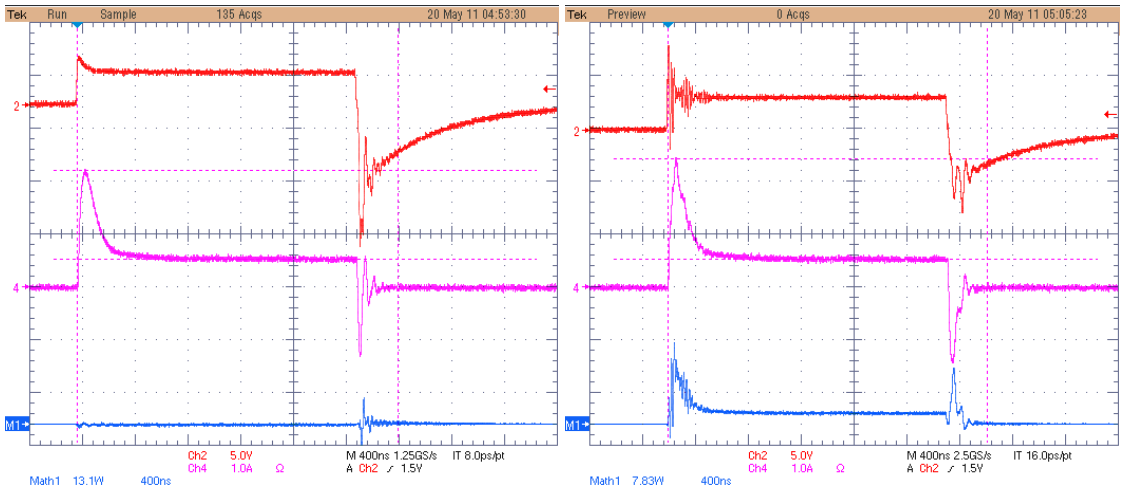



**Figure 7.3. AC-coupled gate driver output waveforms. Left: without Vds. Right: with Vds applied. Ch2 (Red, 5 V/div) - Gate voltage. Ch4 (Purple, 1 A/div) - Gate current. M1 (blue) - Gate power.**

Analyzing the waveforms on the left in Figure 7.3 it can be observed that both the voltage and current have two stages like in the case of the DC coupled gate driver. When the output of the optocoupler goes high the gate voltage quickly builds up to the value of 4.6 V. At the same time the current is rising rapidly to the peak value of 2.2 A. The duration of the peak in Figure 7.3 is limited to approximately 150 - 200 ns by the RC time constant. The second stage of the gate driver that sustains the conduction of SiC VJFET is also shown. The current value of approximately 500 mA appears to be flowing at this time, which is apparently a bit high. This is a miscalculation in the design process, as a result of the wrong gate resistor value selection. It should be noted that the current can be as low as 100 mA in order to achieve the lowest Rds(on) possible and in turn reduce the losses in the gate driver. The voltage stabilizes at the level of 3 V. During turn-off the gate capacitances are discharged resulting in the negative current in the Figure 7.3. The power measurements that appear in the Figure 7.3 are incorrect due to the error in the oscilloscope settings. Unfortunately, this fact does not allow making a comparison of driving power of both gate driver types.

The waveforms on the right in Figure 7.3 shows the gate output with the DC bus applied to the power circuit. It can be seen that the waveforms are heavily distorted, especially the gate voltage waveform. The influence of the main power circuit on the AC-coupled gate driver circuit appears to be intensive, showing the weak noise immunity of this driver circuit. The voltage and current peaks has now reached 8 V and 2.5 A respectively. An interesting fact to mention is that

in this case the turn-off is slower since the negative voltage peak is lower in amplitude. The shape of power loss is correct though the value acquired is incorrect.

### 7.1.3. Proposed SiC VJFET two-stage gate driver

#### 7.1.3.1 Changes in the measurement setup

Unlike other measurements, which were performed at the laboratory facilities of Eltek Valere the following experiment (refers only to section 7.1.3) with the proposed gate driver circuit is held at the power electronics laboratory at NTNU. A new measurement and testing station had to be built from scratch. Though, the half-bridge converter is the same converter discussed in section 6.1.2.

The list of new measurement equipment for this experiment can be observed in Table 7.3. Lower bandwidth current and voltage probes as well as the oscilloscope are used in this case, therefore the measurement results are expected to be diversified from the previous ones.

**Table 7.3 List of measurement equipment for the experiment with proposed gate driver circuit**

| Equipment | Type | Bandwidth |
|---|---|---|
| **Oscilloscope** | Tektronix MSO2024 | 200 MHz, 1 Gs/s |
| **Current probe (Drain)** | Tektronix P6021 | 60 MHz |
| **Current probe (Gate)** | Micro-Rogowski coil | 50 MHz |
| **Voltage probe** | Tektronix P5200 | 100 MHz |

Among other changes, a 300 V power supply is now used to energize the main power circuit as well as the inductor has an iron core and the inductance value of 1 mH (almost twice higher inductance value compared to the previous case, which is 535 uH according to section 6.1.3). The input control signal is now generated by means of standard laboratory function generator. It should be mentioned though that this generator is able to produce a double-pulse signal, which is vital for the upcoming experiment.

The devices under test for this particular experiment can be observed in Table 7.4.

**Table 7.4 Objects under test for gate measurements with proposed SiC VJFET gate driver**

| Switch | Freewheeling diode | Gate Driver |
|---|---|---|
| SemiSouth SiC VJFET SJEP120R063 | CREE C3D20060 SiC Schottky diode | Proposed two-stage gate driver |

### 7.1.3.2 Measurement results for proposed SiC VJFET gate driver

The test is performed with +/- 9 V applied at the gate and no external resistors connected in the gate interface. The gate driver output voltage and current waveforms without the DC bus applied to the power circuit can be observed in Figure 7.4.

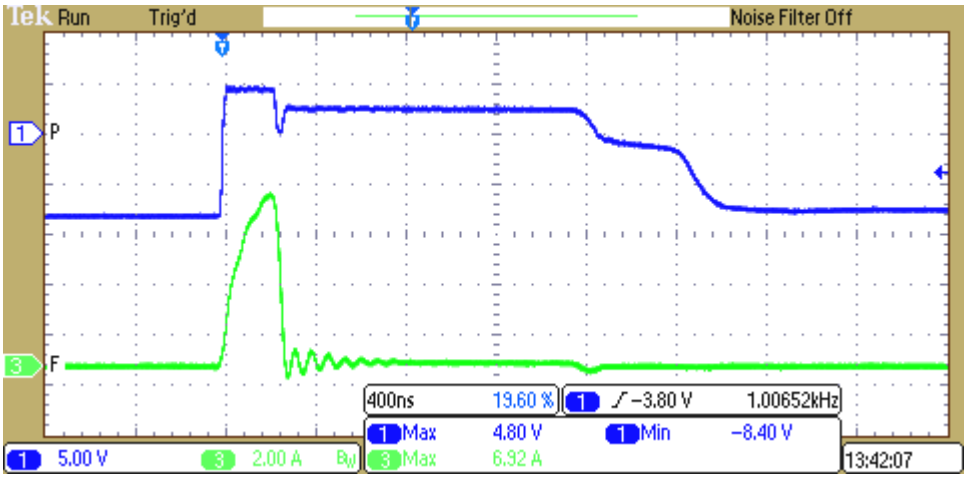



**Figure 7.4. Proposed gate driver output waveforms without Vds applied. Ch1 (Blue, 5 V/div) - Gate voltage. Ch3 (Green, 2 A/div) - Gate current.**

Analyzing the waveforms it can be concluded that the overall behaviour of the proposed gate driver is according to expectations and is similar to commercial gate driver (Figure 7.1). Though the turn-off of the driver appears to be slow and might result in unacceptable turn-off losses of the SiC VJFET. The results of the switching of SiC VJFET will be addressed recently.

Figure 7.5 shows a close-up on the gate driver turn-on event.

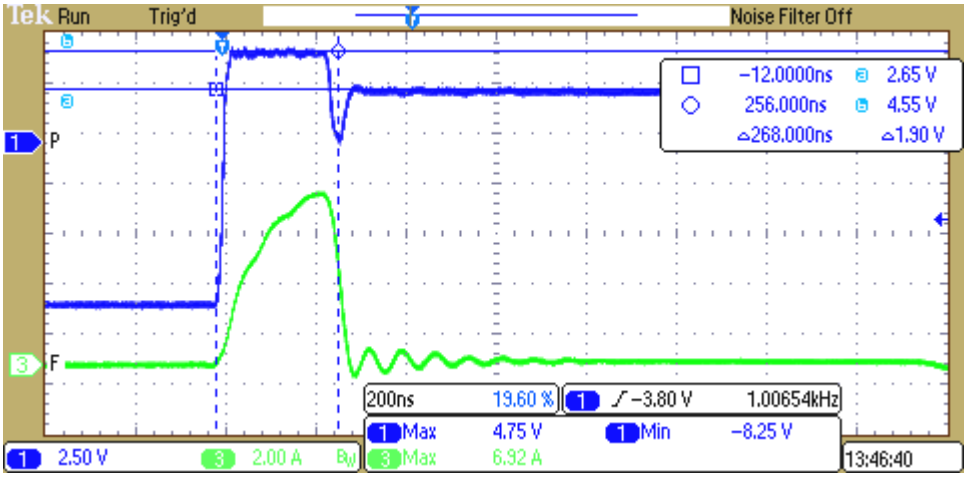



**Figure 7.5. A close-up on the gate driver turn-on. Ch1 (Blue, 2.5 V/div) - Gate voltage. Ch3 (Green, 2 A/div) - Gate current.**

The waveforms reveal that both the buffer stage (section 4.4.5) and the on-state stage (section 4.4.4) of the proposed gate driver perform well. As expected the buffer stage is only activated for slightly more than 200 ns in order to reduce the turn-on losses and achieve a fast

turn-on transition. In order to adjust the correct buffer stage timing one can vary the C108 capacitor (Figure 4.6). In this case the capacitor value should be reduced. It should be mentioned that according to section 4.1.2 it is desirable to overdrive the gate for 100 – 200 ns. The gate voltage is held at the level of 4.75 V during the turn-on process and the gate current reaches an impressive value of 6.92 A. After the buffer stage is deactivated the on-state stage takes over when the voltage stabilizes at the level of 2.65 V and the current drops to the value as low as 130 mA in order to sustain the conduction of SiC VJFET and achieve the low on-state losses. A close-up on the on-state conduction current is seen in Figure 7.6.

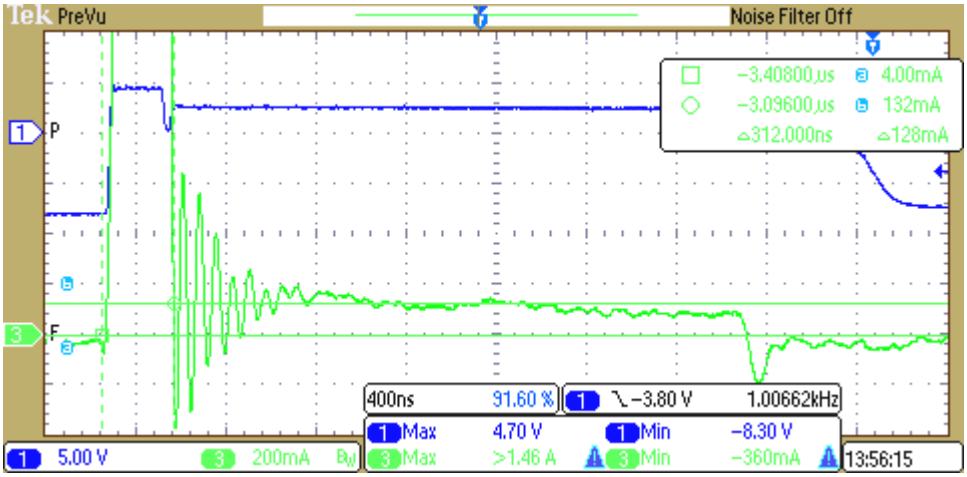



**Figure 7.6. A close-up on the second stage (140 mA on-state stage) of the proposed gate driver. Ch1 (Blue, 5 V/div) - Gate voltage. Ch3 (Green, 200 mA/div) - Gate current.**

The analysis of the measured gate current proves that the gate of SiC VJFET consumes a fraction of current in order to sustain the conduction of drain current thus it is expected that the gate drive losses are higher than, for instance, in the case of SiC MOSFET (section 2.4.2). On the other hand, the on-state gate current is not dependent on the drain current magnitude, like in the case of SiC BJT.

The turn-off stage of gate driver circuit can be observed in Figure 7.7.

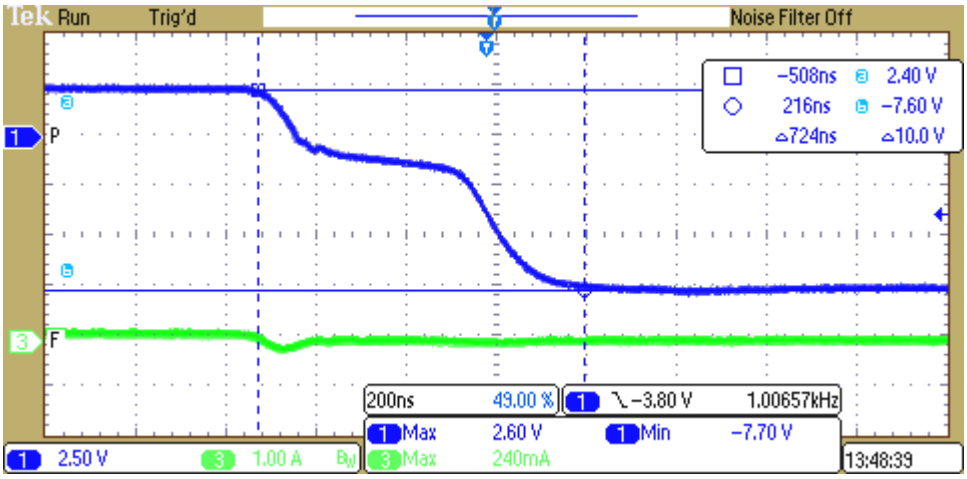



**Figure 7.7. A close-up on the gate driver turn-off. Ch1 (Blue, 2.5 V/div) - Gate voltage. Ch3 (Green, 1 A/div) - Gate current.**

Figure 7.7 reveals the unexpected behaviour of the turn-off stage of the proposed gate driver. The total turn-off time from the on-state value down to negative turn-off voltage is estimated to be 724 ns. It should be reminded though that SiC VJFET is a normally-off device meaning that the conducting channel is totally pinched off when no voltage is applied to the gate. Analyzing the gate voltage waveform it can be concluded that the zero crossing occurs approximately after 100 ns and it can be assumed that the transistor is totally-off by that time. It should be noted that in the ideal case the gate driver needs to switch faster than the transistor. Since the switching of SiC VJFET lies in the range of tens of nano-seconds the turn-off of the proposed gate driver is considered unacceptable and the design needs to be revised in order to find the possible error or new solution. Gate voltage tail affects the noise immunity of the gate thus making it vulnerable to spikes and glitches as well as it limits the duty cycle of the gate driver.

For comparison, Figure 7.8 shows the gate output with the DC bus applied to the power circuit.

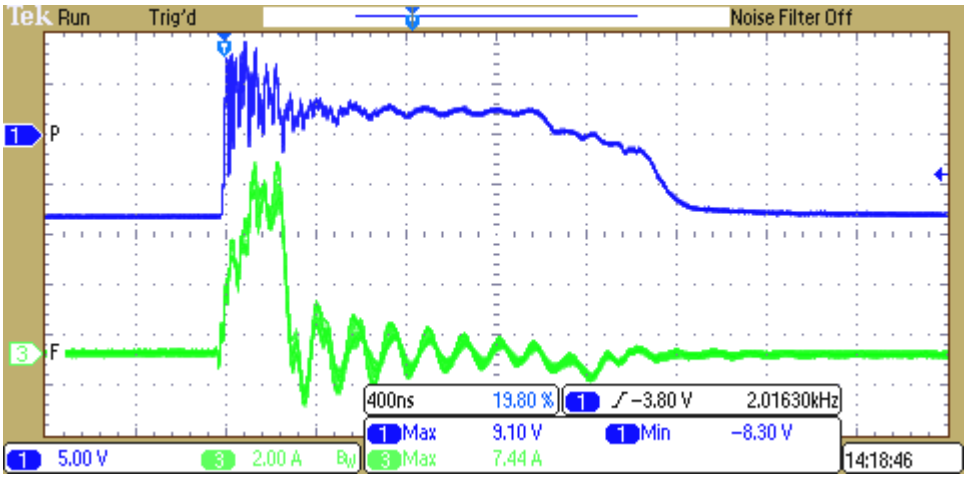



**Figure 7.8. Proposed gate driver output waveforms with Vds applied. Ch1 (Blue, 5 V/div) - Gate voltage. Ch3 (Green, 2 A/div) - Gate current.**

It can be noticed that the waveforms are heavily distorted when the switching of the main power circuit occur. The influence of the power circuit on the proposed gate driver circuit appears to be intensive, showing the weak noise immunity of the driver. This can be caused by the fact that the stray inductance of the gate oscillates with the input capacitance of SiC VJFET thus showing the need of reduction of the physical length between the output of the gate driver and the gate of SiC VJFET. A reduction of physical lengths in the main power circuit is also important.

Figure 7.9 shows the estimated gate power loss for the case without (left)/with (right) the DC bus applied to the power circuit.

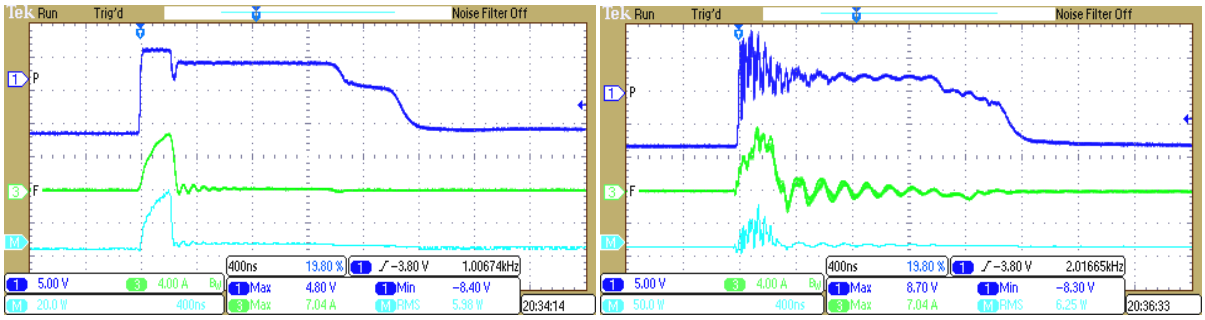



**Figure 7.9. Gate driver power loss estimation. Ch1 (Blue, 5 V/div) - Gate voltage. Ch3 (Green, 4 A/div) - Gate current. M – Gate power (Light blue, 20 W/div(left); 50 W/div(right)).**

The results show that a significant power is dissipated in the gate driver with the estimated RMS value of 5.98 W for the case when the power circuit is disconnected and 6.25 W when the power circuit is energized. The mean power dissipation value for both the turn-on and turn-off is estimated to be 1.56 W and 1.62 W respectively. This is lower than in the case of

commercial SiC VJFET gate driver (section 7.1.1) where the estimated mean power is 2.3 W and 2.7 W respectively. The lower power dissipation can be explained by the fact that the turn-off loss is almost absent due to improper performance of turn-off stage.

The result from the double-pulse test of SiC VJFET switching at 15 A and 300 V can be observed in Figure 7.10.

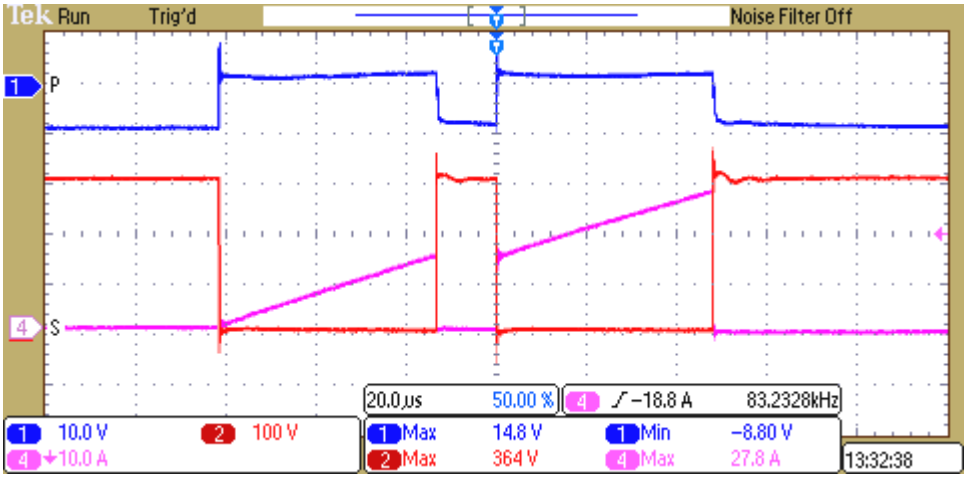



**Figure 7.10. SiC VJFET switching waveforms, full cycle of double-pulse test. Ch1 (Blue, 10 V/div) – Gate voltage, Ch2 (Red, 100 V/div) – Drain-source voltage, Ch4 (purple, 10 A/div) – Drain current.**

It can be seen that the proposed gate driver fulfils the overall requirement of driving the SiC VJFET. An interesting fact is that the peak gate voltage reaches and impressive value of 14.8 V without any damage to the gate. A close-up on the 1st turn-off of the SiC VJFET can be observed in Figure 7.11.

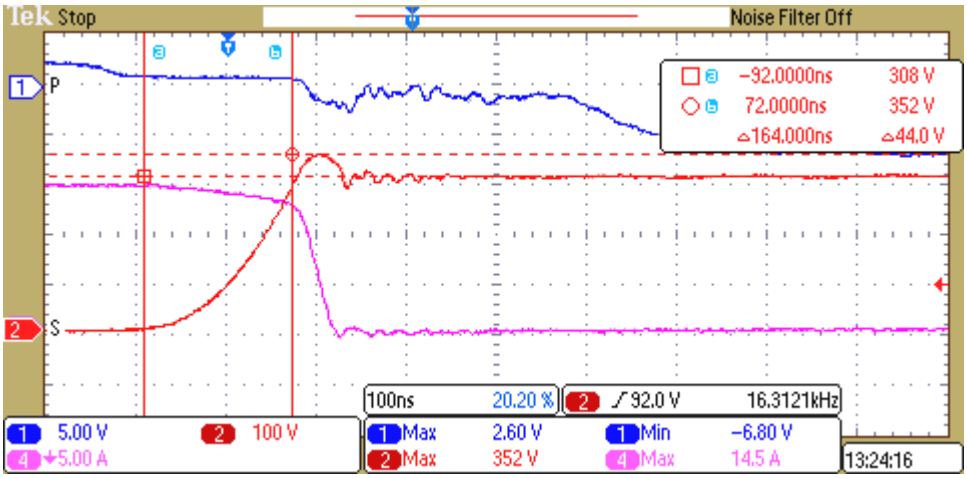



**Figure 7.11. SiC VJFET switching waveforms, 1st turn-off. Ch1 (Blue, 5 V/div) – Gate voltage, Ch2 (Red, 100 V/div) – Drain-source voltage, Ch4 (purple, 5 A/div) – Drain current.**

The measured rise time of the drain-source voltage Vds starting from on-state value to off-state value of 300 V is 164 ns which is almost 6 times slower than in the case of commercial SiC VJFET gate driver (Figure 7.16), taken into account that previous experiments are

performed with Vds = 500 V. This can be explained by the poor turn-off performance of the gate driver which was already discussed before. The voltage overshoot is 44 V with Vds peak value of 352 V. A close-up on the 2nd turn-on of the SiC VJFET can be observed in Figure 7.12.

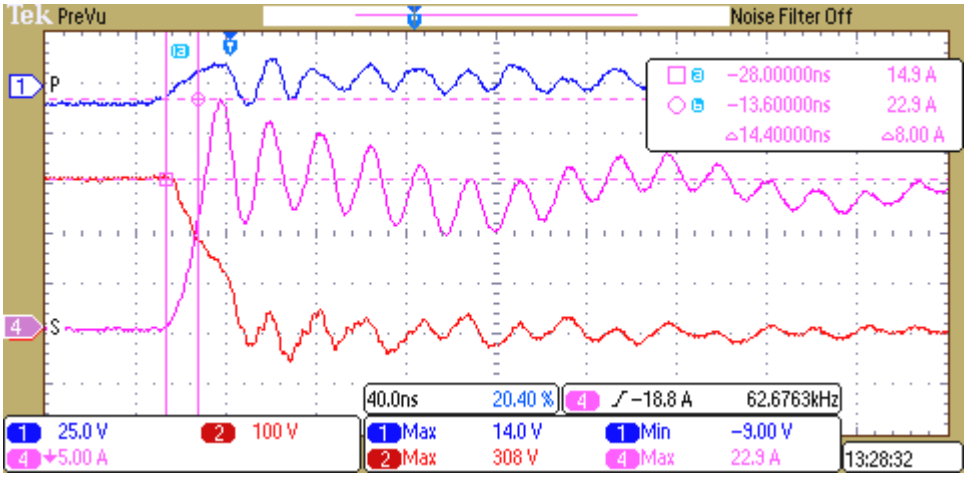



**Figure 7.12. SiC VJFET switching waveforms, 2nd turn-off. Ch1 (Blue, 25 V/div) – Gate voltage, Ch2 (Red, 100 V/div) – Drain-source voltage, Ch4 (purple, 5 A/div) – Drain current.**

The measured rise time of the drain current Id is 14.4 ns with the current overshoot of 8 A. The peak value of drain current is 22.9 A. An important issue to mention is the excessive ringing in both the gate circuit and the main power circuit. The switching energy measurements for this experiment are reflected in Figure 7.13.

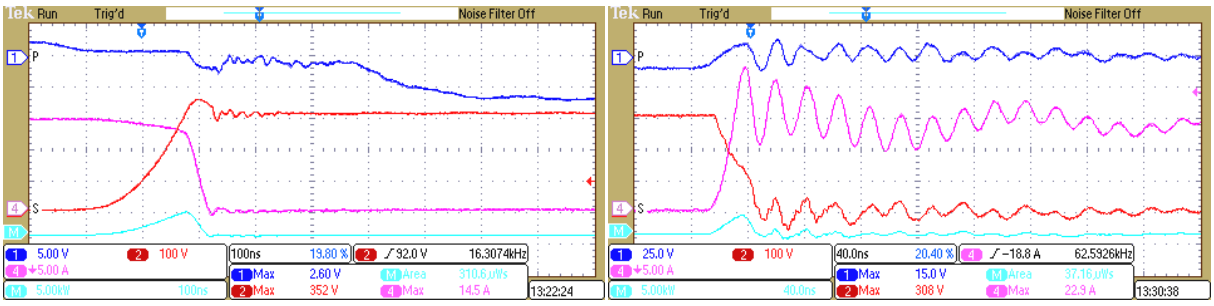



**Figure 7.13. SiC VJFET switching energy estimation. Left: 1st turn-off. Right: 2nd turn-on.**

The obtained switching energy is estimated to be 310.6 uJ in the case of the 1st turn-off and 37.1 uJ in the case of the 2nd turn-on. This once again proves that the proposed gate driver has the ability of fast turn-on, while the turn-off is rather slow resulting in relatively high turn-off switching loss. This fact once again highlights the importance of high performance ability of the gate driver circuit. The switching energy results are close to what was measured with commercial SiC VJFET gate driver with values of 247 uJ and 97.3 uJ respectively. It should be noted though that the previous experiments were performed with Vds = 500 V and the direct comparison between the measurement results cannot be done.

#### 7.1.3.3 Issues related to experiments with proposed gate driver

Some of the most significant issues will be addressed as bullets with brief description below. Possible solutions for the optimization of performance of the designed gate driver circuit will be given in the later stages of this section. Figure 7.14 shows a close-up on the proposed gate driver connected to the gate of the SiC VJFET during the double-pulse test procedure.

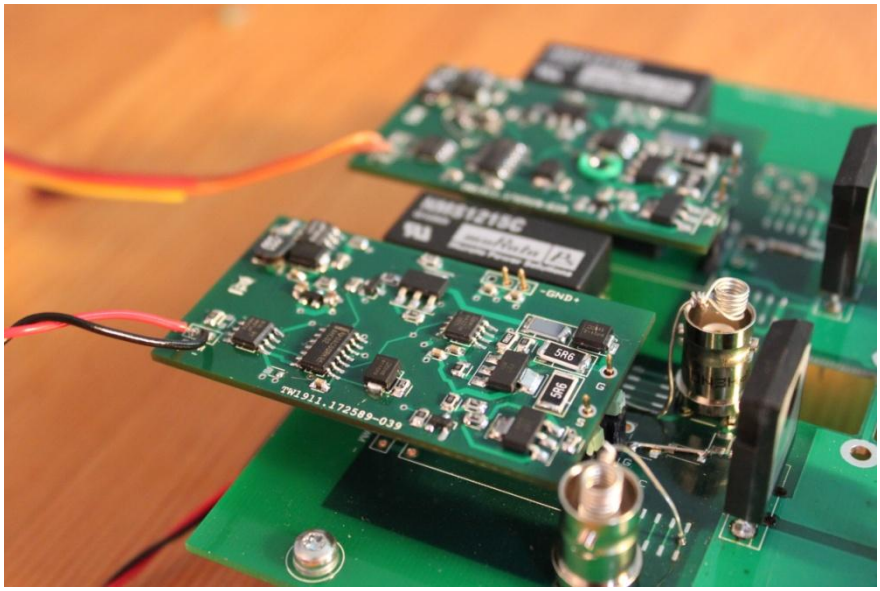


**Figure 7.14. Proposed gate driver circuit connected to the main power board**

- An error in design process revealed an inner layer overlap, resulting in a short circuit between the -9 V supply and ground plane (GND). The tracing of error was made by disconnecting the -9 V from different vias on the PCB and measuring the impedance between -9 V supply and GND. When the error point was found the via was drilled out to terminate the connection between the inner layers on the board. Then the -9V is delivered by means of a wire from nearest available point. It is worth mentioning that the process of tracing the error is very time consuming.
- The supply for logic gates and optocoupler are common and was designed to be within 5 V limit. In fact this supply was taken between -9 V and internally generated -4 V. Experiment revealed that 5 V is not enough to drive the optocoupler and a solution to generate at least 7 V was required, unless the alternative for the optocoupler is found. It was decided to increase the supply for optocoupler by means of connecting it between the -9 V and GND resulting in sufficient operating voltage. This solution in turn created a

new issue since both optocoupler and logic is fed from the same supply. The maximum supply voltage for logic is 5.5 V. A simple yet robust solution was implemented with voltage divider circuit leaving the 5 V for logic and 9 V for optocoupler. The result of this change can be observed in Figure 4.11 of section 4.5.

- Three voltage levels were fed to the board, i.e. +9 V, -9 V and GND. Since the SiC VJFET needs a small amount of current during on-state a low continuous current stage was implemented. To reduce the power losses +9 V supply was stepped down to as low as +5 V by means of switch-mode dc-dc converter as discussed in section 4.4.1. The testing of the dc-dc stage revealed a lack of ground connection and as a result some changes were made to the PCB. GND connection was taken from the nearest available point using an external wire.
- The voltage reference of the PCB was chosen to be -9 V since this is the recommended voltage for transistor turn-off and also for keeping it as far as possible from turn-on threshold. As a result the buffer IC was suppose to withstand 18 V swing, i.e. from -9 V to +9 V. This appeared to be the maximum allowed supply voltage of the buffer IC thus the measurements with +/- 12 V and +/- 15 gate voltage combinations was not possible. A solution could be to operate the buffer IC from GND to +15 V. In this case some modifications must be done to connections on the board. It is worth mentioning that the turn-off is not vital for this particular stage since IC only supplies base current for middle power PNP transistor (section 4.4.5) which in turn supplies the turn-on current for the main power switch.

The issues described above are only a small fraction of engineering challenges that had to be overcome during the testing of the gate driver. It should be mentioned that all the challenges on the way to get the driver up and running and further optimization of performance is a valuable experience that will definitely come in handy in the later circuit design projects.

#### 7.1.3.4 Design improvement proposals

Some ideas on how to fix the issues related to the existing design of the proposed gate driver circuit and optimize the prototype will be addressed below.

- Re-design of the power supply for optocoupler and the logic
- Selection of buffer IC with high maximum supply voltage of at least 30 V

- Re-calculation of the PNP transistor biasing circuits (on-state and turn-off stages)
- Re-checking the component compatibility and input/supply requirements
- Selection of only one solution for the buffer stage (either commercial IC or discrete solution)

## 7.2. Experiment #2 – Variable gate resistor Rg

The objective of this experiment was to find the influence of different gate resistor values on the switching characteristics of SiC VJFET, which is considered as the main candidate for replacing Si MOSFETs and IGBTs. Switching times and especially switching energies were of great interest. According to [30], the higher the positive supply voltage $V_P$ of the driver the higher the corresponding gate resistance $R_G$ is needed for a given gate current, and consequently the greater the high frequency oscillation damping in the gate circuit. On the other hand, a higher $V_P$ may result in higher losses in the gate resistor that is used to limit the constant gate current required for on-state conduction. No universal values can be recommended, therefore it is mainly the application that decides the proper selection of gate resistor value. Table 7.5 shows the devices under test for this particular experiment.

**Table 7.5. Objects under test for experiment with variable Rg**

| Switch | Freewheeling diode | Gate Driver |
|---|---|---|
| SemiSouth SiC VJFET SJEP120R063 | CREE C3D20060 SiC Schottky diode | SemiSouth SGDR600P1 |

SiC VJFET is used as the main power switch together with the SiC C3D20060 Schottky diode. The driver circuit for SiC VJFET is the commercial two-stage gate driver from SemiSouth described in section 4.5. For the initial experiment the gate supply voltage was set to +/- 9 V. It is worth mentioning that this experiment was performed with a RC snubber (22 Ω, 47 nF) connected across the dc-link, which according to [30] yield cleaner waveforms in the expense of slightly higher losses. The series RC combination across the DC link reduces the amount of high frequency noise feedback through the miller capacitance of the device. A small 2.2 nF capacitor was also connected close across the gate-source of the device to increase the noise immunity of the gate.

### 7.2.1. Rg = 2.2 Ω

The waveforms showing the full cycle of the double-pulse test is shown in Figure 7.15. The maximum values of the drain-source voltage Vds and the drain current also appear on the right side of the figure. ***These numbers show the absolute maximum values in the waveforms which in most of the cases relate to the last turn-off of the transistor, which is out of scope in the next measurements.***

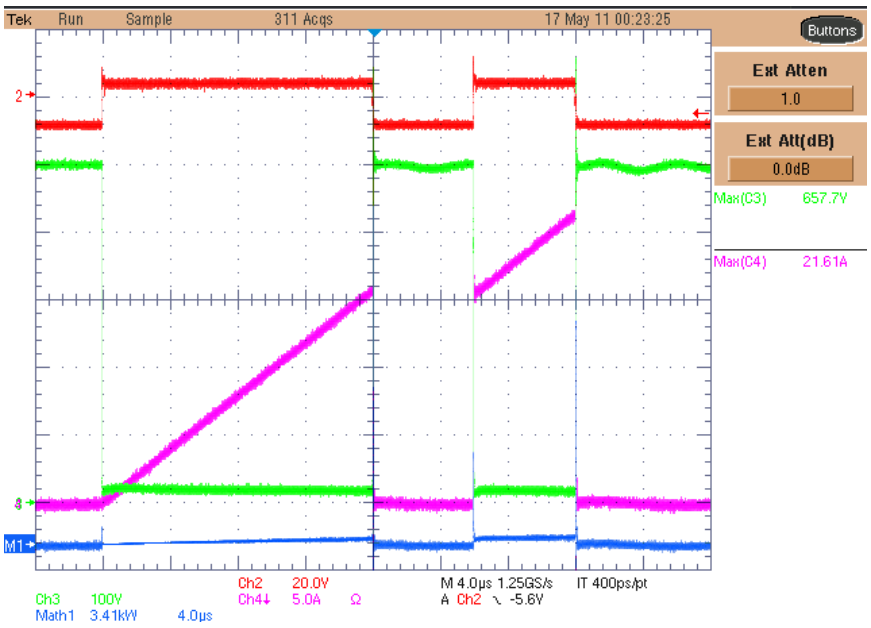



**Figure 7.15. SiC VJFET switching waveforms, full cycle of double-pulse test. Ch2 (red, 20 V/div) – Gate-source voltage Vgs, Ch3 (green, 100 V/div) – Drain-source voltage Vds, Ch4 (purple, 5 A/div) – Drain current Id, M1 (blue) – switching power dissipation.**

It can be seen that during the first pulse the current builds up until it reaches the desired value of 15 A. The pulse width to achieve the drain current of 15 A is set to 16 us, as already mentioned in section 6.1.3. During the 1st turn-off the current is commutated to the freewheeling diode and then back to SiC VJFET during the 2nd turn-on.

The most important waveforms during the double-pulse test are the 1st turn-off and the 2nd turn-on, as was already described in section 6.3. During these periods of time transistor switches at the full load current, which is 15 A. During the 1st turn-off the dv/dt of $V_{ds}$ is measured and during the 2nd turn-on the di/dt of $I_d$ is measured. Current and voltage overshoots are also monitored.

A close-up on the 1st turn-off of the SiC VJFET can be observed in Figure 7.16.

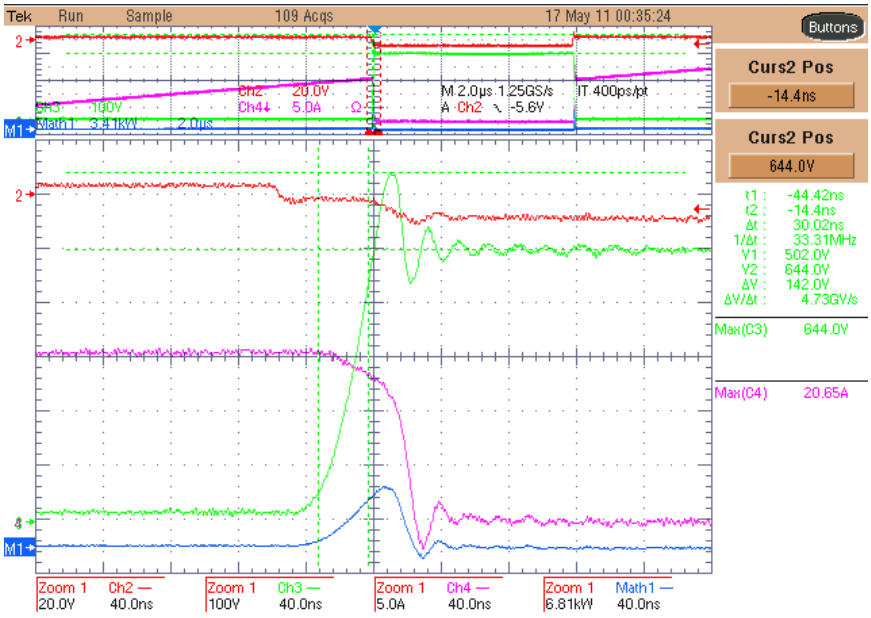



**Figure 7.16. SiC VJFET switching waveforms, 1st turn-off. Ch2 (red, 20 V/div) – Gate-source voltage Vgs, Ch3 (green, 100 V/div) – Drain-source voltage Vds, Ch4 (purple, 5 A/div) – Drain current Id, M1 (blue) – switching power dissipation.**

The measured rise time of the drain-source voltage Vds starting from on-state value to off-state value of 500 V is 30 ns resulting in a dv/dt of 4.73 kV/µs. The voltage overshoot is 142 V with Vds peak value of 642 V. A close-up on the 2nd turn-on of the SiC VJFET can be observed in Figure 7.17.

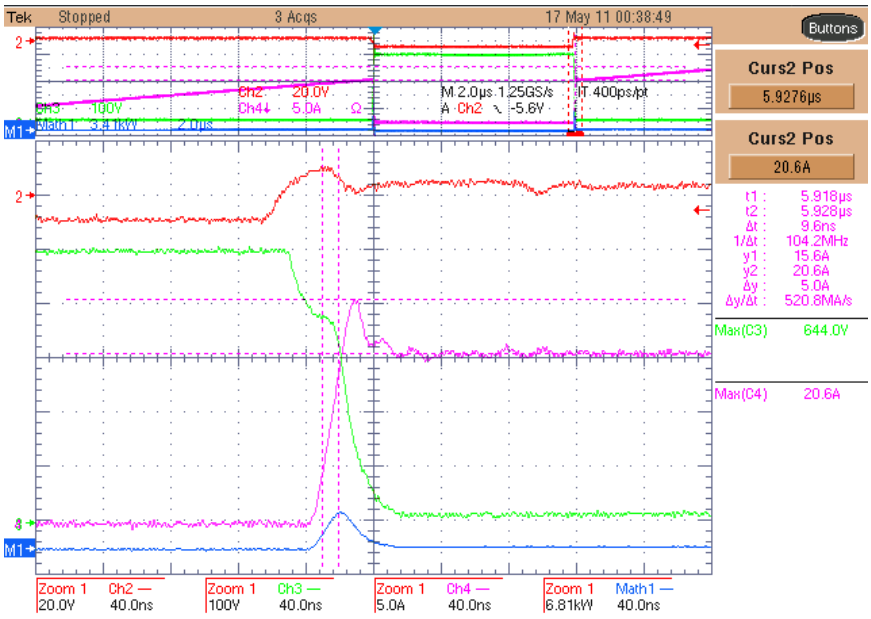



**Figure 7.17. SiC VJFET switching waveforms, 2nd turn-on. Ch2 (red, 20 V/div) – Gate-source voltage Vgs, Ch3 (green, 100 V/div) – Drain-source voltage Vds, Ch4 (purple, 5 A/div) – Drain current Id, M1 (blue) – switching power dissipation.**

The measured rise time of the drain current Id is 9.6 ns resulting in a di/dt of 0.52 A/ns. The current overshoot is 5 A with Id peak value of 20.6 A. The switching energy measurements for this experiment are summarized in Table 7.6.

**Table 7.6. Switching energy results for Vg = +/- 9 V and Rg = 2.2 Ω**

| | Switching energy | | |
|---|---|---|---|
| | **Id = 15 A** | **Id = 10 A** | **Id = 5 A** |
| **Eoff (uJ)** | 247 | 129 | 44.4 |
| **Eon (uJ)** | 97.3 | 53.8 | 28.5 |
| **Total (uJ)** | 344.3 | 182.8 | 72.9 |

Figure 7.18 shows the switching energy chart based on the results from Table 7.6.

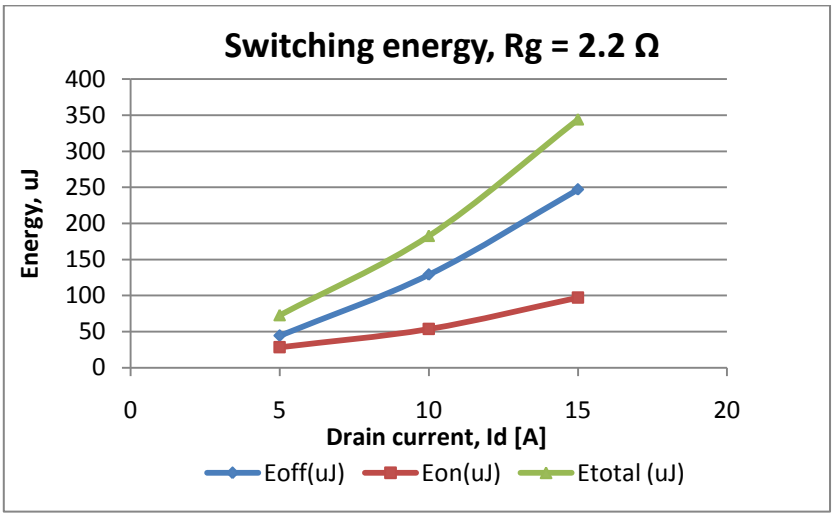



**Figure 7.18. SiC VJFET switching energy chart for Rg = 2.2 Ω**

### 7.2.2. Rg = 3.4 Ω

A close-up on the 1st turn-off of the SiC VJFET can be observed in Figure 7.19.

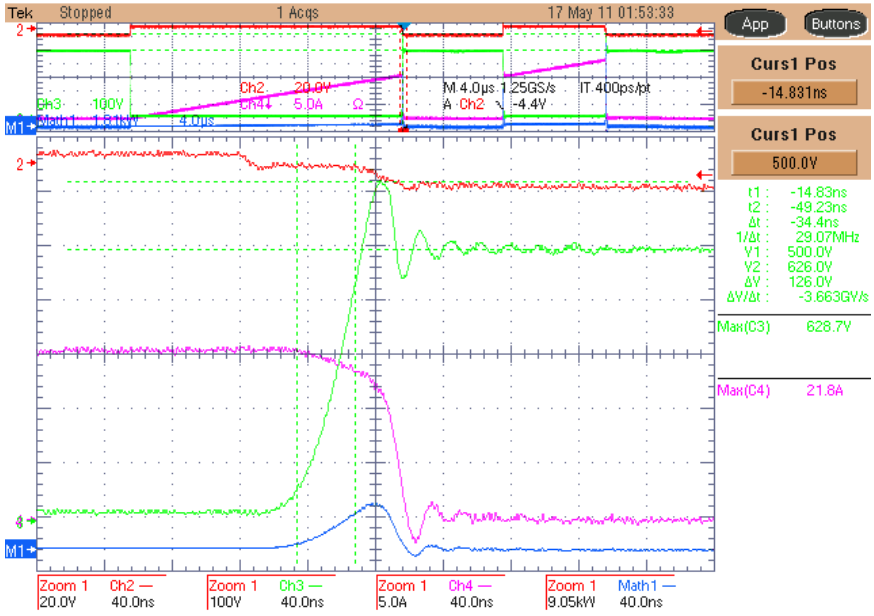



**Figure 7.19. SiC VJFET switching waveforms, 1st turn-off. Ch2 (red, 20 V/div) – Gate-source voltage Vgs, Ch3 (green, 100 V/div) – Drain-source voltage Vds, Ch4 (purple, 5 A/div) – Drain current Id, M1 (blue) – switching power dissipation.**

The measured rise time of the drain-source voltage Vds starting from on-state value to off-state value of 500 V is 34.4 ns resulting in a dv/dt of 3.66 kV/µs. The voltage overshoot is 126 V with Vds peak value of 626 V. A close-up on the 2nd turn-on of the SiC VJFET can be observed in Figure 7.20.

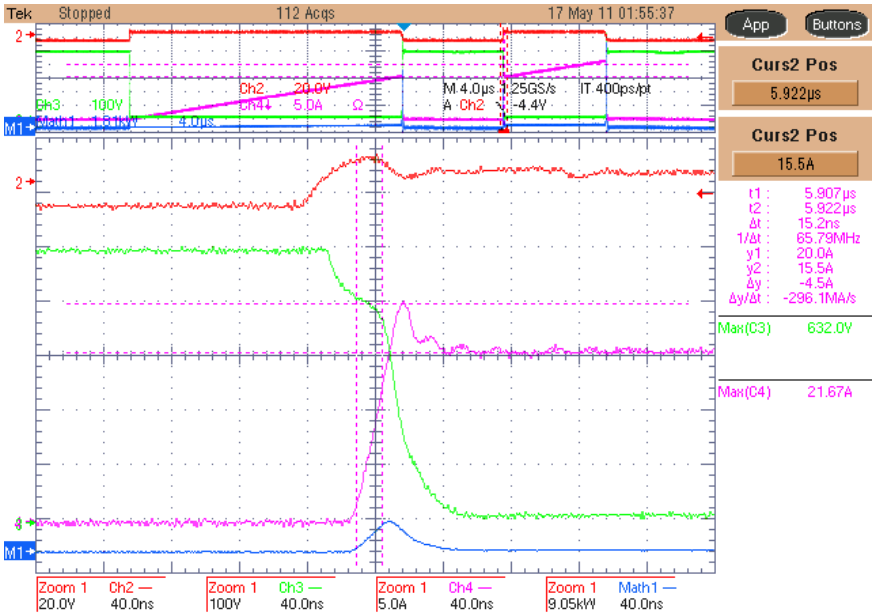



**Figure 7.20. SiC VJFET switching waveforms, 2nd turn-on. Ch2 (red, 20 V/div) – Gate-source voltage Vgs, Ch3 (green, 100 V/div) – Drain-source voltage Vds, Ch4 (purple, 5 A/div) – Drain current Id, M1 (blue) – switching power dissipation.**

The measured rise time of the drain current Id is 15.2 ns resulting in a di/dt of 0.3 A/ns. The current overshoot is 4.5 A with Id peak value of 20 A. The switching energy measurements for this experiment are summarized in Table 7.7.

**Table 7.7. Switching energy results for Vg = +/- 9 V and Rg = 3.4 Ω**

**Switching energy**

| | Id = 15 A | Id = 10 A | Id = 5 A |
|---|---|---|---|
| **Eoff (uJ)** | 281 | 149 | 53.8 |
| **Eon (uJ)** | 130 | 74.1 | 40.7 |
| **Total (uJ)** | 411 | 223.1 | 94.5 |

Figure 7.21 shows the switching energy chart based on the results from Table 7.7.

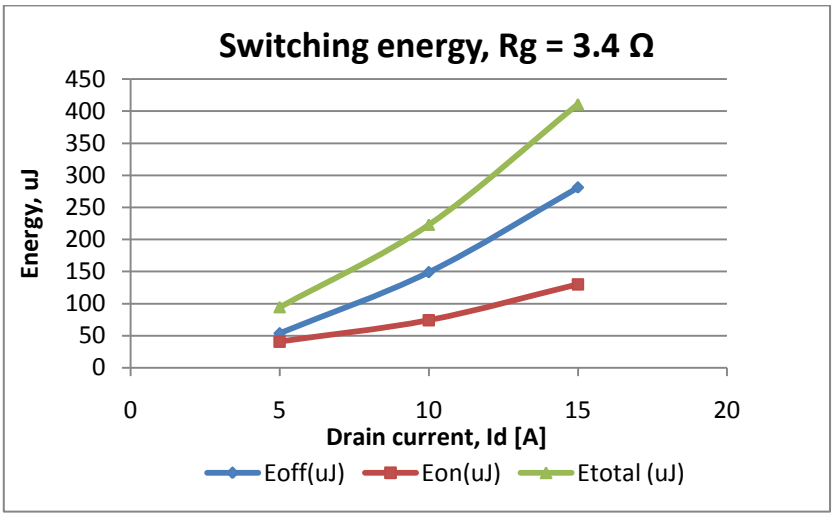



**Figure 7.21. SiC VJFET switching energy chart for Rg = 3.4 Ω**

### 7.2.3. Rg = 6.8 Ω

A close-up on the 1st turn-off of the SiC VJFET can be observed in Figure 7.22.

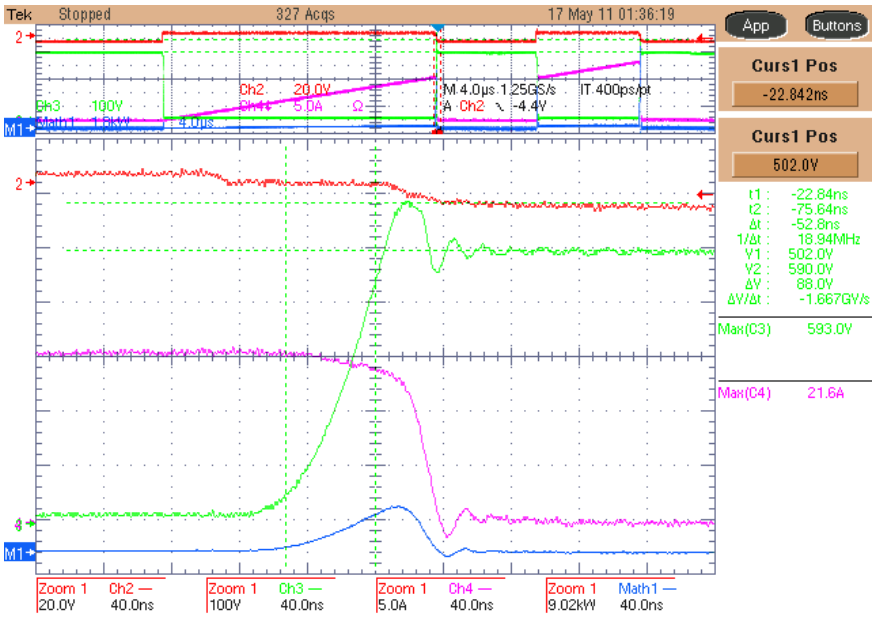



**Figure 7.22. SiC VJFET switching waveforms, 1st turn-off. Ch2 (red, 20 V/div) – Gate-source voltage Vgs, Ch3 (green, 100 V/div) – Drain-source voltage Vds, Ch4 (purple, 5 A/div) – Drain current Id, M1 (blue) – switching power dissipation.**

The measured rise time of the drain-source voltage Vds starting from on-state value to off-state value of 500 V is 52.8 ns resulting in a dv/dt of 1.67 kV/µs. The voltage overshoot is 88 V with Vds peak value of 590 V. A close-up on the 2nd turn-on of the SiC VJFET can be observed in Figure 7.23.

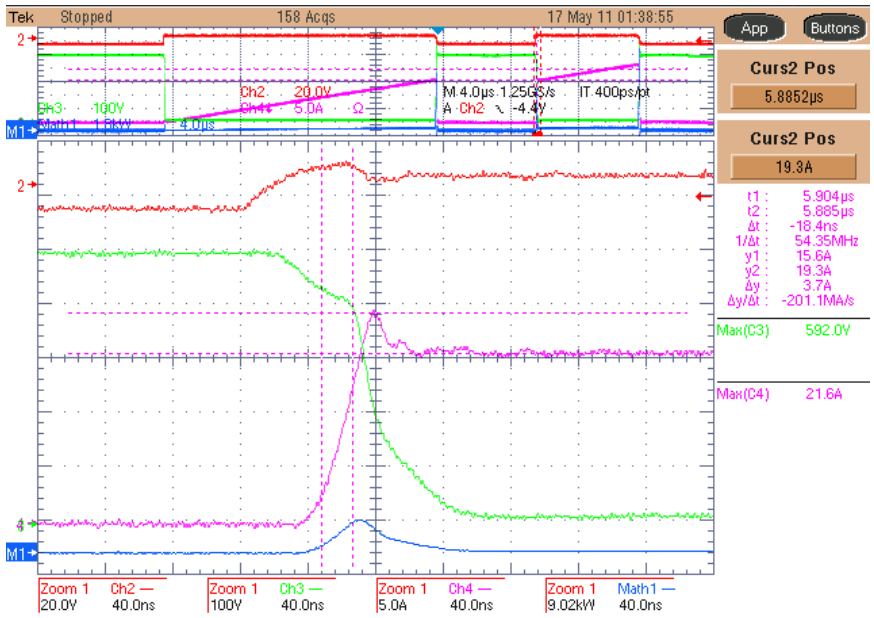



**Figure 7.23. SiC VJFET switching waveforms, 2nd turn-on. Ch2 (red, 20 V/div) – Gate-source voltage Vgs, Ch3 (green, 100 V/div) – Drain-source voltage Vds, Ch4 (purple, 5 A/div) – Drain current Id, M1 (blue) – switching power dissipation.**

The measured rise time of the drain current Id is 18.4 ns resulting in a di/dt of 0.2 A/ns. The current overshoot is 3.7 A with Id peak value of 19.3 A. The switching energy measurements for this experiment are summarized in Table 7.8.

Table 7.8. Switching energy results for Vg = +/- 9 V and Rg = 6.8 Ω

**Switching energy**

| | Id = 15 A | Id = 10 A | Id = 5 A |
|---|---|---|---|
| **Eoff (uJ)** | 377 | 206 | 79.8 |
| **Eon (uJ)** | 198 | 121 | 68.3 |
| **Total (uJ)** | 575 | 327 | 148.1 |

Figure 7.24 shows the switching energy chart based on the results from Table 7.8.

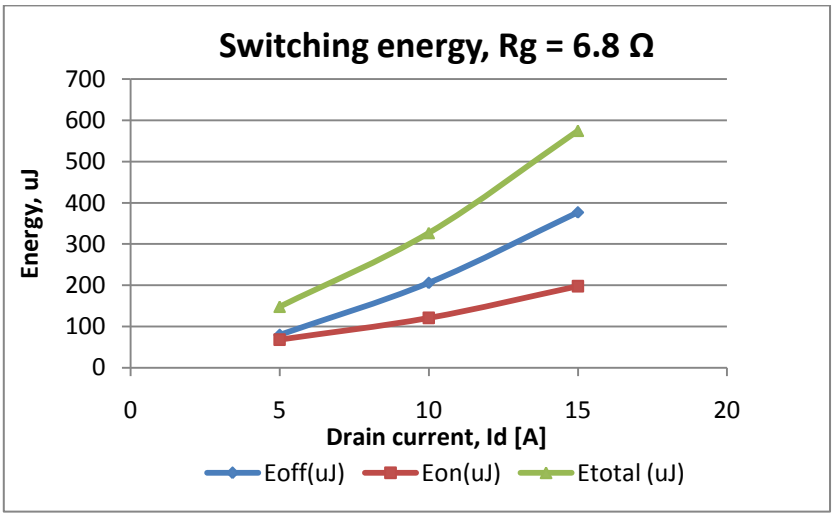



Figure 7.24. SiC VJFET switching energy chart for Rg = 6.8 Ω

## 7.3. Experiment #3 - Variable gate voltage Vg

The objective of the first experiment was to find the influence of different gate supply voltage values on the switching characteristics of SiC VJFET.

The results from the previous experiment revealed that the gate resistance Rg value of 3.4 Ω gives the optimal relationship between the switching speed/losses and the di/dt together with the both the drain current and drain-source voltage overshoots. This value is therefore chosen as the default gate resistance value for the next experiments. ***The result from the combination of Rg = 3.4 Ω and Vg = +/- 9 V is already shown in the previous section.***

### 7.3.1. Vg = +/- 12 V

A close-up on the 1st turn-off of the SiC VJFET can be observed in Figure 7.25.

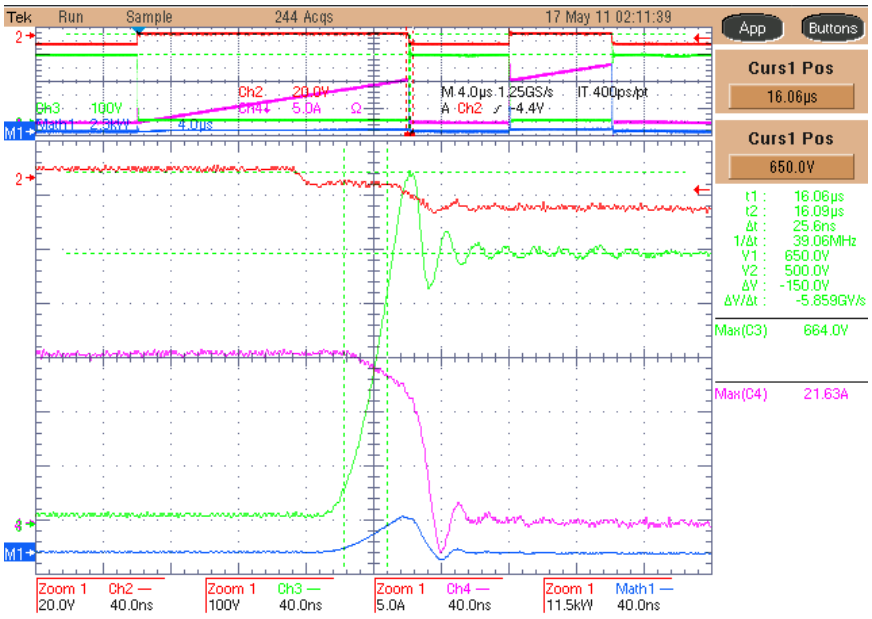



**Figure 7.25. SiC VJFET switching waveforms, 1st turn-off. Ch2 (red, 20 V/div) – Gate-source voltage Vgs, Ch3 (green, 100 V/div) – Drain-source voltage Vds, Ch4 (purple, 5 A/div) – Drain current Id, M1 (blue) – switching power dissipation.**

The measured rise time of the drain-source voltage Vds starting from on-state value to off-state value of 500 V is 25.6 ns resulting in a dv/dt of 5.86 kV/µs. The voltage overshoot is 150 V with Vds peak value of 650 V. A close-up on the 2nd turn-on of the SiC VJFET can be observed in Figure 7.26.

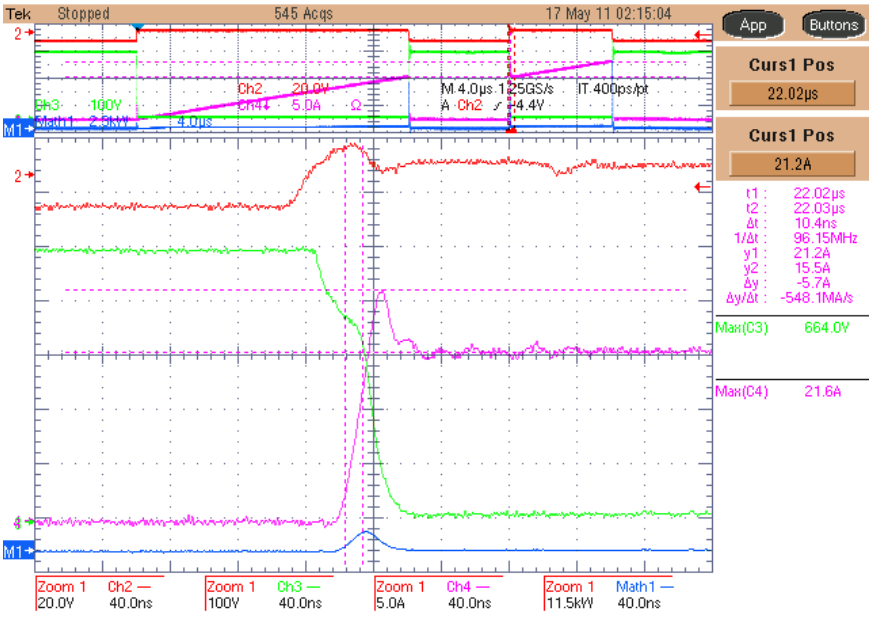



**Figure 7.26. SiC VJFET switching waveforms, 2nd turn-on. Ch2 (red, 20 V/div) – Gate-source voltage Vgs, Ch3 (green, 100 V/div) – Drain-source voltage Vds, Ch4 (purple, 5 A/div) – Drain current Id, M1 (blue) – switching power dissipation.**

The measured rise time of the drain current Id is 10.4 ns resulting in a di/dt of 0.55 A/ns. The current overshoot is 5.7 A with Id peak value of 21.2 A. The switching energy measurements for this experiment are summarized in Table 7.9.

**Table 7.9. Switching energy results for Vg = +/- 12 V and Rg = 3.4 Ω**

| | Switching energy | | |
|---|---|---|---|
| | **Id = 15 A** | **Id = 10 A** | **Id = 5 A** |
| **Eoff (uJ)** | 239 | 124 | 44 |
| **Eon (uJ)** | 76.1 | 44.3 | 24.4 |
| **Total (uJ)** | 315.1 | 168.3 | 68.4 |

Figure 7.27 shows the switching energy chart based on the results from Table 7.9.

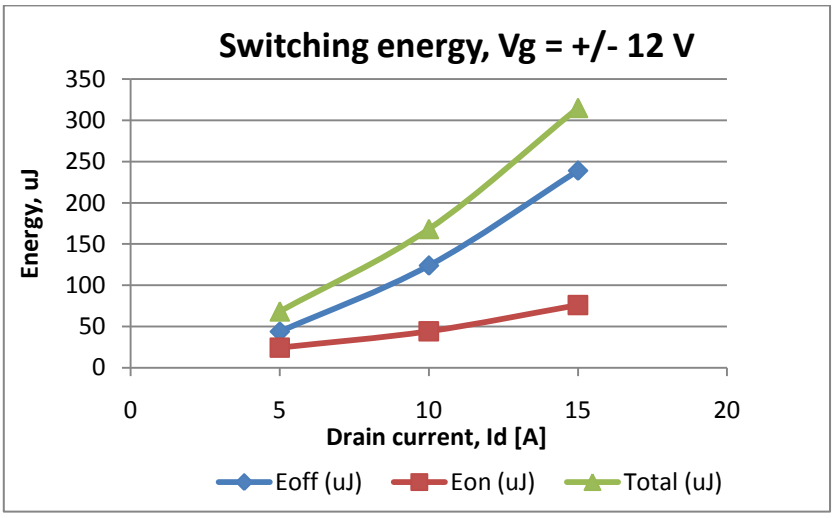



**Figure 7.27. SiC VJFET switching energy chart for Vg = +/- 12 V**

### 7.3.2. Vg = +/- 15 V

A close-up on the 1st turn-off of the SiC VJFET can be observed in Figure 7.28.

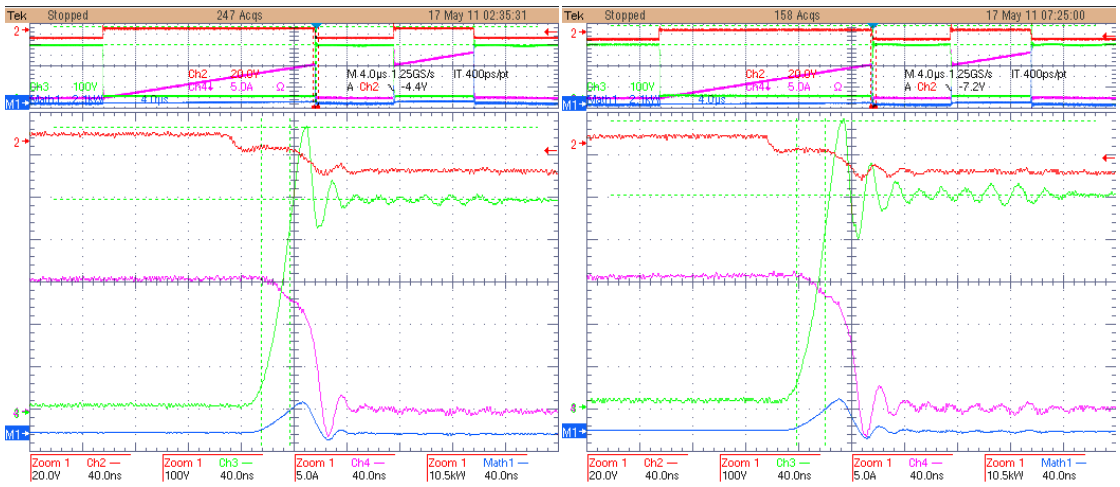


**Figure 7.28. SiC VJFET switching waveforms, 1st turn-off. Ch2 (red, 20 V/div) – Gate-source voltage Vgs, Ch3 (green, 100 V/div) – Drain-source voltage Vds, Ch4 (purple, 5 A/div) – Drain current Id, M1 (blue) – switching power dissipation. Left: with RC snubber. Right: without RC snubber.**

The analysis provided will be addressed to the case with RC snubber connected across the dc-link. The measured rise time of the drain-source voltage Vds starting from on-state value to off-state value of 500 V is 21.6 ns resulting in a dv/dt of 7.96 kV/µs. The voltage overshoot is 172 V with Vds peak value of 650 V. The rise and fall times were not affected by the absence of RC snubber, though the voltage peak was slightly increased. It is also seen from Figure 7.28 that RC snubber yields cleaner waveforms and provides faster high frequency oscillation damping.

A close-up on the 2nd turn-on of the SiC VJFET can be observed in Figure 7.29.

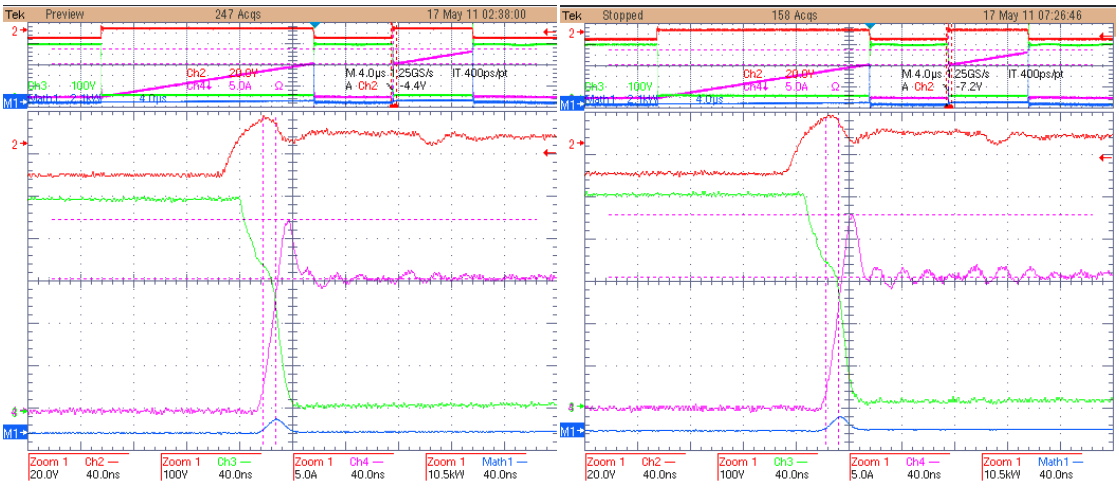


**Figure 7.29. SiC VJFET switching waveforms, 2nd turn-on. Ch2 (red, 20 V/div) – Gate-source voltage Vgs, Ch3 (green, 100 V/div) – Drain-source voltage Vds, Ch4 (purple, 5 A/div) – Drain current Id, M1 (blue) – switching power dissipation. Left: with RC snubber. Right: without RC snubber.**

As in the previous case, the analysis provided will be first addressed to the case with RC snubber connected across the dc-link. The measured rise time of the drain current Id is 9.6 ns

resulting in a di/dt of 0.72 A/ns. The current overshoot is 6.9 A with Id peak value of 22.4 A. Also in this case the rise and fall times were not affected by the absence of RC snubber. Only the current peak was increased. Figure 7.29 shows that RC snubber yields cleaner waveforms and provides faster damping of high frequency oscillations. The switching energy measurements for this experiment are summarized in Table 7.10.

**Table 7.10. Switching energy results for Vg = +/- 15 V and Rg = 3.4 Ω**

**Switching energy**

| | Id = 15 A | | Id = 10 A | | Id = 5 A | |
|---|---|---|---|---|---|---|
| | RC snubber | Without RC snubber | RC snubber | Without RC snubber | RC snubber | Without RC snubber |
| **Eoff (uJ)** | 207 | 208 | 105 | 105 | 37.7 | 37.2 |
| **Eon (uJ)** | 46.5 | 44.2 | 26.5 | 25.5 | 14.8 | 14.3 |
| **Total (uJ)** | 253.5 | 252.2 | 131.5 | 130.5 | 52.5 | 51.5 |

Figure 7.30 shows the switching energy chart based on the results from Table 7.10.

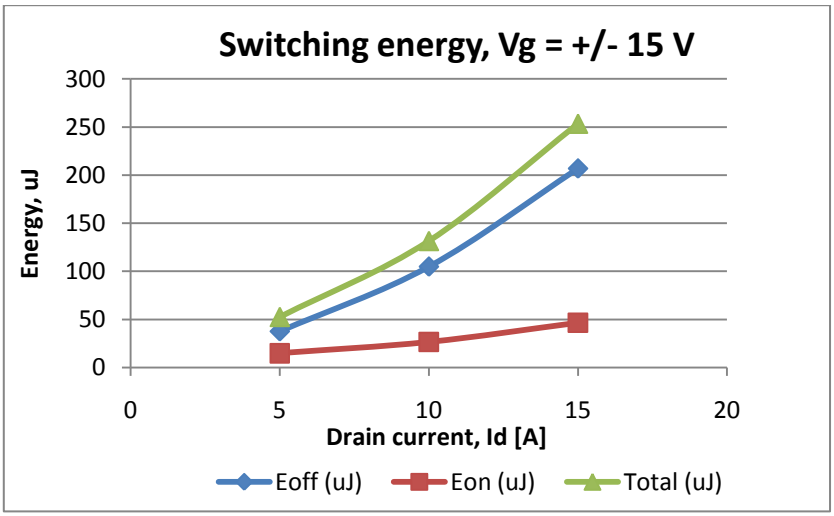



**Figure 7.30. SiC VJFET switching energy chart for Vg = +/- 15 V**

Figure 7.31 shows the influence of the lower side transistor switching on the upper side transistor gate.

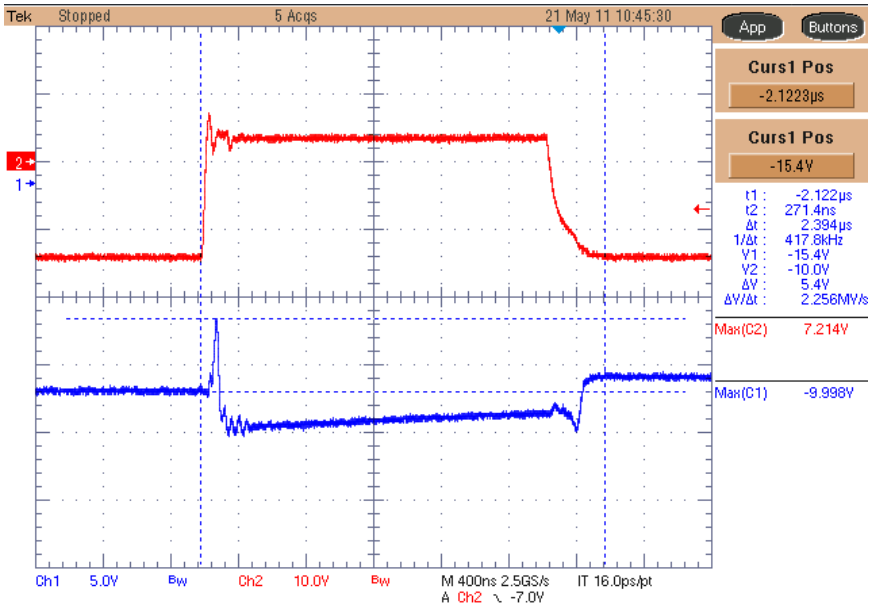



**Figure 7.31. The effect of switching the lower transistor on upper transistor gate. Ch2 (Red, 10 V/div) - Lower transistor gate voltage. Ch1 (Blue, 5 V/div) - Upper transistor gate voltage.**

It can be seen that when the lower transistor turns-on a glitch appears on the upper transistor gate. This glitch has reached -10 V though which in this case is far from the threshold gate-source voltage of the SiC VJFET, i.e. 1 V. It should be mentioned that this test was performed with the Cgs connected tight across the gate-source of the device. Minimizing the inductance in the gate provides higher noise immunity of the gate, i.e. significant overvoltages/overcurrents can be avoided. ***The upper waveform shows the lower transistor gate voltage, while the lower waveform shows the upper transistor gate voltage.***

## 7.4. Experiment #4 - Change in freewheeling diodes

The objective of this experiment was to find the influence of different freewheeling diodes on the switching characteristics of SiC VJFET. It should be noted that Rg = 3.4 Ω and Vg = +/- 15 V are chosen as the default values for the next experiments. Table 7.11 shows the devices under test for this particular experiment.

**Table 7.11. Objects under test with changed freewheeling diode**

| Switch | Freewheeling diode | Gate Driver |
|---|---|---|
| SemiSouth SiC VJFET SJEP120R063 | SemiSouth S30S120 SiC Schottky diode | SemiSouth SGDR600P1 |

SiC VJFET is still used as the main power switch, but at this time the S30S120 SiC Schottky diode from SemiSouth is chosen as the freewheeling diode. The driver circuit for SiC

VJFET is the commercial two-stage gate driver from SemiSouth described in section 3.6.1. A close-up on the 1st turn-off of the SiC VJFET can be observed in Figure 7.32.

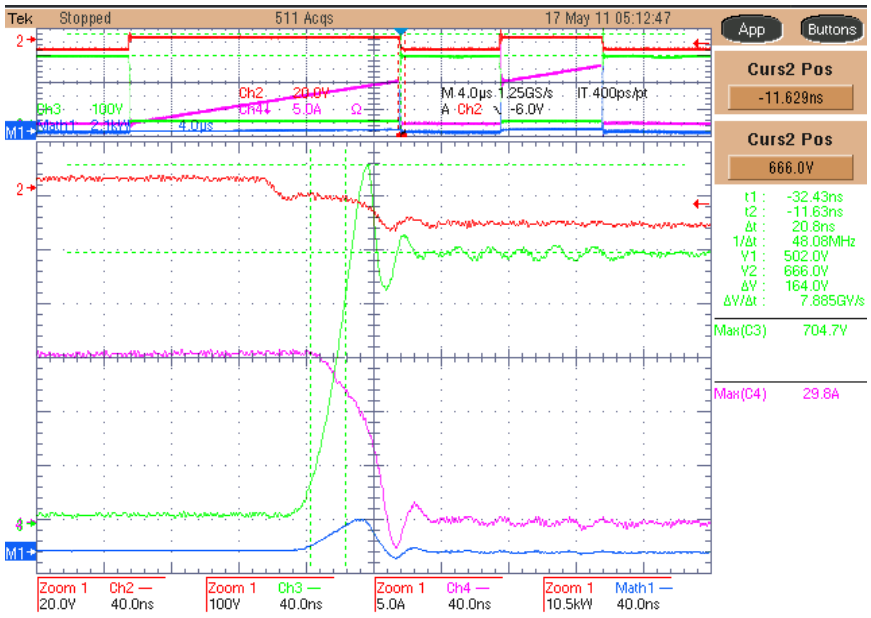



**Figure 7.32. SiC VJFET switching waveforms, 1st turn-off. Ch2 (red, 20 V/div) – Gate-source voltage Vgs, Ch3 (green, 100 V/div) – Drain-source voltage Vds, Ch4 (purple, 5 A/div) – Drain current Id, M1 (blue) – switching power dissipation.**

The measured rise time of the drain-source voltage Vds starting from on-state value to off-state value of 500 V is 20.8 ns resulting in a dv/dt of 7.89 kV/µs. The voltage overshoot is 164 V with Vds peak value of 664 V. A close-up on the 2nd turn-on of the SiC VJFET can be observed in Figure 7.33.

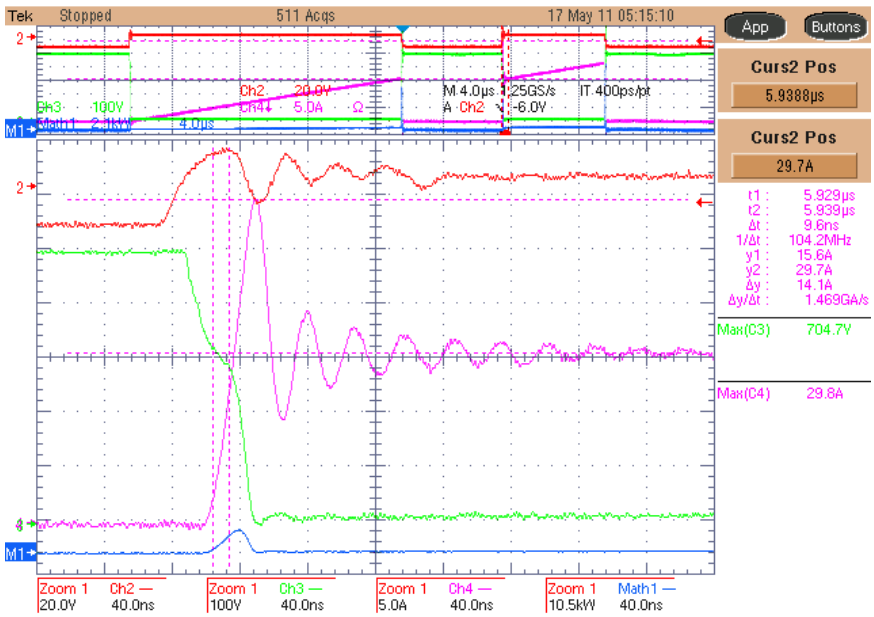



**Figure 7.33. SiC VJFET switching waveforms, 2nd turn-on. Ch2 (red, 20 V/div) – Gate-source voltage Vgs, Ch3 (green, 100 V/div) – Drain-source voltage Vds, Ch4 (purple, 5 A/div) – Drain current Id, M1 (blue) – switching power dissipation.**

The measured rise time of the drain current Id is 9.6 ns resulting in a di/dt of 1.47 A/ns. The current overshoot is 14.1 A with Id peak value of 29.7 A. The switching energy measurements for this experiment are summarized in Table 7.12.

**Table 7.12. Switching energy results for Vg = +/- 15 V and Rg = 3.4 Ω and S30S120 SiC Schottky diode**

| | Switching energy | | |
|---|---|---|---|
| | **Id = 15 A** | **Id = 10 A** | **Id = 5 A** |
| **Eoff (uJ)** | 180 | 82.8 | 28.6 |
| **Eon (uJ)** | 65.2 | 41.1 | 25.8 |
| **Total (uJ)** | 245.2 | 123.9 | 54.4 |

Figure 7.34 shows the switching energy chart based on the results from Table 7.12.

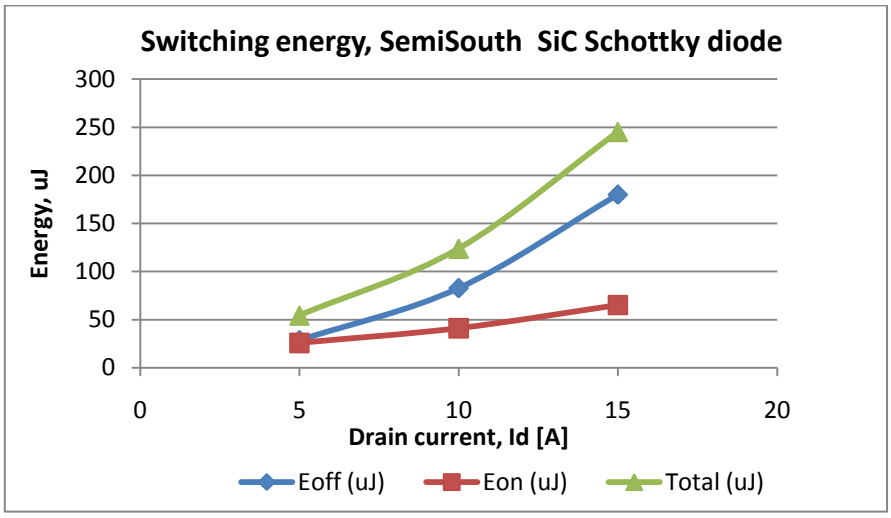



**Figure 7.34. SiC VJFET switching energy chart with SiC Schottky diode from SemiSouth**

## 7.5. Experiment #5 - SiC BJT and SiC MOSFET test with AC-coupled gate driver

This experiment was performed without RC snubber (22 Ω, 47 nF) connected across the dc-link, as well as without 2.2 nF capacitor connected across the gate-source (base-emitter) of the device.

### 7.5.1. SiC BJT

Table 7.13 shows the devices under test for this particular experiment.

**Table 7.13. Objects under test with changed gate driver circuit**

| Switch | Freewheeling diode | Gate Driver |
|---|---|---|
| TranSiC BT1206AC SiC BJT | CREE C3D20060 SiC Schottky diode | AC coupled |

SiC BJT is used as the main power switch together with the C3D20060 SiC Schottky as the freewheeling diode. The driver circuit for SiC BJT is the AC coupled gate driver described in section 3.6.3. The gate resistor value is 56 Ω and the RC combination is 2 Ω and 22 nF respectively. The waveforms showing the full cycle of the double-pulse test is shown in Figure 7.35.

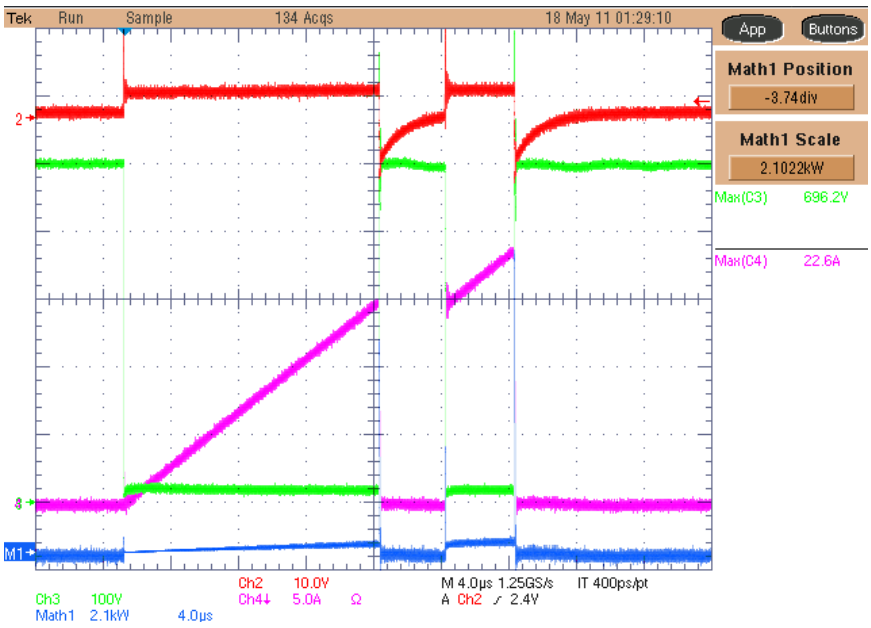



**Figure 7.35. SiC BJT switching waveforms, full cycle of double-pulse test. Ch2 (red, 10 V/div) – Base-emitter voltage Vbe, Ch3 (green, 100 V/div) – Collector-emitter voltage Vce, Ch4 (purple, 5 A/div) – collector current Ic, M1 (blue) – switching power dissipation.**

It can be observed that the shape of the gate voltage resembles the one described in section 3.6.3. The RC combination provides relatively fast turn-on and drags the gate negative for limited amount of time during the turn-off. A close-up on the 1$^{st}$ turn-off of the SiC BJT can be observed in Figure 7.36.

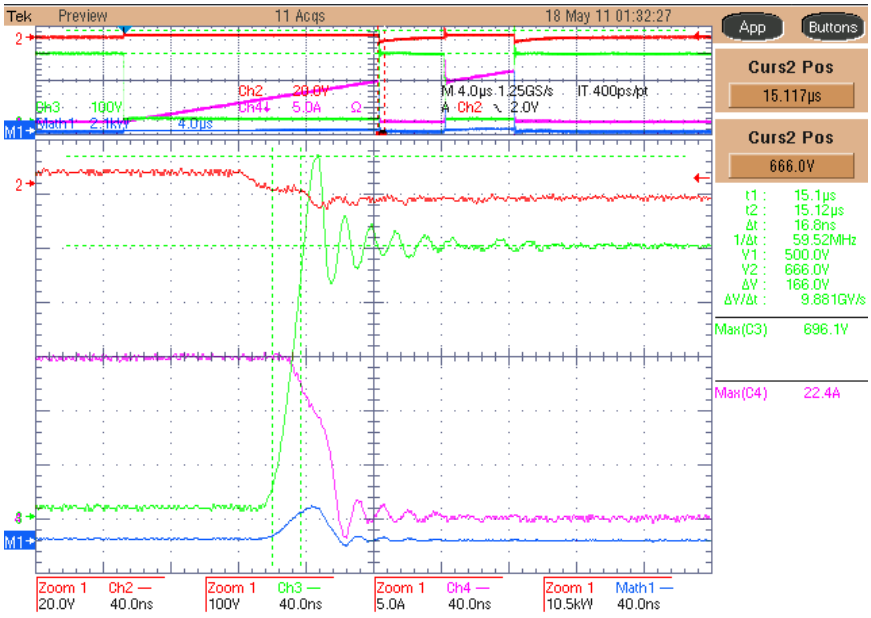



**Figure 7.36. SiC BJT switching waveforms, 1st turn-off. Ch2 (red, 20 V/div) – Base-emitter voltage Vbe, Ch3 (green, 100 V/div) – Collector-emitter voltage Vce, Ch4 (purple, 5 A/div) – collector current Ic, M1 (blue) – switching power dissipation.**

The measured rise time of the collector-emitter voltage Vce starting from on-state value to off-state value of 500 V is 16.8 ns resulting in a dv/dt of 9.89 kV/µs. The voltage overshoot is 166 V with Vce peak value of 666 V. A close-up on the 2nd turn-on of the SiC BJT can be observed in Figure 7.37.

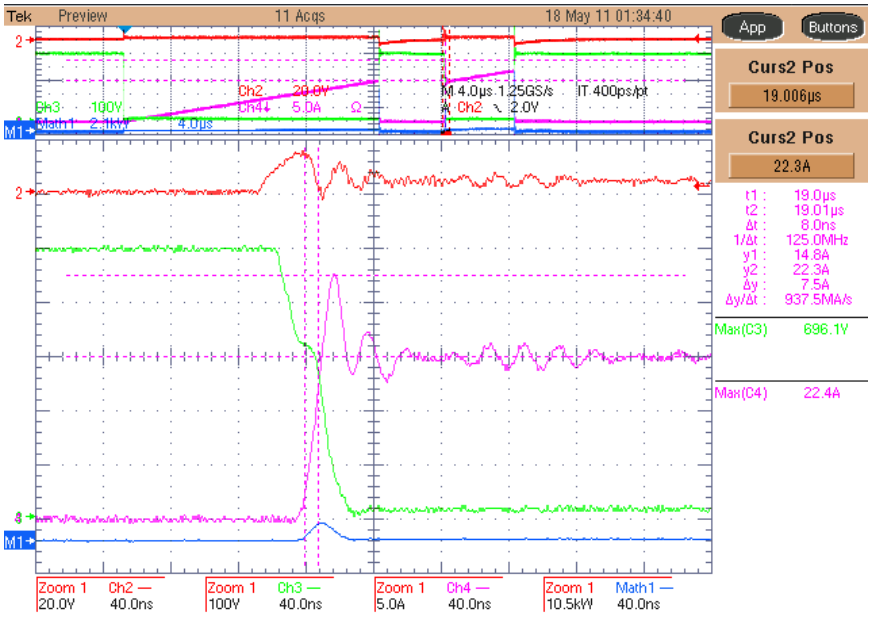



**Figure 7.37. SiC BJT switching waveforms, 2nd turn-on. Ch2 (red, 20 V/div) – Base-emitter voltage Vbe, Ch3 (green, 100 V/div) – Collector-emitter voltage Vce, Ch4 (purple, 5 A/div) – collector current Ic, M1 (blue) – switching power dissipation.**

The measured rise time of the collector current Ic is 8 ns resulting in a di/dt of 0.94 A/ns. The current overshoot is 7.5 A with Ic peak value of 22.3 A. The switching energy measurements for this experiment are summarized in Table 7.14.

**Table 7.14. Switching energy results for SiC BJT**

| | Switching energy | | |
|---|---|---|---|
| | **Id = 15 A** | **Id = 10 A** | **Id = 5 A** |
| **Eoff (uJ)** | 153 | 80 | 31.8 |
| **Eon (uJ)** | 49.4 | 40.4 | 28 |
| **Total (uJ)** | 202.4 | 120.4 | 59.8 |

Figure 7.38 shows the switching energy chart based on the results from Table 7.14.

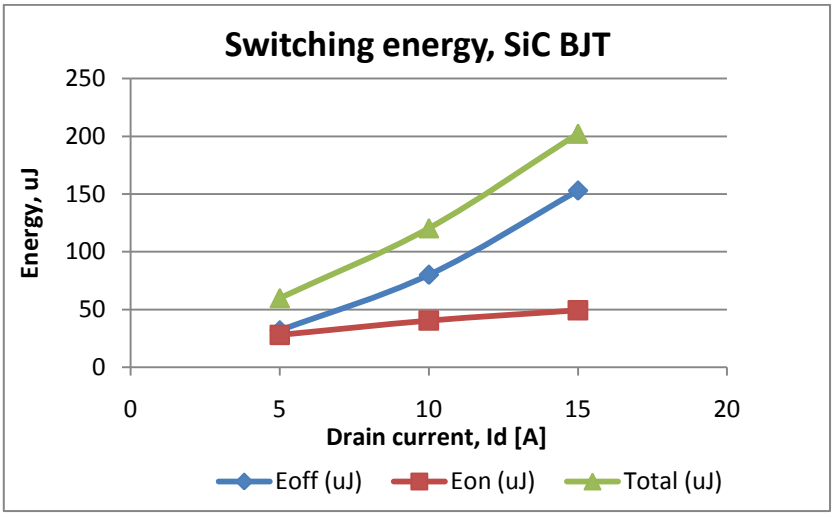



**Figure 7.38. SiC BJT switching energy chart**

### 7.5.2. SiC MOSFET

Table 7.15 shows the devices under test for this particular experiment.

**Table 7.15. Objects under test with changed gate driver circuit and SiC MOSFET as the main switch**

| Switch | Freewheeling diode | Gate Driver |
|---|---|---|
| CREE CMF20120 SiC MOSFET | CREE C3D20060 SiC Schottky diode | AC-coupled |

SiC MOSFET is used as the main power switch together with the C3D20060 SiC Schottky as the freewheeling diode. The driver circuit is the same AC coupled gate driver as in the previous experiment.

As any other power MOSFET, SiC MOSFET has a body diode, which in some applications can be used as the freewheeling diode. The use of this diode is not recommended though [21] due to high forward voltage drop. An external SiC Schottky diode is suggested. As a result, the test of this diode was not performed during the experiment. The waveforms showing the full cycle of the double-pulse test is shown in Figure 7.39.

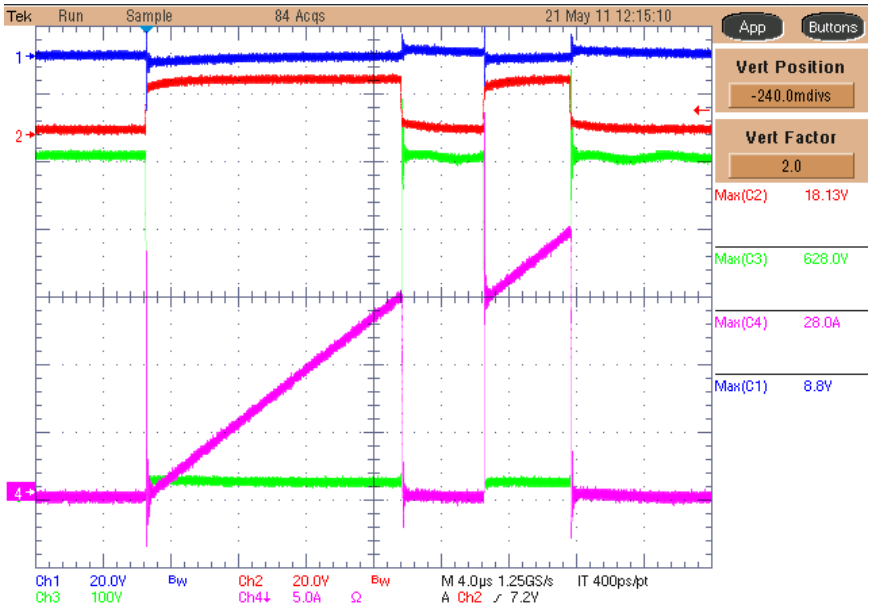



**Figure 7.39. SiC MOSFET switching waveforms, full cycle of double-pulse test. Ch1 (blue, 20 V/div) – upper transistor gate-source voltage, Ch2 (red, 20 V/div) – lower transistor gate-source voltage, Ch3 (green, 100 V/div) – Drains-source voltage Vds, Ch4 (purple, 5 A/div) – drain current Id.**

Analyzing the waveforms it can be seen that the behaviour of the gate driver circuit with SiC MOSFET is different from the one with SiC BJT, even though the same gate driver is used. The gate voltage does not go negative during the turn-off and the exponential behaviour of the gate voltage is seen during both the turn-on and turn-off.

For comparison Figure 7.40 shows the output waveforms of the gate driver connected to the gate of Si CoolMOS.

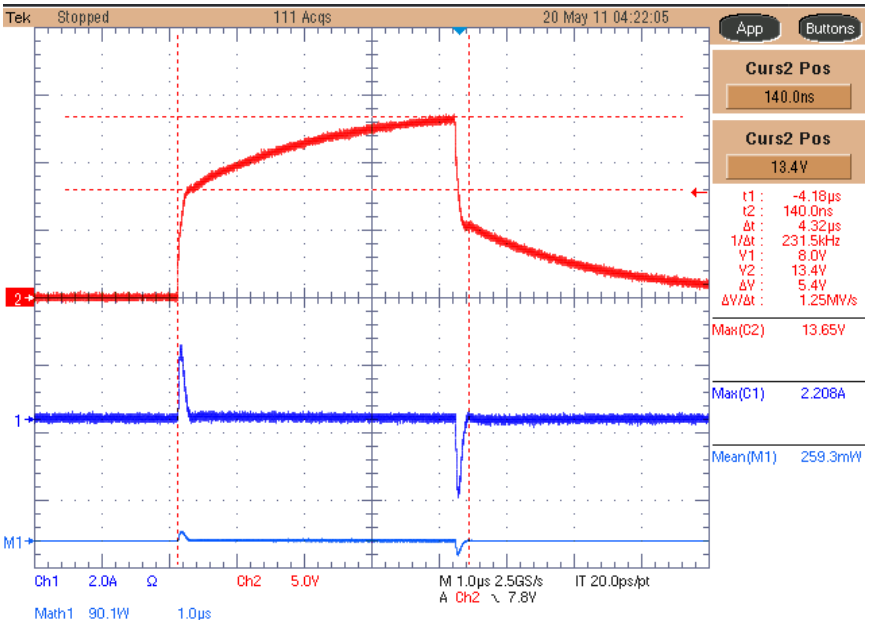



**Figure 7.40. Gate driver output waveforms. Ch2 (Red, 5 V/div) - Gate voltage. Ch1 (Blue, 2 A/div) - Gate current. M1 (light blue) - Gate power.**

As in the case of SiC MOSFET the exponential behaviour of the gate voltage is obvious as well as the fact that voltage does not become negative. The discharge of the gate capacitances occurs since both positive and negative current peaks appear in the Figure 7.40.

A close-up on the 1st turn-off of the SiC MOSFET can be observed in Figure 7.41.

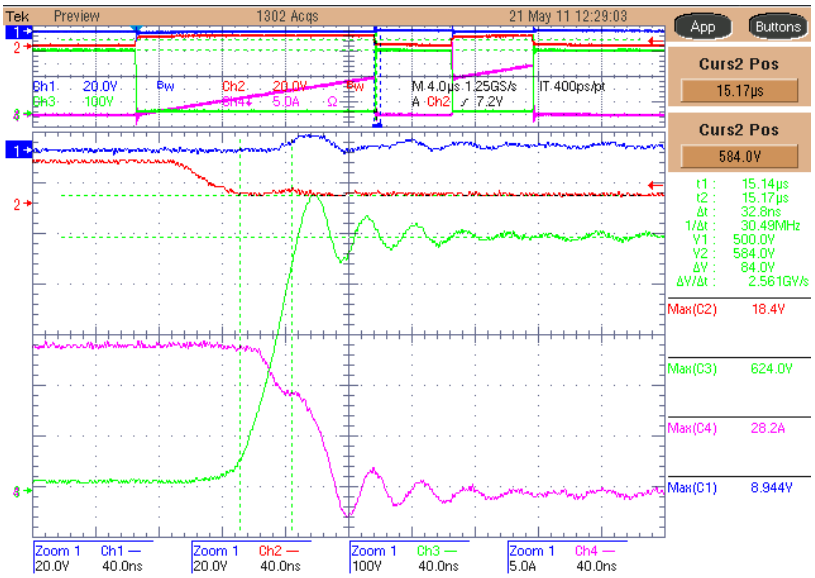



**Figure 7.41. SiC MOSFET switching waveforms, 1st turn-off. Ch1 (blue, 20 V/div) – upper transistor gate-source voltage, Ch2 (red, 20 V/div) – lower transistor gate-source voltage, Ch3 (green, 100 V/div) – Drain-source voltage Vds, Ch4 (purple, 5 A/div) – Drain current Id.**

The measured rise time of the drain-source voltage Vds starting from on-state value to off-state value of 500 V is 32.8 ns resulting in a dv/dt of 2.56 kV/µs. The voltage overshoot is 84

V with Vds peak value of 584 V. A close-up on the 2nd turn-on of the SiC MOSFET can be observed in Figure 7.42.

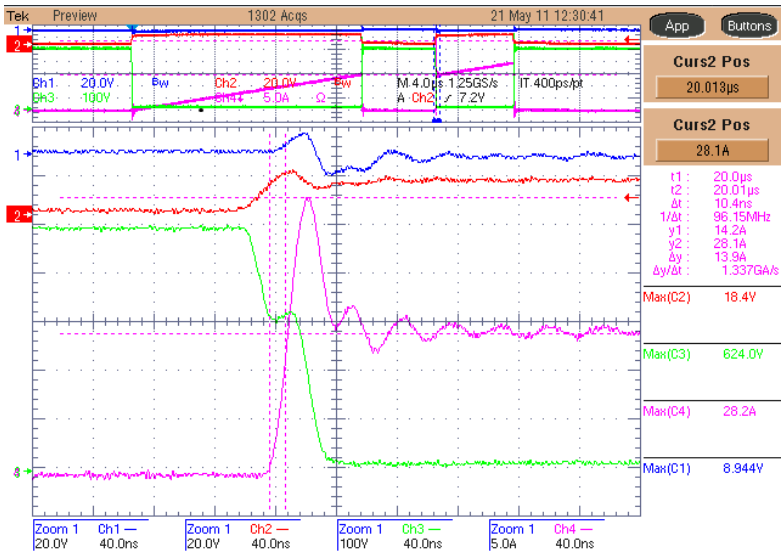



**Figure 7.42. SiC MOSFET switching waveforms, 2nd turn-on. Ch1 (blue, 20 V/div) – upper transistor gate-source voltage, Ch2 (red, 20 V/div) – lower transistor gate-source voltage, Ch3 (green, 100 V/div) – Drain-source voltage Vds, Ch4 (purple, 5 A/div) – Drain current Id.**

The measured rise time of the drain current Id is 10.4 ns resulting in a di/dt of 1.34 A/ns. The current overshoot is 13.9 A with Id peak value of 28.1 A.

Figure 7.42 reveals the Miller plateau of the SiC MOSFET. This appears as the horizontal stage of the drain-source voltage. When the device switches, the gate voltage is actually clamped to the plateau voltage and stays there until sufficient charge has been added/ removed for the device to switch. It is useful in estimating the driving requirements, because it shows the voltage of the plateau and the required charge to switch the device. Thus, one can calculate the actual gate drive resistor, for a given switching time.

The switching energy measurements for this experiment are summarized in Table 7.16.

**Table 7.16. Switching energy results for SiC MOSFET**

| | **Switching energy** | | |
|---|---|---|---|
| | **Id = 15 A** | **Id = 10 A** | **Id = 5 A** |
| **Eoff (uJ)** | 188 | 116 | 61.9 |
| **Eon (uJ)** | 137 | 97.3 | 47.7 |
| **Total (uJ)** | 325 | 213.3 | 109.6 |

Figure 7.43 shows the switching energy chart based on the results from Table 7.16.

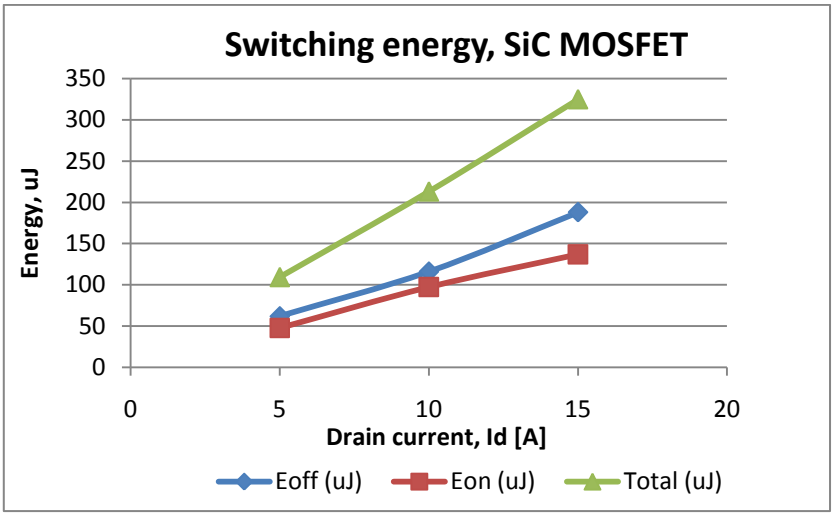



**Figure 7.43. SiC MOSFET switching energy chart**

Figure 7.44 shows the influence of the lower side transistor switching on the upper side transistor gate.

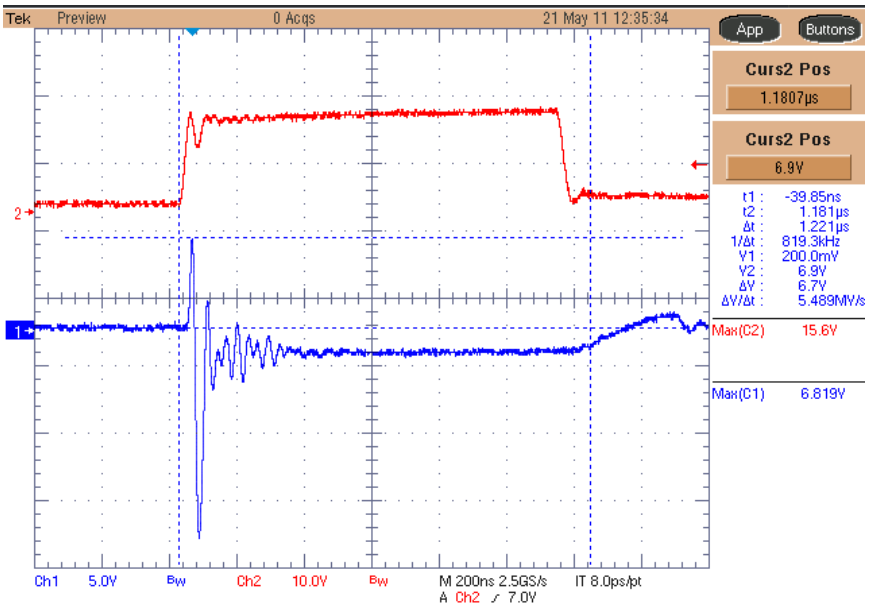



**Figure 7.44. The effect of switching the lower SiC MOSFET on upper transistor gate. Ch2 (Red, 10 V/div) - Lower transistor gate voltage. Ch1 (Blue, 5 V/div) - Upper transistor gate voltage.**

As in the previous case with SiC VJFET, SiC MOSFETs connected in bridge configuration experience mutual interference. It can be seen that when the lower transistor turns-on a glitch appears on the upper transistor gate. This glitch has reached an impressive value of almost 7 V, which is 4 V above the actual threshold voltage, without causing the shoot-through of the bridge leg. This is an interesting fact that is worth to be studied more closely. It should be mentioned that this test was performed without the Cgs connected across the gate-source of the device and the gate driver circuit used is not providing a fixed negative bias during the turn-off.

A solution to reduce the glitches is to minimize the inductance in the gate which yields higher noise immunity, consequently significant overvoltages can be avoided. ***The upper waveform shows the lower transistor gate voltage, while the lower waveform shows the upper transistor gate voltage.***

# 8. ANALYSIS OF OBTAINED RESULTS

This chapter contains a comparative analysis of the results obtained in chapter 7 and chapter 5.

## 8.1. Simulation results

The results from simulated circuit showed a good approximation of what the output of the laboratory prototype should look like. The simulated gate driver design was split into sections to be able to find all the issues on the way to final circuit simulation. Almost all of the sections showed the expected output behaviour compared to the expectations. The turn-off stage (section 4.4.6) introduced some confusion since rather slow turn-off behaviour was observed (Figure 5.13). The final simulation result is sufficient enough and coincides well with the output of the commercial gate driver circuit from SemiSouth (Figure 3.15).

## 8.2. Measurement results

In this section the results obtained during the laboratory experiments will be analyzed and compared. The main effort during measurements was put on driving SiC VJFET and its switching behaviour. As discussed in section 2.4.1 SiC VJFETs are considered as the replacement for Si MOSFETs and IGBTs in a variety of applications.

### 8.2.1. Gate measurements

The analysis and comparison of performance of the designed two-stage gate driver for SiC VJFET with commercial SiC VJFET gate driver revealed similar switching behaviour. Though due to multiple design imperfections of the proposed driver the commercial driver appears to be more optimized and tuned, especially when the switching losses of SiC VJFET are concerned. Table 8.1 shows the obtained output characteristics comparison for both gate driver circuits.

**Table 8.1. A comparison of output characteristics of proposed and commercial SiC VJFET gate driver**

| *Gate driver* | *Peak voltage, V* | *Peak current, A* | *Mean power, W* |
|---|---|---|---|
| ***Proposed*** | 4.75 | 6.92 | 1.56 |
| ***SemiSouth*** | 7.6 | 5.8 | 2.33 |

Despite lower peak voltage a 6.92 A peak current has been achieved thus proving the high output current capability of the designed driver. The mean power is slightly lower with a value of 1.56 W compared to 2.33 W in the SemiSouth case. The lower power demand can be explained by the fact that the turn-off loss is almost absent due to slow turn-off. Another reason is the lower instantaneous loss during fast turn-on transition. Both drivers show the requirement of relatively powerful supply for the SiC VJFET gate driver.

Table 8.2 summarizes the results of actual switching performance of both gate driver circuits in the double-pulse test. It should once again be emphasized that these measurements were performed in different laboratory conditions and probably the most important thing is that the drain voltage in the case of proposed gate driver circuit is only 300 V, due to laboratory equipment limitations. Other differences in the measurement setups can be found in chapter 6 and section 7.1.3.1.

**Table 8.2. A comparison of switching characteristics of proposed and commercial SiC VJFET gate driver**

| *Gate driver* | *Vds, V* | *Id, A* | *Turn-off* | | | *Turn-on* | | |
|---|---|---|---|---|---|---|---|---|
| | | | ***Time, ns*** | ***Overshoot, V*** | ***Energy, uJ*** | ***Time, ns*** | ***Overshoot, A*** | ***Energy, uJ*** |
| ***Proposed*** | 300 | 15 | 164 | 44 | 310.6 | 14.4 | 8 | 37.1 |
| ***SemiSouth*** | 500 | 15 | 30 | 142 | 247 | 9.6 | 5 | 97.3 |

As expected, the results are diversified due to different measurement conditions as well as the difference in gate driver turn-off circuit operation. The turn-off time of SiC VJFET with the proposed gate driver is nearly 6 times slower than for the case with SemiSouth driver. Though, the overshoot is more than 3 times lower. The turn-on results are quite similar proving the effectiveness of the designed buffer stage. The important thing to mention is a high drain current overshoot, despite lower drain voltage which reveals the layout problems in the setup.

### 8.2.2. Other measurements

Figure 8.1 shows a comparison of total switching energy losses of SiC VJFET when the external gate resistor is varied between the values 2.2 Ω, 3.4 Ω and 6.8 Ω.

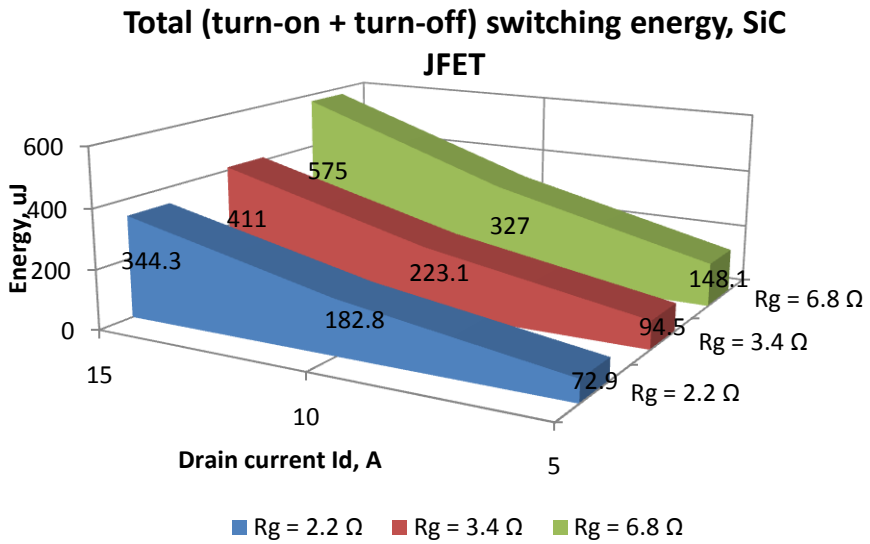



**Figure 8.1. Total switching energy comparison of SiC VJFET with variable Rg**

Analyzing the chart in Figure 8.1 it can be observed that total switching energy increases proportionally with increased gate resistor value as well as the drain current Id. This corresponds well with what was expected since the higher gate resistor value slows down the switching transition. This in turn increases the time the switch spends in the active region where the power dissipation is high. On the other hand, section 7.2 reveals another interesting fact. By increasing the gate resistor from 2.2 Ω to 6.8 Ω the turn-off voltage overshoot was reduced from 142 V to 88 V. The current overshoot decreased from 5 A to 3.7 A. Figure 8.2 shows a comparison of switching times when the gate resistor is varied.

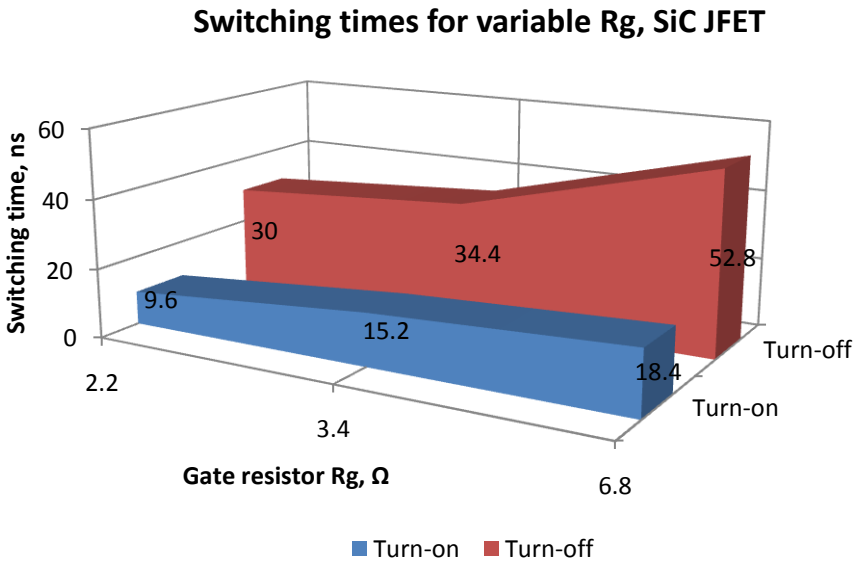



Figure 8.2. Switching time comparison of SiC VJFET with variable Rg

The results once again prove that the speed indeed decreases with increased gate resistor value. The influence of the gate resistor is especially sensed in the turn-off case.

Figure 8.3 shows a comparison of switching times of SiC VJFET when the gate voltage is varied between the values +/- 9 V, +/- 12 V and +/- 15 V.

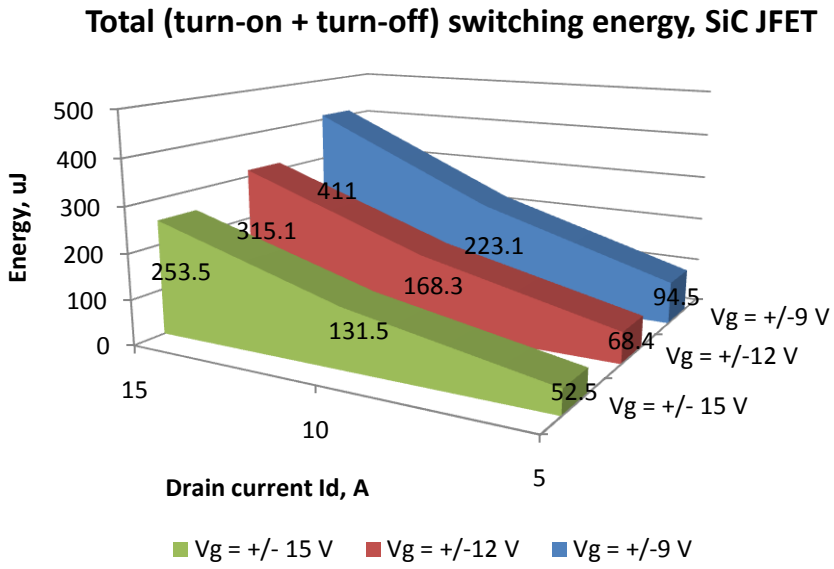



Figure 8.3. Total switching energy comparison of SiC VJFET with variable Vg

Observing the case with variable gate voltage seen in Figure 8.3 it can be concluded that the switching energy decreases with increased gate voltage. This is due to the fact that higher gate voltages yield higher switching speed. Consequently, the device spends less time in the

active region and the losses are therefore decreased. This fact is confirmed in Figure 8.4, where the results for switching times versus applied gate voltage are shown.

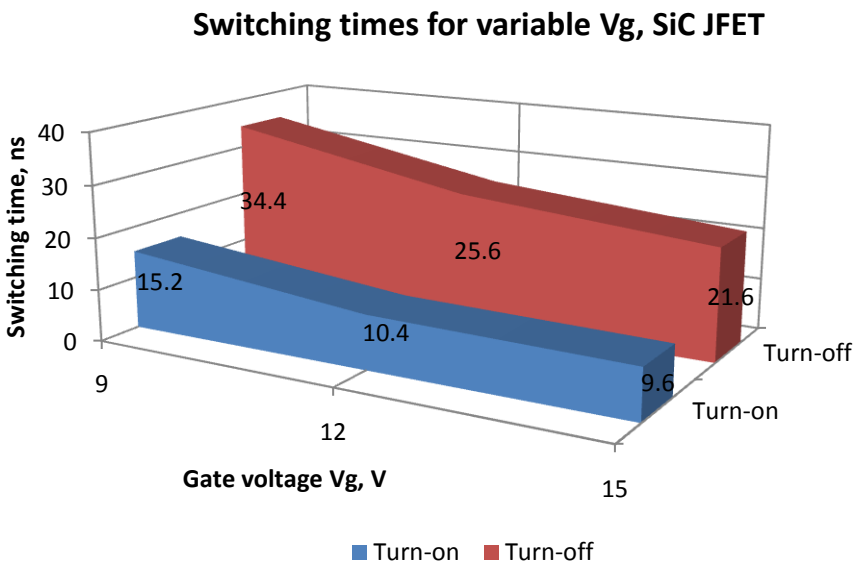



**Figure 8.4. Switching time comparison of SiC VJFET with variable Vg**

A comparison of switching energy results for the case when different freewheeling diodes are used can be seen in Figure 8.5.

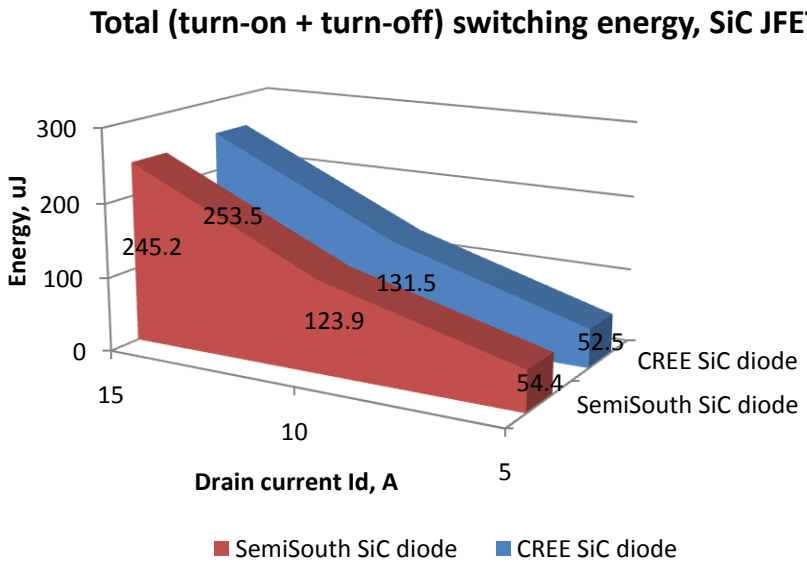



**Figure 8.5. Total switching energy comparison of SiC VJFET with different freewheeling diodes**

Both SiC Schottky diodes showed similar switching energy results. An analysis of the switching waveforms (Figure 7.28, Figure 7.29, Figure 7.32 and Figure 7.33) of SiC VJFET with different diodes revealed significant differences. In both cases the turn-on/off times were comparable with 9.6 ns/21.6 ns for CREE diode and 9.6 ns/20.8 ns for SemiSouth diode respectively. The current overshoot in the case of SemiSouth diode reached and impressive value of 14.1 A, while this value was only 6.9 A for CREE diode. It should be noted that such current spikes produce EMI issues and in some applications can be critical. As a result, this diode is not recommended to use as the freewheeling diode in the bridge configurations.

Figure 8.6 shows a comparison of total switching energy losses of different SiC transistors as a function of drain current. ***Same gate driver circuit (section 3.6.3) was used for driving the SiC BJT and SiC MOSFET, while the gate driver for SiC VJFET was the commercial driver from SemiSouth (section 3.6.1).***

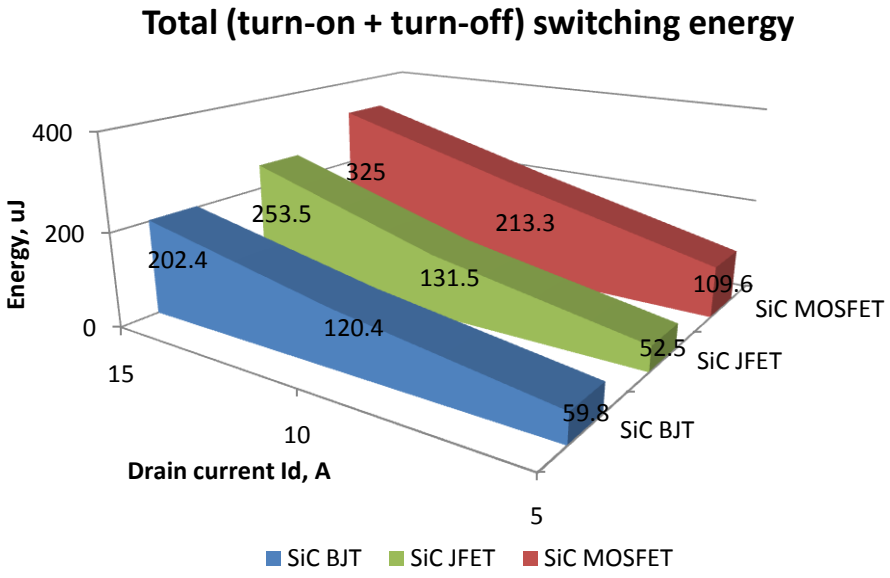



**Figure 8.6. Total switching energy comparison of different SiC transistors**

From Figure 8.6 it can be observed that the SiC BJT showed far more superior results than other two SiC transistors with only 202.4 uJ energy loss at 500 V and 15 A. The results for SiC VJFET and SiC MOSFET are 253.5 uJ and 325 uJ respectively. This might be due to the fact that the base driver circuit was properly tuned to achieve high performance. According to manufacturer (section 3.6.3) these SiC BJT transistors overcame the drawback of the Si power BJTs that resulted in a rather slow turn-off transition due to the bipolar operation of the device. This is in fact impressive taken into account that a simple, cost effective base driver circuit was used. SiC MOSFET showed a relatively poor result with the switching energy twice as high almost at all drain current levels compared to other SiC transistors. This introduces a requirement of using a different gate driver specifically designed for the needs of the SiC MOSFET. The results of SiC VJFET are satisfactory and correspond to what manufacturer state [46].

Analyzing the switching times once again the SiC BJT appears to be the fastest one with turn-on/off times of 8 ns/16.8 ns respectively. SiC VJFET is on the second place with 9.6 ns/21.6 ns and SiC MOSFET is the slowest with 10.4 ns/32.8 ns respectively.

SiC VJFET and SiC BJT showed similar voltage overshoots with 172 V for the first one and 166 V for the latter. SiC MOSFET showed the best result with only 84 V, but this is mainly

due to the rather slow switching. Current overshoots are again similar with SiC VJFET and SiC BJT, while this result is far worse for SiC MOSFET. These are 6.9 A, 7.5 A and 13.9 A respectively.

# 9. CONCLUSIONS AND FURTHER SCOPE

The main objective of the master thesis was to develop the gate driver circuit for new SiC VJFET transistor and characterize its gate requirements. This was successfully done along with the measurement results compared to the commercial SiC VJFET gate driver. A rather complex requirements of the gate makes the gate driver design procedure for SiC VJFET a challenging and interesting task. The performance of the proposed gate driver appears to be sufficient to drive the SiC VJFET in the converter though the optimization and especially shaping of the gate voltage/current waveforms must be done in order to extract the maximum performance of the SiC VJFET and obtain the lowest possible switching and on-state losses. It is concluded that the power supply for the gate driver must have significant power capability. This is due to high power demand of the gate driver, which is 1.56 W and 2.33 W for the proposed gate driver and for the commercial gate driver from SemiSouth respectively.

Simulations were also carried out for validating the design of the driver circuit. The simulated circuit shows good correspondence with what was expected and described in the scientific papers. The design of the entire system was very challenging. It added practical constraints to theoretical operation and software simulation. Design of circuit topologies, editing schematics and layouts, as well as component selection were new challenges. Overcoming them was not just very interesting and informative, but also beneficial for dealing with future circuit designs.

Other gate/base driver circuits used in the experiments were also characterized (section 7.1). The commercial DC-coupled gate driver circuit from SemiSouth (section 3.6.1) used to drive SiC VJFET presented outstanding output characteristics and high noise immunity. It was capable of providing both SiC VJFETs in the bridge configuration with adequate driving power and a degree of safety. The AC-coupled SiC BJT base drive circuit (section 3.6.3), which was also developed during the thesis, displayed a relatively good performance taken into account the simple design and cost effective nature of this driver.

The secondary objective was to characterize different SiC transistors, i.e. SiC VJFET, SiC MOSFET and SiC BJT. Two SiC Schottky diodes were also tested as the freewheeling diodes. Extensive experiments were performed on the developed half-bridge converter utilizing various combinations of SiC transistors, SiC diodes and gate/base driver circuits. The obtained results are analyzed in chapter 8 and the main conclusion is that these transistors switch

extremely fast and with relatively low energy losses so that they can be used in high-frequency applications. This will yield significant power loss reduction and power density increase. In other words, converters that utilize SiC transistors can be made extremely compact. SiC BJT showed the best result with the highest switching speeds (turn-on/off times of 8 ns/16.8 ns respectively) and lowest energy losses (202.4 uJ at 500 V and 15 A) compared to other two SiC transistors. The voltage/current overshoots during the switching are rather high though reaching 166 V and 7.5 A respectively. These overshoots stress the power semiconductor device and introduce EMI problems. SiC MOSFET showed rather poor switching behaviour with turn-on/off times of 10.4 ns/32.8 ns and 325 uJ energy loss at 500 V and 15 A. The voltage/current overshoots are 88 V and 13.9 A. The poor performance can be explained by the application of unsuitable gate driver circuitry which was not specifically tuned for voltage requirements of SiC MOSFET.

The performance of SiC VJFET lies in between the other two SiC transistors described above. The turn-on/off times are 9.6 ns/21.6 ns respectively with a 253.5 uJ energy loss at 500 V and 15 A. The voltage/current overshoots are 172 V and 6.9 A. The experiments with variable gate resistor and applied gate voltage revealed linear dependence on the switching speeds and losses. By varying the gate resistor value from 2.2 Ω to 6.8 Ω the switching losses increase from 344,3 uJ to 575 uJ (at Vds = 500 V, Id = 15 A and +/- 9 V applied at the gate). The turn-on/off time is increased from 9.6 ns to 18.4 ns and from 30 ns to 52.8 ns respectively. On the other hand, the slower switching speed yields lower voltage/current overshoot which is decreased from 142 V to 88 V and from 5 A to 3.7 A. Another way to control the switching behaviour of the transistor is to vary the applied gate voltage. By increasing the gate voltage from +/- 9 V to +/- 15 V the losses are decreased from 411 uJ down to 235.5 uJ. The turn-on/off speed in this case is decreased from 15.2 ns to 9.6 ns and from 34.4 ns to 21.6 ns respectively. Depending on the application the designer can find the trade-off between switching speed, voltage/current overshoot and switching losses. In general results for SiC VJFET showed that this transistor appears to be a robust solution for PV converters with high switching speed, relatively low switching losses and low EMI issues. Despite the benefits mentioned above, SiC transistors are still too expensive for commercial converters and the reduction in cost must be achieved in order to make their appearance in future designs possible. In addition, the high switching speed makes the converters fairly sensitive to parasitic and even small stray inductances and capacitances might introduce severe oscillations during switching. Hence, the power electronic designers need to take extra precautions when using SiC transistors.

## FURTHER SCOPE

In this section a scope for the further research activities will be addressed.

Since the operation of the proposed gate driver for SiC VJFET is not utilized to its full potential some corrections (section 7.1.3.4) in the existing design and optimization of laboratory prototype should be made.

Testing of the developed half-bridge converter in PWM mode might be a good way to evaluate the performance of both the two-stage gate driver and SiC VJFET. High temperature testing of the gate driver is also a challenge.

Including protection circuits for the gate driver and laboratory implementation should be done in order to obtain a more reliable operation of the gate driver and to protect the transistor from possible failures. For example, a short circuit protection based on the transistor saturation detection principle is an interesting and challenging task to fulfil.

Finally, the analysis of the possibility of building a PV inverter (e.g. H-bridge inverter) utilizing SiC transistors should be done.

# REFERENCES


[1] *T. Kerekes, "Analysis and Modeling of Transformerless Photovoltaic Inverter Systems," PhD Thesis, Faculty of Engineering, Science & Medicine at Aalborg University, Aalborg University, 2009.*

*[2] "Solar Generation: Solar Photovoltaic Electricity Empowering the World," The European Photovoltaic Industry Association and Greenpeace International2011.*

*[3] G. C. W. Kleinkauf, and M. Ibrahim, "PV Systems Technology - State of the art developments and trends in remote electrification," Dec. 01, 2005.*

*[4] "Trends in Photovoltaic Applications: Survey report of selected IEA countries between 1992 and 2009," IEA - International Energy Agency,2010.*

*[5] "Trends in Photovoltaic Applications: Survey report of selected IEA countries between 1992 and 2007," IEA - International Energy Agency,2008.*

*[6] World Wildlife Fund (WWF), et al., "THE ENERGY REPORT: 100% RENEWABLE ENERGY BY 2050," 978-2-940443-26-0, 2011.*

*[7] A. S. Joanna Lewis, Tian Tian. (2009). International Motivations for Solar Photovoltaic Market Support: Findings from the United States, Japan, Germany and Spain. Available: http://www.efchina.org/*

*[8] J. Casady, "SemiSouth's transistors boost photovoltaic system efficiencies," SemiSouth2009.*

*[9] S. V. Araujo and P. Zacharias, "Analysis on the potential of Silicon Carbide MOSFETs and other innovative semiconductor technologies in the photovoltaic branch," in Power Electronics and Applications, 2009. EPE '09. 13th European Conference on, 2009, pp. 1-10.*

*[10] F. Schimpf, "Grid connected Converters for Photovoltaic, State of the Art, Ideas for Improvement of Transformerless Inverters," presented at the NORPIE/2008, Nordic Workshop on Power and Industrial Electronics, 2008.*

*[11] S. B. Kjaer, et al., "A review of single-phase grid-connected inverters for photovoltaic modules," Industry Applications, IEEE Transactions on, vol. 41, pp. 1292-1306, 2005.*

*[12] A. R. Alonso, et al., "An overall study of a Dual Active Bridge for bidirectional DC/DC conversion," in Energy Conversion Congress and Exposition (ECCE), 2010 IEEE, 2010, pp. 1129-1135.*

*[13] "German Patent HERIC-Topology: DE 102 21 592 A1, issued 04.12.2003."*

*[14] "German Patent H5-Topology: DE 10 2004 030 912 B3, issued 19.01.2006."*

*[15] J. B. CASADY and R. W. JOHNSON, "Status of Silicon Carbide (SiC) as a WideBandgap Semiconductor for HighTemperature Applications: A Review " NASA Center for Commercial Development, Electrical Engineering Department, 200 Broun Hall, Auburn University, AL 36849-5201, U.S.A.1999.*

*[16] A. Grigorjevs, "High performance power conversion," Specialization project, Department of Electric Power Engineering, Norwegian University of Science and Technology, Trondheim, 2010.*

*[17] I. Abuishmais, et al., "On understanding and driving SiC power JFETs," in Applied Power Electronics Conference and Exposition (APEC), 2011 Twenty-Sixth Annual IEEE, 2011, pp. 1071-1075.*

*[18] A. Elasser, et al., "A comparative evaluation of new silicon carbide diodes and state-of-the-art silicon diodes for power electronic applications," Industry Applications, IEEE Transactions on, vol. 39, pp. 915-921, 2003.*

*[19] "Silicon Carbide Enhancement-Mode Junction Field Effect Transistor and Recommendations for Use," SemiSouth Laboratories, Inc., Application note,2009.*

*[20] R. Kelley, et al., "Improved two-stage DC-coupled gate driver for enhancement-mode SiC JFET," in Applied Power Electronics Conference and Exposition (APEC), 2010 Twenty-Fifth Annual IEEE, 2010, pp. 1838-1841.*

*[21] B. Callanan, "Application Considerations for Silicon Carbide MOSFETs," Cree Inc., Application note,2011.*

*[22] L. Balogh, "Design and Application Guide for High Speed MOSFET Gate Drive Circuits," Texas Instruments, Application Note,.*

*[23] "CMF20120D-Silicon Carbide Power MOSFET 1200V 80 mΩ," Cree Inc., Datasheet,2011.*

*[24] O. Stalter, et al., "Advanced solar power electronics," in Power Semiconductor Devices & IC's (ISPSD), 2010 22nd International Symposium on, 2010, pp. 3-10.*

*[25] M. S. Mazzola and R. Kelley, "Application of a Normally OFF Silicon Carbide Power JFET in a Photovoltaic Inverter," in Applied Power Electronics Conference and Exposition, 2009. APEC 2009. Twenty-Fourth Annual IEEE, 2009, pp. 649-652.*

[26] *C. Wilhelm, et al., "Development of a highly compact and efficient solar inverter with Silicon Carbide transistors," in Integrated Power Electronics Systems (CIPS), 2010 6th International Conference on, 2010, pp. 1-6.*

[27] *N. Mohan, et al., Power electronics: Converters, Applications and Design: John Wiley & Sons, 2003.*

[28] *A. D. Pathak and R. E. Locher, "HOW TO DRIVE MOSFETs AND IGBTs INTO THE 21ST CENTURY," IXYS corporation,2004.*

[29] *"Two-Stage Opto Coupled Gate Driver Demo Board," SemiSouth Laboratories, Inc., Application note,2010.*

[30] *"JFET Gate Driver and Layout Considerations," SemiSouth Laboratories, Inc., Application note,2009.*

[31] *B. Callanan, "SiC MOSFET Double Pulse Fixture," Cree Inc., Application note,2011.*

[32] *B. Callanan, "SiC MOSFET Isolated Gate Driver," Cree Inc., Application note,2011.*

[33] *"BitSiC Characteristics and Switching," TranSiC, Application Note TSC-TR005,2010.*

[34] *A. Lindgren and M. Domeij, "Degradation free fast switching 1200 V 50 a silicon carbide BJT's," in Applied Power Electronics Conference and Exposition (APEC), 2011 Twenty-Sixth Annual IEEE, 2011, pp. 1064-1070.*

[35] *B. Wrzecionko, et al., "Novel AC coupled gate driver for ultra fast switching of normally-off SiC JFETs," in IECON 2010 - 36th Annual Conference on IEEE Industrial Electronics Society, 2010, pp. 605-612.*

[36] *Robin Kelley, et al., "Optimized Gate Driver for Enhancement-mode SiC JFET," SemiSouth Laboratories, Inc.,2009.*

[37] *R. L. Kelley, et al., "Power factor correction using an enhancement-mode SiC JFET," in Power Electronics Specialists Conference, 2008. PESC 2008. IEEE, 2008, pp. 4766-4769.*

[38] *"SJEP120R063 SiC JFET," SemiSouth Laboratories, Inc., Datasheet, available at www.semisouth.com, 2011.*

[39] *Wikipedia article on spice simulations. Available: http://en.wikipedia.org/wiki/SPICE*

[40] *Homepage of LTspice. Available: http://www.linear.com/designtools/software/*

[41] *LTspice Yahoo group. . Available: http://tech.groups.yahoo.com/group/LTspiceFiles/*

[42] *"LT1107 - Micropower DC/DC Converter," Linear Technology, Datasheet.*

[43] *T. L. Skvarenina, The Power Electronics Handbook (Industrial Electronics): CRC Press; 1 edition, 2001.*

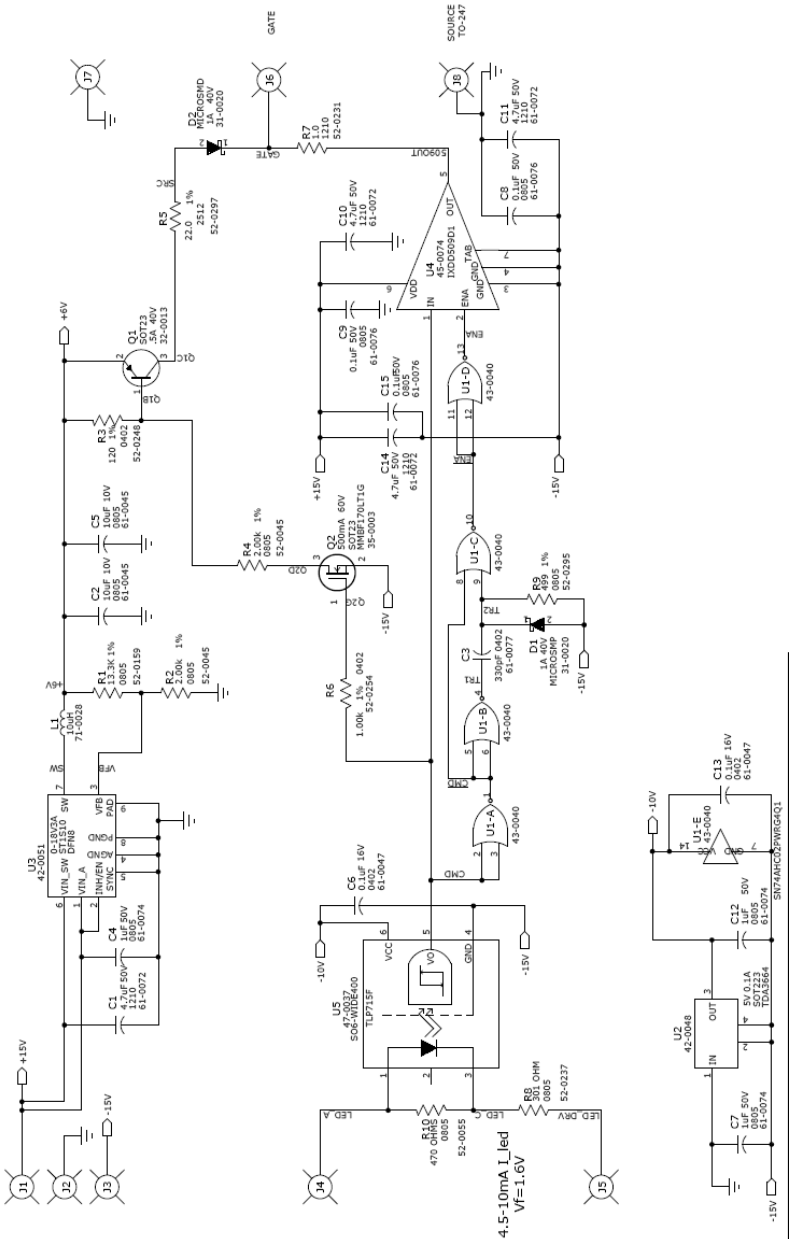
*[44] D. D. Katsis. Using a Rogowski Coil for Device Evaluation with a Double-Pulse Circuit.*

*[45] D. Xiao, "On Modern IGBT Modules: Characterization, Reliability and Failure Mechanisms," Master thesis, Department of Electric Power Engineering, Norwegian University of Science and Technology, Trondheim, 2010.*

*[46] "The SJEP120R063 – Reduced Switching Losses in the New Low-Inductance Test Fixture," SemiSouth Laboratories, Inc., Application note,2009.*

# Appendix

# *Appendix A*




**Two-Stage Opto-coupled Gate Driver Schematic**

SemiSouth

Preliminary

***Demo Board***

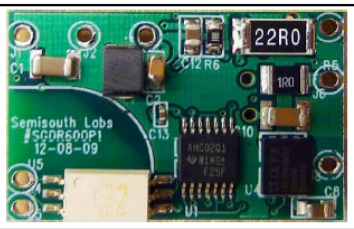
# SGDR600P1

## Two-Stage Opto Coupled Gate Driver Demo Board

The SGDR600P1 is an optoisolated, two-stage gate driver optimized for high speed, hard switching of SemiSouth's SJEP120R050 and SJEP120R063 normally-off SiC VJFETs. The SGDR600P1 gate driver provides a peak output current of +6/- 3A for fast turn-on transients yeilding record low switching energy losses.

| Product Summary | | |
|---|---|---|
| $V_{DD}/V_{SS}$ | +15V/-15V | V |
| $I_{PK}$ | +6/-3 | A |
| $F_{SW(MAX)}$ | 250 | kHz |
| Duty Cycle | 0-100 | % |

SGDR600P1

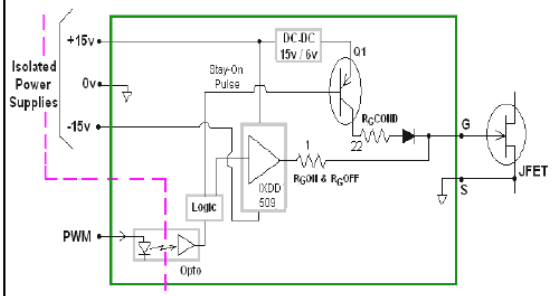



0.75" x 1.10"

### Features:

- Suitable for driving SJEP120R063 or SJEP120R050
- Two-stage driver - switching & conduction
- Peak gate current of +6/-3A
- Switching frequency up to 250 kHz
- Duty cycle: 0 to 100%
- Low BOM cost

Schematic Overview



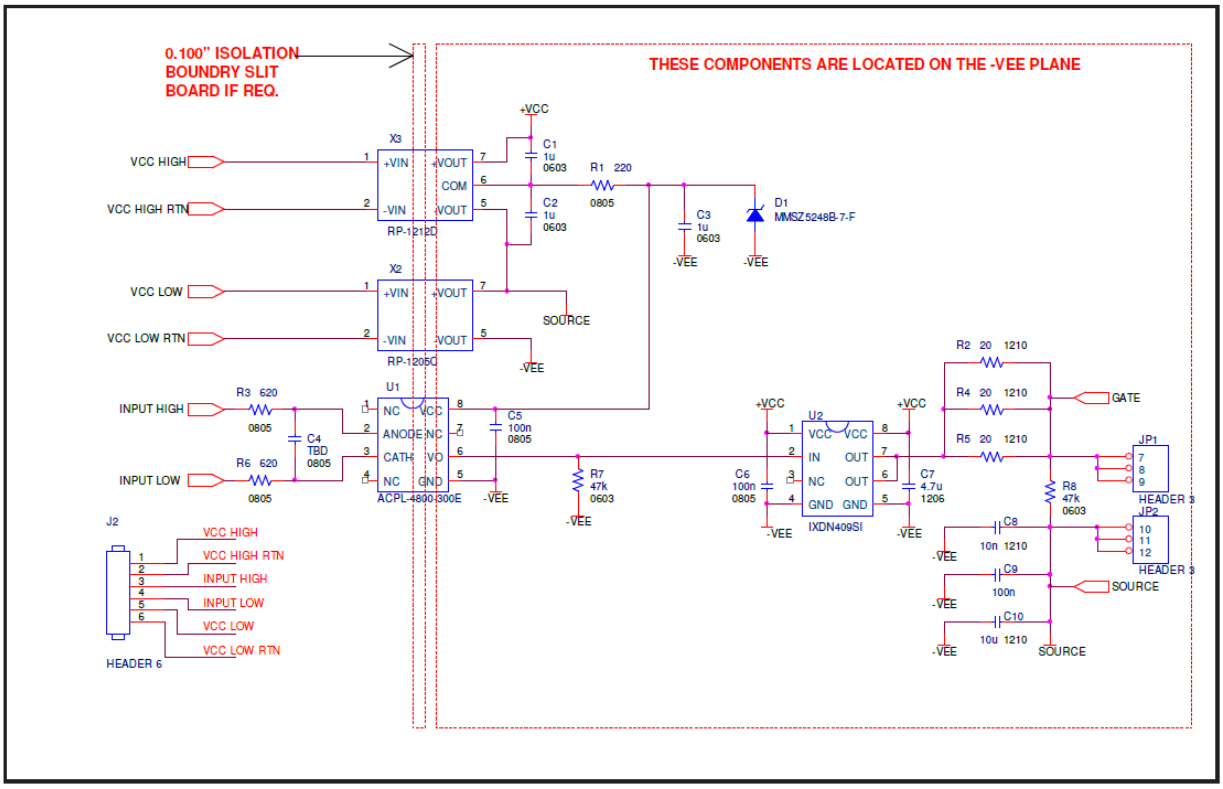

### Applications:

- Hard Switched Bridge Topologies
- Inverters/Converters
- IT/Telecom Power Supplies
- Product Evaluation
- Research

### MAXIMUM RATINGS

| Parameter | Symbol | Conditions | Value | Unit |
|---|---|---|---|---|
| Positive supply voltage | $V_{CC}$ | to GND | + 15 | V |
| Negative supply voltage | $V_{EE}$ | to GND | -15 | V |
| Input current logic HIGH | $I_{F(ON)}$ | | 10 | mA |
| Peak Output Current | $I_O$ | Not connected to the JFET, output shorted to GND or pure capacitive load | + 9 | A |
| | | | - 9 | |
| Operating temperature | $T_{OP}$ | | + 85 | ℃ |
| Storage temperature | $T_{ST}$ | | + 100 | ℃ |

# *Appendix B*

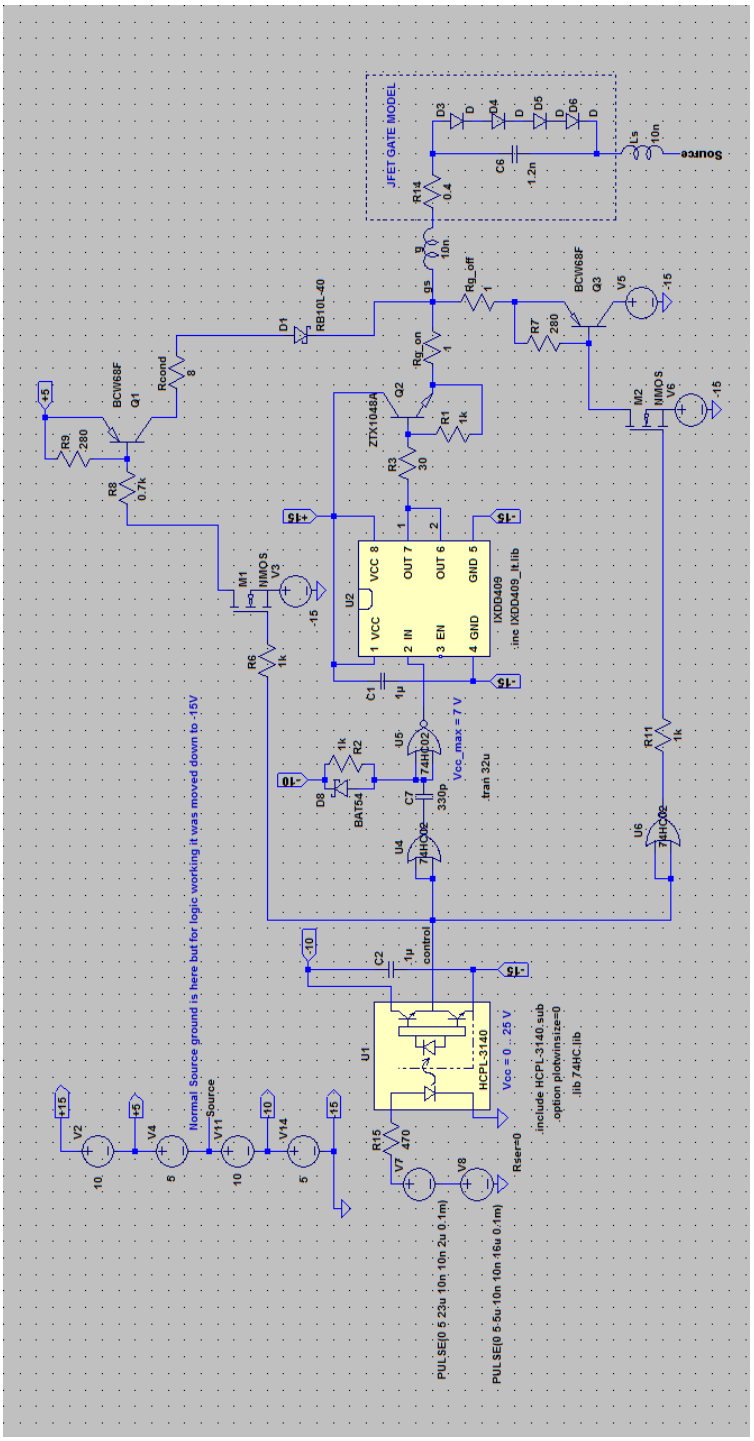



Schematic of the isolated SiC MOSFET gate driver

| Item | Qty | Part Reference | Value | Description | Manufacturer | Manufacturer P/N |
|---|---|---|---|---|---|---|
| 1 | 3 | C1 C2 C3 | 1u | CAP CER 1.0UF 25V X5R 20% 0603 | AVX Corporation | 06033D105MAT2A |
| 2 | 1 | C4 | TBD | CAP CER TBD 0805 | TBD | TBD |
| 3 | 2 | C5 C6 | BNC | CAP .10UF 50V CERAMIC X7R 0805 | Kemet | C0805C104K5RACTU |
| 4 | 1 | C7 | 4.7µ | CAP CER 4.7UF 50V X5R 1206 | Kemet | C1206C475K5PACTU |
| 5 | 1 | C8 | 10n | CAP CERAMIC 10000PF 50V NP0 1210 | Kemet | C1210C103J5GACTU |
| 6 | 1 | C9 | 100n | CAP .10UF 50V CERAMIC X7R 1206 | Kemet | C1206C104K5RACTU |
| 7 | 1 | C10 | 10µ | CAP CERAMIC 10UF 16V X5R 1210 | Kemet | C1210C106K4PACTU |
| 8 | 1 | D1 | MMSZ5248B-7-F | DIODE ZENER 18V 500MW SOD123 | Diodes Inc | MMSZ5248B-7-F |
| 9 | 1 | J2 | Header 6 | 6 Pin Header cut from PBC36SAAN | Sullins Connector Solutions | PBC36SAAN |
| 10 | 1 | JP1 | Header 3 | 3 Pin Header cut from PBC36SAAN | Sullins Connector Solutions | PBC36SAAN |
| 11 | 1 | JP2 | Header 3 | 3 Pin Header cut from PBC36SAAN | Sullins Connector Solutions | PBC36SAAN |
| 12 | 1 | R1 | 220 | RES 220 OHM 1/8W 5% 0805 SMD | Vishay/Dale | CRCW0805220RJNEA |
| 13 | 3 | R2 R4 R5 | 20 | RES 20 OHM 1/2W 5% 1210 SMD | Vishay/Dale | CRCW121020R0JNEA |
| 14 | 2 | R3 R6 | 620 | RES 620 OHM 1/8W 5% 0805 SMD | Vishay/Dale | CRCW0805620RJNEA |
| 15 | 2 | R7 R8 | 47k | RES 47K OHM 1/10W 5% 0603 SMD | Vishay/Dale | CRCW060347K0JNEA |
| 16 | 1 | U1 | ACPL-4800-300E | OPTOCOUPLER IPM 5MBD 8-SMD GW | Avago Technologies US Inc. | ACPL-4800-300E |
| 17 | 1 | U2 | IXDN409SI | Gate Driver Integrated Circuit | IXYS - Clare | IXDN409SI or IXDN609SI |
| 18 | 1 | X2 | RP-1205C | Unreg1 W DC-DC Conv 12V in 5V out | Recom | RP-1205D |
| 19 | 1 | X3 | RP-1212D | Unreg1 W DC-DC Conv 12V in +/- 12V out | Recom | RP-1212D |

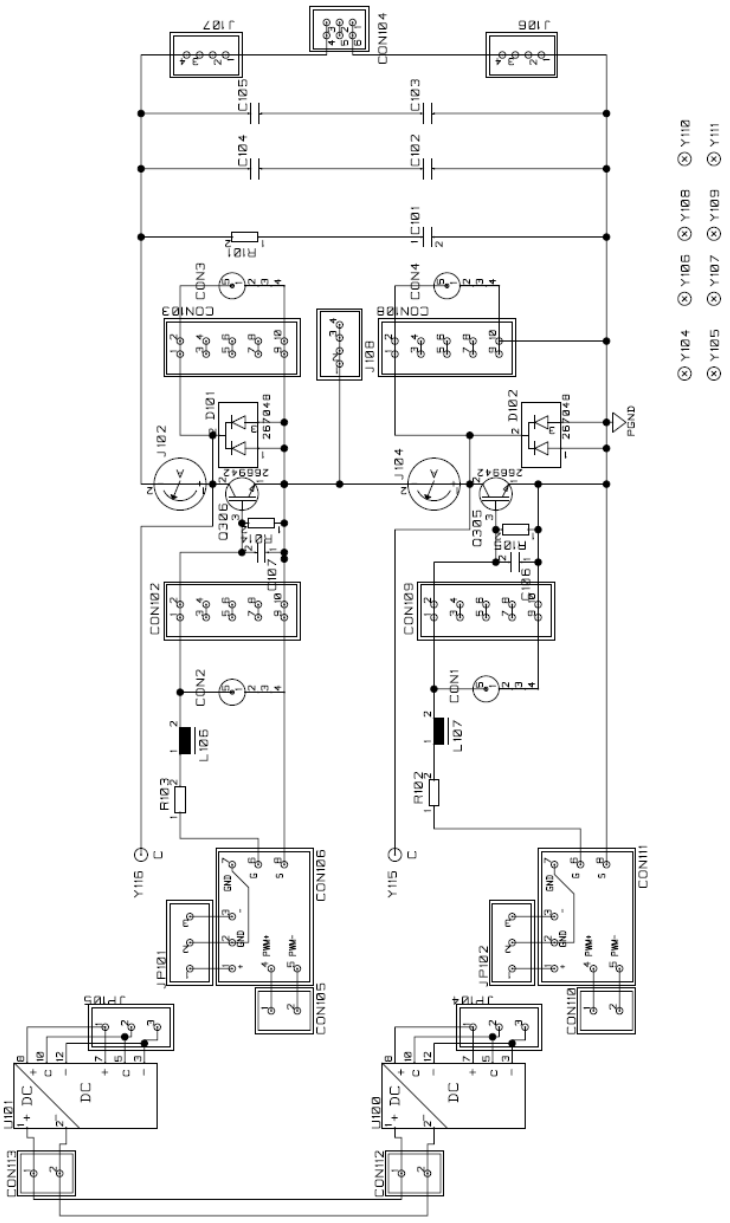
Bill of materials for SiC MOSFET gate driver

# *Appendix C*

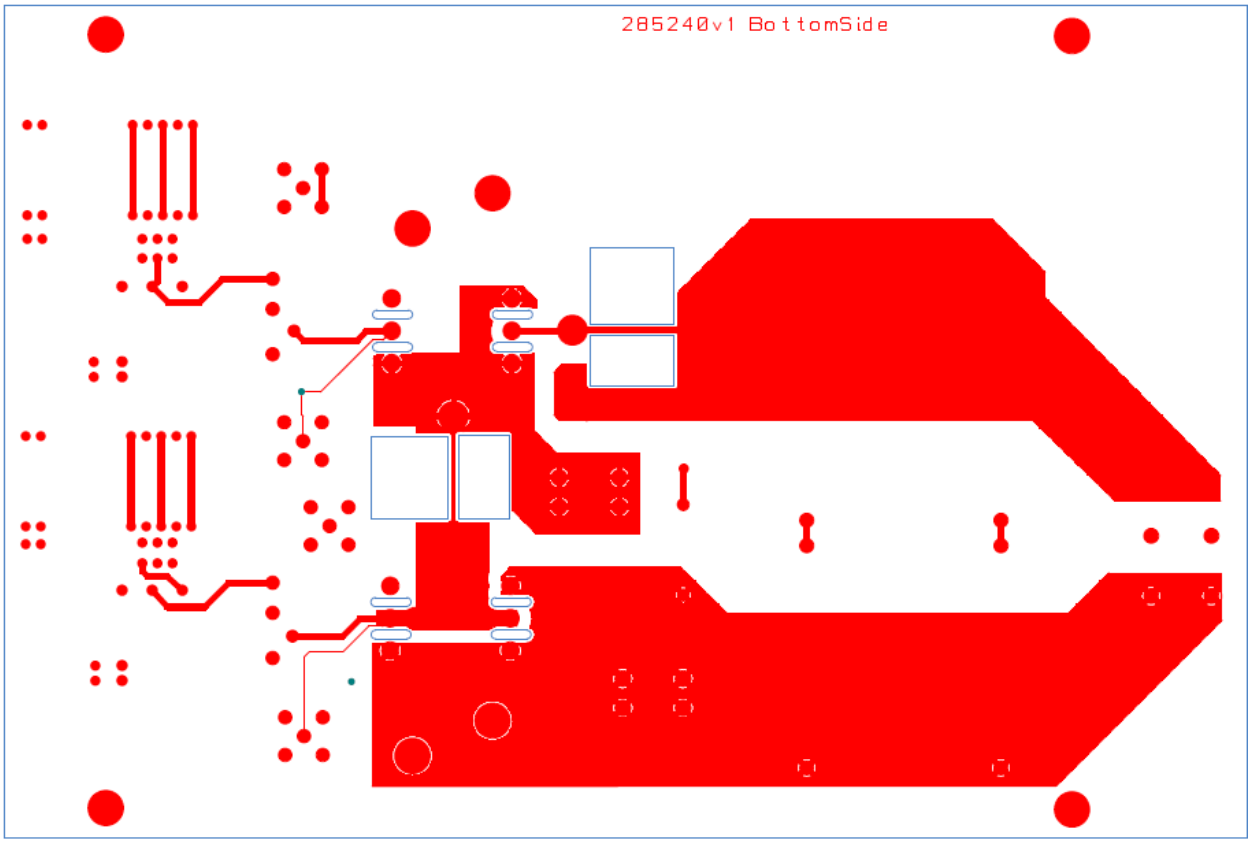



**A complete simulated circuit of the proposed gate driver circuit for SiC VJFET**

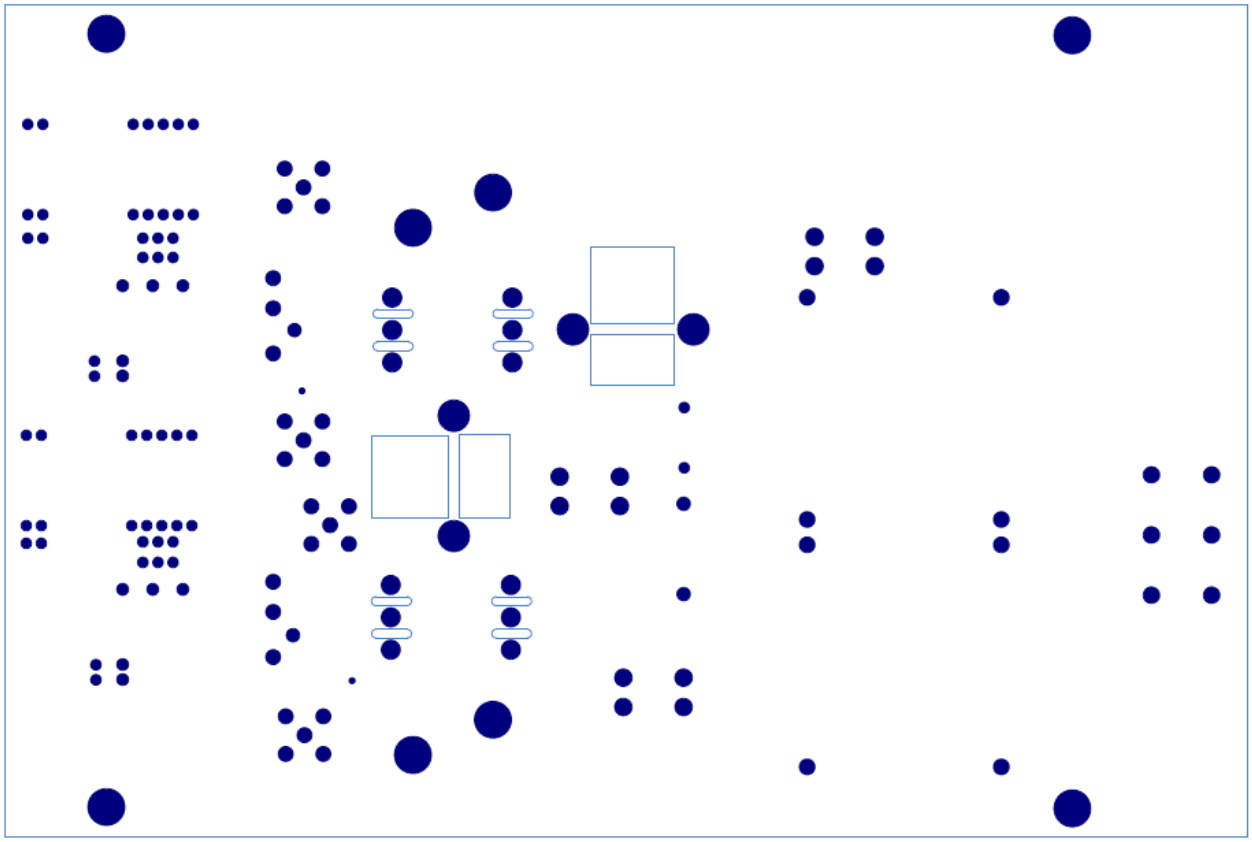
## *Appendix D*



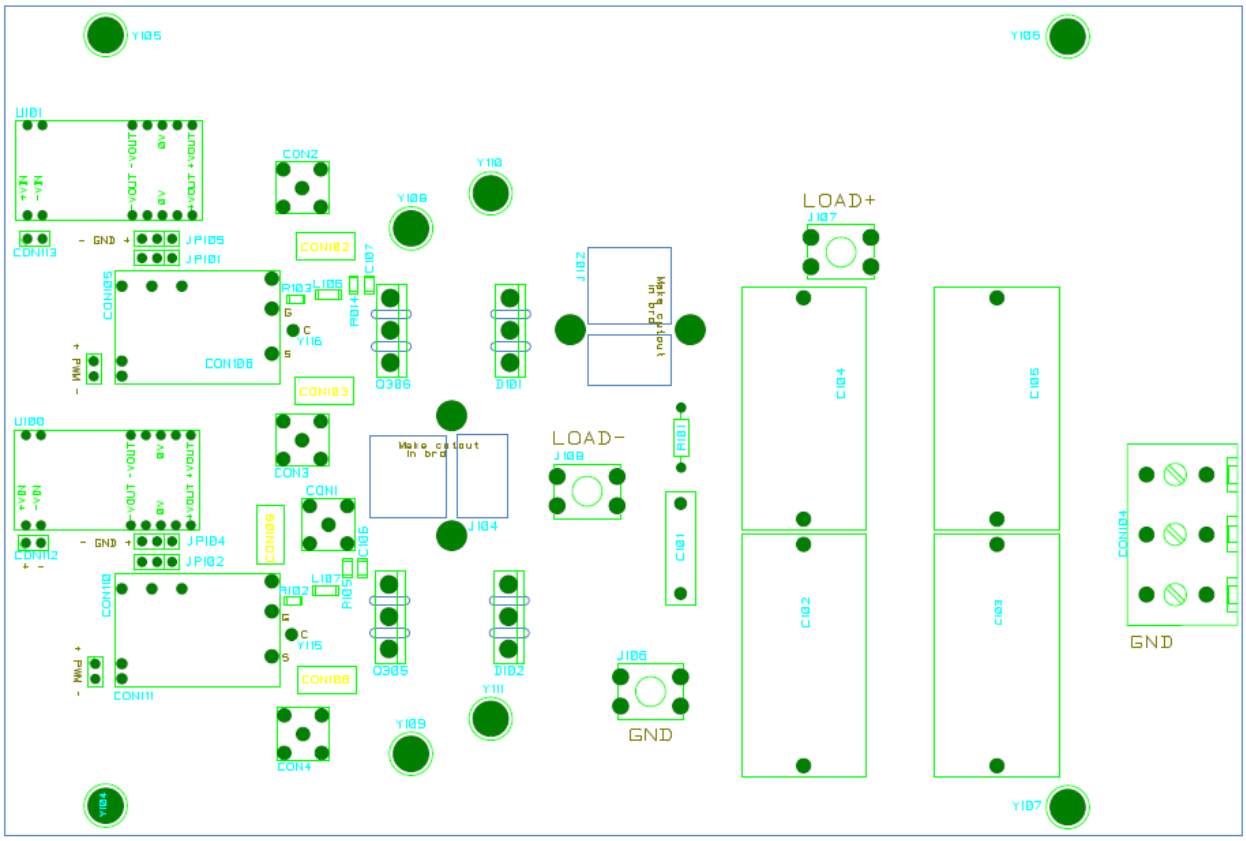
**Schematic of the developed half-bridge power board**



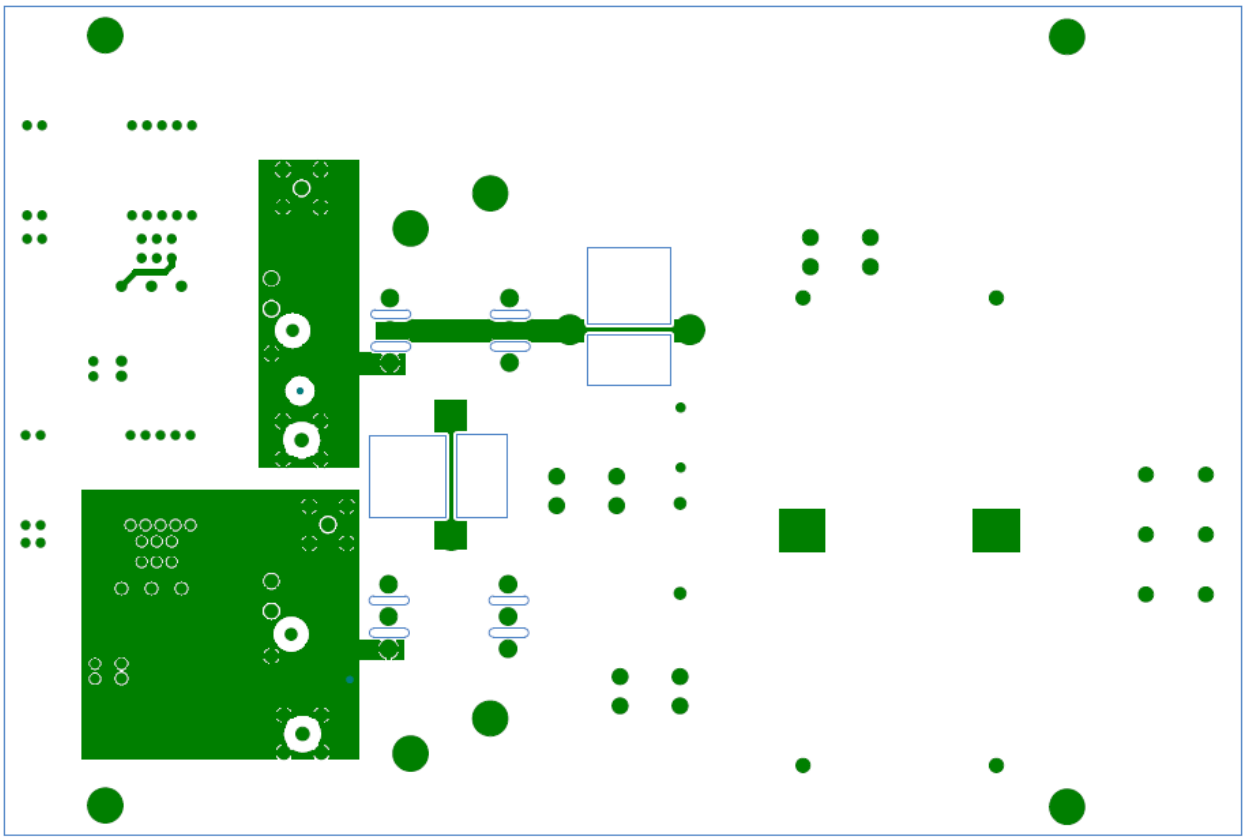

Bottom layer of the half-bridge converter board



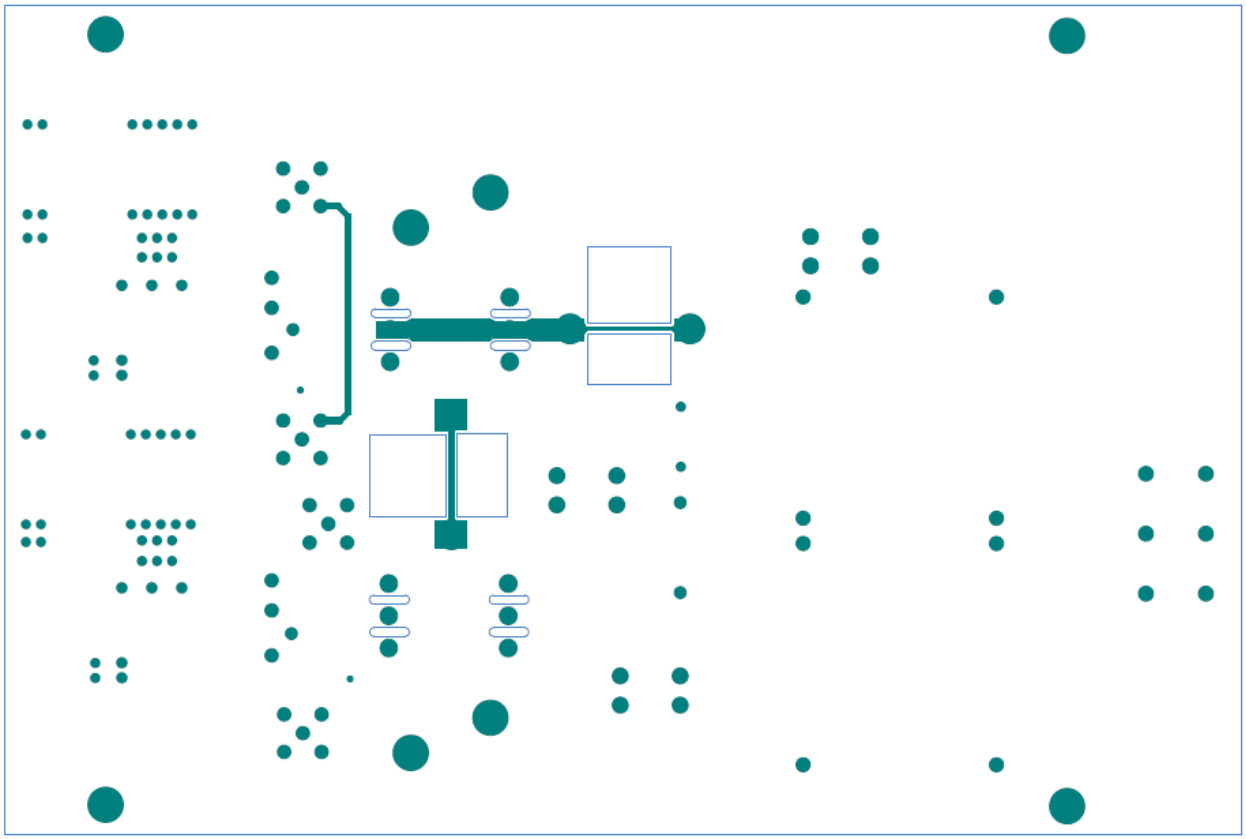
Bottom layer solder mask of the half-bridge converter board



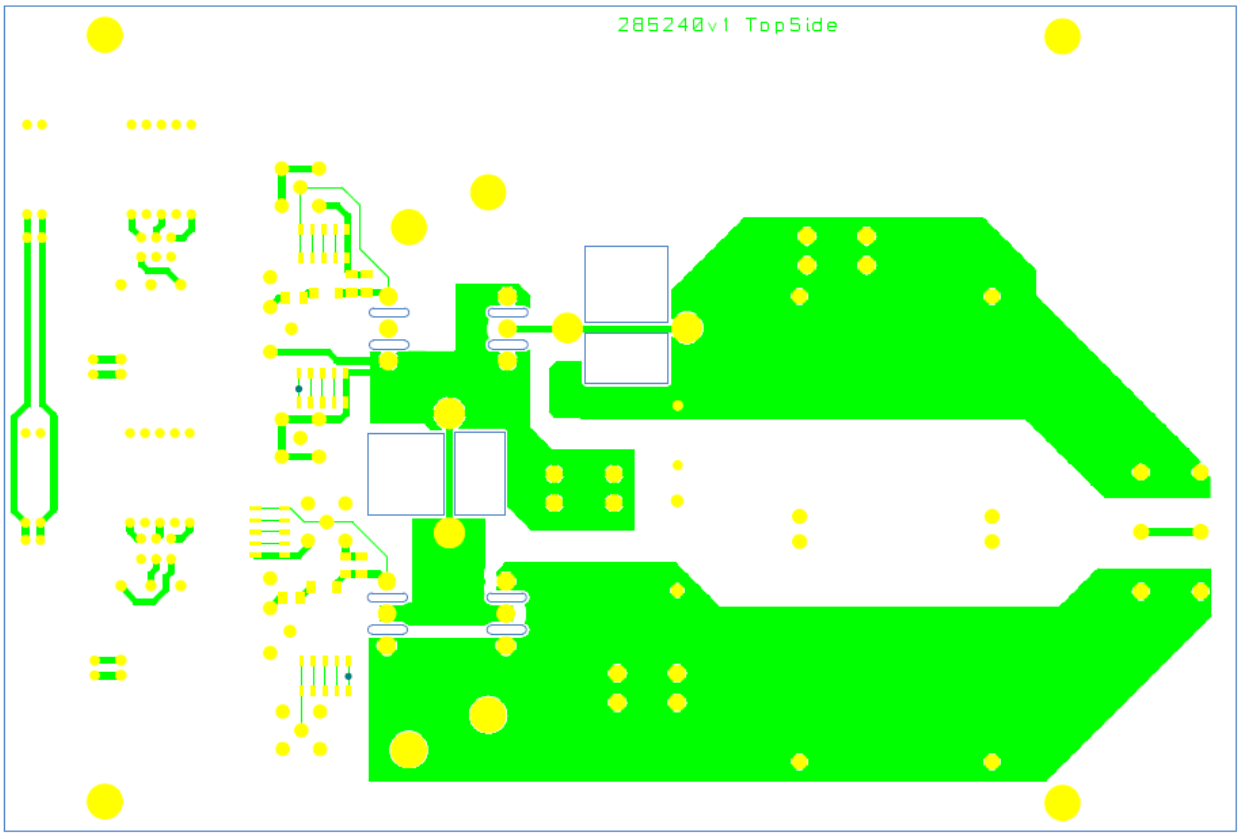

Component reference, top side



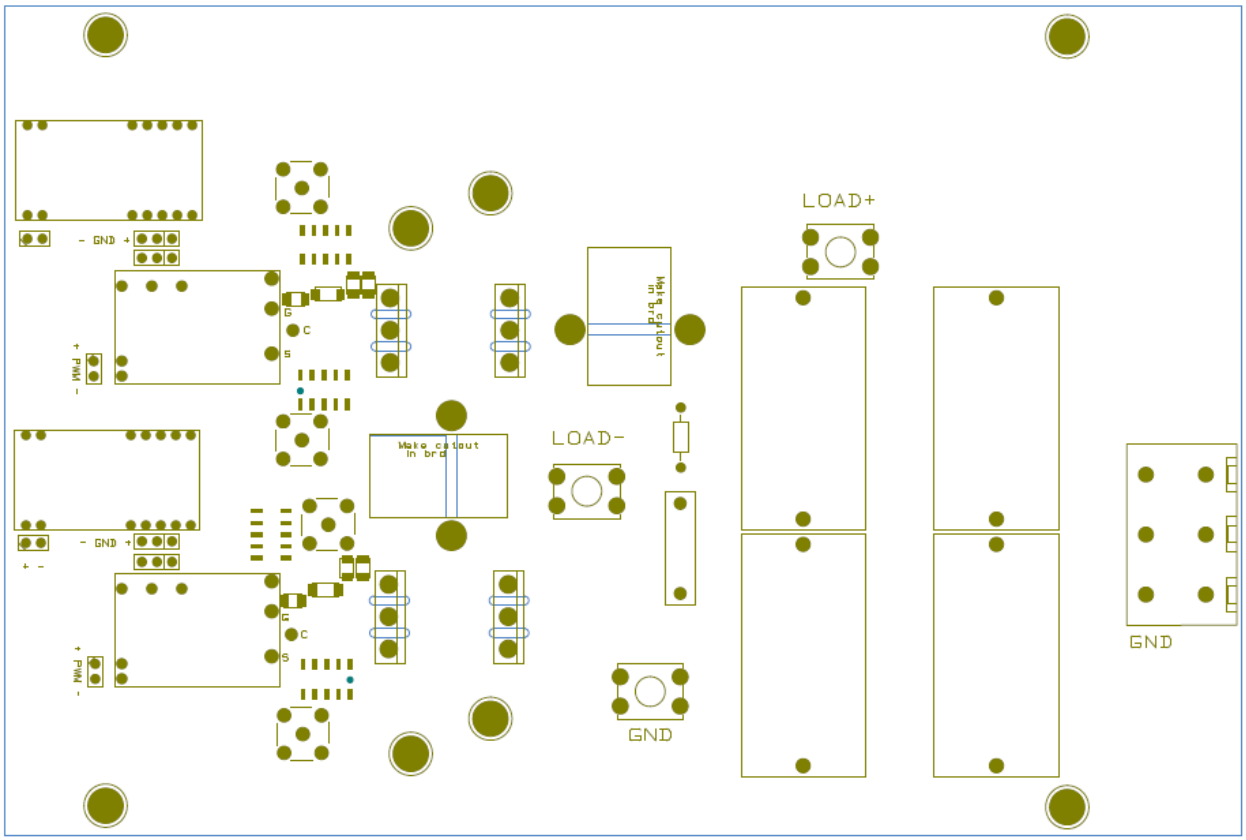
Inner layer 1



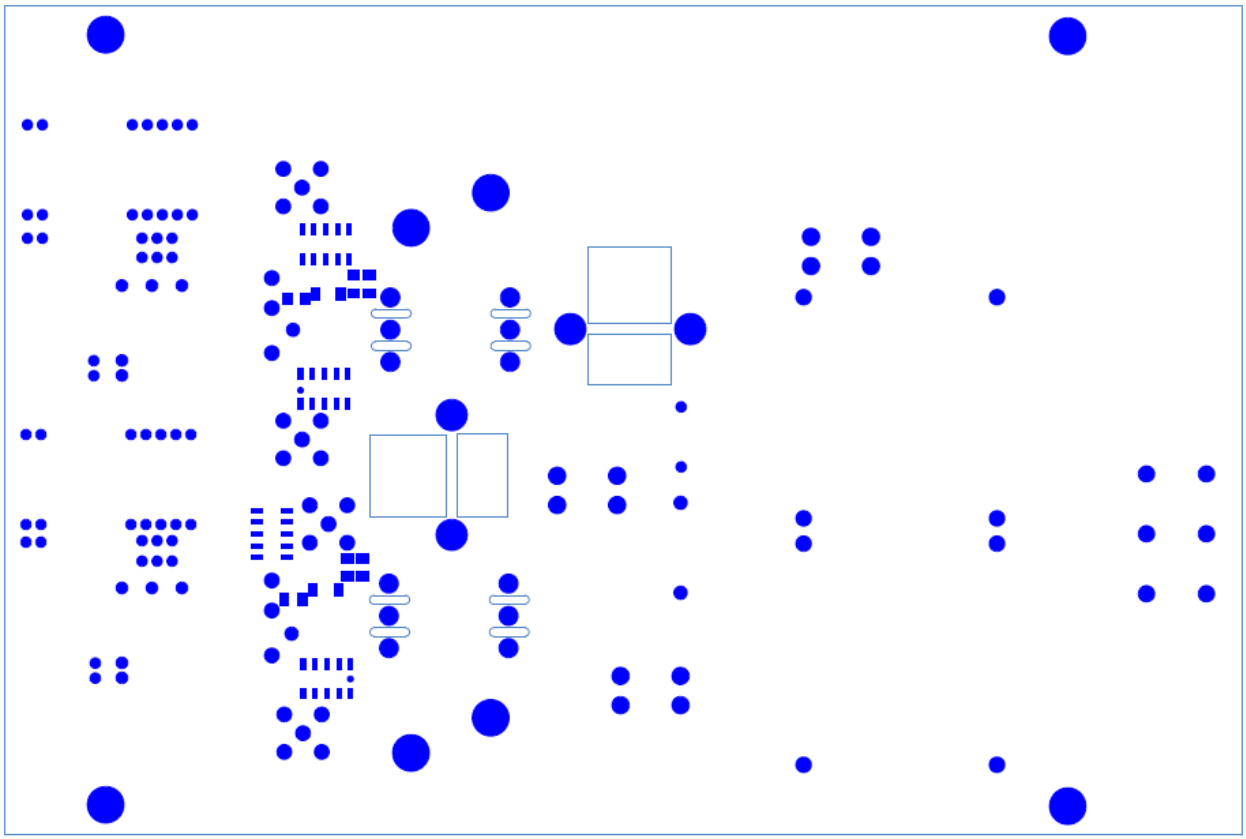
Inner layer 2




Top layer of the half-bridge converter board

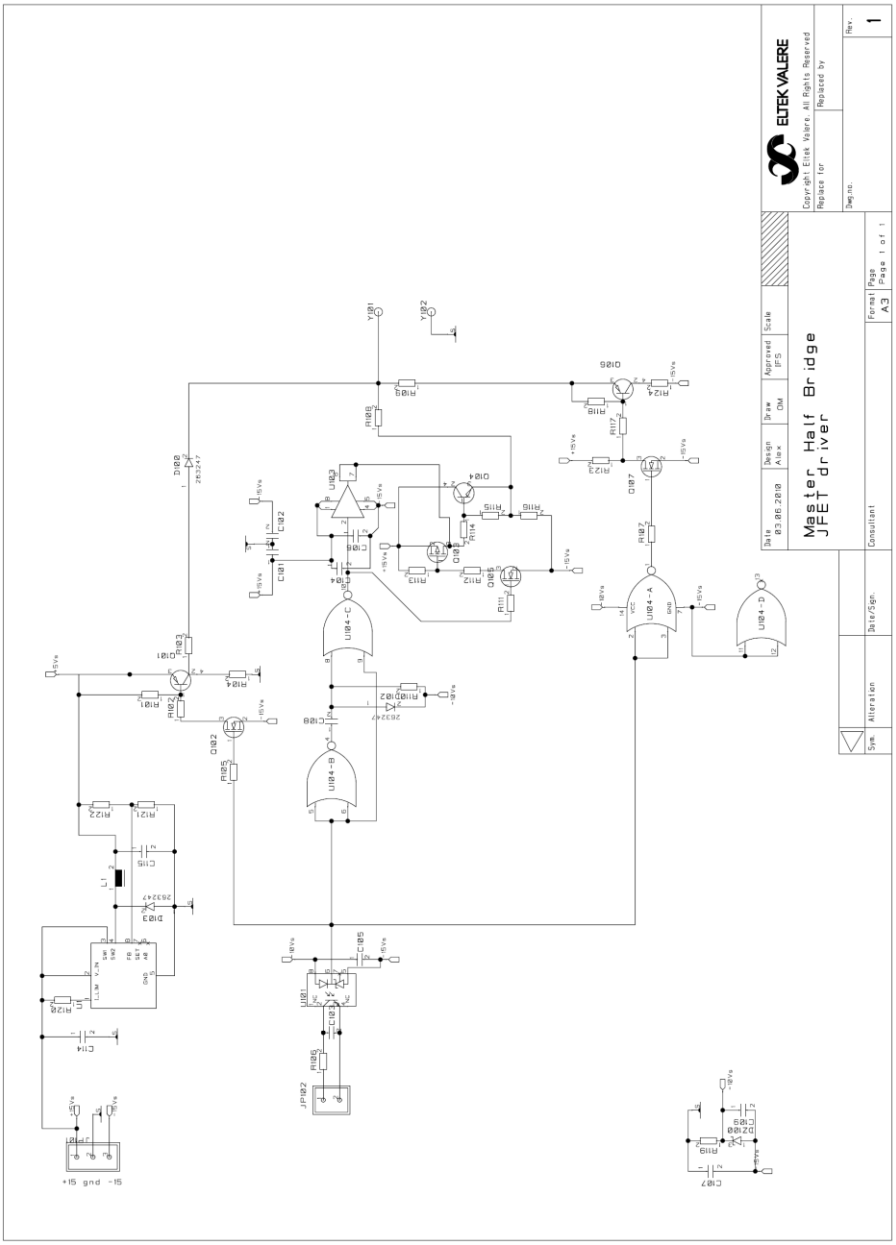



Top layer silk screen

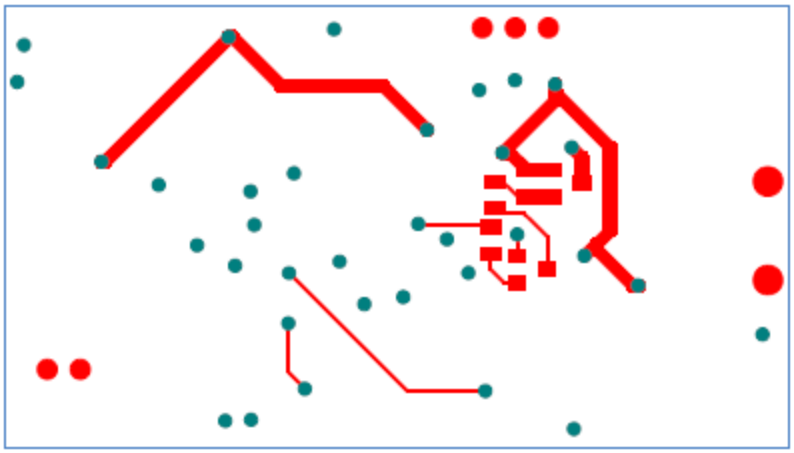


Top layer solder mask

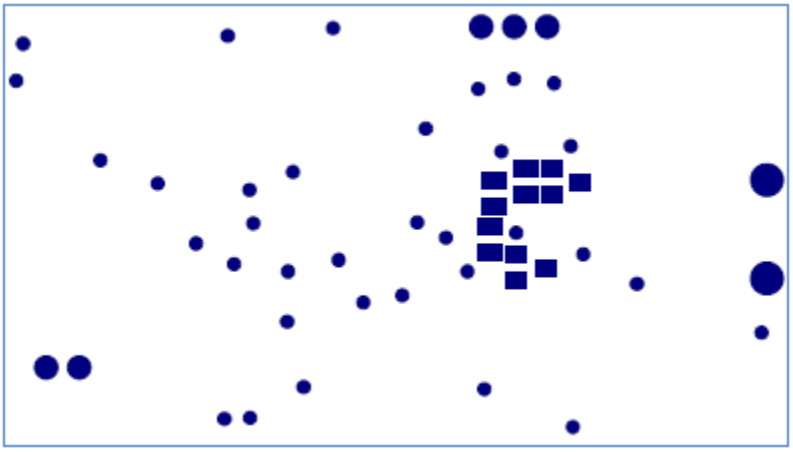
# *Appendix E*



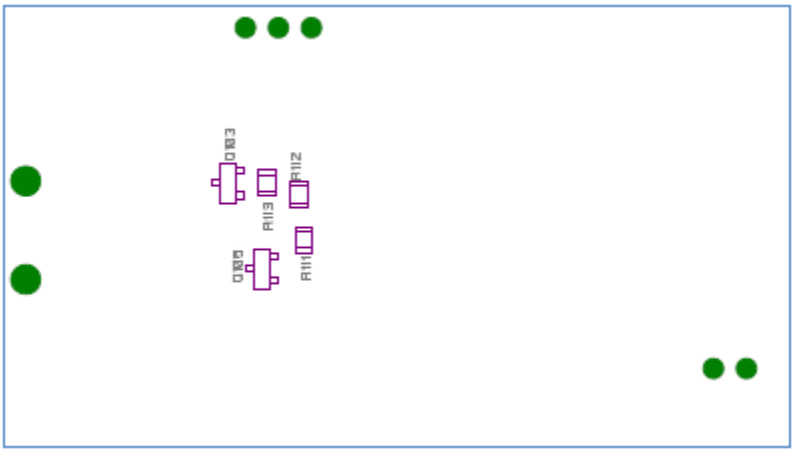

**Schematic of the proposed gate driver circuit**



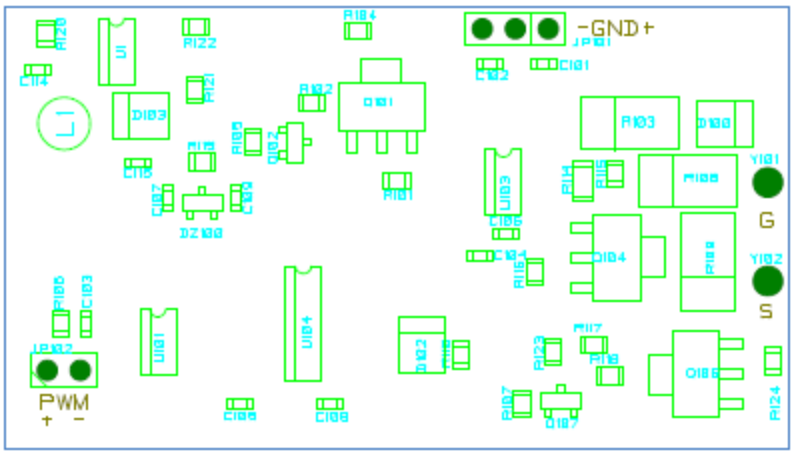
**Bottom layer of designed gate driver circuit**



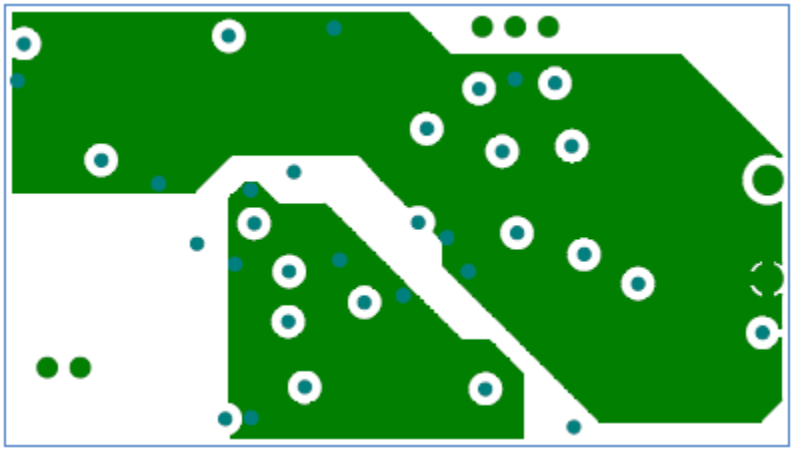
**Bottom solder mask of designed gate driver circuit**



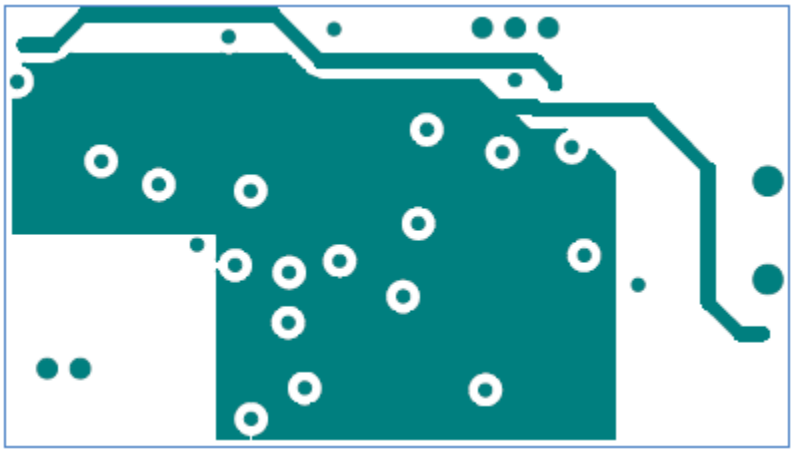

**Component reference, bottom side**



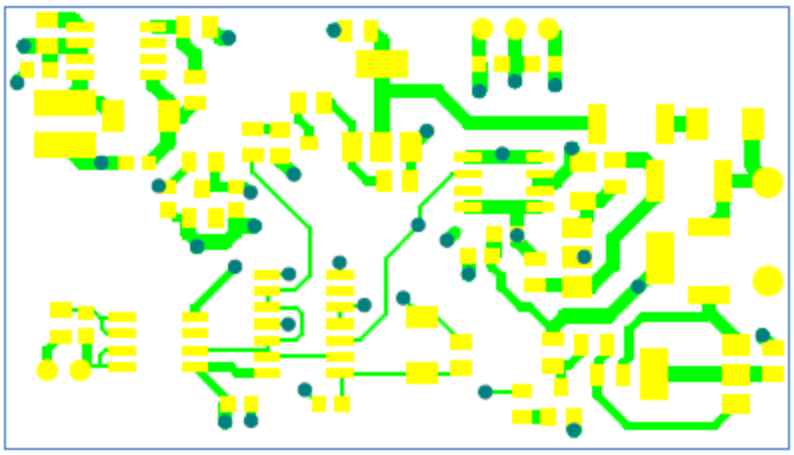

**Component reference, top side**



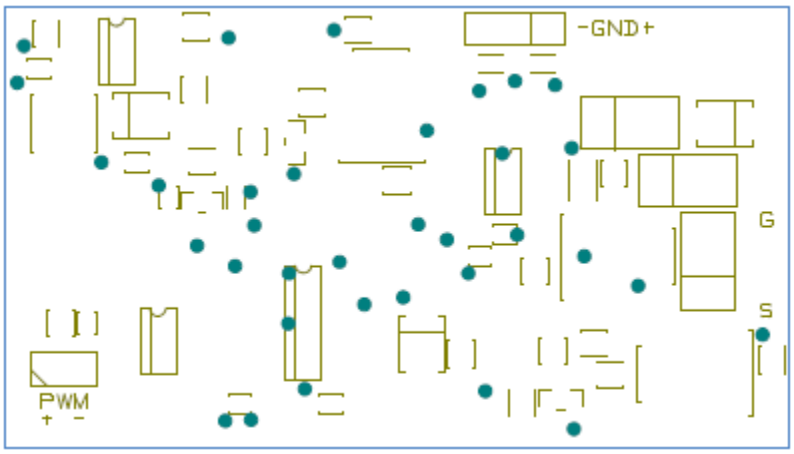
**Inner layer 1**



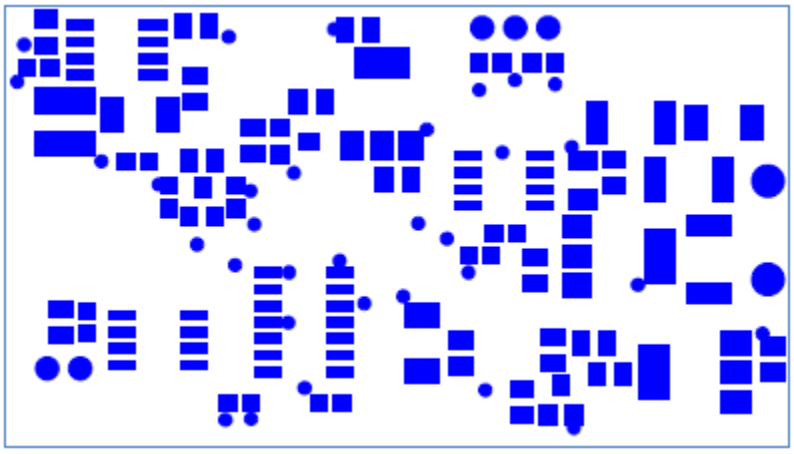
**Inner layer 2**



Top layer of designed gate driver circuit

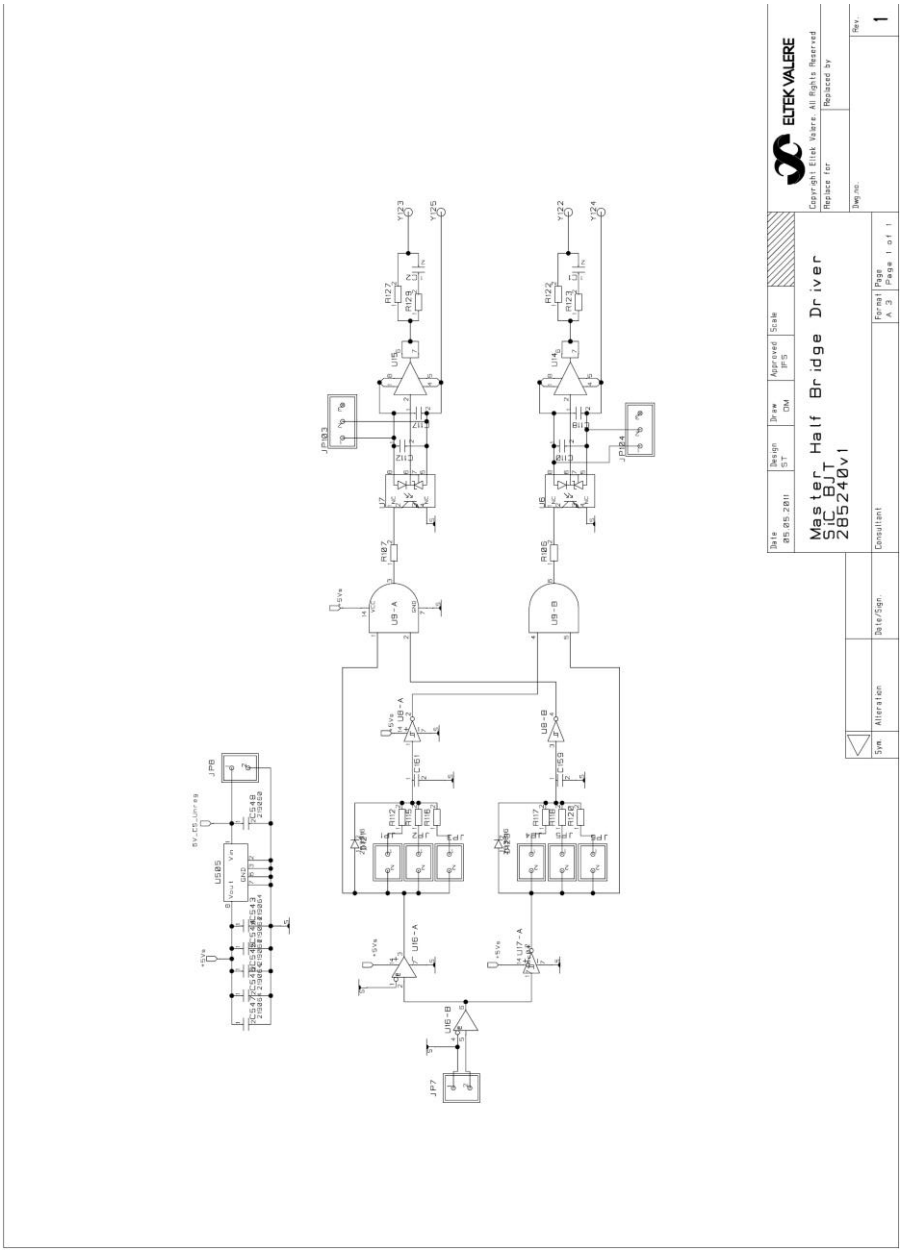



Top layer silk screen



Top solder mask of designed gate driver circuit

# *Appendix F*




**Schematic of the half-bridge SiC BJT base driver**

## *Appendix G*

SemiSouth

PRELIMINARY

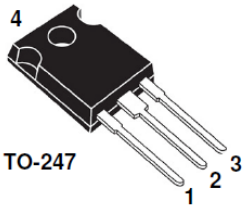
***Silicon Carbide***

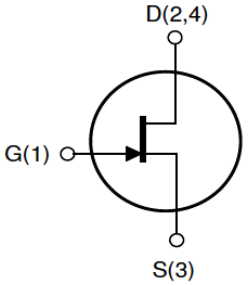
# SJEP120R063

## Normally-OFF Trench Silicon Carbide Power JFET

| Product Summary | | |
|---|---|---|
| $BV_{DS}$ | 1200 | V |
| $R_{DS(ON)max}$ | 0.063 | Ω |
| $E_{TS,typ}$ | 440 | µJ |

**Features:**
- Compatible with Standard Gate Driver ICs
- Positive Temperature Coefficient for Ease of Paralleling
- Temperature Independent Switching Behavior
- 150 °C Maximum Operating Temperature
- $R_{DS(on)max}$ of 0.063 Ω
- Voltage Controlled
- Low Gate Charge
- Low Intrinsic Capacitance




Internal Schematic

**Applications:**
- Solar Inverter
- SMPS
- Power Factor Correction
- Induction Heating
- UPS
- Motor Drive

### MAXIMUM RATINGS

| Parameter | Symbol | Conditions | Value | Unit |
|---|---|---|---|---|
| Continuous Drain Current | $I_{D,\ Tj=125}$ | $T_j$ = 125 °C | 30 | A |
| | $I_{D,\ Tj=150}$ | $T_j$ = 150 °C | 20 | |
| Pulsed Drain Current (1) | $I_{DM}$ | $T_j$ = 25 °C | 60 | A |
| Short Circuit Withstand Time | $t_{SC}$ | $V_{DD}$ < 800 V, $T_C$ < 125 °C | 50 | µs |
| Power Dissipation | $P_D$ | $T_C$ = 25 °C | 250 | W |
| Gate-Source Voltage | $V_{GS}$ | AC(2) | -15 to +15 | V |
| Operating and Storage Temperature | $T_j$, $T_{stg}$ | | -55 to +150 | °C |
| Lead Temperature for Soldering | $T_{sold}$ | 1/8" from case < 10 s | 260 | °C |

(1) Limited by pulse width
(2) $Rg_{EXT}$ = 0.5 ohm, tp < 200ns, see Figure 5 for static conditions

### THERMAL CHARACTERISTICS

| Parameter | Symbol | Value | | Unit |
|---|---|---|---|---|
| | | Typ | Max | |
| Thermal Resistance, junction-to-case | $R_{th\ JC}$ | - | 0.6 | °C / W |
| Thermal Resistance, junction-to-ambient | $R_{th\ JA}$ | - | 50 | |

# C3D20060D–Silicon Carbide Schottky Diode

*Z-REC™* RECTIFIER

| | |
|---|---|
| $V_{RRM}$ | = 600 V |
| $I_{F(AVG)}$ | = 20 A |
| $Q_c$ | = 50 nC |

## Features

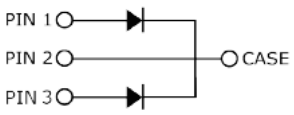
- 600-Volt Schottky Rectifier
- Zero Reverse Recovery Current
- Zero Forward Recovery Voltage
- High-Frequency Operation
- Temperature-Independent Switching Behavior
- Extremely Fast Switching
- Positive Temperature Coefficient on $V_F$

## Package


TO-247-3

## Benefits

- Replace Bipolar with Unipolar Rectifiers
- Essentially No Switching Losses
- Higher Efficiency
- Reduction of Heat Sink Requirements
- Parallel Devices Without Thermal Runaway




## Applications

- Switch Mode Power Supplies
- Power Factor Correction
  - Typical PFC $P_{out}$ : 2000W-4000W
- Motor Drives
  - Typical Power : 5HP-10HP

| Part Number | Package | Marking |
|---|---|---|
| C3D20060D | TO-247-3 | C3D20060 |

## Maximum Ratings

| Symbol | Parameter | Value | Unit | Test Conditions | Note |
|---|---|---|---|---|---|
| $V_{RRM}$ | Repetitive Peak Reverse Voltage | 600 | V | | |
| $V_{RSM}$ | Surge Peak Reverse Voltage | 600 | V | | |
| $V_{DC}$ | DC Blocking Voltage | 600 | V | | |
| $I_{F(AVG)}$ | Average Forward Current (Per Leg/Device) | 10/20 | A | $T_C$=150°C | |
| $I_{FRM}$ | Repetitive Peak Forward Surge Current (Per Leg/Device) | 67/134<br>44/88 | A | $T_C$=25°C, $t_p$=10 ms, Half Sine Wave, D=0.3<br>$T_C$=110°C, $t_p$=10 ms, Half Sine Wave, D=0.3 | |
| $I_{FSM}$ | Non-Repetitive Peak Forward Surge Current (Per Leg) | 90/157<br>71/115 | A | $T_C$=25°C, $t_p$=10ms, Half Sine Wave, D=0.3<br>$T_C$=110°C, $t_p$=10 ms, Half Sine Wave, D=0.3 | |
| $I_{FSM}$ | Non-Repetitive Peak Forward Surge Current (Per Leg/Device) | 250/500 | A | $T_C$=25°C, $t_p$=10 µs, Pulse | |
| $P_{tot}$ | Power Dissipation (Per Leg) | 136.3<br>59 | W | $T_C$=25°C<br>$T_C$=125°C | |
| $T_J$ , $T_{stg}$ | Operating Junction and Storage Temperature | -55 to +175 | °C | | |
| | TO-247 Mounting Torque | 1<br>8.8 | Nm<br>lbf-in | M3 Screw<br>6-32 Screw | |

# CMF20120D-Silicon Carbide Power MOSFET

*Z-FET™* MOSFET

N-Channel Enhancement Mode

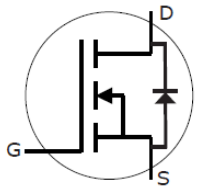
| | |
|---|---|
| $V_{DS}$ | = 1200 V |
| $R_{DS(on)}$ | = 80 mΩ |
| $I_{D(MAX)}$@$T_c$=25°C | = 33 A |

## Features

- Industry Leading $R_{DS(on)}$
- High Speed Switching
- Low Capacitances
- Easy to Parallel
- Simple to Drive
- Pb-Free Lead Plating, ROHS Compliant, Halogen Free

## Package


TO-247-3




## Benefits

- Higher System Efficiency
- Reduced Cooling Requirements
- Avalanche Ruggedness
- Increased System Switching Frequency

| Part Number | Package |
|---|---|
| CMF20120D | TO-247-3 |

## Applications

- Solar Inverters
- High Voltage DC/DC Converters
- Motor Drives

## Maximum Ratings

| Symbol | Parameter | Value | Unit | Test Conditions | Note |
|---|---|---|---|---|---|
| $I_D$ | Continuous Drain Current | 33 | A | $V_{GS}$@20V, $T_C$ = 25°C | |
| | | 17 | | $V_{GS}$@20V, $T_C$ = 100°C | |
| $I_{Dpulse}$ | Pulsed Drain Current | 78 | A | Pulse width $t_p$ limited by $T_{jmax}$ $T_C$ = 25°C | |
| $E_{AS}$ | Single Pulse Avalanche Energy | 2.2 | J | $I_D$ = 20A, $V_{DD}$ = 50 V, L = 9.5 mH | |
| $E_{AR}$ | Repetitive Avalanche Energy | 1.5 | J | $t_{AR}$ limited by $T_{jmax}$ | |
| $I_{AR}$ | Repetitive Avalanche Current | 20 | A | $I_D$ = 20A, $V_{DD}$ = 50 V, L = 3 mH $t_{AR}$ limited by $T_{jmax}$ | |
| $V_{GS}$ | Gate Source Voltage | -5/+25 | V | | |
| $P_{tot}$ | Power Dissipation | 150 | W | $T_c$=25°C | |
| $T_J$ , $T_{stg}$ | Operating Junction and Storage Temperature | -55 to +125 | °C | | |
| $T_L$ | Solder Temperature | 260 | °C | 1.6mm (0.063") from case for 10s | |
| $M_d$ | Mounting Torque | 1<br>8.8 | Nm<br>lbf-in | M3 or 6-32 screw | |

TranSiC

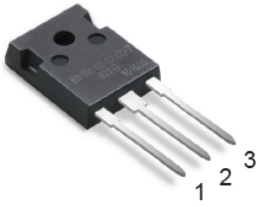
Preliminary Data Sheet

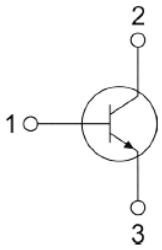
# BitSiC BT1206AC-P1

The BitSiC1206 is a 6 A power transistor developed and manufactured for high efficiency. These NPN bipolar junction transistors made of Silicon Carbide utilizes the latest BitSiC technology developed by TranSiC. This transistor is ideally suited for switched power applications requiring high efficiency and high current density of the semiconductors. The BitSiC offer very low on state losses combined with fast switching with very low temperature dependence.

| | |
|---|---|
| $V_{CEO}$ | 1200V |
| $V_{CE(SAT)}$ | 0.75V (6A, 150ºC) |
| $R_{ON(SAT)}$ | 125mΩ (150ºC) |

The BitSiC is packaged in a standard plastic TO-247 that can handle junction temperatures of up to 175 °C. The high operating temperature enables higher short time elevated junction temperatures that occur during periods of peak power in a numerous applications. This BitSiC is typically to be used in green systems like photo voltaic inverters as these applications benefit from the low losses of the BitSiC. However, every power application requiring high efficiency, light weight or small size benefits from using this high performance BitSiC. As well as applications requiring semiconductors with high resistance against radiation.




**Features**

- High operating junction temperature 175ºC
- Fast and temperature independent switching
- Wide reverse bias SOA
- Excellent capability to withstand short-circuit.
- Excellent immunity to cosmic rays

**Typical applications:**

- High temperature DC/DC converters
- High temperature AC/DC inverters
- High temperature Motor drives
- High temperature actuator controls

Maximum ratings, at T = 25°C, unless otherwise specified

| Parameter | Symbol | Conditions | Value | Unit |
|---|---|---|---|---|
| Collector-Emitter Voltage | $V_{CEO}$ | | 1200 | V |
| Emitter-Collector Voltage | $V_{EC}$ | | 30 | |
| Collector-Base Voltage | $V_{CBO}$ | | 1200 | |
| Emitter-Base Voltage | $V_{EBO}$ | | 30 | |
| Collector current | $I_C$ | DC | 6 | A |
| | $I_{CM}$ | $t_P$ < 10 ms | 20 | |
| | $I_{CP}$ | non rep. $t_P$ < 300 µs | 40 | |
| Base current | $I_B$ | DC | 1 | |
| | $I_{BM}$ | $t_P$ < 10 ms | 2 | |
| | $I_{BM}$ | non rep. $t_P$ < 300 µs | 10 | |
| Storage temperature | $T_{stg}$ | | -55 to 100 | ºC |
| Operating junction temperature | $T_{jmax}$ | | 175 | |
| Maximum power dissipation | $P_{TOT}$ | TO-247, $T_c$ = 25ºC | - | W |
| Mounting torque | | TO-247, M3 Screw | - | Ncm |

LINEAR TECHNOLOGY

# LT1107

## Micropower DC/DC Converter Adjustable and Fixed 5V, 12V

## FEATURES

- Operates at Supply Voltages from 2V to 30V
- Consumes Only 320µA Supply Current
- Works in Step-Up or Step-Down Mode
- Only Three External Components Required
- Low-Battery Detector Comparator On-Chip
- User Adjustable Current Limit
- Internal 1A Power Switch
- Fixed or Adjustable Output Voltage Versions
- Space Saving 8-Pin MiniDIP or SO-8 Package

## APPLICATIONS

- Palmtop Computers
- 3V to 5V, 5V to 12V Converters
- 24V to 5V, 12V to 5V Converters
- LCD Bias Generators
- Peripherals and Add-On Cards
- Battery Backup Supplies
- Cellular Telephones
- Portable Instruments

## DESCRIPTION

The LT®1107 is a versatile micropower DC/DC converter. The device requires only three external components to deliver a fixed output of 5V or 12V. Supply voltage ranges from 2V to 12V in step-up mode and to 30V in step-down mode. The LT1107 functions equally well in step-up, step-down, or inverting applications.

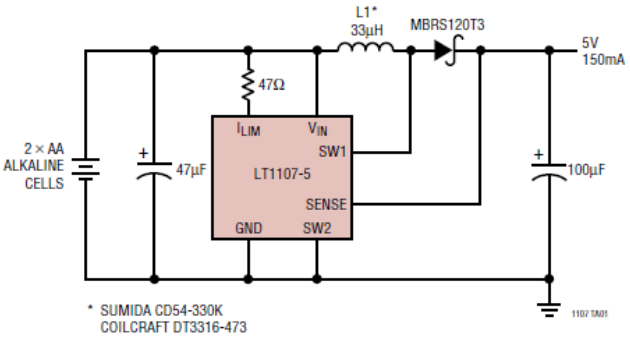
The LT1107 is pin-for-pin compatible with the LT1111, but has a duty cycle of 70%, resulting in increased output current in many applications. The LT1107 can deliver 150mA at 5V from a 2AA cell input and 5V at 300mA from 24V in step-down mode. Quiescent current is just 320µA, making the LT1107 ideal for power-conscious battery-operated systems. The 63kHz oscillator is optimized to work with surface mount inductors and capacitors.

Switch current limit can be programmed with a single resistor. An auxiliary gain block can be configured as a low-battery detector, linear post regulator, undervoltage lock-out circuit, or error amplifier.

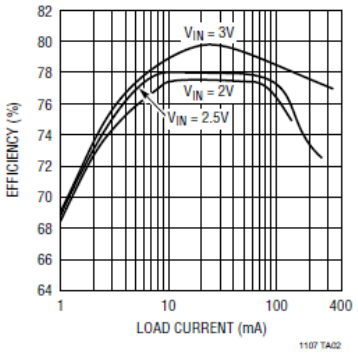


## TYPICAL APPLICATION

**Palmtop Computer Logic Supply**




**Efficiency**



Murata Power Solutions

# NMS Series

## 6kVDC Isolated 2W Dual Output DC/DC Converters

### FEATURES

- RoHS compliant
- UL1950 recognized
- Efficiency to 82%
- Power density up to 0.44W/cm³
- Dual outputs
- Low profile package
- UL 94V-0 package material
- No heatsink required
- Footprint 4.75cm²
- 6kVDC isolation
- 5V & 12V input
- 5V, 9V, 12V and 15V output
- Internal SMD construction
- Fully encapsulated with toroidal magnetics
- MTTF up to 747 kHrs
- PCB mounting

### DESCRIPTION

The NMS series of DC/DC converters are UL1950 recognized which makes them ideal for all telecom and safety applications where approved isolation is required. The low profile package allows mounting in rack systems without risk of touching other boards. The output configuration allows all of the rated power to be drawn from a single pin provided the total load does not exceed 2 watts. The devices feature low noise and low isolation capacitance suiltable for applications in high noise environments, e.g. heavy electrical machine interface.

c UL us

RoHS COMPLIANT 2002/95/EC

25

For full details go to www.murata-ps.com/rohs

### SELECTION GUIDE

| Order Code | Nominal Input Voltage | Output Voltage | Output Current | Efficiency | Isolation Capacitance | MTTF[1] |
|---|---|---|---|---|---|---|
| | V | V | mA | % | pF | kHrs |
| **NMS0505C** | 5 | ±5 | ±200 | 74 | 1.8 | 747 |
| **NMS0509C** | 5 | ±9 | ±111 | 76 | 1.9 | 327 |
| **NMS0512C** | 5 | ±12 | ±83 | 77 | 2.0 | 169 |
| **NMS0515C** | 5 | ±15 | ±67 | 78 | 2.1 | 93 |
| **NMS1205C** | 12 | ±5 | ±200 | 78 | 1.9 | 365 |
| **NMS1209C** | 12 | ±9 | ±111 | 81 | 2.0 | 224 |
| **NMS1212C** | 12 | ±12 | ±83 | 82 | 2.1 | 136 |
| **NMS1215C** | 12 | ±15 | ±67 | 82 | 2.2 | 82 |

When operated **with** additional external load capacitance the rise time of the input voltage will determine the maximum external capacitance value for guaranteed start up. The slower the rise time of the input voltage the greater the maximum value of the additional external capacitance for reliable start up.

### INPUT CHARACTERISTICS

| Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Voltage range | Continuous operation, 5V input types | 4.5 | 5 | 5.5 | V |
| | Continuous operation, 12V input types | 10.8 | 12 | 13.2 | |

### OUTPUT CHARACTERISTICS

| Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Rated Power[2] | $T_A$=0°C to 70°C | | | 2 | W |
| Voltage Set Point Accuracy | See tolerance envelope | -7.5 | | 10 | % |
| Line regulation | High $V_{IN}$ to low $V_{IN}$ | | 1.0 | 1.2 | %/% |
| Load Regulation | 10% load to rated load, 5V output types | | 10 | 15 | % |
| | 10% load to rated load, 9V output types | | 6 | 15 | |
| | 10% load to rated load, 12V output types | | 6 | 15 | |
| | 10% load to rated load, 15V output types | | 6 | 15 | |
| Ripple and Noise | BW=DC to 20MHz, all output types | | | 200 | mV p-p |

### ISOLATION CHARACTERISTICS

| Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Isolation test voltage | Flash tested for 1 second | 6000 | | | VDC |
| Resistance | Viso= 500VDC | | 10 | | GΩ |

### GENERAL CHARACTERISTICS

| Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Switching frequency | All input types | | 35 | | kHz |

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Short-circuit protection[3] | 1 second |
| Lead temperature 1.5mm from case for 10 seconds | 300°C |
| Internal power dissipation | 900mW |
| Input voltage $V_{IN}$, NMS05 types | 7V |
| Input voltage $V_{IN}$, NMS12 types | 15V |

1. Calculated using MIL-HDBK-217F with nominal input voltage at full load.
2. See derating graph.
3. Supply voltage must be disconnected at the end of the short circuit duration.

All specifications typical at $T_A$=25°C, nominal input voltage and rated output current unless otherwise specified.

# MIC4421/4422

## 9A-Peak Low-Side MOSFET Driver

## Bipolar/CMOS/DMOS Process

## General Description

MIC4421 and MIC4422 MOSFET drivers are rugged, efficient, and easy to use. The MIC4421 is an inverting driver, while the MIC4422 is a non-inverting driver.

Both versions are capable of 9A (peak) output and can drive the largest MOSFETs with an improved safe operating margin. The MIC4421/4422 accepts any logic input from 2.4V to $V_S$ without external speed-up capacitors or resistor networks. Proprietary circuits allow the input to swing negative by as much as 5V without damaging the part. Additional circuits protect against damage from electrostatic discharge.

MIC4421/4422 drivers can replace three or more discrete components, reducing PCB area requirements, simplifying product design, and reducing assembly cost.

Modern Bipolar/CMOS/DMOS construction guarantees freedom from latch-up. The rail-to-rail swing capability of CMOS/DMOS insures adequate gate voltage to the MOSFET during power up/down sequencing. Since these devices are fabricated on a self-aligned process, they have very low crossover current, run cool, use little power, and are easy to drive.

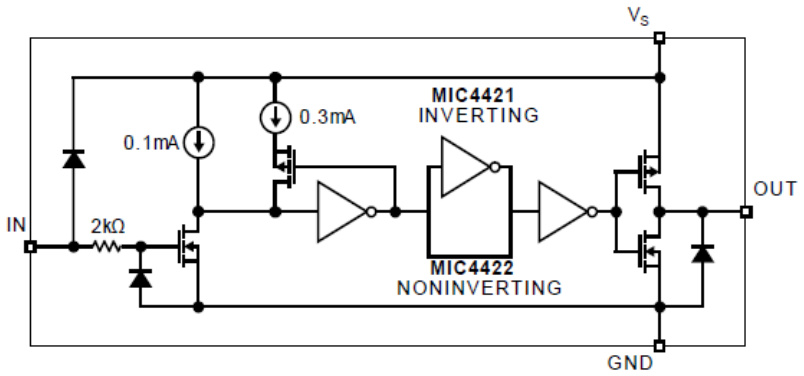
## Features

- BiCMOS/DMOS Construction
- Latch-Up Proof: Fully Isolated Process is Inherently Immune to Any Latch-up.
- Input Will Withstand Negative Swing of Up to 5V
- Matched Rise and Fall Times ..... 25ns
- High Peak Output Current ..... 9A Peak
- Wide Operating Range ..... 4.5V to 18V
- High Capacitive Load Drive ..... 47,000pF
- Low Delay Time ..... 30ns Typ.
- Logic High Input for Any Voltage from 2.4V to $V_S$
- Low Equivalent Input Capacitance (typ) ..... 7pF
- Low Supply Current ..... 450µA With Logic 1 Input
- Low Output Impedance ..... 1.5Ω
- Output Voltage Swing to Within 25mV of GND or $V_S$

## Applications

- Switch Mode Power Supplies
- Motor Controls
- Pulse Transformer Driver
- Class-D Switching Amplifiers
- Line Drivers
- Driving MOSFET or IGBT Parallel Chip Modules
- Local Power ON/OFF Switch
- Pulse Generators

## Functional Diagram



**B140HB**

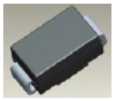
## 1.0A SURFACE MOUNT SCHOTTKY BARRIER RECTIFIER

### Features

- Low Leakage Current
- Guard Ring Die Construction for Transient Protection
- Ideally Suited for Automated Assembly
- Low Power Loss, High Efficiency
- Surge Overload Rating to 45A Peak
- **Lead Free, RoHS Compliant (Note 1)**
- **Green Molding Compound (No Halogen and Antimony) (Note 2)**

### Mechanical Data

- Case: SMB
- Case Material: Molded Plastic. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Lead Free Plating (Matte Tin Finish). Solderable per MIL-STD-202, Method 208 e3
- Polarity: Cathode Band or Cathode Notch
- Weight: 0.093 grams (approximate)



Top View

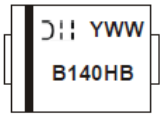
Bottom View

### Ordering Information (Note 3)

| Part Number | Case | Packaging |
|---|---|---|
| B140HB-13-F | SMB | 3000/Tape & Reel |

Notes:
1. EU Directive 2002/95/EC (RoHS). All applicable RoHS exemptions applied, see EU Directive 2002/95/EC Annex Notes.
2. Product manufactured with Data Code 0924 (week 24, 2009) and newer are built with Green Molding Compound.
3. For packaging details, go to our website at http://www.diodes.com.

### Marking Information



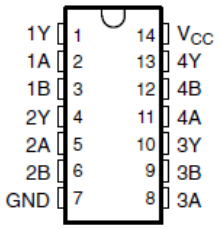

B140HB = Product type marking code
= Manufacturers' code marking
YWW = Date code marking
Y = Last digit of year (ex: 2 for 2002)
WW = Week code (01 to 53)

# SN54AHC02, SN74AHC02
# QUADRUPLE 2-INPUT POSITIVE-NOR GATES

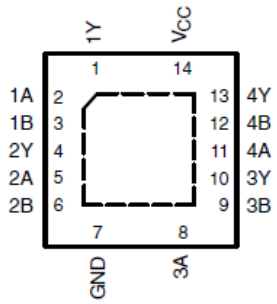
SCLS254K– DECEMBER 1995 – REVISED JULY 2003

- Operating Range 2-V to 5.5-V $V_{CC}$
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

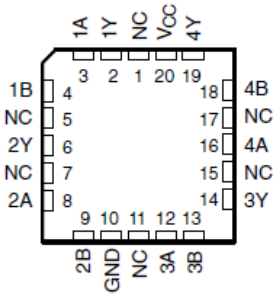
**SN54AHC02 . . . J OR W PACKAGE**
**SN74AHC02 . . . D, DB, DGV, N, NS OR PW PACKAGE**
**(TOP VIEW)**




**SN74AHC02 . . . RGY PACKAGE**
**(TOP VIEW)**




**SN54AHC02 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description/ordering information

The 'AHC02 devices contain four independent 2-input NOR gates that perform the Boolean function $Y = \overline{A} \cdot \overline{B}$ or $Y = \overline{A + B}$ in positive logic.

**ORDERING INFORMATION**

| $T_A$ | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| –40°C to 85°C | QFN – RGY | Tape and reel | SN74AHC02RGYR | HA02 |
| | PDIP – N | Tube | SN74AHC02N | SN74AHC02N |
| | SOIC – D | Tube | SN74AHC02D | AHC02 |
| | | Tape and reel | SN74AHC02DR | |
| | SOP – NS | Tape and reel | SN74AHC02NSR | AHC02 |
| | SSOP – DB | Tape and reel | SN74AHC02DBR | HA02 |
| | TSSOP – PW | Tube | SN74AHC02PW | HA02 |
| | | Tape and reel | SN74AHC02PWR | |
| | TVSOP – DGV | Tape and reel | SN74AHC02DGVR | HA02 |
| –55°C to 125°C | CDIP – J | Tube | SNJ54AHC02J | SNJ54AHC02J |
| | CFP – W | Tube | SNJ54AHC02W | SNJ54AHC02W |
| | LCCC – FK | Tube | SNJ54AHC02FK | SNJ54AHC02FK |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

# BC636; BCP51; BCX51

## 45 V, 1 A PNP medium power transistors

Rev. 08 — 22 February 2008 Product data sheet

## 1. Product profile

### 1.1 General description

PNP medium power transistor series.

Table 1. Product overview

| Type number[1] | Package | | | NPN complement |
|---|---|---|---|---|
| | NXP | JEITA | JEDEC | |
| BC636[2] | SOT54 | SC-43A | TO-92 | BC635 |
| BCP51 | SOT223 | SC-73 | - | BCP54 |
| BCX51 | SOT89 | SC-62 | TO-243 | BCX54 |

[1] Valid for all available selection groups.

[2] Also available in SOT54A and SOT54 variant packages (see Section 2).

### 1.2 Features

- High current
- Two current gain selections
- High power dissipation capability

### 1.3 Applications

- Linear voltage regulators
- High-side switches
- MOSFET drivers
- Amplifiers

### 1.4 Quick reference data

Table 2. Quick reference data

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CEO}$ | collector-emitter voltage | open base | - | - | –45 | V |
| $I_C$ | collector current | | - | - | –1 | A |
| $I_{CM}$ | peak collector current | single pulse; $t_p \leq 1$ ms | - | - | –1.5 | A |
| $h_{FE}$ | DC current gain | $V_{CE}$ = –2 V; $I_C$ = –150 mA | 63 | - | 250 | |
| | $h_{FE}$ selection -10 | $V_{CE}$ = –2 V; $I_C$ = –150 mA | 63 | - | 160 | |
| | $h_{FE}$ selection -16 | $V_{CE}$ = –2 V; $I_C$ = –150 mA | 100 | - | 250 | |

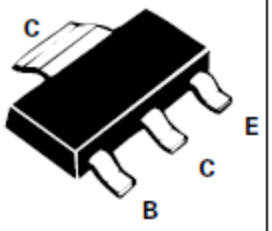
# SOT223 NPN SILICON PLANAR HIGH CURRENT (HIGH PERFORMANCE) TRANSISTORS

**FZT851**
**FZT853**

ISSUE 2 - OCTOBER 1995

FEATURES

* Extremely low equivalent on-resistance; $R_{CE(sat)}$ 44mΩ at 5A
* 6 Amps continuous current, up to 20 Amps peak current
* Very low saturation voltages
* Excellent $h_{FE}$ characteristics specified up to 10 Amps




PARTMARKING DETAILS - DEVICE TYPE IN FULL
COMPLEMENTARY TYPES - FZT851 FZT951
FZT853 FZT953

## ABSOLUTE MAXIMUM RATINGS.

| PARAMETER | SYMBOL | FZT851 | FZT853 | UNIT |
|---|---|---|---|---|
| Collector-Base Voltage | $V_{CBO}$ | 150 | 200 | V |
| Collector-Emitter Voltage | $V_{CEO}$ | 60 | 100 | V |
| Emitter-Base Voltage | $V_{EBO}$ | 6 | 6 | V |
| Peak Pulse Current | $I_{CM}$ | 20 | 10 | A |
| Continuous Collector Current | $I_C$ | 6 | | A |
| Power Dissipation at $T_{amb}$=25°C | $P_{tot}$ | 3 | | W |
| Operating and Storage Temperature Range | $T_j$:$T_{stg}$ | -55 to +150 | | °C |

*The power which can be dissipated assuming the device is mounted in a typical manner on a P.C.B. with copper equal to 4 square inch minimum

SILICON LABS

# Si8220/21

## 0.5 AND 2.5 AMP ISODRIVERS WITH OPTO INPUT (2.5, 3.75, AND 5.0 $kV_{RMS}$)

### Features

- Functional upgrade for HCPL-0302, HCPL-3120, TLP350, and similar opto-drivers
- 60 ns propagation delay max (independent of input drive current)
- 14x tighter part-to-part matching versus opto-drivers
- 2.5, 3.75, and 5.0 $kV_{RMS}$ isolation
- Transient Immunity
  - 30 kV/µs
- Under-voltage lockout protection with hysteresis
- Resistant to temperature and aging effects
- Gate driver supply voltage
  - 6.5 V to 24 V
- Wide operating range
  - –40 to +125 °C
- RoHS-compliant packages
  - SOIC-8 narrow body
  - SOIC-16 wide body

### Applications

- IGBT/ MOSFET gate drives
- Industrial control systems
- Switch mode power supplies
- UPS systems
- Motor control drives
- Inverters

### Safety Regulatory Approvals

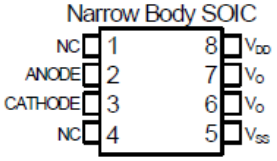
- UL 1577 recognized
  - Up to 5000 Vrms for 1 minute
- CSA component notice 5A approval
  - IEC 60950-1, 61010-1, 60601-1 (reinforced insulation)
- VDE certification conformity
  - IEC 60747-5-2 (VDE 0884 Part 2)
  - EN 60950-1 (reinforced insulation)

### Description

The Si8220/21 is a high-performance functional upgrade for opto-coupled drivers, such as the HCPL-3120 and the HPCL-0302 providing 2.5 A of peak output current. It utilizes Silicon Laboratories' proprietary silicon isolation technology, which provides a choice of 2.5, 3.75, or 5.0 $kV_{RMS}$ withstand voltages per UL1577. This technology enables higher performance, reduced variation with temperature and age, tighter part-to-part matching, and superior common-mode rejection compared to opto-isolated drivers. While the input circuit mimics the characteristics of an LED, less drive current is required, resulting in increased efficiency. Propagation delay time is independent of input drive current, resulting in consistently short propagation time, tighter unit-to-unit variation, and greater input circuit design flexibility.

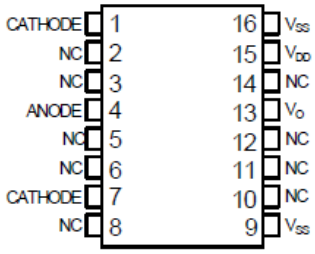
**Pin Assignments:**
**See page 19**

Narrow Body SOIC




Top View

Wide Body SOIC




Top View

Patent pending

April 1995

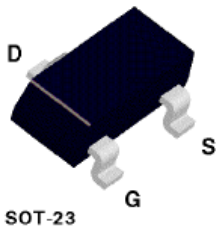
# BS170 / MMBF170
## N-Channel Enhancement Mode Field Effect Transistor

### General Description

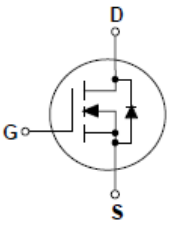
These N-Channel enhancement mode field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. These products have been designed to minimize on-state resistance while provide rugged, reliable, and fast switching performance. They can be used in most applications requiring up to 500mA DC. These products are particularly suited for low voltage, low current applications such as small servo motor control, power MOSFET gate drivers, and other switching applications.

### Features

- High density cell design for low $R_{DS(ON)}$.
- Voltage controlled small signal switch.
- Rugged and reliable.
- High saturation current capability.




SOT-23




### Absolute Maximum Ratings

$T_A$ = 25°C unless otherwise noted

| Symbol | Parameter | BS170 | MMBF170 | Units |
|---|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | 60 | | V |
| $V_{DGR}$ | Drain-Gate Voltage ($R_{GS} \leq 1M\Omega$) | 60 | | V |
| $V_{GSS}$ | Gate-Source Voltage | ± 20 | | V |
| $I_D$ | Drain Current - Continuous | 500 | 500 | mA |
| | - Pulsed | 1200 | 800 | |
| $P_D$ | Maximum Power Dissipation | 830 | 300 | mW |
| | Derate Above 25°C | 6.6 | 2.4 | mW/°C |
| $T_J, T_{STG}$ | Operating and Storage Temperature Range | -55 to 150 | | °C |
| $T_L$ | Maximum Lead Temperature for Soldering Purposes, 1/16" from Case for 10 Seconds | 300 | | °C |
| **THERMAL CHARACTERISTICS** | | | | |
| $R_{\theta JA}$ | Thermal Resistacne, Junction-to-Ambient | 150 | 417 | °C/W |

BS170 Rev. C / MMBF170 Rev. D

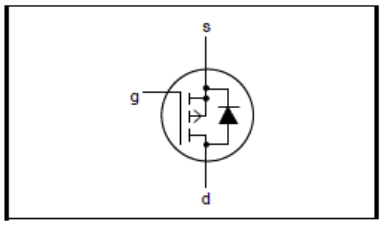
# P-channel enhancement mode MOS transistor

# BSH201

## FEATURES

- Low threshold voltage
- Fast switching
- Logic level compatible
- Subminiature surface mount package

## SYMBOL




## QUICK REFERENCE DATA

$V_{DS}$ = -60 V

$I_D$ = -0.3 A

$R_{DS(ON)} \leq 2.5\ \Omega$ ($V_{GS}$ = -10 V)

## GENERAL DESCRIPTION

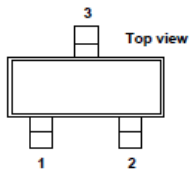
P-channel, enhancement mode, logic level, field-effect power transistor. This device has low threshold voltage and extremely fast switching making it ideal for battery powered applications and high speed digital interfacing.

The BSH201 is supplied in the SOT23 subminiature surface mounting package.

## PINNING

| PIN | DESCRIPTION |
|---|---|
| 1 | gate |
| 2 | source |
| 3 | drain |

## SOT23




## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_{DS}$ | Drain-source voltage | | - | -60 | V |
| $V_{DGR}$ | Drain-gate voltage | $R_{GS}$ = 20 kΩ | - | -60 | V |
| $V_{GS}$ | Gate-source voltage | | - | ± 20 | V |
| $I_D$ | Drain current (DC) | $T_a$ = 25 °C | - | -0.3 | A |
| | | $T_a$ = 100 °C | - | -0.19 | A |
| $I_{DM}$ | Drain current (pulse peak value) | $T_a$ = 25 °C | - | -1.2 | A |
| $P_{tot}$ | Total power dissipation | $T_a$ = 25 °C | - | 0.417 | W |
| | | $T_a$ = 100 °C | - | 0.17 | W |
| $T_{stg}$, $T_j$ | Storage & operating temperature | | - 55 | 150 | °C |

## THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| $R_{th\ j\text{-}a}$ | Thermal resistance junction to ambient | FR4 board, minimum footprint | 300 | - | K/W |