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Design of an RF PA and Linear Dynamic Supplies for Power Envelope Tracking (PET) on Gate and Drain

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Summary

This thesis is about the design and production of a class AB power amplifier, gate tracker circuit and drain tracker circuit. A newly developed envelope tracking (ET) technique called Power Envelope Tracking (PET) is evaluated and tested by using the manufactured designs.

The designed power amplifier (PA) has a small signal gain of 13.0dB and a 1dB bandwidth of 450MHz around a center frequency of 2.4GHz. Peak power added efficiency (PAE) is 53.3% at an output power of 40.5dBm. The 3rd order intermodulation distortion (IMD) is -17dBc at an output power of 37dBm.

The designed drain tracker has a controllable linear gain of 0 to 50 times, with a -6dB gain bandwidth of 200MHz. The frequency where the first 180° phase shift occurs is 100MHz and the output impedance at 50MHz is (5.5 + j2.8)Ω.
For the gate tracker, the controllable linear gain is 0 to 10 times, with a -6dB gain bandwidth of 250MHz. The frequency where the first 180° phase shift occurs is 250MHz and the output impedance at 50MHz is (14.6 + j56.2)Ω.

Simulations and measurements of the PET technique show that there are clear benefits by using the technique. Compared to the more traditional ET technique, the PET technique achieves better linearity and almost the same efficiency at a lower required tracking bandwidth. Simulations show that the bandwidth required for ET is 3 times larger than the bandwidth required for PET. When comparing a PA that uses PET to modulate the supply voltages with a PA that uses constant supply voltages there are substantial benefits. For a 1MHz QAM signal, the PAE is 9.4% higher, the EVM is 2.4% lower, the ACPR is on average 8.3dBc lower and the signal to total distortion ratio (STDR) is 7.7dB higher.

Sammendrag

Denne masteroppgaven handler om designet og produksjonen av en klasse AB effektforsterker, en gate tracker krets og en drain tracker krets. En nyutviklet envelope tracking (ET) teknikk som kalles Power Envelope Tracking (PET) er vurdert og testet ved å bruke de produserte designene.

Den designede effektforsterken har en småsignal forsterkning på 13.0dB og 1dB båndbredde på 450MHz rundt en senterfrekvens på 2.4GHz. Maksimal power added efficiency (PAE) er 53.3% ved en utgangseffekt på 40.5dBm. Tredje ordens intermodulasjons distorsjon er -17dBc ved en utgangseffekt på 37dBm.

Den designede drain trackeren har en kontrollerbar lineære forsterkning mellom 0 og 50 ganger, med en -6dB båndbredde på 200MHz. Frekvensen der det første 180° faseskiftet oppstår er 100MHz, og utgangsimpedansen ved 50MHz er (5.5 + j2.8)Ω.

For gate trackeren er den kontrollerbare lineære forsterkningen mellom 0 og 10 ganger, med en -6dB båndbredde på 250MHz. Frekvensen der det første 180° faseskiftet oppstår er 250MHz, og utgangsimpedansen ved 50MHz er (14.6 + j56.2)Ω.

Simuleringer og målinger av PET teknikken viser at det er klare fordeler ved å bruke denne teknikken. Sammenlignet med den mer tradisjonelle ET teknikken oppnår man bedre linearitet, nesten lik effektivitet, samt lavere nødvendig tracking båndbredde når man bruker PET teknikken. Simuleringer viser at den nødvendige båndbredden for ET er 3 ganger større enn den nødvendige båndbredden for PET. Når man sammenligner en effektforsterker som bruker PET for å modulere driftsspenningene med en effektforsterker som bruker konstante driftsspenninger, ser man klare fordeler med PET. For et 1MHz QAM signal er PAE 9.4% høyere, EVM 2.4% lavere, ACPR er i gjennomsnitt 8.3dBc lavere og STDR er 7.7dB høyere.

Table of Contents

Abbreviations

RF	=	Radio frequency
PA	=	Power amplifier
GaN	=	Gallium nitrade
HEMT	=	High-electron-mobility transistor
PAE	=	Power added efficiency
PET	=	Power envelope tracking
DUT	=	Device under test
IMD	=	Intermodulation distortion
DC	=	Direct current
QAM	=	Quadrature amplitude modulation
ACPR	=	Adjacent channel power ratio
EVM	=	Error vector magnitude
STDR	=	Signal to total distortion ratio

Chapter 1

Introduction

1.1 Motivation

There is significant activity around the subject of Power Amplifiers both in industry and in universities as well as science-centres. Power amplifiers have great economic and technological importance because they are one of the main cost drivers in development and manufacturing of radio-equipment, and therefore a crucial component in our wireless world. In portable devices, the PA accounts for a significant amount of the battery's power usage. This is also the case for base stations. In fact, in 2014, base stations consumed 1% of global electricity [1]. Technical good and efficient PA solutions both in handheld devices and base stations are therefore very important.

1.2 Problem description

The designs and experiments presented in this report is made as a master thesis in analog circuit design and radio systems at NTNU. A PA is designed based on the PA presented by Høydal in [2]. It is based on a packaged discrete transistor by Wolfspeed (CGH40010), which is a 10W GaN HEMT device. The operating frequency is set to 2.4GHz with a 1dB bandwidth of at least 200MHz. The gain should exceed 12dB and the output power should be above 40dBm. In addition, the efficiency and linearity should be as good as possible.

To increase the efficiency and linearity of the PA, a technique called power envelope tracking [3], is demonstrated on the gate and drain of a power amplifier. The gate tracking aims to enhance the linearity and the efficiency of the amplifier, while the drain tracking will enhance the DC-RF efficiency of the amplifier. Linear tracker circuits for gate and drain are therefore designed. These circuits should have as high bandwidth as possible, while keeping the distortion at a minimum. This is important in order to achieve fast and accurate tracking. Since the tracker circuits are linear, they are not very efficient. It is therefore the PA efficiency that is maximized and not the total efficiency.

Chapter 2

Theory

2.1 Amplifier classes

When designing an amplifier, a broad variety of classes can be used. Class A, AB, B and C amplifiers are classified by their biaspoint, which will set the conduction angle for the amplifier. A lower conduction angle usually results in higher efficiency, but lower linearity, and vice versa. This is shown in Figure 2.1. Other classes, such as class D, E and F uses other techniques, including using the transistor as a switch and harmonic tuning to increase the efficiency of the amplifier.

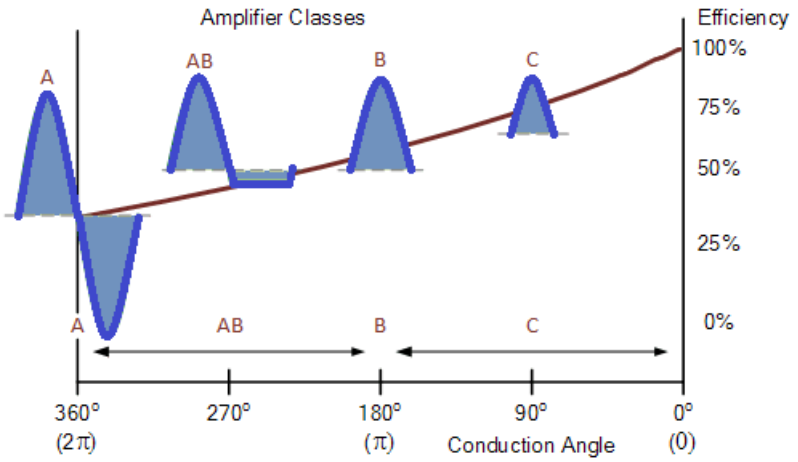

Figure 2.1: Efficiency and conduction angle for different amplifier classes

2.1.1 Operating point of a class AB amplifier

One specific type of amplifier is the class AB amplifier. It is accomplished by biasing the transistor such that the DC drain current has a value between zero and half the maximum DC drain current, given by the inequality: $0 < I_{DS} < I_{max}/2$. The class AB amplifier is a compromise between the class A and class B amplifiers, providing higher efficiency than a class A amplifier and better linearity than a class B amplifier as shown in Figure 2.1. Figure 2.2 shows the operating curve of the class AB amplifier. The point Q is the operating point of the class AB amplifier. Points A and B are the operating points of a class A amplifier and a class B amplifier. It is seen that the operating point of the AB amplifier is somewhere between the operating points of the A and B amplifiers.

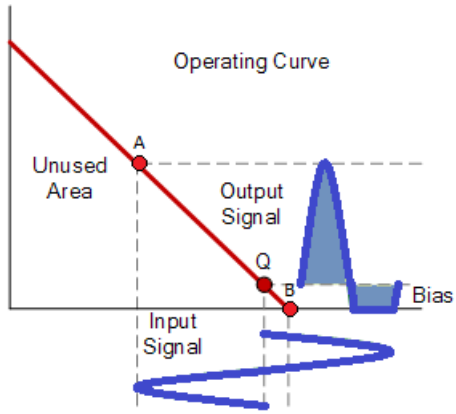

Figure 2.2: Operating curve for class AB amplifier

2.2 DC bias network

In order to protect the DC sources on gate and drain, bias networks needs to be placed between the transistor and the DC sources, as shown in figure 2.3.

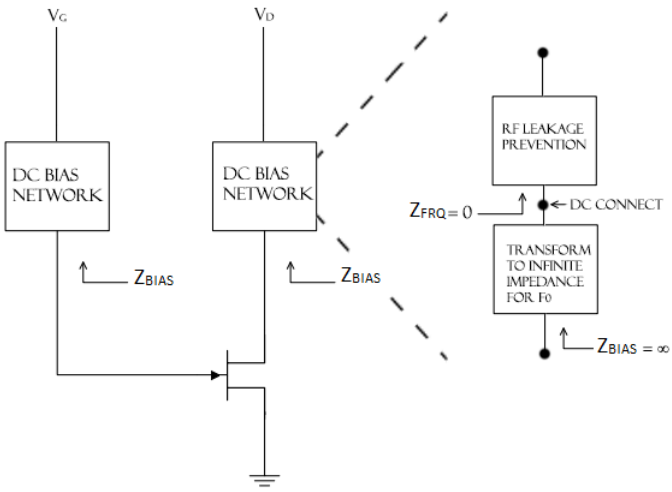

Figure 2.3: Placement of DC bias network

To affect the DC sources minimally, the bias network must provide zero RF leakage to the DC sources. This means that $Z_{BIAS} = \infty$ at f_0, and Z_{BIAS} is well defined at all other frequencies. As illustrated in figure 2.3 a bias network usually consists of two parts. One part that transforms Z_{BIAS} to ∞ at f_0. This can be realized by using a large inductor giving $Z_L = j\omega L_{LARGE} \rightarrow \infty$ or by using a quarter wavelength transformer tuned such that $Z_{BIAS} = \infty$ at f_0. The other part shorts all other frequencies to ground to prevent leakage to the DC source. This can be accomplished by introducing a network of capacitors connected to ground between the DC connect and the DC source, as shown in figure 2.4. The values of the capacitors are chosen to be ”low”, ”medium” and ”large” to ensure that a wide range of frequencies will be shorted. To prevent shorting of the tracking signal when tracking is used, large capacitors in the bias network must be removed in order to achieve correct tracking operation.

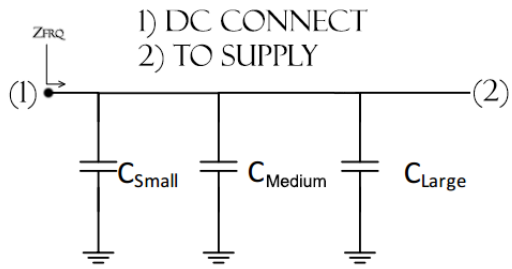

Figure 2.4: Frequency shorting circuit.

2.3 Stabilization and stabilization network

A crucial part when designing an amplifier is to ensure its stability. Failing to do so could introduce oscillations or other unstabilities, which is undesired. To avoid this it is common to design the amplifier such that it is unconditionally stable for all frequencies. This means that the stability circles at the input and output should either be totally outside the smith chart or cover the whole Smith chart, as illustrated in figure 2.5.

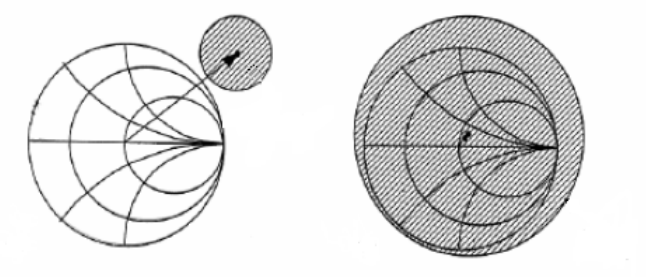

Figure 2.5: Stabilization circles either totally outside or covering the whole Smith chart

One technique of measuring the stability is by using the μ factor, which is defined by equation 2.1. [4]

$$\mu = \frac{1 - \mid S_{11} \mid}{\mid S_{22} - S_{11}^{*} \mid + \mid S_{21} S_{12} \mid} > 1 \tag{2.1}$$

If the μ factor is greater than 1, the amplifier is unconditionally stable at the given frequency. The μ factor also gives an indication of how stable the device is, where a higher value indicates a higher stability. To make a device stable, resisitive loading may be used to alter the position of the stability circles and increase the μ factor.

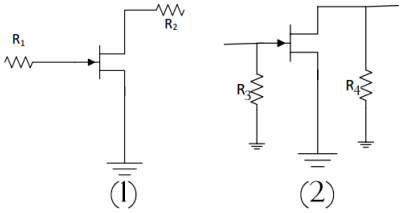

Figure 2.6: Resistive loading

Figure 2.6 illustrates two stabilization networks which may be used to increase the μ factor. Type 1 in figure 2.6 moves the stability circles along an increasing real impedance, and type 2 moves the stability circles along an increasing real admittance in the smith chart. In PA designs, loss at the output should be avoided to prevent attenuation of the already am-

plified signal. Another way of stabilizing the device is to use frequency selective loading. This stabilization network will introduce loss at a given frequency range.

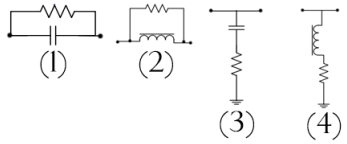

Figure 2.7: Frequency selective loading configurations

Some examples of frequency selective loading is illustrated in figure 2.7. Network 1 or 2 in figure 2.7 could replace the series resistor in figure 2.6 and introduce loss for frequencies below $\frac{1}{RC}$ for network 1, and for frequencies above $\frac{1}{RL}$ for network 2. The shunt resistors in figure 2.6 may be replaced by network 3 or 4 in figure 2.7, where they introduce loss for frequencies above $\frac{1}{RC}$ and below $\frac{1}{RL}$ respectively.

2.4 Impedance matching

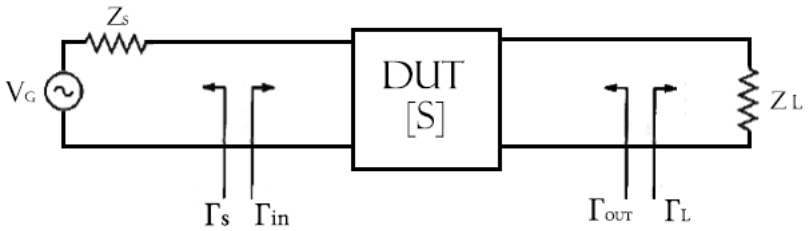

Figure 2.8: Impedances of DUT

Figure 2.8 shows the impedances seen at the input and output of a device, respectively Γ_{in} and Γ_{out}. And the impedances seen at the source and load, respectively Γ_S and Γ_L. It is possible to introduce matching networks between input and source aswell as between output and load, to alter Γ_S and Γ_L as desired. This is called impedance matching.

2.4.1 Matching for maximum power transfer

For PAs it is desired to match for maximum power transfer. This is realized by a complex conjugate matching network. To make a conjugate match, a network that sets $\Gamma_S = \Gamma_{in}^*$ is introduced between the source and device. For the load, a network that sets $\Gamma_L = \Gamma_{out}^*$ is introduced between the load and device. It is worth noting that the amplifier will be narrowbanded when matched for maximum power transfer. It is therefore common to allow some mismatch at the input to make the amplifier more broadbanded.

2.4.2 Matching with harmonic tuning

It is also possible to implement matching networks that controls the harmonics of a signal. Since the harmonics are introduced at the output of the amplifier, harmonically tuned matching networks are used for output matching. This is done by having a network that is tuned to have a specific impedance value for a specific frequency. An example of an architecture that utilizes harmonic tuning is the class F amplifier. For a class F amplifier the impedances for all odd harmonics are set to ∞, resulting in a theoretical efficiency of 100%. Other amplifier classes such as class AB can also utilize harmonic tuning to increase the efficiency.

2.5 Power added efficiency (PAE)

Power added efficiency is a means of measuring the efficiency of an amplifier. It is given by equation 2.2. Where G is the gain, P_{out} is the RF output power, P_{in} is the RF input power, P_{DC} is the DC input power and η is the drain efficiency. [5]

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} = \frac{P_{out} - \frac{P_{out}}{G}}{P_{DC}} = \eta \cdot (1 - \frac{1}{G}) \tag{2.2}$$

2.6 Envelope tracking (ET)

Envelope tracking is a technique which is used to increase the efficiency of a PA. This is achieved by using the envelope of the signal to alter the supply voltage of the PA proportionally to the envelope. The principle of this technique is shown in figure 2.9.

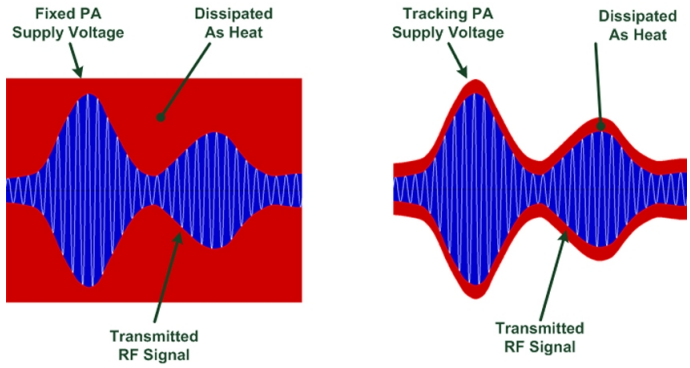

Figure 2.9: Left: PA with fixed supply voltage. Right: Supply voltage modulated using ET. [6]

As seen, the voltage supply is ”tracking” the envelope. This allows the PA to operate close to saturation for all envelope levels, resulting in increased efficiency. For more information on ET see [7].

2.7 Power envelope tracking (PET)

A variation of ET is Power envelope tracking (PET). PET is a newly developed technique that significantly reduces the bandwidth required of the drain supply for an envelope tracked PA. The basis of this technique is to develop a drain voltage function that tracks the power of the envelope. Morten Olavsbråten and Dragan Gecan shows in reference [3] that this drain voltage function can be given by equation 2.3.

$$v_d(t) = a_0 + a_2 \cdot v_{s,env}^2 = a_0 + a_2 \cdot p_{env}(t) \tag{2.3}$$

Where $p_{env}(t)$ is the power of the envelope, given by $p_{env}(t) = v_s(t) * v_s^*(t) = v_{s,env}^2$, $v_{s,env}$ is the envelope of the input signal and a_0 and a_2 are constants, thus giving 2 degrees of freedom. An extension to this function is the 2nd order PET, given by equation 2.4. Higher order extensions follow the same trend.

$$v_d(t) = a_0 + a_2 \cdot p_{env}(t) + a_4 \cdot p_{env}^2(t) \tag{2.4}$$

In [3] it is shown that: "The use of pure Power Envelope Tracking (PET) results in significant lower bandwidth, with some reduction of efficiency, compared to ET. A 2nd order PET extension doubles the PET bandwidth and achieve almost the same efficiency as ET". For a more thorough explanation of PET, see reference [3].

2.8 Linearity metrics

To quantize the linearity of the PA, the metrics third-order intermodulation distortion (TO-IMD), adjacent channel power ratio (ACPR), error vector magnitude (EVM) and signal to total distortion ratio (STDR) are used.

Third-order intermodulation distortion is the measure of the third-order distortion products that the PA produces when two tones closely spaced in frequency are fed at the input. This distortion is normally close to the carrier and thus hard to filter out. Therefore, TO-IMD is a useful metric to inspect when looking at the linearity of the PA.

The adjacent channel power ratio is somewhat related to the TO-IMD. ACPR is the ratio between the adjacent channel, meaning the intermodulation signal, and the main channel, which is the useful signal. TO-IMD and ACPR are both measured in dBc, meaning decibels relative to carrier.

For a digitally modulated signal being transmitted by an ideal transmitter, the constellation points will be at ideal locations. Ideal transmitters do not exist and the actual constellation points will therefore deviate from the ideal locations. The error vector magnitude is a measure of how far away the actual points are from the ideal points. It is calculated by using formula 2.5. Here, P_{ref} is the amplitude of the outermost point in the constellation diagram and P_{error} is the amplitude of the error vector. This is illustrated in figure 2.10.

$$EVM(\%) = \sqrt{\frac{P_{error}}{P_{ref}}} \cdot 100\% \tag{2.5}$$

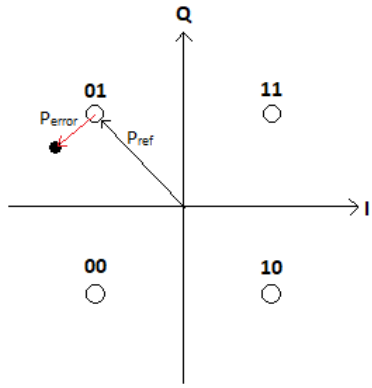

Figure 2.10: Constellation diagram of 4QAM illustrating the EVM

Signal to total distortion ratio is a metric that evaluates the distortion outside of the signal bandwidth (ACPR) and the distorion inside the signal bandwidth (EVM) and incorporates them in one metric, the STDR. This is very useful when optimizing a PA for linearity, instead of optimizing both the ACPR and EVM, only the STDR needs to be optimized. STDR is measured in dB, and a higher value translates to better linearity. For the derivation of STDR, see [8] and [9].

Chapter 3

Design & Implementation

3.1 Design of PA

A revised version of the PA designed in [2] is designed. The PA is designed according to the specifications in table 3.1.

	Specification
Frequency (f_0)	2.4GHz
1dB Bandwidth (B)	200MHz
Gain (G)	$>$12dB
Output Power (P_o)	$>$40dBm
Efficiency	As high as possible
Linearity	As good as possible with 2 tone test
Area	100mm x 100mm

Table 3.1: Design specifications

The design process of the PA follows the procedure explained in table 3.2.

Step 1	Choose bias point
Step 2	Check stability and design stability network
Step 3	Design of the bias networks
Step 4	Design of the matching networks
Step 5	Fine tuning
Step 6	Design of the layout
Step 7	Manufacturing and measurements

Table 3.2: Design procedure

Agilent ADS is the software used to design and simulate the PA. The substrate used is the FR-4 substrate. The properties of the substrate are described in table 3.3.

H	ϵ_r	μ_r	Cond	T	TanD
$1.6 * 10^{-3}m$	4.4	1.0	$5.96 * 10^7$	$35 * 10^{-6}m$	0.02

Table 3.3: Electrical properties for the FR-4 substrate.

Where H is the substrate thickness, ϵ_r is the relative dielectric constant, μ_r is the relative permeability, Cond is the conductor conductivity in Siemens/meter, T is the conductor thickness and TanD is the dielectric loss tangent.

3.1.1 Choice of nominal bias point

Since the amplifier is to be used with PET on gate and drain it will vary between Class A, AB and B depending on the gate voltage. The amplifier is therefore designed with a nominal bias point that makes it a class AB amplifier. As described in section 2.1.1 this means that the drain current has a value between zero and half of the maximum DC drain current. In this design, the amplifier is nominally biased such that I_{DS} = 250mA. In the simulations, this corresponds to a gate voltage of V_G = -2.6V. During the design the drain voltage has a value of V_D = 28V.

3.1.2 Stabilization

To ensure the stability of the PA, a stability circuit is designed. This is realized by implementing a frequency selective RC-tank at the input of the transistor, as well as adding a resistor between the DC-feed and input matching network. To assure further stability at lower frequencies, a 50Ω line to ground is introduced right before the DC-block. The stability network can be seen in figure 3.5.

3.1.3 Design of the bias network

As described in section 2.2, bias networks has to be implemented in order to minimally affect the DC sources. In this design, a $\frac{\lambda}{4}$ radial stub tuned for f_0 is used in conjunction with one shorting capacitor of 10pF. The PA is to be used with PET, therefore, only one small shorting capacitor is used in order to minimize the capacitance on the output of the tracker circuits. The DC-feed lines are used as a part of the matching networks. Additionaly, the DC feed points are optimized, meaning that the DC will be inserted at the most optimum point in the circuit. The bias network can be seen in figure 3.5.

3.1.4 Design of matching networks

The PA is designed according to the architecture shown in figure 3.1. As seen, input and output matching networks must be implemented.

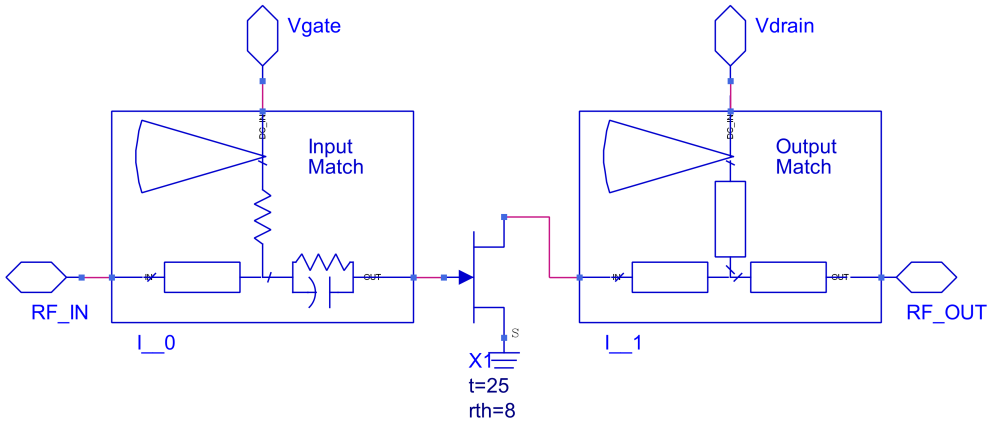

Figure 3.1: PA architecture

Output matching network

In order to achieve a highly efficient PA, the output matching network is implemented as a harmonically tuned network, as described in section 2.4.2. To increase the efficiency, a full reflection of the second and third harmonics is desired. By using a load-pull test bench in ADS to find the loads that ensures the highest efficiency, optimum loads for f, $2f$ and $3f$ are found for f = 2.3GHz, 2.4GHz, 2.5GHz. These loads are plotted in a smith chart giving nine points as shown in figure 3.2. To get the desired reflections, S11 for the matching network is optimized to get as close as possible to the optimum load points for the respective frequencies. Figure 3.3 shows S11 of the matching network and the optimum load points plotted in a smith chart.

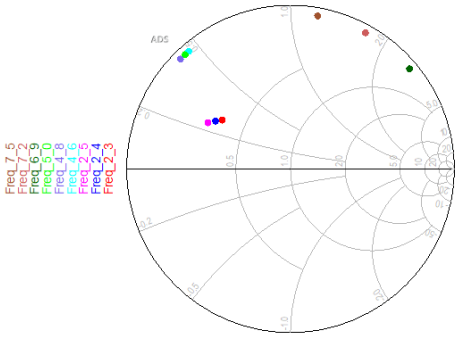

Figure 3.2: Optimum load points for output matching network.

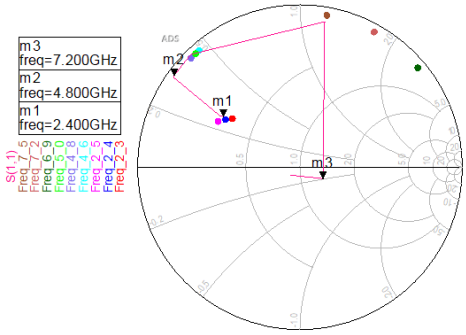

Figure 3.3: Optimum load points and S11.

The simulation model of the output matching network can be seen in figure 3.4. The circuit element legend is seen in figure 7.1 in the appendix.

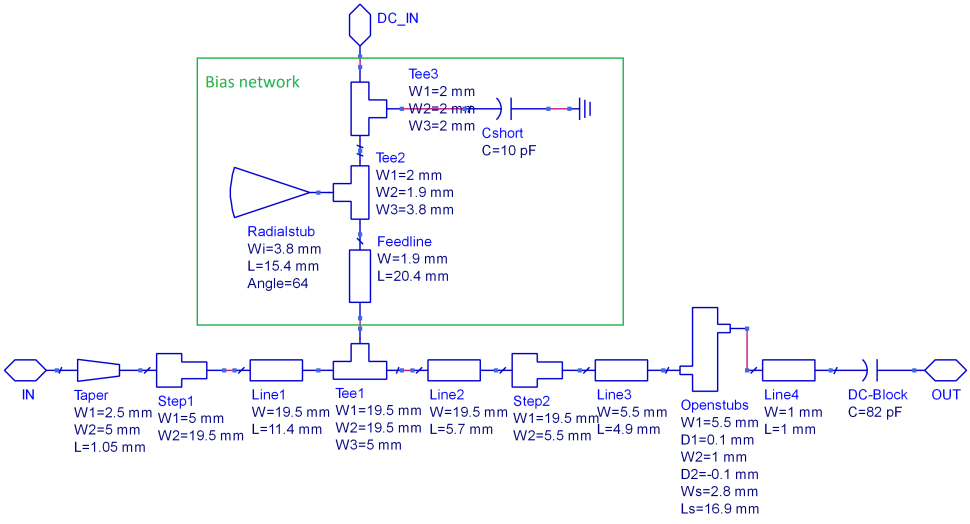

Figure 3.4: Simulation model of the output matching network

Input matching network

At the input, the matching network is designed as a complex conjugate match in order to achieve maximum power transfer. As described in section 2.4.1 a perfect complex conjugate match gives a narrowbanded PA. Some mismatch is therefore allowed in order to meet the requirements for the 1dB bandwidth. To achieve this, a 4-element match consisting of 3 microstrip lines and 1 symmetric pair of open stubs is implemented. Here, one of the microstrip lines used in the matching network is the DC-feed line. Figure 3.5 shows the simulation model of the input matching network.

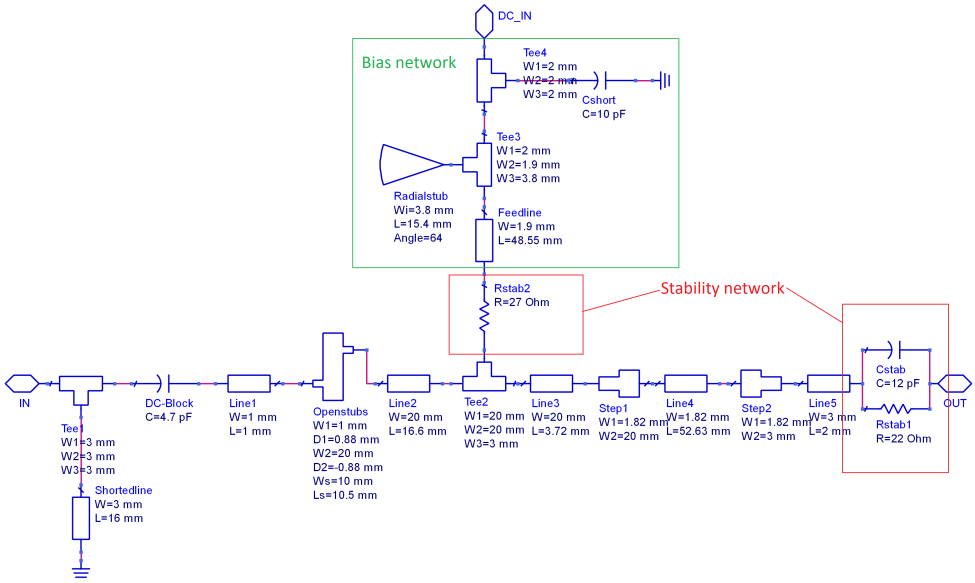

Figure 3.5: Simulation model of the input matching network

3.1.5 Design of the layout and manufacturing

After fine-tuning the input and output networks, the layout is designed. The layout has to fit inside an area of 100mm x 100mm. To meet this requirement, some transmission lines has to be bended, giving the final layout as shown in figure 3.6.

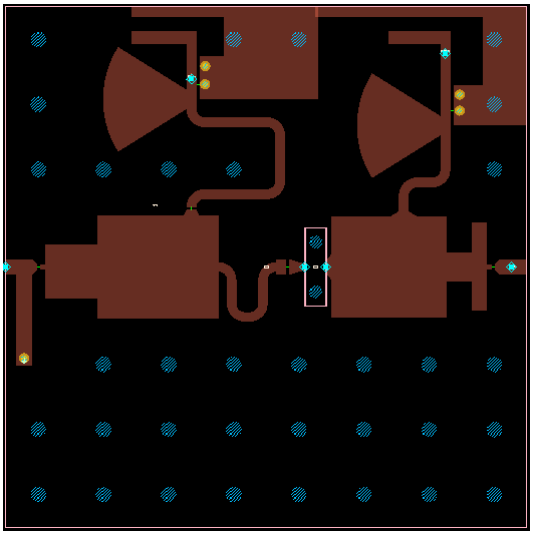

Figure 3.6: Layout

Next, the circuit is manufactured and the components are soldered on the printed circuit board. The finished product is shown in figure 3.7.

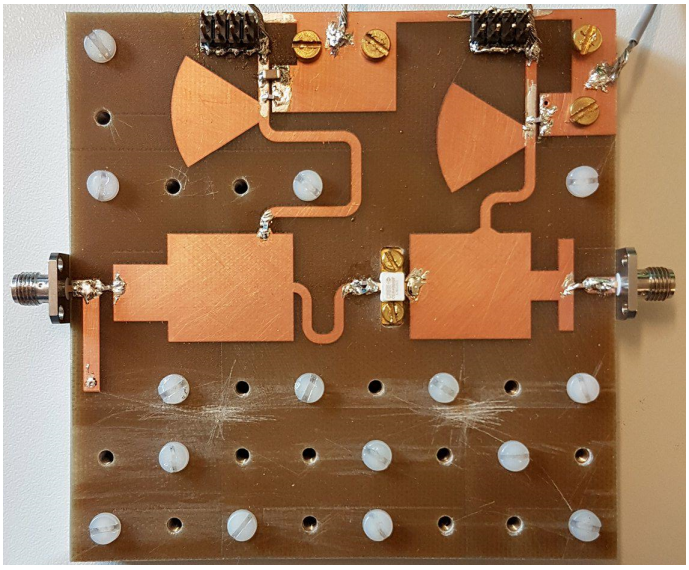

Figure 3.7: Manufactured circuit

3.1.6 Measurements

To validate the behavior and performance of the PA, measurements of the PA are executed in the lab. To characterize the S-parameters, small signal measurements are done according to the setup in figure 3.8. In order to characterize the efficiency, linearity and output power of the PA, 1-tone and 2-tone measurements are done according to the setup in figure 3.9.

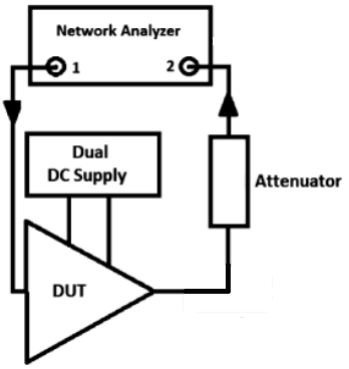

Figure 3.8: Small signal measurement setup

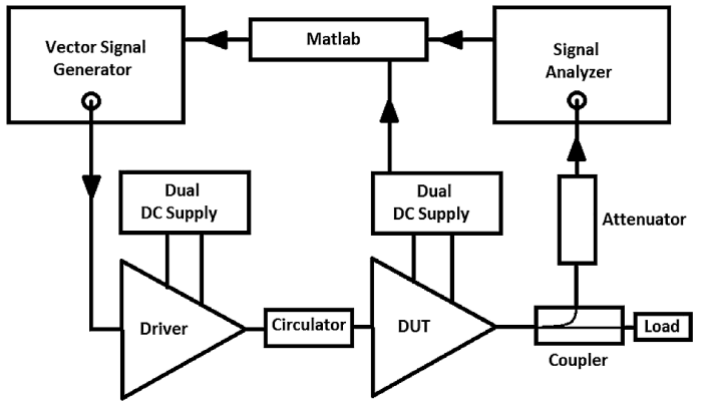

Figure 3.9: Large signal measurement setup

3.2 Design of Tracker circuits

In order to realize PET on the PA, tracker circuits for the supply voltages must be designed. The purpose of these circuits is to translate a normalized voltage value given from a signal generator to the actual supply voltage the PA requires. The tracker circuits should have as high bandwidth as possible to operate at the speeds needed for PET.

3.2.1 Gate tracker

The purpose of the gate tracker is to supply the gate of the PA with voltages varying from -3V to -2V. One proposed solution of such a tracker is shown in figure 3.10.

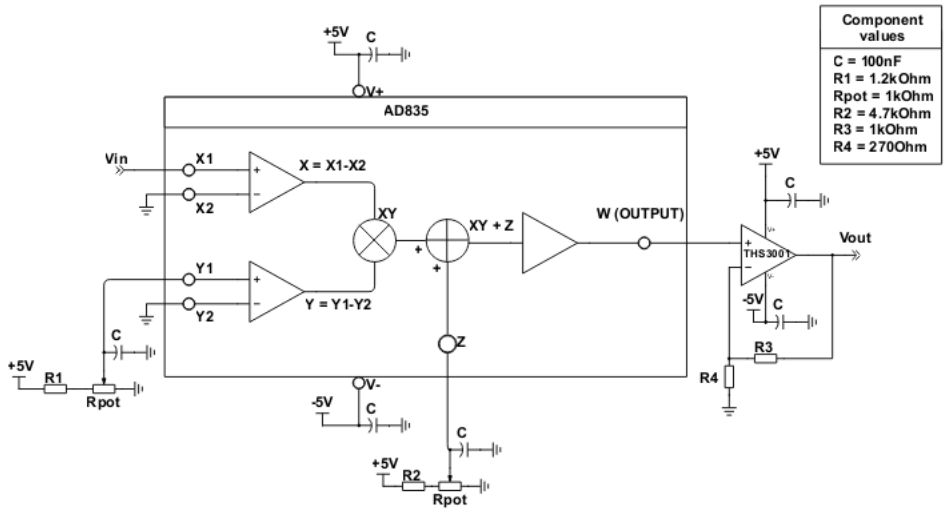

Figure 3.10: Gate tracker schematic

Here, AD835 is a 250 MHz, Voltage Output, 4-Quadrant Multiplier by Analog Devices [10]. In this schematic, the AD835 is used to control the gain and to add a DC offset. The voltages applied on the ports Y1 and Z can be controlled by varying the resistance of the potentiometers R_{pot}. By varying the voltage on port Y1 the gain can be controlled. Similarly, the DC offset is controlled by varying the voltage on port Z. THS3001 is a 420-MHz high-speed current-feedback amplifier by Texas Instruments [11]. It is used as a non-inverting amplifier to achieve the desired gate voltage.

3.2.2 Drain tracker

The purpose of the drain tracker is to supply the drain of the PA with voltages varying from 6V to 28V. A proposed solution, which is basically an extended version of the gate

tracker, is shown in figure 3.11.

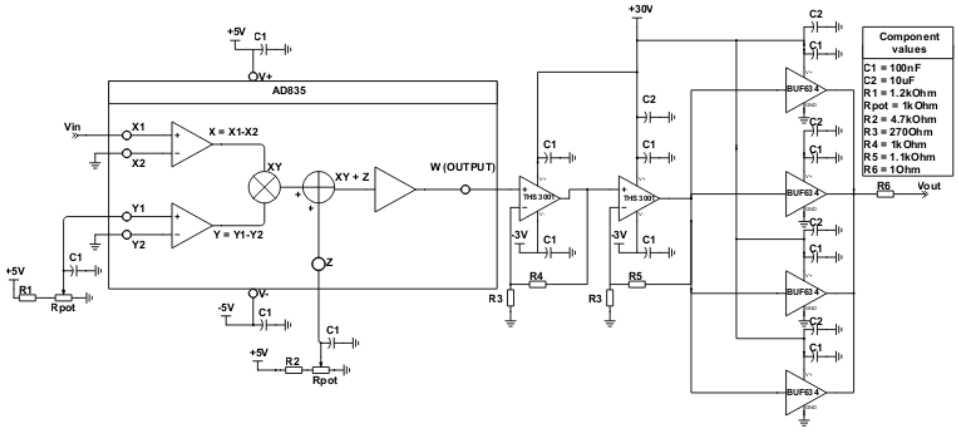

Figure 3.11: Drain tracker schematic

The operation of the drain tracker is similar to that of the gate tracker. The AD835 is used to control the gain and to add a DC offset. Two THS3001 is used as non-inverting amplifiers in series in order to achieve the desired gain. BUF634 is a 250-mA High-Speed Buffer by Texas Instruments [12]. 2 to 4 BUF634's are connected in parallel to get enough current delivered to the PA. In addition, a 1Ω resistor, R_6, is used as a current sensing resistor to be able to measure the current.

3.2.3 Measurements

To validate the behaviour of the tracker circuits, measurements are done. The parameters measured are magnitude response, phase response and output impedance. For the magnitude and phase response measurements, the setup shown in figure 3.12 is used.

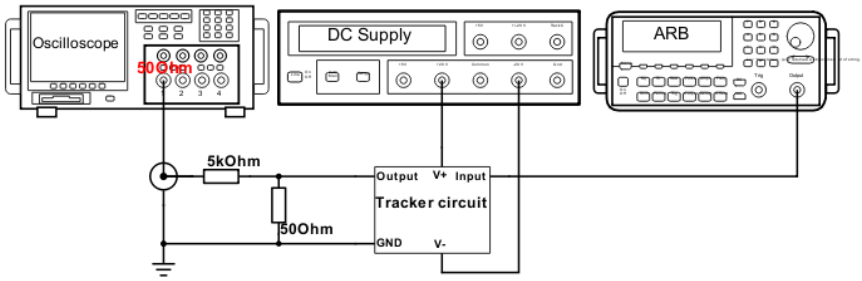

Figure 3.12: Measurement setup for magnitude and phase response measurements.

Here, the tracker circuit is connected directly to a 50Ω load. This is to eliminate reflections and distortion when measuring high frequencies. The 5kΩ resistor in series with the 50Ω load makes a voltage divider that operates as a 1:100 measurement probe. A 50mV peak to peak sinusoidal signal is applied on the input and the gain and phase shift is measured for different frequencies using an oscilloscope.

For the output impedance measurements, the setup shown in figure 3.13 is used.

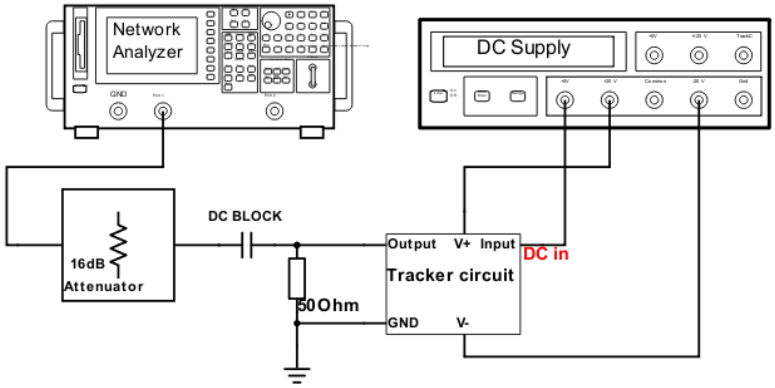

Figure 3.13: Measurement setup for output impedance measurements.

For these measurements, the tracker circuit is set to output an appropriate DC voltage value. The purpose of the DC block is to prevent DC input to the network analyzer. The 16dB attenuator is to protect the network analyzer, in case the tracker circuit oscillates. By analyzing S11 given from the network analyzer, the output impedance of the tracker circuit is found. During these measurements, averaging is used on the measured signal.

3.3 Design of tracker function

In order to achieve high performance using PET, good design of the tracker function is crucial. The purpose of the tracker function is to determine what level the supply voltage should have, given a specific input power level. The tracker function could be designed to achieve e.g. max PAE, flat phase or flat gain for all input power levels. To gain the data required to design the tracker functions, 1-tone measurements, as described in section 3.1.6, are conducted for a wide range of drain and gate voltages. Using this data, V_{supply} vs V_i functions are found for both gate and drain. These functions are found in MATLAB.

3.4 Tracking simulations

By using MATLAB, a real 16-QAM signal-sequence is applied to the measured PA data. Using MATLAB, the performance of a variety of tracker functions are simulated for this signal-sequence. First, the signal is applied to a nominal bias function, meaning constant gate and drain voltage, to be able to compare the tracking performance to the untracked performance. Thereafter, simulations of drain tracker functions are executed, keeping the gate voltage constant. Lastly, simulations of both gate and drain tracker functions are executed, utilizing PET on both the gate and drain voltage supply.

3.5 Tracking measurements

Tracking measurements are executed according to figure 3.14. The signal generator receives the QAM-signal and tracker functions from MATLAB. It then outputs the voltage trajectories for the given tracker functions to the tracker circuits in order to achieve dynamic supply voltages for the PA. The QAM-signal is output to a preamp that amplifies the signal to achieve sufficient input power at the PA. A power meter is used to get exact measurements of the input power at the PA. By analyzing the output of the PA with a signal analyzer, linearity and power measurements are calculated in MATLAB. The drain voltage and drain current, V_d and I_d, are measured with a mixed signal oscilloscope and are used in PAE calculations in MATLAB. To get accurate drain current measurements, a differential probe (N2792A from Keysight) is used.

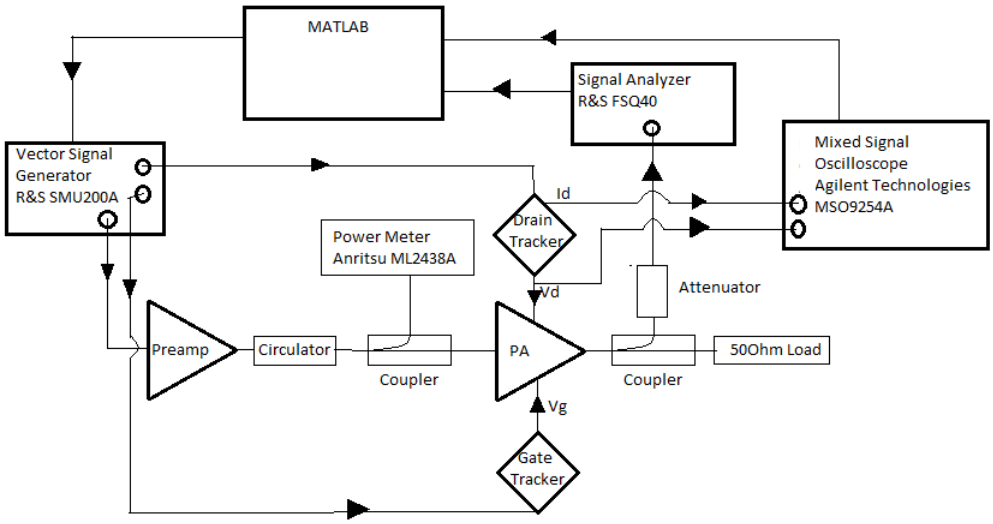

Figure 3.14: Measurement setup for Tracking measurements.

Chapter 4

Results

4.1 PA

Before executing PET, the PA is characterized at nominal bias (I_{DS} = 250mA, V_D = 28V). To evaluate the accuracy of the simulation model, it is of interest to compare the measured results with the simulated results. The following figures 4.1 to 4.5 show the PAs S21, PAE, Output power, Transducer power gain and Third order intermodulation products. These results are summarized in table 4.1.

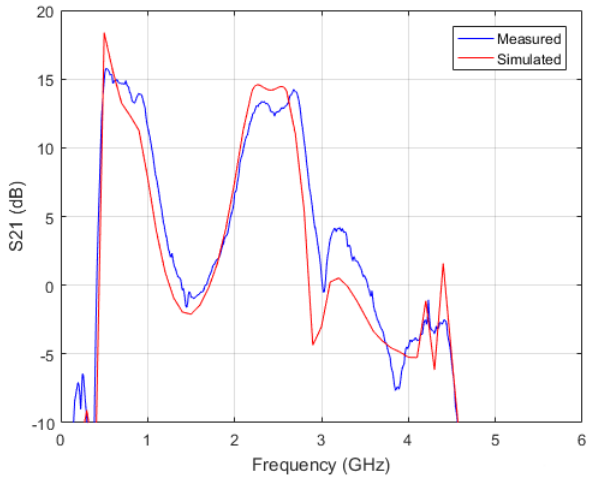

Figure 4.1: S21 at nominal bias, I_{DS} = 250mA, V_D = 28V

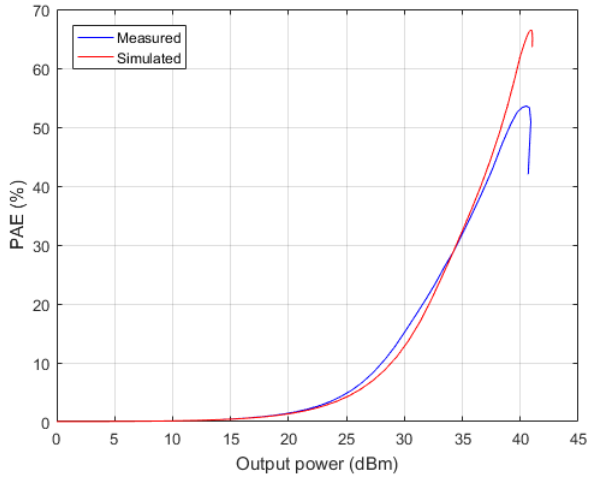

Figure 4.2: PAE vs output power at nominal bias, I_{DS} = 250mA, V_D = 28V

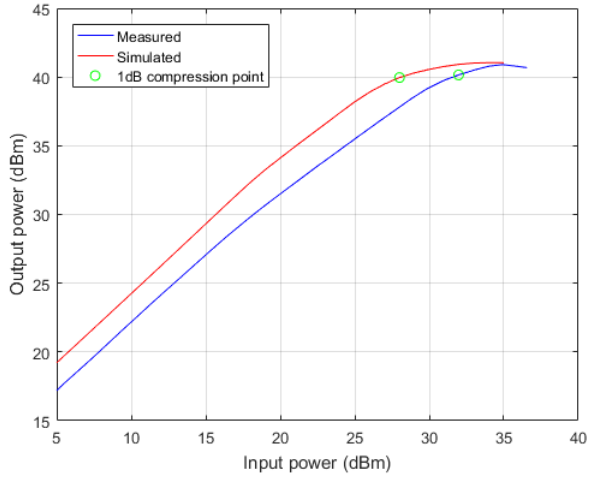

Figure 4.3: Output power vs input power at nominal bias, I_{DS} = 250mA, V_D = 28V

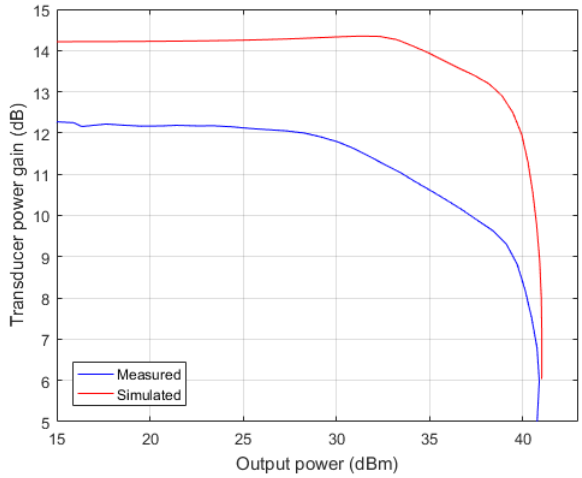

Figure 4.4: Transducer power gain vs output power at nominal bias, I_{DS} = 250mA, V_D = 28V

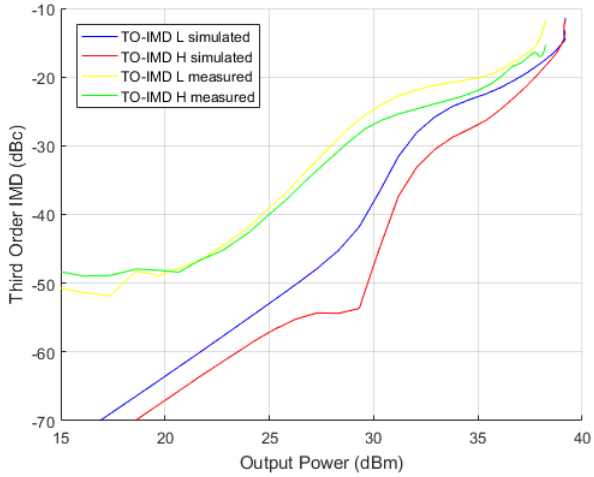

Figure 4.5: Third order IMD vs output power at nominal bias, I_{DS} = 250mA, V_D = 28V

	Simulations	Measurements
Frequency (f_0)	2.4GHz	2.4GHz
1dB Bandwidth (B)	400MHz	450MHz
Gain (G)	14.2dB	13.0dB
Output Power (P_o) @ max PAE	40.9dBm	40.5dBm
1dB compression point	40dBm	40.2dBm
Efficiency (max PAE)	66.5%	53.3%
3rd order IMD(P_o=37dBm)	-20dBc	-17dBc

Table 4.1: Overview of PA specifications at nominal bias, I_{DS} = 250mA, V_D = 28V

4.2 Tracker circuits

The magnitude and phase response, as well as the output impedance of the tracker circuits are measured as described in section 3.2.3. All measurements are done with a 50Ω load. Figures 4.6, 4.7 and 4.8 show the magnitude response, phase response, and output impedance of the drain tracker respectively. Figures 4.9, 4.10 and 4.11 show respectively the magnitude response, phase response, and output impedance of the gate tracker. The results are summarized in tables 4.2 and 4.3.

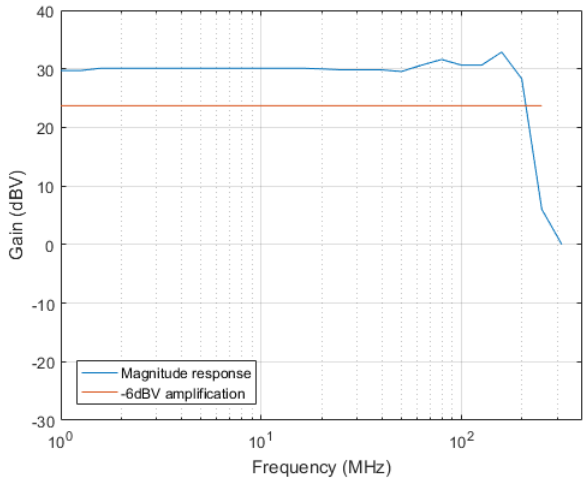

Figure 4.6: Magnitude response for the drain tracker circuit

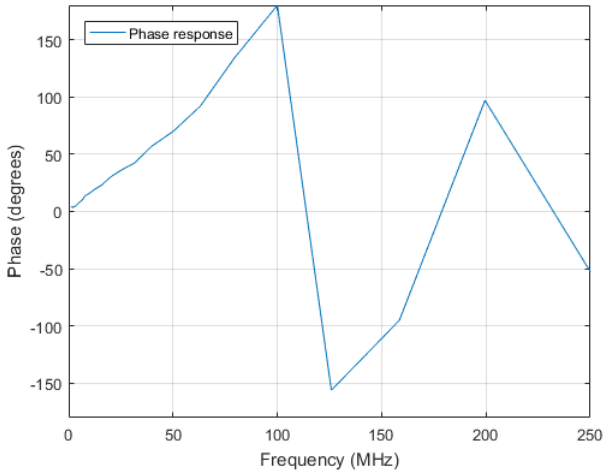

Figure 4.7: Phase response for the drain tracker circuit

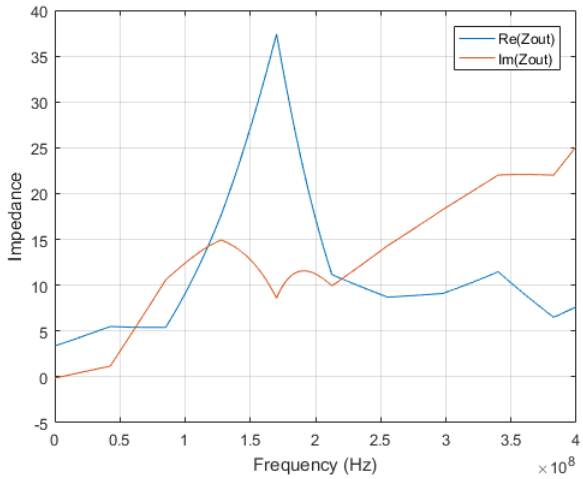

Figure 4.8: Z_{Out} for the drain tracker circuit

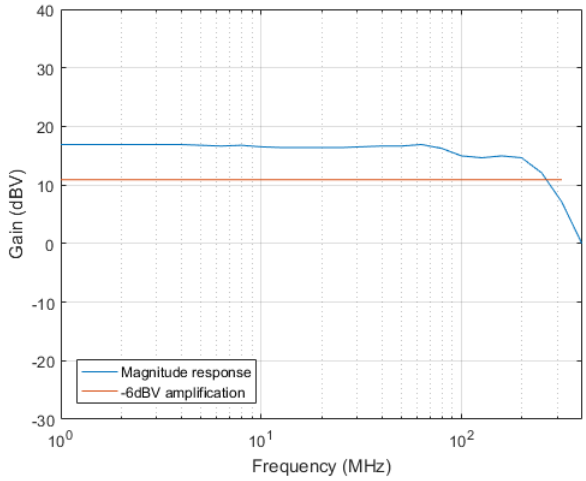

Figure 4.9: Magnitude response for the gate tracker circuit

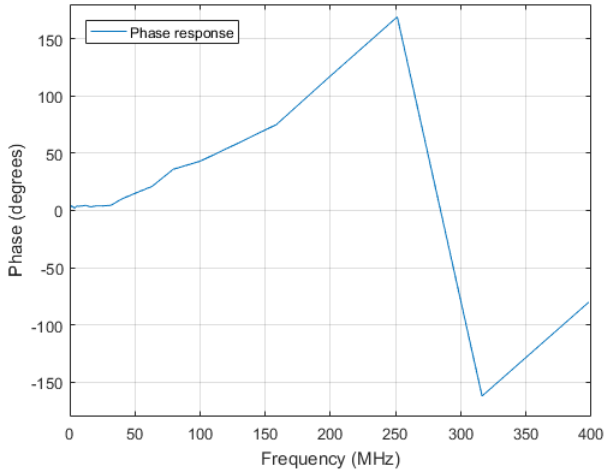

Figure 4.10: Phase response for the gate tracker circuit

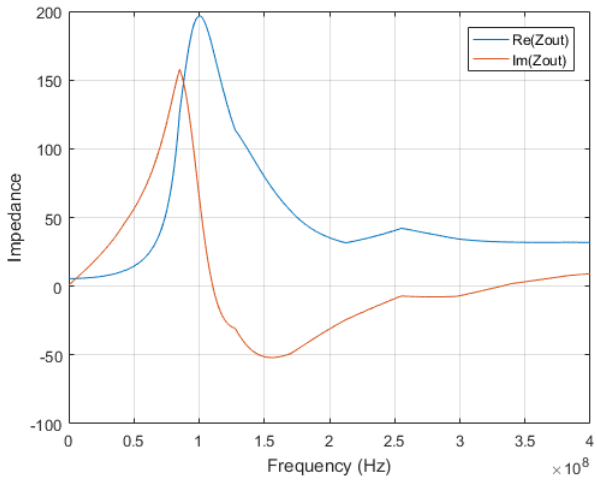

Figure 4.11: Z_{Out} for the gate tracker circuit

Table 4.2: Measured characteristics of drain tracker circuit

Measured gain at 50MHz	31.62
Achievable gain at 50MHz	0-50
-6dB gain Bandwidth	200MHz
Frequency where 180 degree total phase shift occur	100MHz
Output impedance at 50MHz	(5.5 + j2.8)Ω

Table 4.3: Measured characteristics of gate tracker circuit

Measured gain at 50MHz	7
Achievable gain at 50MHz	0-10
-6dB gain Bandwidth	250MHz
Frequency where 180 degree total phase shift occur	250MHz
Output impedance at 50MHz	(14.6 + j56.2)Ω

Here, achievable gain indicates the gain that can be achieved by controlling the gain by using the AD835 as described in section 3.2.1. It should also be noted that the phase response in figures 4.7 and 4.10 includes both the linear phase shift due to delay in the circuits and the frequency dependant phase shift.

4.3 Tracker function

In order to obtain the data required to make the tracker function, the PA is characterized for a wide range of drain voltages and drain currents. More specifically, for drain voltages from 6V to 28V and drain currents from 10mA to 300mA. Since it is of most interest to design the tracker function to either achieve max PAE or flat gain, PAE and transducer power gain are plotted in figures 4.12 to 4.25 for a wide range of drain voltages and drain currents.

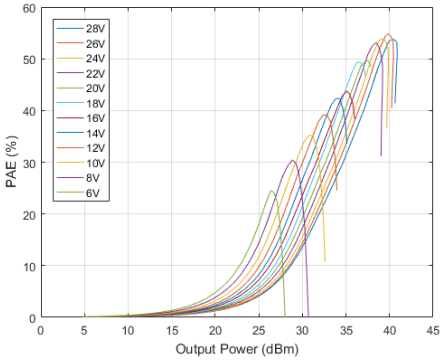

Figure 4.12: PAE with varying V_D for I_{DS} = 300mA

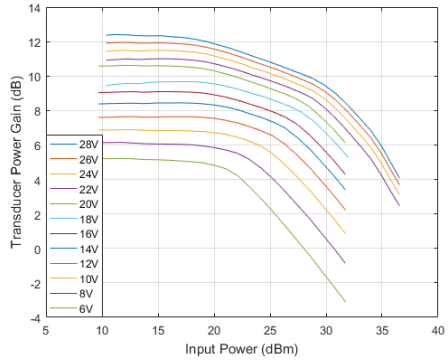

Figure 4.13: Transducer power gain with varying V_D for I_{DS} = 300mA

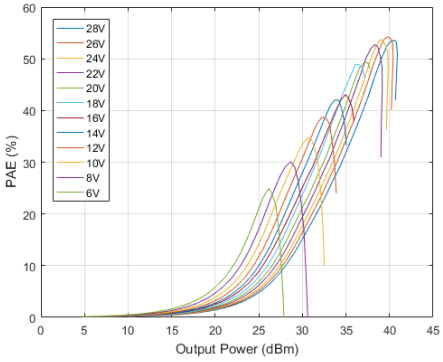

Figure 4.14: PAE with varying V_D for I_{DS} = 250mA

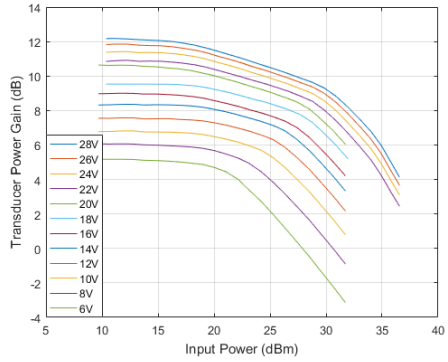

Figure 4.15: Transducer power gain with varying V_D for I_{DS} = 250mA

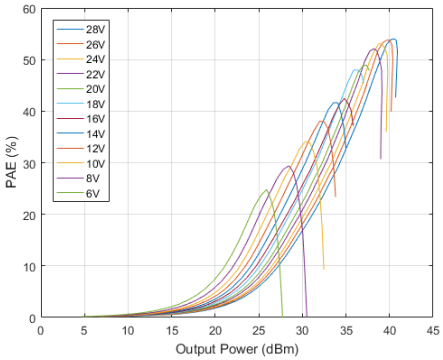

Figure 4.16: PAE with varying V_D for I_{DS} = 200mA

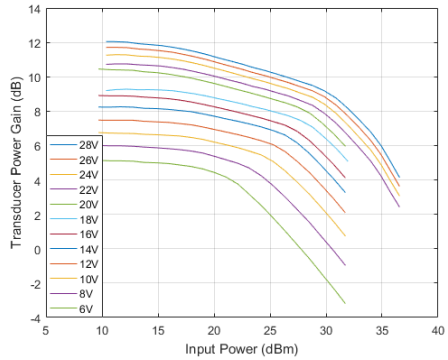

Figure 4.17: Transducer power gain with varying V_D for I_{DS} = 200mA

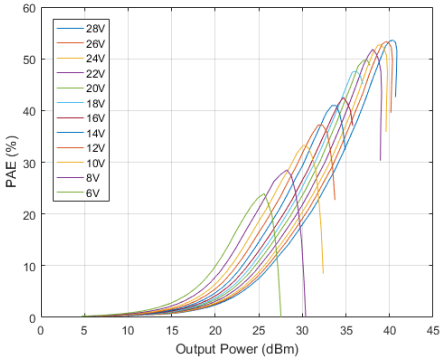

Figure 4.18: PAE with varying V_D for I_{DS} = 150mA

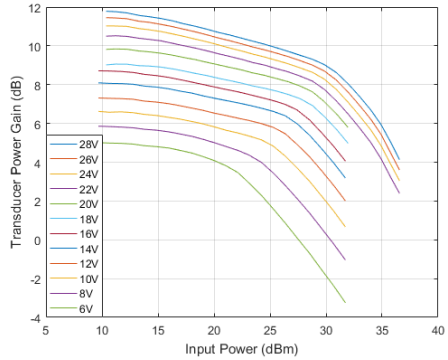

Figure 4.19: Transducer power gain with varying V_D for I_{DS} = 150mA

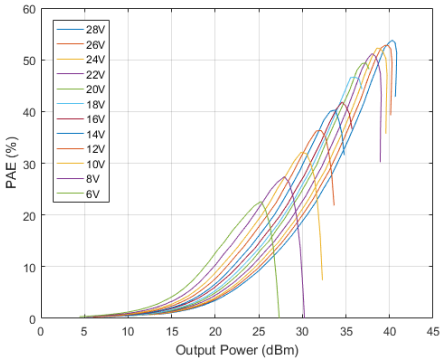

Figure 4.20: PAE with varying V_D for I_{DS} = 100mA

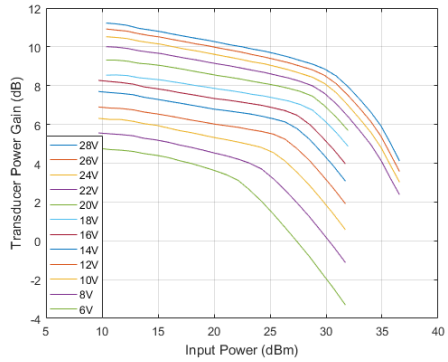

Figure 4.21: Transducer power gain with varying V_D for I_{DS} = 100mA

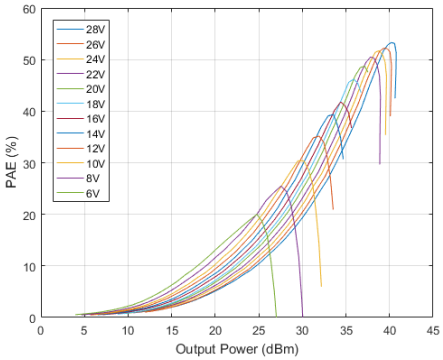

Figure 4.22: PAE with varying V_D for I_{DS} = 50mA

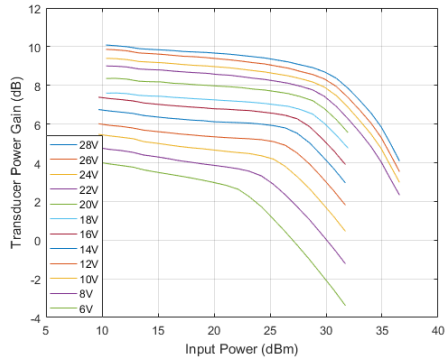

Figure 4.23: Transducer power gain with varying V_D for I_{DS} = 50mA

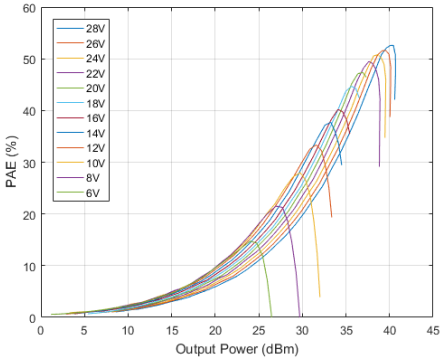

Figure 4.24: PAE with varying V_D for I_{DS} = 10mA

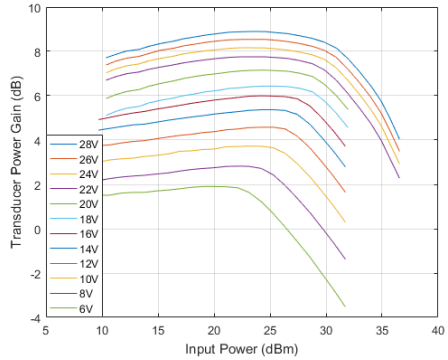

Figure 4.25: Transducer power gain with varying V_D for I_{DS} = 10mA

By analyzing these data, different supply voltage trajectories, also called tracker functions, are generated in MATLAB. Drain voltage supply trajectories yielding max PAE using ET, max PAE using PET, flat gain and flat gain using PET are presented in figure 4.26. The trajectory for a constant supply is also included in the figure. For all these cases a constant gate supply voltage V_g = -2.43V is used.

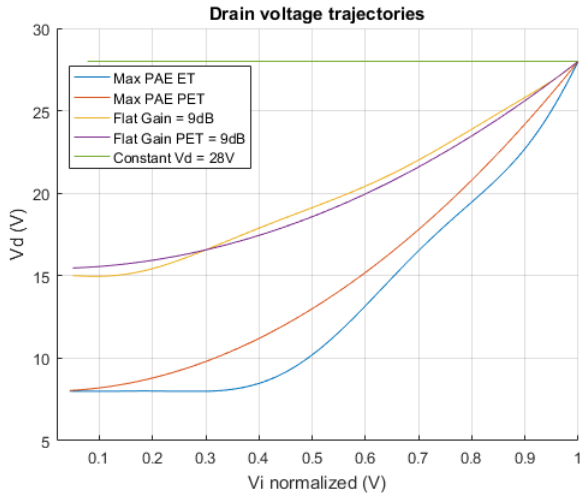

Figure 4.26: Drain tracker functions, V_g = -2.43V

The former trajectories utilize a constant gate supply voltage. By modelling both the gate supply and the drain supply voltage with PET trajectories, higher performance can be reached. In this case, this is done and both voltage trajectories are optimized to achieve max PAE whilst maximizing the linearity. Figures 4.27 and 4.28 show the trajectories of respectively the drain voltage trajectory and the gate voltage trajectory. The drain voltage trajectory is modelled as a 1st order PET function given by equation 4.1. The gate voltage trajectory is modelled as a 4th order PET function given by equation 4.2. Both are normalized to a maximum V_i of 1V.

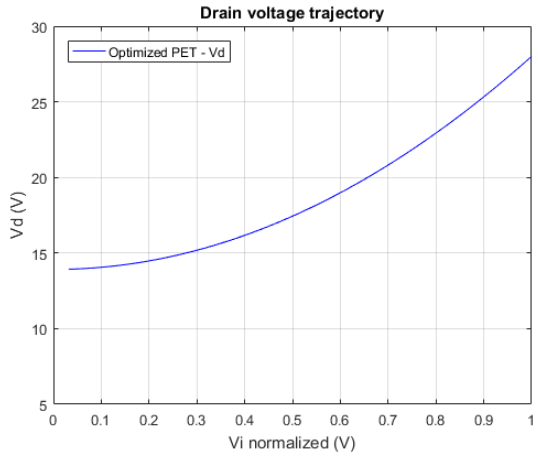

Figure 4.27: Optimized PET drain tracker function

$$v_d(t) = 13.9 + 14.08 \cdot v_i^2 \tag{4.1}$$

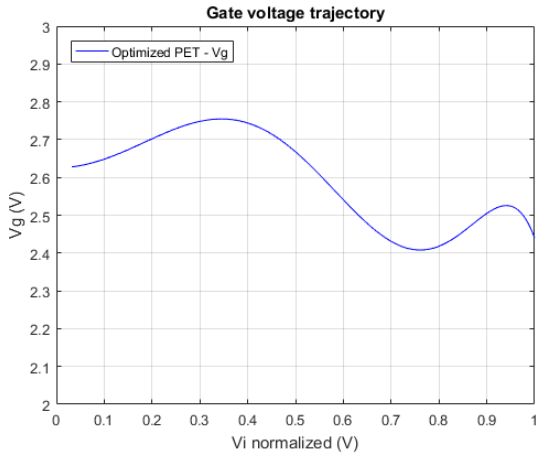

Figure 4.28: Optimized PET gate tracker function

$$v_g(t) = 2.63 + 2.44 \cdot v_i^2 - 13.71 \cdot v_i^4 + 21.09 \cdot v_i^6 - 10 \cdot v_i^8 \tag{4.2}$$

4.4 Tracking simulations

Tracking simulations are executed by sending a 4MHz 16QAM signal sequence through the trajectories given by figures 4.26, 4.27 and 4.28. For that specific sequence; PAE, gain, ACPR, EVM and STDR are calculated for the different supply voltage trajectories. The spectrum of V_d is also given and is shown in figure 4.29. Figures 4.30 and 4.31 are plots of respectively the PAE trajectories and gain trajectories. All the results are summarized in table 4.4. Here, the bandwidth is defined as the frequency where the signal is -60dBV relative to the spectral level and P_o is the average output power.

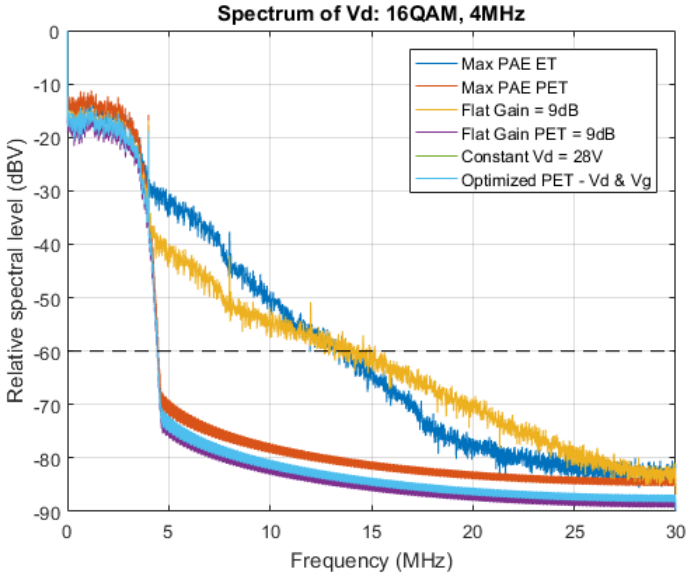

Figure 4.29: Spectrum for different trajectories, Constant V_d = 28V only exists at 0Hz

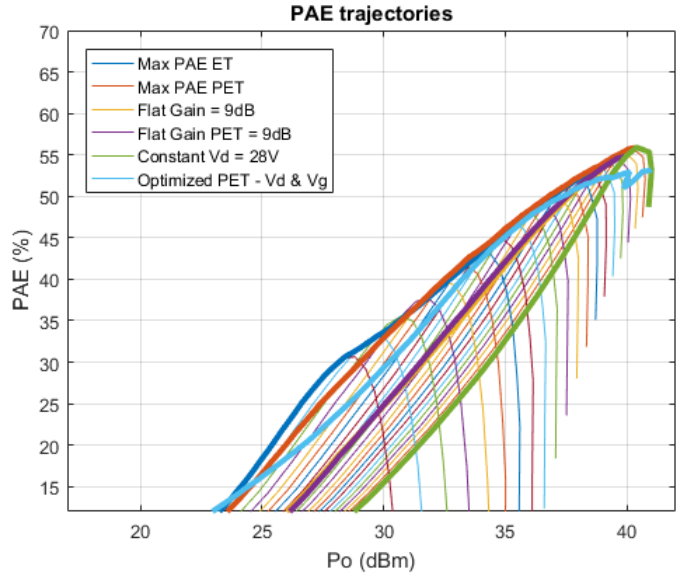

Figure 4.30: PAE for different trajectories

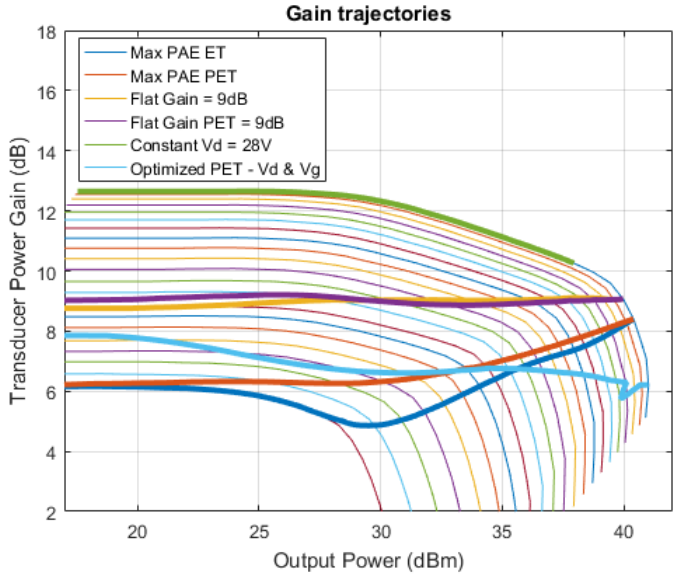

Figure 4.31: Gain for different trajectories

Simulation	Po(dBm)	Gain(dB)	PAE(%)	EVM(%)	ACPR(dBc) Lower, Upper	STDR(dB)	BW(MHz)
Max PAE ET	31	5.8	36.4	8.3	-29.7, -29.5	20.2	14
Max PAE PET	32.1	6.8	38.7	4.7	-33.8, -33.6	24.1	4.4
Flat Gain = 9dB	33.2	9	35.1	3.5	-37.2, -37	27.8	14
Flat Gain PET = 9dB	33.1	8.9	34.9	3.5	-37.2, -37	27.8	4.4
Constant V_d = 28V	32.4	11.5	22.4	4.5	-34.5, -34.3	25.1	-
Optimized PET - V_d & V_g	34.7	6.7	44.3	1	-43.5, -43.3	34.8	4.4

Table 4.4: Summary of results from tracking simulations of a 4MHz 16QAM signal

4.5 Tracking measurements

Measurements are executed as described in section 3.5. Tables 4.5, 4.6 and 4.7 display the results from tracking measurements of a 1MHz 16QAM signal, 5MHz 16QAM signal and 10MHz 16QAM signal, respectively. For more results, see the appendix.

Measurement	Po(dBm)	PAE(%)	EVM(%)	ACPR(dBc) Lower, Upper	STDR(dB)
Constant V_d and V_g, nominal bias	31.7	19	4	-34.5, -35.2	26
Constant V_g, ideal ET on drain	31.3	32.4	6.5	-30.3, -30.2	21.3
Constant V_g, max PAE PET on drain	30.8	30.3	4	-34.3, -34	24.7
Constant V_g, optimal PET on drain	32.2	28.4	1.6	-43.6, -42.6	33.7

Table 4.5: Summary of results from tracking measurements of a 1MHz 16QAM signal

Measurement	Po(dBm)	PAE(%)	EVM(%)	ACPR(dBc) Lower, Upper	STDR(dB)
Constant V_d and V_g, nominal bias	31.8	19.2	5	-32.8, -34.4	24.6
Constant V_g, ideal ET on drain	31.3	31.7	7.4	-30.9, -30.8	21
Constant V_g, max PAE PET on drain	30.9	29.4	4.7	-35.6, -34.1	23.9
Constant V_g, optimal PET on drain	32.4	28.5	3.2	-40.8, -45	28.2

Table 4.6: Summary of results from tracking measurements of a 5MHz 16QAM signal

Measurement	Po(dBm)	PAE(%)	EVM(%)	ACPR(dBc) Lower, Upper	STDR(dB)
Constant V_d and V_g, nominal bias	31.5	18.3	7.2	-30.7, -32.3	21.2
Constant V_g, ideal ET on drain	31.1	29.9	9.4	-31.4, -31.3	19.7
Constant V_g, max PAE PET on drain	30.8	27.7	4.3	-36.4, -33.8	25.1
Constant V_g, optimal PET on drain	32.1	26.7	3.8	-43.2, -38.3	26.7

Table 4.7: Summary of results from tracking measurements of a 10MHz 16QAM signal

Chapter 5

Analysis

5.1 PA

As seen in figure 4.1, the measured results of S21 follow the same trend as the simulated results. The bandwidth is actually slightly higher at the expense of the gain, which is around 1dB lower. The PA is as mentioned a revised version of the PA designed in [2]. In that design, problems according stability and bandwidth are discovered. This is compensated for in this revised design at the cost of lower gain.

From the 1-tone measurements it can be seen that the PAE is lower in the measurements than in the simulations, which is expected. The PAE being 53.3% at 2.4GHz, is around 5% lower than the design in [2]. Since the gain in the revised design is lower, it follows from equation 2.2 that the PAE also will be reduced, as a lower gain will result in a lower PAE. It is also seen that the amplifier is capable of delivering an output power over 40dBm, having an output power of 40.5dBm at peak PAE.

From the two-tone measurements it is seen in figure 4.5 that the simulated third order IMD is lower than the measured, which is expected since a produced non-ideal device usually has poorer performance than a device in simulations, even when simulating with non-ideal components. What is worth noting from figure 4.5 is that for both the simulated and measured third order IMD, the high and low sides deviate. This is an indication that there could be some memory effects in the amplifier, which means that the gain of the PA may variate due to parameters such as the frequency of the signal, the envelope of the signal and the temperature.

5.2 Tracker circuits

5.2.1 Drain tracker

As seen in figure 4.6 and table 4.2, the gain bandwidth of the drain tracker is 200MHz. Here the bandwidth is defined as the point where the voltage gain is halved, which is the same as -6dBV. Figure 4.7 shows that the phase response is the limiting factor for the bandwidth. At 30MHz there is a phase shift of 45°, and when operating with bandwidths higher than 30MHz, this should be compensated for in order to achieve good performance. This compensation could be done by either digital predistortion of the signal or by adding delay to the signal. If this is implemented, the drain tracker should be able to operate sufficiently at frequencies up to 200MHz.

The purpose of the drain tracker is to operate as a dynamic voltage source. An ideal voltage source has a very low non-zero impedance, typically below 1Ω. It is therefore desired that the impedance of the tracker is as low as possible. The measurements in figure 4.8 show that the output impedance has a low real value up to around 100MHz. The real impedance has a peak at 170MHz and decreases as the frequency increases. It is seen in figure 4.8 that the output impedance contains a positive imaginary value that increases with frequency. This indicates an inductance and could be attributed to the wirelengths, which will be more inductive at higher frequencies. The big variations in output impedance could be caused by inaccurate measurement techniques. BNC coax cables are used in the measurements where it is seen that the measured S11 changes when the position of the cable is altered. The cables should therefore have the exact same position during the calibration and measurements. Some alteration of the cable position may have occured and caused some inaccurate measurements.

5.2.2 Gate tracker

For the gate tracker, the gain bandwidth is 250MHz. This is seen in figure 4.9 and table 4.3. From figure 4.10 it is seen that a phase shift of 45° occurs at 100MHz. When comparing the drain tracker and gate tracker it is seen that the gate tracker is operable at higher frequencies at the cost of gain.

Compared to the drain tracker, the output impedance of the gate tracker is higher. Looking at figure 4.11 shows a great variation in output impedance as a function of frequency. The imaginary part also switches between being inductive and capacitive. This variation in output impedance is unwanted and can be reduced by adding a buffer circuit, e.g. the BUF634 used in the drain tracker, at the output.

5.3 Tracker function

The different drain voltage functions are shown in figures 4.26 and 4.27. Figure 4.28 shows the optimized gate voltage function. It is seen that Max PAE ET and PET functions utilize a high range of drain voltages, going from 8V to 28V. The Max PAE ET curve is a

detroffed function, whereas an ideal ET curve will clip the signal at 8V. This will require a higher bandwidth and the detroffed signal is therefore preferred. It is worth noting that the PET curves have a natural detroff caused by the nature of the second order function. When analyzing the curves for flat gain and the optimized PET function it is seen that these curves utilize a lower range of drain voltages when compared to the max PAE curves. For the optimized drain and gate voltage functions, a 1st order PET function is used for the drain voltage function and a 4th order PET function is used for the gate voltage function. The 1st order PET function is used on the drain to minimize the required bandwidth for the drain tracker. As seen in section 4.2, the gate tracker has a higher bandwidth than the drain tracker and can therefore meet the bandwidth requirements of the 4th order PET function. Different results can be gained by trying other orders of the PET function. As seen in [3], a higher order function will result in higher efficiency and bandwidth requirements, and lower linearity. In this paper, only one combination of gate and drain functions are presented. For future works, other combinations of the orders of the tracker functions may be evaluated to achieve better performance.

5.4 Tracking simulations

Tracking simulations are done for the tracker functions; max PAE ET, max PAE PET, flat gain = 9dB, flat gain PET = 9dB, constant V_d = 28V and optimized PET - Vd Vg. These are seen in figures 4.26, 4.27 and 4.28. These functions are chosen because they are easy to implement with the current measurements. Phase measurements are not done and therefore, no tracker function giving flat phase is implemented. To keep it as simple as possible, only one variation of the QAM-signal was evaluated for the simulations. Figure 4.29 demonstrates one of the greatest benefits of the PET technique, the bandwidth requirements. The PET technique requires around 3 times lower signal bandwidth than the ET and flat gain techniques. This means that the tracker circuits require lower bandwidth in order to use the PET technique compared to the other techniques.

A summary of the tracking simulation results are seen in table 4.4. To be able to get a good comparison of the simulations, the average output power should be around the same level. It is seen that there are some variations in the output power, but keeping in mind that a higher output power results in higher PAE and lower linearity and vice versa, the trends are seen. Comparing the max PAE ET PET techniques shows that the PAE is almost the same while the linearity by using the PET technique is much better. The flat gain techniques have lower PAE, but even better linearity whilst having flat gain. By keeping the drain voltage constant, a higher average gain is achieved at the cost of lower PAE. Lastly, it is seen that using an optimized PET function for both the gate and drain voltages yields a significant improvement in the linearity of the PA, while keeping the PAE high as well. Compared to the constant voltage case, it is seen from these results that using PET on the drain voltage will increase the efficiency while keeping the linearity the same. By using PET on the gate voltage, the linearity is increased by a significant amount; a STDR value of almost 10dB.

5.5 Tracking measurements

Originally, the driver PA used in the 1 tone measurements was going to be used for the tracker measurements. During other measurements at the lab, this PA stopped working. Therefore, another PA is used as a preamp, giving 12dB gain compared to the 22dB gain of the driver PA. During measurements it is discovered that the signal generator has a hardware limitation that allows it to output a maximum of 13dB output power for a QAM-modulated signal. This means that there is a limitation in average input power for the PA at around 25dB. To be able to get more significant results, a higher average input power is required. Still, the results in tables 4.5, 4.6 and 4.7 show some of the same trends as the simulations: The max PAE PET function has around the same linearity as the constant voltage while having a PAE at the same level as the ideal ET. When analyzing the results from the optimal PET function it is seen that the linearity is significantly improved while having almost the same PAE as the ideal ET. As in the simulations, the average output power should be around the same level to be able to get a good comparison of the measurements. Here, as in the simulations, it is seen that there are some variations in the output power, but the trends are still seen.

It should be noted that these tracker measurements are conducted with a constant gate voltage while altering the drain voltage function. Measurements utilizing both a gate and drain voltage function are also done. During measurements it is seen that there are some kind of instabilities that are corrupting the test results and the results are therefore rejected. There may be many reasons for these instabilities. When applying the gate tracker to the PA, a 10μF shorting capacitor in the gate bias network is removed. This makes the PA less stable at lower frequencies and a low frequency oscillation may occur which will corrupt the signal. Another possible reason is the high output impedance of the gate tracker, which may have excited some oscillations when applied to the PA. When probing the circuit, it is seen that there is a low amplitude oscillation on the drain and gate voltages. These may be induced by the probe, or they could be the reason for the corrupted results. Coupling between the cables and wires may also be a reason for the instabilities.

Chapter 6

Conclusion

In this thesis a design of a class AB power amplifier is presented. As shown in table 4.1, the center frequency is 2.4GHz with a 1dB bandwidth of 450MHz. The gain at center frequency is 13.0dB and it delivers 40.5dBm output power at a max PAE of 53.3%. The 3rd order IMD is shown to be -17dBc at an output power of 37dBm.

The designs of tracker circuits for gate and drain are also presented. From table 4.2 it is seen that the drain tracker has a controllable gain of 0 to 50, while having a -6dB gain bandwidth of 200MHz. The frequency where the first 180° phase shift occurs is 100MHz and the output impedance at 50MHz is (5.5 + j2.8)Ω. From table 4.3 it is seen that the gate tracker has a controllable gain of 0 to 10, while having a -6dB gain bandwidth of 250MHz. The frequency where the first 180° phase shift occurs is 250MHz and the output impedance at 50MHz is (14.6 + j56.2)Ω.

Optimal PET tracking functions are found for both drain and gate. The optimal drain function is a 1st order PET given by equation 4.1: $v_d(t) = 13.9 + 14.08 \cdot v_i^2$. The optimal gate function is a 4th order PET given by equation 4.2: $v_g(t) = 2.63 + 2.44 \cdot v_i^2 - 13.71 \cdot v_i^4 + 21.09 \cdot v_i^6 - 10 \cdot v_i^8$

These results and designs are used to demonstrate the PET technique through simulations and measurements. It is seen that the PET technique has a big benefit over the ET technique in terms of required bandwidth and linearity, while achieving almost the same efficiency. The PET technique is also a simpler technique than ET and requires less complex circuitry because of the lower bandwidth requirements.

To conclude: In this thesis it is shown that PET is a promising technique in terms of efficiency, linearity, bandwidth requirements and complexity. These are important parameters in the technology today and emphasize the importance of further research of the PET technology. And maybe one day, e.g. in the future emergence of the 5G technology, PET could prove to be a valuable technique.

Chapter 7

Future works

For future works, a new revised PA may be designed, in order to achieve better efficiency and gain. Revised versions of the tracker circuit should also be designed. The tracker circuits in itself are not very efficient and to benefit from the efficiency increase of the PET technique, more efficient tracker circuits should be designed. This will increase the overall efficiency, and not just the PA efficiency. For the gate tracker specifically, a buffer should be added on the output to reduce the output impedance.

In this paper, only one combination of gate and drain functions are presented. For future works, other combinations of the orders of the tracker functions may be evaluated to achieve better performance. Measurements of the phase could also be conducted in order to achieve tracker functions optimized to give flat phase. Future works could also evaluate the use of predistortion techniques at both the RF-signal and the tracker signals to achieve even better linearity.

The only signals used to evaluate the tracking performance in this thesis are QAM signals. A natural extension of this thesis is to execute tracking on other modulated signals such as LTE, OFDM and PSK techniques.

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Appendix

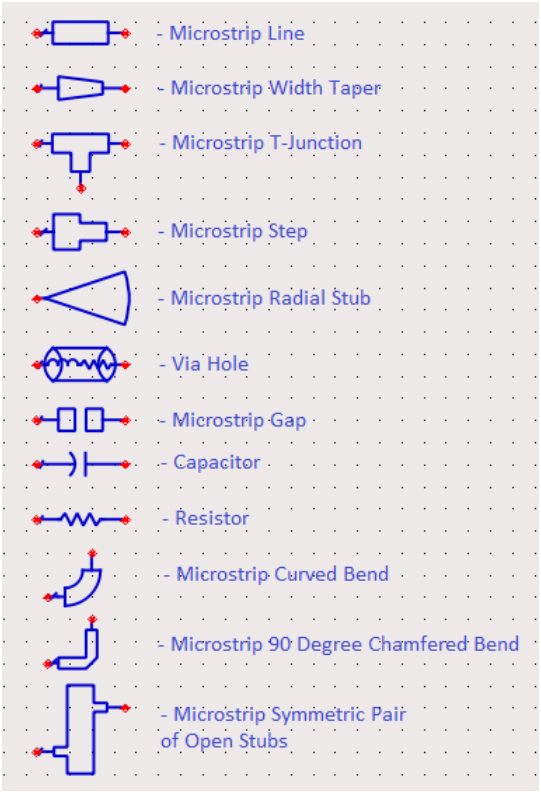

Figure 7.1: Circuit element legend

Measurement	Po(dBm)	PAE(%)	EVM(%)	ACPR(dBc) Lower, Upper	STDR(dB)
Constant Vd and Vg, nominal bias	31.7	19	0.8	-35.3, -35.8	28.1
Constant Vg, ideal ET on drain	31.2	30.5	1.2	-31.3, -30.9	23.1
Constant Vg, max PAE PET on drain	30.9	29.6	0.9	-36.2, -36	27.4
Constant Vg, optimal PET on drain	32.2	28	0.7	-43.9, -44.7	36

Table 7.1: Summary of results from tracking measurements of a 1MHz 4QAM signal

Measurement	Po(dBm)	PAE(%)	EVM(%)	ACPR(dBc) Lower, Upper	STDR(dB)
Constant Vd and Vg, nominal bias	31.8	19.3	2.8	-33.5, -35.1	26.5
Constant Vg, ideal ET on drain	31.2	31	2.5	-31.8, -31.6	23.2
Constant Vg, max PAE PET on drain	30.8	29	1.3	-37.8, -36.1	28.2
Constant Vg, optimal PET on drain	32.3	28.3	1.9	-41.9, -46.4	32.5

Table 7.2: Summary of results from tracking measurements of a 5MHz 4QAM signal

Measurement	Po(dBm)	PAE(%)	EVM(%)	ACPR(dBc) Lower, Upper	STDR(dB)
Constant Vd and Vg, nominal bias	31.6	18.4	6.1	-31.7, -33.1	20.6
Constant Vg, ideal ET on drain	31.0	28.8	5.6	-32.2, -31.9	22.4
Constant Vg, optimal PET on drain	32.2	26.8	5.4	-35.2, -37.8	23.6

Table 7.3: Summary of results from tracking measurements of a 10MHz 4QAM signal