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Developement of a digitally controlled low power single phase inverter for grid connected solar panel

Raphael Marguet

Master of Science in Electric Power Engineering
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Supervisor: Lars Einar Norum, ELKRAFT

Norwegian University of Science and Technology
Department of Electric Power Engineering

Problem Description

The work consists in developing a power conversion unit for solar panel connected to the grid. This unit will be a single phase inverter in the low power range (24/48 V - 100/200 W), with digital control and without a DC-DC stage. The final system should be suitable for laboratory work.

This master project will be complete, starting with a detailed specification of the project and finishing with an experimental validation.

Assignment given: 28. August 2009
Supervisor: Lars Einar Norum, ELKRAFT

Preface

This master thesis is a part of the Master program in Technology at the Norwegian University of Science and Technology in Trondheim, Norway. It has been written under the supervision of Professor Lars E. Norum at the Department of Electrical Power Engineering.

In this project a photovoltaic (PV) system power conversion stage is studied and developed. The system consist of a single digitally controlled DC-AC stage meant to connect a solar energy source (PV modules) to the grid. As the system is developed for future laboratory work it will be single-phased and operate at low power for security reasons and ease of work. This report will first give general notions in the domain of PV systems before covering the hardware and software design and the testing of the entire system. It is mainly meant to be a detailed documentation of the project in order that further work and improvements can be brought to it.

I would like to give special thanks to my head supervisor Lars Norum who has enabled me to work on a very interesting subject, and for his support and advices throughout the project. I would also like to thank Fritz Schimpf, my second supervisor who kindly shared his experience and knowledge with me, for his great help and support. Also thanks to Marie Busuttil who supported me throughout the entire master, and Silje Simonsen. I improved my knowledge on many levels throughout this master thesis, as well theoretically than practically which was my main motivation along with its application to "Solar Energy", an energy which has a great future in my modest opinion.

Raphaël Marguet
Trondheim, January 28st 2010

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Introduction

In the last few years the interest in solar energy has strongly increased. The democratization of photovoltaic solar park in the industry of energy production as well as private photovoltaic solar panels has brought many new problematics. From production park in the range of mega Watts to small remote power supplies, this energy source needs a special power conversion stage: DC to AC. Solar power, among with wind power and other renewable energy source, has also brought decentralized generation: energy production from many small energy sources. Indeed many low power solar systems now have a grid connection.

The goal of this project is to develop a single-phase low power inverter designed for connecting a solar energy source such as PV modules, to the electric grid. The inverter will be developed with digital control.

The system should be suitable for a laboratory setup which can be used for demonstration, learning or testing its different aspects (digital control, filtering of the inverter's output ...). The system will therefore show a simple structure but nonetheless cope with different topics such as: DC power input, DC to AC conversion, filtering, grid connection and digital control. The entire system will be studied from scratch. The project will thus present many different aspects, from theoretical operation to electronic board conception and will be completed with series of validation tests on the final system.

Chapter 1

The Background of Photovoltaic Systems

1.1 What is a PV System?

A photovoltaic system (often called PV system) is based on a arrangement of photovoltaic cells and power electronics components (often called Balance of Systems) in order to produce electricity from solar energy.

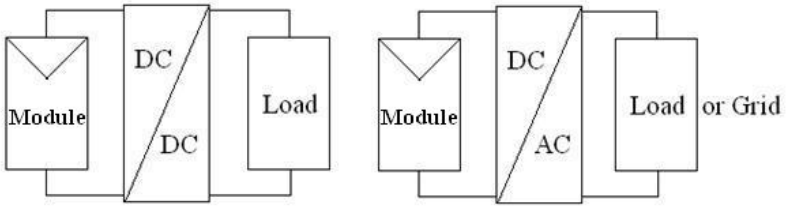


Figure 1.1: Two basic structures of PV systems

1.1.1 Stand-alone Systems

Stand-alone systems are systems supplying local loads and that are not connected to the grid. These systems are often used when the loads are located in remote areas (mountains ...) or when the load consumption is very small (a streetlight for example: the solar systems charges batteries during the day and the stored power is enough to produce light during the night).

1.1.2 Grid-connected Systems

Grid-connected systems are often larger system that have a purpose of "energy production". The bigger system are often managed by energy production companies whereas the smaller ones have private owners (system installed on the roof of a private housing for example). These systems rarely have storage capacities since the grid can be used as an "unlimited" energy sink (or source).

1.2 The PV System Components

A grid connected PV System will have different components from an isolated PV System (stand-alone).

The simplest structure is a direct connection (using a DC-DC converter) between the PV panels and the load (Figure 1.1), but we will see later on that some components need to be added in order to get the best out of the PV System. If the PV panels are connected to an AC load, or the grid, an inverter has to be added between the panels and the load. In both cases, energy storage systems can be added.

The topology of the entire PV System will then depend on its use and has to be reconsidered for each application. In order to make the most efficient PV System for our application, we first need to understand the working and the importance of each part: PV cells, modules, array, and the power electronics components.

1.2.1 The PV Cell

The PV cell is usually a special PN junction. If the cell is illuminated, a current and a voltage on its terminal are created. The amount of voltage and current directly depends on the cell illumination. The I-V characteristic equation of a PV cell is the following:

$$I = I_l - I_s \times (exp(\frac{qV}{mkT})) \tag{1.1}$$

I_l = photocurrent (A)
I_s = reverse saturation current ($\approx 10^{-8}/\mathrm{m}^2$)
V = cell voltage (V)
$q = 1.6\ 10^{-19}$ C
$k = 1.38\ 10^{-23}$ J/K
T = temperature (K)
m = cell ideality factor ($1 \ldots 5$; 1 = ideal)

Equation 1.1 shows that the PV cell is limited in current and in voltage. The cell will then not be damaged in an open-circuit condition or a short-circuit condition. In this case we can measure I_{sc}, the short-circuit current and V_{oc}, the open-circuit voltage. The maximum power, P_{max}, is defined as:

$$P_{max} = V_{mpp} \times I_{mpp} = FF \times V_{oc} \times I_{sc} \tag{1.2}$$

FF is the Fill Factor, I_{mpp} and V_{mpp} the current and voltage at Maximum Power Point (MPP, see below). The Fill Factor represents the quality of the cell. Typical Fill Factors vary from 0.5 to 0.82. The value of the Fill Factor depends on the physic of the cell. The schematic model of the PV cell and it's I-V characteristic are shown in Figure 1.2.

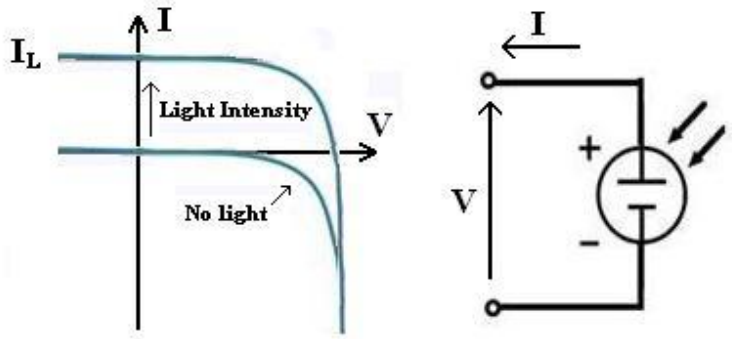


Figure 1.2: PV cell schematic and its I-V curve

When the cell is not illuminated, it behaves like a diode.

- As we said before, the current created by the cell depends on the cell illumination's (or irradiance). As irradiance increases, the generated power increases (Figure 1.3).
- The efficiency of the cell also depends on it's temperature. As temperature increases, the cell power decreases. I_s, the reverse saturation current is highly temperature dependant. This results in a decreasing open circuit voltage (V_{oc}) for increasing temperature (2.3 mV/°C) (see Figure 1.3). Equation 1.2 shows that if V_{oc} decreases, P_{max} decreases also. This aspect of the PV cell is important because when the cell is illuminated, only 20% of the irradiance is converted into electricity, the rest being converted into heat. Therefore it is important to ensure a very good cooling of the cell.
- Each characteristic has a maximum power point (MPP), which corresponds to the maximum power (IxV) that can be drawn out of the cell. This maximum power is obtained for a certain voltage and a certain current. The corresponding (I_{mpp},V_{mpp}) point is called MPP.

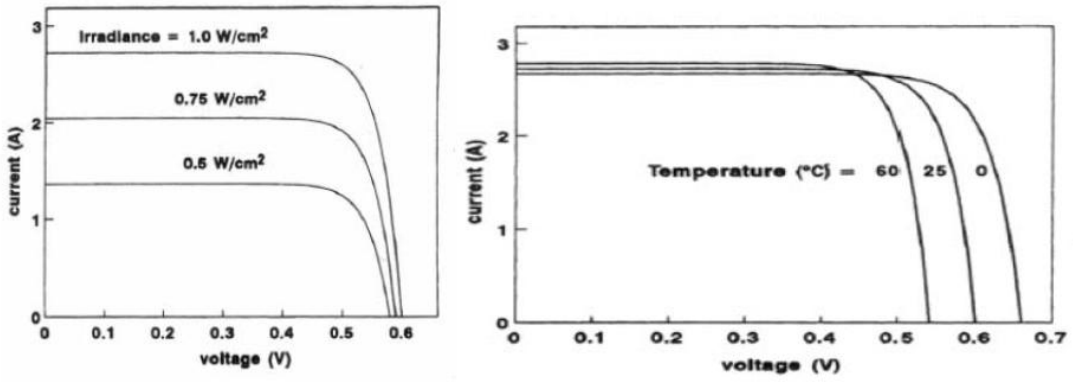


Figure 1.3: Cell characteristic for different irradiance levels and temperatures

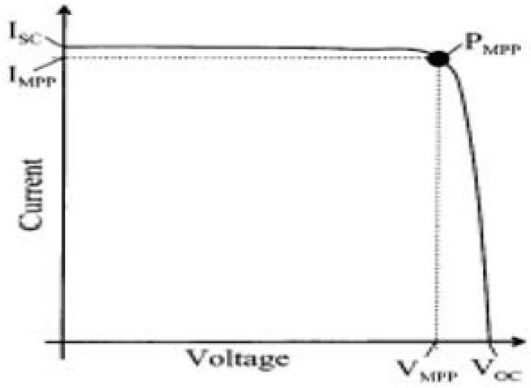


Figure 1.4: PV Cell characteristic with Maximum Power Point

1.2.2 The PV Module

A PV Module is formed by PV cells connected in series. Usually, modern modules contain from 60 to 70 cells depending of the technology (monocrystalline or polycrystalline silicon). This permits to have a sufficient output voltage, suitable for PV systems. Usual modules have a V_{oc} of about 40V and generate from 150 to 200 Watts, but it is also possible to find modules which have lower output powers. Two considerations have to be taken into account when connecting modules.

- When the module is not illuminated:
  It is possible, depending on the system configuration, that when the module is not illuminated (night or general shading) the diodes (PV cells) are forward biased by the system storage battery for example. This will result in a battery discharge (current flowing in the opposite direction) in the PV module. To avoid this, a blocking diode can be connected in series with the module (Figure 1.5). However,

under day illumination, this blocking diode will represent a loss of energy.

- When the module is partly shaded:
  If only a few cells are shaded in a module connected in parallel with other modules, then these cells can be forward biased. The result will be the heating of the cell and probable cell failure. Modules are generally protected from this phenomenon by adding bypass diodes (Figure 1.5). Instead of flowing in the shaded cell, current will flow through the bypass diode.

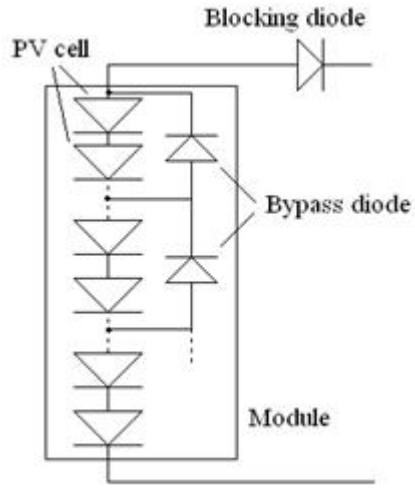


Figure 1.5: PV module with blocking and bypass diodes

- It is also important that all cells have the same I-V characteristic for the same irradiance level. Otherwise, a part of the power generated by some cells will be dissipated by the one having a different characteristic. If the cells characteristics are identical (or at least very close), then it is possible to draw out the maximum power of every cells by looking at the MPP of the whole module.

1.2.3 The PV Array

PV systems need a certain voltage to work in good conditions. To obtain this voltage, modules are arranged in series and in parallel. Series connection permits to increase the voltage while parallel connection increases the current.

- We previously said that each module had a MPP. To obtain the best efficiency we need the modules connected in series to have their MPP for the same current and the modules connected in parallel for the same voltage.
- Different array arrangements allow different combination of output voltages. For example, two modules connected in series, in the opposite direction and with the

middle point grounded provide a negative and a positive voltage (Figure 1.6). Three sets of this combination of module could feed a 3-phase inverter for example.

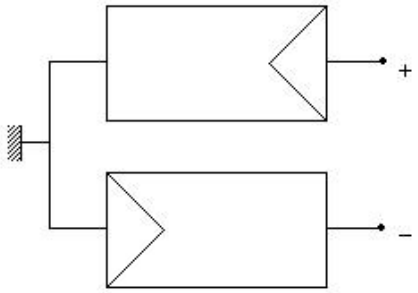


Figure 1.6: Parallel combination providing + and - voltages

1.3 Power Electronics in a PV System

1.3.1 Various Power Electronics Components

- Charge controllers:

If the PV System has energy storage (batteries...) then charge controllers must be added. The load has to be disconnected if the batteries are discharged and, on the contrary, the PV panels have to be disconnected if the batteries are fully charged. Furthermore, charging and discharging must be controlled for optimal performance under different temperature, load, and PV production conditions.

- Converters/Inverters:

Any PV system will need a type of converter (DC/DC, DC/AC). Many different configurations of converters exist depending of the topology of the PV system: how many modules, connected in series or in parallel, connected to the grid or to an isolated load, etc.

Usually more than one conversion stage is used, for example DC-DC plus DC-AC. These configurations must be adapted to the topology of the PV system by taking account the efficiency of the total system, the size (fixed or embedded system) and also, to a certain extent, the price.

- MPP Tracking:

Maximum power point tracking[1] is one of the most important features. It permits the system to always draw as much power as possible from the PV module. The MPP is

[1]Maximum Power Point Tracking will be called “MPPT” throughout the rest of the document.

found for a certain (I,V) couple of the I-V curve of the solar system. MPP tracking is most of the time done by a DC/DC converter directly connected to the module. By modifying the duty cycle of the converter's switches, the current or the voltage of the module's terminal are modified. The DC/DC converter can then control the (I,V) couple, hence the MPP. Sometimes, if the array is connected to the grid or an AC load, the MPP tracking is done by the DC/AC converter.

Ideally, each Module should have the same MPP characteristic which will permit to have only one MPP tracking for the whole array. But module's MPP characteristic varies for many reasons: illumination, temperature ... Therefore in order to have the best efficiency for our system, MPP tracking for each module should be the best solution.

However, if the PV installation is too small, the sum of the local losses (due to individual MPP) will be greater than the gains made on the total efficiency. And even if there is a total efficiency gain, it is still possible that the cost of individual MPP is greater than the profit gain. Therefore in some cases it can be either useless or unprofitable to use MPP tracking.

1.3.2 Various Voltage Transformation Stages

The basic configuration of this stage would be either to connect a DC-DC converter (boost converter), for a DC load, or a DC-AC converter for an AC load or grid connection (1.7).

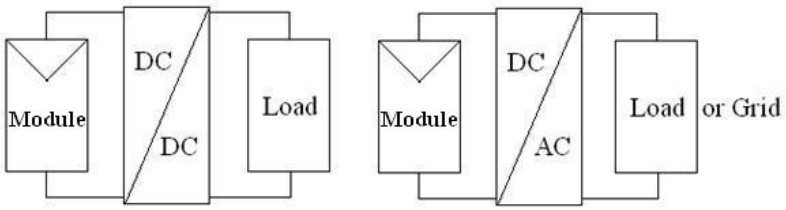


Figure 1.7: Two basic structures of PV systems

In most cases a converter is needed for many reasons. One of the main one is that the DC voltage delivered by the PV panels varies with the illumination while the voltage (peak voltage for AC voltage) needed for the load or the grid is constant. A converter using a MPP algorithm permits to always make the PV panels work at their optimal voltage and current point in order to get the maximum power out of the panel.

However, a great number of configurations can be chosen, each with its advantages and disadvantages. Depending on the PV panels' configuration, more than one boost converter can be used for MPP tracking, as well as more than one inverter can be used also. Different configurations are shown in Figure 1.8.

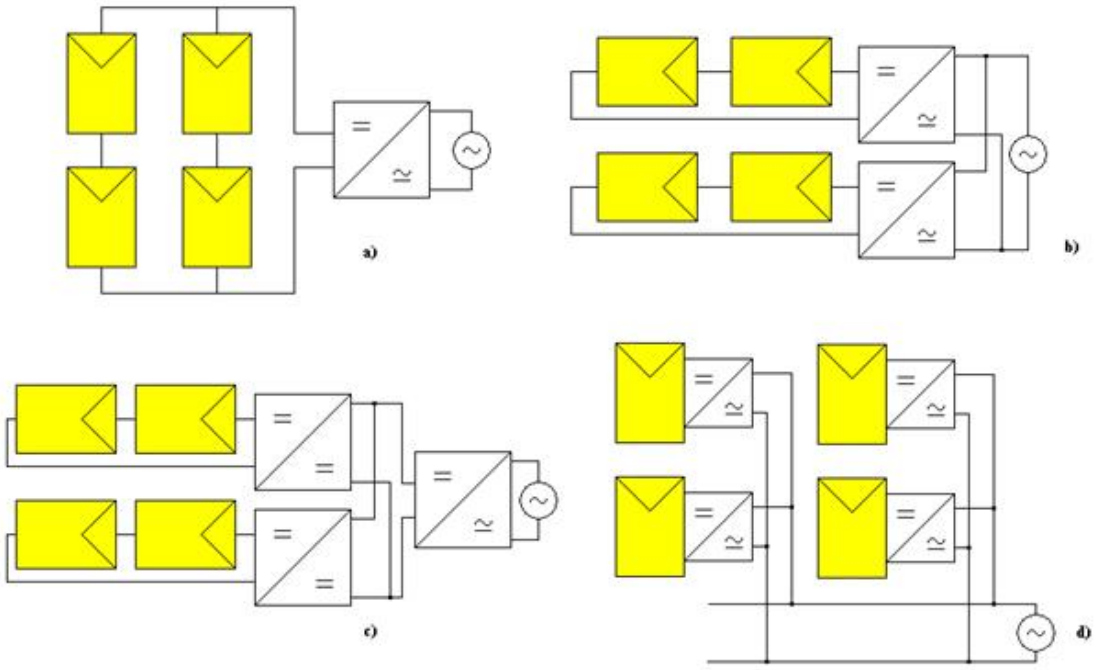


Figure 1.8: Different configurations of converters and inverters with PV modules

- When the DC voltage is higher than the peak AC voltage, no boost converter is needed. In that case a single inverter can operate the MPP tracking (Figure 1.8.a), leading to a highly efficient system.
- In case of more than one string, an inverter for each string can be used (Figure 1.8.b), leading to an independent MPP tracking for each string. But adding inverters also adds losses. The balance between the added losses due to numerous inverters and the reduced losses due to separate MPP tracking has to be made in order to choose the best solution.
- In some cases, a two stage conversion is used. The first stage is a DC-DC conversion, permitting a large input voltage range for each string. The first stage converters are connected in parallel before being connected to the DC-AC inverter (Figure 1.8.c), which is the second stage.
- It is sometime chosen to have an inverter behind each module (Figure 1.8.d), therefore connected to the grid only. These configurations are often chosen for practical reasons: low power level inverters are small and can be integrated into the housing, easier installation since there is no DC wiring. On the other hand these configurations have lower efficiency because of the low power levels and do not use MPP tracking because the efficiency gain is not significant compared to its cost. Furthermore the PV panel has a longer life time than the inverter. If the

inverter breaks down, the whole system (PV panel + inverter) has to be replaced.

Chapter 2

Project Description

The aim of this project is to design a low power inverter for the connection of solar panels to the grid and/or a local load. The inverter is wanted to be simple and efficient. A general description of its main characteristics are found below.

2.1 General Description

In order to make a simple and small inverter, the usual DC-DC stage (between the solar panels and the inverter) is left out. Therefore there is only one stage between the solar panels and the grid (a DC-AC stage: the inverter) which reduces the total losses.

Of course leaving out the DC-DC stage brings new constraints, the main one being that the panel output voltage cannot be boosted.Also, the MPPT usually done by the DC-DC stage is now done by the inverter.

The output nominal ratings of the inverter are 5A and 36V. The nominal output power is therefore approximately 200W. These values are well adapted for example for 2 x 24V or 4 x 12V solar panels input. Indeed in order to work properly, the input voltage must be slightly greater than the output voltage. The inverter can then be connected to the grid through a 36V/230V transformer.

Digital control/MPPT of the inverter will be done with a Digital Signal Processor (DSP) from Texas Instruments.

Summary of the inverters main characteristics:

- No DC-DC stage
- Digital control
- Output nominal ratings: (5A, 36V) $\approx$ 200W

- Grid connected through transformer (36V/230V)

Using digital control (opposed to analog control) brings some advantages. A DSP being easy to program, different control algorithms (as well as MPPT algorithms) can be tested and corrected very easily and quickly, the system is very flexible.

In this project, the TMS320C2000 Developers kit board (from Texas Instruments) will be used for simplicity because it is "ready to be used". Of course any other kind of DSP's can be used. Details on the control of the system are given in section **2.3**.

The whole system will consist in 3 electronic boards: the "Developers Kit" board, a "signal scaling board" and a "power electronic" board. The design of each board and their operation mode will be discussed later on in chapter 4.

Summary of the system's equipment and general schematic (Figure 2.1):

- TMS320C2000 Developers kit board (use of the F2808 DSP)
- One "signal" board (signal scaling, drivers, interface between DSP and the power electronics)
- One "power electronic board"

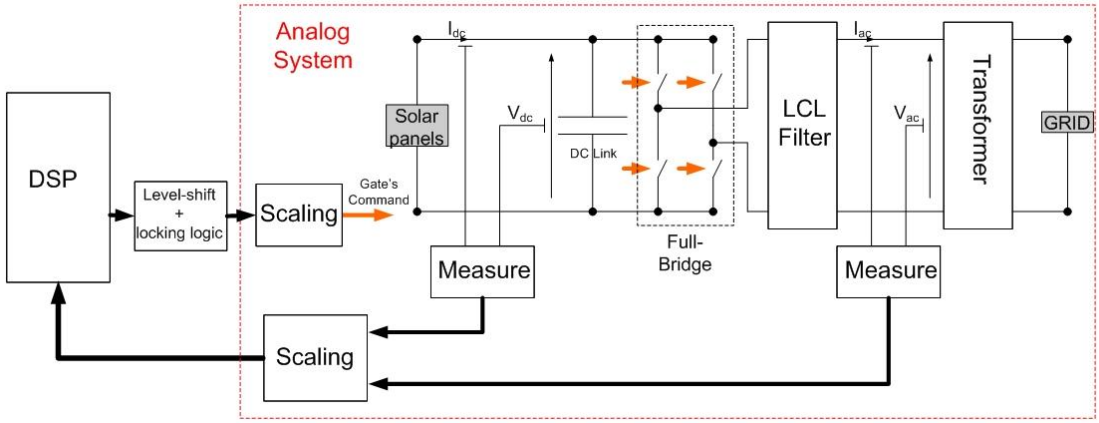


Figure 2.1: General schematic of the whole system

2.2 System Topology

The topology of the inverter is one of the first aspects of the system to define. Indeed each topology needs an appropriate control. Here a Full-Bridge topology is chosen (see Figure 2.2).

This topology has the main advantage of being able to deliver at the output the entire input DC voltage (positively or negatively), in opposition to a Half-Bridge technology.

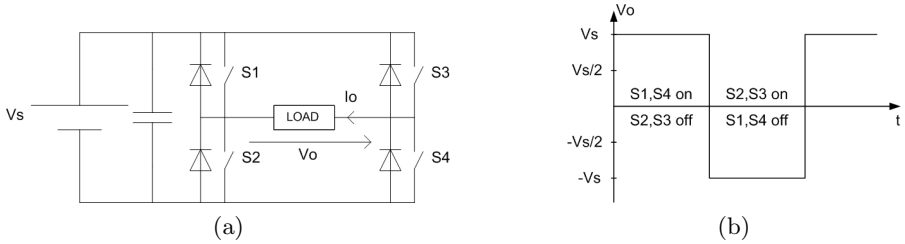


Figure 2.2: Full-bridge schematic and it's switching characteristic

Furthermore it allows the use of a "unipolar PWM command" (described in section 5.1) which gives a more precise and effective control of the inverter.

2.3 System Control

The control of the system will be digital (use of a DSP) therefore giving great flexibility. The DSP can be differently programmed which is very useful for leading studies on different control method easily and quickly.

2.3.1 Type of Control

Since the inverter shall be connected to the grid, the output voltage does not need to be controlled (the grid is acting like an ideal AC power supply). Therefore the inverter is based on a current (injected to the grid and in phase with the grid voltage) control loop.

2.3.2 MPPT control

As an improvement to the inverter's control, a MPP tracking control can later be used for increasing the efficiency of the system and using the maximum power available delivered by the PV modules. The digital aspect of the control allows a later easy implementation of this MPPT control, provided of course that the hardware design allows it.

Chapter 3

DSP Programming

This chapter describes the method used in the project to program the DSP. The control developed throughout the project will be introduced in chapter **5**.

3.1 General Information

As previously seen in figure 2.1 the control of the inverter will be digital (use of a Digital Signal Processor or DSP). In this section general information will be given about what is needed in order to use a digital control.

The Needed Equipment

The inverter will be composed of an analog electronic circuit and a DSP. In order to program the DSP, several hardware-components will be required.

Hardwares:

- A Digital Signal Processor possessing at least 4 ADC channels and 4 PWM channels. The DSP used for the project is the TMS320F2808 from Texas Instruments.
- A J-Tag Emulator (DSP to PC connection)

The Programming Method

DSP programming is usually written in C language in Code Composer Studio (or any other IDE[1]. But writing a correct and efficient program directly in C-code requires a

[1]Integrated Development Environment

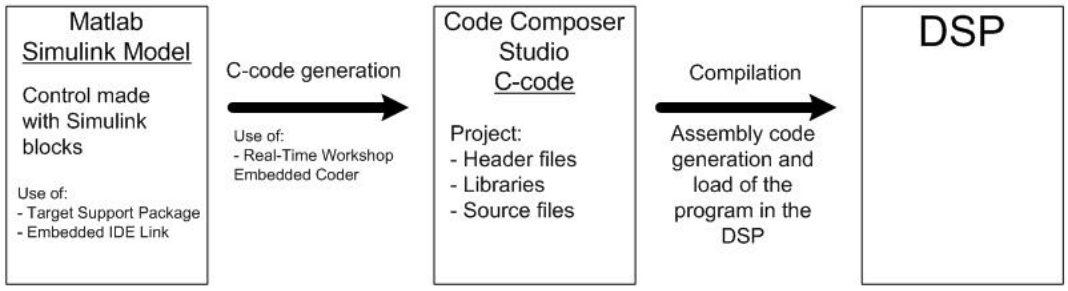


Figure 3.1: DSP programming steps

certain knowledge. Therefore another programing method is used, "Model-based programming": the inverter's control program will be realized with Simulink and the C-code will be automatically generated from the Simulink model. Code Composer Studio is then used to compile the C-code and load it in the DSP.

The figure 3.1 summarizes the programing steps of this method.

- Advantages of model-based programming:
  - The use of an intuitive graphical interface (Simulink blocks in a Simulink model file)
  - No C-code programming knowledge is required
- Disadvantages of model-based programming:
  - The generated C-code could be more efficient

3.2 Code Composer Studio (CCS)

The configuration of CCS will be examined first since the configuration of Matlab needs CCS to be configured first. The configuration of CCS consists in telling CCS which system will be used (here a TMS320F2808 form Texas Instruments) in order to have a correct communication between the DSP and CCS.

Configuration of CCS

NOTE: The J-Tag emulator needs to be correctly installed in order to correctly configure CCS.

To configure CCS, the "Setup Code Composer Studio" application has to be launched.

In the CCS Setup, the board as well as the J-Tag emulator that are used have to be chosen. In this project, the "Blackhawk USB 2000 - F2808 Controller" is used.

3.3 Matlab's use

Matlab and Simulink will be used to create the inverter control program that will be implemented in the DSP. The control is simply made in a Simulink model file. However special toolboxes are needed, they are described in the next section.

3.3.1 The Needed Toolboxes

The following toolboxes are needed.

- Real-Time Workshop 7.4:
  Required by Real-Time Workshop Embedded Coder
- Real-Time Workshop Embedded Coder 5.4:
  Generates C-code from the Simulink model
- Target Support Package 4.0:
  Deploys the generated code onto the DSP
- Embedded IDE Link 4.0:
  Connects Matlab and Simulink to the embedded software development environment Code Composer Studio

3.3.2 Configuration of Matlab

Programming the DSP becomes very easy once Matlab and Simulink have been correctly configured.

The first step is to verify the configuration of the Embedded IDE Link toolbox. The correct configuration is necessary for creating a CCS project (containing all the header files, libraries and source files that will be generated from the Simulink Model).

The detailed configuration steps are found in the *Product Help* of Matlab $\longrightarrow$ *Embedded IDE Link* $\longrightarrow$ *For Use with TI's Code Composer Studio* $\longrightarrow$ *Getting Started* $\longrightarrow$ *Configuration*

The second step is to configure the simulation options of the Simulink model that will be used (in the model: *Simulation* $\longrightarrow$ *Configuration parameters...*). In the Configuration parameters panel, several information needs to be considered:

- In the *Solver* tab:
  The start and stop time of the simulation have no effect on the code generated
  The type **must** be *Fixed-step* in order to generate code

- In the *Hardware Implementation* tab:
  The device vendor and device type have to be chosen accordingly

- In the *Real-Time Workshop* tab:
  The system target file that must be used is: csslink_ert.tlc This particular system target file is necessary when using the Embedded IDE Link (the _ert version must be used when using Real-Time Workshop Embedded Coder whereas the _grt version is to be used with Real-Time Workshop).

- In the *Real-Time Workshop* $\longrightarrow$ *Embedded IDE Link* tab:
  The build action can be chosen to be "Build" only (which only creates the project in CCS with the corresponding C-code) or "Build and execute" (which builds the project, loads the program in the DSP, and runs the program). The "Build" option is recommended if Real-Time Mode is needed because it needs to be selected before running the program in the DSP (see section **3.4.3**).

More information on the configuration of the model can be found in:
Product Help of Matlab $\longrightarrow$ *Real-Time Workshop Embedded Coder* $\longrightarrow$ *Getting started* $\longrightarrow$ *Learning and Using RTW Embedded Coder Software* $\longrightarrow$ *Understanding the Demo Model* $\longrightarrow$ *Viewing the Configurations Options for Code Generation*
and in:
Product Help of Matlab $\longrightarrow$ *Embedded IDE Link* $\longrightarrow$ *For Use with TI's Code Composer Studio* $\longrightarrow$ *User Guide* $\longrightarrow$ *Project Generator* $\longrightarrow$ *Setting Model Configuration Parameters.*

3.4 Instructions for Programming the DSP

Once all the hardwares and softwares are installed and configured, programming the DSP is not very difficult. It is done in 3 steps:

1. Control design with Matlab/Simulink

2. Generating the C-code

3. Loading and running the code on the DSP

NOTE: Steps 2 and 3 are done in a few "mouse click" making the programming very simple.

3.4.1 Control design with Matlab

A simple Simulink model file is used for the design of the control.

The first Simulink block to insert in the model is the "Custom Board" (found in the Embedded IDE Link library). This block configures the Simulink model for the DSP that is used (F2808 in the case of this project).

In addition any block from the library of the Target Support Package corresponding to the concerned DSP (C280x in our case), or from other Simulink toolboxes, can be used in order to create the desired control.

The demo tutorial "ADC-PWM Synchronization via ADC Interrupt" of the Target Support Package is a simple and efficient way to see and try a first example using the ADC and the PWM blocks of the DSP.

Finally the Configuration Parameters of the simulation must be properly tuned, as described in section 3.3.2.

3.4.2 Creating the program C-code

Before the generation of the C-code, it is better to check that, as written in section 3.3.2, the configuration parameters of the Embedded IDE Link is "Build".

The C-code is generated either by:

- Clicking on the *Incremental Build* button in the Simulink model's toolbar
- Clicking on *Tools* $\longrightarrow$ *Real-Time Workshop* $\longrightarrow$ *Build Model*

Matlab should then launch CCS, generate the project, and build it. In CCS, in the output window, the following message should appear:

Build Complete,
0 Errors, 0 Warnings, 0 Remarks.

A file, named after the name of the project and with a ".out" extension will also be created.

3.4.3 Loading and running the code on the DSP

Once the project is built and contains no errors, the ".out" file can be loaded in the DSP via *File* $\longrightarrow$ *Load Program ...*.

NOTE: The following commands should be executed every time before the program is "Run" on the DSP.

1. Menu *Debug* $\longrightarrow$ *Reset CPU*

2. Menu *Debug* $\longrightarrow$ *Restart*
3. Menu *Debug* $\longrightarrow$ *Go main*

The DSP is now halted and the program is ready to be run.

Real-Time Mode

If the Real-Time Mode is needed, for example for watching the values of certain variables (ADC conversion results, PWM signals...), the Real-Time Mode option (in the *Debug* menu) **must** be selected **after** the resetting command sequence and **before** running the program.

Refresh options can be configured in the entry *Real-Time Refresh Options ...* under the *View* menu.

Chapter 4

Designing the System's Boards

This chapter concentrates on the different electronic board that the whole system consists of. All schematic and layouts of the boards of the system can be found in Appendix **A**.

4.1 Boards of the System

The figure 4.1 shows the 3 boards of the system and their connections. Detailed inputs and outputs of each board will be described in further sections.

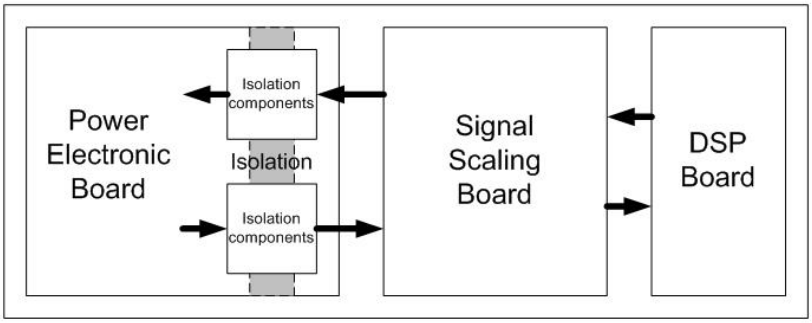


Figure 4.1: Isolation of different parts of the system

4.1.1 PCB Design Software: EAGLE

The software used for designing the printed circuit board is EAGLE, a software from Cadsoft. This software has been chosen for it's simplicity and suits well students that have never designed a printed circuit board before (compared to Orcad which is a much more professional software).

The first step in designing a printed circuit board is creating the schematic of the board. EAGLE has numerous libraries of components (more can be found on the software's website) which makes it very easy. The second step is making the layout of the components on the board.

Creating a new library

As some components did not have a corresponding package (or footprint) in the existing libraries it was necessary to create them. Each library consist in a series of "packages" and "symbols" which are used to create "devices".

The footprints of the following devices have been created for this project:

- DC-DC converter from XP Power
- Current sensors from LEM
- Optocoupler gate drivers from Avago Technologies

Sometimes footprints from other devices can be used, however the schematic symbol often does not correspond and can bring confusion when looking at the schematic. Therefore it is sometimes necessary only to change the symbol of a device (it has been done for the optocoupler gate driver for example).

4.2 The TI "Digital Power Experimenter Kit"

The TI "Digital Power Experimenter Kit" is the DSP board used for this project simply because it was available. In a later stage, a DSP control card could directly be integrated to the inverters PCBs.

4.2.1 Board Description

The DSP board is part of a kit. However only the DSP control card with its inputs and outputs will be used. Figure 4.2 shows the block diagram and the used inputs/outputs of the board.

Descriptions of the ADC and the PWM channels are found in the next sections. Throughout the rest of the document this board will simply be referred as the "DSP board".

The Analog Digital Converter (ADC)

In this project the ADC will receive signals corresponding to various signal measurements made at the inverters input or output: Input DC voltage, Input DC current, Output AC

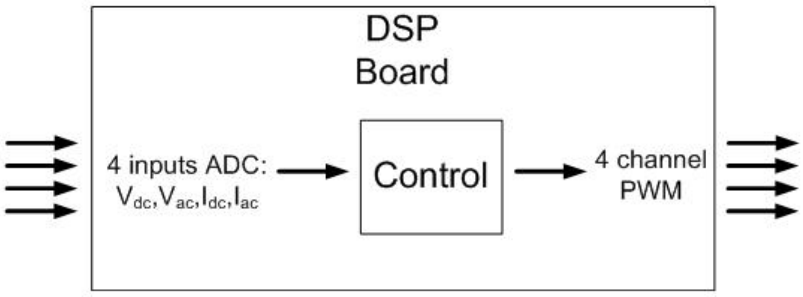


Figure 4.2: Block Diagram of the DSP board

voltage, Output AC current. Theses signals will be used for the creation of the inverter's command signal as well as in the MPPT algorithm.

The ADC connector on the board consists of 8 female pins which have an input voltage range from 0 to 3 Volts. The measured currents and voltages will have to be scaled in order to respect this range.

The Phase Width Modulation (PWM) Channels

The DSP has 6 PWM channels, each consisting in 2 signals, A and B (1A, 1B, 2A, 2B ... 6A, 6B). The A and B PWM signal of each channel cam be programed in many different ways (identical, complementary...) and options such as deadband delay can be easily added. We will therefore use both A and B signals of channels 1 and 2 in order to generate 4 PWM signals, one for each inverter's switch.

NOTE: The channels 3 to 6 are already used for the board's integrated buck-boost. In order to be used as outputs, function properly, and for safety reasons, resistors R5, R6, R7, R8, R9 and R10 (shown in the kit schematic, see Appendix A) must be removed.

The PWM channels connector consists of 12 pins which have an output voltage range from 0 to 3 Volts. The generated signals will also have to be scaled in order to become a proper mosfet command.

4.3 The Power Electronic Board

This board contains all the "power electronic" and the measurements circuits of the different currents and voltages. The power electronic part of the system must be electronically isolated from the rest of the system (signal scaling board and DSP). See Figure 4.3. This mean that the power supplies for each part, as well as the grounds, should be different. It permits to eliminate the risk of destroying certain components with too high

currents/voltages and also brings better signal precision since the noisy power ground is separated from the signal ground.

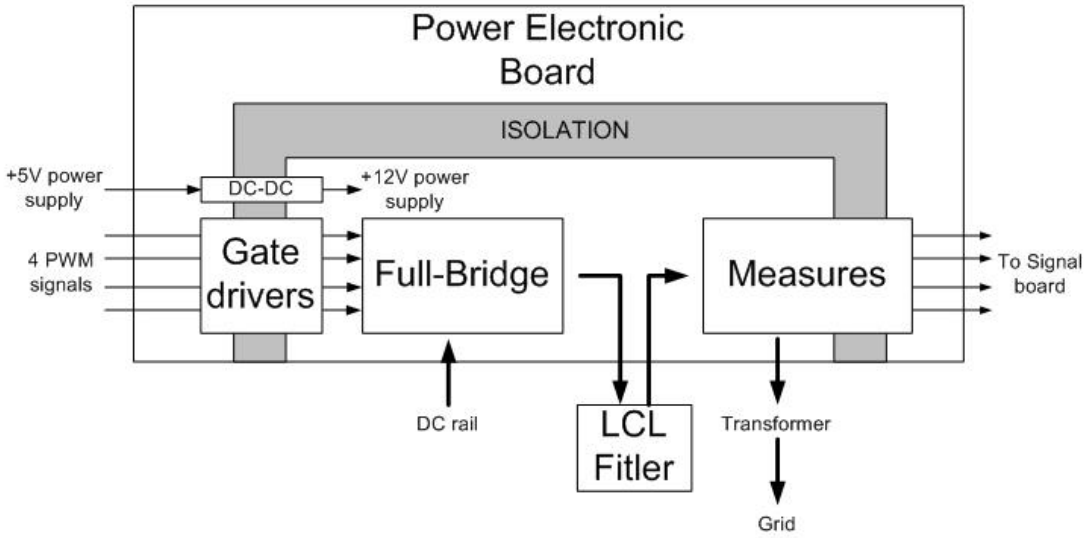


Figure 4.3: Block Diagram of the Power board

4.3.1 Board Description

This board will consist of the following components:

- DC rail connector (from solar panels)
- DC link capacitor
- The 4 mosfets of the full-bridge
- Connector to the LCL-filter
- Connector from the LCL-filter
- Connector to the transformer
- Current and voltage sensors
- Isolation components (optocouplers and isolation amplifiers)
- Various electronic components for managing the right power supply of the IC components

See figure 4.3.

4.3.2 Board Design

Power supply:

As previously stated the board will have 2 different power supplies and 2 different grounds in order to isolate the power electronic part from the signal part. The main power supply of this board will be +5V and will come from the Signal Scaling board.

A IV0512SA DC-DC converter (from XP Power[1]) will be used in order to bring a +12V power supply on the power electronic side of the board. Since some components of the power electronic side also need a +5V supply, a L78L05 (from ST Microelectronics[2]) is used to deliver +5V from the +12V power supply.

DC link capacitor:

The capacitor is a necessary link between the solar panels, which have a varying output voltage, and the full-bridge which needs a quite stable input voltage. The capacitor will also smooth out the voltage perturbations. The chosen capacitor value is 4.7mF and is rated for 100V.

Power Mosfets and their gate drivers:

The chosen Mosfets are the IRFB4110G (from International Rectifier[3]). They have a Drain-to-Source breakdown voltage of 100V and a low Drain-to-Source "ON" resistance (3.7mΩ). The Drain current limitation is much higher than the needed Drain current. The maximum gate threshold voltage given by the datasheet is 4V. This mean that the gate signals should be safely higher than 4V to ensure a correct switching.

The HCPL-3180 gate drive optocoupler (from Avago Technologies[4]) will be used for driving the mosfet's gate signals. The advantage of this component is the galvanic isolation that it provides between the signal side and the power side. A resistor (called "gate resistor") needs to be added between the optocoupler and the mosfet. The calculation of the gate resistor value is made following the datasheet recommendation. A so-called "'Bootstrap capacitor" is also needed to apply an appropriate voltage to the mosfet's gate in order to turn it on.

[1] www.xppower.com
[2] www.st.com
[3] www.irf.com
[4] www.avagotech.com

Current transducers:

Two current sensors (LTS 25-NP from LEM[5]) will be used for measuring both the DC current coming from the solar panels and the AC current at the output of the LCL filter. They are Hall effect sensors which brings galvanic isolation between the primary circuit (high power) and the secondary circuit (electronic circuit).

The DC current range that is to be measured is [0;10V] whereas the AC current range will be [-10;10V]. The primary nominal current of the sensor is 8A if 3 primary turns are made in the pins connection. For a measured current of 0A, the output voltage is 2.5V. The output voltage then increase/decrease when the measured current increases/decreases. The output voltage follows the following equation:

$$V_{out} = \frac{I_p \times 0.6}{I_{pn}} + V_{ref} \tag{4.1}$$

Since the wanted measuring range for the DC current measurement is [0;10A], the output voltage range of the sensor that should be considered is [2.5;3.25V].

For the AC current measurement ([-10;10A] voltage range), the output voltage range of the sensor that should be considered is therefore [1.75;3.25V].

DC and AC Voltage sensing:

The DC voltage sensing will be made at the capacitor's pins whereas the AC voltage sensing will be made at the output of the LCL filter.

The ACPL-782T (from Avago Technologies) isolation amplifier will be used in order to bring galvanic isolation between the signal side and the power side of the board. This device has 2 input pins (V_{in+} and V_{in-}) and 2 output pins (V_{out+} and V_{out-}). As shown in equation 4.2 the output pins have an offset of 2.5V in addition to their respective input signal multiplied by 8 (internal gain of the amplifier).

The datasheet of the ACPL-782T states that for a linear and accurate operation, the signals V_{in+} and V_{in-} must be in the range [-0.2;0.2V]. Therefore V_{out+} and V_{out-} will be in the range [2.5-(1.6×0.2) ; 2.5+(1.6×0.2)]. We can also simply write that (V_{out+}-V_{out-}) will be in the range [-1.6;1.6V].

NOTE: For the DC voltage measurement the V_{in-} pin is connected to ground. Consequently, (V_{out+}-V_{out-}) will be in the range [0;1.6V].

$$V_{out\pm} = (V_{in\pm} \times 8) + 2.5 \tag{4.2}$$

[5] www.lem.com

- AC voltage

The AC voltage is measured with the voltage divider shown in figure 4.4 which permits to keep the sign of the measured voltage.

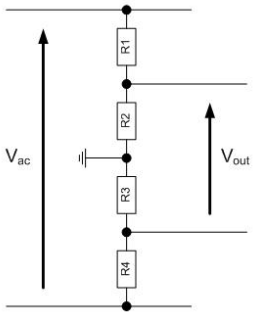


Figure 4.4: AC Voltage divider

In figure 4.4 if R1 equals R4 and R2 equals R3, then:

$$V_{out} = \frac{V_{ac} \times (2 \times R2)}{2 \times (R1 + R2)} \tag{4.3}$$

The voltage divider ratio will approximately be:

$$\frac{2 \times R2}{2 \times (R1 + R2)} = \frac{|55|}{|0.2|} = 275 \tag{4.4}$$

$|55|$ being the maximum voltage that we want to be able to measure and $|0.2|$ because of the ACPL-782T characteristics.

- DC voltage

The DC voltage is measured with a classic voltage divider with the same ratio as the AC voltage divider: 275.

LCL Filter

The LCL filter parameters have been determined throughout a Matlab simulation. Though the filter will not be added directly on the printed circuit board (for easier access/replacements of the filter components), it will be described here how it has been designed.

The LCL filter design procedure that was followed is explained in details in [1] and [2]. A summary of the method is given below:

1. Choice of the tolerable current ripple at the inverter's output $\longrightarrow L_{inv}$
2. Choice of the reactive power absorbed in rated condition $\longrightarrow C_f$
3. Choice of the desired total current ripple reduction $\longrightarrow L_g$
4. Calculation of the resonance frequency $\longrightarrow R_d$, damping resistor

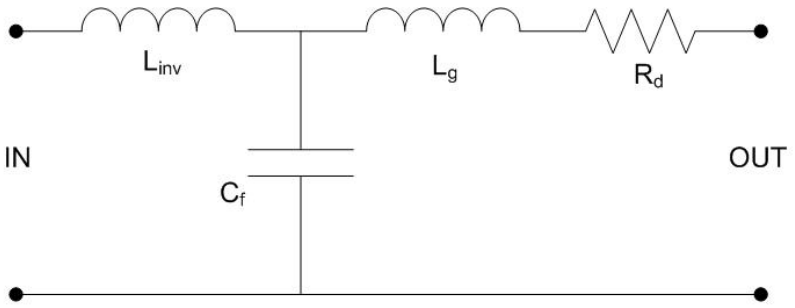


Figure 4.5: LCL filter connected at the output of the inverter

The calculation of the filter's parameters can be programed in a Matlab M-file. Choosing L_{inv}, x (the tolerable decrease of power factor) and r (the ripple reduction) allows to find the remaining parameters (L_g, C_f and R_d).

A Simulink model can then be used to simulate the system with the previously calculated parameters to verify the proper operation of the filter.

The calculations will be detailed in section **6.2**.

The Transformer

The 200VA transformer used to connect the output of the filter to the grid has one primary winding, for the 230V side and 2 secondary windings rated at 18V. These 2 secondary windings can be connected in parallel and support 5.55A.

Once connected to the grid and the secondary windings connected in parallel a measurement of the voltage on the secondary side gives a RMS value of 20.4V (thus a peak value of 28.8V).

4.3.3 Tests and corrections

In this section will be listed the different tests and corrections that have been made on the board. Of course the schematic and layout files have been modified to take into account the corrections and now present a properly working board.

- Test of the power supply of the board

The +5V power supply of the "signal" side components is correct. The DC-DC converter gives a good +12V supply for the "power" side. However, the L78L05 voltage regulator is not working. The problem comes from an error that I made in the design of the component in the EAGLE library. The design has been reviewed and is now correct.

- Test of the gate drivers

The HCPL-3180 are tested. They are fed with PWM signals with an amplitude of 5V. The gate signal of each mosfet is observed to verify the proper gate driving. The gate driver operate correctly.

- Test of the voltage sensing

The DC and the AC voltage measurements are tested with a DC power supply. These tests are meant to check that the voltages sensing are working properly. The DC voltage is tested for several values between 0 and 30V whereas the AC voltage is tested with several values between -30 and 30V. The measurements are properly working.

NOTE: A precise calibration of both current and voltage measurements will be implemented in software.

- Test of the current sensing

Both DC and AC current measurements are also tested. DC current is tested for several values between 0 and 10A whereas AC current is tested for several values between -10 and 10A. It appears that there is an error in the design of the footprint of the current transducers in EAGLE (top view designed instead of bottom view designed).

As previously described, the current transducers have an output voltage of 2.5V for a sensed current of 0A. This output voltage increases/decreases when the sensed current increases/decreases meaning that an output voltage superior to 2.5V represents a **positive** current and inferior to 2.5V a **negative** current. However the design error consequence is that the current are sensed in the wrong direction. Therefore an output voltage superior to 2.5V represents a **negative** current and inferior to 2.5V a **positive** current.

For the AC measurement the error can be easily corrected directly in the ADC. But for the DC measurement, this means that the output voltage range that needs to be considered is not [2.5;3.25V] (as planned in section **4.3.2**) but [1.75;2.5V].

Furthermore, the output signal and the power supply signal inversion is another consequence of the design error. This error was fixed by scraping the 2 concerned tracks and making new correct connections by soldering 2 wires.

4.4 The Signal Scaling Board

This board is an important link between the DSP board and the power electronic board. Indeed, signals generated by the DSP cannot be used as they are, they must be scaled. Of course this is also true with the input signals of the DSP (system measurements).

4.4.1 Board Description

The tasks that this board will have to accomplish are the following:

- Level-shift the PWM signals generated by the DSP for the isolation gate drivers of the mosfets and provide locking-logic.
- Scale the outputs of the voltage sensors for the ADC's inputs.
- Scale the outputs of the current sensors for the ADC's inputs.

Figure 4.6 shows a block diagram of the board.

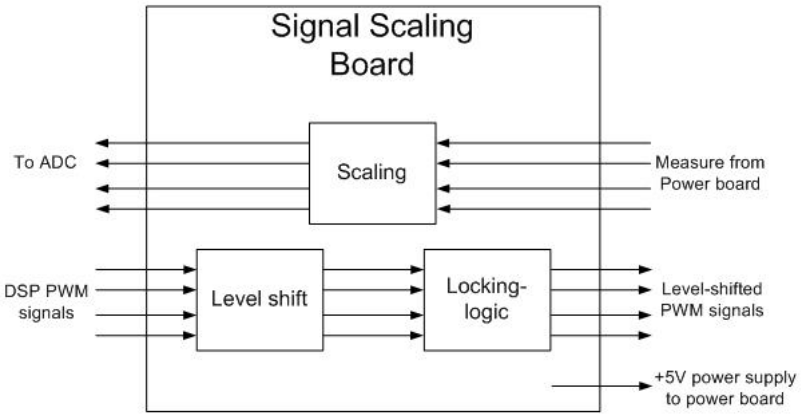


Figure 4.6: Block Diagram of the Signal Board

4.4.2 Board Design

Power Supply

This board has 2 different power supplies, both of +5V. One is for supplying the different IC's of both the signal and the power board and the other one (which has a better precision) is for supplying the different voltage dividers.

The LM340T5 7805 (from National Semiconductor[6]) is used for providing the main +5V

[6] www.national.com

supply of the board. The device is rated for a 1A output current. This characteristic is necessary since the device provides a supply voltage for a lot of devices (on both signal and power board).

The REF02AP precision voltage reference (from Burr-Brown Products from Texas Instruments) provides a precise +5V voltage to the 3 different voltage dividers used in this board (see later on AC voltage scaling, AC and DC current scaling). In order to operate correctly, the REF02 needs a power supply of 8V minimum. Therefore both LM340T5 7805 and REF02 are supplied with an external power supply higher than 8V.

PWM level-shifting

The DSP generates PWM signals that have a voltage range of 0 to 3V. These signals cannot drive the actual mosfet's isolation gate drivers directly. In order to amplify these signals, the TPS2814 Texas Instruments gate driver has been used.

An additional advantage of using the TPS2814 is that it can add a safety-locking-function to the PWM signals. Two mosfets of the same inverter leg cannot be put "On" at the same time otherwise a short circuit is created. Even though the command signals generated by the DSP should take this into account, a programming error could lead to this situation. The TPS2814 permits to avoid this with a simple logic system:

- If 2 PWM signals of mosfets of the same inverter leg are "high" at the same time, the outputs signals are "low"
- If the 2 PWM signals have a different state ("high"&"low" or "low"&"high") or if both signals are "low", the outputs signals are equal to the input signals.

The use of the TPS2814 adds a new constraint: the Positive-going input threshold voltage of the device is, typically, 3.3V (maximum 4V). But the PWM signal of the DSP is in the range 0 to 3V. So a 5V voltage pull-up circuit is added in order to be sure that the threshold voltage is obtained.

The signals generated by the TPS2814 can then be safely used by the optocouplers without any risk of short circuiting any leg of the inverter.

Scaling the voltage sensing

- AC voltage scaling

It has been seen in section 4.3.2 that the voltage measurement signal coming from the power board will be in the following range [-1.6;1.6V]. But the DSP's ADC can only receive signals in the range [0;3V]. The signal coming from the power board therefore needs to be scaled.

The scaling will be done with a amplifier circuit (using a TLC272 operational amplifier from Texas Instruments). The circuit will have to recenter the signal range into the range [0;3.2V] and then scale this range to a [0;3V] range on order not to loose information.

The circuit is shown in figure 4.7.

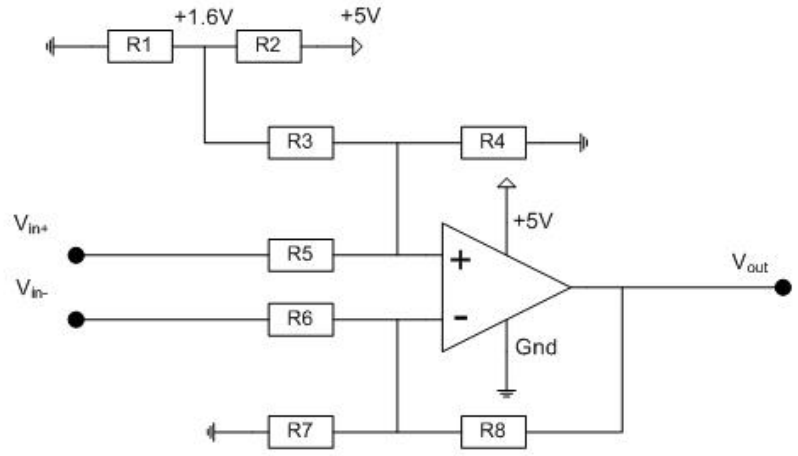


Figure 4.7: Amplifier circuit for the AC voltage scaling

In order to have balanced input signals, R3, R5, R6 and R7 will be equal and R4 will be equal to R8. The amplification factor α will be equal to $\frac{R4}{R5}$.

The resistors R1 and R2 are used as voltage divider in order to obtain 1.6V for re-centering the [-1.6;1.6V] signal around 1.6V.

The output signal of the amplifier follows equation 4.5:

$$\alpha \times (V_{in+} - V_{in-} + 1.6V) = V_{out} \in [0; \alpha \times 3.2V] \tag{4.5}$$

- DC voltage scaling

It was noted in section 4.3.2 that the DC voltage measurement signal will be in the range [0;1.6V]. The signal does not need to be re-centered this time, a simple gain will be sufficient. The figure 4.8 shows the circuit employed.

The resistors R1 and R4 are equal as well as R2 and R3. The amplification factor α will be equal to $\frac{R1}{R2}$. The output signal of the amplifier follows equation 4.6.

$$\alpha \times (V_{in+} - V_{in-}) = V_{out} \in [0; \alpha \times 1.6V] \tag{4.6}$$

The factor α is chosen equal to 1.88 which gives a V_{out} signal between [0;3V].

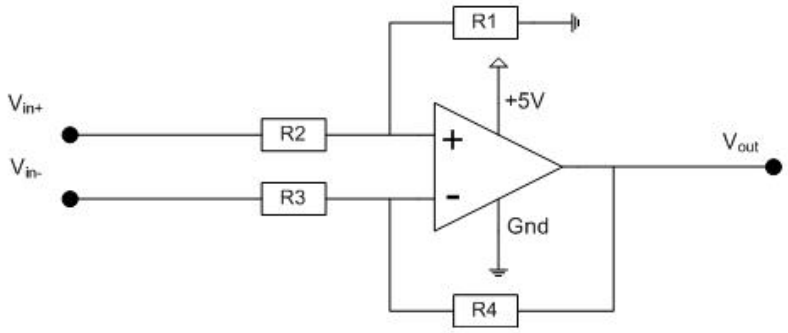


Figure 4.8: Amplifier circuit for the DC voltage scaling

Scaling the current sensing

In section 4.3.2 it has been seen that the correspondence between "measured current" and "output signal" is as following:

- DC current : 0 ... 10A $\longrightarrow$ 1.75 ... 2.5V
- AC current : 10 ... -10A $\longrightarrow$ 1.75 ... 3.25V

These signals have to be scaled for the [0;3V] voltage input range of the ADC.

- AC current scaling

The scaling of the AC current measurement will have to re-center the signal range around 0.75V ([1.75;3.25V] $\longrightarrow$ [0;1.5V]) and then scale the range to [0;3V] with a amplifier circuit gain (α) of 2.

The used amplifier circuit is shown in figure 4.9. Since the current sensor has only one output signal, it is connected on the positive pin of the amplifier. A voltage of 1.75V is obtained with a voltage divider (R5 and R6 on figure 4.9) and is connected to the negative pin of the amplifier.

The resistors R1 and R4 are equal as well as R2 and R3 and bring a amplification factor $\alpha = \frac{R1}{R2}$ of 2.

NOTE: It is important to remember that for the AC current measurement, 0V on the ADC pin corresponds to a current of 10A whereas 3V corresponds to a current of -10A. This is due to the design error mentioned in section 4.3.3.

- DC current scaling

The scaling of the DC current measurement is very similar to the AC current measurement scaling. The range [1.75;2.5V] needs to be shifted to [0;0.75V]. The same circuit

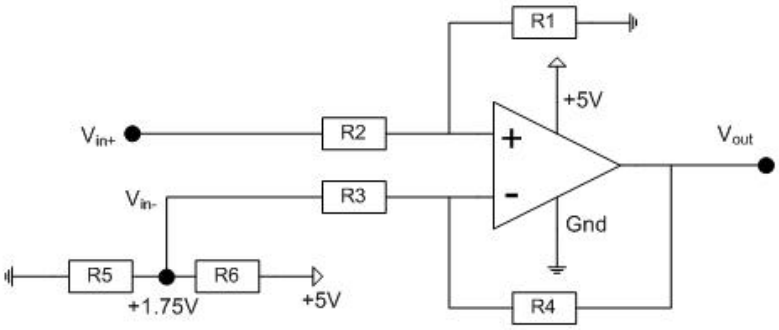


Figure 4.9: Amplifier circuit for the AC current scaling

as shown in figure 4.9 is used. This permits to subtract 1.75V to the DC current measurement signal. Again, R1 and R4 are equal as well as R2 and R3, but this time the amplification factor $\alpha = \frac{R1}{R2}$ is 4.

4.4.3 Tests and corrections

In this section will be listed the different tests and corrections that have been made on the board. The schematic and layout files have also been modified to take into account the corrections and now present a properly working board.

- Test of the power supply of the board

The measured main power supply voltage (from the 7805) is $\approx$ 4.8V which is enough for a correct operation of the IC's of both signal and power board. The measured output current is $\approx$ 0.3A.

The measured output voltage of the REF02 of this device is 4.997V which gives a good enough precision.

NOTE: In order to add protection to the "signal board-to-ADC" connection and limit the current flowing to the ADC, 4 resistors of 4.7kΩ have been added between the amplifiers output signal and the connector to the ADC.

- Test of the DC voltage scaling

The test of the DC voltage scaling reveals an error in the schematic. For the voltage measurements, two signals come out of the isolation amplifier on the power board. Between the 2 signals, the higher one is to be connected to the
+" pin of the amplifier on the signal board. The lowest one is to be connected to the
-" pin of the amplifier. The error was that the two signals were inverted and connected to the wrong pin of the amplifier. The tracks have been scratched and correct wire connections has been made. After correction the DC voltage scaling was correctly working.

- Test of the AC voltage scaling

Testing the AC voltage sensing reveals that there was an error in choosing the resistors R3, R5, R6 and R7 (seen in Figure 4.7). These resistors have the same value as the resistors R4 and R8. Thus the α factor is 1 and not 0.9375 as it should ($[0; 3.2V] \times 0.9375 = [0; 3V]$]). The consequence is that the measured range of the AC voltage is slightly truncated at high values (close to 50V).

NOTE: The resistors have not been changed to a correct value!

- Other tests

The tests of the DC current scaling and the AC current scaling show proper operations. No corrections are needed.

Chapter 5

Control Structure

The control structure of the inverter is detailed in this chapter. Only the theory will be developed. Matlab simulations of the control structure will be studied in chapter 6.

5.1 The Unipolar PWM command

The chosen type of command is a Unipolar PWM command. This type of command permits to switch the mosfets in such a way that the output voltage of the inverter can be equal to the DC input voltage, or it's opposite (V_{DC} or -V_{DC}), but also to 0V.

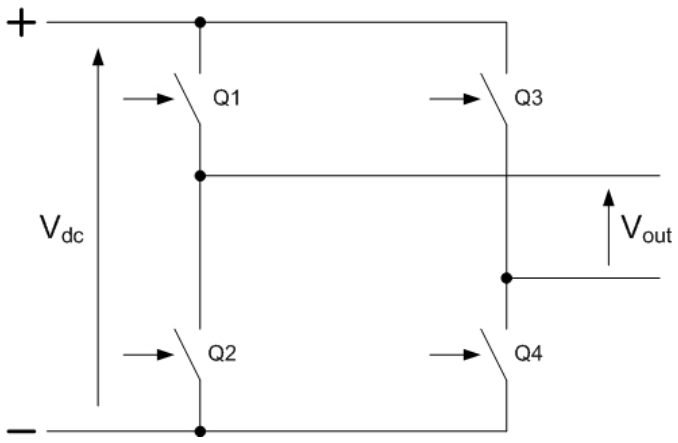


Figure 5.1: Schematic of the 4 mosfets of the inverters

Depending on how the switches in Figure 5.1 are controlled, various output voltage can be obtained:

- Q1 and Q4 are ON , Q2 and Q3 are OFF $\longrightarrow$ $V_{out} = +V_{DC}$
- Q2 and Q3 are ON , Q1 and Q4 are OFF $\longrightarrow$ $V_{out} = -V_{DC}$
- Q1 and Q3 are ON , Q2 and Q4 are OFF $\longrightarrow$ $V_{out} = 0V$
- Q2 and Q4 are ON , Q1 and Q3 are OFF $\longrightarrow$ $V_{out} = 0V$

5.1.1 Generation of the Gate Signals

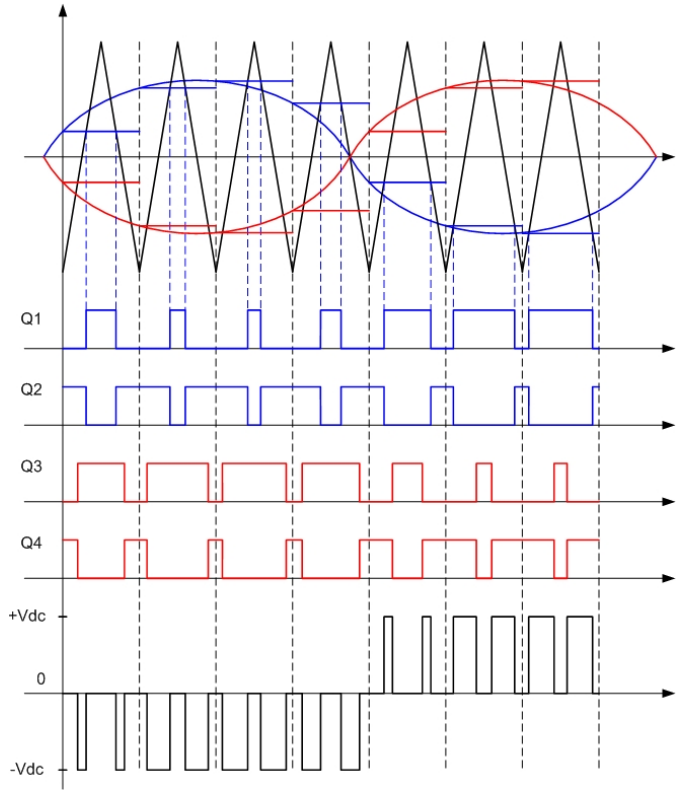


Figure 5.2: Diagram of the gate signal generation logic and the resulting inverters output voltage

The generation of the gate signals is done by comparing an "error" signal with a sawtooth signal. If the sawtooth carrier signal is superior to the error signal, the gate signal is "high", if it is inferior to the error signal, the gate signal is "low".

The error signal is a rough sinusoidal running at 50Hz (see section **5.2**) whereas the sawtooth signal is running at 20kHz.

Below are the rules for generating the gate signals of each switches:

- Gate signal of Q1 ⟶ comparison between the error signal and the sawtooth signal
- Gate signal of Q2 ⟶ opposite of gate signal of Q1
- Gate signal of Q3 ⟶ comparison between the opposite of the error signal and the sawtooth signal
- Gate signal of Q4 ⟶ opposite of gate signal of Q3

A diagram of the switching logic of the switches is shown in Figure 5.2. The blue sinusoidal is the original error signal while the red sinusoidal is it's constructed opposite. The blue error signal is used for switching the firs leg of the inverter (Q1 and Q2) while the red error signal is used for the second leg of the inverter (Q3 and Q4).

NOTE: The ratio between the error signal frequency and the sawtooth signal frequency has not been respected in Figure 5.2 in order to make an understandable schematic. The sawtooth frequency should be much higher, thus making a much more progressive PWM.

5.2 The Control Loop

The inverter will be connected to the grid which can be seen as an ideal AC voltage source. Therefore the voltage at the output of the inverter does not need to be controlled. The inverter only possesses a current control loop.

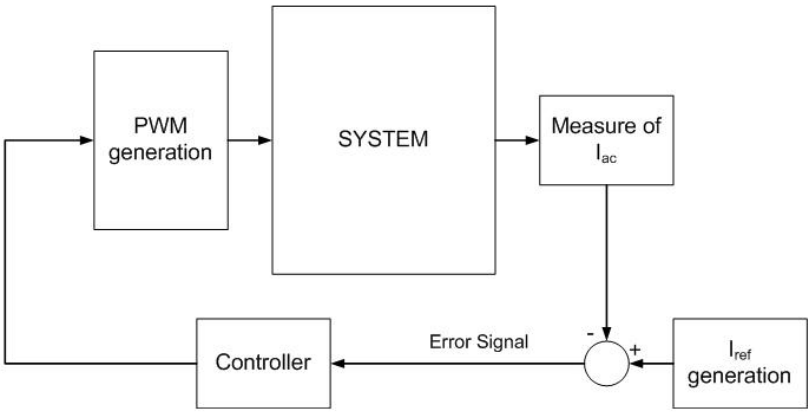


Figure 5.3: Control loop of the inverter

The current control loop (shown in Figure 5.3) consists of the following parts:

- The generation of a "reference current", I_{ref}

- The comparison between I_{ref} and the measured AC current, I_{ac}, giving the control "error signal"
- A control made on this error signal
- The feeding of the error signal to the PWM generator (comparison between the error signal and the sawtooth signal (see description in section **5.1.1**)

The reference current is an ideal sinusoidal signal created with the phase of the grid voltage, V_{dc}, and an amplitude value. This control permits to feed only active power to the grid since the injected current will be in phase with the grid voltage. The control of the amplitude value is necessary if MPP tracking is used.

Chapter 6

Simulations and Results

Matlab and Simulink have been used for running system simulations with the help of the Plecs toolbox which permits to simulate electrical circuit.

6.1 Plecs Circuit

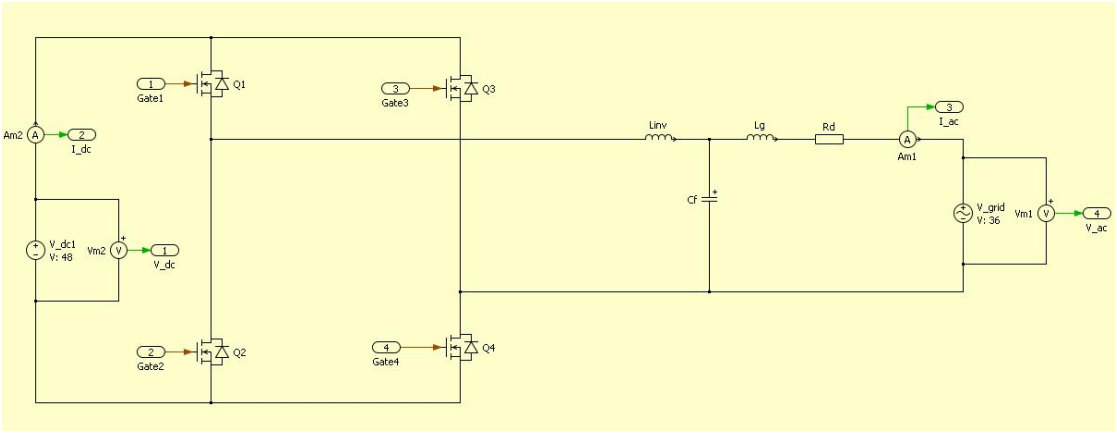


Figure 6.1: Plecs circuit used in the simulations

The Plecs circuit used in the simulation (see Figure 6.1) consists of the following components:

- A DC voltage source (ideal representation of the Solar panels + DC link)
- 4 ideal Mosfets composing the full-bridge inverter
- The LCL filter and a damping resistor
- A AC voltage source (ideal representation of the grid)

- 2 Ammeter and 2 voltmeter for measuring V_{dc}, V_{ac}, I_{dc} and I_{ac}

NOTE: The transformer is not represented in the simulation. Instead, the grid voltage is lowered to the secondary voltage value of the transformer: 36V.

6.2 LCL Filter Simulation

The LCL filter calculations are based on the work presented in [1].

```
% System parameters
Pn = 150;          %Inverter power: 150 W
En = 36;           %Grid voltage: 36 V
fn = 50;           %Grid frequency: 50 Hz
wn = 2*pi*fn;
fsw = 20000;       %Switching frequency: 20000 Hz
wsw = 2*pi*fsw;

% Base values
Zb = (En^2)/Pn;
Cb = 1/(wn*Zb);
Lb = Zb/wn;

% Tolerable decrease of power factor
x = 0.027;

% Ripple reduction
reduction = 0.1;

% Filter parameters
Linv = 0.006       %Inverter side inductance
Cf = x*Cb          %Filter capacitor

% Calculation of the factor, r, between Linv and Lg
[r]=r_calculation(reduction,Linv,Cb,wsw,x)

%Grid side inductance (including transformer inductance)
Lg = r*Linv

% Calculation of wres, resonance frequency of the filter
wres = sqrt((Linv+Lg)/(Linv*Lg*Cf));
% Impdedance of the filter capacitor at resonance frequency
Zc_sw = 1/(wres*Cf);

%Damping resistance
Rd = 0.33*Zc_sw
```

Listing 6.1: Matlab code for calculation of the filters parameters

Listing 6.1 shows the code used for determining correct values for the filters components L_{inv} (inverter side inductance), C_f (filter capacitor), L_g (grid side inductance), and R_d

(damping resistor).

The values for the LCL filter components found with the Matlab code are the following:

- L_{inv}: 6mH
- L_g: 43μH
- C_f: 13μF
- R_d: 0.6 Ω

L_{inv} is chosen with the desired current ripple on the inverter side, [1].

The simulation model used for determining the values of the filters parameters is a simplified control model: *a*) the modulation index is created by taking the difference between an ideal 50Hz sinusoidal (representing I_{ref}) and the measured AC current, *b*) no control is made on the error signal and *c*) the connection to the grid is removed and replaced by a resistive load. The schematic of the model can be found in Appendix A.

The DC voltage is 48V, the amplitude of I_{ref} is fixed to 4A and the load is 5Ω. The expected voltage amplitude is therefore 20V. The result are shown in Figure 6.2.

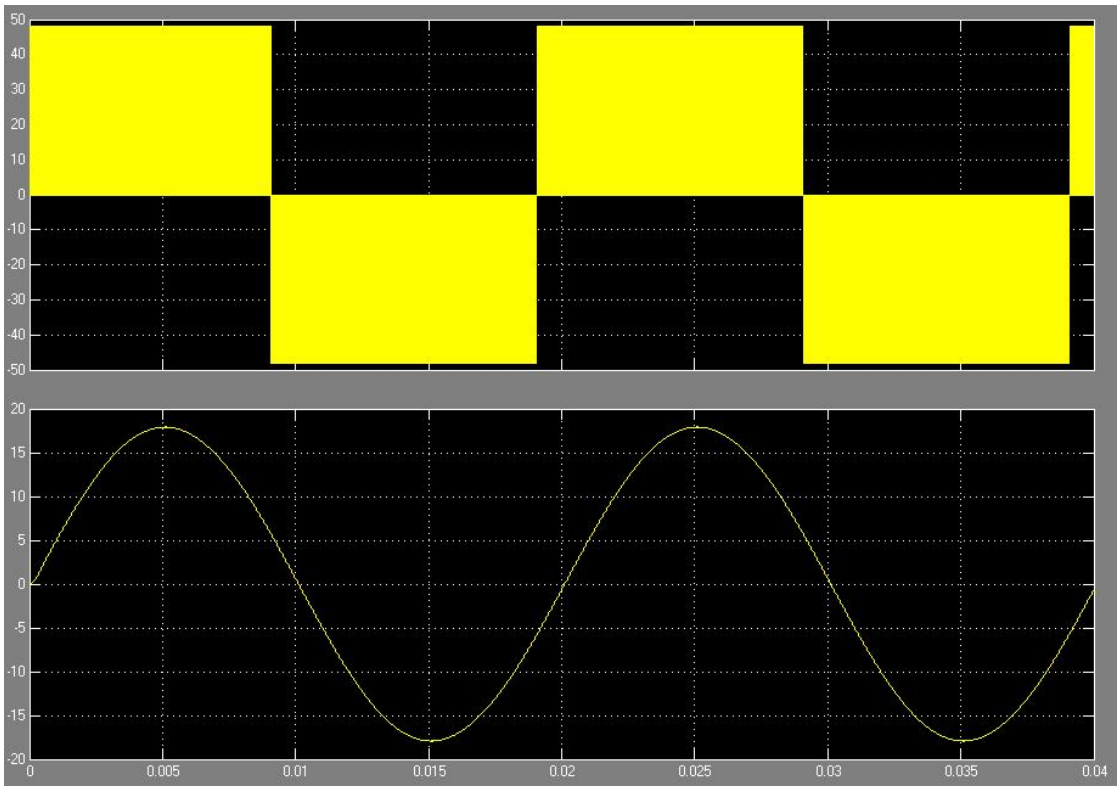


Figure 6.2: "Before filter" output voltage and "After filter" output voltage

The voltage is lower than expected ($\approx$ 18V) because no controller is added to this simulation model. Therefore there is a gain error between the reference current and the measured AC current. But the inverters output voltage is successfully filtered to a 50Hz sinusoidal demonstrating the correct tuning of the filters parameters.

6.3 Complete System Model

The following sections show the obtained results when simulating the complete system with 3 different type of control on the feedback of the current control loop.

6.3.1 No Controller: Complete_model_1.mdl

Figure 6.3 shows the model used in the simulation of the entire system without any control on the feedback.

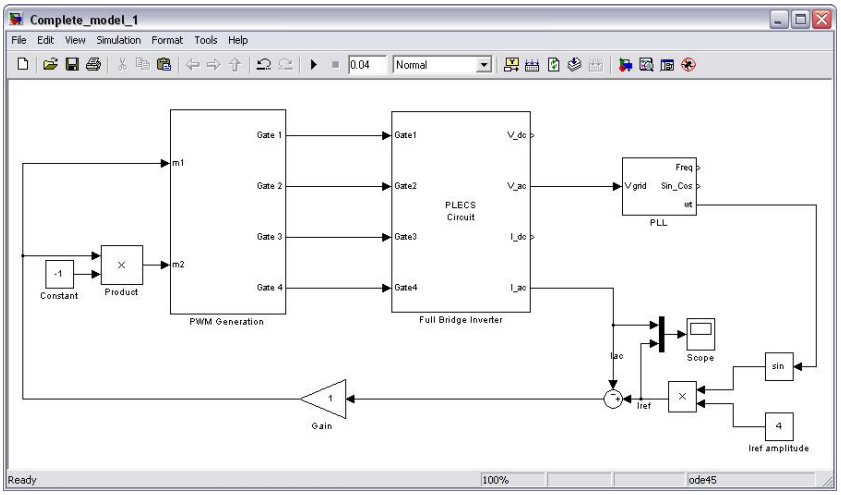


Figure 6.3: Simulink model of the complete system without any control on the feedback

Figure 6.4 shows that without any control, a static error is present between the current reference and the AC current.

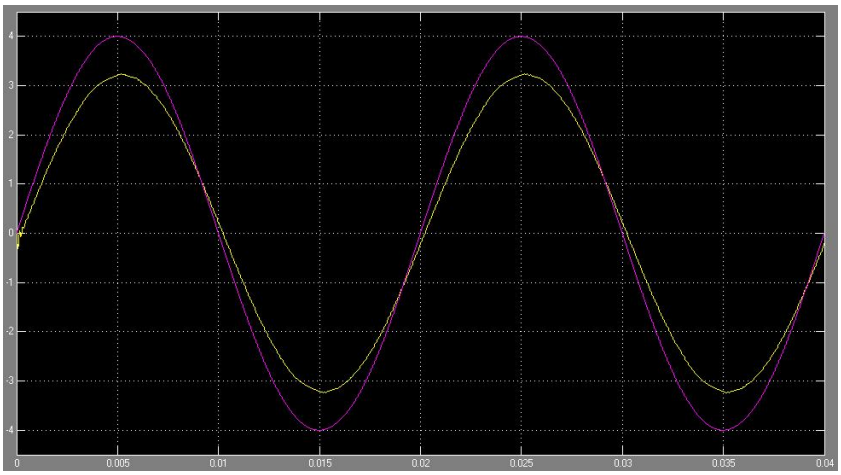


Figure 6.4: Simulation of model Complete_model_1.mdl: reference current (purple) and measured AC current (yellow)

6.3.2 P Controller: Complete_model_2.mdl

In this model (Figure 6.5), a simple P controller is added to the feedback.

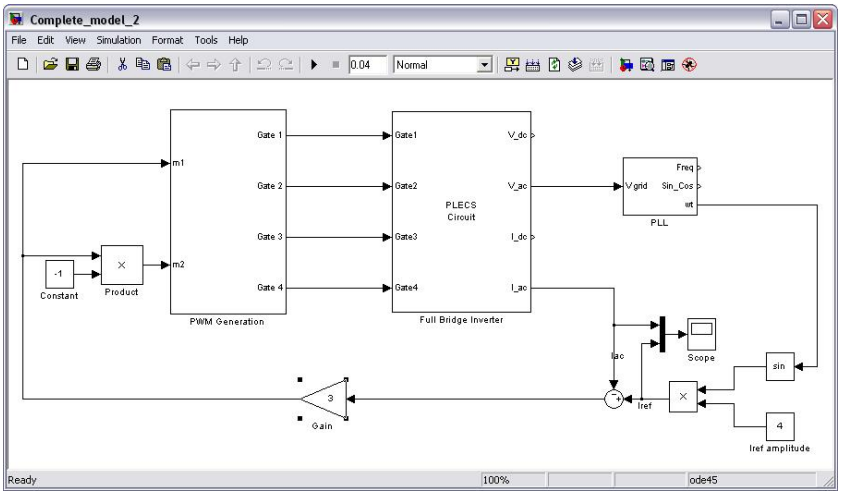


Figure 6.5: Simulink model of the complete system with a P controller on the feedback

Figure 6.6 shows that the static error is decreased but is not yet equal to zero. A further increase of the gain value of the P controller leads to high frequency oscillations around the desired value which is not desirable.

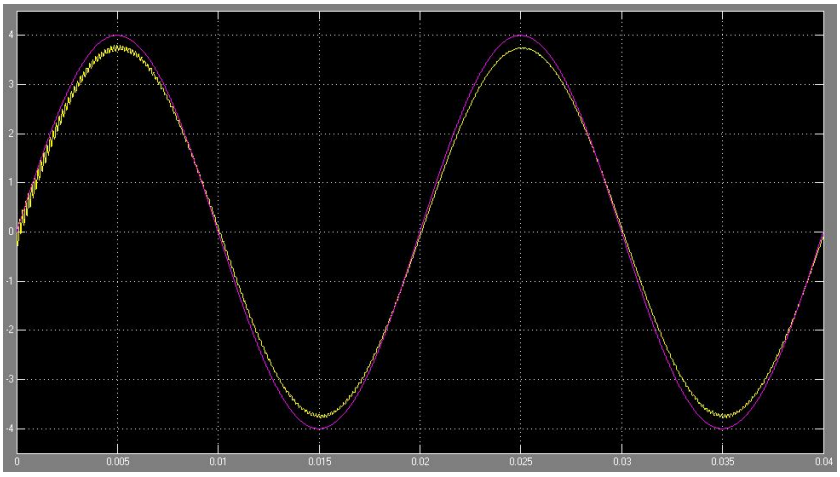


Figure 6.6: Simulation of model Complete_model_2.mdl: reference current (purple) and measured AC current (yellow)

6.3.3 PI Controller: Complete_model_3.mdl

In the model of Figure 6.7, a PI controller replaces the P controller.

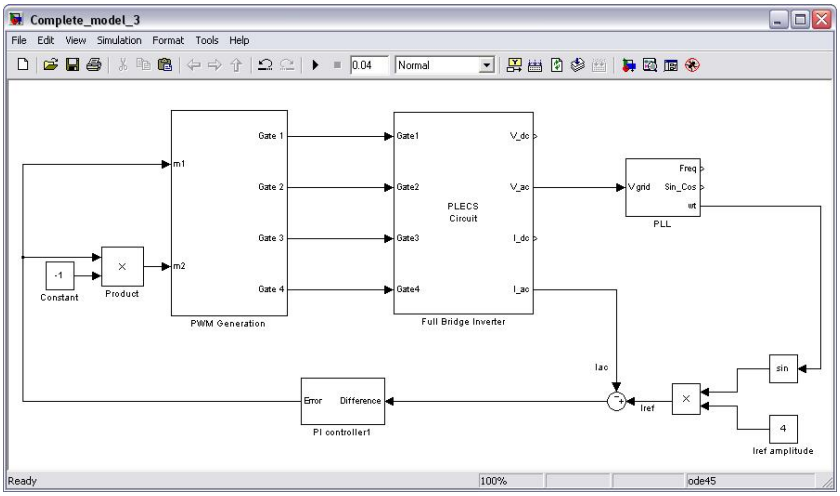


Figure 6.7: Simulink model of the complete system with a PI controller on the feedback

Figure 6.8 shows that the static error is completely gone now, but a very small phase shift is now present. Since no precise calculations for designing the PI controller has been made (the controller values were found by running Matlab simulations), a better tuning of the PI can decrease further this phase error. The measurement of the time delay gives 0.0002 seconds, which corresponds to a phase shift of $\frac{\Pi}{50}$ which already gives a power factor very close to 1.

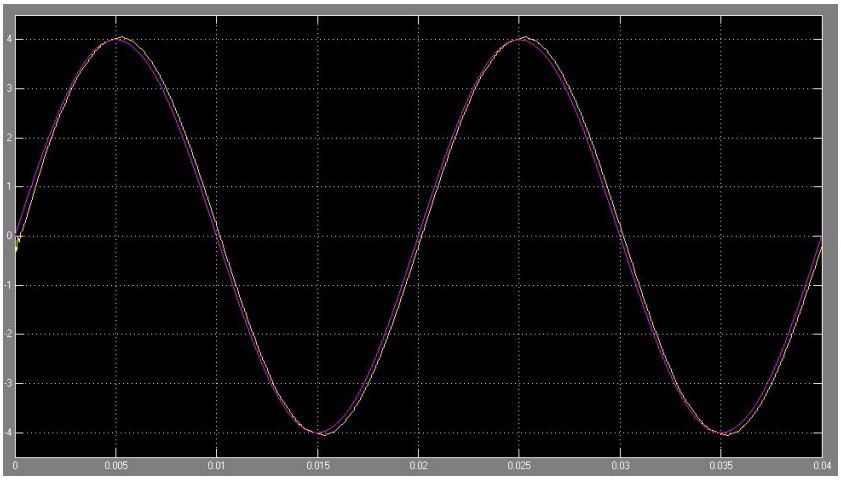


Figure 6.8: Simulation of model Complete_model_3.mdl: reference current (purple) and measured AC current (yellow)

Chapter 7

Softwares: Control Models

The different test softwares of the inverter are described in this chapter. The PWM generation and the ADC conversion were tested independently. Once they are correctly working, open loop and closed loop control models can be built.

7.1 PWM Test Model: Test_PWM.mdl

The Simulink model of the PWM test software is shown in Figure 7.1. The main parameters of the ePWM blocks and their configuration are shown below:

NOTE: This is a valid configuration which ensures synchronization of the PWM signals, inversion between 2 PWM signals of the same leg, and deadbands.

- **"General" tab parameters (for both blocks ePWM and ePWM1):**
  - Counting mode: Up-Down (sawtooth signal)
  - Timer period: 2500 clock cycles (meaning 2500 "Up" counts plus 2500 "Down" counts, the clock being 100Mhz, 5000 clock cycles corresponds to a frequency of 20kHz for the sawtooth signal)
  - For block ePWM:
    - Sync output selection: CTR = Zero, synchronization done when counter equals zero.
  - For block ePWM1:
    - Sync output selection: Disable
    - Phase offset source: Specify via dialog

    - Phase offset value: 0

- **"ePWMA" tab parameters:**
  - For Block ePWM:
    - CMPA Source: Input port, the compare value for module A (it will be the modulation index)
    - Action when counter = CMPA on CAU: Clear. When the **C**ounter **A** counts **U**p (CAU) and equals CMPA, the output is "Cleared" low
    - Action when counter = CMPA on CAD: Set. When the **C**ounter **A** counts **D**own (CAD) and equals CMPA, the output is "Set" high
  - For Block ePWM1:
    - CMPA Source: Input port, the compare value for module A (it will be the modulation index)
    - Action when counter = CMPA on CAU: Set
    - Action when counter = CMPA on CAD: Clear
- **"ePWMB" tab parameters:**
  - For block ePWM:
    - CMPB Source: Specify via dialog, only the compare value for module A (CMPA) is used
    - Action when counter = CMPA on CAU: Set
    - Action when counter = CMPA on CAD: Clear
  - For block ePWM1:
    - CMPB Source: Specify via dialog, only the compare value for module A (CMPA) is used
    - Action when counter = CMPA on CAU: Clear
    - Action when counter = CMPA on CAD: Set
  - **"Deadband unit" tab parameters (for both blocks ePWM and ePWM1):**
    - Deadband polarity: AHC, Active High Complementary
    - Signal source for RED: ePWMxA
    - Signal source for FED: ePWMxA
    - RED and FED deadband period: 100
  - **"Event Trigger" tab parameters (for ePWM block only):**

* Enable ADC start module A: Checked
* Number of event for SOCA to be generated: First event
* Module A counter match condition: CTR = Zero (starts an ADC conversion when counter A equals zero)

NOTE: For more information on the configuration of the blocks, refer to the block help or to the "ePWM Module Reference Guide" of Texas Instruments.

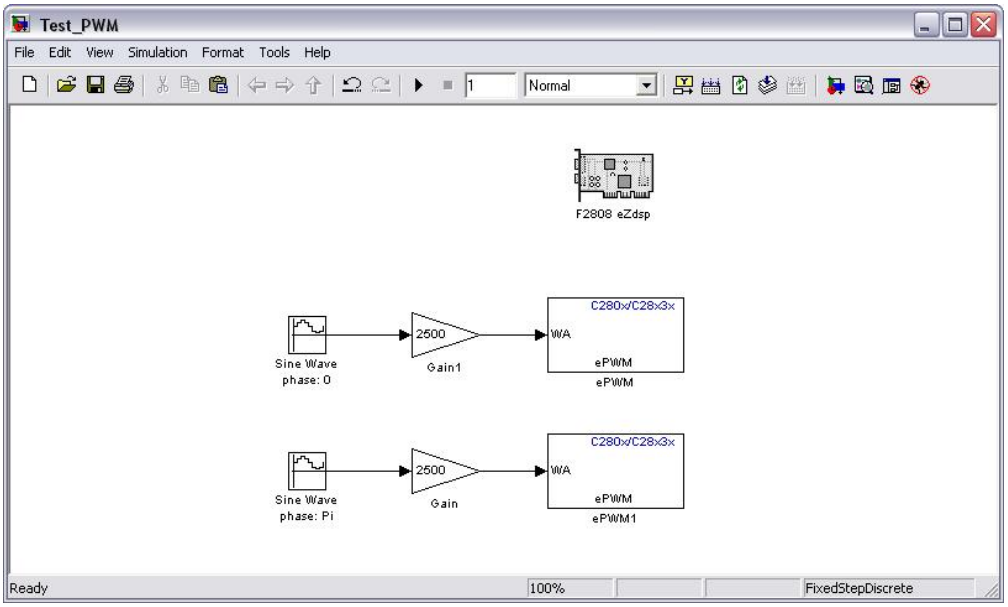


Figure 7.1: Simulink Model for the test of the PWM generation

7.2 ADC Test Model: Test_ADC.mdl

The Simulink model of the ADC software is shown in Figure 7.2. The main parameters of the ADC block and their configuration are shown below:

- **"ADC Control" tab parameters:**
  - Module: A and B
  - Conversion mode: Simultaneous (samples the channels A and B at the same time)
  - Start of conversion: ePWMxA
  - Sample time: 0.00005 (this value is needed, even though it is not used)
  - Data type: double

- **"Input Channels" tab parameters:**
  - Number of conversions: 2
  - Conversions no. 1 and 2: ADCINA4 and ADCINB4 (name of the physical pins to which the measured signals are connected)
  - Conversions no. 3 and 4: ADCINA5 and ADCINB5
  - Use multiple output ports: Checked

NOTE: For more information on the configuration of the blocks, refer to the block help or to the "ADC Module Reference Guide" of Texas Instruments.

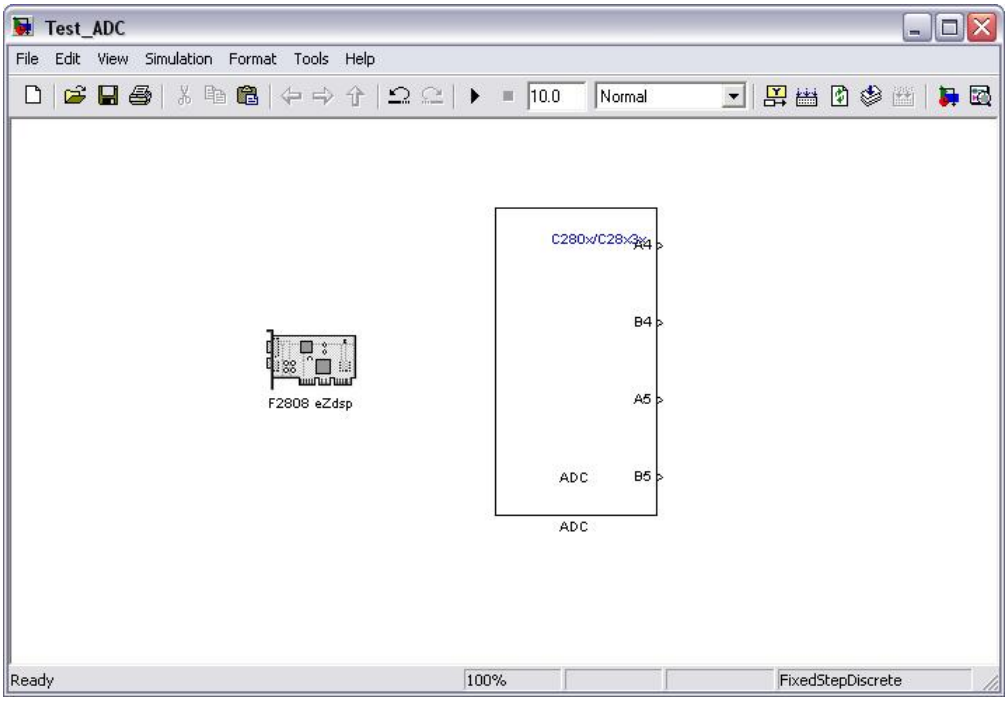


Figure 7.2: Simulink Model for the test of the ADC block

To check that the ADC is correctly working, the use of the watchdog window in CCS is required. It allows to watch the following registers: ADCRESULT0, ADCRESULT1, ADCRESULT2 and ADCRESULT3 which respectively correspond to the AD conversion of the followings signals: V_{ac}, V_{dc}, I_{ac} and I_{dc}.

The digital value of the input analog voltage that is obtained at the output of the ADC block in the model is derived by:

- Digital value = 0 when input $\leq$ 0V
- Digital value = $4096 \times \frac{Input\ Analog\ Voltage - ADCLO}{3}$ when 0V $\leq$ input $\leq$ 3V (ADCLO is approximately 0; the exact value is not necessary to know since calibration will

be made between the measured voltages and currents and the ADC results)

- Digital value = 4095 when input $\geq$ 3V

NOTE: The values in the register seen in the watchdog window are different from the output of the ADC block in the model, they are multiplied by 16 and are therefore comprised between 0 and 65520.

A transformation has to be made at the output of the ADC in order to convert the digital values back to real values and use them in the control. Calibration tests have been carried out in section **8.3** where the determination of the transformation equations is explained.

7.3 Closed Loop Control Software

7.3.1 First model: Test_closed_loop_1.mdl (Inverter not connected to grid)

The first model of the closed loop control will only be using the measured value of I_{ac} in order to verify that the loop is correctly closed (see Figure 7.3).

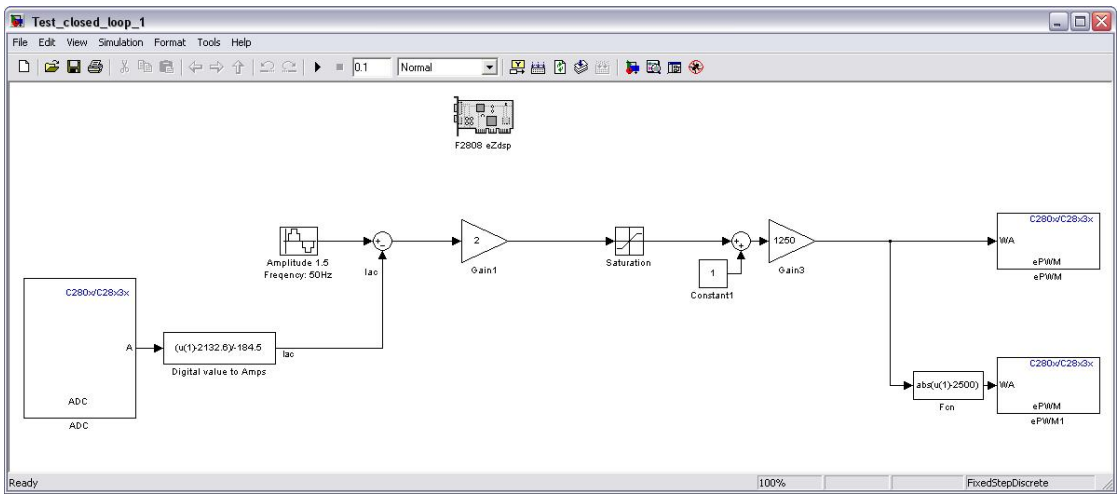


Figure 7.3: First Simulink model for the test of the closed loop control

The reference current is generated by an ideal sinusoidal. The error (I_{ref}-I_{ac}) is then driven into a P controller (gain of 2). A saturation block is placed at the output of the P controller. The saturation limits are -0.9 and 0.9 and prevent the modulation index from being too high and the mosfets to be "ON" for an entire period.

The next blocks are used to shift and scale the modulation index for the ePWM block. Indeed, the ePWM block sawtooth carrier signal is a counter counting 2500 times up and

2500 times down. The modulation index (which will correspond to the value CMPA) must therefore be between 0 and 2500. The controlled error signal coming out of the PI is restricted to [-0.9;0.9]. The addition of a constant equal to 1 shifts this error signal to [0.1;1.9], and a gain of 1250 scales it to [125;2375].

NOTE: The datasheet of the ePWM block states that for a deadband period being set to 100 for a DSP clock of 100MHz this corresponds to a "real" deadband period of 1μs, or 100 clock cycles. Therefore the maximum saturation limits can be [-0.92;0.92]. Otherwise there is a possibility that a Mosfet stays "ON" for an entire period and damages the bootstrap circuit.

7.3.2 Second model: Test_closed_loop_2.mdl (Inverter not connected to grid)

The second closed loop control test is similar to the first closed loop control test except that it includes a PI controller instead of a simple gain. The PI controller comes from the Matlab simulation of the whole system presented in section **6.3**.

Figure 7.4 shows the control model.

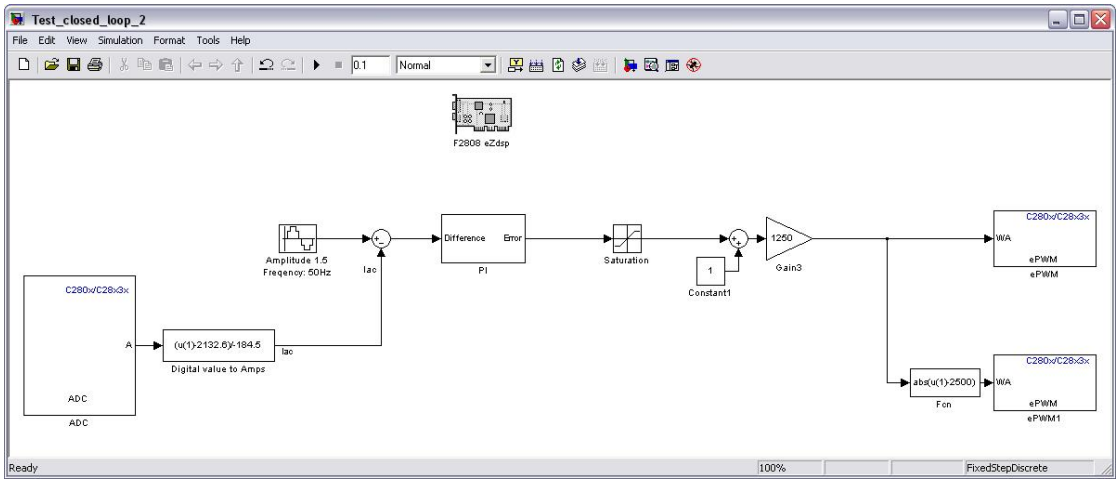


Figure 7.4: Second Simulink model for the test of the closed loop control

7.3.3 Third Model: Test_open_loop_1.mdl (Inverter not connected to grid)

In this model (Figure 7.5) a loop with the AC voltage measurement is tested. The measured V_{ac} (which is known to have a peak value of 28.8V) is scaled down to a signal between -1 and 1, thus the "division by 30" block. This scaled down voltage measurement is then directly used as a modulation index for the PWM blocks.

The 3 other "digital value-to-real value" transformation blocks are shown in this model but are not used.

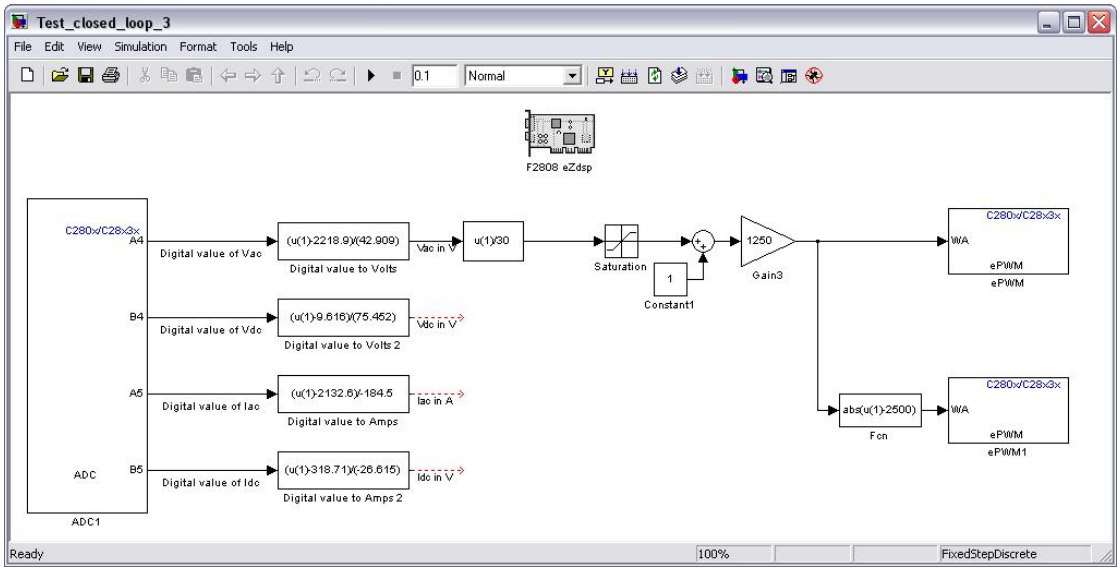


Figure 7.5: Firs Simulink model for the test of an open loop control

7.3.4 Fourth Model: Test_open_loop_2.mdl (Inverter not connected to grid)

With this model we want to use a PLL to obtain the phase of the grid voltage and use it to create a current reference that can later be used in a current control loop.

The "Discrete 1-phase PLL" block of the SimPowerSystems toolbox is used as shown in Figure 7.6. The output of the PLL is the ramp w×t varying between 0 and 2×pi. The sinus of this ramp multiplied by a desired amplitude gives the reference current I_{ref} which is then directly fed to the PWM block as a modulation index. In this test the current amplitude can not really be fixed since the saturation block will limit it to [-0.9;0-9], it is therefore fixed to 1.

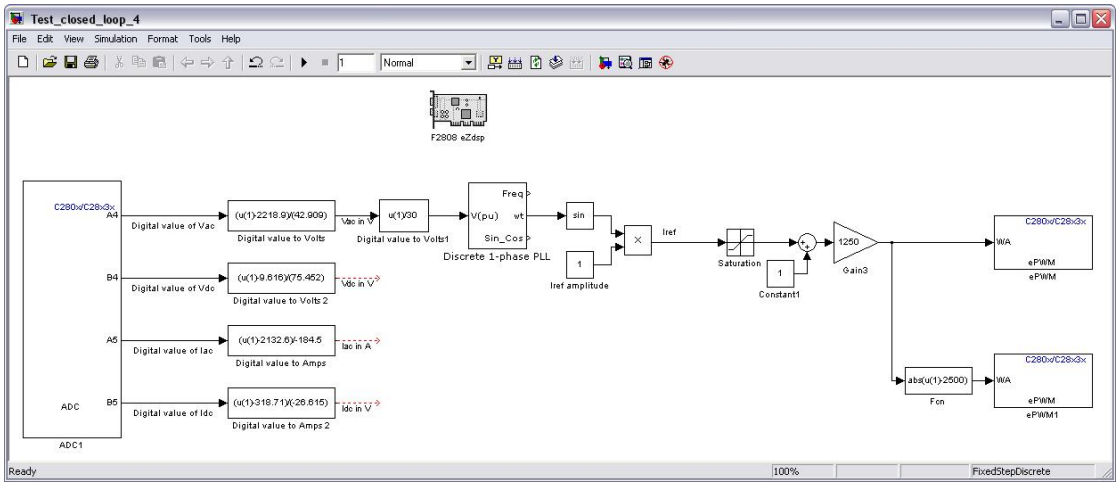


Figure 7.6: Second Simulink model for the test of an open loop control

7.3.5 Fifth Model: Test_closed_loop_3.mdl (Inverter connected to grid)

The fifth test model (see Figure 7.7) is a closed loop model using the measurement of V_{ac} and I_{ac} to generate a current injected to the grid which is in phase with the grid voltage. The reference current is generated with V_{ac}'s phase and a reference amplitude before being compared to the actual measured I_{ac}. The error between the reference signal and the measured signal can then be controlled with a PI controller.

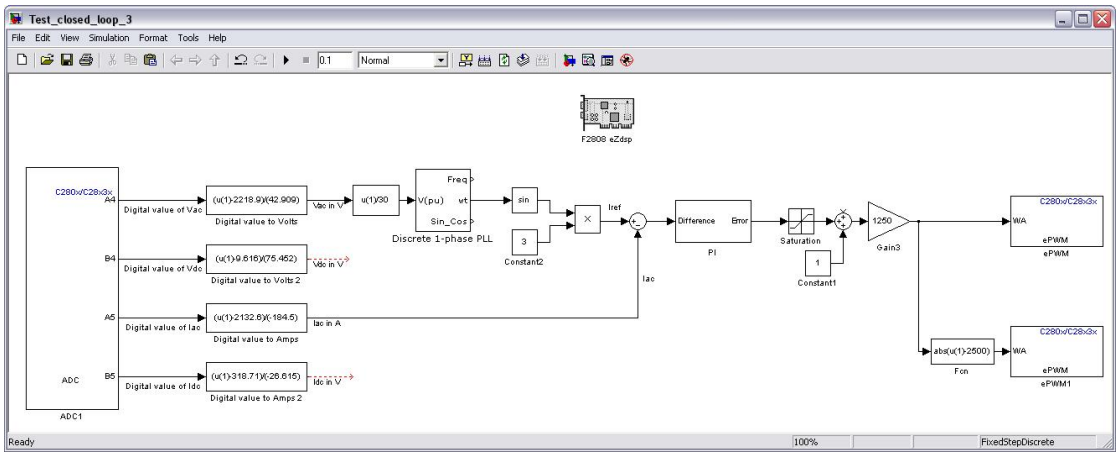


Figure 7.7: Second Simulink model for the test of a closed loop control

Chapter 8

Tests and Measurements

The results of the different tests carried on the inverter are presented in this chapter.

8.1 PWM Generation

The PWM generation is tested with the model shown in section **7.1**.

Figure 8.1 shows 2 scope screen captures of the 4 PWM signals at the output of the DSP generated by the model shown in Figure 7.1. PWM signals for Q1, Q2, Q3 and Q4 are shown from top to bottom. It can be seen that Q2 is the opposite of Q1 (and Q4 the opposite of Q3). Furthermore, the 4 signals are correctly synchronized.

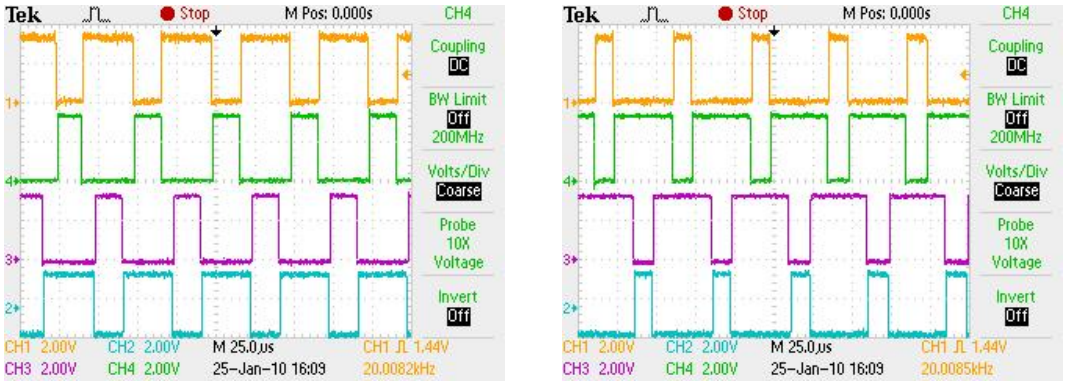


Figure 8.1: 3 examples of the 4 generated PWM signals

Figure 8.2 is a time zoom of Figure 8.1 which shows the generated deadbands that prevents short-circuiting the Mosfets.

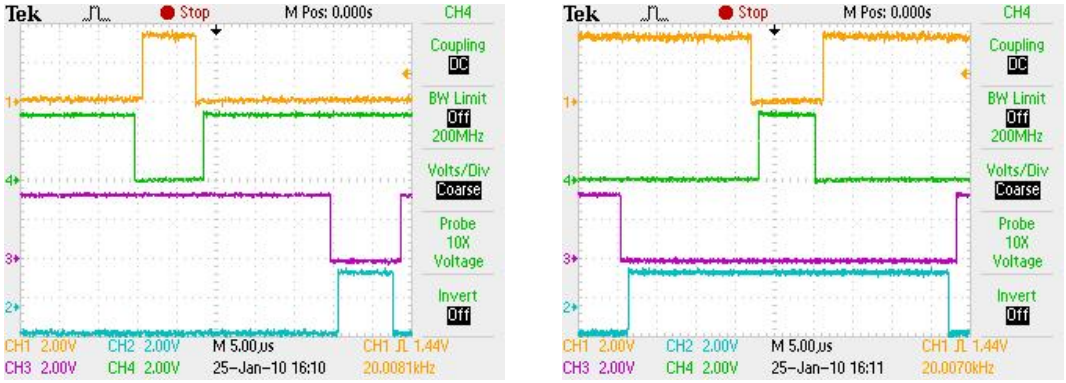


Figure 8.2: 2 examples of the 4 generated PWM with their respective deadbands

8.2 LCL Filter

The LCL filter is tested with the PWM generation test model. There is no closed loop control. The aim is to verify the correct filtering of the LCL filter.

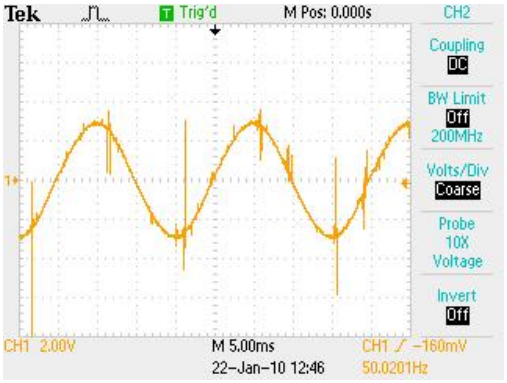
Components with values found in section **6.2** were not easy to find or order. However, a 11mH inductance, a 100μH inductance and a 10μF capacitor were available. A Matlab simulation with these new filter components values show that the filtering is correct. These components are therefore used in the built system.

No connection to the grid is made yet. The output of the filter is only connected to a resistive load.

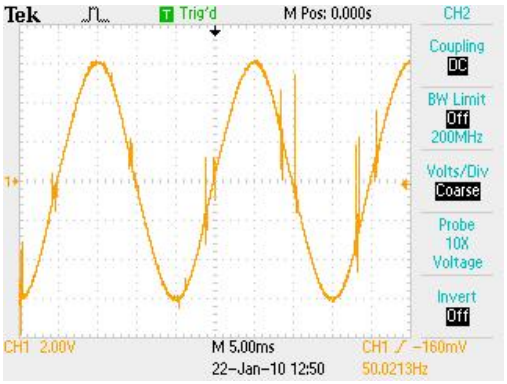
Conditions of the test:

- $V_{dc} = 20V$
- Open loop control with an ideal sinusoidal modulation index

The noise observed on the filter's output voltage comes from the switching command. The 50Hz sinusoidal output voltage, as well as the AC current, changes with the resistive load (see Figure 8.3).



(a) R≈3.5Ω and measured I_{ac}=0.83A



(b) R≈17Ω and measured I_{ac}=0.35A

Figure 8.3: LCL filter output voltage with 2 different loads

8.3 AD Conversion Calibration

The AD converter can be tested independently. The model described in section **7.2** is used. Successively DC voltage, AC voltage, DC current and AC current measurements are tested and calibrated.

NOTE: AC voltage and current measurement do not necessarily need to be AC values. In fact it is easier to check that the AD conversion is correct with DC values.

In the following sections tables containing the measured real values and their digital correspondence (in both watchdog window and ADC block output) of V_{dc}, V_{ac}, I_{dc} and I_{ac} can be found. Figures 8.4 to 8.7 plots their relation. The linearization function of Excel gives the linearized equation of each calibration measurement. It is this linearized equation that is used in the control model to transform the digital values back to their real values. The linearized equations of each curve figure at the bottom left of the plots.

DC voltage calibration

Vdc (V)	ADC - Watchdog value	ADC block output
6,158	7600	475
15,42	18752	1172
36,05	43680	2730

Table 8.1: ADC results of the DC voltage measurements

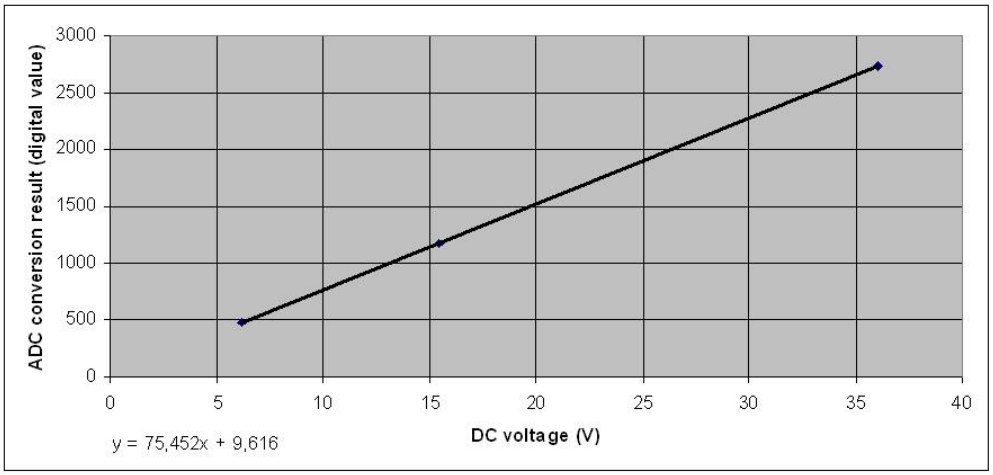


Figure 8.4: ADC Conversion result for different DC voltages

AC voltage calibration

Vac (V)	ADC - Watchdog value	ADC block output
-36,04	10800	675
-20,15	21650	1353,125
-10,1	28600	1787,5
0,002	35400	2212,5
10,13	42500	2656,25
20,75	49700	3106,25
36,04	60300	3768,75

Table 8.2: ADC results of the AC voltage measurements

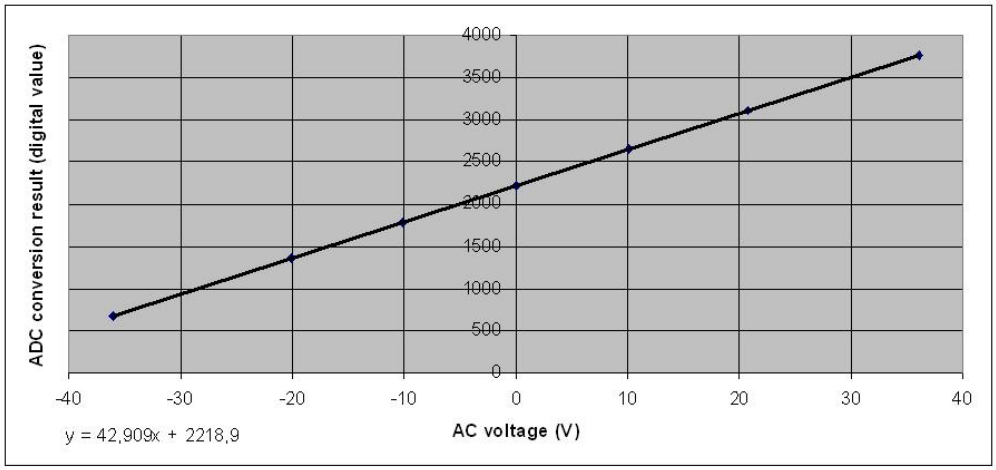


Figure 8.5: ADC Conversion result for different AC voltages

DC current calibration

Idc (A)	ADC - Watchdog value	ADC block output
0	5136	321
0,54	4848	303
1,03	4640	290
3,03	3808	238
5,07	2944	184
6,12	2496	156

Table 8.3: ADC results of the DC current measurements

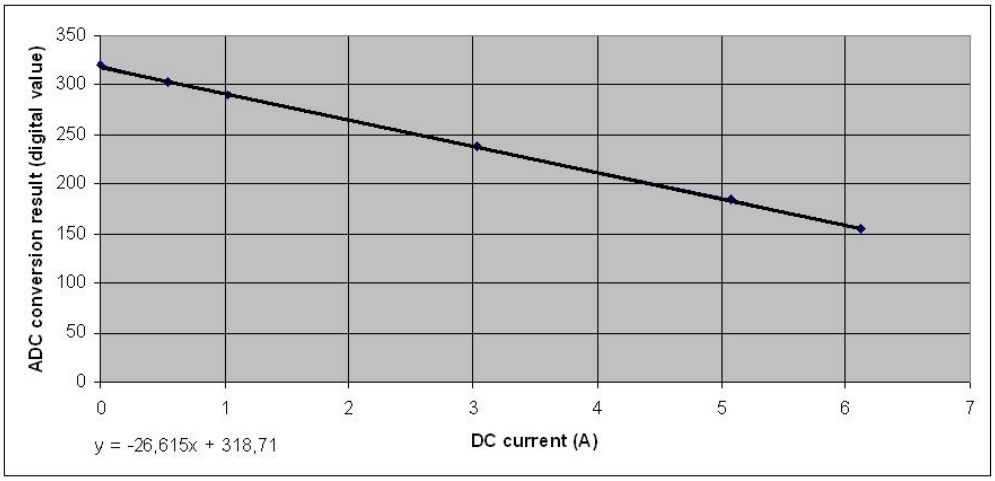


Figure 8.6: ADC Conversion result for different DC currents

AC current calibration

Iac (A)	ADC - Watchdog value	ADC block output
-6,15	52288	3268
-5,07	49104	3069
-3,04	43088	2693
-1,07	37264	2329
-0,65	36060	2253,75
0	34112	2132
1,11	30816	1926
3,07	25040	1565
5,01	19344	1209
6,12	16080	1005

Table 8.4: ADC results of the AC current measurements

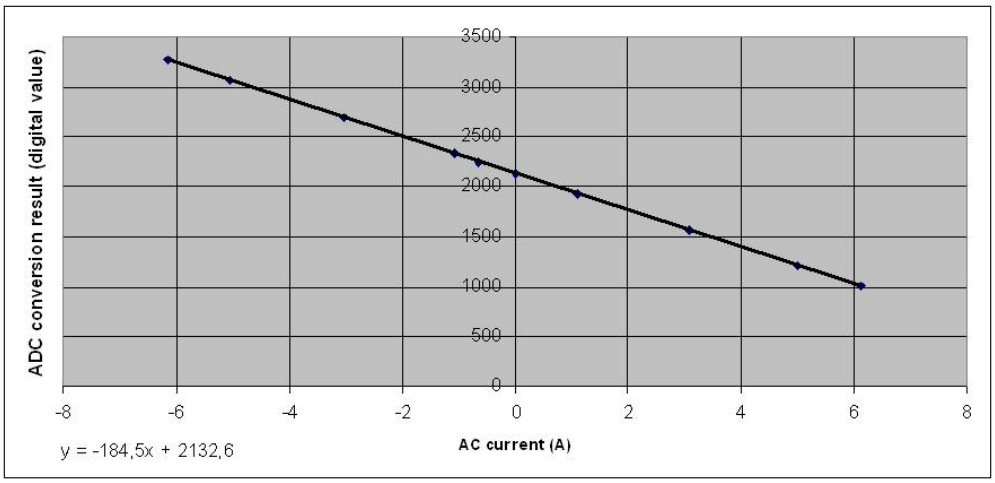


Figure 8.7: ADC Conversion result for different AC currents

8.4 Closed Loop Control

Since every step of the system (PWM generation, inverter switching and filtering and ADC measurements) have been tested and are correctly working, simple closed loop control tests can be made.

8.4.1 First Closed Loop Control Test (Inverter not connected to grid)

The closed loop control model Test_closed_loop_1.mdl described in section **7.3.1** is used here. This model is a current control loop which has an ideal current reference of 1.5A of amplitude.

For this test the connection to the grid is not made. Instead a resistive load is connected. The test shows the good measurement of the AC current and it's use in a simple closed current control loop.

Table 8.5 shows the measurements of I_{dc}, V_{ac} and I_{ac} in RMS value for 2 different resistive load (R) values. In addition the DC and AC powers are calculated. The value of V_{dc} is set to 25V and the measurements are made once for R=5Ω and once for R=10Ω.

It can be seen that the DC and AC power are roughly equal, showing a good power transfer, but more importantly, that under varying load, the system adapts the AC voltage in order to keep a constant AC current. Furthermore the value of 1.05A RMS is to be multiplied by $\sqrt{2}$ (in order to obtain the amplitude of the current) which gives 1.48A. The current control loop is therefore correctly working since the reference current of the model has an amplitude of 1.5A.

		V (V RMS)	I (A RMS)	P (W)
R=10W	DC	25,00	0,45	11,25
	AC	10,61	**1,05**	11,14
R=5W	DC	25,00	0,24	6,00
	AC	5,30	**1,05**	5,57

Table 8.5

8.4.2 Second Closed Loop Control Test (Inverter not connected to grid)

Model Test_closed_loop_2.mdl described in section **7.3.2**: the results show that the control is improved: the signals are less noisy and the system is much more silent. However a fine tuning with a proper PI tuning method of the PI has not been made. Therefore no significant results are displayed here.

8.4.3 First Open Loop Control Test (Inverter not connected to grid)

The open loop control model Test_open_loop_1.mdl described in section **7.3.1** is used here. The direct utilization of the "measured V_{ac}" signal makes a sort of simple phase synchronization.

The observed signals are shown in Figure 8.8.

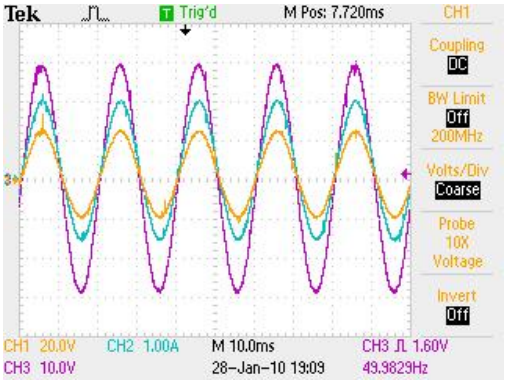


Figure 8.8: AC voltage on the inverter side of the transformer (green), voltage at the output of the filter/across the load (yellow) and the current through the load (blue)

The output voltage of the inverter (after the filter) is well synchronized to the grid voltage and well filtered.

8.4.4 Second Open Loop Control Test (Inverter not connected to grid)

The Test_open_loop_2.mdl model is used for testing the Discrete PLL block of the SimPowerSystems toolbox. It appears during the test that this control does not work. As seen on Figure 8.9 the inverter's output voltage (and current) has a frequency of 12.5Hz, one fourth of the desired frequency. The PLL block seems to have a wrong configuration. But this block (part of the Extra Library of the SimPowerSystems toolbox) does not have any documentation. No configuration solution has been found in order to make this block work.

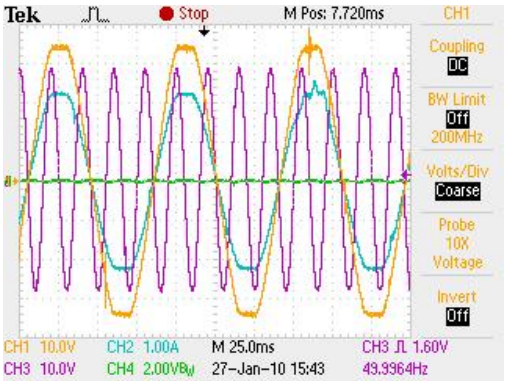


Figure 8.9: AC voltage on the inverter side of the transformer (purple), voltage at the output of the filter/across the load (yellow) and the current through the load (blue)

8.4.5 Third Closed Loop Control Test (Inverter connected to grid)

The model Test_closed_loop_3.mdl never worked properly. No significants results can be shown for this model.

8.5 Known Errors

The tests of the whole system revealed new design errors that could not have been seen in previous tests. Some of the problems have been partially corrected while others remain unsolved.

Filter capacitors of the operational amplifiers on the signal scaling board: Partially corrected

The capacitors named C1 and C2 (see schematic of the signal scaling board in Appendix A) are filter capacitors on the operational amplifier circuit of the measurement signal of V_{ac}. The values of these capacitors were not correctly chosen leading to a malfunction of the amplifier circuit. As a first step the capacitors were simply removed. The signal was then correct but a little bit noisy.

Additionally the capacitors C7 and C8 (on the same schematic as previously), filter capacitors of the operational amplifier circuit of the measurement of I_{ac}, added a phase shift on the measurement signal of I_{ac} leading to a wrong control. The capacitors were removed here also, removing the phase shift but leading to a more noisy signal.

The values of C1, C2, C7 and C8 should be correctly chosen in the future in order to improve the quality of the signal. However the circuit is still operational without these resistors and it does not prevent testing the system.

Linearly decreasing AC and DC current: Not corrected

It has been noted in certain cases that the supplied DC current and therefore the AC current (at the filter's output) decrease at a constant rate. The decrease rate is fast enough to be easily observed within a few minutes. Turning on and off both DC power supply and AC connection to the grid does not "reset" the currents to their initial values (values on firs turn on of the test). However the resetting of the DSP does reset the current to their initial values. This behavior tends to show a problem in the digital control. A few changes have been tried out without success in the models configuration. This is a problematic behavior that needs to be corrected.

NOTE: Therefore no precise efficiency calculation has been made for there is a problem that has not yet been resolved:

AC voltage measurement problem: Not corrected

The section **4.3.3** states that the AC voltage sensing is properly working. Nevertheless, when the output of the LCL filter is connected to the transformer and that the connection with the grid is made, the voltage sensing is not correct.

Tests have been made and it has been determined that the error concerns the design of the AC voltage measurement circuit. The circuit consist of a 4 resistor voltage divider with a ground connection in the middle (as seen in section **4.3.2**). The connection point of the voltage divider that is connected to the low side of the filter's output is also connected to the source of mosfet Q3. The voltage at this point is therefore a rectangular signal.

The division of the LCL filter inductances in 2, one half on each branch of the filter ("low" voltage and "high" voltage branch) such as in Figure 8.10, might be a solution for this problem.

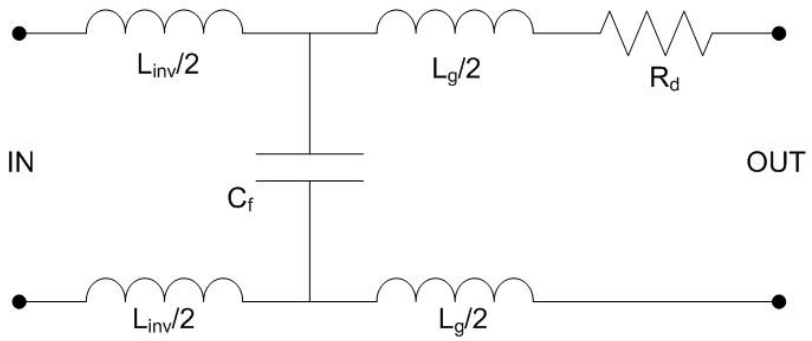


Figure 8.10: Possible filter design solution

Furthermore, the circuit at the input of the isolation amplifier ACPL-782 used for the measurement of the AC voltage should probably be reconsidered. The actual design had not been tested before (validated only theoretically).

Chapter 9

Further Work

A list of the digital available content of this project (schematics, programs ...) can be found in Appendix **D**.

9.1 Error corrections

Obviously the errors described in the report should be corrected before continuing working on this project. Here is a quick summary of the discovered errors during the project:

- Amplifier circuit in the AC voltage scaling on the signal scaling board: the amplifier factor α is 1 though it should be closer to (at least under) 0.9375
- Values of the filter capacitors of the amplifier circuit of the measurement scalings on the signal scaling board
- Correct the AC and DC constant current decrease that is observed in certain cases
- Solve the AC voltage measurement circuit on the power electronic board in order to have a correct voltage measurement when the inverter is connected to the grid

9.2 Hardware

Some hardware design improvements can also be made:

- The use of the TI developer's kit board is not necessary. A much simpler board could be considered or the DSP control card could be integrated on the signal scaling board

- Change the resistor devices in the schematic of the scaling signal board in order to be able to solder the resistors flat (the total size of the signal scaling should then also increase)
- Provide some easy test point on the boards in order to simplify the different validation tests.

9.3 Control

Not many control model have been tested yet. The closed loop current control with the inverter connected to the grid has not correctly worked. Here is a list of possible changes:

- Correct the configuration of the PLL block used in model Test_closed_loop_3.mdl
- Tune the PI control
- Change the PWM generation methods
- Include a MPPT algorithm to the control

Conclusion

The aim of this master thesis project was to build a grid-connected single-phase inverter with digital control. The design of the entire system was a challenge in this project. It was decided to use only a DC-AC stage between the DC power input and the grid connection. Two electronic boards were made. One consisting of the full-bridge inverter and the measuring circuits and one acting as an interface between the "power electronics" and the DSP board used for digital control. The two boards are fully functional except for the AC voltage measurement which has to be reconsidered.

Simulations were carried out as well for validating the design of the board as to compare the built system with its simulation model. Furthermore model-based programing was used in order to create a control program for the DSP. Several control programs have been tested on the system.

The final system does not properly work yet when connected to the grid , due to a design error in the measurement of the AC voltage. But as it has been seen throughout the testings, it is working as a stand-alone inverter. Different digital control, such as MPP tracking for example, would have been very interesting to study. Unfortunately the working state of the system did not enable it.

As for myself, the design of the entire system was very challenging. It added practical constraints to theoretical operation. Design of circuit topologies, editing schematics, lay-outs, learning how to choose a component, and using digital control were new difficulties. Overcoming them was very interesting and formative.

References

During the entire work of this project, many articles, books or documentations have been used. They will be listed here, classed on their subjects.

General literature on photovoltaic systems: [3].

Literature on inverters topology: [4].

Literature on inverter control: [5], [6], [7] and [8].

Literature on DQ-frame control: [9], [10], and [11].

Literature on LCL filter design: [2] and [1].

And the following Texas Instruments documentation files: SPRU716B (ADC reference guide), SPRU791F (PWM reference guide) and SPRU712G (System control and interrupts reference guide).

Bibliography

[1] S. V. Araújo, A. Engler, B. Sahan, and F. L. M. Antunes, "Lcl filter design for grid-connected npc inverters in offshore wind turbines," *7th Internatonal Conference on Power Electronics, ICPE '07*, pp. 1133–1138, October 2007.

[2] M. Liserre, F. Blaabjerg, and S. Hansen, "Design and control of an lcl-filter based three-phase active rectifier," *Industry Applications Conference, 2001. Thirty-Sixth IAS Annual Meeting. Conference Record of the 2001 IEEE*, pp. 299–307, October 2001.

[3] R. A. Messenger and J. Ventre, *Photovoltaic System Engineering.* CRC, 2nd ed., 2003.

[4] B. Hu, L. Chang, and Y. Xue, "Study of a novel buck-boost inverter for photovoltaic systems," *International Conference on Electrical Machines and Systems, ICEMS 2008*, pp. 2602–2606, October 2008.

[5] J. Hu, J. Zhang, and H. Wu, "A novel mppt control algorithm based on numerical calculation for pv generation systems,"

[6] F. Luo, P. Xu, Y. Kang, and S. Duan, "A variable step maximum power point tracking method using differential equation solution," *2007 Second IEEE Conference on Industrial Electronics and Applications*, pp. 2259–2263, 2007.

[7] W. Swiegers and J. H. Enslin, "An integrated maximum power point tracker for photovoltaic panels," *Industrial Electronics, 1998. Proceedings. ISIE '98. IEEE International Symposium on*, pp. 40–44, July 1998.

[8] D. Boroyevich, "Modeling and control of three-phase pwm converters," *The 2nd IEEE International Power and Energy Conference Johor Bahru, MALAYSIA*, November 2008.

[9] A. Roshan, R. Burgos, A. C. Baisden, F. Wang, and D. Boroyevich, "A d-q frame controller for a full-bridge single phase inverter used in small distributed power generation systems," *Applied Power Electronics Conference, APEC 2007 - Twenty Second Annual IEEE*, pp. 1048–2334, 2007.

[10] R. Zhang, M. Cardinal, P. Szczesny, and M. Dame, "A grid simulator with control of single-phase power converters in d-q rotating frame," *Power Electronics Specialists Conference, 2002. pesc 02. 2002 IEEE 33rd Annual*, pp. 1431–1436, 2002.

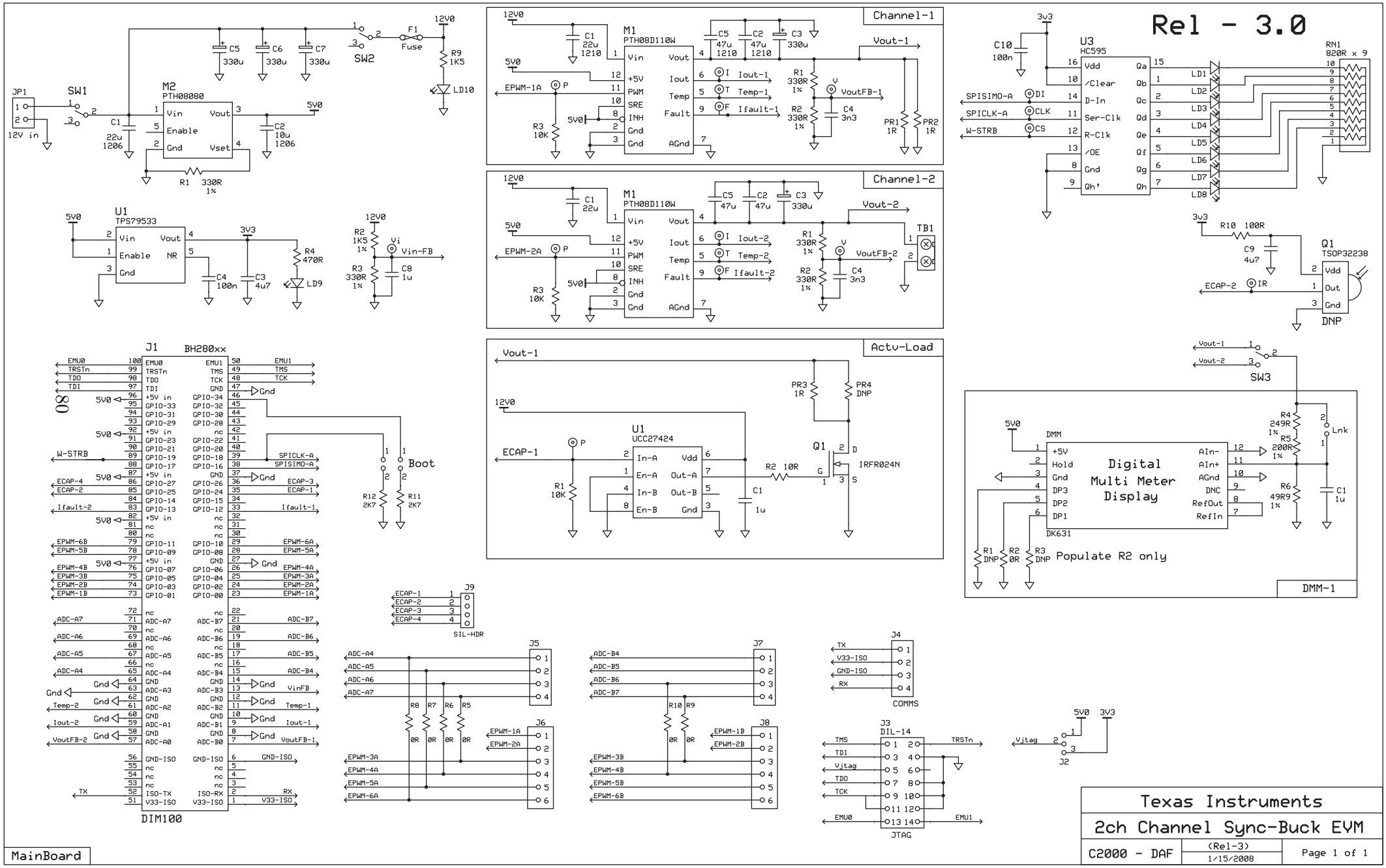
[11] M. Milosevic, "Decoupling control of d and q current components in three-phase voltage source inverter,"

Appendix A

Schematic and layouts of the boards

NOTE:

1. **The schematic of the power board has been changed compared to the built board: the current sensor footprint has been corrected in EAGLE, consequently, the output signals of the current sensors do not respect the isolation space and the AC current is measured in the wrong direction. The layouts of the current sensors should be reconsidered.**
2. **On the schematic of the signal scaling board, resistors RDC20, RDC21, RAC20 and RAC21 have been added in order to protect the ADC from a too high input current.**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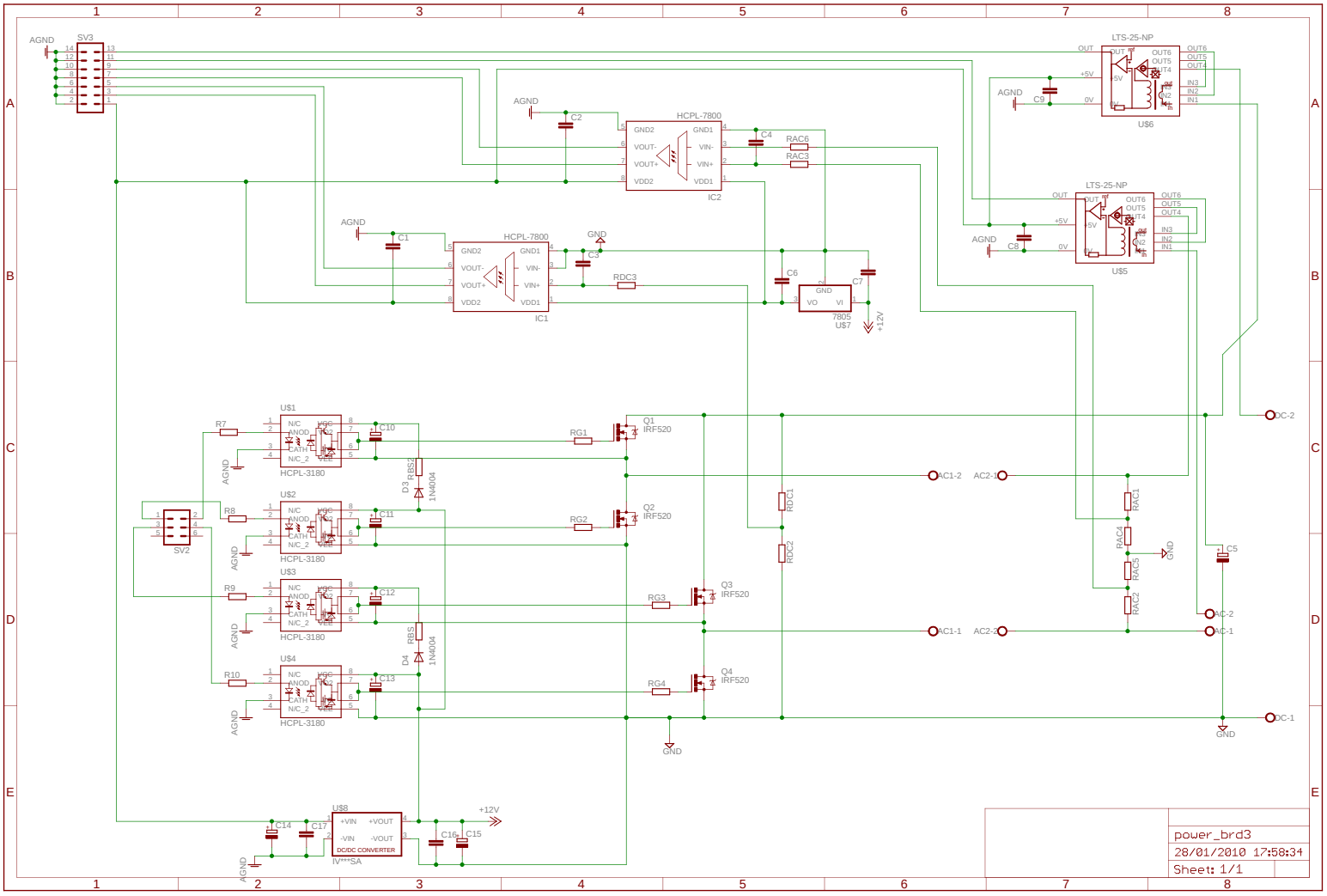
Channel-1
Channel-2
Actv-Load
M1
PTH08D110W
M2
PTH08080
U1
TPS79533
U1
UCC27424
U3
HC595
J1
BH280xx
DIM100
Digital
Multi Meter
Display
DMM
DK631
Populate R2 only
DMM-1
Boot
DNP
Texas Instruments
2ch Channel Sync-Buck EVM
C2000 - DAF
(Rel-3)
1/15/2008
Page 1 of 1
MainBoard



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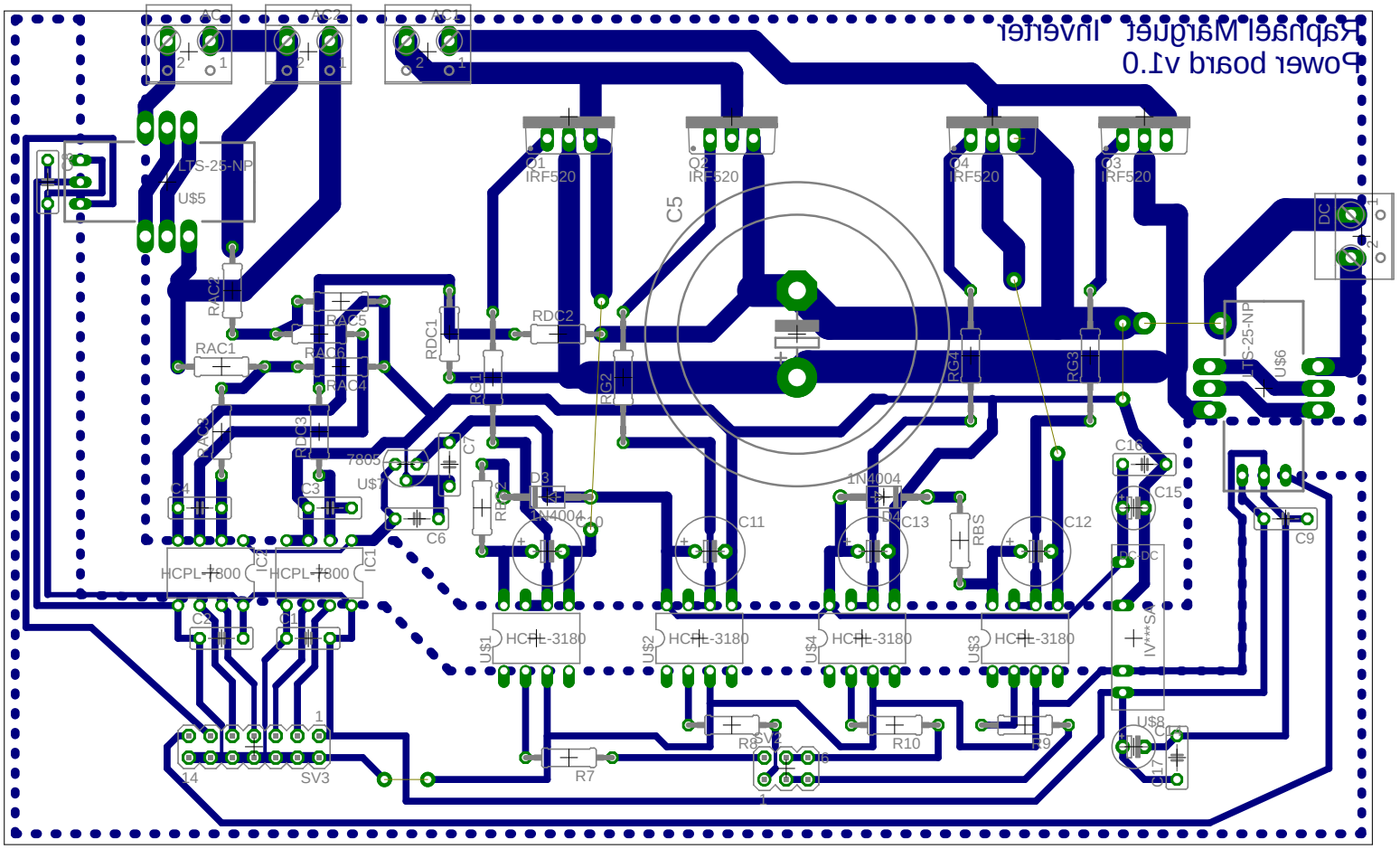

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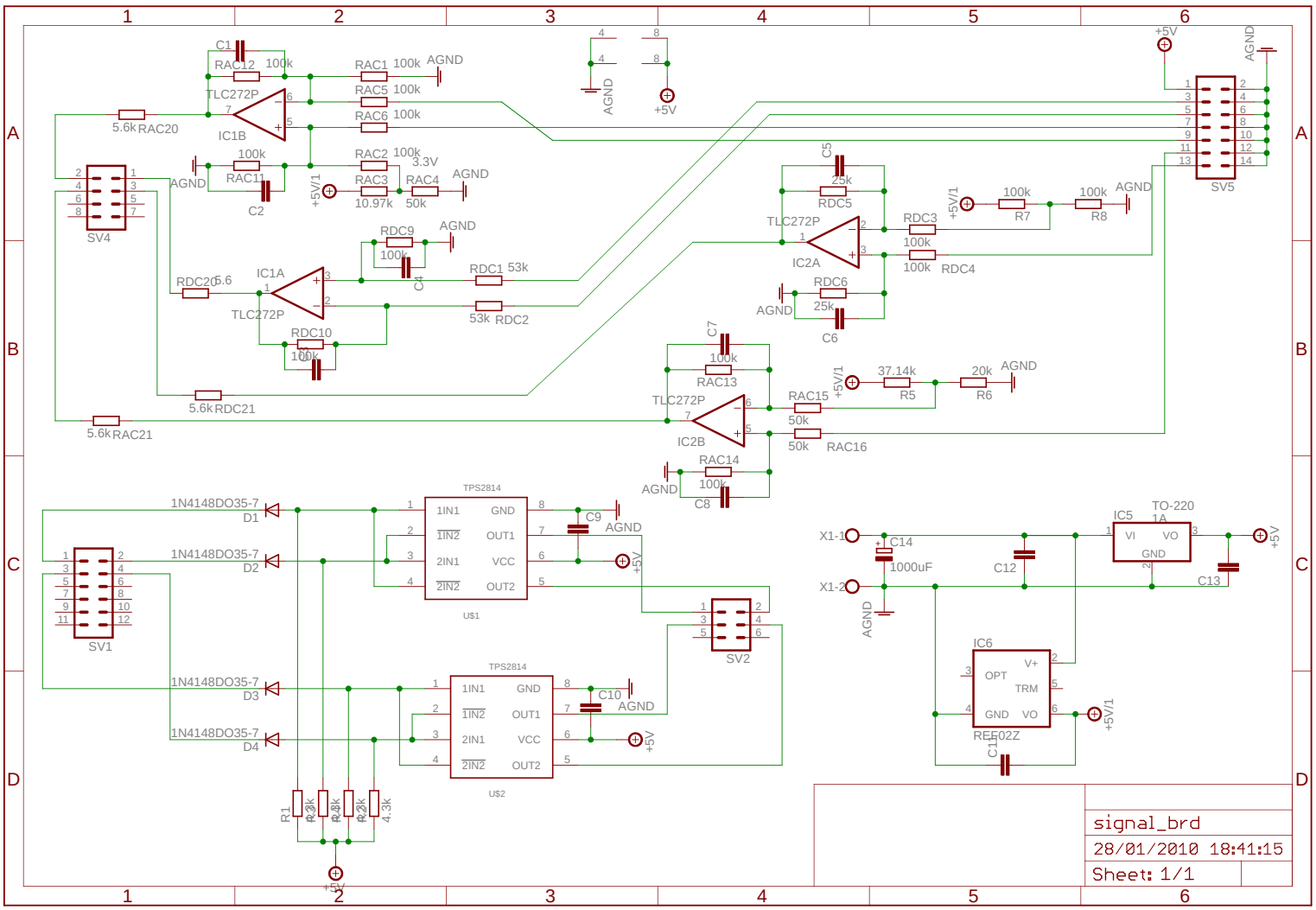
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IC1B
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IC2B
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U$2
REF02Z
TO-220
SV1
SV2
SV4
SV5
+5V
AGND
+5V/1
3.3V
5.6k RAC20
5.6k RAC21
5.6k RDC21
5.6 RDC20
100k RAC1
100k RAC2
100k RAC3
10.97k
100k RAC4
50k
100k RAC5
100k RAC6
100k RAC11
100k RAC12
C1
C2
RDC1 53k
53k RDC2
RDC9 100k
RDC10 100k
C4
RDC3 100k
RDC4 100k
RDC5 25k
RDC6 25k
C5
C6
100k R7
100k R8
RAC13 100k
RAC14 100k
RAC15 50k
RAC16 50k
37.14k R5
20k R6
C7
C8
1N4148DO35-7 D1
1N4148DO35-7 D2
1N4148DO35-7 D3
1N4148DO35-7 D4
C9
C10
R1 4.3k
4.3k
4.3k
4.3k
4.3k
X1-1
X1-2
C14 1000uF
C12
C13
C11
IC5 1A
IC6
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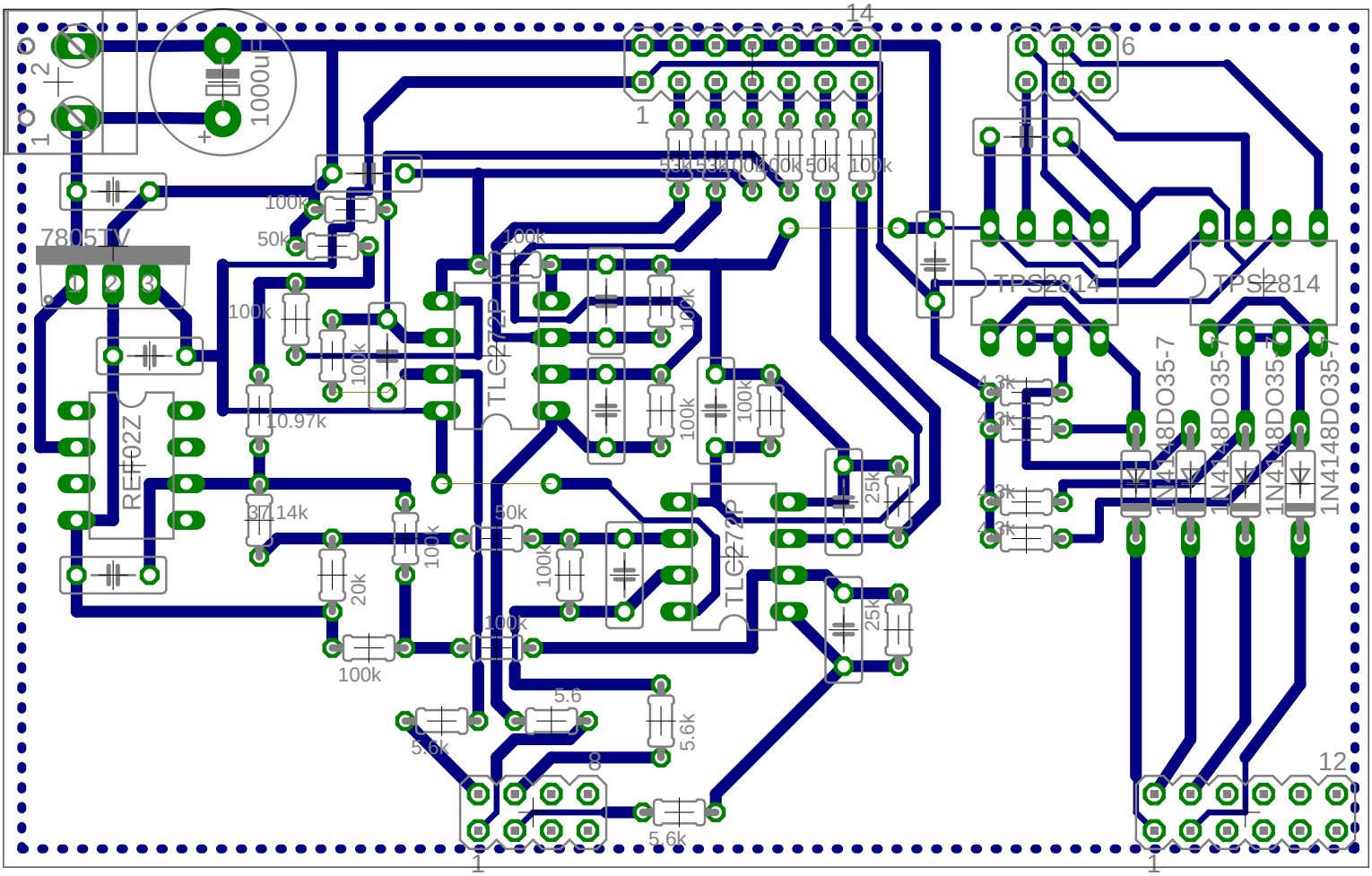
1IN2
2IN1
2IN2
GND
OUT1
OUT2
VCC
VI
VO
V+
OPT
TRM



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Appendix B

List of the values of the boards components

The components are called by their name on the schematics. Values are in Ω

B.1 Signal Scaling Board

RAC1 = 100k
RAC2 = 100k
RAC3 = 120
RAC4 = 56
RAC5 = 100k
RAC6 = 100k
RAC11 = 100k
RAC12 = 100k
RAC13 = 100k
RAC14 = 100k
RAC15 = 47k
RAC16 = 47k
RAC20 = 5.6k
RAC21 = 5.6k

RDC1 = 56k
RDC2 = 56k
RDC3 = 100k
RDC4 = 100k
RDC5 = 25k
RDC6 = 25k

RDC9 = 100k
RDC10 = 100k
RDC20 = 5.6k
RDC21 = 5.6k

R1 = 4.3k
R2 = 4.3k
R3 = 4.3k
R4 = 4.3k
R5 = 39k
R6 = 22k
R7 = 39k
R8 = 22k

D1 = 1N4148
D2 = 1N4148
D3 = 1N4148
D4 = 1N4148

B.2 Power Board

RAC1 = 100k
RAC2 = 100k
RAC3 = 39
RAC4 = 364
RAC5 = 364
RAC6 = 39

RDC1 = 100k
RDC2 = 364k
RDC3 = 39

R7 = 50
R8 = 50
R9 = 50
R10 = 50

RG1 = 5
RG1 = 5
RG1 = 5
RG1 = 5

RBS = 300
RBS2 = 300

C10 = 10μF
C11 = 10μF
C12 = 10μF
C13 = 10μF

Appendix C

First page of the datasheets of the used components

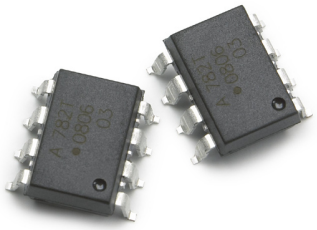
ACPL-782T-000E

Automotive Isolation Amplifier

Data Sheet

Lead (Pb) Free
RoHS 6 fully compliant

RoHS 6 fully compliant options available;
-xxxE denotes a lead-free product



Description

The ACPL-782T isolation amplifier was designed for voltage and current sensing in electronic motor drives and battery system monitoring. In a typical implementation, and motor currents flow through an external resistor and the resulting analog voltage drop is sensed by the ACPL-782T. A differential output voltage is created on the other side of the ACPL-782T optical isolation barrier. This differential output voltage is proportional to the motor current and can be converted to a single-ended signal by using an op-amp as shown in the recommended application circuit. Since common-mode voltage swings of several hundred volts in tens of nanoseconds are common in modern switching inverter motor drives, the ACPL-782T was designed to ignore very high common-mode transient slew rates (of at least 10 kV/μs).

The high CMR capability of the ACPL-782T isolation amplifier provides the precision and stability needed to accurately monitor motor current and DC rail voltage in high noise motor control environments, providing for smoother control (less "torque ripple") in various types of motor control applications.

The product can also be used for general analog signal isolation applications requiring high accuracy, stability, and linearity under similarly severe noise conditions. The ACPL-782T utilizes sigma delta (Σ–Δ) analog-to-digital converter technology, chopper stabilized amplifiers, and a fully differential circuit topology.

Together, these features deliver unequaled isolation-mode noise rejection, as well as excellent offset and gain accuracy and stability over time and temperature. This performance is delivered in a compact, auto-insertable, industry standard 8-pin DIP package that meets worldwide regulatory safety standards. (A gull-wing surface mount option -300E is also available).

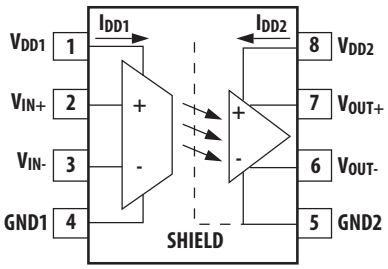
Features

- ±2% Gain Tolerance @ 25°C
- 15 kV/μs Common-Mode Rejection at V_{CM} = 1000V
- 30ppm/°C Gain Drift vs. Temperature
- 0.3 mV Input Offset Voltage
- 100 kHz Bandwidth
- 0.004% Nonlinearity
- Compact, Auto-Insertable Standard 8-pin DIP Package
- Worldwide Safety Approval (pending):
  - UL 1577 (3750 V_{RMS}/1 min.) and
  - CSA
  - IEC/EN/DIN EN 60747-5-5
- Qualified to AEC-Q100 Test Guidelines
- Automotive Operating Temperature -40 to 125°C
- Advanced Sigma-Delta (Σ–Δ) A/D Converter Technology
- Fully Differential Circuit Topology

Applications

- Automotive Motor Inverter Current/Voltage Sensing
- Automotive AC/DC and DC/DC converter Current/Voltage sensing
- Automotive Battery ECU
- Automotive Motor Phase Current Sensing
- Isolation Interface for Temperature Sensing
- General Purpose Current Sensing and Monitoring

Functional Diagram



The connection of a 0.1 μF bypass capacitor between pins 1 and 4, pins 5 and 8 is recommended.

CAUTION: *It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.*

TS-HA Series two terminal snap-in

- 3000 hour* life at 105ºC with high ripple current capability
- Wide range of case sizes including 20mm, low profile lengths
- ***NEW:*** 40mm diameter sizes through 100WV.
- Can vent construction

Rated Working Voltage:	10 ~ 250 VDC	385 ~ 450 VDC
Operating Temperature:	-40 ~ +105ºC	-25 ~ +105ºC
Nominal Capacitance:	68 ~ 68000µF (±20% tolerance)	33 ~ 470µF (±20% tolerance)
Dissipation Factor: (120 Hz, +20ºC)	Working Voltage [V]: 10 / 16 / 25 / 35 / 50 / 63 / 80 / 100 - 450 Max. D.F. (%): 55 / 45 / 35 / 30 / 25 / 20 / 17 / 15 For capacitance values > 33000µF, add the value of: (rated cap. [µF] - 33000) / 1000	
Endurance:	3000 hours* at +105ºC with maximum specified ripple current (see page 4) *2000 hours for 20mm diameter or 20mm length sizes	

Part Number System

E C □ □ — Common Code/ Terminal Type | □ □ — Voltage Code | A — Series | □ □ □ — Capacitance Code | □ — Case Diameter | □ — Top Vinyl Plate

Common Code/ Terminal Type	
ECOS	6.3mm Length Terminal (Standard)
ECEC	4mm Length "Short" Terminal
(See page 7)	

Case Diameter	
A	20mm
B	22mm
C	25mm
D	30mm
E	35mm
F	40mm

Top Vinyl Plate	
25 ~ 50mm lengths	
A	With Plate
B	Without plate
20mm length	
L	With Plate
G	Without plate

Ripple Current Multipliers: Page 7

TS-HA Standard Ratings

Cap. (µF)	Size (mm) D x L	Max 105°C R.C. (A_{rms}) 120Hz	Max 105°C R.C. (A_{rms}) 10k~100kHz	20°C ESR (Ω, max.) 120Hz	20°C ESR (Ω, max.) 20kHz	Panasonic Part Number
10 VDC Working, 13 VDC Surge						
6800	20 x 25	1.30	1.50	0.110	0.093	**ECOS1AA682AA**
8200	20 x 30	1.60	1.84	0.091	0.077	**ECOS1AA822AA**
10000	20 x 30	1.80	2.07	0.075	0.063	**ECOS1AA103AA**
12000	20 x 35	2.20	2.53	0.062	0.053	**ECOS1AA123AA**
15000	20 x 40	2.30	2.65	0.053	0.045	**ECOS1AA153AA**
4700	22 x 25	0.85	0.98	0.159	0.135	**ECOS1AA472BA**
6800	22 x 25	1.30	1.50	0.110	0.093	**ECOS1AA682BA**
10000	22 x 25	1.80	2.07	0.075	0.063	**ECOS1AA103BA**
12000	22 x 30	2.20	2.53	0.062	0.053	**ECOS1AA123BA**
15000	22 x 35	2.30	2.65	0.053	0.045	**ECOS1AA153BA**
18000	22 x 40	2.40	2.76	0.044	0.038	**ECOS1AA183BA**
22000	22 x 45	2.60	2.99	0.038	0.032	**ECOS1AA223BA**
27000	22 x 50	3.10	3.57	0.033	0.028	**ECOS1AA273BA**
15000	25 x 25	2.30	2.65	0.053	0.045	**ECOS1AA153CA**
18000	25 x 30	2.40	2.76	0.044	0.038	**ECOS1AA183CA**
22000	25 x 35	2.60	2.99	0.038	0.032	**ECOS1AA223CA**
27000	25 x 40	3.10	3.57	0.033	0.028	**ECOS1AA273CA**
33000	25 x 45	3.40	3.91	0.027	0.023	**ECOS1AA333CA**
39000	25 x 50	3.70	4.26	0.025	0.021	**ECOS1AA393CA**
22000	30 x 25	2.60	2.99	0.038	0.032	**ECOS1AA223DA**
27000	30 x 30	3.10	3.57	0.033	0.028	**ECOS1AA273DA**
33000	30 x 35	3.40	3.91	0.027	0.023	**ECOS1AA333DA**
39000	30 x 40	3.70	4.26	0.025	0.021	**ECOS1AA393DA**
47000	30 x 45	4.20	4.83	0.023	0.020	**ECOS1AA473DA**
56000	30 x 50	5.00	5.75	0.022	0.019	**ECOS1AA563DA**
27000	35 x 25	3.10	3.57	0.033	0.028	**ECOS1AA273EA**
33000	35 x 30	3.40	3.91	0.027	0.023	**ECOS1AA333EA**
39000	35 x 30	3.70	4.26	0.025	0.021	**ECOS1AA393EA**
47000	35 x 35	4.20	4.83	0.023	0.020	**ECOS1AA473EA**
56000	35 x 40	5.00	5.75	0.022	0.021	**ECOS1AA563EA**
68000	35 x 50	5.50	6.33	0.021	0.020	**ECOS1AA683EA**
62000	40 x 40	5.42	6.23	0.023	0.022	**ECOS1AA623FA**
82000	40 x 50	7.36	8.46	0.018	0.017	**ECOS1AA823FA**

Cap. (µF)	Size (mm) D x L	Max 105°C R.C. (A_{rms}) 120Hz	Max 105°C R.C. (A_{rms}) 10k~100kHz	20°C ESR (Ω, max.) 120Hz	20°C ESR (Ω, max.) 20kHz	Panasonic Part Number
16 VDC Working, 20 VDC Surge						
6800	20 x 30	2.20	2.53	0.085	0.068	**ECOS1CA682AA**
8200	20 x 35	2.40	2.76	0.071	0.057	**ECOS1CA822AA**
10000	20 x 40	2.60	2.99	0.066	0.053	**ECOS1CA103AA**
3300	22 x 20	1.30	1.50	0.216	0.173	**ECOS1CA332BL**
3300	22 x 25	1.30	1.50	0.176	0.141	**ECOS1CA332BA**
4700	22 x 25	1.52	1.75	0.123	0.099	**ECOS1CA472BA**
6800	22 x 25	2.20	2.53	0.085	0.068	**ECOS1CA682BA**
8200	22 x 30	2.40	2.76	0.071	0.057	**ECOS1CA822BA**
10000	22 x 30	2.60	2.99	0.066	0.053	**ECOS1CA103BA**
12000	22 x 35	2.90	3.34	0.055	0.044	**ECOS1CA123BA**
15000	22 x 40	3.20	3.68	0.046	0.037	**ECOS1CA153BA**
18000	22 x 45	3.50	4.03	0.040	0.034	**ECOS1CA183BA**
4700	25 x 20	1.60	1.84	0.152	0.121	**ECOS1CA472CL**
10000	25 x 25	2.60	2.99	0.066	0.053	**ECOS1CA103CA**
12000	25 x 30	2.90	3.34	0.055	0.044	**ECOS1CA123CA**
15000	25 x 35	3.20	3.68	0.046	0.037	**ECOS1CA153CA**
18000	25 x 40	3.50	4.03	0.040	0.034	**ECOS1CA183CA**
22000	25 x 45	3.80	4.37	0.033	0.028	**ECOS1CA223CA**
27000	25 x 50	4.20	4.83	0.028	0.025	**ECOS1CA273CA**
6800	30 x 20	1.80	2.07	0.105	0.084	**ECOS1CA682DL**
12000	30 x 25	2.90	3.34	0.055	0.044	**ECOS1CA123DA**
15000	30 x 30	3.20	3.68	0.046	0.037	**ECOS1CA153DA**
18000	30 x 30	3.50	4.03	0.040	0.034	**ECOS1CA183DA**
22000	30 x 35	3.80	4.37	0.033	0.028	**ECOS1CA223DA**
27000	30 x 40	4.20	4.83	0.028	0.025	**ECOS1CA273DA**
33000	30 x 45	4.70	5.41	0.023	0.020	**ECOS1CA333DA**
39000	30 x 50	5.10	5.87	0.022	0.020	**ECOS1CA393DA**
10000	35 x 20	2.40	2.76	0.071	0.057	**ECOS1CA103EL**
18000	35 x 25	3.50	4.03	0.040	0.034	**ECOS1CA183EA**
22000	35 x 30	3.80	4.37	0.033	0.028	**ECOS1CA223EA**
27000	35 x 30	4.20	4.83	0.028	0.025	**ECOS1CA273EA**
33000	35 x 35	4.70	5.41	0.023	0.020	**ECOS1CA333EA**
39000	35 x 40	5.10	5.87	0.022	0.020	**ECOS1CA393EA**
47000	35 x 45	5.50	6.33	0.020	0.018	**ECOS1CA473EA**
56000	35 x 50	6.00	6.90	0.019	0.017	**ECOS1CA563EA**
47000	40 x 40	5.50	6.33	0.020	0.018	**ECOS1CA473FA**
68000	40 x 50	7.29	8.38	0.015	0.014	**ECOS1CA683FA**

HCPL-3180

2.5 Amp Output Current, High Speed, Gate Drive Optocoupler

AVAGO TECHNOLOGIES

Data Sheet

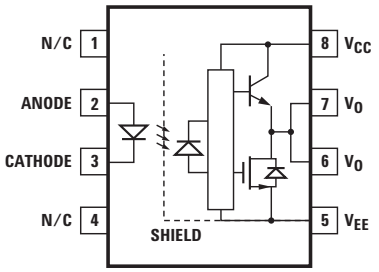
Lead (Pb) Free
RoHS 6 fully compliant

RoHS 6 fully compliant options available;
-xxxE denotes a lead-free product

Description

This family of devices consists of a GaAsP LED. The LED is optically coupled to an integrated circuit with a power stage. These optocouplers are ideally suited for high frequency driving of power IGBTs and MOSFETs used in Plasma Display Panels, high performance DC/DC converters, and motor control inverter applications.

Functional Diagram



A 0.1 µF bypass capacitor must be connected between pins V_{CC} and Ground.

Features

- **2.5 A maximum peak output current**
- **2.0 A minimum peak output current**
- **250 kHz maximum switching speed**
- **High speed response: 200 ns maximum propagation delay over temperature range**
- **10 kV/µs minimum Common Mode Rejection (CMR) at V_{CM} = 1500 V**
- **Under Voltage Lock-Out protection (UVLO) with hysteresis**
- **Wide operating temperature range: –40°C to 100°C**
- **Wide V_{CC} operating range: 10 V to 20 V**
- **20 ns typical pulse width distortion**
- **Safety approvals:**
  – UL approval, 3750 V_{rms} for 1 minute
  – CSA approval
  – IEC/EN/DIN EN 60747-5-2 approval

Applications

- **Plasma Display Panel (PDP)**
- **Distributed Power Architecture (DPA)**
- **Switch Mode Rectifier (SMR)**
- **High performance DC/DC converter**
- **High performance Switching Power Supply (SPS)**
- **High performance Uninterruptible Power Supply (UPS)**
- **Isolated IGBT/Power MOSFET gate drive**

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation, which may be induced by ESD.

International
IOR Rectifier

PD - 96214

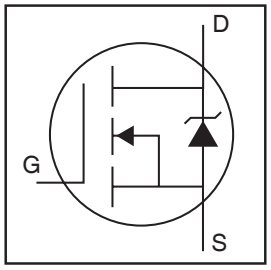
IRFB4110GPbF

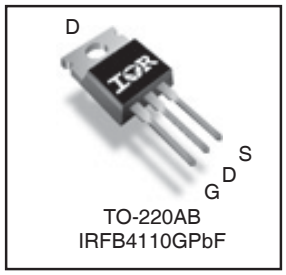
HEXFET® Power MOSFET

Applications
- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

V_{DSS}	100V
$R_{DS(on)}$ typ.	3.7mΩ
max.	4.5mΩ
I_D (Silicon Limited)	180A ①
I_D (Package Limited)	120A

Benefits
- Improved Gate, Avalanche and Dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free
- Halogen-Free





TO-220AB
IRFB4110GPbF

G	D	S
Gate	Drain	Source

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, VGS @ 10V (Silicon Limited)	180①	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	130①	
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Wire Bond Limited)	120	
I_{DM}	Pulsed Drain Current ②	670	
P_D @T_C = 25°C	Maximum Power Dissipation	370	W
	Linear Derating Factor	2.5	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery ④	5.3	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300	
	(1.6mm from case)		
	Mounting torque, 6-32 or M3 screw	10lbf·in (1.1N·m)	

Avalanche Characteristics

$E_{AS\ (Thermally\ limited)}$	Single Pulse Avalanche Energy ③	190	mJ
I_{AR}	Avalanche Current ②	See Fig. 14, 15, 22a, 22b	A
E_{AR}	Repetitive Avalanche Energy ②		mJ

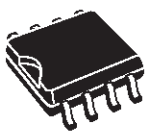
Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑧	—	0.402	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	62	

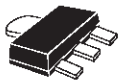
L78L00 SERIES

POSITIVE VOLTAGE REGULATORS

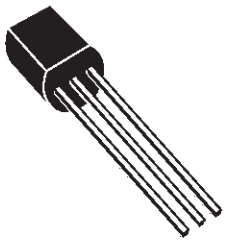
- OUTPUT CURRENT UP TO 100 mA
- OUTPUT VOLTAGES OF 3.3; 5; 6; 8; 9; 12; 15; 18; 24V
- THERMAL OVERLOAD PROTECTION
- SHORT CIRCUIT PROTECTION
- NO EXTERNAL COMPONENTS ARE REQUIRED
- AVAILABLE IN EITHER ± 5% (AC) OR ± 10% (C) SELECTION



SO-8



SOT-89



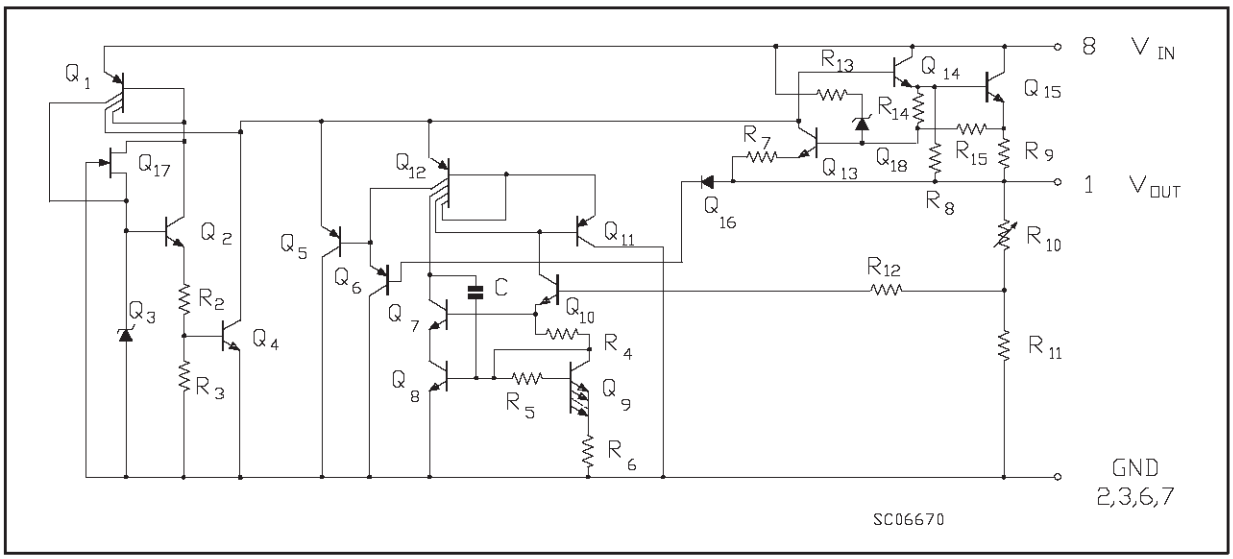
TO-92

DESCRIPTION

The L78L00 series of three-terminal positive regulators employ internal current limiting and thermal shutdown, making them essentially indestructible. If adequate heatsink is provided, they can deliver up to 100 mA output current. They are intended as fixed voltage regulators in a wide range of applications including local or on-card regulation for elimination of noise and distribution problems associated with single-point regulation. In addition, they can be used with power pass elements to make high-current voltage regulators.

The L78L00 series used as Zener diode/resistor combination replacement, offers an effective output impedance improvement of typically two orders of magnetude, along with lower quiescent current and lower noise.

BLOCK DIAGRAM



National Semiconductor

July 2006

LM340/LM78XX Series 3-Terminal Positive Regulators

General Description

The LM140/LM340A/LM340/LM78XXC monolithic 3-terminal positive voltage regulators employ internal current-limiting, thermal shutdown and safe-area compensation, making them essentially indestructible. If adequate heat sinking is provided, they can deliver over 1.0A output current. They are intended as fixed voltage regulators in a wide range of applications including local (on-card) regulation for elimination of noise and distribution problems associated with single-point regulation. In addition to use as fixed voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents.

Considerable effort was expended to make the entire series of regulators easy to use and minimize the number of external components. It is not necessary to bypass the output, although this does improve transient response. Input bypassing is needed only if the regulator is located far from the filter capacitor of the power supply.

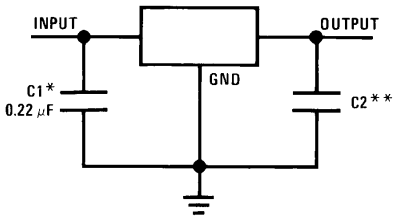
The 5V, 12V, and 15V regulator options are available in the steel TO-3 power package. The LM340A/LM340/LM78XXC series is available in the TO-220 plastic power package, and the LM340-5.0 is available in the SOT-223 package, as well as the LM340-5.0 and LM340-12 in the surface-mount TO-263 package.

Features

- Complete specifications at 1A load
- Output voltage tolerances of ±2% at T_j = 25˚C and ±4% over the temperature range (LM340A)
- Line regulation of 0.01% of V_{OUT}/V of ΔV_{IN} at 1A load (LM340A)
- Load regulation of 0.3% of V_{OUT}/A (LM340A)
- Internal thermal overload protection
- Internal short-circuit current limit
- Output transistor safe area protection
- P^+ Product Enhancement tested

Typical Applications

Fixed Output Regulator

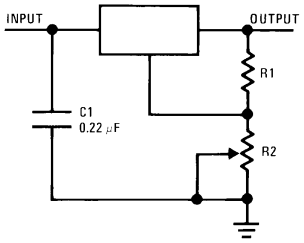


00778101

*Required if the regulator is located far from the power supply filter.

**Although no output capacitor is needed for stability, it does help transient response. (If needed, use 0.1 µF, ceramic disc).

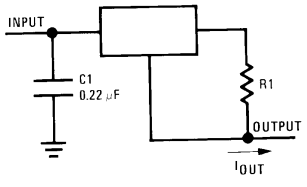
Adjustable Output Regulator



00778102

V_{OUT} = 5V + (5V/R1 + I_Q) R2 5V/R1 > 3 I_Q,
load regulation (L_r) ≈ [(R1 + R2)/R1] (L_r of LM340-5).

Current Regulator

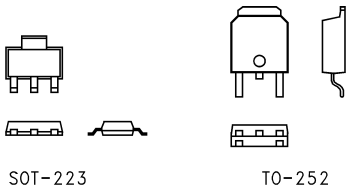


00778103

$$I_{OUT} = \frac{V2\text{-}3}{R1} + I_Q$$

ΔI_Q = 1.3 mA over line and load changes.

Comparison between SOT-223 and D-Pak (TO-252) Packages



00778138

Scale 1:1

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Current Transducer LTS 25-NP

I_{PN} = 25 At

For the electronic measurement of currents: DC, AC, pulsed, mixed with galvanic isolation between the primary circuit (high power) and the secondary circuit (electronic circuit).

16054

Electrical data

I_{PN}	Primary nominal current rms		25	At
I_{PM}	Primary current, measuring range		0 .. ± 80	At
V_{OUT}	Output voltage (Analog) @ I_P		2.5 ± (0.625·I_P/I_{PN})V	
	I_P = 0		2.5 [1]	V
G	Sensitivity		25	mV/A
N_S	Number of secondary turns (± 0.1 %)		2000	
R_L	Load resistance		≥ 2	kΩ
R_{IM}	Internal measuring resistance (± 0.5 %)		50	Ω
TCR_{IM}	Temperature coefficient of R_{IM}		< 50	ppm/K
V_C	Supply voltage (± 5 %)		5	V
I_C	Current consumption @ V_C = 5 V	Typ	28+I_S [2]+($V_{OUT}$$R_L$)	mA

Accuracy - Dynamic performance data

X	Accuracy @ I_{PN}, T_A = 25°C		± 0.2		%
	Accuracy with R_{IM} @ I_{PN}, T_A = 25°C		± 0.7		%
ε_L	Linearity error		< 0.1		%
			Typ	Max	
TCV_{OUT}	Temperature coefficient of V_{OUT} @ I_P= 0	- 10°C .. + 85°C	50	100	ppm/K
		- 40°C .. - 10°C		150	ppm/K
TCG	Temperature coefficient of G	- 40°C .. + 85°C		50 [3]	ppm/K
V_{OM}	Magnetic offset voltage @ I_P = 0,				
	after an overload of 3 x I_{PN}			± 0.5	mV
	5 x I_{PN}			± 2.0	mV
	10 x I_{PN}			± 2.0	mV
t_{ra}	Reaction time @ 10 % of I_{PN}		< 100		ns
t_r	Response time to 90 % of I_{PN} step		< 400		ns
di/dt	di/dt accurately followed		> 60		A/µs
BW	Frequency bandwidth (0 .. - 0.5 dB)		DC .. 100		kHz
	(- 0.5.. 1 dB)		DC .. 200		kHz

General data

T_A	Ambient operating temperature	- 40 .. + 85	°C
T_S	Ambient storage temperature	- 40.. + 100	°C
m	Mass	10	g
	Standards	EN 50178: 1997	
		IEC 60950-1: 2001	

Notes: [1] Absolute value @ T_A = 25°C, 2.475 < V_{OUT} < 2.525

[2] I_S = I_P/N_S

[3] Only due to TCR_{IM}

Features

- Closed loop (compensated) multi-range current transducer using the Hall effect
- Unipolar voltage supply
- Isolated plastic case recognized according to UL 94-V0
- Compact design for PCB mounting
- Incorporated measuring resistance
- Extended measuring range.

Advantages

- Excellent accuracy
- Very good linearity
- Very low temperature drift
- Optimized response time
- Wide frequency bandwidth
- No insertion losses
- High immunity to external interference
- Current overload capability.

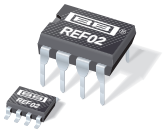
Applications

- AC variable speed drives and servo motor drives
- Static converters for DC motor drives
- Battery supplied applications
- Uninterruptible Power Supplies (UPS)
- Switched Mode Power Supplies (SMPS)
- Power supplies for welding applications.

Application domain

- Industrial.

REF02



SBVS003B – JANUARY 1993 – REVISED JANUARY 2005

+5V Precision VOLTAGE REFERENCE

FEATURES

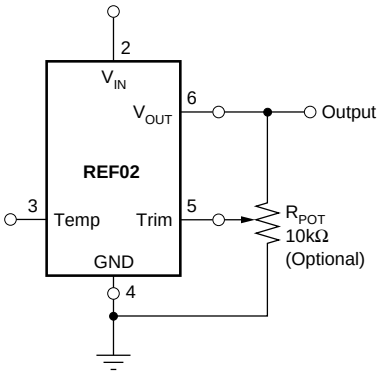
- **OUTPUT VOLTAGE: +5V ±0.2% max**
- **EXCELLENT TEMPERATURE STABILITY: 10ppm/°C max (–40°C to +85°C)**
- **LOW NOISE: 10μV_{PP} max (0.1Hz to 10Hz)**
- **EXCELLENT LINE REGULATION: 0.01%/V max**
- **EXCELLENT LOAD REGULATION: 0.008%/mA max**
- **LOW SUPPLY CURRENT: 1.4mA max**
- **SHORT-CIRCUIT PROTECTED**
- **WIDE SUPPLY RANGE: 8V to 40V**
- **INDUSTRIAL TEMPERATURE RANGE: –40°C to +85°C**
- **PACKAGE OPTIONS: DIP-8, SO-8**

APPLICATIONS

- **PRECISION REGULATORS**
- **CONSTANT CURRENT SOURCE/SINK**
- **DIGITAL VOLTMETERS**
- **V/F CONVERTERS**
- **A/D AND D/A CONVERTERS**
- **PRECISION CALIBRATION STANDARD**
- **TEST EQUIPMENT**

DESCRIPTION

The REF02 is a precision 5V voltage reference. The drift is laser trimmed to 10ppm/°C max over the extended industrial and military temperature range. The REF02 provides a stable 5V output that can be externally adjusted over a ±6% range with minimal effect on temperature stability. The REF02 operates from a single supply with an input range of 8V to 40V with a very low current drain of 1mA, and excellent temperature stability due to an improved design. Excellent line and load regulation, low noise, low power, and low cost make the REF02 the best choice whenever a 5V voltage reference is required. Available package options are DIP-8 and SO-8. The REF02 is an ideal choice for portable instrumentation, temperature transducers, Analog-to-Digital (A/D) and Digital-to-Analog (D/A) converters, and digital voltmeters.



+5V Reference with Trimmed Output

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1 Watt
IA Series

- Dual Output
- SIP or DIP Package
- 1000 VDC Isolation
- Short Circuit Protection
- -40 °C to +85 °C Operation
- MTBF >1.1 MHrs
- 3 Year Warranty

Specification

Input

Input Voltage Range	• Nominal ±10%[5]
Input Reflected Ripple Current	• 20 mA pk-pk (5 Hz to 20 MHz with 12 µH)
Input Reverse Voltage Protection	• None

Output

Output Voltage	• See table
Minimum Load	• None[6]
Line Regulation	• 1.2%/1% Δ Vin
Load Regulation	• ±10% 20-100% load change (3.3 V models ±20%)
Setpoint Accuracy	• ±3%
Ripple & Noise	• 75 mV pk-pk max, 20 MHz bandwidth
Temperature Coefficient	• 0.02%/°C
Maximum Capacitive Load	• ±100 µF

General

Efficiency	• See table
Isolation Voltage	• 1000 VDC minimum
Isolation Resistance	• 10^9 Ω
Isolation Capacitance	• 60 pF typical
Switching Frequency	• Variable, 80 KHz typical
MTBF	• >1.12 MHrs to MIL-HDBK-217F at 25 °C, GB

Environmental

Operating Temperature	• -40 °C to +85 °C
Storage Temperature	• -40 °C to +125 °C
Case Temperature	• 100 °C max
Cooling	• Convection-cooled

Notes

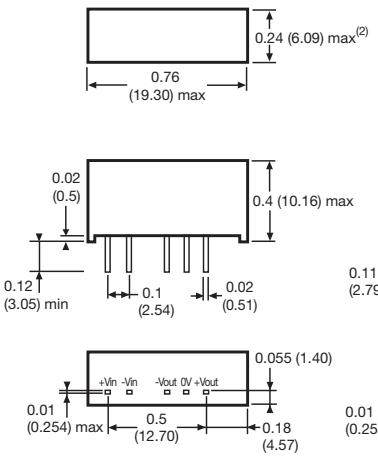
1. Replace 'S' in model number with 'D' for DIP package.
2. SIP 48 Vin models, dimension is 0.28 (7.20) max.
3. DIP 48 Vin models, dimension is 0.27 (6.88) max.
4. Outputs power-trade.
5. For 48 V models a 10 µF capacitor is required between +Vin and -Vin pins.
6. Operation at no load will not damage unit but it may not meet all specifications.
7. All dimensions in inches (mm).
8. Pin pitch tolerance: ±0.014 (±0.35)
9. Case tolerance ±0.02 (±0.5)
10. Weight: SIP 0.004 lbs (2.2 g), 48 V SIP 0.005 lbs (2.7 g), DIP 0.005 lbs (2.4g)

Input Voltage[5]	Output Voltage	Output Current[4]	Efficiency	Model Number[1]
3.3 VDC	±5.0 V	±100 mA	66%	IA0305S^
5 VDC	±3.3 V	±151 mA	65%	IA0503S^
	±5.0 V	±100 mA	74%	IA0505S†^
	±9.0 V	±55 mA	77%	IA0509S†^
	±12.0 V	±42 mA	78%	IA0512S†^
	±15.0 V	±33 mA	80%	IA0515S†^
	±24.0 V	±21 mA	80%	IA0524S^
12 VDC	±3.3 V	±151 mA	66%	IA1203S^
	±5.0 V	±100 mA	75%	IA1205S†^
	±9.0 V	±55 mA	76%	IA1209S†^
	±12.0 V	±42 mA	78%	IA1212S†^
	±15.0 V	±33 mA	80%	IA1215S†^
	±24.0 V	±21 mA	76%	IA1224S^
24 VDC	±3.3 V	±151 mA	68%	IA2403S^
	±5.0 V	±100 mA	74%	IA2405S†^
	±9.0 V	±55 mA	76%	IA2409S^
	±12.0 V	±42 mA	78%	IA2412S†^
	±15.0 V	±33 mA	78%	IA2415S†^
	±24.0 V	±21 mA	78%	IA2424S^
48 VDC	±3.3 V	±151 mA	60%	IA4803S
	±5.0 V	±100 mA	70%	IA4805S†
	±9.0 V	±55 mA	72%	IA4809S
	±12.0 V	±42 mA	74%	IA4812S†
	±15.0 V	±33 mA	74%	IA4815S
	±24.0 V	±21 mA	70%	IA4824S

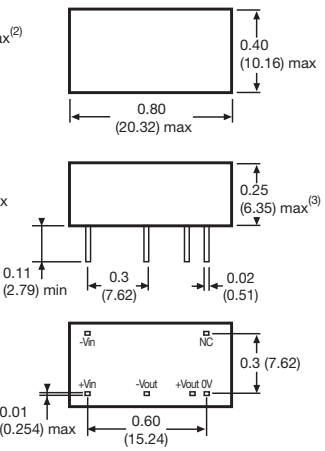
† Available from Farnell. See pages 266-269.
^ Available from Newark. See pages 270-272.

Mechanical Details

SIP Package

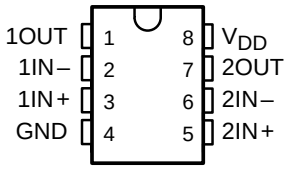


DIP Package

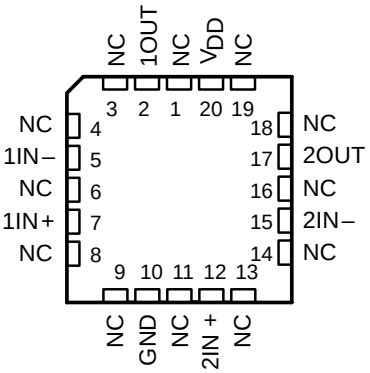


- **Trimmed Offset Voltage:**
  TLC277 . . . 500 μV Max at 25°C,
  V_{DD} = 5 V
- **Input Offset Voltage Drift . . . Typically 0.1 μV/Month, Including the First 30 Days**
- **Wide Range of Supply Voltages Over Specified Temperature Range:**
  0°C to 70°C . . . 3 V to 16 V
  –40°C to 85°C . . . 4 V to 16 V
  –55°C to 125°C . . . 4 V to 16 V
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail (C-Suffix, I-Suffix types)**
- **Low Noise . . . Typically 25 nV/$\sqrt{\text{Hz}}$ at f = 1 kHz**
- **Output Voltage Range Includes Negative Rail**
- **High Input impedance . . . 10^{12} Ω Typ**
- **ESD-Protection Circuitry**
- **Small-Outline Package Option Also Available in Tape and Reel**
- **Designed-In Latch-Up Immunity**

D, JG, P, OR PW PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC – No internal connection

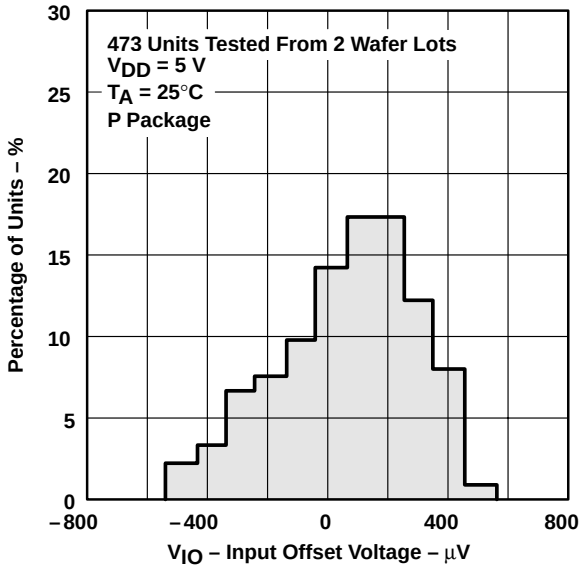
description

The TLC272 and TLC277 precision dual operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, low noise, and speeds approaching those of general-purpose BiFET devices.

These devices use Texas Instruments silicon-gate LinCMOS™ technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

The extremely high input impedance, low bias currents, and high slew rates make these cost-effective devices ideal for applications previously reserved for BiFET and NFET products. Four offset voltage grades are available (C-suffix and I-suffix types), ranging from the low-cost TLC272 (10 mV) to the high-precision TLC277 (500 μV). These advantages, in combination with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

DISTRIBUTION OF TLC277
INPUT OFFSET VOLTAGE



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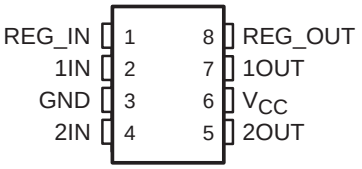
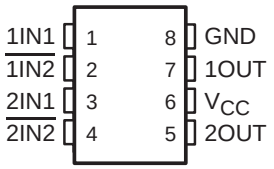
SLVS132F − NOVEMBER 1995 − REVISED OCTOBER 2004

- **Industry-Standard Driver Replacement**
- **25-ns Max Rise/Fall Times and 40-ns Max Propagation Delay − 1-nF Load, V_{CC} = 14 V**
- **2-A Peak Output Current, V_{CC} = 14 V**
- **5-μA Supply Current — Input High or Low**
- **4-V to 14-V Supply-Voltage Range; Internal Regulator Extends Range to 40 V (TPS2811, TPS2812, TPS2813)**
- **−40°C to 125°C Ambient-Temperature Operating Range**

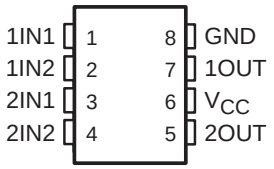
TPS2811, TPS2812, TPS2813 . . . D, P, AND PW PACKAGES
(TOP VIEW)



TPS2814 . . . D, P, AND PW PACKAGES
(TOP VIEW)



TPS2815 . . . D, P, AND PW PACKAGES
(TOP VIEW)



description

The TPS28xx series of dual high-speed MOSFET drivers are capable of delivering peak currents of 2 A into highly capacitive loads. This performance is achieved with a design that inherently minimizes shoot-through current and consumes an order of magnitude less supply current than competitive products.

The TPS2811, TPS2812, and TPS2813 drivers include a regulator to allow operation with supply inputs between 14 V and 40 V. The regulator output can power other circuitry, provided power dissipation does not exceed package limitations. When the regulator is not required, REG_IN and REG_OUT can be left disconnected or both can be connected to V_{CC} or GND.

The TPS2814 and the TPS2815 have 2-input gates that give the user greater flexibility in controlling the MOSFET. The TPS2814 has AND input gates with one inverting input. The TPS2815 has dual-input NAND gates.

TPS281x series drivers, available in 8-pin PDIP, SOIC, and TSSOP packages operate over a ambient temperature range of −40°C to 125°C.

AVAILABLE OPTIONS

T_A	INTERNAL REGULATOR	LOGIC FUNCTION	PACKAGED DEVICES		
			SMALL OUTLINE (D)	PLASTIC DIP (P)	TSSOP (PW)
−40°C to 125°C	Yes	Dual inverting drivers Dual noninverting drivers One inverting and one noninverting driver	TPS2811D TPS2812D TPS2813D	TPS2811P TPS2812P TPS2813P	TPS2811PW TPS2812PW TPS2813PW
	No	Dual 2-input AND drivers, one inverting input on each driver Dual 2-input NAND drivers	TPS2814D TPS2815D	TPS2814P TPS2815P	TPS2814PW TPS2815PW

The D package is available taped and reeled. Add R suffix to device type (e.g., TPS2811DR). The PW package is only available left-end taped and reeled and is indicated by the R suffix on the device type (e.g., TPS2811PWR).

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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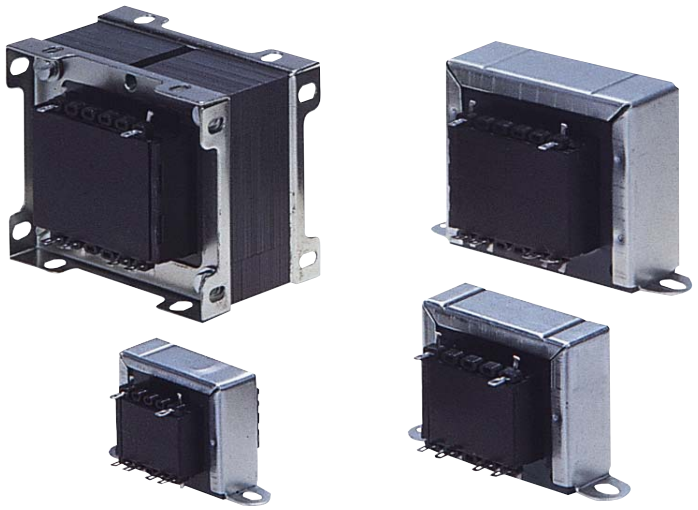
Chassis Mounting Transformers

230V Single Primary

6VA to 200VA



Features:

- Chassis mounting low voltage mains transformers with 230V ac primary winding.
- 2 secondary winding that can be connected in series or parallel.
- Double section bobbins on interleaved lamination provide 3.75kV isolation.
- Fixing by clamp on models up to 50VA, and frame construction above.
- Tested to meet EN60065.

Specifications

VA	Dimensions				Fixing Style	Weight (kg)	Typical Regulation (%)
	Width	Depth	Height	FC			
6	45	40	37	54	Clamp	0.2	25
12	59	50	50	72		0.4	12
20		56				0.55	10
50	79	62	65	92		1.0	
75		75	67	54 x 54	Frame	1.5	
100	89	68	75	57 x 44		1.6	
150	100	78	85	72 x 58		2.2	
200		90		72 x 68		2.8	7

Dimensions : Millimetres

Appendix D

List of the Available Digital Content

D.1 Matlab Files

D.1.1 Simulink Simulation Files

- Complete_model_1.mdl
- Complete_model_2.mdl
- Complete_model_3.mdl
- r_calculation.m
- Param.m

D.1.2 Simulink Control Models

- Test_ADC.mdl
- Test_PWM.mdl
- Test_closed_loop_1.mdl
- Test_closed_loop_2.mdl
- Test_closed_loop_3.mdl
- Test_open_loop_1.mdl
- Test_open_loop_2.mdl

D.2 EAGLE Files

D.2.1 Schematics

- power.brd
- signal.brd

D.2.2 Layouts

- power.sch
- signal.sch

D.3 Others

- All the complete datasheets of the components