

FAIRCHILD

A Schlumberger Company

2N6759/2N6760**N-Channel Power MOSFETs,
5.5 A, 350 V/400 V**

Power And Discrete Division

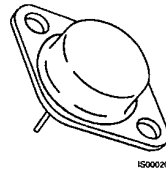
T-39-11

Description

These devices are n-channel, enhancement mode, power MOSFETs designed especially for high voltage, high speed applications, such as off-line switching power supplies, UPS, AC and DC motor controls, relay and solenoid drivers.

- V_{GS} Rated at ± 20 V
- Silicon Gate for Fast Switching Speeds
- I_{DSS} , $R_{DS(on)}$, Specified at Elevated Temperature
- Rugged
- Low Drive Requirements
- Ease of Paralleling

TO-204AA

2N6759
2N6760

2

Maximum Ratings

Symbol	Characteristic	Rating 2N6760	Rating 2N6759	Unit
V_{DSS}	Drain to Source Voltage	400	350	V
V_{DGR}	Drain to Gate Voltage $R_{GS} = 1.0 \text{ M}\Omega$	400	350	V
V_{GS}	Gate to Source Voltage	± 20	± 20	V
T_J , T_{slg}	Operating Junction and Storage Temperatures	-55 to +150	-55 to +150	$^{\circ}\text{C}$
T_L	Maximum Lead Temperature for Soldering Purposes, 1/16" From Case for 10 s	300	300	$^{\circ}\text{C}$

Maximum On-State Characteristics

$R_{DS(on)}$	Static Drain-to-Source On Resistance	1.0	1.5	Ω
I_D	Drain Current Continuous at $T_C = 25^{\circ}\text{C}$	5.5	4.5	A
	Continuous at $T_C = 100^{\circ}\text{C}$	3.5	3.0	
I_{DM}	Pulsed	8.0 ²	7.0 ²	

Maximum Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.67	1.67	$^{\circ}\text{C/W}$
P_D	Total Power Dissipation at $T_C = 25^{\circ}\text{C}$	75	75	W
	at $T_C = 100^{\circ}\text{C}$	30	30	
	Linear Derating Factor	0.6	0.6	W/ $^{\circ}\text{C}$

Notes

All values are JEDEC registered except as noted. For information concerning connection diagram and package outline, refer to Section 7.

Electrical Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Characteristic	Min	Max	Unit	Test Conditions
Off Characteristics					
$V_{(BR)DSS}$	Drain Source Breakdown Voltage ¹			V	$V_{GS} = 0\text{ V}$, $I_D = 1.0\text{ mA}$
	2N6760	400 ²			
	2N6759	350 ²			
I_{DSS}	Zero Gate Voltage Drain Current		1	mA	$V_{DS} = \text{Rated } V_{DSS}$, $V_{GS} = 0\text{ V}$
			4		$V_{DS} = \text{Rated } V_{DSS}$, $V_{GS} = 0\text{ V}$, $T_C = 125^\circ\text{C}$
I_{GSS}	Gate-Body Leakage Current		± 100	nA	$V_{GS} = \pm 20\text{ V}$, $V_{DS} = 0\text{ V}$
On Characteristics					
$V_{GS(th)}$	Gate Threshold Voltage	2.0	4.0	V	$I_D = 1.0\text{ mA}$, $V_{DS} = V_{GS}$
$R_{DS(on)}$	Static Drain-Source On-Resistance ¹			Ω	$V_{GS} = 10\text{ V}$
	2N6760		1.0		$I_D = 3.0\text{ A}$
	2N6759		1.5		$I_D = 3.5\text{ A}$
	2N6760		2.2		$I_D = 3.5\text{ A}$, $T_C = 125^\circ\text{C}$
	2N6759		3.3		$I_D = 3.0\text{ A}$, $T_C = 125^\circ\text{C}$
$V_{DS(on)}$	Drain-Source On-Voltage ¹		6.7	V	$V_{GS} = 10\text{ V}$; $I_D = 5.5\text{ A}$
	2N6760		7.0		$V_{GS} = 10\text{ V}$; $I_D = 4.5\text{ A}$;
	2N6759				$V_{DS} = 15\text{ V}$, $I_D = 3.5\text{ A}$
g_{fs}	Forward Transconductance ¹	3.0	9.0	S (Ω)	
Dynamic Characteristics					
C_{iss}	Input Capacitance	350	800	pF	$V_{DS} = 25\text{ V}$, $V_{GS} = 0\text{ V}$
C_{oss}	Output Capacitance	50	300	pF	$f = 1.0\text{ MHz}$
C_{rss}	Reverse Transfer Capacitance	20	80	pF	
Switching Characteristics ($T_C = 25^\circ\text{C}$, Figures 9, 10)					
$t_{d(on)}$	Turn-On Delay Time		30	ns	$V_{DD} = 175\text{ V}$, $I_D = 3.5\text{ A}$
t_r	Rise Time		35	ns	$V_{GS} = 10\text{ V}$, $R_{GEN} = 15\text{ }\Omega$
$t_{d(off)}$	Turn-Off Delay Time		55	ns	$R_{GS} = 15\text{ }\Omega$
t_f	Fall Time		55	ns	
Q_g	Total Gate Charge		30 ²	nC	$V_{GS} = 10\text{ V}$, $I_D = 7.0\text{ A}$ $V_{DD} = 180\text{ V}$

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Electrical Characteristics (Cont.) ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Characteristic	Min	Typ	Max	Unit	Test Conditions
Source-Drain Diode Characteristics						
I_S	Continuous Source Current 2N6760 2N6759			5.5 4.5	A	
I_{SM}	Pulsed Source Current 2N6760 2N6759			8.0 7.0	A	
V_{SD}	Diode Forward Voltage 2N6760 2N6759	0.75		1.5	V	$I_S = 5.5 \text{ A}; V_{GS} = 0 \text{ V}$
		0.70		1.4		$I_S = 4.5 \text{ A}; V_{GS} = 0 \text{ V}$
t_{rr}	Reverse Recovery Time		550^2		ns	$V_{GS} = 0 \text{ V}, T_J = 150^\circ\text{C}$ $I_F = I_{SM}, dI_F/dt = 100 \text{ A}/\mu\text{S}$
Q_{RR}	Reverse Recovery Charge		8.0^2		μC	$V_{GS} = 0 \text{ V}, T_J = 150^\circ\text{C}$ $I_F = I_{SM}, dI_F/dt = 100 \text{ A}/\mu\text{S}$

Notes

1. Pulse test: Pulse width $\leq 300 \mu\text{s}$, Duty cycle $\leq 2\%$
3. Non-JEDEC registered value.

Typical Performance Curves

Figure 1 Output Characteristics

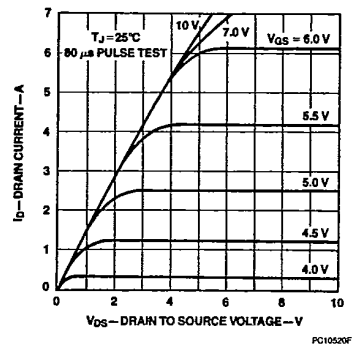
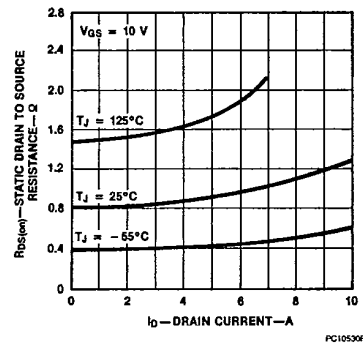


Figure 2 Static Drain to Source Resistance vs Drain Current



Typical Performance Curves (Cont.)

Figure 3 Transfer Characteristics

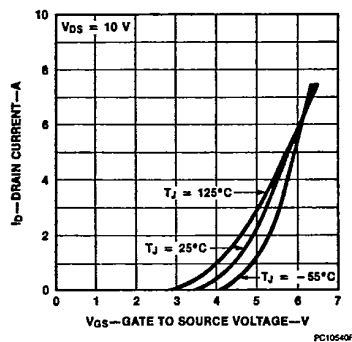


Figure 5 Capacitance vs Drain to Source Voltage

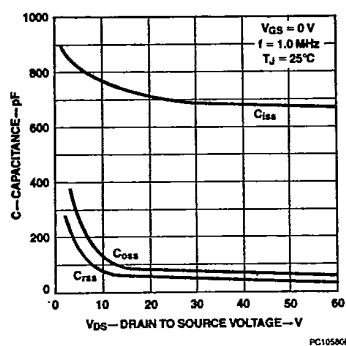


Figure 7 Forward Biased Safe Operating Area

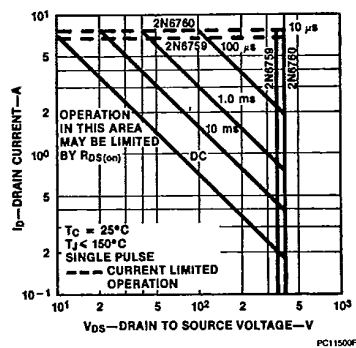


Figure 4 Temperature Variation of Gate to Source Threshold Voltage

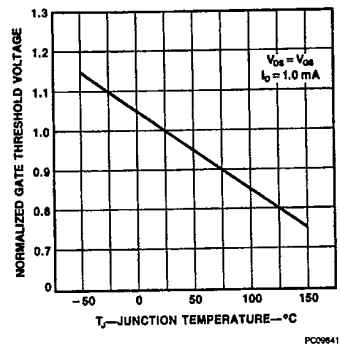


Figure 6 Gate to Source Voltage vs Total Gate Charge

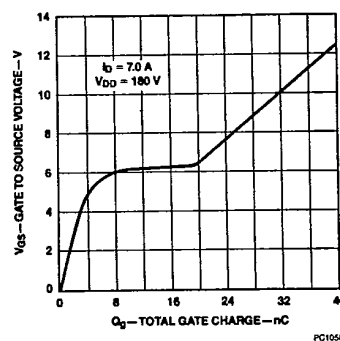
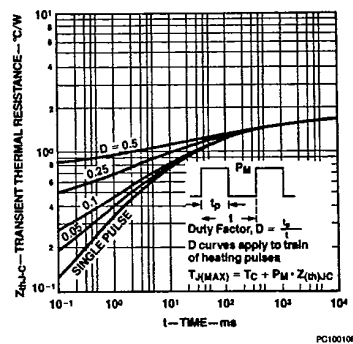


Figure 8 Transient Thermal Resistance vs Time



Typical Electrical Characteristics

Figure 9 Switching Test Circuit

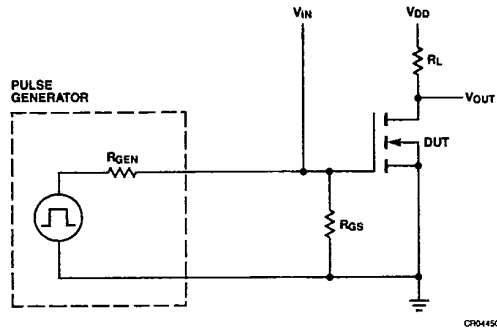


Figure 10 Switching Waveforms

