NTNU

Norwegian University of
Science and Technology

Development of a Grid Connected PV System for Laboratory Use

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Problem Description

A laboratory setup of a grid connected PV inverter system is currently under development at NTNU. The system will consist of a PV panel input, a converter stage consisting of a DC-DC converter, DC link and DC-AC converter, and a transformer stage. The finished system is intended for implementation at the University of Dar Es Salaam in Tanzania for teaching purposes in Power Electronics and Digital Control in PV Systems.

The focus of this master thesis is development of a control design for a DC-DC converter implemented in the PV system. This includes consideration of the input from the PV panels and the DC-DC converter stage. A DC-DC converter design is already available. The focus will be on hardware testing and evaluation, software development and interconnection of the hardware and software modules.

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Supervisor: Lars Einar Norum, ELKRAFT

Acknowledgements

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In this report a future PV system meant for laboratory use in the previous mentioned African University has been considered. The system will include PV modules for power input, a DC-DC converter for MPPT (Maximum Power Point Tracking) and a DC-AC inverter connected to the grid through a transformer. Previous to this master thesis Supratim Basu at Bose Research designed the circuit diagram for the DC-DC converter, and this prototype was built and tested during the fall 2008. The scope for this thesis has been on the control design of the DC-DC converter stage.

The theoretical background is written based on the assumption that the contents of this report will be read by people with some basic knowledge within the area. Some chapters are also a bit more comprehensive, with regards to students that will continue to work on this laboratory assignment in the future. Some information is based on knowledge gained through courses at the University as well as through working experience. Figures without reference I have mainly created myself or the reference is mentioned another place in the chapter.

I would like to give special thanks to my head supervisor Lars Norum for help and support and giving a push in the right direction at times when my focus has been unclear. The same applies for my co-supervisor Fritz Schimpf, to which I am very grateful for all the extra time spent on helping me and giving me useful advices along the way. Also thanks to Supratim Basu for designing the converter circuit, Vladimir Klubicka and Bård Almaas in the Servicelab and Ph.D. candidate Chee Lim for help and good advices. The work with my master thesis has been a highly instructive process. Especially the practical work has increased my knowledge about power electronics control and software development intended for this. Despite times of frustration I really recommend laboratory work as a way of working and learning.

Last, but not least, thanks to Ragnar Ulsund for providing social input throughout the spring of 2009 by arranging cake and coffee break once a week.

Silje Odland Simonsen
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Abbreviations

AC	Alternating Current
ADC	Analog-to-Digital Converter/Conversion
CCM	Continuous Conduction Mode
CC	Constant Current
CT	Continuous Time
CV	Constant Voltage
DC	Direct Current
DCM	Discontinuous Conduction Mode
DSP	Digital Signal Processor
EMD	Electromagnetic Discharge
EOC	End of Conversion
ESR	Equivalent Series Resistance
ePWM	Enhanced Pulse-Width Modulation
FCCM	Forced CCM
GPIO	General Purpose Input/Output
IC	Integrated Circuit
ISR	Interrupt Service Routine
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
MPP	Maximum Power Point
MPPT	Maximum Power Point Tracking
MSB	Most Significant Bit
P&O	Perturb and Observe
P	Proportional
PI	Proportional + Integral
POPI	Power In - Power Out
PV	Photovoltaic
PWM	Pulse-Width Modulation
SOC	Start-of-Conversion
STC	Standard Test Conditions
SMPS	Switched mode power supplies
TI	Texas Instruments

1 Introduction

The world energy consumption has within the recent decades become an important topic in the society, both in a political and social aspect. The energy production has mainly been based on energy sources like oil, gas and coal, which until recently was looked upon as close to inexhaustible. As the world energy consumption is growing with a drastically high rate and the fossil fuels reserves are shrinking, the need for renewable energy resources has gained more focus. Both renewable and non-renewable energy resources are mostly created by the sunrays hitting the surface of the earth. The sun is a non-polluting resource responsible for the sustained life on earth, and while non-renewable energy resources has been generated over a long period, renewable energy resources is broadly speaking always available. Among the renewable energy resources are hydro power, wind power and solar energy. While hydro power has been a well known technology for a long time, there is a lot of research going on with wind and solar power today [13].

Solar energy as a energy source has a large theoretical potential, and can be utilized both directly and indirectly. The potential is especially large on the African continent. The climate change is a global environmental problem that might affect especially people in developing countries, as many of these human beings already suffer from difficult living conditions. The solar irradiance at the African continent is considerable and there is a great need of developing knowledge on how to utilize the solar energy to increase the living standards [10].

In this master thesis a grid connected PV inverter system will be studied. The PV system will utilize the solar energy as the power source and transfer the power into the grid through conditioning by power electronics. The power electronics is an essential part of a PV system, and it is necessary to understand how to utilize and control this part for optimization of the power generation. To support the teaching in control of the power electronics through digital signal processing, a laboratory setup of the PV inverter system is under development. The long term goal is to implement this laboratory setup in an African University, primarily in Dar es Salaam, Tanzania, and Makerere, Uganda. These two countries have a quite similar energy situation, where a mixture of grid connected and isolated systems has lead to tapped energy resources. This has again lead to a striving for utilization of renewable energy sources, with solar energy as the most important (more information about this can be found in [11], [9] and [34]).

The system to be considered is shown in figure 1. The low voltage level in the grid in Tanzania and Uganda, to which this system will be connected, is ranging from 240 V to over 400 V. But as this particular system is meant for laboratory use on a University level, the voltage level needs a modification for safety reasons. To ensure that the voltages are not dangerous for students doing experiments, the voltage level has been planned to be around 48 V. The panels will produce an output that lies within the range of 0-60 V. The same range will also be applied at the output of the DC-DC converter. The inverter stage must produce an output voltage proportional to the grid voltage level. Hence it must

consider both the grid voltage as well as the output voltage from the DC-DC converter and adjust the inverter operation from this information. To be able to connect to the grid, a transformer is included between the inverter stage and the grid.

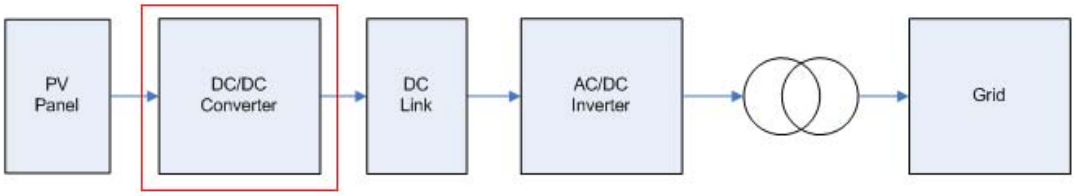


Figure 1: Simplified sketch of the circuit

The system has a quite simple structure, consisting of the following parts:

1. A **PV panel** producing the power input
2. A **DC-DC converter** creating a potential difference between input and output
3. A **DC link** for energy storage and filtering
4. An **inverter** for interconnection to the grid
5. A **transformer** for transformation from low voltage (LV) to grid voltage (HV)

The system can be divided in three main parts which are to be considered; these are the PV panels, the power electronics and the control system. The PV panels are the point of power input and the main emphasis will be on how to extract the maximum power from the panels at any time through power conditioning by the power electronics stage. This stage includes the DC-DC converter, the DC link and the inverter. The DC-DC converter is responsible for Maximum Power Point Tracking, while the inverter is keeping the DC link voltage on a constant level. The DC link is decoupling each of the converter stages and its purpose is to act as an energy storage element and filter. To obtain a stable system operation the voltages in the system need to be monitored and controlled. This is accomplished by implementing a control system through digital signal processing.

Previous to this master thesis a master project was performed. In this project the main emphasis was on exploring and developing parts of the hardware needed in the PV system. A DC-DC converter designed by Supratim Basu at Bose Research in India was built and tested, with regards to functionality and possible improvements. The project resulted in a operating converter, suitable for the purpose intended. With the hardware part of the specified part of the system in operation, the next step is to look at the software.

In this master thesis the main focus will be on developing software suitable for control of the DC-DC converter stage in addition to a hardware interface between the converter and the hardware of the control system.

2 Background

In this section a presentation of a PV system together with some additional theory will be given. Part of the theory is similar to the one given in the previous master project. This is done to be able to present the master thesis as a complete piece of work, independent of the master project. Some parts have also been altered and extended.

2.1 What is a PV system?

The term PV is short for photovoltaic, which means that the system is designed around the photovoltaic cell. This cell by itself has a small power output and has a maximum power generation of less than 3 W (normally between 1 and 2 W)[1]. The required power output is in most realistic situations a lot higher than this, and to produce this amount of power many PV cells are connected in series to PV modules. For even higher power output PV modules are connected together to PV arrays. A more detailed description of each of these units will be given later in this chapter. The theoretical background about the PV system is mainly based on the references [32], [42], [40] and [41].

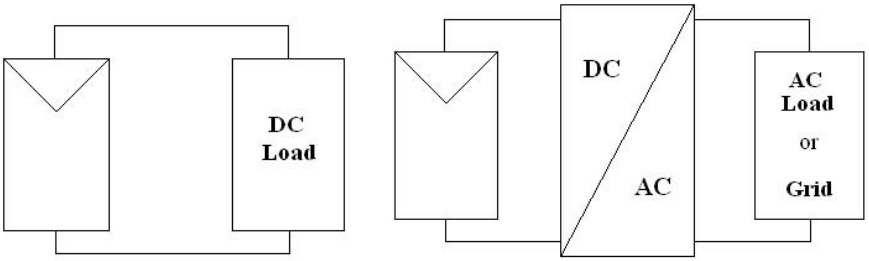
The photovoltaic part alone does not represent a whole PV system; a connection to other elements called BOS ("Balance of system") components is required [38]. The BOS components are typically energy storing mechanisms (like batteries or capacitors), charge control and power electronics conditioning the input power to a preferred output (DC-DC converters or DC-AC inverters). It is important to note that the load is also considered a part of the PV system.

The PV cell produces a DC output, which indicates that the choice of components in a PV system must be done based on the area of application. In a stand-alone system (solar home system) the photovoltaic part is often directly connected to a DC load. In a system connected directly to the grid or an AC load an inverter is needed to get a suitable power output. Figure 2 shows the most basic structures of each of the system structures.

2.1.1 Stand-alone system

In a stand-alone system the simplest structure will be as in figure 2a with the PV panel connected directly to the load. This system will in most situations produce a power output dissimilar to the optimal output available. As will be shown later in this chapter other components must be added to get a more efficient system. Because of the varying power input in solar cells, it is typical to add energy storing components (i.e. batteries) to ensure a continuous output. When batteries are implemented in the system, charge controllers have to be added. These controllers avoid discharge and overcharge of the

[1] The normal rating of a PV cell is normally 0.5-0.6 V and 2.0 A



(a) DC load (b) AC load or grid connection

Figure 2: PV system with DC and AC load or grid connection

batteries. When the batteries are fully charged, the PV panels are disconnected to avoid overcharging, and when the batteries are discharged the load is disconnected. The charge controllers will provide for optimal charging and discharging depending on several parameters, as temperature, load conditions and power input from the PV panels.

2.1.2 Grid connected system

In a DC-AC grid connected system it is not so common to add batteries as energy storage. This is due to the fact that the grid can be utilized as an "unlimited" energy source or sink, thus additional energy storage is unnecessary.

2.2 The working principle of photovoltaics

It is important to understand how the photovoltaic system is compounded and how it works when exposed to sunlight. As mentioned earlier, the photovoltaic part is the power source in the system. The task of the photovoltaic part is direct transformation of the solar irradiance into electricity, and the physics behind this transformation will now be examined.

2.2.1 The Photovoltaic cell

The photovoltaic (PV) cell is the smallest constituent in a photovoltaic system. A PV cell is a specially designed pn junction (a semiconductor), mainly silicon based and the power input is made possible by a phenomenon called the photoelectric effect. The characteristic of photoelectric effect was discovered by the French scientist, Edmund Bequerel, in 1839, when he showed that some materials produce electricity when exposed to sunlight. The photons in the light are absorbed by the material and electrons are released, which again creates a current and an electric field because of charge transfer. The nature of light and the photoelectric effect has been examined by several scientists the last century, for instance Albert Einstein, which has lead to the development of the solar cell as it is today [32].

An ideal PV cell can be modeled as an ideal current source in anti-parallel with a diode. The current on the terminals of the PV cell will then be the difference between the photon current I_l and the diffusion current through the diode. This can be expressed as:

$$I = I_l - I_o(e^{\frac{qV}{mkT}} - 1) \tag{1}$$

where:

I_l is the component of cell current due to photons [A]

I_o is the reverse saturation current[A]

V is the cell voltage [V]

T is the cell temperature [K]

q = 1.6e-19 [C°]

k = 1.38e-23 [j/K] Boltzmann's constant

m is the ideality factor (m=1 for an ideal cell)

The current equation shows that the PV cell is limited both in current and voltage. For low voltage or during short circuit the exponential term will have a minor influence on the current, which gives an approximately constant current equal to the sum of the cell

current I_l and the reverse saturation current I_o. As the voltage is increased the exponential term will increase accordingly and eventually the voltage will reach a maximum where the cell current equals zero (open circuit). The current in the cell can not go negative.

This representation of the PV cell can be made more realistic as shown in figure 3 (reference [23]). Here R_S and R_{SH} are the series and shunt resistances respectively and account for the parasitic losses in the PV cell. Ideally the shunt resistance should be close to infinity and the series resistance close to zero.

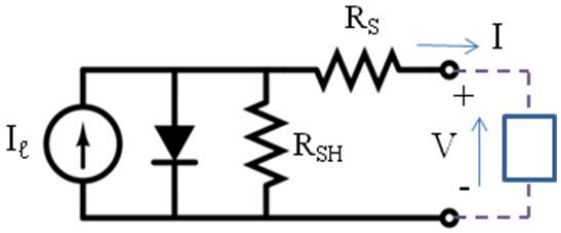


Figure 3: Simplified equivalent circuit of a PV cell

With the inclusion of the parasitic losses, the current equation will be slightly different. A current will also flow through the shunt resistance and an extra term will be subtracted from the original equation. As the series resistance is rather small, the extra term will reduce due to the negligible voltage loss over R_s. This can be seen in equation 2. However, as the shunt resistance is assumed close to infinity this term is disregarded in further examinations.

$$I = I_l - I_o(e^{\frac{qV}{mkT}} - 1) - \frac{V + I \cdot R_s}{R_{sh}} = I_l - I_o(e^{\frac{qV}{mkT}} - 1) - \frac{V}{R_{sh}} \tag{2}$$

The limitations on voltage and current mean that the cell is not harmed when operating under open circuit or short circuit conditions. The short circuit is the maximum current appearing when the voltage is set to zero, for a given irradiance and temperature. This leads to $I_{sc} = I_l$ (see equation 1).

The open circuit voltage is the maximum voltage for a given light and temperature when the cell current is set equal to zero:

$$V_{OC} = \frac{kT}{q} ln \frac{I_l + I_o}{I_o} \cong \frac{kT}{q} ln \frac{I_l}{I_o} \tag{3}$$

The power output of a PV cell is given by multiplying the current and the voltage that belongs together on the I-V characteristic. On background of the high cost and general request for high efficiency it is desired to optimize the power output from the PV cell, and the maximum power point (MPP) in a solar cell is given by:

$$P_{MPP} = V_{MPP} \cdot I_{MPP} \tag{4}$$

The characteristic of an ideal PV cell with the maximum power point is shown in figure 4 (reference [40]).

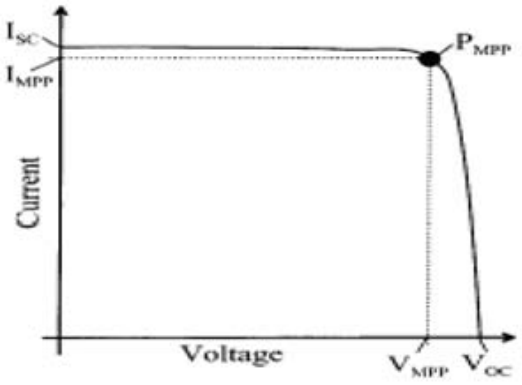


Figure 4: Ideal PV cell with maximum power point

A general rule for the MPP is that it is always found on the knee of the characteristic, where the hyperbola of "I*V = constant" is tangent to the I-V characteristic in only one point. If a hyperbola strikes the characteristic in more than one point, the maximum power point for that particular characteristic is not yet found. Another common way of finding the maximum power point is to plot the cell power vs. cell voltage. It's worth to add that the value of V_{MPP} is normally around 80 % of V_{OC} and I_{MPP} is around 91 % of I_{SC}.

The quality of the cell is given in terms of the fill factor FF. The fill factor gives the share of the theoretically maximum power output that is actually produced:

$$FF = \frac{P_{MPP}}{I_{SC} \cdot V_{OC}} \tag{5}$$

The fill factor is dependent of the internal resistance of the cell, where the ideal cell will have a FF = 1 (this is not yet possible with today's technology). In real cells today the fill factor varies between 0.5-0.8.

Conditions that influence the working operation of PV cells

- Temperature

  The temperature of the PV cell is an important parameter that has to be taken into consideration in PV system operation. The PV cell has given temperature coefficients for both the current (β) and the voltage (-α). The current coefficient is mostly negligible, hence it is mainly the voltage temperature coefficient that is considered during calculations. For silicon based cells the coefficient $\alpha = 2.3\frac{mV}{C^\circ}$ per cell. This can also be seen in equation 1, where the diode is used to include the temperature coefficient.

- Irradiance

  In this case the impact of irradiance on the cell voltage is negligible, and thus it is the short circuit current that is considered in calculations. This current is normally set proportional to the irradiance E (given in $\frac{kW}{m^2}$):

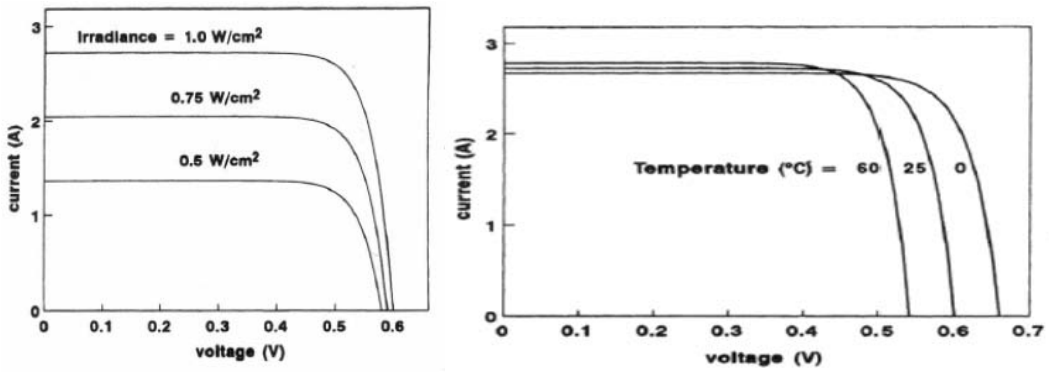
$$I_{SC}(E) = I_{SC}(at\_STC) \cdot E \tag{6}$$

Standard Test Conditions (STC) [12] is the universal industrial standard of laboratory test conditions under which PV cells can be used. There are three factors in this standard[2]:

Table 1: Standard test conditions (STC)

	Notation	*Value*	*Unit*
Irradiance	E	1	$\frac{kW}{m^2}$
Air mass	AM	1.5	-
Cell temperature	T	25	C°

Figure 5 shows the I-V characteristics for different values of irradiance and temperature. While changing the irradiance level the temperature is assumed constant, and vice versa. Here it is quite evident that when the PV cell is operated away from the MPP the cell in reality operates as either a constant voltage source or a constant current source.



(a) Irradiance (b) Temperature

Figure 5: I-V characteristics for different levels of irradiation and temperature

It should be emphasized that during the open circuit or short circuit conditions there is no power production, given as one of the parameters is zero in each case.

The power vs. voltage characteristic for STC, as well as different levels of irradiance and temperature is shown in figure 6. Both figures 5 and 6 are taken from reference [40].

[2]Air mass indicates the clarity of the air that the sunlight passes trough

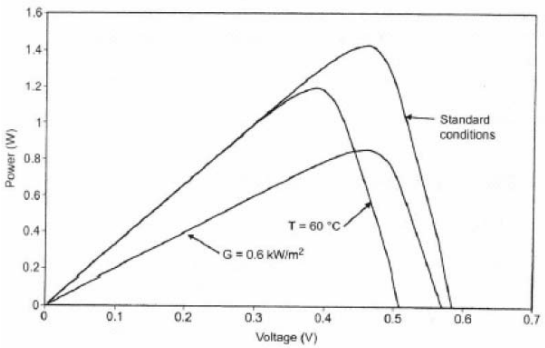


Figure 6: P-V characteristic of a PV cell

2.2.2 The Photovoltaic Module

In most practical situations the output from a single PV cell is smaller than the desired output. To get the adequate output voltage, the cells are connected in series into a PV module. The industry standard is 12 V PV modules, and with a voltage output of 0.5-0.6 V of each cell it would be fair to assume a series connection of about 20-24 cells. But as the goal is to keep the voltage V_{MPP} within a satisfactory range (around 12 V) during average irradiance, a safety margin must be included. The standard number of cells connected in series to get 12 V in a module is around 36, and the module is able to generate around 70-100 W.

When making a module, there are a couple of things that need consideration.

- No or partly illumination of the module

  During the night, when none of the modules are illuminated, an energy storage (like a battery) connected directly in series with the modules makes the cells forward biased. This might lead to a discharge of the energy storage. To prevent this from happening a **blocking diode** can be connected in series with the module. But during normal illumination level this diode represents a significant power loss.

- Shading of individual cells

  If any of the cells in a module is shaded, this particular cell might be forward biased if other unshaded parts are connected in parallel. This can lead to heating of the shaded cell and premature failure. To protect the system against this kind of failure, the modules contain **bypass diodes** which will bypass any current that cannot pass through any of the cells in the module.

It's important to emphasize the importance of connecting PV cells with the same I-V characteristic. To optimize the generation, the maximum available output should occur at the same irradiance level for all the modules. This implies equal voltage for parallel connection and equal current for series connection. If the characteristics vary, some cells

might generate power while others are dissipating power.

The placement of bypassing and blocking diodes in the system is shown in figure 7 [19].

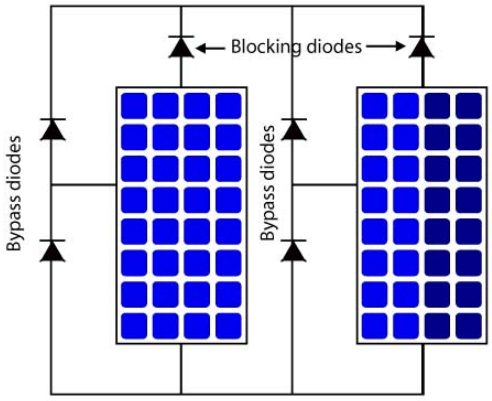


Figure 7: A PV module with bypass and blocking diodes

2.2.3 The Photovoltaic Array

If the output voltage and current from a single module is smaller than desired, the modules can be connected into arrays. The connection method depends on which variable that needs to be increased. For a higher output voltage the modules must be connected in series, while connecting them in parallel in turn gives higher currents. It is important to know the rating of each module when creating an array. The highest efficiency of the system is achieved when the MPP of each of the modules occurs at the same voltage level.

The relation between each of the PV parts are shown in figure 8 (reference [41]).

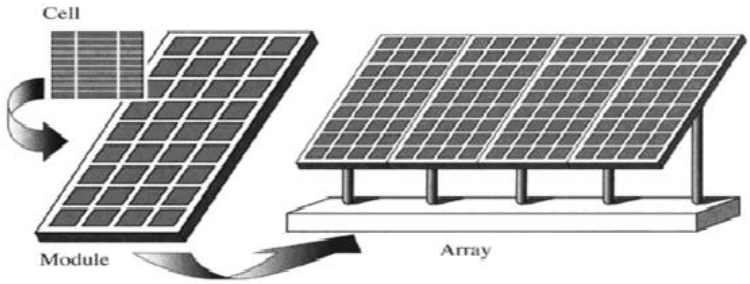


Figure 8: Relation between the PV cell, a module and an array

The term PV panel will be used from now on when referring to the photovoltaics of the system, independent of what composition will be used later.

2.3 Power electronics in a PV system

The voltage produced by the photovoltaic cells will vary according to the sunlight intensity (irradiance), but the system output requires a constant voltage value. To be able to process and control the electric energy in the system (i.e. the voltages, currents, frequency) there is a need for a power electronic interface. A typical setup of a power electronic system is shown in figure 9. The power flows from the input to the output through a processor stage, which is controlled through a negative feedback signal from either the input or the output (or both). The theory about the power electronics is mainly based on references [33], [14] and [30] and all the figures are collected from these references (some with modifications).

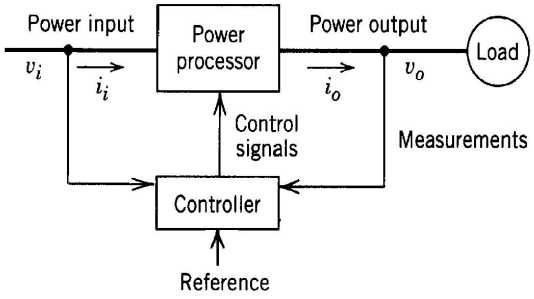


Figure 9: Block diagram of a power electronic system

The power input can be a DC as well as an AC signal. The output depends on the requirement from the load. In a PV system the power input will always be a DC signal given by the functionality of the PV cell (which is varying with the amount of energy absorbed from the sun).

The power processor can be described as a power conversion stage. It typically consists of one or more converters, often with an energy storage element included. A PV system intended for grid connection usually has a power processor as shown in figure 10. In the system considered in this master thesis Converter 1 corresponds to a DC-DC converter, while Converter 2 is a DC-AC converter (inverter). This way the output is connected directly to an AC load or to the grid.

The controller can be implemented to control both the converters separately to ensure a stable interface between each of the stages, i.e. between the input and Converter 1, the two converter stages, and Converter 2 and the output.

2.3.1 DC-DC Switch Mode Converters

The purpose of DC-DC Switch Mode Converters in general DC power supplies is to convert unregulated DC input to regulated or controlled DC output at a desired voltage

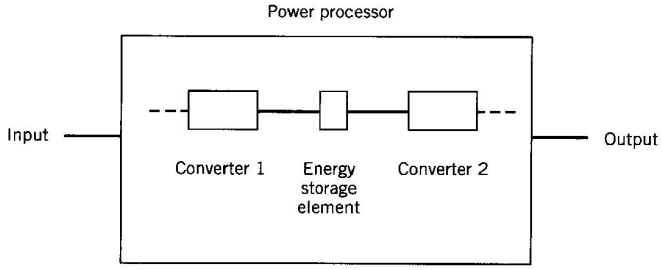


Figure 10: Block diagram of a power processor

level. In such systems the input is often fluctuating due to rectification and the output is requiring a constant output. In a PV system, on the other hand, the DC-DC converter is actually controlling the input by considering the unregulated output. By help of MPP Tracking (which will be explained later) the converter adjusts its operation according to the output value to find the optimal operating voltage of the PV module.

There are several different kinds of DC-DC converters in use in the industry today, but most of them are based on two basic converter topologies:

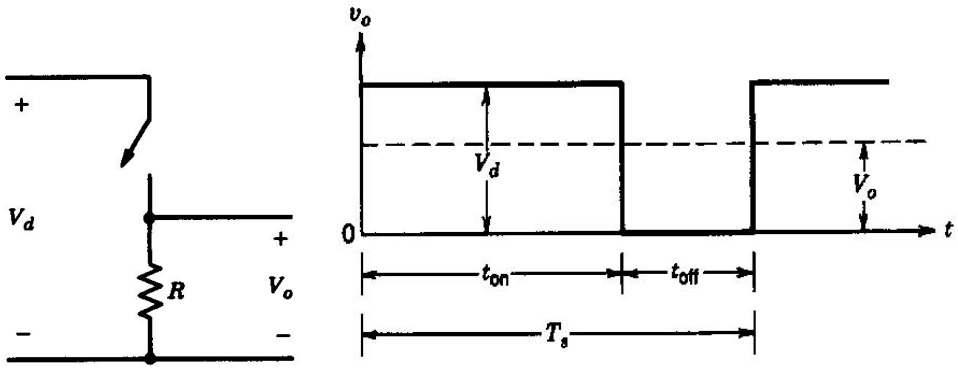
- Buck converter (step-down)
- Boost converter (step-up)

Each of the topologies will be explained later in the report.

Control of DC-DC converters The voltage transformation in a DC-DC switch mode converter is done by utilizing switches, hence the name "switch mode converters". The switches are controlled to be on and off for a certain amount of time through a method called pulse width modulation (PWM). The switching period $T_s = t_{on} + t_{off}$ (and hence the frequency) is held constant while the ratio of the on time to the switching time is varied. This ratio is called the switch duty ratio D, or duty cycle. By using switch mode control in the circuit in figure 11a, the output voltage v_o will be a constant pulse as shown in figure 11b. Because of inductive and capacitive circuit elements in the converter topologies the output voltage may have a certain amount of ripple, but the average output voltage should be constant (given as the dashed line V_o).

The switch control signal can be generated by comparing a control value (which most often is an amplified error) to a repetitive waveform v_{st}. The control value may be the difference between the actual and the desired output voltage V_o (as seen in figure 12. The effects of the comparison are:

- when $v_{control} > v_{st}$: switch on
- when $v_{control} < v_{st}$: switch off



(a) Switch mode circuit (b) Switch mode graph

Figure 11: The principle of switching

The duty cycle D can now be defined in two different ways:

$$D = \frac{t_{on}}{T_s} = \frac{v_{control}}{\hat{V}_{st}} \tag{7}$$

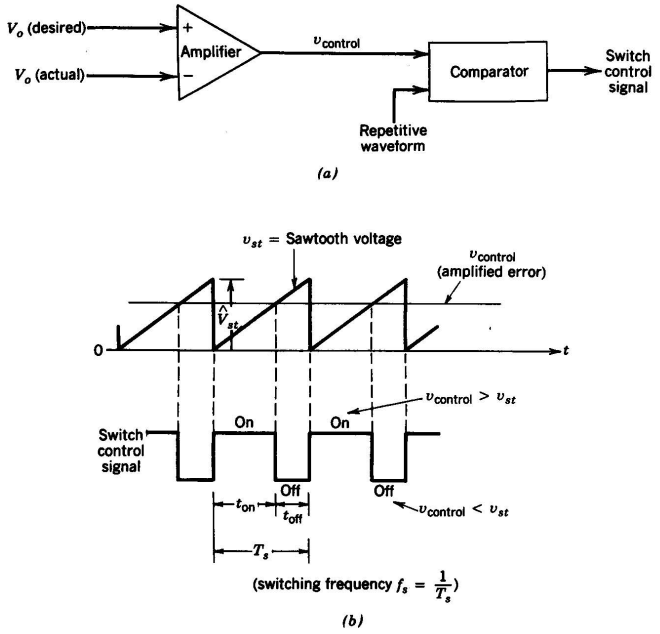
The frequency (and T_s) can also be varied in a PWM switching mode. This method might make it hard to filter the ripple components in the converter waveforms, and will not be used in the master thesis. Thus there will be no further explanation on this subject.

Common for both the converter topologies is the direction of transferred energy. The energy is unidirectional, which means that it can be transferred in one direction only. As there is seldom a requirement of a bidirectional flow in a grid connected PV system, the buck and boost converter topologies are more than sufficient for this application.

In the following sections the converter topologies will be analyzed with steady state conditions, the switches are assumed to be ideal and losses in the capacitors and inductors are neglected. In addition the switching time is assumed much shorter than the electric time constant of the circuit. Then the model analysis will be extended to include perturbation in the converter operation.

2.3.2 Steady state analysis

When analyzing each of the converter topologies, it is first assumed that they operate in steady state. This implies a constant duty cycle, which means that the current starts from the same value at the beginning of every switching cycle. Due to the inductor the current will charge and discharge through one cycle, and steady state condition implies that $\triangle I_{on} = \triangle I_{off}$. The change in current is the only factor deciding whether or not the



Pulse-width modulator: (*a*) block diagram; (*b*) comparator signals.

Figure 12: The principle of PWM control

system is in steady state. In a DC-DC converter with an optimal design it is assumed that the switching ripples are very small compared to the average values, often less than 1 %. This is often referred to as the small or linear ripple approximation.

- **Buck converter**

The buck converter is often referred to as a step-down converter, and as the name implies, the converter produces a lower DC voltage output than the input. The circuit of the buck converter can be seen in figure 13.

This circuit is an improved version of the circuit in figure 11a. The resistive load is replaced by a diode to overcome the problem of stored inductive energy that will normally appear in the circuit. In figure 11a this energy can harm the switch because there are no other components that can dissipate it. Secondly a low-pass filter is used to reduce the output voltage fluctuations as much as possible. This is achieved by wise selection of filter parameters to reduce the corner frequency f_c (this will also be explained later). The output voltage v_o will be as in figure 11b.

The buck converter will have different circuit schemes for each of the switch positions. To obtain the relationship between the input and output of the converter (and hence the duty cycle) the current through the inductor will be examined. The filter capacitor is assumed to be so large that $v_o(t) = V_o$, which means that no current will flow through it.

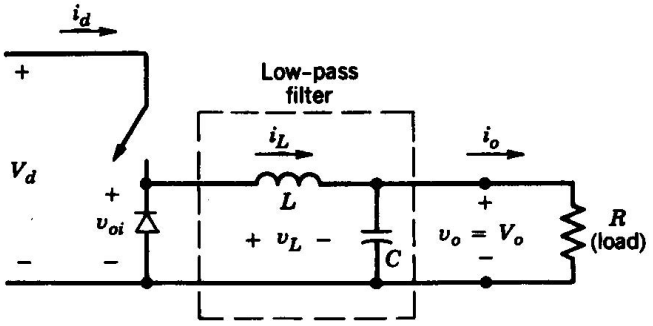


Figure 13: Buck converter

Thus it can be concluded that the inductor current equals the output current for both switch positions. The earlier assumption about the system being in steady state implies that the voltage and current waveforms repeat for each time period T_s. This can be seen by considering each of the circuits in figure 14.

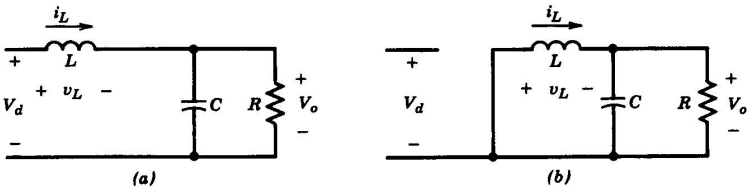


Figure 14: Buck converter circuit for a) t_{on} and b) t_{off} in CCM

When the switch is on, the input voltage V_d leads to a linear increase in the inductor current. As the switch is turned off, the diode becomes forward biased and the stored energy in the inductor makes the current continue to flow. But as the energy is transferred from the inductor to the load, the current is decreasing again.

The inductor voltage is given as:

$$v_L = L\frac{di_L}{dt} \tag{8}$$

As the inductor voltage is repeating itself for each time period, the change for each period is zero:

$$(i_L)_{on} = (i_L)_{off}$$

$$\int_0^{t_{on}} v_L dx = \int_{t_{on}}^{T_s} v_L dx$$

By considering the voltage curve in figure 15 the equation can easily be solved:

$$(V_d - V_o)t_{on} = V_d(T_s - t_{on})$$

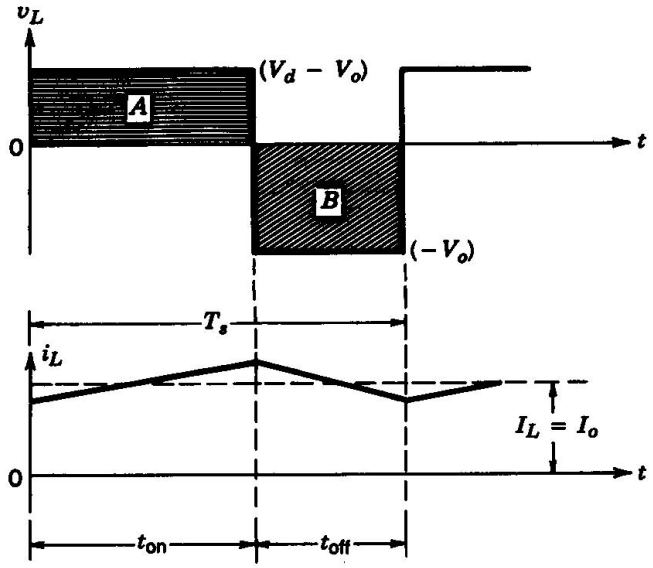


Figure 15: Inductor voltage and current of the buck converter

By some rearrangement, the relationship between the input and the output voltage is found:

$$\frac{V_o}{V_d} = \frac{t_{on}}{T_s} = D \tag{9}$$

The buck converter is actually equivalent to a transformer where the turns ratio is changed by varying the duty cycle. This can be shown mathematically by considering the power input and output. Neglecting the losses in the circuit gives the following relations:

$$P_d = P_o$$
$$V_d I_d = V_o I_o$$

$$\frac{V_o}{V_d} = \frac{I_d}{I_o} = D \tag{10}$$

This is also referred to as a POPI (Power In - Power Out) type converter [17].

Output voltage ripple in a buck converter The theoretical value of the filter capacitor is assumed to be so large that the output voltage is constant. But in a realistic buck converter this will not be the case, and there will be produced a ripple in the output voltage.

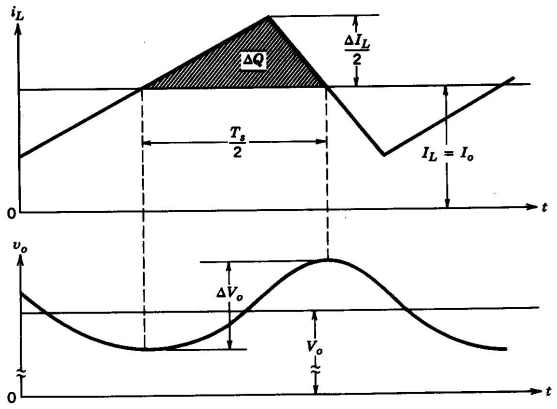


Figure 16: Output voltage ripple in a buck converter

The inductor current consists of two components, an average component flowing through the resistive load, and a ripple component assumed to flow through the capacitor. The ripple current introduces an additional charge $\triangle Q$, which can describe the ripple voltage:

$$\triangle V_o = \frac{Q_c}{C} = \frac{1}{C}(\frac{1}{2}\frac{T_s}{2}\frac{\triangle I_L}{2}) = \frac{1}{8C}\triangle I_L T_s \tag{11}$$

To minimize the ripple, the low-pass filter has to be selected so that the corner frequency $f_c = \frac{1}{2\pi\sqrt{LC}} \ll f_s$. This deduction is done assuming the ESR, which is the resistive part of the capacitor and inductor impedances, to be negligible.

- **Boost converter**

As opposed to the buck converter, the boost converter produces an output voltage which is higher than the input voltage. The circuit is according to figure 17.

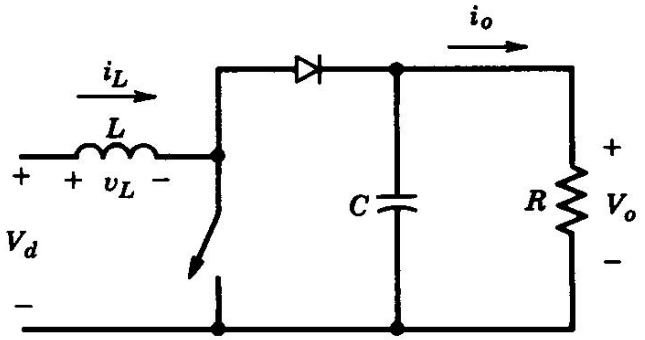


Figure 17: Boost converter

This topology also has different circuit schemes depending on the state of the switch, as seen in figure 18. When the switch is on the output stage is isolated from the input caused by the reverse biased diode. The input will supply the inductor with a constant voltage, and the inductor current will increase according to equation 8. When the switch is turned off, the output will be supplied both by the input and the inductor, and the current through the inductor will decrease because of this energy transfer.

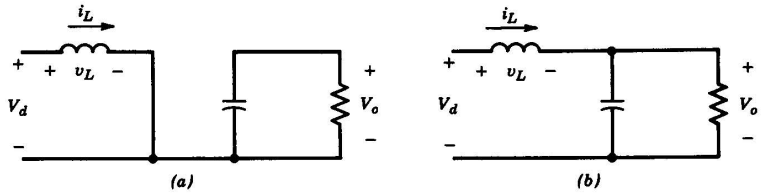


Figure 18: Boost converter circuit for a) t_{on} and b) t_{off} in CCM

The voltage and current graphs of the inductor through one time period is shown in figure 19. The shapes are equal to those of the buck converter, but the voltage of the inductor is different due to the placement of the switch and the diode.

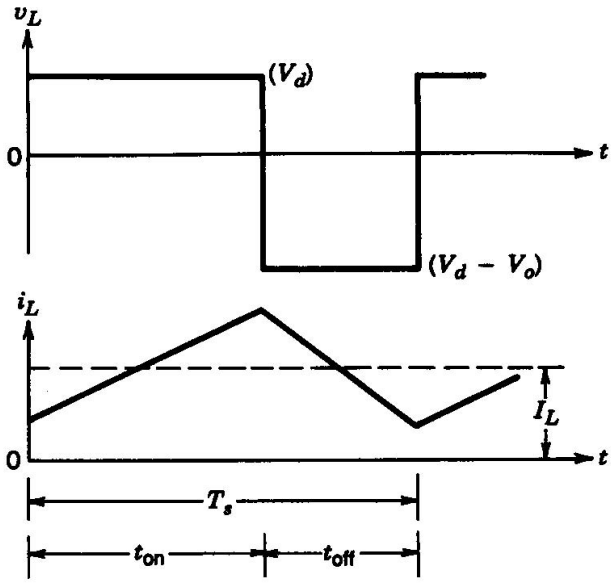


Figure 19: Inductor voltage and current of the boost converter

The same considerations regarding the inductor current can be done for this converter as in the previous section, which leads to the connection:

$$V_d t_{on} = (V_o - V_d)(T_s - t_{on})$$

After some rearrangements the equation becomes:

$$\frac{V_d}{V_o} = (1 + D) = \frac{I_o}{I_d} \tag{12}$$

The last term of the equation is yielded from the assumption of no power loss in the circuit (i.e. P_{in} equals P_{out}), and as for the buck it is referred to as a POPI converter.

Parasitic elements In a boost converter there will be losses due to the switches, the diode, the capacitor and the inductor. When the duty cycle gets close to one, the output voltage will theoretically increase against infinity, but due to the parasitic elements the ratio of V_o on V_d will actually go to zero. The ideal and the real characteristic of the conversion ratio versus duty ratio is shown in figure 20.

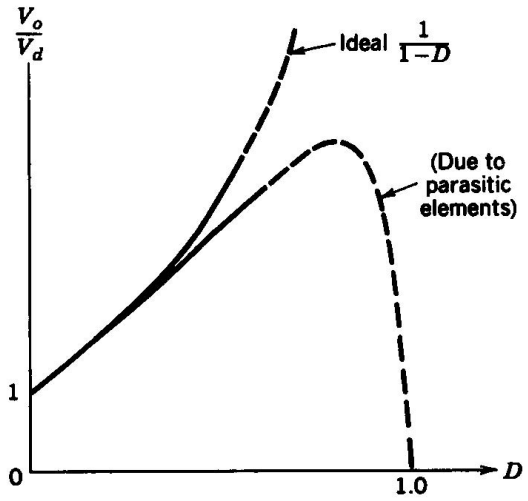


Figure 20: The effect of parasitic elements in a boost converter

In general the parasitic elements will seldom have a big impact because the duty ratio goes into saturation before entering the steep slope of the parasitic curve.

Output voltage ripple in a boost converter The output voltage ripple will also be present in a boost converter due to the capacitor value. When the switch is on the stored energy in the capacitor will be sent to the load, causing a discharge and decreased voltage. When the switch is off the capacitor is charged again by the input.

The ripple voltage $\triangle V_o$ can be written as:

$$\triangle V_o = \frac{Q_c}{C} = \frac{I_o D T_s}{C} = \frac{V_o}{R}\frac{D T_s}{C} \tag{13}$$

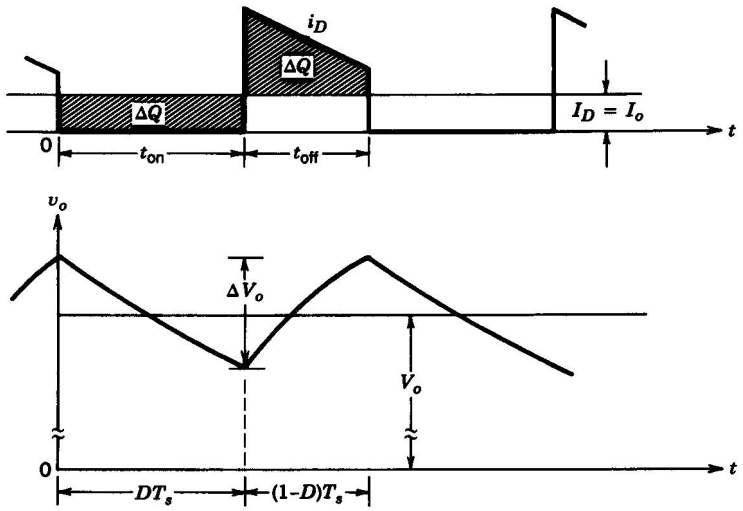


Figure 21: Output voltage ripple in a boost converter

This equation can also be utilized to find a capacitor value suitable for the circuit, choosing a worst case tolerated value of the ripple $\triangle V_o$. Normally the values D and R are dependent on the operation, but when calculating for a specific point of operation these values are known.

2.3.3 CCM cs. DCM

With steady state conditions the system can operate differently, depending on the starting point of the current. When the average of the current stays at a non-zero value throughout (which implies that $i_L(kT_s) > 0$), the system is operating in so-called Continuous Conduction Mode (CCM). When the current on the other hand goes to zero before the end of every cycle, the system is in the Discontinuous Conduction Mode (DCM). The condition where the current starts and ends at zero every cycle with continuous conduction is referred to as the boundary conduction mode (BCM). For normal operation the CCM is most common, but at light loads (increased load resistance) the DCM is advantageous as it causes less power losses in the circuit. The transition from CCM to DCM happens when the load current decreases, hence the output power is reduced or the input voltage is increased. All of the deductions done with Buck and Boost converters up till now has assumed CCM.

Most conventional topologies goes by the name "non-synchronous", where a diode is included to prevent current from flowing in the wrong direction. The topologies described in the previous chapters belongs to this category. However, this diode is also the reason why the system goes from CCM to DCM, because any negative current is denied access through the diode. So-called "synchronous" topologies have become more common in

the industry today, where the diode is replaced by a MOSFET switch in anti-parallel with the diode. By doing this, DCM is prevented from happening because the current is allowed to go negative through the switch and hence away from the load. The power loss in the MOSFET is a lot lower than across a diode and the conduction losses is reduced. So when the output power is lowered, the converter will not go into DCM, but rather Forced CCM [30].

2.3.4 Small signal AC modeling

In a dynamic system with closed loop (feedback) control where either the input or the output conditions change over time, there will be transitions between steady state operating points. This is due to the perturbation in duty cycle requested by the control system. The analysis of DC-DC converters must be extended from steady state analysis to consider the dynamic variations caused by the reactive circuit components (inductor and capacitor) when the system variables are susceptible to changes. This kind of analysis is referred to as small signal analysis, where the system is analysed when exposed to small variations. As for steady state conditions, the switching ripples in this analysis are assumed to be small compared to the average value and are further ignored.

In this analysis the system is linearized, assuming the signal disturbances so small that no parts of the system will go into saturation or become unstable (hence the name "small signal modeling"). By linearizing the power stage, a transfer function can be developed, and the controller of the system can be determined through utilization of the Nyquist stability criterion and Bode plots (these terms are explained in detail in the references [2] and [36]). It must be noted, however, that this method provides the tools for developing a transfer function only valid for either CCM or DCM.

When the duty cycle is exposed to perturbation, it will be a sum of the steady state duty cycle D and an introduced ac term:

$$d(t) = D + D_m \cdot cos(\omega_m t) = D + \tilde{d} \tag{14}$$

where the $\sim$ symbol indicates the perturbation, the value of D_m is a lot smaller than D and the frequency ω_m is much smaller than the switching frequency of the converter. All variables in the system can be written like this, as the sum of a DC term and an AC perturbation term. In a PV system where the DC link voltage is assumed to be constant, the AC term will disappear.

The method for creating the small signal AC model for a converter in either CCM or DCM can be shortly summarized:

1. Average the waveforms over one switching period to remove the switching harmonics
2. Perturb and linearize the averaged model about a quiescent operating point

3. Separate the equations into DC and AC components
4. Transform the AC equations into the Laplace domain
5. Solve for the transfer function

A method for developing the transfer function for a buck converter is found in the reference [27]. This method is also possible to use for a boost converter in a PV system, which is explained in appendix I.

2.3.5 Buck versus boost in a PV system

In grid connected systems with varying input from the source (like PV or wind), the input voltage might be both higher or lower than the AC voltage. This makes both buck and boost operation necessary, depending on the input voltage. Both converter topologies are applicable for MPPT. In real systems, however, the boost converter is the one most utilized. Normally the DC link voltage will be at least 350 V, and if enough modules cannot be connected in series to obtain this voltage level in small systems, a boost stage is necessary.

It has been presented in earlier studies that the efficiency for a boost converter operating in CCM varies slightly for varying duty cycle, while the efficiency variation for a buck converter is considerable. For a closer study, turn to reference [17].

For a boost converter the current through the inductor will equal the input current, while for a buck converter it will equal the output current. This can also be seen in the figures 14 and 18.

2.3.6 DC-AC Switch Mode Inverters

The purpose of DC-AC Switch Mode Inverters is to produce a sinusoidal AC output from a DC input through PWM. The inverter is able to control both the magnitude and the frequency of the AC output. Inverters that have an input assumed to be a DC voltage source is referred to as Voltage Source Inverters (VSIs), and can be divided into three categories: PWM inverters, square wave inverters and single-phase inverters with voltage cancellation. In a PV system PWM inverters are most frequently utilized and their purpose is to keep the DC-link voltage at a constant voltage level by adjusting the DC link current. The PWM in inverter circuits is more complex than for DC-DC Switch Mode Inverters shown in figure 12. To be able to produce a sinusoidal output voltage waveform with the required frequency, the control signal need to be sinusoidal as well. And the signal it is being compared to is a triangular waveform rather than a sawtooth signal. The frequency of the waveform creates the switching frequency and is ordinarily kept constant. For a more thorough explanation about DC-AC Switch Mode Inverters, see reference [33].

2.4 Operational amplifier

The operational amplifier (normally called op amp) is an electronic circuit which is an important part of many circuits today, and it has many ranges of application for transforming a signal. It consists of two inputs, one output and positive and negative power supply, as shown in figure 22.

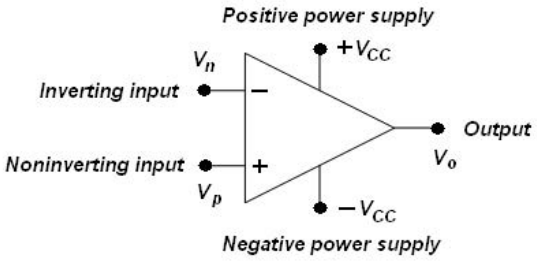


Figure 22: Operational amplifier

At the name implies, this circuit is providing an amplification of the input. The output of the op amp equals the difference between the non-inverting and the inverting input multiplied by a large gain A. This linear operation is valid as long as the output voltage stays within the limits of the positive and negative power supply. The power supplies do not need to be of the same magnitude. When the output exceeds the power supply limits, the device goes into saturation. Hence the op amp has three distinct regions of operation. These can be summed up as:

$$\begin{aligned} A(V_p - V_n) < -V_{CC}: &\quad \Rightarrow V_o = -V_{CC} \\ -V_{CC} \leq A(V_p - V_n) \leq +V_{CC} &\Rightarrow V_o = A(V_p - V_n) \\ A(V_p - V_n) > +V_{CC}: &\quad \Rightarrow V_o = +V_{CC} \end{aligned} \tag{15}$$

In an ideal op amp the equivalent resistance seen by the input is considered to be infinitely large. This implies that no current is flowing in the input port, and hence (V_p - V_n) equals zero. This is seen in the equivalent circuit in figure 23. Seen into the output the op amp appears as a source in series with an output resistance. This resistance is assumed to be negligible. In a real op amp, however, the equivalent input resistance is observed to be of finite magnitude, i.e. 1 $M\Omega$ or more, and the output resistance not completely negligible. The gain A, which in an ideal op amp is assumed constant, has also shown to be varying for different operating conditions.

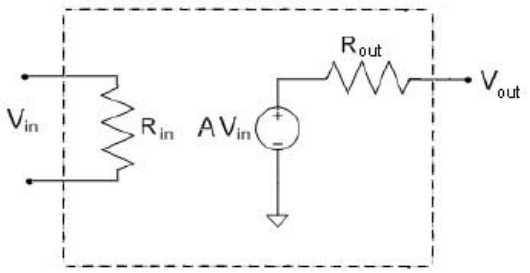


Figure 23: Equivalent circuit of the op amp

Difference amplifier circuit The difference amplifier circuit is a frequently used op amp circuit. The circuit gives an output which is proportional to the difference between the two input voltages (that is between the inverting and the non-inverting input). A circuit diagram is shown in figure 24.

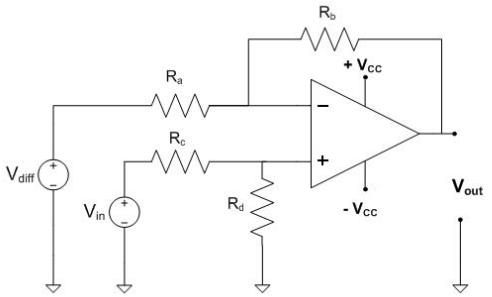


Figure 24: Difference amplifier circuit

Through considering the sum of the currents away from the inverting input node, the output voltage is found to be:

$$V_{out} = \frac{R_d(R_a + R_b}{R_a(R_c + R_d)} V_{in} - \frac{R_b}{R_a} V_{diff} \tag{16}$$

So the output is proven to be the difference between a scaled V_{in} and a scaled V_{diff}. For simplification of this difference, the scaling of each of the voltages can be made equal by setting $\frac{R_a}{R_b} = \frac{R_c}{R_d}$. This replacement yields a more straightforward expression for the output voltage:

$$V_{out} = \frac{R_b}{R_a}(V_{in} - V_{diff}) \tag{17}$$

The ratio $\frac{R_b}{R_a}$ can also be called the gain factor of the circuit.

To obtain a circuit where the output voltage equals the difference of the input voltages without any scaling, all the resistors must be given the same value.

The theoretical background on operational amplifiers is based on the references [5] and [36].

2.5 Filters

Ripple and noise in the signals can generate distortion in the measurements and thus create errors and unstable operation in the system. The noise can be removed by implementing filters, or frequency selective circuits. Depending on type of elements and placement in the circuit the filters can eliminate certain unwanted frequencies. The typical filter types are low-pass, high-pass, bandpass and bandreject. Noise is a typical high frequent distortion type and can be partly or totally removed by implementing a low pass filter between the input and the output of a circuit. Ideal filters will have a frequency limit where the passing of signal goes from maximum to zero, called the cutoff frequency ω_c, but in real circuits this is not possible. At frequencies higher than the cutoff frequency the signals passed through the circuit will decay with a gradient of -20n dB per decade (when examined in a Bode diagram [2] [36]), where n is the order of the filter. So it is hard to remove all kinds of distortion from a signal.

Filters can be divided in two types, the passive and the active filters. The passive filters incorporate utilization of passive circuit elements like resistors, inductors and capacitors, while the active filters also include operational amplifiers (which is characterized as an active circuit element).

More theory on filters and how to design them is found in [5] and [36].

In the system analysed in this master thesis noise in the measurements is a typical issue, and a low-pass filter will be of interest.

RC filter A simple, but often sufficient filter is the RC-filter, shown in figure 25.

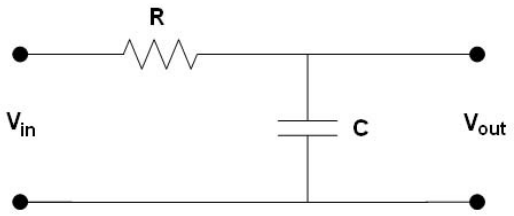


Figure 25: First order low-pass RC filter circuit

The transfer function between the input and the output of the filter (in the Laplace domain) is:

$$H_f(s) = \frac{V_{out}}{V_{in}} = \frac{\frac{1}{RC}}{s + \frac{1}{RC}} = \frac{\omega_c}{s + \omega_c} \tag{18}$$

Thus the values of the resistor and the capacitor decides the cutoff frequency.

Butterworth Filter - design method The Butterworth filter is a design method which leads to maximal flatness in the passband. The filter might be both active and passive and of many different orders depending on the requirement. A normalized [3] first order Butterworth filter has the transfer function:

$$H_{B1}(s) = \frac{V_{out}}{V_{in}} = \frac{1}{s + 1} \tag{19}$$

This filter equals the first order RC-filter with $RC = 1$.

The general unity gain equation of the Butterworth filter is given as:

$$\mid H_f(\omega) \mid = \frac{1}{\sqrt{1 + (\frac{\omega}{\omega_c})^{2n}}} \tag{20}$$

By increasing the order of the filter, the decay of the slope at frequencies higher than the cutoff frequency will be steeper. To obtain a circuit giving a higher order, first and second order filters are cascaded to get the desired order. A circuit that gives the second order transfer function of the Butterworth filter cascade is shown in figure 26.

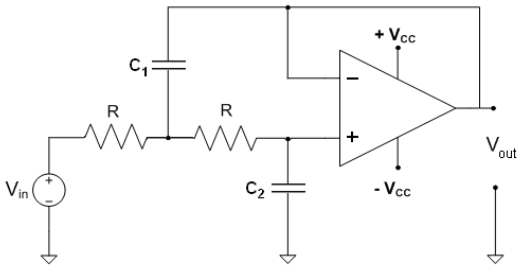


Figure 26: Second-order circuit in Butterworth cascade

The transfer function for this filter is given as:

$$H_{B2}(s) = \frac{1}{s^2 + b_1 s + 1} \tag{21}$$

[3] when the cutoff frequency $\omega_c = 1\frac{rad}{s}$ and gain equal to 1 in the passband

This is obtained by choosing the resistor values to be $R = 1\Omega$ and the capacitor values:

$$b_1 = \frac{2}{C_1} \tag{22}$$

$$1 = \frac{1}{C_1 C_2} \tag{23}$$

Only the Butterworth filter circuit of first order is utilized in this thesis, but the procedure of increasing the order might be useful for later development. A closer description is given in reference [36].

3 DC-DC Converter Control in PV Converter Systems

All electrical systems containing a converter stage with controllable switches often requires some sort of control. This control ensures that the required power available is transferred to the output according to preset limitations. For PV converters the maximum power available is decided by the PV cell characteristic (see figure 4), but this value often mismatches the Maximum Power Point (MPP) of the load. By implementing Maximum Power Point Tracking (MPPT) in a PV system, the MPP of the PV cell can be maintained (i.e. tracked) and hence the number and size of the PV panels can be reduced or the energy yield can be optimized.

This type of control is called direct duty cycle control and is the easiest to implement in such a system. To ensure a more stable output of the MPPT, an inner voltage control loop can be implemented. This is called voltage mode control (where the ramp in the PWM module is generated by an internal clock in the processor and has a fixed frequency). Another way of doing MPPT is by current mode control, which incorporates an additional feedback loop, coming from the switch current. This is a way of keeping the current within given boundaries, and this way the current through the switches can be controlled. This method is not implemented in the master thesis, but is mentioned with ulterior motive for later use.

This chapter will give an overview over the different control schemes already mentioned. There are a lot of information that can be presented about control theory, but it is assumed that the reader is familiar with certain terms, and more detailed descriptions can be found in the references if desired.

3.1 Maximum Power Point Tracking

Due to the moving sun, which leads to change in irradiance angle on the PV panels, and the variation in amount of irradiance hitting the panels, the energy which the PV panels are able to absorb do not stay constant over time. Hence the PV characteristic will also change, i.e. it will move, as shown in figure 5. When this happens, the I-V characteristic changes and the MPP will move. If the system was previously operating at the MPP, there will most probably be a power loss with the same operating point and new conditions.

To overcome this problem, an electronic system called MPPT has been developed (see [39, 28]. This system includes no moving parts and must not be confused with a physical tracking system (where the solar modules are turned to track the sun). The system utilizes a high efficient converter (either DC-DC or DC-AC) to extract the maximum power available from the modules at any time. The superior method of doing this is to measure the instantaneously power output from the PV panels and check if the power output increases or decreases after adjustment of the duty cycle D. The code for the MPPT will be written into the DSP.

There are several MPPT algorithms in use today, incorporating different techniques to maximize the power transfer from the PV panels. The efficiency of each of these techniques are varying, with changing atmospheric conditions being one of the major reasons. Some of the most frequently used algorithms will be presented shortly in the next sections, based on the references [18] and [20].

3.1.1 Perturb and Observe (P&O)

This is the most commonly used method of MPPT, because of its simplicity in both structure and measurement requirements. The algorithm constantly adjusts the electrical operating point by measuring the operating voltage and current of the PV panel to observe the change in power transfer. Studying the power vs. voltage curve of a PV cell in figure 6 can make it clearer how the tracking is done. The perturbation is done by changing the voltage stepwise in a certain direction, and the power change is observed. If the change is positive, it is obvious that the MPPT has moved the operating point of the PV panel closer to the MPP. Thus the voltage is continued perturbed in the same direction. If the change on the other hand is negative, the operating point has become less optimal and the direction of perturbation must be changed. This algorithm can be described by the following statements:

If $\frac{dP}{dV} > 0$: The PV panel has achieved an operating point closer to the MPP
If $\frac{dP}{dV} < 0$: The PV panel has achieved an operation point further away from the MPP

With utilization of this algorithm, there will always be oscillations around the MPP during steady state operation. This can be a problem, leading to a slightly more unstable system. Another drawback of this algorithm is tracking in the wrong direction, caused by rapid change in the irradiance or temperature which will confuse the MPPT. Both of these drawbacks cause power loss.

A flowchart of this algorithm (in discrete form) is shown in figure 27.

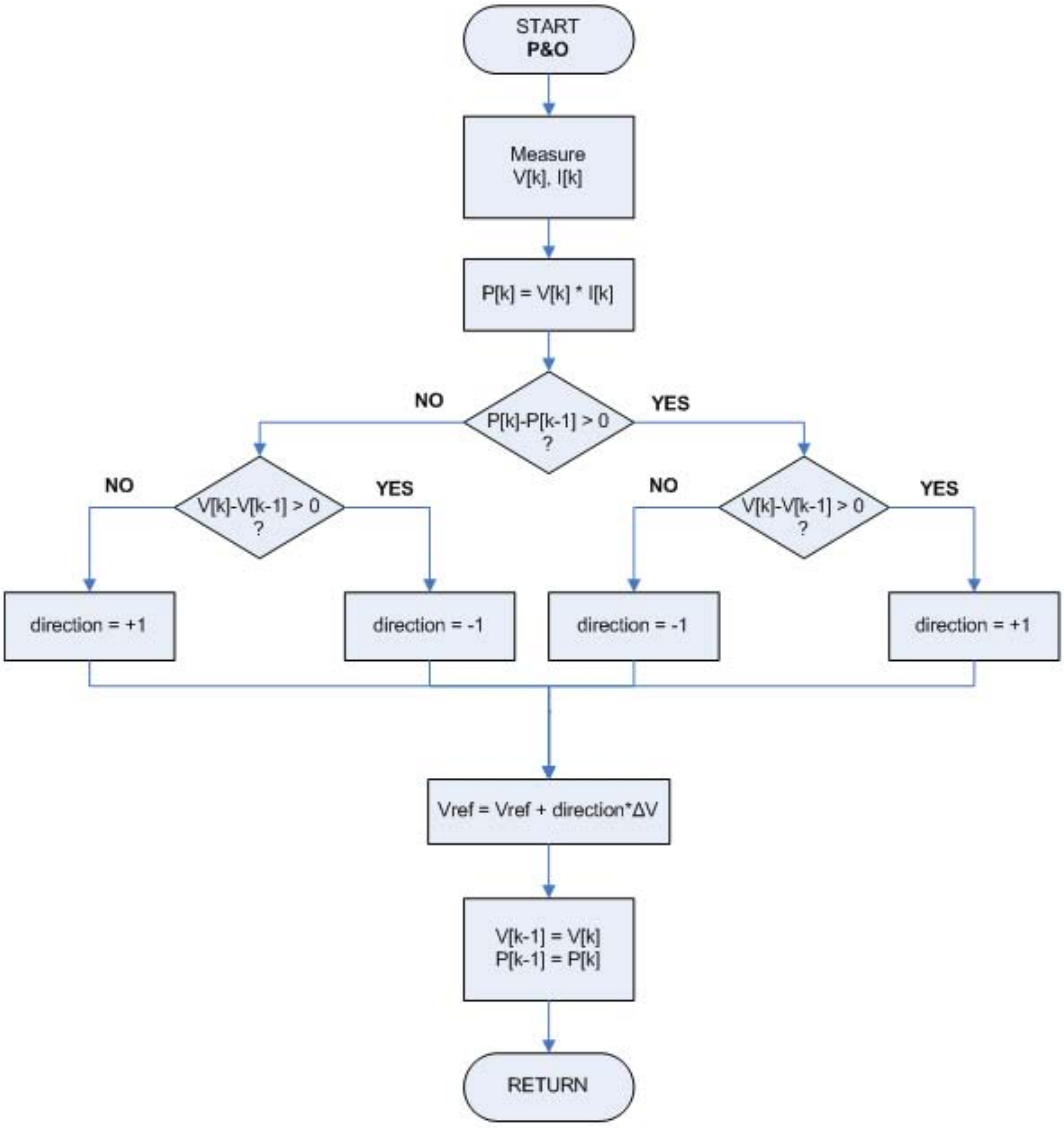


Figure 27: Flowchart of the Perturb and Observe algorithm

3.1.2 Incremental Conductance (INC)

This algorithm is an improvement of the P&O method. As previously mentioned, a drawback of the P&O is the oscillations around the MPP. The Incremental Conductance method takes this into consideration and stops tracking when the MPP (with the prevailing atmospheric conditions) is found. As the name implies, the algorithm uses the incremental conductance as background of operation, which is the current divided by the voltage (inverted resistance). The MPPT wants to find the point where the gradient of the power over current equals zero (as in equation 24), and by using the product rule, the relation in equation 25 is found.

$$\frac{dP}{dV} = 0 \tag{24}$$

$$\frac{dP}{dV} = \frac{d(IV)}{dV} = \frac{dI}{dV}V + I\frac{dV}{dV} = \frac{dI}{dV}V + I \tag{25}$$

$$\frac{dI}{dV} = -\frac{I}{V} \tag{26}$$

The advantage of this algorithm is that it takes into account the changes in irradiance, which the P&O algorithm is less capable of. The drawback is the added complexity which gives an additional computational time and might slow down the sampling frequency.

A flowchart of this algorithm (in discrete form) is shown in figure 28.

NOTE: The voltage and current change will seldom be equal to zero, but by allowing the change to be within a certain range ϵ, the perturbation stage can be bypassed.

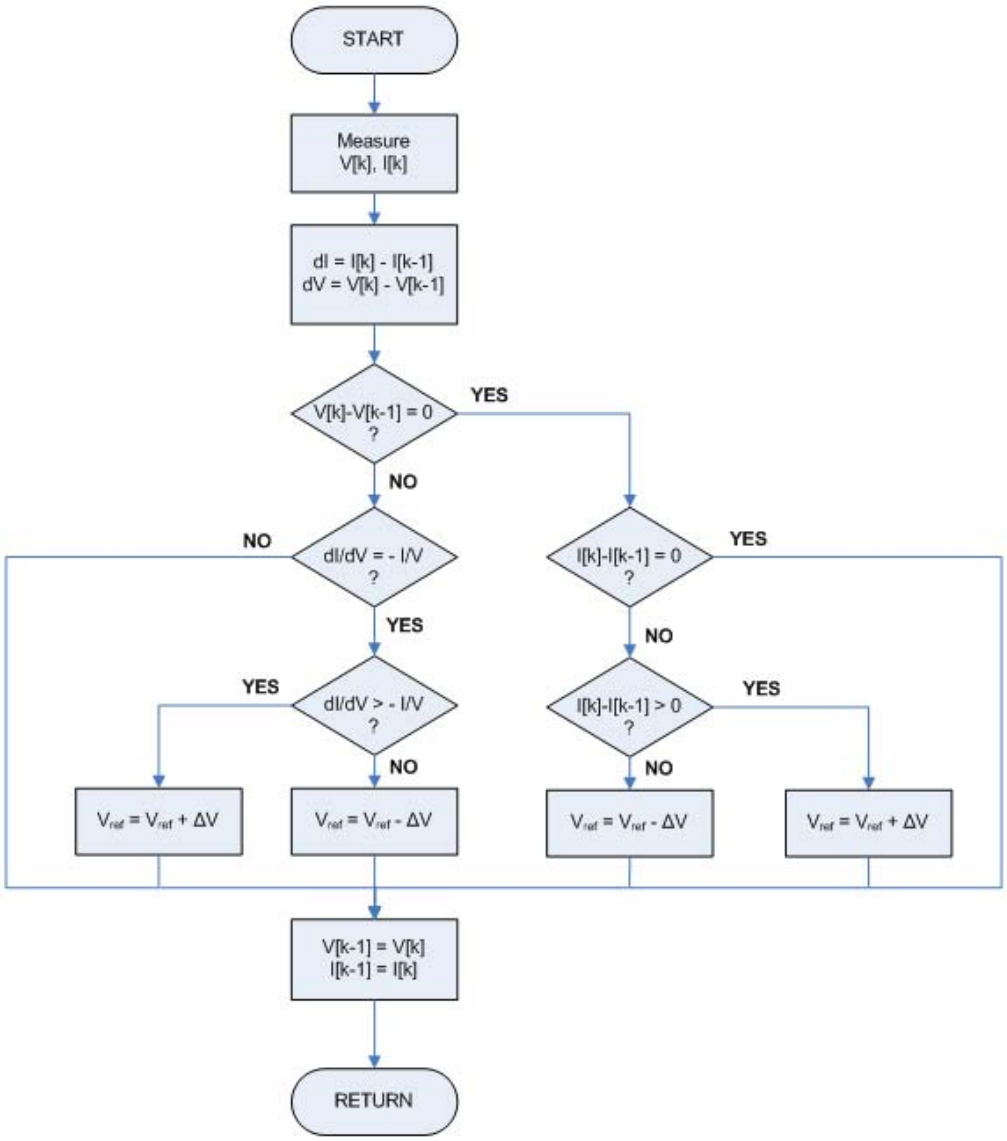


Figure 28: Flowchart of the Incremental Conductance algorithm

3.1.3 Constant Voltage (CV)

The open circuit voltage of the PV panel changes both with varying temperature and irradiance, but the change is rather small concerning different irradiance levels. By disregarding the irradiance dependence, the voltage can be said to be only dependent on the temperature level. The MPP of a PV panel is normally found to be a certain fraction of the open circuit voltage, with the most common value set to 0.76-0.8. By measuring the open circuit voltage value and multiplying with a value within this range, a rather tolerable operating point is found. As a PV panel operation is not ideal, it is quite evident that the MPP is not constantly located at this point, which might give an operating point away from the MPP. Also, the measurement of the open voltage requires frequent disconnection of the PV panel, which leads to a considerable power loss.

This algorithm is simple and requires only one value of measurement, which makes it adequate if the demand of optimal operation is not required. For initialization of the PV system operation the CV algorithm is very suitable, where the open circuit voltage is measured at the start-up to decide the initial starting point of the MPPT.

3.1.4 Optimizing MPPT algorithms

Two important factors of implementing MPPT is the duty cycle step and the execution time period. Ideally these parameters should be as small as possible. A very small duty cycle step decreases the oscillations, while a small execution time increases the speed of the algorithm. However, in a real system it is impossible to operate with these conditions, due to parasitics causing noise, time delays etc. The dynamic response of the system must be considered when choosing the parameters. How sensitive the specific algorithm is for rapid atmospheric changes is also important to take into consideration.

Choice of duty cycle step The smaller the step of the duty cycle, the lower the steady state losses when oscillating around the MPP. However, a too low duty cycle step can make the MPPT less efficient during rapid changes in the atmospheric conditions. During sunny days the atmospheric conditions will not vary too much, but on cloudy days this will be an issue.

In the DSP Controller the duty cycle step is varied by changing the controlled variable (which equals the input voltage in this system). The relation between the change in duty cycle and change in voltage is given as:

$$\triangle d = (1 - \frac{V_{in}}{V_{out}})_1 - (1 - \frac{V_{in}}{V_{out}})_2 = (\frac{V_{in}}{V_{out}})_2 - (\frac{V_{in}}{V_{out}})_1 = \frac{1}{V_{out}} \triangle V_{in} \tag{27}$$

Choice of time step The time step should be sat as low as possible without causing instability in the system, which can be done by considering the dynamic step response of the system. The system must be allowed to reach a new steady state condition before next perturbation (or be within a certain limit of the new steady state condition).

The mathematical background for optimizing the duty cycle and time step of a MPPT algorithm is presented in reference [35].

3.1.5 Efficiency of MPPT algorithms

The efficiencies of the different algorithms already mentioned are varying due to the accuracy of the algorithm, and experimental results presented in [18] are quoted here:

Table 2: Efficiency of different MPPT algorithms

	P&O	*INC*	*CV*
Array	$96,5\%$	$98,2\%$	$88,1\%$
Simulator	$97,2\%$	$98,5\%$	$92,7\%$

As expected, the CV algorithm has the worst efficiency, followed by P&O and then the Incremental Conductance. Seen as the efficiencies between P&O and INC are quite close, it must be considered whether or not the efficiency of the INC algorithm evens out the increased complexity.

3.2 Voltage mode control - Controllers

The task of the MPPT is to change the reference value of the input voltage, and the purpose is to change the magnitude of the input voltage accordingly. But to get the system to follow the reference signal is not a matter of course when no other type of control is implemented. In most processes today it is customary to implement a feedback loop and a controller to ensure an optimal operation of the system while at the same time avoiding stresses that can harm any of the system components. The controller modifies the error signal between the reference value and the input value from the feedback and will normally try to minimize the error. Figure 29 shows the block diagram of the system with feedback from the input. The controller is often referred to as a compensator. Implementing a feedback loop corresponds to closed loop control of the system. The controller output and plant input u equals the duty cycle, and the plant corresponds to the DC-DC converter.

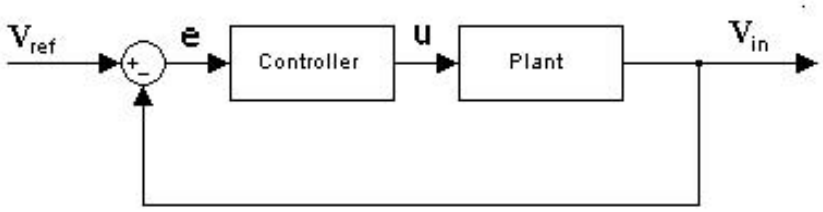


Figure 29: Block diagram of the system with feedback from input

A power system is an analog or continuous time (CT) system and can be controlled both by utilizing analog and digital control. A system that contains both continuous and digital time signals is referred to as a Digital Control System [37].

3.2.1 Analog vs. digital control

When implementing an analog controller, physical building is required and the circuit comprises the use of operational amplifiers together with circuit elements as resistors and capacitors [36]. Through different configurations of these devices, different regulators can be made. This makes analog control rather cheap and has up till now been a common way of implementing closed loop control. Analog control is described by classical control theory as the Laplace transform or differential equations.

Digital control is another way of controlling a system, through utilization of a digital computer. The recent decades digital control has become more common, as this method has a lot of advantages compared to the analog counterpart. The digital world is discrete and rather an imitation of the real world (which is equal to an analog system). To be

able to utilize digital control on analog systems, conversion stages between these two must be present. Digital control is described by difference equations, which is needed because the digital computer's lacking ability to integrate.

Previously the analog control was most commonly used, as it was cheaper and more accurate. But as the knowledge about the digital control and digital signal processing has developed and the cost has been reduced, it has become more common to utilize digital control for industrial applications. Another great advantage is that the same hardware design can be used for several applications without need of modification (as will be necessary with analog control). This will simplify the control development as well as being less time consuming.

There are benefits and drawbacks with both the types of control, which are summarized in figure 30.

	Analog	Digital
+	High bandwith High resolution in both time and magnitude Easy to understand	Insensitive to environment Flexible in use Capable of more advanced control
-	Sensitive to environment (temperature, EMI) Sensitive to aging Not flexible (hardware) Complex systems means larger parts	Bandwith limitation (due to sampling) Resolution limitation Numerical problems (rounding) CPU performance limitation Interface requirement

Figure 30: Analog vs. digital control

The information about analog and digital control is mainly based on the references [31, 26, 15, 37, 2, 16].

3.2.2 Analog control - Continuous time systems

It is assumed that the knowledge about differential equations and the Laplace transform is familiar to the reader, and these areas will not be further explained[4]. However, the most common controller types will be shortly presented.

The simplest and most common controllers are P (Proportional), PI (Proportional + Integral) and PID (Proportional + Integral + Derivate) controllers[5]. The P-part, the I-part and the D-part have different advantages that can influence the system operation.

The P-controller is a simple gain or amplification that scales the error signal. This controller controls the speed regulation of the step response of the controlled signal. A

[4]To refresh this knowledge, turn to the references [2], [36] and [15]

[5]The PID-controller will not be further explained

small gain might give a stable step response with a long settling time, while a large gain might give an overshoot which makes the step response oscillate to the new value. A too large gain can make the system unstable. The P-controller transfer function in the CT system is given as:

$$h_c(t) = K_p e(t) \tag{28}$$

and can be replaced by the controller block in figure 29. In the Laplace domain the P-controller is denoted as:

$$h_c(s) = K_p e(s) \tag{29}$$

A drawback of the P-controller is that it does not consider the values from the previous cycle, and in most cases it is unable to cancel out the error.

The PI controller takes the error into account by adding an integrator. The purpose of the integrator is to give infinite gain when the frequency is zero (that means passing trough as much of the DC-term of the signal as possible), so the error between the reference and the feedback signal is minimized.

The transfer functions for the PI-controller in the CT system and the Laplace domain respectively are:

$$h_c = K_p(e(t) + \frac{1}{T_i}\int_0^t e(\sigma)d\sigma) \tag{30}$$

$$h_c = K_p\frac{1 + T_i s}{T_i s} \tag{31}$$

where T_i is the integration time or reset time. The integral action in a system where the output can go into saturation can lead to a slow system with undesirable effects. If the integral part gets so large that the system goes into saturation the feedback will no longer have any effect. This leads to a continuous increase in error that will slow down the system when the error is finally reduced (the error is so large that it takes time before the integrator is able to reduce it). This happening is called *integrator windup* and should be avoided. One way of doing this is to stop the integrator action when the system goes into saturation.

See references [2] and [4] for a more accurate description of the controllers.

3.2.3 Tuning of analog controllers

When implementing a controller in a dynamic system the controller must be adjusted by choosing the right values of the parameters, i.e. the gain and the time constants. There are several ways of doing this. When the sampling interval is very short, the behavior of the digital controller is very close to that of the analog controller. This means that tuning rules of analog controllers can be applied. The Ziegler-Nichols rules ([2], [45]) is a common way of tuning to find the right parameters. It must be noted that the use of Ziegler-Nichols assumes a stable open loop operation.

The ultimate-sensitivity method is one of the Ziegler-Nichols rules and is a common way of tuning experimentally. The controller is implemented in the system with T_i set to infinity (and T_d of the derivative part set to zero). The gain is then increased until the system reaches the limit of stability, which occurs when a step response leads to a stationary oscillation. Now the parameters of the controller can be deduced through finding the "the critical gain K_{pk}", and the period of the oscillation T_{pk}. The parameters are calculated depending on the controller type, and can be found in the table.

Table 3: Ziegler-Nichols method

Controller	K	T_i
P	$0.5K_{pk}$	∞
PI	$0.45K_{pk}$	$0.85T_{pk}$

The Ziegler-Nichols method can be seen as a tool to test the feedback loop.

3.2.4 Digital control - Discrete time systems

In the analog system the feedback signal will always be a continuous signal. A digital system, however, operates in the discrete plane and is not able to deal with continuous values. The system has to read the measured values through **sampling**, which means that a sample of the continuous signal is collected at a fixed interval T_s and a series of values is sent to the digital software as binary numbers. This is called discretization of analog values, and is executed through Analog-to-Digital Conversion (ADC). The sampler can be seen as a switch that is closed in a very short time interval.

As mentioned, the controller in a digital system is approximated by difference equations, which produce a discrete output signal every sample instant. Before sending this signal to the analog system, a conversion to the CT system is required. This is done through Digital-to-Analog Conversion (DAC) and a hold function. The DAC converts a binary number to an analog signal, but the output signal to the plant must be continuous. To accomplish this a hold element referred to as zero-order hold (ZOH) is implemented to hold the voltage value constant during the sample period. This gives a stepwise output which will be similar to a continuous signal at high sampling frequencies. It is important

to be aware of the impact the hold function has on the system. A time delay of half the sampling period is introduced, which can introduce less damping and higher possibility of instability.

In a system containing a converter stage, and hence generation of a PWM signal, there is no actual digital-to-analog conversion appearing between the input and the output of the PWM. The digital input from the DSP sent to the PWM module is converted to a pulse signal that defines the duration of the on and off state of the converter switches. This signal again affects the analog behavior of the system. Actually there will be an indirectly DA Conversion comprising the PWM module together with the converter stage.

The sample frequency is an important factor in digital systems. If the sampling frequency is too low compared to the bandwidth of the sampled values (which equals the switching frequency) a phenomenon called *aliasing* might occur. This means that high frequencies are folded down into lower frequencies and information about the continuous signal is lost. To avoid this the input values must have a theoretical frequency lower than half of the sampling frequency. Shannon's sampling theorem states this as:

$$\omega_c \leq \frac{\omega_s}{2} \tag{32}$$

In practice however, the ratio often shows out to be required a lot higher, at around 10. This can be solved either by increasing the sampling frequency or implementing a filter between the analog side and the ADC input. The filter hence should be designed according to the sampling theorem. However, the switching frequency is normally quite high, which gives a requirement of a very large sampling frequency. This can be a problem for the DSP, as the sampling will require too many cycles of the processor and too few cycles for calculation. Another drawback of implementing a filter is that the circuit introduces a phase delay in the measurements, which can be a problem for stability of the control system.

A way of avoiding both aliasing, calculation time problems and phase delay is by *synchronizing* the switching and the sampling frequency. This technique provides for rejection of the input ripple, and the ADC will read a value approximate to the average value (from references [8] and [37]).

Developing a discrete controller A discrete controller can be developed through various methods, with utilization of either transform or state-space techniques. The transform techniques are also known as the classical techniques, and employ Fourier, Laplace or Z-transforms to develop the required controller. The state-space techniques are known as the modern techniques and employ the state-space formulation to develop the controller. As the last mentioned tool will not be used in this master thesis, there will not be any further explanations on this matter.

When the sampling period is very small digital signals are close to continuous, and the controller design methods for CT systems can be used. The controller is designed in the CT system (with Laplace transformation) and then transform techniques are used to obtain the corresponding discrete equation. This is also referred to as design by emulation. Within this type of methods there are three common methods:

1. Backward Euler
2. Forward Euler
3. Trapezoidal (Tustin's method)

The two first methods are of first order, which means that they are using only one sampled value in the conversion. Each of the methods uses this sample and does an averaging either forward or backward in time (hence the names). The third method is also called bilinear transformation, which alludes to utilization of two sampled values in the calculations. The trapezoidal rule is used to find the control value. The three methods gives quite similar results, but Tustin's method is slightly more accurate.

The drawback of this way of designing the control is that the digital control will always be equal to or worse than the continuous controller, never better. But for a rather simple system these techniques will still be more than sufficient.

The result of the transformation is a replacement of the Laplace operator s with the discrete z-operator. Table 4 shows the equivalent to the s-operator in the discrete domain for each of the transform techniques:

Table 4: Numerical integration methods

Method	*Equivalent*
Backward Euler	$\frac{z-1}{zT_s}$
Forward Euler	$\frac{z-1}{T_s}$
Trapezoidal	$\frac{2}{T_s}\frac{z-1}{z+1}$

The z-operator will correspond to a time delay where

$$zx[k] \Rightarrow x[k+1]$$
and
$$z^{-1}x[k] \Rightarrow x[k-1]$$

3.2.5 Discrete PI-controller

Apart from the PID-controller, one of the most common controller types in the digital controlled systems today is the PI-controller. To implement this controller in the DSP, the continuous controller is discretized through the trapezoidal transformation. Equation 31

of the PI-controller in the Laplace domain is also the basis of the digital PI-controller when using design by emulation.

By utilizing the trapezoidal integration method, replacing the s-operator by the z-operator and doing some rearrangements, the transfer function of the discrete PI-controller becomes:

$$h_c(z) = \frac{u(z)}{e(z)} = \frac{(K_p T_s + 2K_p T_i) + (K_p T_s - 2K_p T_i)z^{-1}}{2T_i(1 - z^{-1})} \tag{33}$$

A rearrangement of this function and replacement of the z-operator by the time delay gives the difference equation:

$$u[k] = u[k-1] + g_0 e[k] + g_1 e[k-1] \tag{34}$$

where g_0 and g_1 will be decided from which transform technique is used. With the trapezoidal ("Tustins") method the parameters are defined as:

$$g_0 = K_p(\frac{T_s}{2T_i} + 1) \tag{35}$$

$$g_1 = K_p(\frac{T_s}{2T_i} - 1) \tag{36}$$

3.2.6 Other types of controllers

In control theory the P-, PI- and PID-controllers are the standard controllers presented. But there are also other types that can be utilized in such systems, like the Type I, Type II and Type III controllers [26]. These controllers are a bit more complex, but also more accurate as they take the poles and zeros of the plant into consideration.

4 System description

A simplified overview of the full grid connected system being studied is shown in figure 31. The yellow blocks indicate the power electronic part of the system, where the power transfer is happening. The grey block indicate the control part, which is responsible for the superior control and hence indirectly affecting the power transfer.

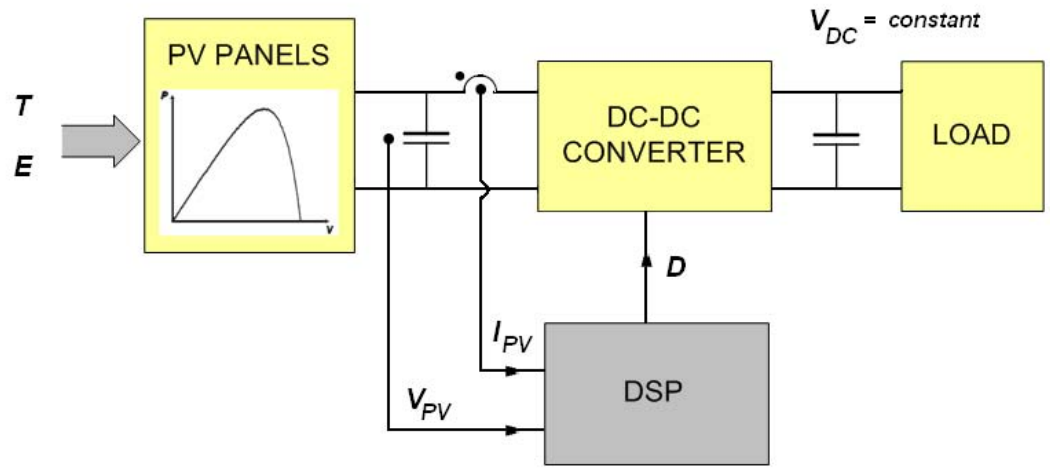


Figure 31: Simplified block diagram of the PV system

The PV panels generate the power in the system, and the power production ability is decided by the irradiance E and the temperature T. The DC-DC converter is responsible for maximum power transfer to the load through MPPT. This is obtained through feedback from the PV panel terminals to the DSP Controller, which again alters the duty cycle of the DC-DC converter. The load represents the connection to the grid through an inverter stage and transformer. The DC link voltage is assumed to be kept constant by the inverter stage.

In the previous master project the system was analyzed with open loop control, regulating the output of the converter. In this master thesis the main focus is on closed loop control, with a PV characteristics input to implement MPPT.

In the following sections each of the system parts utilized in the master thesis will be presented.

4.1 PV panels

The power supply will be PV panels connected in a combination to obtain the desired voltage and current levels. The system has maximum ratings of 60 V and 20 A, and the desired voltage level is about 48 V. When implementing a PV panel, the values stated for each panel is the open circuit voltage V_{OC}, the short circuit current I_{SC} and the maximum power point (V_{MPP} and I_{MPP}). A PV panel can be purchased at the Norwegian company REC Solar, the Japanese company SHARP or other solar companies. A PV panel suitable for this system should have a voltage rating of V_{OC} less than 60 V (as this is the maximum limit), according to the maximum voltage.

An example of a PV panel can be the **NT-175 (E1)** delivered by SHARP [43], which has the following specifications:

Table 5: PV Panel NT-175 specifications

Definition	*Variable*	*Rated value*
Open circuit voltage	V_{OC}	44,4 V
Short circuit current	I_{SC}	5,40 A
Voltage at maximum power	V_{PM}	35,4 V
Current at maximum power	I_{PM}	4,95 A

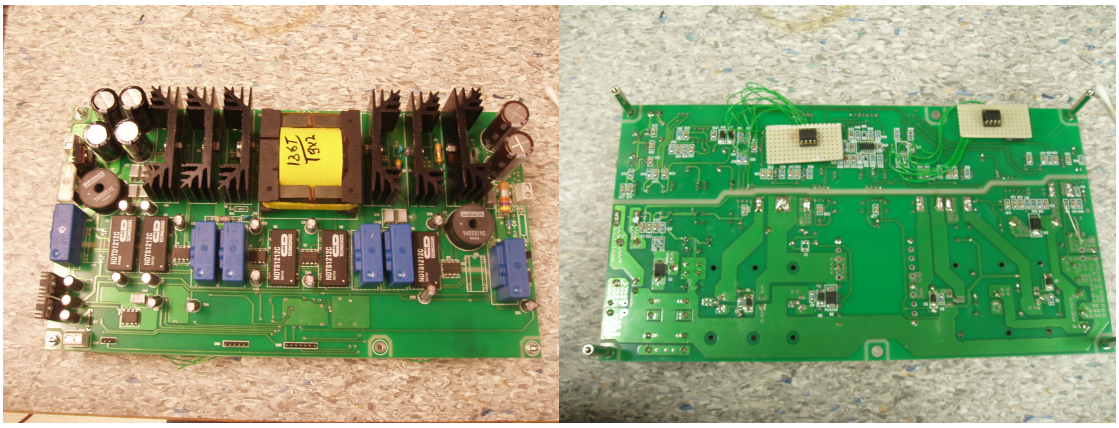
Any number between 1 and 4 of these modules can be connected in parallel as source for the converter, to obtain a short circuit current equal to or below the maximum current limit of the converter.

4.2 The DC-DC converter circuit design

The DC-DC converter designed for the PV system laboratory setup was built in the master project previous to the master thesis. The presentation of the circuit was done in the master project report, but the most important parts of the presentation is included also in this report to get a complete and independent system presentation. Some parts are also extended or altered.

4.2.1 The DC-DC converter hardware

The finished PCB (printed circuit board) of the converter is shown in figure 32. The full circuit schematic (included power supply and driver circuits) is presented in detail in appendix A. The design includes driver circuits and DSP connection circuits which are connected to the power electronic part through galvanic isolation. This is clearly seen on the schematic over the PCB (appendix B), where the galvanic isolation is visible as a thick blue line.



(a) Top side (b) Bottom side

Figure 32: The circuit board of the converter

An overall representation of the DC-DC converter placement in the system is shown in figure 33. The input and output currents and voltages together with the transistor currents are given as possible inputs to the DSP controller, which generates PWM signals based on these values. The transistor currents and the output voltage is also fed directly to the gate driver circuits to prevent the generated PWM signals to reach the circuit in case of overload. This will be explained in more detail later in this chapter.

The next sections will give a short explanation of each of the segments in the complete circuit diagram.

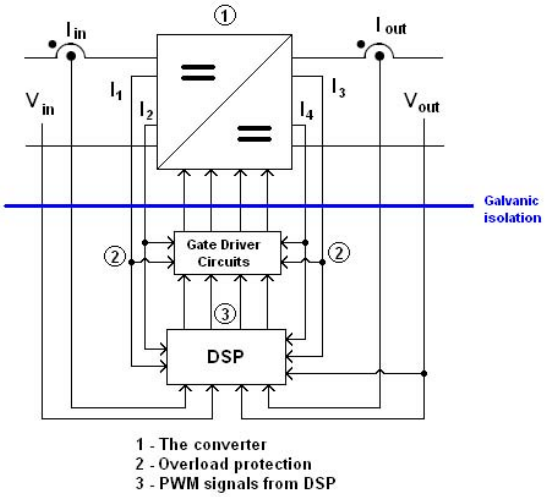


Figure 33: Block diagram of the DC-DC converter structure

4.2.2 Circuit overview

The DC-DC converter is shown in figure 34. The converter is designed as full bridge, where the design permits for the unit to be operated as a buck converter, a boost converter or a buck-boost converter[6]. The converter consists of four independent MOSFET-transistors (Q1-Q4) which are controlled through separate gate signals. The inductor L_1 and the capacitors C_7 and C_8 represents the inductor and the capacitor common for all three converter topologies.

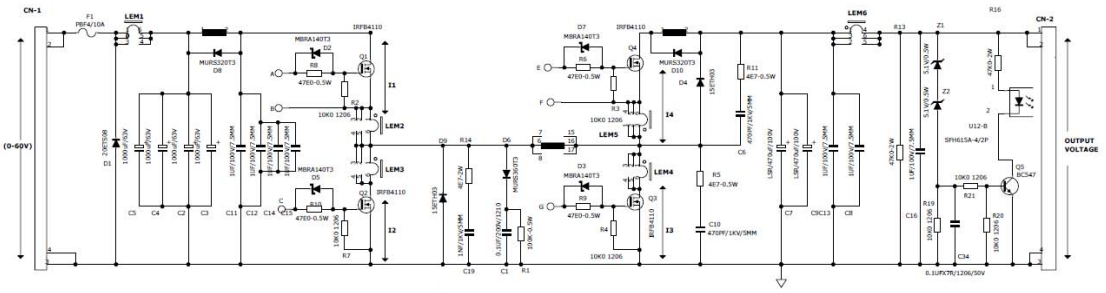


Figure 34: Circuit scheme of the DC-DC converter

At the input of the converter a fuse is implemented to prevent damage on the circuit in case of a short circuit. Secondly a CLC-filter is included to reduce the output voltage ripple without having to increase the converter size and minimize the generation of the

[6]The operation as a buck-boost converter gives a negative voltage output and will not be considered any further

electromagnetic interference (EMI) [33, 1]. During overload conditions the inductor in the CLC-filter will, together with D_8, limit the change in current $\frac{di_1}{dt}$ through Q1. This also applies for the current through Q4, which is limited by L_3 and D_{10}.

The diodes D_9 and D_4 are connected in antiparallel to the transistors Q_2 and Q_4, each with an unpolarized series R-C snubber connected in parallel [33]. These snubbers limit the maximum voltage and change in voltage $\frac{dv}{dt}$. The diodes give the possibility to operate the converter both as a synchronous and non-synchronous converter (see 2.3.3).

At the output of the converter circuit filter capacitors (both electrolyte and foil types) will work to reduce the output voltage ripple.

Just before the output CN2 the voltage protection is found. When the voltage exceeds the breakdown voltage of the zener diodes, the remaining overvoltage potential will turn off all the switches through an optocoupler in a voltage protection circuit.

4.2.3 The converter operation

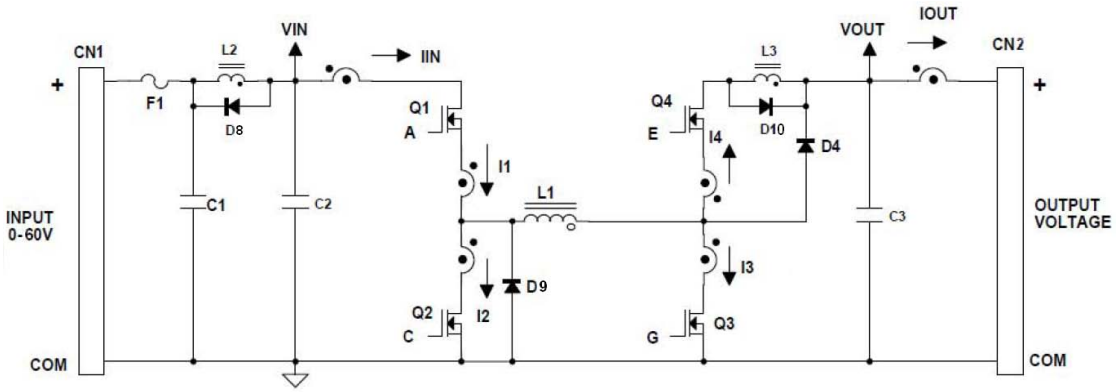


Figure 35: The DC-DC converter circuit

The DC input from the PV modules is fed to the input CN1 in figure 35, and the connection to the DC-link and the inverter stage will be at the output CN2. The switches used are MOSFET transistors and can be seen as the Q1, Q2, Q3 and Q4. Each of them have separate control, through the separate gate signals A, C, E and G. By configuring the MOSFETs separately the power circuit can be configured as any of the wanted converter topologies.

NOTE: The pin sequence at CN3 might be confusing. The PWM3 signal is connected to switch Q4, while the PWM4 signal is connected to Q3!

NB! The explanation of the circuit is double some places, need to clean up!

Operation as buck converter To operate as a buck converter, the switching scheme will be as shown in table 6 below[7]. This configuration includes

Table 6: Switch control for buck operation

Switch	*Input signal*
Q1	PWM
Q2	$\overline{PWM}$
Q3	OFF
Q4	ON

Operation as boost converter For a boost configuration the PWM signals apply to the transistors on the right side of the H-bridge, Q3 and Q4.

Table 7: Switch control for boost operation

Switch	*Input signal*
Q1	ON
Q2	OFF
Q3	PWM
Q4	$\overline{PWM}$

The inductor L_1 and the capacitor C_3 is common for both configurations.

4.2.4 Measurements in the circuit

Voltage measurements The input and output voltages are scaled down in voltage dividers [36] and sensed through isolation amplifiers (ISO-124) before being sent to the output at CN6. The voltage division is done to make sure that the voltage on the input of the amplifier are not too large before connecting to the DSP Controller. From the datasheet it is found that the ISO-124 can withstand a voltage of up to 100 V, but the power supply range can vary from $\pm$ 4 to $\pm$ 18 V. In this circuit the positive power supply is 12 V and the negative approximately -10 V, which slightly limits the voltage input in case of faulty components. The isolation amplifiers have unity amplification and are implemented mainly for galvanic isolation.

Current measurements Isolated and independent current measurements are accomplished through six separate current transducers (LEM sensors). The sensor devices collect the currents flowing through each of the MOSFET switches together with the

[7]Remember that a transistor in ON state corresponds to short circuit and a transistor in OFF state corresponds to an open circuit

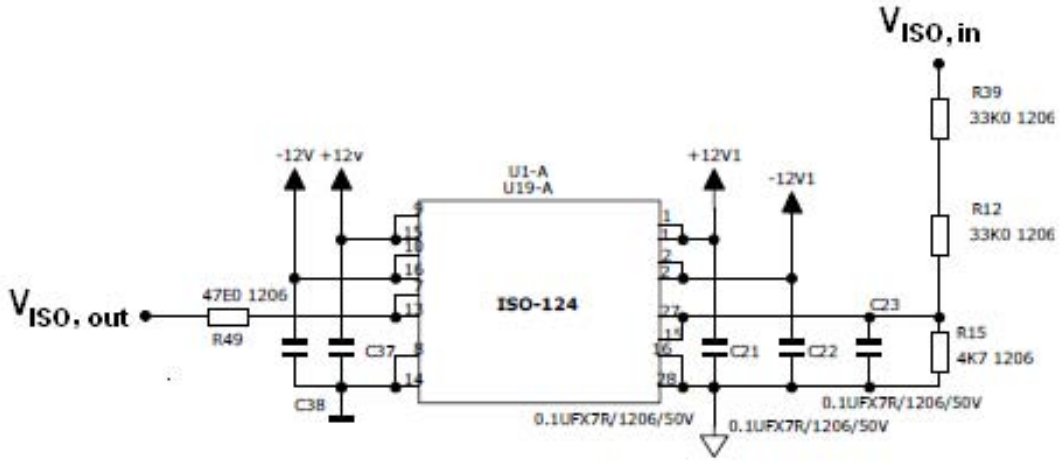


Figure 36: Circuit scheme of the voltage measurement circuit

input and output currents. The sensors transform the currents to voltages which are sent to the output at CN5.

The working principle of the current transducers are based on the so-called Hall effect, named after the discoverer, American physicist Edwin Herbert Hall. The Hall effect is apparent when a conductor with mobile electrical charge carriers (a current) are exposed to a magnetic field perpendicular to the direction of carriers. This exposure causes the Lorentz force to act on the current. The force creates a displacement of the carriers and hence a voltage potential difference called the Hall voltage, which is proportional to the conductor current.

The Hall effect principle for open loop operation is shown in figure 37 [7].

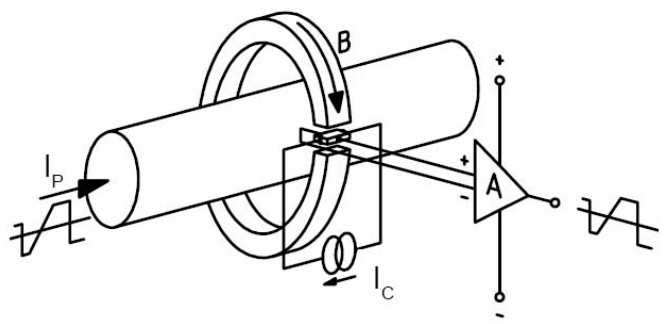


Figure 37: Hall effect: Principle of operation of current transducers

4.2.5 Protection

In case of too high voltages and currents protection has been added to the circuit.

Current protection A fuse F1 is included at the input to protect the circuit from too high values of input current (which equals the output current). During overload conditions the inductor L_2 will, together with D_8, limit the change in current $\frac{di_1}{dt}$ through Q1. This also applies for the current through Q4, which is limited by L_3 and D_{10}. In addition the measured switch currents are sent directly to the logical drivers for safety reasons as an overcurrent protection. In case of overload the drivers are turned off (see figure 38.

Voltage protection The voltage protection circuit block is not included in figure 35, but can be seen on the full circuit scheme in figure 34. Two zener diodes in series are connected in parallel with the output. When the output voltage exceeds the total nominal reverse zener diode voltage the zener diodes will start conducting. Parts of this current will be sent to the gate of the transistor Q5, making it turn to ON position. This action will send a current through an optocoupler (component U12-B) and hence trigger the drivers to act. When overvoltage condition occurs, a signal is sent directly to the drivers, turning all the switches to OFF position.

The simplified overview over the overload protection circuits is shown in figure 38). When the voltages from either of the protection circuits exceeds the reference value, the output signal from the comparator goes high. When the gate driver circuits receive this signal they turn off the PWM signal outputs (a low signal from the comparators hence implies no overload conditions).

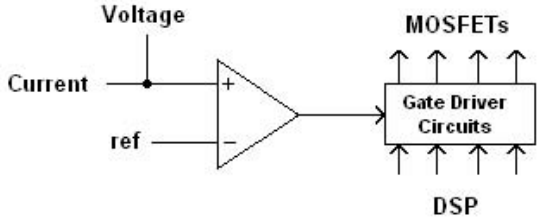


Figure 38: Overload protection

4.2.6 Control circuits

The control circuit includes all the circuitry excluded the power circuit.

Power supply The control circuits are powered by an external DC power supply connected to CN3, with a range of 15-30 V. Each of the MOSFET transistors have separate power supply through DC-DC converters supplied from the external power source.

Processor The measured currents and voltages are sent to an external DSP Controller at the outputs CN5 and CN6. In the DSP Controller the data are processed and used to generate PWM signals transferred to the logical drivers through the input CN4.

Gate drivers The gate drivers control the output to the transistor switches. When the signals from the overload protection comparators are low, the PWM signals from the DSP are passed to the switches, while high signals makes the gate drivers block the transfer.

4.2.7 Alterations of the circuit

While building and testing the PCB there were encountered some errors in either the use of components or the mounting. Thus there were made some changes, which is commented in the following table, to prevent doing the same errors when building the next PCB. An overview over the alterations in the circuit are documented in appendix D.

Change of components

- R16
  The resistor R16 is placed in series with the optocoupler in the overvoltage protection circuits. The original value was set to 47 kΩ, which prevented the voltage protection from functioning properly. Thus it was changed to a lower resistance value.
- Q5
  The transistor Q5 is also a part of the overvoltage protection circuits. It was discovered that the arrived component was another than originally ordered, with a pin sequence that made it difficult to mount it on the board with right placement of the pins.
- Z1 and Z2
  Each of them was supposed to have a breakdown value of 56 V, which is considerably high compared to the overall voltage level of the circuit. The ordered component was also too big for the PCB and had to be changed to zener diodes found in the Servicelab. It was decided to replace the 56 V zener diodes with two of 30 V, so the breakdown voltage became a total of 60 V.

- R22-R26 and R35
  These resistors was placed in parallel with the current transducers, which was unnecessary. The LEM transducers are designed to transform the currents to voltage, which makes the resistors redundant. When this was noticed, they were removed from the PCB. These removals also improved the heat generation in the circuit, as the resistors caused losses and also breakdown of the voltage regulator U17.

Other situations causing errors

- D9
  The diode was placed the wrong way at the board and created a short circuit. It is still enough space on the PCB to place the diode in opposite direction with heat-sink attached, but it is important to remember the changed placement for the next PCB.
- Heat sink for U17
  There is not made any room for a heat sink for the voltage regulator U17. At first it was attempted to implement a small scale heat sink, but the component did not withstand the heat more than one test. The replaced component was connected to a larger heat sink with isolation in between to prevent a short circuit in the next regulator U13.

4.3 Hardware interface

As the PCB is complete for operation and working, the next step is to connect it to the DSP Controller. In this case the development of a hardware interface is needed, as the analog and the digital parts of the system have different voltage and current levels. The power electronics part has maximum values of 60 V and 20 A, and nominal values are set to 48 V and 16 A. When the voltages and currents in the circuit are measured, the values are translated into low voltage values through the galvanic isolation. This translation might not be sufficient as the ADC module of the DSP Controller can only withstand a voltage of between 0 and 3 V.

4.3.1 Selection of suitable hardware interface circuits

The connections between the analog and the digital system will be the ADC and the DAC. The ADC comprises the current and voltage measurements, while the DAC includes the transfer of the switch pulse signal to the gate drivers.

The hardware interface circuits will be rather simple in construction, for instance with utilization of simple voltage division or scaling with an amplifier circuit. In this case it is important to find suitable values for the electrical components.

Before this process can be started, a specification of the different voltage and current levels must be made. The currents from the input, the output and through the switches when turned on are measured through current transducers, while the input and output voltages are measured through isolation amplifiers. Hence there must be made two different specifications, one for the currents and one for the voltages.

4.3.2 Current measurements

The LEM current transducer takes in the current and translates it to a corresponding voltage value through galvanic isolation between the primary and secondary circuit. Figure 39 shows the relationship between the measured current and the voltage. I_{pn} is the primary nominal current, which can be both positive and negative. The output voltage V_{out} will be positive no matter the polarity of the current. The equation used to draw the graph is:

$$V_{out} = 2,5V \pm 0,625 \cdot \frac{I}{I_{pn}} \tag{37}$$

where:

I is the measured current [A]

I_{pn} is the primary nominal r.m.s. current [A]

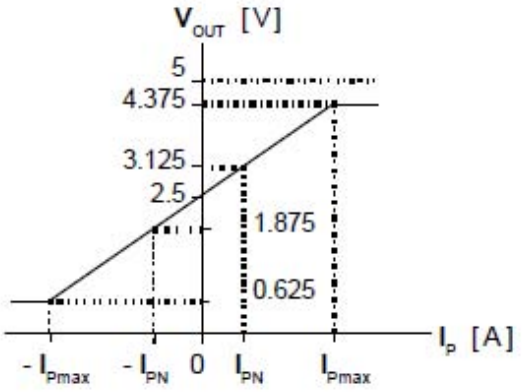


Figure 39: Current transducers: Relationship between input current and voltage

Even though the LEM transducers are capable of measuring currents of both polarities, it has to be considered whether or not this is necessary. A component which requires bipolar current direction could be a battery or internal load, but such a component will most probably be connected to the DC link rather than the terminals of the PV panel. However, the construction of the converter circuit permits for both synchronous and non-synchronous operation, that is both positive and negative currents flowing through the switches. Even though only non-synchronous operation will be utilized in this thesis, the circuit design for both bidirectional and unidirectional flow will be presented.

As mentioned previously, the nominal value of the converter current is set to 16 A. To be sure to utilize the full range of the bit-size in the ADC module, the upper current limit should be decided to be in accordance to the expected operating current. The primary nominal r.m.s. current is set to be $I_{pn} = 50A$.

Unidirectional flow With the above given current values, equation (37) gives a voltage range of:

$$2,5V \leq V_{out} \leq 2,5V + 0,2V = 2,7V \tag{38}$$

Now, as this has been established, the actual scaling circuit must be developed. There are several possibilities to do this. When viewing the minimum output voltage from the current transducer, it is obvious that the DSP Controller should read this as 0 V. The easiest way to accomplish this is to subtract a constant reference value equal to the minimum voltage level (2,5 V) from the output of the transducer. Then the range will be from 0 to 0,2 V. This reference value can be obtained through a voltage divider from a voltage source in the control circuits. Multiplying the maximum value with a constant equal to 15 will get the range required from the DSP. The block diagram in figure 40 shows the transformation of the voltage.

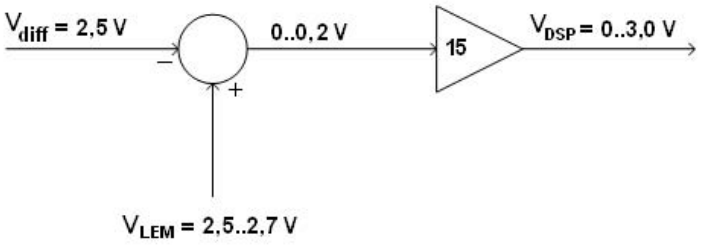


Figure 40: Block diagram of voltage scaling, unidirectional flow

Transforming this diagram into a real life circuit can be accomplished by using a difference amplifier circuit [36]. Here the non-inverting input will be the voltage output from the currents transducers, while the inverting input will be a constant voltage of 2,5 V. The gain will be 15.

Bidirectional flow The deduction can be done similar to that of unidirectional flow. The current range is twice the size, as the negative currents will be measured as well. Then the voltage range will be:

$$2,3V \leq V_{out} \leq 2,7V \tag{39}$$

The constant reference value providing a transformation of -16 A to equal 0 V in the DSP will now be 2,3 V and the gain will be half the gain of the unidirectional case, which is 7,5.

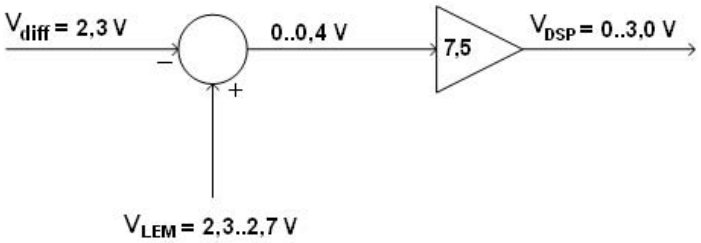


Figure 41: Block diagram of voltage scaling, bidirectional flow

Transforming this diagram into a real life circuit is accomplished the same was as for unidirectional flow (difference amplifier circuit). Here the non-inverting input will be the voltage output from the currents transducers, while the inverting input will be a constant voltage of 2,3 V. The gain will be 7,5.

Common hardware interface It is decided to scale the voltages from the current transducers through a difference amplifier circuit. The voltage range will be the same for all the measurements, hence only one design is required, independent of which current needs to be measured. This simplifies the development and testing of the circuit, as only one circuit is required for this part.

The ratio of the resistor values should be as close to the gain as possible, or a little less. The values of the resistors are decided by the available components in the Servicelab, where they have the EIA resistor series E12 [8] [29]. To make the difference amplifier circuit as simple as possible, the resistors will, if possible, be chosen so that series or parallel coupling of resistors is unnecessary. With this assumption the possible resistor couples are found.

The operational amplifier used for the circuit should have a positive power supply of 3-5 V and negative power supply of zero. Not all op amps are designed for giving a zero output, so this is an important issue concerning the choice of the component.

The difference amplifier circuit used for scaling the voltage from the LEM transducers is shown in figure 42. For this circuit the TLC272 CMOS precision dual operational amplifier used. Designing for bidirectional flow halves the resolution in the DSP when there is only unidirectional flow.

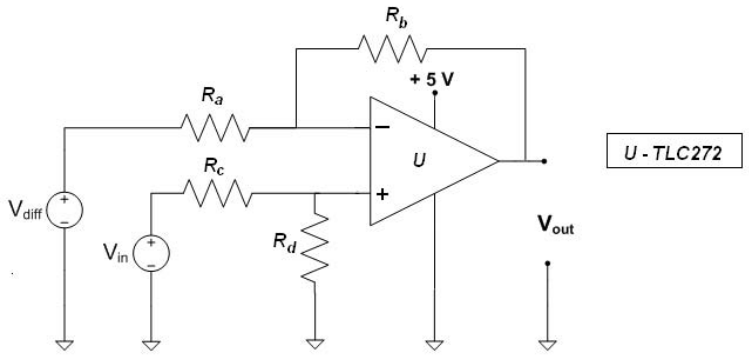


Figure 42: Difference amplifier circuit for bipolar current direction, I_{max} = 16 A

The difference amplifier circuit for unipolar current direction is equal to figure 42, except for the resistor values. As the gain has increased to 15, the resistor values are changed.

The chosen resistor values are summarized in table 8. For the bidirectional flow the gain is slightly smaller than the theoretical value. This will make the resolution a bit smaller, but at the same time work as an extra protection, as the voltage for nominal current flow will not exceed 3 V.

The HI for the **current measurements** needs testing, to make sure that zero current

[8] which means that there are 12 different values per decade

Table 8: Resistor values in the difference amplifier circuits

Current flow	$R_a(= R_c)$	$R_b(= R_d)$	α
Unidirectional	$22k\Omega$	$330k\Omega$	15
Bidirectional	$56k\Omega$	$417k\Omega$	7,446

flow gives out the right value for both unipolar and bipolar current values. For the unipolar situation zero current should give zero voltage to the DSP, while the bipolar circuit should give out approximately 1,5 V. An offset is expected for these measurements also. The voltage input on the inverting side of the operational amplifier needs power supply, which is taken directly from the control circuit of the DC-DC converter PCB. The voltage is taken from the 5 V level and transferred down in a voltage divider between $R_1 = 4,7k\Omega$ and $R_2 = 5,6k\Omega$.

4.3.3 Voltage measurements

The input and output voltages are scaled down in voltage dividers (it is assumed that voltage division is a familiar term) and then measured through separate precision isolation amplifiers. The voltage dividers for the input and the output voltage measurements have different resistor ratios and must be analyzed separately.

PV voltage The voltage divider operates with $R_1 = 4,7k\Omega$ and $R_2 = 66k\Omega$, which gives the relation:

$$V_{ISO,PV} = 0,0665V_{PV} \tag{40}$$

The voltage into the isolation amplifier (i.e. the input to the DSP) is proportional to the input voltage from the converter. Hence the minimum output voltage will be zero (with the earlier assumption that the input voltage will never be negative), while the maximum output voltage is decided by the upper limit of the input voltage. The maximum voltage of the DC-DC converter is set to be 60 V, but the nominal voltage will be 48 V. Hence the voltage range under normal operation will be assumed not to exceed the nominal value. In case of higher voltage levels a safety measure is done through use of limiting zener diodes at the output of the isolation amplifier.

Voltages that surpass the limits of the ADC module will saturate the DSP. As the input voltage always will be positive, the lower limit will never go into saturation (except if a negative offset voltage is present). The upper limit might on the other hand be in the danger zone, and it must be found out which value of the voltage that corresponds to a DSP input voltage of 3 V. With $V_{ISO} = 3$ V, V_{PV} is found to be 45,11 V. Which means that the voltage-divider prevents the DSP of reading voltages up to the nominal value. The upper limit might also be different due to voltage offset.

DC link voltage Here the voltage divider operates with $R_1 = 4.7k\Omega$ and $R_2 = 112k\Omega$, which gives the voltage equation:

$$V_{ISO,DC} = 0,04 \cdot V_{PV} \tag{41}$$

Here the upper limit of the voltage read by the DSP without risk of saturation can be $V_{DC} = \frac{V_{DSPmax}}{0.04} = 75V$. There is no risk of saturation, but the range of the DSP will not be fully utilized, hence reducing the resolution and precision of the measured values. The maximum output voltage can be determined by the overvoltage protection circuit on the output of the converter circuit. Through wise decision of the zener diodes the maximum tolerated voltage can be decided.

4.3.4 Upscaling the voltage of the PWM signal

The PWM signals generated in the DSP has an output voltage of 3,3 V, while the input buffer stages (TPS2814) in the converter need a voltage level of more than 8 V to interpret the signal as an ON signal. An upscale of the voltage is necessary, and this can be done in several ways. One method is to use a driver circuit (IC) that is intended for voltage scaling. Another is utilizing a circuit with two transistors and some resistors. As the driver circuit were not available at the time, the transistor circuit was chosen.

The circuit is shown in figure 43.

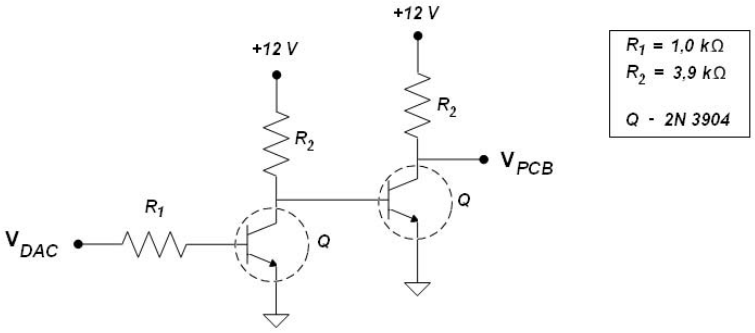


Figure 43: Transistor circuit to upscale PWM voltage

4.3.5 Filtering of the signals

Noise in the measured values requires some filtering before they are sent to the ADC. Nyquist's sampling theorem says that the cutoff frequency of this filter must be at least half of the sampling frequency. With a regular first order RC-filter like described in 2.5 the value must be:

$$\frac{1}{RC} = \omega_c \leq \frac{\omega_s}{2} = \frac{2\pi f_s}{2} \Rightarrow RC \leq \frac{1}{\pi f_s} \tag{42}$$

Calculations are done with f_s =20 kHz, and the values are chosen to be R = $4,7k\Omega$ and C = 3,3 nF. This filter is implemented between the output of the HI circuits and the input of the ADC module.

The voltage divider supplying the difference voltage V_{diff} delivers quite a noisy signal which transmits to the values sent to the DSP, and a capacitor is put in parallel with the output resistor of the voltage divider.

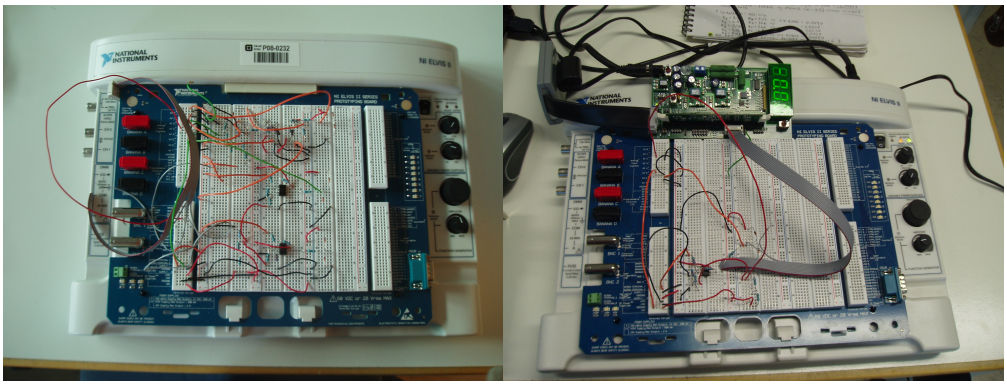
4.3.6 Planning the interface circuits through the use of NI ELVIS II

To construct the hardware interface, some pretesting is required. As the real components will have a behaviour deviating from the ideal world, the circuit must be tested to see whether it is sufficient for the use intended or not. A simple way of accomplishing this is to mount the circuit on a vero-board. But that requires some soldering and might be quite time consuming. To avoid this National Instruments has developed NI ELVIS II, an Instrumentation, Prototyping, and Teaching Platform for Labs [21]. The prototyping board consists of a board where the electrical components can be placed directly without soldering needed, so-called plug and play.

A simple presentation of NI ELVIS II The instrumentation utilized for simple testing is the NI ELVIS II Series Workstation combined with an interchangable prototyping board. The workstation consists of built-in instruments like Variable power supply (VPS) and a function generator. These can be controlled both from a computer based Instrument Launcher software as well as knobs for manual operation. Experiments can be extended with peripheral connectivity through BNC and banana-style connectors. The Prototyping board is an advanced type of veroboard which connects to the instruments offered by the workstation. A link to a user manual for the presented instruments setup is given in [22].

When a suitable circuit scheme is found, a complete circuit scheme for all measurements will be designed and implemented. This can be done either by designing a PCB or by mounting all the circuits on a simple veroboard. The first alternative is more elegant, but might be more complex and time consuming than the latter alternative.

Current measurements The difference amplifier circuit was tested by utilizing the NI ELVIS II Platform with the prototyping board as shown in figure 44. In the beginning the testing was independent of the output of the DC-DC converter. Instead the varying input from the converter was simulated by using the built-in Variable Power Supply (VSP), varying from 2,3 V or 2,5 V to 2,7 V. To produce the reference voltage on the



(a) Platform with test setup (b) Platform connected to DSP Controller

Figure 44: NI ELVIS II

inverting input of the op amp, a voltage divider was needed. This is due to the fact that the platform offers two different DC voltage sources, 15 V and 5 V. The 5 V source was used because it was closest to the required voltage level. The built-in oscilloscope showed the output of the circuit.

Voltage measurements The voltage is already scaled down to a reasonable level trough the voltage divider, and the additional requirement was an overvoltage protection implemented with zener diodes saturating to high levels of the input voltage of the DSP Controller.

4.3.7 HI - experimental results

The finished hardware interface circuits were tested part by part before the actual interconnection between the DC-DC circuit and the DSP Controller was done. This is especially important to make sure no unexpected faults occurs in the circuits. In addition care must be taken so the voltage limits are not exceeded and destroys the DSP card. The testing was done with the setup shown in figure 45, both with and without the DSP Controller connected.

Collecting the measured values must be done by powering the control circuits, or else the values are not transferred past the galvanic isolation of the PCB.

First the voltage measurements were tested. As for now there has not been any new hardware interface design added to the circuit because the existing circuits are satisfactory for the testing. So the most important task is to check that the voltage dividers give out the right values and transfer them to the input of the DSP card. For the current measurements it was most important to see that the output of the differential circuit was according to plan. Through testing with different voltage values on both the input and

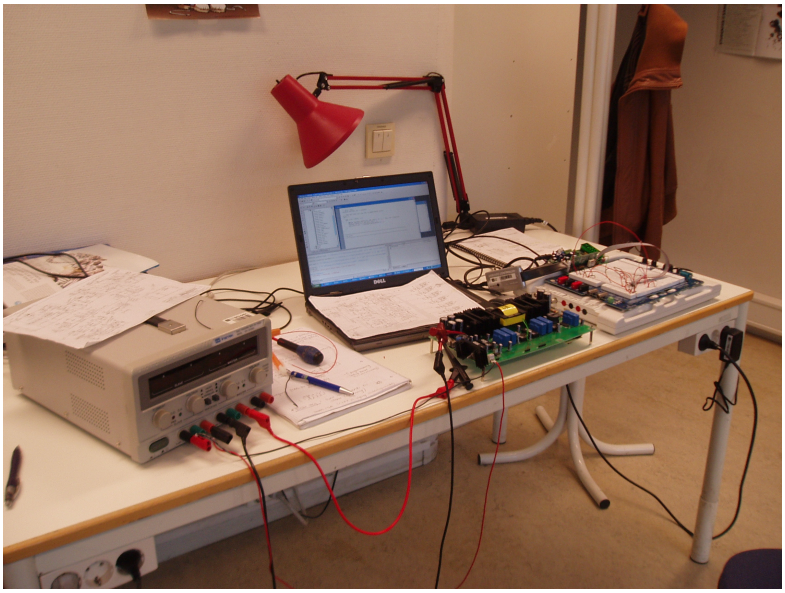


Figure 45: Setup with NI Elvis II

the output of the circuit (separate), the value transfer was proven to be working. The values are not exact and will give an offset value in the DSP Controller, which needs to be taken into consideration when using the values for calculation in the program.

The transistor circuit boosting the voltage of the PWM pulses was tested, and measurements were done both before and after the circuit. At first attempt another transistor type was used in the circuit (BC546), but it introduced a time delay which made the duty cycle a bit higher than the one generated in the DSP. When the transistors were replaced by the faster TLC272, the time delay was not an issue and the voltage level increased from about 3,3 V to around 12 V as intended.

4.4 TMS320F2808 DSP Controller

Texas Instruments has developed several Digital Signal Controllers with quite similar properties which could be chosen for this implementation purpose. The one chosen is the TMS320F2808 [25], one of the most common models in use today. Some of the features available (relevant for this thesis) are:

- High-performance Static CMOS Technology
- High-performance 32-bit CPU
- On-Chip Memory (FLASH, ROM,RAM)
- Three 32-bit CPU Timers
- Ultra-Fast 12-bit 16-Channel ADC
- 6 ePWM modules with 2 independent PWM outputs per module
- System clock frequency of 100 MHz
- I/O Voltage of 3.3 V

The DSP Controller card platform (socket) alternatives are various. The **Digital Power Experimenter Kit** offers a platform with an additional circuit of converters mounted on the board, and on this board the pins for some of the ADC inputs and ePWM outputs are marked explicitly. This board contains some direct connections between the ADC inputs and the ePWM outputs through 0 ohm resistances, which must be removed if utilized. On the platform delivered with the card TMS320F2808, no additional circuitry is found on the card, and pins are only marked with numbers for each GPIO. To find out which GPIO is assigned for the ADC or the ePWM signal transfer, the circuit diagrams of the DSP must be examined. These are also presented in appendix F.

The control card is shown in figure 46.

Figure 46: TMS320F2808 Control Card

A microcontroller could also have been used, but when having a system that requires a fast response DSP is the preferred choice [6].

5 Development of the program code in CCS

The development of the software files in Code Composer Studio was done through utilization of the example files found on the homepage of Texas Instruments in addition to user specific code done in the C programming language. The example files also include additional header files and initialization files. Before presenting the code development, the features of utilizing digital control will be shortly presented.

5.1 General about DSP features and background

5.1.1 The structure in the DSP

At first sight the structure in a DSP can seem quite complex. As mentioned, the DSP handles several types of programming languages, which must be placed in different files (memory locations). All code of same type can theoretically be placed in the same file, but this might not always be a good idea, as the code can be comprehensive and untidy and accidental changes to fixed code might occur. A way of creating a structure that is easy to understand and easy to change is to separate the code pieces by their functionality.

Main Every C program contains one or more functions. The main loop is the main function where all the initialization and definitions are carried out. Other functions in the program are called from here. Interrupt handling are also initiated here. There is seldom any explicit calculations done within the main loop, normally there is only a background loop running infinitely.

Initialization All modules to be used during the DSP operation need initialization. The initialization calls are done in the main loop, addressing functions placed in other files in memory. Initialization code is rarely changed, and putting the code elsewhere is a very tidy way of structure, making sure that the code is not changed by accident.

Interrupts In a digital controller the calculations happens at fixed intervals, referred to as interrupts. While the interrupt handling is initialized and set for operation in the main function, the actual interrupt codes are normally placed elsewhere. The processor must handle the different interrupts by running an Interrupt Service Routine (ISR), and the ISR always has the highest priority.

The main function and interrupts are often placed in the same code file, while initialization is done elsewhere in the memory.

5.1.2 Fixed point vs. floating point representation

DSP Controllers have two different ways of representing numbers, which are fixed and floating point. The DSP Controller used in this master thesis has a fixed point representation, which can be a challenge when doing calculations with decimal numbers. To avoid overflow and unexpected results, some extra care must be taken when defining variables and doing calculations.

Fixed point Fixed point DSPs usually store numbers in a variable of minimum 16 bits, with 4 different ways to represent a number. These are signed integer, unsigned integer, signed fraction and unsigned fraction. In fixed point DSPs the numbers are uniformly spread on 2^{16} or 2^{32} levels. For implementation of counters, loops and numbers sent from the ADC or to the DAC, fixed numbers are necessary.

Floating point Floating point DSPs store numbers by utilizing a minimum of 32 bits. The main feature of Floating Point (and main difference from Fixed Point DSPs) is that the values are not uniformly spread. For large numbers the gap between the numbers are larger than for small numbers. Floating Point DSPs are also able to handle fixed point numbers, but the handling of fixed point operations might be slower than for Fixed Point DSPs.

For a comprehensive and rather well explained introduction to Digital Signal Processing, look up the reference [44].

5.1.3 Representation of numbers

In the world of programming there are several different ways of representing numbers, with the decimal, binary and hexadecimal numeral systems most common. In computer programming the binary number system is found in use everywhere, due to its straightforward implementation in digital electronics.

The decimal numeral system The most common numeral system in everyday life is the decimal system, also denoted base ten [9]. In this system the numbers are represented with 10 different digits, in a range of 0 to 9. When mentioned in relation to other numeral systems, a decimal number is shown with the number 10 as subscript (for example 1010_{10}).

[9] The base number is a notation of how many different digits are used to represent numbers

The binary numeral system In the modern computer science the binary number system is found in use everywhere. The system is represented by two numbers, 0 and 1. Computers are composed of millions of individual switches which can be in ON or OFF position, hence the state is represented by the digit. The digit 0 represents a switch in OFF position, while the digit 1 represents a switch in ON position. A binary number is represented by the number 2 as subscript (like 1010_2, which equals 10_{10}).

The hexadecimal numeral system As previously mentioned, the decimal system is mostly used in the everyday life, while the binary system is mostly found in the world of computer science. When working with computers, it is most often created an interface between these two number systems so that it is not necessary for people to deal directly with the binary numbers. However, sometimes it is necessary with this direct contact. Then a binary number can be quite confusing to work with. So to be able to represent a number with less digits, hexadecimal numbers are often used. This system uses base 16 numbers, where the decimal numbers 0 to 9 and the characters A to F are the building stones. The characters A to F represents the numbers 10 to 15.

Representing negative numbers In computer hardware the binary digits are the building stones of the system. Binary numbers normally represents only positive (unsigned) numbers, but a representations of negative numbers is in most cases necessary. To be able to represent negative (signed) numbers in the binary system, several methods are available:

1. Sign-and-magnitude
2. One's Complement
3. Two's Complement

The sign-and-magnitude method divides the number in two. One bit is reserved for sign representation (most often the MSB) while the rest of the bits in the number represents the number value. The number is positive when the sign bit is 0, and negative for sign bit equal to 1.

One's Complement represents negative numbers through the complement of the positive number. As for the sign-and-magnitude method the MSB is representing the sign of the number, 0 for positive, 1 for negative. To obtain a negative's number representation each bit in the positive magnitude part of the number is inverted (0 to 1 and the other way round).

Both of the previous methods have two representations of the number 0. A way to avoid this is to use **the Two's Complement method**, which is the most common way to represent negative numbers in the binary number system. This method is very similar to the One's Complement method, the only difference is an added 1 to the complementary number. In addition to the advantage of only one representation of zero, this method

is also very advantageous when it comes to arithmetic. Addition and subtraction can be done regardless of the sign. In the programming tools used in this master thesis the Two's Complement method is utilized.

Overflow When a number exceeds the limits of its defined range, an event called overflow occurs. This happens when for instance an unsigned integer of 16 bit (with a range from 0 to $2^{16} = 65\ 536$) goes negative. Instead of interpreting the number as negative, the program starts from the maximum limit and subtracts the negative number. If the value is -7000, the program will "see" (65 536 - 7000) = 58 536. This might cause unexpected actions.

5.1.4 Handling of variables

When programming in C caution must be taken when writing the code and choosing variable types. The variables can be defined as signed or unsigned and the bit size can be set (most often to 16 or 32 bit). Especially when doing direct multiplication in the C language it is important that the compiler is told how to handle the variable, to ensure correct treatment of the values.

Casting Arithmetic operations with different variable definitions of the operands and the target variable is a typical error in C programming, and might cause overflow. If a arithmetic operations with two 16 bit numbers or mixed numbers is going to be stored in a 32 bit variable, casting of the variables might be necessary. This means temporarily redefining one of the variables equal to the target variable, during that specific operation only.

How to select proper type definitions is explained in a manual from TI on Digital Signal Processing: *How to Write Multiplies Correctly in C Code.*

5.1.5 Digital-to-Analog Conversion through PWM generation

In SMPS the output will be a PWM signal to decide the on and off state of the switches. The output hence will not actually be a regular analog value, but a logical signal indirectly deciding the operational voltage and current values of the converter. The DSP has its own module designed specifically for generation of PWM-signals, called ePWM. The module operates like in figure 12, with a control signal (found trough a feedback loop or defined as a constant in the program code) compared with a repetitive waveform. The repetitive waveform is generated by an internal clock in the DSP, and can be set to be a sawtooth or a triangular wave. Each ePWM module has two independent PWM outputs, called A and B, acting on a common repetitive waveform.

5.2 Programming tools

The additional tools used in the control development in this master thesis were the software Code Composer Studio IDE (Integrated Development Environment) v3.3 [24] (delivered from Texas Instruments) and the Blackhawk USB2000 Controller [3], providing the connection between the controller and the software program.

5.2.1 Code Composer Studio

The software development platform Code Composer Studio is especially designed by Texas Instruments to cooperate with the DSP controller chosen. It contains features like a project manager window with compiler, assembler and Linker build options as well as full C/C++ & Assembly Debugging. For running the DSP Controller in CCS, Texas Instruments has several example files for initialization of the different modules of the DSP Controller. The most important ones used in this master thesis are listed in appendix F.3. The files ending with .c is written i C language, while .asm indicates that the file is written in assembly. More details about the contents of the files can be found in the file *C280x/C2801X C/C++ Header Files and Peripheral Examples Quick Start* (found on the homepage of TI).

In addition to these files a main file is needed for running the control operation. In the main loop the setup of the DSP is done, like initialization of the different modules, conversion of sampled values, control code and generation of PWM signals.

As Code Composer Studio handles both C/C++ and the assembly language, it is possible to build a program with each of the programming languages as desired. The example files and general structure of the program is mainly based on C/C++ language, which might seem more logical and easy to understand, and the programming is quite straightforward. Assembly code might be harder to understand, but at the same time it provides clearer insight in how the processor works if understood properly.

Figure 47 shows the user interface of CCS, with some of the main windows that are available. These are:

1. Project manager (overview over included files in a specific project)
2. Editor window with C/C++ or assembly code
3. Status window (for debugging)
4. Watch window (for observing variables)

Other windows available are graphical presentation and memory window.

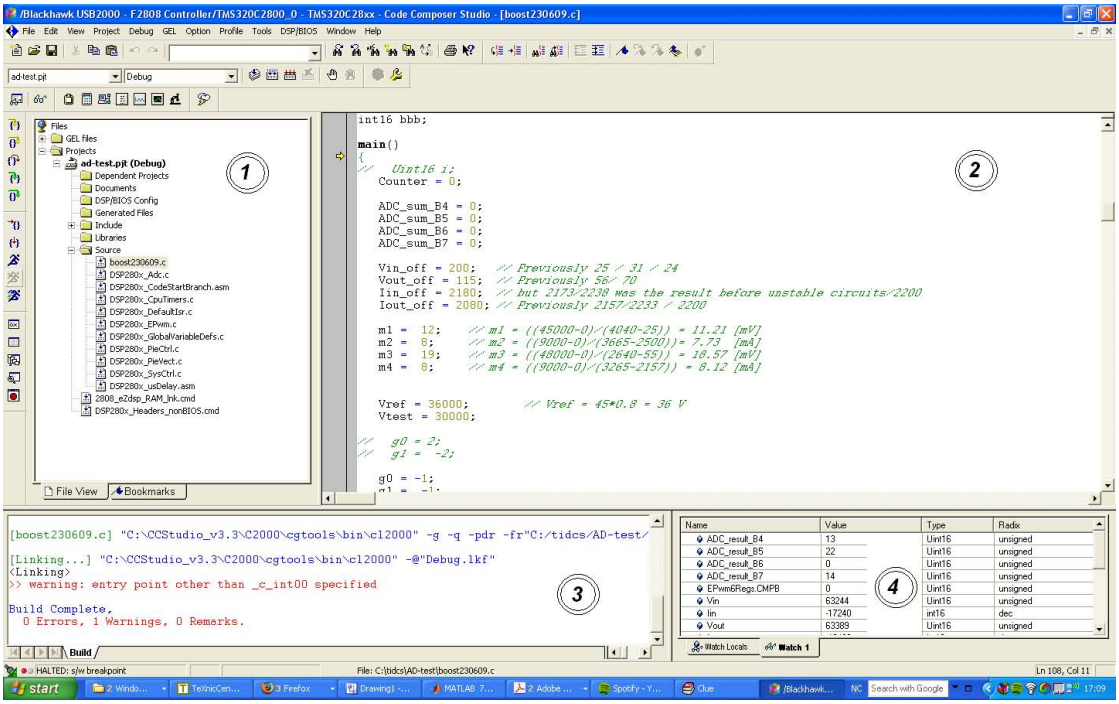


Figure 47: The user interface of Code Composer Studio

5.2.2 Blackhawk USB2000 Controller

Blackhawk USB2000 Controller is a JTAG Emulator specially designed for cooperation with TI TMS320C2000 DSP developers. It creates communication between the host PC and the controller and is compatible with Code Composer Studio.

5.3 Operations and routines in the programming

For developing the program code it is important to know which routines are necessary for correct program execution. These operations can be divided into two groups, basic and high level. The basic operations make sure the fundamental tasks are done, like system initialization and operation. The high level routines provide for superior control to prevent unstable operation due to errors (like a regulator and the MPPT) or manual changes of variables during operation.

5.3.1 Basic operations and routines

Some basic building block routines are necessary to include in the DSP program. These can be summarized as follows:

Event/Operation	*Explanation*
ADC Conversion	Sampling of the values and storing in defined variables
Boundary check	Make sure no variables are outside its limits (especially duty cycle)
Error calculation	Calculate the error between the reference value and the sampled value
Multiplication	Handles the multiplication operation of two values
Division	Handles division of numbers

5.3.2 High level routines

The high level routines includes the control of the DC-DC converter operation. These comprise the regulator (which can be either a P, PI, PID or other types of controller) and MPPT. The MPPT delivers the reference value for the feedback control loop.

5.4 Development of each block

The block diagram in figure48 shows what is intended to happen within the DSP Controller. This equals the grey box in figure 31 in section 4.

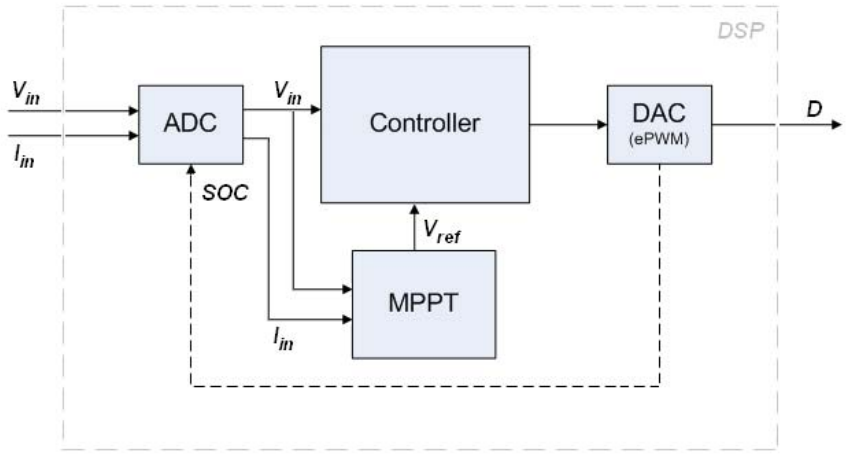


Figure 48: Block diagram of DSP contents

The values from the PV terminals will be collected from the circuit through sampling in the ADC module in the DSP. Then the voltage will be transferred further to the controller, where the error between this voltage and the reference voltage is calculated. The controller calculates a new compare value which is sent to the DAC module (ePWM module). Here the control signal is compared to a sawtooth signal as described in figure 12. One of the output signals from the DAC will then be a pulse described by the duty cycle D. Another output signal from the DAC module triggers the Start-of-Conversion in the ADC as indicated from the feedback loop. The MPPT algorithm will also be implemented in the DSP Controller, using the sampled values from the ADC to calculate a new reference value. This value is then sent to the controller for error calculations.

5.4.1 Graphical overview over the DSP operation

The operation of the DSP related to the generated sawtooth signal in the ePWM6 module is shown in figure 49. The period PRD is the sampling period. Every time the sawtooth begins a new cycle (counter CTR = 0), the ePWM6A signal goes high. When the counter equals the compare value COMPA, the ePWM6A signal goes low and generates an interrupt that triggers the Start-of-Conversion (SOC). When all the values are converted, an End-of-Conversion (EOC) signal generates a new interrupt where the raw values are scaled and the control code is executed. The controller calculates a new compare value COMPB which is updated in the ePWM register and used during the next cycle. The

remaining time of the cycle is spent on running the background loop (which is often an infinite loop in the main loop normally doing nothing).

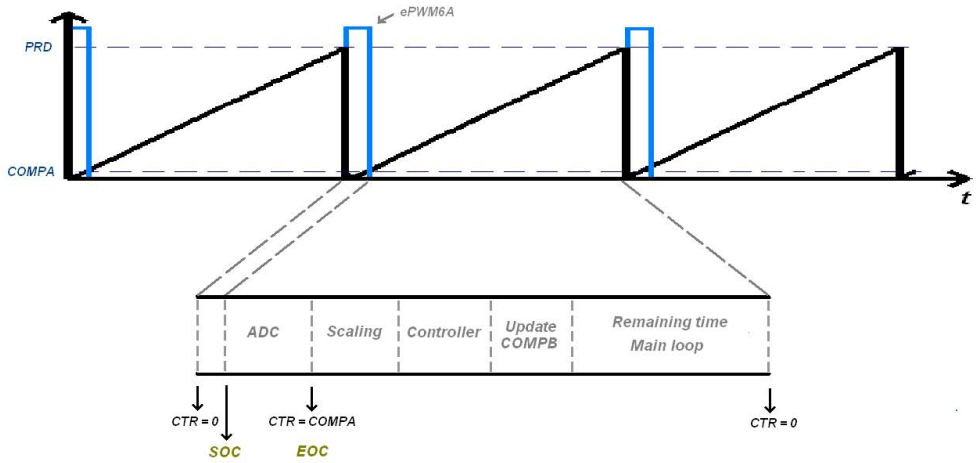


Figure 49: Graphical overview of DSP operation

In the following sections the code development of the different modules are described, without any direct C code reproduction. The complete code with comments is given in the appendix E. The reference guide regarding the current module is given in each section and can be found at the homepage at TI.

5.4.2 ADC module

When developing the code for the ADC, it is important to know what information is required. The ADC module needs initialization, which is done within the main loop. The ADC also needs to know how many values it should sample, from which pins and in what sequence. The module is able to read the values in series (sequential mode) or several values at the same time (simultaneous mode).

Measured values and pin allocations The input voltage is a given measurement requirement in the calculations. The MPPT algorithm also requires the current for power calculations, as seen in the block diagram (figure 48. Accordingly there are two variables needed for the control loop in the DSP. In addition the output voltage and currents are included, to be able to observe the converter operation and make sure that no unexpected incidents occur during normal operation (like unexpected behavior of the electronic load).

There will be 4 conversions of variables in a sequential mode (the simplicity of the program avoids problems concerning too little time for calculation after AD conversion), and each of the variables is assigned a pin as stated in table 9.

Table 9: ADC pin allocation

Measured value	*Pin*
Input voltage	B4
Input current	B5
Output voltage	B6
Output current	B7

ADC interrupt During the conversion the sampled values are stored in temporary variables. When the conversion is complete (referred to as EOC (End-of-Conversion)), an interrupt is triggered where the sampled values are stored in the right variables and used for calculations. This interrupt is called *adc_isr*.

Information about the ADC module features and operation is found in the *TMS320x280x DSP Analog-to-Digital Converter (ADC) Reference Guide* (SPRU716B).

Scaling All measurements have an offset and gain error that will influence the calculations if not taken into consideration. This is due to several reasons, like inaccurate resistor values, inaccuracies of reference voltages, offset of sensors, tolerances in gain and offset error of op amps. Hence it is necessary to **calibrate** the complete measurement chain before using the values for calculations.

The calibration process can be done in two different ways in the DSP. Automatic scaling is implemented in the program initialization code and is done at every startup, while manual calibration is done once and implemented in the program. The automatic scaling is the most elegant way of calibration, but is also more complex to implement. In this master thesis the manual approach is chosen.

The next step is to scale the bit values to meaningful values. Instead of storing the raw bit values in the variables, physical units are preferred. When fixed point variables are used, care must be taken so that the accuracy stays as high as possible. Therefore the voltages are stored in mV and the currents in mA.

The two linear scalings (calibration and scaling to meaningful units) are done in one step in the DSP program. This is shown in the following equations.

$$V_{in} = (V_{measured} - V_{offset})_{raw} \cdot \frac{(V_1 - V_2)_{real}}{(V_1 - V_2)_{raw}} \tag{43}$$

$$I_{in} = (I_{measured} - I_{offset})_{raw} \cdot \frac{(I_1 - I_2)_{real}}{(I_1 - I_2)_{raw}} \tag{44}$$

5.4.3 ePWM module setup

The operation of the boost converter is set to be PWM switching of Q3 and $\overline{PWM}$ switching of Q4, but the design of the converter circuit allows boost conversion without the inverted switching at Q4. Therefore this approach is chosen, with the ePWM6B output connected to Q3. The switch Q1 must be in constant ON-state, which is done by connecting the gate directly to the 12 V voltage level in the control circuits. This could also have been done by using a ePWM output or a regular GPIO, but as there are no topology transitions during the system operation the simplest approach is chosen.

Information about the ePWM module features and operation is found in the *TMS320x28xx, 28xxx Enhanced Pulse Width Modulator (ePWM) Module Reference Guide* (SPRU791).

5.4.4 Start-of-conversion (SOC) sequence trigger

As seen in the block diagram of the DSP (figure 48 there is a feedback from the DAC block to the ADC block, indicating a SOC signal. The ADC needs to be told when to start the conversion of values, and this trigger signal can be generated in several ways (either continuously, from an ePWM module or a peripheral GPIO). By selecting the ePWM module to trigger the SOC, the sampling frequency and the switching frequency are synchronized (see 3.2.4). When only one PWM signal is required for converter operation, one ePWM module can be used for both generating the gate switching signal and the SOC. The SOC can be seen as an implicit interrupt. The ePWM6A output is used for SOC and is started right after the sawtooth has started a new cycle.

5.4.5 Controller

The code for the controller is placed within the interrupt *adc_isr*. After the storage of the variables the controller calculates the new duty cycle value and stores the variable in the compare variable of the ePWM module. Two different types of controllers are used, which are the P- and the PI-controller. The code is divided in two, where the P-part and the I-part is calculated separately. This makes it possible to remove the I-part and hence switch between the two controllers without changing the code during operation. The controller execution is shown in the flow diagram in figure 50.

The parameters of the P- and PI-controllers are often found to be fractional values, which represents a challenge in the DSP. This was solved by multiplying the parameter value by a value 2^n to become an integer number. Then the error variable was truncated (divided) by the same number, so that the output was scaled correctly.

5.4.6 MPPT

The MPPT is not required to be as fast as the voltage controller, and therefore the MPPT code is placed in the main loop (as seen in figure 49). Code placed in the main loop will normally be executed when there is time left after running an ISR, and will not necessarily happen at a fixed interval. This is not fortunate, and to avoid random execution of the MPPT one of the CPU timers is set to control the execution of the MPPT algorithm. Every time the timer reach a certain preset point in time the MPPT algorithm runs and the CPU counter is reset. This way the MPPT is actually disguised as an interrupt. The P&O algorithm is chosen for MPPT due to simplicity and less arithmetic calculations needed. The efficiency is also expected to be rather good.

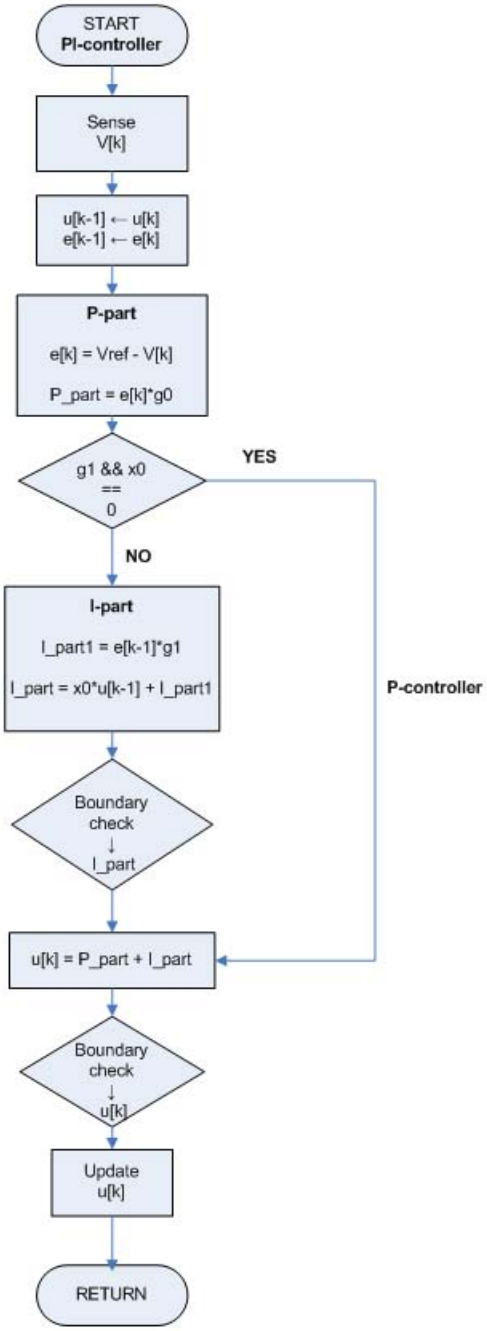


Figure 50: Flow diagram of the implemented P-/PI-controller

6 Experimental setup and results

This thesis has had an experimental approach to the development of the control system. Based on the theoretical approach through small signal AC modeling the controller could have been based on the transfer function. The different transfer functions for CCM and DCM however makes this a more cumbersome method, as the controller will be based on only one of the operation modes. In real systems the transition between these two modes will occur rather often, and an experimental approach through utilization of the Z-N method will lead to a controller valid for the whole range of operation.

The basic modules of the software, like the ADC and the ePWM (DAC) programming code, could be developed and tested separately without full system setup. But for the control code development, first the controller and then the MPPT, a complete system was required for testing and observation of the system response.

6.1 Equipment

A full overview over all components included in any of the experiments is given in appendix G.

6.2 Laboratory setup

The experiments were performed in a power electronics laboratory with the setup shown in figure 51.

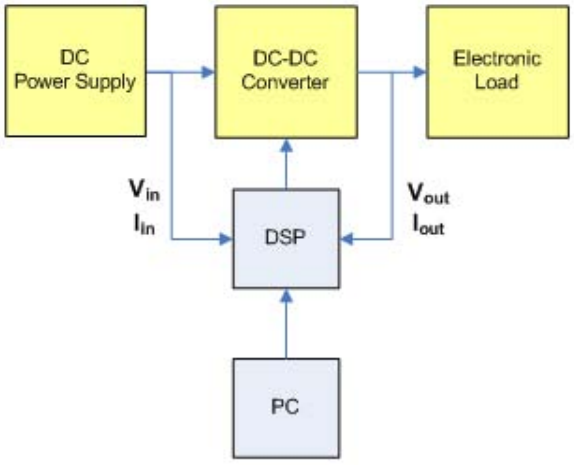


Figure 51: Laboratory setup

The yellow blocks indicate the part of the system where the actual power transfer is happening, from the DC power supply, through the converter and to the electronic load. The blue blocks indicate the control part (digital part) of the system, which includes collection of values from the power circuits and generated output signal sent to the converter for influence of the power transfer (this is almost equal to figure 31).

To be able to do testing of the controller and the MPPT a PV Simulator was used as power supply. The PV simulator is equivalent to connecting a PV panel in parallel with a capacitor. For supplying the input of the control circuits a separate DC power supply was used[10].

The generation of the PWM signals needed for the switch control came from the DSP Controller, with a constant switching frequency of 20 kHz (equal to the sampling frequency). The converter was set to **boost operation** through connecting the switch Q1 to the control voltage level of 12 V on the PCB for continuous ON-state operation and switching Q3 from the DSP board. The switch Q4 was never used with inverted PWM signal, as the diode D4 could operate as boost circuit diode. Hence the converter was always run as a non-synchronous DC-DC converter, introducing both CCM and DCM operation.

The load was represented by an electronic load which could be operated as either an constant voltage, constant current or constant resistance load. In these experiments it was set to constant voltage (CV) operation when the PV Simulator was utilized. Using the CV operation is equivalent to having a DC link capacitor in parallel with a load.

The HI circuits are assumed included in the figure and are not shown explicitly.

A picture of the real laboratory setup is shown in figure 52.

6.3 PV simulator as DC power input

The PV simulator has rated values at:

Table 10: Rated values of PV simulator

	Value
V	300 V
I	20 A

The simulator has in general a square I-V characteristic, where the MPP is found when both the voltage and the current are at their maximum values. To adapt the characteristic to a more common and non-ideal regular PV characteristic, the MPP can be defined in the simulator and the curve will be adjusted. Hence there are 4 values that define the

[10] In the finished laboratory setup the control circuits must be supplied from the PV panels

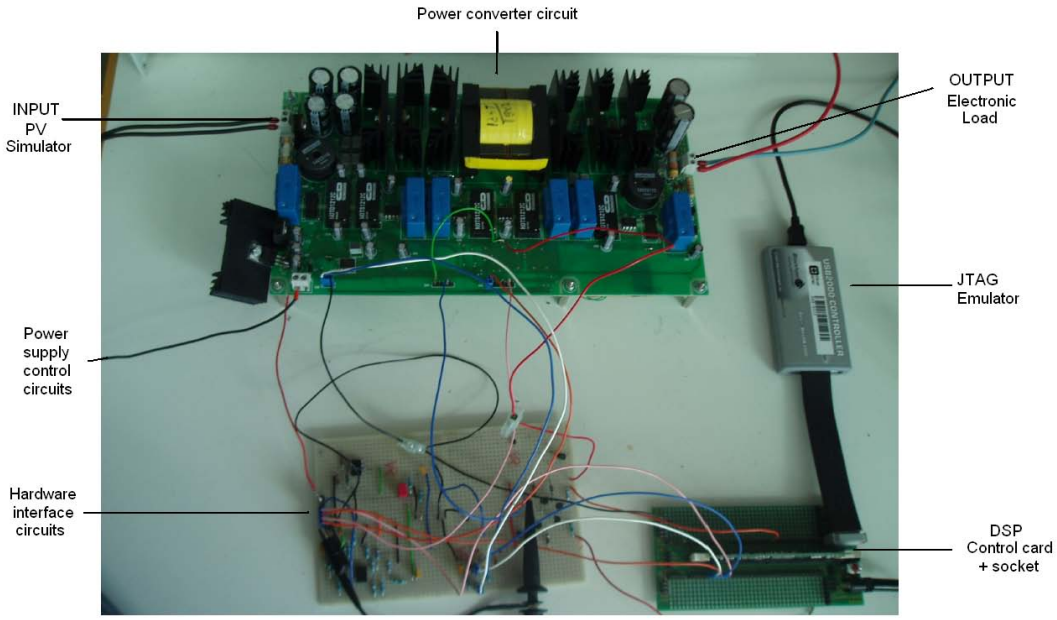


Figure 52: Laboratory setup - real

curve. These are given in the table 11 together with the values used in the experiments. The maximum power was set to be 180 W, valid for irradiance level E = $1000\frac{kW}{m^2}$ and temperature level T = $21°C$.

Table 11: PV Simulator variables

Variable	*Definition*	*Chosen values*
U0	Open circuit voltage	45 V
Ik	Short circuit current	6 A
Umpp	MPP voltage	36 V
Impp	MPP current	5 A

It was noted after some testing that the simulator at this voltage level has an offset of 4 V, so both U0 and Umpp had to be set to 4 V less than wanted as output. When the control circuits are turned on and no PWM signal is sent to the switch (i.e. D = 0), no current is flowing in the circuit and the DC link voltage is equal to the PV simulator open circuit voltage of 45 V.

The irradiation and temperature levels can be varied through separate knobs on the simulator, as well as programmed from a computer. The I-V and P-V characteristics for the PV Simulator was found for different levels of the atmospheric conditions and can be found in appendix H.2.

6.4 Experimental results

Several experiments were performed and the most important results of these will be presented. The experiments included ADC and DAC tests with SOC included, calibration, implementation of the controller by use of Ziegler-Nichols method and MPPT.

6.4.1 ADC

The 4 defined values from the input and the output were collected through the ADC module. In the beginning the values were varying a lot, and it was hard to decide a specific value. When the filters on the output of the HI circuits were implemented some improvement was obtained, but still the variation was rather large. It was decided to use average values hopefully to even out the variations. The averaging made the variations a bit smaller, as well as easier to read. This averaging made the whole system operation slower (depending on over how many values the averaging was done), and the interrupt handling shown in figure 49 was changed. The SOC and the EOC still happened as in the figure, but the controller calculations and the duty cycle update was occurring at a slower rate.

Calibration of the measurements The calibration was done manually. The values were a bit noisy, which made it hard to find suitable values, but the averaging of the measurements made it slightly better. The slope was slightly nonlinear, which created some errors between the real values and the ones in the DSP program. Thus the offset and slope values were altered during the experiments to fit the operation better.

6.4.2 Ziegler-Nichols

The Ziegler-Nichols method was used to find the controller parameters. The code for a P-controller was implemented and the gain was increased until the system reached the critical stability. This gain was found to be $K_{p,k} = -\frac{4}{32}$ with the time period of the stationary wave $T_{p,k} = 26$ ms.

For implementing the P- and the PI-controller the starting parameters were found to be as presented in the table 12.

Table 12: Parameters for P- and PI-controller by use of Z-N

Controller type	K_p	T_i
P	$-\frac{2}{32}$	∞
PI	$-\frac{2}{32}$	21,7 ms

6.4.3 P-controller

When implementing a P-regulator for boost converter control, the parameter gain must be negative. This is due to the fact that when:

$e > 0$: $V_{ref} > V_{in} \Rightarrow V_{in}$ must be increased, and D must decrease.
$e < 0$: $V_{ref} < V_{in} \Rightarrow V_{in}$ must be decreased, and D must increase.

During the testing it was obvious that the system was more affected by the controller gain at low reference values, and the slower the controller, the larger the gain could be without the system becoming unstable. When the measured values were averaged over a low number of values, the system soon experienced stationary oscillations, especially in the electronic load. This was probably caused by resonance in the system, and it was decided to make the controller execution slower. After testing of several controller frequencies the P-controller was set to run for every 256th ADC.

The P-controller was tested within the voltage range from 0 to 45 V with the gain from the Z-N method. Then it was increased to $-\frac{3}{32}$, and it turned out that the system was still operating under stable conditions with the increased gain. A test series was done for the last gain with stepwise variation of the reference voltage. This is presented in figure 53, showing the voltage values of the PV simulator, the input of the circuit and the voltage read by the DSP compared to the reference voltage.

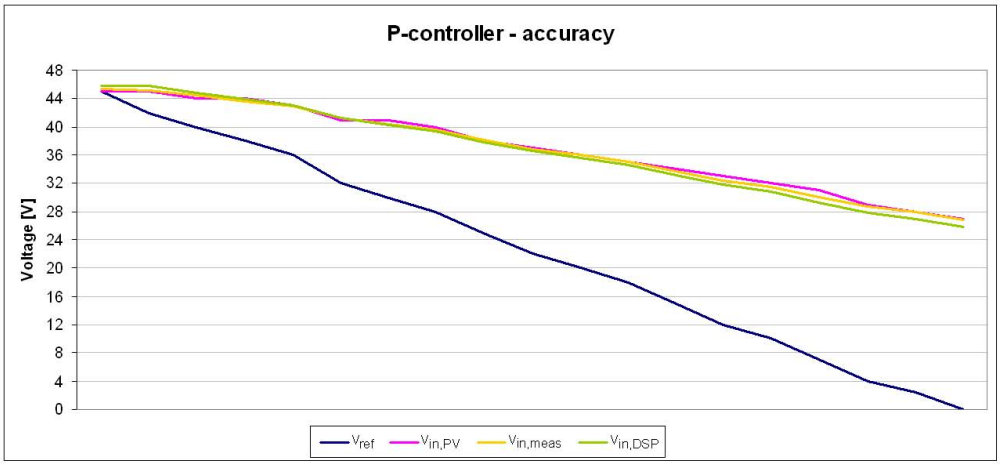


Figure 53: Accuracy of the implemented P-controller

As expected, the controller was not able to follow the reference value too well. The deviation was rather large, especially for lower reference values. The largest duty cycle delivered by the DSP was almost 2500, which is only half of the possible range. To obtain a system following the reference an integrator is absolutely necessary.

6.4.4 PI-controller

When programming the PI-controller the definition of the variables is even more important than for the P-controller. There are more arithmetic operations in this recursive algorithm, and the outcome of the variable can be different than intended. All variables were defined to 16 bit, with a mix of signed and unsigned integers.

The parameters for the continuous PI transfer function is given in table 12, and the discrete parameters g_0 and g_1 had to be calculated from these.

$$g_0 = K_p(\frac{T_s}{2T_i} + 1) = -\frac{2}{32}(\frac{50us}{2 \cdot 21,7ms} + 1) = -\frac{2}{32} = K_p \tag{45}$$

$$g_1 = K_p(\frac{T_s}{2T_i} - 1) = -\frac{2}{32}(\frac{50us}{2 \cdot 21,7ms} - 1) = \frac{2}{32} = -K_p \tag{46}$$

It actually turned out that both parameters should have the same sign to get correct adjustments according to the reference value. With the code implemented the best solution was found when both parameters were equal, and the reference was followed quite satisfactory. The gain was increased to see how large it could be before the system turned unstable and was found to be -$\frac{4}{32}$. So with a gain at -$\frac{3}{32}$ the system was stable for the whole voltage range.

With the implemented code it was discovered that the gain parameter values do not affect the operation too much as long as they are equal. Seen in relation with the Z-N and discretization of the controller the choice of parameters was not so important as long as the gain was not too high. The duty cycle value of the previous cycle is rather dominant, so the error calculations do not affect the operation so much at lower error values. The fact that the handling of the variables in the code makes the error handling less effective might be a drawback of the algorithm. So the structure of the code is rather important when the parameters are tuned. However, as the reference is followed rather well with the implemented PI-controller, it is decided to use this one. It must be noted that when the duty cycle goes into saturation, the controller is not able to follow a too large step change in the reference. But during normal operation the reference change will be decided by the MPPT, with a constant change that is rather small. And within the linear operation step changes of at least ± 10 V are followed.

Measurements done with the highest possible gain was done with the reference voltage changed stepwise from 45 V down to 0 V, as for the P-controller. The whole range is shown in figure 54. Considering the reference voltage and the voltage read by the DSP, the controller was working properly for the whole range until a lower reference voltage of 1,5 V. At this stage the duty cycle went into saturation. This is not visible in the figure, as there were no measurements done for lower values than reference voltage equal to 1,5 V.

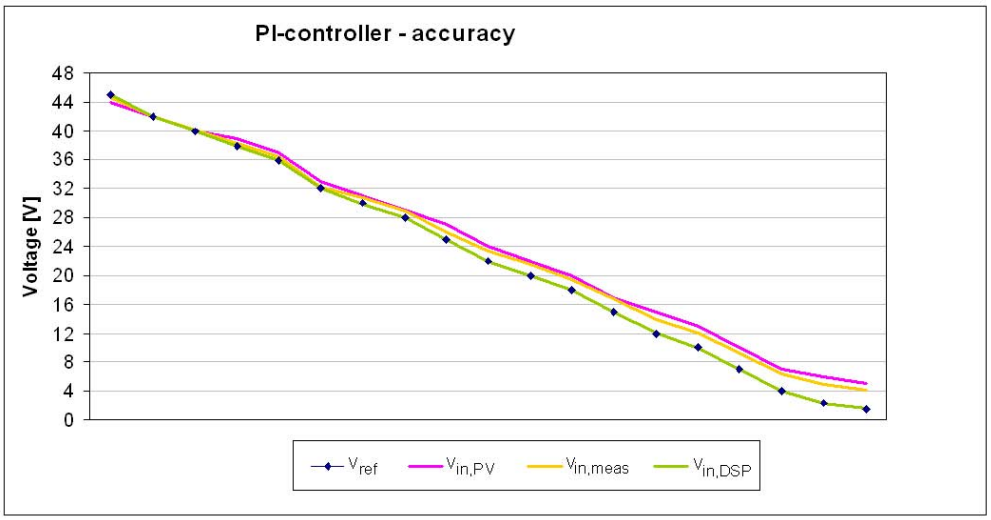


Figure 54: Accuracy of the implemented PI-controller

By observing the difference between the values in the DSP and the actual voltage, it is clear that the calibration is of great importance. The calibration parameters in the code are adjusted for large voltage values, so at lower voltage values the deviation between the actual input voltage and the voltage in the DSP is increasing.

6.4.5 P&O MPPT

The MPPT experiments were run with different parameters of duty cycle step and time step to see the difference in the power output and the oscillation ripples. The power production was varying a little for each experiment. It was done experiments with smaller step change, which caused a slightly lower power output over time. But the power loss was not significantly. It was decided to use a step change of $\triangle d = 0,01$(equal to DELTAV = 480), and a MPPT sample time of 1 second. With this time step the MPPT was running quite slowly, but the results were satisfactory and made it easier to do controlled changes in the atmospheric conditions throughout one experiment.

By comparing the power production after implementation of the MPPT with the maximum power point of different atmospheric conditions, it could be considered how well the implemented MPPT algorithm is working. The MPPT was executed for variations in irradiance levels (with constant temperature T = $21°C$) and in temperature levels (with constant irradiance E = $1000\frac{kW}{m^2}$). The sampling was done once every second, and the step change in voltage (perturbation) was set to 1 % of the DC-link voltage, 0,48 V.

Variations in irradiance levels When varying the irradiance level, the change was done stepwise, as it will be in reality. Throughout a normal day with partly clouding,

the change in irradiance level changes in steps and rather rapid due to clouds covering the sun for shorter or longer durations. As mentioned previously the current is the factor most affected by these variations, and this was also shown in the measurements. While the voltage had a rather small range of change, the current had stepwise increases or decreases (depending on increase or decrease in the irradiation level).

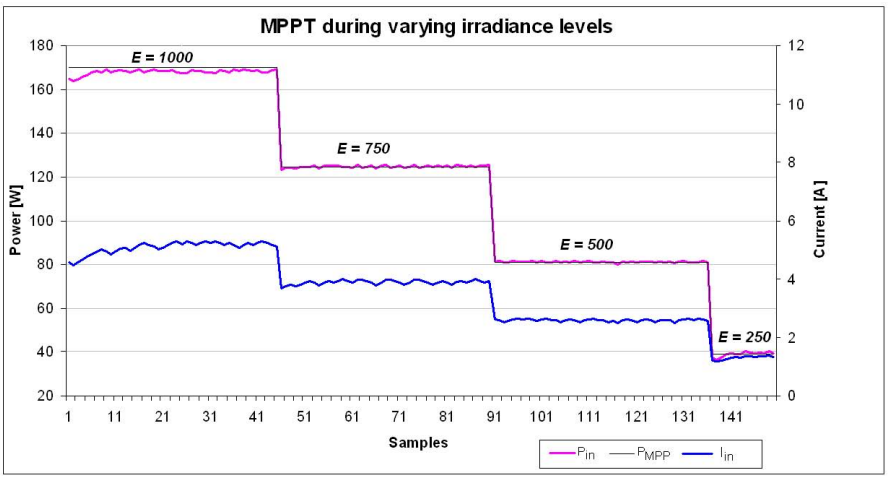


Figure 55: MPPT for stepwise change in irradiance level

The MPPT can be seen in figure 55. The black graph accounts for the theoretically maximum achievable power for that particular temperature and irradiance level. It is obvious that the characteristics found for the PV Simulator are not totally accurate, as the generated power from the PV panels are at times higher than the assumed MPP. Considering the inaccuracies of the measurements, the MPPT algorithm is concluded to track the MPP rather well for varying irradiance levels.

Actually the MPPT is not affecting the operation too much in this case, because it is changing the voltage level. The current is the factor experiencing the biggest change in case of irradiance variations, which is also visible in figure 55. Based on the figure and the theoretical background presented in the beginning of the report, the V_{MPP} is not varying too much.

Variations in temperature levels To really test the capability of the implemented MPPT algorithm, changes in temperature were executed. In reality the temperature changes will be changing steadily and continuously over time and will not change stepwise like the irradiance level. In these experiments, however, the MPPT was working under stepwise changes of the temperature. This way the MPPT can be said to be tested for extreme conditions. The result of a stepwise increase in temperature with 30 seconds at each temperature level is shown in figure 56.

The MPPT is able to find the maximum rather well and at a fast speed. It is shown that

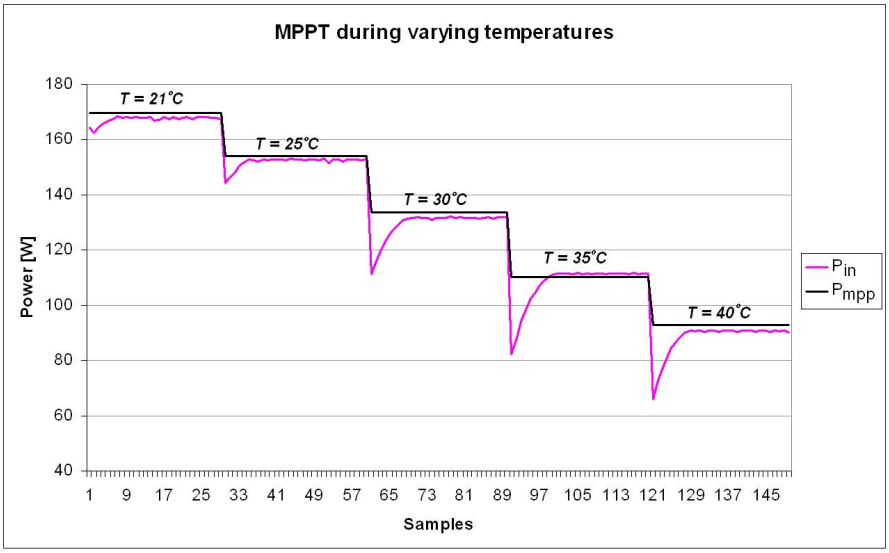


Figure 56: MPPT for stepwise change in temperature level

each time the temperature increase, the MPPT will track a little too far, but then change direction and move towards the current MPP. Considering the fact that the temperature change will not be this brutal in reality, it is assumed that the tracking in the wrong direction will not occur as often and as far as in this experiment. The MPP found from the characteristic appears to be quite accurate, except for the temperature levels T = $35°C$ and T = $45°C$. But this is rather due to different operating conditions when doing the MPPT experiments and when finding the PV simulator characteristic. A difference in behavior during increase and decrease in the temperature was also discovered. The MPPT is tracking more in the wrong direction when the temperature increases then decreases.

7 Discussion

The full system setup studied in this master thesis consists of a DC source simulating the PV-panel, a DC-DC converter and a load representing the grid connection through an inverter and a transformer. The DC source is a PV simulator with a PV System I-V characteristic, giving the possibility to do experiments on a realistic system. A program was developed to create an independent control of the system, comprising MPPT and a PI-controller. The developing process together with the experimental results will be discussed further.

In this master thesis there has been presented a lot of theoretical background regarding the converter topologies and available control developing tools that has not been utilized in the laboratory work. This has been done with the ulterior motive of presenting methods that can be used or explored in the further development of the system. In the control development the focus on simplicity has been chosen in deciding the controller and MPPT algorithm. It has also been focused on giving an overall overview of the system composition and giving a platform for further development.

7.1 Boost converter as DC-DC converter topology

Even though the available converter circuit is designed to operate as both boost, buck and buck-boost converters, the boost topology was chosen for the control development. The obvious reason of making this decision was the suitability of this kind of converter topology in a PV converter system. In most of these systems the DC link voltage will be at least 350 V, and for small systems this voltage level might require too many modules connected in series (due to cost and size). By implementing a boost converter as a power processor stage in the system, the input voltage can be less than the DC link voltage.

The DC link voltage level was assumed to be 48 V, approximately the same as nominal voltage range of the converter. With a desire of operating at maximum 50 V, the demand for stepping up the voltage was most frequent. If the DC link voltage level is lowered (to for instance 24 V), the range between boost and buck operation will be more evenly spread. This might be an idea for future development, where the buck topology is likely to be utilized in the development process. Gradually the system will probably be required to switch between the buck and the boost mode during normal operation. In this situation there will be a defined voltage range where the system changes from one operation scheme to the other.

7.2 Development of the hardware interface

Before the complete system could be assembled, the interconnection of the converter and the digital controller had to be considered. Before the separate components could be connected, a hardware interface was needed because of different voltage tolerances.

There are of course many ways to create circuits to scale the voltage levels, and the ones chosen had both some advantages and some drawbacks.

The difference amplifier circuits were found suitable seen in connection with the characteristic of the current transducers. It was a good way to scale the "zero current" voltage of 2,5 V to approximately zero and hence be able to utilize the full resolution range in the DSP Controller. Regarding the current direction there was a little uncertainty whether or not to design the circuits for unidirectional or bidirectional current. In a grid connected PV system the current direction will normally flow in only one direction, towards the grid. As mentioned in the theoretical background there is normally no energy storing components in these systems that requires current flowing the other way. If so, this component will most probably be connected to the DC-link, which again requires no negative current through the converter stage. But as the converter is designed for both synchronous and non-synchronous operation, it was decided to not exclude the possibility of bidirectional current. The proposed HI circuit is not difficult to alter in the future, but it should be decided a range for the current before implementing the circuit together with the converter circuit on the PCB. Especially with the input voltage V_{diff} in mind, which will have to be supplied from a source on the PCB.

Using voltage dividers is a simple and effective way of obtaining voltage scaling, and has been utilized several places in the circuit. It must be remembered that the resistors values are given with a certain precision range and will vary slightly. This might cause unexpected voltage drift, which might affect other values in the system. For the voltage dividers used to scale down the input and output voltages the possible voltage drift can be accounted for through the calibration in the DSP program.

The hardware interface circuits were changed several times because of changed nominal value selection and lack of overvoltage protection. There was a bit uncertainty with regards to the limits, as the converter has never been tested before. The NI ELVIS II equipment proved to be a quite useful tool in the development process. The circuits in question are rather simple and well known, and hence they where assumed to operate as intended. But for more complex circuits the NI ELVIS can be a powerful tool. It's easy to make alterations in the circuit as well as doing simple testing using the built-in tools of the workstation.

It was encountered a lot of noise in the hardware interface circuits, especially in the current measurements. It was attempted to reduce the noise through implementing filters and averaging the measured values, which was improving the system slightly. However, the averaging of the measurements in the DSP Controller should be avoided in the future, due to reduction in the bandwidth of the control loop. The averaging can be said to equal a low pass filter with very low corner frequency.

A reason for the noise was especially the earthing of the system. As seen from the system setup, the connection between the DSP, the HI and the converter PCB caused a lot of wiring, and some of the connections were a bit unstable. To be able to connect and disconnect the separate circuit boards without having to solder, the connections was mainly

done through pin connections. These were easily broken without extra protection and could some times cause short circuits if they got in contact with other pins. Eventually the system became more stable when the system earth was placed in one point. It is also expected that these connection problems will vanish (or diminish) if the whole system is mounted on one PCB. Thus the connections will automatically be more stable.

7.3 Development of the software

The development of the software was quite a challenge without no previous knowledge about practical Digital Signal programming. Understanding the structure and operation of the DSP controller was the main challenge and it was a time consuming process. But after a lot of reading and testing the understanding increased and the learning outcome has been great.

The development of the program structure and code was a very instructive process. The possibility to create the parts one at a time, without needing a complete system up and running, makes this process very suitable for a laboratory setup. The program could be divided in different modules, like the ADC, the generation of PWM signals and a controller to modify the program. It was chosen to develop the code in the C programming language, as the example files from TI as well as Code Composer Studio are more adjusted for this. The C language is similar to other modern programming languages, and the code structure was rather familiar. The main challenge when starting the programming was understanding the structure of the DSP Controller and how the module registers were managed.

An evident source of error was the definition of variables in the C program code. When defining variables as a 32 bit number, incidents of overflow happened a lot because of mixed arithmetic (between 16 and 32 bit numbers). However, learning how to handle the variables while programming is a step in the process of understanding the digital programming, and once learned it was quite straightforward.

The program code was based on the example files from TI, which turned out to be very helpful in the program development. To overcome the possible problem of dealing with fixed point numbers the variables were given in mV and mA. This solution provided higher resolution and accuracy of the measurements read by the digital controller.

7.3.1 Calibration

The calibration was done manually through measuring the offset values and slope of the values. This could also have been done by the program itself through the initialization process, and should also be included in the program code at a later stage. The calibration was done manually and then altered along the way to fit the actual values as good as possible. It was discovered that the slope is slightly non-linear, and the calibration will

not be right for all values of the reference value. The value read from the DSP is following the reference quite well with the PI controller, but by measuring the actual voltage from the PV simulator it was noted that the difference was increasing with decreasing voltages. So how the calibration is done in the program is important for how the actual values are managed. For now there has not been decided a limit for the voltage range of the input, and the calibration was best fitted for higher voltage values. If the range is decreased, the calibration can be better fitted for this range.

7.3.2 The voltage mode controller

The program code developed for the controller was structured so that it is possible to easily change between P- and PI-controller during operation. This was initially done for simplifying the testing during the laboratory work, but might also be useful for later. The implementation of the P-controller was mostly done for developing reasons, as the utilization of the Ziegler-Nichols rules requires a P-controller for finding the critical stability limit of the system. The P-controller alone is seldom a sufficient controller in industrial system, but operates as an important basic block of the more advanced controllers utilized.

A more applicable type of controller is the PI-controller. It is still a rather simple type of controller compared to other more complex types (as the Type I, Type II and Type III often used in converter system), but at the same time it serves its purpose. As seen from the experimental tests the integral part of the controller was able to remove the error that the P-controller could not handle. From the flow diagram of the implemented controller code earlier in this report, a boundary check of the integral part is normally necessary. This is to prevent the controller to be too slow if the error gets too big. However, due to the structure of the code this was not actually directly implemented. At the end of every execution of the controller the duty cycle was checked for overflow. This was indirectly working as a limitation on the integral part, as the integral comprises the previous value of the duty cycle.

The parameters of the controllers was initially found by utilizing one of the Ziegler-Nichols rules. This is a well-known way of experimentally tuning controllers, and must be said to be a good starting point. However, additional tuning is often necessary to optimize the controller parameters. This was evident both for the P- and the PI- controllers, where the parameters were changed. The P-controller gain was increased from $-\frac{2}{32}$ to $-\frac{3}{32}$, as a larger gain gives a slightly smaller error. In the PI-controller the parameter values were calculated from the Z-N parameters, and while g_0 was kept as initially calculated, g_1 had to change sign. It has been mentioned that a digital controller based on emulation from a continuous controller most probably will give a poorer result than in the original controller. This was not proved to be a problem in this thesis, as the PI-controller was providing a proper closed loop control.

Due to oscillations between the digital controller and the electronic load during the

experiments the execution frequency of the controller was decreased to avoid instability. The oscillations were most probably caused by resonance between the converter circuit and the electronic load. The controller speed reduction should be avoided in the future, as the bandwidth of the control loop is reduced 7.2. It must be remembered that the electronic load is only a replacement for the rest of the system (inverter stage, transformer and grid), and when the whole system (or parts of it) is connected, the conditions of the system will be different. This may require a change of the code and also the parameters.

In this master thesis direct duty cycle control was utilized through voltage mode control. This is the easiest method and it proved to be sufficient. In the future it is also possible to implement current mode control by applying a current feedback loop from the switches.

7.3.3 MPPT

As the system was tested for the first time, the simplest MPPT algorithm P&O was implemented in the C program code. This algorithm was also expected to have a rather high efficiency, and it was interesting to observe the capability of the algorithm. As seen from the experimental results the MPPT was rather successful, tracking the MPP of both variations in irradiance and temperature levels. The oscillations around the MPP was observed, and sometimes the tracker was confused and tracked a few steps in the wrong direction. This was more obvious when the temperature was changing, as the PV voltage the parameter most temperature dependent and the MPPT is changing the voltage and not the current. With too large step changes of temperature, especially at high temperatures, the MPPT was unable to track until the temperature decreased to a certain level again. When the steps was decreased, this was no longer a problem. The stepwise temperature changes will not happen in real systems (at least not as fast as in the experiments), and the functionality of the MPPT was seen to be satisfactory.

The MPPT parameters duty cycle step and time step were not intentionally optimized. During the experiments several values were tested, and finally the values $\triangle d = 0.01$ and $T_{MPPT} = 1s$ were chosen. The duty cycle step was set to 1 % of the DC link voltage, and this choice was found to contribute to the rather good tracking. The slow speed of the MPPT execution was set to make it easier to change the atmospheric conditions during the experiments. This was done manually, and to have control over when changes were to be executed, an time interval of 1 second was suitable. It must be mentioned that the higher the duty cycle step change, the higher the ripple will be. The stability of the system must be taken into consideration when choosing the sample time and the step change. This applied for constant irradiance and temperature throughout the test.

The tests were done for rather slow changes. So it was not actually tested how well functioning the algorithm is for rapid change in irradiance. But as mentioned in the results, the current is the most affected variable, and hence the voltage is not needed to change as much. With this argument it is assumed that the MPPT will operate quite satisfactory for these conditions as well.

By implementing the INC algorithm an improvement of the MPPT efficiency might have been obtained, but for now the P&O algorithm was seen sufficient for testing. Earlier studies have also observed decreased efficiency of the INC algorithm, due to the same reasons as for P&O, giving oscillations around the MPP. For further work it would be interesting to implement also this algorithm to analyze how much the efficiency is affected. Due to noise and measurement and quantization errors the MPPT efficiency is in general observed to be unable to be maximized.

7.4 General experience with the DSP Control Equipment

There were encountered several errors during the work, where the DSP disconnected while running or attempting to run. This was caused by a very noise sensitive connection between the DSP board and the emulator. The importance of testing the HI circuits before connecting the converter to the DSP Controller was evident during the experiments. Errors in the circuit design, like wrong choices of components or lack of overvoltage protection, were causing damaged DSP cards and lost connection between the DSP controller and the Emulator. It is important to remember not to touch circuit components while they are powered, especially if a person is not connected to ground. The person might be electrically charged to very high voltages, leading to electrostatic discharge (ESD), damaging the sensitive CMOS semiconductors.

7.5 Evaluation of the development process

The process of developing different parts for the laboratory module was both challenging and instructive. Knowing the theory about the physics behind is important, but understanding how the system works in reality requires hands on work.Development of software together with hardware operation requires understanding of the way the software utilized processes inputs and outputs and how variables are stored.

Altogether, the development process has provided insight in the suitability of such laboratory work. Students learning about Electrical Engineering and Digital Signal Processing at University level normally gain a lot of insight in the theoretical background within these areas. This theory is often limited to ideal cases, which is seldom the case in real life. To really understand the real life operation of such a system (like the PV system analyzed in this master thesis), laboratory work will function as a great learning platform.

To be able to implement this kind of system, the student is required to understand both the power stage as well as the control stage. These two areas represent two very important areas in the world of electrical power engineering. This applies especially for utilization of renewable energy sources, where the implementation of power conditioning is done by utilizing power converters.

However, it must be emphasized that the learning process will depend on how the laboratory setup is implemented when completed and how it is utilized.

8 Conclusion

The main purpose of this master thesis was to develop a closed loop control system for a DC-DC converter in a PV system through digital control. The intention of the control is to do Maximum Power Point Tracking (MPPT) to extract maximum amount of power from the PV input.

The boost converter topology was chosen for the analysis, due to the fact that this topology is more applicable in PV systems than the buck converter. The DC link voltage was set at a constant level of 48 V, while the input voltage could vary from 0 to 45 V.

Before connecting the digital controller to the converter circuit a hardware interface was necessary, caused by different voltage tolerances. A differential amplifier circuit was implemented for scaling the current measurements, while the voltage measurements were already scaled in voltage dividers. A first order RC filter was implemented in each of the circuits for noise reduction. The generated PWM signal needed a voltage boost before being sent to the gate of the converter switch, and this was done through a circuit with two transistors connected in series.

There were a lot of noise in the measurements, caused especially by unstable earthing of the system. Eventually all the different circuits (on the low power side) were connected to a common earth at the main PCB, which made the signals slightly more stable. It is assumed that the noise generation in the system will improve if the whole hardware system is mounted on one PCB. This way the connection through the wiring is avoided.

The control system was implemented through digital control, utilizing the C programming language for code generation. Control code for a P- and a PI-controller was developed where the parameters were found through tuning by Ziegler-Nichols' ultimate sensitivity method. This method proved to be rather accurate, but some adjustments were made to improve the controller functionality. Using the P-controller gave a deviation between the reference voltage and the actual input that increased with decreasing reference voltage. This was as expected, and an integral part was implemented to create the PI-controller. Now the reference was followed with high accuracy. The final parameters for each of the controllers were $K_{p,P} = -\frac{3}{32}$ (P-controller) and $g_0 = g_1 = \frac{2}{32}$ (PI-controller). It was discovered differences between the voltage read by the DSP and the actual input voltage, which was due to the calibration. It was evident that the calibration affects the system operation.

To conclude the Perturb & Observe MPPT algorithm was implemented. The MPPT was tested for both step changes in irradiance and temperature levels. When varying the irradiance level the current was the parameters most affected. Even though the MPP was tracked rather well there was uncertainty regarding the MPPT algorithm capability since the voltage was only exposed to minor changes. When the temperature was changed, the voltage was affected in higher degree. The MPPT was able to track the MPP rather well, and tracking in the wrong direction only happened right after a step change. In

real life the temperature will normally not change in steps, so this test was said to be done under extreme conditions.

The experimental approach for developing the control of the system was the focus in this thesis. This was a highly instructive process that has given a high increase in the knowledge about digital signal control of a PV system.

9 Recommended changes for next version of the PCB

It is strongly recommended to redesign the PCB before building a new one.

- Low input power supply to the control circuits
  The power needed to supply the control circuits is set to vary between 15 and 30 V. As long as the voltage is close to the lower limit, the loss in component U17 is not too big, but higher input voltages can be unfortunate. In the future the control circuit will be powered by the PV panel, and an idea to do this can be through a buck converter stage. Hence there will be less heat generation and a step closer to the real system.

- 3,3 V input to the input buffer stage for the PWM signals
  At the present PCB the input buffer stage requires a voltage input of the PWM signal of about 8 V and a voltage boost circuit was required. Doing a redesign to change the threshold voltage to 3,3 V can bypass the need of the transistor circuit proposed in the hardware interface section

- Fault feedback to DSP
  During overload conditions (either overvoltage or overcurrent) a signal should be sent to the DSP when the protection circuitry is active. This signal can be stored in a variable containing a 1 when the protection is active, and zero otherwise. This can done by some type of connection from in between the comparators and the gate drivers.

- Assemble all hardware on one PCB
  In this master thesis there has been 3 separate circuit boards, which are the converter circuit, the HI circuits and the DSP control card with socket. The connection of these parts has been a source of instability during the operation and it could be wise to collect all on one board (it is most important to include the interface board on the PCB, but also including the socket for the DSP Controller can make the system more complete).

- Include voltage dividers for establishment of the input voltage to the differential amplifier circuits

- Easier available outputs to do measurements through oscilloscope
  This might be a useful feature. Observing the waveforms of the voltages and currents during the system operation is a good way for gaining knowledge about the different converter topologies. The graphical interface CCS has a graph feature, but the current version is not too satisfying. In addition it displays only the discrete values, while there is no possibility observing the analog values.

- Update the system schematic
  Several versions of the schematic are available today, which might be confusing and lead to wrong connections.

10 Scope for further work

The development of the laboratory setup is still has some way to go, and there are many tasks that can be suggested for further work.

- Optimize the control system developed in this master thesis

  It has been proven that it is possible to control the converter with direct duty cycle control and PI-controller, as well as performing simple MPPT without the system getting unstable. However, there are still a lot of possibilities to optimize the system control. The code for the PI-controller can be improved, and an additional control loop can be added to implement current mode control. In addition the MPPT algorithm can be extended to the Incremental Inductance and be compared to the P&O to see whether or not the efficiencies are in accordance with previous experiments.

- Develop a control system for buck and buck-boost converter

  Up till now only the boost operation of the DC-DC converter has been tested with control run from the DSP Controller. The control scheme for the buck and the buck-boost operation schemes will probably be a bit different, but based on the theoretical background presented in this report

- Utilize actual PV modules as power source

  While testing the converter the source of the power supply has been less important. A task for further work could be to get hold of a suitable PV module to use as power supply. This can open up for a lot more testing and implementing the use of Maximum Power Point Tracking.

- Develop control code in assembly programming language

  Code Composer Studio operates with both C/C++ and Assembly programming languages. The example programs from TI are mainly based on C code programming, with some assembly coding included. The programming in this master thesis has been created the same way, and the use of assembly coding has been minimal. An idea for further work is to develop the same code with assembly programming language, as this gives a more intuitive understanding of how the processor works.

- Assemble the system

  When the inverter has been built the system can finally be put together. This opens up for a large-scale testing, where the system efficiency and the function of the MPPT can be examined. It should also be considered whether or not a battery and charge controller in the system. While putting the system together it is important to have in mind that this is meant for laboratory use. So it is important to have factors like safety and easy understanding of the setup in mind.

- Development of the lab assignment

  As this PV system is planned for laboratory use, there is a need for a laboratory assignment. The assignment can be presented as a development similar to the one that has been done in this master thesis, developing parts of the system one by one and making sure the different parts are working.

- Further testing of the DC-DC converter

  The testing of the DC-DC converter done until now has been rather limited and has mainly led to the conclusion that it actually works. It would be interesting to give a more thorough testing, examining for instance the dependency of frequency and duty cycle. The testing can give valuable information about the design, and this way it is possible to suggest possibilities of altering the circuit if necessary.

- Simulate the DC-DC converter stage included closed loop control

  The simulation in the master project has been limited to simple tests without any use of control. Closed loop control can easily be included in the model and can be used as a way to plan the DSP control development. A collation between the simulation and the actual result will also be of interest. The program toolbox PLECS has also been extended to generate C-code directly from the simulation, which might be interesting to try out.

- Develop the controller through use of Matlab/Simulink

  There are several ways of developing the controller for the system. In this thesis the experimental method has been the basis, but another method available can be through knowing the transfer function of the converter and developing the controller by using the SISO toolbox in Matlab. This requires more knowledge about the development of the converter transfer functions, which was not included in the thesis. The theoretical background of transfer functions are explained quite thoroughly in the references [33], [14] and [30].

- Field trip to the University of Dar es Salaam (Tanzania)

  Before implementation of the laboratory setup a visit to the University of Dar es Salaam in Tanzania can be useful. Exploring the conditions and possibilities of implementation might give valuable information for adjusting the system to the final product

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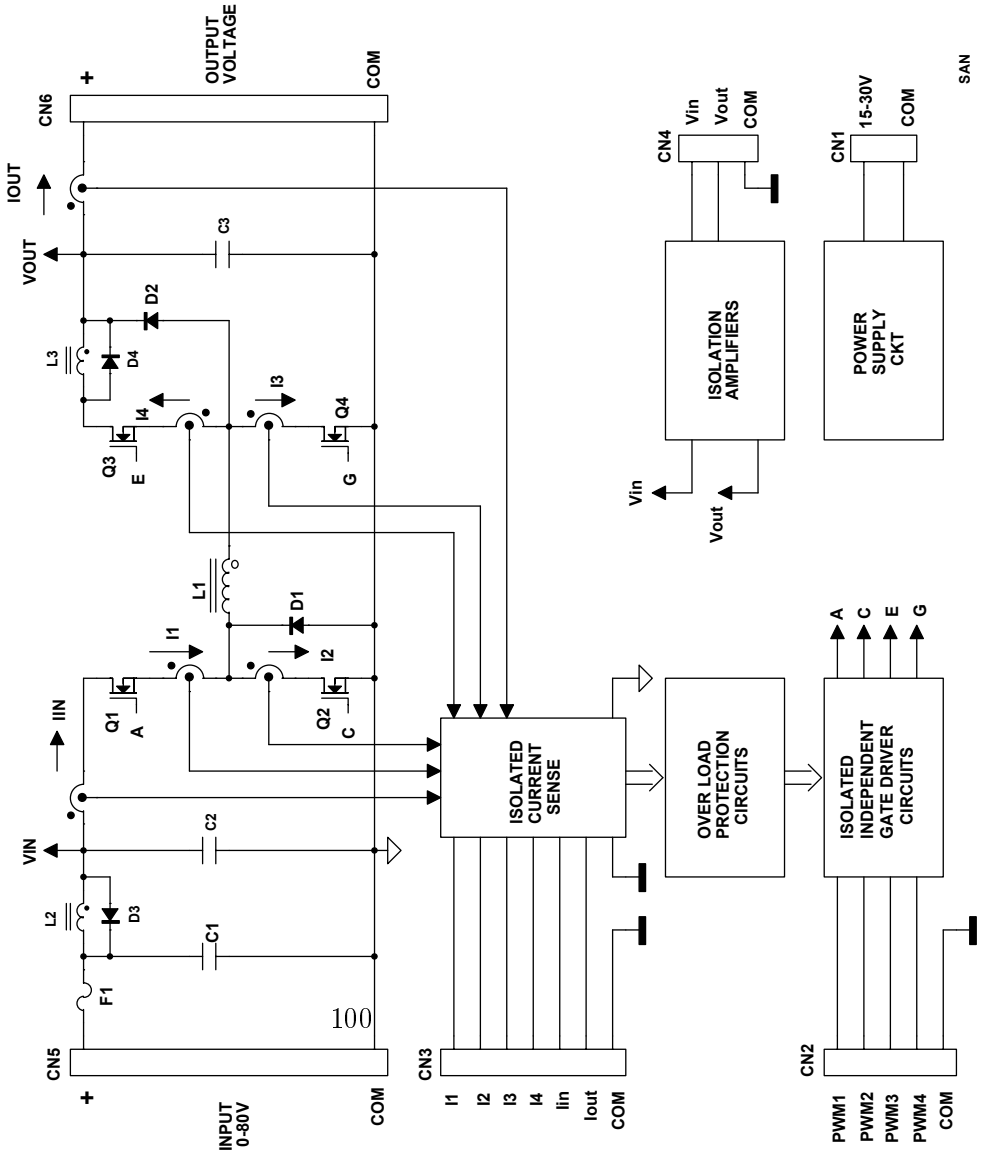
A Circuit diagram of the DC-DC converter design scheme

Supratim Basu

Buck Boost Converter Laboratory Module

The laboratory module described below can be configured as a Buck converter or a Boost Converter or a Buck-Boost Converter. The proposed design scheme has the following features.

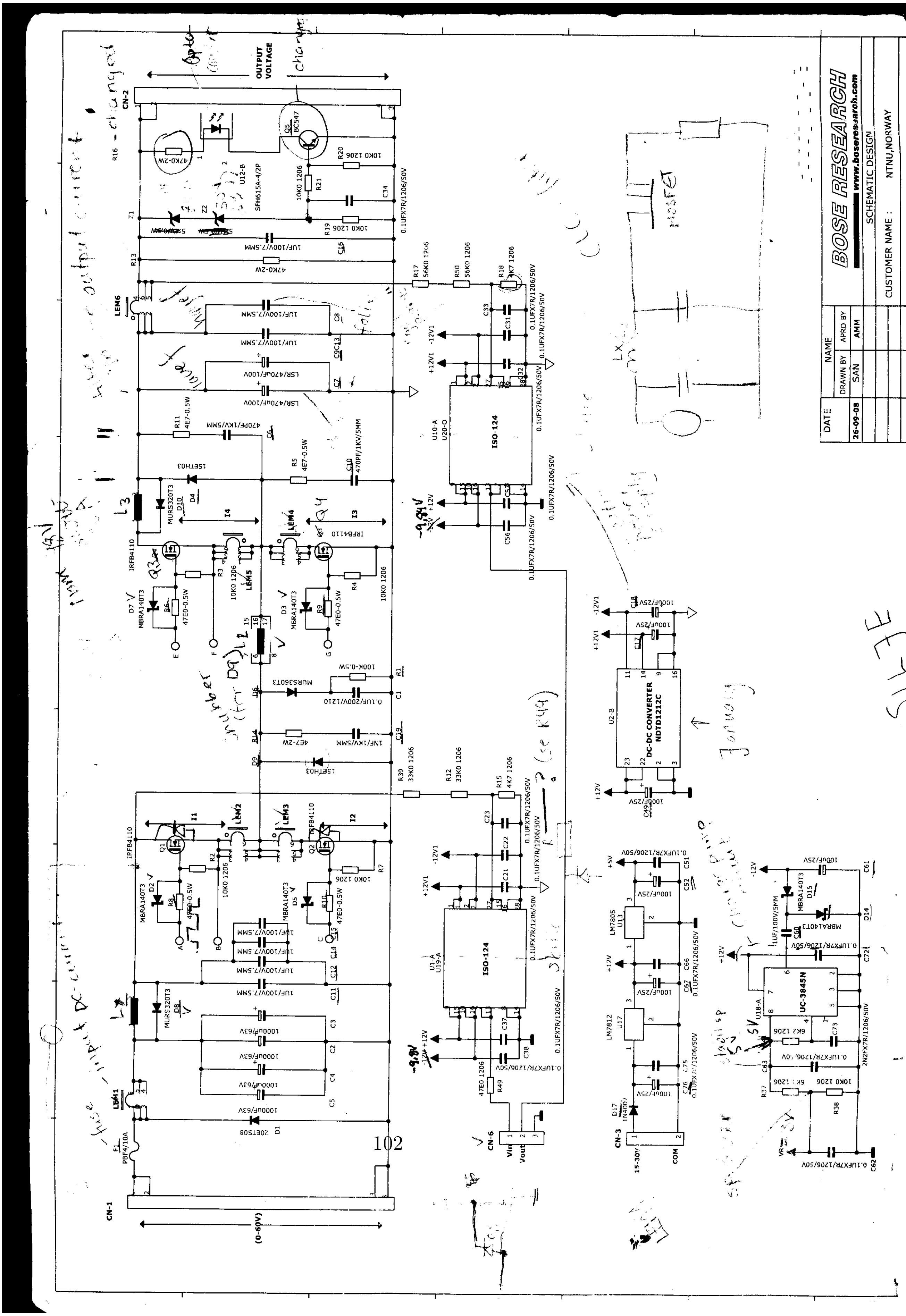
- Independent and Isolated control of four Mosfet switches.
- Independent and Isolated current sense of all four Mosfet switches and measurements of input and output DC current.
- Independent current limit protection of each of the four Mosfet switches.
- Independent and Isolated voltage sense of input and output DC voltage.
- A single 15-30 V dc supply powers all circuits.
- All components can be purchased from Farnell.

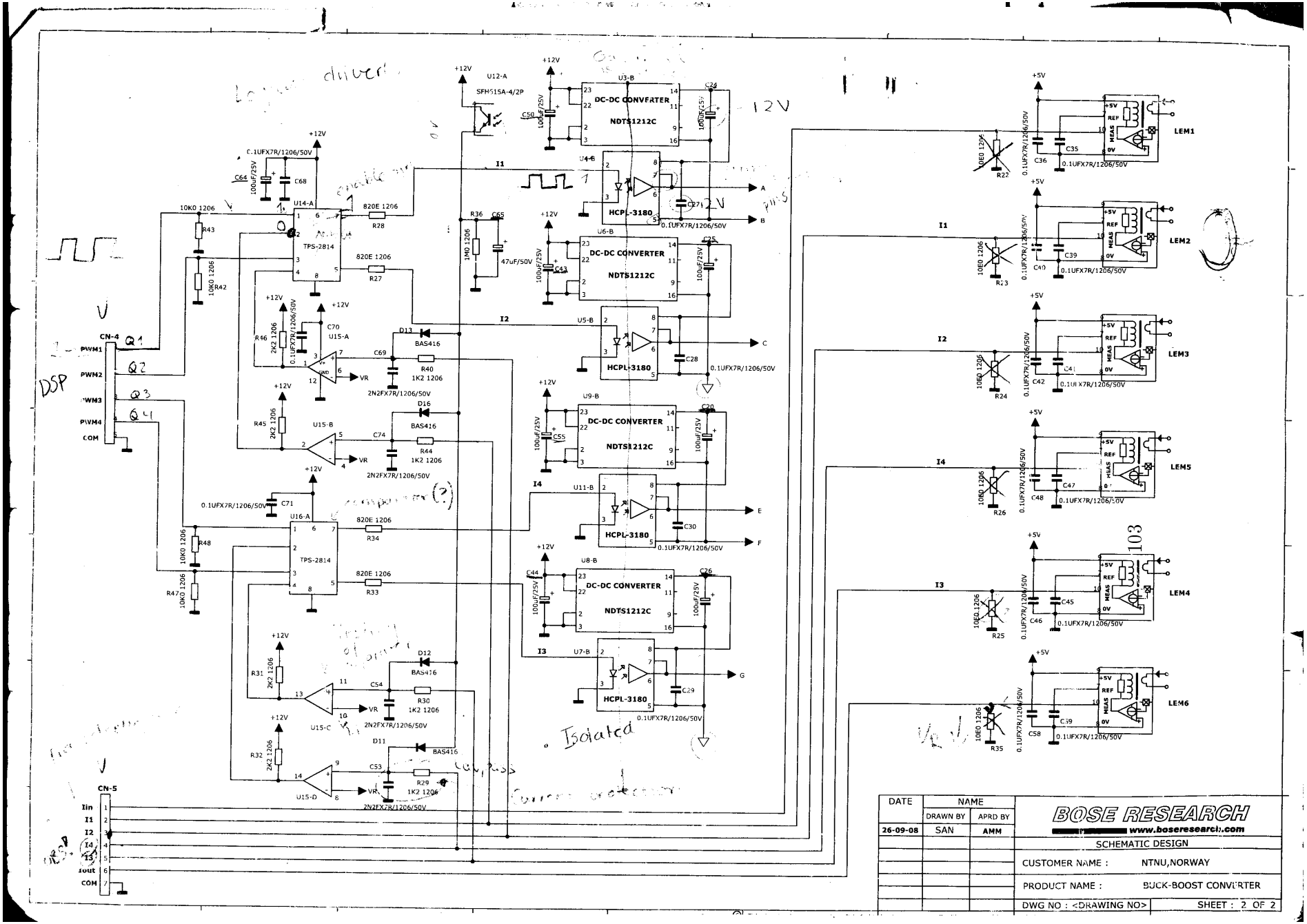


The design scheme is explained in detail with reference to the block schematics given above. Input dc from the solar panel is connected at CN5. All the four Mosfets Q1/Q2/Q3/Q4 are independently controlled from TTL level PWM signals at CN2 by isolated driver circuits. Independent and isolated current sense of all four Mosfet switches and measurements of input and output DC current, are done by LEM sensors. The measured isolated current signals are connected at CN3.This measured current sense signal is also used to provide independent current limit protection of each of the four Mosfet switches. Independent and isolated voltage sense of input and output DC voltage are provided by isolation amplifiers and are connected at CN4. A single external 15-30 V dc supply at CN1 powers all control circuits.

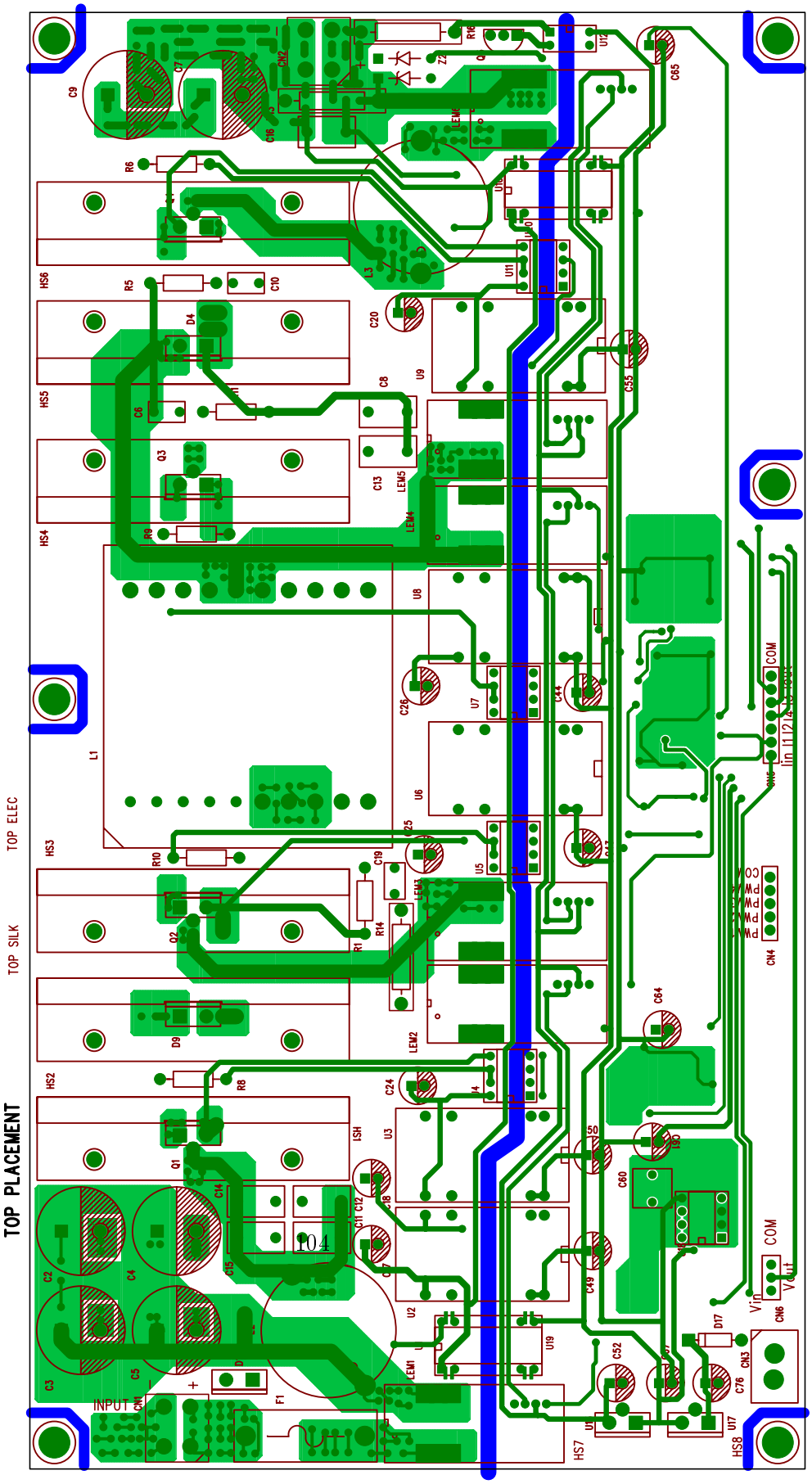
By configuring all the four Mosfets independently, the power circuit can be configured as a Buck converter or a Boost Converter or a Buck-Boost Converter. Q1/Q2/L1/C3 configures as a buck converter while L1/Q4/D2/Q3 configures as a boost converter. During overload conditions, L2/D3 and L3/D4 provides di/dt limiting of Q1/Q3 respectively. The stepped up or stepped down voltage is connected at CN6.

The complete detailed schematic design is given in the next two pages.

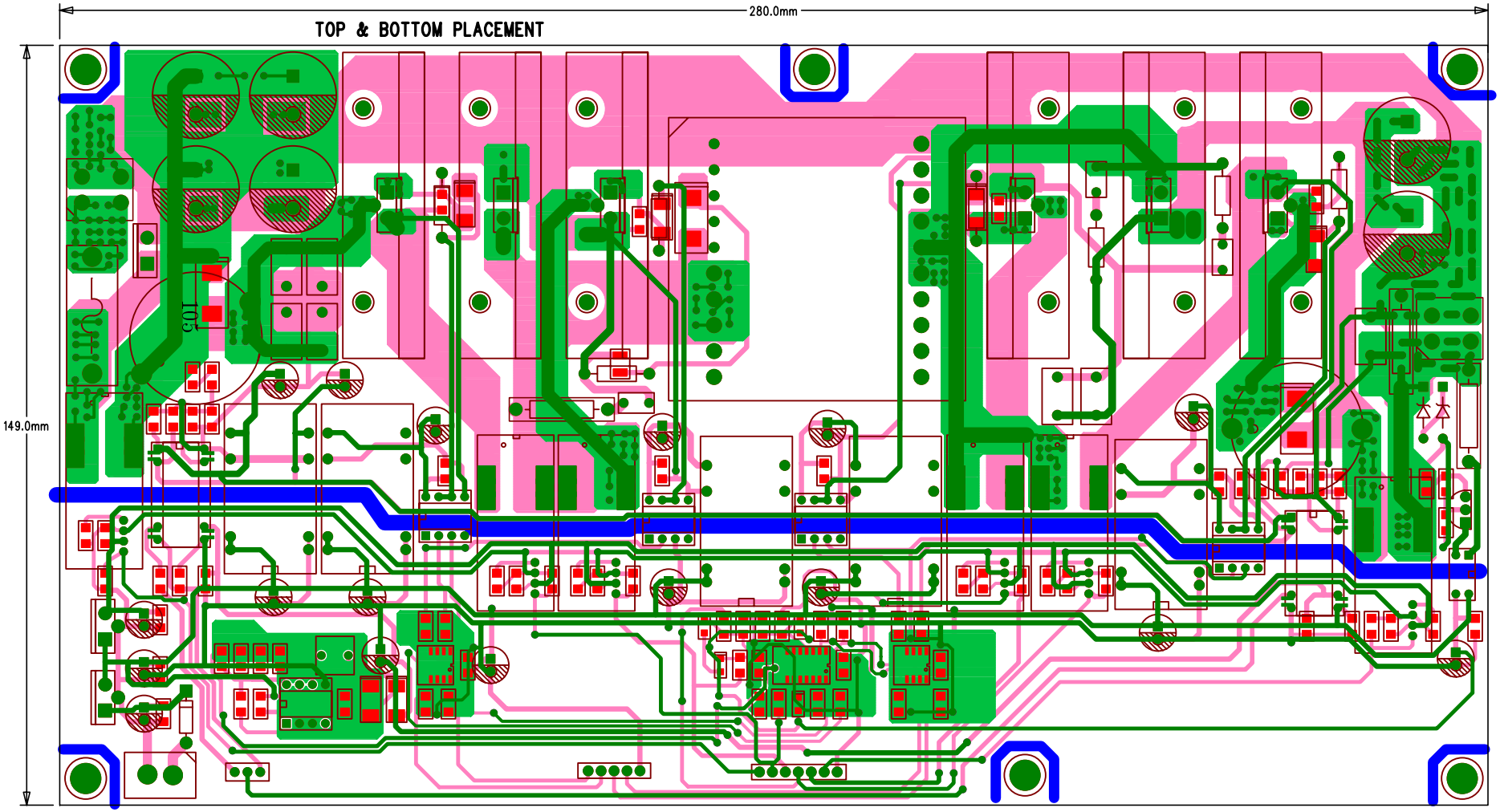

BOSE RESEARCH
www.boseresearch.com
SCHEMATIC DESIGN
CUSTOMER NAME :
NTNU,NORWAY
DATE
26-09-08
NAME
DRAWN BY
SAN
APRD BY
AMM
OUTPUT VOLTAGE
CN-2
CN-1
(0-60V)
ISO-124
DC-DC CONVERTER
NDTD1212C
UC-3845N
LM7805
LM7812
CN-3
CN-6


CN-4
PWM1
PWM2
PWM3
PWM4
COM
CN-5
Iin
I1
I2
I4
I3
Iout
COM
TPS-2814
U14-A
U15-A
U15-B
U15-C
U15-D
U16-A
SFH615A-4/2P
U12-A
DC-DC CONVERTER
NDTS1212C
HCPL-3180
U3-B
U4-B
U5-B
U6-B
U7-B
U8-B
U9-B
U11-B
LEM1
LEM2
LEM3
LEM4
LEM5
LEM6
BOSE RESEARCH
www.boseresearch.com
SCHEMATIC DESIGN
CUSTOMER NAME : NTNU,NORWAY
PRODUCT NAME : BUCK-BOOST CONVERTER
DWG NO : <DRAWING NO>
SHEET : 2 OF 2
DATE
NAME
DRAWN BY
APRD BY
26-09-08
SAN
AMM

B Design of the PCB



BUCKBOOST_25SEP08_5.00P - Fri Sep 26 20:27:30 2008



Bill Of Materials for Buck Boost Converter

Ref	Description	Manufacturer Part No	Manufacturer	FARNELL ORDER CODE
C2	1000µF, ±20%, 63V,-55°C to +105°C, Type PM, Radial, Pitch 7.5mm	UPM1J102MHD	NICHICON	9452117
C3	1000µF, ±20%, 63V,-55°C to +105°C, Type PM, Radial, Pitch 7.5mm	UPM1J102MHD	NICHICON	9452117
C4	1000µF, ±20%, 63V,-55°C to +105°C, Type PM, Radial, Pitch 7.5mm	UPM1J102MHD	NICHICON	9452117
C5	1000µF, ±20%, 63V,-55°C to +105°C, Type PM, Radial, Pitch 7.5mm	UPM1J102MHD	NICHICON	9452117
C6	470pF, ±10%, 1kVDC,High voltage ceramic disc Capacitor, -25°C to +85°C	DEBB33A471KC1B	MURATA	9527125
C7	470µF, ±20%, 100V,-55°C to +105°C, Type PM, ESR =0.076E , Radial, Pitch 7.5mm	UPM2A471MHD	NICHICON	8812802
C8	1uF, ±20% ,100V , Stacked-film capacitor, 7.5mm Pitch	B32560J1105K	EPCOS	9752382
C9	470µF, ±20%, 100V,-55°C to +105°C, Type PM, ESR =0.076E , Radial, Pitch 7.5mm	UPM2A471MHD	NICHICON	8812802
C10	470pF, ±10%, 1kVDC,High voltage ceramic disc Capacitor, -25°C to +85°C	DEBB33A471KC1B	MURATA	9527125
C11	1uF, ±20% ,100V , Stacked-film capacitor, 7.5mm Pitch	B32560J1105K	EPCOS	9752382
C12	1uF, ±20% ,100V , Stacked-film capacitor, 7.5mm Pitch	B32560J1105K	EPCOS	9752382
C13	1uF, ±20% ,100V , Stacked-film capacitor, 7.5mm Pitch	B32560J1105K	EPCOS	9752382
C14	1uF, ±20% ,100V , Stacked-film capacitor, 7.5mm Pitch	B32560J1105K	EPCOS	9752382
C15	1uF, ±20% ,100V , Stacked-film capacitor, 7.5mm Pitch	B32560J1105K	EPCOS	9752382
C16	1uF, ±20% ,100V , Stacked-film capacitor, 7.5mm Pitch	B32560J1105K	EPCOS	9752382
C17	100µF, ±20%, 25V,-55°C to +105°C, Type PM, Radial, Pitch 2.5mm	UPM1E101MED	NICHICON	8812462
C18	100µF, ±20%, 25V,-55°C to +105°C, Type VZ, Radial, Pitch 2.5mm	UVZ1E101MED	NICHICON	8812462
C19	1nF, ±10%, 1kVDC, High voltage ceramic disc Capacitor,-25°C to +85°C	DEBE33A102ZC1B	MURATA	9527184

C20	100µF, ±20%, 25V,-55°C to +105°C, Type PM, Radial, Pitch 2.5mm	UPM1E101MED	NICHICON	8812462
C24	100µF, ±20%, 25V,-55°C to +105°C, Type PM, Radial, Pitch 2.5mm	UPM1E101MED	NICHICON	8812462
C25	100µF, ±20%, 25V,-55°C to +105°C, Type PM, Radial, Pitch 2.5mm	UPM1E101MED	NICHICON	8812462
C26	100µF, ±20%, 25V,-55°C to +105°C, Type PM, Radial, Pitch 2.5mm	UPM1E101MED	NICHICON	8812462
C43	100µF, ±20%, 25V,-55°C to +105°C, Type PM, Radial, Pitch 2.5mm	UPM1E101MED	NICHICON	8812462
C44	100µF, ±20%, 25V,-55°C to +105°C, Type PM, Radial, Pitch 2.5mm	UPM1E101MED	NICHICON	8812462
C49	100µF, ±20%, 25V,-55°C to +105°C, Type PM, Radial, Pitch 2.5mm	UPM1E101MED	NICHICON	8812462
C50	100µF, ±20%, 25V,-55°C to +105°C, Type PM, Radial, Pitch 2.5mm	UPM1E101MED	NICHICON	8812462
C52	100µF, ±20%, 25V,-55°C to +105°C, Type PM, Radial, Pitch 2.5mm	UPM1E101MED	NICHICON	8812462
C55	100µF, ±20%, 25V,-55°C to +105°C, Type PM, Radial, Pitch 2.5mm	UPM1E101MED	NICHICON	8812462
C60	1uF, ±20% ,100V , Stacked-film capacitor, 7.5mm Pitch	B32560J1105K	EPCOS	9752382
C61	100µF, ±20%, 25V,-55°C to +105°C, Type PM, Radial, Pitch 2.5mm	UPM1E101MED	NICHICON	8812462
C64	100µF, ±20%, 25V,-55°C to +105°C, Type PM, Radial, Pitch 2.5mm	UPM1E101MED	NICHICON	8812462
C65	47µF, ±20%, 50V, -55°C to +105°C, Type PS, Radial, Pitch 2.5mm	UPS1H470MED	NICHICON	8813035
C67	100µF, ±20%, 25V,-55°C to +105°C, Type PM, Radial, Pitch 2.5mm	UPM1E101MED	NICHICON	8812462
C76	100µF, ±20%, 25V,-55°C to +105°C, Type VZ, Radial, Pitch 2.5mm	UPM1E101MED	NICHICON	8812462
CN1	Spring terminal block	FFKDS/V-2.54	PHOENIX	304-1062
CN2	Spring terminal block	FFKDS/V-2.54	PHOENIX	304-1062
CN3	2PIN HEADER		MOLEX	973-1393
CN4	5 PIN HEADER-STRAIGHT		HARWIN	102-2253
CN5	8 PIN HEADER-STRAIGHT		HARWIN	102-2257
CN6	3 PIN HEADER-STRAIGHT		HARWIN	102-2249
D1	If(av) =20A,V(rrm) =800V, Rectifier Diode,TO-220AC package –	20ETS08 –	I.R –	1351324
D2	If(av) = 1A,Vrrm = 40V, schottky Power Rectifier, SMA Package –	MBRA140T3G –	ON SEMICONDUCTOR –	9555986 1155679

D3	If(av) = 1A,Vrrm = 40V, schottky Power Rectifier, SMA Package	MBRA140T3G	ON SEMICONDUCTOR	9555986
	–	–	–	1155679
D4	If(av) =15A,V(rrm) =300V, Ultra fast rectifier,TO-220AC package	15ETH03SPbF	INTERNATIONAL RECTIFIER	8656940
	–	–	–	1351275
D5	If(av) = 1A,Vrrm = 40V, schottky Power Rectifier, SMA Package	MBRA140T3G	ON SEMICONDUCTOR	9555986
	–	–	–	1155679
D6	If(av) = 3A,Vrrm = 600V, Ultrafast Rectifier, SMC Package	MURS360T3G	ON SEMICONDUCTOR	1459153
	–	–	–	
D7	If(av) = 1A,Vrrm = 40V, schottky Power Rectifier, SMA Package	MBRA140T3G	ON SEMICONDUCTOR	9555986
	–	–	–	1155679
D8	If(av) = 3A,Vrrm = 200V, Ultrafast Rectifier, SMC Package	MURS320T3G	ON SEMICONDUCTOR	9557555
	–	–	–	
D9	If(av) =15A,V(rrm) =300V, Ultra fast rectifier,TO-220AC package	15ETH03SPbF	INTERNATIONAL RECTIFIER	8656940
	–	–	–	1351275
D10	If(av) = 3A,Vrrm = 200V, Ultrafast Rectifier, SMC Package	MURS320T3G	ON SEMICONDUCTOR	9557555
	–	–	–	
D11	If = 200mA, Vrrm = 85V, Dual Switching Diode,SOD-323 Package	BAS416	NXP	8734399
	–	–	–	
	–	–	–	
D12	If = 200mA, Vrrm = 85V, Dual Switching Diode,SOD-323 Package	BAS416	NXP	8734399
	–	–	–	
	–	–	–	
D13	If = 200mA, Vrrm = 85V, Dual Switching Diode,SOD-323 Package	BAS416	NXP	8734399
	–	–	–	
	–	–	–	
D14	If(av) = 1A,Vrrm = 40V, schottky Power Rectifier, SMA Package	MBRA140T3G	ON SEMICONDUCTOR	9555986
	–	–	–	1155679
D15	If(av) = 1A,Vrrm = 40V, schottky Power Rectifier, SMA Package	MBRA140T3G	ON SEMICONDUCTOR	9555986
	–	–	–	1155679
D16	If = 200mA, Vrrm = 85V, Dual Switching Diode,SOD-323 Package	BAS416	NXP	8734399
D17	If(av) = 1A, V(rrm) = 1000V, Package, DO-41 Package	1N4007	ON SEMICONDUCTOR	1467514
F1	11.4 X 9.4 X 24.4mm FUSE HOLDER	4628	KEYSTONE	116-2740
	11.4 X 9.4 X 24.4mm FUSE COVER	4628C	KEYSTONE	117-6774
	10A/250V AC Miniature Fuse 5 X 20mm	0001.2714.11	SCHURTER	444-8420
HS1	SCREW MOUNTABLE HEATSINK	1.25 GY-50	AAVID	175-009
HS2	SCREW MOUNTABLE HEATSINK	1.25 GY-50	AAVID	175-009
HS3	SCREW MOUNTABLE HEATSINK	1.25 GY-50	AAVID	175-009
HS4	SCREW MOUNTABLE HEATSINK	1.25 GY-50	AAVID	175-009

HS5	SCREW MOUNTABLE HEATSINK	1.25 GY-50	AAVID	175-009
HS5	SCREW MOUNTABLE HEATSINK	1.25 GY-50	AAVID	175-009
HS6	SCREW MOUNTABLE HEATSINK	1.25 GY-50	AAVID	175-009
HS7	SCREW MOUNTABLE HEATSINK	SK 95/25SA220	FISCHER	462-1544
HS8	SCREW MOUNTABLE HEATSINK	SK 95/25SA220	FISCHER	462-1544
L1	ETD 49/25/16,Ferrite Core,Ungapped,N87 Grade,AL=3800 +30/-20% ETD-49,20 Pin Horizontal coil former, ETD49/25/16 YOKE, Stainless spring steel (0.4 mm)	ETD 49/25/16-3C90 CPH-ETD49-1S-20P CLI-ETD49	FERROX CUBE FERROX CUBE FERROX CUBE	305-6417 305-6338 105-778
L2	HIGH CURRENT INDUCTOR 1400SERIES	1422311C	C&D TECHNOLOGIES	107-7056
L3	HIGH CURRENT INDUCTOR 1400SERIES	1422311C	C&D TECHNOLOGIES	107-7056
LEM1	CURRENT TRANSDUCER	LAS 50-TP/SP1	LEM	1617418
LEM2	CURRENT TRANSDUCER	LAS 50-TP/SP1	LEM	1617418
LEM3	CURRENT TRANSDUCER	LAS 50-TP/SP1	LEM	1617418
LEM4	CURRENT TRANSDUCER	LAS 50-TP/SP1	LEM	1617418
LEM5	CURRENT TRANSDUCER	LAS 50-TP/SP1	LEM	1617418
LEM6	CURRENT TRANSDUCER	LAS 50-TP/SP1	LEM	1617418
Q1	Vdss=100V,Id=180A, Rds-on=3.7mE,N-Channel Mosfet,TO-220AB Package, Pb-free. –	IRFB4110PbF –	INTERNATIONAL RECTIFIER –	1436955
Q2	Vdss=100V,Id=180A, Rds-on=3.7mE,N-Channel Mosfet,TO-220AB Package, Pb-free. –	IRFB4110PbF –	INTERNATIONAL RECTIFIER –	1436955
Q3	Vdss=100V,Id=180A, Rds-on=3.7mE,N-Channel Mosfet,TO-220AB Package, Pb-free. –	IRFB4110PbF –	INTERNATIONAL RECTIFIER –	1436955
Q4	Vdss=100V,Id=180A, Rds-on=3.7mE,N-Channel Mosfet,TO-220AB Package, Pb-free. –	IRFB4110PbF –	INTERNATIONAL RECTIFIER –	1436955
Q5	Vceo=250V,Ic=30mA,TO-92 Package,NPN Transistor –	BF422ZL1G –	ON SEMICONDUCTOR –	955-6400
R1	100K, ±5%, 0.5W, MFR	SFR160000-1004-JA100	PHOENIX PASSIVE	9475559
R5	4E7, ±1%, 0.5W, MFR	SFR16S-47R-5	PHOENIX PASSIVE	9476075

R6	47E0, ±1%, 0.5W, MFR	SFR16S-47R-5	PHOENIX PASSIVE	9476075
R8	47E0, ±1%, 0.5W, MFR	SFR16S-47R-5	VISHAYBC COMPONENTS	9476075
R9	47E0, ±1%, 0.5W, MFR	SFR16S-47R-5	VISHAYBC COMPONENTS	9476075
R10	47E0, ±1%, 0.5W, MFR	SFR16S-47R-5	VISHAYBC COMPONENTS	9476075
R11	4E7, ±1%, 0.5W, MFR	SFR16S-4R7-5	VISHAYBC COMPONENTS	9476091
R13	47K0, ±5%, 2W, MFR	2306 198 53473	VISHAY BC COMPONENTS	550280
R14	4E7, ±5%, 2W, MFR	MFP2-4R7 JI	WELWYN	1565476
R16	47K0, ±5%, 2W, MFR	2306 198 53473	VISHAY BC COMPONENTS	550280
U1	Precision Low cost Isolation Amplifier ,SOIC	ISO-124	TI	1212426
U19	Precision Low cost Isolation Amplifier	ISO-124	TI	1212426
U2	Isolated 3W Dual Output DC/DC Converters –40°C to +85°C	NDTD1212C	C&D TECHNOLOGIES	129-3599
U3	Isolated 3W Single Output DC/DC Converters –40°C to +85°C	NDTS1212C	C&D TECHNOLOGIES	129-3580
U4	2.5 Amp Output Current, High Speed, Gate Drive Optocoupler	HCPL-3180-000E	AVAGO TECHNOLOGIES	9130179
U5	2.5 Amp Output Current, High Speed, Gate Drive Optocoupler	HCPL-3180-000E	AVAGO TECHNOLOGIES	9130179
U6	Isolated 3W Single Output DC/DC Converters –40°C to +85°C	NDTS1212C	C&D TECHNOLOGIES	129-3580
U7	2.5 Amp Output Current, High Speed, Gate Drive Optocoupler	HCPL-3180-000E	AVAGO TECHNOLOGIES	9130179
U8	Isolated 3W Single Output DC/DC Converters –40°C to +85°C	NDTS1212C	C&D TECHNOLOGIES	129-3580
U9	Isolated 3W Single Output DC/DC Converters –40°C to +85°C	NDTS1212C	C&D TECHNOLOGIES	129-3580
U10	Precision Low cost Isolation Amplifier, SOIC package	ISO-124	TI	1212426
U20	Precision Low cost Isolation Amplifier	ISO-124	TI	1212426
U11	2.5 Amp Output Current, High Speed, Gate Drive Optocoupler	HCPL-3180-000E	AVAGO TECHNOLOGIES	9130179
U12	4 Pin Type Optocoupler,CTR 80% to 160%, DIP4 Package,-55°C to 100°C	PC817X1J000F	SHARP	970-7697
U13	100mA , 5V 3-Terminal Fixed Positive Voltage regulator, TO-220Package, 0°C to 125°C	LM7805	NATIONAL SEMICONDUCTOR	1467364

U14	DUAL HIGH-SPEED MOSFET DRIVERS, SO8 package	TPS2814	TI	9854401
U15	Quad Comparator,SO-14 Package, 0°C to 70°C	LM339M	NATIONAL SEMIONDUCTOR	9487654 1468955
U16	DUAL HIGH-SPEED MOSFET DRIVERS	TPS2814	TI	9854401
U17	100mA , 12V 3-Terminal Fixed Positive Voltage regulator, TO-220Package, 0°C to 125°C	LM7812	NATIONAL SEMICONDUCTOR	1467365
U18	Current Mode PWM Controller,PDIP-8 Package, 0°C to 70°C	UC3845N	ST UNITRODE	9882928 1101214
Z1	47V,0.5W,Zenerdiode,DO-35 package	1N5370BG	ON SEMI	9558276
Z2	47V,0.5W,Zenerdiode,DO-35 package	1N5370BG	ON SEMI	9558276

FOLLOWING COMPONENTS OR EQUIVALENT ALTERNATIVES CAN BE USED

C1	0.1µF, ±10%, 200V, X7R, -55°C to +125°C, Case Size 1210	12102C104MAT2A	AVX
C21	0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	EPCOS
	0.1µF, ±10%, 50V, X7R, Case Size1206	VJ1206Y104KXAAT##	VISHAY VITRAMON
	0.1µF, ±10%, 50V, X7R, Case Size1206	12065C104KAT2A	AVX
C22	0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	EPCOS
	0.1µF, ±10%, 50V, X7R, Case Size1206	VJ1206Y104KXAAT##	VISHAY VITRAMON
	0.1µF, ±10%, 50V, X7R, Case Size1206	12065C104KAT2A	AVX
C23	0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	EPCOS
	0.1µF, ±10%, 50V, X7R, Case Size1206	VJ1206Y104KXAAT##	VISHAY VITRAMON
	0.1µF, ±10%, 50V, X7R, Case Size1206	12065C104KAT2A	AVX
C27	0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	EPCOS
	0.1µF, ±10%, 50V, X7R, Case Size1206	VJ1206Y104KXAAT##	VISHAY VITRAMON
	0.1µF, ±10%, 50V, X7R, Case Size1206	12065C104KAT2A	AVX
C28	0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	EPCOS
	0.1µF, ±10%, 50V, X7R, Case Size1206	VJ1206Y104KXAAT##	VISHAY VITRAMON
	0.1µF, ±10%, 50V, X7R, Case Size1206	12065C104KAT2A	AVX
C29	0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	EPCOS
	0.1µF, ±10%, 50V, X7R, Case Size1206	VJ1206Y104KXAAT##	VISHAY VITRAMON
	0.1µF, ±10%, 50V, X7R, Case Size1206	12065C104KAT2A	AVX
C30	0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	EPCOS
	0.1µF, ±10%, 50V, X7R, Case Size1206	VJ1206Y104KXAAT##	VISHAY VITRAMON
	0.1µF, ±10%, 50V, X7R, Case Size1206	12065C104KAT2A	AVX
C31	0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	EPCOS
	0.1µF, ±10%, 50V, X7R, Case Size1206	VJ1206Y104KXAAT##	VISHAY VITRAMON
	0.1µF, ±10%, 50V, X7R, Case Size1206	12065C104KAT2A	AVX
C32	0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	EPCOS
	0.1µF, ±10%, 50V, X7R, Case Size1206	VJ1206Y104KXAAT##	VISHAY VITRAMON
	0.1µF, ±10%, 50V, X7R, Case Size1206	12065C104KAT2A	AVX
C33	0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	EPCOS
	0.1µF, ±10%, 50V, X7R, Case Size1206	VJ1206Y104KXAAT##	VISHAY VITRAMON
	0.1µF, ±10%, 50V, X7R, Case Size1206	12065C104KAT2A	AVX
C34	0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	EPCOS
	0.1µF, ±10%, 50V, X7R, Case Size1206	VJ1206Y104KXAAT##	VISHAY VITRAMON
	0.1µF, ±10%, 50V, X7R, Case Size1206	12065C104KAT2A	AVX
C35	0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	EPCOS

	0.1µF, ±10%, 50V, X7R, Case Size1206	VJ1206Y104KXAAT##	VISHAY VITRAMON
	0.1µF, ±10%, 50V, X7R, Case Size1206	12065C104KAT2A	AVX
C36	0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	EPCOS
	0.1µF, ±10%, 50V, X7R, Case Size1206	VJ1206Y104KXAAT##	VISHAY VITRAMON
	0.1µF, ±10%, 50V, X7R, Case Size1206	12065C104KAT2A	AVX
C37	0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	EPCOS
	0.1µF, ±10%, 50V, X7R, Case Size1206	VJ1206Y104KXAAT##	VISHAY VITRAMON
	0.1µF, ±10%, 50V, X7R, Case Size1206	12065C104KAT2A	AVX
C38	0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	EPCOS
	0.1µF, ±10%, 50V, X7R, Case Size1206	VJ1206Y104KXAAT##	VISHAY VITRAMON
	0.1µF, ±10%, 50V, X7R, Case Size1206	12065C104KAT2A	AVX
C39	0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	EPCOS
	0.1µF, ±10%, 50V, X7R, Case Size1206	VJ1206Y104KXAAT##	VISHAY VITRAMON
	0.1µF, ±10%, 50V, X7R, Case Size1206	12065C104KAT2A	AVX
C40	0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	EPCOS
	0.1µF, ±10%, 50V, X7R, Case Size1206	VJ1206Y104KXAAT##	VISHAY VITRAMON
	0.1µF, ±10%, 50V, X7R, Case Size1206	12065C104KAT2A	AVX
C41	0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	EPCOS
	0.1µF, ±10%, 50V, X7R, Case Size1206	VJ1206Y104KXAAT##	VISHAY VITRAMON
	0.1µF, ±10%, 50V, X7R, Case Size1206	12065C104KAT2A	AVX
C42	0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	EPCOS
	0.1µF, ±10%, 50V, X7R, Case Size1206	VJ1206Y104KXAAT##	VISHAY VITRAMON
	0.1µF, ±10%, 50V, X7R, Case Size1206	12065C104KAT2A	AVX
C45	0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	EPCOS
	0.1µF, ±10%, 50V, X7R, Case Size1206	VJ1206Y104KXAAT##	VISHAY VITRAMON
	0.1µF, ±10%, 50V, X7R, Case Size1206	12065C104KAT2A	AVX
C46	0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	EPCOS
	0.1µF, ±10%, 50V, X7R, Case Size1206	VJ1206Y104KXAAT##	VISHAY VITRAMON
	0.1µF, ±10%, 50V, X7R, Case Size1206	12065C104KAT2A	AVX
C47	0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	EPCOS
	0.1µF, ±10%, 50V, X7R, Case Size1206	VJ1206Y104KXAAT##	VISHAY VITRAMON
	0.1µF, ±10%, 50V, X7R, Case Size1206	12065C104KAT2A	AVX
C48	0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	EPCOS
	0.1µF, ±10%, 50V, X7R, Case Size1206	VJ1206Y104KXAAT##	VISHAY VITRAMON
	0.1µF, ±10%, 50V, X7R, Case Size1206	12065C104KAT2A	AVX
C51	0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	EPCOS
	0.1µF, ±10%, 50V, X7R, Case Size1206	VJ1206Y104KXAAT##	VISHAY VITRAMON
	0.1µF, ±10%, 50V, X7R, Case Size1206	12065C104KAT2A	AVX
C53	2n2F, ±10%, 50V, X7R, Case Size1206	B37872K5222K0**	EPCOS
	2n2F, ±10%, 50V, X7R, Case Size1206	VJ1206Y222KXAAT	VISHAY VITRAMON
	2n2F, ±10%, 50V, X7R, Case Size1206	12065C222KAT2A	AVX
C54	2n2F, ±10%, 50V, X7R, Case Size1206	B37872K5222K0**	EPCOS
	2n2F, ±10%, 50V, X7R, Case Size1206	VJ1206Y222KXAAT	VISHAY VITRAMON
	2n2F, ±10%, 50V, X7R, Case Size1206	12065C222KAT2A	AVX
C56	0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	EPCOS
	0.1µF, ±10%, 50V, X7R, Case Size1206	VJ1206Y104KXAAT##	VISHAY VITRAMON
	0.1µF, ±10%, 50V, X7R, Case Size1206	12065C104KAT2A	AVX
C57	0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	EPCOS
	0.1µF, ±10%, 50V, X7R, Case Size1206	VJ1206Y104KXAAT##	VISHAY VITRAMON
	0.1µF, ±10%, 50V, X7R, Case Size1206	12065C104KAT2A	AVX
C58	0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	EPCOS
	0.1µF, ±10%, 50V, X7R, Case Size1206	VJ1206Y104KXAAT##	VISHAY VITRAMON
	0.1µF, ±10%, 50V, X7R, Case Size1206	12065C104KAT2A	AVX
C59	0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	EPCOS
	0.1µF, ±10%, 50V, X7R, Case Size1206	VJ1206Y104KXAAT##	VISHAY VITRAMON
	0.1µF, ±10%, 50V, X7R, Case Size1206	12065C104KAT2A	AVX

C62	0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	EPCOS
	0.1µF, ±10%, 50V, X7R, Case Size1206	VJ1206Y104KXAAT##	VISHAY VITRAMON
	0.1µF, ±10%, 50V, X7R, Case Size1206	12065C104KAT2A	AVX
C63	0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	EPCOS
	0.1µF, ±10%, 50V, X7R, Case Size1206	VJ1206Y104KXAAT##	VISHAY VITRAMON
	0.1µF, ±10%, 50V, X7R, Case Size1206	12065C104KAT2A	AVX
C66	0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	EPCOS
	0.1µF, ±10%, 50V, X7R, Case Size1206	VJ1206Y104KXAAT##	VISHAY VITRAMON
	0.1µF, ±10%, 50V, X7R, Case Size1206	12065C104KAT2A	AVX
C68	0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	EPCOS
	0.1µF, ±10%, 50V, X7R, Case Size1206	VJ1206Y104KXAAT##	VISHAY VITRAMON
	0.1µF, ±10%, 50V, X7R, Case Size1206	12065C104KAT2A	AVX
C69	2n2F, ±10%, 50V, X7R, Case Size1206	B37872K5222K0**	EPCOS
	2n2F, ±10%, 50V, X7R, Case Size1206	VJ1206Y222KXAAT	VISHAY VITRAMON
	2n2F, ±10%, 50V, X7R, Case Size1206	12065C222KAT2A	AVX
C70	0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	EPCOS
	0.1µF, ±10%, 50V, X7R, Case Size1206	VJ1206Y104KXAAT##	VISHAY VITRAMON
	0.1µF, ±10%, 50V, X7R, Case Size1206	12065C104KAT2A	AVX
C71	0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	EPCOS
	0.1µF, ±10%, 50V, X7R, Case Size1206	VJ1206Y104KXAAT##	VISHAY VITRAMON
	0.1µF, ±10%, 50V, X7R, Case Size1206	12065C104KAT2A	AVX
C72	0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	EPCOS
	0.1µF, ±10%, 50V, X7R, Case Size1206	VJ1206Y104KXAAT##	VISHAY VITRAMON
	0.1µF, ±10%, 50V, X7R, Case Size1206	12065C104KAT2A	AVX
C73	2n2F, ±10%, 50V, X7R, Case Size1206	B37872K5222K0**	EPCOS
	2n2F, ±10%, 50V, X7R, Case Size1206	VJ1206Y222KXAAT	VISHAY VITRAMON
	2n2F, ±10%, 50V, X7R, Case Size1206	12065C222KAT2A	AVX
C74	2n2F, ±10%, 50V, X7R, Case Size1206	B37872K5222K0**	EPCOS
	2n2F, ±10%, 50V, X7R, Case Size1206	VJ1206Y222KXAAT	VISHAY VITRAMON
	2n2F, ±10%, 50V, X7R, Case Size1206	12065C222KAT2A	AVX
C75	0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	EPCOS
	0.1µF, ±10%, 50V, X7R, Case Size1206	VJ1206Y104KXAAT##	VISHAY VITRAMON
	0.1µF, ±10%, 50V, X7R, Case Size1206	12065C104KAT2A	AVX
R2	10K0, ±1%, 0.25W, Case Size 1206	CR1206-FX-1002ELF	BOURNS
	10K0, ±1%, 0.25W, Case Size 1206	MCR18-EZP-F-1002	ROHM
	10K0, ±1%, 0.25W, Case Size 1206	RCA1206-10K0-FK-EA00	VISHAY
R3	10K0, ±1%, 0.25W, Case Size 1206	CR1206-FX-1002ELF	BOURNS
	10K0, ±1%, 0.25W, Case Size 1206	MCR18-EZP-F-1002	ROHM
	10K0, ±1%, 0.25W, Case Size 1206	RCA1206-10K0-FK-EA00	VISHAY
R4	10K0, ±1%, 0.25W, Case Size 1206	CR1206-FX-1002ELF	BOURNS
	10K0, ±1%, 0.25W, Case Size 1206	MCR18-EZP-F-1002	ROHM
	10K0, ±1%, 0.25W, Case Size 1206	RCA1206-10K0-FK-EA00	VISHAY
R7	10K0, ±1%, 0.25W, Case Size 1206	CR1206-FX-1002ELF	BOURNS
	10K0, ±1%, 0.25W, Case Size 1206	MCR18-EZP-F-1002	ROHM
	10K0, ±1%, 0.25W, Case Size 1206	RCA1206-10K0-FK-EA00	VISHAY
R12	33K0, ±1%, 0.25W, Case Size 1206	CR1206-FX-3302ELF	BOURNS
	33K0, ±1%, 0.25W, Case Size 1206	MCR18-EZP-F-3302	ROHM
	33K0, ±1%, 0.25W, Case Size 1206	RCA1206-33K0-FK-EA00	VISHAY
R15	4K7, ±1%, 0.25W, Case Size 1206	CR1206-FX-4701ELF	BOURNS
	4K7, ±1%, 0.25W, Case Size 1206	MCR18-EZP-F-4701	ROHM
	4K7, ±1%, 0.25W, Case Size 1206	RCA1206-4K70-FK-EA00	VISHAY

R17	56K0, ±1%, 0.25W, Case Size 1206	CR1206-FX-5602ELF	BOURNS
	56K0, ±1%, 0.25W, Case Size 1206	MCR18-EZP-F-5602	ROHM
	56K0, ±1%, 0.25W, Case Size 1206	RCA1206-56K0-FK-EA00	VISHAY
R18	4K7, ±1%, 0.25W, Case Size 1206	CR1206-FX-4701ELF	BOURNS
	4K7, ±1%, 0.25W, Case Size 1206	MCR18-EZP-F-4701	ROHM
	4K7, ±1%, 0.25W, Case Size 1206	RCA1206-4K70-FK-EA00	VISHAY
R19	10K0, ±1%, 0.25W, Case Size 1206	CR1206-FX-1002ELF	BOURNS
	10K0, ±1%, 0.25W, Case Size 1206	MCR18-EZP-F-1002	ROHM
	10K0, ±1%, 0.25W, Case Size 1206	RCA1206-10K0-FK-EA00	VISHAY
R20	10K0, ±1%, 0.25W, Case Size 1206	CR1206-FX-1002ELF	BOURNS
	10K0, ±1%, 0.25W, Case Size 1206	MCR18-EZP-F-1002	ROHM
	10K0, ±1%, 0.25W, Case Size 1206	RCA1206-10K0-FK-EA00	VISHAY
R21	10K0, ±1%, 0.25W, Case Size 1206	CR1206-FX-1002ELF	BOURNS
	10K0, ±1%, 0.25W, Case Size 1206	MCR18-EZP-F-1002	ROHM
	10K0, ±1%, 0.25W, Case Size 1206	RCA1206-10K0-FK-EA00	VISHAY
R22	10E0, ±1%, 0.25W, Case Size 1206	CR1206-FX-10R0ELF	BOURNS
	10E0, ±1%, 0.25W, Case Size 1206	MCR18-EZP-F-10R0	ROHM
	10E0, ±5%, 0.25W, Case Size 1206	RCA1206-10R0-FK-EA00	VISHAY
R23	10E0, ±1%, 0.25W, Case Size 1206	CR1206-FX-10R0ELF	BOURNS
	10E0, ±1%, 0.25W, Case Size 1206	MCR18-EZP-F-10R0	ROHM
	10E0, ±5%, 0.25W, Case Size 1206	RCA1206-10R0-FK-EA00	VISHAY
R24	10E0, ±1%, 0.25W, Case Size 1206	CR1206-FX-10R0ELF	BOURNS
	10E0, ±1%, 0.25W, Case Size 1206	MCR18-EZP-F-10R0	ROHM
	10E0, ±5%, 0.25W, Case Size 1206	RCA1206-10R0-FK-EA00	VISHAY
R25	10E0, ±1%, 0.25W, Case Size 1206	CR1206-FX-10R0ELF	BOURNS
	10E0, ±1%, 0.25W, Case Size 1206	MCR18-EZP-F-10R0	ROHM
	10E0, ±5%, 0.25W, Case Size 1206	RCA1206-10R0-FK-EA00	VISHAY
R26	10E0, ±1%, 0.25W, Case Size 1206	CR1206-FX-10R0ELF	BOURNS
	10E0, ±1%, 0.25W, Case Size 1206	MCR18-EZP-F-10R0	ROHM
	10E0, ±5%, 0.25W, Case Size 1206	RCA1206-10R0-FK-EA00	VISHAY
R27	820E, ±1%, 0.25W, Case Size 1206	CR1206-FX-8200ELF	BOURNS
	820E, ±1%, 0.25W, Case Size 1206	MCR18-EZP-F-820R	ROHM
	820E, ±1%, 0.25W, Case Size 1206	RCA1206-820R-FK-EA00	VISHAY
R28	820E, ±1%, 0.25W, Case Size 1206	CR1206-FX-8200ELF	BOURNS
	820E, ±1%, 0.25W, Case Size 1206	MCR18-EZP-F-820R	ROHM
	820E, ±1%, 0.25W, Case Size 1206	RCA1206-820R-FK-EA00	VISHAY
R29	1K2, ±1%, 0.25W, Case Size 1206	CR1206-FX-1201ELF	BOURNS
	1K2, ±1%, 0.25W, Case Size 1206	MCR18-EZP-F-1201	ROHM
	1K2, ±1%, 0.25W, Case Size 1206	RCA1206-1K20-FK-EA00	VISHAY
R30	1K2, ±1%, 0.25W, Case Size 1206	CR1206-FX-1201ELF	BOURNS
	1K2, ±1%, 0.25W, Case Size 1206	MCR18-EZP-F-1201	ROHM
	1K2, ±1%, 0.25W, Case Size 1206	RCA1206-1K20-FK-EA00	VISHAY
R31	2K2, ±1%, 0.25W, Case Size 1206	CR1206-FX-2201ELF	BOURNS
	2K2, ±1%, 0.25W, Case Size 1206	MCR18-EZP-F-2201	ROHM
	2K2, ±1%, 0.25W, Case Size 1206	RCA1206-2K20-FK-EA00	VISHAY
R32	2K2, ±1%, 0.25W, Case Size 1206	CR1206-FX-2201ELF	BOURNS
	2K2, ±1%, 0.25W, Case Size 1206	MCR18-EZP-F-2201	ROHM
	2K2, ±1%, 0.25W, Case Size 1206	RCA1206-2K20-FK-EA00	VISHAY
R33	820E, ±1%, 0.25W, Case Size 1206	CR1206-FX-8200ELF	BOURNS
	820E, ±1%, 0.25W, Case Size 1206	MCR18-EZP-F-820R	ROHM
	820E, ±1%, 0.25W, Case Size 1206	RCA1206-820R-FK-EA00	VISHAY
R34	820E, ±1%, 0.25W, Case Size 1206	CR1206-FX-8200ELF	BOURNS
	820E, ±1%, 0.25W, Case Size 1206	MCR18-EZP-F-820R	ROHM
	820E, ±1%, 0.25W, Case Size 1206	RCA1206-820R-FK-EA00	VISHAY
R35	10E0, ±1%, 0.25W, Case Size 1206	CR1206-FX-10R0ELF	BOURNS
	10E0, ±1%, 0.25W, Case Size 1206	MCR18-EZP-F-10R0	ROHM
	10E0, ±5%, 0.25W, Case Size 1206	RCA1206-10R0-FK-EA00	VISHAY
R36	1M0, ±1%, 0.25W, Case Size 1206	CR1206-FX-1004ELF	BOURNS
	1M0, ±1%, 0.25W, Case Size 1206	MCR18-EZP-F-1004	ROHM
	1M0, ±1%, 0.25W, Case Size 1206	RCA1206-1M00-FK-EA00	VISHAY

R37	6K8 ±1%, 0.25W, Case Size 1206	CR1206-FX-6801ELF	BOURNS
	6K8 ±1%, 0.25W, Case Size 1206	MCR18-EZP-F-6801	ROHM
	6K8 ±1%, 0.25W, Case Size 1206	RCA1206-6K80-FK-EA00	VISHAY
R38	10K0, ±1%, 0.25W, Case Size 1206	CR1206-FX-1002ELF	BOURNS
	10K0, ±1%, 0.25W, Case Size 1206	MCR18-EZP-F-1002	ROHM
	10K0, ±1%, 0.25W, Case Size 1206	RCA1206-10K0-FK-EA00	VISHAY
R39	33K0, ±1%, 0.25W, Case Size 1206	CR1206-FX-3302ELF	BOURNS
	33K0, ±1%, 0.25W, Case Size 1206	MCR18-EZP-F-3302	ROHM
	33K0, ±1%, 0.25W, Case Size 1206	RCA1206-33K0-FK-EA00	VISHAY
R40	1K2, ±1%, 0.25W, Case Size 1206	CR1206-FX-1201ELF	BOURNS
	1K2, ±1%, 0.25W, Case Size 1206	MCR18-EZP-F-1201	ROHM
	1K2, ±1%, 0.25W, Case Size 1206	RCA1206-1K20-FK-EA00	VISHAY
R41	6K2 ±1%, 0.25W, Case Size 1206	CR1206-FX-6201ELF	BOURNS
	6K2 ±1%, 0.25W, Case Size 1206	MCR18-EZP-F-6201	ROHM
	6K2 ±1%, 0.25W, Case Size 1206	RCA1206-6K20-FK-EA00	VISHAY
R42	10K0, ±1%, 0.25W, Case Size 1206	CR1206-FX-1002ELF	BOURNS
	10K0, ±1%, 0.25W, Case Size 1206	MCR18-EZP-F-1002	ROHM
	10K0, ±1%, 0.25W, Case Size 1206	RCA1206-10K0-FK-EA00	VISHAY
R43	10K0, ±1%, 0.25W, Case Size 1206	CR1206-FX-1002ELF	BOURNS
	10K0, ±1%, 0.25W, Case Size 1206	MCR18-EZP-F-1002	ROHM
	10K0, ±1%, 0.25W, Case Size 1206	RCA1206-10K0-FK-EA00	VISHAY
R44	1K2, ±1%, 0.25W, Case Size 1206	CR1206-FX-1201ELF	BOURNS
	1K2, ±1%, 0.25W, Case Size 1206	MCR18-EZP-F-1201	ROHM
	1K2, ±1%, 0.25W, Case Size 1206	RCA1206-1K20-FK-EA00	VISHAY
R45	2K2, ±1%, 0.25W, Case Size 1206	CR1206-FX-2201ELF	BOURNS
	2K2, ±1%, 0.25W, Case Size 1206	MCR18-EZP-F-2201	ROHM
	2K2, ±1%, 0.25W, Case Size 1206	RCA1206-2K20-FK-EA00	VISHAY
R46	2K2, ±1%, 0.25W, Case Size 1206	CR1206-FX-2201ELF	BOURNS
	2K2, ±1%, 0.25W, Case Size 1206	MCR18-EZP-F-2201	ROHM
	2K2, ±1%, 0.25W, Case Size 1206	RCA1206-2K20-FK-EA00	VISHAY
R47	10K0, ±1%, 0.25W, Case Size 1206	CR1206-FX-1002ELF	BOURNS
	10K0, ±1%, 0.25W, Case Size 1206	MCR18-EZP-F-1002	ROHM
	10K0, ±1%, 0.25W, Case Size 1206	RCA1206-10K0-FK-EA00	VISHAY
R48	10K0, ±1%, 0.25W, Case Size 1206	CR1206-FX-1002ELF	BOURNS
	10K0, ±1%, 0.25W, Case Size 1206	MCR18-EZP-F-1002	ROHM
	10K0, ±1%, 0.25W, Case Size 1206	RCA1206-10K0-FK-EA00	VISHAY
R49	47E0, ±1%, 0.25W, Case Size 1206	CR1206-FX-47R0ELF	BOURNS
	47E0, ±1%, 0.25W, Case Size 1206	MCR18-EZP-F-47R0	ROHM
	47E0, ±1%, 0.25W, Case Size 1206	RCA1206-47R0-FK-EA00	VISHAY
R50	56K0, ±1%, 0.25W, Case Size 1206	CR1206-FX-5602ELF	BOURNS
	56K0, ±1%, 0.25W, Case Size 1206	MCR18-EZP-F-5602	ROHM
	56K0, ±1%, 0.25W, Case Size 1206	RCA1206-56K0-FK-EA00	VISHAY

D Alternated components

Changed components

Component id	Old component/value	New component	Reason of change
R16	47 kΩ	4,7 kΩ	Too high resistance, could prevent voltage protection from functioning properly
R22	10 Ω	removed	Redundant in the circuit (causing additional power losses)
R23	10 Ω	removed	Redundant in the circuit (causing additional power losses)
R24	10 Ω	removed	Redundant in the circuit (causing additional power losses)
R25	10 Ω	removed	Redundant in the circuit (causing additional power losses)
R26	10 Ω	removed	Redundant in the circuit (causing additional power losses)
R35	10 Ω	removed	Redundant in the circuit (causing additional power losses)
Z1	56 V	30 V	Too high breakdown voltage, could prevent voltage protection from functioning properly
Z2	56 V	30 V	Too high breakdown voltage, could prevent voltage protection from functioning properly
Q5	BF422	BC546	Wrong component with wrong pin sequence

Other alterations

Component id	Scenario
D9	Opposite direction placement on PCB, leading to a short circuit
U17	Too small heat sink, and too little space on the PCB for heatsink of required size

E Program code the control system

```
//###########################################################################
//
//    Name: Closed loop control code for a DC-DC converter (boost) doing MPPT
//
//    Author:          Silje Odland Simonsen
//    Last change:     3rd of July, 2009
//
//---------------------------------------------------------------------------
// Purpose of program:
//
// A DC-DC boost converter is used for Maximum Power Point Tracking (MPPT) in
// a PV converter system. The program is collecting values from the input
// and output of the converter, and adjusting the reference voltage value to
// find the MPP of the PV source.
//
// The program contains code for:
// 1) P/PI-controller
// 2) MPPT algorithm (Perturb and Observe)
//
//###########################################################################

#include "DSP280x_Device.h"     // DSP280x Headerfile Include File
#include "DSP280x_Examples.h"   // DSP280x Examples Include File

// ADC start parameters
#define ADC_MODCLK 0x4 //HSPCLK = SYSCLKOUT/2*ADC_MODCLK2 = 100/(2*4) = 12.5MHz
#define ADC_CKPS   0x1 //ADC module clock = HSPCLK/2*ADC_CKPS = 6.25MHz
#define ADC_SHCLK  0xf // S/H width in ADC module periods  = 16 ADC clocks
#define AVG        256 // Average sample limit

#define SHIFT_AVG  8               // Defining the speed of the controller
#define X           180                 // Size of log arrays
#define DELTAV      480                 // Duty cycle step of MPPT

// Duty cycle boundaries
#define D_MAX          4750        // Maximum duty cycle, 5000*0.95 = 4750
#define D_MIN          0           // Minimum duty cycle


// Prototype statements for functions found within this file.
interrupt void adc_isr(void);
interrupt void cpu_timer0_isr(void);

// GLOBAL VARIABLES:

// Counters
Uint16 LoopCount;
Uint16 Counter;

// Readings of sampled values
Uint16 ADC_result_B4;   // Input voltage
Uint16 ADC_result_B5;   // Input current
Uint16 ADC_result_B6;   // Output voltage
Uint16 ADC_result_B7;   // Output current

// Sums up AVG values to find average
Uint32 ADC_sum_B4;
Uint32 ADC_sum_B5;
Uint32 ADC_sum_B6;
Uint32 ADC_sum_B7;
```

```
// Average of ADC_sum_Bx after AVG counts
Uint16 ADC_avr_B4;
Uint16 ADC_avr_B5;
Uint16 ADC_avr_B6;
Uint16 ADC_avr_B7;

// Offset values
Uint16 Vin_off;
Uint16 Vout_off;
Uint16 Iin_off;
Uint16 Iout_off;

// Real values
Uint16 Vin;
Uint16 Vout;
int16 Iin;
int16 Iout;

// Slope [mV/bit] or [mA/bit]
Uint16 m1;
Uint16 m2;
Uint16 m3;
Uint16 m4;

// Controller variables
Uint16 Vref;            // Reference value of the input
int16 error_k;          // Difference: error = Vref - Vin
int16 error_k_1;        // e(k-1)
Uint16 u_k;             // u(k)
Uint16 u_k_1;           // u(k-1)
int16 g0;               // parameter for e(k)
int16 g1;               // parameter for e(k-1)
int16 x0;               // on/off value for u(k-1) in the integral part
int16 PWM;              // Temporary control value
int16 P_part;           // proportional part of P-/PI-controller
int16 I_part;           // integral part of the PI-controller
int16 I_part1;          // e(k-1)*g1

// MPPT variables
int32 dP;               // change in power
Uint32 P_k;             // power at sample k
Uint32 P_k_1;           // power at sample k-1
int32 dV;               // change in voltage
Uint16 V_k;             // voltage at sample k
Uint16 V_k_1;           // voltage at sample k-1
Uint16 I_k;             // current at sample k
Uint16 deltaV;          // duty cycle step
int16 direction;        // direction of perturbation (MPPT)


// Storage arrays
Uint16 Vinlog[X];
Uint16 Vreflog[X];
int16 Ilog[X];
Uint32 Plog[X];
Uint16 Dlog[X];
Uint16 datalog_count;

int16 MPPTstart;        // initialization of the MPPT
```

```
// Counting variables for MPPT
int16 eee;
int16 fff;
int16 ggg;
int16 hhh;


main()
{
// ------------------------------
//  ALLOCATE VARIABLES
// ------------------------------
   Counter = 0;

   ADC_sum_B4 = 0;
   ADC_sum_B5 = 0;
   ADC_sum_B6 = 0;
   ADC_sum_B7 = 0;

// Calibration (manual)
   Vin_off = 250;
   Vout_off = 115;
   Iin_off = 2180;
   Iout_off = 2080;

   m1 = 12;       // m1 = ((45000-0)/(4040-25)) = 11.21 [mV]
   m2 = 8;        // m2 = ((9000-0)/(3665-2500))= 7.73  [mA]
   m3 = 19;       // m3 = ((48000-0)/(2640-55)) = 18.57 [mV]
   m4 = 8;        // m4 = ((9000-0)/(3265-2157)) = 8.12 [mA]


   Vref = 36000;  // Vref = 45*0.8 = 36 V

   g0 = -2;
   g1 =  -2;
   x0 = 1;

   I_part = 0;
   I_part1 = 0;
   P_part = 0;

   u_k = D_MIN;   // will be assigned to last value in interrupt
   error_k = 0;

   V_k_1 = 0;
   P_k_1 = 0;
   deltaV = DELTAV;
   direction = 1;

   MPPTstart = 0;

   eee = 0;
   fff = 0;
   ggg = 0;
   hhh = 0;
```

```
// zero setting the log arrays
   for (datalog_count=0;datalog_count<X;datalog_count++)
   {
         Vinlog[datalog_count] = 0;
         Vreflog[datalog_count] = 0;
         Plog[datalog_count] = 0;
         Ilog[datalog_count] = 0;
         Dlog[datalog_count] = 0;
   }
   datalog_count = 0;


// ------------------------------
// START OF SYSTEM INITIALIZATION
// ------------------------------
// STEP 1 "Initialize System Control"
// PLL, WatchDog, enable Peripheral Clocks
// This example function is found in the DSP280x_SysCtrl.c file.
   InitSysCtrl();

// Specific clock setting:
   EALLOW;
   SysCtrlRegs.HISPCP.all = ADC_MODCLK;  // HSPCLK = SYSCLKOUT/ADC_MODCLK
   EDIS;

// STEP 2: "Initialize GPIO"
// This example function is found in the DSP280x_Gpio.c file and
// illustrates how to set the GPIO to it's default state.
   InitEPwm6Gpio();

// STEP 3: "Clear all interrupts and initialize PIE vector table":
// Disable CPU interrupts
   DINT;

// Initialize the PIE control registers to their default state.
// The default state is all PIE interrupts disabled and flags
// are cleared.
// This function is found in the DSP280x_PieCtrl.c file.
   InitPieCtrl();

// Disable CPU interrupts and clear all CPU interrupt flags:
   IER = 0x0000;
   IFR = 0x0000;

// Initialize the PIE vector table with pointers to the shell Interrupt
// Service Routines (ISR).
// This will populate the entire table, even if the interrupt
// is not used in this example.  This is useful for debug purposes.
// The shell ISR routines are found in DSP280x_DefaultIsr.c.
// This function is found in DSP280x_PieVect.c.
   InitPieVectTable();

// Interrupts that are used in this example are re-mapped to
// ISR functions found within this file.
   EALLOW;  // This is needed to write to EALLOW protected register
   PieVectTable.ADCINT = &adc_isr;
   PieVectTable.TINT0 = &cpu_timer0_isr;
   EDIS;  // This is needed to disable write to EALLOW protected registers
```



```
// STEP 4: "Initialize all the Device Peripherals"
// These functions are found in DSP280x_InitPeripherals.c
```

```
   InitAdc();          // init the ADC
   InitCpuTimers();    // initialize the Cpu Timers

// Configure CPU-Timer 0 to interrupt every second:
// 100MHz CPU Freq, 1 second Period (in uSeconds)
   ConfigCpuTimer(&CpuTimer0, 100, 1000000);
   StartCpuTimer0();

// Enable ADCINT in PIE
   PieCtrlRegs.PIEIER1.bit.INTx6 = 1;
   PieCtrlRegs.PIEIER1.bit.INTx7 = 1;

   IER |= M_INT1;            // Enable CPU Interrupt 1
   EINT;                     // Enable Global interrupt INTM
   ERTM;                     // Enable Global realtime interrupt DBGM

   LoopCount = 0;


// ------------------------------
//  ADC Setup
// ------------------------------

  AdcRegs.ADCTRL1.bit.ACQ_PS = ADC_SHCLK;
  AdcRegs.ADCTRL3.bit.ADCCLKPS = ADC_CKPS;
  AdcRegs.ADCCHSELSEQ1.bit.CONV00 = 0x0C;// select channel B4 for conversion
  AdcRegs.ADCCHSELSEQ1.bit.CONV01 = 0x0D;   // select channel B5 for conversion
  AdcRegs.ADCCHSELSEQ1.bit.CONV02 = 0x0E;   // select channel B6 for conversion
  AdcRegs.ADCCHSELSEQ1.bit.CONV03 = 0x0F;   // select channel B7 for conversion
  AdcRegs.ADCMAXCONV.all = 0x0003;             // 4 conversions in the sequence

  AdcRegs.ADCTRL2.bit.EPWM_SOCA_SEQ1 = 1; //Enable SOCA from ePWM to start SEQ1
  AdcRegs.ADCTRL2.bit.INT_ENA_SEQ1 = 1;   // Enable SEQ1 interrupt (every EOS)


// ------------------------------
//  ePWM6 Setup
// ------------------------------
      //set PWM-period
      EPwm6Regs.TBPRD = 5000; // Period (one count = 10ns) --> fPWM = 20 kHz

      // set compare values A and B
      EPwm6Regs.CMPB = 2500;              // initial duty cycle = 50%
      EPwm6Regs.CMPA.half.CMPA = 25 ;    // Compare A = 25 TBCLK counts, used for
                                              starting ADC-conversion

      EPwm6Regs.TBCTL.bit.CTRMODE = TB_COUNT_UP;     //sawtooth, start counting up
      EPwm6Regs.TBCTR = 0;                           // clear TB counter
      EPwm6Regs.TBCTL.bit.PHSEN = TB_DISABLE;        // Phase loading disabled
      EPwm6Regs.TBCTL.bit.PRDLD = TB_SHADOW;
      EPwm6Regs.TBCTL.bit.SYNCOSEL = TB_SYNC_DISABLE;
      EPwm6Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;       // TBCLK = SYSCLK
      EPwm6Regs.TBCTL.bit.CLKDIV = TB_DIV1;
      EPwm6Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;
      EPwm6Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;
      EPwm6Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO;  // load on CTR = Zero
      EPwm6Regs.CMPCTL.bit.LOADBMODE = CC_CTR_ZERO;  // load on CTR = Zero
      EPwm6Regs.AQCTLA.bit.ZRO = AQ_SET;             // Action-Qualifier
      EPwm6Regs.AQCTLA.bit.CAU = AQ_CLEAR;
      EPwm6Regs.AQCTLB.bit.ZRO = AQ_SET;
      EPwm6Regs.AQCTLB.bit.CBU = AQ_CLEAR;
```

```
    EPwm6Regs.ETSEL.bit.SOCAEN = 1;    // Enable SOC on ADC-sequencer A
    EPwm6Regs.ETSEL.bit.SOCASEL = 4;   // Select SOC from from CPMA on upcount
    EPwm6Regs.ETPS.bit.SOCAPRD = 1;

// Infinite loop
   for(;;)
   {
          LoopCount++;

      // MPPT loop
      if (CpuTimer0.InterruptCount == 1) // once every second
      {
      V_k = Vin;
      I_k = Iin;

      P_k = (Uint32)V_k*(Uint32)I_k;

      if(datalog_count < X)              // log values
      {
      Vinlog[datalog_count] = Vin;
      Vreflog[datalog_count] = Vref;
      Plog[datalog_count] = P_k;
      Ilog[datalog_count] = Iin;
      Dlog[datalog_count] = u_k;
      datalog_count++;
      }

      // MPPTstart - first running
      if (MPPTstart == 0)
      {
      P_k_1 = P_k;
      V_k_1 = V_k;

      MPPTstart = 1;
      }

      dP = (P_k) - (int32)(P_k_1);
      dV = V_k - (int32)V_k_1;
```

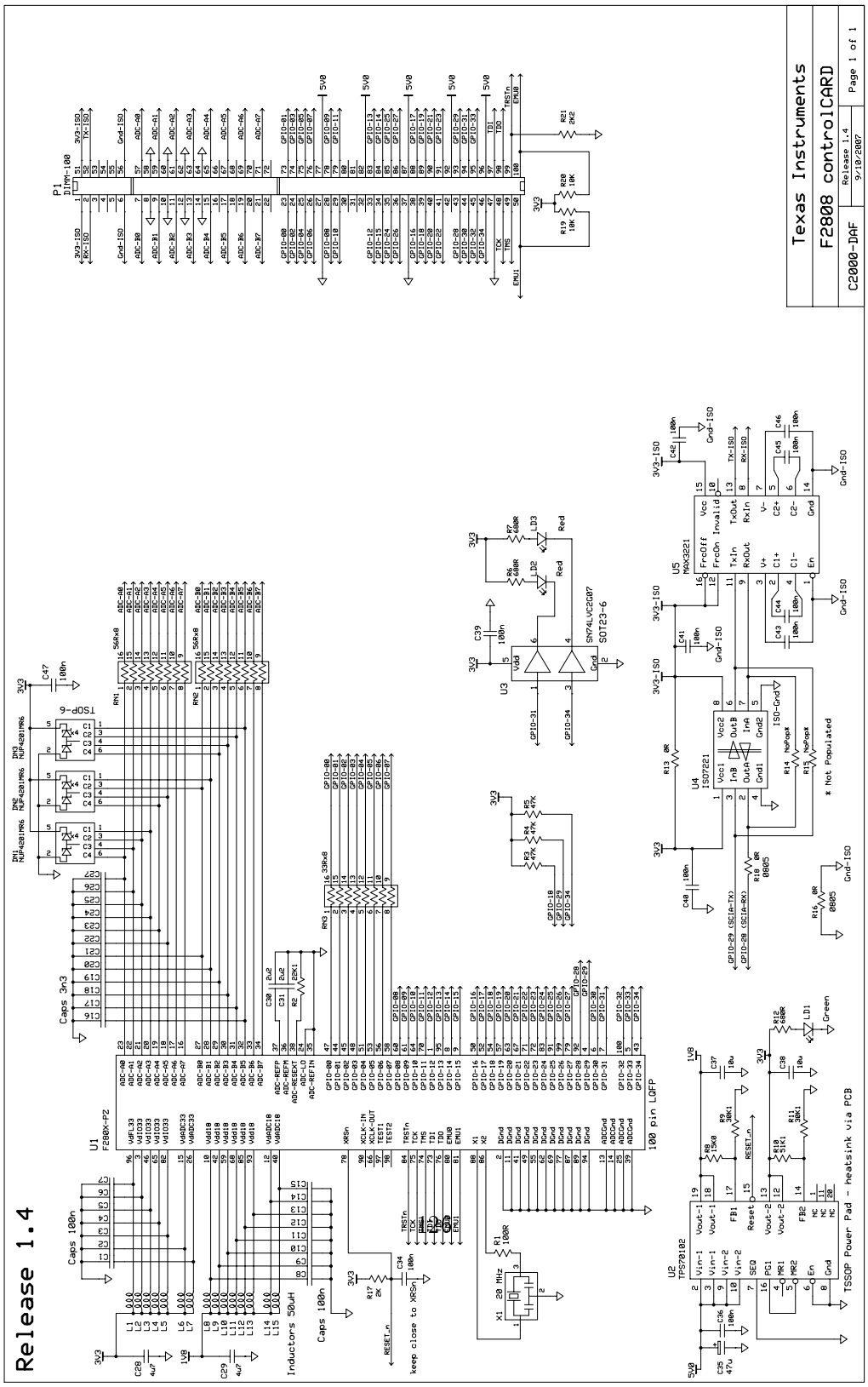
```
// Start evaluation
if (dP > 0)
            {
                  if (dV > 0)
                  {
                        eee++;
                        direction = 1;
                  }
                  if (dV < 0)
                  {
                        fff++;
                        direction = -1;
                  }
            }
            if (dP < 0)
            {
                  if (dV > 0)
                  {
                        ggg++;
                        direction = -1;
                  }
                  if (dV < 0)
                  {
                        hhh++;
                        direction = 1;
                  }
            }

      // Perturbation
      Vref = Vref + direction*deltaV;

      // Boundary test
      if (Vref < 200)
            { Vref = 200;}
      if (Vref > 45000)
            {Vref = 45000;}


      // Value updates
      V_k_1 = V_k;
      P_k_1 = P_k;


      CpuTimer0.InterruptCount = 0; // Reset counter


      } // end MPPT
   } // end LoopCount loop

} // end main
```

```
// ------------------------------
//  INTERRUPTS
// ------------------------------

interrupt void cpu_timer0_isr(void)
{
   CpuTimer0.InterruptCount++;

   // Acknowledge this interrupt to receive more interrupts from group 1
   PieCtrlRegs.PIEACK.all = PIEACK_GROUP1;
}


interrupt void  adc_isr(void)
{

Counter++;

            // Storing sampled values
            ADC_result_B4 = ((AdcRegs.ADCRESULT0>>4));
            ADC_result_B5 = ((AdcRegs.ADCRESULT1>>4));
            ADC_result_B6 = ((AdcRegs.ADCRESULT2>>4));
            ADC_result_B7 = ((AdcRegs.ADCRESULT3>>4));

            // Adding to the sum
            ADC_sum_B4 = ADC_sum_B4 + ADC_result_B4;
            ADC_sum_B5 = ADC_sum_B5 + ADC_result_B5;
            ADC_sum_B6 = ADC_sum_B6 + ADC_result_B6;
            ADC_sum_B7 = ADC_sum_B7 + ADC_result_B7;

if (Counter == AVG)
{
     // Find average value
       ADC_avr_B4 = (ADC_sum_B4 >> SHIFT_AVG);
       ADC_avr_B5 = (ADC_sum_B5 >> SHIFT_AVG);
       ADC_avr_B6 = (ADC_sum_B6 >> SHIFT_AVG);
       ADC_avr_B7 = (ADC_sum_B7 >> SHIFT_AVG);

       // Set sum equal to 0
       ADC_sum_B4 = 0;
       ADC_sum_B5 = 0;
       ADC_sum_B6 = 0;
       ADC_sum_B7 = 0;

     // Calculate real values of voltages and currents
     Vin = (ADC_avr_B4 - Vin_off) * m1;
     Iin = (ADC_avr_B5 - Iin_off) * m2;
     Vout = (ADC_avr_B6 - Vout_off) * m3;
     Iout = (ADC_avr_B7 - Iout_off) * m4;
```

```
// ------------------------------
//  P-/PI-CONTROLLER
// ------------------------------

u_k_1 = u_k;
error_k_1 = error_k;

// P-part
error_k = Vref - Vin;
P_part = (error_k>>5)*g0;

// I-part

I_part1 = (error_k_1>>5)*g1;
I_part = x0*u_k_1 + I_part1;

// Calculation of u(k)
PWM = (I_part) + (P_part);    // CMPB without saturation

// Boundary check
      if (PWM < 0)
      {
            PWM = D_MIN;
      }
      if (PWM > D_MAX)
      {
            PWM = D_MAX;
      }

u_k = PWM;

// update ePWM6 duty cycle
 EPwm6Regs.CMPB = u_k;

// Reset counter
Counter = 0;
}

// Reinitialize for next ADC sequence
  AdcRegs.ADCTRL2.bit.RST_SEQ1 = 1;         // Reset SEQ1
  AdcRegs.ADCST.bit.INT_SEQ1_CLR = 1;       // Clear INT SEQ1 bit
  PieCtrlRegs.PIEACK.all = PIEACK_GROUP1;   // Acknowledge interrupt to PIE


  return;
}

//===========================================================================
// End of program
//===========================================================================
```

F DSP relevant files

F.1 Circuit diagrams overview for TMS320F2808 Control Card



F2808 controlCARD [R1.4] DIMM100 pin-out

V33D-ISO	1	51	V33D-ISO
ISO-RX-RS232	2	52	ISO-TX-RS232
spare	3	53	*spare*
spare	4	54	*spare*
spare	5	55	*spare*
GND_ISO	6	56	GND_ISO
ADCIN-B0	7	57	ADCIN-A0
GND	8	58	GND
ADCIN-B1	9	59	ADCIN-A1
GND	10	60	GND
ADCIN-B2	11	61	ADCIN-A2
GND	12	62	GND
ADCIN-B3	13	63	ADCIN-A3
GND	14	64	GND
ADCIN-B4	15	65	ADCIN-A4
spare	16	66	*spare*
ADCIN-B5	17	67	ADCIN-A5
spare	18	68	*spare*
ADCIN-B6	19	69	ADCIN-A6
spare	20	70	*spare*
ADCIN-B7	21	71	ADCIN-A7
spare	22	72	*spare*
GPIO-00 / EPWM-1A	23	73	GPIO-01 / EPWM-1B / SPISIMO-D
GPIO-02 / EPWM-2A	24	74	GPIO-03 / EPWM-2B / SPISOMI-D
GPIO-04 / EPWM-3A	25	75	GPIO-05 / EPWM-3B / SPICLK-D / ECAP-1
GPIO-06 / EPWM-4A / SYNCI / SYNCO	26	76	GPIO-07 / EPWM-4B / SPISTE-D / ECAP-2
GND	27	77	+5V in
GPIO-08 / EPWM-5A / CANTX-B / ADCSOC-A	28	78	GPIO-09 / EPWM-5B / SCITX-B / ECAP-3
GPIO-10 / EPWM-6A / CANRX-B / ADCSOC-B	29	79	GPIO-11 / EPWM-6B / SCIRX-B / ECAP-4
spare	30	80	*spare*
spare	31	81	*spare*
spare	32	82	+5V in
GPIO-12 / TZ-1 / CANTX-B / SPISIMO-B	33	83	GPIO-13 / TZ-2 / CANRX-B / SPISOMI-B
GPIO-15 / TZ-4 / SCIRX-B / SPISTE-B	34	84	GPIO-14 / TZ-3 / SCITX-B / SPICLK-B
GPIO-24 / ECAP-1 / EQEPA-2 / SPISIMO-B	35	85	GPIO-25 / ECAP-2 / EQEPB-2 / SPISOMI-B
GPIO-26 / ECAP-3 / EQEPI-2 / SPICLK-B	36	86	GPIO-27 / ECAP-4 / EQEPS-2 / SPISTE-B
GND	37	87	+5V in
GPIO-16 / SPISIMO-A / CANTX-B / TZ-5	38	88	GPIO-17 / SPISOMI-A / CANRX-B / TZ-6
GPIO-18 / SPICLK-A / SCITX-B	39	89	GPIO-19 / SPISTE-A / SCIRX-B
GPIO-20 / EQEPA-1 / SPISIMO-C / CANTX-B	40	90	GPIO-21 / EQEPB-1 / SPISOMI-C / CANRX-B
GPIO-22 / EQEPS-1 / SPICLK-C / SCITX-B	41	91	GPIO-23 / EQEPI-1 / SPISTE-C / SCIRX-B
spare	42	92	+5V in
GPIO-28 / SCIRX-A / Resv / TZ5	43	93	GPIO-29 / SCITX-A / Resv / TZ6
GPIO-30 / CANRX-A	44	94	GPIO-31 / CANTX-A
GPIO-32 / I2CSDA / SYNCI / ADCSOCA	45	95	GPIO-33 / I2CSCL / SYNCO / ADCSOCB
GPIO-34	46	96	+5V in
GND	47	97	TDI
TCK	48	98	TDO
TMS	49	99	TRSTn
EMU1	50	100	EMU0

Texas Instruments – C2000

F.2 Relevant documents for the TMS320F2808 Controller

There are a lot of documents available from the homepage of Texas Instruments. The most relevant are listed in the table below, and can also be found among the files included with the thesis. Other related documents can also be found in the documents in the table or at www.ti.com.

Table 13: Relevant files from TI

File name	*Id number*
TMS320C28x CPU and Instruction Set Reference Guide	SPRU430
TMS320x280x, 28xxx System Control and Interrupts Reference Guide	SPRU712
TMS320x280x, 2801x, 2804x DSP Analog-to-Digital Converter (ADC)	SPRU716B
TMS320x28xx Enhanced Pulse Width Modulator (ePWM) Module Ref Guide	SPRU791
Getting Started With TMS320C28x Digital Signal Controllers	SPRAAM0A
TMS320F280x Based Digitally Controlled DC-DC Switching Power Supply	SPRAAB3
Using PWM Output as a Digital-to-Analog Converter on a TMS320F280x DSP	SPRAA88A
TMS320F2808 DSP Data Manual	SPRS230J
Code Composer Studio IDE v3 White Paper	SPRAA08
How to write Multiplies Correctly in C code	SPRA683

F.3 Example files for the DSP Controller

For running the DSP Controller in CCS, Texas Instruments has several example/preprogrammed files for initialization of the different modules of the DSP Controller. The most important ones used in this master thesis are:

File name	***Contents***
DSP280x_Adc.c	ADC Initialization & Support Functions
DSP280x_CodeStartBranch.asm	Branch for redirecting code execution after boot
DSP280x_CpuTimers.c	CPU 32-bit Timers Initialization & Support Functions
DSP280x_DefaultIsr.c	Default Interrupt Service Routines
DSP280x_EPwm.c	ePWM Initialization & Support Functions
DSP280x_GlobalVariableDefs.c	Global Variables and Data Section Pragmas
DSP280x_PieCtr.c	PIE Control Register Initialization Functions
DSP280x_PieVect.c	PIE Vector Table Initialization Functions
DSP280x_SysCtrl.c	System Control Initialization & Support Functions
DSP280x_usDelay.asm	Simple delay function

G Instrument list

The instruments and equipment used while working in the laboratory is listed in this appendix.

Table 14: Laboratory Equipment

Equipment description	*Name/Distributor*	*Id number*
DSP Control Card	TMS320F2808	-
DSP Docking Station	BH28xxx	P08-0225
DSP Power Supply	-	B08-0227
JTag Emulator	Blackhawk USB2000 Controller	P08-0223
PV Simulator	Schulz Electronic	B02-0516-01
PV Power Supply SM300-20 (S290)	Delta Electronica	B02-0516
Digital Power Experimenter Board	TI 2 Ch Buck EVM F280xx	P08-0230
Educational Design and Prototyping Platform	NI ELVIS	P08-0232
Oscilloscope	Tektronix	G04-0315
Function Generator	Agilent 33250A	B03-0316
Multimeter	Fluke	S03-0355
Multimeter	Fluke 117	S03-0385
DC Power supply	EA - PS7065-100	B02-0385
DC Power supply	GW Instek	B02-0461
Electronic Load	EA - EL9080-200	B02-0507
Cables with safety	-	-
Crocodile clip	-	-
Soldering device	-	-

H PV Simulator characteristics

The characteristics for the PV simulator was found by sweeping the reference voltage through the range of 0-45 V and store the input values (current, voltage and power). The sweeping was done for several levels of irradiance and temperatures, as shown in the figures. It must be noted that the values of the characteristics are dependent of the calibration done in the program, and might not correspond exactly to the actual values in the system.

H.1 Changes in irradiance levels

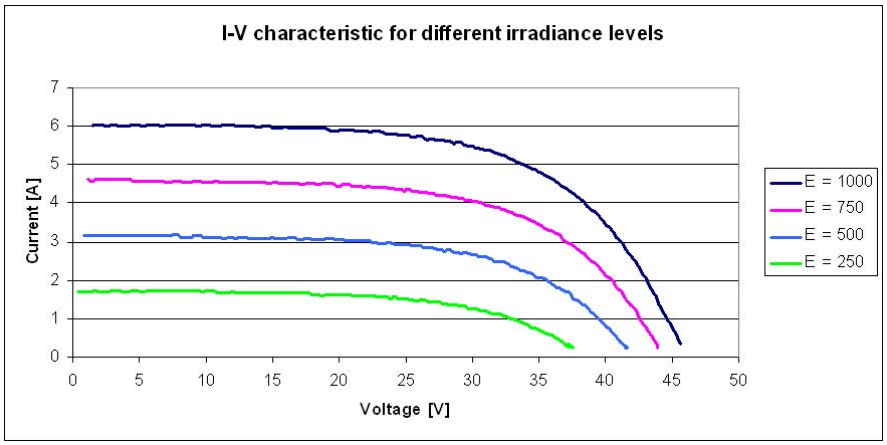


Figure 57: I-V characteristic for different irradiance levels

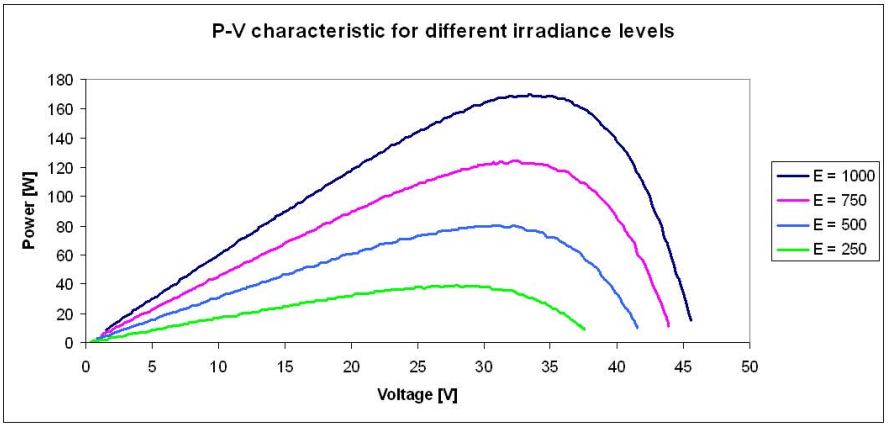


Figure 58: P-V characteristic for different irradiance levels

Table 15: MPP for different irradiance levels

$E[\frac{kW}{m^2}]$	$P_{MPP}[W]$	$V_{MPP}[V]$	$I_{MPP}[A]$
1000	169,96	33,46	5,08
750	124,45	32,21	3,86
500	80,71	30,95	2,61
250	39,07	26,54	1,47

H.2 Changes in temperature levels

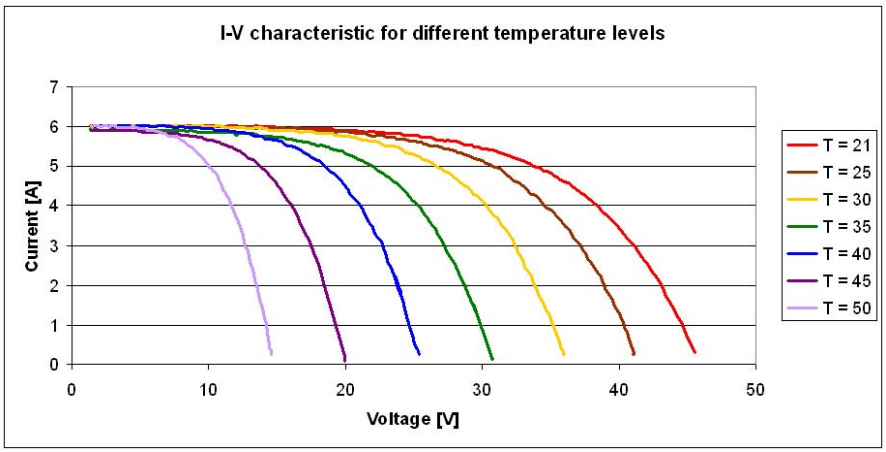


Figure 59: I-V characteristic for different temperature levels

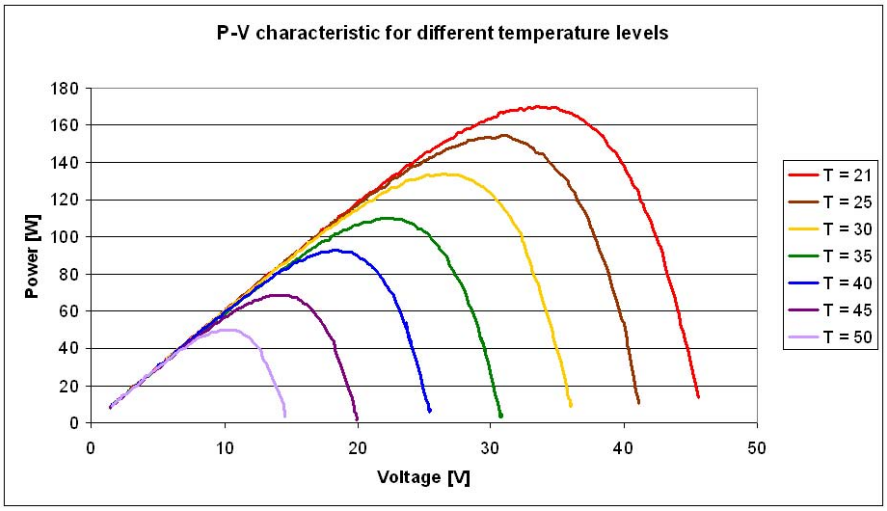


Figure 60: P-V characteristic for different temperature levels

Table 16: MPP for different temperature levels

$T[C°]$	$P_{MPP}[W]$	$V_{MPP}[V]$	$I_{MPP}[A]$
21	169,96	33,46	5,08
25	154,18	30,98	4,96
30	133,66	26,52	5,04
35	110,10	21,98	5,01
40	92,78	18,47	5,02
45	68,88	14,23	4,84
50	50,37	10,48	4,81

I How to develop a compensation network for a boost converter in a PV system

It is common in control theory to develop the socalled "transfer function" for the different parts of the circuit. The transfer function defines the ratio between a defined input and the following output. For the buck and boost converters the control scheme can be divided into the PWM modulator, the switch and the filter at the output.

In the boost converter circuit the output capacitor is in the critical path (which means that the dI/dt is very high during the switch transition) and should be close to the control IC, along with the diode. A paralleled ceramic capacitor might be helpful, as long as it doesn't cause instability.

In a regular DC power supply the input voltage or the load might have sudden changes, and the output voltage is required to suppress the disturbances caused by this. In PV systems it is the input voltage that should withstand the disturbances. As the output voltage is assumed constant, the load changes (through change in current) will cause disturbances in the input voltage.

How to develop the transfer function for the boost converter in a PV System
When using a boost converter for regulating the input voltage in a PV system, the control structure becomes similar to the one of the buck converter if the complementary duty cycle $D' = 1$ - D is used as open loop control input. If the switches Q3 and Q4 are used for complimentary switching the converter can be operated in CCM, which allows for developing the transfer function for CCM. The transfer function can then be developed through utilization of a method presented in the technical brief "Designing Stable Compensation Networks for Single Phase Voltage Mode Buck Regulators" from Intersil. All figures in this section is taken from this paper, to give explanations and present the relations to the boost converter in this master thesis.

The basic block diagram of the converter control is shown in figure 61. The modulator accounts for the PWM module. The input from the error amplifier corresponds to the control value which is compared to the repetitive waveform, and the output of the modulator is the duty cycle D.

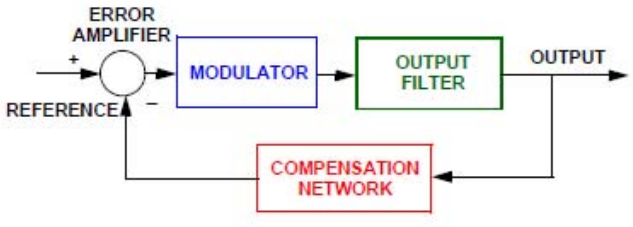


Figure 61: Basic block of the buck regulator

The transfer function for the modulator will normally correspond to a linear amplifier (due to the Sample-and-Hold effect of the DAC module), which can be written as:

$$G_{PWM} = \frac{d}{v_c} = \frac{1}{\hat{V_{tri}}} \tag{47}$$

In the technical brief the switch and the PWM modulator gain is merged into the modulator block, where the value of the switch is the output voltage of the boost converter.

The filter part of the converter is shown in figure 62. Since the buck converter corresponds to the boost converter seen in the opposite direction, V_{OUT} represents the input voltage. The ESR is the equivalent series resistance of the input capacitor, and DCR is the DC resistance of the inductor.

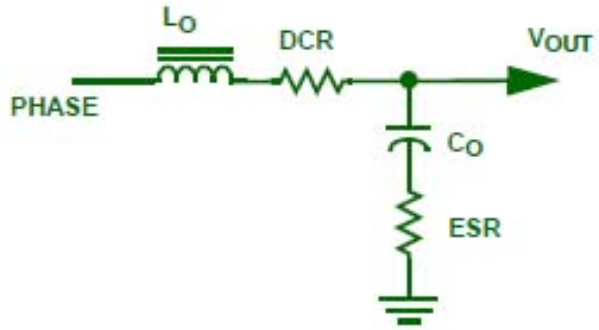


Figure 62: Output filter

There will be introduced a zero due to the ESR of the input capacitor, and two poles due to the LC filter. Assuming a constant DC link voltage will also ensure that the DC gain of the transfer function is constant. The resulting (open loop) transfer function for complimentary control to input is then:

$$G_d' v_{in} = G_M \frac{1 + s \cdot ESR \cdot C_{in}}{1 + (ESR + DCR) C_{in} s + s^2 \cdot L_{boost} \cdot C_{in}} \tag{48}$$

Now the compensator or controller can be developed through several tools, for instance Matlab.