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Control of Multi-terminal VSC-HVDC Systems

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Problem Description

The North Sea has a vast amount of wind energy with largest energy per area densities located about 100-300Km of distance from shore. Should this energy be tapped by offshore wind farms, HVDC transmission would be the more feasible solution at such distances of subsea transmission. On the other hand Norwegian oil/gas platforms in the North Sea use electricity from gas fired turbines at offshore sites. These gas turbines have much less efficiency than onshore generation of electricity and also release large amounts of green house gases. Therefore supplying the platforms with power from onshore transmitted by HVDC will result in benefits both from economic and environmental protection perspectives.

Given these two interests for HVDC in the Norwegian offshore, the use of Multiterminal HVDC (MTDC) is a potential solution for the integration of the wind farms and oil/gas platforms into the onshore grid.

Control systems for multiterminal HVDC (MTDC) networks should be developed and their operation be analyzed. First controllers for two-terminal HVDC connected to different types of AC grids must be developed and analyzed. Then this must be extended to develop control of multiterminal HVDC system. Models should be developed in PSCAD/EMTDC simulation software and results should be analyzed to validated proposed control schemes.

Assignment given: 22. January 2008
Supervisor: Tore Marvin Undeland, ELKRAFT

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Abstract

The North Sea has a vast amount of wind energy with largest energy per area densities located about 100-300Km of distance from shore. Should this energy be tapped by offshore wind farms, HVDC transmission would be the more feasible solution at such long subsea distances. On the other hand Norwegian oil/gas platforms in the North Sea use electricity from gas fired turbines at offshore sites. These gas turbines have much less efficiency than onshore generation of electricity and also release large amounts of green house gases. Therefore supplying the platforms with power from onshore transmitted by HVDC will result in benefits both from economic and environmental protection perspectives.

Given these two interests for HVDC in the Norwegian offshore, the use of Multiterminal HVDC (MTDC) is a potential solution for the integration of the wind farms and oil/gas platforms into the onshore grid system. Hence, this thesis focuses on the operation and control of MTDC systems. The MTDC system is desired to be capable of interfacing with all kinds of AC grids namely: stiff, weak and passive grid systems.

Compared to the classical thyristor based converter, VSC has several features that make it the most suitable converter for making of MTDC, the most decisive being its ability of bidirectional power transfer for fixed voltage polarity. VSC-HVDC is also suitable for implementing control of active and reactive current in synchronously rotating *d-q* reference frame which in turn results in decoupled control of active and reactive power.

In the first two chapters of the thesis literatures are reviewed to understand operation of VSC and its use in HVDC systems. Afterwards controllers are developed for different AC connections (stiff, weak and passive) and for different DC parameter (power, DC voltage) control modes. DC voltage and active power control are implemented by active current control and AC voltage and reactive power control are achieved by reactive power compensation. Tuning techniques for the PI controllers are discussed and used in the simulation models. Finally control techniques for reliable operation of MTDC are developed. In order to validate theoretical arguments, each of the control schemes was developed and simulated in PSCAD/EMTDC simulation software.

Simulation results indicate that satisfactory performance of VSC-HVDC was obtained with the proposed active/reactive power controllers, AC/DC voltage controllers, frequency and DC overvoltage controllers.

For coordinated multiterminal operation, *voltage margin control method* and *DC voltage droop characteristic* were used. These are control methods based upon realization of desired P-U_{DC} characteristic curves of converter terminals.

Four-terminal MTDC system with different AC grid connections was used to study the multiterminal operation. Simulations have shown that *voltage margin control method* results in reliable operation of MTDC during loss of a terminal connection **without the need for communication between terminals**. The use of DC voltage droop control along with voltage margin control enabled load sharing among VSC-HVDC terminals in DC voltage control mode according to predetermined participation factor.

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Finally I would like to thank my parents, my brother and my sister for their love and support.

Acronyms

AC	alternating current
DC	direct current
HVDC	high voltage direct current
VSC	voltage sourced converter
PWM	pulse width modulation
SV-PWM	space vector pulse width modulation
MTDC	multiterminal HVDC
FACTS	flexible AC transmission system
IGBT	insulated gate bipolar transistor
IEGT	injection enhanced gate transistor
GTO	gate turnoff thyristor
IGCT	integrated gate commutated thyristor
GCT	gate commutated turnoff thyristor
PCC	point of common coupling

Chapter 1

Introduction

1.1 Background

Advancement in production technology of semiconductors and control systems has brought a new era of multifarious applications for power electronic devices. One such application that has become an important element in the modern electric power industry is High Voltage Direct Current (HVDC) transmission technology. Although the first commercial HVDC link was used for submarine power transmission, it has also been in use for the purpose of reducing transmission losses in long distance power links and interconnection of asynchronous power grids.

The earliest HVDC system used mercury valves which, on the advent of power semiconductor technology, were subsequently replaced by thyristor valves. The thyristor based HVDC system, also called classical HVDC, is currently superior in transmitting maximum bulk power for long distances and in a given right of way corridor [1]. With the price of thyristors decreasing and their voltage and current ratings increasing, it is expected that classical HVDC will remain dominant in point to point long distance and submarine bulk power transmission.

Although the classical HVDC has the aforementioned advantages, the need for active network connection at both ends (and hence its inability to supply passive loads), its consumption of reactive power at both terminals, its inability to reverse the direction of current flow, and its susceptibility to commutation failures have been the down sides of classical HVDC. These constraints have limited the use of classical HVDC to power transmission between two points. In the light of this understanding, Voltage Sourced Converter - HVDC (VSC-HVDC), a recent arrival in the arena of high voltage technology, has eliminated all the mentioned drawbacks of

classical HVDC and opened new application areas and possibilities. VSC-HVDC consists of three phase switch mode converter and uses pulse width modulation (PWM) for controlling its phase voltages.

Since VSC-HVDC does not need changing its DC voltage polarity for either direction of power flow and is capable of independent control of active and reactive power flow, it has attracted attention as a promising candidate for developing Multiterminal HVDC (MTDC) system. MTDC is a DC equivalent of AC grid which will have DC transmission network connecting more than two AC/DC converter stations. The range of operating voltage of the DC transmission is expected to be with in specified upper and lower limits. The upper limit of the operating DC voltage can be determined by the ratings of the DC cables, DC circuit breakers or the forward blocking capacity of the IGBTs used in the VSC. The lower limit of the operating DC voltage is determined by the maximum of the operating AC voltages of all the converter stations incorporated in the MTDC system.

If the upper limit of the operating voltage is exceeded, there could follow equipment failure and perhaps subsequent blackout. When the DC operating voltage becomes below the minimum limit, one or more of the VSC-HVDC stations go into 'saturation' condition due to over modulation and the VSC-HVDC terminal will no more respond properly to the controllers.

In practice, the upper and lower voltage limit settings of the MTDC should have sufficient safety margins from the previously mentioned limits.
It is desirable that:

1. The DC voltage of the MTDC should be free from oscillations during disturbances and fault occurrences on the AC sides of the VSC-HVDC stations.
2. Each terminal is capable of independent control of active and reactive power, AC voltage support and frequency droop control as per the need.

With these requirements fulfilled, each VSC-HVDC station will act as inertia-less synchronous machine in the sense that there is almost no delay in the power control response. This is a feature useful in stabilizing the AC system connected to the VSC-HVDC terminal during disturbances.

Another interesting feature is, unlike with synchronous generators, it is possible to implement negative sequence voltage control with VSC-HVDC. This is useful in phase voltage control of the three phase system in unbalanced conditions.

During isolated operation, VSC-HVDC terminal can serve as STATCOM to supply reactive power to the AC system.

1.2 MTDC for Offshore Wind Farms in the North Sea

One interesting potential for application of MTDC in Norway is to interconnect offshore wind farms and oil/gas platforms into the national grid onshore. The offshore wind energy of Norway is said to surpass the nation's current production of hydropower. This vast amount of energy resource, together with the remoteness of the area from public sight, has stimulated research works towards developing offshore wind farms in the North Sea.

Although the challenges of developing offshore wind farms in the deep sea are enormous, equally balanced by the interest for harnessing the energy resource out there and increasing energy price, it is expected that realization of commercial offshore wind farms in the deep North Sea will be a near future [2]. Many of these sites of vast wind energy potentials are located 100-300 Km from onshore [2]. For reasons of large capacitive currents HVAC will likely not be a technically and economically feasible solution for such submarine distances. This makes HVDC the more feasible solution in this particular case.

On the other hand the Norwegian oil and gas platforms, which currently use gas turbines except in one case [15], contribute towards a large share of the total CO_2 emission in Norway [16]. For economic and environmental protection reasons there has been a tendency towards replacing the gas turbines with electric supply from onshore grid.

An interconnection between the offshore wind farms, the platforms and onshore grid results in reduced operational costs, increased reliability and reduced CO_2 emissions. MTDC network will then be the core of such an interconnection system. MTDC can also open new power market

opportunities and result in better utilization of transmission lines [17]. A schematic of MTDC interconnecting an offshore wind farm, offshore oil/gas platform and onshore grid system is shown in Figure 1.1.

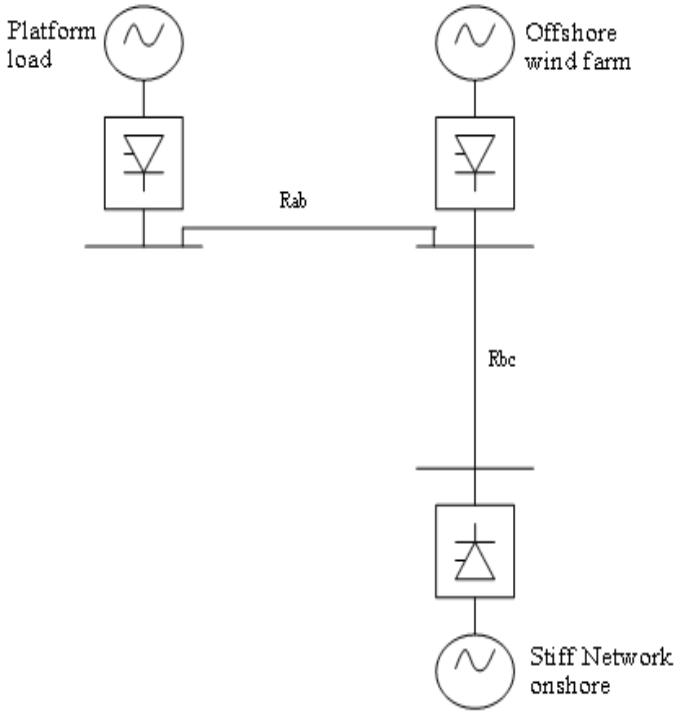


Figure 1.1: Proposed interconnections for offshore oil/gas platform, offshore wind farm and onshore grid.

1.3 Scope of the Thesis Work

This thesis work focuses on operation and control of MTDC system based upon VSC terminals. MTDC is a fairly new field of research and so far there is no MTDC system in commercial operation by the time this thesis was written. Operating MTDC system in all possible scenarios of AC connections (passive load, weak grid and stiff grid) and with different controls of DC parameters (constant power, constant DC voltage) must be investigated. Hence VSC-HVDCs connected to the various types of the AC grid systems will be established and control systems developed. Finally the proposed control techniques together with the MTDC models will be simulated in PSCAD/EMTDC software to analyze the steady state and dynamic responses. Simulation results should validate proposed control schemes and show the possibility of building MTDC with VSC terminals.

Chapter Two

Operating Principles of VSC-HVDC

2.1 Types of Power Semiconductors

Semiconductor devices that are used for power electronic applications such as HVDC and Flexible AC Transmission Systems (FACTS) are classified into *uncontrolled, half-controlled and fully controlled* semiconductors depending upon the controllability of their ON and OFF states. Power diodes belong to the uncontrolled semiconductor devices category where as thyristors are in the half-controlled group since their switching-on is controlled. Fully-controlled semiconductors allow controlling both switching-on and switching-off. Hence the term '*switch'* in power electronics often refers to the fully controlled semiconductor devices.

Although power transistors are the most common types of switches, there are also special types of fully controlled thyristors that belong to the same group [3]. Below is a summary of fully-controlled high power semiconductors.

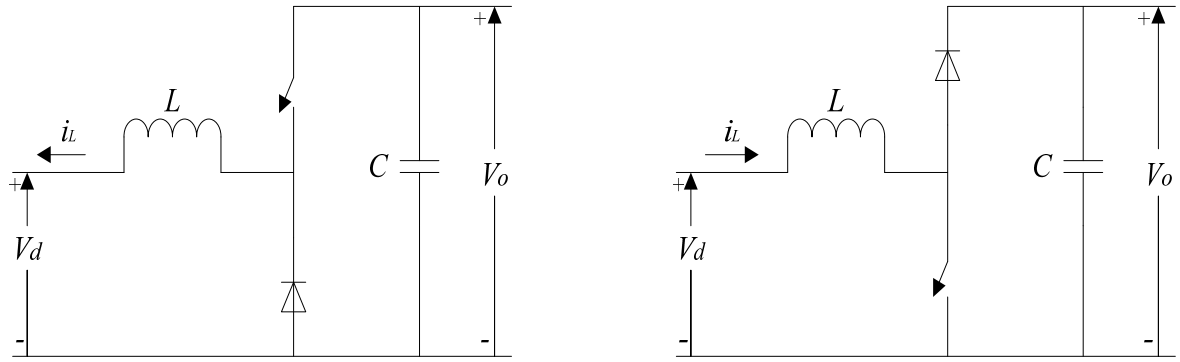
Table 2.1 Summary of fully-controlled high power semiconductors

Acronym	Type	Full name
IGBT	Transistor	Insulated Gate Bipolar Transistor
IEGT	Transistor	Injection Enhanced Gate Transistor
GTO	Thyristor	Gate Turnoff Thyristor
IGCT	Thyristor	Integrated Gate Commutated Thyristor
GCT	Thyristor	Gate Commutated Turnoff Thyristor

Since the voltage rating of a single semiconductor device would be too small as compared to the voltage levels of HVDC transmission, several tens of them will be stacked in series and in parallel and controlled simultaneously to achieve the required voltage and current ratings respectively.

2.2 Understanding VSCs

The operating principles of VSC can be understood by tracking its topology back to the simplest switch mode DC-DC converters: namely step-down (Buck) converter and step-up (Boost) converters. *Switch mode* refers to the high frequency switching of the electronic valves involved in the energy conversion process. Step-up and step-down DC-DC converters are shown in Figure 2.1. A rigorous discussion of these DC-DC converters is found in [3].



a. Step-down converter

b. Step-up converter

Figure 2.1: Schematics of step-down (Buck) and step-up (Boost) converters

Note that in Figure 2.1 the step-down and step-up converters convey power in opposite directions.

In order to conduct current, the switches in the converters must be forward biased in addition to providing the pulse width modulated signals to the switch gates. When the switches are forward biased, the voltages relations will be given by:

$$V_d = D_1 V_o \tag{2.1}$$

for the step-down converter and

$$V_d = (1 - D_2) V_o \tag{2.2}$$

for the step-up converter respectively.

D_1 and D_2 are duty ratios of the switches in the step-down and step up converters respectively. The duty ratio of a switch is defined as the ratio of its ON-state time during one cycle to one period of the switching frequency.

$$D = \frac{T_{on}}{T_s} \tag{2.3}$$

And

$$T_s = \frac{1}{f_s} \tag{2.4}$$

where f_s is the switching frequency.
This relation is shown in the following diagram.

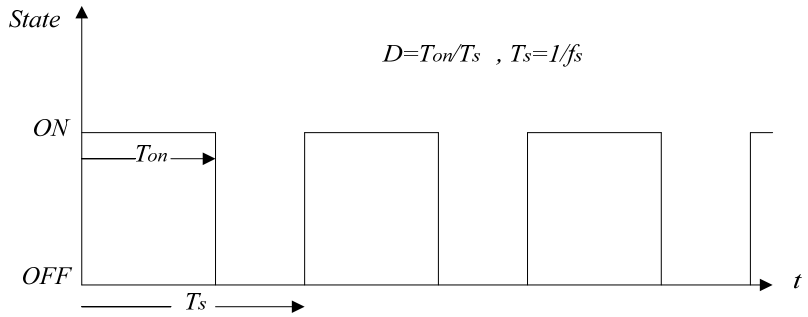


Figure 2.2: Duty cycle of a switch

The biasing of the switches depends on the difference of the Thevenin's equivalent voltages of the external networks connected on the left and right sides of the converter.

If the gates are reverse biased while supplied with the switching pulses, there will be no current flow and the input-output voltage relations given by equations (2.3) and (2.4) will no more hold true.

Since the step-down and step-up converters transfer power only to the left and to the right sides respectively, it would be possible to combine the two to make a bidirectional DC to DC converter as shown in Figure 2.3.

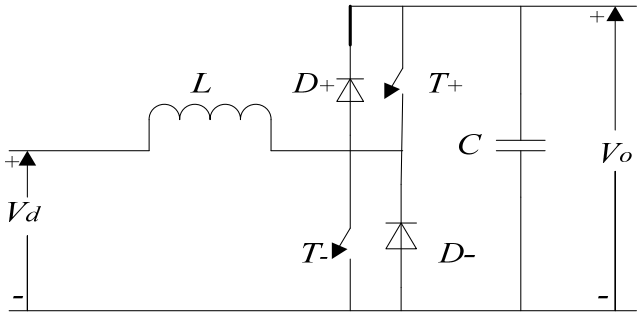


Figure 2.3: Bidirectional DC-DC converter

Equations (2.3) and (2.4) must be equal for continuous bidirectional power conversion.

$$\begin{aligned} V_d &= D_1 V_o \\ &= (1 - D_2) V_o \\ \rightarrow D_2 &= 1 - D_1 \end{aligned} \tag{2.5}$$

Equation (2.5) indicates that T_+ and T_- are complementary; meaning when T_+ is in ON-state T_- will be in OFF-state and vice versa. Hence only one PWM signal generator is needed for both switches of the bidirectional converter.

After rearranging the switches and splitting the DC capacitor into two, we get the following topology shown in Figure 2.4.

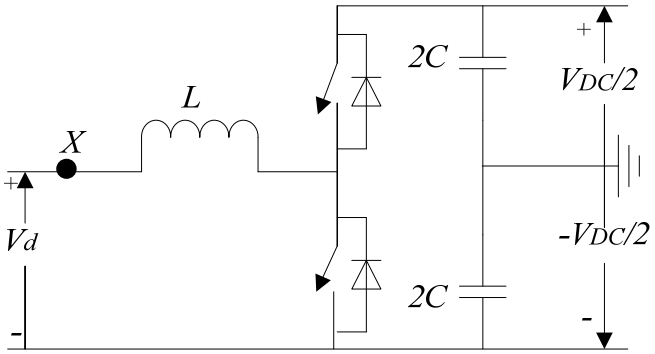


Figure 2.4: Rearrangement of the bidirectional DC-DC converter

We define the phase voltage as the voltage of point X with reference to the ground.

$$\begin{aligned} V_{ph} &= V_d + \frac{-V_{DC}}{2} \\ &= D_1 V_{DC} + \frac{-V_{DC}}{2}, \qquad 0 \le D_1 \le 1 \\ &= (2D_1 - 1)\frac{V_{DC}}{2} \end{aligned} \tag{2.6}$$

Assigning $K=2D_1 - 1$,

$$V_{ph} = \frac{KV_{DC}}{2}, \qquad -1 \le K_1 \le 1 \tag{2.7}$$

By varying the constant K, it is possible to interface different levels of DC voltages of the same or opposite polarities for bidirectional power flow.

If we now replace the constant K with a sinusoidal function of variable amplitude, we can get sinusoidal phase voltage (V_{ph}).

$$K = m_a \sin(wt), \qquad 0 < m_a \le 1 \tag{2.8}$$

In time domain,

$$V_{ph} = \frac{V_{DC} m_a \sin(wt)}{2} \tag{2.9}$$

And in phasor domain,

$$\hat{V}_{ph} = \frac{m_a V_{DC}}{2\sqrt{2}} \angle 0^o , \tag{2.10}$$

Where m_a is the amplitude modulation ratio and is between 0 and 1.

The bidirectional converter together with the sinusoidal PWM consist the *half bridge single phase switch mode converter* [3]. Three of the half bridge single phase converters connected in parallel and with sinusoidal modulation signals of 120^o apart from each other constitute the *three phase switch mode converter*, also known as *Voltage Source Converter* (VSC).

The phrase '*Voltage Source*' refers to the fact that the polarity of DC voltage in VSC is fixed for both rectifier and inverter mode of operations. For thyristor based converters, it is the polarity of current which is fixed for both modes of operations. The three phase bidirectional converter (VSC) is shown in Figure 2.5.

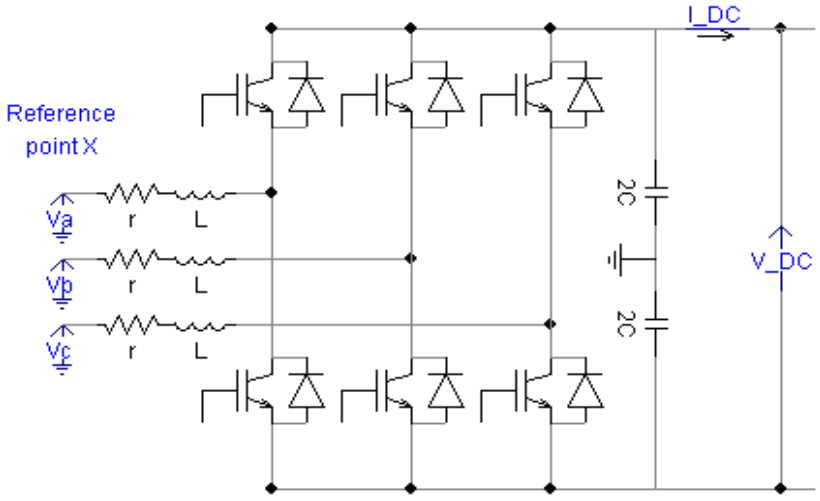


Figure 2.5: Voltage sourced converter

The ratio of the frequency of the modulating signal (f_s) to that of the frequency of fundamental AC component (f_1) is called frequency modulation ratio (m_f) and is given by:

$$m_f = \frac{f_s}{f_1} \tag{2.11}$$

If this ratio is small (<21), m_f must be chosen to be an odd integer in order to get an odd symmetry ($f(-t) = -f(t)$) as well as half wave symmetry ($f(-t) = -f(t + T_1/2)$), where $T_1 = 1/f_1$. By doing so only odd harmonics of sine terms will be found in the phase voltages of the VSC.

In three phase systems, only harmonics in the line-to-line voltages are of concern. Considering the m_f^{th} harmonic, the phase difference between harmonics in phase A and phase B is ($m_f * 120^o$). Choosing m_f as a multiple of three will make this phase difference equivalent to zero (a multiple of 360^o). The same treatment applies for the $m_f +/- j$, harmonics with j = *odd positive integer*. Choosing $m_f = 3$ will create harmonics near to the fundamental frequency and result in very large voltage distortions. Hence the minimum recommended value for m_f is 9. The zero sequence harmonics occurring in the phase voltages are usually eliminated by a Δ connected or ungrounded Y connected transformer. The transformer is usually an integral part of VSC-HVDC and contributes to the series inductance (L filter) needed for AC current smoothening.

For very large values of m_f (>21) the sub-harmonics due to asynchronous modulation will be small and m_f can be assigned non-integral values.

2.3 PWM Techniques

There are several PWM techniques used for VSCs. The simplest one, which also was assumed in previous discussions about VSC, is the pure sinusoidal PWM.

2.3.1 Sinusoidal PWM

Sinusoidal PWM generates pulse width modulated signal by comparing the instantaneous magnitude of a triangular waveform with sinusoidal input reference. This is shown in Figure 2.6.

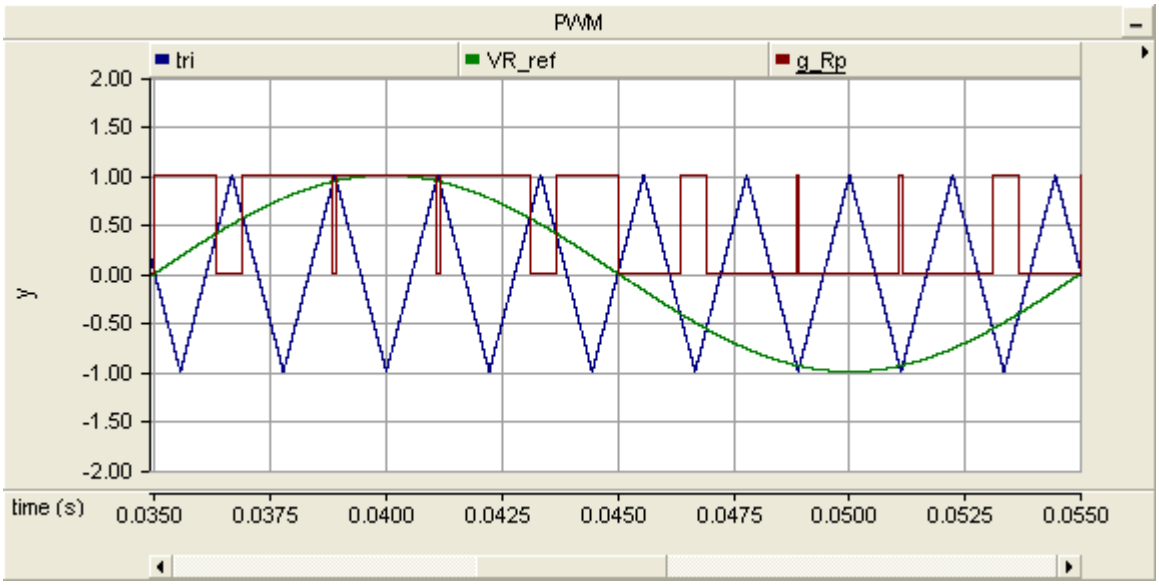


Figure 2.6: Pure sinusoidal PWM with $m_f=9$

Optimized PWM (OPWM), Space Vector - PWM (SVPWM) and Sinusoidal PWM with Third Harmonic Injection are other types of PWM techniques used for VSCs.

2.3.2 Optimized PWM

This is used for selective harmonic elimination by pre-calculated waveform of PWM. It can also be arranged to minimize the number of switchings around the instant of maximum current flow. This results in reduction of power loss as compared with the simple triangular carrier wave PWM, but also has the disadvantage of computational complexity and variable switching frequency changing with operating conditions.

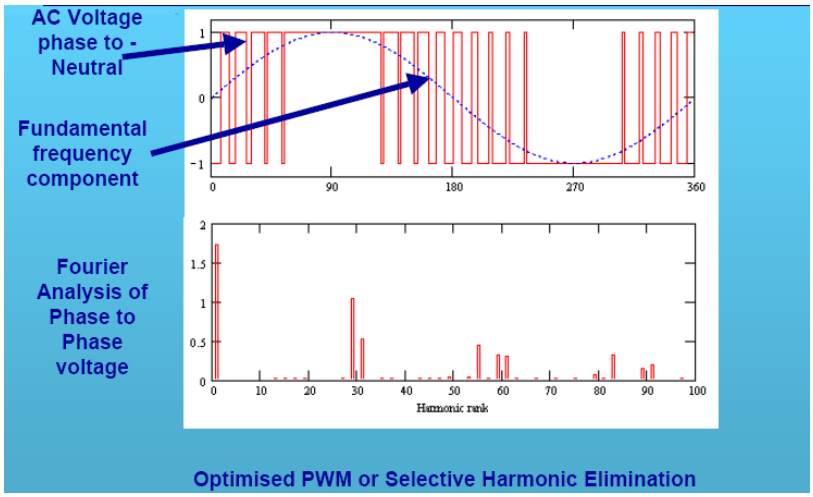


Figure 2.7: Harmonic spectrum of optimized PWM [7]

2.3.3 Space Vector PWM (SVPWM)

This type of modulation has an objective of minimizing the number of switchings there by reducing switching losses. SVPWM also results in better utilization of the DC bus by increasing the available output voltage by approximately 15% (i.e. to $U_{DC}\sqrt{3}/2$) compared to the sinusoidal PWM, which gives a maximum phase voltage amplitude of $U_{DC}/\sqrt{2}$ [5]. In this type of modulation the reference voltage is mapped into switching space vector diagram and the duty cycles of the switches will be calculated based on the mapping.

Table 2.2 Table of IGBT Switchings

Output Voltage Vector	Status of Switches		
	T_{A+}	T_{B+}	T_{C+}
U_0	1	0	0
U_{60}	1	1	0
U_{120}	0	1	0
U_{180}	0	1	1
U_{240}	0	0	1
U_{300}	1	0	1

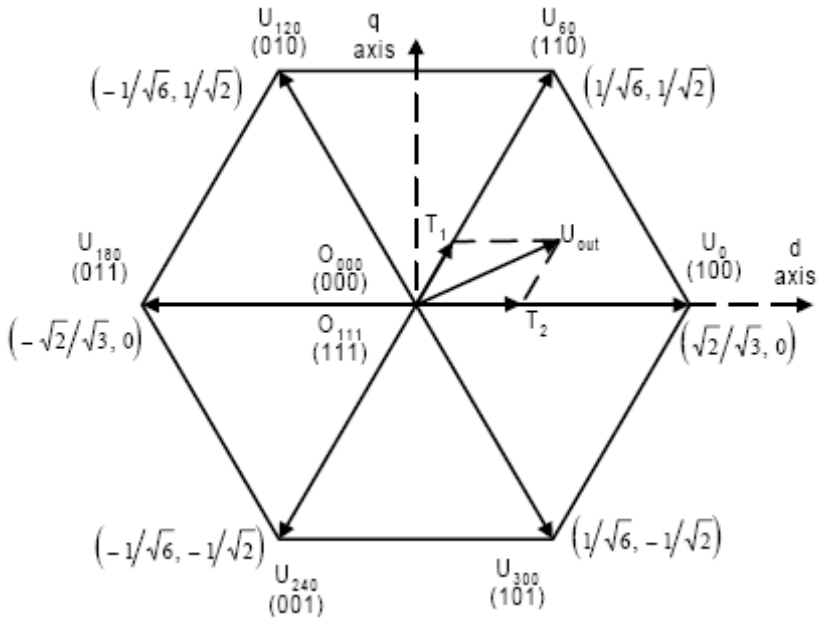


Figure 2.8: Switching map of SVPWM

U_{out} in Figure 2.8 indicates the required output voltage phasor in d-q reference frame. In order to calculate the duty ratios of the voltage vectors that generate U_{out}, the sector where U_{out} lies should first be identified. Once this sector is found, the duty cycles are calculated from the voltage-time balance during one switching period (T_w).

When U_{out} lies in the first sector ($0<\theta<60^o$):

$$\begin{aligned} T_{sw}U_{out}e^{j\theta} &= T_{sw}(d_0 0 + d_1U_0 + d_2U_{60}) \\ &= T_{sw}\frac{U_{DC}}{2}(d_1 + d_2e^{j\pi/3}) \end{aligned} \quad , \qquad d_0 + d_1 + d_2 = 1 \qquad (2.12)$$

where d_0, d_1 and d_2 are duty cycles of 0, U_0 and U_{60} voltage vectors.

Equating the direct and quadrature axis components,

$$U_{out}\cos\theta = d_1 U_0 + \frac{1}{2}d_2$$
$$U_{out}\sin\theta = \frac{\sqrt{3}}{2}d_2 \qquad (2.13)$$

Hence,

$$d_2 = \frac{2}{\sqrt{3}}U_{out}\sin\theta$$
$$d_1 = \frac{1}{\sqrt{3}}U_{out}(\sqrt{3}\cos\theta - \sin\theta) \qquad (2.14)$$
$$d_0 = 1 - d_1 - d_2$$

The corresponding switching patterns are shown in Figure 2.9.

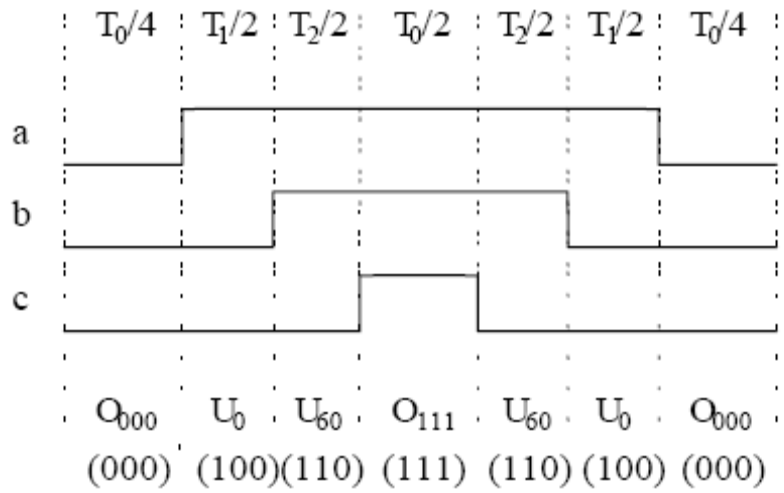


Figure 2.9: Switching pattern for U_{out} in $U_0 - U_{60}$

2.3.4 Sinusoidal PWM with Third Harmonic Injection

This type of PWM uses injection of third harmonics in to all the three phases to increase the size of maximum available line to line voltage vector.

2.4 Two Level and Multilevel Converters

The VSC considered so far has only two levels of instantaneous AC voltage (i.e. $+U_{DC}$ and $-U_{DC}$). Hence this type of VSC is called a two level VSC as opposed to multilevel VSCs that have more than two instantaneous voltage levels.

Multilevel converters have the advantages of [7]:

1. Fewer switching operations for similar harmonic performance
2. Lower voltage per switches
3. Lower power loss

The switching patterns for two level and three level converters are shown in Figure 2.10 below.

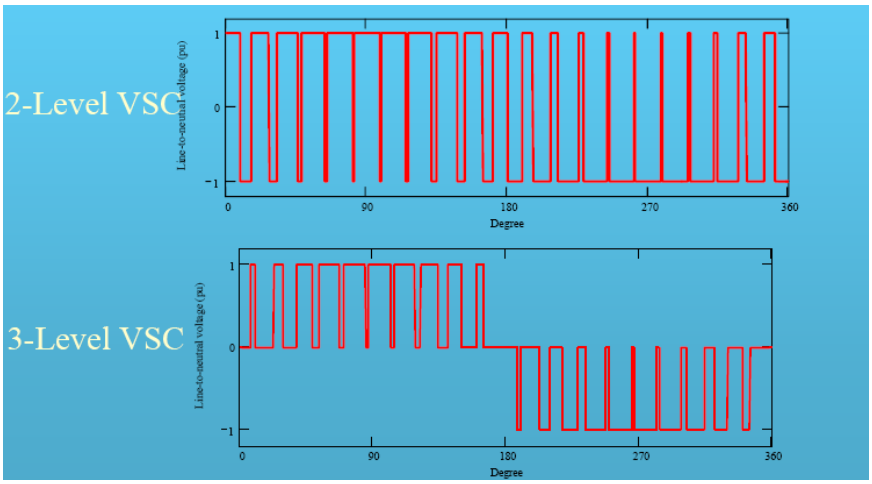


Figure 2.10: Switching patterns for two-level and three-level VSCs respectively [7]

There are three topologies of multilevel converters, namely: diode clamped, flying capacitor clamped and cascaded multilevel converters. The following diagram depicts these three topologies of multilevel VSCs.

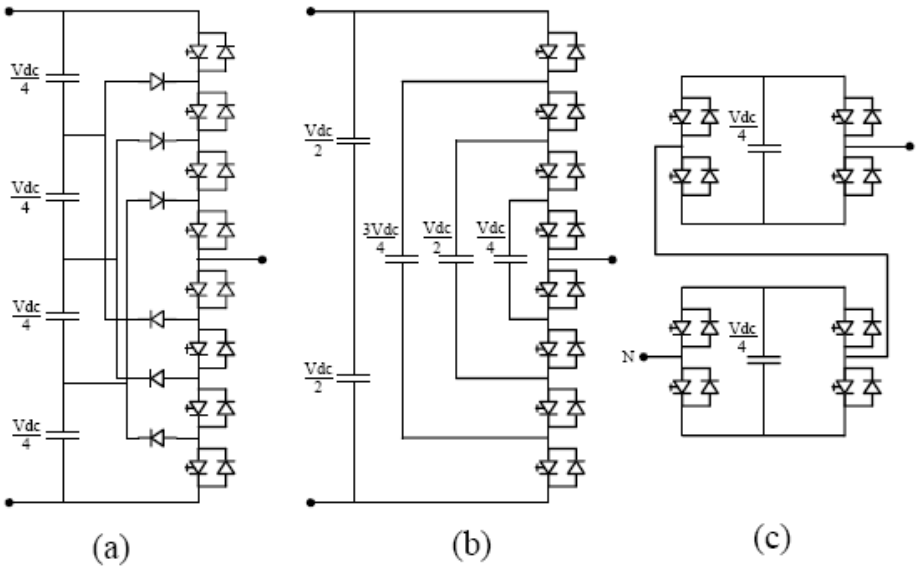


Figure 2.11: One-leg five-level multilevel topologies: a. Diode clamped, b. Flying capacitor clamped, c. Cascaded H-bridges

Detailed comparisons of the advantages and disadvantages of the different topologies of multilevel VSCs are discussed in literature [6].

Chapter Three

Modeling of Multiterminal VSC-HVDC System

3.1 Introduction

VSCs have vast areas of applications ranging from small electric drive systems to high voltage DC transmission systems (referred in this paper as VSC-HVDC). VSC has two degrees of freedom, namely the amplitude modulation index (m_a) and the phase displacement (φ). In comparison, thyristor based converter has only one degree of freedom, i.e. the firing angle (α). Degree of freedom refers to the number of independently alterable parameters and is an indication of the maximum number of independently controllable output quantities. This higher flexibility together with its fixed voltage polarity for both rectifier and inverter modes of operation make VSC-HVDC the core component in developing MTDC. This chapter discusses design of VSC-HVDC, features of MTDC, types AC buses, and also establishes methodologies to be used in modeling of MTDC system.

3.2 Design of VSC-HVDC

The VSC-HVDC that will be considered in this paper is a two level VSC with pure sinusoidal PWM. Although in practice a converter leg consists of a package of several semiconductors connected in series and in parallel, in the VSC modeling of this paper single IGBT and diode components with very high voltage ratings will form the anti-parallel connections. In addition protection circuits (Snubbers) are not considered in the VSC models.

Design specifications will be made for one VSC and will be used for all VSC-HVDC terminals throughout this thesis work. It should be noted that although the same VSC-HVDC design will be

used consistently, different control strategies will be employed depending on the requirement for control objective at hand. Configuration of VSC-HVDC is shown in Figure 3.1.

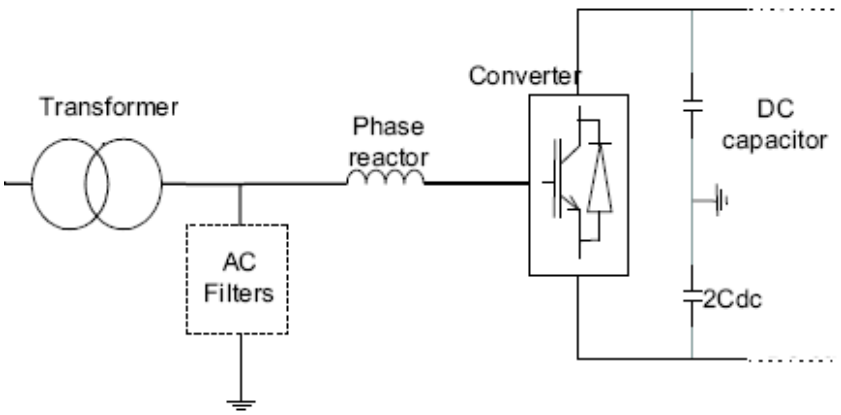


Figure 3.1 Configuration of VSC-HVDC

Current Smoothening Inductance (L filter)

As it was discussed in Chapter 2, a series inductance is used for smoothening of the phase currents. The inductance is calculated as.

$$L = Max(\frac{V_h}{h\omega_o I_h}) \tag{3.1}$$

where V_h is harmonic voltage determined from voltage harmonic table for sinusoidal PWM, I_h is the amount of acceptable harmonic current and h is the harmonic number.

Transformer

Usually, the converters are connected to the AC system via transformers. The transformer has the main purpose of transforming the AC voltage in to a level suitable to the converter. Transformers usually have a leakage inductance between 0.1 - 0.2 p.u. [4].

Phase reactors

Part of the series phase inductance required comes from the transformer (if there is any) and the rest of it is provided by series connected phase reactors.

AC filters

In addition to the series inductance, AC filters can be used to eliminate the voltage harmonics entering into the AC system. The AC filter is a shunt connected high pass filter tuned in the order of the PWM frequency.

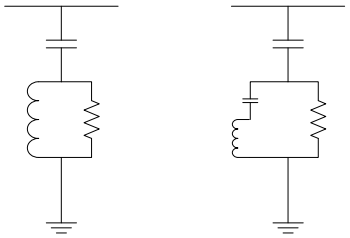


Figure 3.2: Passive high pass filters: a. Second order filter b. Third order filter

DC Capacitors

The use of PWM in VSC results in current harmonics occurring in the DC side of the VSc-HVDC. These current harmonics in turn causes ripple on the DC side voltage. The use of shunt connected capacitor filters out such ripple and results in smoother DC voltage.

While on one hand the use of DC capacitors improves the steady state performance, the dynamic response during disturbances (fault occurrence, load switching) will suffer if capacitors of too large size are used. Therefore both steady state and dynamic response performances should be considered in selecting the size of the DC capacitor.

Hence a time constant, defined as the ratio of the energy stored in the capacitor at rated DC voltage to the rated apparent power of the converter is used for specifying the capacitor size [4].

$$\tau = \frac{CU_{DC}{}^2}{2S_n} \tag{3.2}$$

Taking the speed of current controllers (which are fastest of all controllers in the VSC-HVDC)

into consideration, a time constant of not less than 5 ms was suggested in literature [4].

DC Cables

The shunt capacitance, shunt resistance and series inductance of the DC cables are neglected. Only the series resistance of the DC cable is modeled as a lumped resistive element.

3.2 MTDC Feature Development

Before starting with modeling of MTDC, it is necessary to describe the expected basic features of MTDC system.

An MTDC is expected to consist of several VSC-HVDC terminals connected to each other by DC network. The MTDC should work with a fixed DC voltage level or with in a small window of upper and lower limits. Each of the terminals should be able to adopt different control strategy depending upon terminal specific needs. VSC-HVDC should monitor and control DC side parameters as well as AC side parameters.

3.2.1 DC bus parameter control

On the DC side, the VSC-HVDC may operate in constant DC voltage mode, constant power mode, or constant DC current mode [8]. When the VSC-HVDC is supplying power to passive load, none of the DC parameters is controlled.

3.2.2 AC bus parameter control

On the AC side, the VSC-HVDC may operate in constant AC voltage mode or constant reactive power mode depending on the type of the grid connection. Frequency droop can also be added optionally in the AC bus control.

3.3 Types of AC Networks

AC networks are classified as strong (stiff) grid, weak grid and passive network depending on the stiffness of the AC voltage at the point of common coupling (PCC).

When an AC connection is said to be stiff grid, it means that the AC voltage at the PCC remains constant irrespective of the magnitude and direction of active and reactive power flow.

Weak grid on the other hand has its AC voltage at PCC changing with power flow. This happens due to significant resistive voltage drop across transmission line and is usually associated with long transmission lines.

The AC voltage in passive network is totally dependent on the voltage output of the VSC, hence the name passive network.

In this paper stiff grid is modeled by ideal three phase AC source with constant voltage where as weak grid is represented by ideal three phase AC source in series with line inductance and resistance. Passive network is modeled by resistive and inductive loads.

3.4 VSC-HVDC Terminal Control Configurations

The maximum possible number of controllable output quantities depends on the number of available degrees of freedom. The parameters to be controlled at a terminal should be capable decoupling or at least should be weakly correlated. As discussed before there are three types of AC grid connections, namely passive network, weak grid and stiff grid systems. According to the characteristics of the AC network, VSC-HVDC terminals can be classified in to two major categories.

a. VSC-HVDC for Passive AC network

When the VSC-HVDC is the only source in the AC network it is connected to, the network is said to be passive network. In this type of network connection, the only control objective of the VSC-HVDC is to maintain constant AC line-line voltages.

b. VSC-HVDC for Active AC Network

When VSC-HVDC is connected to active AC network, like in the passive network case, AC voltage at PCC should be kept constant. If the AC connection is stiff grid, the AC voltage level will be constant (stiff) by itself and the VSC-HVDC terminal controls reactive power flow from

the AC side. On the other hand if the connection at PCC is a weak grid connection, the AC voltage should be controlled by reactive power compensation. By considering weak and stiff grids types of connections and constant active power or constant DC voltage control modes, we can get four different control modes of VSC-HVDC terminals, i.e. constant P-V_{AC} terminal, constant V_{AC}-U_{DC} terminal, constant P-Q terminal, and constant Q-U_{DC} terminal.

Hence, the different control modes in passive and active network connections give rise to five possible types of VSC-HVDC terminals.

Type 1: Constant AC voltage for passive network (V_{AC} control)

When feeding power to passive network, the control objective becomes to maintain a constant level of AC voltage at the point of common coupling (PCC). The active and reactive power flows is dependent on the passive network components and therefore are not decoupled. Since there is only one source of AC voltage, there will be no need for frequency control.

Type 2: Constant P- V_{AC} control

P-V_{AC} control is applied when the VSC-HVDC terminal is connected to a weak grid while constant power flow is needed. Since the AC voltage of a weak grid is not constant by itself, it should be maintained to a constant level by the VSC. Active power flow controller maintains constant power flow via the HVDC. The reference input for the power controller may come from a central power dispatching station or can be manually set by operators at site.

Type 3: V_{AC} - U_{DC} control

This is used when VSC-HVDC connected to a weak grid is required to maintain constant DC voltage level. The AC voltage as well as the DC voltage must be regulated by the VSC. As will be shown later on, AC voltage is controlled by reactive power compensation and DC voltage is regulated by active power compensation.

Type 4: P-Q control

This is used when a stiff AC grid is connected to the VSC-HVDC and when constant power control mode is required. Active and reactive powers have their own references and will be

independently controlled. If there is no requirement for control of reactive power flow, Q_{ref} will be assigned a value of zero.

Type 5: Q- U_{DC} control

When the VSC-HVDC terminal is connected to a stiff network and is required to regulate DC voltage, constant Q-U_{DC} mode of control is applied. The generated reactive power will be transported by the stiff grid for consumption at some other site in the AC network.

Frequency control

The Phase lock Loop (PLL) of VSC-HVDC is normally phase locked with the AC voltages and hence is not disturbed by small frequency changes in the AC system. Similarly the power and voltage controllers do not have natural frequency droop characteristics. But by including a frequency bias factor, the VSC-HVDC terminal can be made to contribute for the aggregated frequency droop characteristics of the AC system.

3.5 Synchronous *d-q* Reference Frame

The use of synchronously rotating d-q rotating frame allows decoupled control of active and reactive power flows. The basis for transforming three phase system into a two phase system lies on emulating them as virtual fluxes and representing the three space vectors with equivalent two space vectors that give the same resultant in the course of time [9]. It is assumed that the system under treatment is three phase balanced. Mathematically,

$$X_a + X_b + X_c = 0 \tag{3.3}$$

where X is a phase voltage or phase current space vector

The phase transformation from stationary *abc* to stationary *α-β* frame of reference is given by Clark transformation equation:

$$X_{\alpha\beta} = X_\alpha + jX_\beta = k\left[X_a + X_b e^{j\frac{2\pi}{3}} + X_c e^{j\frac{4\pi}{3}} \right] \tag{3.4}$$

where k is a constant number.

abc and *α-β* reference frames are given shown in Figure 3.3 below.

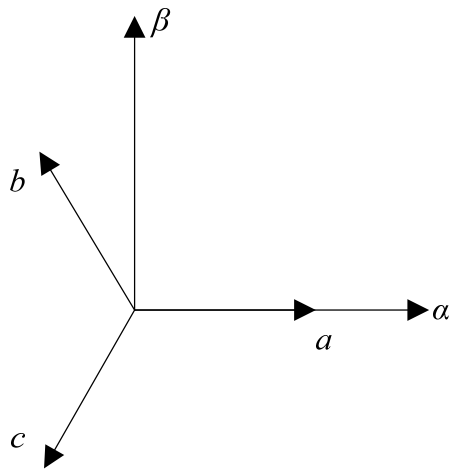


Figure 3.3: Stationary *abc* and *α-β* reference frames

In matrix form Clark transformation is given by equation 3.5.

$$\begin{bmatrix} X_\alpha \\ X_\beta \end{bmatrix} = k \begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} X_a \\ X_b \\ X_c \end{bmatrix} \tag{3.5}$$

α-β to *d-q* reference frames transformation is given by Park transformation as in equation (3.6).

$$X_{dq} = X_{\alpha\beta} e^{-j\theta} \tag{3.6}$$

Expanded matrix form of Park transformation is obtained as:

$$\begin{bmatrix} X_d \\ X_q \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} X_\alpha \\ X_\beta \end{bmatrix} \tag{3.7}$$

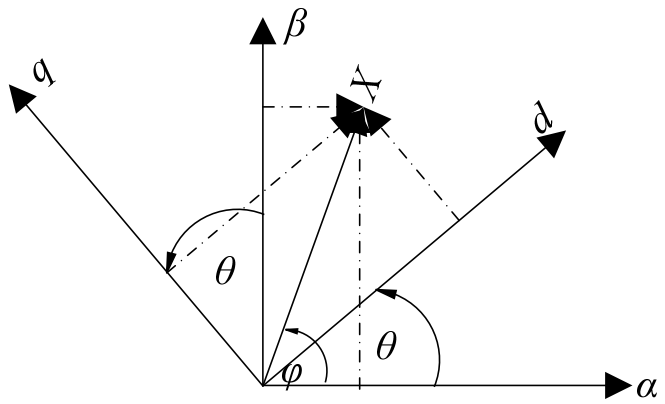


Figure 3.4 Stationary (*α-β*) and rotating (*d-q*) reference frames

Direct *abc* to *d-q* transformation is given by [10]:

$$\begin{bmatrix} X_\alpha \\ X_\beta \end{bmatrix} = k \begin{bmatrix} \cos\theta & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ -\sin\theta & -\sin(\theta - \frac{2\pi}{3}) & -\sin(\theta + \frac{2\pi}{3}) \end{bmatrix} \begin{bmatrix} X_a \\ X_b \\ X_c \end{bmatrix} \tag{3.8}$$

θ is the transformation angle and equal to ωt where ω is electrical frequency in *rad/s* of the AC system under consideration. Substituting for voltage and current phasors;

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = k \begin{bmatrix} \cos\theta & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ -\sin\theta & -\sin(\theta - \frac{2\pi}{3}) & -\sin(\theta + \frac{2\pi}{3}) \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \tag{3.9}$$

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = k \begin{bmatrix} \cos\theta & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ -\sin\theta & -\sin(\theta - \frac{2\pi}{3}) & -\sin(\theta + \frac{2\pi}{3}) \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{3.10}$$

If k is taken as $\sqrt{2/3}$, the power calculated in the d-q reference frame will have the same magnitude as the power calculated from *abc* reference frame [10] and the transformation is said to be *power invariant*. The complete power invariant transformation matrix and inverse matrix are shown below.

$$\begin{bmatrix} X_\alpha \\ X_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos\theta & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ -\sin\theta & -\sin(\theta - \frac{2\pi}{3}) & -\sin(\theta + \frac{2\pi}{3}) \end{bmatrix} \begin{bmatrix} X_a \\ X_b \\ X_c \end{bmatrix} \tag{3.11}$$

$$\begin{bmatrix} X_a \\ X_b \\ X_c \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos\theta & -\sin\theta \\ \cos(\theta - \frac{2\pi}{3}) & -\sin(\theta - \frac{2\pi}{3}) \\ \cos(\theta + \frac{2\pi}{3}) & -\sin(\theta + \frac{2\pi}{3}) \end{bmatrix} \begin{bmatrix} X_\alpha \\ X_\beta \end{bmatrix} \tag{3.12}$$

On the other hand if *k=2/3* is chosen, the amplitude of the phase voltages in both *d-q* and *abc* reference frames will be the same and the transformation is said to be *voltage invariant*. The complete transformation matrix and inverse matrix for voltage invariant transformation are given by:

$$\begin{bmatrix} X_\alpha \\ X_\beta \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos\theta & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ -\sin\theta & -\sin(\theta - \frac{2\pi}{3}) & -\sin(\theta + \frac{2\pi}{3}) \end{bmatrix} \begin{bmatrix} X_a \\ X_b \\ X_c \end{bmatrix} \tag{3.13}$$

$$\begin{bmatrix} X_a \\ X_b \\ X_c \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \cos(\theta - \frac{2\pi}{3}) & -\sin(\theta - \frac{2\pi}{3}) \\ \cos(\theta + \frac{2\pi}{3}) & -\sin(\theta + \frac{2\pi}{3}) \end{bmatrix} \begin{bmatrix} X_\alpha \\ X_\beta \end{bmatrix} \quad (3.14)$$

In this thesis work, voltage invariant Park and inverse Park transformations will be used.

3.6 Phase Lock Loop

If the VSC-HVDC is connected to passive network, there will be only one source of AC voltage (i.e. the VSC-HVDC terminal itself) and there will be no issue of synchronization. The PWM of VSC-HVDC in passive network gets its sinusoidal signal from fixed frequency oscillator circuit. For all the other cases, where the VSC-HVDC terminal is connected to active AC system, frequency and phase must be detected at the reference point X and the converter should be synchronized accordingly. This action is performed by phase lock loop (PLL) circuit.

PLL is a circuit that synchronizes a local oscillator with a reference sinusoidal input. This ensures that the local oscillator is at the same frequency and in phase with the reference input. The local oscillator is voltage controlled oscillator (VCO). The block diagram of a PLL is shown in Figure 3.5.

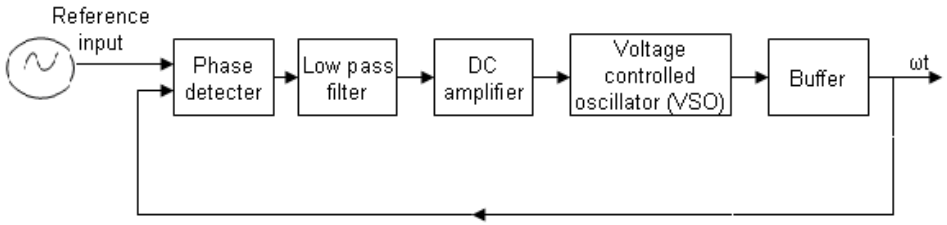


Figure 3.5: Block diagram of phase lock loop (PLL)

One type of PLL called DQZ type is shown in Figure 3.6 [13].

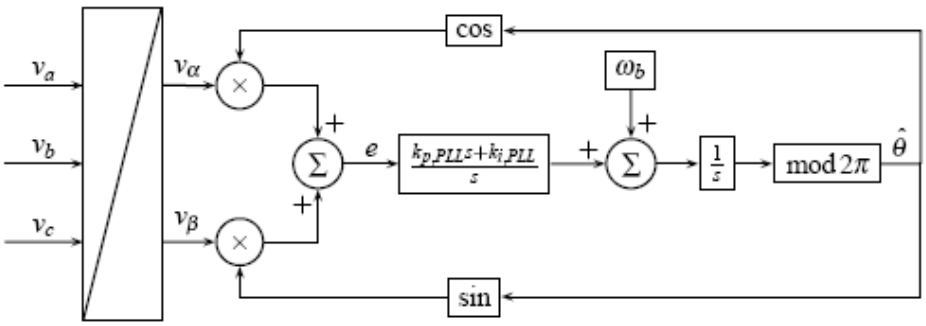


Figure 3.6: DQZ Type of PLL

The PLL is phase locked to phase-A of the AC voltage at reference point (X) and provides the angle of transformation (ωt) for Park and inverse Park transformation matrices.

3.7 P.U. System

Per unit (p.u.) system makes comparison of systems with different ratings easier. But more than this, with the use of p.u. it is easier to design and implement the controllers of the VSC-HVDC.

The p.u. system is based on name plate ratings for power, peak values of rated phase current and voltage [9]. By doing so, the rated current and voltage in the transformed *d-q* reference frame will be unity. The base quantities used for to p.u. conversions are given below.

$$
\begin{aligned}
V_{d,b} &= V_{q,b} = \sqrt{\frac{2}{3}} V_n \\
I_{d,b} &= I_{q,b} = \sqrt{2} I_n \\
Z_{d,b} &= \frac{V_{d,b}}{I_{d,b}} = \frac{V_n}{\sqrt{3} I_n} = Z_n \\
S_{d,b} &= \frac{2}{3} S_n \\
S_{DC} &= S_n = \sqrt{3} V_n I_n = \frac{3}{2} V_{d,b} I_{d,b} \\
I_{DC,b} &= \frac{S_{DC}}{V_{DC,b}} = \frac{3}{4} I_{d,b} = \frac{3\sqrt{2}}{4} I_n \\
Z_{DC,B} &= \frac{V_{DC,b}}{I_{DC,b}} = \frac{8}{3} Z_{d,b} = \frac{8}{3} Z_n
\end{aligned}
\qquad (3.15)
$$

3.7 Convention for Direction of Current and Power Flow

Using a consistent rule for defining positive and negative directions for current and power flows makes understanding the overall system operation easier. In this paper AC current and AC power will have positive value if each is going away from the VSC-HVDC at the point of common coupling. Similarly, DC-current and power are assumed to be positive for when they are flowing away from the VSC-HVDC at the reference point for DC measurements.

Chapter 4

Control Strategy

In this chapter the details of the controls for the different modes of VSC-HVDC operation, mentioned in the previous chapter, will be discussed. It is assumed that there is only positive sequence component in the AC networks interfaced with the MTDC through the VSC-HVDC terminals. It is also considered that the VSC-HVDC terminals operate only in the linear modulation range and are not over modulated.

4.1 Equivalent Circuit of VSC-HVDC in Synchronously rotating d-q reference frame

Schematic of a VSC-HVDC terminal is shown in Figure 4.1.

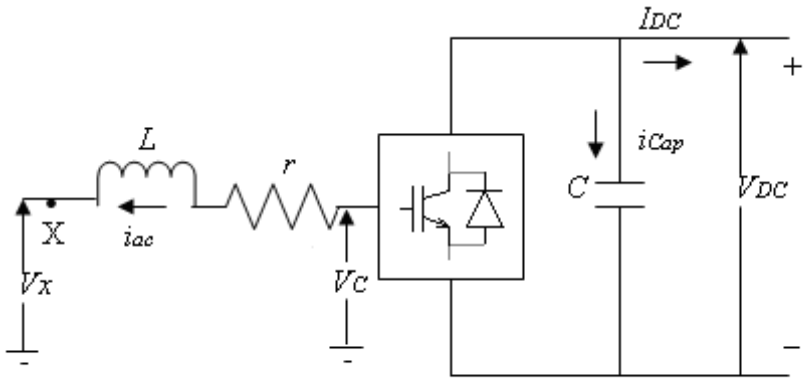


Figure 4.1: Schematic of a VSC-HVDC terminal

L and *r* represent the total inductance and resistance coming from transformer and phase reactor. Point *x* is the point of common coupling (PCC) of the VSC-HVDC and the AC system. This is the reference point for measuring AC quantities and also for the PLL. *c* is the reference point for converter output voltage.

Applying Kirchoff's Voltage Law (KVL) across *x*-*c*:

$$U_{x,abc} - U_{c,abc} = r i_{abc} + L \frac{di_{abc}}{dt} \tag{4.1}$$

Applying voltage invariant Clark transformation:

$$U_{x-\alpha\beta} - U_{c-\alpha\beta} = r i_{\alpha\beta} + L \frac{di_{\alpha\beta}}{dt} \tag{4.2}$$

From Park's transformation [5]:

$$\begin{aligned} U_{x-\alpha\beta} &= U_{x-dq} e^{j\omega t} \\ U_{c-\alpha\beta} &= U_{c-dq} e^{j\omega t} \\ i_{\alpha\beta} &= i_{dq} e^{j\omega t} \end{aligned} \tag{4.3}$$

where ω is frequency of the fundamental component in AC network.

Substituting equation (4.3) in equation (4.2):

$$U_{x-dq} e^{j\omega t} - U_{c-dq} e^{j\omega t} = r i_{dq} e^{j\omega t} + L \frac{d(i_{dq} e^{j\omega t})}{dt} \tag{4.4}$$

Dividing all terms by $e^{j\omega t}$;

$$U_{x-dq} - U_{c-dq} = r i_{dq} + j\omega L i_{dq} + L \frac{di_{dq}}{dt} \tag{4.5}$$

The expanded form of equation (4.5), after rearranging, will be:

$$L \frac{d}{dt} \begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} U_{xd} \\ U_{xq} \end{bmatrix} - \begin{bmatrix} U_{cd} \\ U_{cq} \end{bmatrix} - r \begin{bmatrix} i_d \\ i_q \end{bmatrix} - \omega L \begin{bmatrix} 0 & 1 \\ -1 & 0 \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} \tag{4.6}$$

$\begin{bmatrix} 0 & 1 \\ -1 & 0 \end{bmatrix}$ is the matrix form of *j* and has an effect of rotating phasors by 90^o.

Base on equation (4.6), the d and q axes equivalent circuits of the VSC-HVDC, as seen from the AC network side, are given by Figure 4.2.

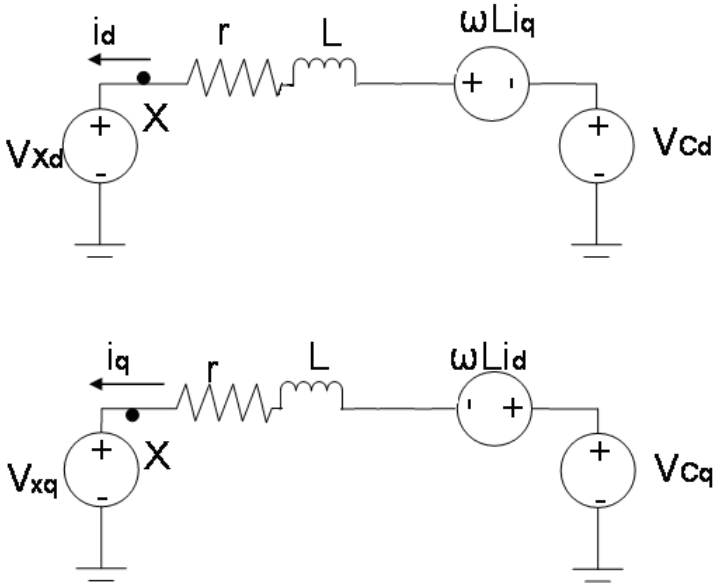


Figure 4.2: d and q axes equivalent circuits of VSC-HVDC

The apparent power exchange observed from reference point *X* and in *d-q* reference frame is given by:

$$\begin{aligned} S_{dq} &= \frac{3}{2} U_{x-dq} i_{dq}^{*} \\ &= \frac{3}{2} (U_{xd} + jU_{xq})(i_d - ji_d) \\ &= \frac{3}{2} \left\{ (U_{xd} i_d + U_{xq} i_q) + j(U_{xq} i_d - U_{xd} i_q) \right\} \end{aligned} \tag{4.7}$$

For a steady state operation, active power exchange at the AC side (at PCC) will be equal to the

power exchange at the DC bus. Mathematically;

$$\begin{aligned} P_{dq} &= P_{DC} \\ \frac{3}{2}(U_{xd}i_d + U_{xq}i_q) &= U_{DC}I_{DC} \end{aligned} \tag{4.8}$$

From equation (4.8), the DC current at steady state becomes:

$$I_{DC} = \frac{P_{dq}}{U_{DC}} = \frac{3(U_{xd}i_d + U_{xq}i_q)}{2U_{DC}} \tag{4.9}$$

The converter as seen from the DC network side will be a constant current source of I_{DC} current.

4.2 Control of VSC-HVDC for Passive Networks

A VSC-HVDC connected to passive network has to maintain constant rms phase voltages for all line currents ranging from no load to full load current. Since there is no decoupling of active and reactive powers here, a simple controller based on phase measurements can be made without the use of *d-q* reference frame. The VSC-HVDC and its reference signal generators will have the structure shown in Figure 4.3.

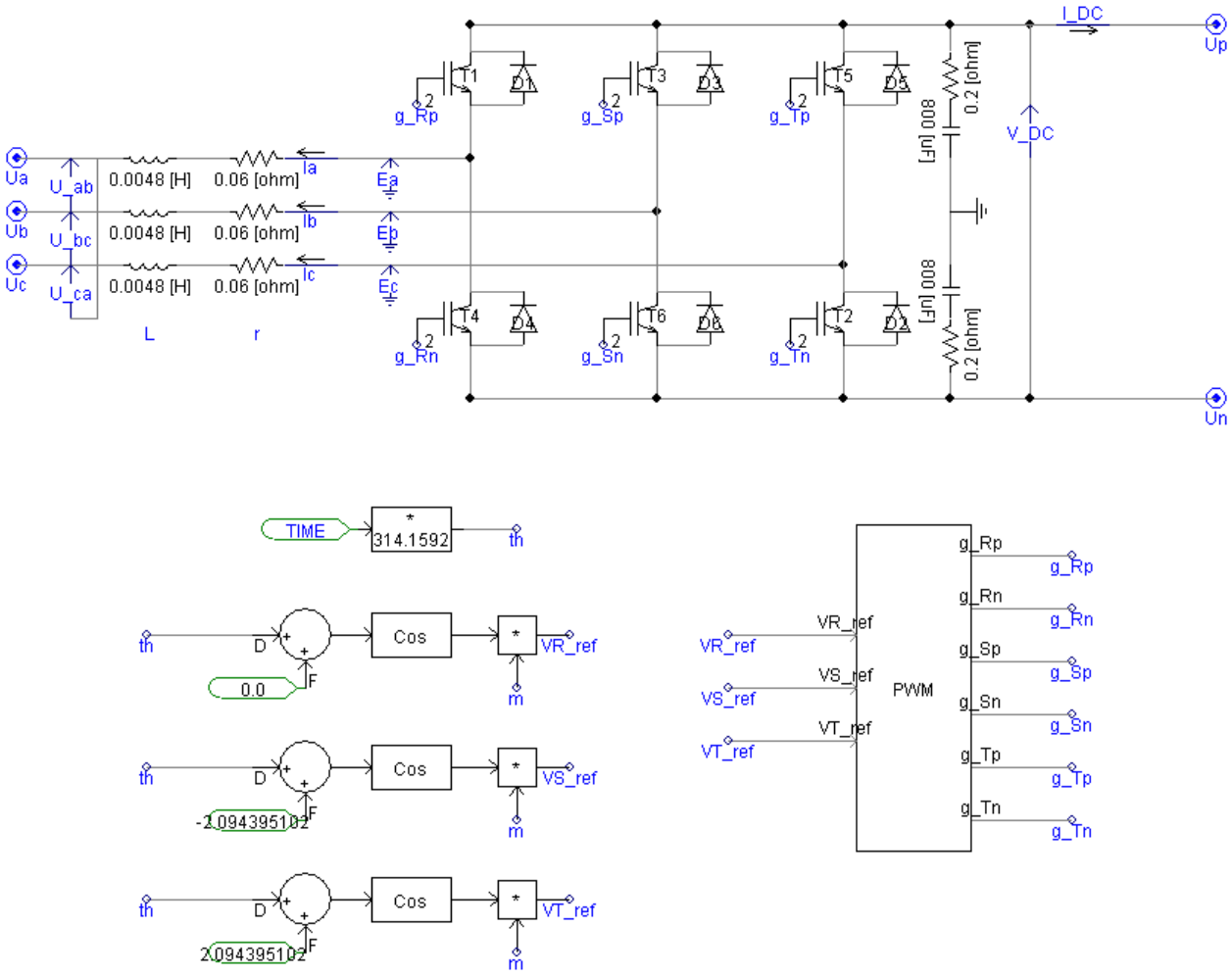


Figure 4.3: *abc* signal generation for voltage references for the PWMs

The per-phase equivalent of the VSC and the AC network can be modeled as in Figure 4.4.

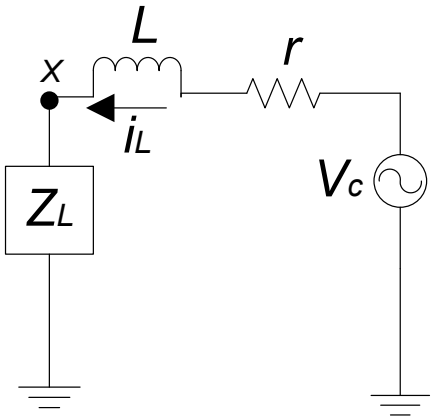


Figure 4.4: Single line diagram of VSC-HVDC

In Figure 4.4 $V_{c,rms}$ is the rms phase voltage output of the converter and Z_L is load impedance. From Chapter 2,

$$V_{c,rms} = \frac{mU_{DC}}{2\sqrt{2}} \tag{4.10}$$

By voltage divide rule, the voltage across the load is given by;

$$\begin{aligned} V_{x,rms} &= \frac{Z_L}{Z_L + (j\omega L + r)} V_{c,rms} \\ &= \frac{Z_L}{Z_L + (j\omega L + r)} \frac{U_{DC}}{2\sqrt{2}} m \end{aligned} \tag{4.11}$$

From equation (4.11), the AC voltage controller will be:

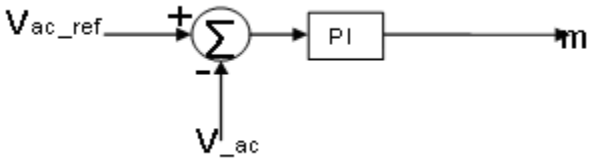


Figure 4.5: AC voltage controller for passive network

4.3 Control of VSC-HVDC Connected to Active AC Network

When active AC network is connected with VSC-HVDC, the use of the space vector in the control design and implementation enables to make a fully decoupled linear control of active and reactive currents.. The *d-q* reference frame is selected in such a way that the d-axis is aligned to the voltage phasor of phase- A of point *X*. This means that the PLL should be phase locked to phase-A voltage phasor of the reference point, *X*. This results in:

$$\begin{aligned} V_{xq} &= 0 \\ V_{xd} &= V_x \end{aligned} \tag{4.12}$$

The simplified VSC equivalent in d-q reference will be as shown in Figure 4.6.

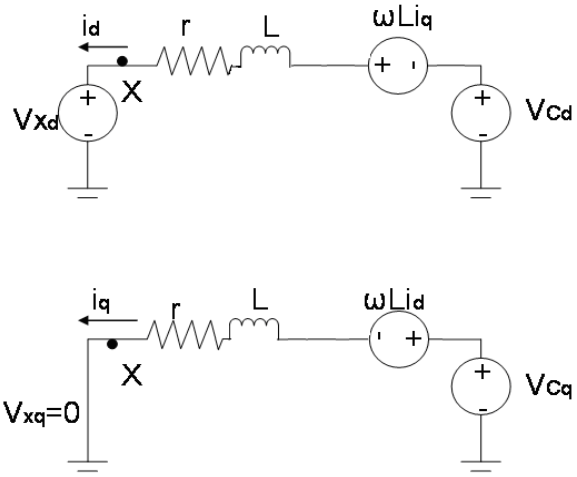


Figure 4.6: Equivalent circuits in *d* and *q* axes of VSC-HVDC for d-axis aligned with voltage phasor of phase-A

From Figure 4.6, the active and reactive powers become:

$$\begin{aligned} P_{dq} &= \frac{3}{2} U_{xd} i_d \\ Q_{dq} &= \frac{-3}{2} U_{xd} i_q \end{aligned} \tag{4.13}$$

a. Inner current controller (Inner current loop)

The inner current controller is developed based upon equation (4.6). Figure 4.7 shows the d-axis and q-axis current controllers of the inner current loop.

The converter has a delay of $e^{-T_w s} \approx 1/(1+T_w s)$ due to the sinusoidal pulse width modulator and $T_w = 1/2f_s$ where f_s is the switching frequency of the converter. Proportional integral (PI) controllers are used for closed loop control and the zeroes of the PI controllers are selected to cancel the dominant pole in the external circuit. For a typical VSC, the time constant $\tau = L/r$ is much higher than T_w and hence will be the dominant pole to be canceled.

The cross coupling currents in equation (4.6) are compensated by feed forward terms in the controllers as shown in Figure 4.7.

i_d* and i_q* are reference currents for the d-axis and q-axis current controllers respectively.

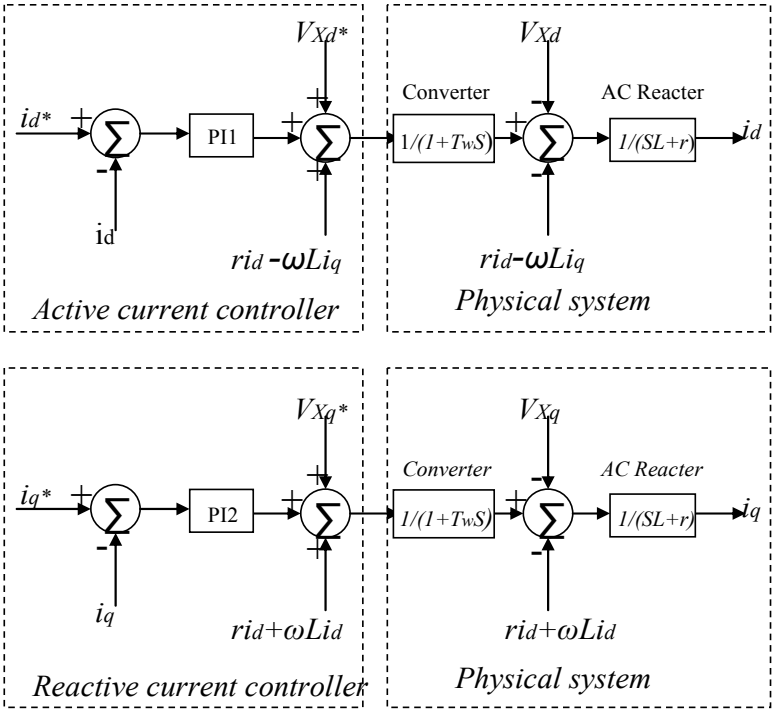


Figure 4.7: Inner current controllers

b. Outer controllers

The outer controllers consist either of AC voltage and reactive power controllers and either of DC voltage or active power controllers. Active current (i_d) is used to control either of active power flow or DC voltage level. Similarly, the reactive current (i_q) is used to control either of reactive power flow into stiff grid connection or AC voltage support in weak grid connection.

4.3.1 Active Power Control

The apparent active power flow is given by equation (4.13) and from equation (4.12);

$$V_{xd} = V_x \tag{4.14}$$

Where V_x is resultant voltage in d-q reference frame and is desired to have constant value. Hence active power flow can be controlled by active current (i_d) and the active power controller is given by Figure 4.8.

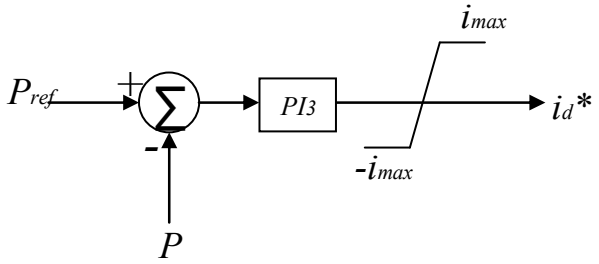


Figure 4.9: PI controller for active power control

The output of the active power controller (i_d^*) will be the reference input to the d-axis current controller of the inner current loop in Figure 4.7.

In order to limit the magnitude of current in the VSC HVDC to a maximum limit, the output of the active power controller is followed by a limiter function of +/-i_{max} limits, where:

$$i_{max} = i_{rated} \tag{4.15}$$

4.3.2 Reactive Power Control

The reactive power from equation (4.13) is given by:

$$Q_{dq} = \frac{-3}{2} U_{xd} i_q \tag{4.16}$$

The reactive power is controlled by reactive current (i_q^*) and is implemented as in Figure 4.9.

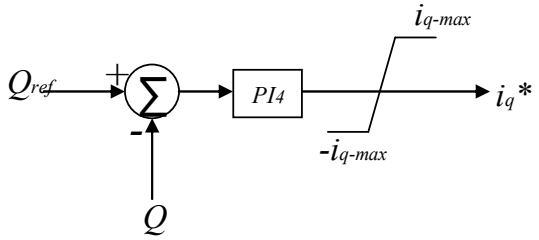


Figure 4.9: PI controller for reactive power control

As in the case for active power control, i_q* will be the reference input for the reactive current

controller of the inner current loop in Figure 4.7.

i_q* is limited to +/-$I_{q\text{-}max}$ in such a way that the total converter current should not exceed the rated current (I_{max}=I_{rated}). This takes the assumption that that priority is given to transfer of active power.

Hence:

$$i_{q\_max} = \sqrt{I_{max}{}^2 - i_d^{*2}} \tag{4.17}$$

4.3.3 DC Voltage Control

From energy balance of the VSC-HVDC terminal:

$$\begin{aligned} &P_{ac} + P_{DC} + P_{cap} = 0 \\ &\frac{3}{2} V_{xd} i_d + V_{DC} I_{DC} + V_{DC} i_{cap} = 0 \end{aligned} \tag{4.18}$$

where I_{DC} and i_{cap} are the DC bus current and the capacitor current respectively.

From equation (4.18) the current through the capacitor will be:

$$i_{cap} = -(\frac{3V_{Xd} i_d}{2V_{DC}} + I_{DC}) \tag{4.19}$$

And the same current in terms of voltage across the capacitor is given by:

$$i_{cap} = C \frac{dV_{DC}}{dt} \tag{4.20}$$

From equations (4.19) & (4.20) the differential equation for the DC voltage becomes:

$$\frac{dV_{DC}}{dt} = -\frac{1}{C}\left(\frac{3V_{Xd}i_d}{2V_{DC}} + I_{DC}\right)$$
$$= \frac{-3V_{Xd}i_d}{2CV_{DC}}\left(i_d + \frac{2V_{DC}}{3V_{Xd}}I_{DC}\right) \qquad (4.21)$$

From equation (4.21) it is seen that DC voltage can be regulated by control of active current (i_d^*). The I_{DC} term in equation (4.21) is compensated by feed forward control in the DC voltage regulator.

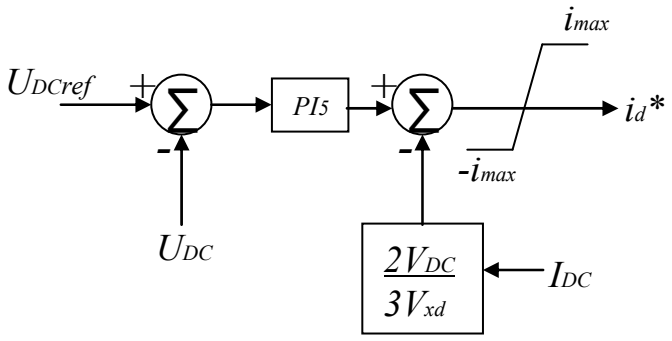


Figure 4.10: DC voltage regulator

4.3.4 AC Voltage Control

Weak grid connection has significant line resistance and inductance, as shown in Figure 4.11 This creates considerable amount of voltage fluctuations with changing active power flow. Therefore if the AC network connected to the VSC-HVDC terminal is a weak grid, the AC voltage at PCC must be regulated by the converter.

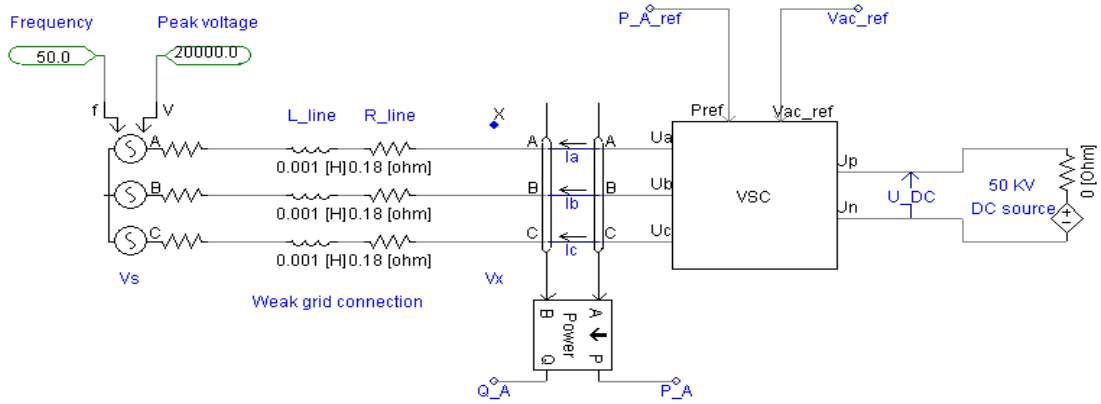


Figure 4.11: Weak grid modeling by series resistance plus inductance

By applying KVL across the line impedance;

$$\hat{V}_x - \hat{V}_s = (r_{line} + jwL_{line})\hat{i}_s \tag{4.22}$$

Where V_x is the reference voltage (has an angle of zero), $r_{line}+j\omega L_{line}$ is the line impedance and i_s is given by:

$$\begin{aligned}\hat{i}_s &= \left(\frac{S}{V_x}\right)^* \\ &= \left(\frac{P+jQ}{V_x}\right)^* \\ &= \left(\frac{P-jQ}{V_x}\right)\end{aligned} \tag{4.23}$$

Substituting equation (4.23) into (4.22);

$$\begin{aligned}\hat{V}_x &= \hat{V}_s + (r_{line} + j\omega L_{line})\hat{i}_s \\ &= \hat{V}_s + (r_{line} + j\omega L_{line})\left(\frac{P-jQ}{V_x}\right) \\ &= \hat{V}_s + (\frac{Pr_{line} + Q\omega L_{line}}{V_x}) + j(\frac{P\omega L_{line} - Qr_{line}}{V_x})\end{aligned} \tag{4.24}$$

The quadrature axis change in voltage due to active and reactive power has little effect on the resultant voltage magnitude V_x. Therefore, V_x is approximately;

$$\hat{V}_x = \hat{V}_s + \left(\frac{Pr_{line} + Q\omega L_{line}}{V_x}\right) \tag{4.25}$$

In equation (4.25) P is determined by the desired amount of active power flow. Hence, voltage V_x can be maintained constant by reactive power compensation. This relation is mathematically given by:

$$\Delta V_x = \frac{\omega L_{line}}{V_x} \Delta Q \tag{4.26}$$

The block diagram of the AC voltage controller is given by:

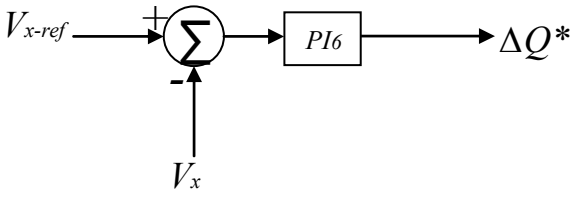


Figure 4.12: AC voltage control by reactive power compensation

ΔQ^* is a reference input to the reactive power controller (Figure 4.9).

4.3.5 Frequency Control

The active AC system consists of synchronous generators with natural frequency droop characteristics with respect to power. They also implement frequency droop control which is useful for distributed compensation for power unbalance occurring at some point in the system [10]. The VSC-HVDC can also be set to contribute to the aggregate frequency droop characteristics of the entire AC system. The frequency droop control can be realized as shown in Figure 4.13 [10].

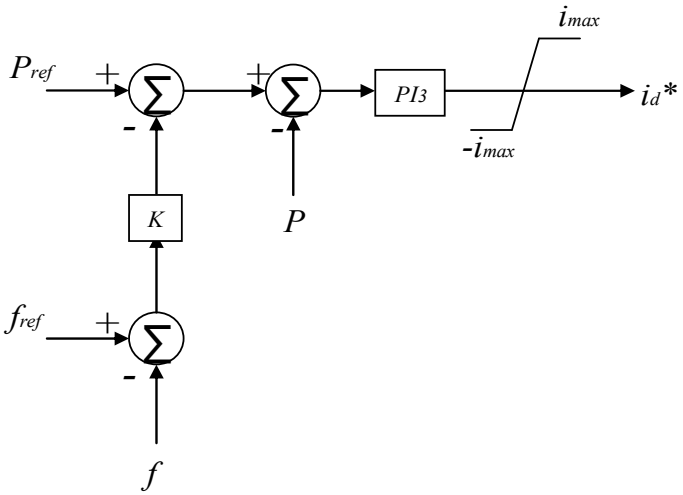


Figure 4.13: Frequency droop control

K in Figure 4.13 is called frequency bias factor and is assigned according to desired amount of contribution of the VSC-HVDC terminal for frequency control.

4.4 Control Loop Transfer Functions

In order to specify the parameters of the different PI controllers, the open loop transfer functions (TFs) of each control scheme must be determined. In order to do so, first the Laplace transformed equivalent of the physical systems must be identified. System transfer function is derived from the linearized differential equation of the respective state variable.

When seen from an outer control loop, the time delay in an inner loop is approximately the sum of all the delays in the inner loop.

4.4.1 TF of Inner Current Loop

After eliminating the feed forward elements from Figure 4.7, the corresponding open loop transfer function of the inner current loop is established as follows.

$$\begin{aligned} O.L. &= K_{p1}\left(\frac{1+T_{i1}S}{T_{i1}S}\right)\left(\frac{1}{1+T_wS}\right).\frac{1}{r}\left(\frac{1}{1+\tau S}\right) \\ &= K_{p2}\left(\frac{1+T_{i2}S}{T_{i2}s}\right)\left(\frac{1}{1+T_wS}\right).\frac{1}{r}\left(\frac{1}{1+\tau S}\right) \end{aligned} \tag{4.27}$$

Where $\tau=L/r$

4.4.2 TF of DC Voltage Control Loop

The block diagram of the complete DC voltage control loop is shown in Figure 4.14.

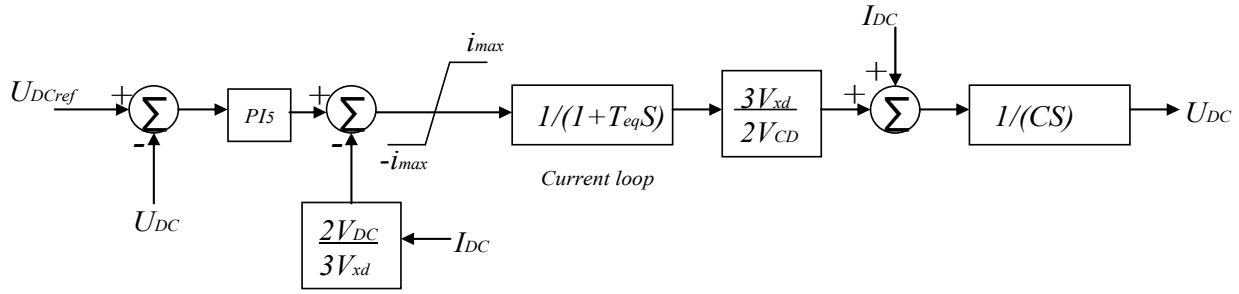


Figure 4.14: Closed loop control diagram of DC voltage regulator

Neglecting the constant disturbances, the open loop transfer function becomes;

$$O.L. = K_{p5}\left(\frac{1+T_{i5}S}{T_{i5}S}\right)\left(\frac{1}{1+T_{eq}S}\right).\frac{3V_{xd}}{2V_{DC}}.\frac{1}{Cs} \tag{4.28}$$

where T_{eq} is the total time delay in the current control loop.

4.4.3 TF of Active / Reactive Power Control Loops

The control loop for active power is shown in Figure 4.15.

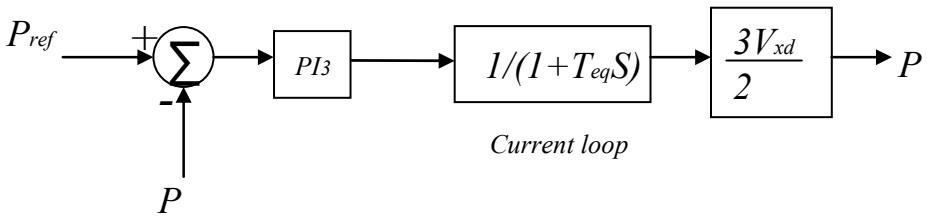


Figure 4.15: Active power control loop

The open loop gain of active (and reactive) power control is given by:

$$O.L. = K_{p3}\left(\frac{1+T_{i3}S}{T_{i3}S}\right)\left(\frac{1}{1+T_{eq}S}\right).\frac{3V_{xd}}{2} \quad K_{p4}\left(\frac{1+T_{i4}S}{T_{i4}S}\right)\left(\frac{1}{1+T_{eq}S}\right).\frac{3V_{xd}}{2} \tag{4.29}$$

4.4.4 TF of AC Voltage Control Loop for Weak Grid Connection

The AC voltage control diagram for weak grid connection is shown in Figure 4.16.

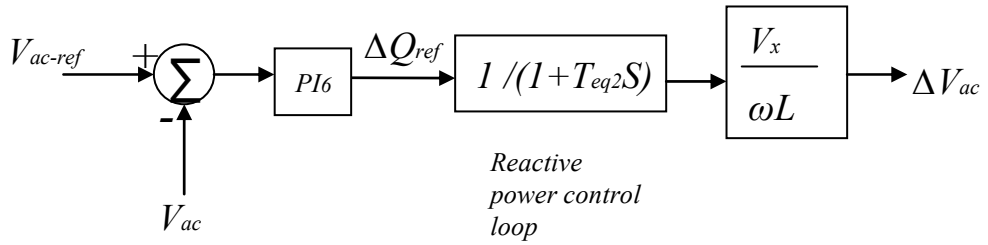


Figure 4.16: Block diagram of closed loop AC voltage control loop

The corresponding open loop transfer function is given by:

$$O.L. = K_{p6}\left(\frac{1+T_{i6}S}{T_{i6}S}\right)\left(\frac{1}{1+T_{eq2}S}\right).\frac{V_{xd}}{\omega L} \tag{4.30}$$

4.4.5 TF of AC Voltage Control Loop for Passive AC Network

AC voltage control loop for passive load connection is shown in Figure 4.17.

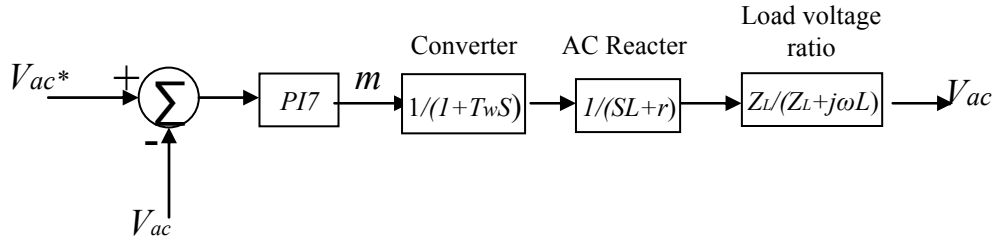


Figure 4.17: Block diagram of AC voltage control loop for passive load

The transfer function of the physical system in Figure 4.17 can be derived as follows.

At steady state, the AC voltage magnitude at PCC is given by voltage divide rule:

$$V_x = V_c\left|\frac{Z_L}{Z_L + j\omega L}\right| \tag{4.31}$$

where Z_L is the equivalent Thevenin impedance of the AC network and V_c is the converter output voltage.

From the *d-q* equivalent circuit in Figure 4.6 it was seen that the physical system has a delay function of $1/(1+\tau S)$, which remains the same for any reference frame.
The open loop gain of the AC voltage control loop becomes:

$$O.L. = K_{p7}\left(\frac{1+T_{i7}S}{T_{i7}S}\right)\left(\frac{1}{1+T_wS}\right).\left(\frac{1}{1+\tau S}\right)\left|\frac{Z_L}{Z_L+j\omega L}\right| \tag{4.32}$$

In practice, measurement instruments are usually equipped with noise filters. In addition, the instruments themselves have their own time delays. The sum total of these delays can affect the performance of the controllers. Therefore these additional delays must be taken in to consideration while designing practical PI controllers.

4.5 Tuning of PI Controllers

The PI controllers must be tuned for optimal performance of the control loops. The objectives in PI tuning are:
1. To get fast response of the system, i.e. to increase the cutoff frequency as high as possible, and
2. To get small overshoot, or to get a good damping of oscillations

To optimize speed of response and system stability, *modulus optimum* and *symmetrical optimum* techniques are applied depending on the form of the open loop transfer function of the control loop at hand [11].

4.5.1 Modulus Optimum Criterion

Modulus optimum technique is used for plants with low order (<3) transfer functions and makes the cutoff frequency as high as possible. Hence when there are one dominant and another minor pole in the transfer function, the integral time constant of the PI controller is selected to cancel out the dominant pole. Given the open loop transfer function:

$$O.L. = K_{p1}\left(\frac{1+T_{i1}S}{T_{i1}S}\right)\left(\frac{1}{1+T_wS}\right).\frac{1}{r}\left(\frac{1}{1+\tau S}\right) \quad , \tau >> T_w \tag{4.33}$$

The time constant of the PI controller is assigned as: $T_{i1} = \tau$

The crossover frequency, ω_c, is usually chosen one or two orders smaller than $1/T_w$ in order to avoid noise and interference from the switching frequency components.

From the unity gain requirement at ω_c,

$$\left|O.L.\right| = \left|\left(\frac{K_{p1}}{T_{i1}S}\right)\left(\frac{1}{1+T_wS}\right).\frac{1}{r}\right|_{s=j\omega_c} \tag{4.34}$$

From equation (4.34), proportional constant of the PI controller is determined as:

$$K_{p1} = \omega_c T_{i1} r\left|1+j\omega_c T_w\right| \tag{4.35}$$

4.5.2 Symmetrical Optimum Criterion

When one pole of the open loop transfer function is near origin or at the origin itself, the modulus optimum criterion can not be applied. Instead, symmetrical optimum design method is used for specifying the PI controllers. The method has an advantage of maximizing the phase margin [11]. Given the transfer function:

$$O.L. = K_{p5}\left(\frac{1+T_{i5}S}{T_{i5}S}\right)\left(\frac{1}{1+T_{eq}S}\right).\frac{3V_{xd}}{2V_{DC}}.\frac{1}{Cs} \tag{4.36}$$

The phase angle for $S=j\omega$ will be:

$$\begin{aligned}\angle O.L. &= \tan^{-1}(T_{i5}\omega S) - 90^o - \tan^{-1}(T_{eq}\omega S) - 90^o \\ &= \tan^{-1}(T_{i5}\omega S) - \tan^{-1}(T_{eq}\omega S) - 180^o \\ &= \phi_m - 180^o\end{aligned} \tag{4.37}$$

where Φ_m is the phase margin.

Differentiating Φ_m with respect to cutoff frequency ω_c,

$$\frac{d\phi_m}{d\omega_c} = \frac{T_{i5}}{1+(T_{i5}\omega_c)^2} - \frac{T_{eq}}{1+(T_{eq}\omega_c)^2} = 0 \tag{4.38}$$

Solving equation (4.38):

$$\omega_c = \frac{1}{\sqrt{T_{i5}T_{eq}}} \tag{4.39}$$

Substituting equation (4.39) in (4.38):

$$\angle\phi_m = \tan^{-1}\sqrt{\frac{T_{i5}}{T_{eq}}} - \tan^{-1}\sqrt{\frac{T_{eq}}{T_{i5}}} \tag{4.40}$$

$$\text{Let} \quad \tan^{-1}\sqrt{\frac{T_{i5}}{T_{eq}}} = \theta \tag{4.41}$$

$$\rightarrow \tan^{-1}\sqrt{\frac{T_{eq}}{T_{i5}}} = 90^o - \theta \tag{4.42}$$

Φ_m in terms of θ becomes,

$$\phi_m = \theta - (90 - \theta) = 2\theta - 90 \tag{4.43}$$

And

$$\sin\phi_m = \sin(2\theta - 90) = -\cos 2\theta \tag{4.44}$$

From half-angle trigonometric equations:

$$\sin\theta = \sqrt{\frac{1-\cos 2\theta}{2}}$$
$$\cos\theta = \sqrt{\frac{1+\cos 2\theta}{2}} \tag{4.45}$$
$$\tan\theta = \sqrt{\frac{1-\cos 2\theta}{1+\cos 2\theta}}$$

Combining equations (4.41), (4.44) and (4.45),

$$\sqrt{\frac{T_{i5}}{T_{eq}}} = \tan\theta = \sqrt{\frac{1-\cos 2\theta}{1+\cos 2\theta}} = \sqrt{\frac{1+\sin\phi_m}{1-\sin\phi_m}} \tag{4.46}$$

Equation 4.46 gives integral time constant of:

$$\begin{aligned} T_{i5} &= T_{eq}\left(\frac{1+\sin\phi_m}{1-\sin\phi_m}\right) \\ &= a^2\, T_{eq} \end{aligned} \tag{4.47}$$

where a is a constant number. A value of $a=T_{i5}/T_{eq}$ ratio between 4 and 16 is recommended in [11].

From the unity gain requirement at cutoff frequency,

$$\begin{aligned} |O.L.| &= \left| K_{p5}\left(\frac{1+j\omega_c T_{i5}}{j\omega_c T_{i5}}\right)\left(\frac{1}{1+j\omega_c T_{eq}}\right).\frac{3V_{xd}}{2V_{DC}}.\frac{1}{j\omega_c C}\right| \\ &= K_{p5}\left|1+j\omega_c T_{i5}\right|\left|\frac{1}{j\omega_c T_{i5}-\omega_c{}^2 T_{eq}T_{i5}}\right|\frac{3V_{xd}}{2V_{DC}}.\frac{1}{j\omega_c C} \\ &= K_{p5}\frac{3V_{xd}}{2V_{DC}}.\frac{1}{j\omega_c C} \\ &= 1 \end{aligned} \tag{4.48}$$

From equation (4.48) the proportional constant becomes:

$$K_{p5} = \frac{2V_{DC}}{3V_{xd}}\omega_c C \tag{4.49}$$

4.6 Control of Multiterminal VSC-HVDC (MTDC)

The control system for multiterminal VSC-HVDC consists of a central master controller and local terminal controllers at the site of each VSC-HVDC station. The master controller is provided with minimum set of functions necessary for coordinated operation of the terminals. This includes such as start and stop, and setting references for active and reactive power [12].

The terminal controllers are mainly responsible for:

-active power control

-reactive power control

-DC voltage regulation and

-AC voltage regulation

The structures of the individual controllers have been discussed in previous topics. When the different VSC-HVDC terminals are connected together, the control schemes should be modified to tolerate loss of connection to some converter stations and still be able to operate properly. To achieve this objective, control schemes called *voltage margin method* and *DC voltage droop control* were suggested in literatures [12] and [13] respectively.

4.6.1 MTDC Control by DC Voltage Margin

An MTDC consisting of four terminals is shown in Figure 4.18. An MTDC link should have at least one of the terminals configured in constant DC voltage control mode. To study the operation of the different types of terminals connected together, the MTDC model shown in Figure 4.18 has terminals of different control modes.

The active power - DC voltage ($P\text{-}U_{DC}$) characteristics of different VSC-HVDC terminals corresponding to constant DC voltage, constant power and passive load terminals are shown in Figure 4.19.

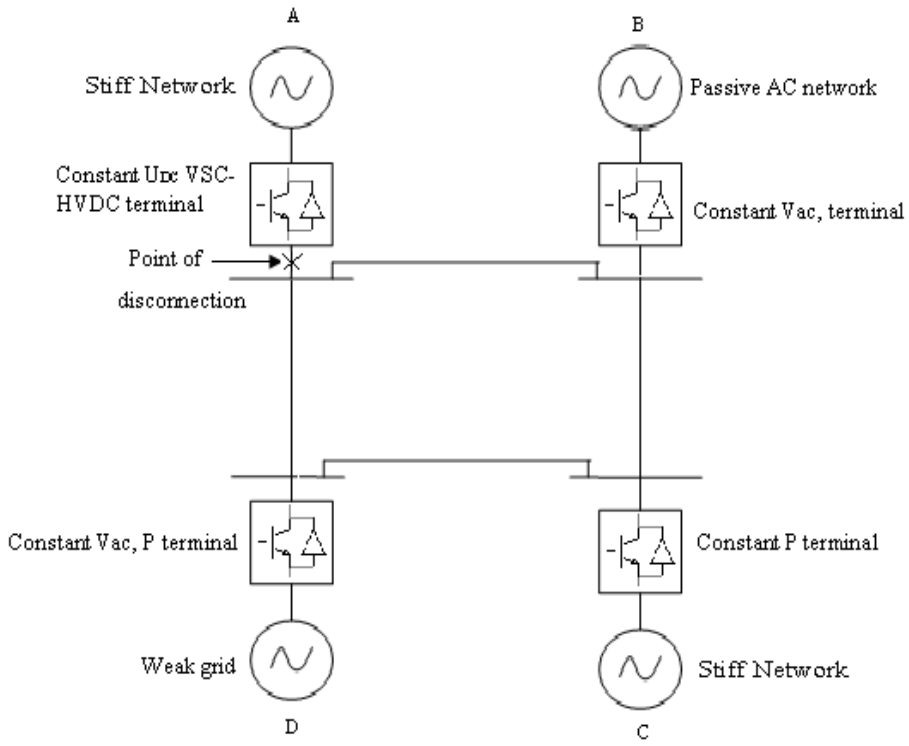


Figure 4.18: Four terminal MTDC

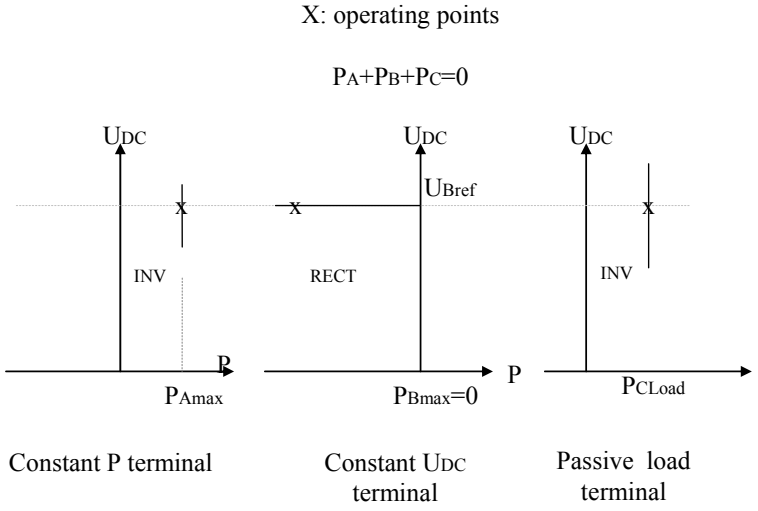


Figure 4.19: P-U_{DC} characteristic curves

The operating points (shown by X's in the figure) are determined from the power balance equation.

$$\sum_{i=1}^{n} P_i = P_A + P_B + P_C = 0 \qquad (4.50)$$

As it was discussed in chapter 3, positive power represents inverter mode and negative power indicates rectifier mode of operation.

When there is one DC voltage regulator in the MTDC and others operating in constant power control mode, the system remains stable given that power demand and supply are balanced. The DC voltage regulator has the role of compensating for power unbalances in the MTDC system. Therefore even if some connections to VSC-HVDC terminals are lost, as long as the DC voltage regulator is in operation and total power demand/supply in the MTDC is not exceeded, the MTDC system remains in a stable state. But, if for some reason the DC regulating terminal is disconnected from the MTDC, the MTDC will become unstable and system black out may follow. If the unbalance during loss of the DC voltage regulating terminal causes power deficit into the MTDC, some or all of the VSC-HVDC terminals will go into the saturation (over modulation) region. If on the other hand the disconnection causes excess power flowing into the MTDC, the DC voltage level will rise continuously to dangerously high voltage levels and is likely to cause material losses at minimum. To avoid such unfavorable situations, the P-U_{DC} characteristics of some terminals (connected to active AC networks) can be modified to cross the line $P=0$ as in Figure 4.20. By doing so, the MTDC system will have a redundancy of DC voltage controllers that operate at different operating conditions and DC voltage level with in limits.

Legend: operating points
X: when all three terminal are functional
O: when connection to A is lost
S: when A and C are disconnected from the MTDC
ΔVDC=Voltage margin

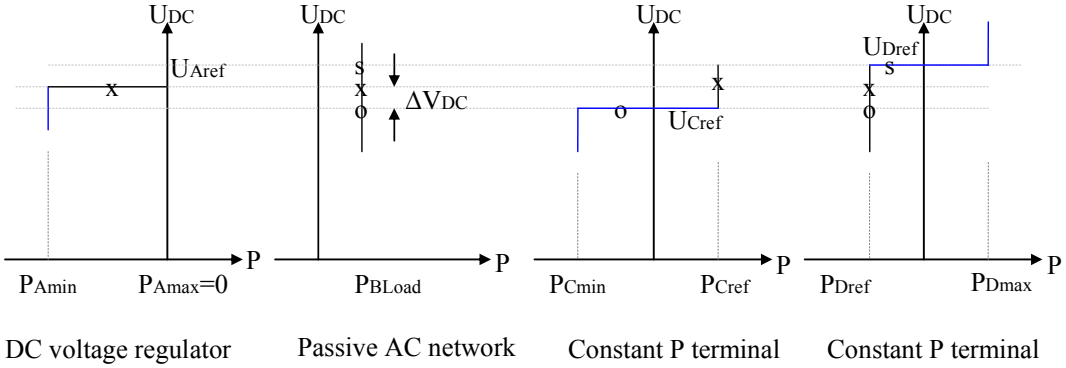


Figure 4.20: P-U_{DC} characteristic curves with voltage margin control

With this assignment of P-U_{DC} characteristics if connection to DC voltage regulating terminal (A) is lost, the DC voltage rise or drop due to the loss of connection will be limited only to the predetermined voltage margin. If there is DC voltage rise, it will go up until the other terminal with next higher DC voltage reference setting (terminal D in Figure 4.20) takes over the duty of DC voltage regulation. On the other hand if the DC voltage level has reduced, the terminal with the next lower DC voltage setting will start to act as DC slack bus with in few tens of milliseconds. The difference between DC voltage settings of two DC regulating terminals of consecutive references is called *voltage margin*. Mathematically:

$$\Delta U_{margin} = U_{Aref} - U_{Cref} \tag{4.51}$$

Selecting too small DC voltage margin between two terminals causes unwanted interaction of the DC voltage controllers even for slight DC voltage perturbations due to load switchings or sudden change of active power references. Too large voltage margin can reduce the maximum available AC voltage or can reduce the maximum amount of transferable power. Therefore selecting the size of the DC voltage margin is an optimization problem that should consider these two constraints.

The modified P-U_{DC} characteristic curves (of terminals C and D in Figure 4.20) can be realized by the following control structure.

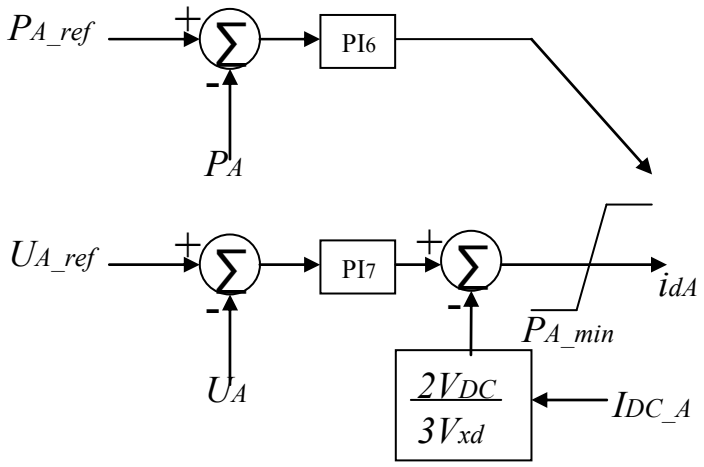


Figure 4.21: Implementation of voltage margin control

All converters including the one at DC voltage regulating terminal have their own natural upper and lower power transfer limits which are basically determined by the maximum DC current capacities. Taking these natural upper and lower limits, a two-stage DC voltage margin control P-U_{DC} curve is shown below [12].

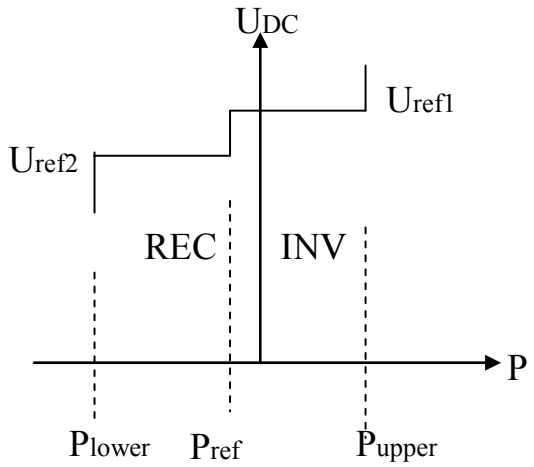


Figure 4.22: P-U_{DC} characteristic of two-stage voltage margin control

The two-stage DC voltage margin control has an advantage of using one terminal as a backup DC voltage regulator for both DC voltage rise up and DC voltage drop down.

Implementation of two-stage DC voltage margin control is shown in the figure below.

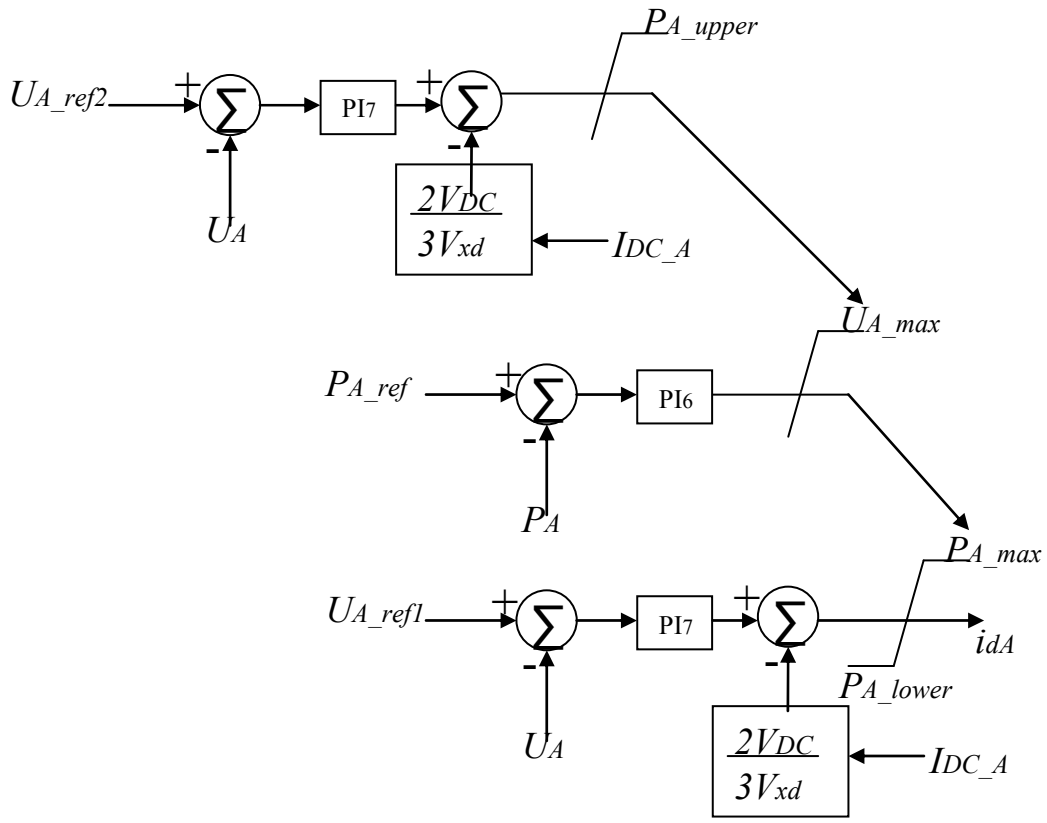


Figure 4.23: Implementation of two-stage voltage margin control

For its simplicity of implementation, only one stage-voltage margin control will be used in the models of this thesis work.

4.6.2 MTDC Control by DC Voltage Droop

If the MTDC network consists of several VSC-HVDC terminals, the DC voltage control method discussed previously will put the burden of DC voltage regulation on just one converter terminal. DC voltage control by droop characteristics enables two or more terminals in the MTDC to share the duty of DC voltage regulation according to their predetermined DC voltage droop characteristics.

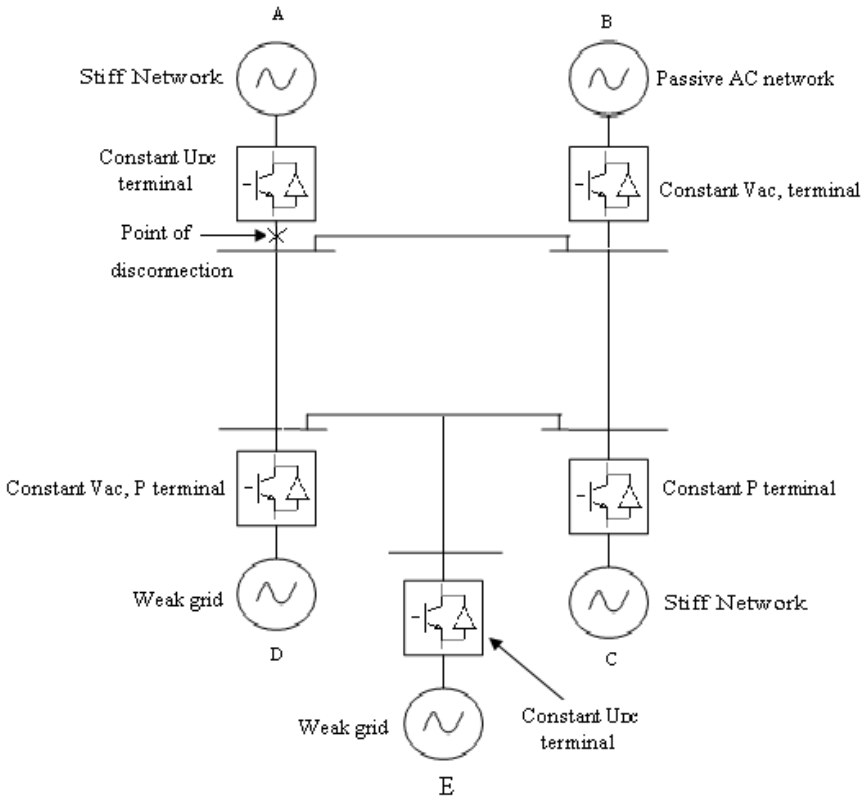


Figure 4.24: Five terminal MTDC with two DC voltage regulating terminals

DC droop control is a modification of the voltage margin control where the horizontal line sections of the characteristic curves (i.e. constant U_{DC}) will be replaced by a line with a line with small slope (i.e. droop). This is shown in Figure 4.25 below.

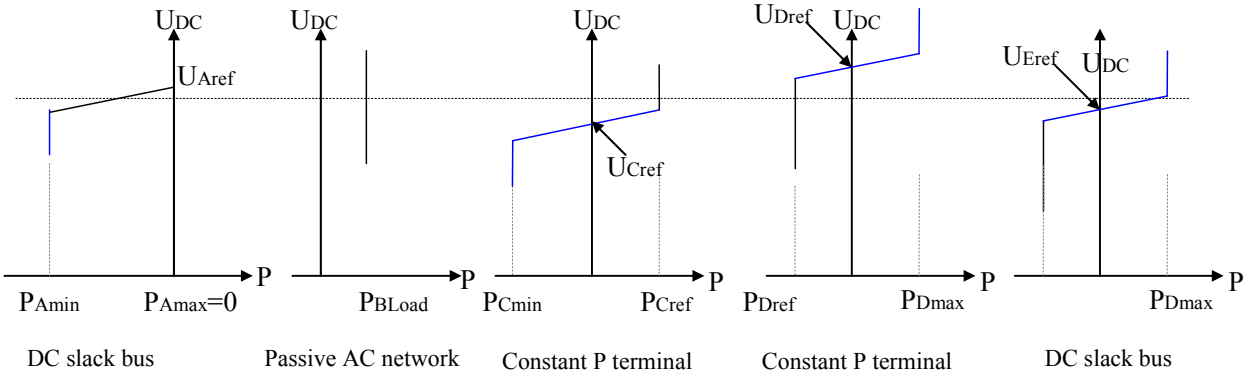


Figure 4.25: DC voltage droop control

The power-DC voltage droop control is an exact equivalent of the power-frequency droop control

implemented in AC grids for primary control [13]. The droop control is possible only with the use of proportional controller in the DC voltage regulator. The droop relation is derived in [13] and is shown below.

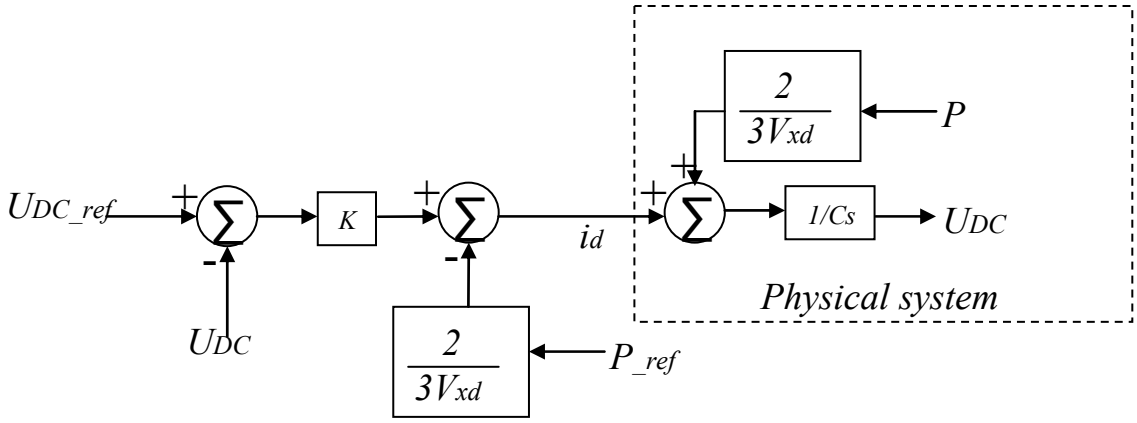


Figure 4.26: DC voltage regulation for droop control

As can be seen in Figure 4.26, the controller consists only of proportional gain in order to tolerate steady state errors. A power mismatch will result in the required P-U_{DC} characteristic curve. Mathematically;

$$(U_{DCref} - U_{DC})K - \frac{2\,\mathrm{P}_{ref}}{3V_d} + \frac{2\,\mathrm{P}}{3V_d} = 0 \tag{4.52}$$

$$\rightarrow \Delta U_{DC} = \frac{2\Delta\,\mathrm{P}_{ref}}{3KV_d} \tag{4.53}$$

Hence the DC voltage droop, δ_{DC} is given by:

$$\frac{\Delta U_{DC} / U_{DC\_rated}}{\Delta\,\mathrm{P}_{ref} / \mathrm{P}_{rated}} = \frac{2}{3KV_d}\frac{\mathrm{P}_{rated}}{U_{DC\_rated}} = \delta_{DC} \tag{4.54}$$

The proportional gain K can be selected according to the required amount of the DC droop, δ_{DC}.

$$K = \frac{2}{3V_d \delta_{DC}} \frac{\mathrm{P}_{rated}}{U_{DC\_rated}} \tag{4.55}$$

By varying *K,* it is possible to schedule the percentage contribution of the terminal for DC voltage regulation.

When *n* number of terminals in an MTDC system operate in DC voltage droop control mode, the participation factor in faction of ith terminal is given by:

$$\lambda_i = \frac{K_i}{\sum_{j=1}^{n} K_j} \tag{4.56}$$

where K_j is the proportional gain of j^{th} terminal in DC voltage control mode.

4.7 DC Overvoltage Controller

When connection of an inverting terminal to MTDC is lost or when a converting terminal is connected instantaneously, there will be DC voltage spike occurring for a fraction of second. This is because, no matter how small it is, there is always some delay in the controllers and the physical system. Voltage spikes are caused by fast charging of the DC capacitors.

Likewise, the sudden addition of a converter or loss of inverter terminal from the MTDC leads to a counter phenomenon called voltage dip (see Figure 4.27).

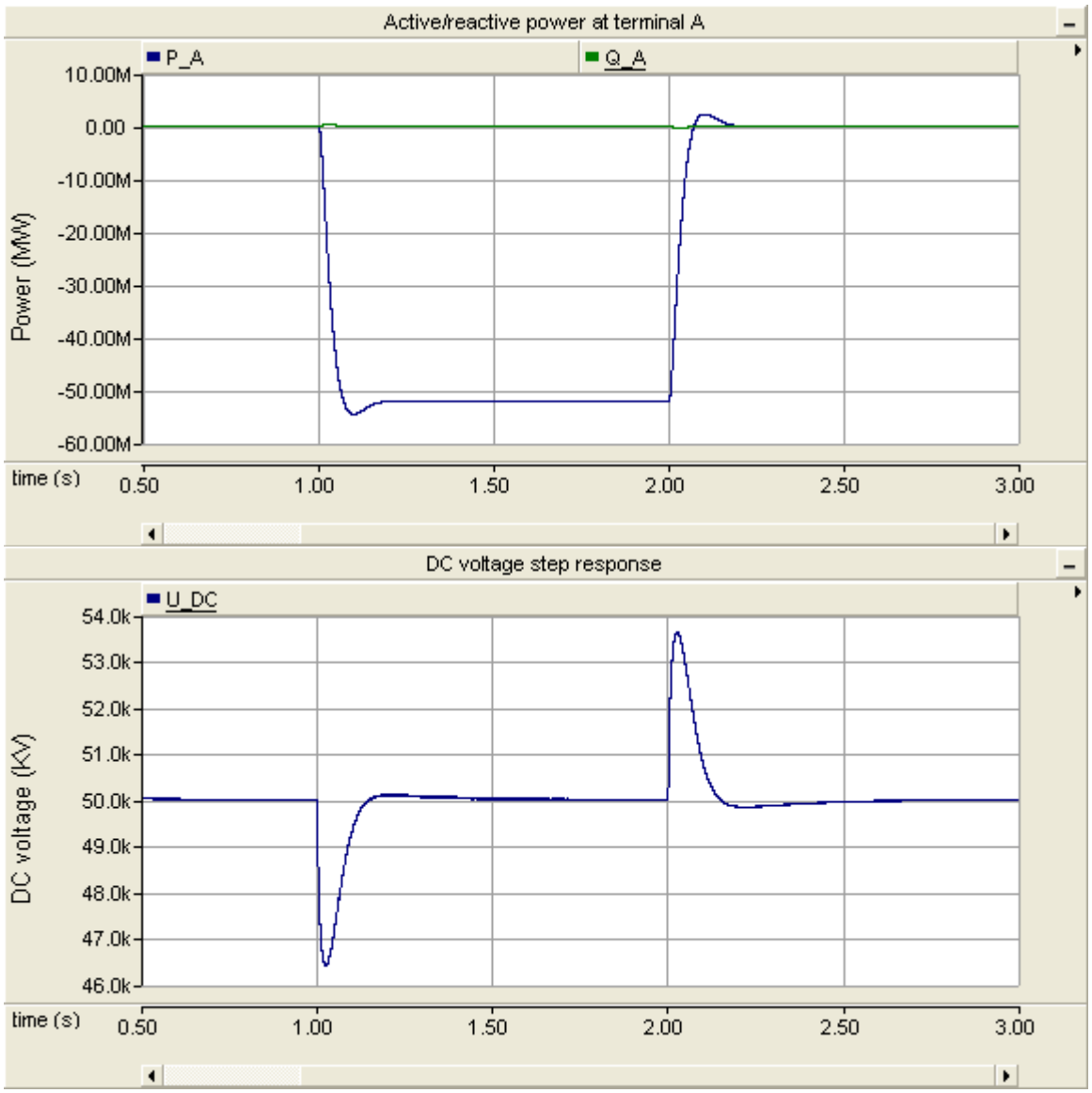


Figure 4.27: Voltage dip and over voltage in the DC bus due to change in power flow

From safety and protection point of view, voltage dips are of much less concern. But voltage spikes may lead to over voltages and cause a threat for equipments as well as personnel safety. On literature [14] the use a logical circuit controller was suggested as overvoltage protection and a modified version of the controller is shown below.

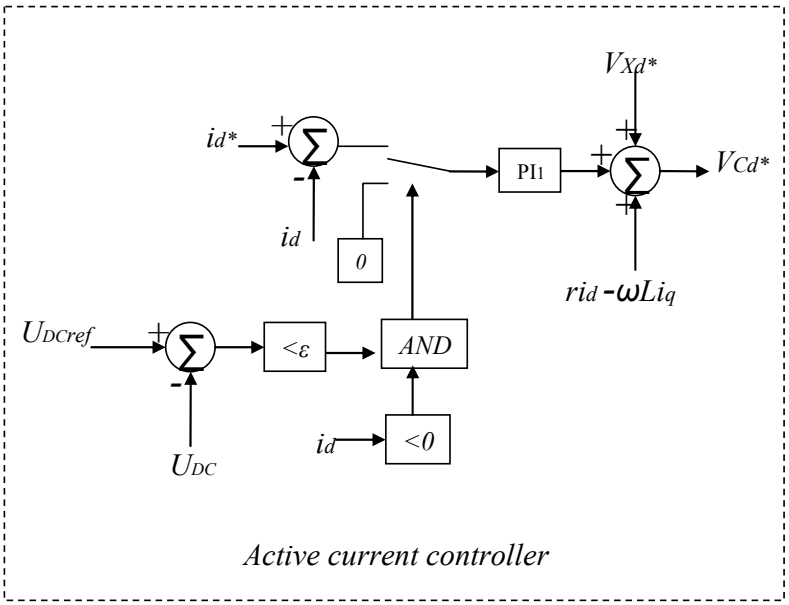


Figure 4.28: Overvoltage controller

The overvoltage controller is implemented only at the DC voltage regulating terminal. As shown in Figure 4.28, the VSC-HVDC will be temporarily disabled when ΔU_{DC} exceeds a predetermined limit of ε. Consequently the capacitor voltage drops due to discharging by the uninterrupted i_{DC} and the VSC-HVDC goes back to its normal operation. Since the discharging occurs quickly, the overvoltage controller will interfere only for a small fraction of second.

Chapter 5

Simulation Studies

This chapter is concerned with simulation studies of the different VSC-HVDC control structures described in Chapter 4. The PSCAD/EMTDC electromagnetic transient simulation software was used for modelling of the different cases VSC-HVDC connections including MTDCs. Simulation results are expected to validate the required characteristics of the controllers discussed in the previous chapter.

5.1 Specification of the VSC

For the sake of simplicity, one VSC-HVDC specification established and used for all converters models. The current carrying capacity limits of transmission lines are not considered in the model developments. AC and DC filters are not included in the model and point X in Figure 5.1 is taken as the reference point for measurements of V_{ac}, P, Q, I_{ac} and also for the PLL.

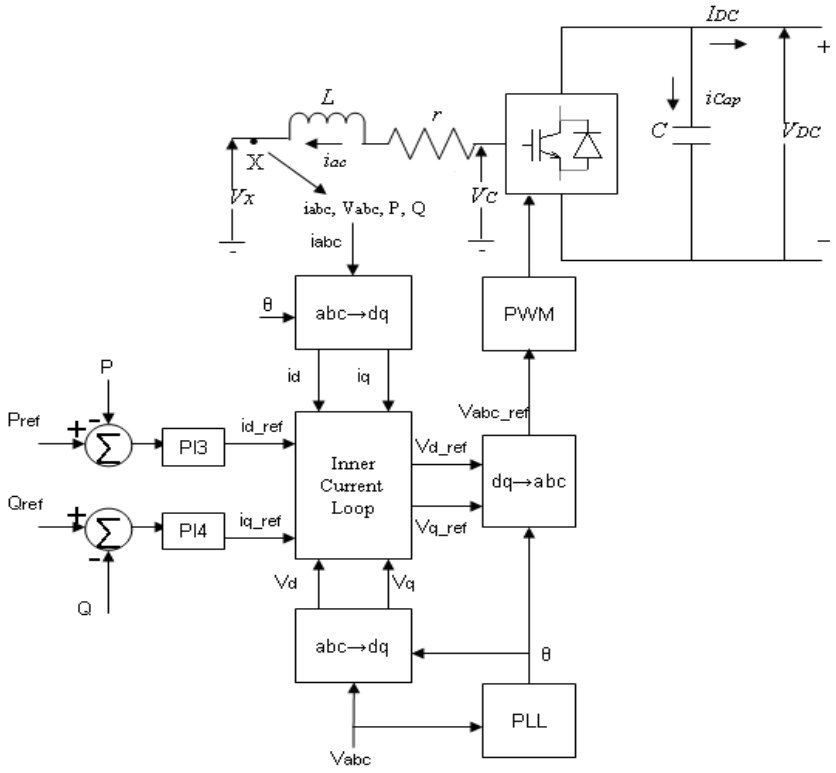


Figure 5.1: Single line diagram of a VSC-HVDC terminal with the basic control structure

Table 5.1: Specifications of VSC used in the models

Parametre	Rating
Rated Power (S_n)	100 MVA
DC voltage (U_{DC})	50KV
Line-line AC voltage (VLL)	24.5KVrms
L-filter impedance ($r+j\omega L$)	(0.01+j0.25)p.u.

The DC capacitance is computed from equation (3.2) as:

$$C = \frac{2\tau S_n}{U_{DC}^2} \tag{5.1}$$

Considering a time constant (τ) of 5ms and using the specifications in Table 5.1:

$$\begin{aligned} C &= \frac{2\tau S_n}{U_{DC}^2} \\ &= \frac{(2)(0.005)100*10^6}{(50*10^3)^2} \\ &= 400*10^6\ \mu F \end{aligned} \tag{5.2}$$

This corresponds to the total capacitance. In the model this equivalent capacitance comes from two serially connected capacitances grounded at their junction node. In such configuration each branch of capacitor will have a rating of twice the total equivalent capacitance. Hence two serially connected capacitors of 800μF are used in the VSC HVDC models.

5.2 P.U. Calculations

Base quantities for *d-q* reference frame are:

$$
\begin{aligned}
&S_b = V_{db} I_{db} = \frac{2\sqrt{3}}{3} V_n I_n = \frac{2}{3} S_n = \frac{2*100}{3} \approx 66.7MVA \\
&V_{db} = V_{qb} = \sqrt{2/3}\, V_n = \sqrt{2/3} * 24.5 = 20KV \\
&I_{db} = I_{qb} = \sqrt{2} I_n = \frac{S_b}{V_{db}} = \frac{66.7MVA}{20KV} \approx 3.333KA \\
&Z_{db} = Z_{qb} = \frac{V_{db}}{I_{db}} = \frac{V_n}{\sqrt{3} I_n} = Z_{sb} = \frac{20KV}{3.333KA} = 6\Omega \\
&L_b = Z_{db} = 6\Omega \\
&C_b = \frac{1}{Z_{db}} = \frac{1}{6\Omega}
\end{aligned}
\tag{5.3}
$$

The base quantities for the DC side of the VSC HVDC are calculated as follows.

$$
\begin{aligned}
&S_{DC,b} = S_n = \frac{3}{2} S_{db} = 100MVA \\
&U_{DC,B} = 2V_{db} = 40KV \\
&I_{DC,b} = \frac{S_{DC}}{U_{DC,b}} = 2.5KA \\
&Z_{DC} = \frac{U_{DC,b}}{I_{DC,b}} = \frac{8Z_{db}}{3} = \frac{8Z_n}{3} = \frac{40KV}{2.5KA} = 16\Omega
\end{aligned}
\tag{5.4}
$$

Physical quantities:

$$
\begin{aligned}
&L = \frac{0.25pu * 6\Omega}{100\pi \quad rad/s} = 0.0048H \\
&r = 0.01pu * 6\Omega = 0.06\Omega \\
&C = 400\mu F
\end{aligned}
\tag{5.5}
$$

The p.u. quantities will be found as:

$$L_{pu} = \frac{L}{L_b} = \frac{0.0048}{6} = 0.0008\,pu * s / rad$$
$$r_{pu} = \frac{r}{Z_{db}} = \frac{0.06}{6} = 0.01\,pu \qquad (5.6)$$
$$C_{pu} = \frac{C}{C_b} = \frac{400}{1/6} = 2400\,pu * rad / s$$

The VSC-HVDC model with the specified component ratings is shown below.

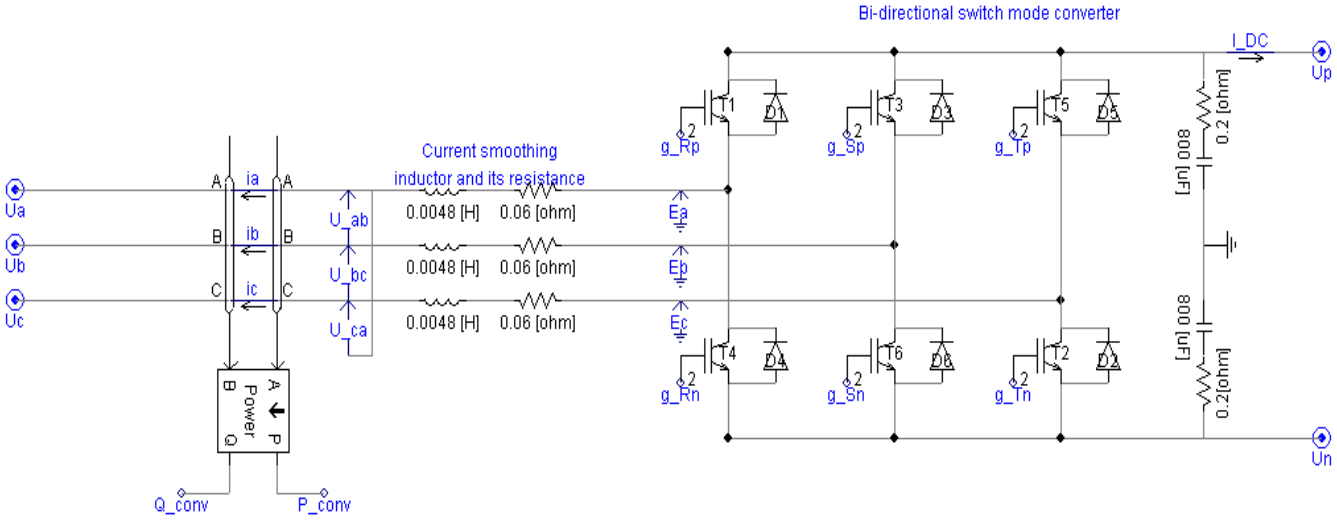


Figure 5.2: VSC-HVDC model in PSCAD

The line-line voltage measurements are used to calculate the phase voltages. This is done inorder to ensure elimination of zero sequence voltage from the voltage measurements. The phase voltages are calculated as follows.

$$V_a = \frac{V_{ab} - V_{ca}}{3}$$
$$V_b = \frac{V_{bc} - V_{ab}}{3} \qquad (5.7)$$
$$V_c = \frac{V_{ca} - V_{bc}}{3}$$

In PSCAD this is implemented as shown in Figure 5.3.

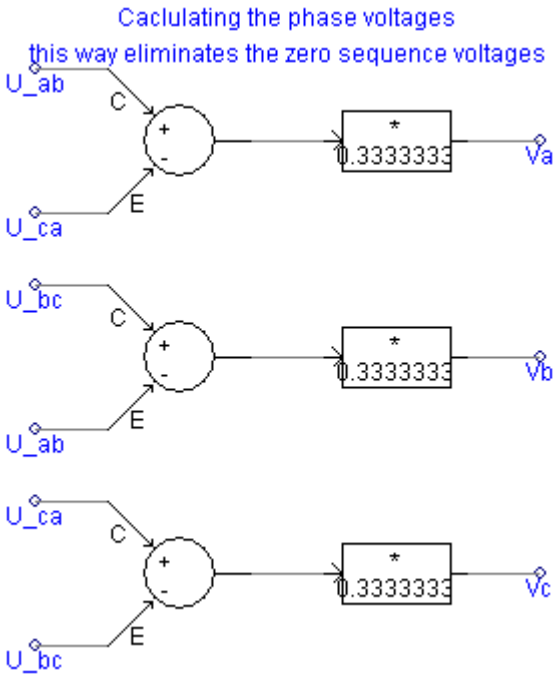


Figure 5.3: Phase voltage calculations from line voltage measurements

Built in PLL from PSCAD was used in the models as shown in Figure 5.4.

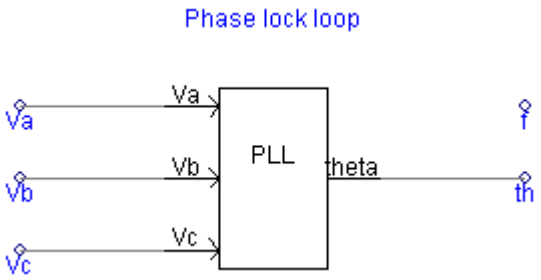


Figure 5.4: Built in PLL used for generation of synchronizing angle (*th/θ*)

The *abc to dq* transformations, *rms* measurements and *pu* conversions in *dq* reference frame are shown in the figure below.

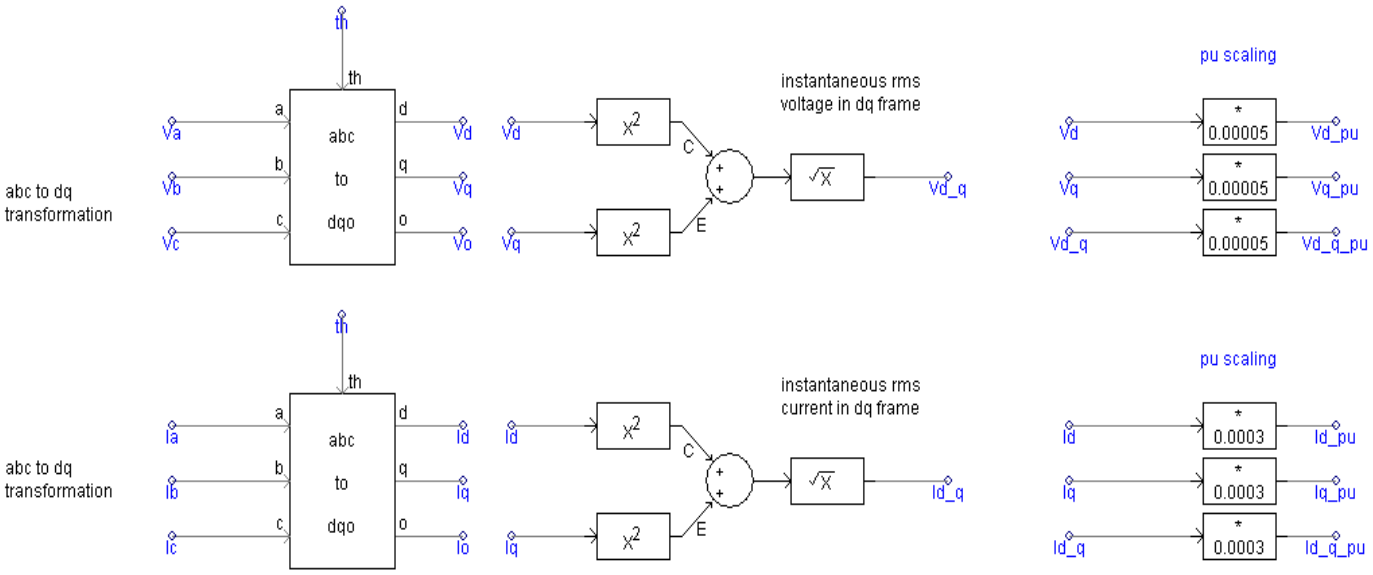


Figure 5.5: *abc to dq* transformations, *rms* measurements and *pu* conversions

The *abc to dq* transformation block consist of Parks transformation matrix coded in Fortran programming language. The angle *th* in Figure 5.5 is the transformation angle generated by the PLL in Figure 5.4.

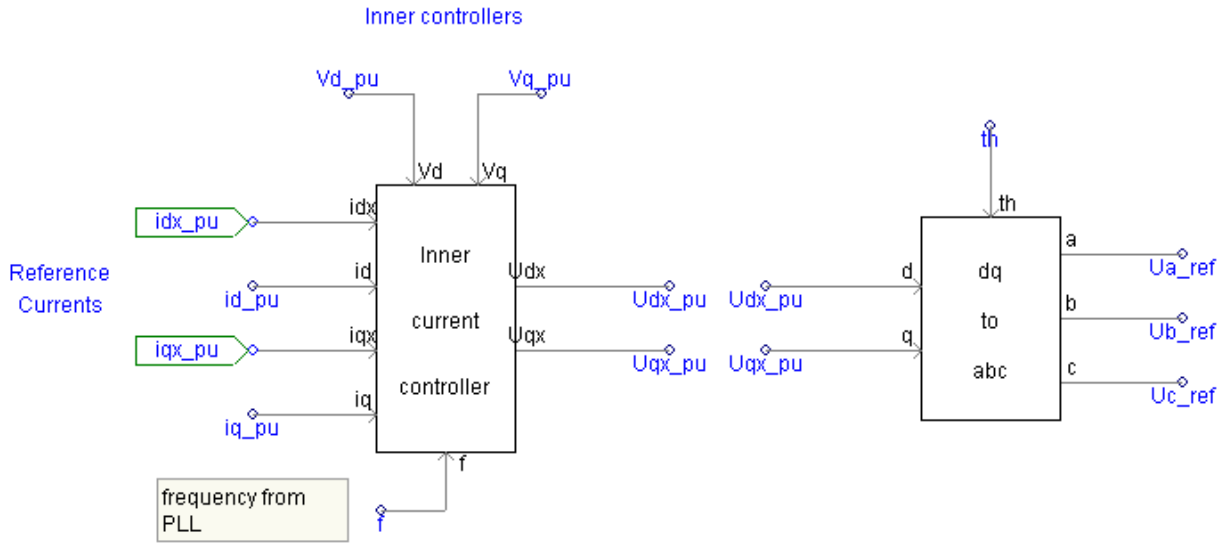


Figure 5.6: Inner current controller block diagram

idx_pu and *iqx_pu* shown in Figure 5.6 are reference current inputs for the active and reactive current controllers respectively.

5.3 Simulation of Inner Current Loop

The block diagram of the inner current loop and the equivalent model in PSCAD are shown in Figure 5.7 and Figure 5.8 respectively. All quantities in the control blocks are in p.u.

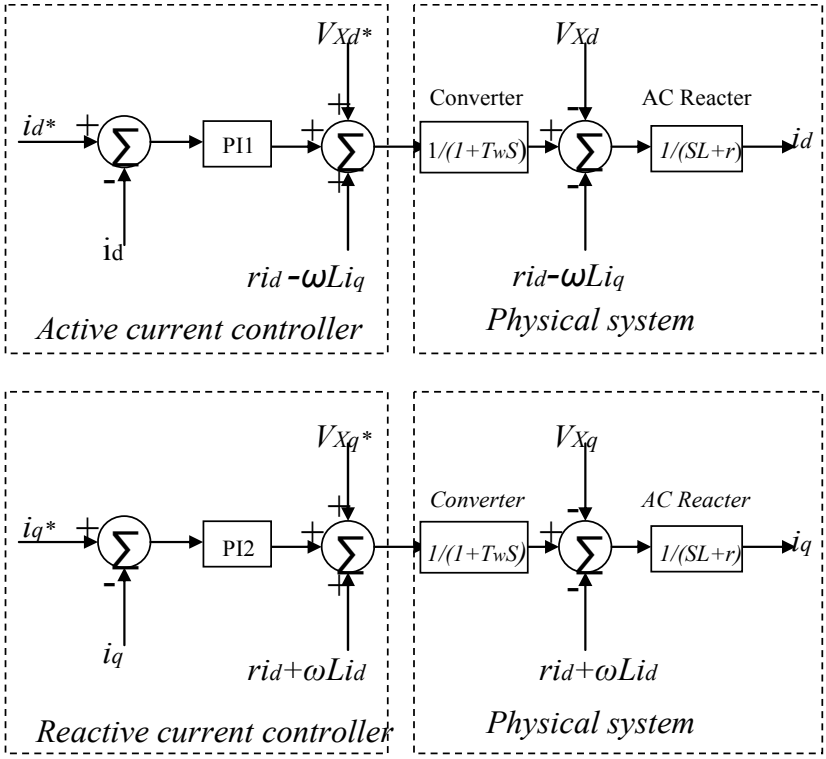


Figure 5.7: Block diagram of the inner current control loop

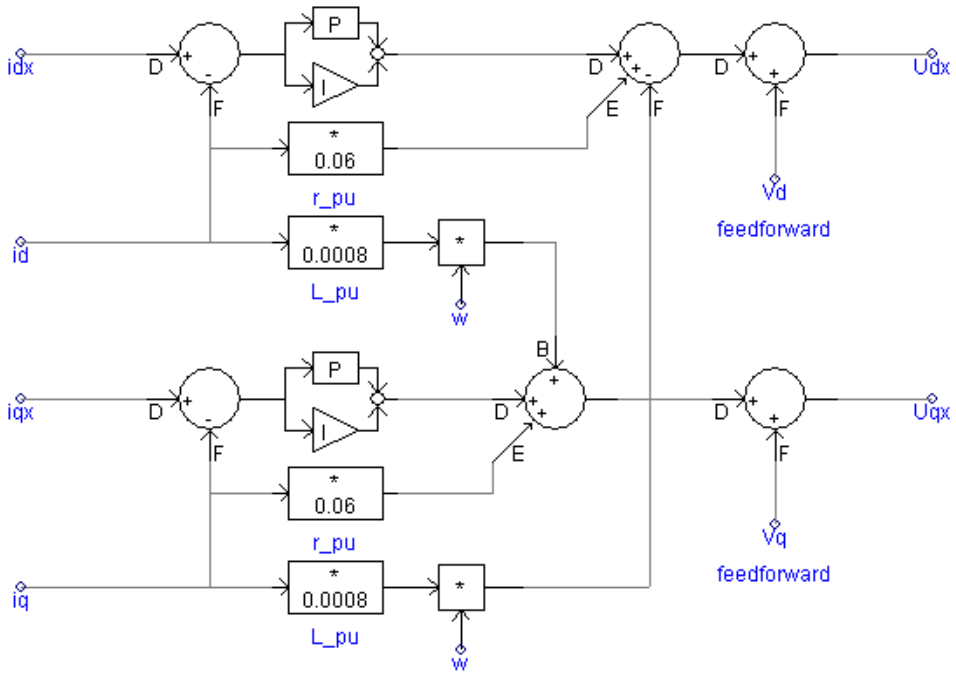


Figure 5.8: Implementation of inner current loop in PSCAD

The PI controllers for the inner current loop are determined by modulus optimum criterion. The time constant T_i is given by:

$$T_{i1} = \tau = \frac{L_{pu}}{r_{pu}} = \frac{L}{r} = \frac{0.0008}{0.06} = 0.0133 \quad \text{s} \tag{5.8}$$

A cut-off frequency of ω_c *=5000/2=2500Hz* was selected.

Therefore the proportional gain becomes:

$$K_{P1} = \omega_c T_i r (1 + T_a^2 \omega_c^2)^{1/2} \tag{5.9}$$

Substituting ω_c*=5000π rad/s,* T_i*=0.0133 s,* r*=0.01pu,* T_a*=10*$^{-4}$ *s* in to equation (5.9), we get

$$K_{P1} \approx 4 \tag{5.10}$$

With the specified PI controller parameters, the following step responses were found.

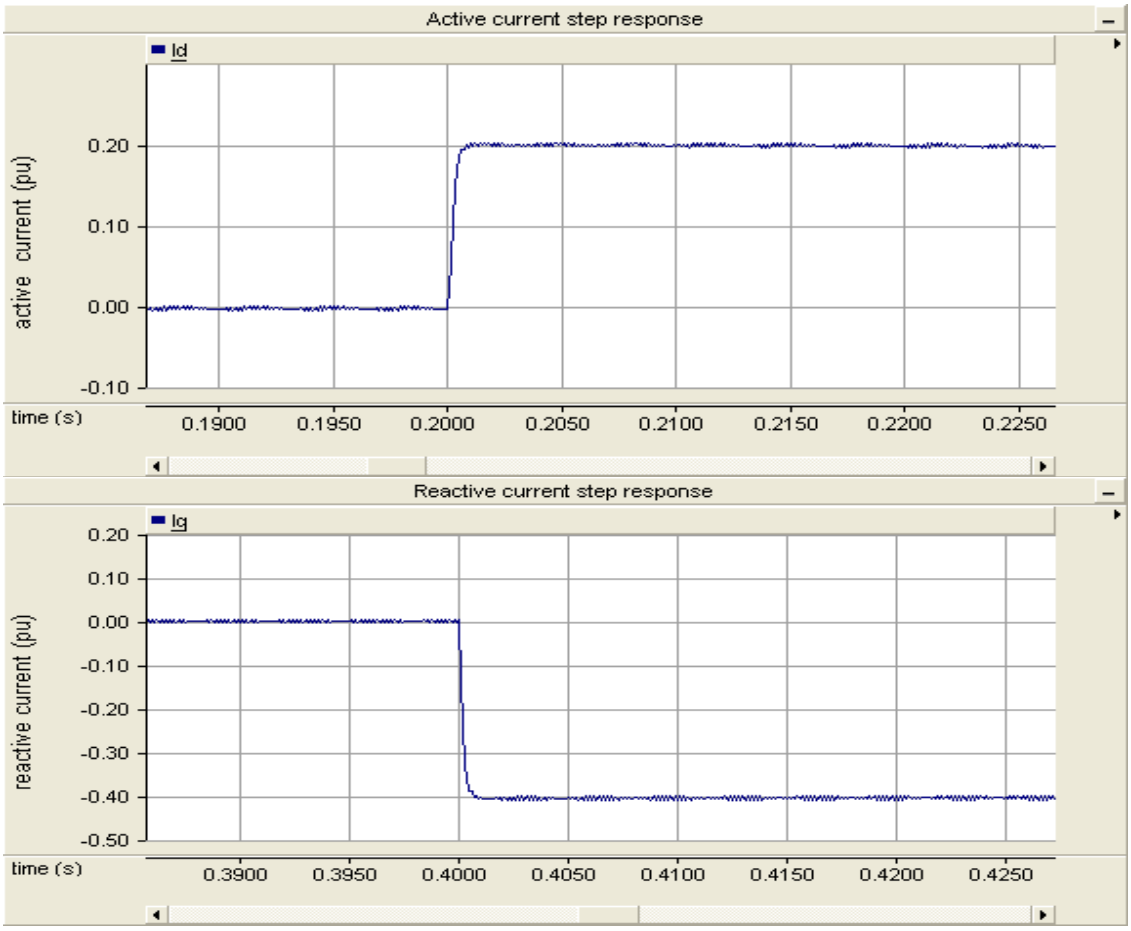


Figure 5.9: Response of the active and reactive current control loops for step inputs of active and reactive currents

As can be seen from Figure 5.9, the active and reactive power controllers resulted in a very fast response for a step change in the input references. The controllers resulted in only a delay of less than 1 ms which can be considered quite satisfactory.

5.4 Simulation of Active & Reactive Power Controllers

To study the control of active/reactive power flow in VSC-HVDC, a VSC HVDC connected to a stiff grid on the AC side and a DC voltage source on the DC side was used. This configuration is shown in Figure 5.10 below.

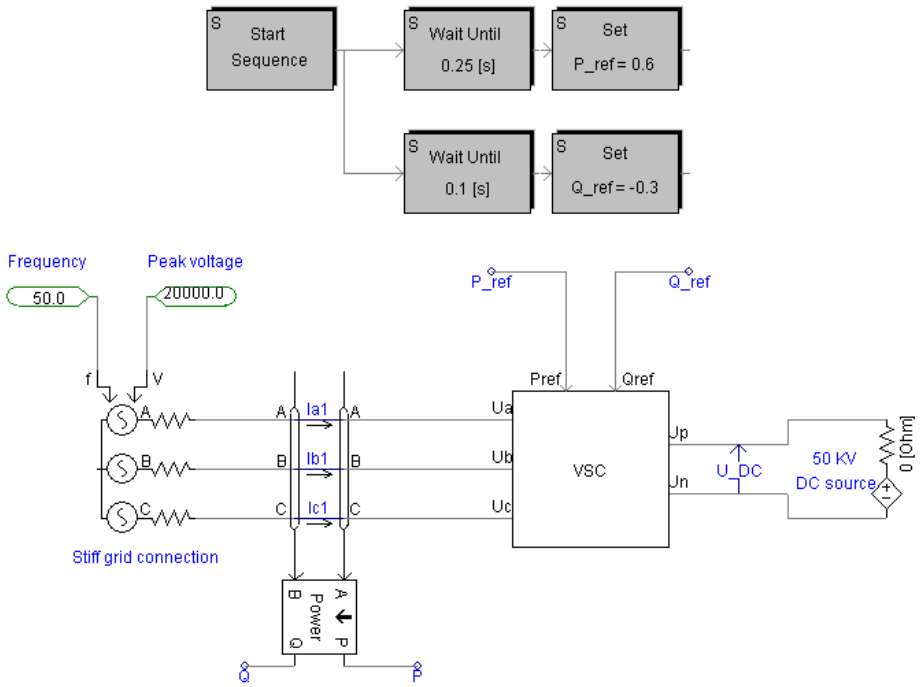


Figure 5.10: PSCAD model for the study of active/reactive power control.

The active and reactive power control structures, found with in the VSC block, are shown below.

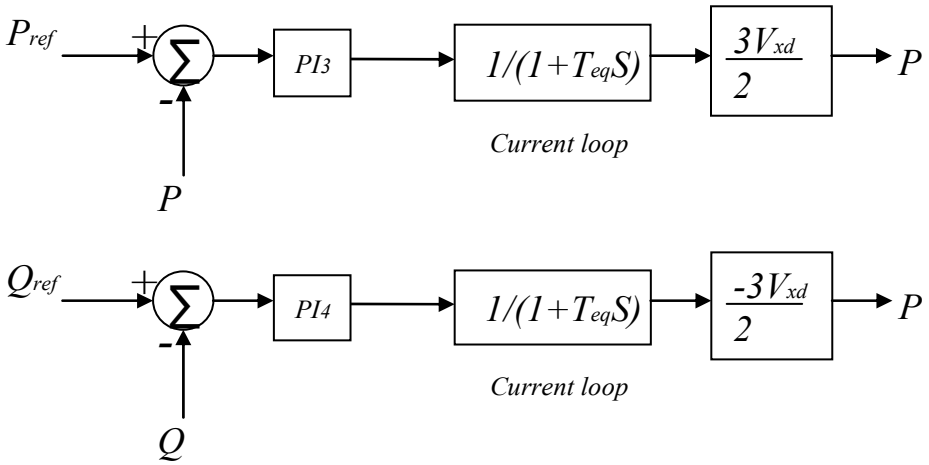


Figure 5.10: Active and reactive power control loops

The total delay in the current control loop is given by:

$$\begin{aligned} T_{eq} &= T_{i1} + \tau + T_{sw} \\ &= 0.0133 + 0.0133 + 0.0001 \\ &\approx 0.0267 \end{aligned} \tag{5.11}$$

A cut-off frequency of $\omega_c = 10\pi$ *rad/s* was selected for the power controllers. The gain of the closed current loop is approximated by unity.

Applying the modulus optimum criteria, the integral constant of the PI controller becomes:

$$T_{i3} = T_{i4} = T_{eq} \approx 0.0266 \quad s \tag{5.12}$$

The open loop gain of the outer controllers at cut-off frequency is given by:

$$O.L. = K_P\left(\frac{1+T_iS}{T_iS}\right)\frac{3}{2}V_{xd}\Big|_{s=j\omega_c} = 1 \tag{5.13}$$

Substituting T_i=0.0266, ω_c=10π rad/s, V_{xd}=1,

$$K_p = \frac{2T_i\omega_c}{3(1+(T_i\omega_c)^2)^{1/2}} = 0.43 \tag{5.14}$$

The following step responses were observed for the active/reactive power control loops with the calculated PI parameters.

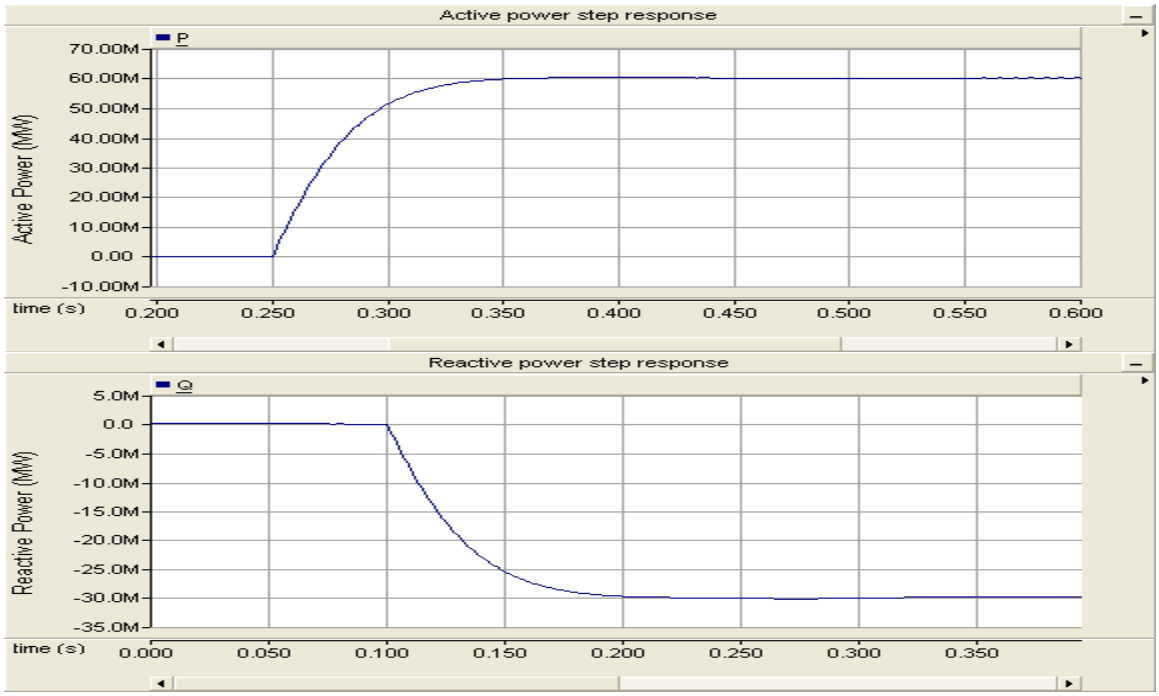


Figure 5.11: Step response of active and reactive power controllers

Figure 5.11 shows that the active /reactive power controllers have resulted in good response time and overshoot. The figure shows that the rise time for the active power controller and the reactive power controller are 0.1 s and 0.2 s respectively. There is negligible amount of overshoot in both cases. Therefore good performance of the active/reactive power controllers is achieved.

5.5 Simulation of DC Voltage Regulator

Two-terminal VSC-HVDC was used to study control of DC voltage under variation of active power flow. The following model in PSCAD consists of one VSC-HVDC terminal working in power control mode and the other one in DC voltage control mode.

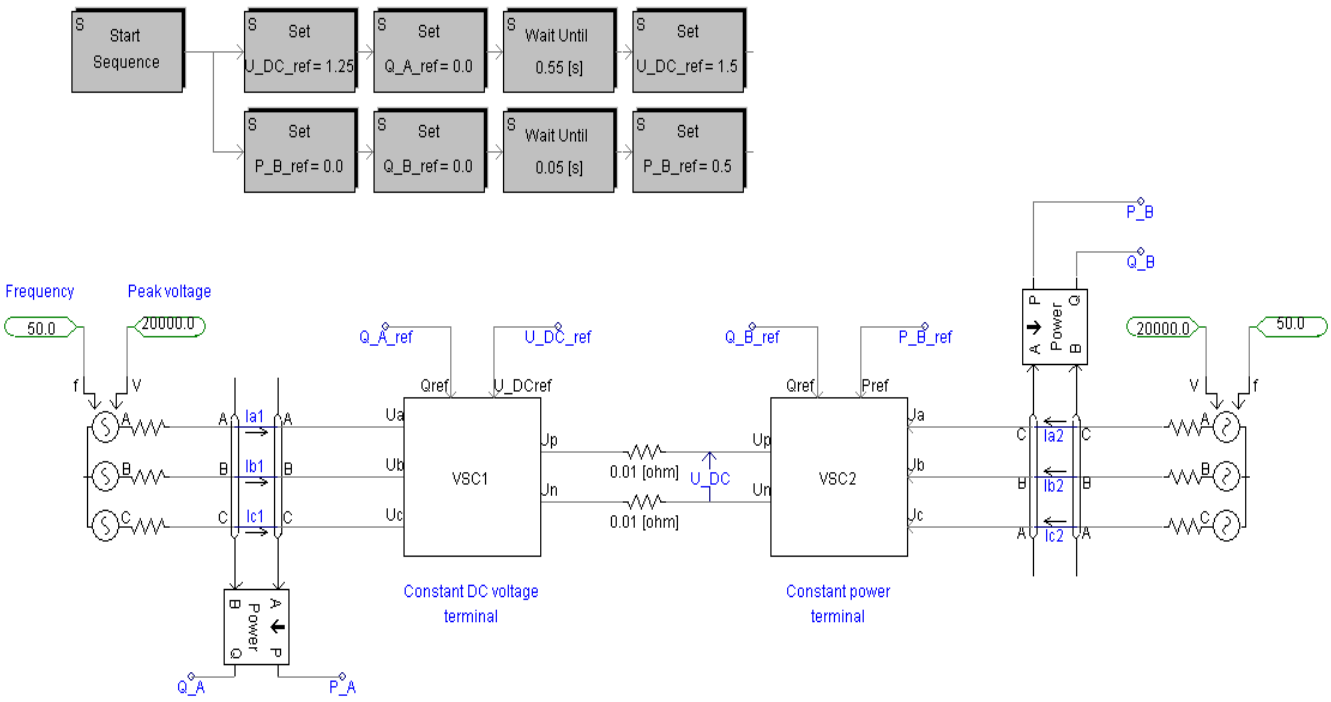


Figure 5.12: Two terminal VSC-HVDC connection

The DC voltage control structure embedded in the VSC- HVDC terminals is shown below.

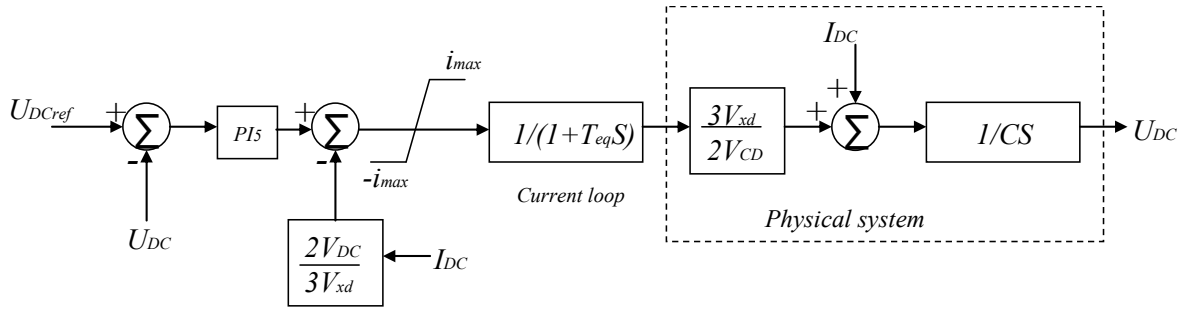


Figure 5.12: Control structures for DC voltage

T_{eq} was shown to be equal to 0.0266 in equation (5.12). The PI controller of the DC voltage regulator was tuned by trial and error. The following settings of the integral and proportional constants were found to give optimal step response.

$$K_{p5} = -3.36$$
$$T_{i5} = -0.05 \qquad (5.15)$$

Using these settings of PI controller, the DC voltage control loop was observed to have the following step response.

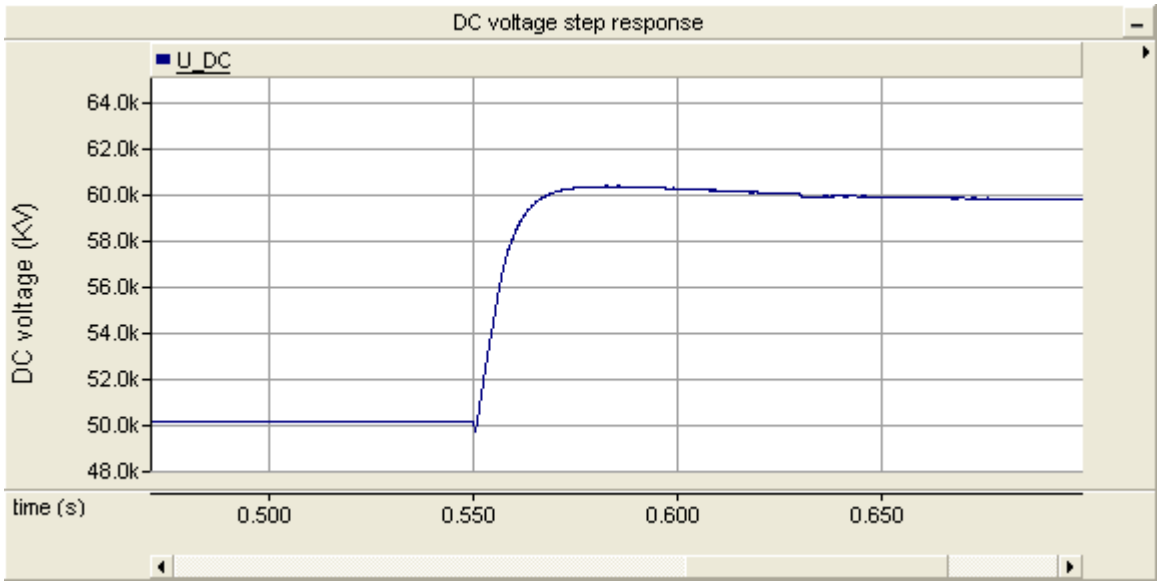


Figure 5.16: Step input response of the DC voltage regulator

As shown in Figure 5.16, the DC voltage controller has resulted in a rise time of 0.025 s and an overshoot of less than 2%. The performance can be considered as good enough.

5.6 Simulation of AC Voltage Control for Weak Grid Connection

In this thesis, the weak grid system was modeled by a line with series inductance and resistance connected to an ideal stiff grid system. A line impedance of $Z_L = r + j\omega L = (0.03 + j0.05)\,pu$ was assumed in the PSCAD model. The PSCAD model of the weak grid system is shown below.

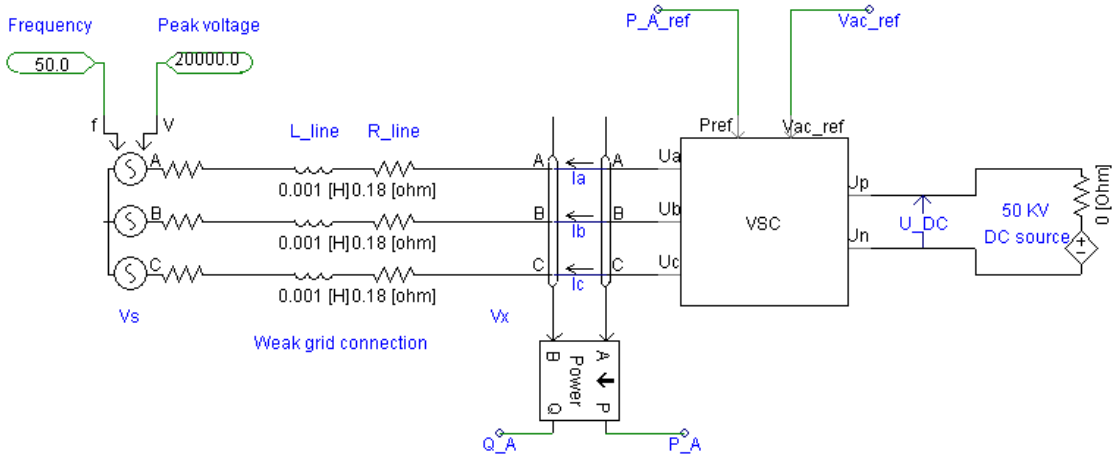


Figure 5.17: PSCAD model for weak grid connection

Due to the presence of considerable amount of series inductance and resistance, the AC voltage at the PCC varies with variations of active power flow when there is no reactive power compensation. This is shown in Figure 5.18.

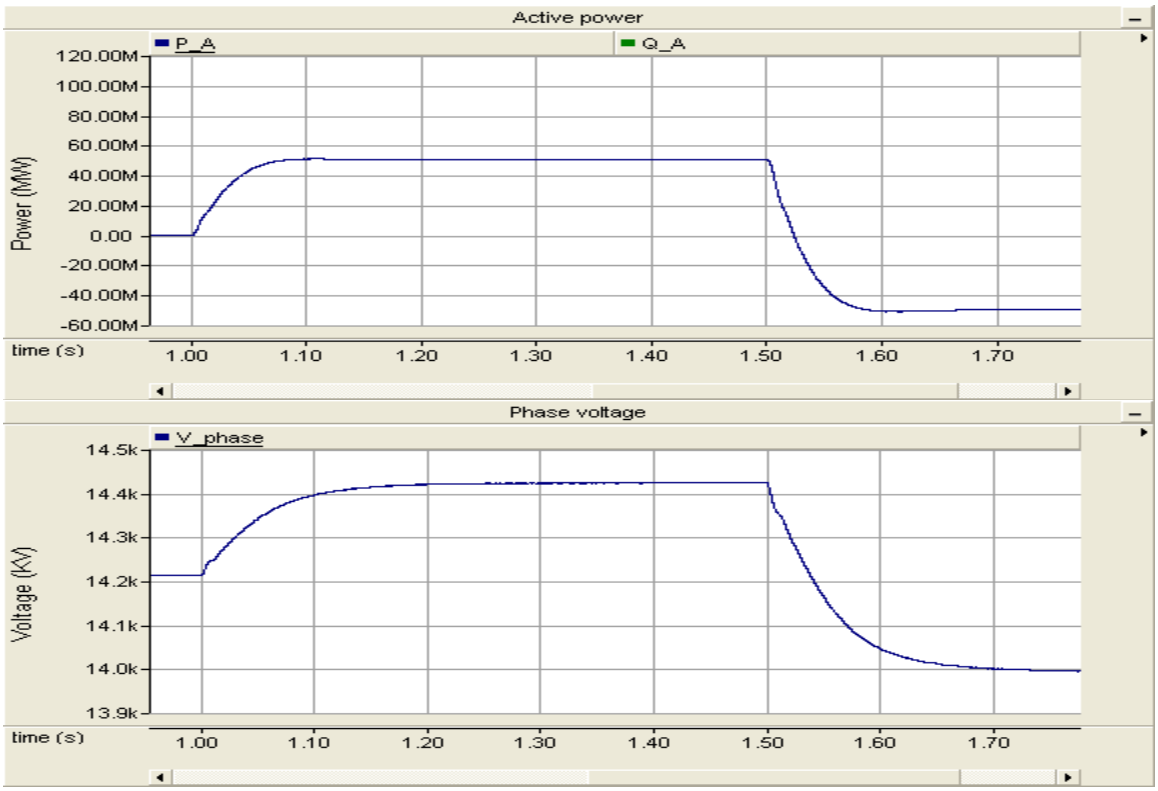


Figure 5.18: AC phase voltage variation with changing active power in the weak grid connection

As it was discussed in chapter 4, AC voltage in weak grid can be controlled by reactive power compensation. The AC voltage control diagram for weak grid connection is shown in Figure 5.19.

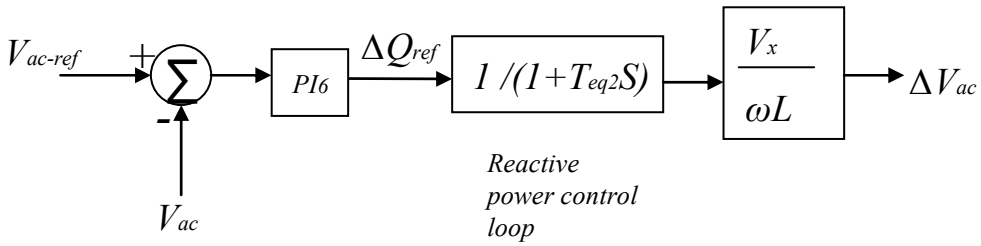


Figure5.19: Block diagram of closed loop AC voltage control loop

The PI regulators were tuned experimentally to the following values.

$$K_{p6} = 50$$
$$T_{i6} = 0.005 \qquad (5.15)$$

With PI parameter settings of equation (5.15), the following step response was observed for the AC phase voltage at the PCC.

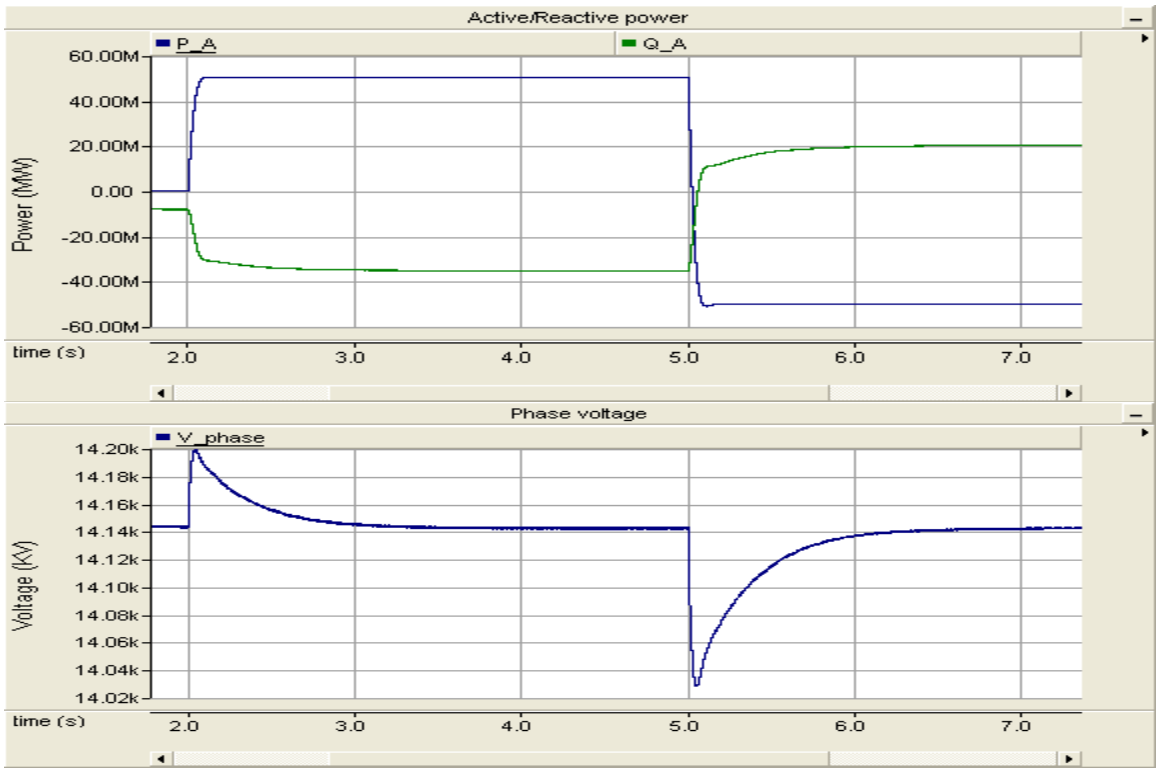


Figure 5.20: Response of AC phase voltage for a step change of active power flow when AC voltage regulation by reactive power compensation is used

In Figure 5.20 it can be seen that the reactive power (the plot in green in the top figure) is changed for every change in active power flow (the plot in blue in the top figure). This reactive power compensation brings the AC phase voltage (shown in the bottom plot) into its originally set reference voltage level. The response time is about 1 s but the steady state is zero. Although the delay is relatively larger, the total performance characteristic is acceptable for this specific application. The argument behind is that the AC voltage regulation is not so speed demanding as power or DC voltage regulation.

5.7 Simulation of AC Voltage Control for Passive AC Network

A two-terminal VSC-HVDC model was used to study control of AC voltage in passive AC connections. In the model one VSC-HVDC terminal was connected to a stiff grid and operated in constant DC voltage control mode and the other terminal was connected to passive loads with switches.

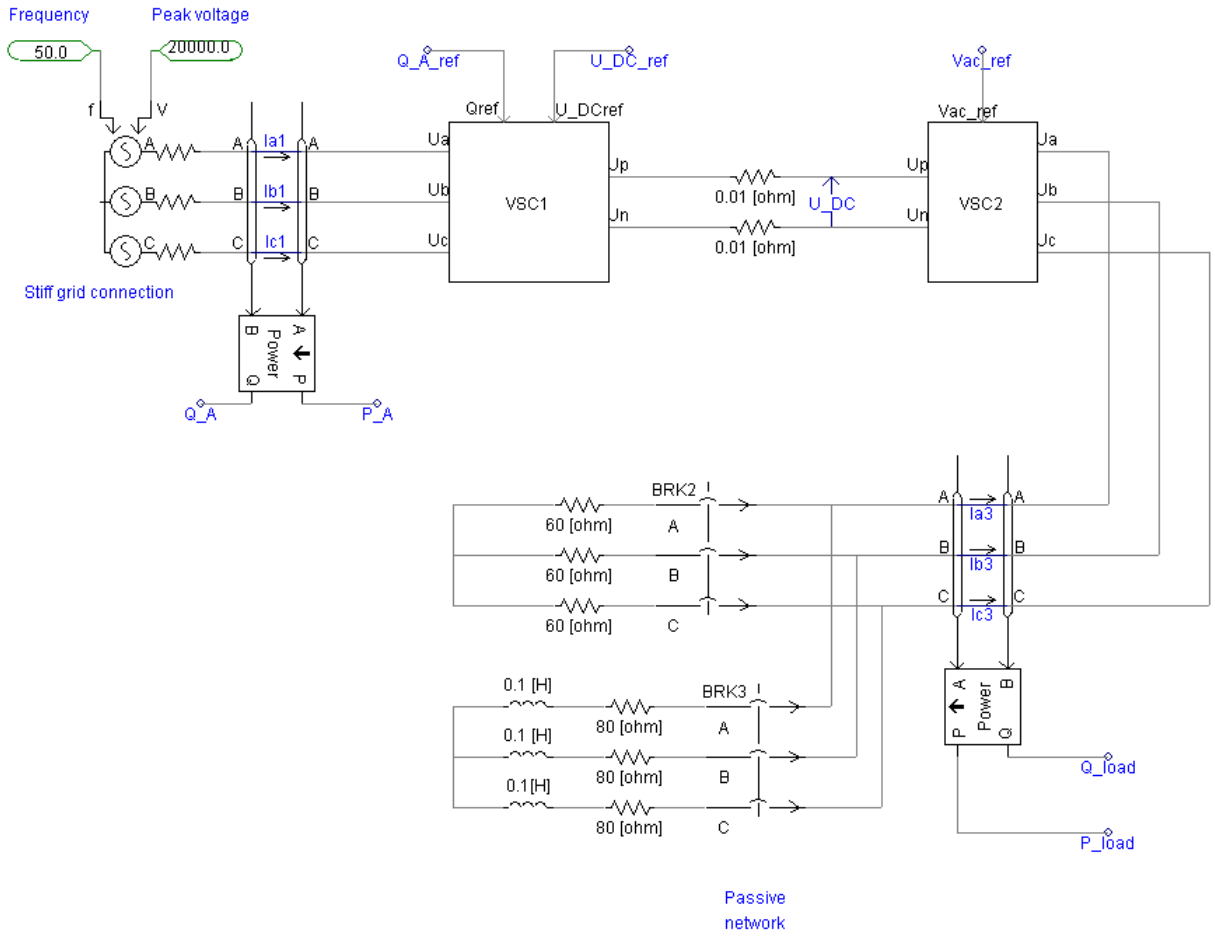


Figure 5.21: PSCAD model for studying control of phase voltage in passive AC systems

Direct control of modulation index (*m*) was applied for the VSC-HVDC connected to the passive AC network.

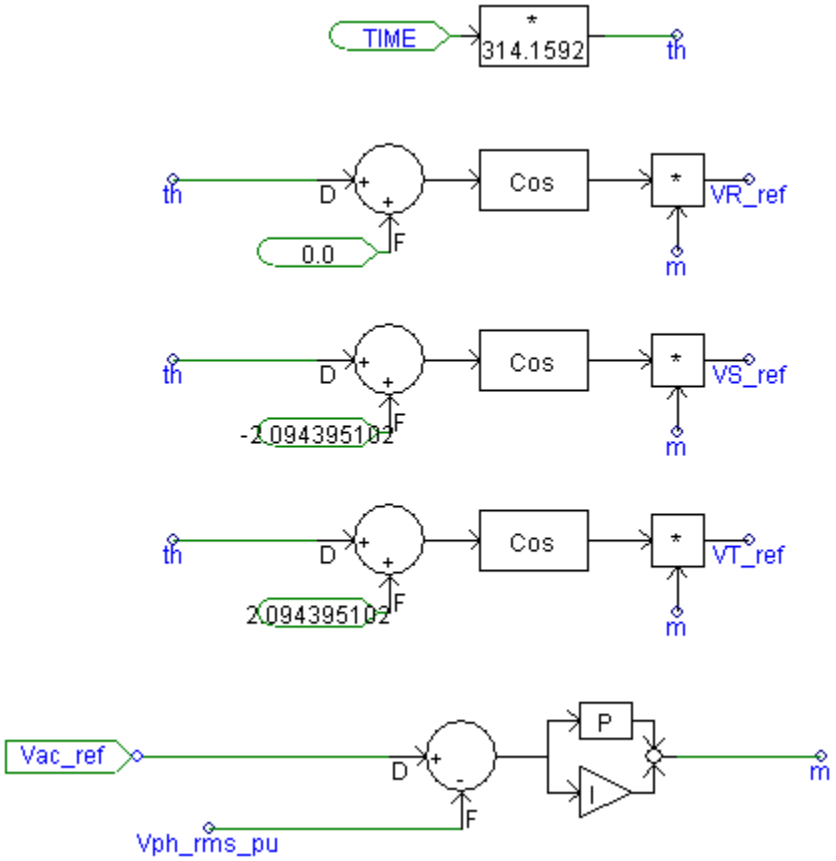


Figure 5.22: AC voltage regulation in passive network by control of modulation index (m)

The controller of AC voltage in VSC-HVDC connected to a passive AC network is shown below.

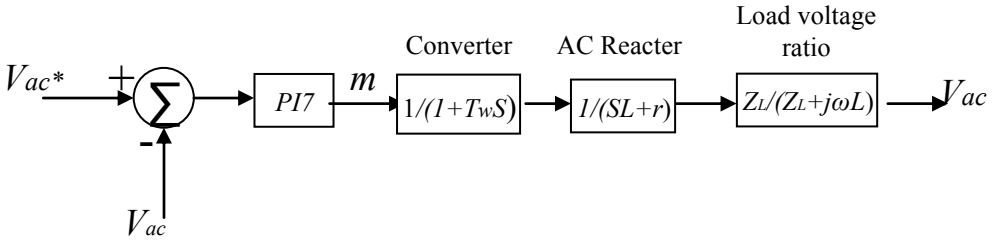


Figure 5.23: Block diagram of AC voltage control loop for passive load

The PI regulator was tuned experimentally to the following proportional and integral constants.

$$K_{p7} = 2.5$$
$$T_{i7} = 0.05 \qquad (5.16)$$

Like in the weak grid systems, in passive AC systems the voltage at PCC varies along with load switching on the AC side when fixed modulation index (m) is used. The AC voltage regulator keeps the AC voltage constant regardless of the power flow to/from the passive network. With the PI parameter settings of the voltage regulator as shown in equation (5.16), the following line to line rms voltage responses were observed when a load was switched-off at the passive AC network.

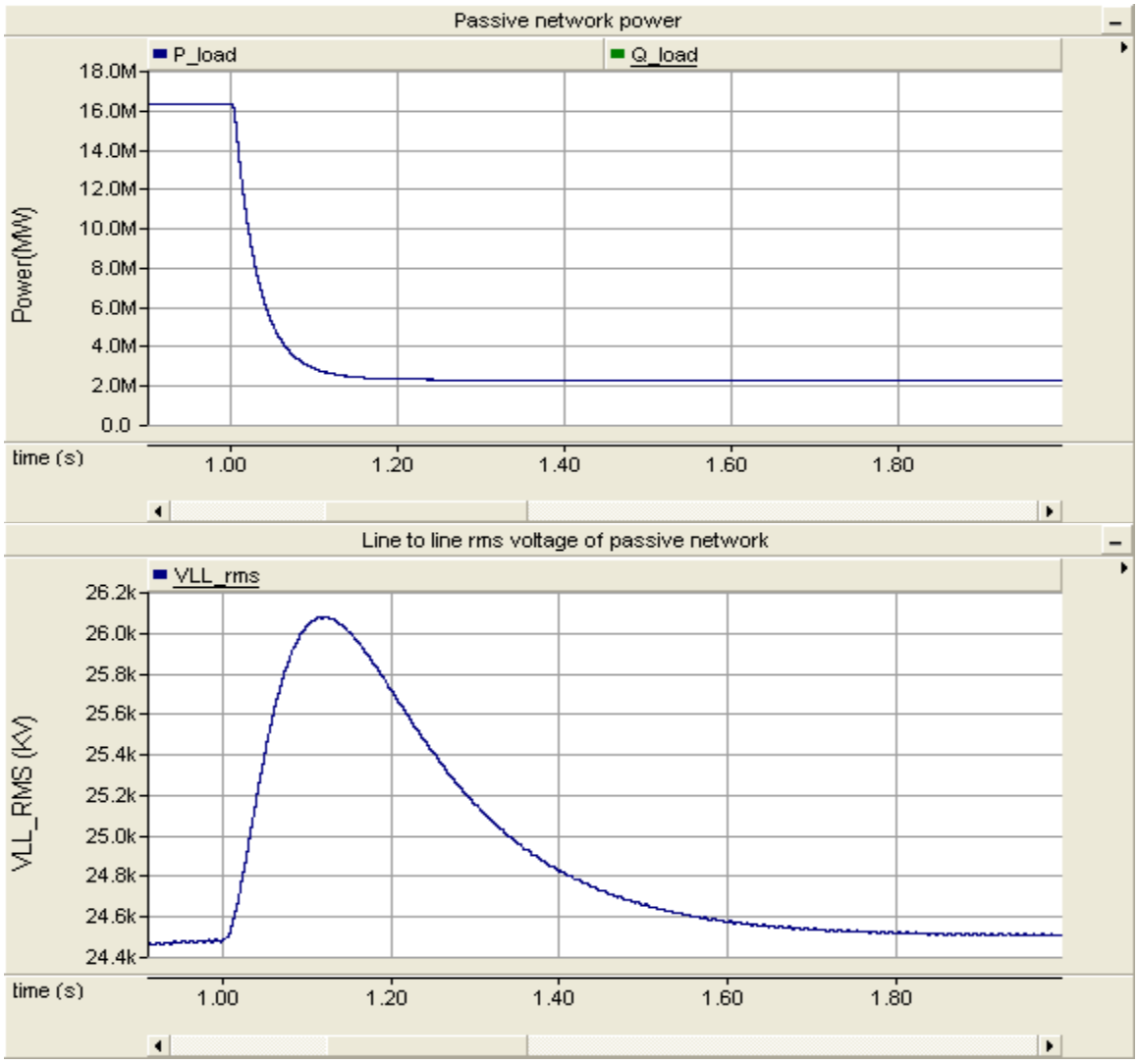


Figure 5.24: Response of line to line rms voltage in the passive network when a load was switched-off in the AC network.

From Figure 5.24 it is observed that the AC voltage regulator has a settling time of about 0.6 s and the steady state error is negligible.

5.8 Simulation of Frequency Control

A two-terminal VSC-HVDC model was used to study the operation of frequency droop control.

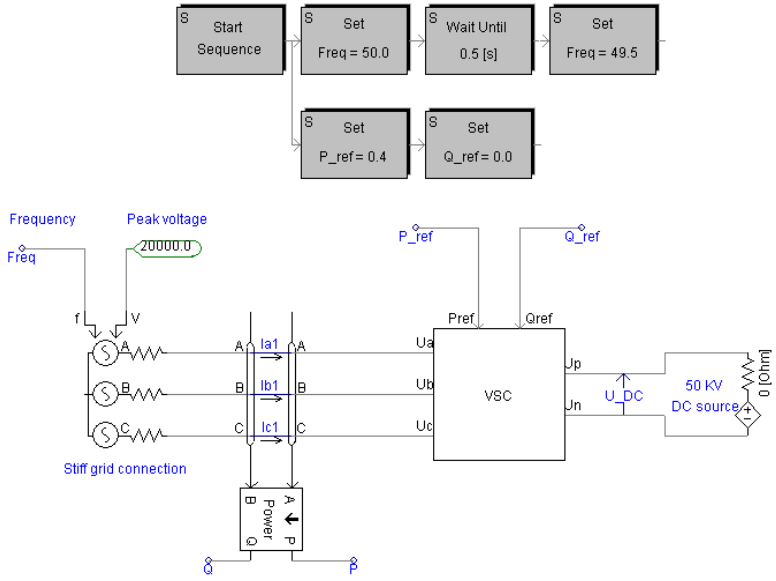


Figure5.25: PSCAD model for frequency droop control

A frequency bias factor *K=25* was selected for the simulation and the following response was observed for a step change in AC frequency.

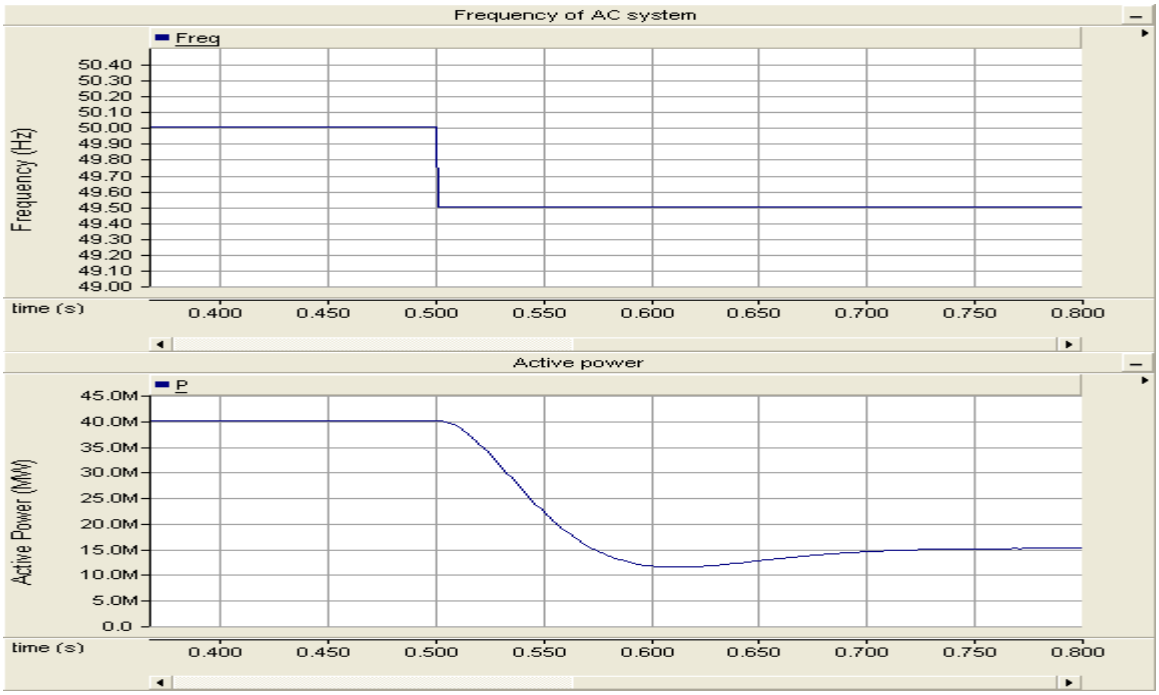


Figure 5.26: Response of the frequency control for a step change in frequency of AC system

5.9 DC Overvoltage Controller

The overvoltage controller suggested in chapter 4 is redrawn in Figure 5.27.

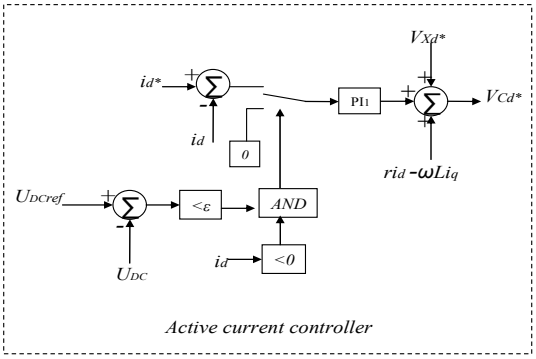


Figure 5.27: Overvoltage control scheme

An overvoltage tolerance margin of $\varepsilon=1\%$ was used for the over voltage controller. With the use of over voltage controller, the voltage spike was limited to +1KV as compared to +3KV with out the use of over voltage controller. This is shown in Figure 5.28.

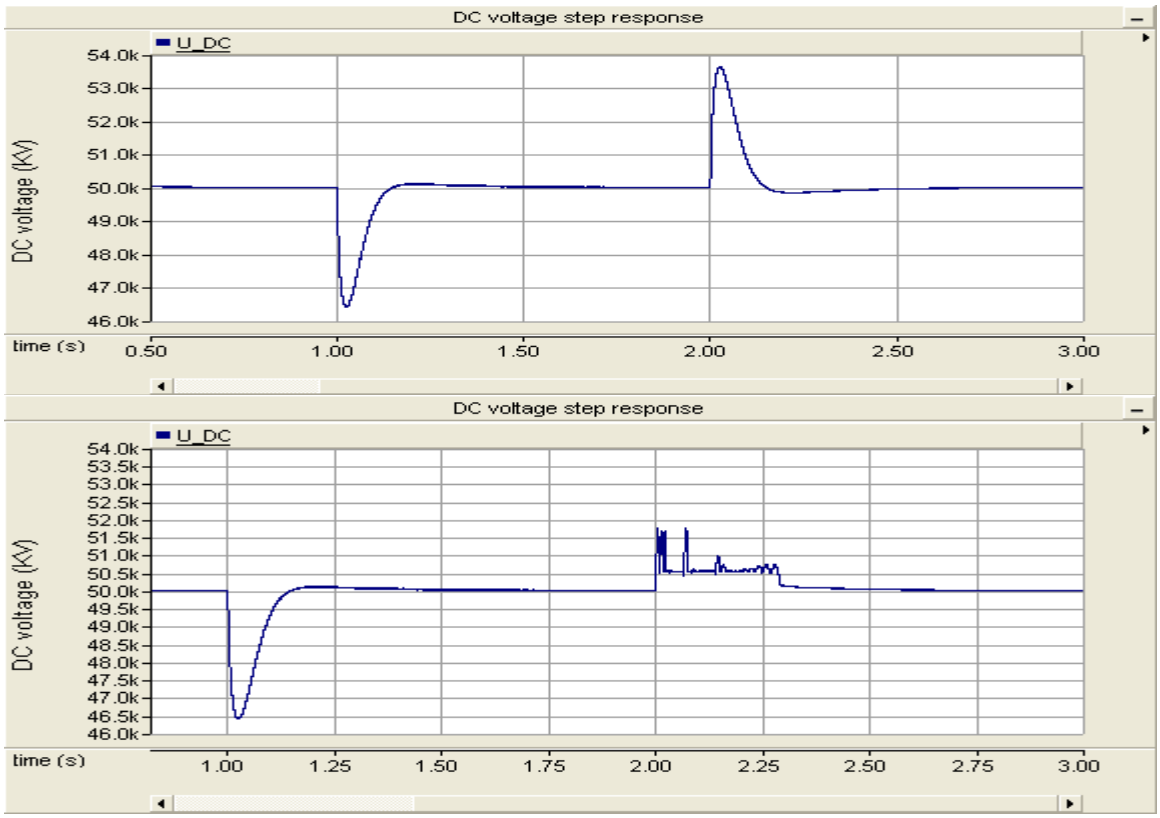


Figure 5.28: DC voltage spikes before and after the use of overvoltage control

5.10 Simulations of MTDC Systems

A four terminal MTDC system consisting of VSC-HVDC terminals connected to different type of AC systems was modelled in PSCAD and its operation was studied with simulations. As it was described in chapter 3, an MTDC system should have at least one VSC-HVDC terminal operating in constant DC voltage control mode. Hence in the four terminal model shown in Figure 5.30, terminal A is assigned to be the DC voltage regulating terminal.

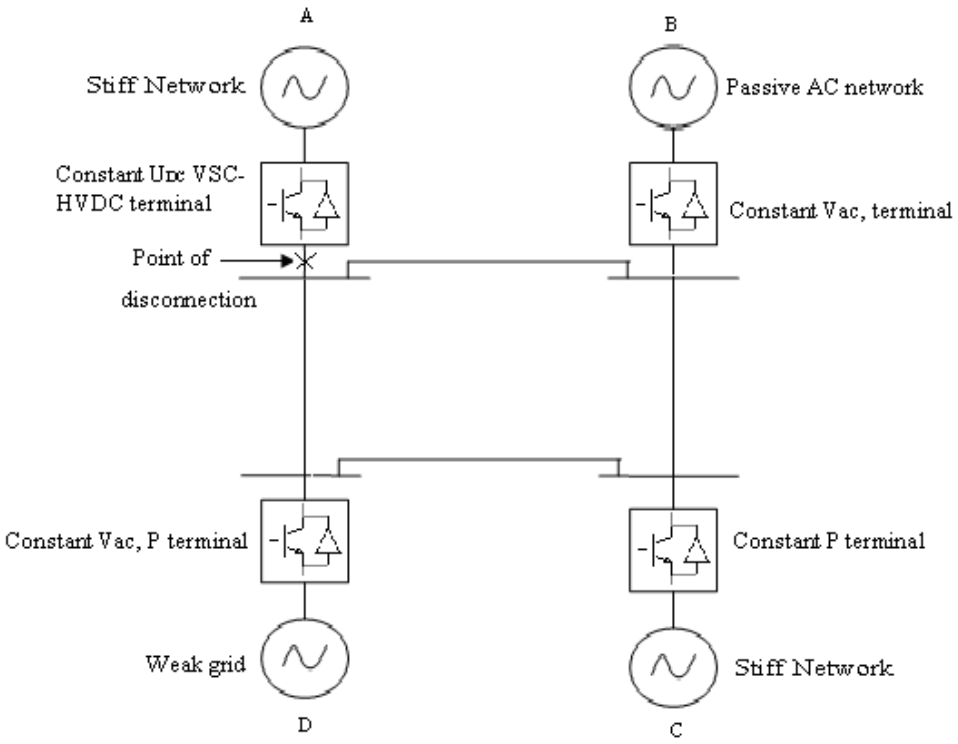


Figure 5.30: Four terminal MTDC model

As shown in Figure 5.30, terminal A and C are connected to stiff grids where as terminals B and D are connected to passive grid and weak grid respectively. From control mode aspect terminals C and D operate in constant power mode and terminal B regulates only its AC voltage level.

The sequence of events listed in Table 5. 2 was used when running the simulation.

Table 5.2 Sequence of events assumed in simulation

Time (s)	Events
0	Initial settings: $U_{A\text{-}DCref}$=50KV, $V_{B\text{-}LLref}$=24.5KVrms, P_{Cref}=0MW, P_{Dref}=0MW
3	A load of 10MW, 1pf switched on at passive AC network of terminal B
7	Additional load of 11.8 MVA, 0.8pf switched on at passive AC network of terminal B
12	Set: P_{Dref}= -50MW (rectifier mode)
16	Set: P_{Cref}= 40MW (inverter mode)
19	Set: Q_{Cref}= 30MVA (reactive power production)
24	Disconnect terminal A from MTDC
29	Switch off 20MW load, 1pf from passive AC network at terminal B

Simulation results are shown in Figures 5.31-5.37.

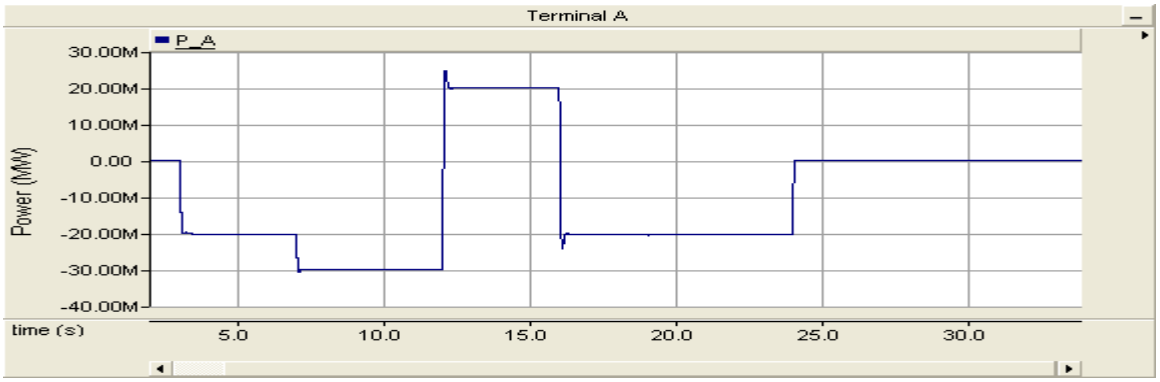


Figure 5.31: Active and reactive power flow profile of terminal A

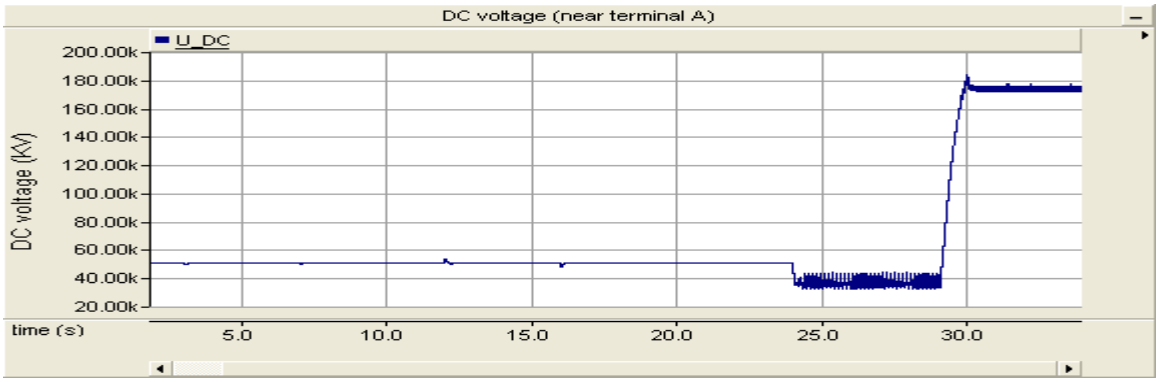


Figure 5.32: DC voltage near terminal A

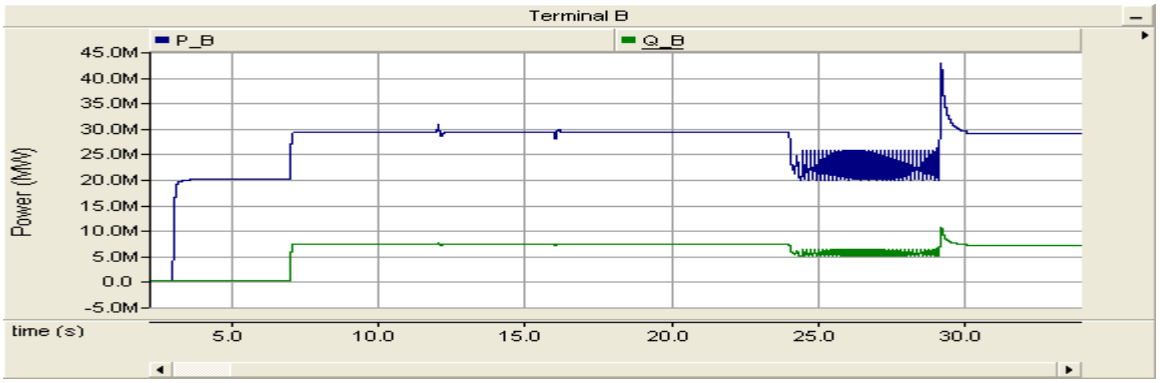


Figure 5.33: Active and reactive power flow profile of terminal B

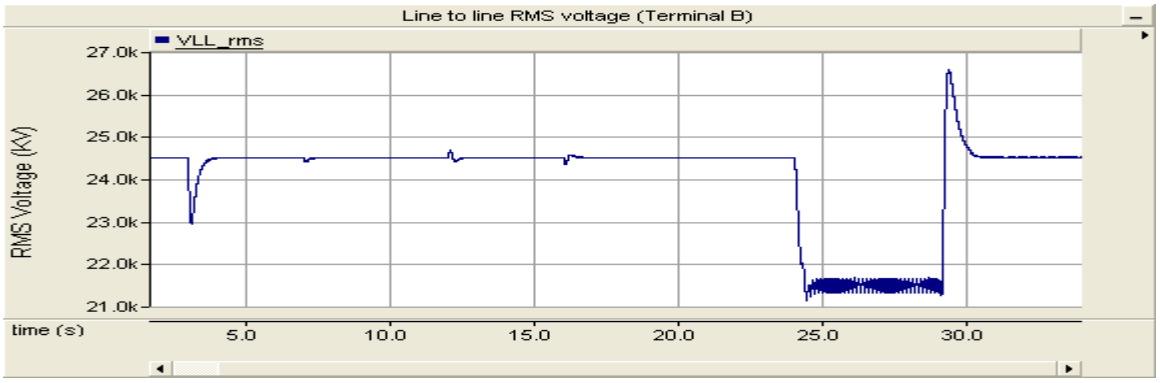


Figure 5.34: AC voltage profile of terminal B

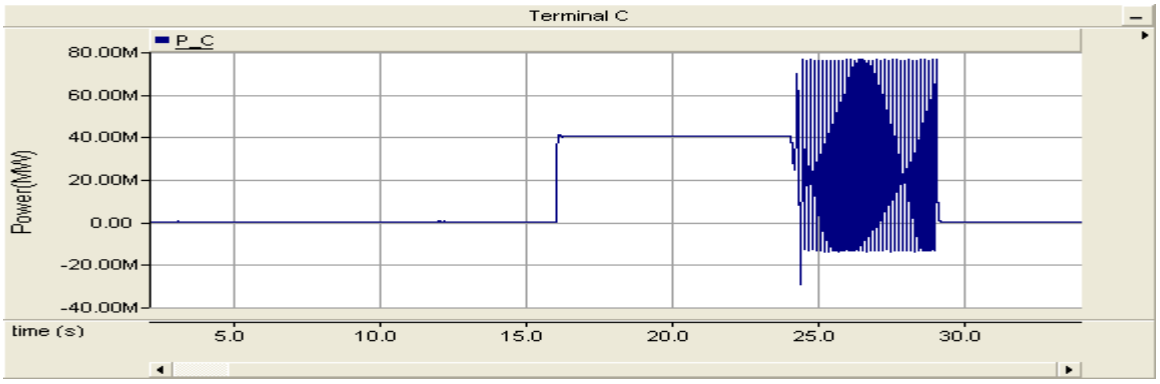


Figure 5.35: Active and reactive power flow profile of terminal C

Figure 5.36: Active and reactive power flow profile of terminal D

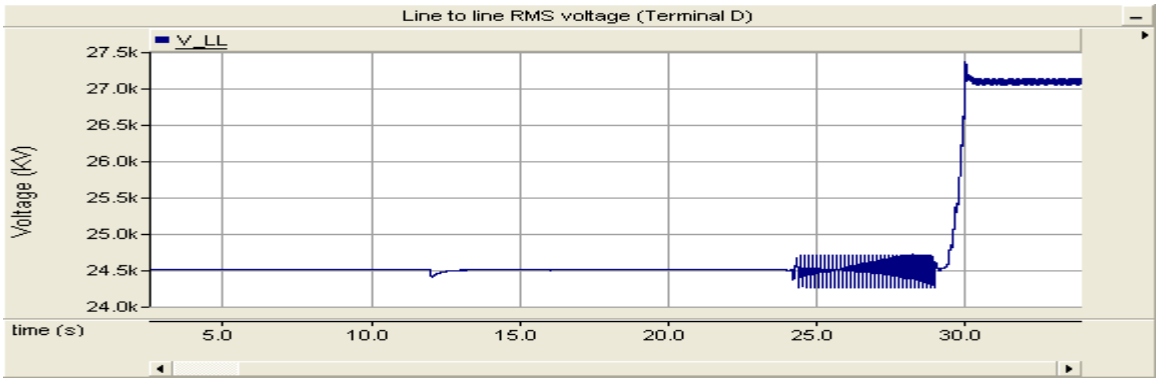


Figure 5.37: AC voltage at terminal D

As the simulation results indicate, the MTDC system works fine as long as the DC voltage regulating terminal (i.e. terminal A) is connected to the MTDC system. This is observed most clearly in the DC voltage plot (Figure 5.32).

Figure 5.32 shows that the DC voltage remained constant enduring large disturbances namely: load switching ON/OFF and changes in references of active power controllers. This was true until terminal A was disconnected at *t=24 s*, after then there was deficit of power inflow into the MTDC which in turn caused the DC voltage to drop down from 50KV to around 35KV.

Disconnection of terminal C at *t=29 s* caused excess of power inflow into the MTDC network which inturn resulted in DC voltage rise up from 50KV to more than 175KV. The large oscillations in the plots indicate that the MTDC system will be unstable without the presence of a DC voltage regulating terminal.

5.11. Simulation of MTDC with Voltage Margin Control

The same four-terminal MTDC was used here but now voltage margin control was implemented at terminals C and D. Also the same sequence of events was used as in the previous case. The DC voltage references are shown in Table 5.3.

Table 5.3: References of DC voltage controllers

VSC-HVDC terminal	DC voltage reference
A	50KV
B	-
C	48KV
D	52KV

It would be sufficient to observe the DC voltage plot to determine whether an MTDC system is stable or not. Hence from the simulation of theMTDC model with voltage margin control, the DC voltage-time plot is shown below. The complete simulation results are found in the appendix.

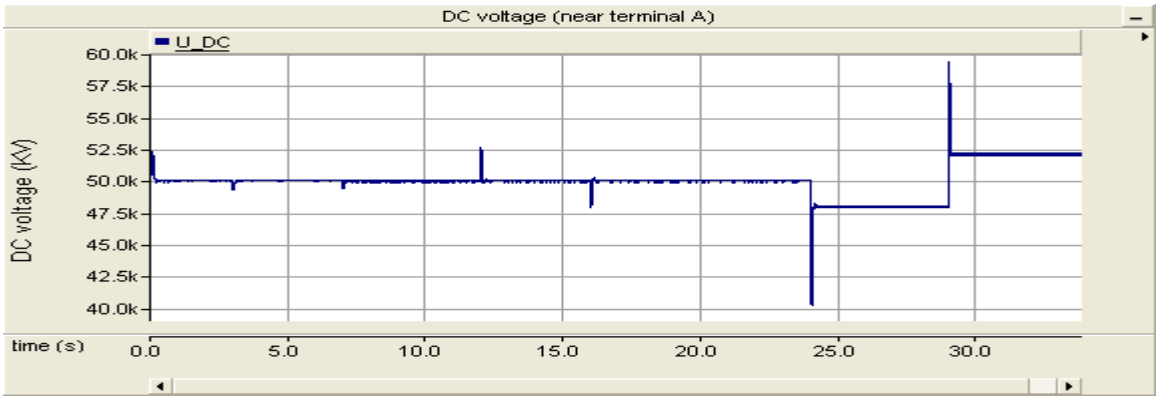


Figure 5.38: DC voltage vs. time plot for MTDC with voltage margin control

In Figure 5.38, it is seen that with the use of voltage margin control the DC bus voltage is limited to maximum and minimum levels of 52 KV and 48 KV respectively.

The voltage margin control has effectively eliminated the excessive voltage rise/ drop problem caused by loss of connection to the DC slack bus (terminal A).

5.12 Simulation of MTDC with Voltage Margin and DC Droop Control

Now a fifth VSC-HVDC terminal was added to the former four-terminal MTDC model. The newly added terminal (E) is desired to participate in the DC voltage regulation together with terminal A. This means that the reference input of the DC voltage controller at terminal E must be the same as that of terminal A.

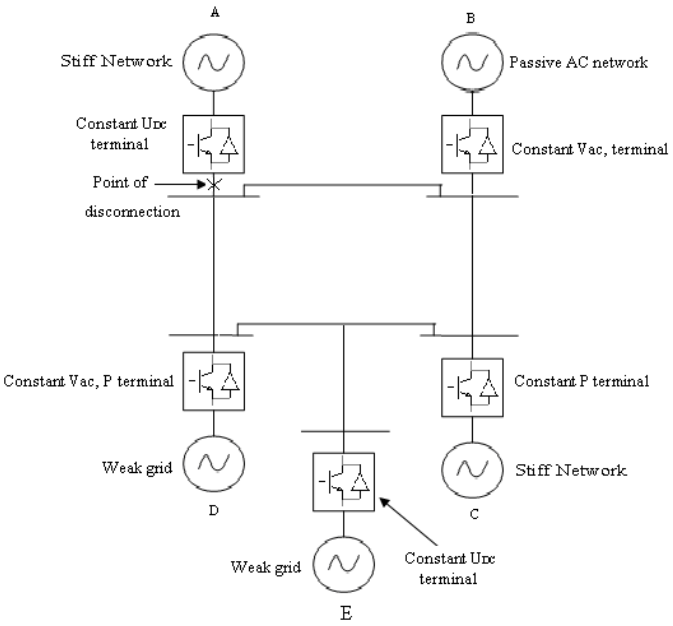


Figure 5.39 : Five-terminal MTDC

A 33% of participation factor for terminal E and 67% for terminal A was assumed randomly.

$$\lambda_E = \frac{1}{3} = \frac{K_E}{K_E + K_A}$$
$$\rightarrow K_E = \frac{1}{2} K_A \qquad 5.17$$

where K_A and K_E are proportional gains of the DC voltage controllers at terminal A and E respectively. The participation factor indicates the active power rectified/inverted by a terminal as

a fraction of the total power demand/supply in the MTDC system to keep the DC voltage constant.

As it was discussed in Chapter 4, no integrator is used with DC voltage droop control. A gain of K_A=*-2* was used for terminal A and *K=-1* was used for terminals C, D and E. The DC voltage reference settings are shown in Table 5.4.

Table 5.4: References of DC voltage controllers

VSC-HVDC terminal	DC voltage reference
A	50KV
B	-
C	48KV
D	52KV
E	50KV

With the use of voltage droop control and the same sequence of events as before, the following plots were obtained. The complete simulation results are available in the appendix.

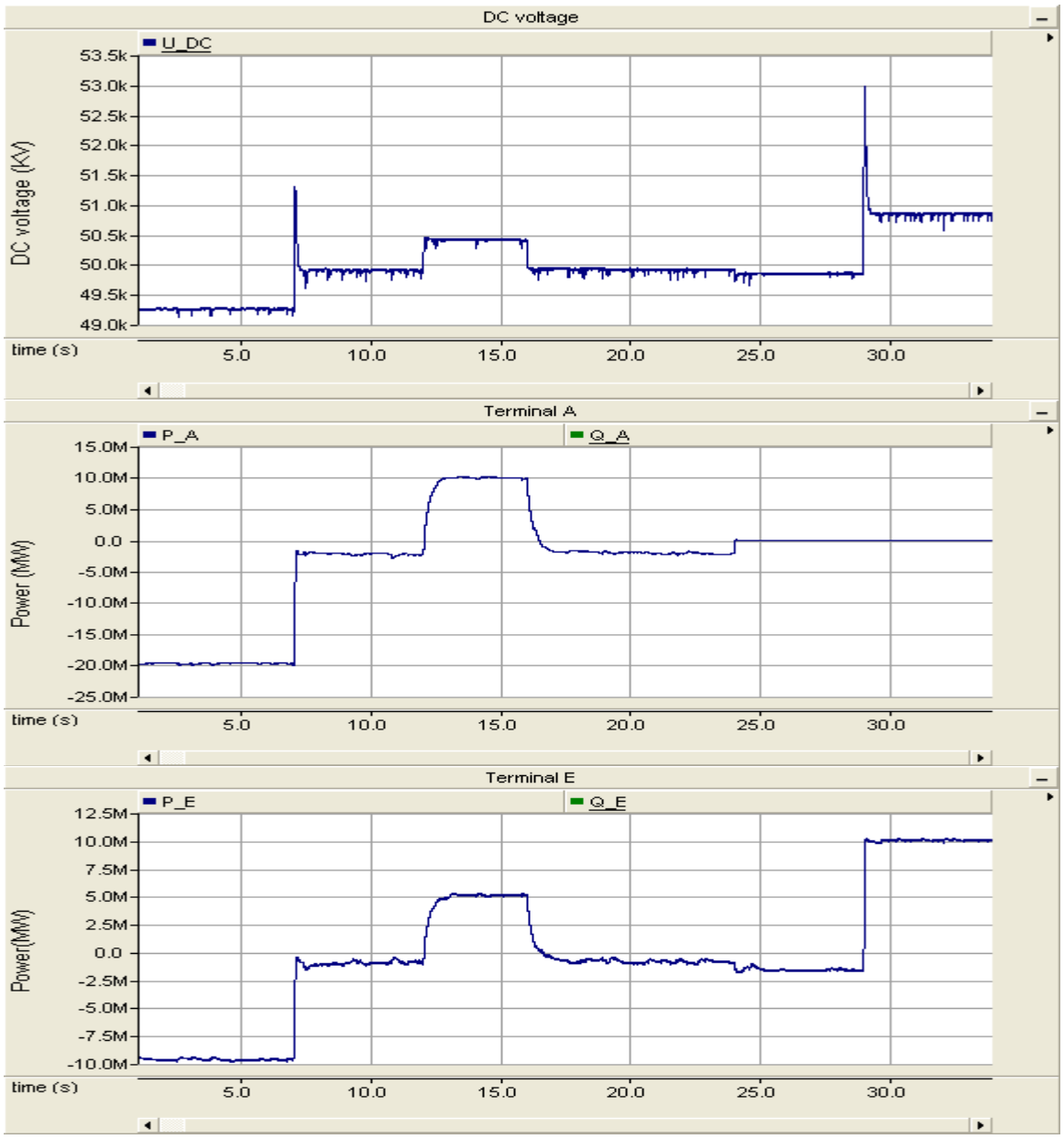


Figure 5.40: Power sharing of DC voltage regulating terminals by DC voltage droop control

From the DC voltage plot in Figure 5.40 it can be seen that the MTDC is affected only little by the disconnection of terminal A at *t=24 s* and by the disconnection of terminal C at *t=29 s.* The steady state DC voltage was kept with in 49KV and 51KV limits.

It was said that the main advantage of the DC voltage droop control is to use two or more terminals in parallel for DC voltage regulation. This is vividly seen from the active power plots of terminals A and E in Figure 5.40. As the figure shows the P_A/P_E ratio remained approximately 2

until terminal A was disconnected from the system. This agrees with the participation factor ratio determined in equation (5.17).

The simulations results lead to the conclusion that voltage margin method merged with DC voltage droop control results in the most robust and reliable operation of MTDC systems.

Chapter 6

Conclusions and Suggested Future Works

6.1 Conclusions

In this thesis control strategies for VSC-HVDCs connected to different types of AC networks were developed. These control strategies were consolidated to develop a four terminal MTDC system.

Simulation results has shown that operation of MTDC is possible with one VSC-HVDC terminal working in DC voltage control mode and the others working in P-control mode or connected to passive AC network. It was observed that this control strategy results in DC voltage collapse/ excessive DC voltage during loss of connection to the DC voltage regulating terminal.

The *voltage margin control* resulted in reliable operation of MTDC during loss of voltage regulating terminal by providing redundancy of voltage controllers at different terminals offset by voltage margins. It was seen that with the use of the voltage margin method, there was no need for communication between terminals for system recovery during terminal disconnections.

DC voltage droop control, together with voltage margin method, enabled sharing of load among two or more DC voltage regulating terminals operating in parallel. The load sharing is determined by preset participation factors of the terminals for DC voltage regulation.

The simulations results lead to the conclusion that *voltage margin method merged with DC voltage droop control* results in the most robust and reliable operation of MTDC systems with out the need for fast communication system between terminals.

6.2 Suggested Further Works

In the MTDC models of this thesis, only one-stage voltage margin method was implemented. Two-stage voltage margin method was discussed but not used. The operation of MTDC with two-stage voltage margin control should be simulated and studied.

L-filter was used in the VSC models of this thesis work. The use of L-C filter reduces the size of the filter. But it also needs active damping against resonance, which is a disadvantage of the L-C filter. A proper L-C filter with resonance control should be used with the VSCs and its impact on operation of the MTDC system should be studied.

In this thesis only ideal three phase AC sources were used for the stiff grid systems. In further work generator and turbine models should be used to study AC/DC interactions of MTDC systems.

Fault analysis & system protection and system stability of MTDC systems are other important issues that must be investigated in further work.

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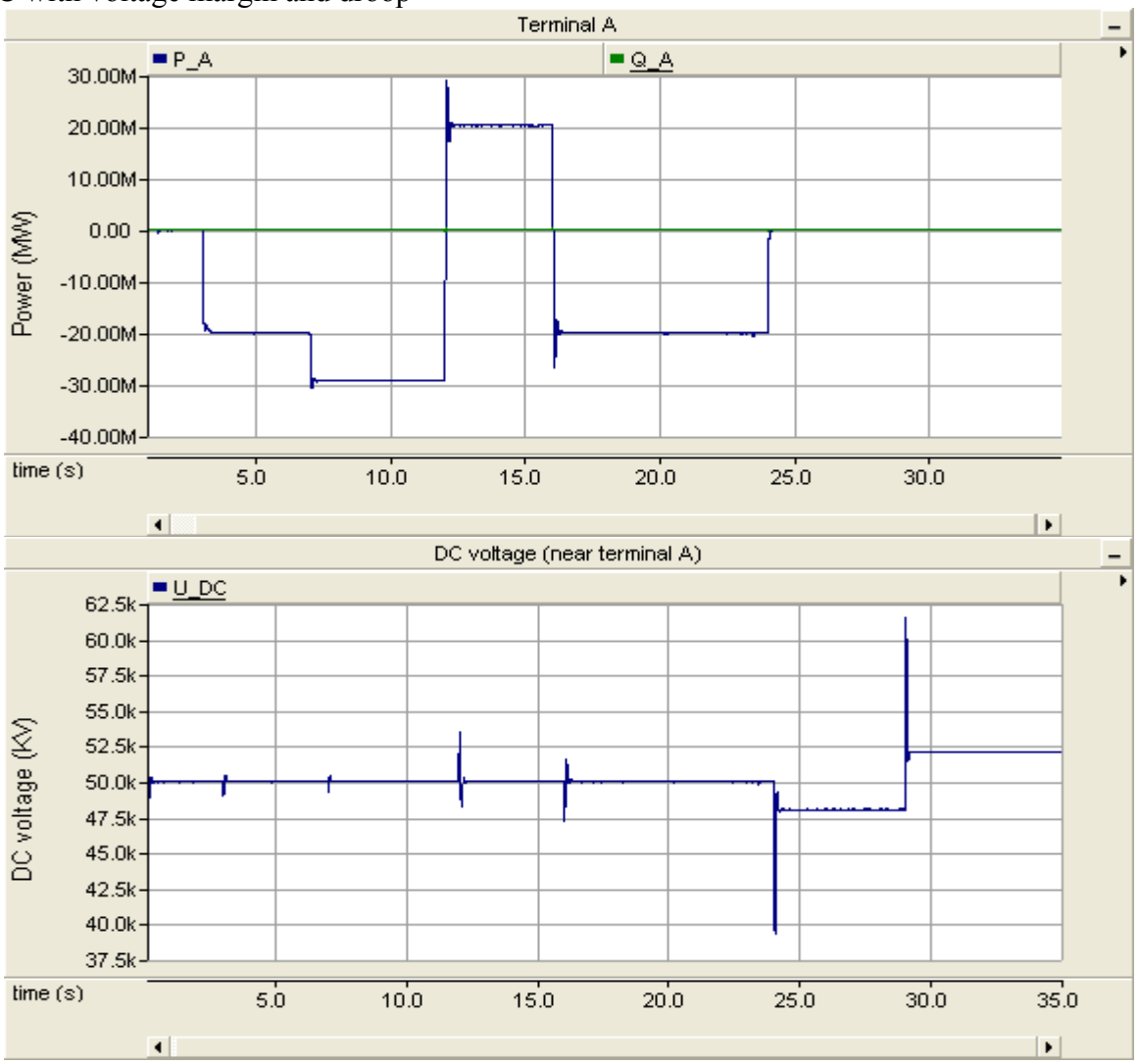
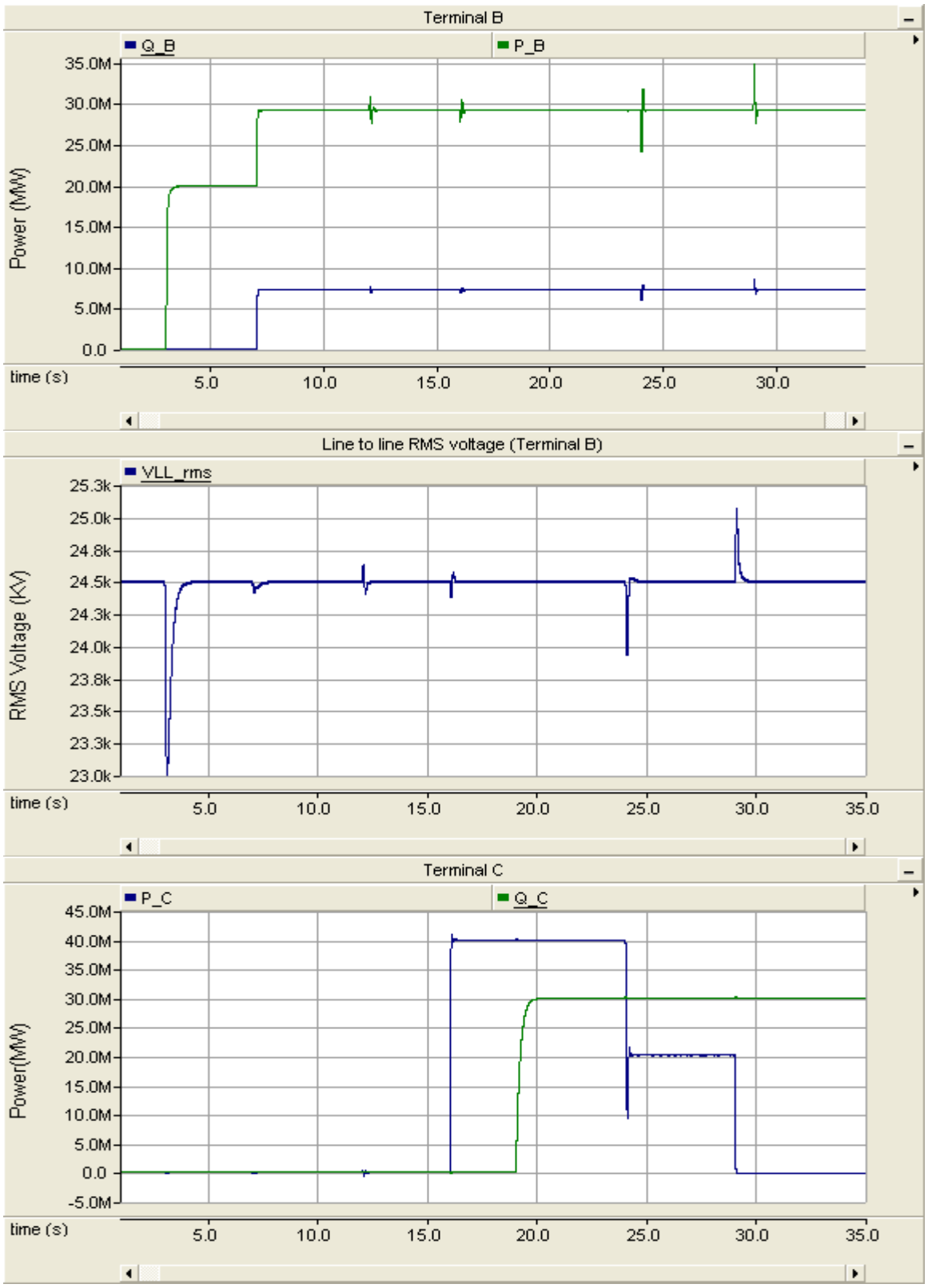
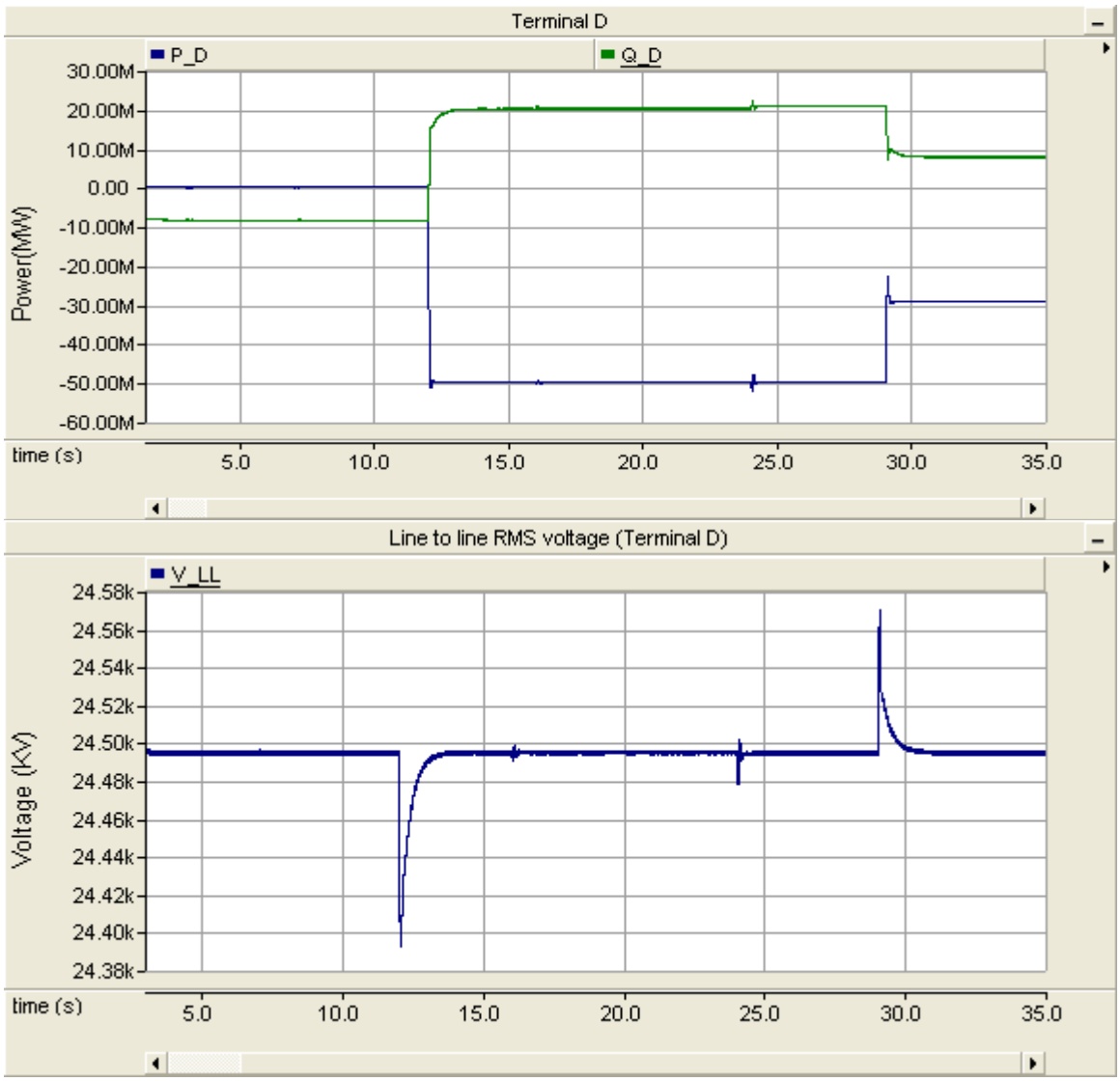
Appendix

A. Complete simulation results of MTDC with voltage margin control

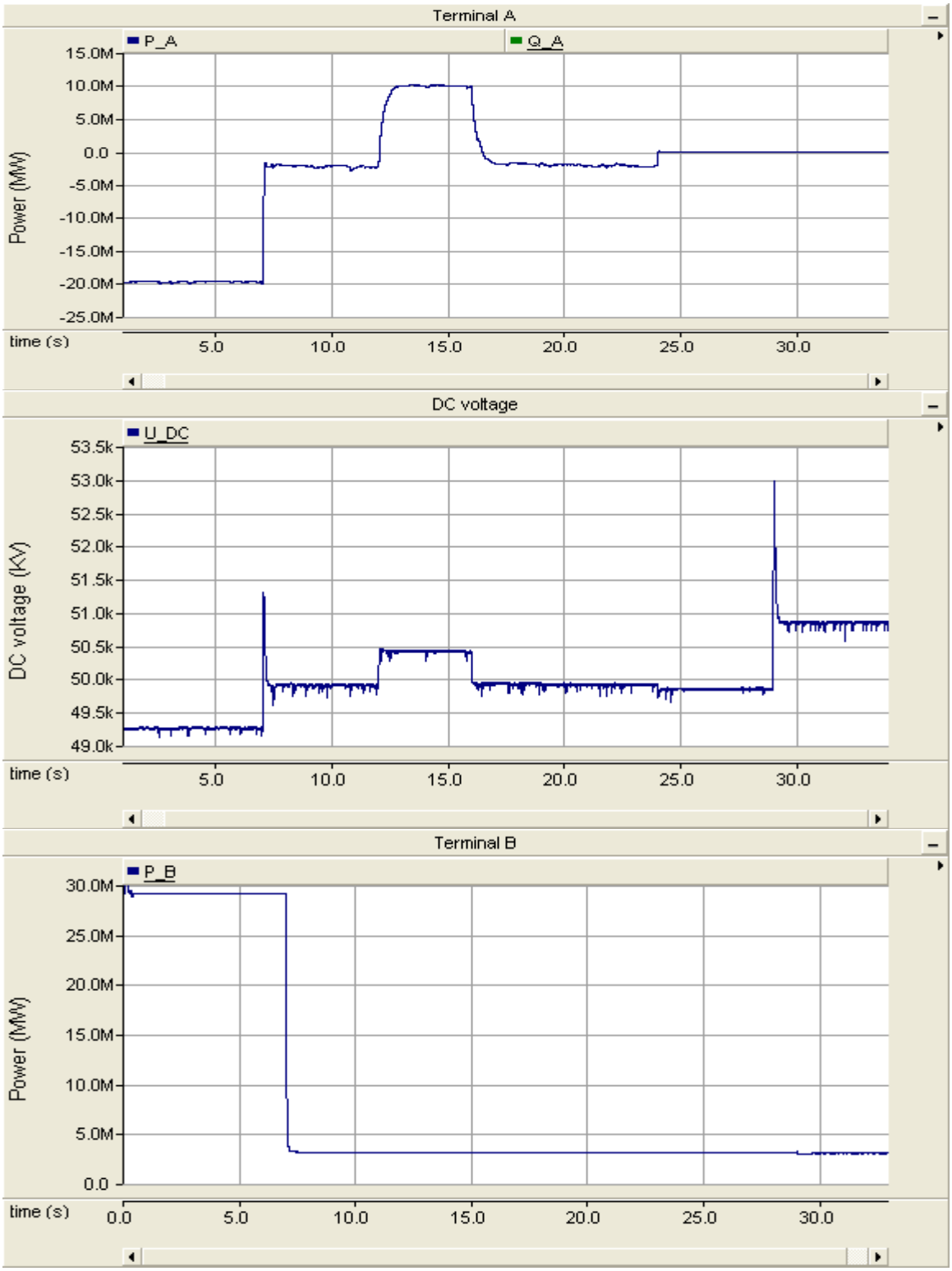
MTDC with voltage margin and droop

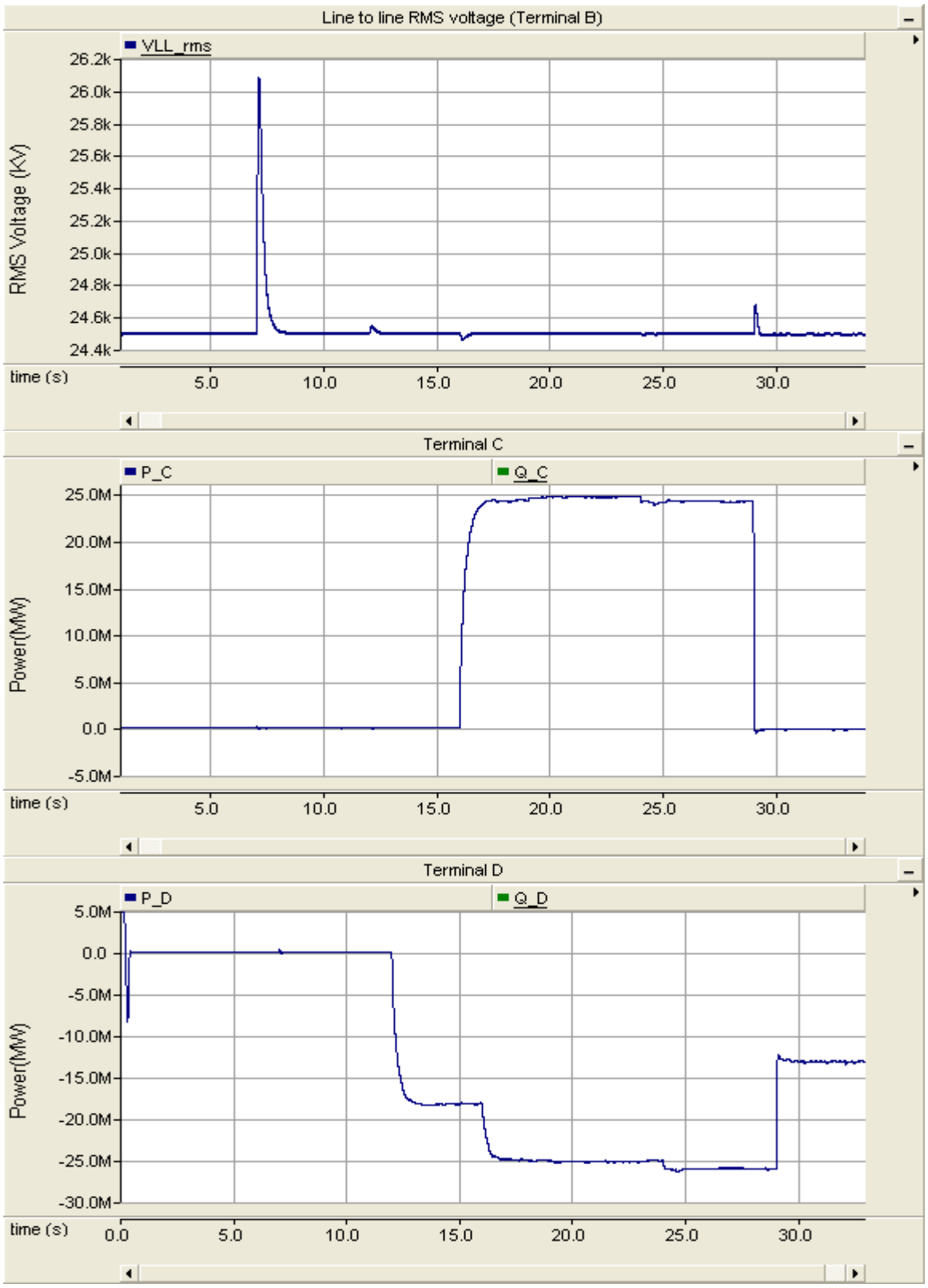


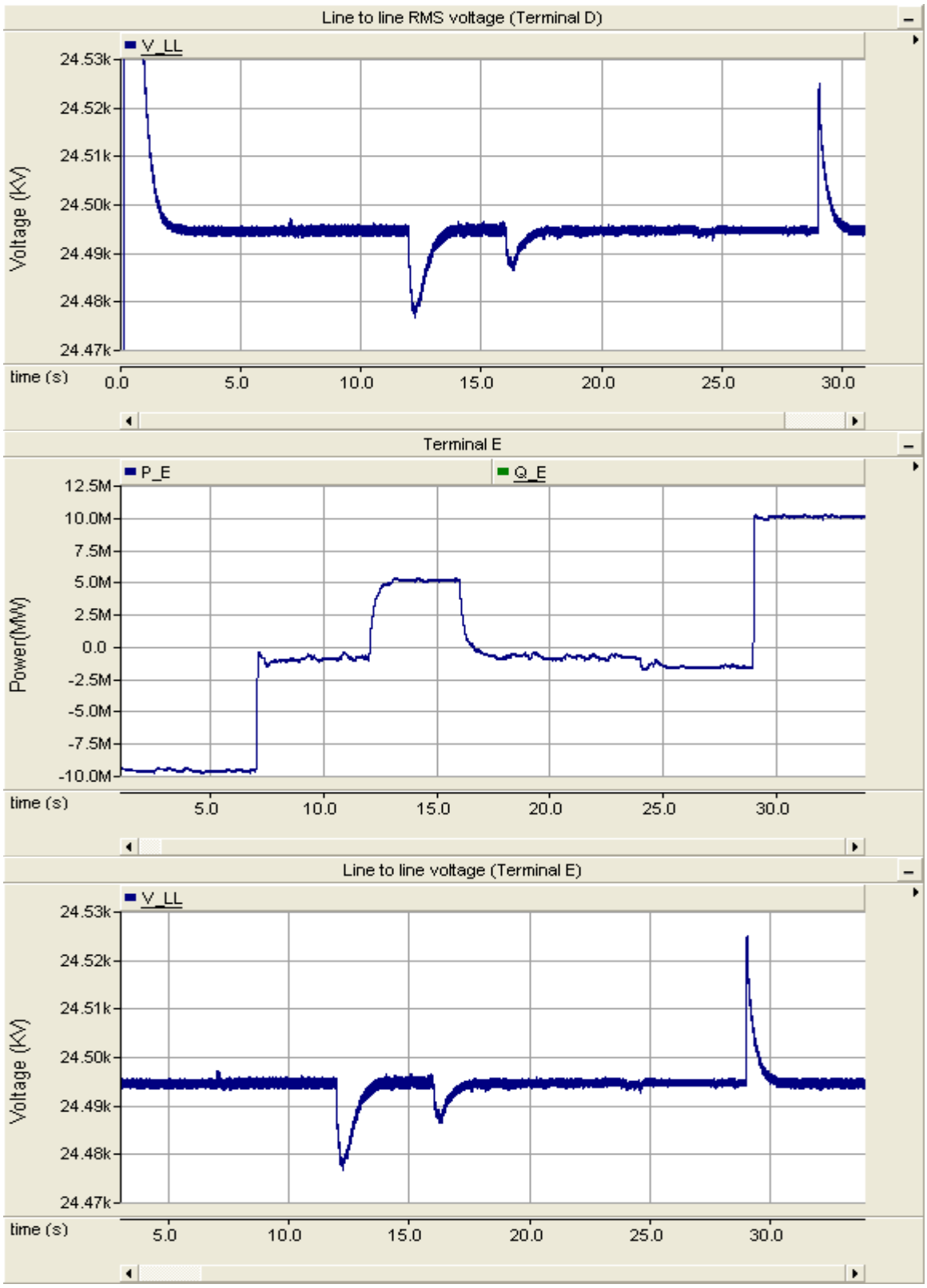

Terminal B
Q_B
P_B
35.0M
30.0M
25.0M
20.0M
15.0M
10.0M
5.0M
0.0
Power (MW)
time (s)
5.0
10.0
15.0
20.0
25.0
30.0
Line to line RMS voltage (Terminal B)
VLL_rms
25.3k
25.0k
24.8k
24.5k
24.3k
24.0k
23.8k
23.5k
23.3k
23.0k
RMS Voltage (KV)
time (s)
5.0
10.0
15.0
20.0
25.0
30.0
35.0
Terminal C
P_C
Q_C
45.0M
40.0M
35.0M
30.0M
25.0M
20.0M
15.0M
10.0M
5.0M
0.0
-5.0M
Power(MW)
time (s)
5.0
10.0
15.0
20.0
25.0
30.0
35.0


Terminal D
P_D
Q_D
30.00M
20.00M
10.00M
0.00
-10.00M
-20.00M
-30.00M
-40.00M
-50.00M
-60.00M
Power(MW)
time (s)
5.0
10.0
15.0
20.0
25.0
30.0
35.0
Line to line RMS voltage (Terminal D)
V_LL
24.58k
24.56k
24.54k
24.52k
24.50k
24.48k
24.46k
24.44k
24.42k
24.40k
24.38k
Voltage (KV)
time (s)
5.0
10.0
15.0
20.0
25.0
30.0
35.0

B. Complete simulation results of MTDC with DC voltage droop control




Line to line RMS voltage (Terminal B)
VLL_rms
RMS Voltage (KV)
26.2k
26.0k
25.8k
25.6k
25.4k
25.2k
25.0k
24.8k
24.6k
24.4k
time (s)
5.0
10.0
15.0
20.0
25.0
30.0
Terminal C
P_C
Q_C
Power(MW)
25.0M
20.0M
15.0M
10.0M
5.0M
0.0
-5.0M
time (s)
5.0
10.0
15.0
20.0
25.0
30.0
Terminal D
P_D
Q_D
Power(MW)
5.0M
0.0
-5.0M
-10.0M
-15.0M
-20.0M
-25.0M
-30.0M
time (s)
0.0
5.0
10.0
15.0
20.0
25.0
30.0


Line to line RMS voltage (Terminal D)
V_LL
24.53k
24.52k
24.51k
24.50k
24.49k
24.48k
24.47k
Voltage (KV)
time (s)
0.0
5.0
10.0
15.0
20.0
25.0
30.0
Terminal E
P_E
Q_E
12.5M
10.0M
7.5M
5.0M
2.5M
0.0
-2.5M
-5.0M
-7.5M
-10.0M
Power(MW)
time (s)
5.0
10.0
15.0
20.0
25.0
30.0
Line to line voltage (Terminal E)
V_LL
24.53k
24.52k
24.51k
24.50k
24.49k
24.48k
24.47k
Voltage (KV)
time (s)
5.0
10.0
15.0
20.0
25.0
30.0

Paper presented at NORPIE-2008 conference at TKK, Helsinki, Finland, June 2008

Multi-Terminal VSC-HVDC System for Integration of Offshore Wind Farms and Green Electrification of Platforms in the North Sea

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***Abstract*—This paper discusses a multi-terminal VSC-HVDC system proposed for integration of deep sea wind farms and offshore oil and gas platforms in to the Norwegian national grid onshore. An equivalent circuit of the VSC in synchronous d-q reference frame has been established and decoupled control of active and reactive power was developed. A three terminal VSC-HVDC was modeled and simulated in EMTDC/PSCAD software. Voltage margin method has been used for reliable operation of the HVDC system without the need of communication. Simulation results show that the proposed multi-terminal VSC-HVDC was able to maintain constant DC voltage operation during load switchings, step changes in power demand and was able to secure power to passive loads during loss of a DC voltage regulating VSC-HVDC terminal with out the use of communication between terminals.**

***Index Terms*—Multi-terminal HVDC, EMTDC/PSCAD, Voltage Source Converters, vector control**

I. Introduction

INTENSIVE research efforts are underway in Norway towards developing large scale deep sea wind farms with expected distances of 100-300 Km from shore [1]. For reasons of large capacitive currents HVAC will not be a technically and economically feasible solution for such submarine distances [7],[9]. This makes HVDC the more feasible solution in this particular case.

On the other hand, the Norwegian oil and gas platforms, which currently use gas turbines except in one case (Troll A [2]), contribute towards a large share of the total CO_2 emission in Norway [10]. For economic and environmental protection reasons there has been a tendency towards replacing the gas turbines with electric supply from onshore grid [8].

An interconnection between the offshore wind farms, the oil and gas platforms and onshore grid can result in reduced operational costs, increased reliability and reduced CO_2 emissions. A multi-terminal HVDC (MTDC) network will then be the core of such an interconnection system. MTDC can also open new power market opportunities and result in better utilization of transmission lines [11].

Classical HVDC based upon line commutated converters has a main challenge in that it needs reversal of voltage polarity during reversal of power flow. This means that classical HVDC is unable to operate at fixed DC voltage level for both rectifier mode and inverter mode of operation. Since maintaining a constant dc voltage during all conditions is one expected and important feature of the MTDC, the thyristor based classical HVDC may not be a good candidate in developing MTDC.

Voltage source converters (VSC) on the other hand do not need reversal of polarity for changing the direction of power flow and also are capable of independent control of active and reactive power. This makes VSC and ideal component in making MTDC.

This paper presents a proposed three terminal VSC-HVDC model linking an onshore grid, offshore wind farm and offshore oil and gas platform and discusses the control strategy for the terminals.

II. Equivalent Circuit of Vsc in Synchronous d-q Reference Frame

A. Voltage Source Converter

A schematic view of voltage source converter is shown in Figure 1. The series inductance on the ac side, also called ac reactor, smoothens the sinusoidal current on the ac network and is also useful for providing the reference point for ac voltage, current and active and reactive power measurements. The shunt connected capacitors on the DC network side are used for DC voltage source and harmonic attenuation.

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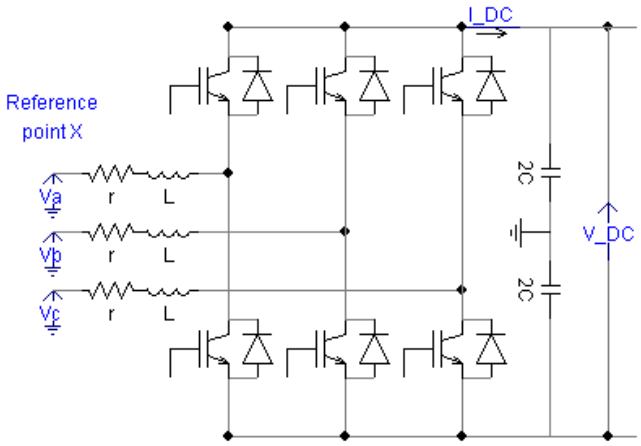

Figure 1. Schematic of VSC

Usually, a VSC station works in either of the four control modes listed below [3].

a. Constant active power control
b. Constant DC voltage control
c. Constant DC current control
d. Constant AC voltage control

In this paper active power control, DC voltage control and AC voltage control will be used at different terminals to establish an MTDC network.

B. Single line diagram representation

A single line diagram of a VSC is shown below in Figure 2.

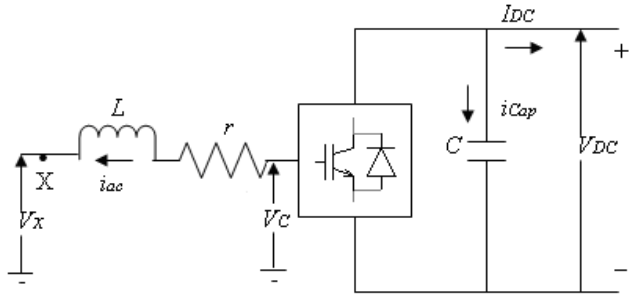

Figure 2. Single line diagram representation of VSC

The reference point for measuring active power, reactive power, and voltage is point X in Figure 2.

Voltage across the ac reactor in *abc* reference frame is given by:

$$V_{Cabc} - V_{xabc} = L\frac{di_{abc}}{dt} + ri_{abc} \tag{2}$$

C. Synchronous d-q reference frame

In order to decouple the active and reactive power controls, the synchronously rotating d-q reference frame will be used for developing the controllers. All the phase quantities will first be transformed in to the α-β reference using the Clark transformation (equation 3) [4][12].

$$\begin{pmatrix} \alpha \\ \beta \\ o \end{pmatrix} = \frac{2}{3}\begin{pmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{pmatrix}\begin{pmatrix} a \\ b \\ c \end{pmatrix} \tag{3}$$

Transforming equation (2) in to α-β representation:

$$V_{C\alpha\beta} - V_{x\alpha\beta} = L\frac{di_{\alpha\beta}}{dt} + ri_{\alpha\beta} \tag{4}$$

The relation between α-β and d-q reference frames is given by Park's transformation (equation 5)[12].

$$x_{dq} = x_{\alpha\beta}e^{-j\omega t} \quad x_{dq} = x_{\alpha\beta}e^{-j\omega t} \tag{5}$$

Where ω is the angular speed of the rotating d-q reference frame and is equal to the radial frequency of the fundamental ac voltage component.

From equations (2) and (5):

$$\begin{aligned} V_{c\alpha\beta} &= V_{cdq}e^{j\omega t} \\ V_{x\alpha\beta} &= V_{xdq}e^{j\omega t} \\ i_{\alpha\beta} &= i_{dq}e^{j\omega t} \end{aligned} \tag{6}$$

From (4) and (6),

$$\begin{aligned} V_{cdq}e^{j\omega t} - V_{xdq}e^{j\omega t} &= L\frac{d\left(i_{dq}e^{j\omega t}\right)}{dt} + ri_{dq}e^{j\omega t} \\ &= e^{j\omega t}L\frac{di_{dq}}{dt} + Li_{dq}\frac{d(e^{j\omega t})}{dt} + ri_{dq}e^{j\omega t} \\ &= e^{j\omega t}L\frac{di_{dq}}{dt} + j\omega Li_{dq}e^{j\omega t} + ri_{dq}e^{j\omega t} \end{aligned} \tag{7}$$

Eliminating $e^{j\omega t}$ from all terms:

$$V_{cdq} - V_{xdq} = L\frac{di_{dq}}{dt} + j\omega Li_{dq} + ri_{dq} \tag{8}$$

Equation 8 defines the mathematical model of the VSC in synchronous d-q reference frame.

The controllers will be developed with reference to d-q quantities and finally the output will be transformed back to the abc stationary frame before it is sent to Pulse Width Modulator (PWM) of the converter.

D. Phase Lock Loop

The Phase Locked Loop (PLL) synchronizes a local oscillator with a reference sinusoidal input. This ensures that the local oscillator is at the same frequency and in phase with the reference input [6]. The local oscillator is voltage controlled oscillator (VCO). The block diagram of a PLL is shown in Figure 3.

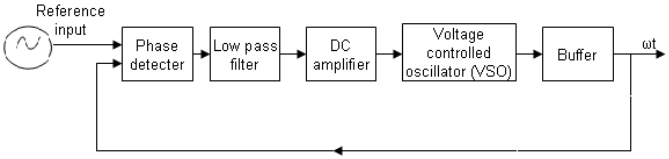

Figure 3. Block diagram of phase lock loop (PLL)

In the VSC the PLL is phase locked with voltage phasor of the phase-a of the reference point. The output of the PLL is used to synchronize and phase lock the the d-q reference plane with the AC source voltage.

E. Equivalent Circuit in d-q reference frame

The Phase Lock Loop (PLL) that provides with the angle for ab→dq/dq→abc transformation blocks is phase locked with phase a voltage of point X. Moreover, the synchronous d-q reference frame is chosen in order to align the d axis with that of the voltage phasor of phase-a at reference point X in stationary abc reference frame. This results in $V_{Xq}=0$ and $V_{Xd}=V_X$. Then, from equation (8) we get the following simplified relation.

$$\begin{pmatrix} sL+r & 0 \\ 0 & sL+r \end{pmatrix}\begin{pmatrix} i_d \\ i_q \end{pmatrix}=\begin{pmatrix} V_{Cd} \\ V_{Cq} \end{pmatrix}-\begin{pmatrix} V_{Xd} \\ 0 \end{pmatrix}+\begin{pmatrix} 0 & \omega L \\ -\omega L & 0 \end{pmatrix}\begin{pmatrix} i_d \\ i_q \end{pmatrix} \quad (9)$$

From equation (9) the equivalent circuit of the VSC in the synchronized d-q reference frame will be as shown in Figure 4 below.

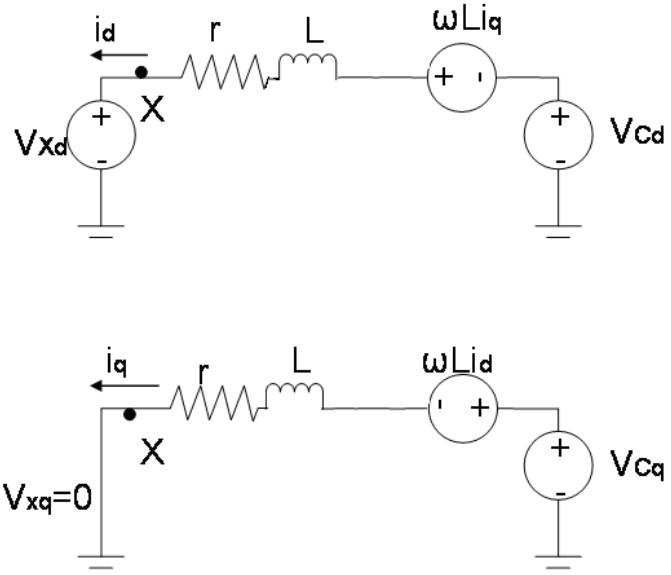

Figure 4. Equivalent circuit diagram of VSC in synchronous d-q reference frame

III. VSC-HVDC CONTROLLERS

A. Inner Current Controllers

The inner current controller can be developed based upon the equivalent circuit in Figure 3 and equation (9) that describes the circuit. Figure 5 shows the d-axis and q-axis current controllers of the inner current loop.

The converter has a delay of $e^{-T_w s} \approx 1/(1+T_w s)$ due to the sinusoidal pulse width modulator and $T_w = 1/2f_s$ where f_s is the switching frequency of the converter. Proportional integral (PI) controllers are used for closed loop control and the zeroes of the PI controllers are selected to cancel the dominant pole in the external circuit. For a typical VSC, the time constant $\tau=L/r$ is much higher than T_w and hence will be the dominant pole to be canceled.

The cross coupling currents in equation (9) are compensated by feed forward terms in the controllers as in Figure 5.

i_d^* and i_q^* are reference currents for the d-axis and q-axis current controllers respectively.

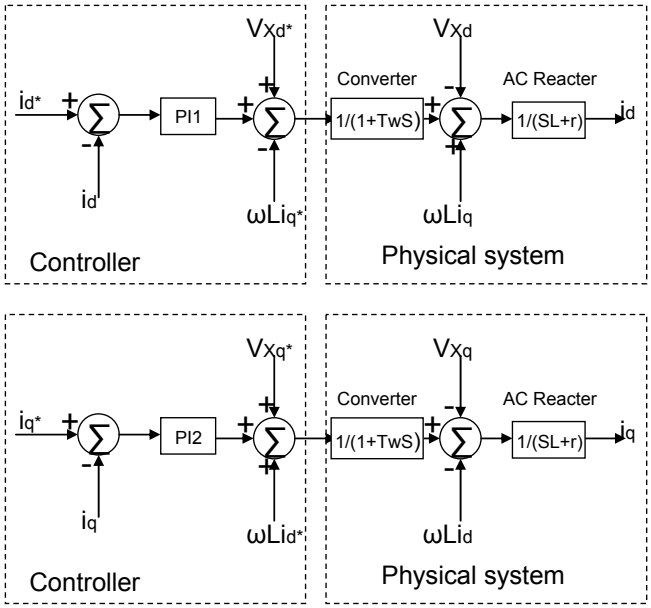

Figure 5: Inner current controllers

B. Outer Controllers

From the d-q equivalent circuit and observing from reference point X, the apparent power injected by the VSC in to the AC network is given by:

$$S = \frac{1}{2}\left(V_{Xd} + j0\right)\left(i_d - ji_q\right) \tag{10}$$

And hence active and reactive powers are given by:

$$P = \frac{3}{2}V_{Xd}i_d \tag{11}$$

$$Q = \frac{-3}{2}V_{Xd}i_q \tag{12}$$

And a small change in the DC voltage can be approximated as:

$$\Delta V_{DC} = \frac{\Delta q_{cap}}{C} = \frac{1}{C}\int i_{cap}dt \tag{13}$$

Where C is the shunt capacitance of the VSC-HVDC, q_{cap} is the charge of the capacitor and i_{cap} is the current going in to the DC capacitor bank as shown in Figure 2. The direction of the currents in the power calculations strictly refer to Figure 2.

From conservation of energy law,

$$\frac{3}{2}V_{Xd}i_d + V_{DC}i_{cap} + V_{DC}I_{DC} = 0 \tag{14}$$

From equations (13) and (14),

$$\frac{d\Delta V_{DC}}{dt} = \frac{-3V_{Xd}}{2CV_{DC}}\left(i_d + \frac{2V_{DC}I_{DC}}{3V_{Xd}}\right) \tag{15}$$

For the sake of simplicity, it is assumed that the VSC-HVDC is connected to a stiff AC network implying that V_{Xd} is
also a constant quantity. With such consideration, it can be seen from equations (11), (12) and (15) that active power and DC voltage are correlated with i_d and reactive power with i_q. Hence controller structures will look like as shown in Figure 6.

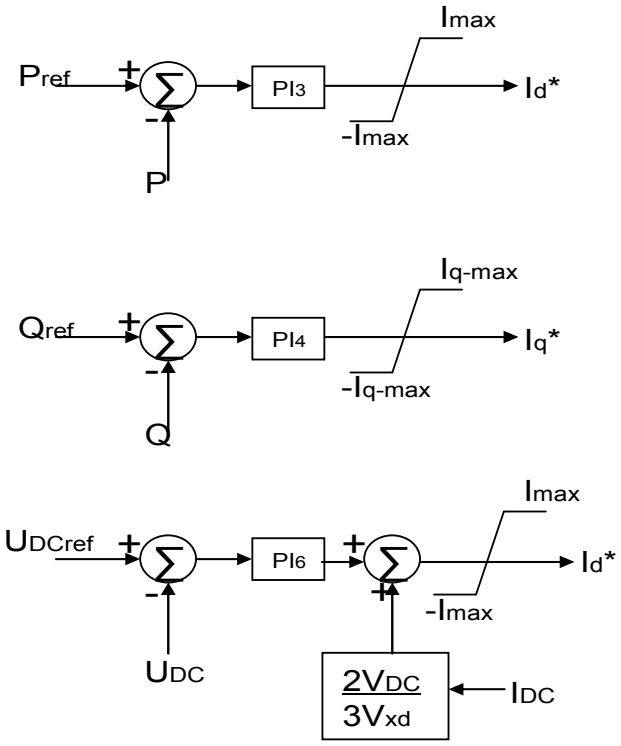

Figure 6. Outer controllers

The DC current is feed forward compensated in the DC voltage controller (Figure 6).

In VSC-HVDC, the maximum current limit of the VSC must not be exceeded at any moment of the operation. On the other hand, priority is given to transfer active power than reactive power. Hence i_d is limited to the maximum current capacity +/-I_{max} and i_q is limited in such a way that the total current will not exceed the rating of the valves. Mathematically:

$$I_{\max} = I_{rated} \tag{16}$$

$$I_{q\max} = \sqrt{\left(I_{rated}^2 - I_d^2\right)} \tag{17}$$

C. VSC-HVDC for Passive Loads

A VSC-HVDC supplying a passive network has the objective of maintaining constant AC voltage for all

operating conditions. Active and passive power consumptions depend on the passive network elements and hence are not directly controlled. The fundamental frequency AC voltage output of the converter is given by [13]:

$$V_C = \frac{1}{2} m V_{DC} \sin(\omega t) \tag{18}$$

where m is modulation index of the PWM.

Voltage at the reference point X will be:

$$V_X = \frac{Z_{LD} V_C}{\left(Z_{LD} + j\omega L + r\right)} \tag{19}$$

Where Z_{LD} is the Thevenin equivalent impedance of the ac network at the point of common coupling and is a variable quantity.

From equations (16) and (17), it is seen that the ac voltage can be controlled by controlling the modulation index m as shown in the figure below.

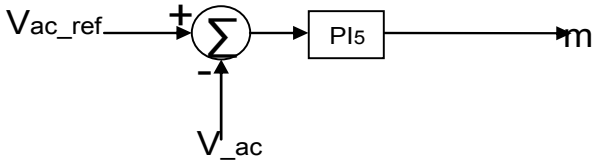

Figure 7. AC voltage regulation by control of modulation index

The complete assembly of the outer and inner controllers is shown in Figure 8 below.

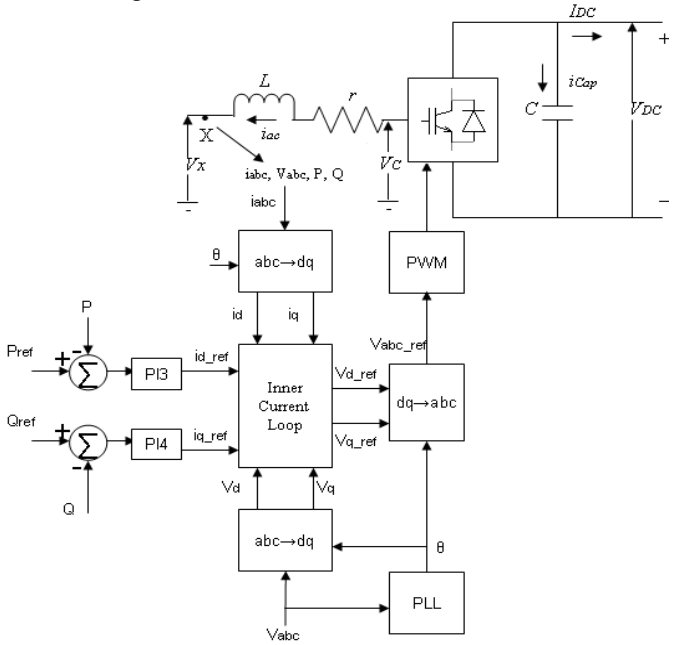

Figure 8. Block diagram of the inner and outer controllers

IV. Proposed Multi-terminal HVDC Model

A multi-terminal VSC-HVDC (MTDC) consists of three or more VSC terminals with different control objectives. A three terminal VSC-HVDC connecting an offshore wind park, a platform and an onshore grid is proposed and analyzed in this paper. The schematic diagram of the proposed MTDC is shown in Figure 9.

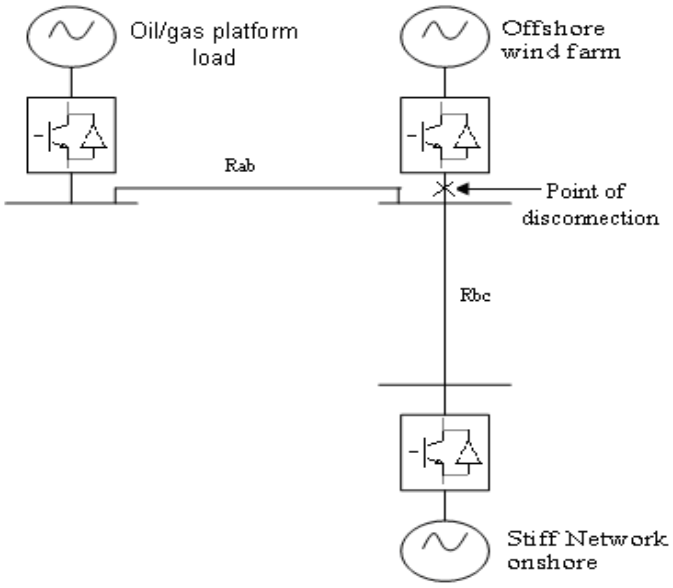

Figure 9. Proposed interconnection of platform, offshore wind farm and onshore grid

It is assumed that the offshore wind farm will supply power both to the platform and to onshore grid. During loss of the wind park terminal, the onshore grid should be able to secure power supply to the platform without a communication system between terminals. The platform is assumed to consist of passive loads. A control scheme called voltage margin method can result in the desired performance characteristics of the MTDC system [5].

According to the voltage margin method, each converter will regulate the DC voltage as long as the power flow through it is within the upper and lower limits and the reference DC voltages of the terminals are offset from one another by a certain voltage margin. This is shown in Figure 10 and Figure 11.

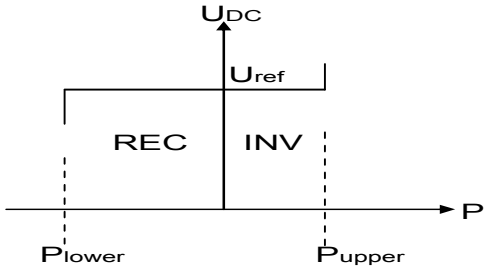

Figure 10. P, U_{DC} characteristic of a converter connected to an active system

When the upper or lower limit is passed, the terminal starts to act as a constant power terminal. The operating DC voltage will be at the point where the following relation is satisfied.

$$P_A + P_B + P_C + \cdots = 0 \qquad (20)$$

Where A, B and C refer to onshore grid, offshore wind farm and oil/gas platform respectively.

This point lies in a horizontal line section of the P-U curve of one of the VSC terminals as can be seen in Figure 11. This voltage determining terminal will act as a dc slack bus and will compensate for variations in power flow.

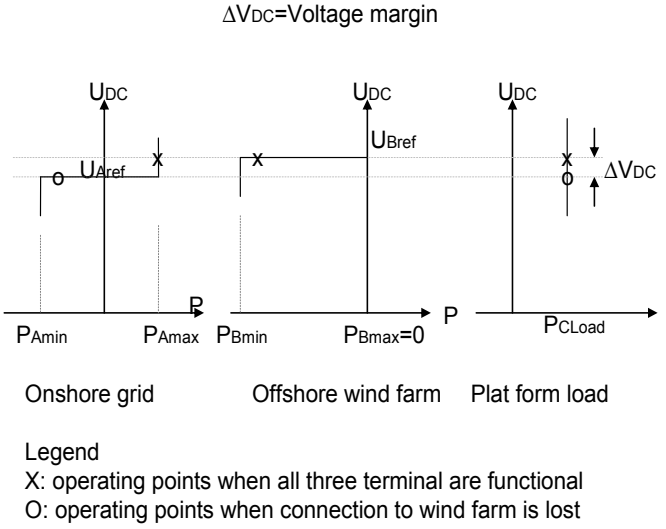

Figure 11. U-P characteristics and operating points of terminals

Negative power in the U_{DC}-P curve of Figure 10 indicates rectifier mode and positive power indicates inverter mode. The wind farm is expected to supply power up to its rated capacity and P_{Bmax} is set to zero assuming that there is no other load connection at the wind farm. Onshore grid on the other hand has an upper limit (P_{Amax}) equal to the scheduled power flow (P_{ref}) from offshore park to onshore. It should be noted that P_{ref} can be varied by an operator at onshore grid connection. The lower limit (P_{Amin}) should at least be equal to the maximum power demand of load at the platform (P_{Cmax}). This ensures that there will be uninterrupted power supply to the platform even during loss of the wind farm. Figure 11 shows that the P-U characteristic curve of the VSC that supplies power to passive network is vertical line. This is because the load depends only on the AC voltage whereas the AC voltage is kept constant independently of the DC voltage. An important feature of using voltage margin method with MTDC is that during loss of one VSC-HVDC terminal, the MTDC will maintain normal operation as long as the power transmission limits are not exceeded at each station [5]. If the terminal lost is a DC voltage regulating bus, the MTDC will automatically find another equilibrium point and the duty of maintaining the DC voltage will be instantaneously transferred to a different terminal.

In order to get the U_{DC}-P curves shown in Figure 11, the controllers at terminals A and B will be modified as in Figure 12 [5].

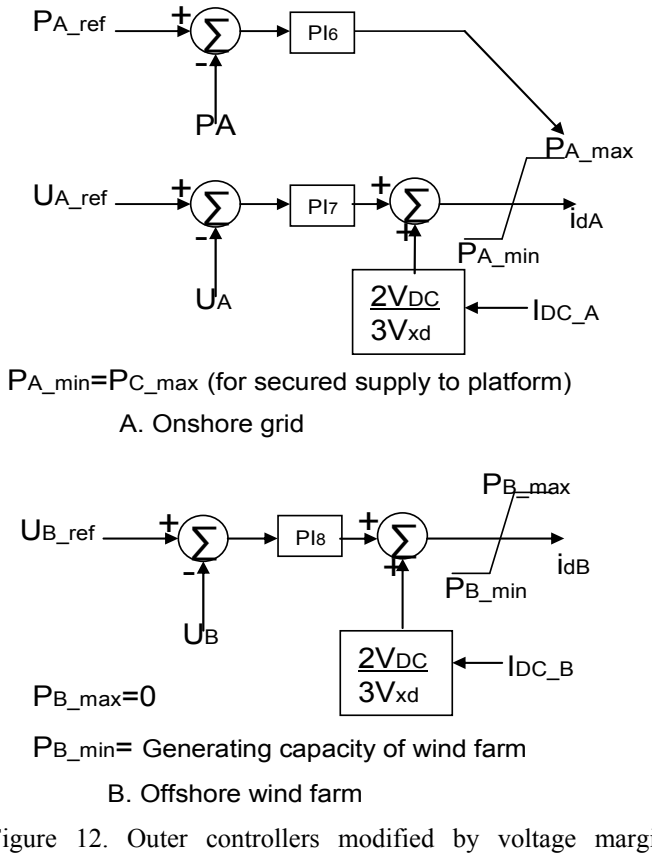

Figure 12. Outer controllers modified by voltage margin method

The DC voltage margin is given by:

$$U_{B\_ref} - U_{A\_ref} = U_{margin} = \Delta V_{DC} \qquad (21)$$

The DC voltage margin should be sufficient enough to avoid interaction of the DC voltage controllers of terminal A and B during DC voltage disturbances while all the terminals are in operation.

V. Simulation Studies

To validate the idea of multi-terminal system proposed for integration of offshore wind farms and platforms into main grid, a three terminal VSC-HVDC system has been modeled and analyzed using PSCAD/EMTDC simulation software. For all converters r=0.4 Ohm, L=0.0048H and C=400uF. The switching frequency in all the three cases was set to 5 kHz. DC cables were represented by series resistances of $R_{ab}=R_{bc}=0.01Ohm$.

The following reference values were used for the terminal controllers.

Table 1. Reference value settings for controllers

Terminal	Pmax	Pmin	Uref
A. Onshore grid	40MW	-60MW	48KV
B. Offshow wind farm	0	-60MW	52KV
C. Platform load	20MW	0	24.5KVrms line to line

For both onshore grid and offshore wind farm, the parameters for the current PI controllers are: PI_1 and PI_2, $K_1=K_2= 0.0824$ $T_1=T_2=0.0068$. The DC voltage controllers in both cases are set to $K_6=-2$, $T_3=-0.01$ and the reactive power controllers are set $K_4=0$ $T_4=-2$. Active power controller at onshore grid connection has $K_4=0.1$ $T_4=0.5$. The ac voltage controller at the platform has $K_5=3$ $T_5=0.05$.

The following table summarizes the events that were run on the simulation for analysis.

Table 2. Description of simulated events

Time (sec)	Event
0	System start up
3	12MW Load connection at platform
8	Onshore grid set to draw 40MW power
12	6.5MW more load connected at platform
17	Connection to Offshore wind farm lost (at point X in Fig 8)

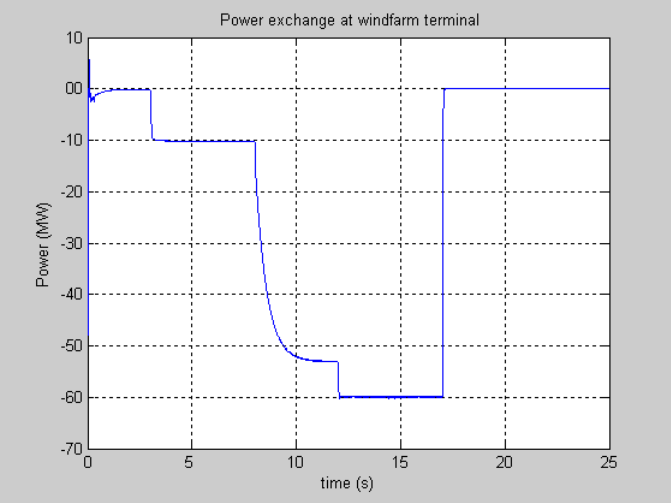

Figure 13. Power generation at the wind farm

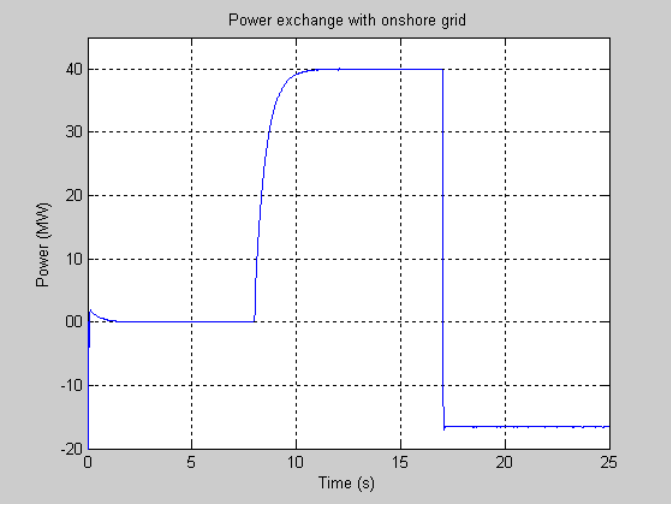

Figure 14. Power exchange with the on shore grid

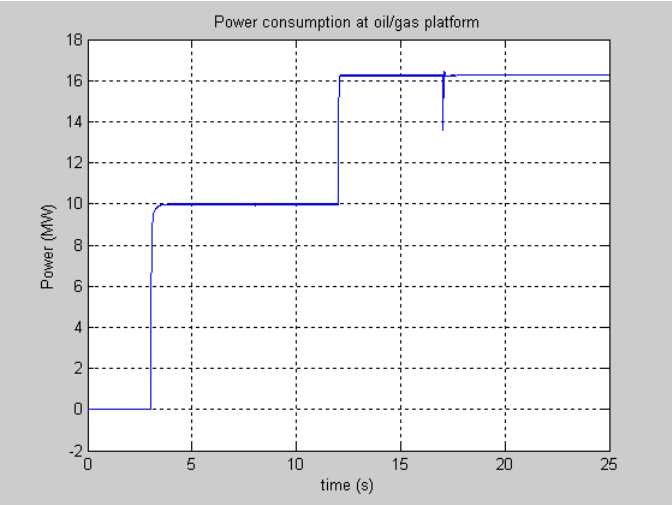

Figure 15. Power consumption at the platform

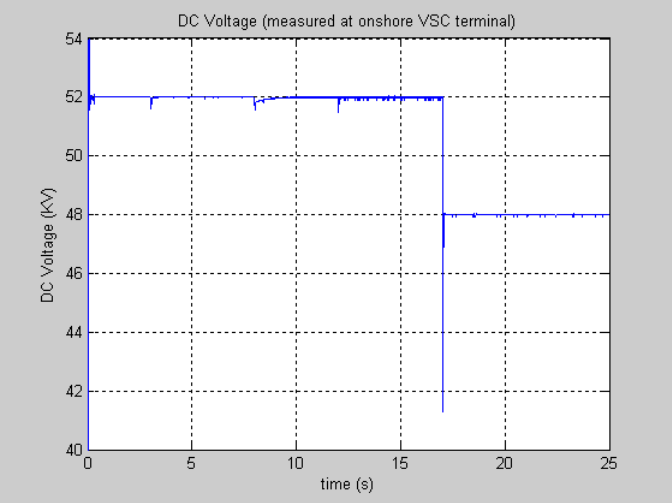

Figure 16. DC Voltage of the MTDC system

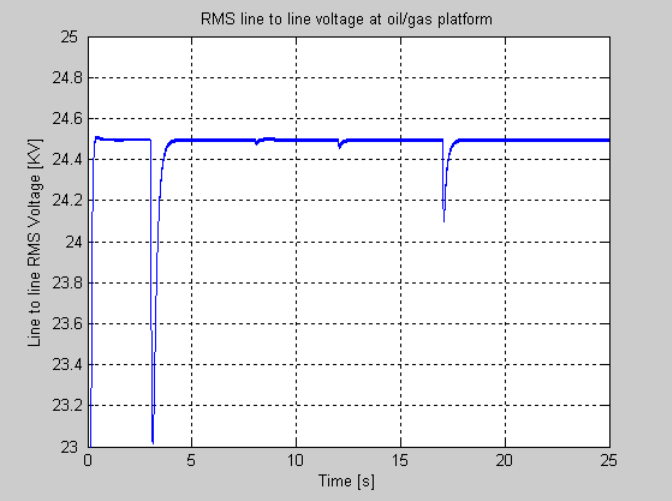

Figure 17. Line to line rms voltage at oil/gas platform load

Figure 13- Figure 17 show that the MTDC has only small steady state error and is stable under severe disturbances. The plots show that change in power reference at onshore grid (at *t=8sec*) and load switchings at platform (at *t*=3sec and *t*=12sec) have caused only minor oscillations on the DC voltage and these oscillations are effectively attenuated quickly. It is also seen that when connection to the wind farm terminal was lost, the onshore grid instantly started to supply the load demand at the platform and also maintained a new constant DC voltage level in the MTDC system. As Figure 14 shows, the power supply to the passive loads at the platform was not affected by the loss of connection to the wind farm.

CONCLUSION

In this paper a three terminal MTDC connecting offshore wind farm, oil & gas platform load and onshore grid was proposed. Equivalent circuit of VSC in d-q reference frame was established and used for developing control strategy for the multi-terminal VSC. This together with voltage margin method was used to control the MTDC system for a stable steady state and dynamic performance. Simulation results have confirmed that the proposed control results in a stable steady state and dynamic state operation and is also capable of restoring operation during loss of DC voltage regulating terminal without the need of communication between terminals.

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