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SENSORLESS DIGITAL CONTROL OF GRID CONNECTED THREE PHASE CONVERTERS FOR RENEWABLE SOURCES

Thesis for the degree of philosophiae doctor

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Abstract

Power electronic converters have become popular in the field of power transformation for renewable energy. Power electronics converters achieve high efficiency, and the price of their components is falling, thus making them even more beneficial for renewable energy applications. Those systems coupled to the grid need to withstand certain utility-defined circumstances which may occur during operation. Additionally the new net regulations for large generation plants specify that during specified severe grid disturbances the relatively delicate converters should stay connected supporting the system. For PV inverters the forthcoming standards may optionally add the possibility of reactive power compensation where for wind-power those standards are already in use.

This thesis focuses on reliable, sensor-less control of the PWM converters coping with varying grid conditions and existing problems. The thesis presents a variety of digital control solutions for interfacing PWM converter with the grid, synchronization, sensor-less operation and grid impedance detection.

The introductory chapter gives the fundamental theory about three-phase converters and control.
The following chapters deal with unbalanced condition and symmetric component decomposition, which is the tool to cope with unbalanced grid voltages or currents.

A sensor-less operation method using dual frame virtual flux model is presented with good results. In addition sensor-less synchronization to the grid is shown. Moreover an algorithm based on virtual flux for grid inductance estimation is also successfully demonstrated. Knowing the grid inductance is important during weak grid operation, since it is needed in order to provide unity power factor to the point of common connection.

At the end of the thesis, a control algorithm for voltage harmonic compensation during stand alone operation is presented. The presented algorithm gives the possibility to supply high quality power in isolated islands, where the load is unknown. Furthermore, this algorithm can be successfully used for UPS applications. The last chapter applies the voltage harmonic control to the Z-source converter having the possibility of achieving higher ac voltage than in conventional VSI, results are promising.

Acknowledgement

At first I would like to thank Professor Tore Undeland for giving me the opportunity to start the PhD studies and being my supervisor for four years. His inspiration has been invaluable to me. The four years which I spend on this PhD was very interesting and educational. When I start PhD I knew the power converters and control only from theory. The possibilities of testing in laboratory DSP programs on grid connected systems also give me a good practical understanding of converter operation.

During my PhD studies I've had the pleasure to stay abroad two times. I would like to thank my friends at University of Seville, Spain. Special thanks to Jose Ignacio Leon Galvan and Sergio Vazques for being good friends, helping out in the new laboratory and numerous technical discussions. I learned a lot of things during 6 months.

Also I would like to thank Junji Kondoh at AIST, Tsukuba, Japan for providing great laboratory help, and being good partner in discussions. Thanks also go to Jan Wiik who worked with me in the laboratory, this give me the correct picture of right order during critical experiments when many persons are involved.

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1. INTRODUCTION

1.1. Preface

This thesis is a part of the ”Technologies for Reliable Distributed Generation of Electric Power from Renewable Energy Sources” project. The research project involves two departments at the Norwegian University of Science and Technology and one industrial partner. The research groups at NTNU are from the Marine Machinery Group in the Department of Marine Engineering and the Energy Conversion Group (ENO) at the Department of Electric Power Engineering.
The funding partners are the Research Council of Norway and industry partner-Powec AS/Power-One.

The project objectives are as follows:

Develop energy efficient solutions and optimal design/manufacturing that enable different distributed renewable energy sources to work as stand alone electric power supplies or to be optimally integrated within the electric power infrastructure.

Transfer this knowledge to industry or eventually establish new industry.

Improve scientific knowledge and develop a scientific competent staff in the field of renewable energy systems. When the project ends, a total of 4 PhD students will be ready to join the industry in the project field.

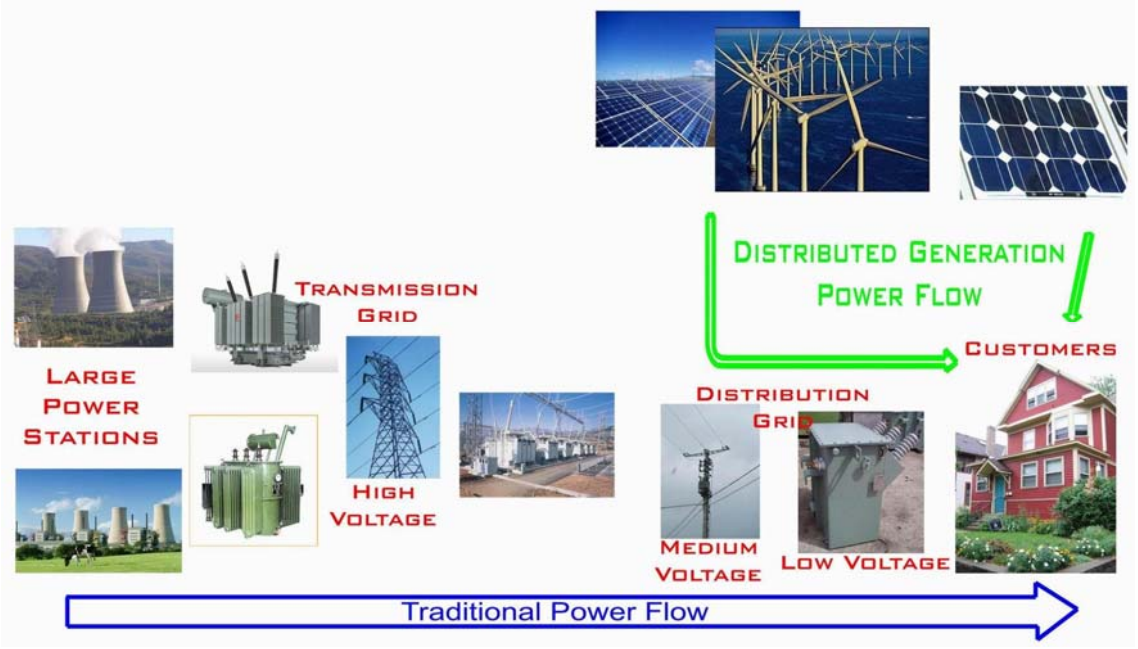

Figure 1.1: Overview of traditional power system and distributed generation

1.2. Background

In recent years power electronics has come with great help to efficiently harness the free energy of nature like wind-, solar- or wave-power. With increasing prices of fossil fuel, and excessive emission of gases causing global warming, researchers and politicians are facing the problem that the cheap energy sources are running out and new solutions are needed. Since the production of electric energy still consumes a large part of the total worldwide coal energy reserve, the traditional power system should be used to enable more green generation and meet environmental concerns. Conventional large power plants deliver electric power to the majority of the population, while emitting large amount of carbon-dioxides. In order to support and unload those plants, a strategy based on a large amount of generation sources, but relatively low power from renewable sources is gaining popularity – the distributed power generation (DG).
One of these solutions which can help to provide green electric power to distributed generation from renewably sources is to use power electronics as an efficient tool in the power conversion chain [bla1], [bla2]. The renewable sources tend to have electric power fluctuations dependent on the environment conditions. Many studies show that energy storage is needed in order to smooth out the power and stabilize the grid. Some examples of energy storage are water pumped solution, chemical battery, flywheel, hydrogen, or compressed air. Power electronic conversion is the key technology to increase efficiency for energy generation or storage. The advantage of distributed generation is that generation can occurs in proximity to the consumer, thus not suffering from transmission losses.

Due to political decisions we observe a large expansion of DG in many countries. For instance in 1991 in Germany, the government started its “1000 Roofs” program subsidizing solar energy. In 2001 the program was extended to “100 000 roofs”. The changes in the law enable quicker PV implementation, the grid companies are also obliged to buy “green” power from any customer and the selling price is higher than from regular power. The plan for Germany and Sweden is also to slowly back out from nuclear power production. In Norway there is a goal to achieve 3 *TWh/year* from wind power until 2010. In Sweden in 2003 the government introduced a new legislation which intends to encourage and increase the production from renewable sources. In Spain the newly build family apartments are obligated to have solar heating systems on roof for water heating. In this way a significant amount of electric energy can be saved.

In a distributed system the important part is the power conversion and control. Modern IGBT transistors easily enable to build power electronics converters which are used to convert DC currents into AC and vice versa in range of hundreds *kW* [ber1]. The availability and cheap price of digital signal processors (DSP) enable digital control technique, which give wide possibilities for control, protection, data logging, statistics, prediction, communication and all kind of embedded intelligence. In the past mostly analog control was used and more advanced function were not available. When using a PWM converter with DSP control it is possible to mimic the synchronous generator used in conventional power plants, and even embed more advanced functions, like active impedance variation and detection, different characteristics of droop control, active damping of low frequency sub-oscillations, etc. More details with droop control

for DG can be read in [bra]. The thesis also not deals with DG impact on power system stability or weak grids. These topics can be found in [mag3].

Most of this PhD thesis presents digital control algorithms, transformations, regulations techniques, communications, detection algorithms which finally end up inside signal processor as a DSP program. Any digital control algorithm consists of a small block of code, and the final overall performance will depend on quality of those small blocks.

1.3. Introduction to the three-phase converters

The three-phase voltage source converter (VSC) which is shown in Figure 1.2 is rather the name of topology and can be recognized dependent on the application under several different names like: grid connected converter, active rectifier, regenerative rectifier, PWM converter. Usually the hardware is the same, only different control schemes are used. Since the converter output voltage is a high frequency kind of square wave, some sort of filter that interconnects the converter to the grid is needed. The simplest filter consists only of an L choke, but due to its inefficiency LC or LCL filters are often employed. An LCL filter gives higher harmonic attenuation and cheaper cost [mal7]. The LCL filter is also vulnerable to resonance since it reassembles resonant circuit; active damping algorithms must be used [bla3], [lis3], [gul1].

The IGBT transistors are commonly used for powers from $5\,kW$ and higher. It is common to assume the life time of an IGBT stage for around 20 years. The most common modulation strategy is PWM with constant frequency switching. To increase the output voltage to maximum and fully utilize voltage in the dc-link, space vector modulation or sinusoidal modulation with third harmonic injection can be used. Currently the dc-link electrolytic capacitor is limiting the life time of the whole converter. Some companies even assume that the DC capacitor should be replaced at certain intervals (e.g. 8 years). For three-phase balanced systems this is not such a problem as for single-phase application where the power is pulsating. Many attempts have been done to replace or minimize this electrolytic capacitor by other topologies (e.g. matrix converter topology) or control scheme (e.g. direct power control).

The most common converter topology used for three-phase renewable sources is shown in Figure 1.2. It employs three transistor bridges connected to a common dc-link bus with a dc capacitor. Further the converter ac output is connected with the grid through a filter.

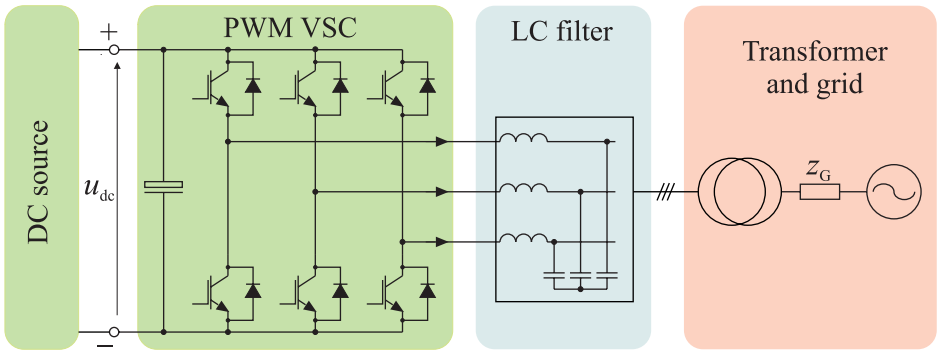

Figure 1.2: The PWM converter placed inside the conversion chain system

Introduction of PWM, IGBT-based converter brings several advantages such as maximum energy extraction from controlled plant, very high efficiency, controllable reactive power, fast response, etc. In the large variety of renewable systems on the market, the power conversion is mostly realized by a PWM converter with IGBT transistors, only for high power and high voltage levels tyristors are still used (e.g. HVDC).

1.4. Motivation for the study

All recent annual statistics shows a constantly increasing share of renewable sources in power generation. We have the luck of living in the century where a large amount of cheap energy is coming from oil, gas and coal, and consumption nowadays is at its peak. The exploration process become more difficult and thus the prices of fossil energy will increase. Like our fathers and grandfathers remember steam locomotives, in a matter of 40 years we will remember cars with internal combustion engine. The same transformation has to happen in electric energy generation, we have to harness more renewable energy from nature. However another scenario is also possible, the use of Nuclear Energy, which has large potential to reduce CO_2 emission but the acceptance from society is low.

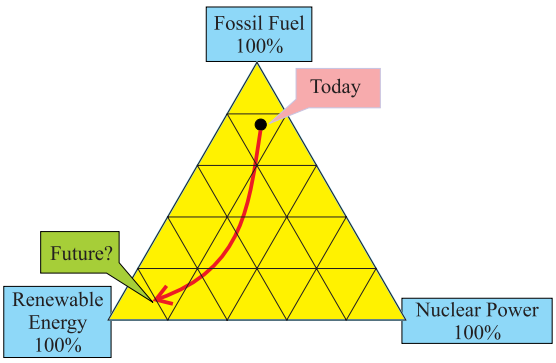

Figure 1.3: Nowadays and future energy production and share path.

Still a lot of research and work has to be done in order to be self-sufficient in energy. One obvious solution is to maximize use of renewable energy combined with energy

saving solutions. The quickest and easiest is to guide society how to not waste the electric energy. For sure in the future generation there will be much more wind-, solar or wave-energy but those are more expensive than conventional sources. Those green sources introduce challenges as power fluctuations, availability on demand and suffer in large investment cost. Figure 1.4 shows the trend in power systems, where renewable sources and storage system are integrated.

A good example of solution for storage is the state of the art water pumped system, which can operate with variable speed, resulting in high efficiency. In many flat or urban areas a use of hydro-based storage is impossible or expensive to build.

In those cases for power systems a relatively new type of battery can be used - the flow battery and the hot temperature battery [bar]. A good examples are two prototypes batteries which are built in Japan at Institute of Advanced Science and Technology (AIST), department of Research in Energy Technology, Tsukuba, Japan.
The first type battery consists of electrodes and exchangeable electrolyte, the power is limited by the area of electrodes (membranes) where the electrolyte during charging/discharging cycle is flowing. The energy is dependent on the volume of the electrolyte storage containers. The advantage of the system is when larger energy capacity is needed, it can be easily expanded by adding extra container with electrolyte. An operating example of Redox flow battery in Tsukuba can deliver 170 kW for 8 hours, there are 4 pairs of 28 m^3 electrolyte tanks, the cell unit weight 12 tons (8 m by 2.5 m by 2.1 m), the converter and transformer unit dimension are 5 m by 2.4 m by 3.1 m. This battery is suitable for quick charge/discharge cycle.

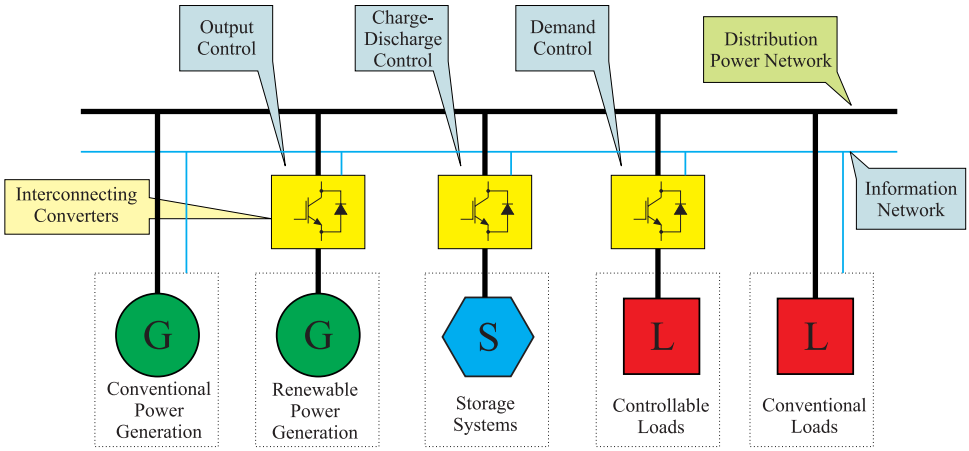

Figure 1.4: Overview of the conventional system combined with controllable renewable and storage sources.

Another relatively new type of battery is a high temperature NaS battery (based on molten Sodium-Sulfur). This battery achieves high efficiency and energy density when nominal internal temperature is maintained (160 °C). When no power is taken an external heat source is needed, but when charged or discharged, the internal losses maintain the internal temperature, so it's suitable for a constant slow charge and discharge cycle. A prototype battery built in Japan can deliver 2000 kW for 8 hours; the

battery unit with transformer and converters has dimensions of 10.2 *m* by 5.5 *m* by 5.2 *m*., the total weight 206 tons. The cost today is high but with automated high-volume production the NaS battery could compete with hydro-storage. The producer of NAS batteries *NGK Insulators* claim the price to drop to $140/*kWh*.

All those solutions mentioned above need power conversion by means of power electronics. The study will look to minimize the overall cost of converter hardware and develop new control methods. Unnecessary sensors can always be removed and estimation can be calculated in a DSP based on remaining sensors. An reduced number of sensors also add reliability; the program is much less prone to fail than real hardware sensor to break. Some of the areas of the thesis scope are: sensor-less operation, grid synchronization, operation with unbalanced conditions, grid impedance detection, stand alone operation, resonant controllers, active damping of LCL grid filter resonances.

As there is growing need for electricity in underdeveloped countries (e.g. parts of Africa) one of possible solutions is to operate a hybrid generation combined of wind, solar, storage and diesel generator. This solution will be still cheaper than building and maintaining a power system grid, especially since the power needs are much lower than in developed countries. The island mode of power generation, bring the power close to the consumer. A voltage control algorithms for stand alone generation will be presented in this thesis in Chapter 7 and Chapter 8.

1.5. State of the art study

Currently there are many ideas for distributed generation which need new control strategies, monitoring and planning. Up to now there is no established one standard for it, some researchers propose even DC current on the distribution level.

The general guide for design, operation and integration of distributed generation with electric power system can be found in [iee1] issued by IEEE.
A significant role in distributed generation is so-called droop control; the aim is to mimic the converter behavior as it would be a conventional synchronous generator. The inverter output voltage amplitude and frequency depends on the linear combination of active and reactive power. Significant work is done by K. De Brabandere, B. Bolsens, J. Van den Keybus and M. Chandorkar [bol1], [bra], [cha2], [kaw1] where the basics of parallel inverter operation take shape. Some work related to impact on power system and power quality is done by Fainan H. Magueed [mag3] and Hilmy Awad [awa].

In an aspect of regulation techniques and inverter advanced control a good reference is work done by D. Zmood and G. Holmes [zmo1]. Some innovative techniques are shown by M. Liserre in [lis5]. Passivity based and frequency domain methods are presented in [har1], [zmo3], and different current controllers strategies in [kaz2].

The research on Resonant Controller (RC) was mentioned first time in 1986 by Rowan, Kerkman. A good reference of using RC for current control presented in 1999 is D. N. Zmood and G.Holmes [zmo1], [zmo2], articles published by P. Mattavieli [mat]

presents voltage control with RC. In recent years highly popularization and different applications were done by R. Teodorescu and M. Liserre [teo2], [lis5], [key].

The repetitive control technique is also gaining the popularity. In operation it is similar to a bank of RC for infinite number of odd harmonic (bank or resonant filters). It can be used for compensation of harmonic distortion and correcting unbalanced condition. The majority of articles are from Gerardo Escobar [esc1], [esc2]. The implementation is very easy compared to the effort realizing the same functionality in synchronous frame or as a bank of individual resonant filter. The implementation uses feedback array and a delay line.

The problem of active damping of oscillation in LCL filters can be solved by many approaches, the most promising method based on virtual flux is proposed by Malinowski [mal2]. A method proposed by P. A. Dahono [dah1] based on "virtual resistor" requires extra capacitor current sensor. Another method suffering voltage capacitor feedback is lead-lag method proposed by Blasko [bla3]. A method proposed by Marco Liserre has no additional sensors, but generic algorithm is used [lis1], [lis3]. A proper controller tuning which will not lead to oscillations is presented [teo3]
The EMI problems, common mode and diferencial associated with filters can be addressed in [bas].

A converter control based on the virtual flux concept first appears by S. Bhattacharya at. el in 1996 [bha1], M. Chandorkar published in 1999 [cha3], [cha1] and developed later by Malinowski in 2004 [mal1], [mal4], [mal5] for application of active rectifier. The virtual flux approach can also find application or can be used in direct torque control (DTC), hysteresis regulators or multilevel converters [mal4], [ser1], [yin1].

There are several publications for grid impedance estimation. One of the first papers on power system identification was presented by Z. Staroszczyk in 2000. In 2004 A. Tarikianen presented identification algorithm for the purpose of voltage feedback in active filter [tar2]. In 2007 M. Liserre published method based on excitation of LCL filter [lis4]. In 2006 A.V. Timbus and U. Borup presented algorithm based on inter-harmonic current injection for purpose of anti islanding detection [tim2], [tim3].

Different PLL structures for grid synchronization for balanced and unbalanced grid conditions were thoroughly presented by Alvaro Luna, Pedro Rodriguez and Remus Teodorescu [lun1], [cio1], [sil1], [tim1]. They allow implementing power control techniques, fulfilling the power quality requirements and overcoming the grid connection problems. Those PLL structures utilizes the positive and negative sequence decompositions, SOGI filters thus making them very robust against distorted voltage.

Several papers were published on the topic of unbalanced current control. They are based on pulsating power correction and single frame current control, full symmetric decomposition with double current controller [ngc1], [son1], [son2] or direct power control [mal1], [tar1].

For the renewably sources operating in stand alone mode or connected to the grid a good source can be [teo1], [mag2], [rod1]

1.6. Publications

Publications on which I have been author or co-author:

1 A. Kulka, T. Undeland, Junji Kondoh, "Dual Frame Virtual Flux, Voltage Sensor-less Algorithm for Three-Phase VSC in Unbalanced Conditions – Experimental Study" submitted to IEEE Transaction on Power Electronics.

2 A. Kulka, T. Undeland, S. Vazquez, L. G. Franquelo, "Stationary Frame Voltage Harmonic Controller for Standalone Power Generation", Conference Proceedings, EPE 07, Aalborg, Denmark, 2-5 Sept., 2007

3 A. Kulka, T. Undeland, "Grid Inductance Estimation by Reactive Power Perturbation for Sensor-less Scheme Based on Virtual Flux" NORPIE 2008, Espoo, Finland, 9 - 11 June 2008

4 A. Kulka, Tore Undeland, "Voltage harmonic control of Z-source inverter for UPS applications" Conference Proceedings, EPE-PEMC 08, Poznan, Poland,1-3 Sept. 2008

5 J. A. Wiik, A. Kulka, T. Isobe, M. Molinas, K. Usuki, T. Takaku, T. Undeland, R. Shimada, "Control design and experimental verification of a series compensated 50 kW permanent magnet wind power generator" IEEE Power Elec. Spec. Conf., PESC, 15-19 June, 2008.

6 J. A. Wiik, A. Kulka, T. Isobe, K. Usuki, M. Molinas, T. Takaku, T. Undeland, R. Shimada, "Loss and Rating Considerations of a Wind Energy Conversion System with Reactive Compensation by Magnetic Energy Recovery Switch (MERS)", Wind Power to the Grid - EPE Wind Energy Chapter 1st Seminar, 2008. EPE-WECS 2008 27-28 March 2008

7 E. S. Hoff, T. P. Fuglset, A. Kulka, T. M. Undeland, "Power electronics laboratory combined with digital regulators", Power Electronics and Applications, European Conference, 2005

1.7. Contributions to the thesis

The main contributions in the thesis are:

- A dual frame virtual flux model which can cope with unbalanced grid conditions. The model measures only two phase currents and the dc-bus voltage and thus can be named voltage sensor-less. The model uses proposed implementation method for separation of positive and negative sequence. The proposed new flux model is faster in time response, compared to those available in literature. The DC capacitor can be smaller due to possibility of supplying constant power for unbalanced grid condition.
- Instant synchronization to the grid without voltage sensors. Due to the fact that the proposed flux model is fast in time response, the synchronization can occur without pre-sampling the grid for detection of the voltage vector angle. The initial position of the voltage flux is not initialized (left zero). The transient synchronization current occurs during inverter start up procedure for less than half of the grid period and is smaller than 1 *p.u.* When the pre-sampling (short-circuit of the grid) is used, and the flux model is initialized, the synchronization current is maintained under 0.05 *p.u.*
- A grid inductance detection algorithm by perturbation of the reactive power. It is based on insufficient dynamic of the current controller in synchronous frame when the cross-coupling term in current controller does not match the Thevenin equivalent inductance of the infinite grid. By injecting reactive power and observing the i_d, i_q converter current responses the inductance can be estimated.
- A novel implementation method for separation of positive and negative sequence components of the unbalanced signal. The algorithm is computationally lightweight, easy to implement and can be adopted in a wide frequency range. It exploits the fact that the grid frequency variations are smaller compared to those found e.g. in a motor drive.
- Harmonic free voltage control algorithm for nonlinear and unbalanced loads for UPS or stand alone operation. The proposed algorithm uses a bank of resonant filters with quadrature output. For each harmonic, two orthogonal components are available enabling adjusting the phase for system delay cancellation. Because the system delay (important especially for higher harmonic) is taken account a high quality output voltage is achieved. The LC output filter is used.
- The concept of voltage harmonic control for Z-source inverter was implemented and tested for UPS application.
- The introduced ideas have been tested in laboratory for verifications. The experimental results are shown in the thesis at the end of the corresponding chapter.

1.8. List of abbreviations and symbols

A - Ampere
AC - Alternating Current
ADC - Analog to Digital Converter
AIST - Institute of Advanced Science and Technology in Japan
B - Boost ratio of the Z-source inverter
CAN - Controller Area Network bus
CBM - Carrier Based Modulation
CC - Current Controller
CCCC - Current Controller Cross Coupling
D - The distortion power
DC - Direct Current
DCC - Dual Current Controller
DFO - Dual Frame Orientation
DG - Distributed Generation
DPC - Direct Power Control
DSP - Digital Signal Processor
DSC - Delayed Signal Cancellation method
DVF - Dual Virtual Flux
FPGA - Field Programmable Gate Array
GI - General Integrator
HPF - High Pass Filter
IGBT - Insulated Gate Bipolar Transistor
LPF - Low Pass Filter
MOSFET - Metal-Oxide Semiconductor Field Effect Transistor
NS - Negative Sequence
NTNU - Norwegian University of Science and Technology
NSS - Negative Sequence Signal/System
P - The active power
PCC - Point of Common Connection
PID - Proportional Integration Derivative type of controller
PLL - Phase Locked Loop
PS - Positive Sequence
PSS - Positive Sequence Signal/System
p.u. - Per-Unit
PV - Photo Voltaic
PWM - Pulse Width Modulation
Q - The reactive power
RC - Resonant Controller (known as: Resonant Filter or GI
SFO - Single Frame Orientation
ST - Shoot through
SVM - Space Vector Modulation
THD - Total Harmonic Distortion
VF - Virtual Flux
VSC - Voltage Source Converter

VOC - Voltage Oriented Control
ZSI - Z-Source Inverter
ZSS - Zero Sequence Signal
φ_g - The angle of the voltage grid derived from the flux model
i_d^n - The *d*-axis, negative sequence current
v_d^n - The *d*-axis, negative sequence voltage
i_d^p - The *d*-axis, positive sequence current
v_d^p - The *d*-axis, positive sequence voltage
i_q^n - The *q*-axis, negative sequence current
v_q^n - The *q*-axis, negative sequence voltage
i_q^p - The *q*-axis, positive sequence current
v_q^p - The *q*-axis, positive sequence voltage
f_s - Sampling frequency of the control system
$\underline{v}_2$ - Space vector, converter filter output voltage
$\underline{v}_1$ - Space vector, converter terminal average output voltage
$\underline{v}_{1,dq}$ - Converter voltage in synchronous coordinate
v_o - Zero sequence voltage
$\underline{v}_{conv}$ - Space vector of converter voltage
$\underline{v}_{crr}$ - Dead-time correction voltage
$v_{inv,\alpha}$ - Alpha component of inverter voltage
$v_{inv,\beta}$ - Beta component of inverter voltage
v_{ref} - reference voltage for space vector modulation
$v_{l\text{-}l}$ - line to line voltage
f_{sw} - Switching frequency of the converter
$\underline{v}^{\alpha\beta}$ - Voltage space vector
$v_{L,1}$ - The 1st voltage harmonic on inverter filter inductance
$v_{L,5}$ - The 5th voltage harmonic on inverter filter inductance
$v_{c,2}$ - Capacitor voltage in Z-source inverter
$i_{d,ref}$ - The *d*-axis reference current
i_{dc} - The dc-link current
$i_{q,ref}$ - The *q*-axis reference current
$i_{o,1}$ - The 1st current harmonic of the load
$i_{o,5}$ - The 5th current harmonic of the load
K - Scaling factor for Clark transform
$K_{i,neg}$ - Integral gain of the negative sequence of PI regulator
$K_{i,pos}$ - Integral gain of the positive sequence of PI regulator
$K_{p,neg}$ - Proportional gain of the positive sequence of PI regulator
$K_{p,pos}$ - Proportional gain of the positive sequence of PI regulator
K_p - Single frame current controller integral gain
K_i - Single frame current controller proportional gain

L_{cc}	-	Inductance in the cross-coupling term of the current controller
L_{fl}	-	Inductance in the flux model
L_{sys}	-	Power system inductance (without converter filter inductance)
L_{min}	-	Inductance of the converter filter
L_1	-	Converter side inductor in LCL filter
L_2	-	Grid side inductor in LCL filter
L_m	-	Inductance of the grid and converter filter
M	-	Modulation index
m_n	-	The n intermediate sample in the digital filter implementation
y_n	-	The n output sample in the digital filter implementation
sw_x	-	Binary signal controlling the inverter bridges, -1 or 1
S_x	-	Reference modulation signal where x={*a*, *b*, *c*} refers the phase
S_α, S_β	-	Components of switching space vector
T_i	-	Time constant of the integrator
T_{ST}	-	Time duration of the shoot-through
T_s	-	Digital control sampling time
T_{sw}	-	Inverter switching time
U_{DC}	-	The dc-link voltage
v_{dc}	-	The dc-link voltage
v_{ffd}	-	The *d*-axis feed-forward voltage
v_{ffq}	-	The *q*-axis feed-forward voltage
$\underline{\Psi}_{conv}$	-	The converter flux space vector
$\Psi_{g,\alpha}$	-	The alpha component of grid flux
$\Psi_{g,\beta}$	-	The beta component of grid flux

2. INTRODUCTION TO THREE-PHASE CONVERTERS AND CONTROL

This chapter introduces the basics of three-phase voltage source converters. First orthogonal transformation is presented followed by modeling of VSC. Different modulation strategies will be shown based on average output voltages. Model with *L* filter in synchronous frame for balanced and unbalanced grid operation is described.

2.1. Transformations

In order to efficiently deal with the three-phase quantities this section introduce the Clark and Park transforms. The first one converts three-phase system to equivalent two phase notation, the second changes the time reference frame from stationary to synchronous. In literature there are many standards to align axes or scale the transformations which could lead to misunderstanding. Basically the selection can be arbitrary as long as the control keeps up with one standard.

2.1.1. The Clark transformation

The Clark transforms maps three-phase *a, b, c* components which are equally shifted by 120° into a two phase system. The new rotating vector is represented by two orthogonal components α and β and is called space vector. The space vector consists of a real (α) and imaginary (β) part which represents two sinusoids shifted by 90° in time. The β component is lagging 90° after α for positive sequence system.
A natural property of the symmetrical three-phases system is that instantaneous sum of the three components is zero:

$$v_a(t) + v_b(t) + v_c(t) = 0 \tag{2.1}$$

where the arbitrary v_a, v_b, v_c voltages represent an equal amplitude sinusoids shifted in space by 120°.

$$v_a(t) = V\cos\left(\omega_1 t\right) \tag{2.2}$$

$$v_b(t) = V\cos\left(\omega_1 t - 2\pi/3\right) \tag{2.3}$$

$$v_c(t) = V\cos\left(\omega_1 t + 2\pi/3\right) \tag{2.4}$$

This enables to represent one of the components by the other two: e.g. $v_c(t) = -(v_a(t) + v_b(t))$, and description of the three-phase system in two phase is possible.
The general transformation from three to two phase system is given by (2.5):

$$\underline{v}(t) = v_\alpha(t) + jv_\beta(t) = \frac{2}{3}K\left[v_a(t) + v_b(t)e^{j2\pi/3} + v_c(t)e^{-j2\pi/3}\right] \tag{2.5}$$

The zero sequence component is equal:

$$\underline{v}_0(t) = \frac{1}{3}\left(v_a(t) + v_b(t) + v_c(t)\right) \tag{2.6}$$

The selection of *K* can be arbitrary, depending on the application and implementation. One choice may be more convenient than another. The other commonly found in literature scaling factors are:

$$\begin{aligned} &\text{Peak value scaling:} && K = 1 \\ &\text{RMS value scaling:} && K = 1/\sqrt{2} \\ &\text{Power invariant:} && K = \sqrt{3/2} \end{aligned} \tag{2.7}$$

For $K = 1$ the amplitude of the *a* phase is equal to the α component and both have the same phase. A zero angle is defined when α is at the positive peak value and β is crossing zero. All transformations in this thesis uses peak valued scaled space vectors representation, often know as a non power invariant.
Since the $v_a(t), v_b(t), v_c(t)$ are scalar values, and the rotation operator $e^{j2\pi/3}$ can be expressed in scalar form too. The transformation can be expressed in equivalent matrix form as (2.8).

$$\begin{bmatrix} \alpha \\ \beta \\ o \end{bmatrix} = \frac{2}{3}K \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \cdot \begin{bmatrix} a \\ b \\ c \end{bmatrix} \tag{2.8}$$

2.1.1.1. Current transformation

The zero sequence component *o* does not exist in the current of the three-phase load provided that there is no neutral connection. The zero sequence voltage doesn't influence the load currents and it can be used to extend the linear operation of converter. Because in our system neutral wire is not used, *o* is not considered. Simplifying (2.8) and for $K = 1$ the α and β component can be written as:

$$\alpha = a \tag{2.9}$$

$$\beta = \left(a + 2b\right) / \sqrt{3} \tag{2.10}$$

$$\beta = \left(-a - 2c\right) / \sqrt{3} \tag{2.11}$$

$$\beta = \left(b - c\right) / \sqrt{3} \tag{2.12}$$

The β equations (2.10), (2.11), (2.12) are redundant, and the selection depends on the number and phase position of sensors in the system. In most cases use of only two current sensors is sufficient. As far as there is no neutral wire the two current sensors can handle unbalanced and distorted conditions. The zero sequence current should be avoided, that means that the dc-link should not be coupled in any way with the output of the converter or load directly or by other components. This is true for most of the motor control. For detection of the leakage current adding the third sensor doesn't make sense, since the leakage current is usually very small and requires other more sensitive measuring circuits.

2.1.1.2. Voltage transformation

When measuring three-phase voltage in the system without neutral connection, it is convenient to measure phase to phase voltage, since the neutral point is not accessible. Two sensors are required. Example of possible α, β transformation using two sensors in phases *ab* and *bc* result in:

$$\alpha = \left(2ab + bc\right) / 3 \tag{2.13}$$

$$\beta = bc / \sqrt{3} \tag{2.14}$$

The α, β components from (2.13) and (2.14) do not contain the inherited 30° phase shift from phase-phase measurement, they are aligned with phase to neutral reference. The amplitude is scaled to mimics the phase to neutral measurement as well.

The transformation from α, β plane to three-phase system (*abc*) which is known as a reverse Clark transform is given by equation (2.15).

$$\begin{bmatrix} a \\ b \\ c \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1 \\ -\frac{1}{2} & \frac{\sqrt{3}}{3} & 1 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{3} & 1 \end{bmatrix} \begin{bmatrix} \alpha \\ \beta \\ o \end{bmatrix} \tag{2.15}$$

2.1.2. The Park transformation

The Park Transformation converts the stationary system into rotating system which is called synchronous coordinate or *dq* coordinates. A space vector which rotates in one

direction converted by Park transformation will be visible as a (not rotating, similar to the standard) complex phasor. The instantaneous angle of the space vector will be referenced to the θ angle. This transform enables to see rotating vectors as dc quantities, thus simplifying analysis and control. The reference angle θ for synchronous frame is usually synchronized with some other rotating quantity, e.g. voltage. It is important that the reference angle θ rotates smoothly, therefore a PLL or virtual flux is often used. The Park and it's inverse transform are the foundation for regulation of rotating ac systems by using dc regulators. It is easier to design and analyze control for quantities which are constant (dc) rather than oscillating (ac) in the steady state.

The new system quantities are *d* (direct) and *q* (quadrate). The conversion from stationary system (α, β) to synchronous (rotating) system is defined as:

$$\begin{bmatrix} d \\ q \end{bmatrix} = \begin{bmatrix} \cos(\theta) & \sin(\theta) \\ -\sin(\theta) & \cos(\theta) \end{bmatrix} \begin{bmatrix} \alpha \\ \beta \end{bmatrix} \tag{2.16}$$

or in vector form:

$$\underline{v}_{dq} = e^{-j\omega t} \cdot \underline{v}_{\alpha\beta} \tag{2.17}$$

Where $\theta = \omega t$, and ω is the angular speed of the synchronous reference frame, $\underline{v}_{\alpha\beta}$ denote the space vector

The conversion from synchronous system to stationary is defined as:

$$\begin{bmatrix} \alpha \\ \beta \end{bmatrix} = \begin{bmatrix} \cos(\theta) & -\sin(\theta) \\ \sin(\theta) & \cos(\theta) \end{bmatrix} \begin{bmatrix} d \\ q \end{bmatrix} \tag{2.18}$$

or in vector form:

$$\underline{v}_{\alpha\beta} = e^{j\omega t} \cdot \underline{v}_{dq} \tag{2.19}$$

In case of direct transformation from three-phase system (*abc*) to synchronous system (*dq*) the equation are given by:

$$\begin{bmatrix} d \\ q \end{bmatrix} = \frac{2}{3} K \begin{bmatrix} \cos(\theta) & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ -\sin(\theta) & -\sin(\theta - \frac{2\pi}{3}) & -\sin(\theta + \frac{2\pi}{3}) \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \tag{2.20}$$

The reverse transformation to (2.20) are given by:

$$\begin{bmatrix} a \\ b \\ c \end{bmatrix} = \begin{bmatrix} \cos(\theta) & -\sin(\theta) \\ \cos(\theta - \frac{2\pi}{3}) & -\sin(\theta - \frac{2\pi}{3}) \\ \cos(\theta + \frac{2\pi}{3}) & -\sin(\theta + \frac{2\pi}{3}) \end{bmatrix} \begin{bmatrix} d \\ q \end{bmatrix} \tag{2.21}$$

In the digital signal processing theory the Park transformation is known as a shift in frequency domain. Park transformation causes all frequency components to be shifted by a specified frequency. This is why 50 *Hz* signal shifted with -50 *Hz* become a DC signal; analogously the 250 *Hz* signal becomes a 200 *Hz*.

Considering the non-sinusoidal signals and transforming them to synchronous frame the sequence of the harmonic must me taken into account. The multiplies of 3rd harmonic (triplen harmonic) are the zero-sequence harmonics, thus even if they exist in the voltage they disappear from the currents. So in three-phase systems harmonics 5, 7, 11, 13, 19,... are those which needs to be taken care. An interesting observation is when signal contains 5th harmonics with negative sequence and 7th harmonic with positive sequence then they will appear in the synchronous frame as 6th harmonic (positive and negative). Analogously the same happens to the -11th and +13 harmonic and so on.

2.2. Modeling of the ideal converter bridge

For the modeling and control purpose usually the ideal switch is assumed, Figure 2.1. The ideal switch changes position between positive and negative supply rail instantaneously and assumes that the voltage drop across the switches are zero. The neutral point is assumed to be in the middle of the splited dc-link voltage. For this configuration the sw_x signals can attain only two discrete values, $+1 \text{and} -1$ which corresponds to output phase connected to $v_{dc}/2$ or $-v_{dc}/2$. Now we will introduce the continuous switching reference signals S_a, S_b, S_c which can be treated as a control signals. They define the proportion of the switch to be in the upper ($sw_x = 1$) or lower ($sw_x = -1$) position. Signal S_x equal of 0 means that the switch 50% of the time is in upper and 50 % of the time in lower position. The output phase voltage is achieved by multiplying the reference signals S_a, S_b, S_c by $v_{dc}/2$. The v_a, v_b, v_c denote average converter output voltage related to *n*. In literature there are other reference configurations e.g. the reference ranges between 0 and 1 and the dc-link consist of one dc-source, with negative dc-bus rail as *n*.

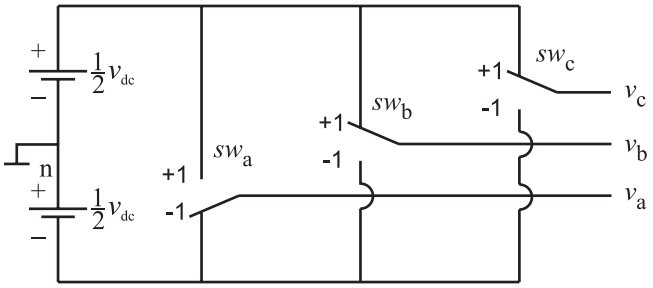

Figure 2.1: Switch model of three-phase VSC

The relationship between reference signal S_x, dc-link voltage and average output voltage is as follows:

$$v_a = \frac{1}{2} v_{dc} \cdot S_a \tag{2.22}$$

$$v_b = \frac{1}{2} v_{dc} \cdot S_b \tag{2.23}$$

$$v_c = \frac{1}{2} v_{dc} \cdot S_c \tag{2.24}$$

The phase to phase voltage relation to the reference signals are:

$$\begin{bmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \end{bmatrix} = \begin{bmatrix} v_a - v_b \\ v_b - v_c \\ v_c - v_a \end{bmatrix} = \frac{1}{2} v_{dc} \begin{bmatrix} S_a - S_b \\ S_b - S_c \\ S_c - S_a \end{bmatrix} \tag{2.25}$$

In order to achieve three-phase symmetric voltages the S_x represents sinusoidal waveforms with equal amplitude, shifted by 120°.

$$v_a(t) = \frac{1}{2} v_{dc} M \cos(\omega_1 t) \tag{2.26}$$

$$v_b(t) = \frac{1}{2} v_{dc} M \cos(\omega_1 t - 2\pi/3) \tag{2.27}$$

$$v_c(t) = \frac{1}{2} v_{dc} M \cos(\omega_1 t + 2\pi/3) \tag{2.28}$$

Now the three-phase output voltage is characterized by two parameters, ω_1 and M. The ω_1 defines the angular frequency and M defines the maximum amplitude of the output voltage. The M is often called the modulation index and defines the linear range of converter operation. M range depends on the type of modulation used, in above case the range is ($0 \le M \le 1$). The $M > 1$ causes saturation of the converter and distortion of the

output voltage (over-modulation). By adding zero sequence signals to S_a, S_b, S_c it is possible to extend the range of M. The discussion is below in this chapter.

Using the space vector notation, the voltage vector of the VSC $\underline{v}_1$ can be expressed as:

$$\underline{v}_1(S_a, S_b, S_c,) = \frac{v_{dc}}{2}\frac{2}{3}\left(S_a + S_b e^{j2\pi/3} + S_c e^{-j2\pi/3}\right) \tag{2.29}$$

And by introducing the switching reference space vector $\underline{S} = Me^{j\omega_1 t}$, the (2.29) can be expressed as:

$$\underline{v}_1 = \frac{1}{2} v_{dc} \underline{S} \tag{2.30}$$

2.3. Modulation strategies

The modulation strategy will be discussed for the most common 2 level converter topology. A good reference for other modulation techniques is [mal5], [swe1] The modulator is responsible to produce timing pulses sw_a, sw_b, sw_c for the transistors from the switching reference signals S_a, S_b, S_c. There are many modulation strategies; the most common are: space vector modulation, sinusoidal modulation with 3rd harmonic, hysteresis. In Figure 2.2 the ideal switches from Figure 2.1 are replaced by two transistors and two anti-parallel diodes per bridge.
There are 6 signals that control the transistors. The two signals in each bridge are fully dependent of each other. If the top transistor is on state, the bottom transistor is off (sw_x=1), and vice versa for (sw_x=-1). From modeling point of view there is still three independent on/off signals belonging to each bridge (sw_a, sw_b, sw_c).

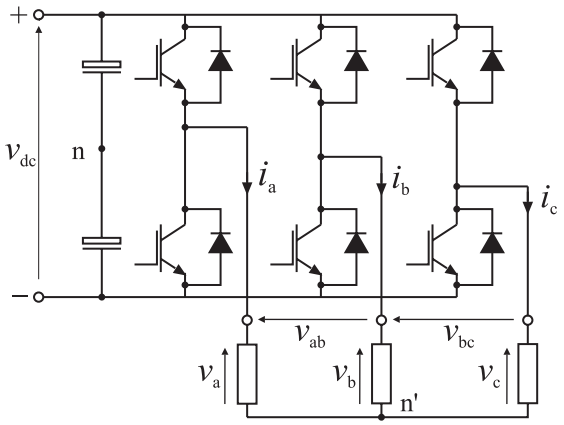

Figure 2.2: Two level, three-phase converter with the load

With three binary control signals, there are 8 possible states in total. When all top or bottom transistors are on, the power is not supplied to the load. These two states are called zero vectors (or inactive states). The remaining 6 states are the active states. By

applying consequent active vectors from Table 2.1 on the load from Figure 2.2 resulting voltage can be seen in Figure 2.3.

Voltage vector	sw_a	sw_b	sw_c	Zero Sequence	v_α	v_β
v0	-1	-1	-1	$-v_{dc}/2$	0	0
v1	1	-1	-1	$-v_{dc}/6$	$v_{dc}2/3$	0
v2	1	1	-1	$v_{dc}/6$	$v_{dc}/3$	$v_{dc}/\sqrt{3}$
v3	-1	1	-1	$-v_{dc}/6$	$-v_{dc}/3$	$v_{dc}/\sqrt{3}$
v4	-1	1	1	$v_{dc}/6$	$-v_{dc}2/3$	*0*
v5	-1	-1	1	$-v_{dc}/6$	$-v_{dc}/3$	$-v_{dc}/\sqrt{3}$
v6	1	-1	1	$v_{dc}/6$	$v_{dc}/3$	$-v_{dc}/\sqrt{3}$
v7	1	1	1	$-v_{dc}/2$	0	0

Table 2.1: Individual vectors and associated states of converter bridges

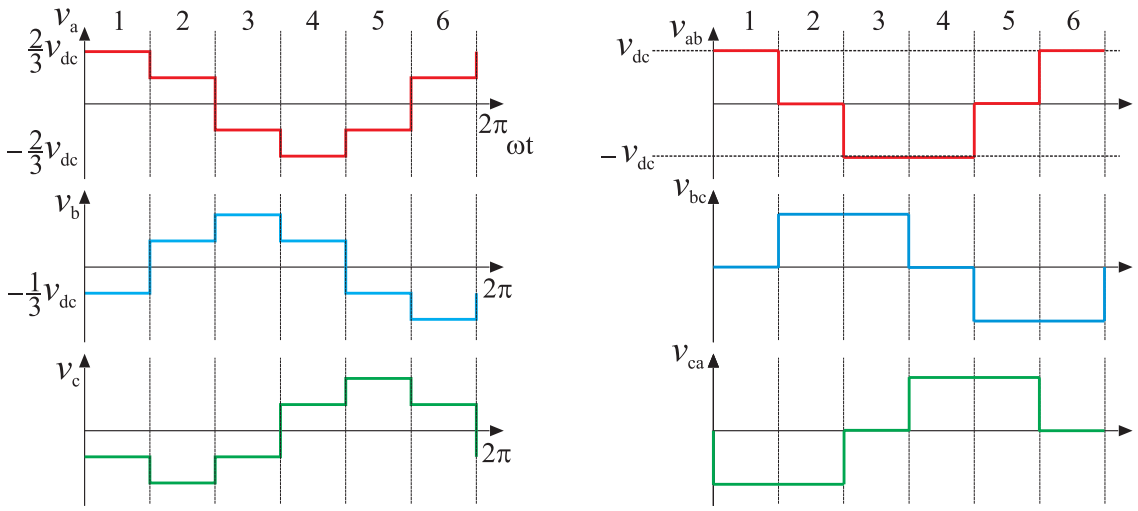

Figure 2.3: The phase output voltage related to dc-link voltage when a sequence of active vectors is applied. The left figure shows the voltage over resistor load when load phases are connected in star. The right figure shows the phase to phase output voltage.

This modulation strategy is called 6-step square modulation. There is no practical use of it for grid connected converters; however it serves the basics for space vector modulation. This modulation can be utilized in electric machines, e.g. brushless dc-motor (BLDC).

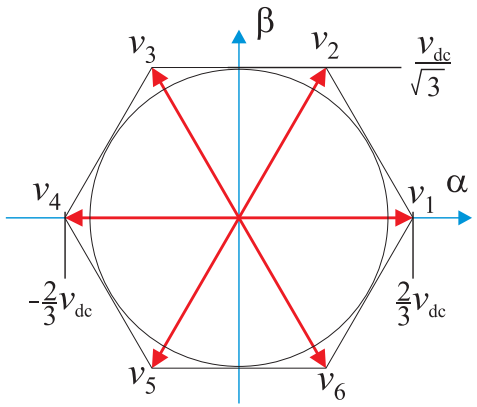

Figure 2.4: Red - active vectors in the α, β plane, that can only be obtained

It is visible in Figure 2.4 that by combining all switching states by using PWM including the zero vectors, any voltage inside the hexagon can be obtained. The zero vectors are placed in the origin of the Figure 2.4. The inscribed circle limits the linear modulation range, the radius of the circle is $v_{dc}/\sqrt{3}$. That leads to conclusion that the maximum obtainable phase voltage is: $|v_1|_{\max} = v_{dc}/\sqrt{3}$

Extending modulation beyond the inscribed circle is called over-modulation. It results in distorted voltage waveforms and should not be used during steady state, however in transients can be used.

2.3.1. Sinusoidal modulation

Sinusoidal modulation or carrier base modulation (CBM) is classical approach, often used in literature. Bases on comparison of triangular carrier signal with reference signals S_a, S_b, S_c seen in Figure 2.5. The comparison results are the logic signals (sw_a, sw_b, sw_c) which switch on and off the transistors in given bridge (Figure 2.6). The three-phase reference signals are displaced in space by 120°.

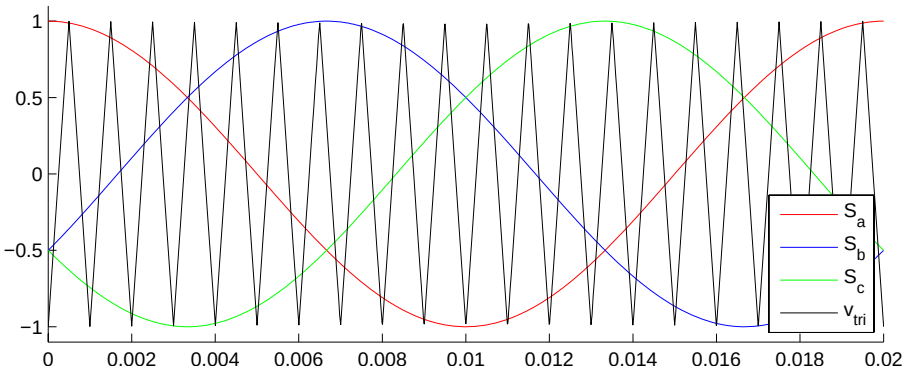

Figure 2.5: Sinusoidal modulation signals. Black – triangular carrier signal, red, blue and green the modulation reference signals.

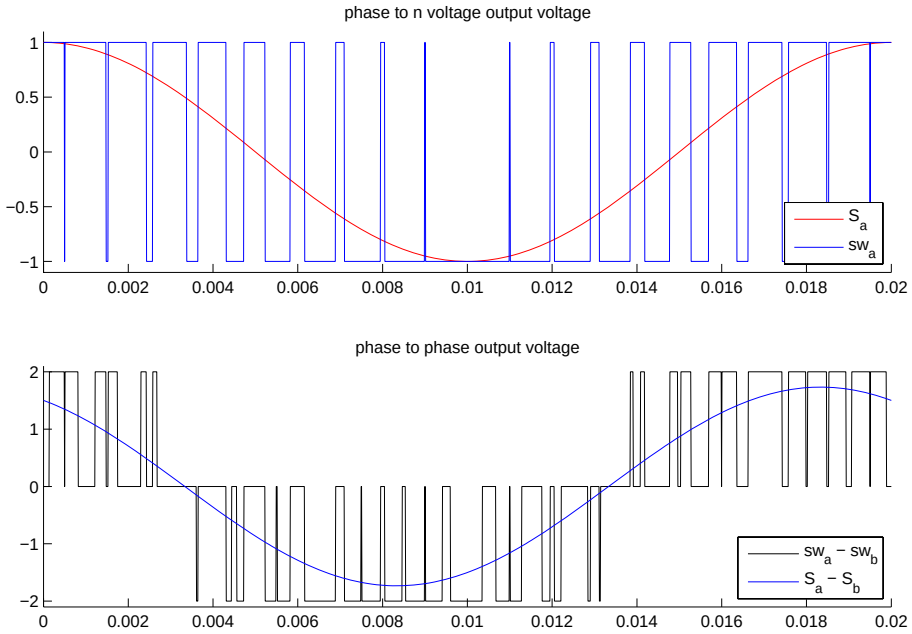

Figure 2.6: Modulation signal and gate signal which corresponds to output voltage. Upper - phase to neutral output voltage. Lower - phase to phase output voltage.

The switching frequency is constant and thus the voltage harmonics are concentrated around the carrier frequency and it's multiplies. The drawback is short linear operations range because the third harmonic zero sequence signals is not utilized.
The maximum peak phase output voltage is equal to half of dc-link voltage:

$$\left|\underline{v}_1\right|_{\max} = \frac{v_{dc}}{2} \tag{2.31}$$

or the maximum line to line peak voltage is:

$$\left|v_{l-l}\right| = \frac{\sqrt{3}v_{dc}}{2} = 0.866 \cdot v_{dc} \tag{2.32}$$

The reference control signals are calculated from modulation index M, and angular frequency ω.

$$S_a(t) = M\cos\left(\omega_1 t\right) \tag{2.33}$$

$$S_b(t) = M\cos\left(\omega_1 t - 2\pi/3\right)$$

$$S_c(t) = M\cos\left(\omega_1 t + 2\pi/3\right)$$

Linear range of operation is limited to $0 \le M \le 1.0$.

2.3.2. Sinusoidal modulation with the third harmonic

By adding the zero-sequence third harmonic signal to all three references the linear range can be expanded without causing over-modulation. The utilization of dc-link voltage is improved (Figure 2.7b) almost at no cost. The injected third harmonic zero sequence signals appears on each of the inverter terminal voltages v_{an}, v_{bn}, v_{cn} however it vanish from phase to phase voltage.

$$S_a(t) = M\cos(\omega_1 t) + v_0 \tag{2.34}$$

$$S_b(t) = M\cos(\omega_1 t - 2\pi/3) + v_0$$

$$S_c(t) = M\cos(\omega_1 t + 2\pi/3) + v_0$$

Where the zero sequence signal is:

$$v_0 = V_0\cos(3\omega_1) \tag{2.35}$$

V_0 represents amplitude, $V_0 \in \langle 0.166...0.25 \rangle$

Linear range of operation is $0 \le M \le 1.15$.

The zero sequence signals with the same amplitude and angle displacement cancel each other in each phase thus not causing line to line distortion. The Figure 2.7 is made in vertical fashion to illustrate the output voltage and boundary of the dc-link voltage. The horizontal axis reflects to real voltage (measurable) and thus the dc-link boundary can be placed vertical. This makes an easy visualization of the zero sequence signal, dc-link voltage and reference signals together. When the reference vector goes beyond the dc-link boundary the over-modulation occurs.

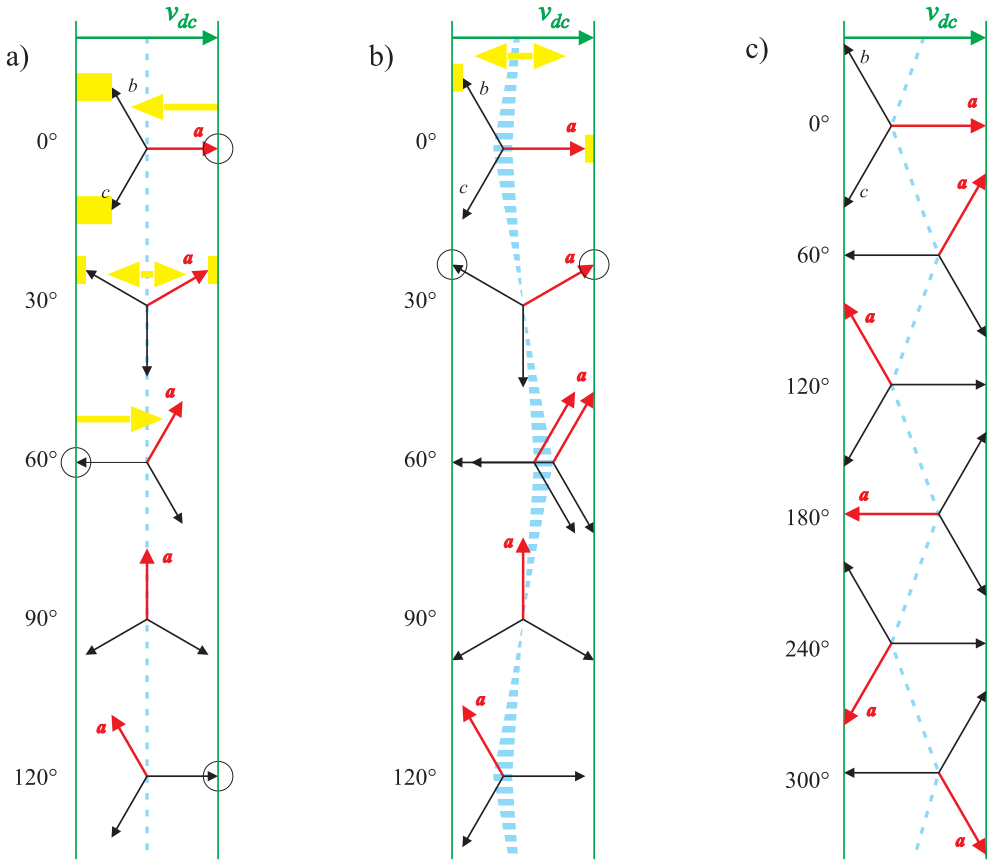

Figure 2.7: Different modulation strategies and different maximum reference voltages

The colors in the Figure 2.7 have the following meaning:
Green - available dc-link voltage span where the reference vector should be placed.
Blue - the zero sequence component and its possible span.
Red - the reference *a* phase vector. The circle shows the limitation (end of linear range).
Yellow - possibility of adding the zero sequence and its direction.
The following sub-figures in Figure 2.7 represents:

a) Sinusoidal modulation without third harmonic, $|\underline{v}_1|_{\max} = v_{dc} / 2$.

b) Sinusoidal modulation with third harmonic, $|\underline{v}_1|_{\max} = v_{dc} / \sqrt{3}$.

c) Six-step modulation and all its positions, $|\underline{v}_1|_{\max} = v_{dc} 2 / 3$

By adding the third harmonic ZSS the maximum phase to phase peak voltage is equal to the dc-link voltage, $\hat{v}_{l-l} = v_{dc}$ thus the linear range is expanded by $2/\sqrt{3}$, which give 15.5 % gain compared to its version without ZSS.
The freedom in shape selection of zero-sequence signal is visible in Figure 2.7b as a blue vertical band. Based on Figure 2.7b the amplitude of the ZSS can be calculated and it should be in the range of 0.166 to 0.245 of the reference amplitude. In practice however this method is not so common due to extra effort to calculate the ZSS.

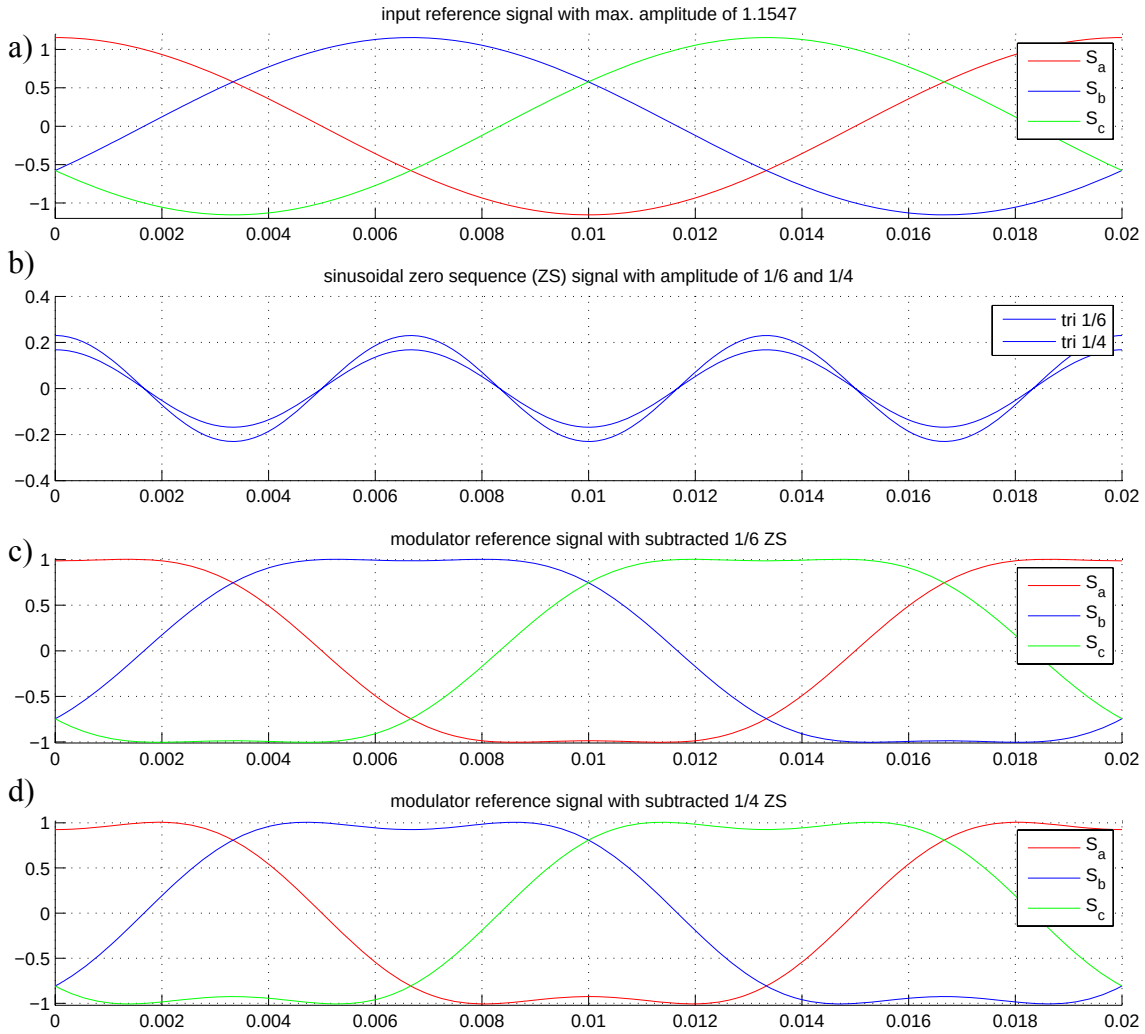

Figure 2.8: Sinusoidal modulation with it maximum and minimum allowed amplitude of sinusoidal zero sequence signal.

As it can be seen in Figure 2.8c the addition of ZSS with amplitude of 1/6 causes almost one phase to be continuously on. This is not desired, since the effective switching frequency is lower and the current ripple can increase. However if properly designed it can be used to decrease switching losses. This type of modulation is called discontinuous modulation. The addition of ZSS with amplitude of 0.25 (Figure 2.8d) improves the situation, but it is clear that the sinusoidal shaped ZSS is not optimal. This is because the shape (Figure 2.8d, blue, between 5 to 8 *ms*) on top side is different than on bottom (green and red).

From practical point of view it is important to keep references away from inverter saturation boundary. In those instances the sensor measurement normally is performed. For the most common symmetrical synchronous sampling method, prevention of switching in this region will cause less noise which can influence the sensor reading.

A good practice would be to limit the duty ratio slightly (e.g. to 99.5 %) to ensure that no switching is performed during measurement, this will not have any influence from control point of view.

2.3.3. Space vector modulation

The SVM bases on vector representation and the proportional selection of converter available states during the switching period. In two-level converter there are six active vectors and two zero vectors (Figure 2.9) to choose from. The states are the same as in the case of six-step modulation shown in Figure 2.7c. The main idea behind SVM is that it uses formula to calculate timing of active (2.36), (2.37) and zero (2.38) vectors. The t_1 and t_2 are the duration time of two neighbor's active states in given sector, the rest of the time t_0 is used for zero vectors. So instead using reference triangular carrier, the equations below are used to calculate the duty ratio of the transistor bridges.

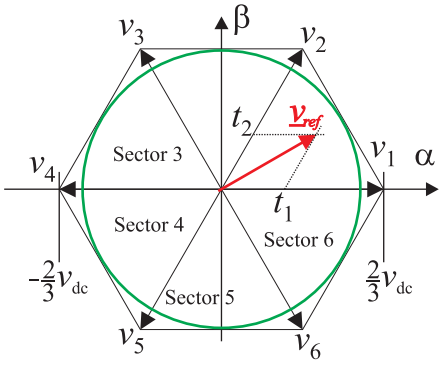

Figure 2.9: Space vector diagram of 2-level converter.

$$t_1 = \frac{\sqrt{3} \cdot T_{sw} \cdot v_{ref}}{v_{dc}} \cdot \sin\left(\frac{\pi}{3} - \theta\right) \tag{2.36}$$

$$t_2 = \frac{\sqrt{3} \cdot T \cdot_{sw} v_{ref}}{v_{dc}} \cdot \sin(\theta) \tag{2.37}$$

$$t_0 = T_{sw} - t_1 - t_2 \tag{2.38}$$

The maximum magnitude of the reference vector $\underline{v}_{\text{ref}}$ corresponds to the radius of the largest circle inscribed within the hexagon shown in Figure 2.9. Since the hexagon is formed by six active vectors having a length of $2v_{\text{dc}}/3$, the maximum reference can be found as: $\left|\underline{v}_{ref,\max}\right| = \frac{2v_{dc}}{3} \cdot \frac{\sqrt{3}}{2} = \frac{v_{dc}}{\sqrt{3}}$, which is the same result as carrier base modulation with ZSS.

The implementation of SVM needs first to calculate the current sector and angle inside it. Based on the angle in the range of first sector the proportion of two active and one zero-vector is calculated as, t_1, t_2 and t_0. The zero state t_0 is usually split into half (t_0 and t_7) for symmetrical PWM and minimum number of possible switching. The duty ratio is calculated for individual phases and then programmed into PWM registers. The implementation of the PWM unit in most microcontrollers consists of a timer and three compare units. When the counting timer value match the compare value a switching action occurs.

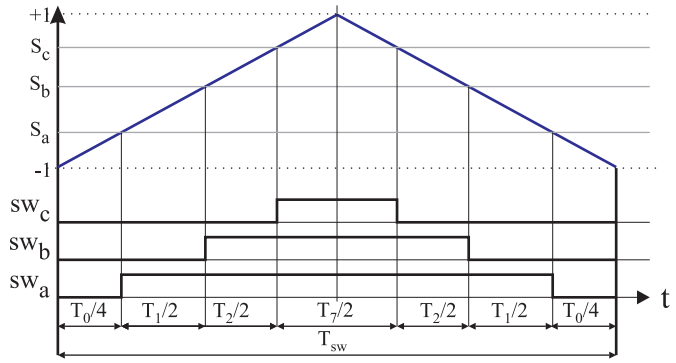

Figure 2.10 Symmetrical Space Vector Modulation, timing diagram

The SVM gives the same linear operation range as carrier based modulation with ZSS. The only difference is in the treatment of variables. In case of sinusoidal modulation the treatment is in natural coordinates and in case of SVM the timing are calculated based on equations (2.36), (2.37), (2.38). The SVM is probably the most common method to derive transistors timing due to its simplicity. More detail can be found in [mal5], [gul2].

There are various modifications of SVM, the aim is to decrease switching losses by introducing switching only in two phases, where the third bridge is continuously on. This group of modulations is called discontinuous SVM (DSVM) and is more described in [mal5]. The disadvantage is that the effective switching frequency is reduced by 33 % but at the same time the switching losses can be decreased up to 50 % dependent on the power factor.
There are some comments regarding implementing on low end DSP or microcontroller. The SVM calculations for the low end DSP system is quite demanding as for the job of only deriving timing pulses. It uses trigonometric functions which are often not available or time optimized on microcontrollers. Implementation often uses *switch* and multiple *case* statements, which are used to find the proper sector (0 to 5), those are causing slightly varying execution time. The simple method presented below presents similar functionality to SVM but with much less of computational burden.

2.3.4. Symmetrical sub-oscillation method

There are computationally less intensive modulation strategies than SVM. This modulation strategy fully utilizes the dc-link voltage and permits extending the modulation range to the entire hexagon from Figure 2.9. There is no reason why the entire hexagon should not be used during transients. The zero-sequence signal is automatically derived. The idea is based on assumption that it is possible to derive the zero sequence signal by looking at the instantaneous phase reference signals (Figure 2.11a), and center it. First the maximum and minimum envelope is found (Figure 2.11b). The average value of envelope is found by adding the upper and lower boundary and dividing it by 2. The average signal (Figure 2.11c) is assumed to be the zero-sequence signal which is subtracted from the input signal (Figure 2.11a). In Figure 2.11a at the time index of 0.02 *s*. the reference is increased to its maximum 1.15. As a

result, observing the modulator output in Figure 2.11d the modulator signal is not greater than 1, which is not causing over-modulation.

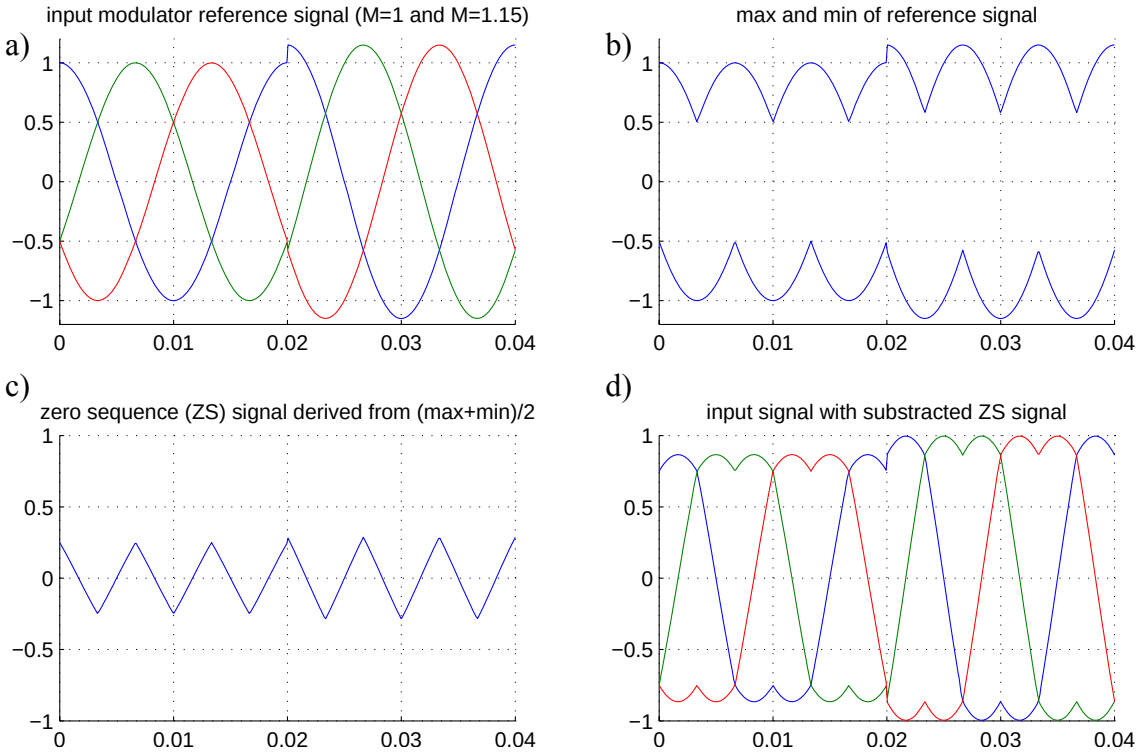

Figure 2.11: Evolution of the signal in proposed simple modulation scheme

The zero sequence signal can be expressed as:

$$v_0 = \frac{1}{2}\left(\max\{v_a, v_b, v_c\} + \min\{v_a, v_b, v_c\}\right) \tag{2.39}$$

And the new modulator signals are:

$$v'_x = v_x - v_0, x = \{a, b, c\} \tag{2.40}$$

The disadvantage of that modulation is that the shape of the zero-sequence signal is not optimal and in some specific inverter environment can cause higher harmonics resulting in leakage current. Improvements in the spectrum can be done by randomizing the ZSS. The advantage is that it is computationally lightweight and thus leaving more time for other control algorithms. Or alternatively the switching frequency can be higher due to shorter execution time. This method was suggested in [swe1] which make the control signals symmetrical, and therefore the name is symmetrical suboscillation method.

2.4. Mathematical model of the converter with L filter

A detailed understanding of VSC model and dynamic behavior enables better design of controller. A single-phase representation of three-phase PWM converter connected to the grid is shown in Figure below.

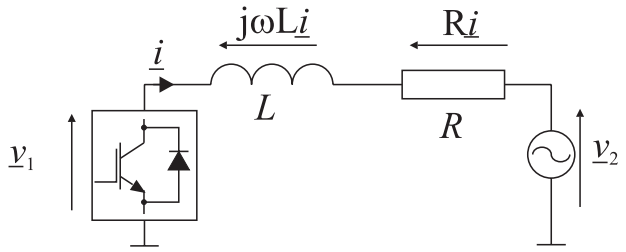

Figure 2.12: Simplified one phase model of VSC.

2.4.1. Ac side model

The PWM converter can be described in vector form based on Figure 2.12 as:

$$\underline{v}_1 = L\frac{d}{dt}\underline{i} + R\underline{i} + \underline{v}_2 \tag{2.41}$$

The $\underline{v}_1$ denotes the inverter average voltage, $\underline{v}_2$ denotes the symmetrical source voltage. The $\underline{v}_1$, $\underline{v}_2$, $\underline{i}$ are stationary frame space vectors with constant angular frequency ω. By multiplying space vectors with $e^{-j\omega t}$ the synchronous variables can be obtained:

$$\underline{v}_1^{\alpha\beta} e^{-j\omega t} = \underline{v}_1^{dq} \tag{2.42}$$

$$\underline{v}_2^{\alpha\beta} e^{-j\omega t} = \underline{v}_2^{dq} \tag{2.43}$$

$$\underline{i}^{\alpha\beta} e^{-j\omega t} = \underline{i}^{dq} \tag{2.44}$$

The superscript $\alpha\beta$ denotes space vector or vector in stationary reference frame and dq denotes synchronous frame. In order to represent the model in synchronous frame, vectors in the equation (2.41) must be expressed using (2.42), (2.43), (2.44).

$$\underline{v}_1^{dq} e^{j\omega t} = L\frac{d}{dt}\left(\underline{i}^{dq} e^{j\omega t}\right) + \left(R\underline{i}^{dq} + \underline{v}_2^{dq}\right) e^{j\omega t} \tag{2.45}$$

The derivation of $L\frac{d}{dt}\left(\underline{i}^{dq} e^{j\omega t}\right) = L\left(\frac{d}{dt}\left(\underline{i}^{dq}\right) + j\omega\underline{i}^{dq}\right)$ and after rearranging the (2.41) results in:

$$\underline{v}_1^{dq} = \left(j\omega L + R \right) \underline{i}^{dq} + L \frac{d}{dt} \left(\underline{i}^{dq} \right) + \underline{v}_2^{dq} \tag{2.46}$$

The equation (2.46) can be decomposed into real and imaginary part, resulting in two equations, (2.47) for *d*- and (2.48) for *q*-axis.

$$v_{1,d} = Ri_d + L \frac{d}{dt} i_d + v_{2,d} - \omega L i_q \tag{2.47}$$

$$v_{1,q} = Ri_q + L \frac{d}{dt} i_q + v_{2,q} + \omega L i_d \tag{2.48}$$

2.4.2. Dc-side model with capacitor.

In order to model the dc-side and capacitor, the current supplied externally by the dc source and currents supplied from the inverter must be known. The dc-bus voltage dynamics are based on the principle of power balancing.

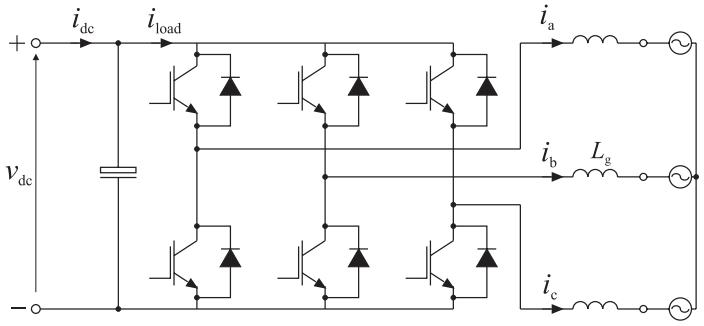

Figure 2.13: Current references used for modeling.

$$C \frac{d}{dt} v_{dc} = i_{dc} - i_{load} \tag{2.49}$$

Where the direction of reference currents can be seen in Figure 2.13.
In steady state i_{load} should be equal i_{dc}. The current i_{load} can be known from the power on the ac side of the converter. The instantaneous ac active power is:

$$p_{load} = \frac{3}{2} \mathrm{Re}\{\underline{v}_1 \cdot \underline{i}_1^*\} \tag{2.50}$$

i_{load} can be expressed as:

$$i_{load} = P_{load} / v_{dc} \tag{2.51}$$

The inverter voltage $\underline{v}_1$ according (2.30) can be expressed in (2.50) as a function of $\underline{S}$ and v_{dc}, and then substituted to (2.51) resulting in:

$$i_{load} = \frac{3}{2}\frac{1}{2}\left(i_\alpha S_\alpha + i_\beta S_\beta\right) \tag{2.52}$$

Where S_α, S_β are the components of switching space vector $\underline{S}$. After transforming (2.49) to synchronous coordinate it result in:

$$C\frac{d}{dt}v_{dc} = i_{dc} - \frac{3}{4}\left(i_d S_d + i_q S_q\right) \tag{2.53}$$

Finally the model of the complete PWM converter in synchronous frame is shown in the Figure 2.14 below.

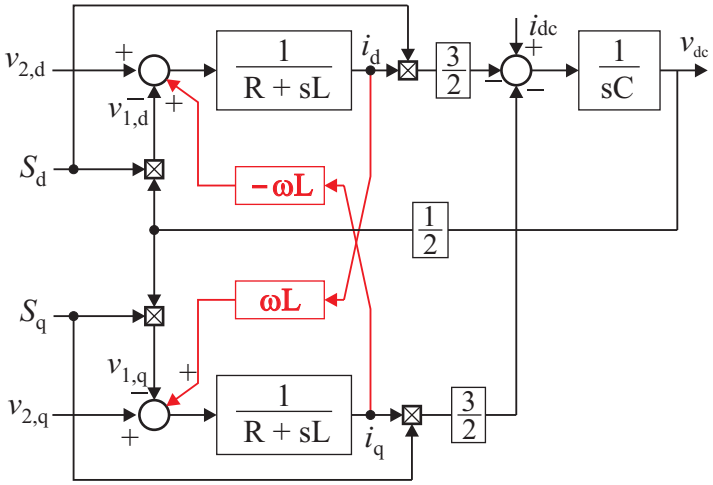

Figure 2.14 Model of the PWM converter in synchronous frame

The visible on Figure 2.14 scaling factors 3/2 and 1/2 can vanish if the power invariant scaling ($K = \sqrt{3/2}$) would be used for Park transformation.

2.4.3. Instantaneous power theory for symmetrical system

The instantaneous reactive power theory was introduced in early 80's by Akagi et al., [aka1], [aka2]. For three-phase symmetrical system (2.54) and (2.55) returns the active and reactive instantenous power. In case of an unbalanced system the interpretation is different because new pulsating power components appear. Using peak value scaled space vector representation (2.7) the active and reactive instantaneous power in symmetrical system can be expressed as:

$$p = \frac{3}{2}\left(v_\alpha i_\alpha + v_\beta i_\beta\right) = u_a i_a + u_b i_b + u_c i_c \tag{2.54}$$

$$q = \frac{3}{2}\left(v_\beta i_\alpha - v_\alpha i_\beta\right) = \frac{1}{\sqrt{3}}\left(u_{bc} i_a + u_{ca} i_b + u_{ab} i_c\right) \tag{2.55}$$

or by using space vector notation

$$p = \frac{3}{2}\mathrm{Re}\{\underline{u}_1 \underline{i}^*\} \tag{2.56}$$

$$q = \frac{3}{2}\mathrm{Im}\{\underline{u}_1 \underline{i}^*\} \tag{2.57}$$

2.5. Mathematical model of the converter with L filter under unbalanced voltage

Based on the knowledge of the previous section 2.4 the model of the VSC for unbalanced voltage can be easily derived. The model can be seen as orthogonal sum of positive sequence system and negative sequence system. The converter three-phase input voltage in synchronous frame can be represented as:

$$\underline{v}_{1,dq} = e^{j\omega t}\underline{v}^p_{1,dq} + e^{-j\omega t}\underline{v}^n_{1,dq} \tag{2.58}$$

The line current is also expressed as $\underline{i}_{dq} = e^{j\omega t}\underline{i}^p_{dq} + e^{-j\omega t}\underline{i}^n_{dq}$, where ω is the angular frequency. The equation (2.59), (2.60), (2.61), (2.62) describes dynamics of the ac side variables in the terms of their separated *dq* frame components. The voltage $\underline{v}_1$ denotes the inverter unbalanced average voltage, $\underline{v}_2$ denotes the unbalanced source voltage. Superscripts *p* and *n* denote the positive and negative sequence components respectively.

$$v^p_{1,d} = Ri^p_d + L\frac{d}{dt}i^p_d + v^p_{2,d} + \omega L i^p_q \tag{2.59}$$

$$v^p_{1,q} = Ri^p_q + L\frac{d}{dt}i^p_q + v^p_{2,q} - \omega L i^p_d \tag{2.60}$$

$$v^n_{1,d} = Ri^n_d + L\frac{d}{dt}i^n_d + v^n_{2,d} - \omega L i^n_q \tag{2.61}$$

$$v^n_{1,q} = Ri^n_q + L\frac{d}{dt}i^n_q + v^n_{2,q} + \omega L i^n_d \tag{2.62}$$

The difference between (2.59),(2.60) and (2.61),(2.62) is the sign of cross-coupling term $\omega L i_d, \omega L i_q$. This implies also that the controller of this plant is different than for balanced system, and must control positive and negative sequence components.

2.5.1. Instantaneous power theory for unsymmetrical system

For the three-phase symmetric system the power definitions are well established. For unbalanced systems there many definitions of power components. A general approach is to define active and reactive power along with distortion power *D* as:
Where

$$P = \sum_{n=1}^{\infty} v_n i_n \cos\gamma \tag{2.63}$$

$$Q = \sum_{n=1}^{\infty} v_n i_n \sin\gamma \tag{2.64}$$

$$S = \sqrt{\sum_{n=1}^{\infty} v_n^2 \sum_{n=1}^{\infty} i_n^2} \tag{2.65}$$

$$D = \sqrt{S^2 - P^2 - Q^2} \tag{2.66}$$

D is a general term for components which do not fit into the P, Q, S, definitions. In an unbalanced condition the negative sequence component is producing power ripples which are visible as a second harmonic of positive sequence. They distort the current waveforms and produce voltage ripples in the dc-link. Usually the main objective is to remove them or compensate by proper control of VSC.
For our control purpose the most frequently proposed power theory by Akagi [aka1] together with symmetric component decomposition is used. The space vector representation of voltages and currents do not contain the zero sequence components. The instantaneous active and reactive power is:

$$p = \frac{3}{2}\left(\underline{v}_d \underline{i}_d + \underline{v}_q \underline{i}_q\right) \tag{2.67}$$

$$q = \frac{3}{2}\left(\underline{v}_q \underline{i}_d - \underline{v}_d \underline{i}_q\right) \tag{2.68}$$

The power flow in particular point may be divided into several terms that are derived from different combination of voltage and current sequence. The power equations for unbalanced condition for three-phase system are in Appendix C.

For two phase systems, the definition of the active and reactive power is split into more terms.

$$p_0 = \frac{3}{2}\left(v_d^p \cdot i_d^p + v_q^p \cdot i_q^p + v_d^n \cdot i_d^n + v_q^n \cdot i_q^n\right) \tag{2.69}$$

$$q_0 = \frac{3}{2}\left(v_q^p \cdot i_d^p - v_d^p \cdot i_q^p + v_q^n \cdot i_d^n - v_d^n \cdot i_q^n\right) \tag{2.70}$$

The remaining combinations correspond to cross product between positive and negative sequences. Those terms represents the oscillating power [rio1], [son1].

$$p_c = \frac{3}{2}\left(v_d^p \cdot i_d^n + v_q^p \cdot i_q^n + v_d^n \cdot i_d^p + v_q^n \cdot i_q^p\right) \tag{2.71}$$

$$p_s = \frac{3}{2}\left(v_d^p \cdot i_q^n - v_q^p \cdot i_d^n - v_d^n \cdot i_q^p + v_q^n \cdot i_d^p\right) \tag{2.72}$$

$$q_c = \frac{3}{2}\left(v_q^p \cdot i_d^n - v_d^p \cdot i_q^n - v_d^n \cdot i_q^p + v_q^n \cdot i_d^p\right) \tag{2.73}$$

$$q_s = \frac{3}{2}\left(v_d^p \cdot i_d^n + v_q^p \cdot i_q^n - v_d^n \cdot i_d^p - v_q^n \cdot i_q^p\right) \tag{2.74}$$

Only the (2.69), (2.70), (2.71), (2.72) power terms can be controlled by the converter currents. The (2.69), (2.70) are controlling the P and Q as in standard single frame symmetrical system. The instantaneous active power can be expressed as:

$$p(t) = p_0 + p_c \cos(2\omega t) + p_s \sin(2\omega t) \tag{2.75}$$

$$q(t) = q_0 + q_c \cos(2\omega t) + q_s \cos(2\omega t) \tag{2.76}$$

As can be noticed from (2.75) the unbalanced voltage can produce second harmonic power components that causes the dc-link ripples. Therefore the (2.71), (2.72) which represents oscillating power should be controlled to zero. The second harmonic reactive power components (2.73)(2.74) are not considered in the unity power factor controller as its average value is zero.

2.6. Dead-time effects and its correction

In the previous sections we have assumed ideal transistors which switching instantaneously. In practice however there are safety precautions and other reasons causing the delay in the signal path. When transistors are switching in one leg, there is short time duration of time inserted causing both transistors to be in off state. This is commonly called dead time and prevents cross conducting current through the bridge when the transistors are changing state. The dead time is usually in the range of few μs so for any condition it must ensure no cross conduction. On the gate signal path from DSP to IGBT transistor there are several contributors of delays. Delays caused by buffers, galvanic isolation, the gate driver and the major part, physical turn on/off time of the transistor. The transistor switching characteristics is nonlinear and temperature dependent. The turn on and turn off times are different depending on the manufacturer. If the converter would be switching without added dead time, the above mentioned delay which is different for every transistor in some cases would case overlapping conduction of both transistors.

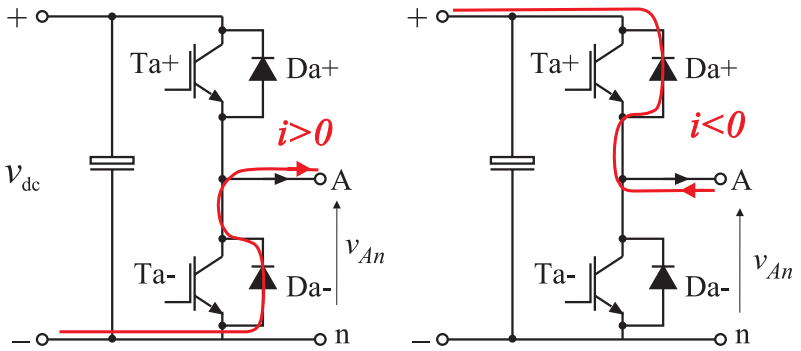

Figure 2.15: Current path during dead time, when both transistors are off

Transistors should not conduct in one leg even for a short time, because most likely they will get destroyed by high short circuit current from the dc-bus. If the dead time is too short and transistors cross conduct occasionally very shortly, they can survive however but it will cause great EMI problems. When the proper dead time is added, the transistor delay becomes insignificant leaving great safety margin.

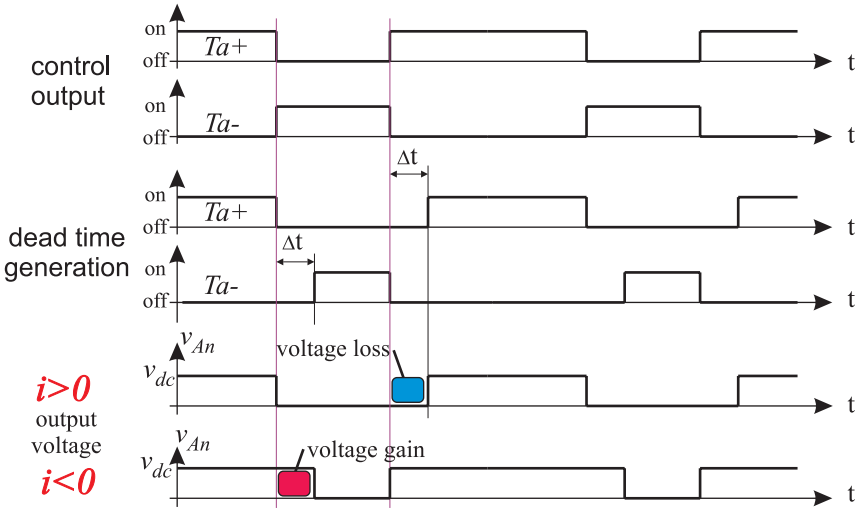

Figure 2.16: Dead time delay insertion during PWM operation

When the dead time is known, and the system unknown delay is influencing in small portion the dead time correction algorithms can be more precise. As can be seen in Figure 2.15 and Figure 2.16 the converter terminal output voltage during dead time depends only on the current direction. The terminal voltage during two cycle of PWM period is shown in Figure 2.16 The current direction causes voltage to be added (voltage gain) or subtracted (voltage loss) from the ideal operation.

Based on the above figures a formula for correcting the effects of dead time can be described as follows:

$$i_A > 0: \qquad \Delta v_{An} = \frac{\Delta t}{T_{sw}} v_{dc} \tag{2.77}$$

$$i_A < 0: \qquad \Delta v_{An} = -\frac{\Delta t}{T_{sw}} v_{dc} \tag{2.78}$$

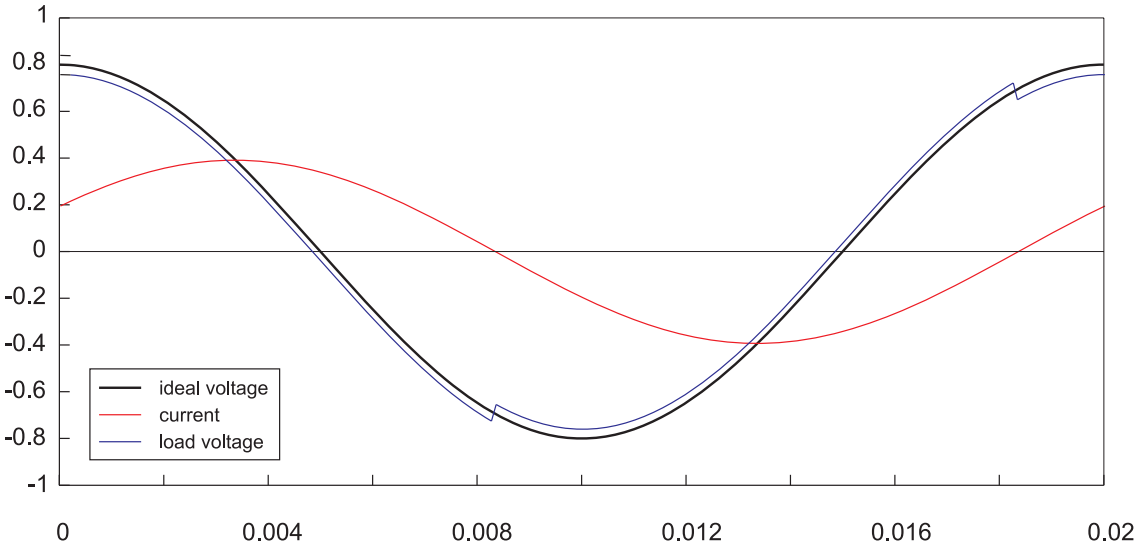

Figure 2.17: Effect of dead time on sinusoidal output voltage

The characteristic small disturbance ("teeth") in the load voltage shown in Figure 2.17 depends on the instant when the current is crossing zero. If the load would be pure resistive the "teeth" would occur at the zero crossing as well. Similar distortion occurs in the line to line voltage, resulting in harmonic distortion. Since the effect of dead time is instantaneous, a precise current measurement is needed in order to compensate for it.

2.6.1. Dead time effects correction algorithm

In this work the dead time effects correction is important for the purpose of virtual flux estimation. The estimation is as good as the description of the model is. In addition to the dead time the IGBT transistor has a nonlinear forward voltage drop. The forward drop as a function of current with different temperatures is presented in Figure 2.18. As we can see the characteristic is non linear, and can be approximated by two parts. The first would be the $\pm 1\ V$ constant drop depending on the current direction (IGBT or diode) and the second part dependent on the current magnitude, modeled as a resistor. Since the forward voltage drop of the diode is similar to the IGBT forward drop they will be modeled as equal. The correction voltage term dependent on the current and results in:

$$v_{crr} = \left(v_{FA} + \frac{\Delta T}{T_{sw}} v_{dc} \right) sign(i) + v_{FB} \tag{2.79}$$

Where v_{FA} represents the constant voltage drop and v_{FB} represents the voltage dependent on the current. $v_{FB} = R_{TD} i$ The series internal resistance of IGBT or diode can be also added to other resistances, e.g the filter series resistance.

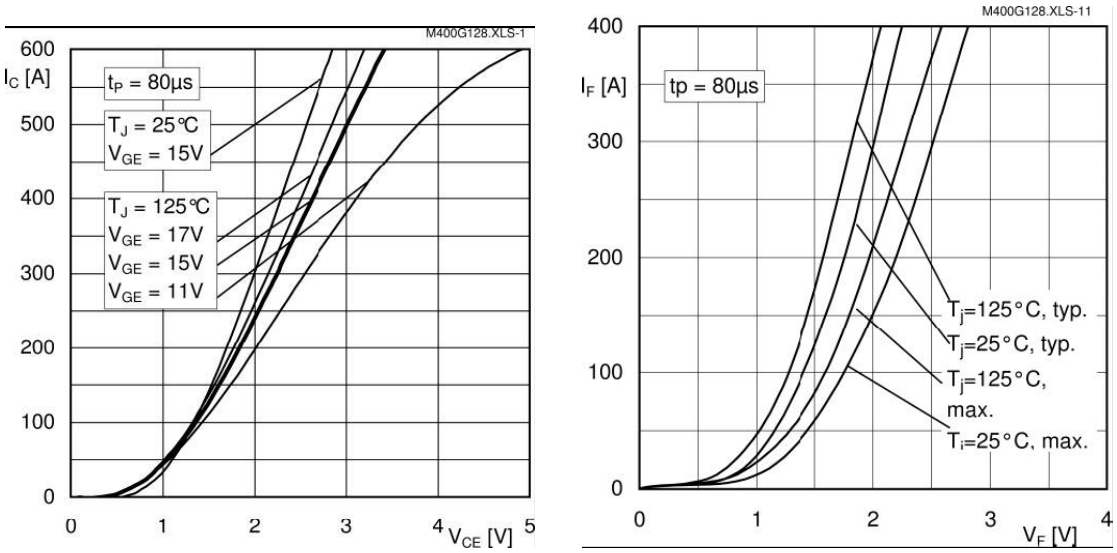

Figure 2.18: Forward voltage drop of the used IGBT module SKB400GB128D
a) IGBT b) diode

2.7. Synchronous sampling

In digital current control systems it is important to synchronize the sensitive measurement with the inverter switching. When the transistors switch on and off they produce high dv/dt which could "pollute" the current measurement. In order to avoid the electromagnetic interference (EMI) the measurement should be taken between switching. Figure 2.19 shows the waveform when the switching is occurring and the point where measurement is taken.

There are also second benefit. When converter is switching it produces current ripples in the load. Measuring in those points marked in Figure 2.19 as T_0 or $T_{sw}/2$ approximate the current ripple by a *mean* value. The resulted measurement of *mean current* often is a noise free, that the low-pass pre-filtering in unnecessary.

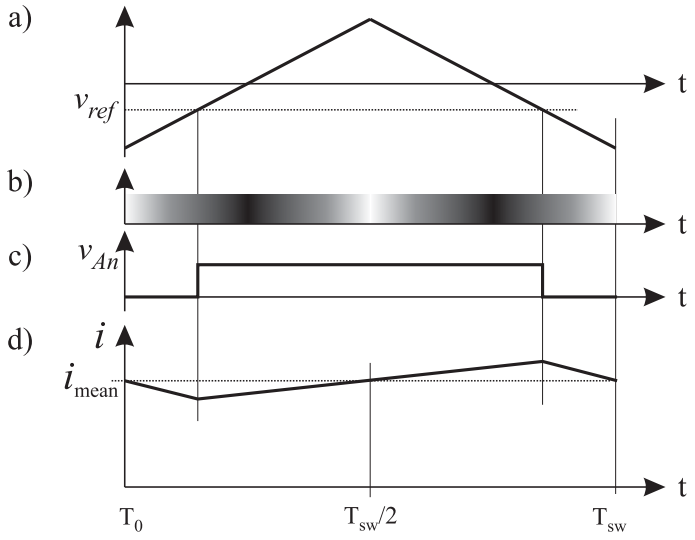

Figure 2.19: Synchronous sampling principle

The Figure 2.19b shows the switching density for the H bridge converter. The assumed switching is always symmetrical around the $T_{sw}/2$ point. The black area represents switching when the output voltage is small or zero (duty cycle around 50 %). The whiter area represent when the converter output voltage is high or close to saturation. In order to assure no switching during measurement it is important to keep voltage references away from inverter saturation boundary. A good practice would be to limit the duty ratio slightly (e.g. to 99.5 %) to ensure that no switching is performed during measurement, this will not have any significant influence from control point of view.
The current sampling in Figure 2.19d during one switching period can occur at the point T_0 or $T_{sw}/2$. This means that the sampling frequency of the control system preferably can be selected as twice frequency of the switching frequency, which can be represented in Figure 2.20b.

$$f_s = 2 f_{sw} \tag{2.80}$$

However if we want update the PWM registers twice per switching period, this violate the assumption that the switching should be symmetrical. Not fulfilling these criteria causes more harmonics in output voltage.
Faster sampling enables higher bandwidth of the current or voltage control loop. In some control cases where especially higher harmonics control is involved it would be beneficial to have sampling frequency twice than switching frequency. The only limitation is the computational power. Since the DSP must execute control algorithms twice fast this is reasonable solution for high performance control on the state of the art DSP. The comparison of two sampling frequencies with principle of updating the PWM comparators is shown in Figure 2.20. The system delay related to updating of the PWM registers is also shortened improving the performance.

When the system does not require high bandwidth control and only main harmonic is controlled the sample rate can be reduced to switching frequency.

$$f_s = f_{sw} \tag{2.81}$$

which is visible in Figure 2.20a.

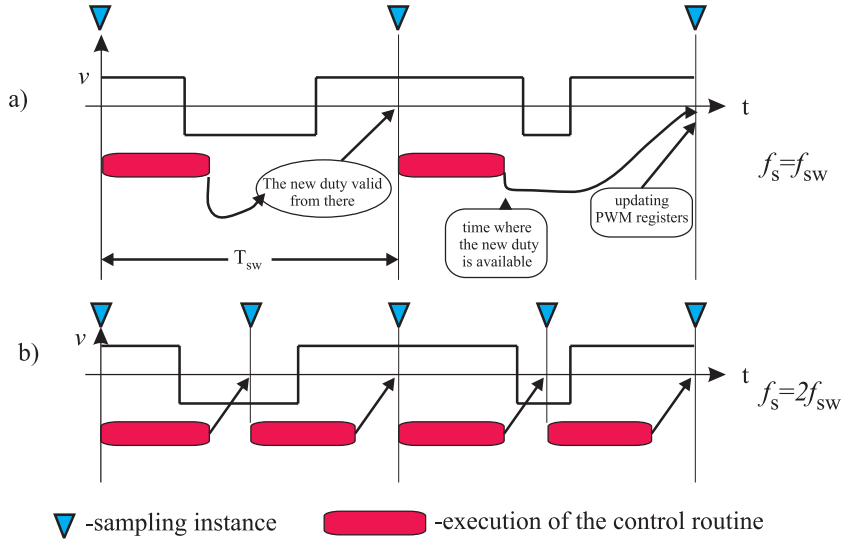

Figure 2.20: Comparison of two sampling frequencies and time restrictions

Asdasdasdasdasd

2.8. Voltage oriented control

The voltage oriented control (VOC) is a strategy developed for use with grid connected converters. It was the first topology enabling grid synchronization based on an earlier developed AC motor theory. It uses the same transformations and synchronous frame current regulators. The topology is depicted in Figure 2.21

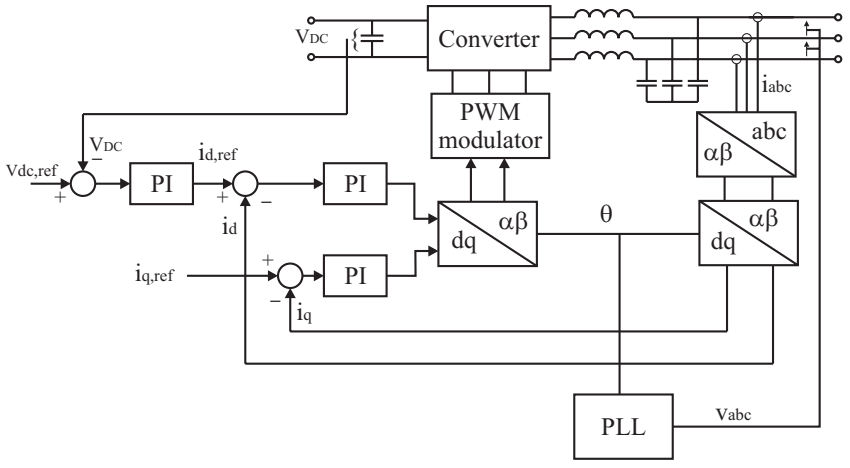

Figure 2.21: Voltage oriented control basic scheme

Both the voltage and current are sensed and transformed to synchronous frame. The synchronous frame is oriented with angle of the measured voltage. First the transformations are performed according to (2.8) and (2.16) to achieve dc quantities. The *d*-axis current regulator is responsible for active power, and *q*-axis regulator for reactive. The *d*-axis reference is usually commanded from the dc-link voltage controller. The dc-link voltage controller is an outer control loop maintaining the appropriate dc

voltage independent of the load characteristic. This system requires only three PI regulators in order to operate under synchronization with the grid and appropriate current control. The *q*-axis reference can be set to zero to achieve unity power factor, or can be controlled by external loop compensating the reactive power. This control topology is able to supply or sink the adjustable dc-voltage, so it can be seen as injecting power to the grid or act as an active rectifier. The reactive power can be adjusted from full capacitive to full inductive character in a fluent way. All previously presented modulation techniques can be used.
The synchronization to the grid is usually performed with some sort of PLL watching the instantaneous grid angle and amplitude. The operation without a PLL is also possible but the stability under grid disturbance cannot be guaranteed. The PLL ensures more reliable results and smoother angle, which is not influenced from grid harmonics, phase jumps or voltage dips.

The PI regulator design is well described in literature. A commonly used criterion allows specifying the settling time or maximum overshoot. An optimum controller design based on symmetry criterion or modulus criterion can be found in [kaz1], [uml1].

2.9. Chapter summary

This Chapter introduces the basics knowledge and classical approach in converter modeling. It introduces different sinusoidal modulation schemes, space vector modulation and explains the influence of zero sequence signals. It shows in details the model of converter with L filter in synchronous frame. The nonlinear effect of dead-time, its influence and correction are presented.

3. SYMMETRIC COMPONENT DECOMPOSITION

In this chapter an implementation of a new method for decomposition into positive and negative sequence is shown. The implementation is verified in a simulation program and used in a laboratory experiment, the results are discussed. The proposed method is based on modified delayed signal cancellation theory. Symmetric decomposition is the basic element when dealing with unsymmetrical systems. It can be used to decompose different signals like currents, voltages or fluxes.

3.1. Introduction

Positive and negative sequence decomposition is used in systems where unbalanced conditions occur. Unbalanced signal consist of two space vectors rotating in opposite direction.

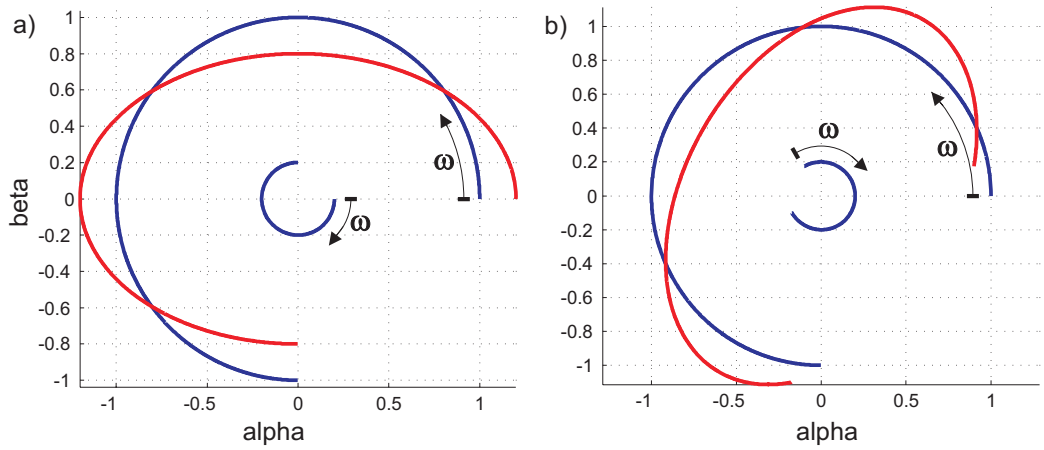

Figure 3.1: Components of the unbalanced space vector.

In the Figure 3.1 the unbalanced signal consists of positive sequence signal (PSS), marked with blue color with unity radius, and a negative sequence signal (NSS), marked blue with amplitude of 0.2. Red is the resulting unbalanced space vector. In order to notice the reference angle of each space vector (angle at t_0), the drawing is made only for the first 270 degrees. In Figure 3.1a the PSS and NSS reference angle is 0, in Figure 3.1b the reference angle of PSS is 0 and NSS is +120 degrees. In general for currents and voltages the unbalanced space vector can be decomposed as:

$$v_\alpha = v_\alpha^p + v_\alpha^n \qquad v_\beta = v_\beta^p + v_\beta^n \qquad i_\alpha = i_\alpha^p + i_\alpha^n \qquad i_\beta = i_\beta^p + i_\beta^n \tag{3.1}$$

The trajectory of the sum voltage vectors is an ellipse and may be represented as:

$$\underline{v} = v_{PS} e^{j\omega t} + v_{NS} e^{-j(\omega t + \phi_{NS})} \tag{3.2}$$

In this chapter the superscript *p* and *n* will denote positive and negative sequence.

3.1.1. Symmetric decomposition in three-phase systems

However we are interested in space vector decomposition, the theory from three-phase system decomposition can be analogously reused to derive the decomposition for two phase systems. There is no need to decompose three-phase systems, a better choice is to first use Clark transformation and then decompose. If the system is three-wire system without the neutral connection the zero-sequence component can be neglected.

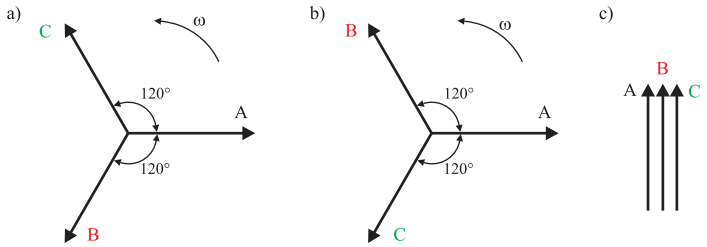

Figure 3.2: Symmetric components: a) positive sequence ABC, b) negative sequence ACB, c) zero-sequence.

Let's assume that the unsymmetrical voltages to be decomposed are v_a. v_b, v_c.
Assume phase *a* as reference for the resulting symmetrical components v^p and v^n .
The equation can be written as:

$$\begin{bmatrix} v_a^p \\ v_a^n \\ v_0 \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & a & a^2 \\ 1 & a^2 & a \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{3.3}$$

where $a=e^{j120}$ is advancing phase by 120°. For phase *b* and *c* the decomposition is as follows:

$$\begin{bmatrix} v_b^p \\ v_b^n \\ v_0 \end{bmatrix} = \frac{1}{3} \begin{bmatrix} a^2 & 1 & a \\ a & 1 & a^2 \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{3.4}$$

$$\begin{bmatrix} v_c^p \\ v_c^n \\ v_0 \end{bmatrix} = \frac{1}{3} \begin{bmatrix} a & a^2 & 1 \\ a^2 & a & 1 \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{3.5}$$

Alternatively the phases *b* and *c* can be easily reconstructed from phase *a*, using the same amplitude and shifting by 120° since they are symmetrical.

The same decomposition can be analogously carried for a two phase system or space vector. Instead of 120° phase advancing the 90° can be used (*j* operator). Two phase graphical decomposition is shown in Figure 3.3.

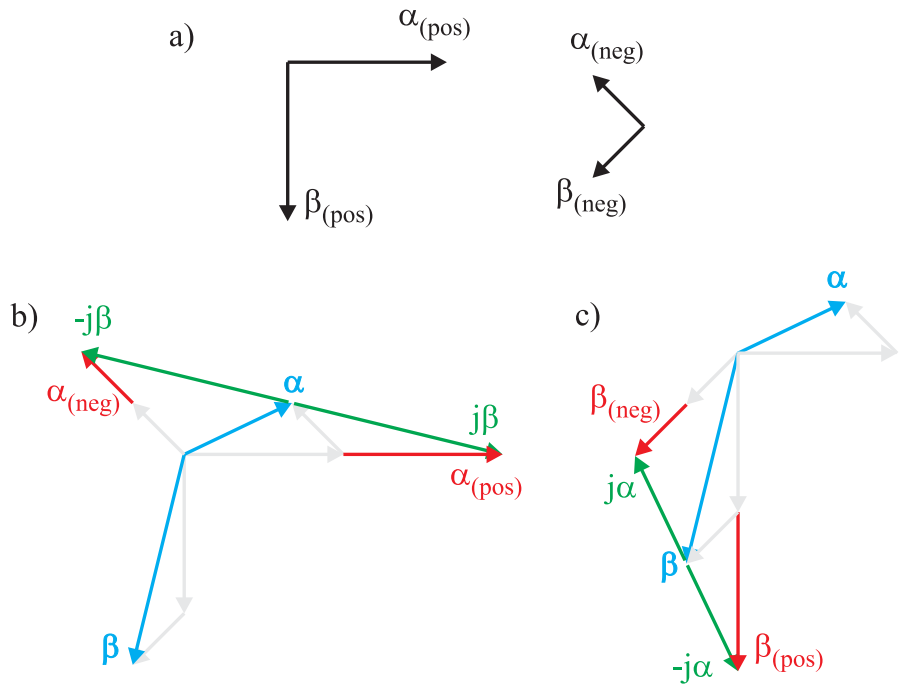

Figure 3.3 Graphical symmetric components decomposition of two-phase system. Space vector decomposition.

In Figure 3.3a there are two opposite direction rotating orthogonal components, which sum is used as unbalanced input. Figure 3.3 b) and c) shows respectively the alpha and beta symmetric component decomposition for PSS and NSS. The resulting red vectors in b) and c) fit with angle and amplitude into the black one in a). The blue vectors are the unbalanced components.

There can be many sources causing unbalance condition, e.g. unbalanced grid voltage, unbalanced currents, unsymmetrical load impedance. For three-phase converter the decomposition is usually performed using complex vectors, which simplifies analysis and implementation.

3.1.2. Symmetric component decomposition for space vector

The equations for two-phase symmetric components decompositions are:

$$\begin{bmatrix} v_\alpha^p \\ v_\alpha^n \end{bmatrix} = \frac{1}{2}\begin{bmatrix} 1 & j \\ 1 & j^{-1} \end{bmatrix}\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} \tag{3.6}$$

$$\begin{bmatrix} v_\beta^p \\ v_\beta^n \end{bmatrix} = \frac{1}{2}\begin{bmatrix} j^{-1} & 1 \\ j & 1 \end{bmatrix}\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} \tag{3.7}$$

Assuming that the unbalanced input vector can be written in the time domain as:

$$\begin{aligned} v_\alpha(t) &= V_\alpha \cos(\omega t) \\ v_\beta(t) &= V_\beta \sin(\omega t - \phi_\beta) \end{aligned} \tag{3.8}$$

Knowing the input signal frequency ω and the period T_0 the phase shift *-j* operator can be defined as $T_0/4$ delay in time domain. The equation decomposed into α and β components for positive and negative sequence can be written as:

$$\begin{aligned} v_\alpha^p(t) &= \frac{1}{2}\left(v_\alpha(t) - v_\beta(t - \tfrac{T_0}{4})\right) \\ v_\beta^p(t) &= \frac{1}{2}\left(v_\beta(t) + v_\alpha(t - \tfrac{T_0}{4})\right) \end{aligned} \tag{3.9}$$

$$\begin{aligned} v_\alpha^n(t) &= \frac{1}{2}\left(v_\alpha(t) + v_\beta(t - \tfrac{T_0}{4})\right) \\ v_\beta^n(t) &= \frac{1}{2}\left(v_\beta(t) - v_\alpha(t - \tfrac{T_0}{4})\right) \end{aligned} \tag{3.10}$$

Equivalently in the complex vector form the equations (3.9) and (3.10) can be written as:

$$\begin{aligned} \underline{v}^{p,\alpha\beta}(t) &= \frac{1}{2}\left(\underline{v}^{\alpha\beta}(t) + j\underline{v}^{\alpha\beta}(t - \frac{T_0}{4})\right) \\ \underline{v}^{n,\alpha\beta}(t) &= \frac{1}{2}\left(\underline{v}^{\alpha\beta}(t) - j\underline{v}^{\alpha\beta}(t - \frac{T_0}{4})\right) \end{aligned} \tag{3.11}$$

The additional superscript $\alpha\beta$ denotes the complex vector.

By delaying the voltage vector by one-fourth of the period, a vector composed of the same positive sequence component and a negative sequence component with equal amplitude and opposite sign is obtained. Therefore, if this delayed vector is added to the voltage vector, the negative sequence voltage is removed. In order to realize the decomposition, two blocks are needed which will have phase lag of 90° for a given frequency.

3.2. Discrete delay implementation based on circular buffer

In most practical applications the system is digital-controlled and thus implementation in discrete time domain is needed. This method of decomposing was proposed in [swe2], [bon1]. Rewriting equation from above in discrete time domain results in:

$$\underline{v}^{p,\alpha\beta}(kT_s) = \frac{1}{2}\left(\underline{v}^{\alpha\beta}(kT_s) + j\underline{v}^{\alpha\beta}(T_s k - T_s n_o)\right) \tag{3.12}$$

$$\underline{v}^{n,\alpha\beta}(kT_s) = \frac{1}{2}\left(\underline{v}^{\alpha\beta}(kT_s) - j\underline{v}^{\alpha\beta}(T_s k - T_s n_0)\right) \tag{3.13}$$

Where the T_s is system sampling time ($f_s=1/T_s$), and the discrete delay n_0 corresponds to ¼ of the period delay T_0.

$$n_0 = T_0 /(4 \cdot T_s) \tag{3.14}$$

However, this solution despite of advantages (fast response time) has several drawbacks, in practice it requires to store data in memory. This can be easily implemented for high end DSP laboratory setup but not widely in industry. The delay (t - T/4) in (3.11) assumes exact delay of 25 % of the fundamental period which has some drawbacks in real implementation. The delay in DSP can only attain discrete values, so the same should frequency. Let's assume sampling frequency f_s=10 *kHz* and base signal frequency of f_0=50 *Hz*, then one period is exactly 200 samples, which gives integer number of 50 samples for 90° phase lag. The next possible delay is 49 or 51 samples which correspond to frequency of signal 49.02 *Hz* or 51.02 *Hz*. This leads to conclusion that for best accuracy the division of switching frequency and signal frequency should be an integer number.
Reassuming, the method is simple and fast (5 *ms*), but a small error appears when signal frequency is not matching the discrete delay. The solution can be to use synchronous PWM (switching frequency correlated with signal frequency by integer factor) but most systems do not use it. Further extensive investigation on error in this method can be read in [bon1], [sve2]

3.3. Proposed implementation based on adaptive filter

The author's motivation is to achieve as little error as possible during phase shifting for practical spectrum of input frequencies. In this case the lowest detectable level of negative sequence will depend on the precision of phase shift. In normal grid condition operation the voltage unbalance is below 2 %, which angle is difficult to derive due to large amplitude of positive rotating component.
The idea is to replace the 5 *ms* discrete delay by an adaptive transfer function. By exploiting the fact that signals of interest have narrow frequency band 45..55 *Hz* a transfer function based on cascaded low pass filters is proposed (3.15). This cascade easily achieves 90 degree phase lag without significant amplitude attenuation for the frequency of interest. This low pass filter cascade can be easily decomposed to two low pass, 1st order filters for efficient DSP implementation.

$$H_1(s) = \left(\frac{\omega_0}{s+\omega_0} \right) \left(\frac{\omega_0}{s+\omega_0} \right) = \frac{\omega_0^2}{\left(s+\omega_0\right)^2} \tag{3.15}$$

For the frequency ω_0 in equation above the attenuation in only -6 *dB*. For the ω_0 frequency the 90° phase lag and 0.5 amplitude attenuation is obtained. The Bode plot is shown below in Figure 3.4.

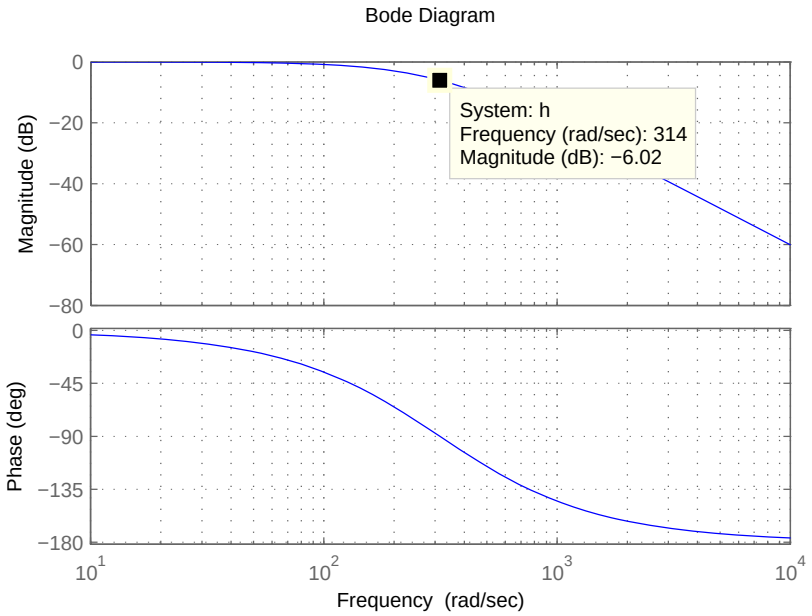

Figure 3.4: Bode plot of the cascaded low pass filter

3.3.1. Discretization

The discretization plays an important role in the accuracy of the phase shift and minimum level of negative sequence detection. The cascade is implemented as two low pass filters. This gives better placement of pole location due to lower order transfer function and the coefficient round-off effect is minimized. This is important as the implementation will take place on fixed point DSP with 32 bit wide data.

There are three commonly known integrator discretization methods: backward Euler, forward Euler and Trapezoidal. The best accuracy result can be achieved if the system delay is taken account. By proper selection of discretization method, the one (or few) sample delay caused by sampling can be cancelled by phase advancing. In other words the different discretization methods allow adjusting the phase response of the controller. Usually there is one sample delay (phase lag) between measurement and new switching vector, and it would advisable if the phase lag can be compensated by the control routine. It is important to keep the proper amplitude and phase responses, as it has influence on detection of small signals. Keeping the distortion of the controller as small as possible enable proper detection of small signals (in amplitude) and thus they are not distorted by controller itself. For large amplitude of NSS this doesn't have much influence, but if the small amplitude of NSS has to be detected, the sensivity is crucial.

Let's first discretize with the simplest forward Euler:

$$H_1(s) = \frac{\omega_0}{s+\omega_0} \Rightarrow H_1(z) = H_1(s)\Big|_{\frac{1}{s}=\frac{T_S}{z-1}} \tag{3.16}$$

$$H_1(z) = \frac{\omega_0 T_S z^{-1}}{1 - z^{-1}\left(1 - T_S \omega_0\right)} \tag{3.17}$$

The complete second order filter can be written in discrete form as:

$$\begin{aligned} m_n &= \omega_0 T_S \left(x_{n-1} - m_{n-1}\right) + m_{n-1} \\ y_n &= \omega_0 T_S \left(2m_{n-1} - y_{n-1}\right) + y_{n-1} \end{aligned} \tag{3.18}$$

Where *x* denote input, *y* output and *m* intermediate discrete samples.
In order to test, the filter is implemented in computer simulation program. The input signal consists of 1.0 *p.u.* of (PSS) and 0.05 *p.u.* of (NSS), the angle is derived. The results are shown in Figure 3.6a.

For comparison another discretisation is chosen, backward for one filter and forward for second. The bilinear transformation for backward discretisation is shown below.

$$H_2(s) = \frac{\omega_0}{s + \omega_0} \Rightarrow H_2(z) = H_2(s)\Big|_{\frac{1}{s} = \frac{zT_S}{z-1}} \tag{3.19}$$

$$H_2(z) = \frac{\dfrac{\omega_0 T_S}{1 + \omega_0 T_S}}{1 - z^{-1}\left(\dfrac{1}{1 + T_S \omega_0}\right)} \tag{3.20}$$

The complete second order filter discretized with backward and forward can be written in discrete form as:

$$\begin{aligned} y_n &= \frac{1}{1 + \omega_0 T_S}\left(y_{n-1} + m_n \omega_0 T_S\right) \\ m_n &= \omega_0 T_S \left(x_{n-1} - m_{n-1}\right) + m_{n-1} \end{aligned} \tag{3.21}$$

The equations (3.18) and (3.21) are implemented *C* language. The comparison of their performance is shown in Figure 3.6.

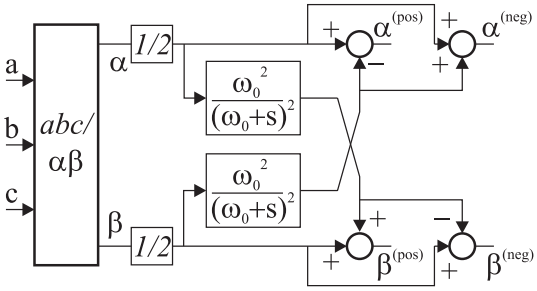

Figure 3.5: The complete positive and negative decomposition block

3.3.2. Simulation results of space vector decomposition

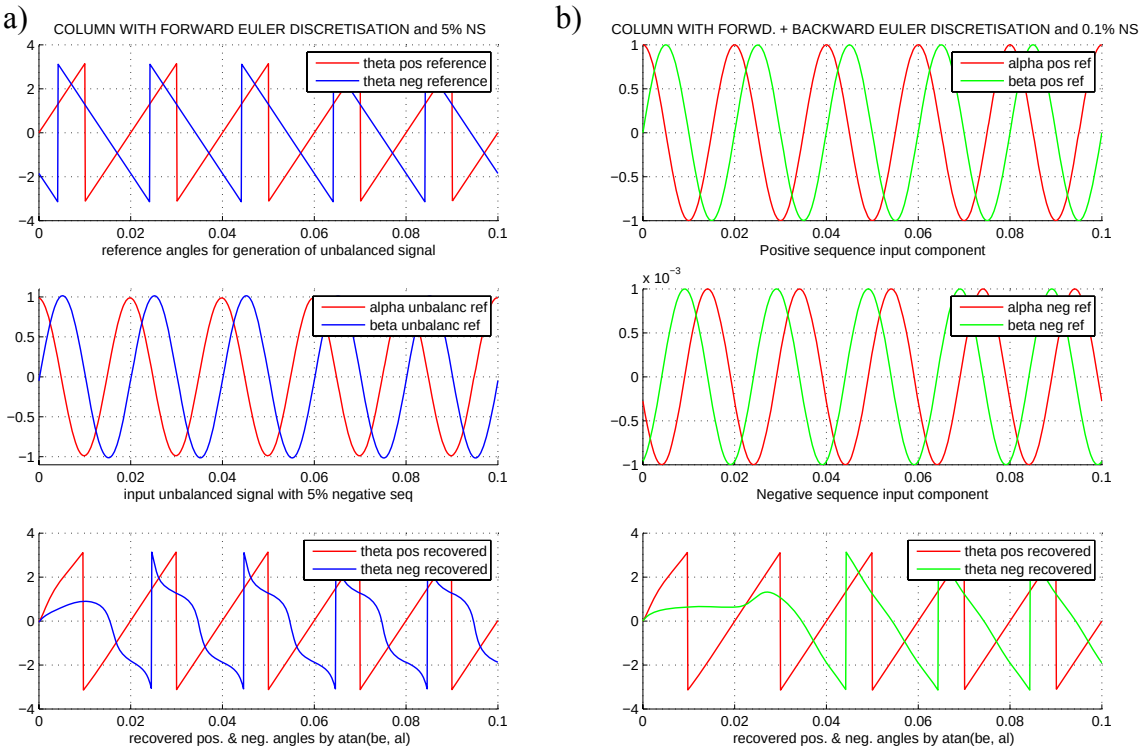

Figure 3.6: Discretisation influence on quality of negative sequence angle detection.
a) column – Negative sequence of 5% and not appriopriate discretisation
b) column – appriopriate discretisation and possible detection level of 0.1% NSS

In Figure 3.6 it is shown how important the discretization selection is for a given system. The resulting angle of the vector for PSS and NSS is visible in the bottom line in Figure 3.6. In Figure 3.6b satisfactory results are achieved even if the negative sequence is as small as 0.1 %. In Figure 3.6a the NSS is 5 % and even with such a large signal angle of NSS is distorted. The sampling frequency is 10 *kHz* and the data width is 32-bits.

For wide frequency input range systems, like e.g. in motor drive this filter can become adaptive. The signal frequency ω_0 in (3.21) must be submitted every call, thus involving few more multiplications. Usually the system frequency can be obtained from PLL, virtual flux model or other source.
For a system where narrow frequency variations are expected, like in grid connected inverters, other solution can be used, not adaptive but based on correction. The nice feature of that filter is that the phase of the filter around the ω_0 frequency is relatively linear. This would allow adding an angle correction term, depending on the frequency. The frequency ω_0 could be calculated once, thus minimizing the execution time of filter. The same would have to be done with amplitude correction. A test performance with frequency and amplitude correction for different frequencies and different level of NSS is shown in Figure 3.7.

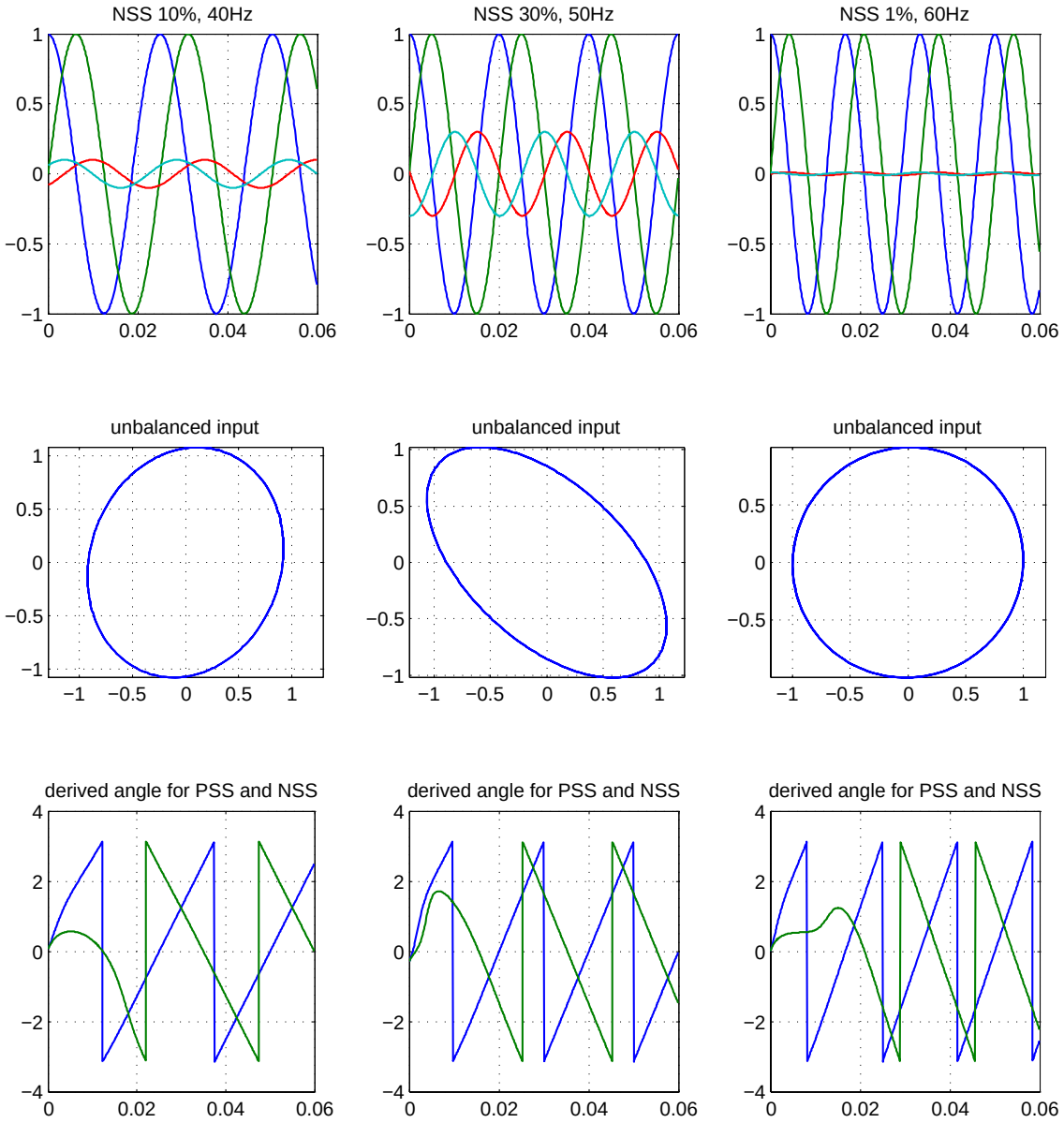

Figure 3.7: Performance under different frequencies and level of NSS. Used discretization method in (3.21)

3.4. Chapter summary

This chapter presents a novel implementation for symmetric component decomposition method. The method is based on well known two phase decomposition commonly recognized as delayed signal cancellation (DSC) method. The motivation of the author was to achieve simple algorithm with very low computational requirements and very high sensitivity for negative sequence. The method can cope with variable frequency and can detect vary small amplitude of NSS. The importance of having simple and

sensitive decomposition method is that it is used in many places of the control scheme. The converter current and the virtual flux need to be decomposed at least.

4. DUAL VIRTUAL FLUX MODEL

This chapter introduces the dual virtual flux (DVF) model and associated with it sensor-less operation of a grid connected converter. To find the amplitude and angle of the grid a voltage measurement normally is used. This approach is called voltage oriented control (VOC), as the angle of measured voltage orients the transformations. In this chapter we will not use grid voltage sensors; instead we will use other available measurement and the model of the system to calculate those signals. The available measurement sensors are the dc-link voltage and two ac currents. The word sensor-less means that reduced number of sensors is used; it doesn't mean that sensors are not used at all.
There are many benefits using sensor-less control, less components (sensors, cables, space, ADC converter). The quality of an estimated signal can be much better than from sensors which are badly placed in system and noise becomes a problem. The quality of the estimate is as good as the model is. The dead time and the filter inductance are relatively easy to model. It is difficult to model the variation of the parameters as a function of temperature, e.g. nonlinear transistor voltage drop or the saturation of the grid inductors.

For systems which are critical a high quality voltage sensor can be used. It doesn't cost much to run measurement in parallel with the virtual flux model in DSP. In case the physical sensor fails the flux model can take over and the operation can continue. That means that reliability to the system can be added with almost no cost.

A very important feature of the proposed DVF estimator is that it returns two independent orientation angles, for positive and negative sequence. The possibility of having two reference angles is that we can use this information for independently controlling the positive and negative sequence current, sensor-less! In this case we have 4 current reference signal to feed in, the positive and negative sequence for direct and quadrature reference current.
This enables many new possibilities, e.g. we can control that the current is always balanced (no negative seq.) in any unbalanced grid condition. In an unbalanced grid condition we can also make that the power drawn by converter is constant. This enable to minimize the dc-capacitor, since the converter ripple in dc-link can be controlled.
Finally we can use it as STATCOM in unbalanced condition, recovering the unbalanced voltage to symmetry by injecting properly pulsating power.

4.1. Introduction to virtual flux.

Many publications has been presented in this topic, starting from 1996 by Bhattacharya [bha1] and consequently improved by [cha1], [cha3], [mal1], [mal4], [gul1]. The idea is to estimate the output voltage of the inverter from the measured dc-link voltage and the duty ratio of switches. The modulator reference signals S_a, S_b, S_c are related to real duty ratio in a linear way, but the dead time and other system nonlinearities must be take into account. The dead time can in many cases be controlled by the DSP. Most inverters have built in hardwire dead time. The realistic dead time must be known for voltage correction. Integration of multiplied dc-link voltage with the duty ratio gives the inverter virtual flux. For more practical reasons the modulator reference voltage, dead time correction and dc-link voltage is used as an estimated inverter voltage vector which is later integrated to achieve inverter virtual flux. Current in the converter filter produces filter flux. Filter flux vector added to inverter flux vector leads to virtual flux vector of the grid. Usually the filter flux vector is very small (few %) and do not contribute significantly the grid flux (the inverter flux is major). The single-phase equivalent model for reference is shown in Figure 4.1.

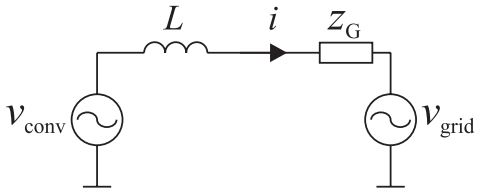

Figure 4.1: Reference model used for virtual flux, L filter used

The virtual flux of the grid in the space vector form can be written as:

$$\underline{\Psi}_g = \int \left(\underline{v}_{conv} - L\frac{d\underline{i}}{dt} \right) dt = \underline{\Psi}_{conv} - L\underline{i} \tag{4.1}$$

Separation into the alpha and beta variables helps in further implementation. The estimated average inverter voltage based on PWM duty ratio and dc-link voltage is:

$$v_{conv,\alpha} = V_{dc}\frac{2}{3}\left(S_a - \frac{1}{2}(S_b + S_c) \right) \tag{4.2}$$

$$v_{conv,\beta} = V_{dc}\frac{1}{\sqrt{3}}\left(S_b - S_c \right) \tag{4.3}$$

The S_a, S_b, S_c are the modulator signals including all model corrections.
The converter flux components are calculated from:

$$\begin{bmatrix} \Psi_{conv,\alpha} \\ \Psi_{conv,\beta} \end{bmatrix} = \begin{bmatrix} \int v_{conv,\alpha} dt \\ \int v_{conv,\beta} dt \end{bmatrix} = \underline{\Psi}_{conv} \tag{4.4}$$

As it is an integral relationship, the virtual flux converter vector is 90° lagging from the inverter voltage vector. The grid flux components are calculated from:

$$\begin{bmatrix} \Psi_{g,\alpha} \\ \Psi_{g,\beta} \end{bmatrix} = \begin{bmatrix} \Psi_{conv,\alpha} \\ \Psi_{conv,\beta} \end{bmatrix} - \begin{bmatrix} Li_{\alpha} \\ Li_{\beta} \end{bmatrix} \tag{4.5}$$

Based on $\Psi_{g,\alpha}$, and $\Psi_{g,\beta}$, finally the grid voltage vector position is:

$$\varphi_g = \arctan\left(\Psi_{g,\beta} / \Psi_{g,\alpha}\right) + \frac{\pi}{2} \tag{4.6}$$

In practice a pure integrator used to estimate VF cannot be used, it will bring some undesirable effects due the dc offset presented in the signal. This dc offset, no matter how small it is, it will bring the integrator to saturation or overflow. This effect of perfect integrator drifting is shown in Figure 4.2.

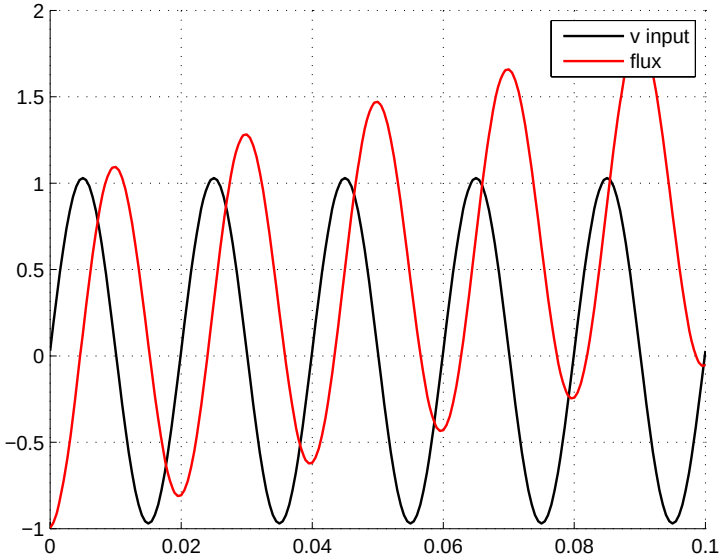

Figure 4.2: Effect of integrator drifting due to 2% offset in the beta component of input signal. The initial integrator state is set to the value of -1.

Since the integration must be performed for two orthogonal components (alpha and beta) the initial condition should be set -1 and 0, to center the derived flux. The ideal integrator flux vector drifting is shown in Figure 4.3.

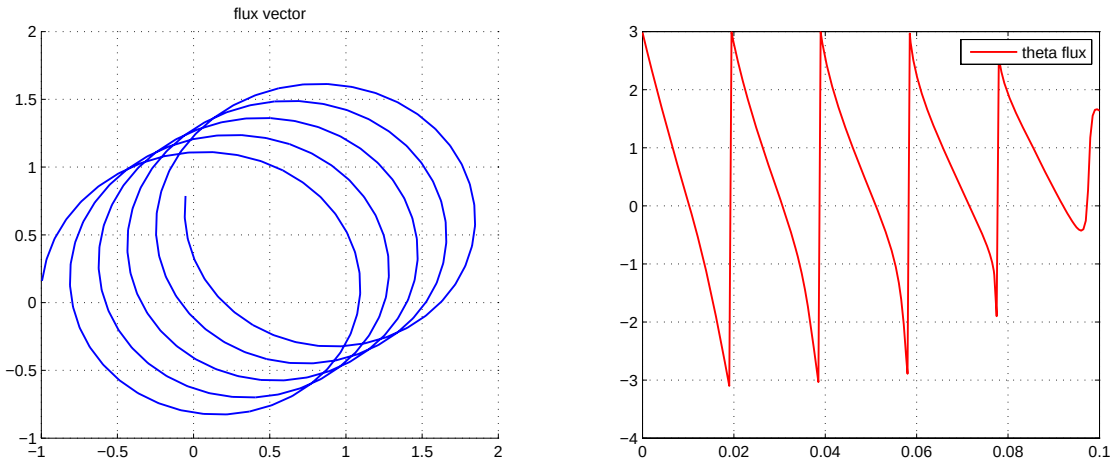

Figure 4.3: Ideal integration and drifting of the vector origin (left) and derived angle of vector in time domain (right)

It is clearly visible in Figure 4.3 as the flux vector drifts; the derived angle is gaining error and thus cannot be used any longer.

A common solution to replace the ideal integrator is to use a first order low pass filter with bandwidth set much lower than grid frequency [mal5]. It is common to set the bandwidth of LPF to 10 % of the signal frequency. In this frequency region the phase lag is approaching 90° giving similar result to integration. The standard flux model estimator is shown in Figure 4.4.

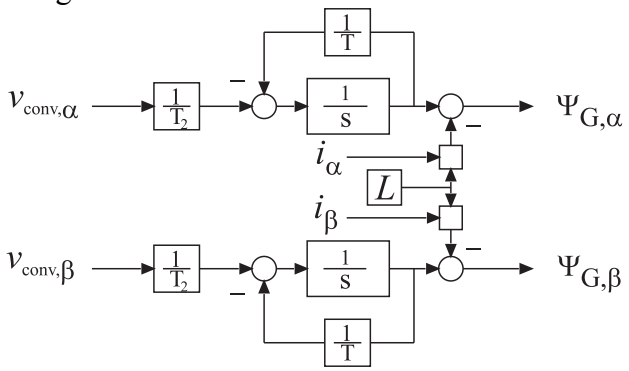

Figure 4.4: Block scheme of the standard virtual flux estimator based on low pass filter

The solution in Figure 4.4 will not cause dangerous infinite integration of the dc offset, instead the dc offset may appear at the output at steady state. The common first order low pass filter solution reduces performance of the system significantly because of amplitude and phase error. For the bandwidth of the low pass filter set to $\omega_{LP}=0.1\ \omega_{50}$, the phase lag is exactly 84.2 degrees. Since the bandwidth must be limited to achieve a proper phase shift, large amplitude attenuation occurs (-20 *dB*). This gives long time response in time domain, and errors in dc component, since dc region is significantly magnified, compared to the frequency of interest (50 *Hz*).

4.2. Proposed virtual flux model

The author's intention was to introduce a transfer function that gives a much faster time response, precise phase shift and little amplitude attenuation. Cascading two low pass filters, with a cut off frequency identical to frequency of interest will produce exactly 90 degree phase shift and only 50 % of the original amplitude (-6 *dB* attenuation).
The proposed second order transfer function is the same as in the earlier case of symmetrical component decomposition in Chapter 3.3. Discretization can be handled in the same manner as for symmetric component decomposition. The complete block scheme of virtual flux estimator is presented in Figure 4.5. The presented transfer function input-output amplitude relation is intended for direct implementation in the system where *per unit* scaling is used (Appendix B).

$$H_1(s) = \frac{\omega_0^2}{(s+\omega_0)^2} \tag{4.7}$$

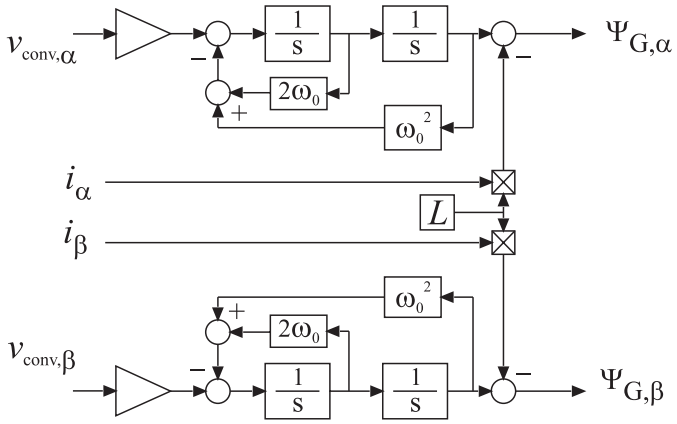

Figure 4.5: Block scheme of the proposed flux estimator

The comparison in time response between standard low pass filter with bandwidth of ω_{LP}=0.1 ω_{50} and proposed filter is shown below in Figure 4.6.

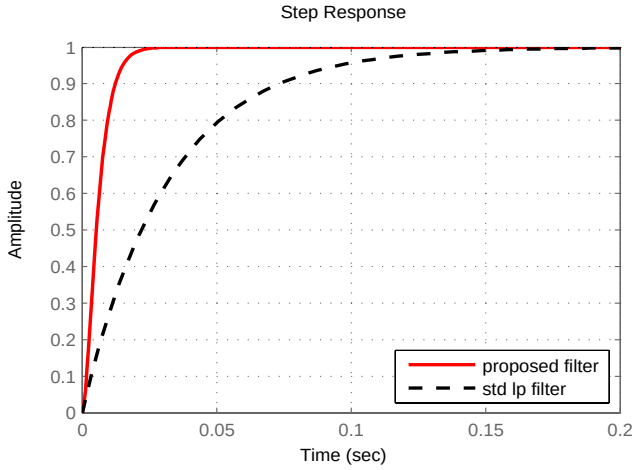

Figure 4.6: Step response of proposed filter (solid line) and standard low pass filter (dotted line)

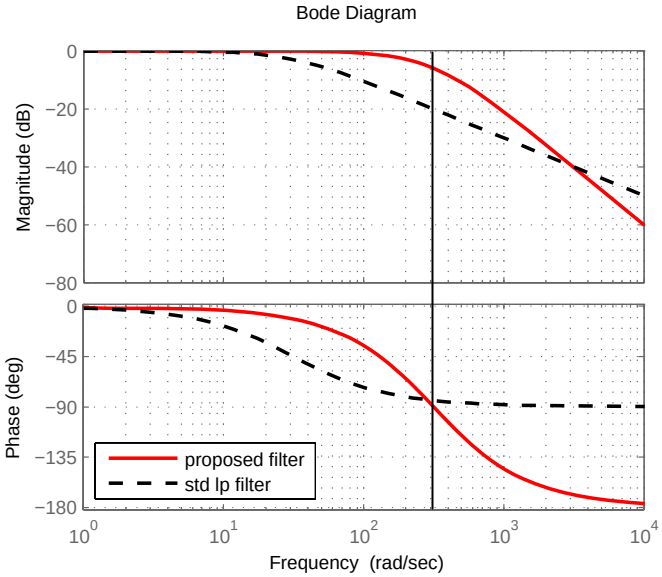

Figure 4.7: Bode plots of the proposed filter (solid line) and standard low pass filter (dotted line) with bandwidth set to 0.1 of signal frequency. The vertical line placed at frequency of 50 Hz, shows the amplitude attenuation and phase difference of both filters

The advantage is also that the phase around 50 *Hz* is changing relatively linear with symmetry. This could be use for phase correction in the case of frequency variations around 50 *Hz* as it is mentioned in Chapter 3.3.2.

4.2.1. Drift compensation

The author's motivation to achieve offset free virtual flux components is the calculation of flux angles. Accurate flux angle is especially important for the negative sequence. As the amplitude of negative sequence flux during normal grid operation is very small, any small dc error will produce relatively high offset compared to flux amplitude. Due to this reason any attempt to calculate negative sequence angle θ=arctan(Ψ_β/Ψ_α) is erroneous.

The offset can be introduced by:

- measurement sensors and its nonlinearity, noise.
- low resolution of the AD converter (10-12 bits)
- sensors and analog circuitry thermal drift
- math errors for finite resolution of calculations in DSP
- dead time, nonlinearity in the power stage (transistors, diodes)

To prevent drift of the zero during flux integration, several adaptive integration algorithms as well a separate drift correction methods have been introduced in the past [huwu], [har2].
Because the flux estimator introduced above is a low pass filter itself, the prevention of dc offset integration results in one goal already achieved. One goal is to stop integration and another to bring the signal back to zero offset.

In the presented filter there still can be dc offset in output flux in steady state if the input is not centric. In order to remove the output dc offset during steady state, derivation action in transfer function is needed ('s' in numerator). One such proposal by Harnefors [har2] for motor drive uses the band pass filter to remove the offset. The well known amplitude characteristic of derivation will amplify higher frequency, adding unwanted noise.

The other commonly known methods are:

- High pass filter. The offset usually is a constant or slowly varying component. Using the high pass filter removes the offset. The components with significant frequency (our virtual flux frequency) are passed through. Unfortunately the high frequency noise can go through as well.
- Method proposed by Niemla. The method constantly monitors the length of the flux vector (modulus), and if the variation is detected an appropriate correction term is added the output. The correction term is derived from subtraction of low pass filtered modulus from instantaneous modulus. In this way the non-eccentricity is detected. Signal with more unbalance causes the result of subtraction to have more ripples, which are used as correction term with appropriate gain.
- Method proposed by Hu&Wu. Uses as pure integrator and low pass filter.
- Methods with saturable feedback
- Methods with integrator and amplitude limitation

The author has used a method based on low pass filter, and then subtraction of the bias signal from the flux vector signal. This method has a simple implementation and is sufficient for this flux model which is unable to drift to infinity/saturation.

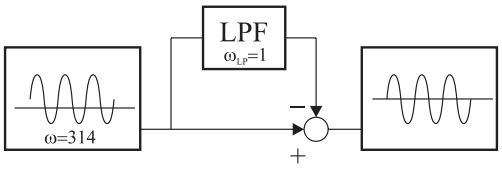

Figure 4.8: Removing an offset from a signal by large time constant LPF

The Figure 4.8 shows the scheme successfully used by the author in laboratory experiment which employs a LPF at the output of flux model. The LPF is set to significantly large time constant (τ>1 s or bandwidth less than 1/1000 of original signal), which corresponds to the fact that the real sensor offset is not changing rapidly.

4.3. Assembly of dual virtual flux model

By cascading the symmetric component decomposition block together with two virtual flux estimators a positive and negative sequence of the flux is achieved. The positive and negative sequence flux rotates much smoother than the real voltage in the grid. The $\varphi_{G,pos}$ and $\varphi_{G,neg}$ are the grid voltage position which orient the Park transformations.

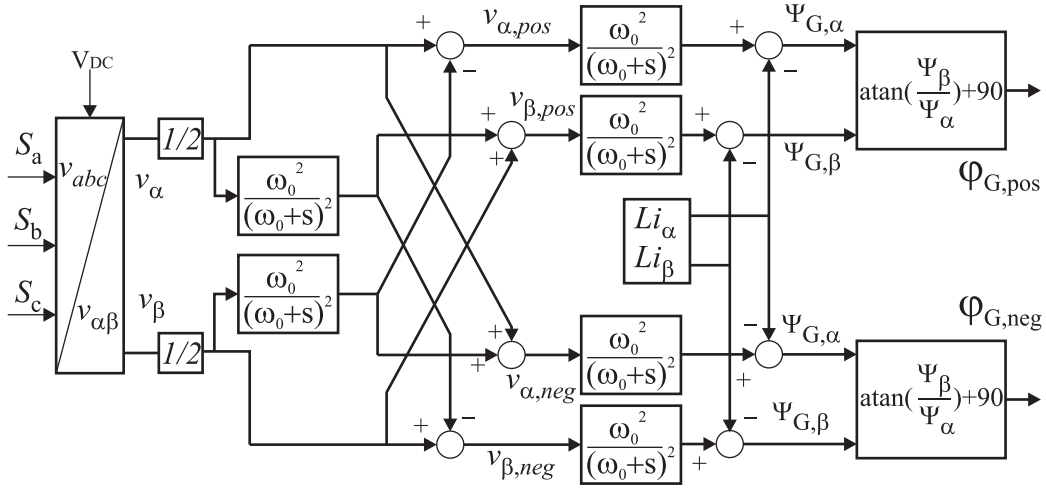

Figure 4.9: Complete dual frame virtual flux model

The drift compensation is not shown here. It is inserted before the atan() function blocks.

4.4. Evaluation of dual frame flux model under unbalanced voltage

The three-phase converter with single frame control is limited to balanced voltage sources. This is however never the case, there is always some imbalance. That imbalance causes current distortion, pulsating power in the dc-link, etc.
The ability of controlling the positive and negative sequence of current for three-phase converters in unbalanced grids is attractive. The main benefits are the possibility of realization constant power flow in unbalanced grids. The constant power flow is understood here as no current ripple occurs in the dc-link capacitor during one period of the grid. Slow rate power variation is allowed. For an unbalanced voltage grid the currents must be unbalanced in such a manner that they would not cause current ripples in the dc-link. In general the ripple in the dc-link can be caused by two sides: one from not supplying the dc-link with constant dc power, and the second that the power supplied by the inverter from the grid is pulsating. Fulfilling those two conditions the dc-link capacitor size can be decreased and the converter life time can be extended significantly. Constant power from "both sides" of the dc-link leads to possibility of eliminating electrolytic capacitor which is often a common point of failure. This large electrolytic capacitor can be replaced with other type of capacitor e.g. long life film capacitor, which is smaller in size and capacitance. A good example of application is the three-phase PV inverter where long life time is required. The power supplied by the photovoltaic module can be seen as "constant" power (or ripple free), the second condition to fulfill is to feed the grid (in any condition) with constant power, and then finally the dc electrolytic capacitor can be eliminated.
Unfortunately there is no such a solution for single-phase grid connected converters and the energy must be stored. Reactive power compensation is another field where some sort of energy storage is required, which for the inverter case is the dc-link capacitor.

The evaluation of double frame flux model will be carried in two steps:

1 Evaluation of supplying balanced currents to the grid with unbalanced voltage. The energy in the dc-link will be fluctuating.
   - To perform it, only a reference for $i_{d,pos}$ or $i_{q,pos}$ current component of positive sequence is given. The negative sequence reference $i_{d,neg}$ and $i_{q,neg}$ and are set zero.

2 Evaluation of supplying constant instantaneous power for unbalanced grid voltage.
   - A specific unbalanced current supplied to the unbalanced grid will cause the power in the dc-link to be constant. All four current references (*d*-, *q*-axis, for positive and negative sequence) must be properly calculated.

There is also another possibility to utilize fully the DVF model. The unbalanced currents can be used to recover unbalanced grid voltage. By supplying proper reactive power to the grid, it's possible to improve the voltage symmetry. This is similar to the low voltage ride through (LVRT) capability but in the less severe way. The principle is also similar to STATCOM but injecting pulsating power instead of constant reactive power.

4.4.1. Experimental results of supplying balanced currents into unbalanced grid

To verify the concept of dual frame virtual (DVF) flux orientation, a laboratory setup was build. Two converters are used with rated power of 20 *kVA* each. The table below shows more details.

rated power	20 *kVA*
filter inductance	750 μH, LC type filter
filter capacitor	25 μF connected in delta
sampling frequency	10 *kHz*
line voltage	230 *V*
DSP	TMS320F2812

Since the control scheme can be changed quickly in software, it is also possible to compare performance of single and dual frame current controller.
The single frame current controller means that there is no sequence separation. The controller is only able to control the positive sequence and thus for unsymmetrical voltage, distorted currents may result. The single frame orientation is depicted in Figure 4.11.
The DVF control is based on standard dual current controller in synchronous frame shown in Figure 4.10 where the frames are oriented by angle based from investigated dual virtual flux model (both positive and negative).

The blocks marked in Figure 4.10 as positive and negative estimated voltage are calculated by equation (3.11), the fluxes are calculated by (4.7) and finally (4.6).

It is worth to remind that both control structures do not use voltage feed-forward term, this is due to intention of having voltage sensor-less control. The influence of providing voltage feed-forward for balanced and unbalanced grid is verified experimentally. The grid voltage sensors were installed and serve only for references and figure plot. If the feed-forward term is present the current controller accommodate faster to the distorted voltage thus resulting in better current performance.

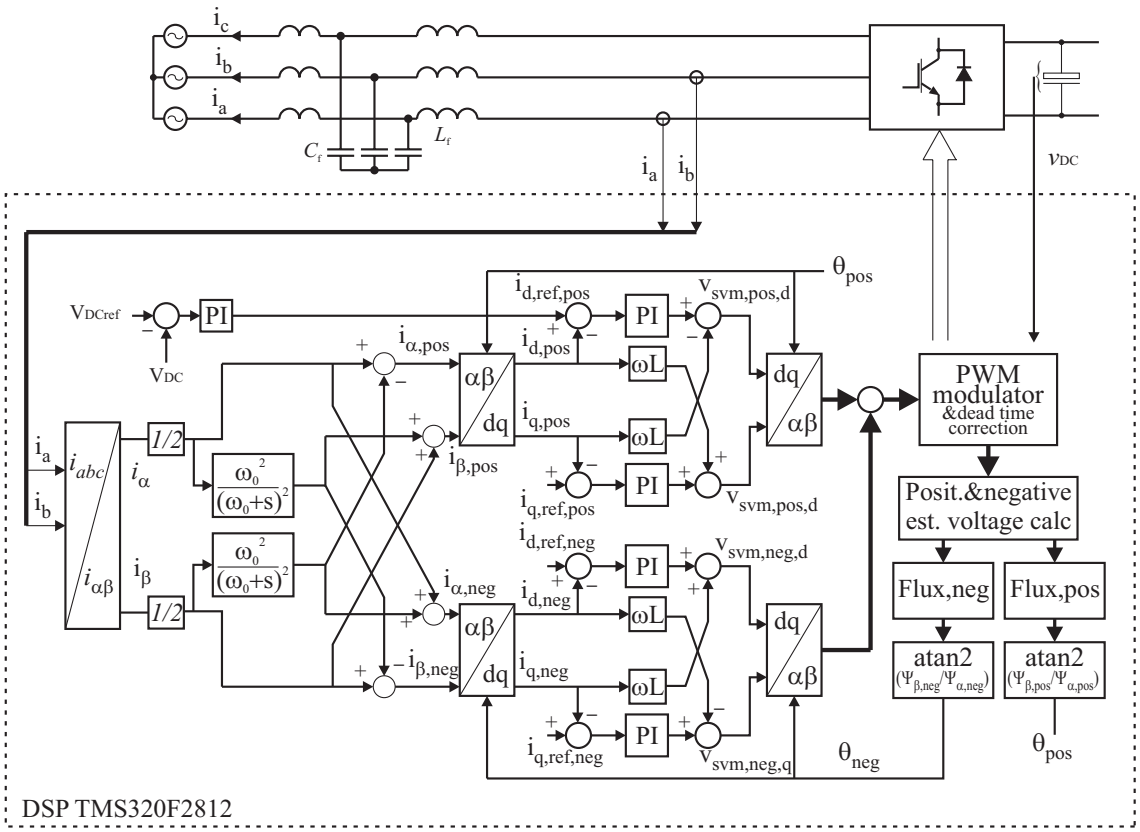

Figure 4.10: Dual current regulator with dual flux model control scheme used in laboratory experiment

The active power is supplied by a second converter which dc-link is back connected to the dc-link of the investigated converter. The dc voltage is also controlled by the second converter, so the reference current at the investigated converter i_d and i_q can be set freely. In Figure 4.10 the dc-link voltage controller is added for completeness only.

The data presented below on various figures based on experiments is first logged to the internal memory of the DSP and later transmitted to the PC via the serial port. In order to test the performance of the current controller in unbalanced condition a special unbalanced voltage source is prepared which is shown in Figure 4.12. Because the two converters are back connected (Figure 4.14), the three-phase transformer acts as a zero sequence separation unit. To make the voltage unbalanced an extra single-phase transformer is used in series with the input of one phase (Figure 4.12). The photograph of laboratory setup is in Chapter 4.5

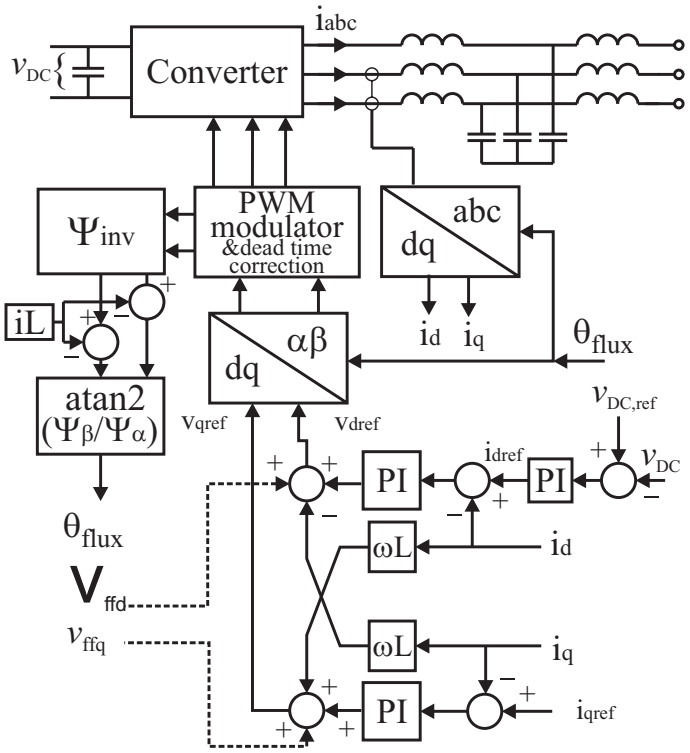

Figure 4.11: Converter control layout for single frame orientation

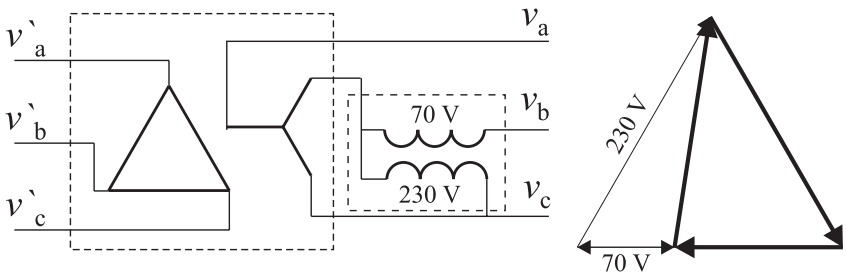

Figure 4.12: Configuration of unbalanced voltage source in experiment

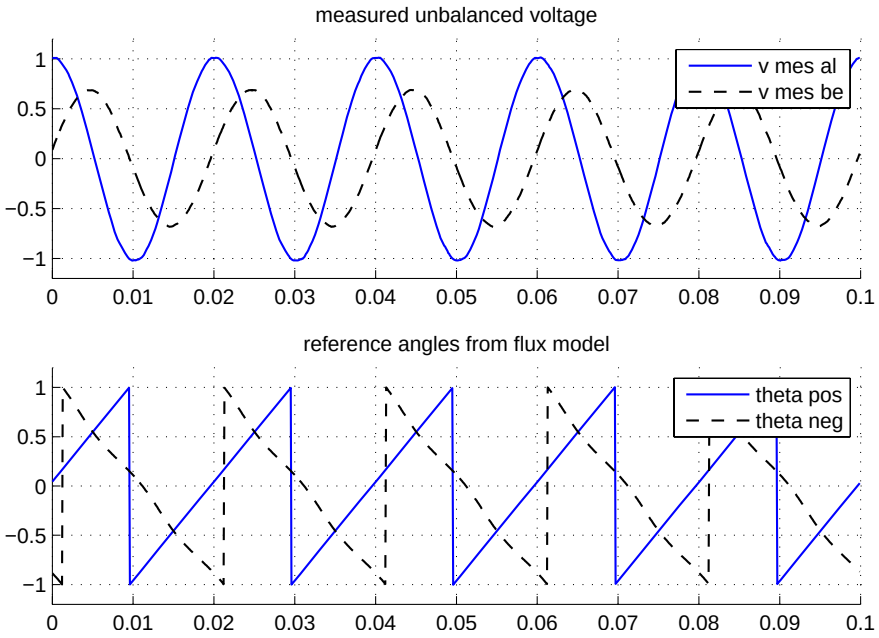

Figure 4.13: The top diagram shows the unbalanced measured grid voltage in laboratory in two phase coordinates (downloaded from DSP). This voltage is the result of connection from Figure 4.12.

The bottom diagram shows the orientation angle of the positive and negative sequence from flux model when the inverter is running in idle mode ($i_{d,ref}$=0, $i_{q,ref}$=0), the voltage sensors are not involved. Unfortunately during the time of experiment the discretization method of (3.18) is used for DVF. This is visible in the bottom of Figure 4.13 as the angle of negative sequence is little distorted. If equations (3.21) would be used instead the negative sequence angle would much better, but (3.21) was not known during the time of experiment.

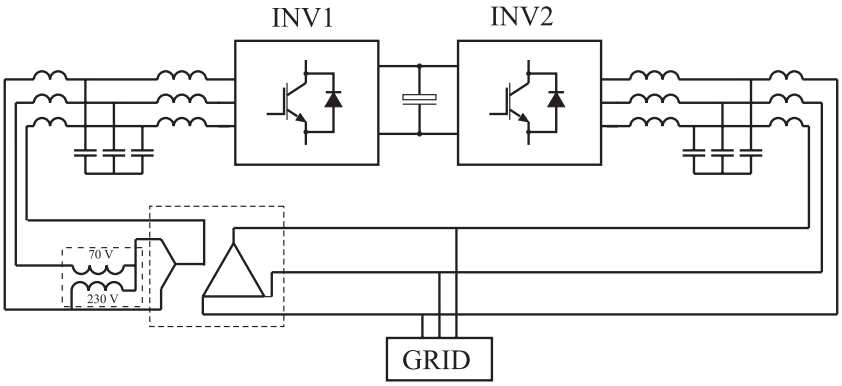

Figure 4.14: The layout of the laboratory setup

It is important to note that the proposed flux model returns independent reference angles for the positive and negative frames. Proper reference for the negative sequence enables to inject reactive and pulsating power in a controlled manner. It can be easily used for

low voltage ride through (LVRT) for symmetrical and unsymmetrical faults by providing proper references.
In many publications with a dual current controller, there is one reference angle. This positive reference is often derived from the PLL, and is orienting the positive frame current controller. The orientation for the negative frame is fed with the minus sign of the positive frame. So the negative frame is rotating in opposite direction but the phase shift between them is always 180°. This has limited application, and can control the negative current only to zero reference.

4.4.1.1. Feasibility of removing voltage measurement sensors for feed-forward

As it is possible to synchronize to the grid without voltage sensors we have to ensure that the voltage measurement in control scheme depicted in Figure 4.10 and Figure 4.11 used as a feed-forward term can be removed as well. In order to remove the voltage measurement completely the influence of the voltage feed-forward is checked by experimental verification.
As can be seen in Figure 4.15 when symmetric voltage is used the influence of feed-forward is insignificant.

For single frame orientation control (Figure 4.11) it is important to have the voltage feed-forward term during unbalanced operation when NSS accounts up to few %. The voltage feed-forward term, v_{ffd}, v_{ffq} support rejecting the100 *Hz* voltage disturbance.

For heavily unbalanced voltage and single frame controller the influence from NSS is much stronger and the voltage feed-forward is not able to compensate it completely. The unbalanced voltage with single frame current control and influence of feed-forward is depicted in Figure 4.16, Figure 4.17, Figure 4.18, Figure 4.19, Figure 4.20 and Figure 4.21. The 100 *Hz* ripples in current waveform simply cannot be compensated completely by increasing bandwidth of the current controller. However by increasing the gains of PI controller the performance could be slightly improved.

For the dual frame current controller the importance of having voltage feed-forward is diminishing due the fact that the signal is split into two frames which handle the positive and negative frequencies separately as dc quantities. There is no risk that PI controller will not be able to reject the negative signal like in single frame control. The situation is similar to balanced single frame condition. No feed-forward also means that during start up of the converter the integration part of PI should be initialized, otherwise smooth current transition is not guaranteed. The performance of dual current controller under heavily unbalanced condition is depicted in Figure 4.22 and Figure 4.23

4.4.1.2. Influence of the voltage feed-forward term on single frame current controller in balanced condition

Laboratory results on single frame current controller oriented by single frame virtual flux model.

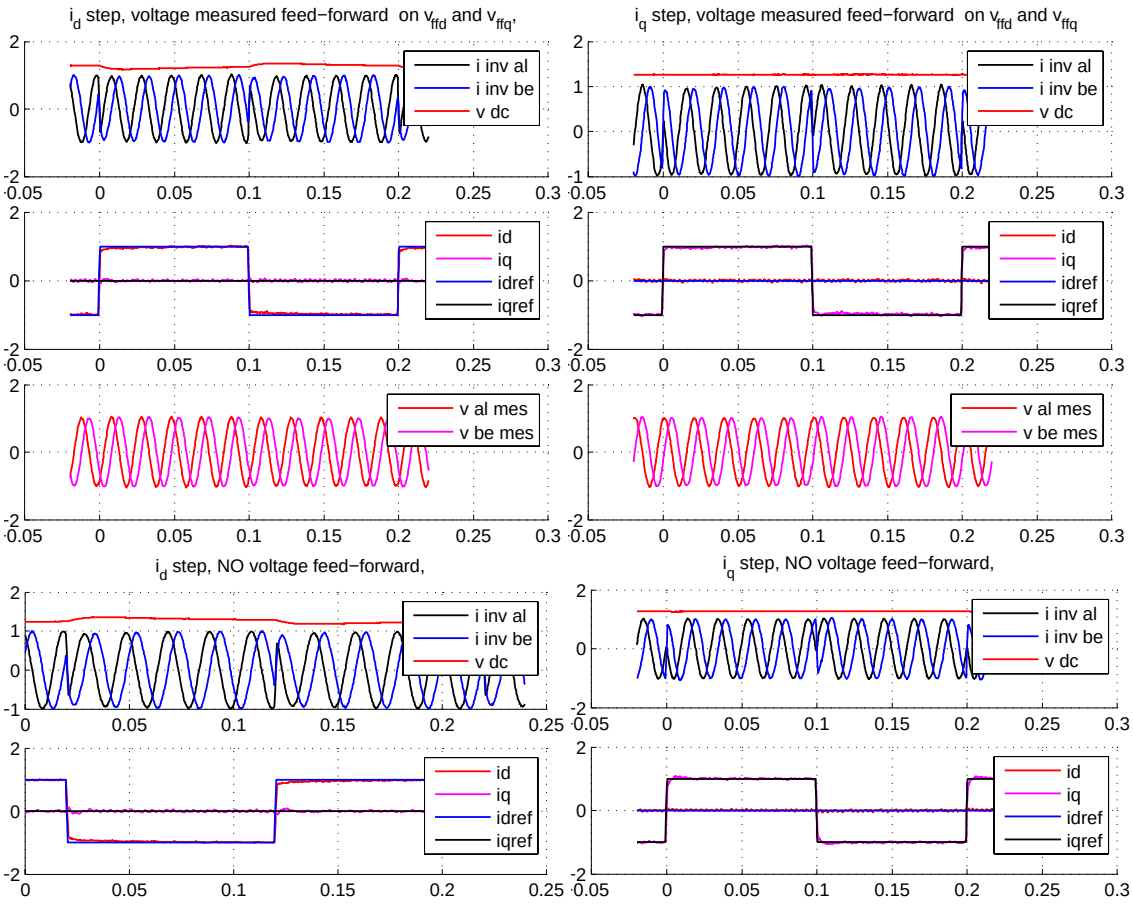

Figure 4.15: Voltage feed-forward influence on single frame orientated by virtual flux model

As it can be expected, there is no influence in the current regulation when voltage is symmetrical. The influence could appear when rapid transient in voltage amplitude would occur, e.g. dips or sags but this is not the case investigated here. The feed-forward influence investigation is carried out here only for a purpose of unbalanced condition and sensor-less operation with virtual flux.

4.4.1.3. Influence of the feed-forward term during unbalanced condition for single frame orientation

Influence of voltage feed-forward during *d*-axis current step – laboratory experiment

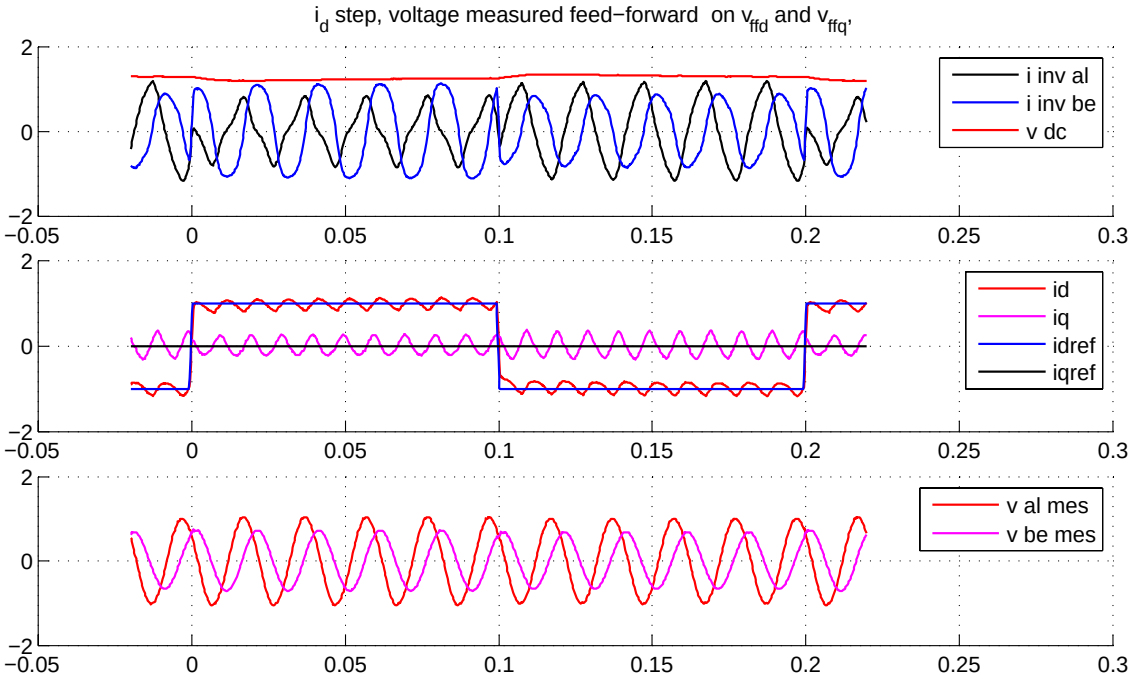

Figure 4.16: Voltage feed-forward, the *d*-axis current step

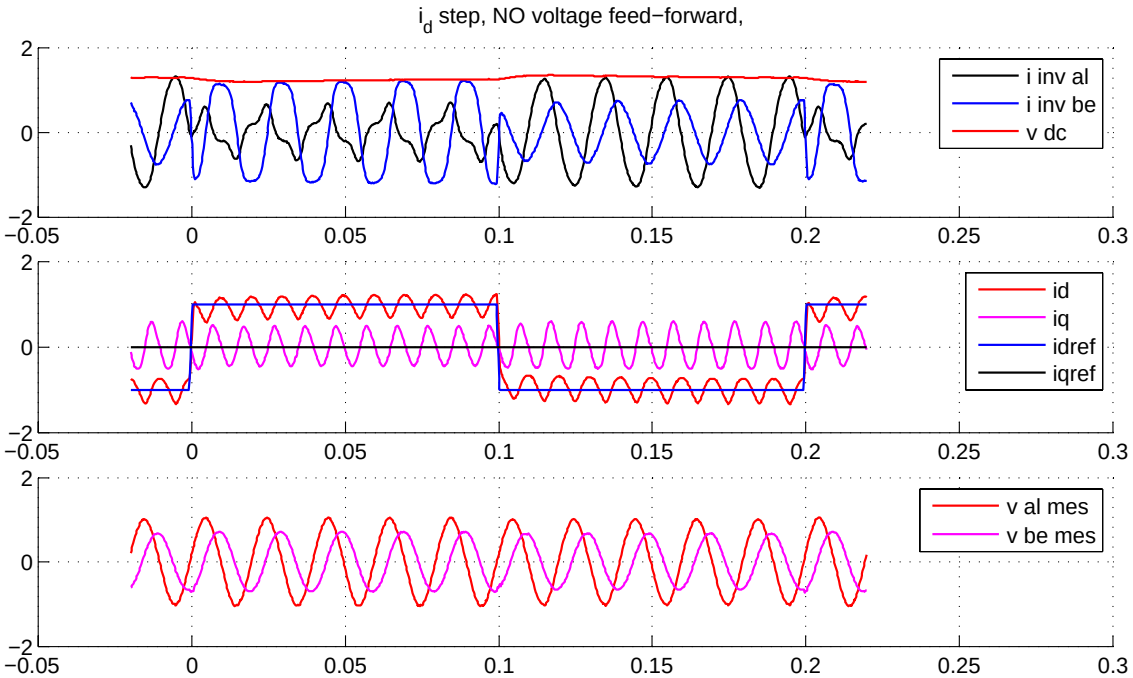

Figure 4.17: No feed-forward voltage, the *d*-axis current step

Influence of voltage feed-forward during *q*-axis current step – laboratory experiment

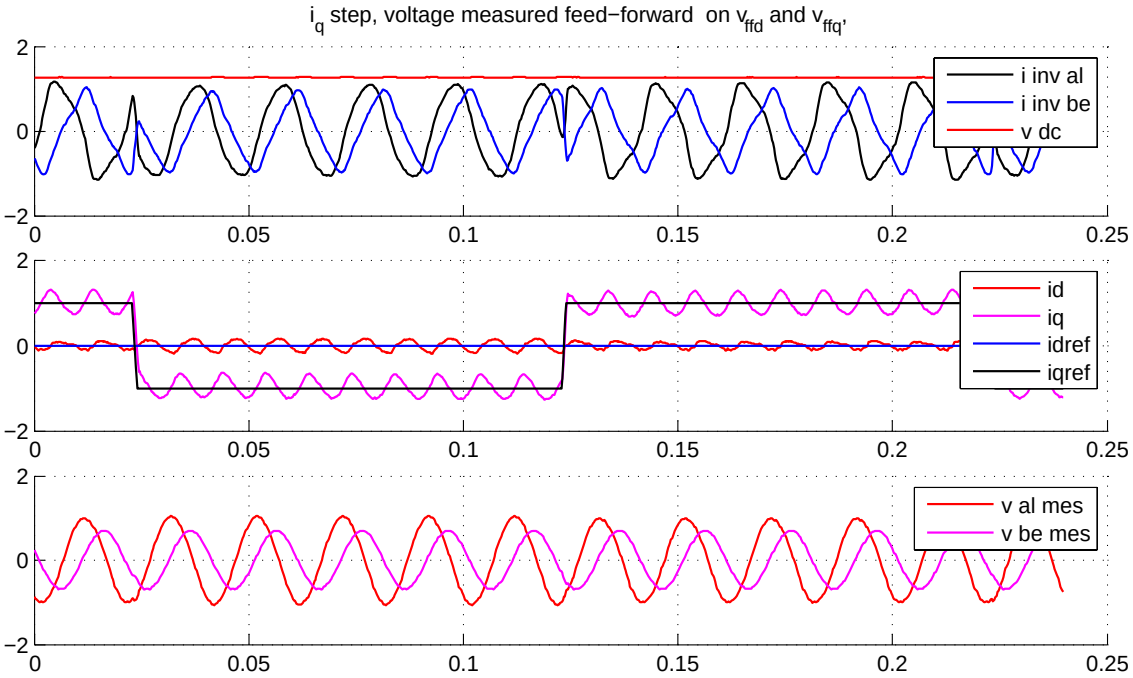

Figure 4.18: Voltage feed-forward, the *q*-axis current step

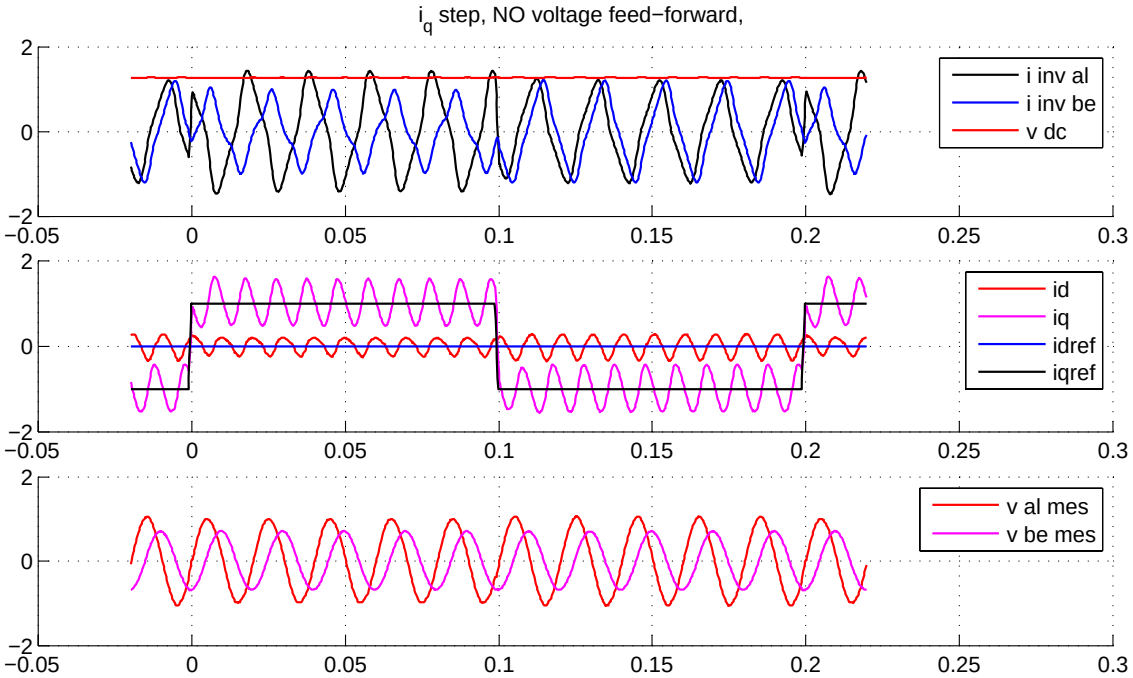

Figure 4.19: No feed-forward voltage, the *q*-axis current step

Influence of partial feed-forward on *d*- and *q*-axis current – laboratory experiment

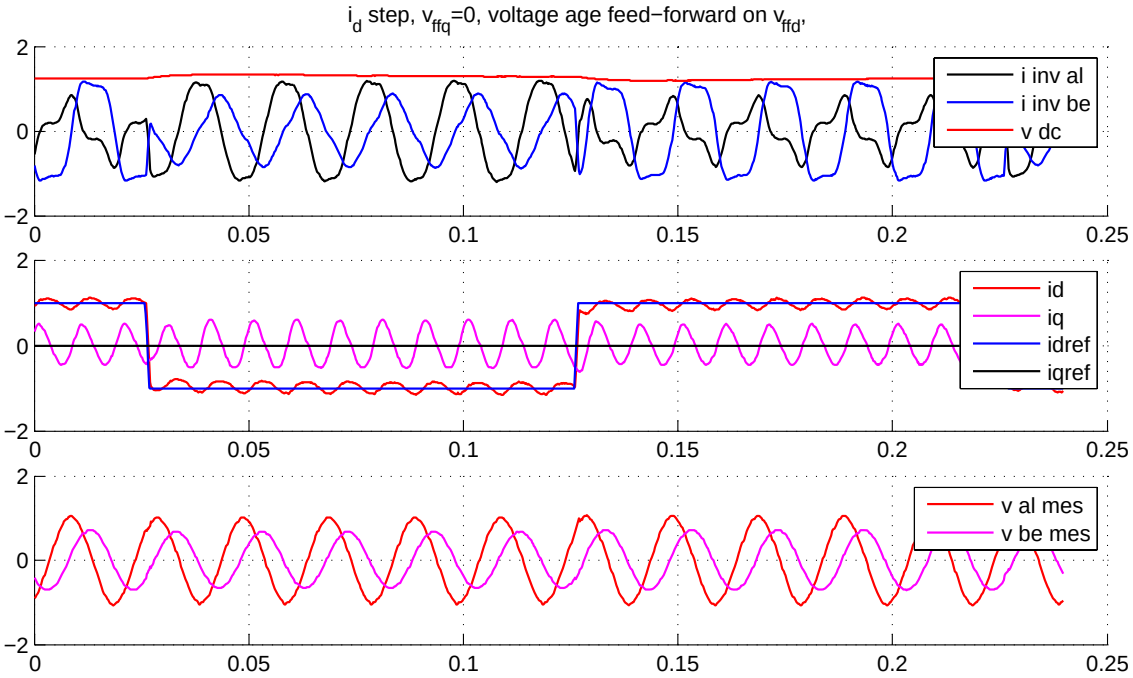

Figure 4.20: The d-axis current step when v_{ffd} is delivered and v_{ffq}=0.

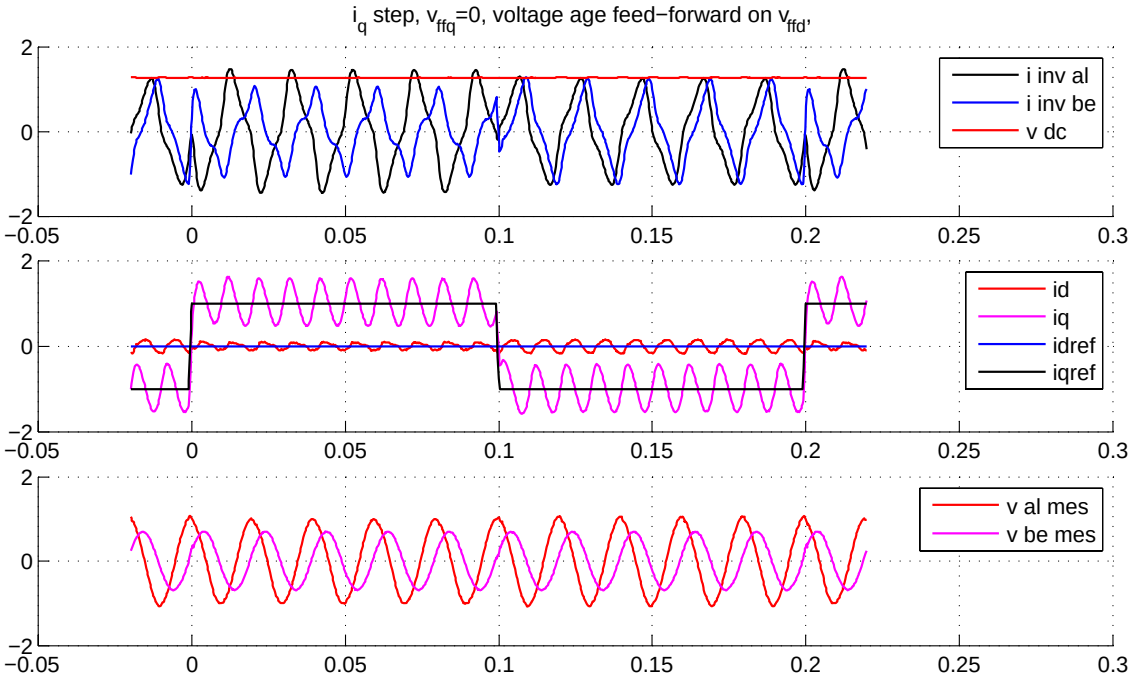

Figure 4.21: The q-axis current step when v_{ffd} is delivered and v_{ffq}=0

As it can be expected, during unbalanced conditions the voltage feed-forward term does not significantly improve the current waveforms. The current controller is not able to reject the 100 *Hz* disturbance, from NSS. The grid current is heavily distorted.

4.4.1.4. Comparison of single and dual frame control under unbalanced voltage - laboratory results

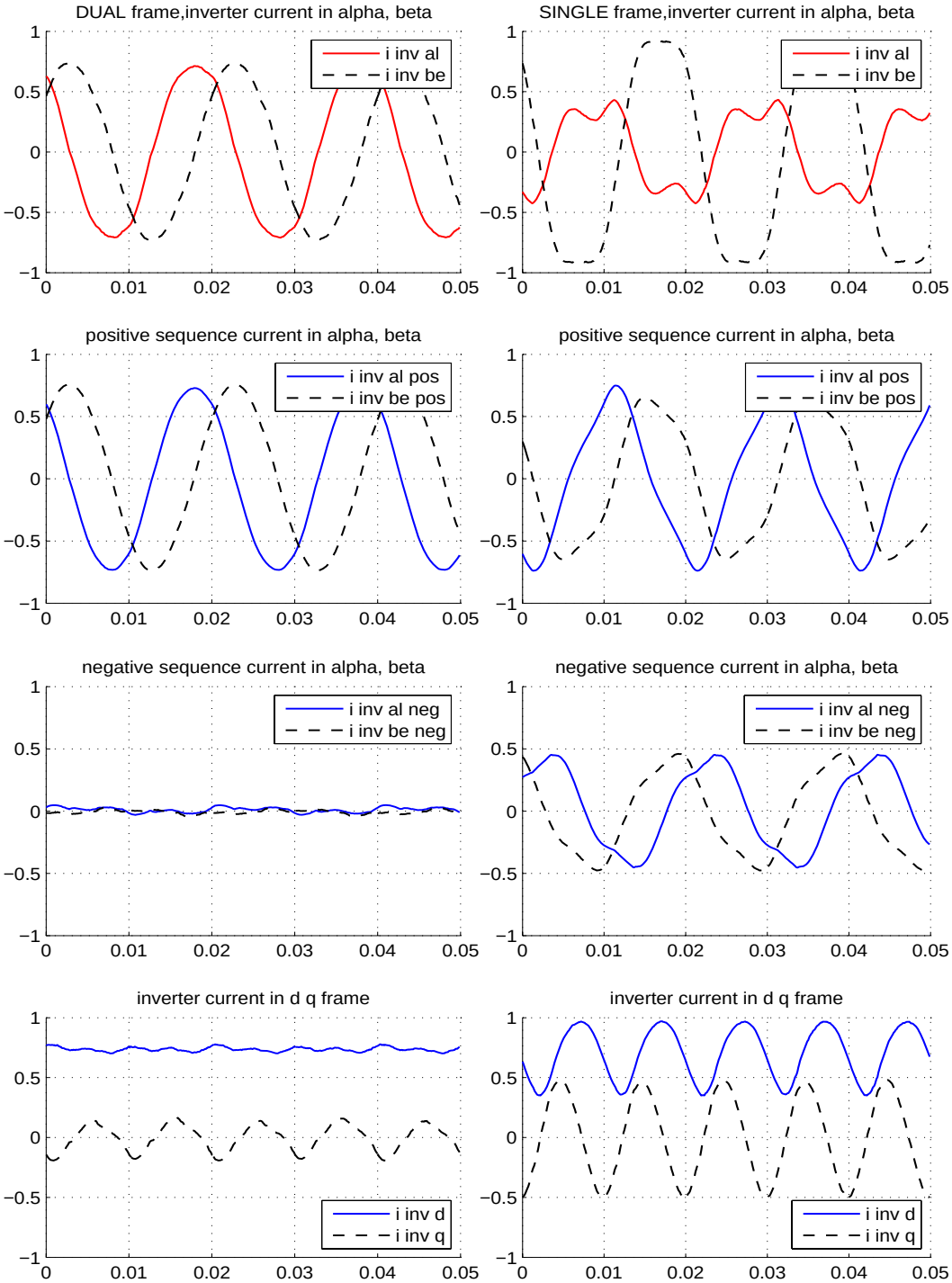

Figure 4.22: Comparison between dual frame and single frame current control. Left column – dual current controller, right column – single current controller. Second and third row from the top represents the decomposed current from the first row. The fourth row represents the i_d and i_q current during unbalanced operation

In Figure 4.22 there is a comparison of the dual and single frame current controller strategy depicted at Figure 4.10 and Figure 4.11 accordingly. For both of the cases the reference current is $i_{d,ref}$=0.75 and there is no voltage feed-forward term to improve the current controller performance. As can be expected the current waveform under unbalanced voltage can be maintained sinusoidal only under dual frame current control.

The current parameters are as follows

$K_{p,pos}$=0.6	$K_{i,pos}$=5	$K_{p,neg}$=0.6,	$K_{i,neg}$=5
$i_{d,ref,pos}$=0.75	$i_{q,ref,pos}$=0	$i_{d,ref,neg}$=0	$i_{q,ref,neg}$=0

For both cases the PI regulator parameters are the same. In case of the single frame current controller the bandwidth of the PI regulator is not enough which results in an unbalanced and nonlinear current. By increasing the gain of PI regulator the response can be improved slightly but it is not the proper solution and can lead to the unstable system.
In the case of dual frame controller the positive sequence current is sinusoidal with amplitude of reference and the negative sequence current is zero.

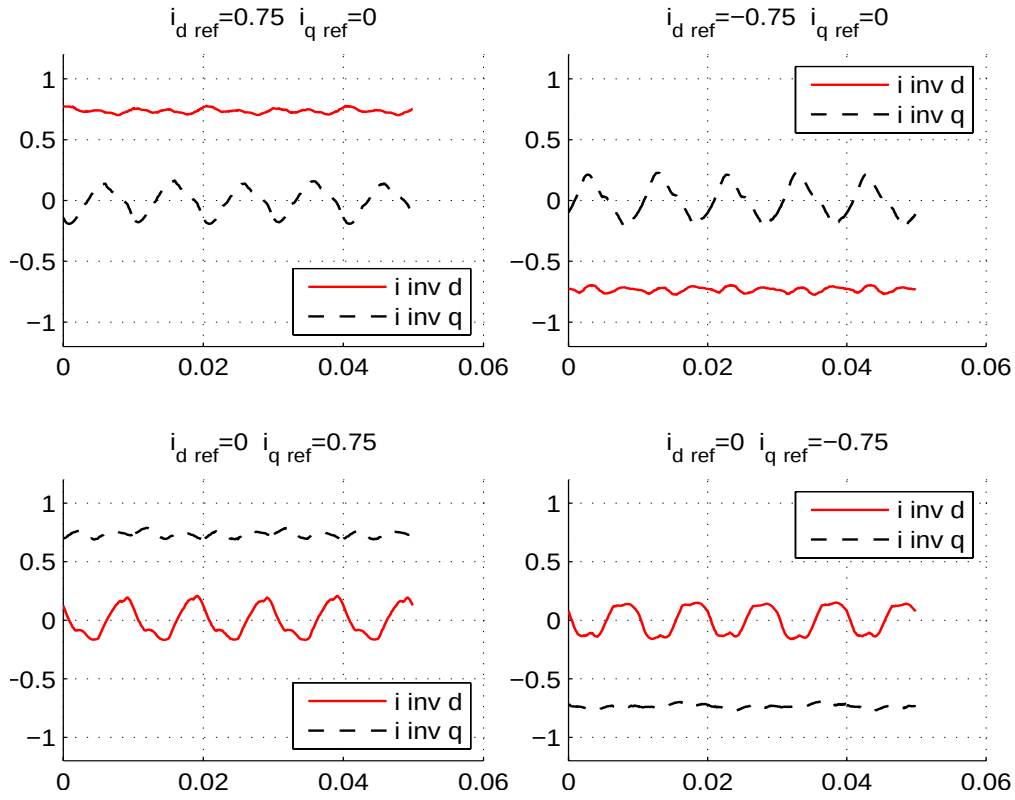

Figure 4.23: Inverter current in d q frame during unbalanced voltage, controlled by dual current controller

In Figure 4.23 the parameters are as follow:

$K_{p,pos}$=0.6	$K_{i,pos}$=5	$K_{p,neg}$=0.6,	$K_{i,neg}$=5
$i_{d,ref,pos}$=±0.75 *p.u.*	$i_{q,ref,pos}$=±0.75 *p.u.*	$i_{d,ref,neg}$=0	$i_{q,ref,neg}$=0

The Figure 4.23 shows the inverter currents corresponding to four quadrant of operation, (currents: active forward, active reverse, reactive inductive, reactive capacitive). All those current reference are given to positive frame only, the negative frame current *d*- and *q*-axis is zero. The dual frame current controller is used. The inverter supply voltage during test is unsymmetrical, and the current are symmetrical due to use of dual frame control.

It is also easy to observe pulsating power related to unbalanced condition; with the average value is zero. The pulsating power is related to equations (2.71) and (2.72).
Balanced current and unbalanced voltage forms circuit where pulsating power is flowing between the inverter and grid. In order to achieve no pulsating power flow for unsymmetrical voltage the currents should be unsymmetrical too.

4.4.1.5. Simulation results of supplying balanced currents into unbalanced voltage grid

The simulation is conducted in order to verify the results from previous section based on experiments. In the case of unbalanced voltage and balanced currents the reference for negative sequence currents are zero.

$$\begin{aligned} i_d^n &= 0 \\ i_q^n &= 0 \end{aligned} \tag{4.8}$$

The below results are from simulation program PSCAD/EMTDC which were exported to Matlab for plotting. The parameters of simulation are as follows:

switching frequency	10 *kHz*
nominal line current (1 *p.u.*)	50 *A*
nominal phase voltage	230 *V*
nominal power	34,5 *kVA*
grid filter inductance	750 μH
grid filter capacitance	25 μF
dc-resistor load,1 *p.u.*	12,25 Ω
dc-link voltage, 1 *p.u.*	650 *V*

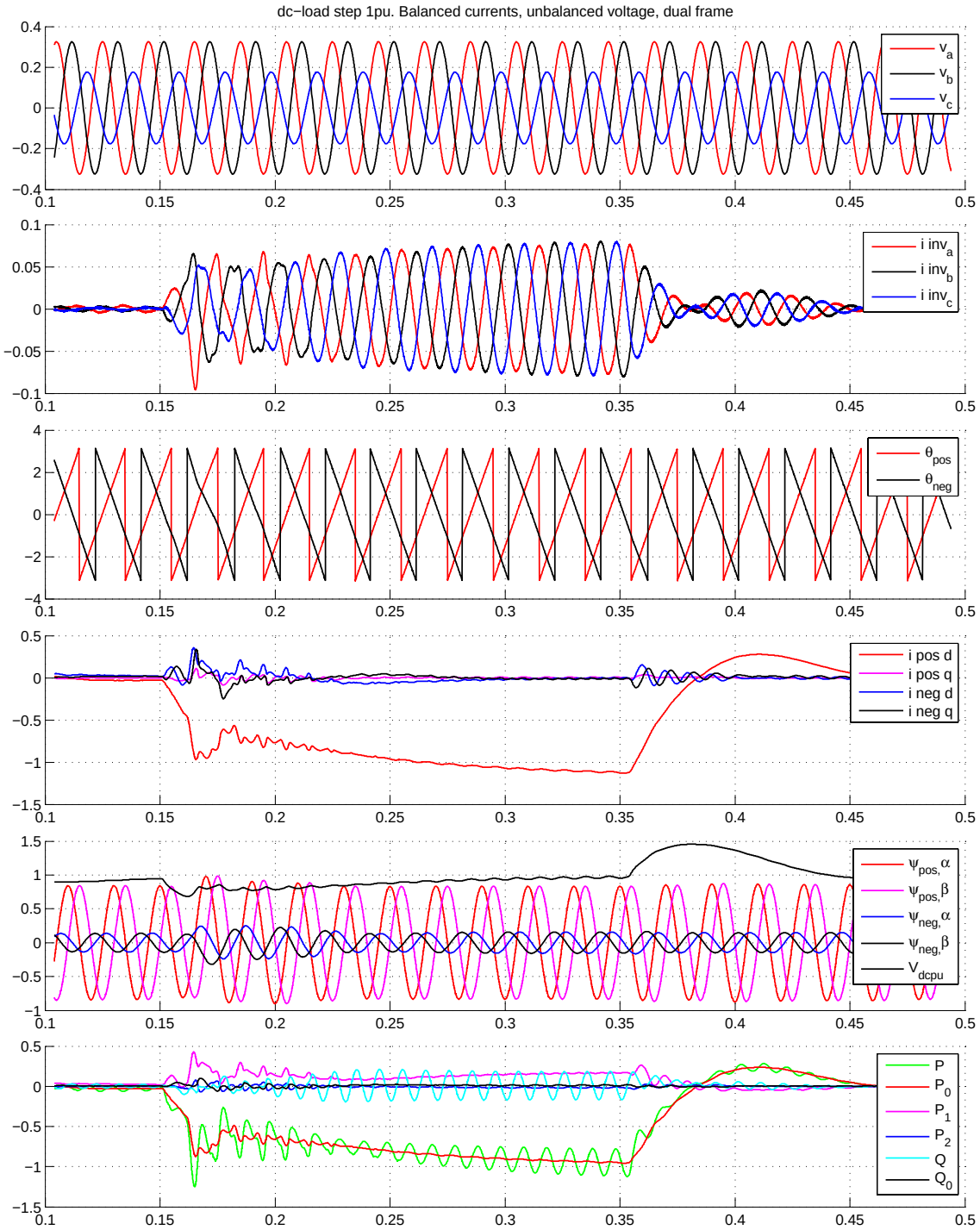

Figure 4.24: Supplying symmetrical currents into unbalanced grid transient response

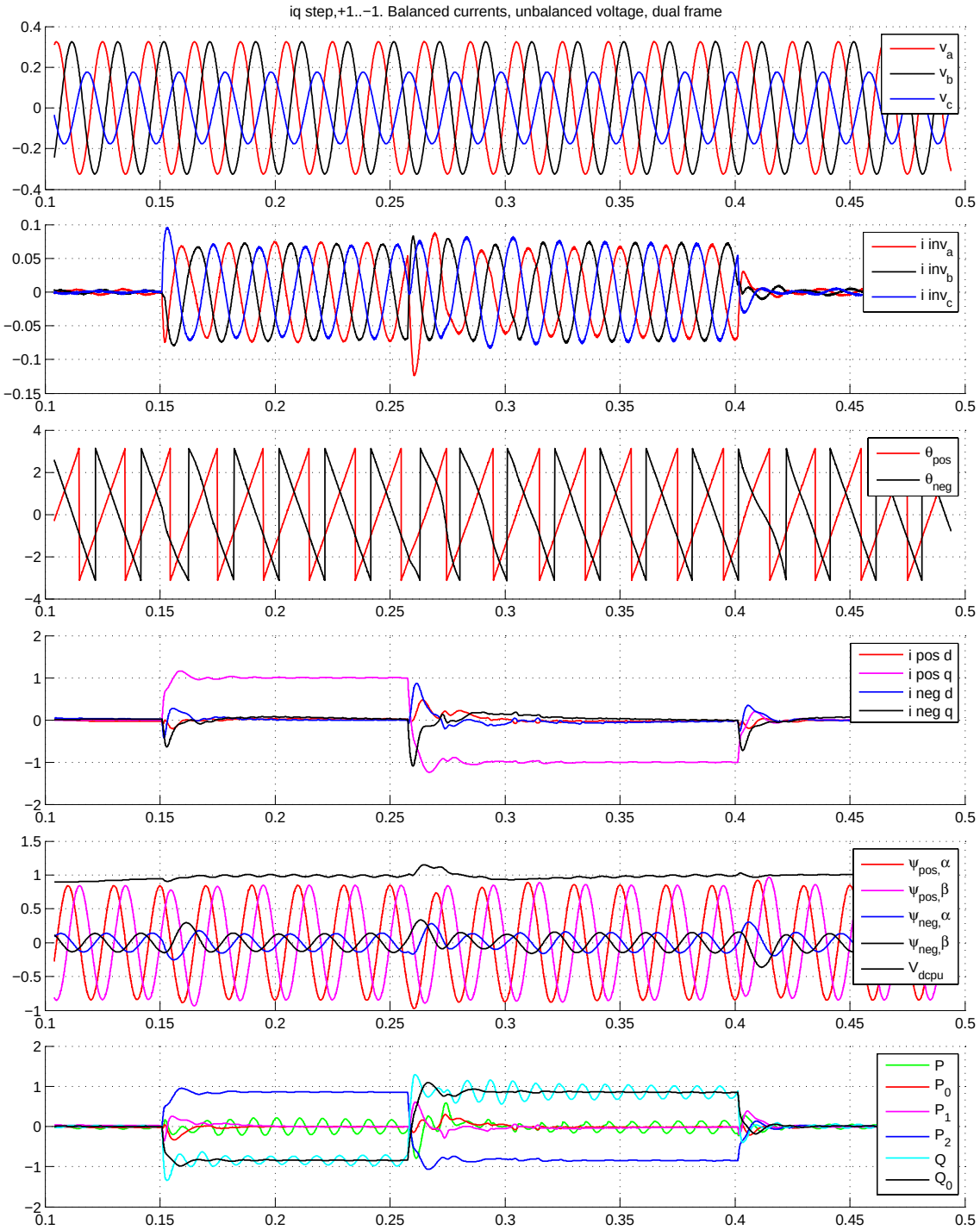

Figure 4.25: Reactive power transient for unbalanced grid and balanced currents

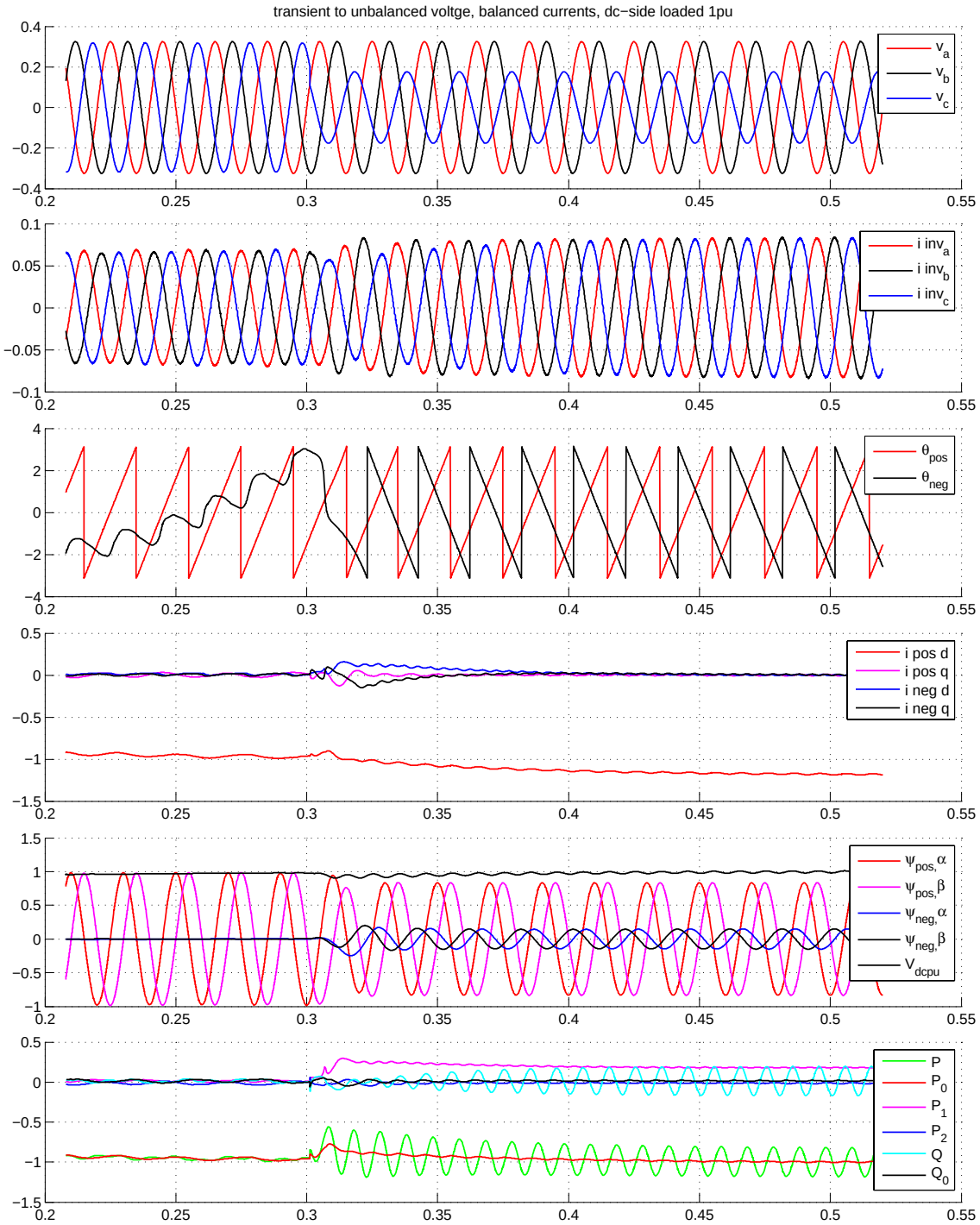

Figure 4.26: Sudden drop of one phase voltage and resulting currents, dc-side load 1 p.u.

4.4.2. Simulation results of supplying constant instantaneous power for unbalanced grid

In order to supply constant power the proper reference to the positive and negative frame current controllers are made. The references are based on unbalanced system power equations (2.69) (2.70) (2.71) (2.72). The direct references for the negative and positive frame can be written as:

$$\begin{aligned} i_{d,ref}^{p} &= -v_{d}^{p} \cdot 2 \cdot P_{dc,ref} / 3D \\ i_{q,ref}^{p} &= -v_{q}^{p} \cdot 2 \cdot P_{dc,ref} / 3D \\ i_{d,ref}^{n} &= v_{d}^{n} \cdot 2 \cdot P_{dc,ref} / 3D \\ i_{q,ref}^{n} &= v_{q}^{n} \cdot 2 \cdot P_{dc,ref} / 3D \end{aligned} \tag{4.9}$$

Where:

$$D = \left(v_{d}^{p}\right)^{2} + \left(v_{q}^{p}\right)^{2} - \left(\left(v_{d}^{n}\right)^{2} + \left(v_{q}^{n}\right)^{2}\right) \tag{4.10}$$

$$P_{dc,ref} = i_{d,ref} v_{dc,ref} \tag{4.11}$$

The $i_{d,ref}$ is the output from the existing dc-link controller.

In all figures from Figure 4.24 to Figure 4.28 the most bottom diagram shows power. The power is calculated according the power equations (2.67), (2.68), (2.69), (2.70) (2.71), (2.72). Where P_c=P_1 and P_s=P_2. The equations (2.67), (2.68) correspond to *P* and *Q* and are valid only for balanced system. They are placed only for comparison with their unbalanced counterparts.

The phase voltage and phase currents are expressed in *kV* and *kA* as it is normally the case in PSCAD. The flux angle is expressed in radians. The synchronous currents for positive and negative frame, the flux and power are expressed in per unit value.

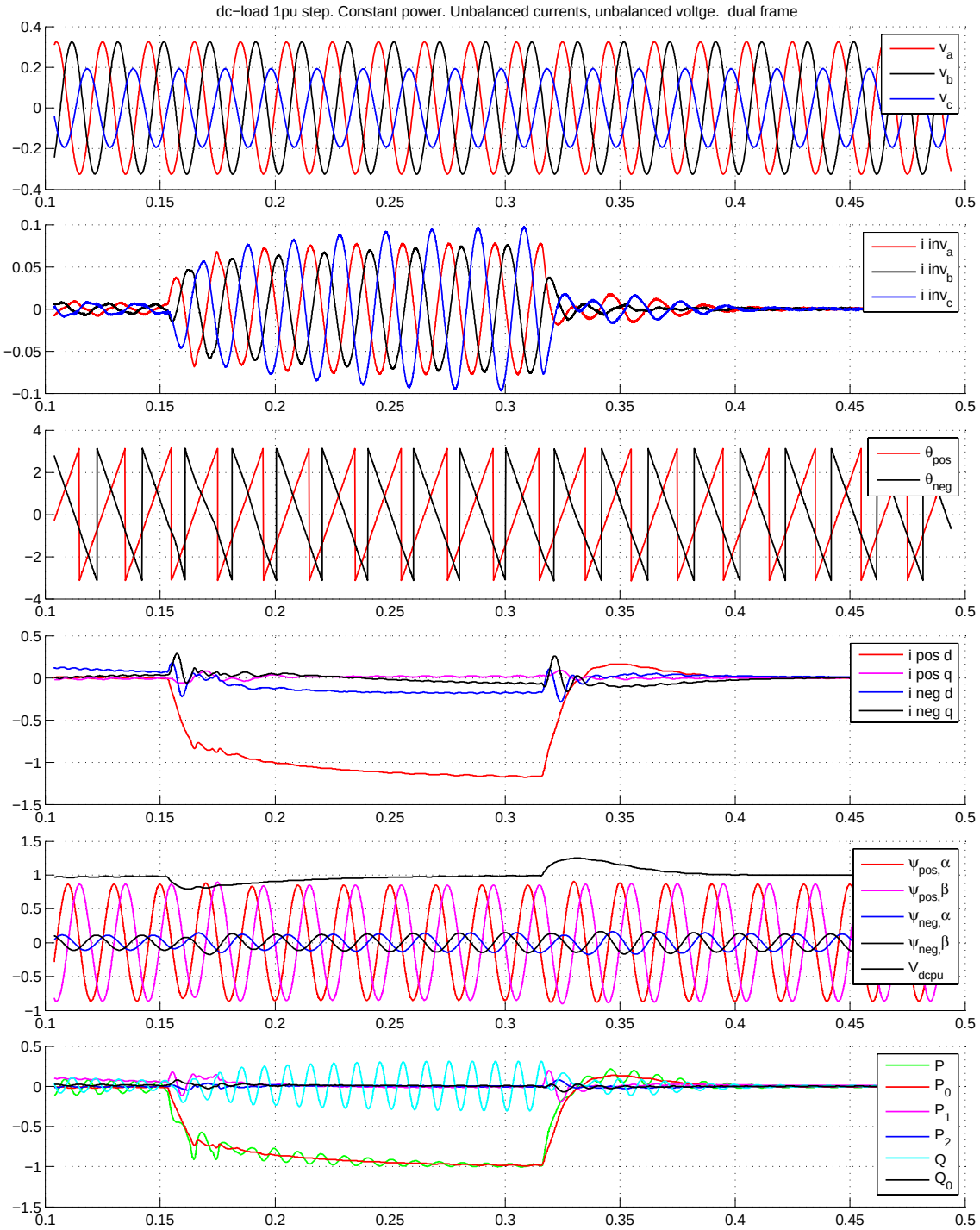

Figure 4.27: Instantaneous pulsating power reduction. Unbalanced voltages and currents

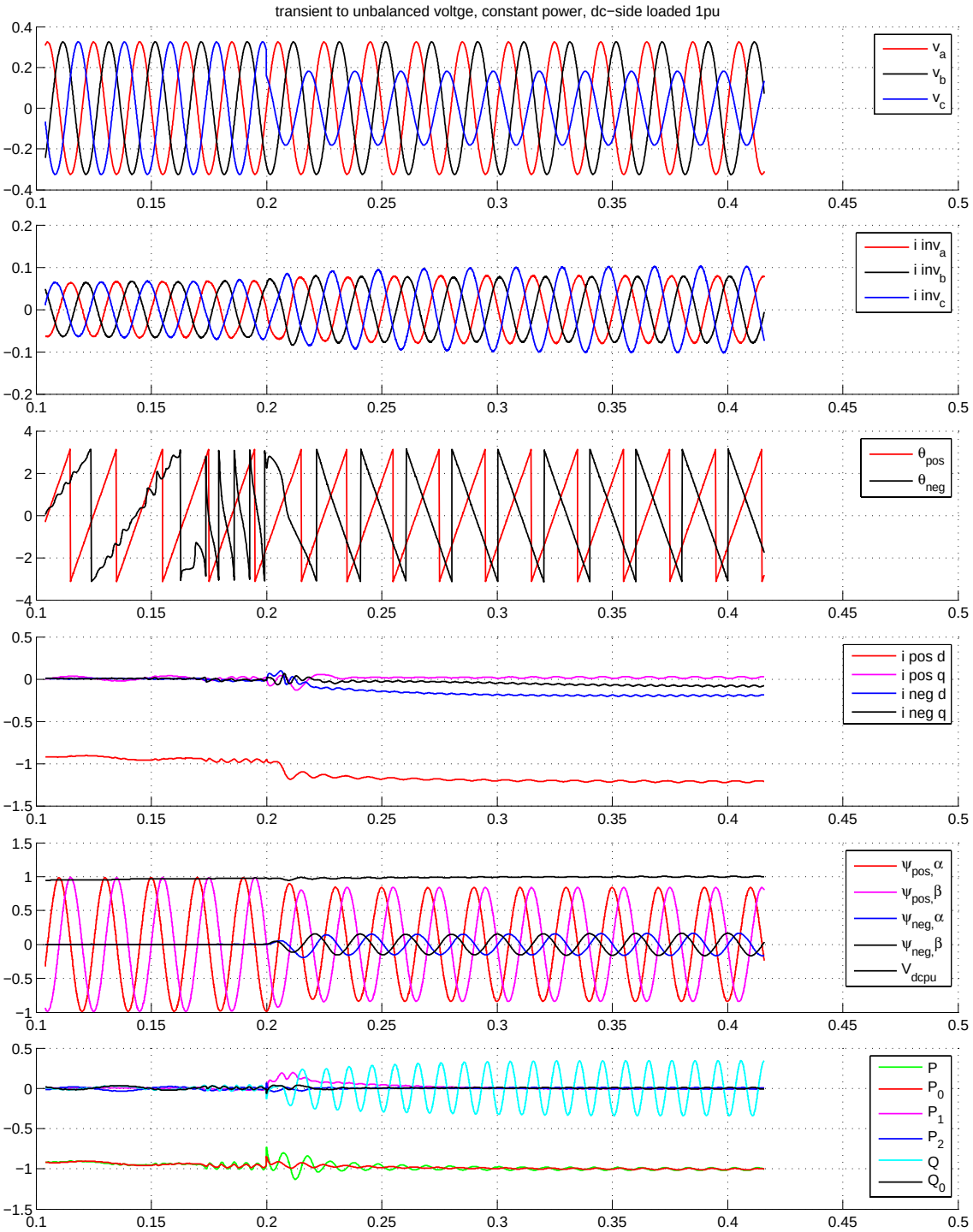

Figure 4.28: Transient to unbalanced voltage while the power should stay constant.

4.5. Laboratory setup

4.5.1. DSP system implementation

The control algorithms are implemented in *C* language. The routines are called every $100\,\mu s$ as the interrupt from timer occurs. The synchronous sampling is used which ensures minimum switching noise at the current measurement.
The DSP is set up in such a way that at the bottom of the reference triangular signal the ADC is set to perform measurement on specified channels. When the ADC is finished it then immediately calls the interrupt in which the control algorithms are executed. The control functions are organized by a state machine which support start of the converter, performs calibration, grid synchronization, etc. When the inverter is ordered to start the ADC calibration and grid synchronization is performed first. When they succeed the controls enters the current control mode.
On the second inverter the dc-link voltage controller is enabled which controls the common voltage by setting proper i_d reference current. In such a dc bus there must be only one dc voltage controller. The dc-link controller at inverter 1 is disabled.
During interrupt execution, the results from ADC are first scaled to *p.u.* notation and transformed by the Clark and Park transformations. Then the error current is derived which is fed to the PI regulator. The output from PI regulator is decoupled from the dc-link voltage. The reference duty ratio is converted back to the stationary frame and relayed to the modulator. If the dead time correction routine is needed then it is additionally called and results fed to the modulator. Modulator converts from two phase system to three-phase and sets the PWM registers for corresponding inverter legs. The symmetric decomposition and DVF model are also called during the interrupt.

4.5.2. Photograph of the laboratory setup

The laboratory setup presented in Figure 4.30 is the main setup used at NTNU for development of this thesis, the layout is depicted in Figure 4.14. It also serves for development of Chapter 4, Chapter 5 and Chapter 6. The Chapter 7 and Chapter 8 have their independent laboratory setups.

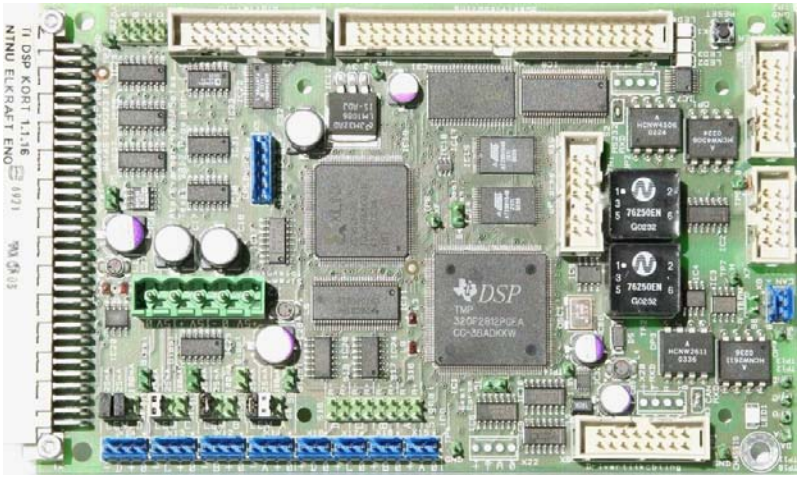

Figure 4.29: Control card used in experiments. DSP – TMS320F2812

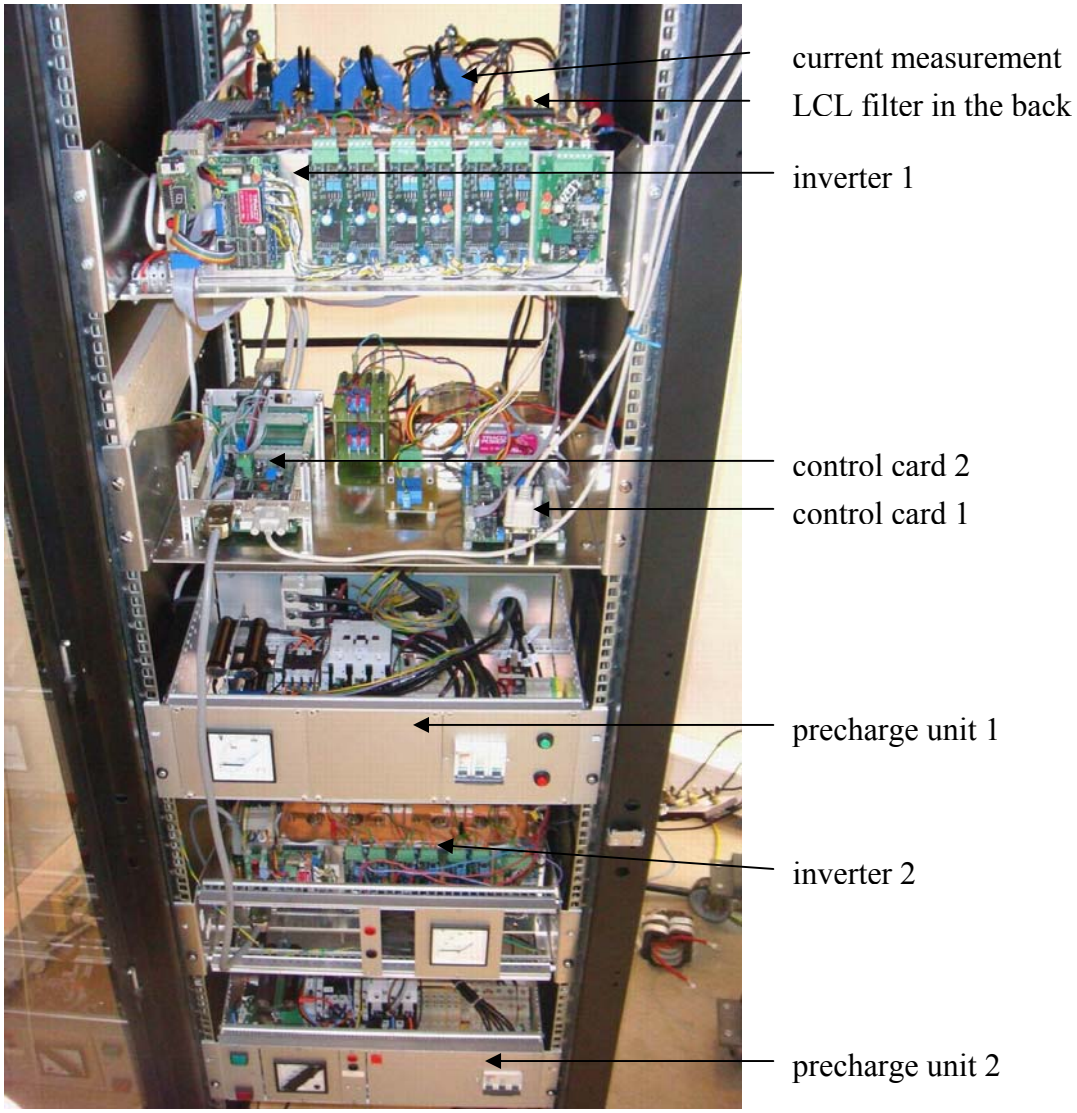

Figure 4.30: Rack with the back to back inverter equipment

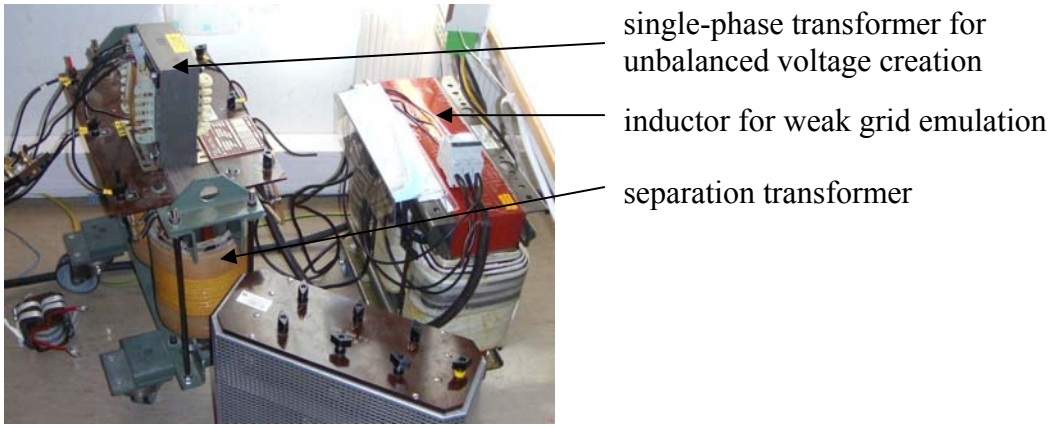

Figure 4.31: Three-phase transformers and inductors

4.6. Chapter summary

The dual virtual flux concept is presented. The model of DVF development is presented and includes: analysis of transfer function, discretization, bias cancellation, implementation, simulation and experimental results. The DVF can operate in unbalanced voltage conditions without using the voltage sensors. The positive and negative frame current control enables cancelation of 100 *Hz* ripples coming from negative sequence. The method is design to operate under heavily unbalanced conditions and thus is difficult to compare with other correction algorithms which based on single frame orientation or DPC.
The advantage of having two independent frames is that the *d*- and *q*-axis reference current of each sequence can be controlled independently. This enables realization of many various functions.

In this Chapter two modes of operation are presented: symmetrical current under unbalanced voltage and constant power under unbalanced voltage and current.

The symmetric current during unbalanced voltage does not provide constant power and the circuit become more similar to single-phase. The possibility of realizing constant power under unbalanced grid is very beneficial for the lifetime of the dc-link capacitor. Converter which was designed for symmetrical operation and especially the dc capacitor might prematurely fail under unbalanced conditions which were not predicted during design stage. The presented solution prevents it by minimizing the current ripples in the dc-link capacitor. The dc-link capacitor life time is highly correlated with current ripple and temperature.

The third mode of operation can be utilized during unsymmetrical faults. By providing proper current reference, it would be possible to provide low voltage ride through (LVRT) capability. For symmetrical system the injection of reactive power to support the voltage does not show difficulties. The injection of reactive power into unbalanced voltages is much more challenging, because must provide pulsating reactive power.

5. SYNCHRONIZATION TO THE GRID

5.1. Synchronization to the grid without voltage sensors

Since there is a possibility of controlling the current without voltage sensors, it is also beneficial if the converter can start operation without them. As the converter is voltage "blind", it uses other sensors and actuators to sense the initial angle of the grid. The standard synchronization procedure which is called sampling here, can be read in [gul2]. The operation is based on inserting the modulator zero vector and measuring the current response. In other words the grid gets short circuited by the inverter switches for a short time (<100 μs) and the current is measured. This usually happens two times, shifted by 90 degrees, and the full grid angle can be calculated. There is no danger of over current since inductors are in series with the grid.

First the standard approach with grid sampling will be presented [gul2]. Secondly the newly proposed method which does not require grid sampling or more important, flux model initialization, is presented. This very nice feature of the proposed flux model is due to the short time response compared to conventional flux model.

5.1.1. Standard synchronization with sampling for balanced voltage

The method assumes that all transistors are in off state, and the dc-link is charged to the peak line voltage. The pre-charging of dc-link is usually done by the internal diodes of the IGBT's and some limiting current resistors in series with the grid. The inverter dc-link capacitor can also be charged from the dc side.
After the dc-link capacitor is pre-charged, the converter can be connected directly to the grid without a large inrush current. The DSP control board must also have the possibility to switch on and off all upper or lower IGBT's instantaneously. Switching all upper or lower transistors for a short time (e.g. 100 μs) will cause short circuit of the grid through the L/LCL filter. After switching on, the current will rise rapidly, and after maximum time or maximum current the transistors are switched off. The currents should be measured and saved. The short circuiting is repeated after 5 ms which corresponds to 90 electrical degrees.
Looking at the angle of both current vectors it is possible to estimate the voltage vector position and other useful information. If the difference is around 90° then we have positive sequence, if -90° then negative, if the difference in currents is large that could

mean that voltage is unbalanced or one phase is disconnected. If both amplitudes are near zero that means that no power exists in the grid.

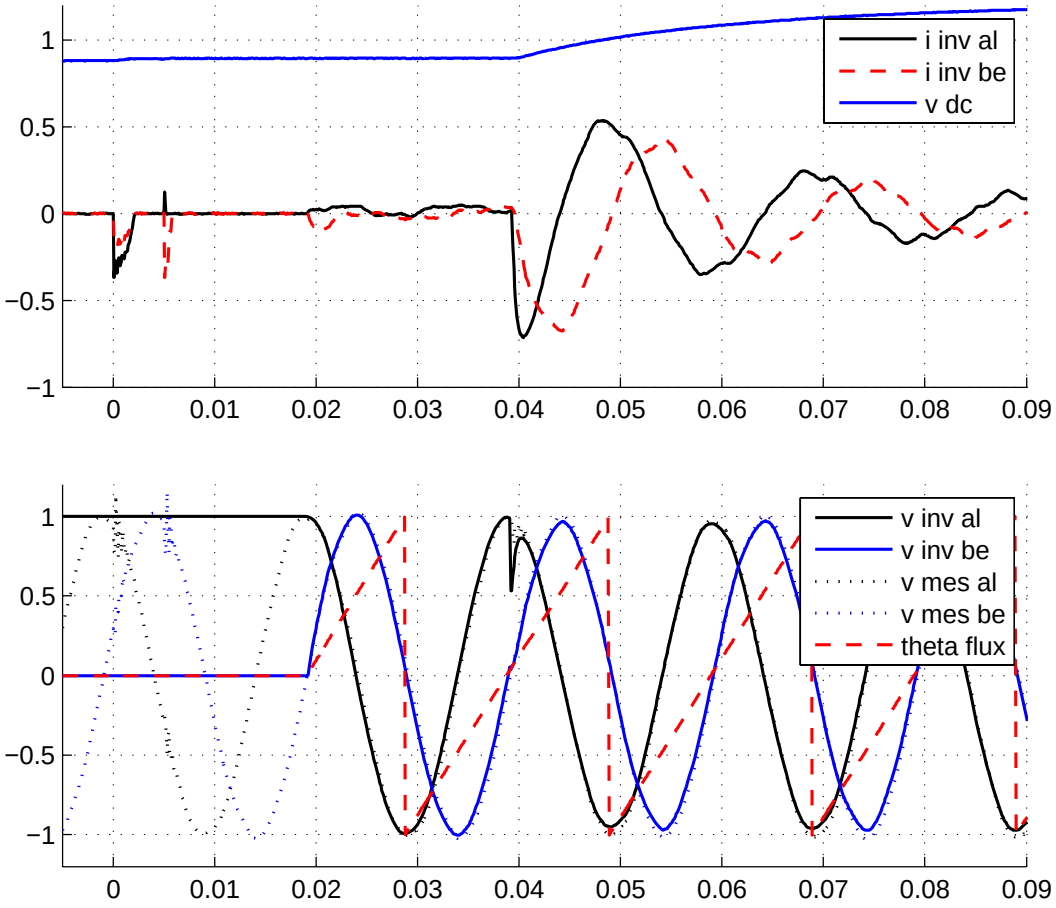

Figure 5.1: Initial start of the converter with sampling. For the inverter filter inductance L is only used (750μH)

Knowing the voltage vector position we have to initialize the flux internal variables as the flux would normally exist for that angle. Initializing the variables is not so convenient; all these initial fluxes must be calculated from amplitude of the currents during sampling. The inductance of the filter should be known. In laboratory setup, precision for estimating of grid angle is ±4°.

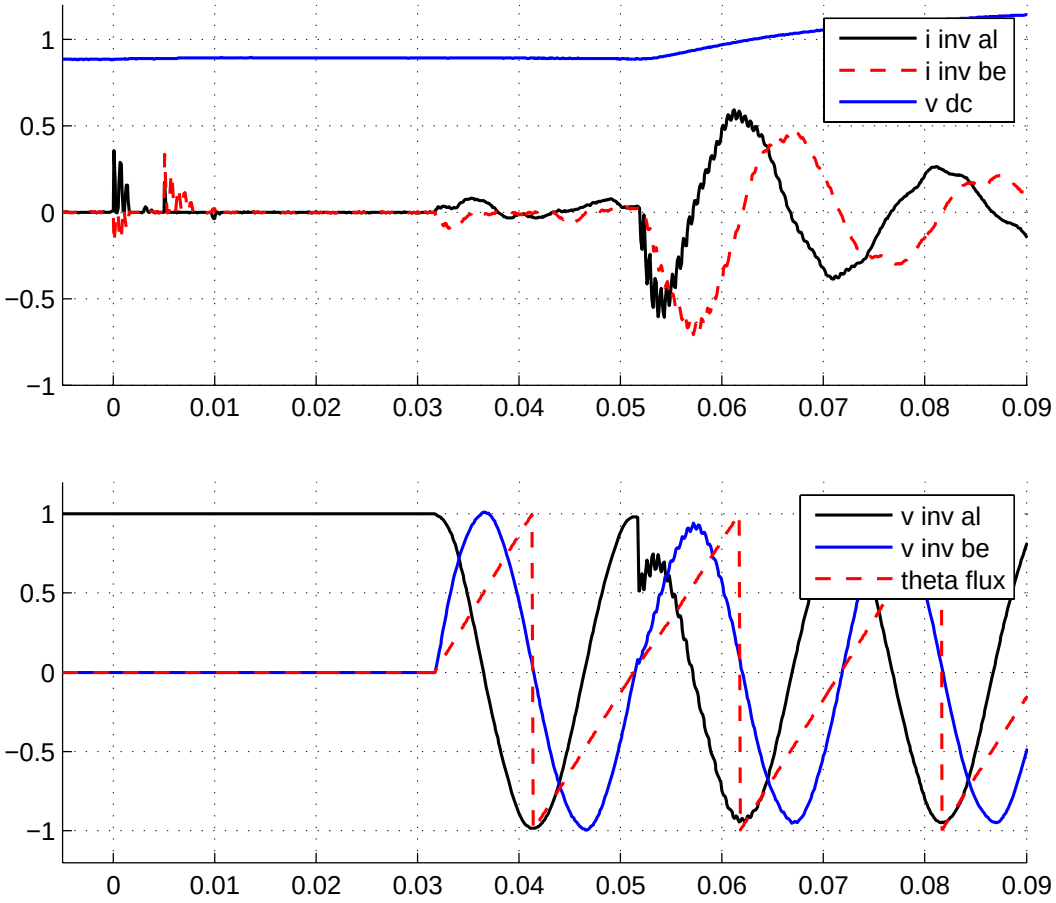

Figure 5.2: Initial start of the converter with sampling. The inverter filter is LC type which is prone to oscillation and those are visible during sampling

In Figure 5.2 at the time index of 0.032 *s*, the estimated grid voltage angle should be zero. The estimation is based on current pulses visible on the upper part of Figure 5.2 at time 0 and 0.005 *s*. At time index of 0.032 *s* the modulator is enabled with initial value of $v_{ref,d}$=1, $v_{ref,q}$=0, the flux model is initiated as well. From 0.032 *s*. the reference currents are set to zero (for only one period) in order to not increase the possible inrush current. Between 0.032 *s* and 0.052 *s* some current is flowing (<0.1 *p.u.*) and during this time the flux model is fully initialized. After one period the dc-link controller is enabled (0.052 *s*) and the active current is visible which is required to charge the dc capacitor to the reference value. The analogy from Figure 5.2 can be directly applied in Figure 5.1, the difference is only use of L filter.

5.1.2. Synchronization without sampling or initialization for balanced voltage condition

For this experiment a balanced input voltage is used together with single frame controller depicted in Figure 4.11. With the proposed flux model it is shown that synchronization can be made without knowing the voltage vector position and the flux model is initialized to zero. During start-up the modulator duty ratio for all three phases is set to 50 %. Only few consequent switching cycles are required for the proposed flux

model in order to output the correct angle. After short time the control converges and the flux model is fully initialized. The disadvantage of this synchronization is that the dc-link voltage is boosted slightly (in the experiment around 15-25 %). Usually the dc-link controller is disabled during start-up, to limit the *d*-axis additional inrush current. The reactive reference current is set to zero as well. The advantage of this method is instantaneous grid synchronization and the flux model internal variables (x_{n-1} and m_{n-1} in (3.21)) can be zero.

The synchronization is initially performed only in one reference frame and after some time the negative frame controller could be activated. This applies either for synchronization with pre-sampling or without.

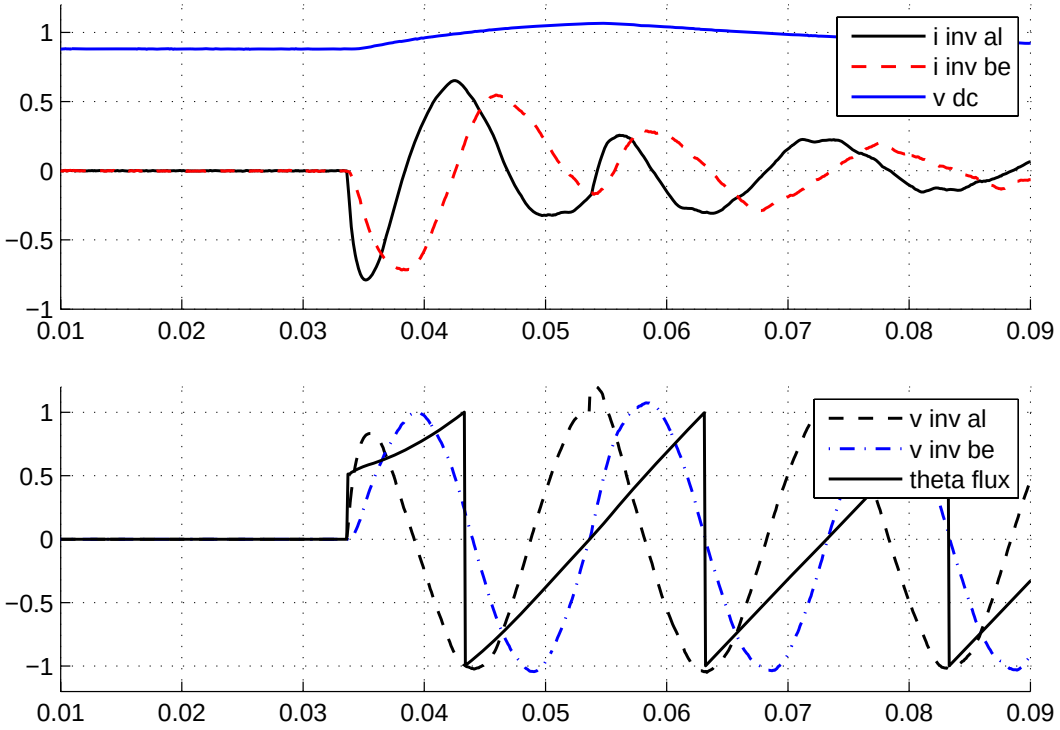

Figure 5.3: Synchronization to the grid without pre-sampling. Visible large current transients

In Figure 5.3 the modulator is enabled at 0.034 *s*, the initial boost of the dc-link voltage is due to the initial duty ratio set to 50% (S_a=S_b=S_c=0) and the fact that some cycles are needed for algorithms to converge. In order to make the action of the dc-link controller visible, the reference dc voltage is set as low as 0.9 *p.u.* and it's enabled at 0.053 *s* (after 20 *ms* from point where modulator is enabled). The per-unit system is in Appendix B.

5.1.3. Synchronization without sampling or initialization for unbalanced voltage condition

The objective is to start the converter with a full model of dual virtual flux with unbalanced input voltage without initialization or pre-sampling. The control is depicted in Figure 4.10. The main difference between this strategy and single frame strategy

introduced in the previous section is that the sequence separation blocks are included. Those blocks are needed for virtual flux and inverter current calculation. Those sequence separation blocks introduces phase lag, which in this case of starting the converter may be unacceptable. The orientation angles could have significant errors which could lead to converter over current. With specific parameters for the positive and negative frame current controller the inrush current is kept well below rated current enabling start of the converter instantaneously. Two cases of different current controller parameters are depiction in Figure 5.4 and Figure 5.5. The slow controller tuning ($K_{p,pos}$=0.6, $K_{i,pos}$=10, $K_{p,neg}$=0.6, $K_{i,neg}$=5) in Figure 5.6 causes a situation close to converter tripping (1.41 *p.u.*). The faster controller tuning in Figure 5.5 ($K_{p,pos}$=1.6, $K_{i,pos}$=20, $K_{p,neg}$=0.8, $K_{i,neg}$=10) lead to inrush current below 0.7 *p.u.*

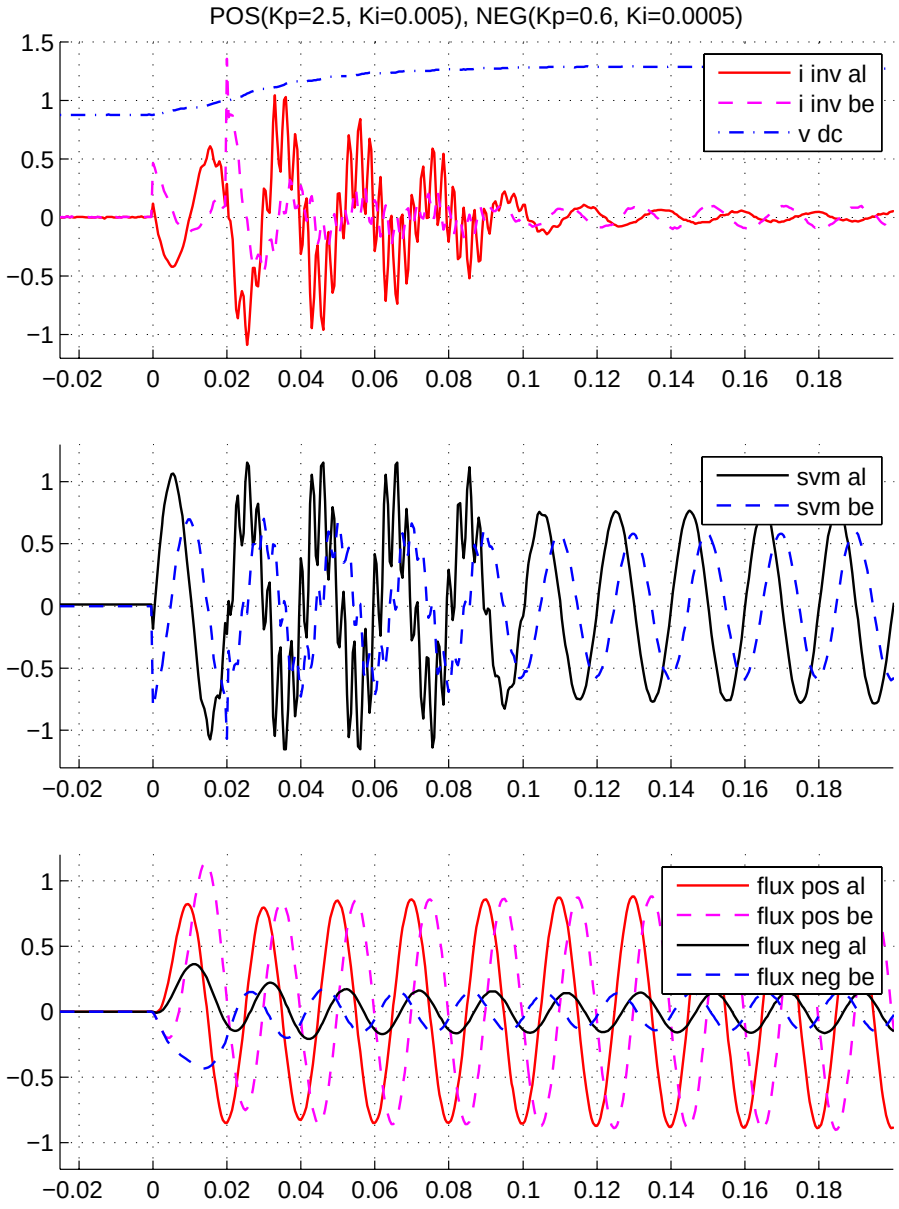

Figure 5.4: Synchronization with dual frame current controller when the active damping circuit is disabled at 0.02 s

The virtual fluxes shown at the bottom are not affected by the current oscillations.

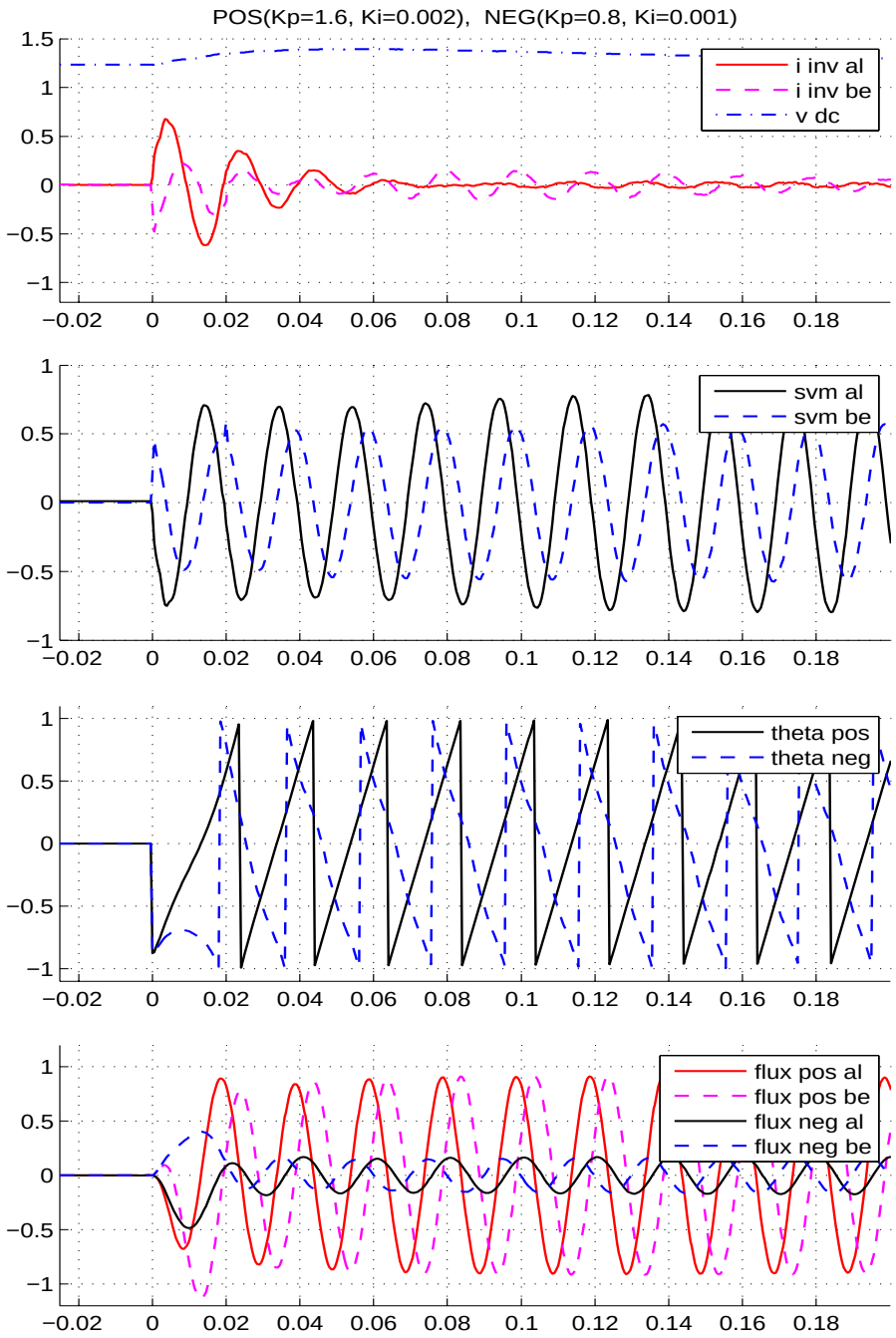

Figure 5.5: Influence of the current controller parameters for the start-up inrush current. The dual current controller is tuned with higher gains

From top to bottom: inrush inverter currents, space vector modulation duty ratio, positive and negative angles produced by the flux model, components of the virtual flux.

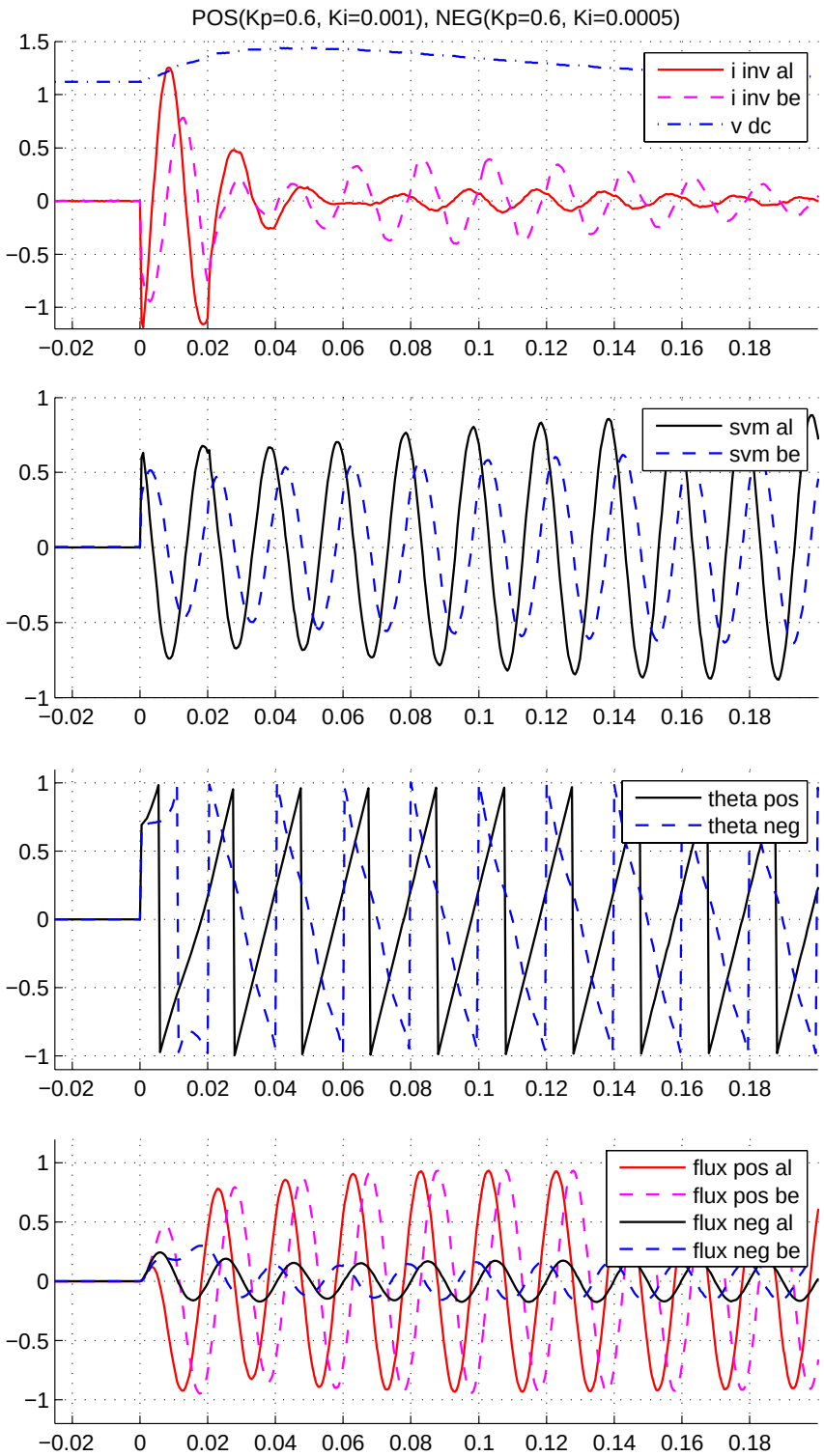

Figure 5.6: Influence of the current controller parameters for the start-up inrush current. The dual current controller is tuned with lower gains

The sub figures explanation is the same as on Figure 5.4.

Experimentally it was found that for positive sequence current controller proportional gain K_p of above 0.6 the converter started normally and any value below result in over-current trip. The maximum value of K_p for which the converter will not trip without active damping is 2.5. Increasing the gain more doesn't result in lower inrush current. The integration part does not play such an important role. The K_p for negative sequence should be below 1 as any higher value will cause trip, and can be as low as 0.1.
At Figure 5.2, Figure 5.3, Figure 5.5 the active damping based on lead-lag method is used. Disabling it will not cause converter trip but the effect will be similar to that in Figure 5.4. Figure 5.4 it is shown that the virtual fluxes components are not influenced by the current oscillations. This is due to inertia character of the sequence separation algorithm and virtual flux estimator.

The per-unit notation was used in DSP implementation which is in the Appendix B.

5.2. Chapter summary

Presented instantaneous synchronization method under unbalanced voltage proves that voltage sensors can be removed from the system. The operation of converter without voltage sensors is possible by above described method and virtual flux approach. The diagrams show that the inrush current is much smaller when initial sampling of the grid angle is performed. The reason is because the flux and current controller models can be initialized with proper values.
The instantaneous synchronization without initial sampling is also possible but the inrush current is higher. The inrush current value is mostly influenced by the parameters of the current controller. Optimal parameters ensure inrush current below 0.7 *p.u.*

The method with initial sampling of grid angle and flux initialization is more suitable for grid connected converter.

6. GRID INDUCTANCE ESTIMATION

6.1. Introduction

In recent years the penetration of distributed power generation is increasing, as well as the development of power electronics. In remote areas often it is not possible to connect to a strong grid, the impedance can vary which could lead to different problems. One example is when in close presence of an inverter, varying impedance can cause instabilities in high frequency range, caused by the LCL filter. The inverter LCL filter resonant frequency should be in the bandwidth of the controller. The LCL filter has advantages of smaller components size compared to the L filter but unfortunately the control is more challenging due to resonances. Knowing the grid impedance, also improve dynamic response of current controller in case of rapid changes of power.
Manufactures of inverters for renewable energy are obliged to deliver unity power factor at the PCC. For example in the wind industry usually the low voltage (690V) output from the full size converter is connected to a step-up transformer which is connected to the medium/high voltage line. There are regulations which specify where the unity power factor must be maintained. The best would be if we automatically could know the inductance of the equipment connected after the inverter, so the PCC could be moved away from the grid filter terminals. For example including transformer leakage inductance into the control would cause the PCC to be moved to the secondary side. Therefore it is beneficial to estimate the leakage inductance of the transformer (which is usually small 3...5%) and include in control algorithms. The same applies to the weak grids.
We assume that we know the parameters of the L or LCL filter which is inserted between the inverter and the transformer. In case of LCL filter having knowledge that the converter will be connected directly to the transformer it would be possible to minimize the inductance of L_2 even more. The second (grid) inductor in the LCL filter L_2 does not carry high frequency components and the reason for adding it is to narrow the spread of resonant frequency. Larger L_2 causes that the grid impedance influence is smaller in proportion to the overall inductance and resonant frequency never goes beyond the controller bandwidth.
This Chapter focuses mostly on estimation of the inductances since they are dominant, and have large influence. They are difficult to estimate by steady state methods or involving active power. The resistive part of the grid impedance is easier to estimate since active power and terminal voltage in steady state can be used with different current levels.

There are many methods to measure grid impedance by dedicated hardware and software. The inverter is not such a trivial platform for measuring grid inductance, the DSP already has computational tasks to perform, and the inverter has a reduced number of sensors.

6.2. Existing impedance detection methods

Various methods can be used for line impedance measurement; normally they employ special hardware devices. Precise acquisition of voltage and current is performed which follows the mathematical calculation to obtain the impedance value. In literature two kind of methods exist: passive and active.

The passive methods are based on observation of non-characteristics harmonics (line voltage and currents). This method depends on existing background distortion of the voltage. Precise voltage measurement is often not available at the inverter platform, thus this method is not used in practice.

Active methods usually produce "disturbance" of the network, followed by response acquisition and processing. There are many ways to "disturb" the network, therefore active methods further can be divided into steady-state and transient methods [tim2], [tim3], [tar2], [lis4], [lis7].
The methods also can be characterized for estimation of impedance for given frequency (50*Hz*) or calculate impedance characteristics as a function of frequency.

There are some methods [tim3] which inject a high frequency, short duration current signal and based on voltage response the inductance is calculated. Fourier analysis of the voltage is used, which require significant amount of computational power and memory. When a filter capacitor is used (LCL filter) the method by injecting short current pulses can be error-prone, thus often in those publications only an L filter is considered.

6.3. Proposed method

A transient method technique is used to estimate the line inductance. The principle of operation is to inject a reactive current (0.2..0.5 *p.u.*) into the grid for a short time (3..5 periods). The reactive current injected by the inverter causes some action in *d*-axis current controller (CC). The response of the d-axis current controller is analyzed. The d-axis current controller should be responsible only for active power, otherwise it means that some extra coupling between *d*- and *q*-axes exists. If the *d*-axis current (i_d) response is significant in amplitude it most likely means that there is a wrong value of L in the cross coupling of the current controller. However this is only visible during transients, because the PI controller will correct it in steady state.
In other words, we will try to find *L* in the cross coupling for which the response of i_d is minimized in amplitude. For the correct value of *L* the orientation of axes during transient is proper and accordingly *d*- and *q*-axes controllers control the active and reactive power independently. If the value of *L* is mistaken the orientation of axes is "twisted" during transient, and reactive controller control some of the active power as

well, which e.g. can be observed as a dc-link voltage variation. The dc-link voltage will return back to the reference level quickly because it is controlled by PI, dc-link controller.
Another very important factor is the source of angle orientation and synchronization technique. This proposed method is evaluated using Virtual Flux model as a synchronization source. The Virtual Flux (VF) model is simple and has only the *L* parameter to change. It quickly follows the distortions and phase jumps in the grid. As an extra bonus the voltage sensor-less control is still maintained.
It has been observed that with voltage sensor based PLL the results cannot be reproduced in the same way. This is because PLL parameters can be tuned to different hold on time, having the effect of adjusting the PLL "inertia". The place where the voltage sensors were connected also has influence. The virtual flux based orientation has embedded terms of inductance (L_{fl}) and current *i* and it will behave better during transients than voltage sensed PLL, which has no information about the *L* or *i* grid.

6.3.1. The cross coupling term

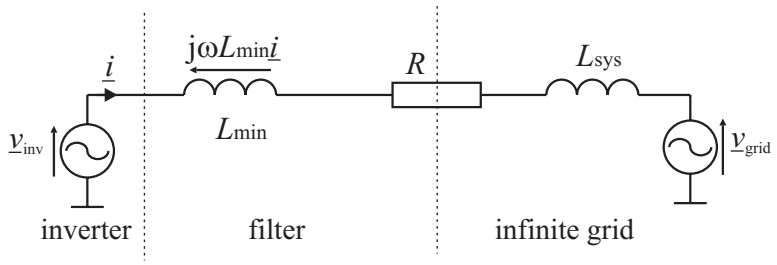

Figure 6.1: Simplified representation of interconnection

The model of the PWM converter in stationary coordinates (α/β) is as follows:

$$\begin{bmatrix} v_{inv,\alpha} \\ v_{inv,\beta} \end{bmatrix} = R\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} + L\frac{d}{dt}\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} + \begin{bmatrix} v_{g,\alpha} \\ v_{g,\beta} \end{bmatrix} \tag{6.1}$$

After transformation to synchronous reference frame (d/q) the equations are:

$$\begin{bmatrix} v_{inv,d} \\ v_{inv,q} \end{bmatrix} = R\begin{bmatrix} i_d \\ i_q \end{bmatrix} + L\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \end{bmatrix} + \omega L\begin{bmatrix} -i_q \\ i_d \end{bmatrix} + \begin{bmatrix} v_{g,d} \\ v_{g,q} \end{bmatrix} \tag{6.2}$$

The term $\omega L i_d$, $-\omega L i_q$ in equation (6.2) is called the cross coupling.
The active and reactive power is given by

$$p = \frac{3}{2}\mathrm{Re}[\underline{v}\cdot\underline{i}^*] = v_\alpha \cdot i_\alpha + v_\beta \cdot i_\beta \tag{6.3}$$

$$q = \frac{3}{2}\mathrm{Im}[\underline{v}\cdot\underline{i}^*] = v_\beta \cdot i_\alpha - v_\alpha \cdot i_\beta \tag{6.4}$$

Now it is clear that the cross coupling term in the current controller is appearing from model transformation from stationary(6.1) to synchronous frame (6.2)

6.3.2. Current controller

The current controller which would provide zero error in steady state can be directly derived from the model of the inverter in synchronous frame. A good reference on designing current controller with parameter tuning is the book by Kazmierkowski [kaz1]

The model of current regulator with the model in synchronous frame is shown below.

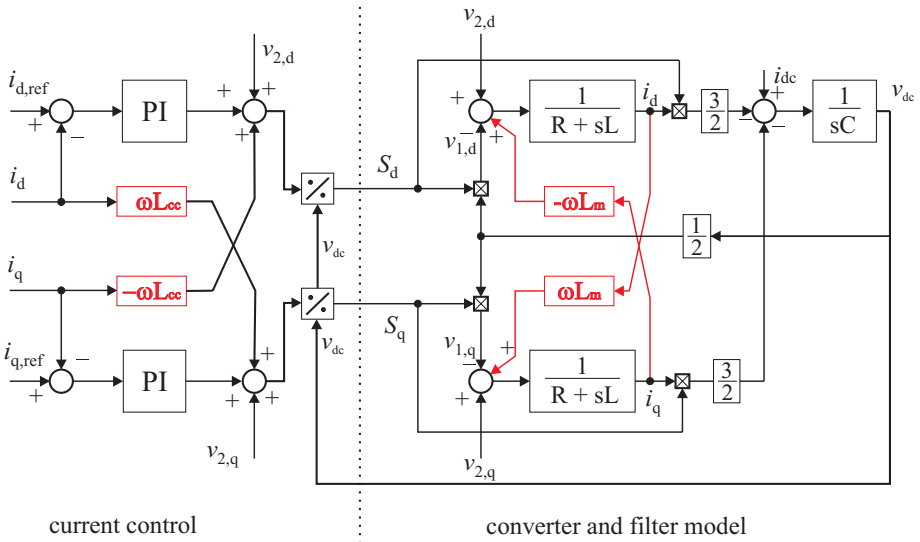

Figure 6.2: Model of current controller with the inverter, filter and grid

From Figure 6.2 it is clear that the cross coupling term submitted to the current controller (L_{cc}) should be as close as possible to the real inductance of the grid and filer (L_m - model inductance). The L_m inductance composes of known filter inductance L_{min} and unknown inductance of the real grid or power system L_{sys}.

$$L_m = L_{\min} + L_{sys} \tag{6.5}$$

The PI controller can be described as transfer function in the form of proportional gain K_p and time constant $T_{i,}$, where $T_i = K_p / K_i$.

$$PI(s) = K_p + \frac{K_i}{s} = K_p \frac{1 + T_i s}{T_i s} \tag{6.6}$$

In our consideration we also do not measure the voltage feed-forward $v_{2,d}$, $v_{2,q}$ which is used in current controller model. This is however a minor obstacle, since in steady state and for balanced grid the PI regulator will correct it. In case where the amplitude of voltage is changing rapidly then the feed-forward would speed up the settling time (supporting the integrators), and the measurement would be needed. It has been observed, that when capacitor voltage is unbalanced then the feed-forward term (in synchronous frame) is distorted. The distortion is usually 100 *Hz* oscillations from the negative sequence. In this situation the single frame controller is not capable of rejecting that signal anyway and the output current is distorted. Thus in unbalance case the voltage feed-forward is not giving any benefits.

In case when we change the direction of i_q with large amplitude we introduce disturbance to our controller which is not able to reject it during the transients. This introduces distortion in *d*-axis which is shown below. The importance of having a correct grid inductance in the control system is illustrated in Figure 6.3. A step of 0.5 *p.u.* is applied for *d*-axis current reference. The same results would be achieved perturbing the *q*-axis current. The mismatch in *L* between model and current regulator is large for better visualization.

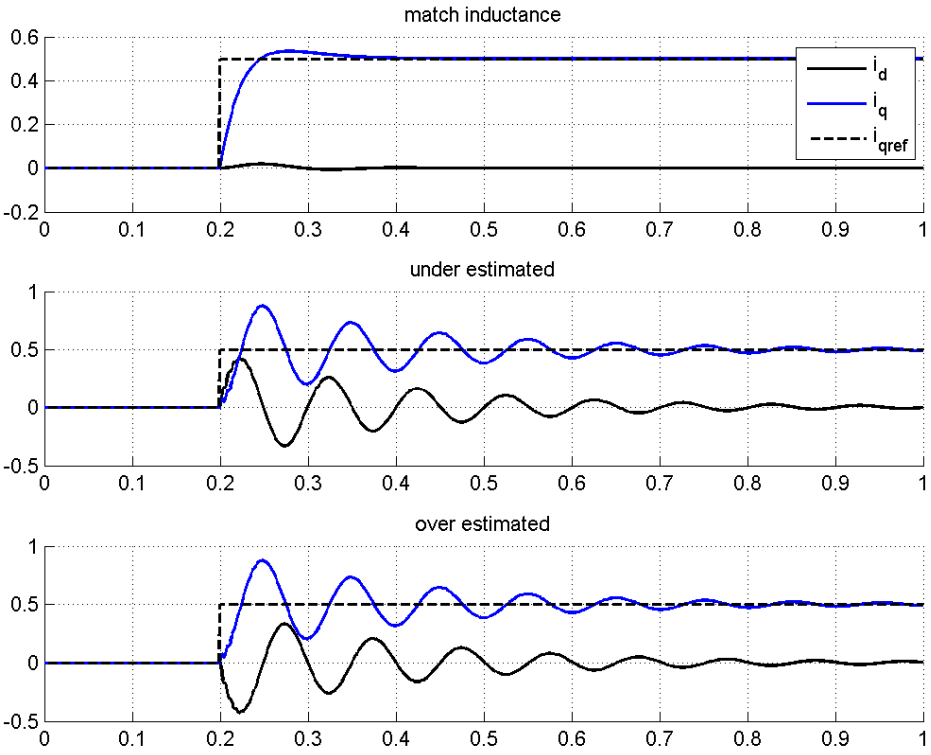

Figure 6.3: Simulated different responses of i_d and i_q dependent on the cross coupling L value in current controller

In the middle and bottom of Figure 6.3 there is over or under compensation of L_{cc} in the current controller. It is a result of L_{cc} in the controller not adequate to the real

inductance of the system and filter (L_m). This configuration could lead to stability problems. In this case the reference angle is distorted and active/reactive current controllers are not controlling proper axes.
The top of Figure 6.3 present the correct response, without overshoot, which means that the inductance used in the cross coupling is the correct estimate of infinite grid inductance. (L_{cc}=L_m).

6.3.3. Dc-bus controller

The dc-bus controller also has influence on performance of this method. The task of dc-bus regulator is to keep the dc voltage as close or equal to a given reference value. The input to the regulator is the voltage dc difference and the output is the active current reference i_d. The amount of the current needed to charge/discharge the capacitor to the desired reference value can be found by the energy equations of the dc bus capacitor. Initially the time constant used for the dc-bur regulator based on the equations:

$$T_i = 8\left(T_{DSP} + T_{PWM}\right), \qquad K_p = \frac{3V_{dc,ref,pu}C_{DC}}{16\left(T_{DSP} + T_{PWM}\right)} \tag{6.7}$$

These equations based on symmetric optimum design and are described in [lis5], [uml1], [gul2]. However in practical experiment they were causing a not acceptable dc-link voltage overshot and the T_i, K_p parameters were changed for slower response. The other tuning criteria can be found in [kaz1]. During simulation it turns out that during transients when $L_{cc} \neq L_m$ dc-link controller gives a higher voltage variation than when L_{cc}=L_m. That leads to the conclusion that when the dc-link controller is tuned to a low bandwidth ("slow response") the possibility to observe lager voltage variations is higher. In the author's opinion this is because the wrong orientation of axes during transients causes the *d* and *q* current controllers to not control their respective axes and the dc-link controller is not able quickly correct the value.

6.3.4. Virtual flux orientation

The integral part in the impedance estimation method is the virtual flux (VF) based derivation of the synchronization angle for Park transformations. The idea is to estimate the output voltage of the inverter from measured dc-link voltage and duty cycles of modulator D_a, D_b, D_c, (6.9)(6.10). The integration of the estimated voltage vector leads to the virtual flux vector of the inverter. The grid flux consists of two components, namely converter flux and flux related to grid filter, transformer or infinite grid.

$$\underline{\Psi}_{grid} = \int\left(\underline{v}_{inv} - L_{fl}\frac{d\underline{i}}{dt}\right)dt = \underline{\Psi}_{inv} - L_{fl}\cdot\underline{i} \tag{6.8}$$

The virtual flux grid vector is 90 degrees delayed from the real grid voltage vector. Based on this angle the synchronization is performed.

$$v_{conv,\alpha} = U_{DC}\frac{2}{3}\left(D_A - \frac{1}{2}(D_B + D_C)\right) \tag{6.9}$$

$$v_{conv,\beta} = U_{DC}\frac{1}{\sqrt{3}}\left(D_B - D_C\right) \tag{6.10}$$

The grid flux components are calculated from:

$$\Psi_{G,\alpha} = \int\left(v_{conv,\alpha} - L_{fl}\frac{di_\alpha}{dt}\right)dt \tag{6.11}$$

$$\Psi_{G,\beta} = \int\left(v_{conv,\beta} - L_{fl}\frac{di_\beta}{dt}\right)dt \tag{6.12}$$

The grid voltage vector position is:

$$\varphi_g = arctg(\Psi_{G,\beta} / \Psi_{G,\alpha}) + \pi/2 \tag{6.13}$$

The inductance L_{fl} substituted in the flux model is partly responsible for the orientation angle of the controller. Also the place where unity power factor occurs depends on the L_{fl} value. The distributed power system can be thought as a series of impedance connections. By increasing the L_{fl} more than the filter inductance the unity point of PCC moves further into the system, for which the commanded reference current i_q=0.
The overall control system is shown in Figure below.

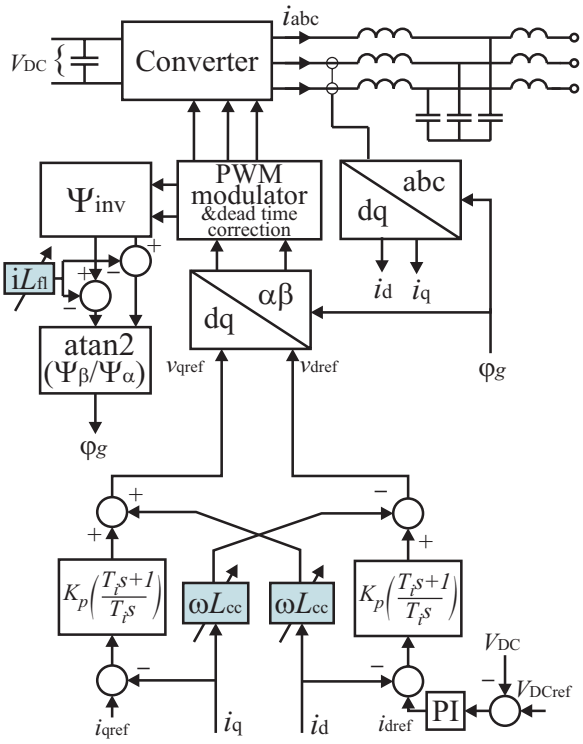

Figure 6.4: Overall block diagram of the control

6.3.5. Usage of LCL filter

In many references for classic current controller design, it is said that the cross coupling inductance should be the value of the filter. This holds true for ideal grid. Normally in case of LCL filter sum of L_1 and L_2 is submitted to the current controller and this is minimal value which must be included L_{min}.
The design of an LCL filter usually assumes that the filter capacitor accounts up to 5..7% of the nominal reactive power. In presented method this reactive current will not disturb the observation.

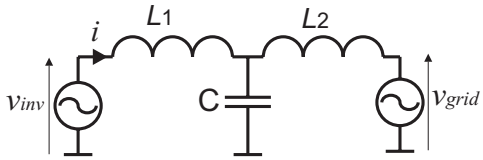

Figure 6.5: Reference model for LCL filter

In a real grid small inductance exist which add to filter inductance. The knowledge of it enables to improve performance.
The result of estimation is the returned value L_{max} which represents the infinite grid inductance together with the filter. This is the maximum value of L_m for which we can tune our controllers, L_{cc} and L_{fl}.
Changing L_{cc} in cross coupling of the current controller from minimum to maximum of the above mentioned value, improve the transient response at PCC .

Similar situation occur when changing L_{fl} from minimum to maximum of above mentioned value, moves the point of PCC with unity power from inverter terminal to the infinite bus.

Also the synchronization angle retuned by virtual flux model is insensitive during reactive power transients; it will only influence the voltage at PCC. It is easy to analyze in Figure 6.6. When reactive current is along C-D path, it will correspond to voltage c-d which is in phase with the grid voltage.

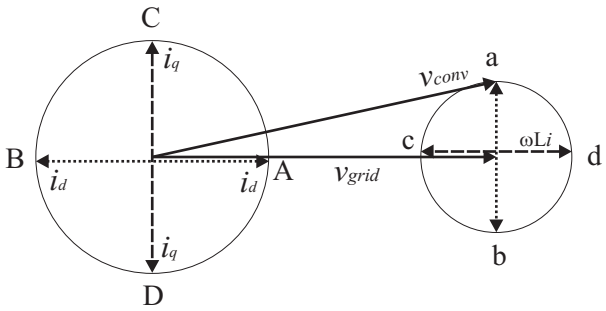

Figure 6.6: Vector diagram of current, grid voltage and inverter voltage

When A-B active power change occurs it corresponds to the a-b path. During transients phase error occurs depending on precision of L_{cc}.

6.3.6. Realization of reactive perturbation method

The method proposed by author is based on commanding reference reactive currents to a capacitive or inductive character for a short time duration. For clarity we assume that the active power is not delivered to the grid and no external current is delivered to the dc-link. The duration of 60 *ms* is enough to observe i_d response which is stored in memory for analysis. The analysis simply involves a peak finding function. Those steps are repeated a few times where the L_{cc} is changed between them. Finding the lowest i_d overshoot means close match of L_{cc} and L_m. The minimum finding function also can be performed directly without storing the response in memory. Only it would be required to store the result of each step in memory.

In general four type of i_d overshoot exist, which are presented in Figure 6.7 as Δi_d .

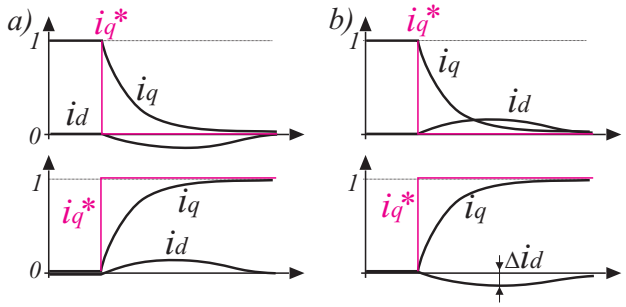

Figure 6.7: Responses of the i_d current for i_q steps from 0 →1 and 1→0.
a) Under compensation of L_{cc} b) Overcompensation of L_{cc}

Experiment results shows that the sufficient step level is from i_{qref}=0.3 *p.u.* For better visualization a linear sweep of L_{cc} is performed in small steps. The changes in L_{cc} are made with 0.2 *p.u.* steps, starting from 0.6 *p.u.* and finishing at 4.0 *p.u.* The known LCL filter inductance is the one unit which physically is has L_{min} value. Starting from 0.6 *p.u.* has no real sense as we know that the included inductance is larger; it is only for demonstration.

After all steps are performed the step with minimum Δi_d, and related to it L_{cc} value is found. The new-found value is called L_{max} and corresponds to an estimated infinite bus inductance expressed in the units of the filter L_{min}. The L_{max} value includes filter value and thus is always larger than one. The L_{max} is expressed in *p.u.* value. The physical grid inductance can be calculated as:

$$L_{sys} = (L_{max} - 1)L_{min} \tag{6.14}$$

During the scanning procedure the L_{fl} value in virtual flux model is set to unity which corresponds to inductance of LCL filter.

Laboratory experiments show that in case of a stiff grid the detected infinite bus inductance is around L_{max}={1.0..1.1} *p.u.*

In case of emulating weak grid by connecting two transformers in series with the converter, the test results in L_{max}=2.5 *p.u.* (so the grid inductance is 1.5 times higher than our LCL filter).

The method is well suited for start up procedures of the converter just after synchronization to the grid. It is also possible to perform this method when active current is applied (online identification during normal operation), but then the added extra reactive current, should not exceed current limits of the converter.
Experiment shows that 3 periods per step is far enough to detect the max and min of the i_d. In the shown results 17 steps were applied, each step L=0.2 *p.u.*

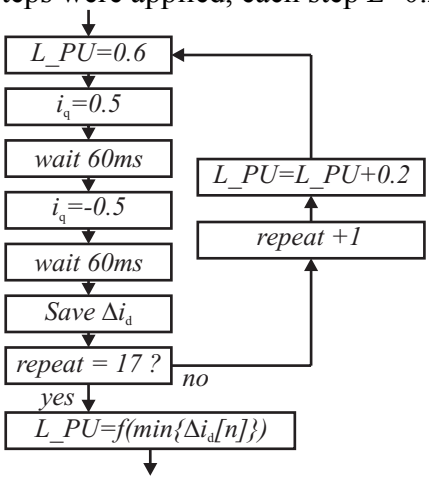

Figure 6.8: Algorithm used for the sweep test

The implementation for laboratory experiment is presented in Figure 6.8.
It assumes wide spectrum of swept inductance, the total detection time is $3_{periods} \cdot 2_{sides} \cdot 17_{steps} \cdot 20\ ms = 2040\ ms$
Significant improvements in detection time is further possible.

6.4. Experimental results

The system is tested in the laboratory on a 20 *kVA* converter using a Texas Instrument TMS320F2812 processor and the LC filter. The test was conducted in the laboratory of Advanced Industrial Science and Technology Institute (AIST), Tsukuba, Japan. At the facility of this laboratory an analog simulator of power system was available. This enables to change the emulated inductors effortlessly with the press of the button. Table below shows more details concerning inverter parameters.

Table 6.1: Parameters during experiment

line to line voltage	230 *V*
rated line current	30 *A*
dc-link reference voltage	1.4 *p.u.* or 455 *V*
filter inductance	800 μH
filter capacitance	25μF capacitor in delta
commanded reactive power step	±0.7 p.u
switching frequency	10 *kHz*
extra inductor emulating weak grid	3 *mH*
dc-link controller parameters	K_{pdc}=7.5, K_{idc}=11.5

For emulating a weak grid a 3 *mH* three-phase grid emulator inductor is inserted in series between filter and the grid. For so called strong grid condition the converter filter is directly connected to the grid.
The K_p, K_i, L_{cc} abbreviations under figures relate to the parameters of the current controller proportional gain, integral gain, and cross coupling inductance, respectively.

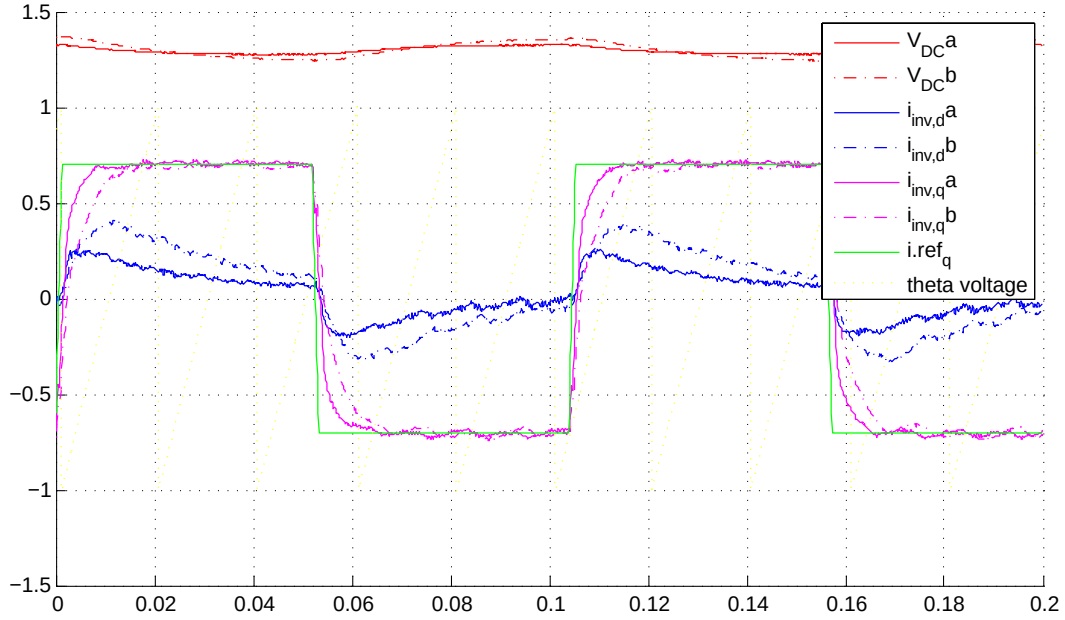

Figure 6.9: Weak grid condition, L_{cc}=1, i_d variation visible (underestimation) a) (solid) K_p=0.6, K_i=5, b) (dotted) K_p=0.3, K_i=1

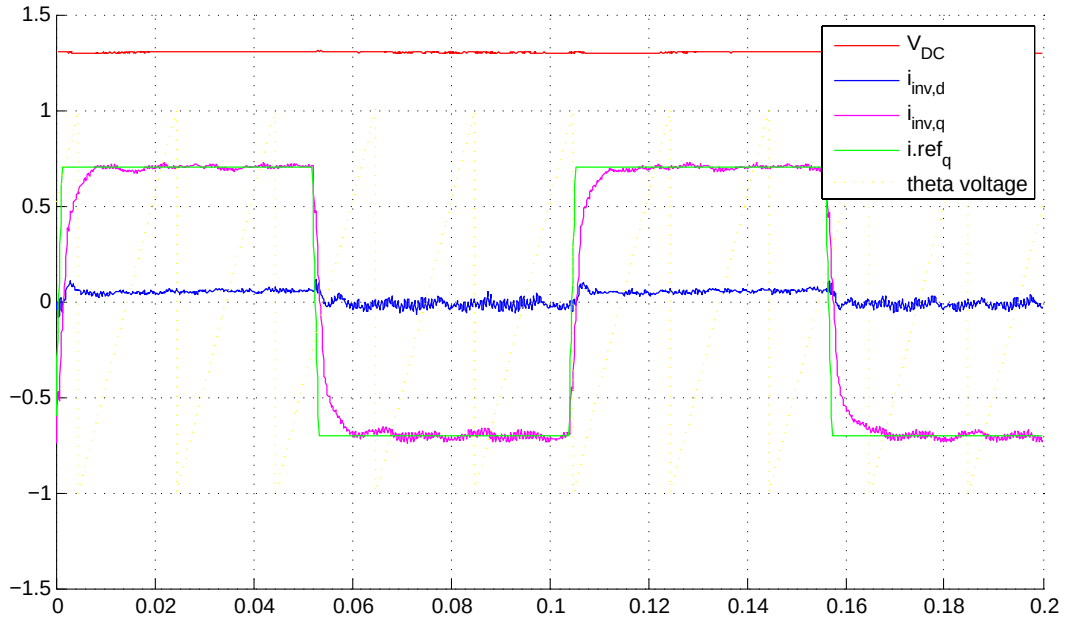

Figure 6.10: Weak grid condition, L_{cc}=4, K_p=0.6, K_i=5, Match between grid and controller inductance. i_d variation minimized.

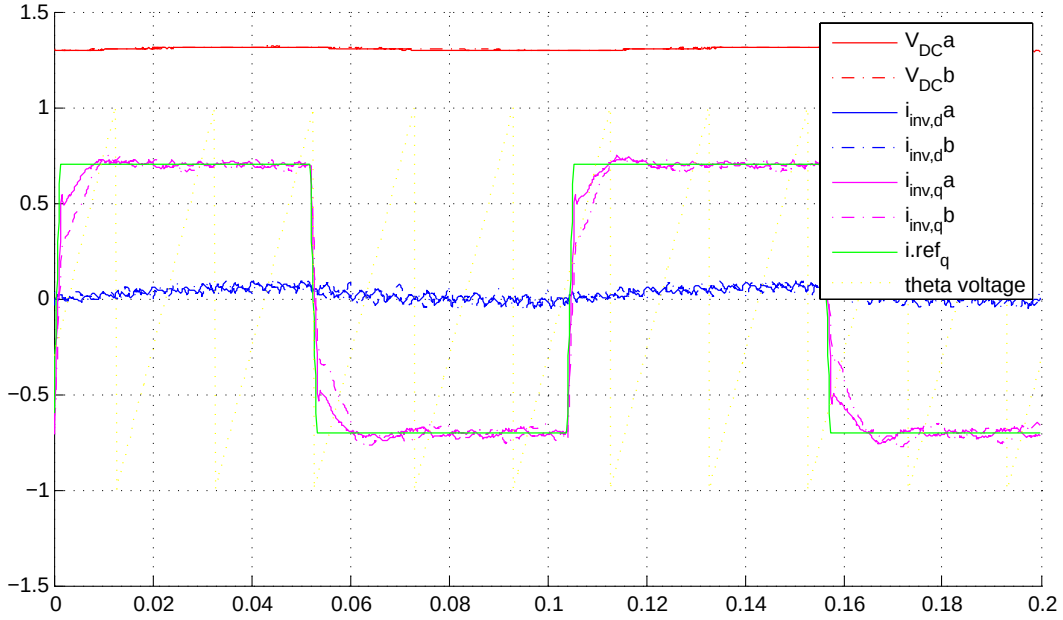

Figure 6.11: Strong grid condition, L_{cc}=1, i_d variation minimized due to inductance match a) (solid) K_p=0.6, K_i=5, b) (dotted) K_p=0.3, K_i=1

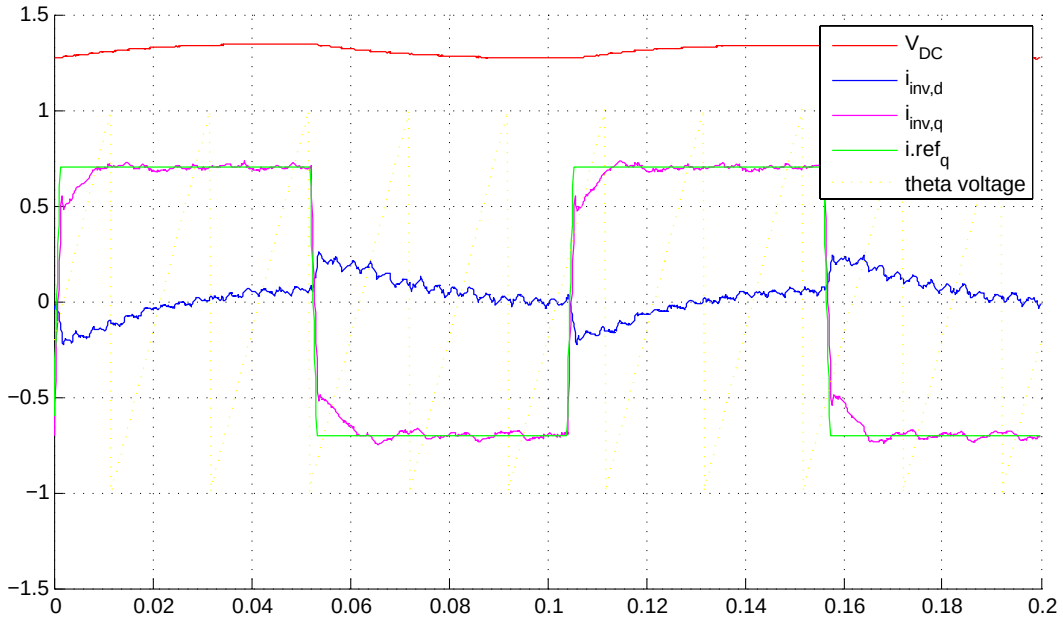

Figure 6.12: Strong grid condition, L_{cc}=4, i_d variation exist due inductance mismatch (overestimation), K_p=0.6, K_i=5

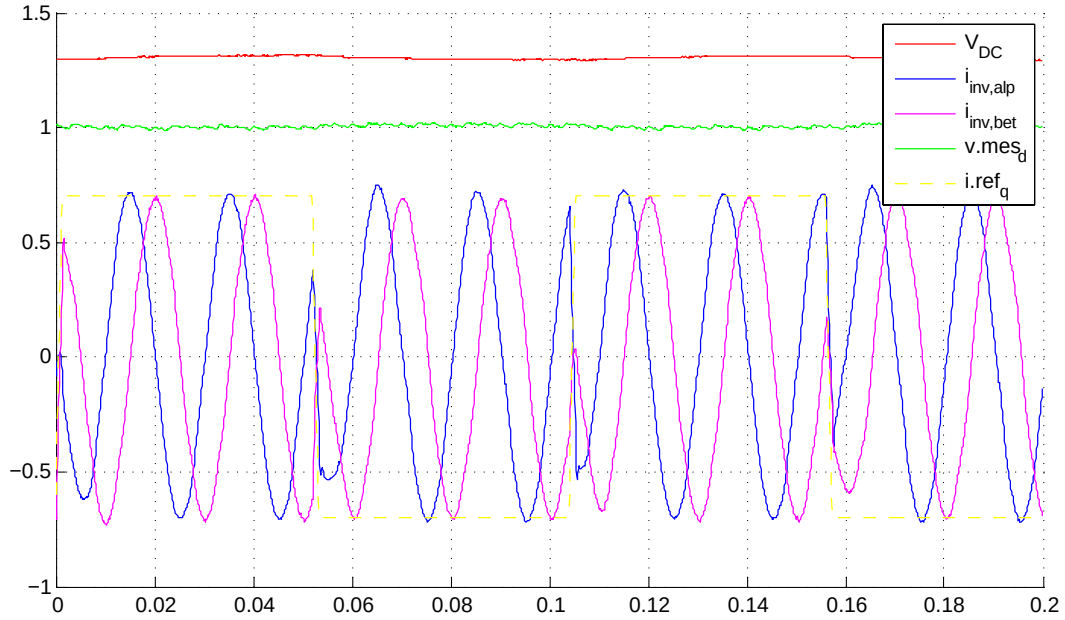

Figure 6.13: Transition of the inverter current (in alpha beta) during pure inductive and capacitive mode of operation. The current controller was used without feed-forward voltage. 0.7 p.u. x 30 *A* = 21 *A* rms

6.4.1. The sweep test results

For the sweep test the same converter and DSP are used. The inductor in the LC filter is changed to 1200 μH and 18 μF capacitor connected in delta. The dc-link voltage reference is set to 1.5 *p.u.* or 488 *V* for rest of the experiment. The commanded reference reactive current during experiment is set to ±0.8 *p.u.* for better visualization of the curves.

Two cases are investigated.

Strong grid - the converter is directly connected to the grid through LC filter (1.2 *mH* = 1 *p.u.*=$L_{\min}$).

Weak grid - between converter and grid an extra inductance of 1.8 *mH* is inserted.

Because a LC filter is used which could lead to oscillation and tripping of converter, an active damping function is used. The active damping function is based on lead-lag compensator [bla1] and is directly implemented in *C* language software like the rest of the control.

The sweep test visualizes the process of changing L_{cc} in the current controller.

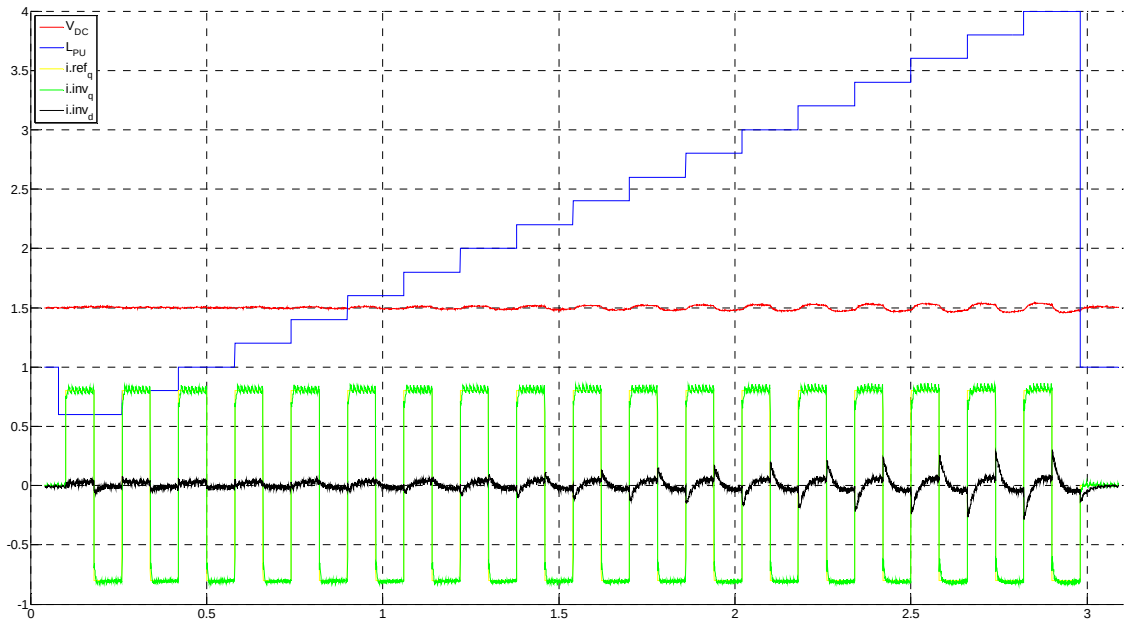

Figure 6.14: Strong grid condition - laboratory measurement results. The smallest variation of dc-link voltage and i_d appear around 1 p.u of L_{cc}, This means that the grid inductance is nearly zero (which is confirmed, because the main supply transformer for the laboratory is very near)

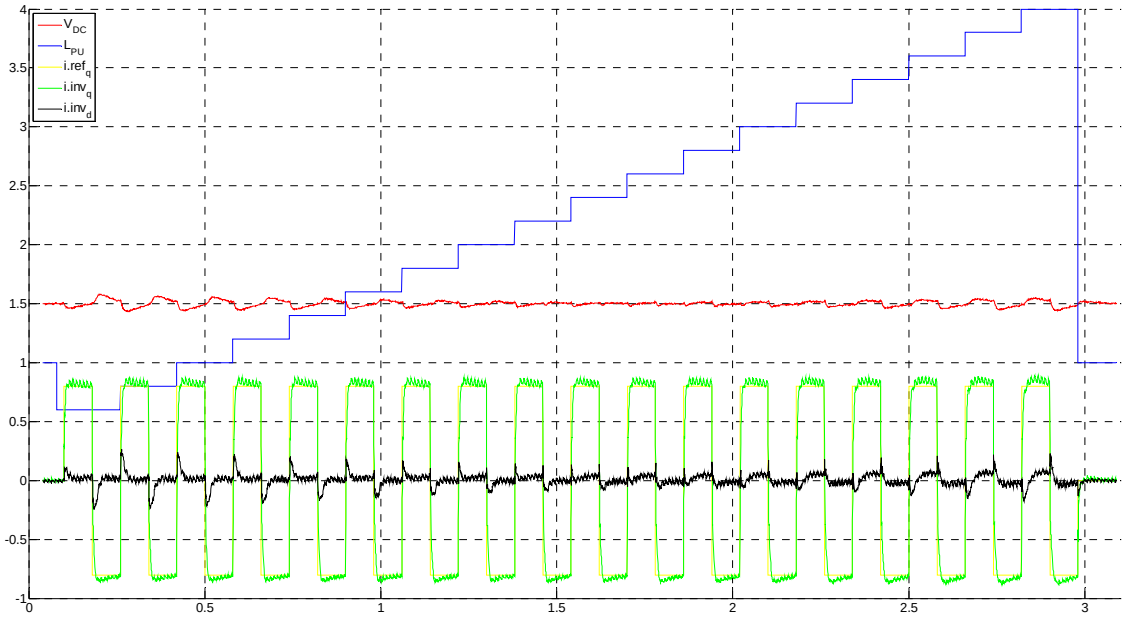

Figure 6.15: Weak grid - laboratory measurement results. The variation of dc-link voltage and i_d current variation are the smallest for inductance (blue line) around 2.4 to 2.6p.u. The total inductance seen from the converter terminals into infinite bus is (2.5 p.u.)·(1.2 *mH*)=3 *mH*. The grid and transformer inductance is 3 *mH*-1.2 *mH*=1.8 *mH*

6.5. Chapter summary

An estimation algorithm of distributed inductance is presented based on virtual flux sensor-less approach. Accuracy of 5 % is achieved in laboratory setup when the grid inductance is significantly higher than filter inductance (weak grid). Exact estimation in the case of strong grid is error prone. Stability and dynamic performance of controller is improved. The algorithm does not require any hardware changes in inverter (cost), all features are implemented in software. This algorithm is able to estimate the impedance when LCL filter capacitor is used.
This algorithm has a large potential for further development. The analytical expression of the overall system could be derived for direct estimation. This however is not a trivial task, the model must include: current controller, virtual flux and dc-link dynamics. If the analytical expression would exist perhaps it would be possible to identify the inductance based on current response of single reactive power injection.

The existing scanning algorithm can also be significantly improved. It should not base on minimum Δi_d searching, but also on direction of i_d. This would minimize the number of steps to just a few. The algorithm could divide the range in half, and then dependent on sign of i_d go up or down with L_{cc}. So the rough estimation would take short time, while more exact estimation would require more iteration.

The laboratory converter is equipped with voltage sensors but does not use it. The synchronization is based on method described in details in Chapter 5.

7. STANDALONE INVERTER OPERATION AND VOLTAGE HARMONIC CONTROL

In this Chapter a stand-alone voltage control is discussed. The method for obtaining sinusoidal output voltage regardless of the nonlinear and unbalanced load will be presented. The resonant controllers are used for selective harmonic cancellation of distortions in the output voltage. The method emulates low output impedance for the higher harmonics thus eliminating the voltage drop over filter inductance when a nonlinear current is draw. The voltage harmonic controller is applied for two kinds of converter topologies: VSI and Z-source. Voltage control of Z-source inverter is presented in Chapter 8. In both cases experimental results are shown.

7.1. Introduction

This Chapter presents a new current sensor-less control scheme for voltage control of VSI with LC output filter; the proposed controller uses a bank of resonant controllers for voltage harmonic control. The proposed control is able to achieve zero steady-state error and selective harmonic compensation. The proposed high performance control scheme can be used in UPS or standalone power generation applications. For the control purpose only ac voltage measurement in required.
Additionally this controller is suitable to use in different paralleling schemes where nonlinear loads must be shared [tul1]. For proper sharing it has the possibility of adjusting the gain of individual voltage harmonics. The harmonic rejection block is also able to operate in a wide frequency range of the fundamental frequency which is required in various sharing methods. The parallel operation and droop control of inverters is not investigated here.
The proposed scheme is fully appropriate for digital implementation of UPS systems where a high quality AC output voltage is important. The diagram block of the proposed controller is shown together with simulation and experimental results. The presented controller shows outstanding performance under nonlinear and unbalanced loads which uses selective harmonic compensators.

The main control objective for uninterruptible power supply (UPS) and stand-alone inverters is to track a pure sinusoidal voltage reference, providing an output voltage without harmonic content in spite of non-linear or unbalanced loads. Several codes and international standards [en1] limit the harmonic content of the output voltage in this

kind of systems. Linear control technique, like PI controllers in stationary frame, has been widely used in the past, however this technique does not comply with the standards. With the aim to reduce the weight, size and cost of the overall system, the LC output filter has been used. Employing an LCL output filter is also possible and is shown in [loh1]. It is well known that these kinds of filters have a resonant peak that can make the system unstable. For all these reasons, many control strategies have been developed to cope with the standards. The list starts with linear PI regulators in synchronous frame [kim1], non-linear controllers based on resonant regulators [teo4], [esc3], [zmo2], [lis6], state feedback controllers [rya1], adaptive controllers [esc4], predictive controllers and repetitive controllers in [esc2].
For long time the majority of controllers used the measured filter capacitor current as a feedback to the controller. The controller presented here does not use the above mentioned sensor – it uses estimation.

7.1.1. System description

The system overview is presented in Figure 7.1. The three-phase output voltages are assumed without neutral wire to be easily decoupled in two independent control variables. The delta-wye isolation transformer can be included giving the natural path for zero sequence currents. The further description can be easily extended to single-phase system or three-phase four wire system.
The effect of DC-bus variation is decoupled in a standard way before the modulator. The measured signals are the DC-link voltage and two phase-to-phase output voltages.
In order to deal with unbalanced and nonlinear loads the positive and negative sequence voltage harmonics must be controlled. We assume no information about the load.

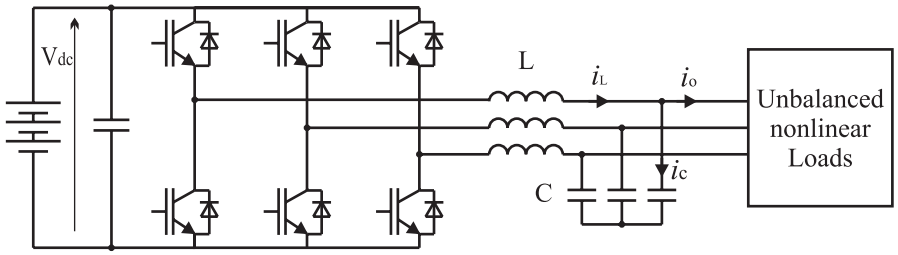

Figure 7.1: Three-phase inverter system with LC output filter

Table 7.1: Names convention used in this chapter.

V_{dc}	dc-link voltage
i_L	inverter/filter current
i_o	load current
i_c	capacitor current
L, C	parameters of the filter
v_{inv}	inverter voltage
v_o	output/load/capacitor voltage

7.1.2. Conventional synchronous frame voltage harmonics compensation

The first idea of harmonic compensation begins in synchronous frame coordinated to the desired harmonic frequency [kim1]. The block diagram of the synchronous frame voltage compensator is shown in Figure 7.2. This type of regulator has been well reported in the literature for three-phase systems, mostly for current control. It is worth to mention that the Park transformation ($\alpha\beta \Rightarrow dq$) in signal processing theory is known as a frequency shifting, and it should be viewed from this perspective. It allows shifting the frequency of the interest into a dc quantity, where the well known dc regulators are used. It should be also observed that e.g. the fifth negative and seventh positive sequence harmonic of 50 *Hz* become a sixth harmonic in synchronous frame.

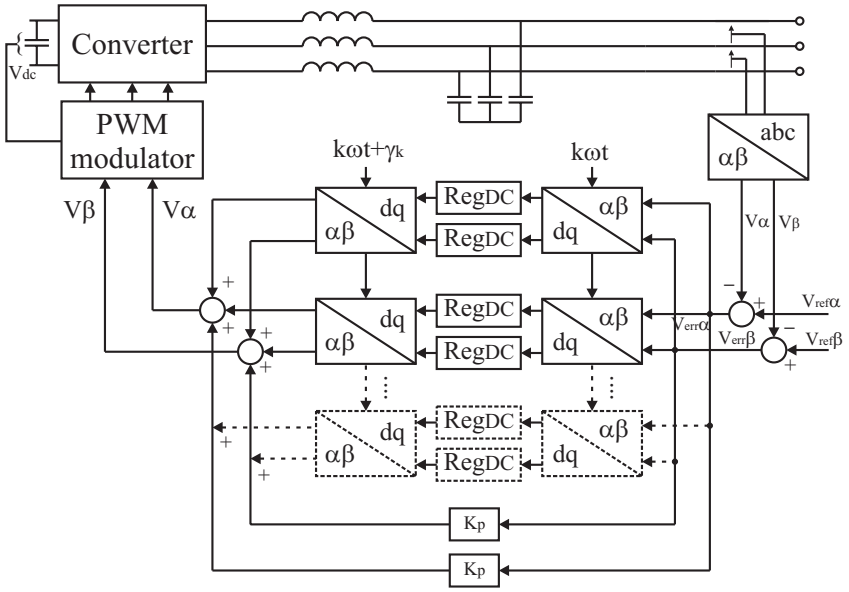

Figure 7.2: Conventional synchronous frame voltage harmonic compensator

The important parameter is the setting of the leading angle γk in Figure 7.2. In the case of UPS with LC filter the γk depends on the *L*/R ratio of filter inductance and often is near zero. For first harmonic the γk should be +90 degrees as the inductance becomes dominant. In order to eliminate given harmonic from the output voltage the control must inject compensating voltage 90 degrees advanced than the current harmonic causing the distortion.

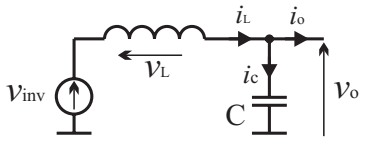

Figure 7.3: Single-phase equivalent of filter output

Let assume that the load current is composed of two harmonics, first and fifth:

$$i_o = I_1 e^{j\omega} + I_5 e^{j\omega 5} = i_{o,1} + i_{o,5} \tag{7.1}$$

The voltage drop over filter inductance is composed of sum of all harmonics:

$$v_L = \sum_{k=1}^{n} \left(i_k e^{j\pi/2} k\omega L \right) = \left(i_{o,1} e^{j\pi/2} \omega L \right) + \left(i_{o,5} e^{j\pi/2} 5\omega L \right) = v_{L,1} + v_{L,5} \tag{7.2}$$

The voltage drop increase as the order of harmonic is higher. The first current harmonic is not causing any distortion, only small drop on filter inductance and resistance. In order to compensate voltage drop of higher harmonics the inverter voltage is:

$$v_{inv} = v_o + v_{L,1} + v_{L,5} = V_{o,1} e^{j0} + \left(i_{o,1} e^{j\pi/2} \omega L \right) + \left(i_{o,5} e^{j\pi/2} 5\omega L \right) \tag{7.3}$$

The corresponding load harmonic current is 90 degrees lagging to the correction inverter voltage. The method of decomposition into separate harmonics easily allows us to do any phase shifting. The disturbing current from the load will match the correcting current from the inverter and there will be no distortion in the output voltage. There also should be added the compensation angle for the system delay which is important for compensation of higher harmonics.

The main disadvantage of using many harmonics compensator is the computational complexity related to synchronous transformation of each harmonic. For each harmonic there is also need to derive accurate synchronous frame reference signal. Another drawback is that scheme is not able to compensate negative sequence harmonics, if only positive sequence harmonics are implemented.

7.1.3. Stationary frame ac compensator – resonant compensator

It is possible to derive stationary frame ac harmonic compensator based on synchronous frame which will achieve zero phase and magnitude error [zmo2], [zmo3]. The derivation is done by frequency shifting property for a stationary PI regulator. Full mathematical transformation can be seen in [zmo2]

$$G_{AC}(s) = G_{DC}(s - j\omega) + G_{DC}(s + j\omega) \tag{7.4}$$

$$G_{dq}(s) = K_p + \frac{K_i}{s} \quad \Leftrightarrow \quad G_{\alpha\beta}(s) = K_p + \frac{K_i s}{s^2 + \omega^2} \tag{7.5}$$

The transient response of the two controllers is identical regardless whether they are implemented in stationary frame as an ac compensator or in synchronous frame as a dc compensator. The transfer function of (7.5) is shown in Figure 7.7 left.

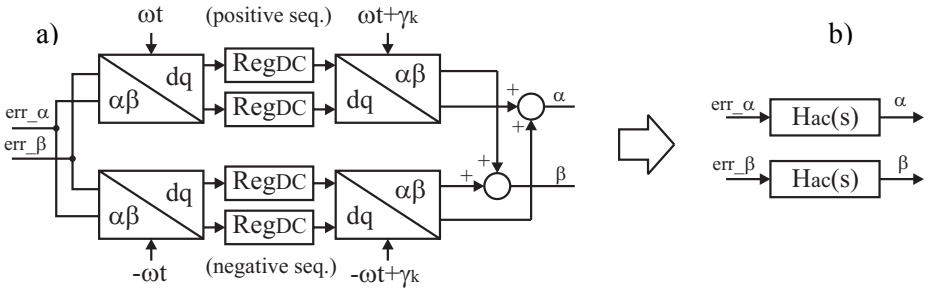

Figure 7.4: a) synchronous frame compensator, b) equivalent compensator in stationary frame

In order to achieve transfer function with characteristic similar to (7.5) but with the phase characteristics shifted by 90 degrees an observation is made. The *s* in the numerator which accounts for the derivative can be removed and replaced with ω to compensate for the amplitude characteristic. In this way a phase characteristics of the new transfer function is lagging compared to the original (7.5). The transfer function of (7.6) is shown in Figure 7.7 right.

$$G'_{\alpha\beta}(s) = K_p + \frac{K_i \omega}{s^2 + \omega^2} \tag{7.6}$$

Now it is possible to access the individual orthogonal components and set the phase characteristic during resonant peak to any ordinary angle γ. The semi-transfer function of the new flexible resonant controller is:

$$H_{ac}(s) = K_i \cdot \frac{s \cdot \cos(\gamma) - \omega \cdot \sin(\gamma)}{s^2 + \omega^2} \tag{7.7}$$

Inserting leading angles of 0 and -90 degrees in equation (7.7) gives respectively:

$$H_{AC\_0}(s) = K_p + \frac{K_i \cdot s}{s^2 + \omega^2} \tag{7.8}$$

$$H_{AC\_90}(s) = K_p + \frac{K_i \cdot \omega}{s^2 + \omega^2} \tag{7.9}$$

The equation (7.8) is the transfer function often used in current control of VSI [teo1]. The time response for a sinusoidal input with constant amplitude of 1.0 for the resonant frequency is shown in Figure 7.5 and Figure 7.6 respectively. For other frequencies than resonant the output amplitude is constants. In Figure 7.5 and Figure 7.6, the change in input frequency is made at the time index of 0.56 *s*, the output frequency remains unchanged and the amplitude is not increasing any more. The obvious difference between Figure 7.5 and Figure 7.6 is that second introduces phase shift of 90 degrees in the output for of resonant frequency.

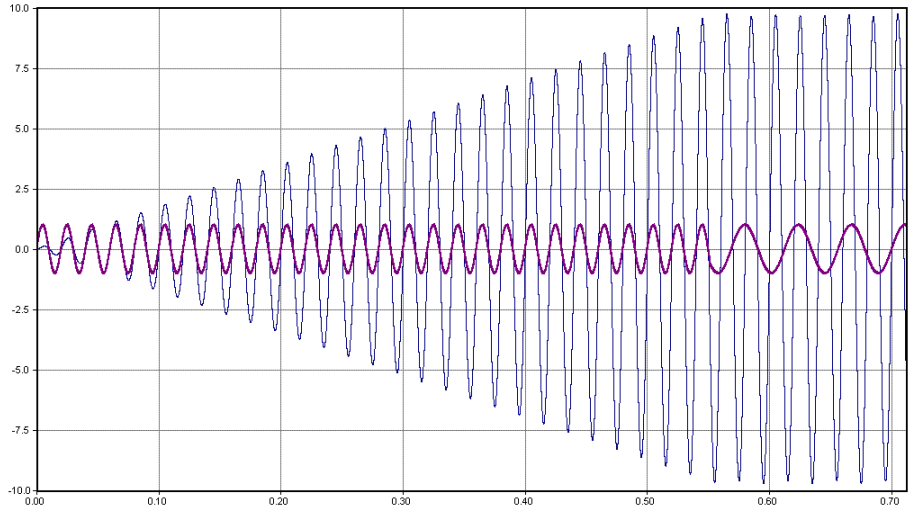

Figure 7.5: Response of transfer function (7.8) for sinusoidal input with constants amplitude of 1.0 and specified resonant frequency

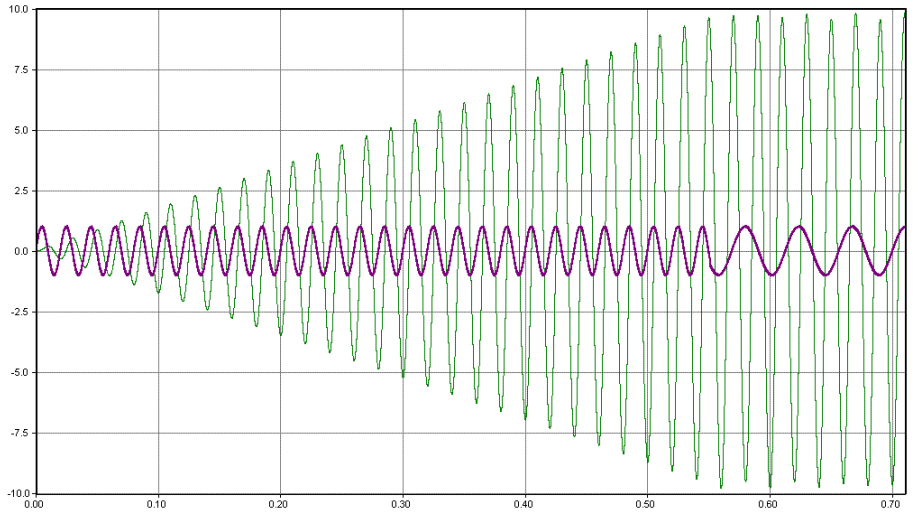

Figure 7.6: Response of transfer function (7.9) for sinusoidal input with constants amplitude of 1.0 and specified resonant frequency

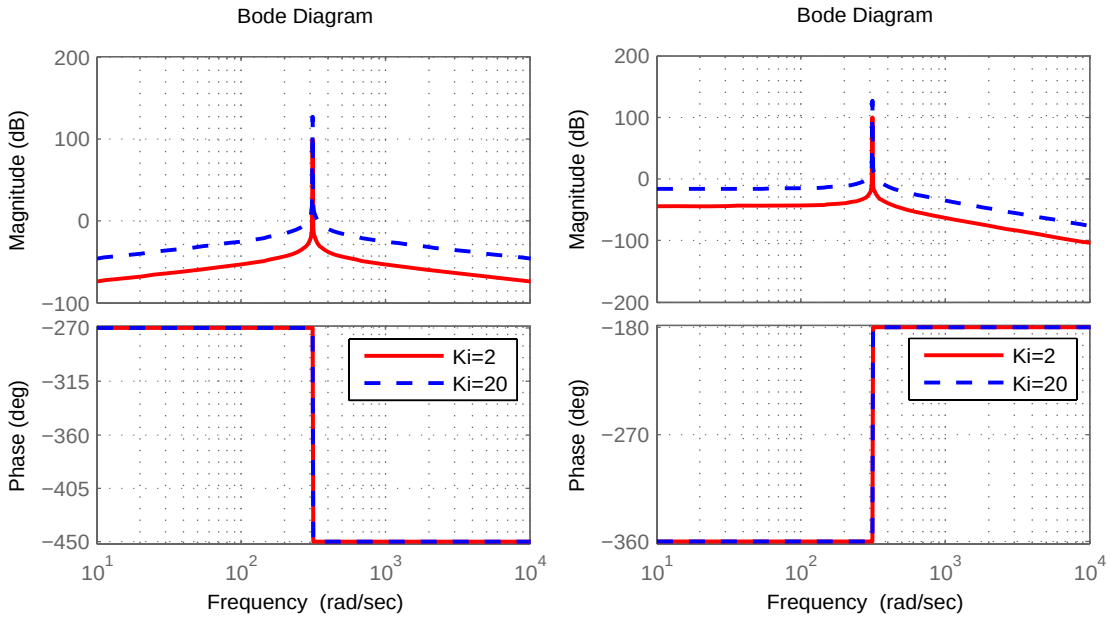

Figure 7.7: Bode plots of the transfer function (7.8) - left and (7.9) – right.

7.2. Control topology

The proposed control topology is depicted in Figure 7.8. The filter capacitor current control is used for harmonic voltage rejection. As an alternative to sensing the capacitor current, a sensor-less scheme is used. It is relevant to use the derivative of the output voltage which is proportional to the capacitor current. Normally the capacitor current contains a large amount of switching noise which can be recognized in the capacitor voltage. The derivative in the digital systems amplifies noises from the input and additionally introduces delay. Higher harmonic order k means larger amplification; $s = j\omega_k$ The derivative delay and system delay can be compensated by adjusting the leading angle of full resonant controller (7.7). Also the natural property of (7.7) being insensitive for any signal (Figure 7.5) excluding the resonant frequency, handles the noisy input signal well.

The system delay is the same for all harmonics, but note that with increased order of harmonic the given leading angle is increasing. For the fundamental harmonic of 50 *Hz*, one sample delay (e.g. 100 μs) is just 1.8 degrees, but for the 11th harmonic it is almost 20 degrees. Only few first harmonics can be compensated with fairly good result without correcting the leading angle for system delay.

The reference for capacitor current $i_{Cref,\alpha}$ $i_{Cref,\beta}$ (7.10) is easily obtained from voltage reference $v_{ref,\alpha}$ $v_{ref,\beta}$ (7.11) by interchanging axes and thus obtaining 90 degrees advanced in reference angle. It can be noted that in the current reference definition, the capacitor value is included, but later on is cancelled out as can be seen in Figure 7.8, avoiding the *C* parameter uncertainty.

$$\begin{bmatrix} i_{C,ref,\alpha} \\ i_{C,ref,\beta} \end{bmatrix} = \begin{bmatrix} -v_{ref,\beta} \\ v_{ref,\alpha} \end{bmatrix} [\omega \cdot C] \tag{7.10}$$

$$\begin{bmatrix} v_{ref,\alpha} \\ v_{ref,\beta} \end{bmatrix} = \begin{bmatrix} \cos(\omega t) \\ \sin(\omega t) \end{bmatrix} \cdot v_{d,ref} \tag{7.11}$$

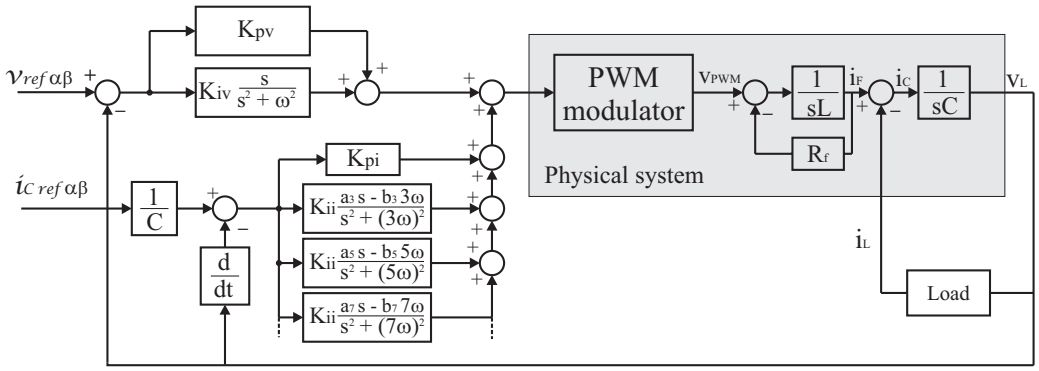

Figure 7.8: Block diagram of the proposed control layout

The use of the derivative of the output voltage in the frequency spectrum gives a signal which in amplitude is proportional to the number of harmonic, thus having natural property of increasing the gain for the higher harmonics. In this case it is desired because it improves detection of the higher harmonic, and the distribution of K_{ii} gain for different harmonic of the capacitor current error can be the same. The coefficients a_k, b_k equals to: $a_k = \cos(\gamma)$, $b_k = \sin(\gamma)$ which are pre-calculated for implementation based on the leading angle and order of the harmonic. The dependence of harmonic order and leading angle is shown in Figure 7.9.

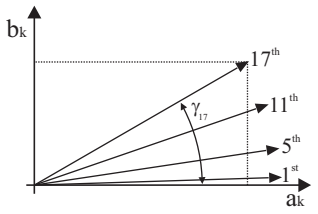

Figure 7.9: Graphical representation of leading angle for specified harmonics and a_k, b_k coefficient

In the simulation 0.031 *rad* is used as value of leading angle for the base harmonic, compensating for the system sampling delay. Since the leading values are known during design, it is worth to pre-calculate them and store in table, thus saving time of DSP by not calling $\sin(\gamma)$ and $\cos(\gamma)$ subroutines.

7.2.1. Discrete implementation

The second order (7.7) transmittance with proportional gain K_p can be represented by state space representation of two integrators as show Figure 7.10.

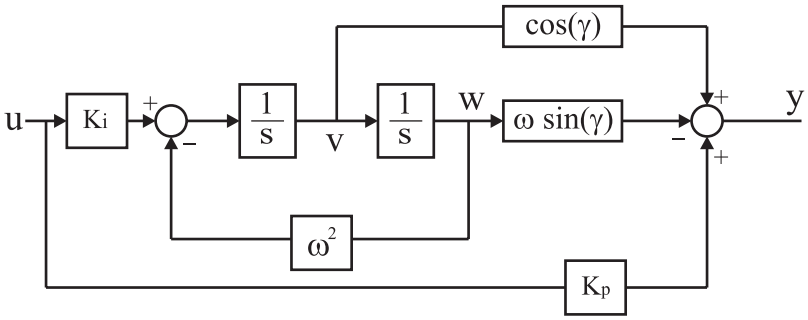

Figure 7.10: Resonant controller as a two integrators with the proportional gain K_p

In order to avoid algebraic loops during the implementation, the integrators must be discretized using different methods, e.g. the first integrator discretized with forward method and second discretized with backward method. The semi-explained code (7.12) contains an implementation of the full resonant controller with proportional term K_p.

$$\begin{cases} v_k = w_{k-1} + T_S \cdot K_i \cdot u_{k-1} - T_S \cdot w_{k-1} \cdot \omega^2 \\ w_k = w_{k-1} + T_S \cdot v_k \\ y_k = u_k \cdot K_p + \cos(\gamma) \cdot v_k - \sin(\gamma) \cdot w_k \\ u_{k-1} = u_k \\ v_{k-1} = v_k \\ w_{k-1} = w_k \end{cases} a \qquad (7.12)$$

Table 7.2: Parameter explanation from (7.12)

T_s	sampling time
K_p	proportional gain
K_i	gain of the resonant controller
u_k	input at a discrete step k
y_k	output at a discrete step k
v,w	intermediate states, see Fig. 8
ω	resonant frequency for given harmonic

For protection purposes it is important to add anti wind-up scheme. The vector sum of harmonic voltage command should not exceed the available dc-link voltage, allowing only specific amplitude of harmonic to be injected. The integration must be stopped when a specific output level has been reach.

7.2.2. Sharing of voltage harmonic in parallel operation

Linear balanced loads can be shared equally by using drop coefficients that make the frequency and the voltage amplitude proportional to the active and reactive power, respectively. The principle of sharing power by droop control is the base for power system operation with different generation sides. Sharing nonlinear and unbalanced loads create voltage harmonics which must be shared as well. Based on available

publications [tul1] it is worth to mention that having the possibility of adjusting the gain of the voltage controller proportional to the amount of delivered VA of that harmonic, a proper sharing of nonlinear and unbalanced loads can be achieved. In various droop methods the output frequency is also varied more than in utility grid, and this controller is suitable for this operation. For example the repetitive control schemes [esc1] are not well suited for wide frequency variation due to an algorithm in which the base frequency is highly related to sampling frequency, instead they shown good performance for constant output frequency, operating as a standalone.

7.3. Simulation results for VSI

The proposed control has been simulated in PSCAD/EMTDC software. The parameters are in Table below.

Table 7.3: Parameters used during simulation

filter inductance	0.75 *mH*
filter capacitance	50 μF
dc-link supply voltage	900 *V*
line to line reference rms voltage	380 *V*
fundamental frequency	50 *Hz*
switching frequency	10 *kHz*
compensated harmonics	3^{rd}, 5^{th}, 7^{th}, 11^{th} and 13^{th}
load	Figure 7.11
sinusoidal modulation without ZSS	Subchapter 2.3.1

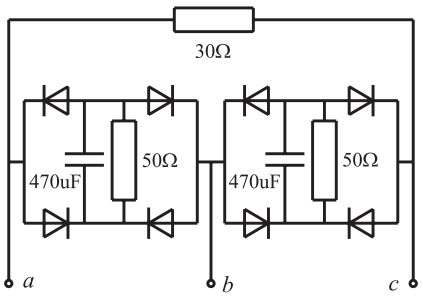

Figure 7.11: Nonlinear, unbalanced load used in simulation

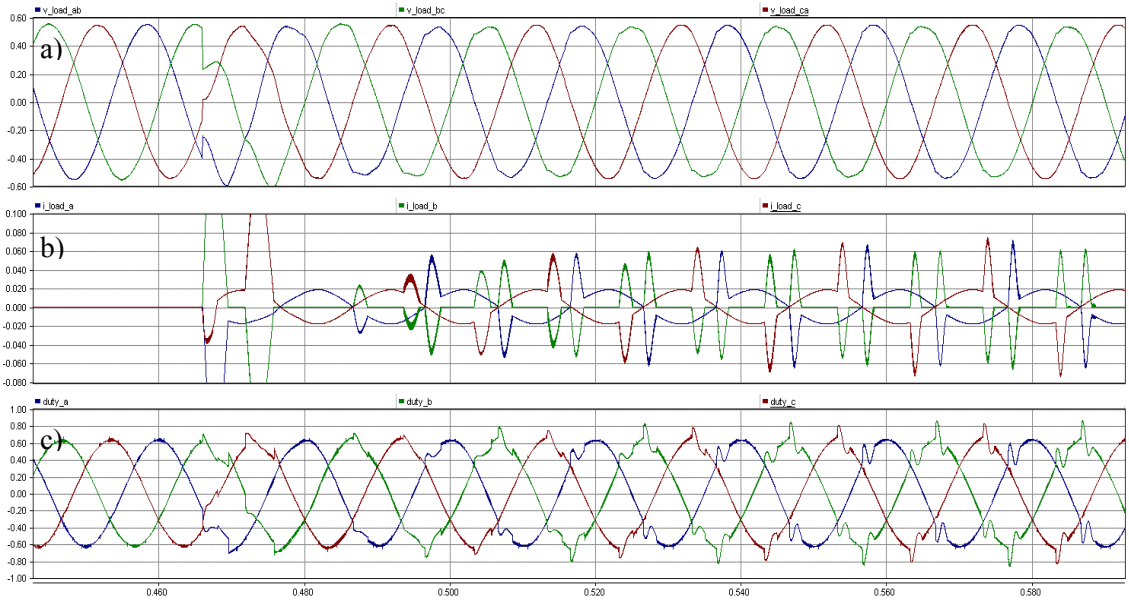

Figure 7.12: Transient response of connecting nonlinear unbalanced load from Figure 7.11 at time index of 0.467 s

In Figure 7.12 and Figure 7.13, a) line to line output voltages, b) load currents, c) output of the controller representing the duty ratio in the three-phases

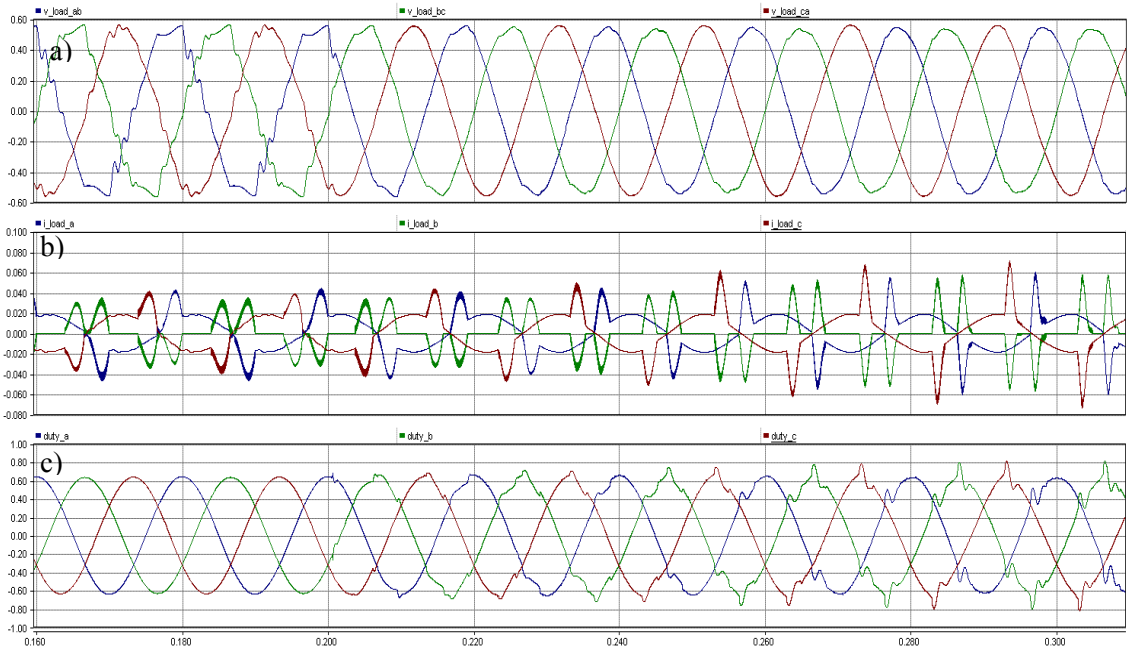

Figure 7.13: Transient response of activating voltage harmonic compensator at the time index of 0.2 s

It has to be observed that in case of nonlinear loads with high crest factor the dc-link voltage must be 10-30 % higher in order to compensate the voltage drop across the filter inductance.

7.3.1. Influence of voltage third harmonic control on modulation

In general control of the third harmonic is not needed as it is zero sequence and cannot influence the line to line output voltage. It has been noted that, in the case where simple sinusoidal modulation without third harmonic is used (like in 2.3.1) adding the third harmonic voltage control (as it is included in Figure 7.8) improves the utilization of dc-link voltage. In other words, the lack of third harmonic in modulation scheme can be compensated by adding 3rd harmonic to the voltage control.
It has been observed that by including the 3rd harmonic voltage controller, the proper waveform set-up time is increased.
To show that dc-voltage utilization is similar to those controls in which 3rd harmonic zero sequence is used, the following tests is made. As a load, three balanced resistors are used. The reference phase peak voltage is set to 320 *V* and the DC-link voltage is to 560 *V*. In modulation scheme without ZS signal in order to get phase peak of 320 *V* the required dc-link voltage must be at least $2 \cdot 320 = 640\ V$. In modulation schemes where 3rd harmonic injection is used the DC-link voltage can be as low as $320 \cdot \sqrt{3} = 554\ V$. In the proposed control there is no third harmonic injection, but the control is still able to fully utilize the dc-link voltage.

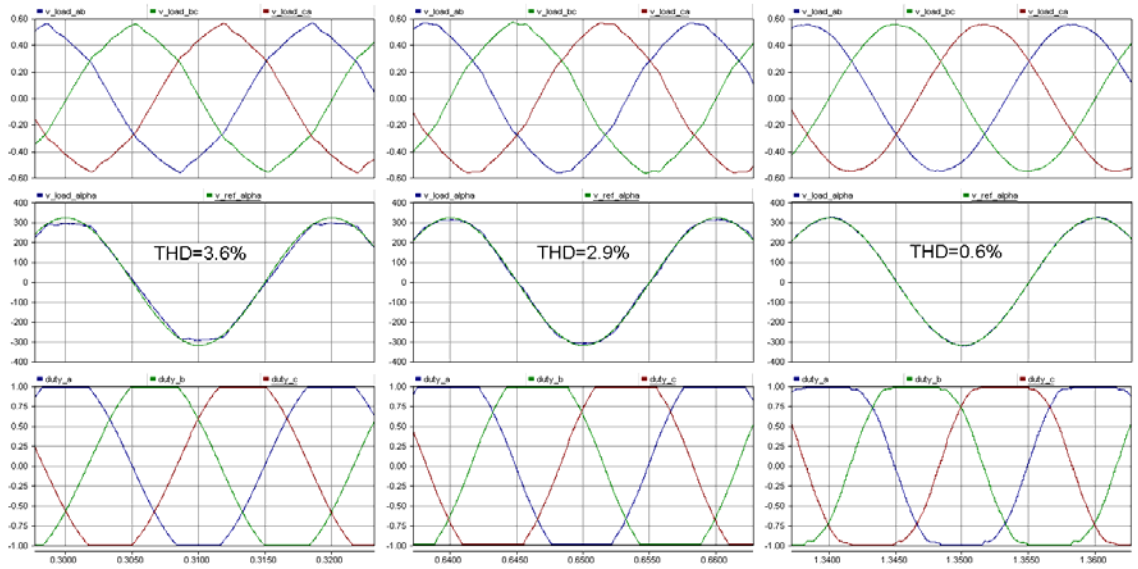

Figure 7.14: Influence of 3rd harmonic compensation for utilization of the DC-link voltage. First row: phase to phase voltage, second: output voltage with reference, third: duty ratio of three phases

Descriptions of the columns in Figure 7.14 is as follows:
First column: no harmonic control, only fundamental voltage as reference THD = 3.6 %
Second column: the first harmonic voltage is enabled, the THD = 2.9 %
Third column: the harmonic compensation (with 3rd) is enabled, THD = 0.6 %.

In all above cases the inverter operates in discontinuous modulation.

7.4. Experimental results for VSI

The control has been verified on 10 *kVA*, three-phase inverter equipped with LC filter and floating point DSP. The experiment was carried out at the Sevilla University of Technology, Spain, laboratory of Power Electronics Group. The actual inverter shown in Figure 7.20 consist of two back to back connected converters. Due to available load limitation it was decided that external 2 *kW* DC power supply will be used. The second inverter was not used.

Table 7.4: Parameters used in experiment

floating point DSP	TMS320VC33.	filter inductance	0.75 *mH*
controlled harmonics	3, 5, 7, 11,13,17	filter capacitance	50 μF
dc-link voltage supply	150 *V*	inv. Rated power	10 *kVA*
ref. phase-phase voltage	50 *V*	K_{pv}	0.4
load resistor	15 Ω	K_{iv}	20
load capacitor	2200 μF	K_{ii}	0.05
dc-link capacitor	3300 μF	K_{pi}	1m

The load is composed of three single-phase rectifiers feeding parallel connected resistors of 15 Ω and capacitor of. 2200 μF The dc-link voltage is 150 *V*, and the commanded phase to phase rms voltage is 50 *V*.

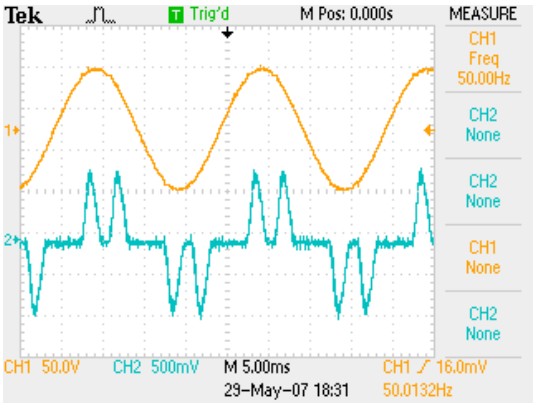

Figure 7.15: Voltage and current of rectifier load. Harmonic compensation is enabled. The one phase is shown, the other phases waveform are similar.

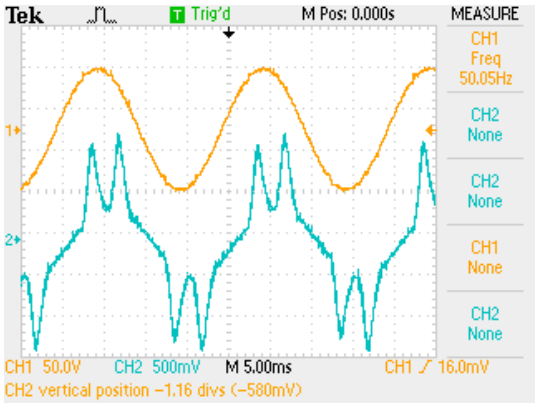

Figure 7.16: Voltage and current of rectifier load with three-phase resistor load. Harmonic compensation is enabled.

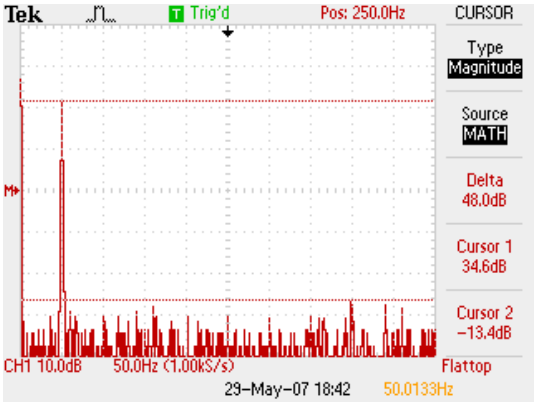

Figure 7.17: Frequency spectrum of the phase to phase output voltage, with voltage harmonic compensation enabled

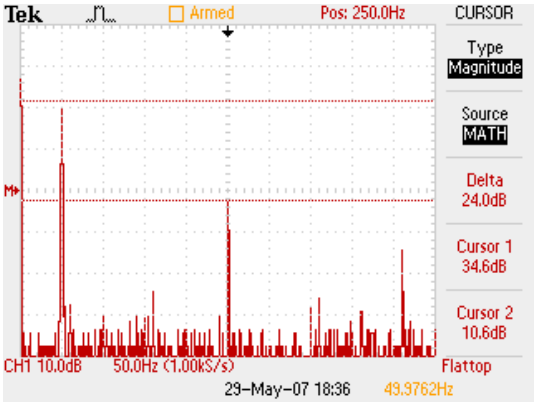

Figure 7.18: Frequency spectrum of the phase to phase output voltage, with voltage harmonic compensation disabled

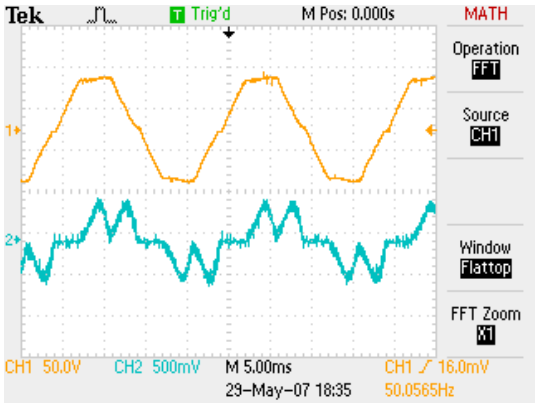

Figure 7.19: Voltages and current for the rectifier load when the harmonic compensation is disabled

For clarity only one of the phase measurements are shown, the other two phases are similar. The scaling factor for current measurement is 10 *A/div*. The measured voltage distortion in Figure 7.15 and Figure 7.16, when harmonic compensation is enabled is 0.8 % THD. In Figure 7.17 the difference between first harmonic and the highest amplitude of unwanted harmonic is 48 *dB*, which is a great result. Figure 7.18 and Figure 7.19 is included for comparisons, when the harmonic compensator is disabled. In this case the measured voltage THD is 7.8 %.

7.4.1. Photograph of the laboratory setup

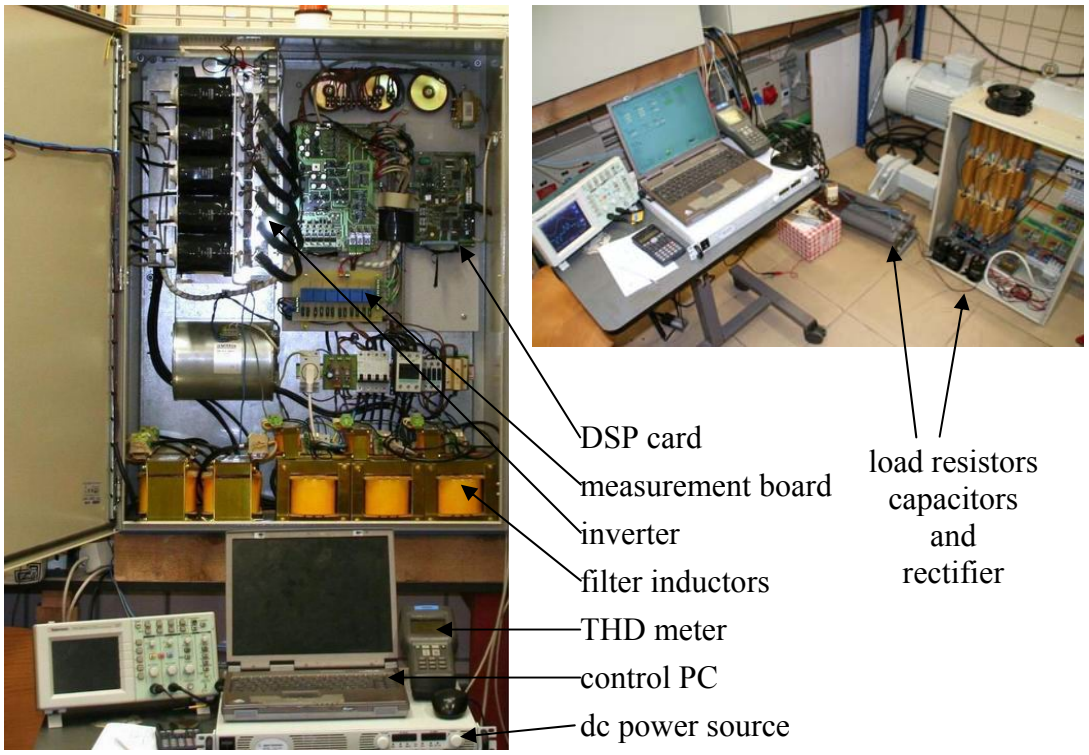

Figure 7.20: The experimental setup

7.5. Chapter summary

In this chapter the estimated filter capacitor current controlled by resonant controller is presented. The RC controller can successfully replace the synchronous *dq*-PI based control method. By using RC it is possible to reduce complexity and computational cost gaining improved harmonic rejection capability. The resonant controller frequency can be tuned on-line to follow the frequency changes required in various droop methods for power sharing. The experimental results show that proposed controller has high performance behavior for any kind of load including non-linear unbalanced loads. The proposed control uses only voltage measurement for control purpose.

8. EVALUATION OF Z-SOURCE INVERTER WITH VOLTAGE HARMONIC CONTROL

This Chapter presents a voltage harmonic control method presented in previous Chapter applied on Z-source inverter topology. Voltage harmonic control enables standalone inverter operation where the output voltage is sinusoidal regardless of the nonlinear and unbalanced loads. The Z-source inverter is able to provide higher ac voltage related to the dc-link voltage than in conventional VSI, possessing embedded property of the boost converter. Control of the equivalent dc boost stage and dc-link capacitors voltage is presented. The resonant regulators are used for selective harmonic cancelation of the output ac voltage. This work also presents optimal control of boost factor and dc-capacitor voltage, reducing the voltage transistor stress under the desired ac voltage level. Experiment implementation on TMS320F2812 DSP show possibility of accommodating blanking time DSP circuits for controlling shoot-through duty ratio without any additional external control logic. Modified space vector modulation gives only two transistor switching per cycle, thus minimizing the switching losses to minimum.

8.1. Introduction

Z-source voltage-type inverter (ZSI) has been proven experimentally and in the literature as an attractive single-stage solution for buck-boost, three-phase dc-ac power conversion [pen1],[pen2]. The general layout is shown in Figure 8.1.

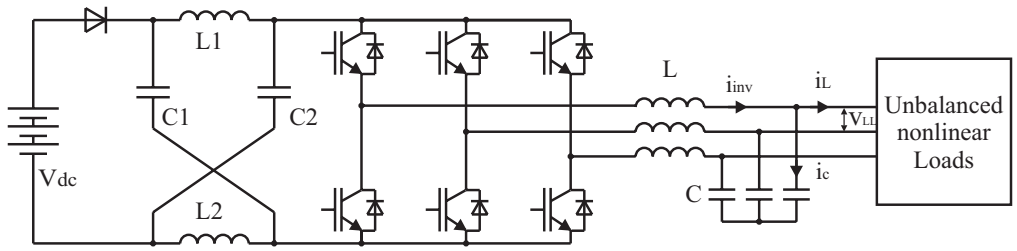

Figure 8.1 Three-phase Z-source inverter.

The Z-source inverter (ZSI) provides special features which can't be found in the traditional VSI inverter.

- The ZSI is a boost converter for dc-ac power conversion and higher peak to peak ac output voltage can be obtained than the available input voltage.
- A short circuit across any phase legs in the dc-link is allowed, the dead time is not necessary. The cross conductive short circuit is called shoot through (ST) state and is similar to those in Current Source Inverter.

- Shorting of any phase legs provide a voltage boost capability thus must be carefully controlled (similar to step-up converter).

The proposed ac voltage control scheme is suited for ZSI with an LC output filter. It use resonant regulators (8.1) and is suited for UPS or standalone power generation where sine wave output voltage is to be maintained. The proposed controller is able to compensate voltage distortion from unbalanced and nonlinear loads, thus controlling negative and positive voltage sequence and its harmonics. For control purpose only two phase to phase output voltages are measured. Since there are two dc-capacitors with similar voltage, a measurement of one pseudo dc-link voltage must be provided.

8.2. AC voltage control

Filter capacitor current control is used for selective harmonic voltage rejection. As an alternative to sensing the capacitor current a sensor-less scheme is used based on derivative of output capacitor voltage. The proposed control topology is depicted in Figure 8.2.

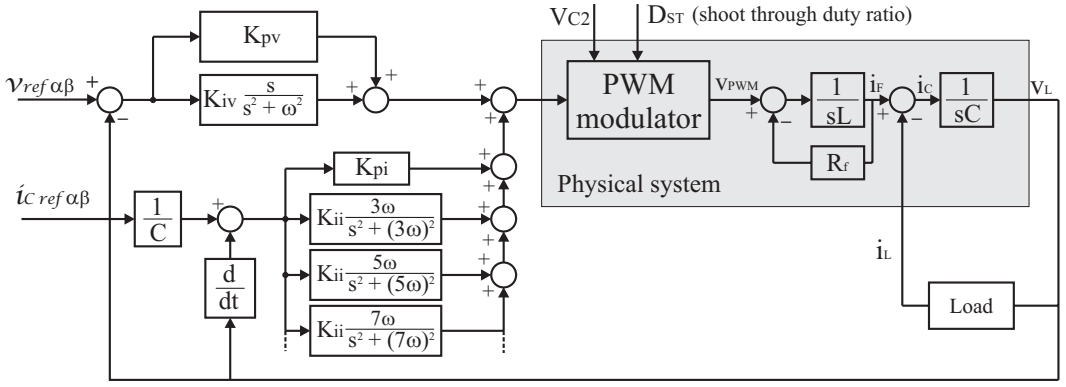

Figure 8.2 ZSI voltage harmonic control scheme

The derivative of filter capacitor current introduces noise and additional delay. It is found that the resonant controller handle this type of signal well because its characteristics is very narrow, providing gain only for given frequency. The delay associated with modulator and discrete derivative can be compensated by adjusting the leading γ angle of resonant controller (8.1) for given harmonic. The leading angle can change phase relation between input and output which can be adjusted due the fact that (8.1) is composed of two orthogonal components.

$$H_{ac}(s) = K_i \frac{s \cdot \cos(\gamma) - \omega \cdot \sin(\gamma)}{s^2 + \omega^2} \tag{8.1}$$

The details of harmonic control are the same as in 7.1.3.

8.3. Modulator with shoot-through states

The ZSI uses modified modulation strategy that insert shoot-through states into standard space vector modulation [mal5]. These shoot-through states boost the dc-link capacitor voltages and can be placed instead of the zero states without altering the normalized volt-sec. average voltage. The duration of each active state in a switching cycle is the same as in traditional SVM, therefore, the output waveform is fully controllable. The generation of switching signals based on standard SVM is shown in Figure 8.3.

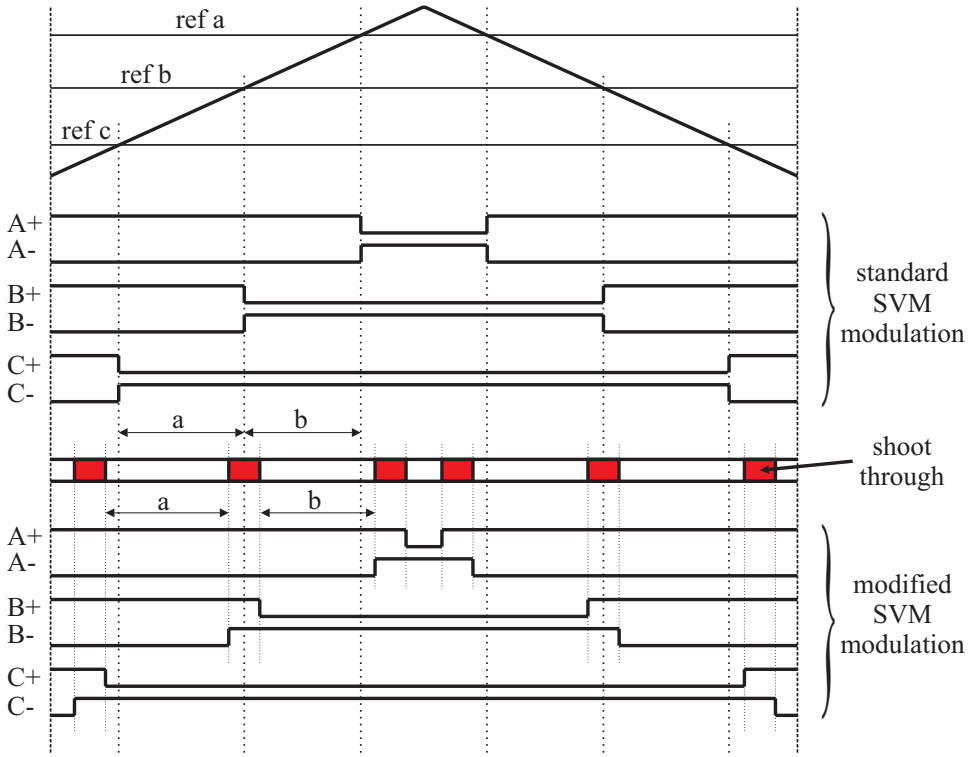

Figure 8.3: Generation of switching signals for ZSI, with shoot-through states (red)

The total time of the shoot-through (ST) state over one switching period is $2T_{ST}$, the modulation is symmetrical. The first shoot-through interval $T_{ST}/3$ is inserted between two active states of standard SVM. This can be seen as a common point between *a* and *b* arrows in Figure 8.3. The neighbor's active states are left and right shifted accordingly by $T_{ST}/6$ with their time intervals kept constant. The remaining two most left and most right shoot-through states with interval of $T_{ST}/3$ are lastly inserted within the zero intervals at the beginning and end of the active states. This way of generating inverter

switching states also ensures that a single device switches twice (on and off) per PWM switching period. The use of shoot-through states does not add additional switching compared to standard SVM.
The reference signals of the inverter legs for upper and lower transistors are shown on Figure 8.4. An important implementation detail is that during the saturation (usually transients), the highest priority is given to the shoot-through states (Figure 8.4b), so the active states are saturated first. This allow boost up the voltage in the dc-link first and then the modulation index can return to no saturated level.

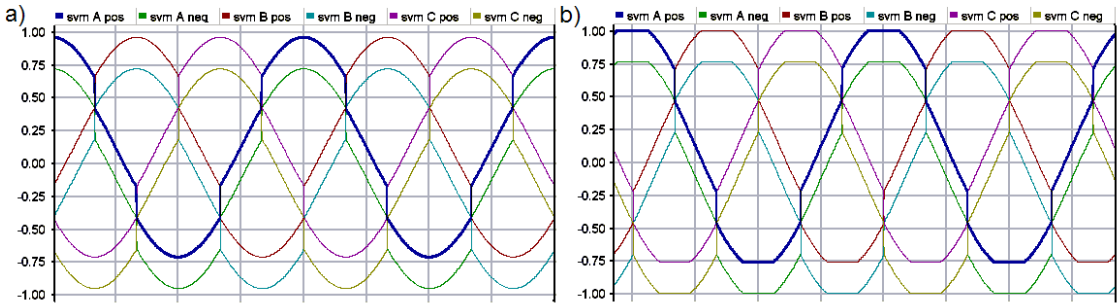

Figure 8.4: Reference signal for modulator, a) normal operation, b) saturated (transients).

8.3.1. Selection of boost inductor inductance

For the simulation and the experiment the switching frequency is set to 10 *kHz*. The shoot-through zero state occurs two times in one phase per switching period. The shoot-through state seen by the dc-link from all three phases occurs 6 times per PWM period. The equivalent switching frequency seen from the Z-source network is 60 *kHz*.

In the experiment the selection of the boost inductance is based on ripple current and maximum transistor current. Since the transistor peak current is 60 A, the converter rated current is defined as 10 A, the rest is reserved for the current ripple. Unfortunately in this DSP the shoot-through state interval is limited to the value which was originally designed and intended as a dead time generation. The maximum shoot-through time is limited to 3 μs. Six shoot-through states in 100 μs switching period results in maximum achievable equivalent boost duty ratio of 18 %.
A relatively short duration of ST state requires small value of the inductance. With this specific hardware it was convenient to have high current ripple (fully utilizing the transistors), but this is not a usual case.
Assumed maximum capacitor voltage of 400 V, maximum ripple current of 40 A, and shoot-through time of 3 μs. The inductance can be calculated as:

$$L = \frac{T_{ST} V_{DC}}{\Delta I} = 30 \mu H \tag{8.2}$$

8.4. Virtual Dc-link voltage controller

The average voltage of pseudo dc-link across the inverter bridge is identical to the capacitor voltage because the average of an inductor voltage is zero. The capacitor voltage on C_1 and C_2 is dependent on the shoot-through time, and it can be stepped up

by adjusting shoot-through time. Reducing the transistor voltage stress under a desired load is important, it should ensure that there is no high boost ratio and simultaneously the modulation index is not fully utilized (and the dc voltage as well). As has been analyzed in [pen1] the voltage gain (boost) is defined as:

$$B = \left(1 - 2T_{ST}/T_{sw}\right)^{-1} \tag{8.3}$$

where $B \geq 1$. The T_{ST} represents half of the shoot-through time during the inverter switching period, and T_{sw} represents the inverter switching period. The ac output voltage relation is:

$$\hat{V}_{phase} = M \cdot B \cdot V_{DC}/2 \tag{8.4}$$

where M is the modulation index. Therefore, to minimize the voltage stress for any given voltage gain, we have to maximize the modulation index M by using as much of the available Dc-link voltage and leaving enough time for the ST state. Defining the shoot-through duty ratio as:

$$D_{ST} = T_{ST}/T_{sw} \tag{8.5}$$

During operation the inverter saturation can be described as $M + D_{ST} \leq 1$. In case of using the boost property, minimum voltage switch stress appears when $M + D_{ST} = 1$.
A discrete-time PI voltage controller based on trapezoidal method of approximation is used to regulate the average voltage V_{C2} of the dc-link, the controller is shown in Figure 8.5. It is important to include the wind-up protection, thus limiting the maximum shoot-through duty ratio.

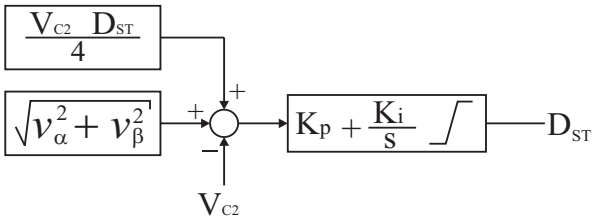

Figure 8.5: Optimal dc-link voltage controller

The aim of this controller is to keep the maximum modulation index as close to unity as possible. The v_α and v_β are the controller reference output voltage, where the modulus is calculated (Figure 8.5). The other feed-forward term is a calculation of the equivalent dc voltage which would be not available for active vectors (consumed by ST):

$$V_{ST} = V_{C2} D_{ST} / 4 \tag{8.6}$$

It is important to add this term, as the D_{ST} is increasing (consuming equivalent time of zero vectors) there is less available time for the active vectors.

8.5. Simulation results

The simulation is performed under PSCAD software package. The dc source voltage is 400 *V*. The reference ac voltage is set 230 *V* rms. The phase to phase voltage waveform is visible in Figure 8.6 top and the phase current in the bottom. As a nonlinear load the rectifier with dc capacitor and resistor is used.

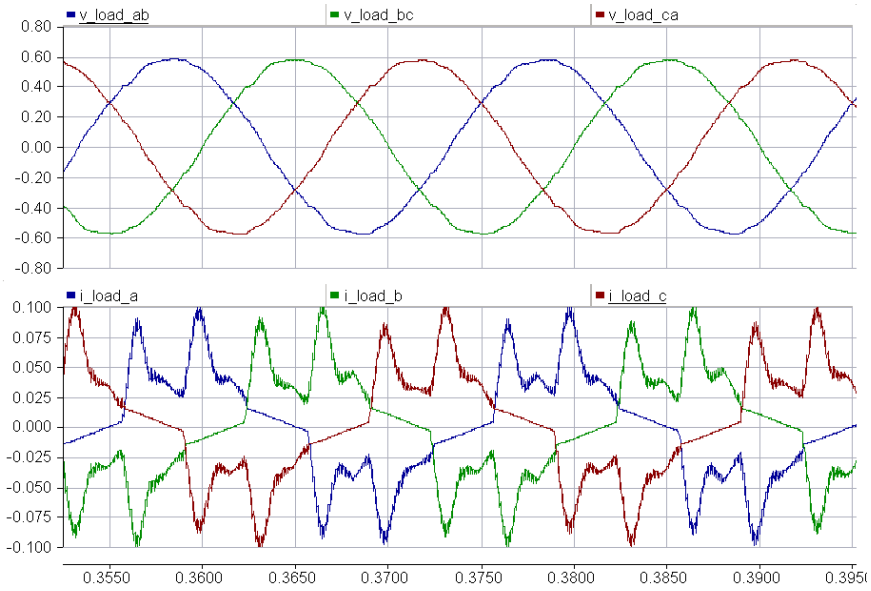

Figure 8.6: top: inverter output voltage, bottom: load current of rectifier load

In order to achieve a low distortion sinusoidal output voltage under nonlinear load the controller has to create a modulation signal which is shown in Figure 8.7

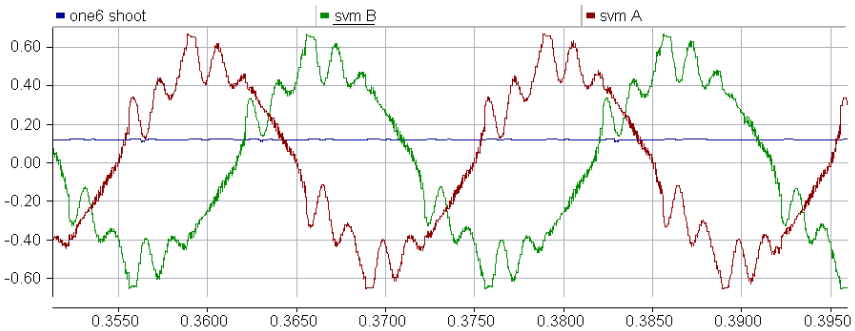

Figure 8.7: Duty ratio of modulation signal when voltage harmonic control is enabled

Figure 8.7 shows only the modulation in phases *a* and *b*, phase *c* is similar. The visible ripples are cancelling the influence of the nonlinear load current on an output filter. In other words, they compensate the voltage drop over filter inductance. The blue line shows the $1/3$ of the shoot-through time, so this is explaining why the modulation index at the peaks is not reaching unity. Summation gives $0.65+3\cdot 0.11=0.98$ which maximally utilizes the dc-link voltage and causes minimum stress in the switches.

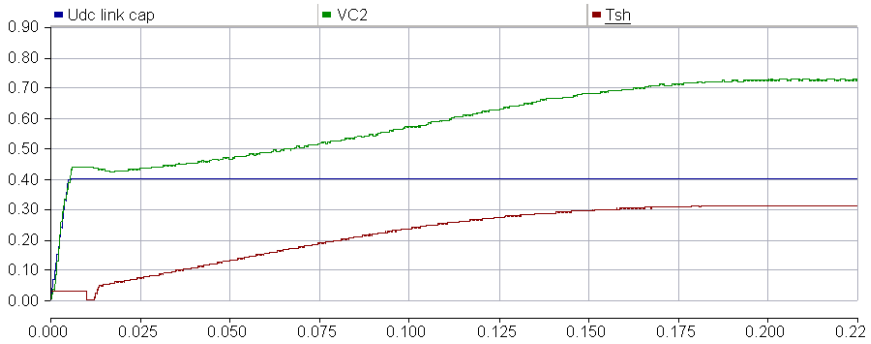

Figure 8.8: Response of the optimal dc-link controller

In Figure 8.8 the start-up response of the dc-link boost controller is shown. Red line represents the shoot-through state duration, blue the supply voltage and green represents the voltage in capacitors of Z network.

The problem can arise when a nonlinear current with high crest factor is drawn (>2). This leads to high spikes in the reference voltage calculated by the set of resonant controllers. The spikes "consume" the dc-link voltage, thus leading to even higher boost factor. The problem in the real implementation was solved by inserting a peak detector and large time constant low-pass filter. The insertion took place in Figure 8.5 between the instantaneous reference v_α and v_β module calculation and the summation block.

8.6. Experimental results for ZSI

Since the standard VSI converter cannot be used due to significant changes in dc-link layout and gate signal interlocking, the $3\,kW$ prototype of Z-source inverter was designed and built. The transistors which are used, have a peak current of $60\,A$, and voltage class of $1200\,V$. The gate driver is based on monolithic, opto-isolated integrated circuit HCPL 316J which requires small galvanic power supply for each transistor. The power board with control card is shown in Figure 8.9. The schematic is in Appendix A.

Over-voltage dc-link protection is also designed, since it easy to boost voltage to a dangerous level for dc-link capacitors and transistors. In case of overvoltage, the protection works in two level modes, first the chopper transistor is turned on damping the energy to a resistor, if the voltage is still increase the pulses from gate drivers are disabled. The schematic of the over-voltage protection is in Appendix A.

Figure 8.9: Photograph of the laboratory setup of Z-source inverter

The gate PWM signals from the DSP card are directly connected to the gate drivers enabling shoot-through. There is no hardware interlocking protection for the upper and lower transistors.
The control DSP is a TMS320F2812 which has all necessary circuits, like A/D converter, PWM generator and embedded hardwire to control dead time. The PWM outputs also can be set to be active high or low. Exploiting those features enables direct DSP control of duty ratio and shoot-through factor. The dead time unit acts as a shoot-through time generator and is adaptively changed during operation. A limitation in DSP is that the shoot-through can be only 3 μs for a given PWM resolution, and there are always six shoot-throughs per switching period, giving a total maximum time of 18 μs. For 100 μs switching period and PWM resolution of 6,66 *ns* running on 150 *MHz* core frequency the step up duty ratio is limited to 18 %. By lowering the PWM resolution the boost factor can be further increased.

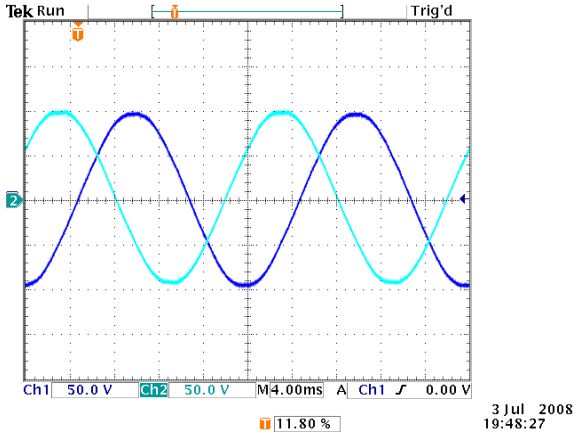

Figure 8.10: Sinusoidal output voltage with harmonic cancellation enabled and no load

In figures below there is a comparison of the voltage waveform by enabling or disabling the voltage harmonic cancellation algorithm.

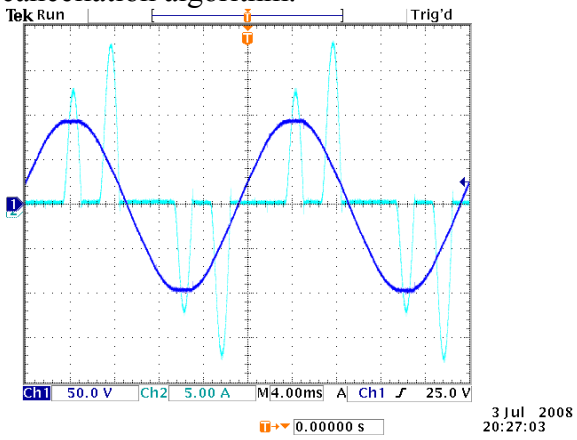

Figure 8.11: Voltage and current under rectifier type of load when harmonic cancelation is enabled

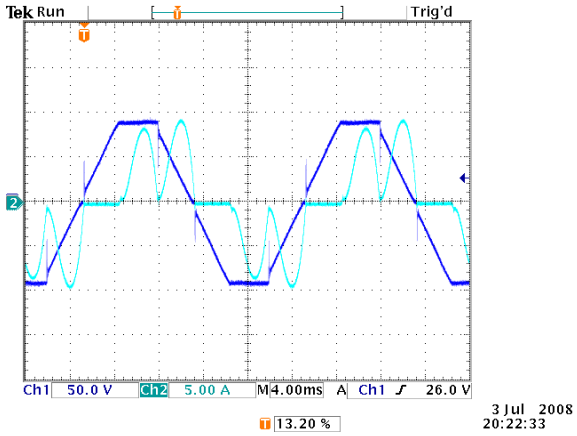

Figure 8.12: Voltage and current under rectifier type of load when harmonic cancelation is disabled

In the Figure 8.12 only the base harmonic is controlled. By enabling the harmonics control and wait the transition time of around 10 grid cycles the voltage is restored, and shown in Figure 8.11. With larger nonlinear currents the distortion is more significant.

Table 8.1: Data of the converter and load for above experiment

boost inductance	2 *x* 33 μH
dc-link capacitor	2 *x* 2200 μF
dc input supply voltage	80 *V*
referenced ac output phase voltage	71 *V*
output filter inductance	3 *x* 750 μH
output filter capacitance, star connected	3 *x* 47 μF
load capacitor	4700 μF, 200 *V*
load resistance	25 Ω, 1 *kW*

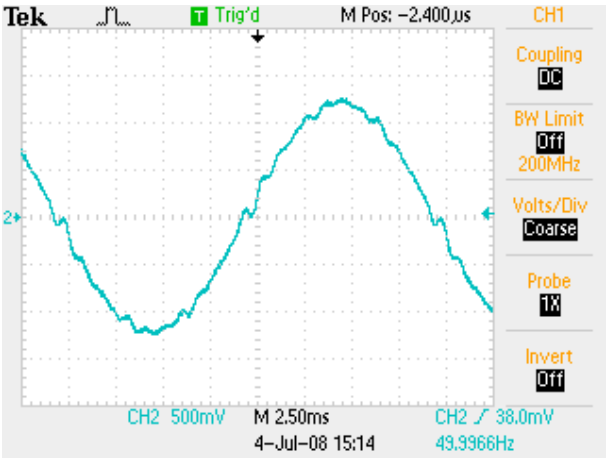

Figure 8.13: Maximum inverter output voltage where no load is applied, the boost ratio is 300 %, the voltage harmonic cancellation is disabled. The reference output voltage is set to 240 V peak, the source is 80 V

With very high boost ratio (the dc-link voltage three times higher than available supply voltage) the effect of inverter harmonics influencing the output voltage is visible in Figure 8.13. The output voltage is distorted due to harmonics coming from the shoot-through state and other second order effects. Enabling the voltage harmonic cancellation did not cause significant improvements in the wave shape. The reference output voltage set to 240 *V* causes that the ST time fluctuates at it maximum even without the load. Connection of any load would cause immediate drop of the ac voltage, as the dc-capacitors discharge.

Experiments show that operation of the Z-source inverter with high boost ratio is inefficient. The voltage harmonic cancellation algorithm can be enabled, significantly improving the voltage shape. The limitation lies in the inverter limited dc voltage and output filter saturation. The current capacity can be improved by increasing the shoot-

through time, but increasing the shoot-through time is not feasible since the maximum transistor current can be cross.

8.7. Chapter summary

This Chapter presented a Z-source inverter for implementing a UPS or stand alone power generation system. It can boost the input voltage by a practical factor of up to 1.5, not worsening the efficiency, reducing cost and component count. The voltage and current transistor class for the Z-source inverter must be higher compared to VSI of the same rated power. For the high boost ratios the efficiency compared to standard VSI with separate boost stage is lower. The boost property can be vital where the input voltage is not changing in a wide range. An example is the battery based UPS where it would be possible to extract more energy from a near drained battery. It can be used in low power, variable speed diesel systems where the variable speed generator technology would be used to save fuel.

The disadvantage is that many components of the ZSI are under high *dV/dt* which could lead to EMI problems and difficult design. The component second order effect is also significant and leads to problem to achieve high efficiency in wide boost ratio.

9. SUMMARY AND FUTURE WORK

9.1. Conclusion

The motivation of this study was to get practical and theoretical knowledge about grid connected converters and control for renewable sources. The thesis is oriented to the sensor-less operation of grid connected converters under unbalanced voltage. The discussion is not only limited to it, also other aspect are described. In general it is possible to distinguish in the thesis between two kinds of control strategies, for current control (Chapter 4-6) and voltage control (Chapter 7-8). Those will fit to the grid connected system synchronized with the grid and stand alone power generation. The current control is used when DG or renewable source is connected and synchronized to the power system. The voltage control can be easily used by one inverter in island operation. Paralleling of stand alone inverters is more challenging because require droop control as a means of inverter communication.
The voltage control together with droop control can form micro-grids and can be operated in the remote areas being supplied from renewably source. Such a hybrid system however requires some sort of storage energy any few independent renewable sources.

Presented in Chapter 4 the dual frame virtual flux concept can operate in unbalanced voltage conditions without using the voltage sensors. The positive and negative frame current control enables cancelation of 100 Hz ripples appearing from the negative sequence. The method is design to operate under heavily unbalanced conditions and thus is very robust. The advantage of having two independent frames is that the d- and q-axis current reference of each sequence can be controlled independently. This enables realization of many various functions.
In general two basic functions can be easily realized; the converters source/supply sinusoidal currents or the power delivered to the dc-link is not pulsating, both in unbalanced grid condition.
The possibility of realizing constant power under unbalanced grid is very beneficial for the lifetime of the dc-link capacitor. A converter which was designed for symmetrical operation and especially the dc capacitor might prematurely fail under unbalanced conditions which were not predicted during the design stage.

The second mode, supplying/sourcing symmetric current during unbalanced voltage has also many applications. One example is an active rectifier when the grid has current restrictions and the current amplitude should be controlled. This functionality however does not provide constant power and in the case of large voltage imbalance the circuit becomes more similar to single-phase. Those two methods are presented in this thesis.

Another application of the DVF concept can be utilized during unsymmetrical faults. By providing the proper current reference, it would be possible to provide low voltage ride through capability (LVRT) during grid transients. For a symmetrical system, the injection of reactive power to support the voltage does not show difficulties. The injection of reactive power into unbalanced voltages during grid transients is much more challenging, because pulsating active/reactive power must be provided rapidly. The DVF is able to control the currents during grid transients and ensures that they not exceeding converter ratings. The LVRT is a recent standard in the wind turbine industry which prevents the disconnection of the turbine from the power system in a case of a short circuit in the grid. In that case the wind turbine should stay connected and supports the grid by continuing injecting the current. The specifications are described in grid codes which are dependent on the country. The main idea is to avoid large loss of power generation after transient disturbances in the grid.

In Chapter 5 an instantaneous synchronization method under unbalanced voltage is presented. The method shows that the voltage sensors can be removed from the system and the converter is still able to synchronize to the grid using only the available current sensors. The start-up procedure is strongly related to the virtual flux sensor-less current control. Two ways of synchronization are shown.
The first kind, perform twice mini-short circuit on the grid and measures the current. This is called “sampling” and is executed twice in order to estimate the position of the voltage vector angle and amplitude. This information can also lead to more information about the state of the grid (no power in the grid, unbalance, etc). When the position is known, the inverter waits until voltage zero angle is approaching and then start the operation with initialized control structure for the zero angle. The flux and other integral variables must be initialized because they guarantee the small synchronization current. The initialization provides a match between the control state and the existing grid state.
The second presented kind of grid instantaneous synchronization is performed without previous knowledge of the grid state, the reference variables are initialized to zero. In this case, grid sampling is not needed. The modulator reference voltage is set initially to 0 which results in 50 % duty ratio in all converter bridges. The 50 % duty ratio initially results in large inrush currents which act as a step-up converter boosting the dc-capacitor voltage. When the control variables settles down the dc-link controller is enables and the dc voltage approaches the reference value. It is also possible to synchronize to the unbalanced grid; in this case a dual flux model is used. Experiment verified the possibility of instantaneous synchronization to the unbalanced grid.

In Chapter 6 the grid inductance algorithm was presented. For a distributed generation the knowledge of grid parameters is very important to ensure stable operation. The algorithm does not require any hardware changes in the inverter, all features are implemented in the software. This algorithm is able to estimate the impedance when an LCL filter capacitor is used. In the laboratory setup an accuracy of 5% is achieved when the grid inductance is significantly higher than the filter inductance (weak grid). Exact

estimation of the stiff grid is difficult; however our interest mainly is to ensure that the grid is not weak. Stability and dynamic performance of the controller is significantly improved.
This algorithm has a large potential to further development. The analytical expression of the overall system could be derived in the future for direct estimation. This is however not a trivial task, the model must include: current controller, virtual flux and dc-link dynamics with many nonlinearities. If the analytical expression would exist, perhaps it would be possible to identify the inductance based on current response of single reactive power injection and knowledge of the LCL filter parameters.
In Chapter 7 and Chapter 8 a voltage control strategy is presented. The same control strategy is applied on two different topologies.

The first topology in Chapter 7 is the voltage source inverter. The control aim is to ensure sinusoidal output voltage in spite of the unbalanced and nonlinear load. In those standalone applications usually the load is not known so the voltage drop on the filter inductance caused by the unknown current must be compensated. In order to compensate for the voltage drop by the unknown current, a compensating voltage must be applied, 90 degrees before the unknown current main distortion harmonic occurs.

The only solution is to construct a controller in a frequency domain where each individual harmonics advances the output by 90 degrees. This can be solved in many ways. The greatest support is delivered by pair of resonant controllers which provide orthogonal output. The estimated filter capacitor current is used at input of resonant controller. The inverter platform does not have a current measurement. The resonant controller can successfully replace the synchronous *dq* PI based method and make the realization on an average DSP possible. The resonant controller frequency can be tuned on-line to follow the frequency changes required in various droop methods for power sharing. The experimental results show that the proposed controller has high performance behavior for any kind of load including non-linear unbalanced loads.

In Chapter 8 a Z-source inverter for a UPS or stand alone power generation system is presented. The natural property of this topology is that it can provide higher ac output voltage related to the dc-link voltage than in traditional VSI. It can boost the input voltage by a practical factor of up to 1.5, not worsening the efficiency, reducing cost and component count. The boost property can be vital where the input voltage is not changing in a wide range and thus gaining on efficiency. An example is the battery based UPS where it would be possible to extract more energy from a near drained battery. It can be used in low power, variable speed diesel generator systems where the variable speed technology would be used to save fuel.

The disadvantage of ZSI is that many components are under high *dV/dt* which could lead to EMI problems and difficult design. The component second order effect is also significant and leads to efficiency problem when high boost ratio is required.
Unfortunately the voltage and current transistor class for a Z-source inverter must be higher compared to a VSI of the same rated power. For the high boost ratios the efficiency compared to standard VSI with separate boost stage is lower.

All Chapters consequently presents solutions for robust and fail proof control of energy from distribution power generation. The distributed generation with large utilization of power electronics actually could support the grid, but a proper standards and procedures must exist on higher system level. The higher system level in large extent means the communication between the units, but also a defined behavior in given situations when the communication is lost.
A good example is the reactive power compensation. With a large penetration of power electronics, the reactive power compensation can easily be made possible from the converter point of view. The problem is on the selection of criterion for doing so.

9.2. Scope of future work

The quality of components is improving; and so should the embedded control algorithms do. Large progress in silicon development and computational power of DSP's and FPGA's is made every year. This new technology enables to uses more advanced algorithms.

The same happens with power silicon, namely the IGBT transistors. With the spread of renewable generation, cheap converters within a MW range are needed. The two-level and three-level converter topology are the most common today. By using more levels, the filter size could be reduced. As the transistor cost is going down it would be beneficial to research topologies which would enable better efficiency and enable smaller filter size. In some applications like PV it is worth to invest in improving the overall efficiency as it will pay back during operation. The potential solution could be in resonant topologies with zero voltage, zero current switching. That would enable higher switching frequency and the filter size can be reduced. Multilevel topologies are also interesting for further exploration. They enable filter size reduction and moreover reduction of common mode voltage output components. Reduced common voltage components enable connection of the inverter directly to the grid without isolation transformer. In case of PV system the inverter size and efficiency is significantly improved.

It can be observed today that the power electronics and control is not the missing element in the development of distribution system. The problem might be the managements of such a large number of generations, balancing the production and needs. From many studies, the conclusion is that with more renewable energy, more storage is needed to cover the peak energy usage. Those two systems can live together, linked by power electronics.

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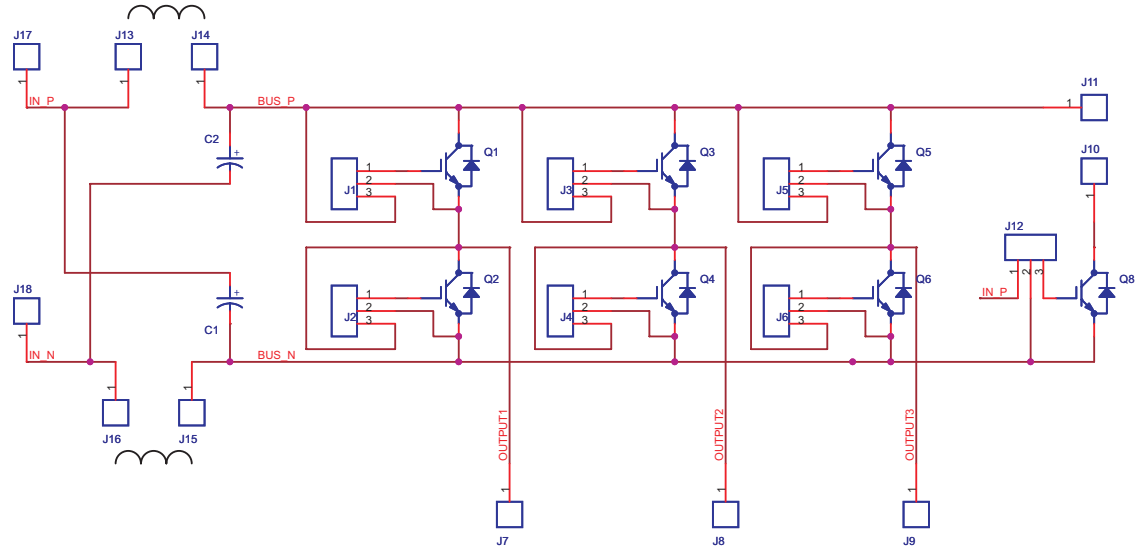
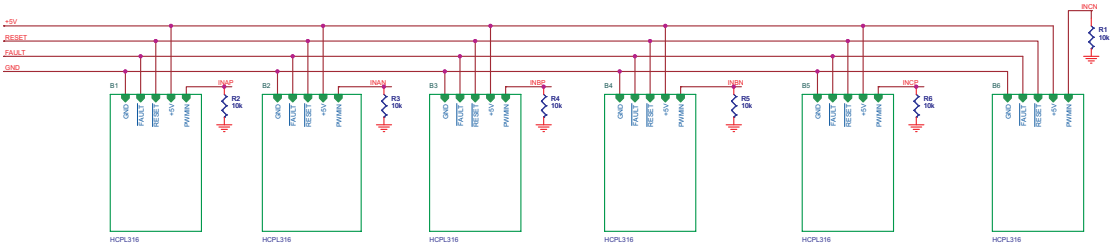
Internet resources

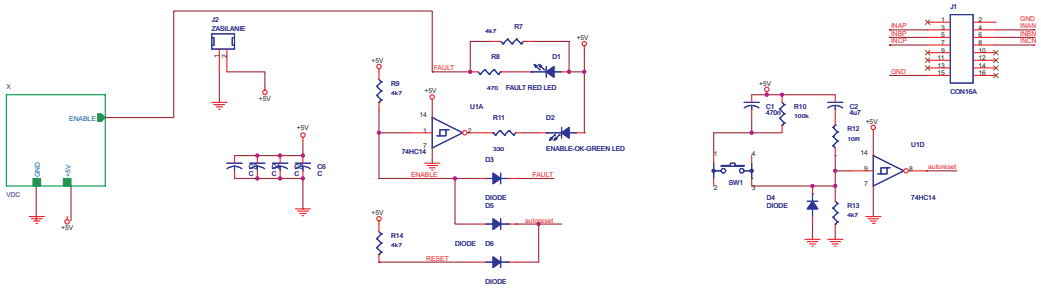
www.ti.com Texas Instrument homepage, large resource on DSP's.

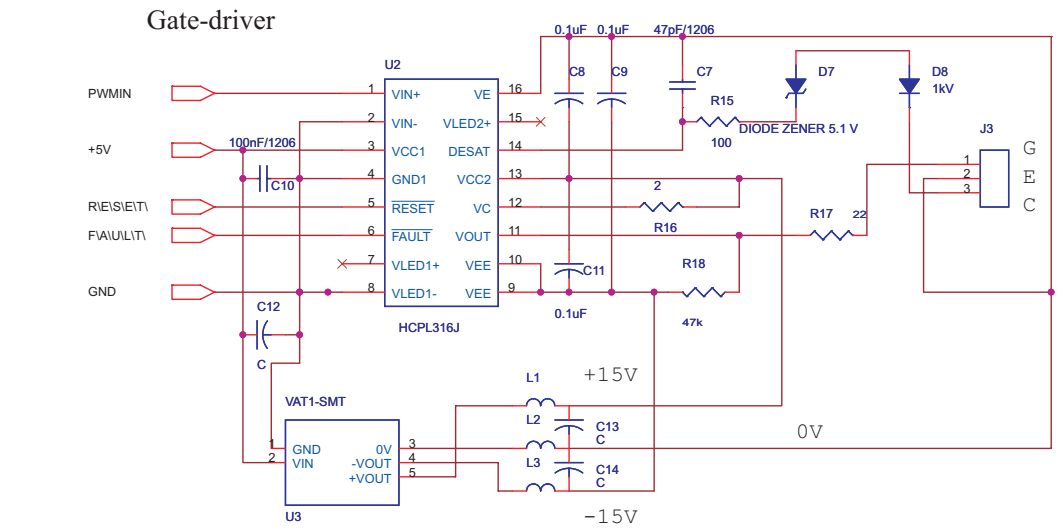
Appendix A: Z-inverter schematics

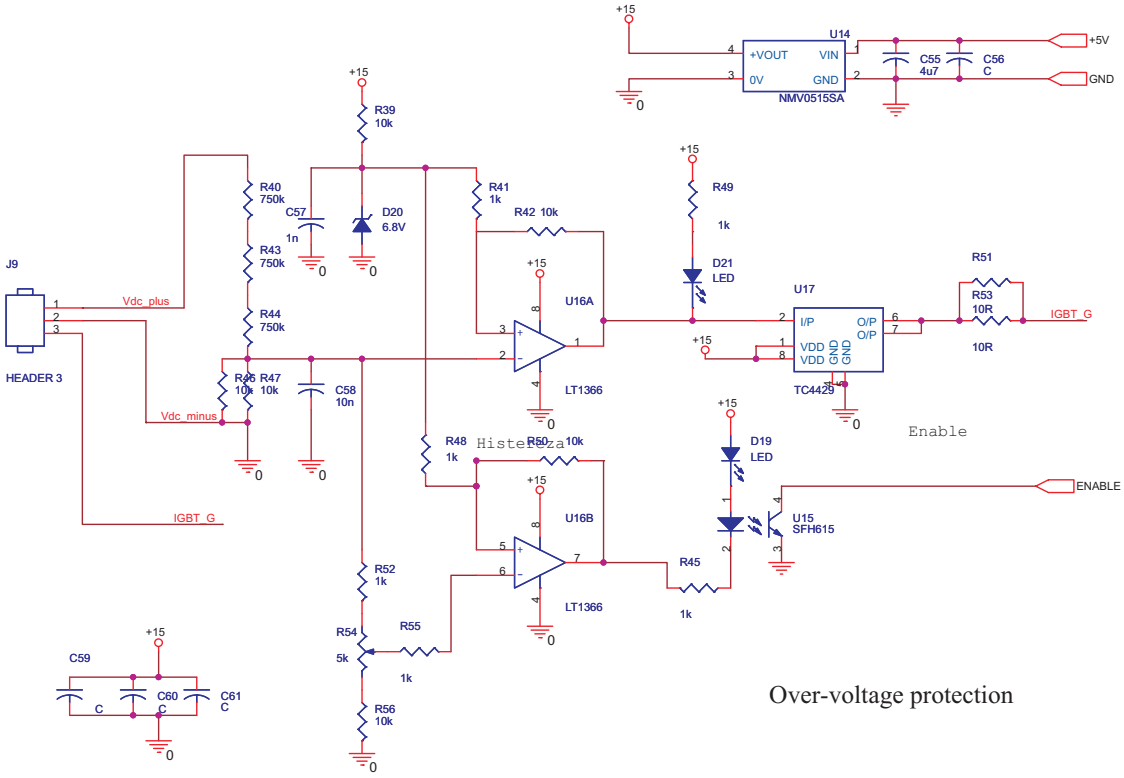
The schematic of the constructed Z-source inverter: power board, system level, gate driver and overvoltage protection circuit.








Gate-driver
PWMIN
+5V
R\E\S\E\T\
F\A\U\L\T\
GND
100nF/1206
C10
C12
C
U2
VIN+
VIN-
VCC1
GND1
RESET
FAULT
VLED1+
VLED1-
VE
VLED2+
DESAT
VCC2
VC
VOUT
VEE
VEE
HCPL316J
0.1uF
0.1uF
47pF/1206
C8
C9
C7
R15
100
DIODE ZENER 5.1 V
D7
D8
1kV
J3
G
E
C
R17
22
R16
2
R18
47k
C11
0.1uF
L1
+15V
L2
L3
C13
C
C14
C
0V
-15V
VAT1-SMT
GND
VIN
0V
-VOUT
+VOUT
U3


+15
U14
+VOUT
VIN
0V
GND
NMV0515SA
C55
4u7
C56
C
+5V
GND
R39
10k
R40
750k
R43
750k
R44
750k
C57
1n
D20
6.8V
R41
1k
R42
10k
J9
HEADER 3
Vdc_plus
Vdc_minus
R46
10k
R47
10k
C58
10n
U16A
LT1366
R49
1k
D21
LED
U17
I/P
O/P
O/P
VDD
VDD
GND
GND
TC4429
R51
R53
10R
10R
IGBT_G
Enable
R48
1k
Histereza
R50
10k
U16B
LT1366
D19
LED
U15
SFH615
ENABLE
R45
1k
R52
1k
R54
5k
R55
1k
R56
10k
C59
C
C60
C
C61
C
Over-voltage protection

Appendix B: Per unit system

The *per unit* (*p.u.*) or *normalized* notation is very useful in designing and comparing different control systems or models. There are several benefits, e.g. software designed in *p.u.* notation ensures easy scalability for different range of voltages or currents. Very often in power electronics we deal with kilowatts and micro henries, the spread is large. When expressed in *p.u.* notation the range becomes 0 to 1. This is especially important for fixed point DSP arithmetic implementation where limited range of numbers is available.

The corresponding normalized quantity will be denoted by subscript "pu" and in general it is:

$$x_{pu} = \frac{x}{x_{base}}$$

Below there is a definition of the following base values:

Phase voltage: $V_{base} = \frac{\sqrt{2}}{\sqrt{3}} V_{LL}$, where V_{LL} is the rms line to line voltage

Phase current: $I_{base} = \sqrt{2} I_n$, where I_n is the nominal phase rms current

Power: $S_{base} = \frac{3}{2} V_{base} I_{base}$

Impedance: $Z_{base} = \frac{V_{base}}{I_{base}}$

Angular frequency: $\omega_{base} = 2\pi f$

Inductance: $L_{base} = \frac{V_{base}}{\omega_{base} I_{base}}$

Capacitance: $C_{base} = \frac{I_{base}}{\omega_{base} V_{base}}$

Flux: $\psi_{base} = \frac{V_{base}}{\omega_{base}}$

Appendix C: Power components in unbalanced system

Each of the symmetrical sequence components represents the symmetrical system. The components from positive and negative sequence cause the second harmonic pulsating power. The power components can be written as:

$$p(t)^{pp} = v_a^p i_a^p + v_b^p i_b^p + v_c^p i_c^p \quad = 3\left|V^p\right|\left|I^p\right|\cos(\varphi_v^p - \varphi_i^p)$$

$$p(t)^{pn} = v_a^p i_a^n + v_b^p i_b^n + v_c^p i_c^n \quad = 3\left|V^p\right|\left|I^n\right|\cos(2\omega t + \varphi_v^p + \varphi_i^n)$$

$$p(t)^{np} = v_a^n i_a^p + v_b^n i_b^p + v_c^n i_c^p \quad = 3\left|V^n\right|\left|I^p\right|\cos(2\omega t + \varphi_v^n + \varphi_i^p)$$

$$p(t)^{nn} = v_a^n i_a^n + v_b^n i_b^n + v_c^n i_c^n \quad = 3\left|V^n\right|\left|I^n\right|\cos(\varphi_v^n - \varphi_i^n)$$

$$p(t)^{n0} = v_a^n i_a^0 + v_b^n i_b^0 + v_c^n i_c^0 = 0$$

$$p(t)^{0p} = v_a^0 i_a^n + v_b^0 i_b^n + v_c^0 i_c^n = 0$$

$$p(t)^{00} = v_a^0 i_a^0 + v_b^0 i_b^0 + v_c^0 i_c^0 = 3\left|V^0\right|\left|I^0\right|\left(\cos(\varphi_v^0 - \varphi_i^0) + \cos(2\omega t + \varphi_v^0 - \varphi_i^0)\right)$$

$$\begin{aligned} p(t) &= v_a i_a + v_b i_b + v_c i_c \\ &= (i_a^p + i_a^n + i_a^0)(v_a^p + v_a^n + v_a^0) \\ &+ (i_b^p + i_b^n + i_b^0)(v_b^p + v_b^n + v_b^0) \\ &+ (i_c^p + i_c^n + i_c^0)(v_c^p + v_c^n + v_c^0) \end{aligned}$$

The equations having the term $\cos(2\omega t + x)$ will cause a second harmonic power ripple; the remaining terms will cause constant power flow.